Application Acceleration with High Level Synthesis

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Lab B – FFT

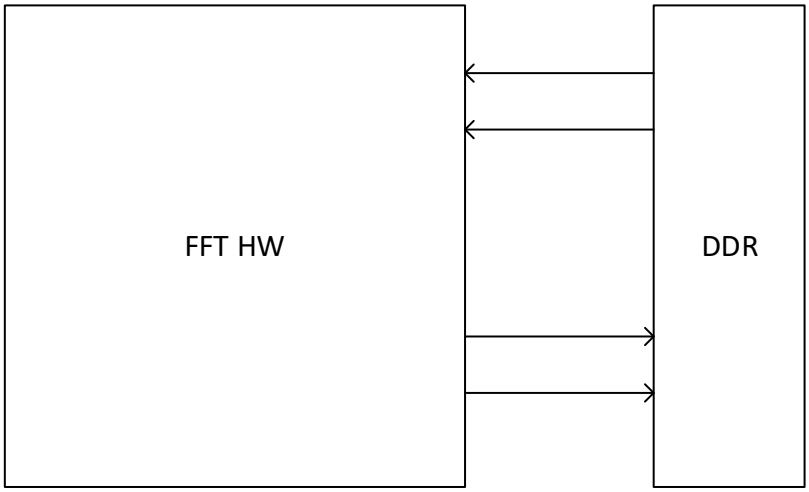

Fig. 1.

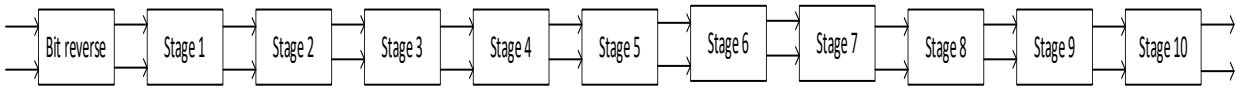

Fig. 2.

Overall block diagram is shown in Fig. 1, Two inputs to the FFT accelerator coming from the main memory, the size of the array inputs are 1024, there are also 2 output arrays with same size coming out from the hardware FFT to the main memory. As we are performing FFT of 1024 points, there are 10 stages plus the bit reverse stage, so 11 stages in total as shown in Fig. 2. Because we are using axi4 burst mode, we use memory copy(memcpy) to transfer data to/from DDR in order to have vitis infers the burst, this forces us to create 12 internal buffers(input/output between stages) where 2 of them are to store data coming from DDR and going to DDR. The rest 10 are inputs of the 10 stages, which will help the design to apply parallelism to reduce overhead between stages.

https://github.com/freud96/LabB_fft