

Introduction

在 Lab A 我是選 Chapter 7 Design Optimization，此章節是用 matrix multiplications 當作例子，透過不同的 directive 設定讓整體 performance 上升，在這個 Chapter 有兩個 lab，總共有 6 個 solutions 一步一步的優化整個電路。

Lab 1 Optimizing a Matrix Multiplier

● Experimental Steps

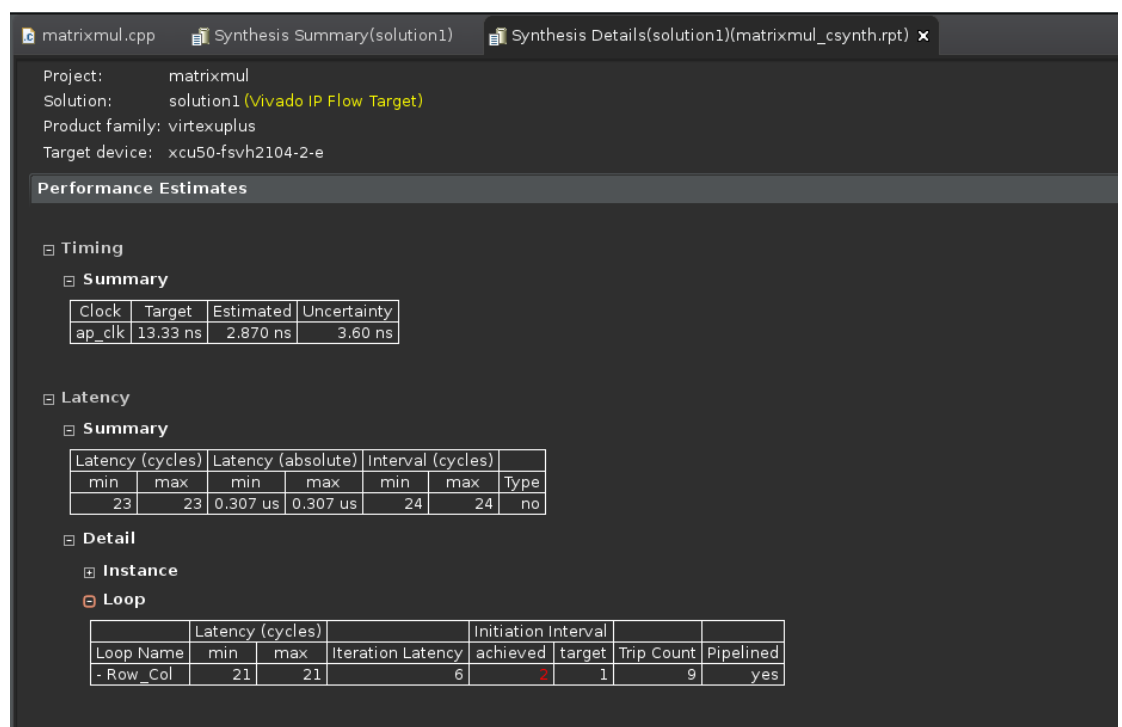
■ Step 1 Create and Open the Project

■ Step 2 Synthesize and Analyze the Design

一開始直接跑 synthesis 從 console 那邊得出他自動優化了哪些步驟，

```
INFO: [HLS 200-10] Checking synthesizability ...
INFO: [HLS 200-111] Finished Checking Synthesizability: CPU user time: 0.02 seconds, CPU system time: 0 seconds, Elapsed time: 0.04 seconds; current allocated memory: 462.598 MB.
INFO: [XFORM 203-510] Pipelining loop 'Col' (Design_Optimization/lab1/matrixmul.cpp:56) in function 'matrixmul' automatically.
INFO: [XFORM 203-502] Unrolling all sub-loops inside loop 'Col' (Design_Optimization/lab1/matrixmul.cpp:56) in function 'matrixmul' for pipelining.
INFO: [HLS 200-489] Unrolling loop 'Product' (Design_Optimization/lab1/matrixmul.cpp:59) in function 'matrixmul' completely with a factor of 3.
INFO: [HLS 200-111] Finished Loop, function and other optimizations: CPU user time: 0.03 seconds, CPU system time: 0.02 seconds, Elapsed time: 0.08 seconds; current allocated memory: 483.938 MB.
INFO: [XFORM 203-541] Flattening a loop nest 'Row' (Design_Optimization/lab1/matrixmul.cpp:54:17) in function 'matrixmul'.
INFO: [HLS 200-111] Finished Architecture Synthesis: CPU user time: 0.01 seconds, CPU system time: 0 seconds, Elapsed time: 0.01 seconds; current allocated memory: 483.938 MB.
INFO: [HLS 200-10] Starting hardware synthesis ...
INFO: [HLS 200-10] Synthesizing 'matrixmul' ...
INFO: [HLS 200-10] ...
```

並得到合成完的 report



The screenshot shows the Synthesis Summary report for a project named 'matrixmul'. The report is displayed in a dark-themed IDE window. The top section shows project details: Project: matrixmul, Solution: solution1 (Vivado IP Flow Target), Product family: virtexuplus, and Target device: xcu50-fsvh2104-2-e. Below this is the 'Performance Estimates' section, which is expanded to show 'Timing' details. The 'Timing' section is further expanded to show 'Summary' information, which includes a table of clock and latency estimates. The 'Latency' section is also expanded to show 'Summary' information, which includes a table of latency estimates. The 'Detail' section is expanded to show 'Loop' information, which includes a table of loop information.

Project: matrixmul
Solution: solution1 (Vivado IP Flow Target)
Product family: virtexuplus
Target device: xcu50-fsvh2104-2-e

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	13.33 ns	2.870 ns	3.60 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
23	23	0.307 us	0.307 us	24	24	no

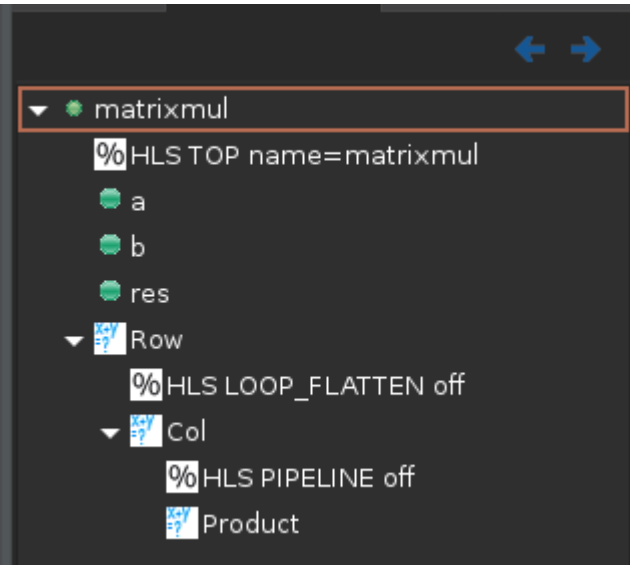
Detail

Instance

Loop

Loop Name	Latency (cycles)		Iteration Latency	Initiation Interval		Trip Count	Pipelined
	min	max		achieved	target		
- Row_Col	21	21	6	2	1	9	yes

於是我透過以下 directive 的設定盡量還原到沒有優化過的樣子，



而下圖是合成完的 report

matrixmul.cpp | Synthesis Summary(solution1) | Synthesis Details(solution1)(matrixmul_csynth.rpt) x

Product family: virtexuplus
Target device: xcu50-fsvh2104-2-e

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	13.33 ns	1.663 ns	3.60 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
160	160	2.133 us	2.133 us	161	161	no

Detail

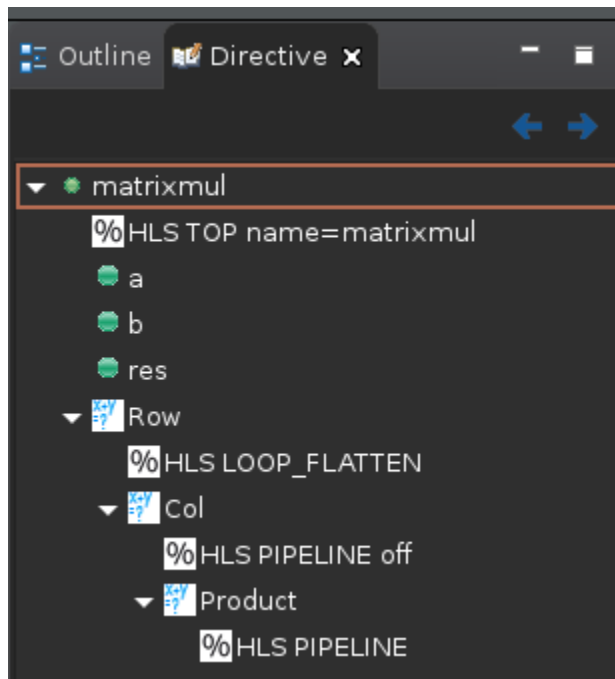
Instance

Loop

Loop Name	Latency (cycles)		Iteration Latency	Initiation Interval		Trip Count	Pipelined
	min	max		achieved	target		
- Row	159	159	53	-	-	3	no
+ Col	51	51	17	-	-	3	no
++ Product	15	15	5	-	-	3	no

■ Step 3 Pipeline the Product Loop

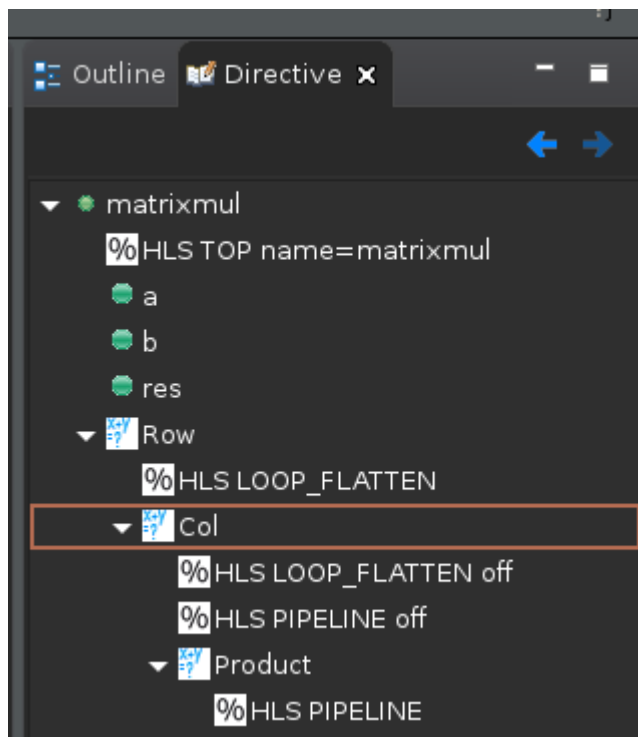
以下是 sol2 的 directive



而他在合成時 console 出現以下資訊，

```
2) Finished Checking Primitives: CPU user time: 0 seconds. CPU system time: 0 seconds. Elapsed time: 0 seconds; current allocated memory: 402.492 MB.
3) Starting code transformations ...
4) Finished Standard Transforms: CPU user time: 0 seconds. CPU system time: 0 seconds. Elapsed time: 0.01 seconds; current allocated memory: 462.621 MB.
5) Checking synthesizability ...
6) Finished Checking Synthesizability: CPU user time: 0.01 seconds. CPU system time: 0 seconds. Elapsed time: 0.01 seconds; current allocated memory: 462.703 MB.
7) Finished Loop, function and other optimizations: CPU user time: 0.02 seconds. CPU system time: 0 seconds. Elapsed time: 0.03 seconds; current allocated memory: 484.051 MB.
541) Flattening a loop nest 'Col' (Design_Optimization/lab1/matrixmul.cpp:56:20) in function 'matrixmul'.
541) Flattening a loop nest 'Row' (Design_Optimization/lab1/matrixmul.cpp:54:17) in function 'matrixmul'.
8) Finished Architecture Synthesis: CPU user time: 0.04 seconds. CPU system time: 0 seconds. Elapsed time: 0.1 seconds; current allocated memory: 484.051 MB.
9) Starting hardware synthesis...
```

於是我將 directive 稍微修改成和 tutorial 相同的情況，

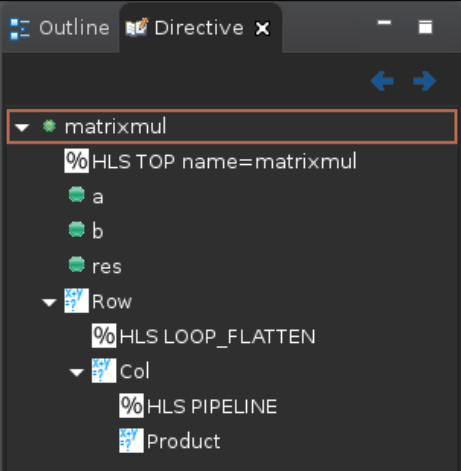


下圖是 sol 2 的合成 report

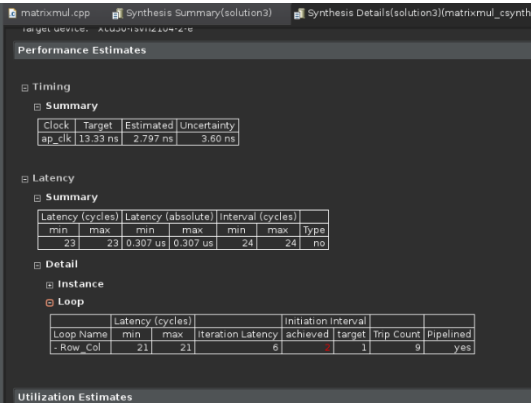


Step 4 Pipeline the Col Loop

下圖是 sol 3 的 directive 設定

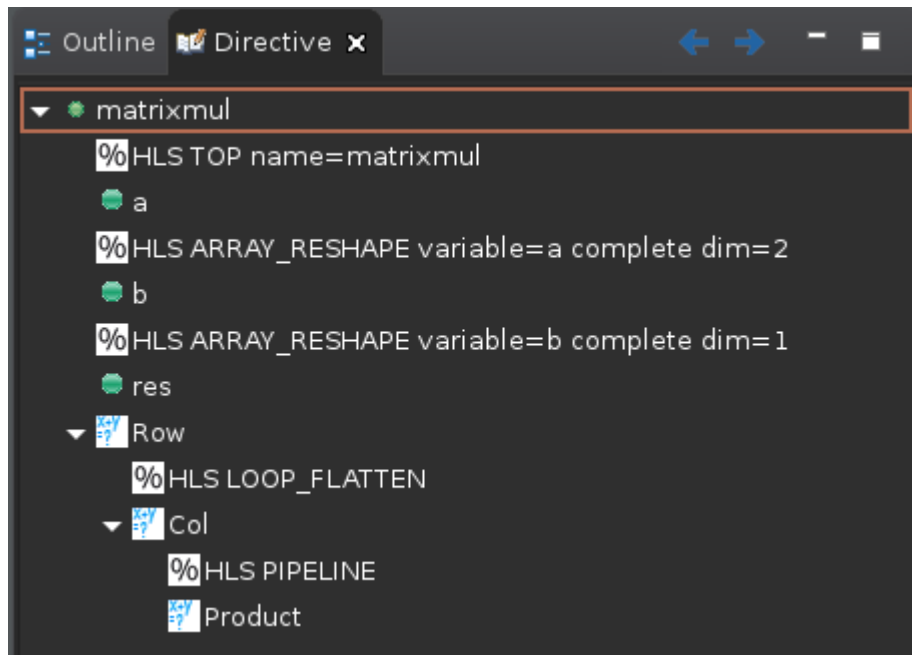


下圖是合成後的 report



■ Step 5 Reshape the Arrays

下圖是 sol 4 的 directive



下圖是合成後的 report

matrixmul.cpp | Synthesis Summary(solution3) | Synthesis Details(solution3)(matrixmul_csynth)

Target: Xilinx:xc7z020:xc7z020-1

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	13.33 ns	2.195 ns	3.60 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		Type
min	max	min	max	min	max	
15	15	0.200 us	0.200 us	16	16	no

Detail

Instance

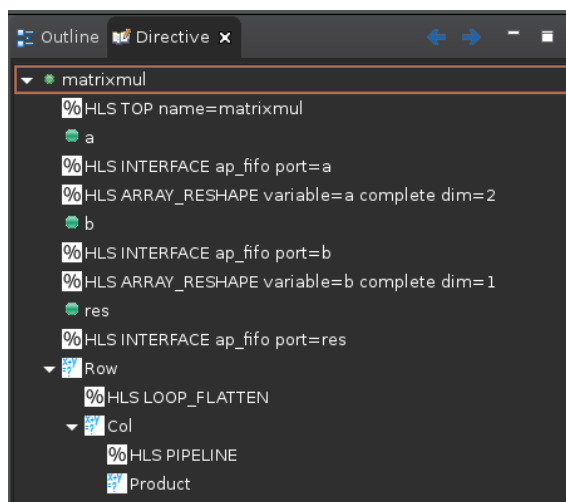
Loop

Loop Name	Latency (cycles)		Iteration	Initiation Interval		Trip Count	Pipelined
	min	max		achieved	target		
Row_Col	13	13	6	1	1	9	yes

Utilization Estimates

■ Step 6 Apply FIFO Interfaces

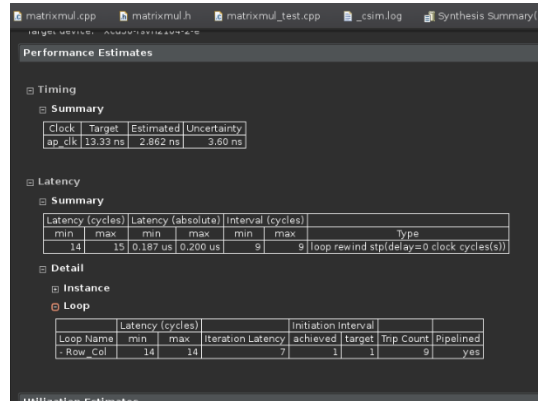
下圖是 sol 5 的 directive



● Lab 2 C Code Optimized for I/O Accesses

■ Step 1 Create and Open the Project

下圖是合成後的 report



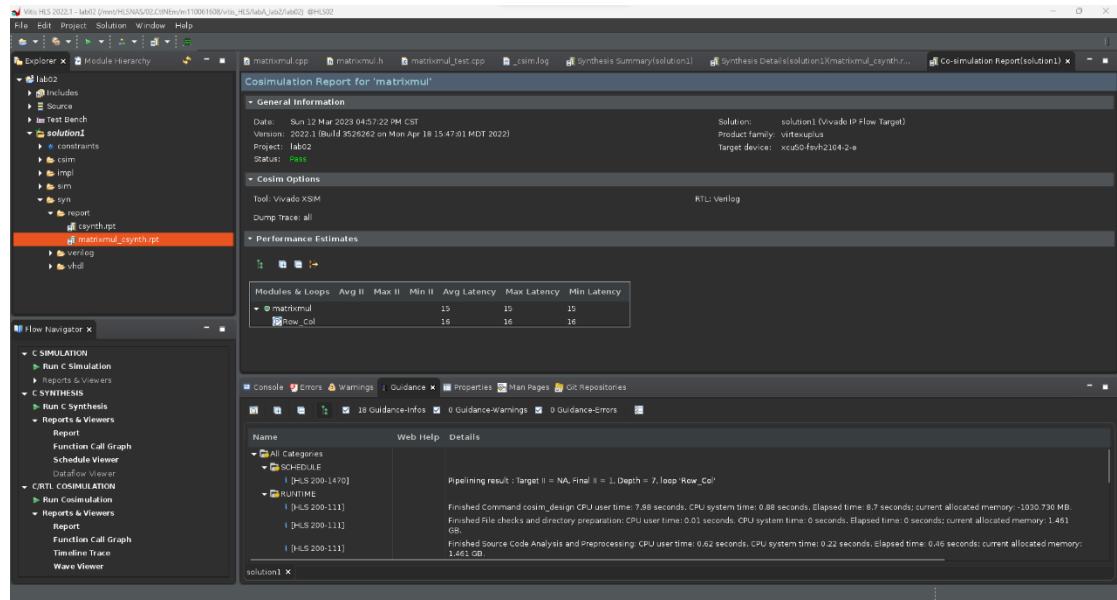
The screenshot shows the 'Performance Estimates' window in Vivado. It contains three sections: Timing, Latency, and Detail. The Timing section has a table with columns: Clock, Target, Estimated, and Uncertainty. The Latency section has a table with columns: Latency (cycles), Latency (absolute), Interval (cycles), and Type. The Detail section has a table with columns: Loop Name, Latency (cycles), Iteration Latency, Initiation Interval, Trip Count, and Pipelined.

Clock	Target	Estimated	Uncertainty
ap_clk	19.39 ns	2.862 ns	3.60 ns

Latency (cycles)	Latency (absolute)	Interval (cycles)	Type
min	max	min	max
14	15	0.187 us	0.200 us
9 loop rewind stp(delay=9 clock cycles(s))			

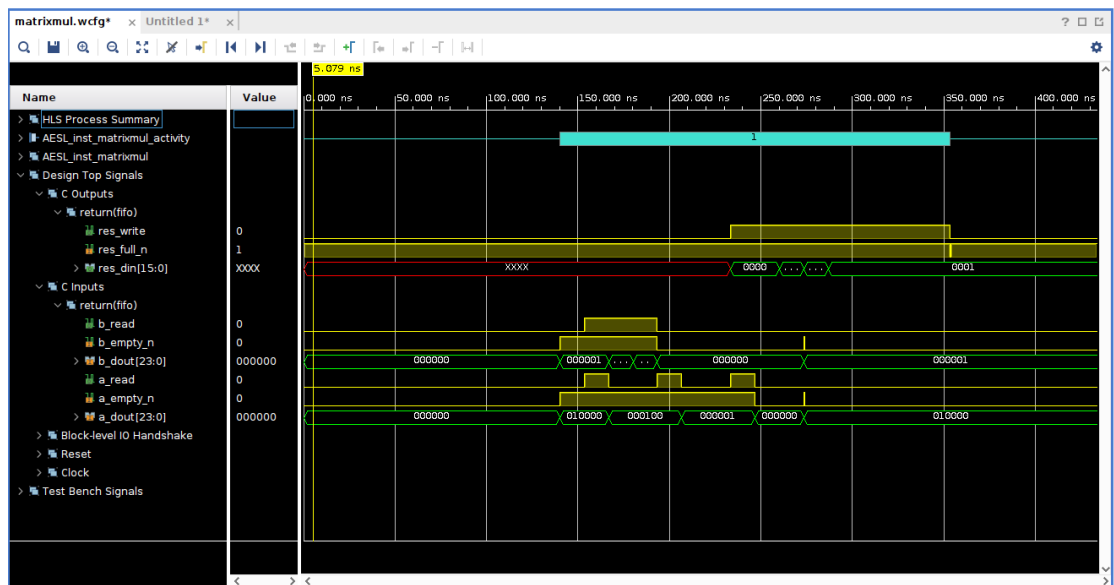
Loop Name	Latency (cycles)	Iteration Latency	Initiation Interval	Trip Count	Pipelined
Row_Col	min	max	achieved	target	
Row_Col	14	14	7	1	1
				9	yes

下圖是 co-sim 的 report 和 waveform



The screenshot shows the Vivado IDE with the 'Co-simulation Report for 'matrixmul'' open. The report includes sections for General Information, Cosim Options, and Performance Estimates. The Performance Estimates section shows a table with columns: Modules & Loops, Avg H, Max H, Min H, Avg Latency, Max Latency, and Min Latency. The Waveform section shows a plot of the signal 'Row_Col' over time.

Modules & Loops	Avg H	Max H	Min H	Avg Latency	Max Latency	Min Latency
matrixmul	15	15	15			
Row_Col	16	16	16			



Github link : https://github.com/sssh311318/HLS_LAB_A