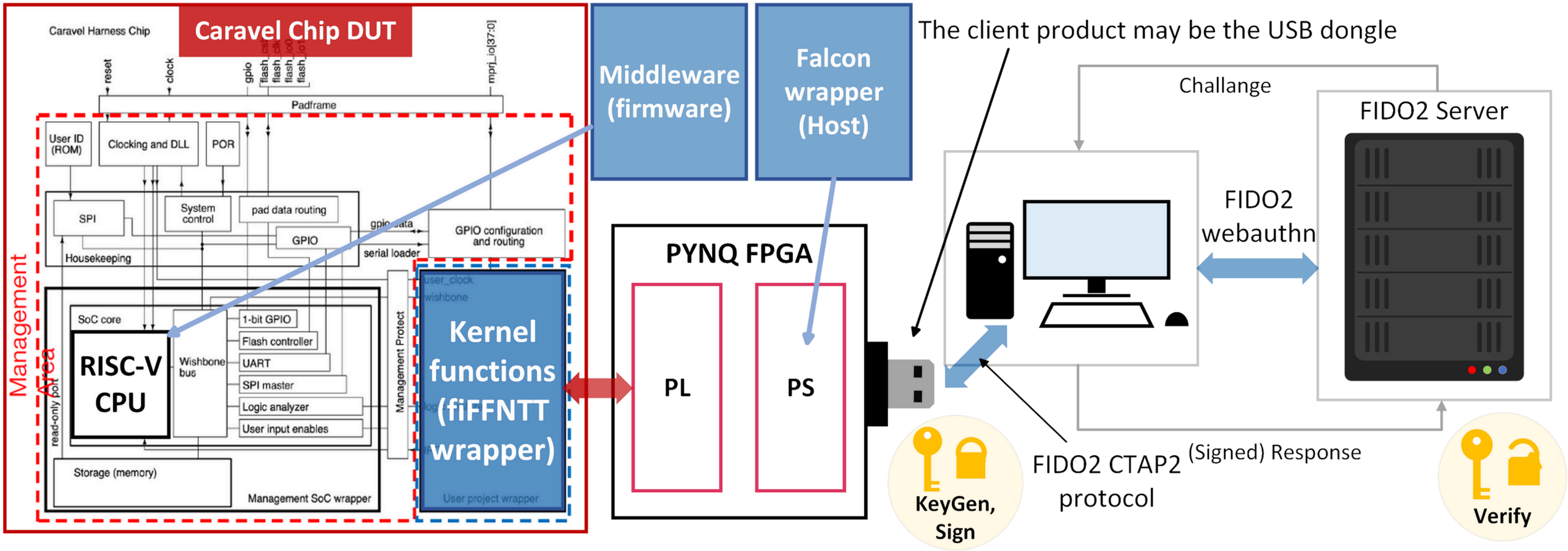
Group 2 & 3

Final Project
Intermediate Status Report

System View


Caravel Chip DUT
Caravel Harness Chip
reset
clock
gpio
mprj_io[37:0]
Padframe
User ID (ROM)
Clocking and DLL
POR
SPI
System control
pad data routing
GPIO
GPIO configuration and routing
Housekeeping
serial loader
Management Area
SoC core
RISC-V CPU
Wishbone bus
1-bit GPIO
Flash controller
UART
SPI master
Logic analyzer
User input enables
Storage (memory)
Management SoC wrapper
Management Protect
user_clock
wishbone
Kernel functions (fiFFNTT wrapper)
User project wrapper
Middleware (firmware)
Falcon wrapper (Host)
PYNQ FPGA
PL
PS
The client product may be the USB dongle
Challange
FIDO2 Server
FIDO2 webauthn
KeyGen, Sign
FIDO2 CTAP2 protocol
(Signed) Response
Verify

Top Down

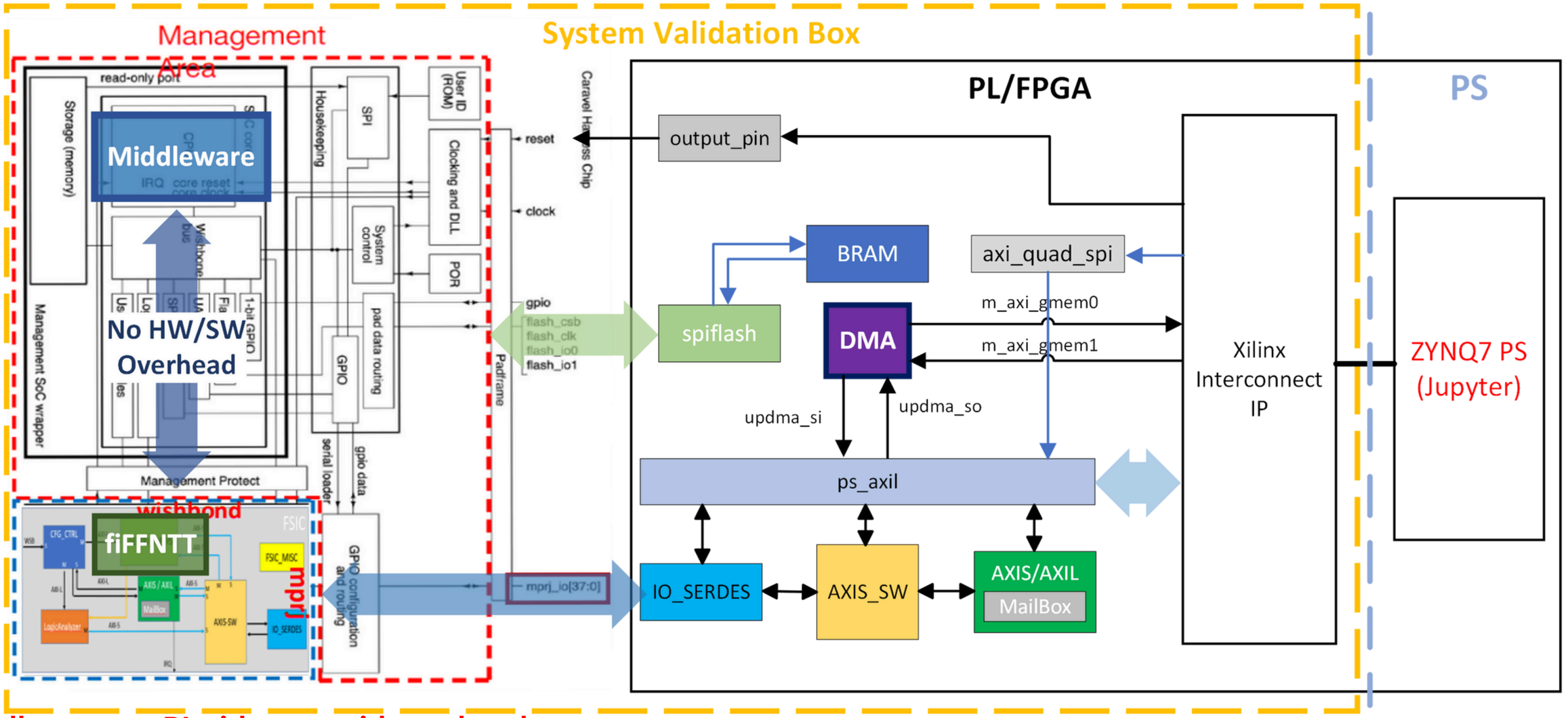
- Falcon API -> Middleware -> Hardware Kernels

Falcon Application Code

Scheduling kernel tasks

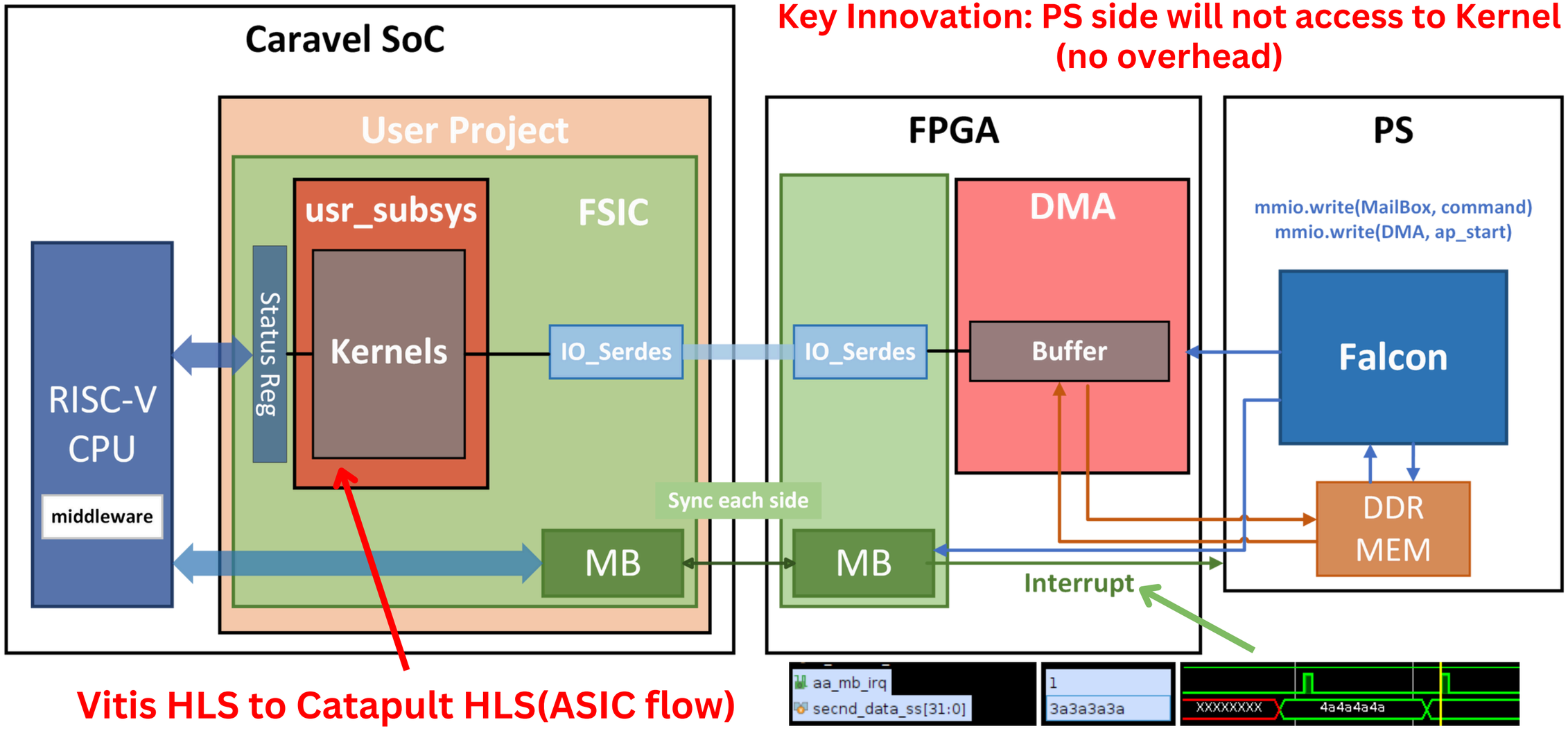
Hardware accelerators

Current Block Diagram



middleware on PL side to avoid overhead

Brief Block Diagram



Current Schedule

Catapult HLS 

Integration into FSIC 

Synopsys flow 

Caravel–FSIC FPGA simulation 

Caravel–FSIC FPGA Validation 

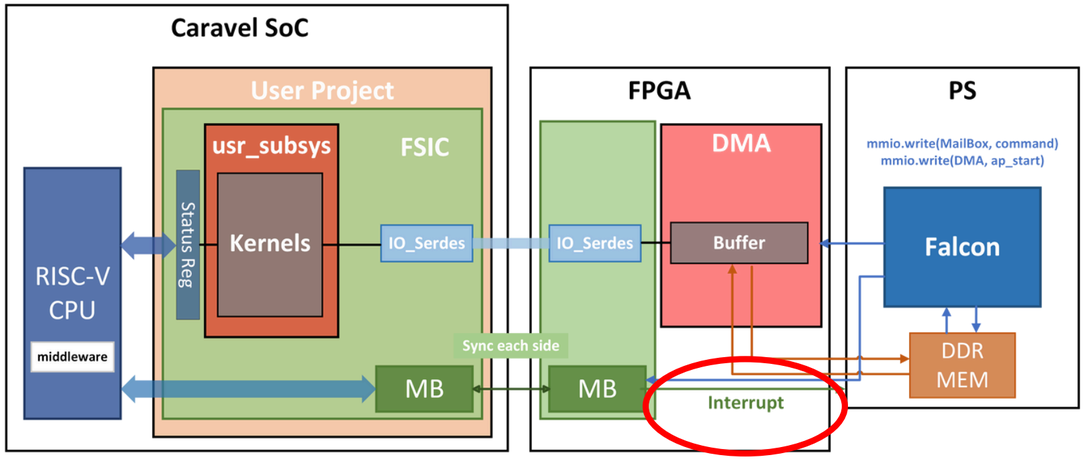
 Undergoing

 Done

Status Report

在lab 5的報告當中提到說我們已完成vitis HLS到catapult HLS的轉換，得到baseline的application accelerator，同時integrate進FSIC。同時我們在simulation以及validation階段均可以跑完一次任意一種演算法(FFT、iFFT、NTT、iNTT)，且算出正確的值。而目前的進度是在simulation階段我們可以成功地依序執行多個演算法，但尚未上板進行validation。而我們interrupt使用lab_fir進行測試可以在simulation階段以及validation使用。

Current Dilemma



Interrupt

In our design, we put our kernel in user project Caravel SoC. When kernel finishing the task, we change the status register. The change in status register will trigger the middleware in RISC-V CPU to write the mailbox, which change the mailbox in FPGA correspondingly. After mailbox is written, it generates interrupt to the PS side.

To achieve this implementation, we add an interrupt controller in our original design. The interrupt is level trigger since we tried edge trigger but couldn’t get the interrupt. Also,We changed the design in our mailbox slightly. However, we can’t have the result we expect to get.

Status Report -
To be tested

1. Verilog testbench只寫一次mailbox然後一直toggle aa_mb_irq_en(0x2100)看是不是也會一直造成interrupt拉起來。

2. firmware讀kernel狀態要拉到uspj外面 不然會跟dma卡在一起。
 同時我們在測試synopsys IC flow的synthesis階段所花費時間過長，可能是因為design並沒有特別進行優化導致design可能過度複雜。

Status Report - Future Work

我們的進度規畫會希望能結合interrupt進行上板validation，同時能夠優化我們的design，並且完成整個synopsys IC flow。