



Denoise-EdgeDetect Filter

組別: 第四組

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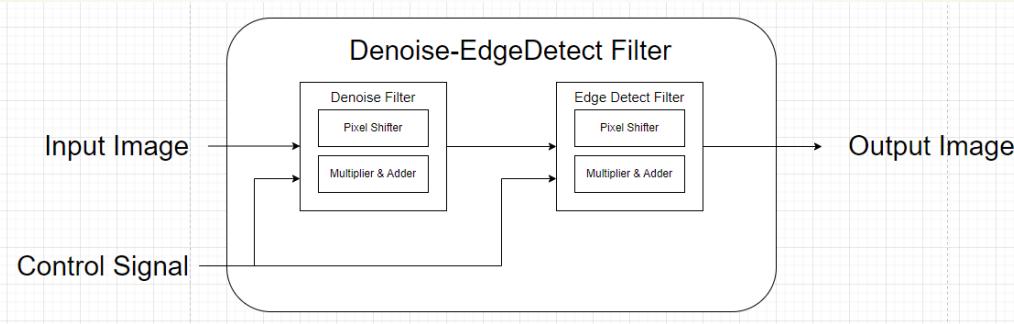


Agenda

- ▶ Catapult HLS (Finsh)
- ▶ Integrate into FSIC (Finsh)
- ▶ Caravel-FSIC FPGA simulation (Encounter some problems)
- ▶ Synopsys flow (Encounter some problems)
- ▶ Caravel-FSIC FPGA validation (Encounter some problems)

Catapult HLS

► System Block



Denoise : Bypass、Gaussian Filter、Medium Filter

EdgeDetect : Bypass、Laplacian Filter、Sobel Filter

Pixel Shifter : Shifts the input image pixel

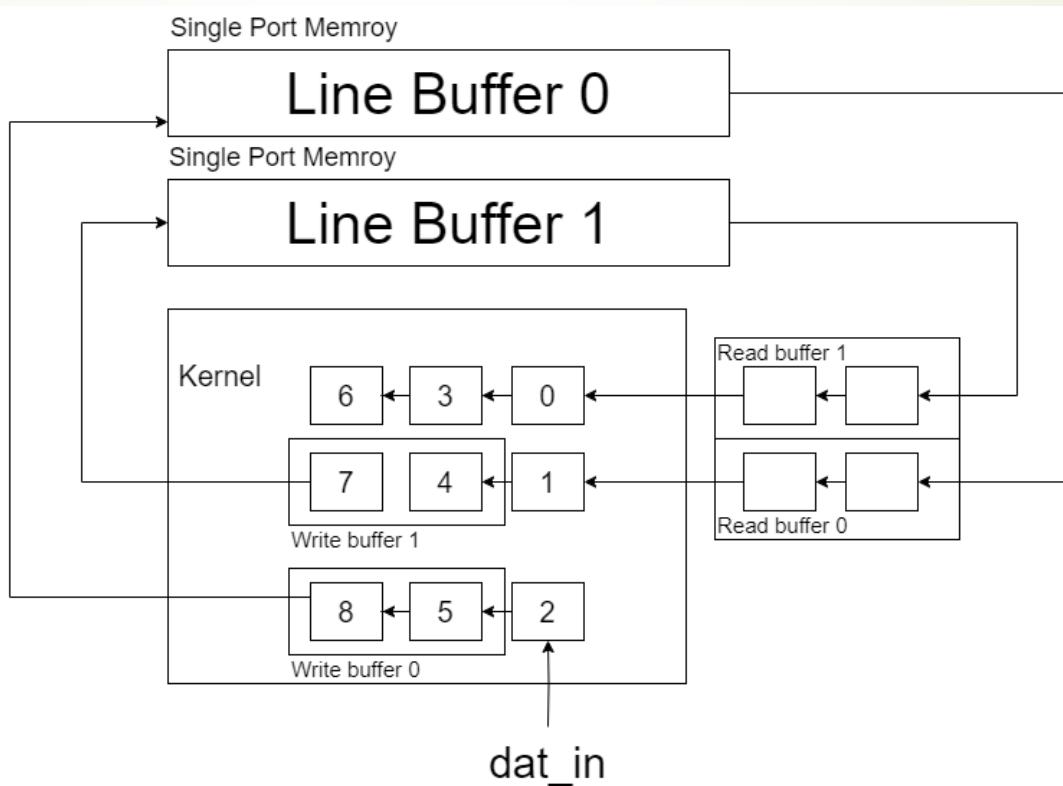
Multiplier & Adder : Performs mathematical operations to apply the kernel to the image pixel

► Synthesis Report

Solution	Latency Cycles	Latency Time	Throughput Cycles	Throughput Time	Slack	Total Area
EdgeDetect_IP::EdgeDetect_Top.v19 (extract)	12	120.00	14	140.00	3.92	10246.53

Catapult HLS

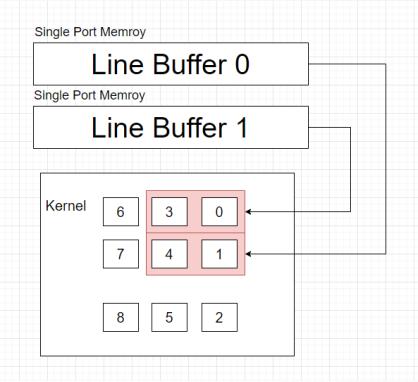
► Pixel Shifter



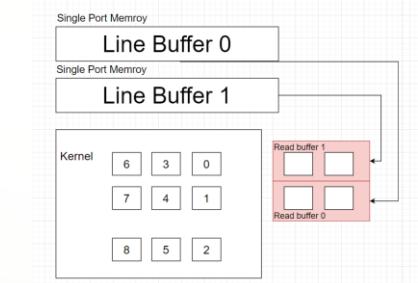
Catapult HLS

► Pixel Shifter – Line buffer access

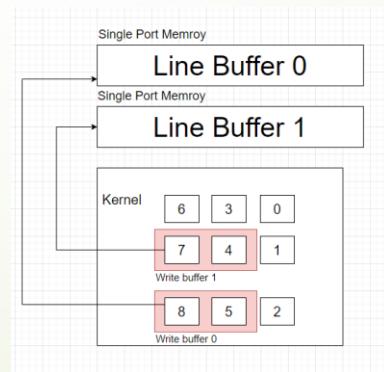
```
// LineBuffer Access  
// first col  
if(x==0){  
    rdbuf0_pix = line_buf0[x/2];  
    rdbuf1_pix = line_buf1[x/2];  
  
    pix[4] = rdbuf0_pix.slc<8>(0);  
    pix[1] = rdbuf0_pix.slc<8>(8);  
  
    pix[3] = rdbuf1_pix.slc<8>(0);  
    pix[0] = rdbuf1_pix.slc<8>(8);  
}else{  
    if ( (x&1)==1 ) {  
        // ReadLineBuffer in x=1, x=3, ... x=odd  
        rdbuf0_pix = line_buf0[(x+1)/2];  
        rdbuf1_pix = line_buf1[(x+1)/2];  
    } else {  
        // WriteLineBuffer in x=2, x=4, ... x=even  
        if(y==0){      // first row => write into buf1  
            line_buf0[(x/2)-1] = wrbuf0_pix;  
        }else{  
            line_buf0[(x/2)-1] = wrbuf0_pix;  
            line_buf1[(x/2)-1] = wrbuf1_pix;  
        }  
    }  
}
```



X=0
> Load Line buffer into kernel



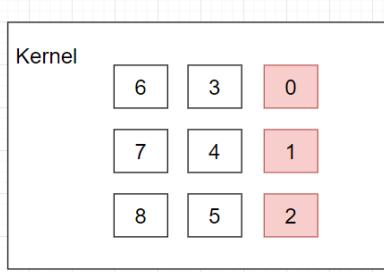
X=1, 3, ..., odd
> Load Line buffer into read buffer



X=2, 4, ..., even
> Write back to line buffer

Catapult HLS

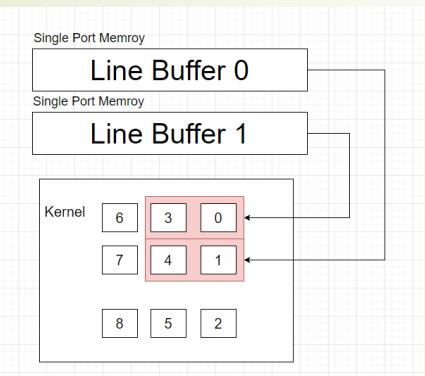
► Pixel Shifter – Load pix0, pix1, pix2



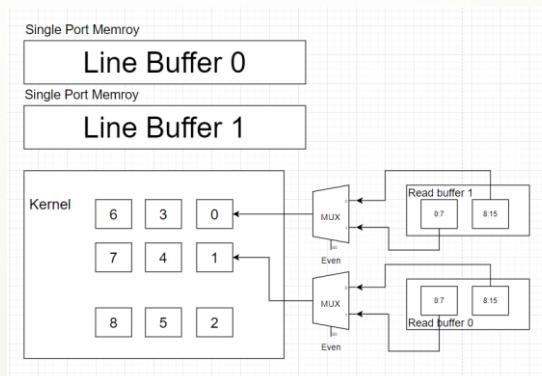
```
// Read Pixel // For uint_pix[0]
pix[0] = (x==0 || x==1)? pix[0]:
           ((x&1)==0)? rdbuf1_pix.slc<8>(0): // even 2, 4, 6, ...
           | rdbuf1_pix.slc<8>(8); // odd 3, 5, 7, ...

pix[1] = (x==0 || x==1)? pix[1]:
           ((x&1)==0)? rdbuf0_pix.slc<8>(0): // even 2, 4, 6, ...
           | rdbuf0_pix.slc<8>(8); // odd 3, 5, 7, ...

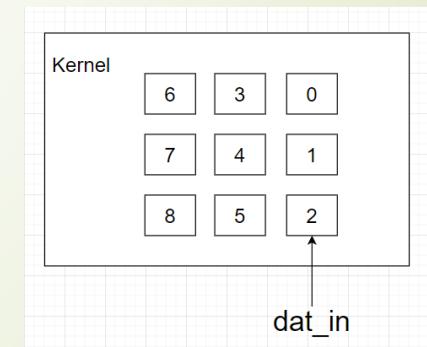
// Read dat_in into pix[2]
if (y <= heightIn-1 && x <= widthIn-1) {
    pix[2] = dat_in.read(); // Read streaming interface
} else{
    pix[2] = pix[2];
}
```



X = 0 or 1 > Remain the same



X = Even > load Read_buffer[0:7]
X = Odd > load Read_buffer[8:15]



Load dat_in into pix2

Catapult HLS

► Pixel Shifter - Padding

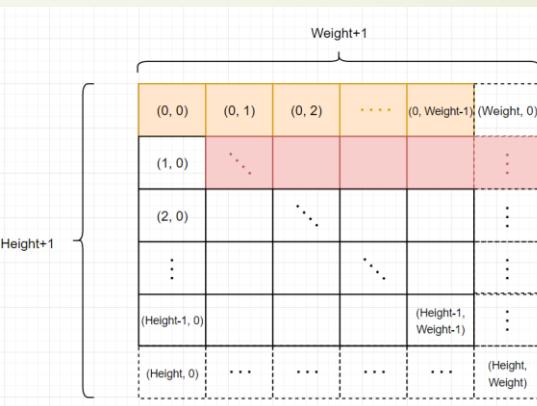
```

if (y == 1) {
    // Top edge
    if (x == 1) {
        // Top-left corner
        pix[7] = pix[4];
        pix[8] = pix[5];
    } else if (x == widthIn) {
        // Top-right corner
        pix[2] = pix[5];
        pix[1] = pix[4];
    }
    pix[0] = pix[1];
    pix[3] = pix[4];
    pix[6] = pix[7];
} else if (y == heightIn) {
}

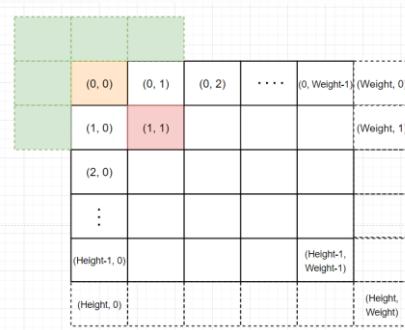
```

Determine if padding to the left($x==1$) or right($x==widthIn$) is needed.

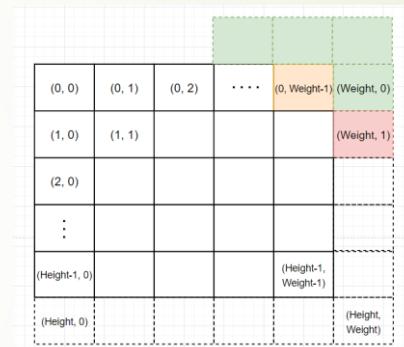
Then, proceed with padding upwards.



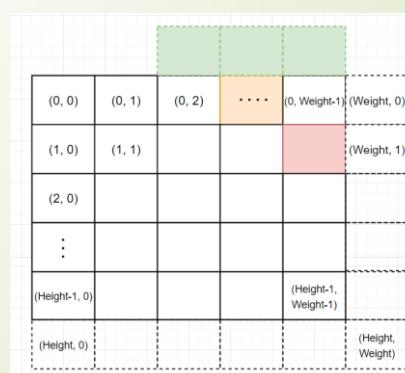
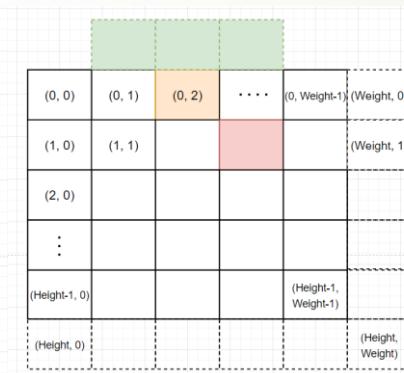
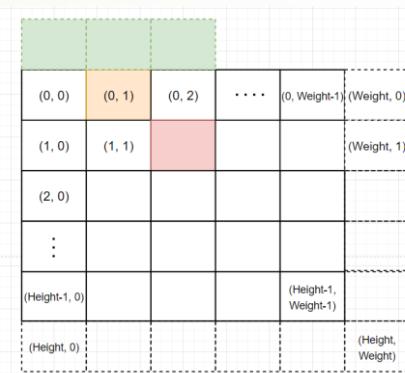
Green: Padding Pixel
Orange: Processing Pixel
Red: For loop idx (x, y)



X=1, Y=1



X=Weight, Y=1



Y=1

Catapult HLS

► Pixel Shifter - Padding

```

} else if (y == heightIn) {
    // Bottom edge
    if (x == 1) {
        // Bottom-left corner
        pix[6] = pix[3];
        pix[7] = pix[4];
    } else if (x == widthIn) {
        // Bottom-right corner
        pix[0] = pix[3];
        pix[1] = pix[4];
    }
    pix[2] = pix[1];
    pix[5] = pix[4];
    pix[8] = pix[7];
} else {

```

Determine if padding to the left($x==1$) or right($x==widthIn$) is needed.

Then, proceed with padding downwards.

(0, 0)	(0, 1)	(0, 2)	...	(0, Weight-1)	(Weight, 0)
(1, 0)					
(2, 0)					
:					
(Height-1, 0)					(Height-1, Weight-1)
(Height, 0)	(Height, Weight)

(0, 0)	(0, 1)	(0, 2)	...	(0, Weight-1)	(Weight, 0)
(1, 0)	..				
(2, 0)		..			
:			..		
(Height-1, 0)					(Height-1, Weight-1)
(Height, 0)	(Height, Weight)

Y=Height, X=1

(0, 0)	(0, 1)	(0, 2)	...	(0, Weight-1)	(Weight, 0)
(1, 0)					
(2, 0)					
:					
(Height-1, 0)					(Height-1, Weight-1)
(Height, 0)					(Height, Weight)

Y=Height,
X=Weight

(0, 0)	(0, 1)	(0, 2)	...	(0, Weight-1)	(Weight, 0)
(1, 0)					
(2, 0)					
:					
(Height-1, 0)					(Height-1, Weight-1)
(Height, 0)	(Height, Weight)

(0, 0)	(0, 1)	(0, 2)	...	(0, Weight-1)	(Weight, 0)
(1, 0)					
(2, 0)					
:					
(Height-1, 0)					(Height-1, Weight-1)
(Height, 0)	(Height, Weight)

Y=Height

(0, 0)	(0, 1)	(0, 2)	...	(0, Weight-1)	(Weight, 0)
(1, 0)					
(2, 0)					
:					
(Height-1, 0)					(Height-1, Weight-1)
(Height, 0)					(Height, Weight)

Catapult HLS

► Pixel Shifter - Padding

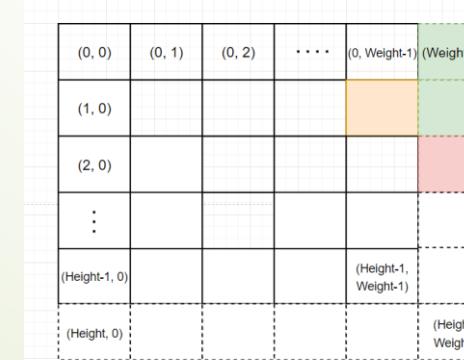
```

} else {
    if (x == 1) {
        // Left edge
        pix[6] = pix[3];
        pix[7] = pix[4];
        pix[8] = pix[5];
    } else if (x == widthIn) {
        // Right edge
        pix[0] = pix[3];
        pix[1] = pix[4];
        pix[2] = pix[5];
    }
}

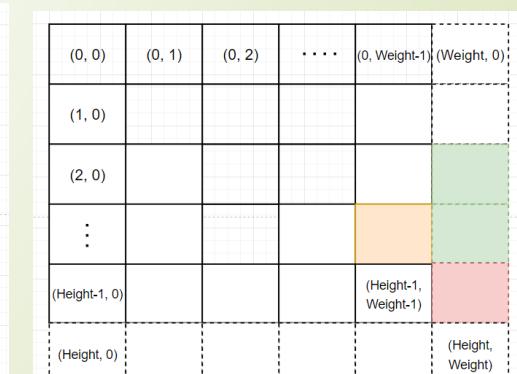
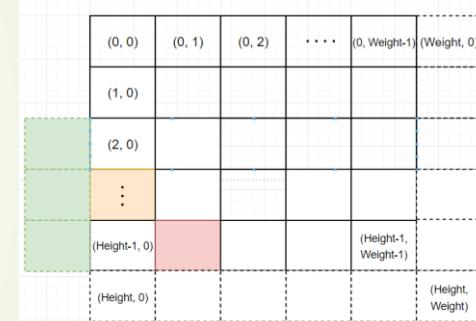
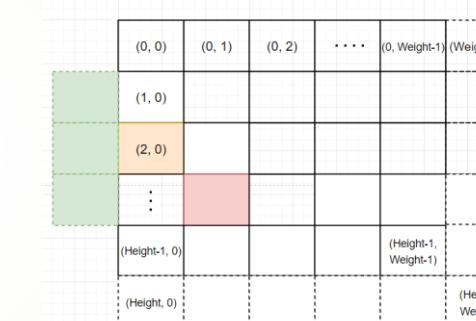
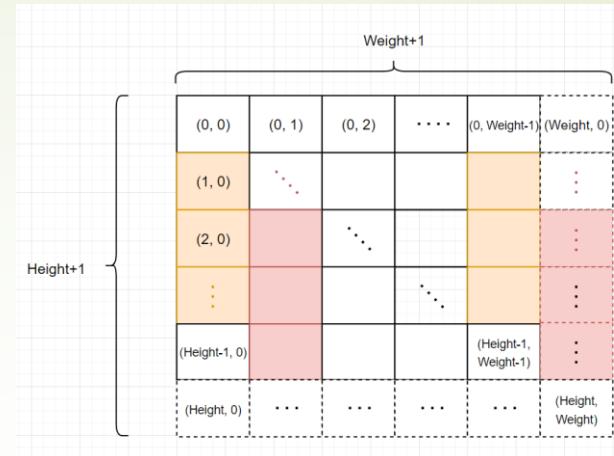
```



Padding left side



Padding right side



Green: Padding Pixel
Orange: Processing Pixel
Red: For loop idx (x, y)

Catapult HLS

► Multiplier & Adder – Calculate

Gaussian Filter

```
 }else if(ctrl_signal == 1){  
    // Gaussian Filter  
    pix_result = 0;  
    for(i=0; i<9; i++){  
        pix_multi_float = pix[i] * Gaussian_kernel[i];  
        pix_result += pix_multi_float / 16;  
    }  
 }else if(ctrl_signal == 2){
```

Laplacian Filter

```
 }else if(ctrl_signal == 1){  
    // Laplacian Filter  
    pix_result = 0;  
    for(i=0; i<9; i++){  
        pix_int = pix[i];  
        pix_result += pix_int * Laplacian_kernel[i];  
    }  
 }else if(ctrl_signal == 2){
```

Sobel Filter

```
 }else if(ctrl_signal == 2){  
    // Sobel Filter  
    pix_result_dx = 0;  
    for(i=0; i<9; i++){  
        pix_int = pix[i];  
        pix_result_dx += pix_int * Sobeldx_kernel[i];  
    }  
    pix_result_dy = 0;  
    for(i=0; i<9; i++){  
        pix_int = pix[i];  
        pix_result_dy += pix_int * Sobeldy_kernel[i];  
    }  
    //printf(" ===== dy_buf=%2d ===== ",dy_buf.to  
    pix_result = pix_result_dx + pix_result_dy;  
    //printf(" ===== pix_resul=%2d ===== \n",pix_  
}
```

Use one multiplier and one adder to finish the calculation

Catapult HLS

► Multiplier & Adder – Calculate

Medium Filter

```
else if(ctrl_signal == 2){  
    // Medium Filter  
    for(i=0; i<9; i++){  
        tmp_pix[i] = pix[i];  
    }  
  
    pix_result = 0;  
    for(j=0; j<5; j++){  
        max_val = tmp_pix[j];  
        max_i = j;  
        for(i=j+1; i<9; i++){  
            if(tmp_pix[i] > max_val){  
                max_val = tmp_pix[i];  
                max_i = i;  
            }  
        }  
        tmp_pix[max_i] = tmp_pix[j];  
    }  
    pix_result = max_val;  
}
```

1. Starting from the jth position, find the maximum value between positions j+1 and END.
2. Once the maximum value is found, swap its position with the jth position to ensure that the values from j+1 to END are less than the value at the jth position (since the values from 0 to jth are not used, there is no need to assign a new value to jth).
3. After five iterations, the maximum value will be the median of the array.

Catapult HLS

► Pixel Shifter – Output

```
// Output dat_out
if (y!=0 && x!=0) {
    // Saturation
    //printf(" ====== pix_result ======
    //printf(" ====== x=%u, y=%u ======
    //printf(" ====== pix_result_sat=%2d, p

    if(pix_result < 0){
        pix_result_sat = 0;
    }else if(pix_result > 255){
        pix_result_sat = 255;
    }else{
        pix_result_sat = pix_result.slc<8>(0);
    }
    dat_out.write(pix_result_sat);
}
```

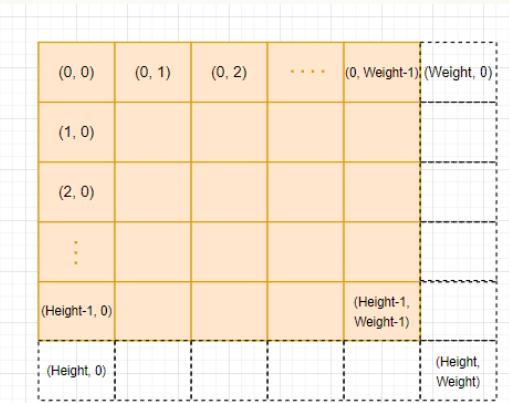
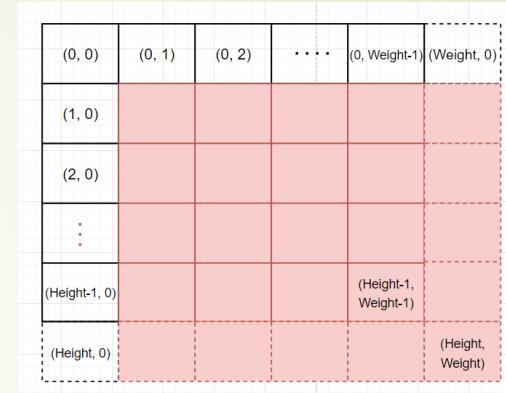
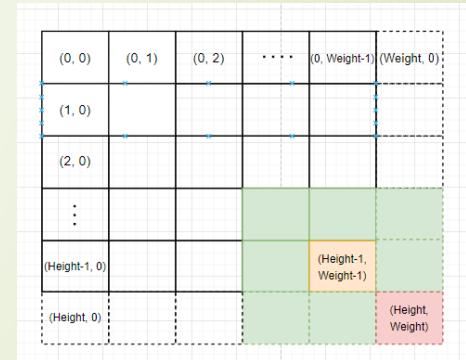
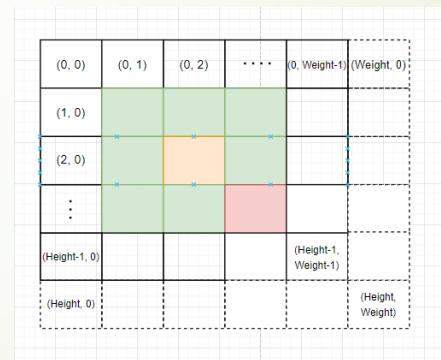
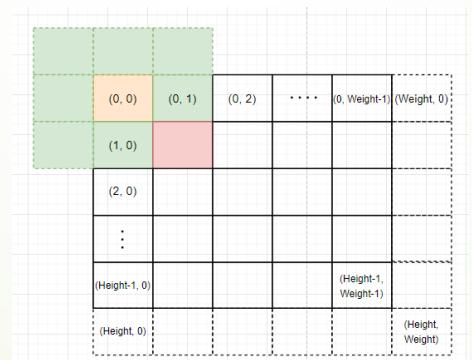


Image Pixel



Output the result when (x != 0 && y != 0)

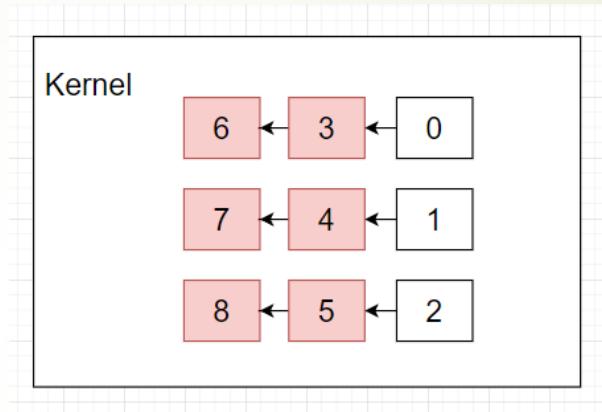


Green: 3X3 Kernel
Orange: Processing Pixel
Red: For loop idx (x, y)

Catapult HLS

► Pixel Shifter – Pixel Shift

```
// Pixel Shift
pix[6] = pix[3]; pix[7] = pix[4]; pix[8] = pix[5];
if(x==0){
    // maintain
    pix[3] = pix[3]; pix[4] = pix[4];
} else{
    // shift
    pix[3] = pix[0]; pix[4] = pix[1];
}
pix[5] = pix[2];
```

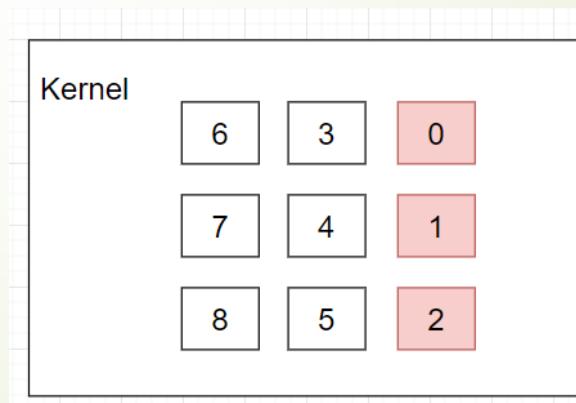


When the output is complete, the pixels need to be shifted.

```
// Read Pixel // For uint_pix[0]
pix[0] = (x==0 || x==1)? pix[0]:
        ((x&1)==0)? rdbuf1_pix.slc<8>(0): // even 2, 4, 6, ...
                    | rdbuf1_pix.slc<8>(8); // odd 3, 5, 7, ...

pix[1] = (x==0 || x==1)? pix[1]:
        ((x&1)==0)? rdbuf0_pix.slc<8>(0): // even 2, 4, 6, ...
                    | rdbuf0_pix.slc<8>(8); // odd 3, 5, 7, ...

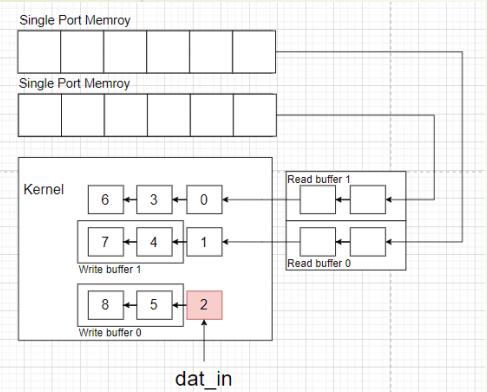
// Read dat_in into pix[2]
if (y <= heightIn-1 && x <= widthIn-1) {
    pix[2] = dat_in.read(); // Read streaming interface
} else{
    pix[2] = pix[2];
}
```



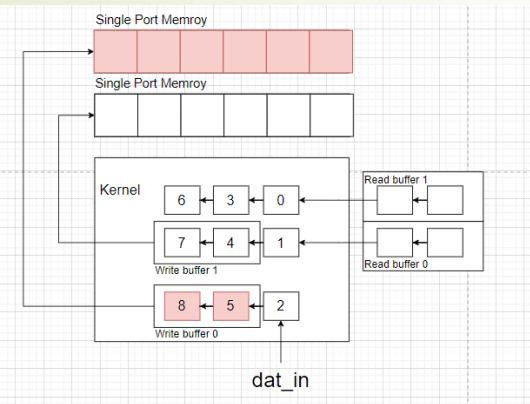
Next, load pix0, pix1, and pix2, and repeat the whole process.

Catapult HLS

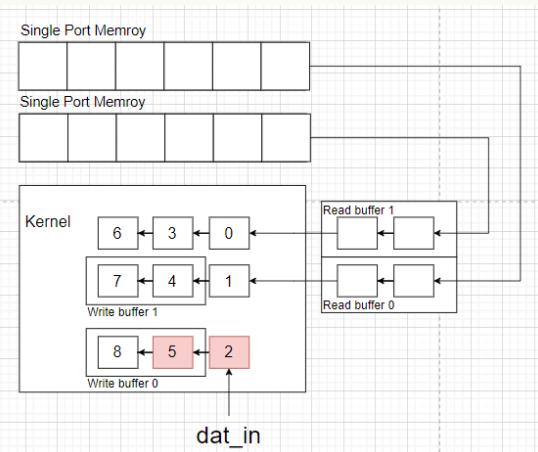
► $Y=0$



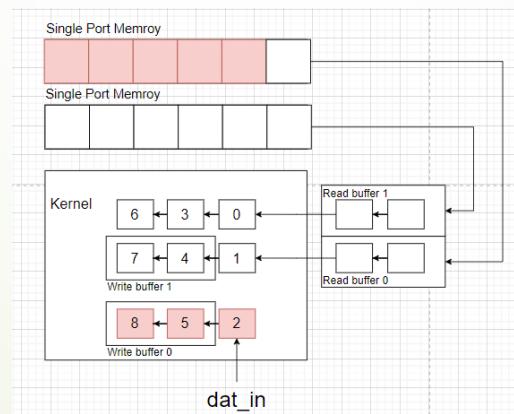
X=0



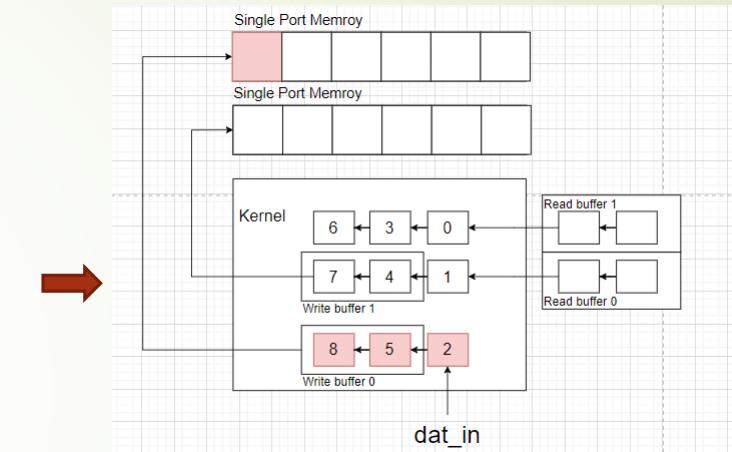
X= Weight



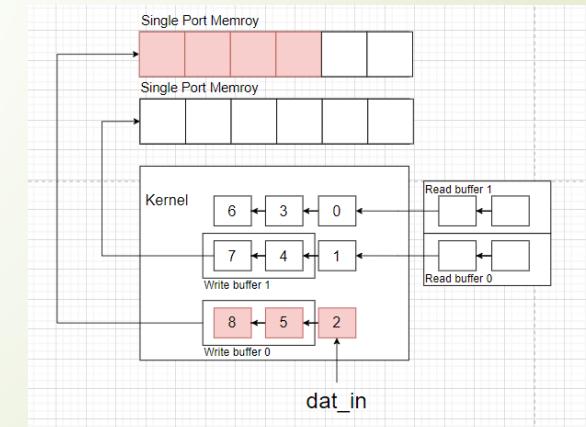
X=1



X= Weight-1



X=2

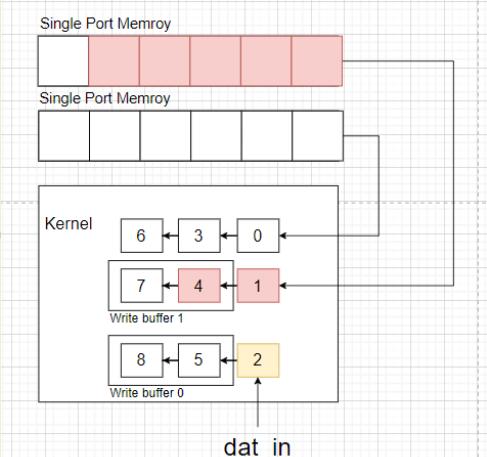


X= ...

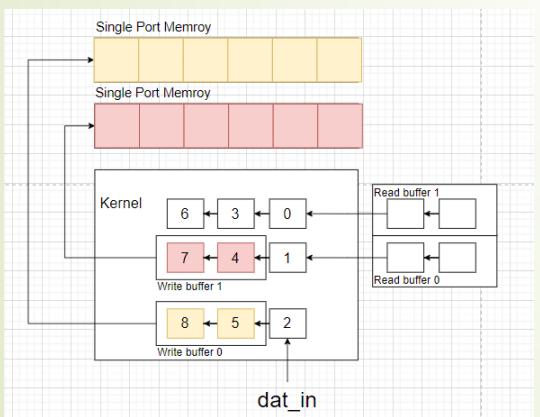


Catapult HLS

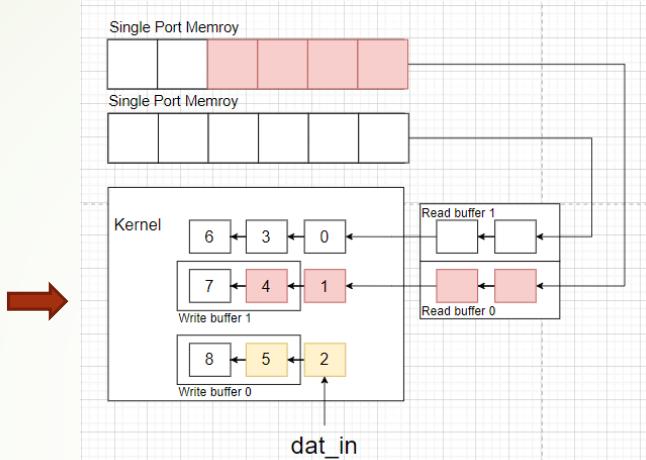
→ $Y=1$



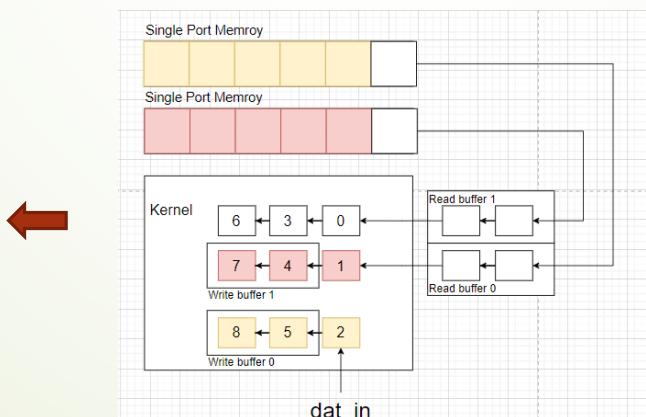
$X=0$



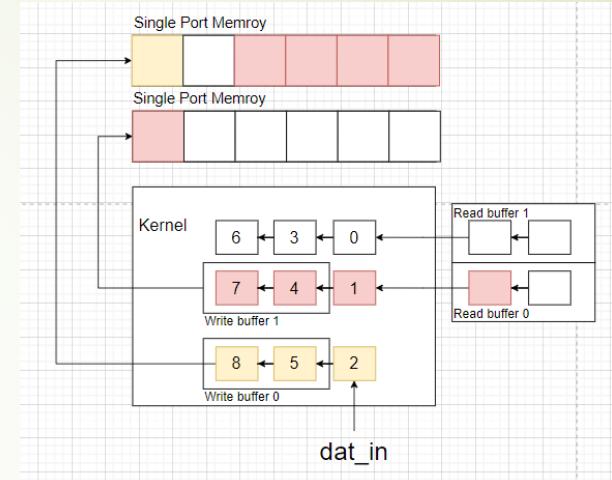
$X= \text{Weight}$



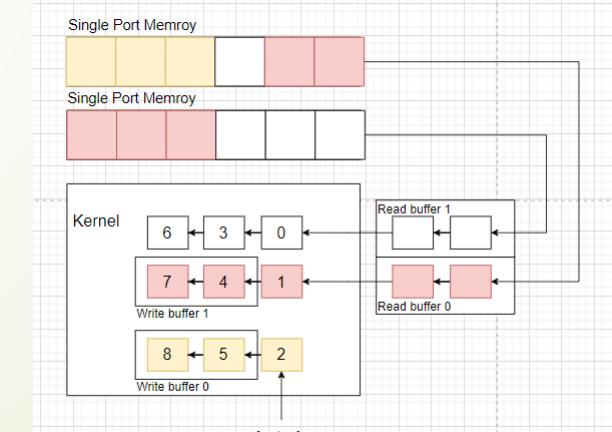
$X=1$



$X= \text{Weight-1}$



$X=2$

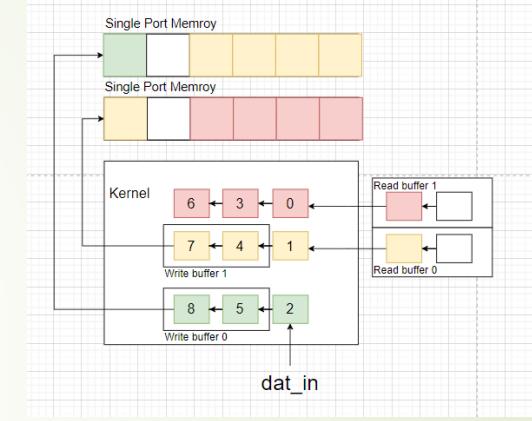
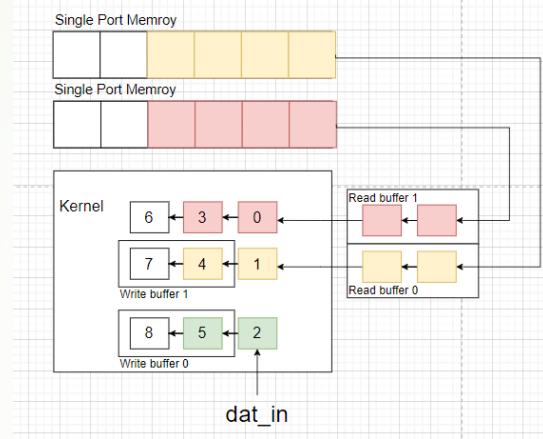
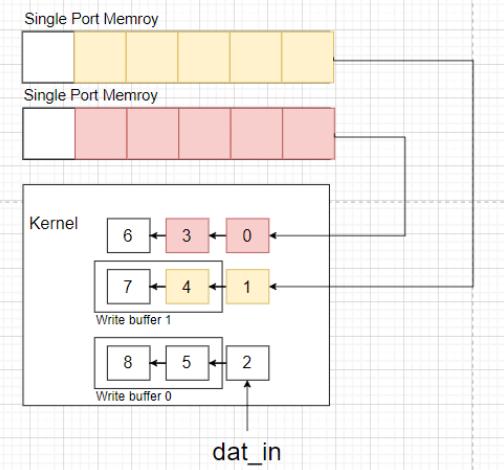


$X= \dots$

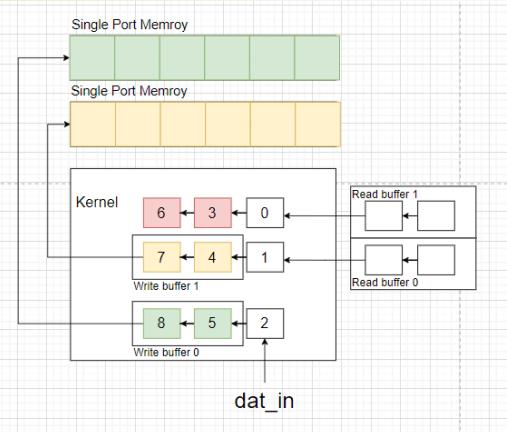


Catapult HLS

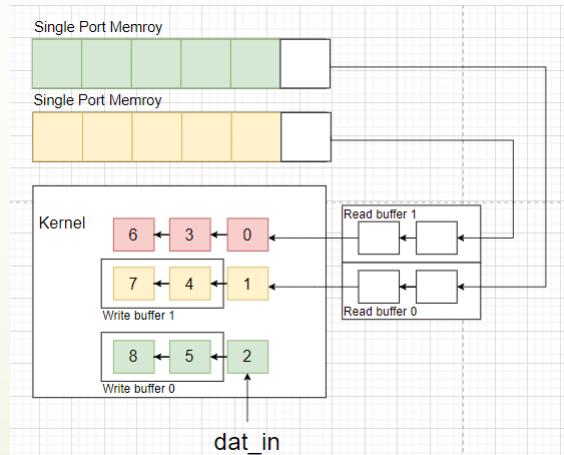
→ $Y=2$



X=0

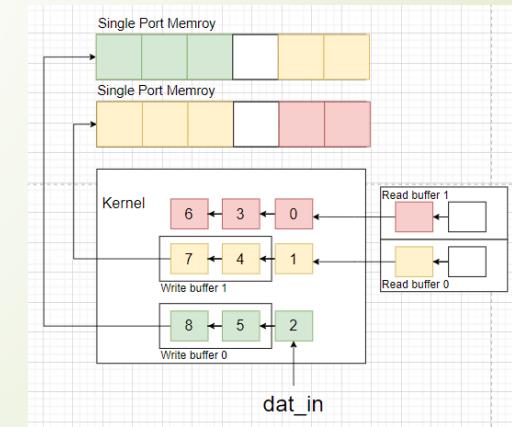


X=1



...

X=2



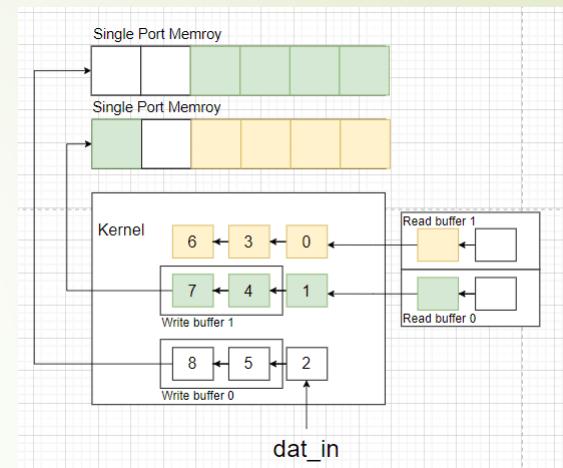
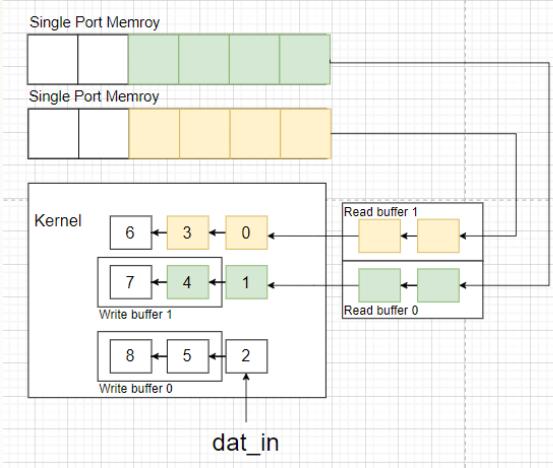
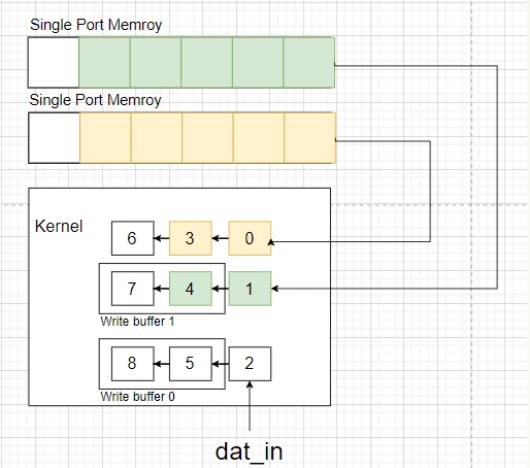
X= ...

X= Weight

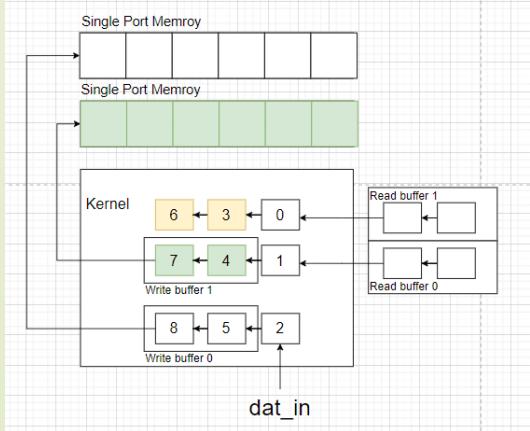
X= Weight-1

Catapult HLS

► Y=Height



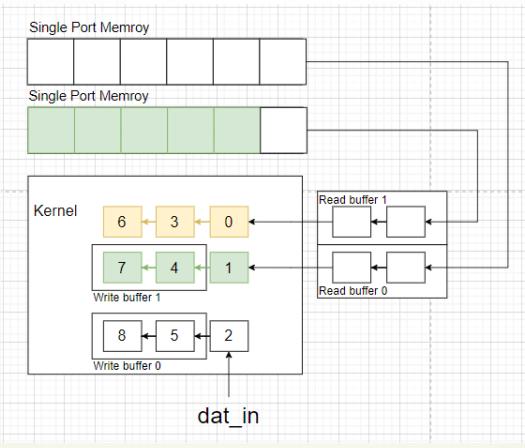
X=0



X= Weight



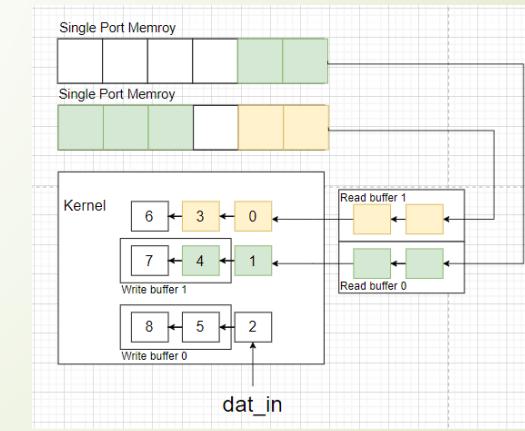
X=1



X= Weight-1

...

X=2



X= ...

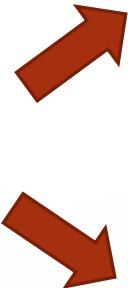
Catapult HLS

Result

Image with Gaussian noise



Gaussian Filter



Medium Filter



Catapult HLS

Result

Image with SaltPepper noise



Gaussian Filter



Medium Filter



Catapult HLS

Result

Image with large edge variation



Laplacian Filter



Sobel Filter



Catapult HLS

Result

Image with small edge variation



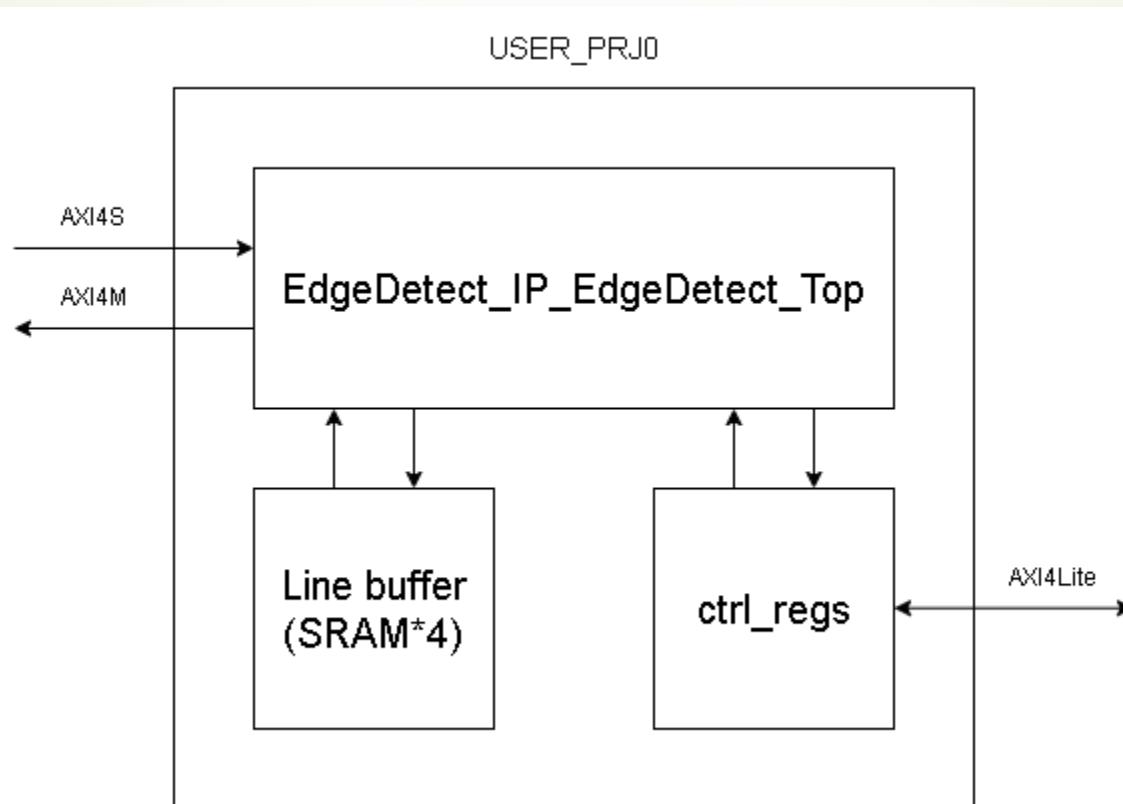
Laplacian Filter



Sobel Filter

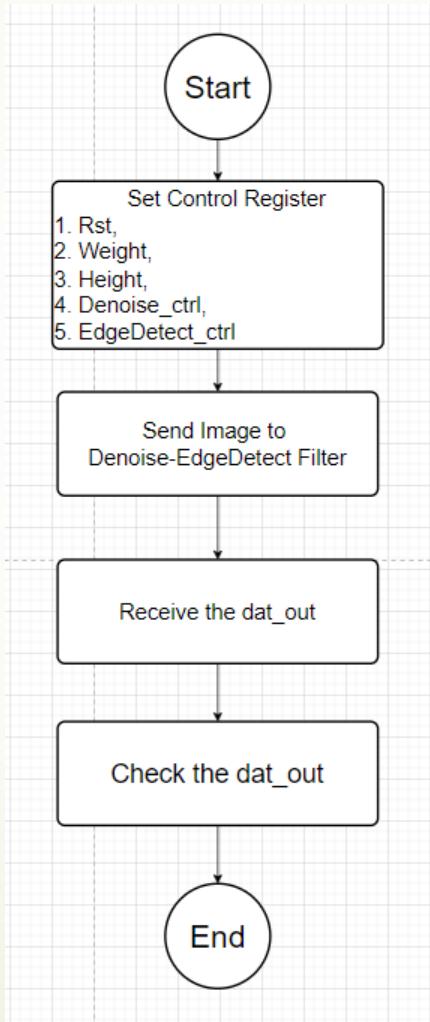


Integrate into FSIC



Caravel-FSIC FPGA simulation

► Flow



FSIC Testbench

```
test001_up_soc_cfg: soc cfg read/write test
    1665=> soc_up_cfg_write : wbs_addr=30000000, wbs_sel=0001, wbs_wdata=00000001
    1945=> soc_up_cfg_read : wbs_addr=30000000, wbs_sel=0001
    1945=> soc wishbone read data result : send soc_cfg_read_event
    1945=> soc_up_cfg_read : got soc_cfg_read_event
    1945=> test001_up_soc_cfg [PASS] cfg_read_data_expect_value=00000001, cfg_read_data_captured=00000001

    2185=> soc_up_cfg_write : wbs_addr=30000000, wbs_sel=0001, wbs_wdata=00000000
    2465=> soc_up_cfg_read : wbs_addr=30000000, wbs_sel=0001
    2465=> soc wishbone read data result : send soc_cfg_read_event
    2465=> soc_up_cfg_read : got soc_cfg_read_event
    2465=> test001_up_soc_cfg [PASS] cfg_read_data_expect_value=00000000, cfg_read_data_captured=00000000

    2705=> soc_up_cfg_write : wbs_addr=30000004, wbs_sel=0111, wbs_wdata=00000080
    2985=> soc_up_cfg_read : wbs_addr=30000004, wbs_sel=0111
    2985=> soc wishbone read data result : send soc_cfg_read_event
    2985=> soc_up_cfg_read : got soc_cfg_read_event
    2985=> test001_up_soc_cfg [PASS] cfg_read_data_expect_value=00000080, cfg_read_data_captured=00000080

    3225=> soc_up_cfg_write : wbs_addr=30000008, wbs_sel=0111, wbs_wdata=00000080
    3505=> soc_up_cfg_read : wbs_addr=30000008, wbs_sel=0111
    3505=> soc wishbone read data result : send soc_cfg_read_event
    3505=> soc_up_cfg_read : got soc_cfg_read_event
    3505=> test001_up_soc_cfg [PASS] cfg_read_data_expect_value=00000080, cfg_read_data_captured=00000080

    3745=> soc_up_cfg_write : wbs_addr=3000000c, wbs_sel=0001, wbs_wdata=00000000
    4025=> soc_up_cfg_read : wbs_addr=3000000c, wbs_sel=0001
    4025=> soc wishbone read data result : send soc_cfg_read_event
    4025=> soc_up_cfg_read : got soc_cfg_read_event
    4025=> test001_up_soc_cfg [PASS] cfg_read_data_expect_value=00000000, cfg_read_data_captured=00000000

    4265=> soc_up_cfg_write : wbs_addr=30000010, wbs_sel=0001, wbs_wdata=00000002
    4545=> soc_up_cfg_read : wbs_addr=30000010, wbs_sel=0001
    4545=> soc wishbone read data result : send soc_cfg_read_event
    4545=> soc_up_cfg_read : got soc_cfg_read_event
    4545=> test001_up_soc_cfg [PASS] cfg_read_data_expect_value=00000002, cfg_read_data_captured=00000002
```

FSIC Testbench

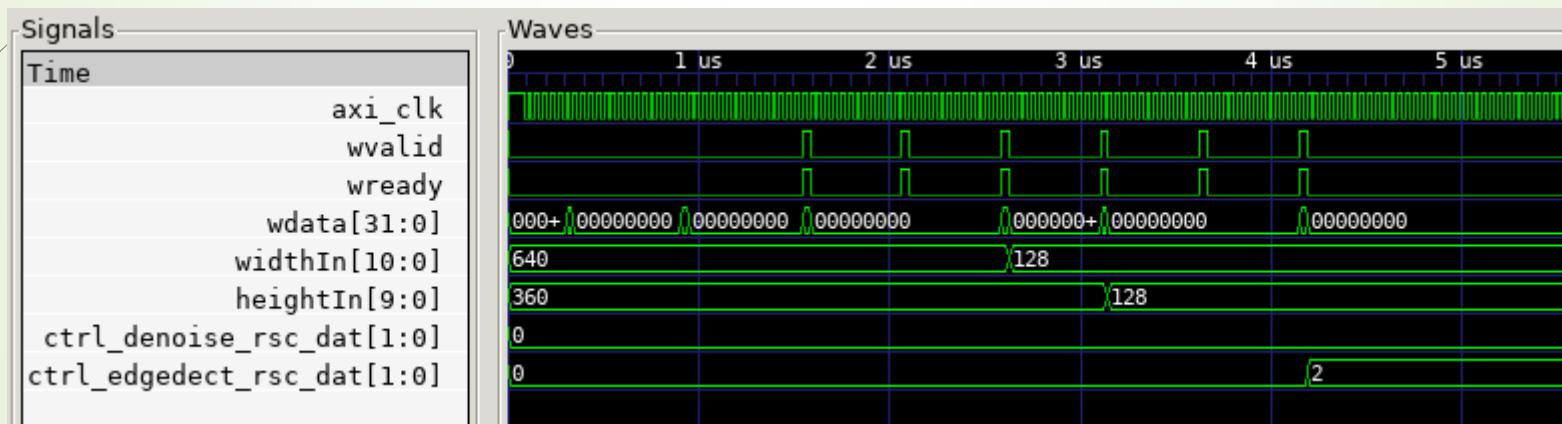
```
5450985=> fpga_axis_req send data, vcnt =      117
5498185=> fpga_axis_req send data, vcnt =      118
5545385=> fpga_axis_req send data, vcnt =      119
5589705=> fpga_axis_req send data, vcnt =      120
5636585=> fpga_axis_req send data, vcnt =      121
5683785=> fpga_axis_req send data, vcnt =      122
5730985=> fpga_axis_req send data, vcnt =      123
5778185=> fpga_axis_req send data, vcnt =      124
5822505=> fpga_axis_req send data, vcnt =      125
5869385=> fpga_axis_req send data, vcnt =      126
5916585=> fpga_axis_req send data, vcnt =      127
5916585=> test002_fpga_axis_req done
5916585=> soc_to_fpga_axis_expect_count =      16384
5916585=> soc_to_fpga_axis_captured_count =      16109
5916585=> fpga_axis_test_length =      16384
5916585=> check_fpga_cnt =      16384
6016225=> soc_to_fpga_axis_captured : send soc_to_fpga_axiis_event
-----
6016225=> test002_up_soc_rpt [PASS] cfg_read_data_expect_value=00000002, cfg_read_data_captured=00000002
-----
6016225=> test002 [PASS] soc_to_fpga_axis_expect_count =      16384, soc_to_fpga_axis_captured_count =      16384
6016225=> test002_up_soc_rpt [PASS] cfg_read_data_expect_value=00000002, cfg_read_data_captured=00000002
-----
```

FSIC Testbench

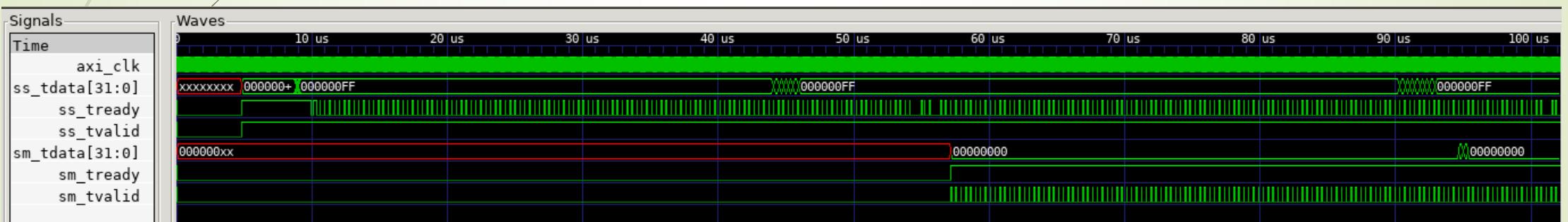
```
6016225=> test002 [PASS] idx3= 16361, soc_to_fpga_axis_expect_value[ 16361] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16361] = 000X00000000
6016225=> test002 [PASS] idx3= 16362, soc_to_fpga_axis_expect_value[ 16362] = 0000xxxxxxff, soc_to_fpga_axis_captured[ 16362] = 000X000000ff
6016225=> test002 [PASS] idx3= 16363, soc_to_fpga_axis_expect_value[ 16363] = 0000xxxxxxff, soc_to_fpga_axis_captured[ 16363] = 000X000000ff
6016225=> test002 [PASS] idx3= 16364, soc_to_fpga_axis_expect_value[ 16364] = 0000xxxxxxff, soc_to_fpga_axis_captured[ 16364] = 000X000000ff
6016225=> test002 [PASS] idx3= 16365, soc_to_fpga_axis_expect_value[ 16365] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16365] = 000X00000000
6016225=> test002 [PASS] idx3= 16366, soc_to_fpga_axis_expect_value[ 16366] = 0000xxxxxx00c, soc_to_fpga_axis_captured[ 16366] = 000X0000000c
6016225=> test002 [PASS] idx3= 16367, soc_to_fpga_axis_expect_value[ 16367] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16367] = 000X00000000
6016225=> test002 [PASS] idx3= 16368, soc_to_fpga_axis_expect_value[ 16368] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16368] = 000X00000000
6016225=> test002 [PASS] idx3= 16369, soc_to_fpga_axis_expect_value[ 16369] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16369] = 000X00000000
6016225=> test002 [PASS] idx3= 16370, soc_to_fpga_axis_expect_value[ 16370] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16370] = 000X00000000
6016225=> test002 [PASS] idx3= 16371, soc_to_fpga_axis_expect_value[ 16371] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16371] = 000X00000000
6016225=> test002 [PASS] idx3= 16372, soc_to_fpga_axis_expect_value[ 16372] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16372] = 000X00000000
6016225=> test002 [PASS] idx3= 16373, soc_to_fpga_axis_expect_value[ 16373] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16373] = 000X00000000
6016225=> test002 [PASS] idx3= 16374, soc_to_fpga_axis_expect_value[ 16374] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16374] = 000X00000000
6016225=> test002 [PASS] idx3= 16375, soc_to_fpga_axis_expect_value[ 16375] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16375] = 000X00000000
6016225=> test002 [PASS] idx3= 16376, soc_to_fpga_axis_expect_value[ 16376] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16376] = 000X00000000
6016225=> test002 [PASS] idx3= 16377, soc_to_fpga_axis_expect_value[ 16377] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16377] = 000X00000000
6016225=> test002 [PASS] idx3= 16378, soc_to_fpga_axis_expect_value[ 16378] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16378] = 000X00000000
6016225=> test002 [PASS] idx3= 16379, soc_to_fpga_axis_expect_value[ 16379] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16379] = 000X00000000
6016225=> test002 [PASS] idx3= 16380, soc_to_fpga_axis_expect_value[ 16380] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16380] = 000X00000000
6016225=> test002 [PASS] idx3= 16381, soc_to_fpga_axis_expect_value[ 16381] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16381] = 000X00000000
6016225=> test002 [PASS] idx3= 16382, soc_to_fpga_axis_expect_value[ 16382] = 0000xxxxxx00, soc_to_fpga_axis_captured[ 16382] = 000X00000000
6016225=> test002 [PASS] idx3= 16383, soc_to_fpga_axis_expect_value[ 16383] = 0001xxxxxx00, soc_to_fpga_axis_captured[ 16383] = 000X00000000
6016225=> soc_up_cfg_write : wbs_addr=30000018, wbs_sel=0001, wbs_wdata=00000001
-----
=====
=====

6017025=> Final result [PASS], check_cnt = 16392, error_cnt = 0000
```

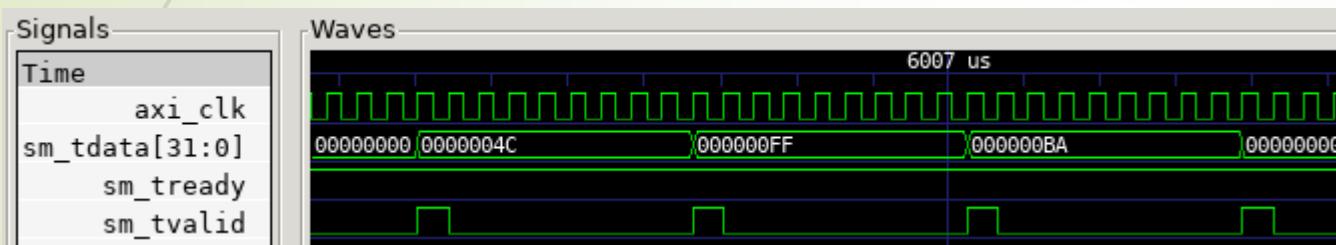
FSIC Testbench



FSIC Testbench

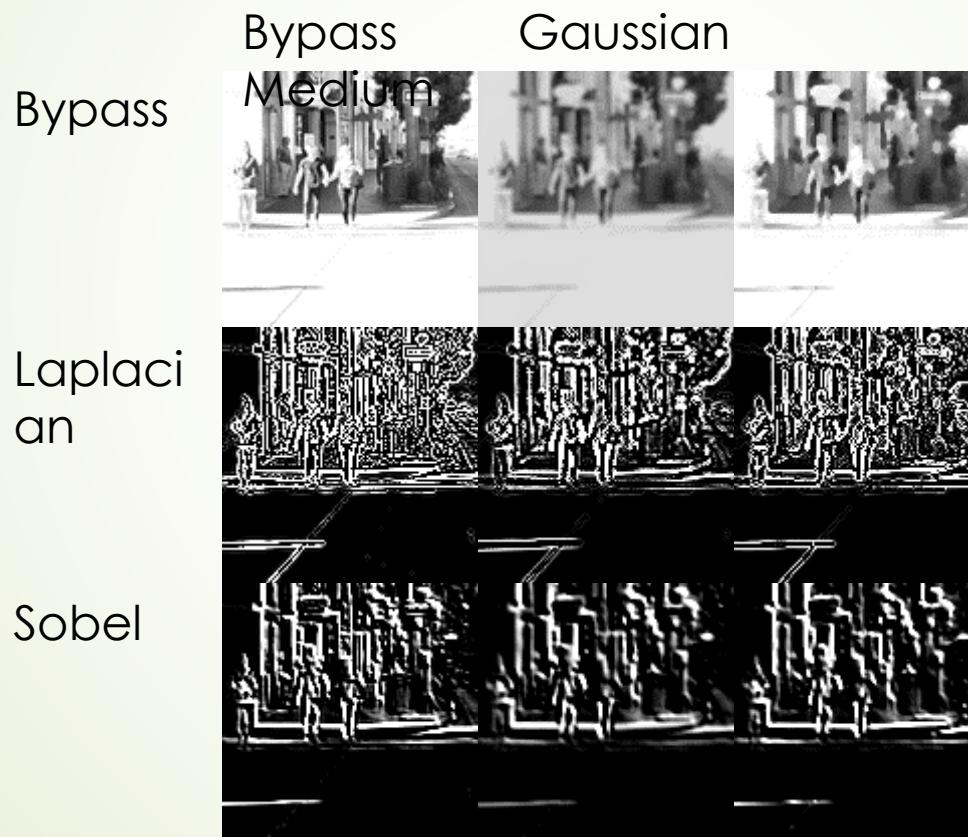


FSIC Testbench

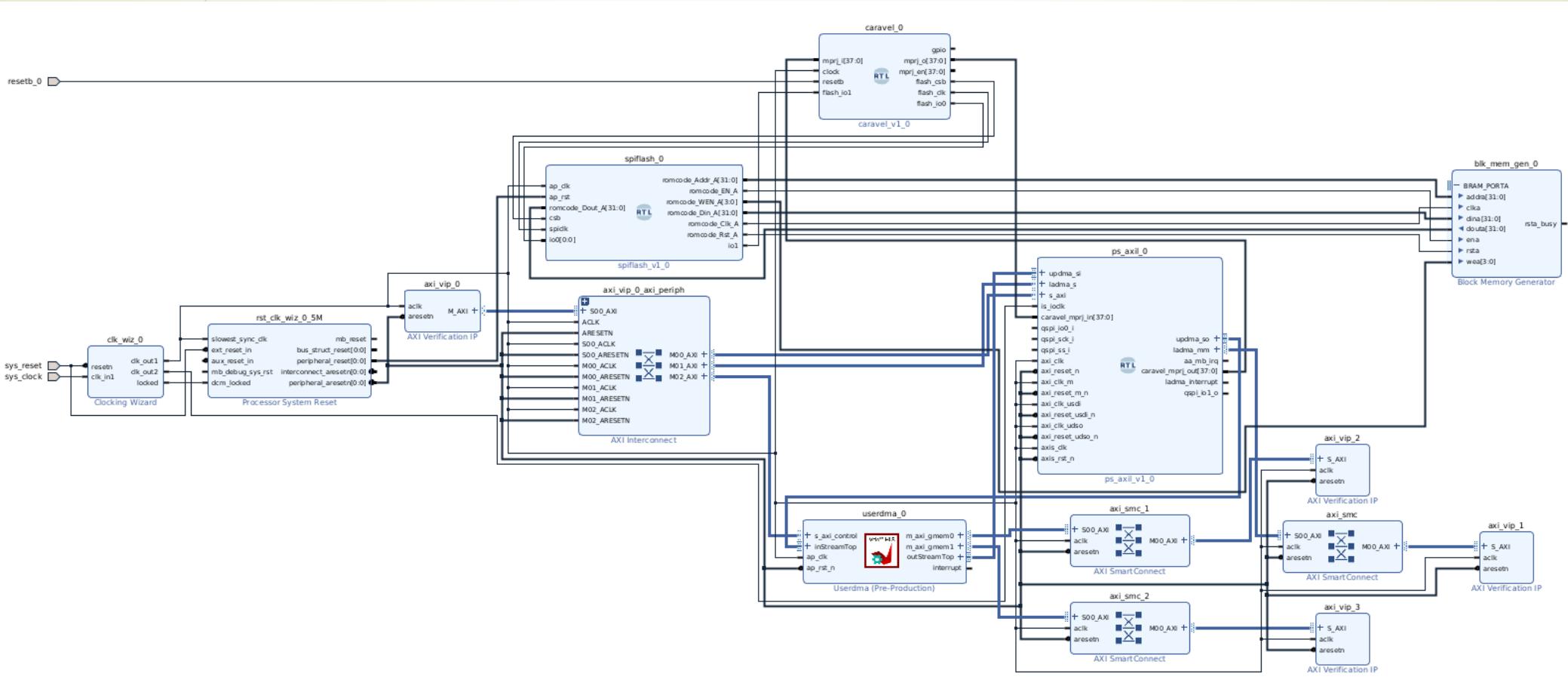


16356	00
16357	4c
16358	ff
16359	ba
16360	00

Result



Caravel-FSIC FPGA Simulation Block Design



Caravel-FSIC FPGA Simulation

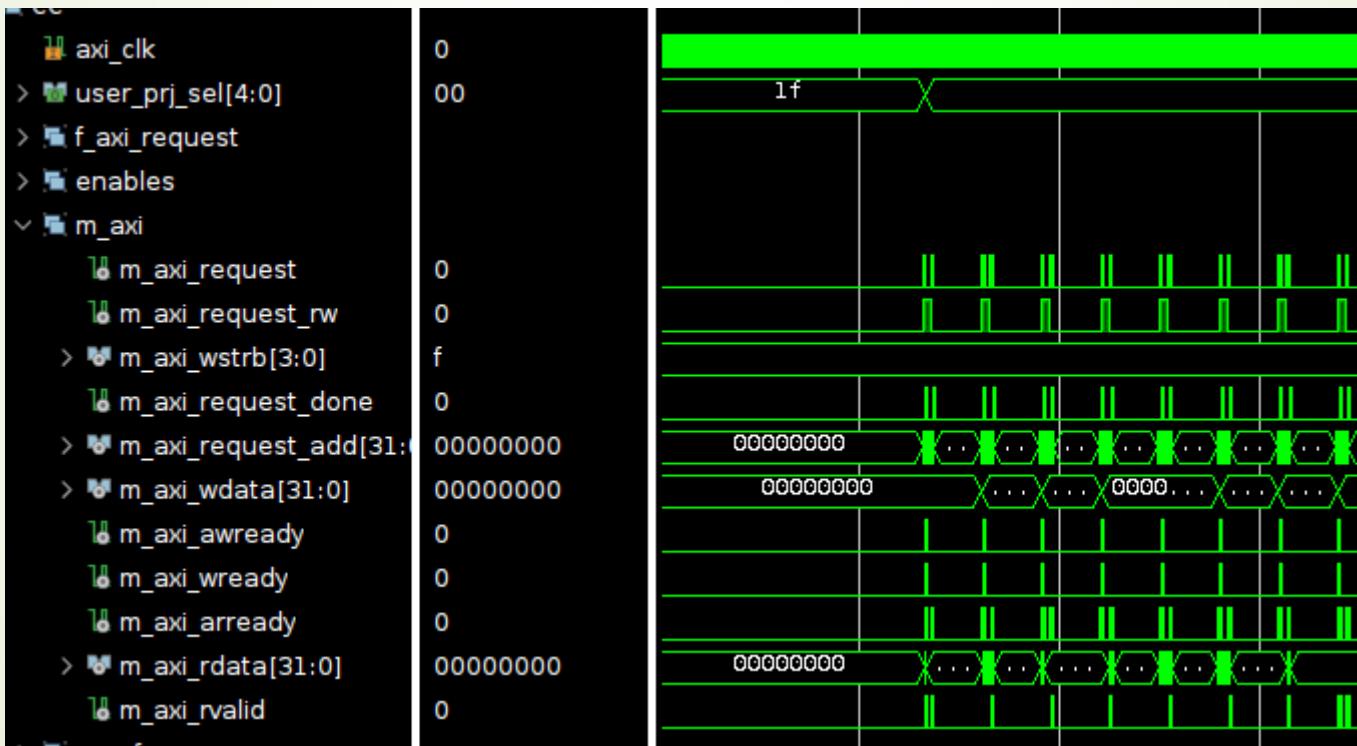
```
8225658=> AXI4LITE_WRITE_BURST 60000000, value: 0001, resp: 00
8237858=> AXI4LITE_READ_BURST 60000000, value: 0001, resp: 00
8237858=> Fpga2Soc_Write SOC_UP offset 000 = 00000001, PASS
8237858=> Fpga2Soc_Write: SOC_UP
8240458=> AXI4LITE_WRITE_BURST 60000000, value: 0000, resp: 00
8252658=> AXI4LITE_READ_BURST 60000000, value: 0000, resp: 00
8252658=> Fpga2Soc_Write SOC_UP offset 000 = 00000000, PASS
8252658=> Fpga2Soc_Write: SOC_UP
8255258=> AXI4LITE_WRITE_BURST 60000004, value: 0080, resp: 00
8267458=> AXI4LITE_READ_BURST 60000004, value: 0080, resp: 00
8267458=> Fpga2Soc_Write SOC_UP offset 004 = 00000080, PASS
8267458=> Fpga2Soc_Write: SOC_UP
8270058=> AXI4LITE_WRITE_BURST 60000008, value: 0080, resp: 00
8282258=> AXI4LITE_READ_BURST 60000008, value: 0080, resp: 00
8282258=> Fpga2Soc_Write SOC_UP offset 008 = 00000080, PASS
8282258=> Fpga2Soc_Write: SOC_UP
8284858=> AXI4LITE_WRITE_BURST 6000000c, value: 0000, resp: 00
8297058=> AXI4LITE_READ_BURST 6000000c, value: 0000, resp: 00
8297058=> Fpga2Soc_Write SOC_UP offset 00c = 00000000, PASS
8297058=> Fpga2Soc_Write: SOC_UP
8299658=> AXI4LITE_WRITE_BURST 60000010, value: 0002, resp: 00
8311858=> AXI4LITE_READ_BURST 60000010, value: 0002, resp: 00
8311858=> Fpga2Soc_Write SOC_UP offset 010 = 00000002, PASS
8311858=> Fpga2Soc_Write: SOC_UP
```

Caravel-FSIC FPGA Simulation

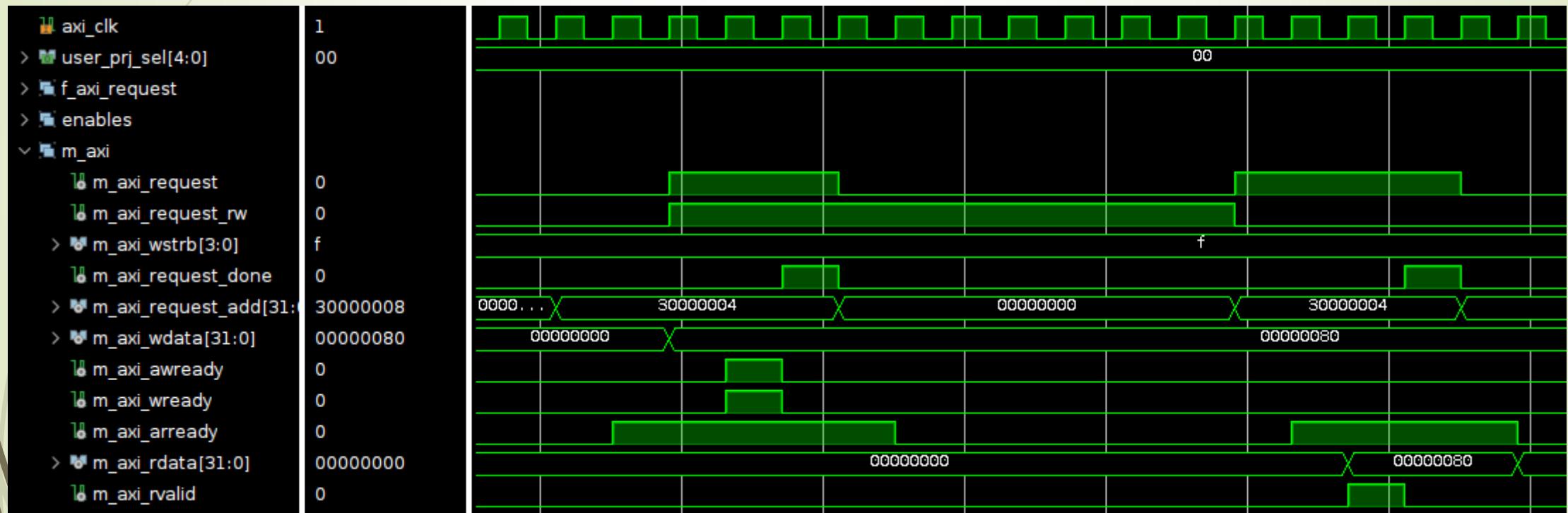
```
8328258=> Starting CheckuserDMADone()...
8328258=> =====
8328258=> FpgaLocal_Read: PL_UPDMA
8328258=> Waiting buffer transfer done...
```

```
38457258=> Buffer transfer done. offset 010 = 00000001, PASS
38457258=> End CheckuserDMADone()...
38457258=> =====
38457258=> End SocUp2DmaPath() test...
38457258=> =====
```

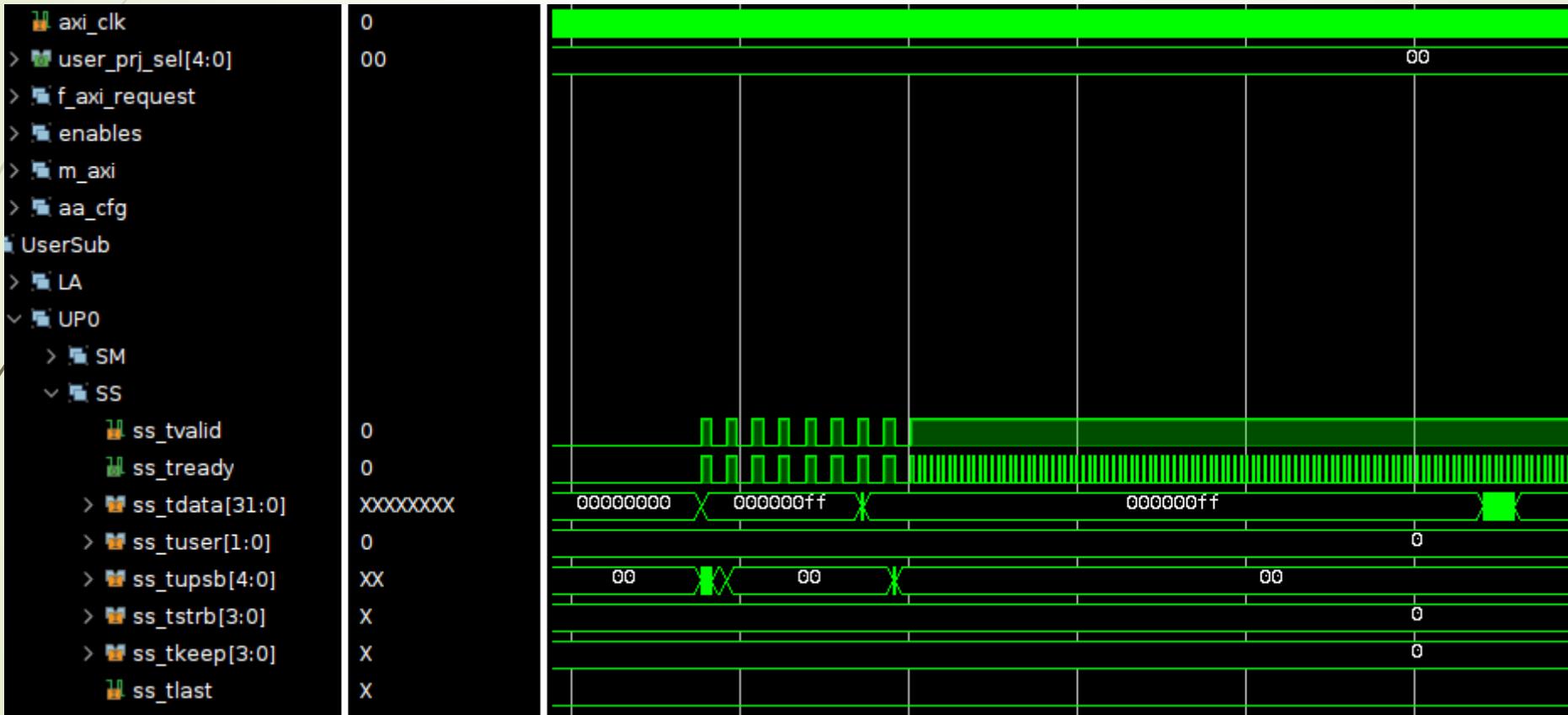
Caravel-FSIC FPGA Simulation



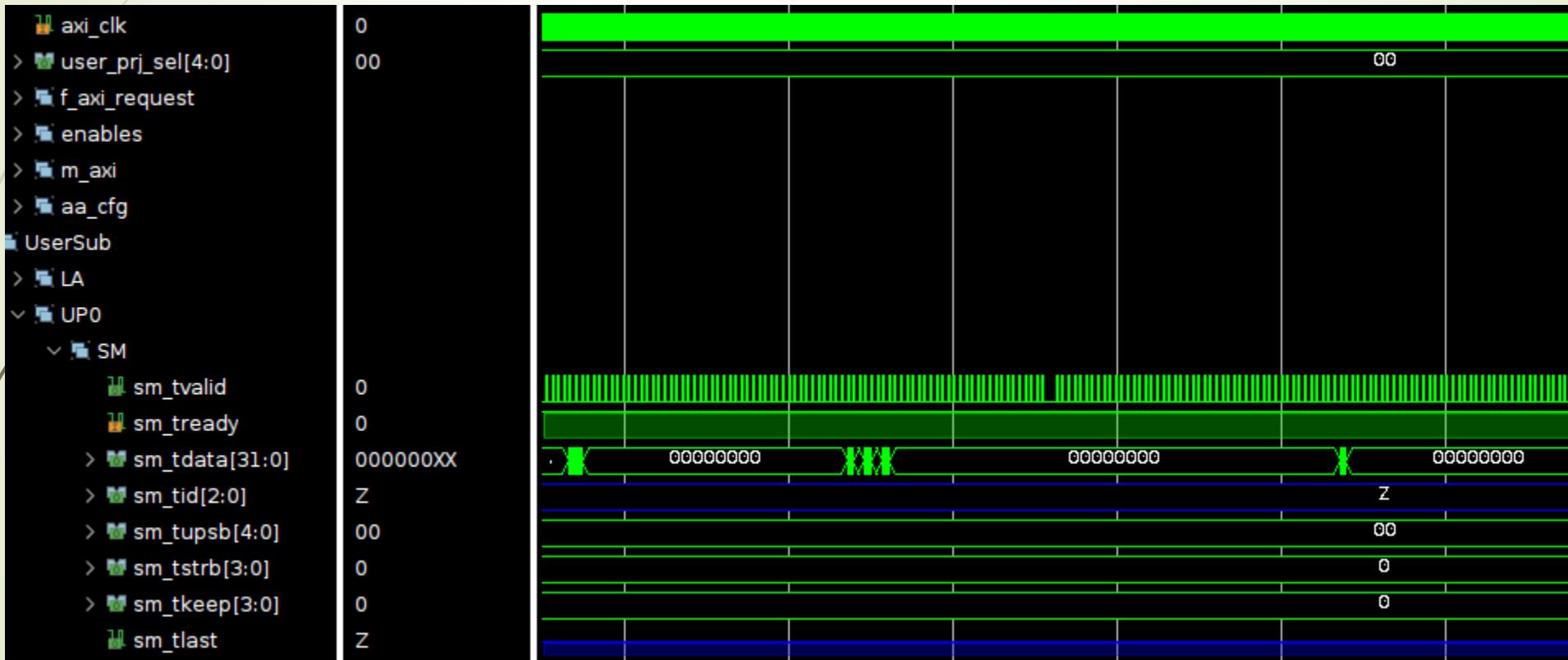
Caravel-FSIC FPGA Simulation



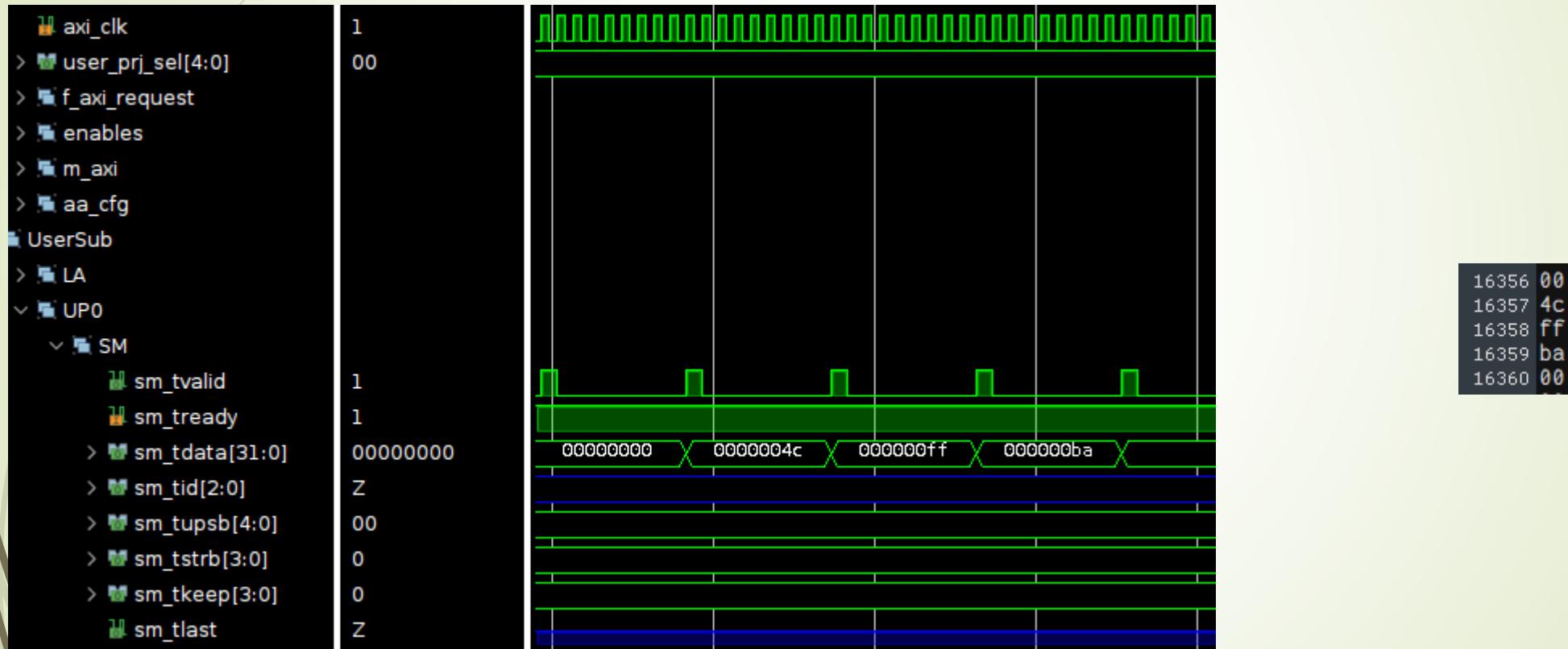
Caravel-FSIC FPGA Simulation



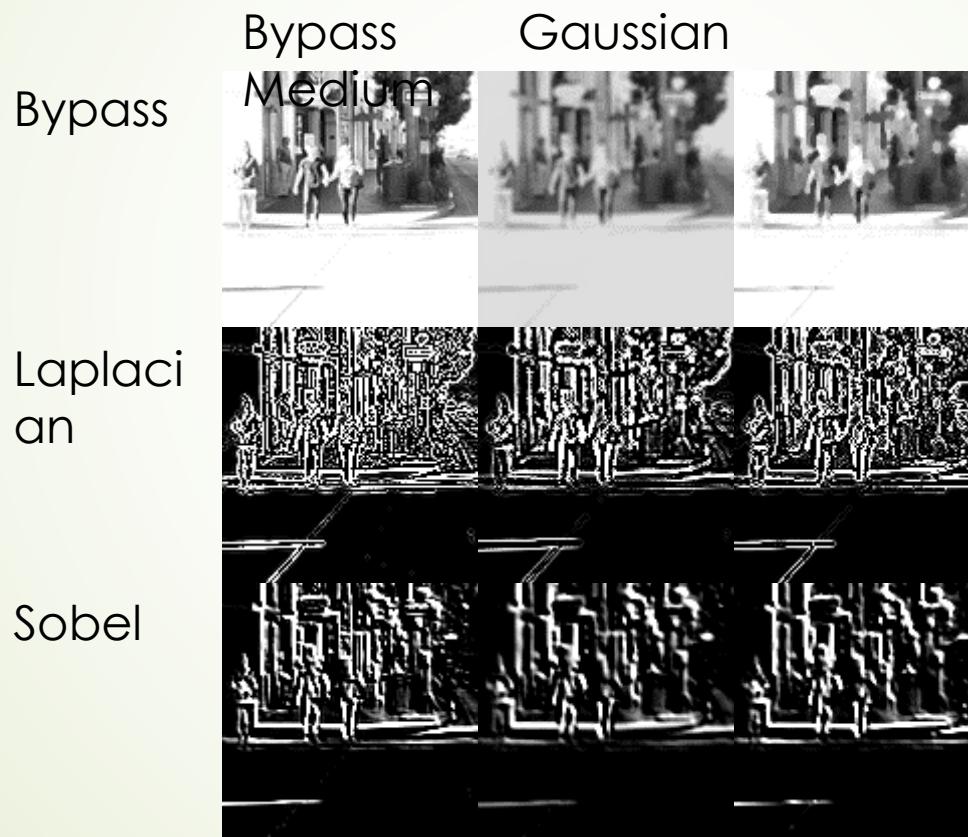
Caravel-FSIC FPGA Simulation



Caravel-FSIC FPGA Simulation



Result



Synopsys flow

► Synthesis

```
Optimization Complete
-----
1
## reporting and output
report_timing > ../../reports/timing_${DESIGN_NAME}_timing_reports.log
report_qor > ../../reports/timing_${DESIGN_NAME}_qor_reports.log
report_area -hierarchy > ../../reports/timing_${DESIGN_NAME}_area_reports.log
report_power -hierarchy > ../../reports/timing_${DESIGN_NAME}_power_reports.log
change_names -rules verilog
1
write_file -format verilog -hierarchy -pg -output ../../input/${DESIGN_NAME}.v
Warning: No PG information is available for design. (UPF-663)
Writing verilog file '/home/m111/m11061631/asc_lab3/lab_formal_release/input/EdgeDetect_IP_EdgeDetect_Top.v'.
Warning: Verilog writer has added 29 nets to module EdgeDetect_IP_Denoise_IP_run using SYNOPSYS_UNCONNECTED_ as prefix. Please use the change_names command to make the correct changes before invoking the verilog writer. (V0-11)
Warning: Verilog 'assign' or 'tran' statements are written out. (V0-4)
Warning: Verilog writer has added 26 nets to module EdgeDetect_IP_EdgeDetect_Filter_run using SYNOPSYS_UNCONNECTED_ as prefix. Please use the change_names command to make the correct changes before invoking the verilog writer. (V0-11)
1
quit

Memory usage for this session 324 Mbytes.
Memory usage for this session including child processes 324 Mbytes.
CPU usage for this session 24 seconds ( 0.01 hours ).
Elapsed time for this session 290 seconds ( 0.08 hours ).
```

Screenshot

```
module EdgeDetect_IP_Denoise_IP_ccs_sample_mem_ccs_ram_sync_singleport_rwport_en_6_16_10_648_648_16_5_gen (
    en, q, we, d, adr, adr_d, d_d, en_d, we_d, q_d,
    port_0_rw_ram_ir_internal_RMASK_B_d,
    port_0_rw_ram_ir_internal_WMASK_B_d);
input [15:0] q;
output [15:0] d;
output [9:0] adr;
input [9:0] adr_d;
input [15:0] d_d;
output [15:0] q_d;
input en_d, we_d, port_0_rw_ram_ir_internal_RMASK_B_d,
    port_0_rw_ram_ir_internal_WMASK_B_d;
output en, we;

SAEDRV14_BUFS_I U1 ( .A(adr_d[1]), .X(adr[1]) );
SAEDRV14_BUFS_I U2 ( .A(adr_d[2]), .X(adr[2]) );
SAEDRV14_BUFS_I U3 ( .A(adr_d[3]), .X(adr[3]) );
SAEDRV14_BUFS_I U4 ( .A(adr_d[4]), .X(adr[4]) );
SAEDRV14_BUFS_I U5 ( .A(adr_d[5]), .X(adr[5]) );
SAEDRV14_BUFS_I U6 ( .A(adr_d[6]), .X(adr[6]) );
SAEDRV14_BUFS_I U7 ( .A(adr_d[7]), .X(adr[7]) );
SAEDRV14_BUFS_I U8 ( .A(adr_d[8]), .X(adr[8]) );
SAEDRV14_BUFS_I U9 ( .A(adr_d[9]), .X(adr[9]) );
SAEDRV14_BUFS_I U10 ( .A(adr_d[0]), .X(adr[0]) );
SAEDRV14_BUFS_I U11 ( .A(d_d[0]), .X(d[0]) );
SAEDRV14_BUFS_I U12 ( .A(d_d[1]), .X(d[1]) );
SAEDRV14_BUFS_I U13 ( .A(d_d[2]), .X(d[2]) );
SAEDRV14_BUFS_I U14 ( .A(d_d[3]), .X(d[3]) );
SAEDRV14_BUFS_I U15 ( .A(d_d[4]), .X(d[4]) );
SAEDRV14_BUFS_I U16 ( .A(d_d[5]), .X(d[5]) );
SAEDRV14_BUFS_I U17 ( .A(d_d[6]), .X(d[6]) );
SAEDRV14_BUFS_I U18 ( .A(d_d[7]), .X(d[7]) );
SAEDRV14_BUFS_I U19 ( .A(d_d[15]), .X(d[15]) );
SAEDRV14_BUFS_I U20 ( .A(port_0_rw_ram_ir_internal_WMASK_B_d), .X(we) );
```

netlist

Synopsys flow

► Planning

```
Maximum memory usage for this session: 359.68 MB  
Maximum memory usage for this session including child processes: 715.13 MB  
CPU usage for this session: 22 seconds ( 0.01 hours)  
Elapsed time for this session: 591 seconds ( 0.16 hours)  
Thank you for using IC Compiler II.  
date > step1_data_setup
```

data_setup

```
Maximum memory usage for this session: 649.85 MB  
Maximum memory usage for this session including child processes: 649.85 MB  
CPU usage for this session: 33 seconds ( 0.01 hours)  
Elapsed time for this session: 646 seconds ( 0.18 hours)  
Thank you for using IC Compiler II.  
date > step2_floorplan
```

floorplan

```
#####
#Save_
Block
save_block -as ${DESIGN_NAME}_3_powerplan_ends
Information: Saving 'EdgeDetect_IP_EdgeDetect_Top:temp_floorplan_ends.design' to 'EdgeDetect_IP_EdgeDetect_Top:EdgeDetect_IP_EdgeDetect_Top_3_powerplan_ends.design'. (DES-028)
1
save_lib
Saving library 'EdgeDetect_IP_EdgeDetect_Top'
1
close_block
Information: Decrementing open count of block 'EdgeDetect_IP_EdgeDetect_Top:temp_floorplan_ends.design' to 1. (DES-022)
1
close_lib
Closing library 'EdgeDetect_IP_EdgeDetect_Top'
1
exit
Maximum memory usage for this session: 348.37 MB
Maximum memory usage for this session including child processes: 348.37 MB
CPU usage for this session: 27 seconds ( 0.01 hours)
Elapsed time for this session: 614 seconds ( 0.17 hours)
Thank you for using IC Compiler II.
date > step3_powerplan
date > all
```

powerplan

Synopsys flow

► Placing and Clock synthesis

```
#####
# Save Block
save_block -as ${DESIGN_NAME}_4_place_ends
Information: Saving 'EdgeDetect_IP_EdgeDetect_Top:temp_powerplan_ends.design' to 'EdgeDetect_IP_EdgeDetect_Top:EdgeDetect_IP_EdgeDetect_Top_4_place_ends.design'. (DES-028)
1
save_lib
Saving library 'EdgeDetect_IP_EdgeDetect_Top'
1
#####
close_block
Information: Decrementing open_count of block 'EdgeDetect_IP_EdgeDetect_Top:temp_powerplan_ends.design' to 1. (DES-022)
1
close_lib
Closing library 'EdgeDetect_IP_EdgeDetect_Top'
Information: The net parasitics of block EdgeDetect_IP_EdgeDetect_Top are cleared. (TIM-123)
1
exit
Maximum memory usage for this session: 715.53 MB
Maximum memory usage for this session including child processes: 715.53 MB
CPU usage for this session: 141 seconds ( 0.04 hours)
Elapsed time for this session: 890 seconds ( 0.25 hours)
Thank you for using IC Compiler II.
date > step4 place
```

placing

```
#####
# Save Block
save_block -as ${DESIGN_NAME}_5_clock_ends
Information: The command 'save_block' cleared the undo history. (UNDO-016)
Information: Saving 'EdgeDetect_IP_EdgeDetect_Top:temp_place_ends.design' to 'EdgeDetect_IP_EdgeDetect_Top:EdgeDetect_IP_EdgeDetect_Top_5_clock_ends.design'. (DES-028)
1
save_lib
Saving library 'EdgeDetect_IP_EdgeDetect_Top'
1
close_block
Information: Decrementing open_count of block 'EdgeDetect_IP_EdgeDetect_Top:temp_place_ends.design' to 1. (DES-022)
1
close_lib
Closing library 'EdgeDetect_IP_EdgeDetect_Top'
Information: The net parasitics of block EdgeDetect_IP_EdgeDetect_Top are cleared. (TIM-123)
1
exit
Maximum memory usage for this session: 1241.62 MB
Maximum memory usage for this session including child processes: 1241.62 MB
CPU usage for this session: 340 seconds ( 0.09 hours)
Elapsed time for this session: 1159 seconds ( 0.32 hours)
Thank you for using IC Compiler II.
date > step5 clock tree synthesis
```

clock tree

Synopsys flow

► Routing

```
A detailed stack trace has been captured in /home/m111/m111061631/asoc_lab3/lab_formal_release/lab2_pnr/work/Synopsys_stack_trace_18692.txt.
```

The tool has just encountered a fatal **error**:

If you encountered this fatal **error** when **using** the most recent Synopsys release, submit the above stack trace and a test case that reproduces the **problem** to the Synopsys Support Center by **using** Enter A Call at <http://solvnet.synopsys.com/EnterACall>.

* **For** information about the latest software releases, go to the Synopsys SolvNet Release Library at <http://solvnet.synopsys.com/ReleaseLibrary>.

* **For** information about required Operating System patches, go to <http://www.synopsys.com/support>

Fatal: Internal system **error**, cannot recover.

Error code=6

```
Release = 'R-2020.09-SP3' Architecture = 'linux64' Program = 'IC Compiler II'  
Exec = '/usr/cadtool/cad/synopsys/icc2/2020.09-sp3/linux64/nwtn/bin/dgcom_exec'
```

```
'533868330 48010806371328 48010806371207 48010806377080 48010392550381 48010392216982 48010392212969 48010392215349 48010804022481 48010804024558 48010434873940 48010434809740  
455750428 455886883 582897498 582663053 626480197 626499846 582786398 582577399 582612714 582663053 626480197 626499846 582647833 582659639 565102098 565119299 6611856 6623769  
48010806289749 27689489'
```

```
A snapshot of runtime data has been captured in /home/m111/m111061631/asoc_lab3/lab_formal_release/lab2_pnr/work/crte_000018692.txt
```

Synopsys flow

► starRC

```
Setup           Elp=00:00:25 Cpu=00:00:01 Usr=1.6      Sys=0.0      Mem=539.8
Layers          Elp=00:00:00 Cpu=00:00:00 Usr=0.0      Sys=0.0      Mem=539.8
HN              Elp=00:00:01 Cpu=00:00:00 Usr=0.2      Sys=0.0      Mem=546.0
Cells           Elp=00:00:01 Cpu=00:00:00 Usr=0.2      Sys=0.1      Mem=560.2
Translate        Elp=00:00:00 Cpu=00:00:00 Usr=0.1      Sys=0.0      Mem=551.8
NetlistSetup     Elp=00:00:00 Cpu=00:00:00 Usr=0.0      Sys=0.0      Mem=480.5
GPD_XtractSetup Elp=00:00:00 Cpu=00:00:00 Usr=0.0      Sys=0.0      Mem=540.1
GPD_NameMap     Elp=00:00:00 Cpu=00:00:00 Usr=0.0      Sys=0.0      Mem=481.0
xTract          Elp=00:00:08 Cpu=00:00:08 Usr=7.5       Sys=0.7      Mem=961.3
xTractPP        Elp=00:00:00 Cpu=00:00:00 Usr=0.0      Sys=0.0      Mem=338.8
ReportViolations Elp=00:00:00 Cpu=00:00:00 Usr=0.0      Sys=0.0      Mem=480.5
ReportOpens      Elp=00:00:00 Cpu=00:00:00 Usr=0.0      Sys=0.0      Mem=480.2
GPD_PostProcess Elp=00:00:00 Cpu=00:00:00 Usr=0.0      Sys=0.0      Mem=480.6
GPD_Converter1   Elp=00:00:01 Cpu=00:00:00 Usr=0.5       Sys=0.0      Mem=336.5
GPD_Converter2   Elp=00:00:00 Cpu=00:00:00 Usr=0.0      Sys=0.0      Mem=332.6
GPD_Converter_merge_c1 Elp=00:00:00 Cpu=00:00:00 Usr=0.0      Sys=0.0      Mem=332.5
GPD_Converter_merge_c2 Elp=00:00:00 Cpu=00:00:00 Usr=0.0      Sys=0.0      Mem=332.5

Done           Elp=00:00:36 Cpu=00:00:10 Usr=10.1     Sys=0.8      Mem=961.3
date > run_StarRC_cmd
date > all
```

Synopsys flow

► Primetime

```
Warning: Unable to resolve reference to 'SAEDRVT14_AOINV_IW_0P5' in 'EdgeDetect_IP_EdgeDetect_Top'. (LNK-005)
Error: Pin "VDDR" of cell "clockgre_a_INV_14_inst_2546" of reference "SAEDRVT14_AOINV_IW_0P5" in design "EdgeDetect_IP_Denoise_IP_run" is dirty because it
      does not exist in the reference block. (LNK-042)
Error: Too many ports on instance 'clockgre_a_INV_14_inst_2546' of 'SAEDRVT14_AOINV_IW_0P5' in 'EdgeDetect_IP_Denoise_IP_run'. (LNK-011)
Error: Pin "VDDR" of cell "clockgre_a_INV_14_inst_2547" of reference "SAEDRVT14_AOINV_IW_0P5" in design "EdgeDetect_IP_Denoise_IP_run" is dirty because it
      does not exist in the reference block. (LNK-042)
Error: Too many ports on instance 'clockgre_a_INV_14_inst_2547' of 'SAEDRVT14_AOINV_IW_0P5' in 'EdgeDetect_IP_Denoise_IP_run'. (LNK-011)
Error: Pin "VDDR" of cell "clockgre_a_INV_23_inst_2548" of reference "SAEDRVT14_AOINV_IW_0P5" in design "EdgeDetect_IP_Denoise_IP_run" is dirty because it
      does not exist in the reference block. (LNK-042)
Error: Too many ports on instance 'clockgre_a_INV_23_inst_2548' of 'SAEDRVT14_AOINV_IW_0P5' in 'EdgeDetect_IP_Denoise_IP_run'. (LNK-011)
Error: Pin "VDDR" of cell "clockgre_a_INV_23_inst_2549" of reference "SAEDRVT14_AOINV_IW_0P5" in design "EdgeDetect_IP_Denoise_IP_run" is dirty because it
      does not exist in the reference block. (LNK-042)
Error: Too many ports on instance 'clockgre_a_INV_23_inst_2549' of 'SAEDRVT14_AOINV_IW_0P5' in 'EdgeDetect_IP_Denoise_IP_run'. (LNK-011)
Error: Pin "VDDR" of cell "clockgre_a_INV_137_inst_2538" of reference "SAEDRVT14_AOINV_IW_0P5" in design "EdgeDetect_IP_Denoise_IP_run" is dirty because i
      t does not exist in the reference block. (LNK-042)
Error: Too many ports on instance 'clockgre_a_INV_137_inst_2538' of 'SAEDRVT14_AOINV_IW_0P5' in 'EdgeDetect_IP_Denoise_IP_run'. (LNK-011)
Error: Pin "VDDR" of cell "clockgre_a_INV_59_inst_2584" of reference "SAEDRVT14_AOINV_IW_0P5" in design "EdgeDetect_IP_EdgeDetect_Filter_run" is dirty bec
ause it does not exist in the reference block. (LNK-042)
Error: Too many ports on instance 'clockgre_a_INV_59_inst_2584' of 'SAEDRVT14_AOINV_IW_0P5' in 'EdgeDetect_IP_EdgeDetect_Filter_run'. (LNK-011)
Error: Pin "VDDR" of cell "clockgre_a_INV_55_inst_2541" of reference "SAEDRVT14_AOINV_IW_0P5" in design "EdgeDetect_IP_EdgeDetect_Filter_run" is dirty bec
ause it does not exist in the reference block. (LNK-042)
```

```
SAEDRVT14_AOINV_IW_0P5 clockgre_a_INV_14_inst_2547 (
    .A ( clockgre_a_INV_14_6 ) , .X ( clockgre_a_INV_14_7 ) , .VDD ( VDD ) ,
    .VDDR ( VDD ) , .VSS ( VSS ) ) ;
SAEDRVT14_AOINV_IW_0P5 clockgre_a_INV_23_inst_2548 (
    .A ( clockgre_a_INV_23_6 ) , .X ( clockgre_a_INV_23_7 ) , .VDD ( VDD ) ,
    .VDDR ( VDD ) , .VSS ( VSS ) ) ;
SAEDRVT14_AOINV_IW_0P5 clockgre_a_INV_23_inst_2549 (
    .A ( clockgre_a_INV_23_8 ) , .X ( clockgre_a_INV_23_9 ) , .VDD ( VDD ) ,
    .VDDR ( VDD ) , .VSS ( VSS ) ) ;
```

Caravel-FSIC FPGA validation

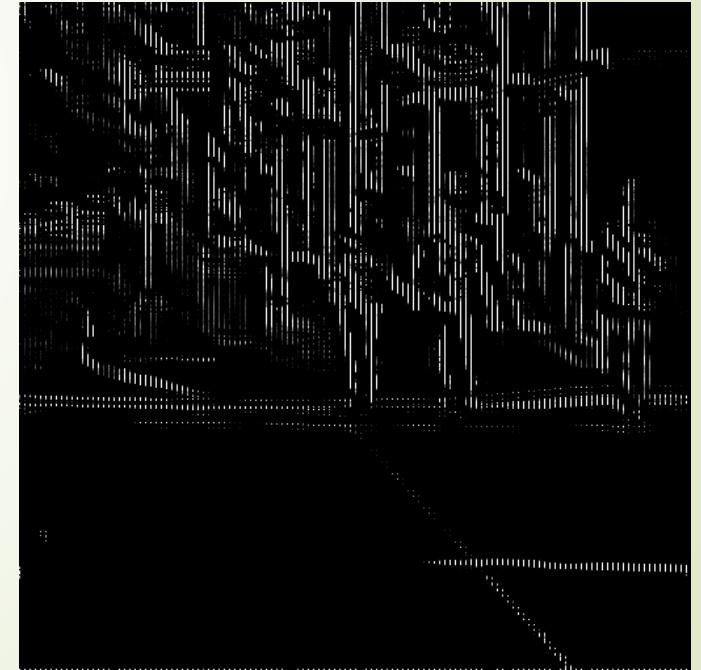
- ▶ We successfully integrated the Caravel-FSIC FPGA, and it operates as expected.
- ▶ Although the FPGA validation results matched the results from earlier simulations, they differed from the outcomes in the C_sim.



Input image with variation enhanced



Output of C_sim



Output of verilog sim and
FPGA validation

Caravel-FSIC FPGA simulation

► Possible Cause

The output from C_sim and validation appears different, revealing a potential issue with the line buffer usage in the Verilog code.

Additionally, the color level range of the output is not as wide as the C_sim result.

This inconsistency might result from the casting of floating-point values to integers during hardware computation.



Thank you