1. Intermediate status:

- **We haven't finished our application accelerator, because our target is the HDR ISP, which contains about 18 individual functional modules.**
- **We listed the status (for final project, including Lab 5 and Lab 6) in the table below:**
- **Note: Red text represents "update" status.**

Identify algorithm C-source code and run Catapult C-sim - 1w		
Tasks	**Person In Charge**	**Status**
Identify test dataset	蔡宗穎	Done. (With the help from 傑閔)
Run Catapult C-sim (pre-HLS verification)	張傑閔	Done.
Kernel HLS implementation, Host implementation - 3w		
Tasks	**Person In Charge**	**Status**
UNPACK	蔡宗穎 (proposal)	Done.
DEPWL		Done.
DPC		Done.
LSC		Done.
BLC		Done by 傑閔.
RNS(N/A)		N/A
WBGAIN		Done by 傑閔.
DEMOASIC		Working on it by 傑閔.
CCM		Done.
LTM	張傑閔 (proposal)	Working on it by 宗穎.
RGBGAMMA		Working on it.
RGBYUV		Working on it.
YGAMMA		Working on it.
CONTRAST		Working on it.
SHARPEN		Working on it.
CNS		Working on it.

SATURATION		Stuck.
YUV2RGB		Stuck.
HDR ISP Integration in Catapult/FSIC		
Tasks	**Person In Charge**	**Status**
HDR ISP HLS-C Top Integration & Catapult C/RTL co-sim	Under Discussion	Stuck.
HDR ISP Integration into FSIC	Under Discussion	Stuck.
Individual Kernel FPGA validation/integration test - 2w		
Tasks	**Person In Charge**	**Status**
FSIC Simulation	張傑閔	Stuck.
FSIC Validation	蔡宗穎	Stuck.
Synopsys Flow – 1w		
Tasks	**Person In Charge**	**Status**
Front-end (Logic Synthesis - DFT)	Under Discussion	Stuck.
Back-end (APR - Signoff)	Under Discussion	Stuck.