STARC Rules 第四部分

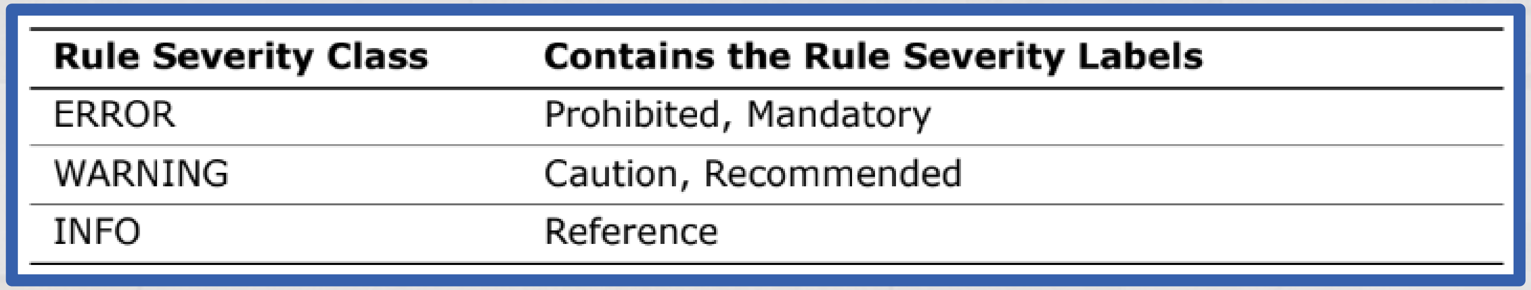
SpyGlass_STARCRules_Reference.pdf - Google 雲端硬碟

PDF P.676 - 845

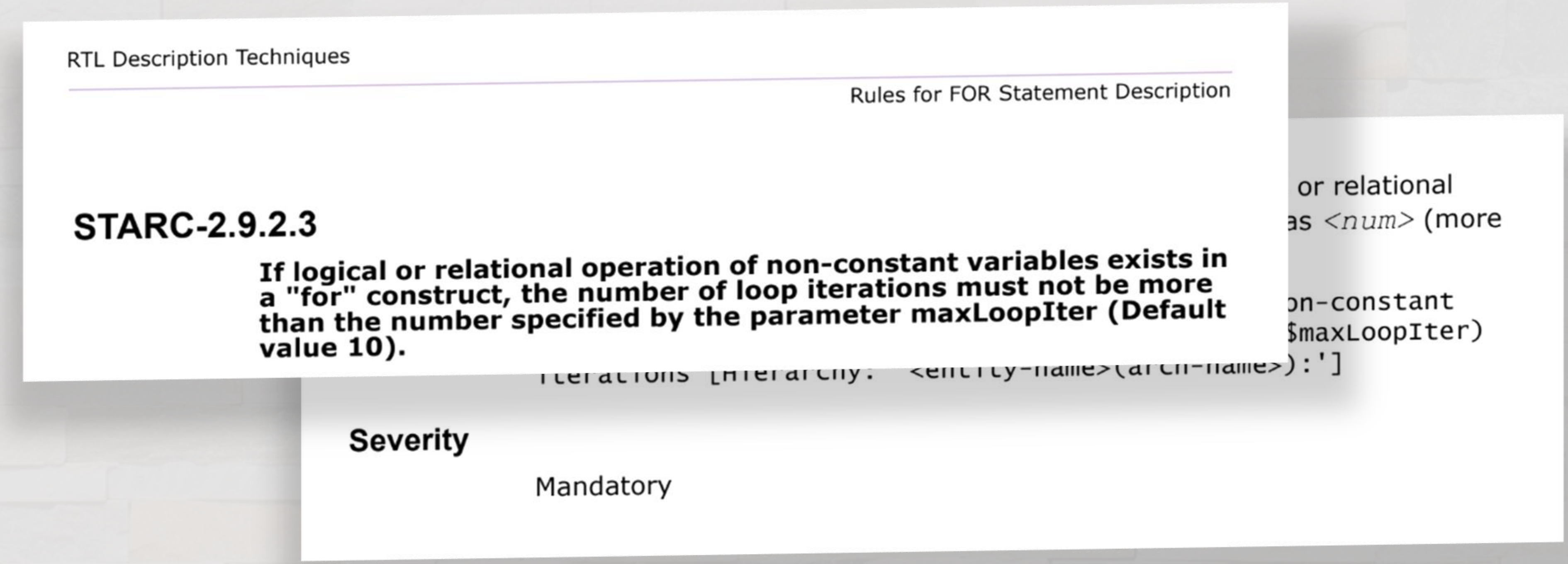
第4組 2023.8.9

Rule Severity Classes

PDF P.166



Rule Severity Class	Contains the Rule Severity Labels
ERROR	Prohibited, Mandatory
WARNING	Caution, Recommended
INFO	Reference



RTL Description Techniques

Rules for FOR Statement Description

STARC-2.9.2.3

If logical or relational operation of non-constant variables exists in a "for" construct, the number of loop iterations must not be more than the number specified by the parameter maxLoopIter (Default value 10).

or relational
as *<num>* (more

```
on-constant
$maxLoopIter)
iterations [Hierarchy: <entity-name>(arch-name>):']
```

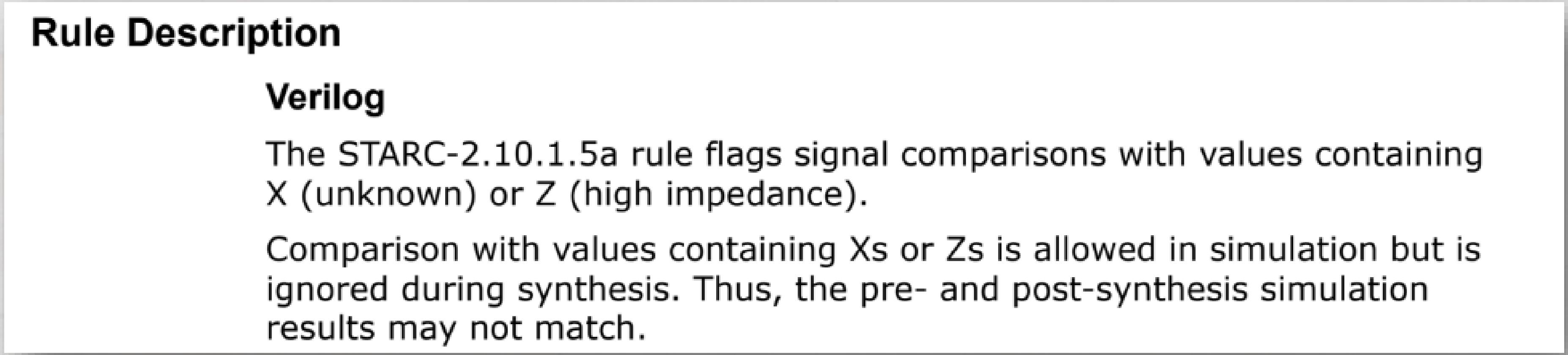
Severity

Mandatory

STARC-2.10.1.5a Mandatory Error

PDF P.679 - 680

- **Signals must not be compared with values containing X or Z. (Verilog)**
- **Comparisons must not be made with values including X and Z. (VHDL)**

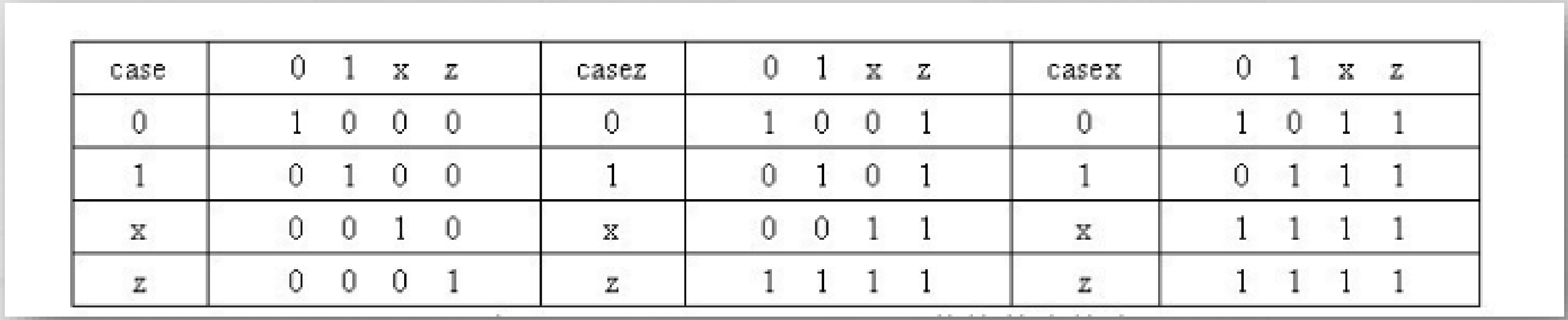


Rule Description

Verilog

The STARC-2.10.1.5a rule flags signal comparisons with values containing X (unknown) or Z (high impedance).

Comparison with values containing Xs or Zs is allowed in simulation but is ignored during synthesis. Thus, the pre- and post-synthesis simulation results may not match.

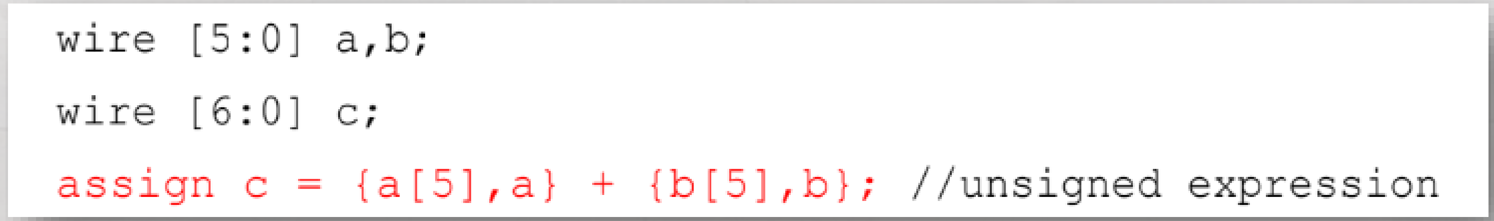


case	0 1 x z	casez	0 1 x z	casex	0 1 x z
0	1 0 0 0	0	1 0 0 1	0	1 0 1 1
1	0 1 0 0	1	0 1 0 1	1	0 1 1 1
x	0 0 1 0	x	0 0 1 1	x	1 1 1 1
z	0 0 0 1	z	1 1 1 1	z	1 1 1 1

STARC-2.10.3.2b Mandatory Error

PDF P.695 - 703

- **LHS and RHS bit-widths in signal assignments must match. (Verilog)**



```
wire [5:0] a,b;
wire [6:0] c;
assign c = {a[5],a} + {b[5],b}; //unsigned expression
```

STARC-2.10.3.3

PDF P.707

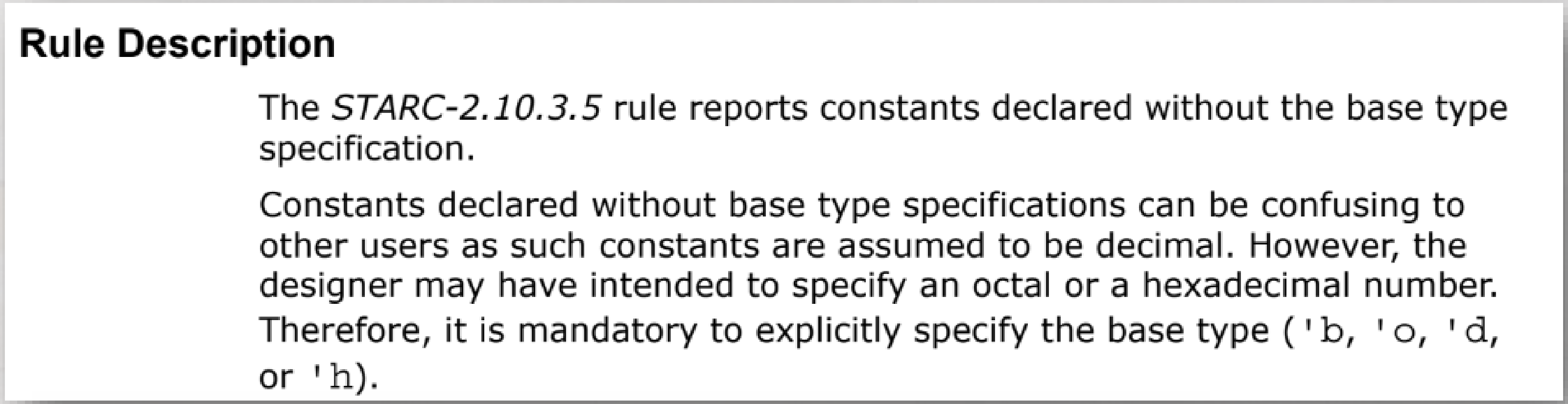
- **If the bit width of right side is wider than the left side, the remaining bits will be omitted. (Verilog)**

STARC-2.10.3.5

Mandatory Error

PDF P.709 - 710

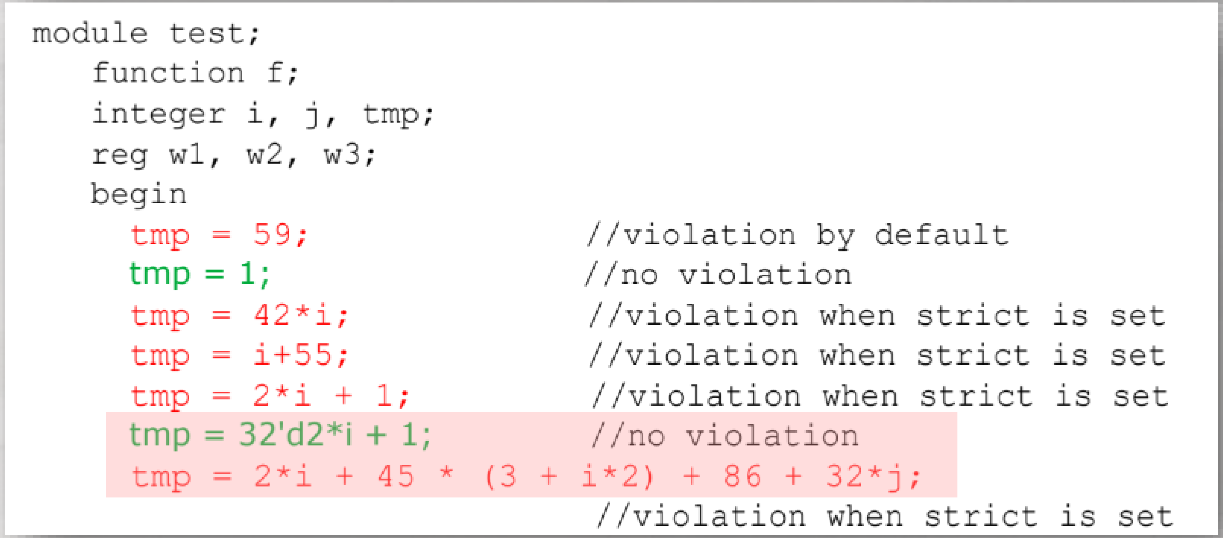
■ **Base should be specified for constant value used. (Verilog)**



Rule Description

The *STARC-2.10.3.5* rule reports constants declared without the base type specification.

Constants declared without base type specifications can be confusing to other users as such constants are assumed to be decimal. However, the designer may have intended to specify an octal or a hexadecimal number. Therefore, it is mandatory to explicitly specify the base type (`'b`, `'o`, `'d`, or `'h`).



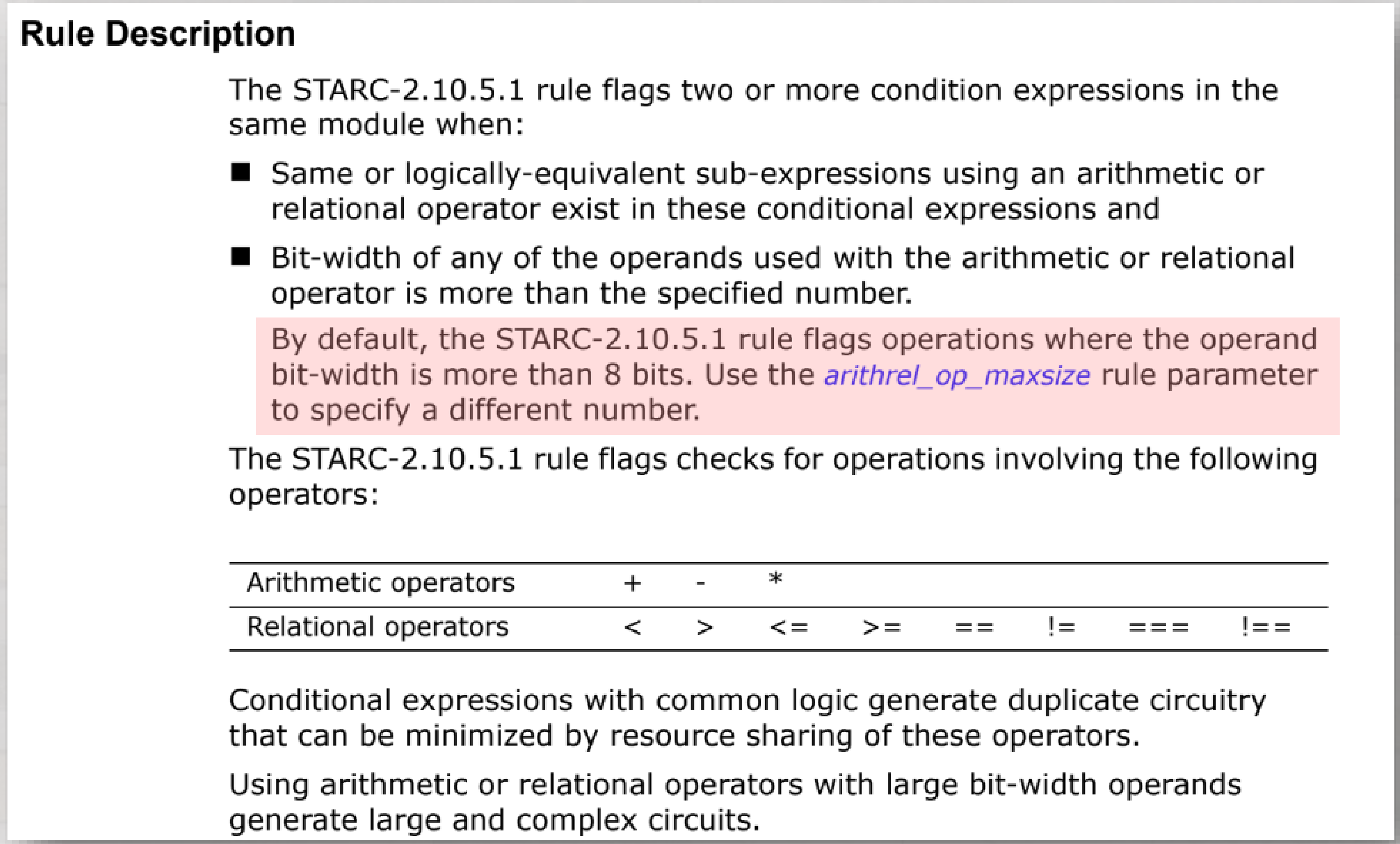
```
module test;
    function f;
    integer i, j, tmp;
    reg w1, w2, w3;
    begin
      tmp = 59;                //violation by default
      tmp = 1;                 //no violation
      tmp = 42*i;              //violation when strict is set
      tmp = i+55;              //violation when strict is set
      tmp = 2*i + 1;           //violation when strict is set
      tmp = 32'd2*i + 1;       //no violation
      tmp = 2*i + 45 * (3 + i*2) + 86 + 32*j;
                               //violation when strict is set
```

STARC-2.10.5.1

PDF P.719 - 721

Caution Warning

- **Arithmetic/relational operation with operand bit-width more than 8 in multiple conditional expressions is same. (Verilog)**



Rule Description

The STARC-2.10.5.1 rule flags two or more condition expressions in the same module when:

- Same or logically-equivalent sub-expressions using an arithmetic or relational operator exist in these conditional expressions and
- Bit-width of any of the operands used with the arithmetic or relational operator is more than the specified number.

  By default, the STARC-2.10.5.1 rule flags operations where the operand bit-width is more than 8 bits. Use the *arithrel_op_maxsize* rule parameter to specify a different number.

The STARC-2.10.5.1 rule flags checks for operations involving the following operators:

Arithmetic operators	+	-	*					
Relational operators	<	>	<=	>=	==	!=	===	!==

Conditional expressions with common logic generate duplicate circuitry that can be minimized by resource sharing of these operators.

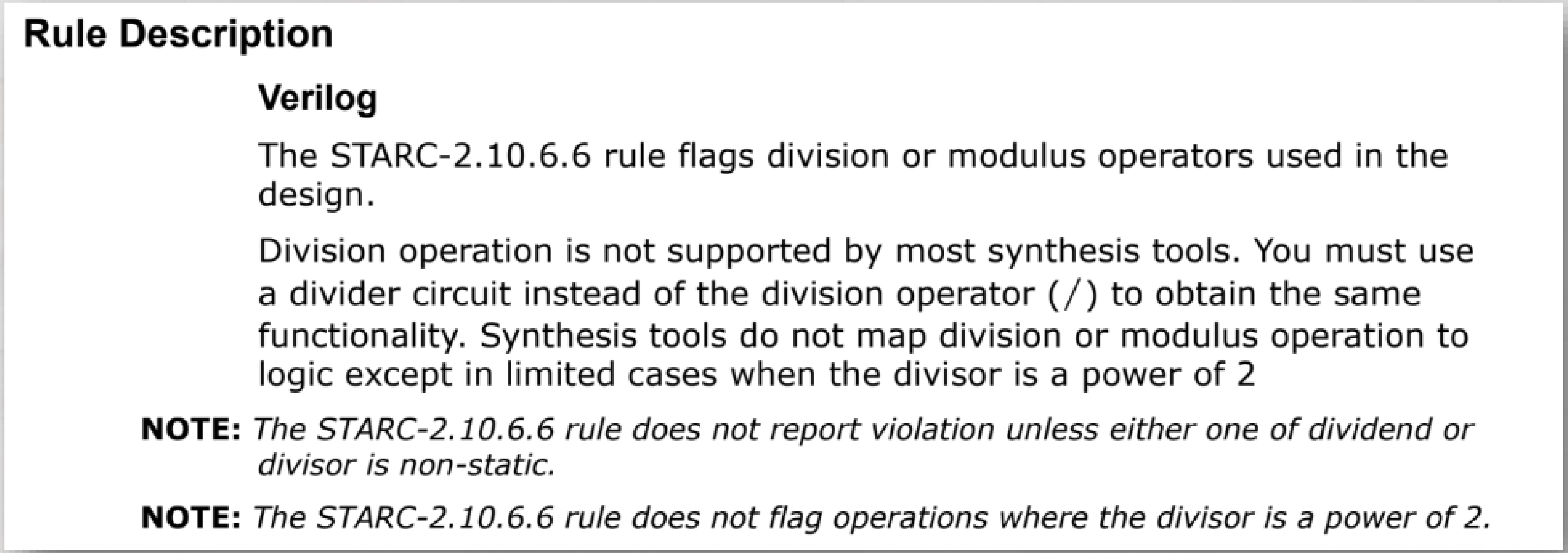
Using arithmetic or relational operators with large bit-width operands generate large and complex circuits.

STARC-2.10.6.6

Prohibited Error

PDF P.734 - 735

- **Do not use division operator or modulus operator. (Verilog)**
- **Do not use division, modulus or remainder operators in the design. (VHDL)**



Rule Description

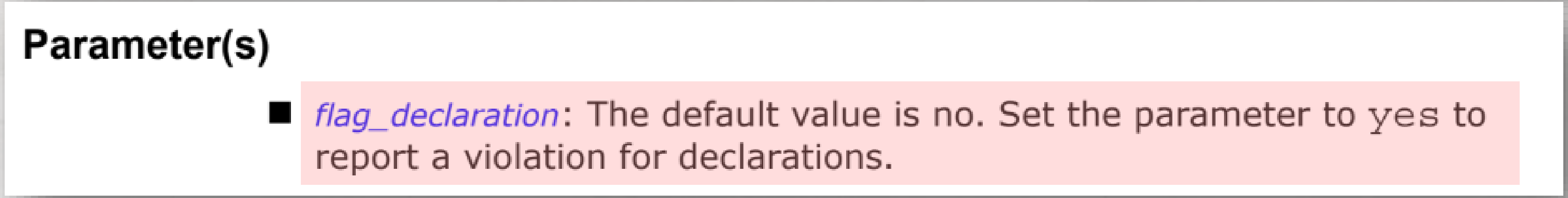
Verilog

The STARC-2.10.6.6 rule flags division or modulus operators used in the design.

Division operation is not supported by most synthesis tools. You must use a divider circuit instead of the division operator (/) to obtain the same functionality. Synthesis tools do not map division or modulus operation to logic except in limited cases when the divisor is a power of 2

NOTE: *The STARC-2.10.6.6 rule does not report violation unless either one of dividend or divisor is non-static.*

NOTE: *The STARC-2.10.6.6 rule does not flag operations where the divisor is a power of 2.*



Parameter(s)

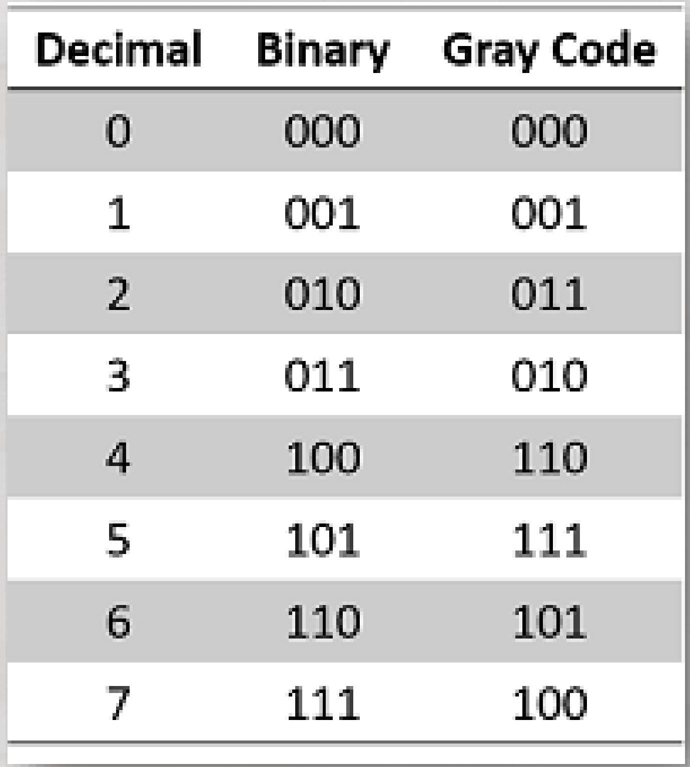
- *flag_declaration*: The default value is no. Set the parameter to `yes` to report a violation for declarations.

STARC-2.11.1.2

PDF P.741 - 742

Recommended Warning

- **Bit change in state transition should be minimal. (use Gray code) (Verilog)**
- **Constant construct should be used to define a FSM state value. (VHDL)**



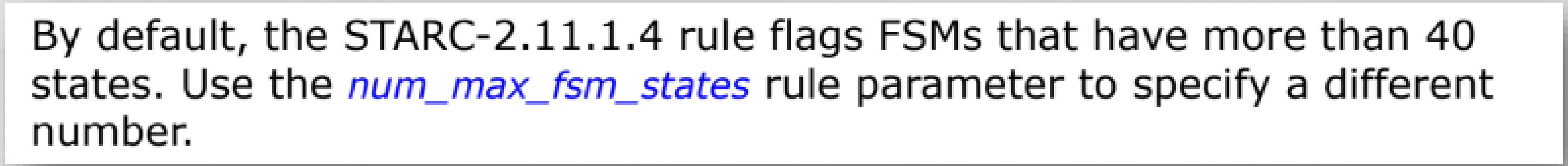
Decimal	Binary	Gray Code
0	000	000
1	001	001
2	010	011
3	011	010
4	100	110
5	101	111
6	110	101
7	111	100

STARC-2.11.1.4

PDF P.744

Mandatory Error

- **Number of states of an FSM should not exceed 40. (Verilog)**
- **Number of states in a FSM must be within 40. (VHDL)**



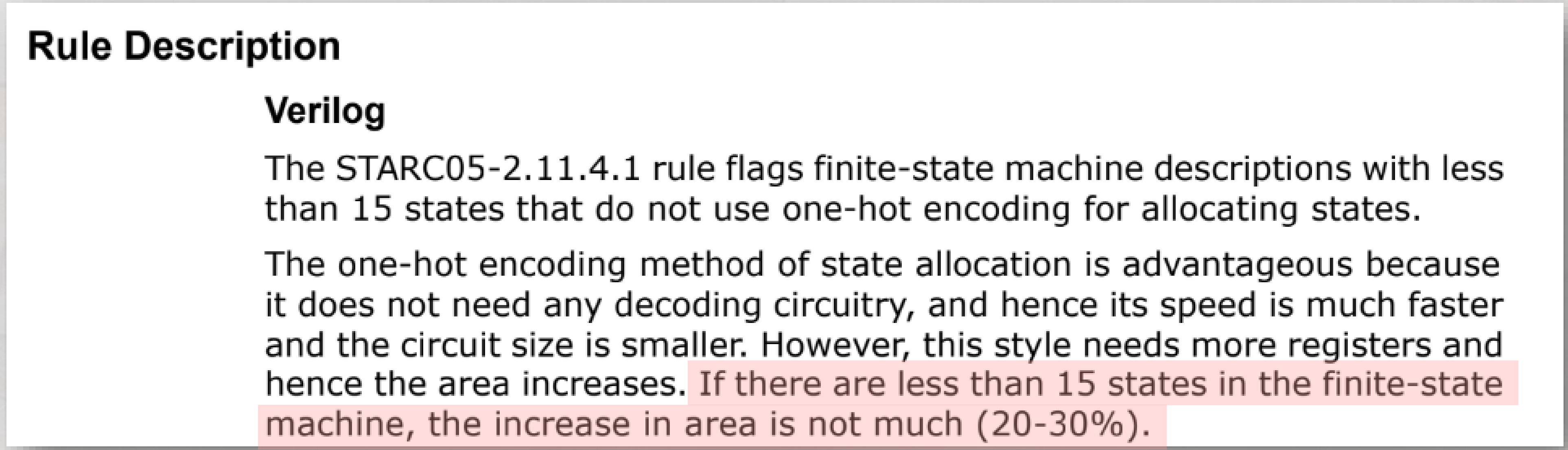
By default, the STARC-2.11.1.4 rule flags FSMs that have more than 40 states. Use the *num_max_fsm_states* rule parameter to specify a different number.

STARC-2.11.4.1

Recommended Warning

PDF P.755

■ **One-hot encoding should be used for allocating states.**



Rule Description

Verilog

The STARC05-2.11.4.1 rule flags finite-state machine descriptions with less than 15 states that do not use one-hot encoding for allocating states.

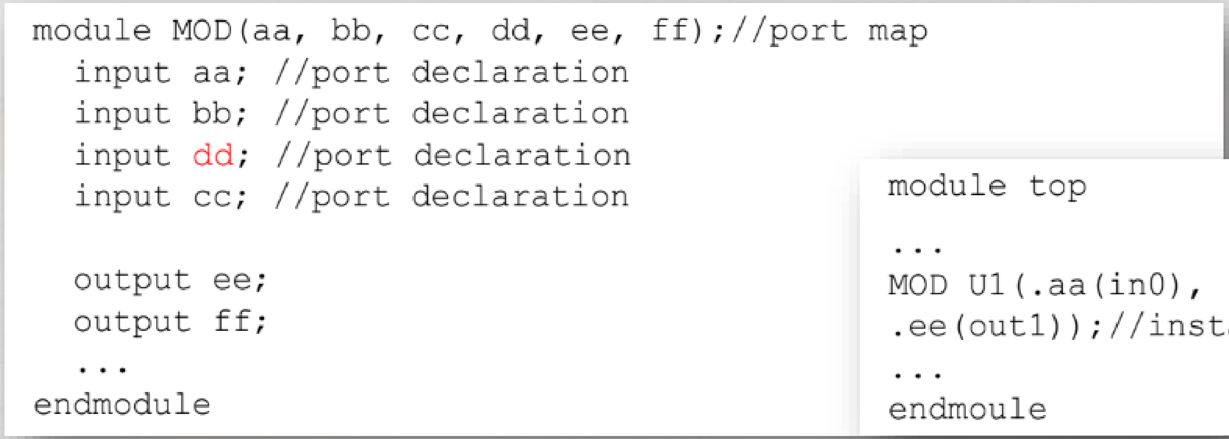
The one-hot encoding method of state allocation is advantageous because it does not need any decoding circuitry, and hence its speed is much faster and the circuit size is smaller. However, this style needs more registers and hence the area increases. If there are less than 15 states in the finite-state machine, the increase in area is not much (20-30%).

STARC-3.1.3.1

Recommended **Warning**

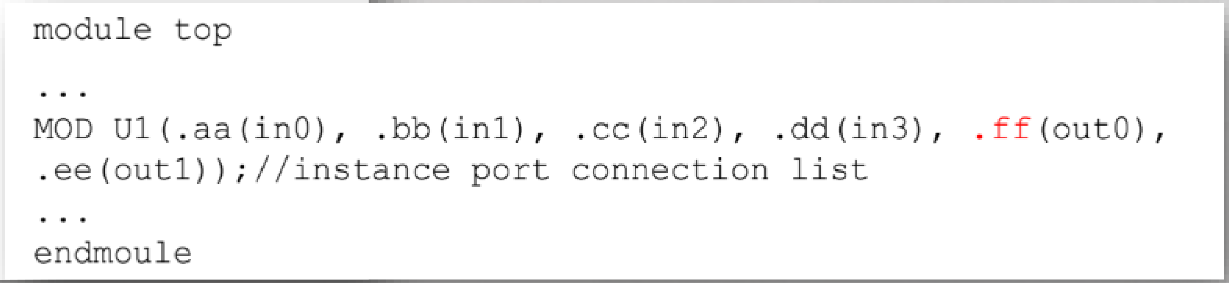
PDF P. 769 - 772

- **The order of module port declarations and instance port connection lists should be same as the order in the module port map. (Verilog)**



```
module MOD(aa, bb, cc, dd, ee, ff);//port map
  input aa; //port declaration
  input bb; //port declaration
  input dd; //port declaration
  input cc; //port declaration

  output ee;
  output ff;
  ...
endmodule
```



```
module top

...
MOD U1(.aa(in0), .bb(in1), .cc(in2), .dd(in3), .ff(out0),
.ee(out1));//instance port connection list
...
endmoule
```

STARC-3.1.3.2a

Recommended **Warning**

PDF P.774 - 775

- **Ports should be declared in recommended order**

- Input > Output > InOut
- Clock > Reset > Others

STARC-3.2.2.4

Mandatory Error

PDF P.801

- **Include files must be specified with relative path names. (Verilog)**

STARC-3.2.2.7

Recommended **Warning**

PDF P.804

- **Constants should be defined using parameters only. (Verilog)**
  - Method 1: Macros *[`define]*
  - ✓ Method 2: Parameters *[parameter]*

STARC-3.2.2.2

Recommended **Warning**

PDF P.799

- **Macros should be read using include files. (Verilog)**

STARC-3.2.2.3

Recommended **Warning**

PDF P.800

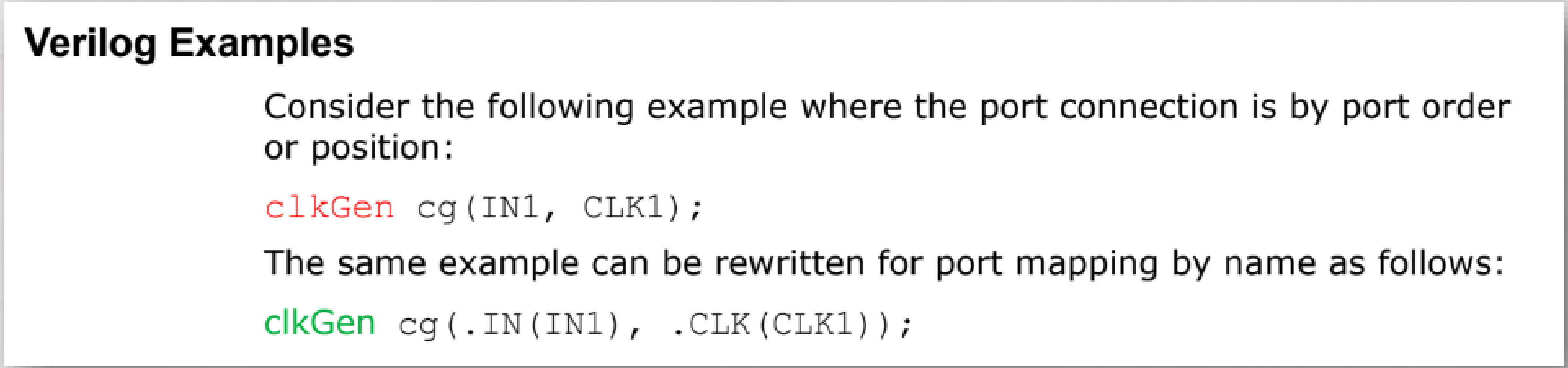
- **Parameters should be read using include files. (Verilog)**

STARC-3.2.3.1

PDF P.805 - 806

Mandatory Error

■ **Port connections in instantiations must be made by named association rather than positional association. (Verilog)**



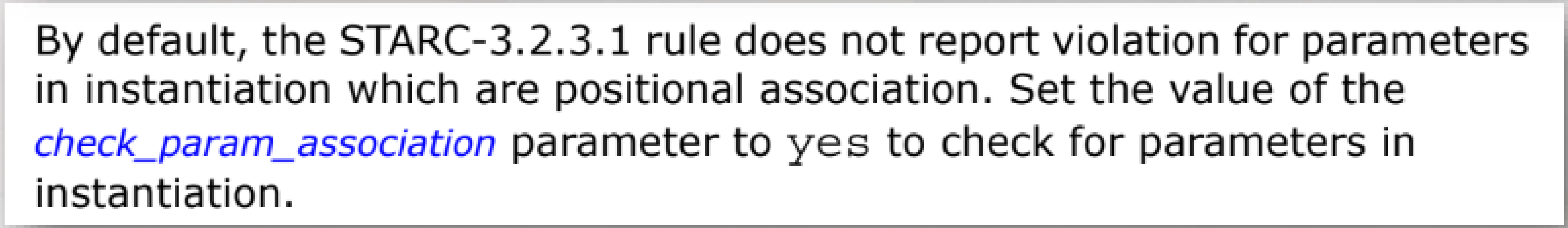
Verilog Examples

Consider the following example where the port connection is by port order or position:

```
clkGen cg(IN1, CLK1);
```

The same example can be rewritten for port mapping by name as follows:

```
clkGen cg(.IN(IN1), .CLK(CLK1));
```



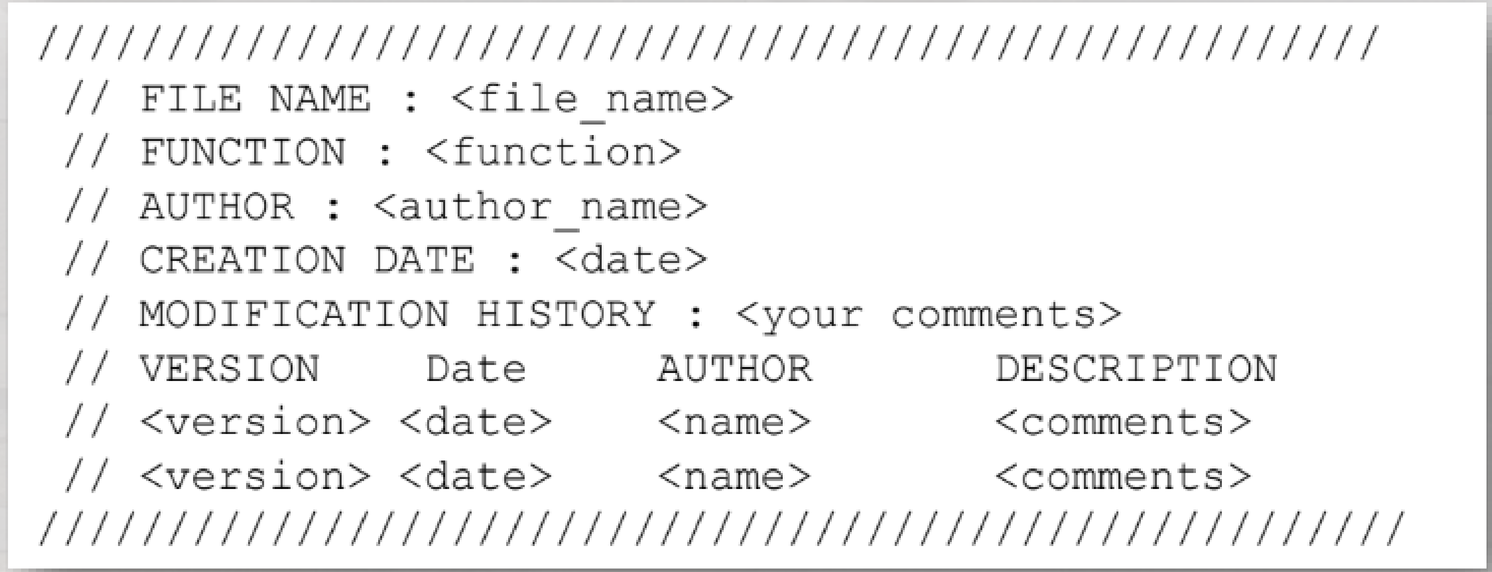
By default, the STARC-3.2.3.1 rule does not report violation for parameters in instantiation which are positional association. Set the value of the *check_param_association* parameter to `yes` to check for parameters in instantiation.

STARC-3.5.3.1

Recommended Warning

PDF P.830 - 831

- **A standard header should be provided in every source file.**



```
/////////////////////////////////////////////////////
 // FILE NAME : <file_name>
 // FUNCTION : <function>
 // AUTHOR : <author_name>
 // CREATION DATE : <date>
 // MODIFICATION HISTORY : <your comments>
 // VERSION    Date     AUTHOR       DESCRIPTION
 // <version> <date>    <name>       <comments>
 // <version> <date>    <name>       <comments>
//////////////////////////////////////////////////////
```

參數設定指令 set_parameter

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Rule Modifying

PDF P.36

Parameters

- assign_check
- ignore_qmark
- snakepath_ff

⋮

+

Value

- yes / no
- positive integer
- set of rule name

⋮

Activate
Modify

$\longrightarrow$

Rules

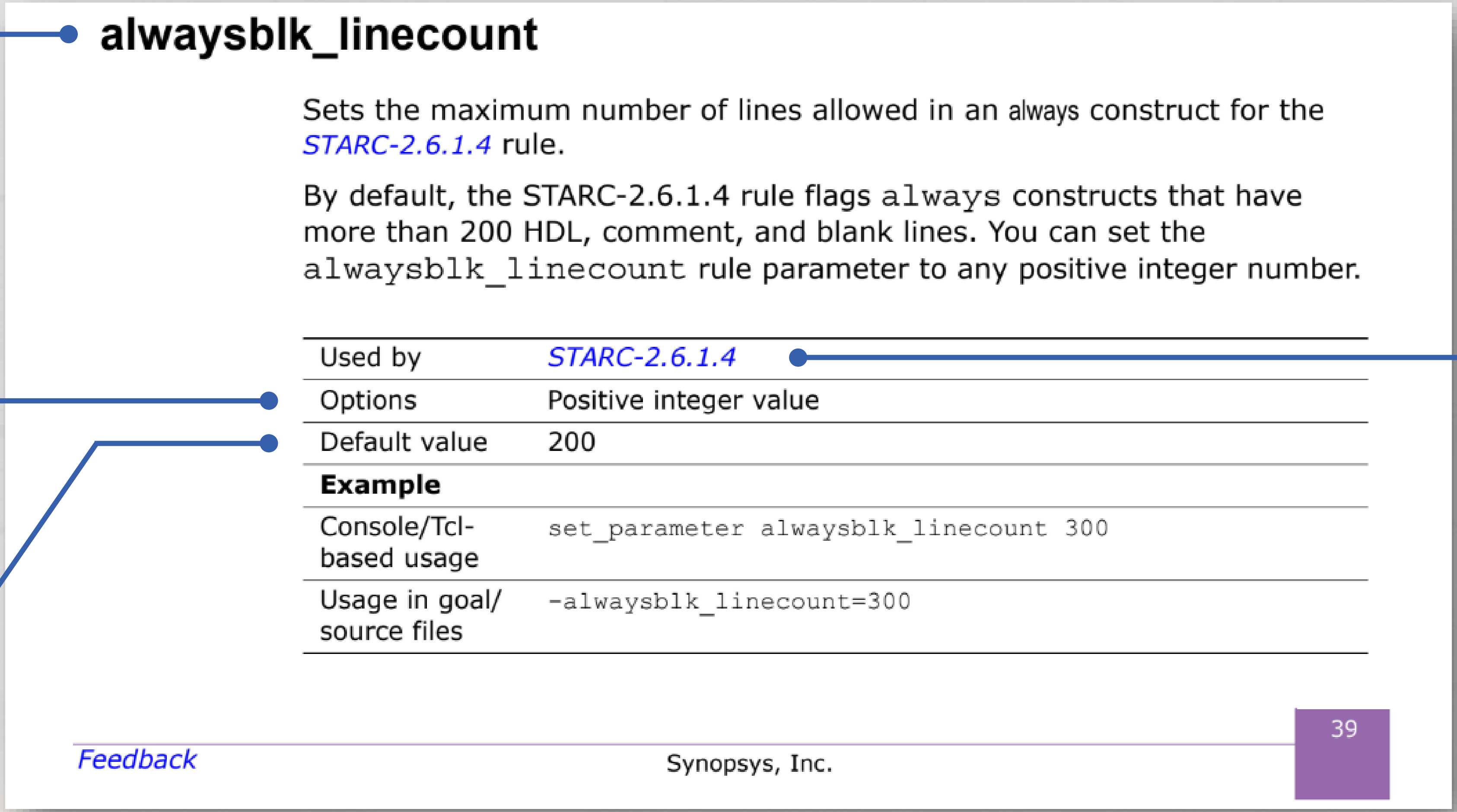
- STARC-1.5.1.1
- STARC-1.1.2.6b
- STARC02-2.7.3.5

⋮

- set_parameter <parameter_name> <parameter_value>

Parameter Dictionary

PDF P.36 - P.155



alwaysblk_linecount

Sets the maximum number of lines allowed in an always construct for the *STARC-2.6.1.4* rule.

By default, the STARC-2.6.1.4 rule flags `always` constructs that have more than 200 HDL, comment, and blank lines. You can set the `alwaysblk_linecount` rule parameter to any positive integer number.

Used by	*STARC-2.6.1.4*
Options	Positive integer value
Default value	200
Example	
Console/Tcl-based usage	`set_parameter alwaysblk_linecount 300`
Usage in goal/ source files	`-alwaysblk_linecount=300`

Feedback Synopsys, Inc. 39

Useful Parameter

PDF P.36 - P.155

- We chose about 40 useful or interesting parameters from total 189 parameters in the PDF

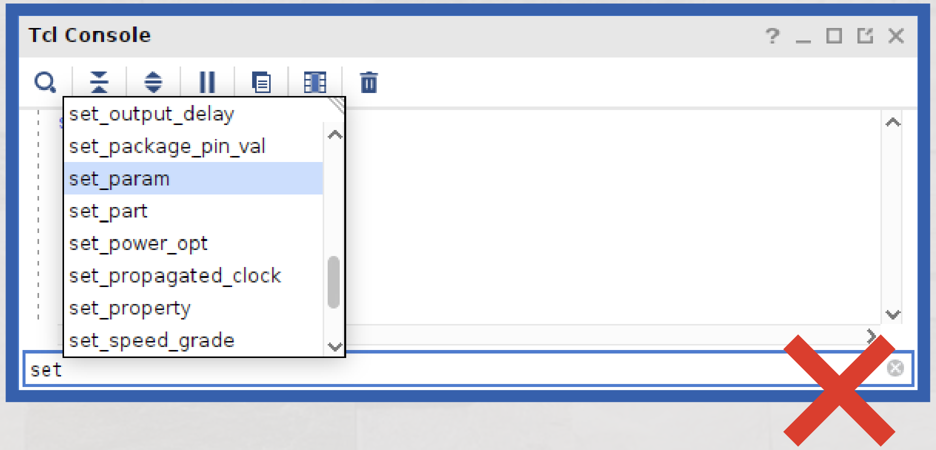
[統整表 - Google 試算表]

Question

① How to provide a standard header in development ?

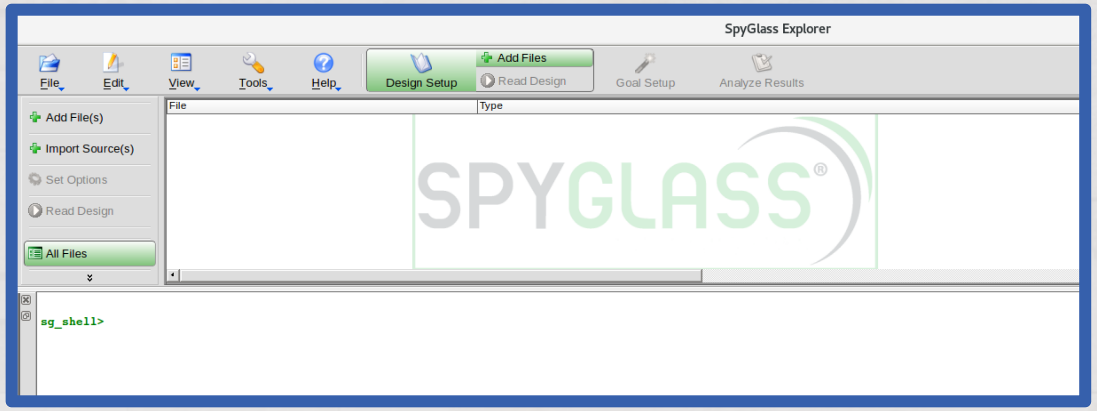
② Where to use those set_parameter comments ?

Vivado TCL console



```
set_output_delay
set_package_pin_val
set_param
set_part
set_power_opt
set_propagated_clock
set_property
set_speed_grade
set
```

SpyGlass Lint TCL console



```
sg_shell>
```