BRAND GUIDELINES

#### //01

# Lint Rules

Lintrules Group 3

Reports non-blocking assignments in a combinational block

### Potential Issues:

Violations may arise when a nonblocking assignment is used in a combinational block

# Debug/Fix:

Use only blocking assignments in combinational blocks

#### Example Code:

```
module group3(set, reset, vic, lukas);
         input set, reset;
         output vic, lukas;
         reg vic, lukas;
         always @(posedge vic) begin
             lukas <= set;
         end
         always @(set or reset) begin
             vic <= set & reset; // non-blocking assignments is used in
11
             lukas <= set | reset;</pre>
12
13
         end
14
15
     endmodule
```

Output port signal is being read

### Potential Issues:

Such modules could lead to an unintended feedback path from the instantiating post-module in the postsynthesis simulation while this issue is not apparent in the pre-synthesis simulation

# Debug/Fix:

Such models are not recommended for some test tools that need to handle inout ports

#### Example Code:

```
module group3(
   input in1,
   input in2,
   output reg out,
   output reg feedback
   );

assign out = in1 & in2; // The output "out" is read in the des
   assign feedback = out | in2;

endmodule
```

We cannot drive or assign reg type variables with an assign statement because a reg variable is capable of storing data and is not driven continuously.

Reg signals can only be driven in procedural blocks such as always and initial



Ensure that the signals or variables have consistent value

### Potential Issues:

The violation is reported arise when a variable or a signal is assigned in both blocking and non-blocking manner

# Debug/Fix:

#### Example Code:

```
1 reg [3:0] kenny;
2
3 kenny <= 1;
4 kenny = 2;
5 // kenny is assigned using both blocking and nonblocking assignments.
6 // Hence, a violation is reported in the case.</pre>
```

Ensure that all assignments to the same signal or variable are made in a consistent manner

# Function/Task

Function	Task
Can <b>not</b> have time-controlling statements- delay, and hence executes in the same simulation time unit	Can contain time-controlling statement/delay and may only complete at some other time
Can <b>not</b> enable a task, because of the above rule	Can enable othertasks and functions
Should have at least one input argument and cannot have <b>output</b> or <b>inout</b> arguments	Can have zero or more arguments of any type
Can return only a <b>single value</b>	Can <b>not</b> return a value, but can achieve the same effect using <b>output</b> argument

Recursive task enable

### Potential Issues:

This rule flags the task statement block, which has a call to task with the same name.

It also reports a message, if a task call is recursive through more than one task.

Ex: task\_0 calls task\_1 and task\_1 calls task\_0



# Debug/Fix:

In the case of recursive task enable, there is always a chance that two tasks call each other infinitely. Avoid such situations by using loop constructs or some alternate method of writing the code

#### Example Code:

```
module group 3(
         input in1,
         input in2,
         output reg out1
         );
         always @(in1 or in2) begin
             MyNameIsVic(out1, in1, in2); // Recursive task calls
         end
10
         task MyNameIsVic;
11
             output o2;
12
             input in1, in2;
13
14
15
              begin
                  MyNameIsVic( o2, in1, in2 ); // Recursive
16
17
              end
18
         endtask
19
20
     endmodule
```

Ensure that a task is not called inside a combinational block

### Potential Issues:

Since tasks may contain event controls, a task called inside a combinational always construct may turn that construct into a sequential always construct.

Violation may arise when a task is called in a combinational block.

# Debug/Fix:

To fix this violation, it is advisable to use functions, rather than tasks inside combinational blocks.

#### Example Code:

```
// No Violation, Task called from sequential block
     always @(posedge clk) begin
         MyNameIsVic(in, out1);
     end
     // Violation, Task called from combinational block
     always @(clk) begin
         MyNameIsVic(in, out1);
     end
10
     // Task
11
     task MyNameIsVic;
12
         input in;
13
14
         output out1;
15
         begin
             <task body>
16
17
         end
18
     endtask
```

Task called in a sequential block

### Potential Issues:

Since tasks may contain event controls, a task called inside a sequential always construct may unexpectedly create an implicit state machine which may not be synthesizable if the task uses different edges or clocks from the block in which it is instanced.

Therefore, while it is not an error to call a task inside a sequential always block, it should be handled with extra caution.

# Debug/Fix:

Nothing to fix if this is done right, but does suggest need for careful review.

#### Example Code:

```
module group3(in, out, clk);
         input [3:0] in;
         input clk;
         output [3:0] out;
         reg [3:0] out;
         reg [3:0] r1, r2, r3;
9
         always @(posedge clk) begin
             r1 = in - 1'b1;
10
11
             MyNameIsVic(r1, r2); // Call a task in sequential always construct
12
             out = r3;
13
         end
14
         task MyNameIsVic;
15
             <task_body>
16
         endtask
18
     endmodule
```

The width of return type and return value of a function should be the same

### Potential issues

#### WIDTH MISMATCH

A violation is reported when the return type width is lesser or greater than the width of the return value of a function.

#### RANGE MISMATCH

A violation is reported when there is an order mismatch between the return type and the return value in a function.

```
function logic [3:0] test_func ();
    // no-violation - widths are same, range are in same order
    logic [4:1] tmp;
    assign test_func = tmp;
5
    endfunction
    function logic [11:0] test_func ();
    // no-violation - widths are same
    logic [3:0] [2:0] tmp;
    return tmp;
    endfunction
```

```
function logic [2:0] [3:0] test_func (); // no-violation - widths are same
    logic [3:0] [2:0] tmp; // rule will not flag for 'swapped ranges'
3
    return tmp;
    endfunction
     function logic [5:0] test_func ();
 2
     logic [2:0] tmp;
     logic [4:0] tmp_2;
 4
     return tmp + tmp_2; // violation when nocheckoverflow yes
 5
     endfunction
```

```
function logic [4:0] test_func ();
    logic [2:0] tmp;
    logic [4:0] tmp_2;
    return tmp + tmp_2; // violation when nocheckoverflow no
5
    endfunction
    function logic signed [4:0] test_func ();
    logic signed [2:0] tmp;
    logic [4:0] tmp_2;
    return tmp + tmp_2; // violation - signed unsigned
    mismatch
    endfunction
```

```
function logic [2:0] test_func (); // no-violation
    return '0;
    endfunction
    function logic [0:2] test_func ();
    logic [2:0] tmp;
3
    return tmp; // violation - order mismatch - ranges are in
4
    reverse order
5
    endfunction
```

### W126~129

do not use delay values which is non-integer, negative, non-constant or containing X or Z.

```
1  out1 = # (8'h1x) in1;
2  integer i=0;
3  out2 = #i in;
```

Do not infer latches

# Suggested Fix

Check the inference to make sure it is what you intended. If not, prevent latch inferences by providing an explicit else clause at the end of the if statement, or default clause at the end of the case statement, to prevent inferring the latch.

```
1  process (reset, d)
2  begin
3  if (reset = '1') then
4  q <= d;
5  end if;
6  end process;</pre>
```

Verilog does not provide a method to check that a connection made to the inputs of a primitive gate (and, or, etc.) is of an appropriate width. If a wider bus is attached, the function simply expands to include the additional bits. This expansion can lead to unexpected behavior if the bus width changes as the design evolves. Thus it is safer to explicitly connect, bit-by-bit, those bits, which should be gated.

# Suggested Fix

Make connections bit-by-bit. For example, use and (b[0],b[1],b[2].) rather than and(b[0:3]).

Use this rule to identify the width mismatch between a module port and the net connected to the port of that module instance.

```
inst IN1 (.in1(a[2:0]+b[2:0]));
     // Width of expression, a[2:0]+b[2:0], will be 4 (7+7=14, 4 bits wide)
     inst IN2 (.in1(a[2:0]*b[2:0]));
     // Width of expression, a[2:0]*b[2:0], will be 6
 4
     inst IN3 (.in1(a1[2:0]*b1[2]));
     // Width of expression, a[2:0]*b1[2], will be 3
6
     inst IN4 (.in1(\{1'b0,a[2:0]\}));
     // Width is 3 bits (leading 0 ignored)
     inst IN5 (.in1({1'b1,a[2:0]}));
9
     // Width is 4 bits (1+3 bits)
10
```

Use named-association rather than positional association to connect to an instance

### W156

Do not connect buses in reverse order. Making reversed connections (for example, 15:0 connected to 0:15) is legal but bad design practice and may represent an error.

### W210

Number of connections made to an instance does not match number of ports on master

### W287a

Some inputs to the instance are not driven or unconnected

# Suggested Fix

If you don't care about the input value, tie it high or low, but do not let it float.

```
module test(in1, in2, clk, out1);
input in1, in2, clk;
output out1;
wire w1, w2;
assign w1 = in1 & in2;
and a1(out1, w1, w2);
// Undriven instance input 'w2'
endmodule
```

### W287c

Inout port of an instance is not connected or connected net is hanging

#### Potential Issues

• The W287c flags module or gate instances where inout ports are not connected or connected net is not used anywhere in the module

• Such descriptions are allowed, they are generally design mistakes. When in the input mode, an unconnected inout port is equivalent to an undriven input which is a design error in CMOS unless it is a pull-up or pull-down.

Tie the input high or low if it will not be used.

### W504

Integer is used in port expression

Do not use integers in port expression. Pass integer to lower level module by parameters.

• In the following example, the W504 rule reports violations because integer variable i and constant integer 2 are used in the expression of port a

```
module m;
integer i;
mm1 u1(.a(i));
mm1 u2(.a(2));
endmodule

module mm1(input a);
endmodule
```

# Synthesis Rules

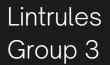
# badimplicitSM1

Identifies the sequential logic in a non-synthesizable modelling style where clock and reset cannot be inferred

#### Potential issues

Violation may arise when uncommon sequential logic is used, which is unsynthesizable.

Since the implicit modeling style is uncommon, it is most likely you made a mistake in modeling a conventional synchronous block. For a standard synchronous logic, it is neither required nor a good practice to use signals other than those present in the sensitivity list to set/reset the circuit.



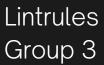
```
module bism1(set,reset,in1,in2,out1);
     input in1,in2,reset,set;
     output out1;
     reg clk,out1;
     always @(posedge clk or negedge set)
6
         if(reset)
             out1 = 0;
         else if(!set)
             out1 = 1;
         else if(in2)
             out1 = in2;
         else
14
             out1 = in1;
     endmodule
```

# badimplicitSM2

Identifies the implicit sequential logic in a non-synthesizable modeling style where states are not updated on the same clock phase

#### Potential issues

A register which is updated on both edges of a clock in a given sequential block leads to ambiguous synthesis results.



To resolve the violation, break the sequential logic into multiple sequential logic blocks, each of which can independently meet the requirement. If the register depends on both edges of the clock, describe the sequential nature separately and use the combinational logic to generate the final output.

In the following example code, SpyGlass reports a violation as the event control expressions use multiple edges.

```
1 always
2 begin
3           @(posedge a or negedge a) out1 <= in1;
4           @(negedge a) out2 <= in1;
5 end
6 endmodule</pre>
```

# badimplicitSM4

Identifies the non-synthesizable implicit sequential logic where event control expressions have multiple edges

#### Potential issues

- A violation is reported A register which is updated on both edges of a clock in a given sequential block leads to ambiguous synthesis results.
- The synthesis tool can get confused about which edge to use for updating the register.
- RTL and gate-level simulation results may not match.

To resolve the violation, break the sequential logic into multiple sequential logic blocks, each of which can independently meet the requirement.

In the following example code, SpyGlass generates a violation as the state depends on more than one edge of the clk clock:

```
module test(out1,out2);
output out1,out2;
reg out1,out2,a,c,clk;
always
begin
     @(posedge clk) out1 <= c; @(negedge clk) out2 <= a;
end
endmodule</pre>
```

# bothedges

Identifies the variable whose both the edges are used in an event control list

#### Potential issues

• A violation is reported when both edges of the same variable are used in an event control list, hence making the variable not synthesizable by some synthesis tools.

To resolve the violation, replicate the block, one switching on the positive edge and the other on the negative edge.

```
module test(q);
3
    output q;
    reg q,d,reset;
6
    always @(posedge reset or negedge reset)
      begin if (reset != 0)
        q = d;
9
      end
```

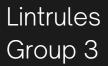
#### mixedsenselist

Mixed conditions in sensitivity list may not be synthesizable

# Rule Description

- The mixedsenselist rule flags mixed edge and non-edge conditions in the sensitivity list of an always construct.
- Such conditions in sensitivity list may not be synthesizable by some synthesis tools.

Decide if you really want to trigger the block on any change in the mixed signal. Check if your requirement can be met by mapping to either a positive-edge change or a negative-edge change. If both are required, consider duplicating the block, one triggering on each edge.



```
1 always @(posedge clock or reset)
2  q = d;
```