Bridge of Life Education

SOC Lab Implementation Project Plan

2023 Fall

Jiin Lai

Special Project Planning for Fall 2023

- Attending Wed 9:00 – 12:00 course session (台達 201)
- Register course EE 525100 “SOC Design” as Auditor to access course material
- Discussion session: Tuesday 6:00 – 8:00 pm (台達 208), Agenda
  - Course material Q & A
  - Key content from last week course material
  - Lab presentation

Lecture & Lab Schedule

week	Date	category	In Class: Lecture, Presentation	Lab	Lab Due
1st Semester					
1	**13-Sep**	**Intro**	Course plan / From Gate to HLS	Lab#1 - Tool installation (1w) - individual	20-Sep
2	**20-Sep**	**HLS**	PYNQ-Lab2 Software Hardware Codesign / HLS Introduction / Kernel IO / Structure Design	Lab#2 - FIR (stream/master) (1w) - individual	27-Sep
3	**27-Sep**	**Verilog**	Verilog and Logic Design	Lab#3- Verilog FIR & XSIM & GTKWave (2w) - individual	18-Oct
4	**4-Oct**	**Caravel**	Caravel SoC System Introduction		
5	**11-Oct**	**Processor**	Computer & Microprocessor Architecture - RISC-V	Lab#4-1 Caravel SOC - Management FW (1w) - team	25-Oct
6	**18-Oct**	**Peripheral**	SoC Peripherals - UART, SPI, I2C, GPIO, UserProject IO, DMA	Lab#4-2 Caravel User Project - FIR (1w) - team	1-Nov
7	**25-Oct**	**Bus**	SOC Interconnect (Wishbone, AXI, Switch, DMA)	Lab#5 - Caravel FPGA (2w) - team	15-Nov
8	**1-Nov**	**Memory**	SOC Memory - Cache/DDR		
9	**8-Nov**	**Presentation**	Caravel SOC Lab Presentation - Lab#4-1, Lab#4-2, Lab#5	Lab#6 & Final Project - WLOS (4-6 w) - team	29-Nov
10	**15-Nov**		Midterm		
11	**22-Nov**	**FW**	Embedded Programming (ISA, Interrupt, Debugging)		
12	**29-Nov**	**EDA**	Static Timing Analysis		10-Jan
13	**6-Dec**	**Presentation**	Caravel SOC Lab Presentation - Lab#A-E, Final Project Proposal		
14	**13-Dec**	**EDA**	Synthesis and Optimization		
15	**20-Dec**	**EDA**	Verification & Simulation		
16	**27-Dec**		No Class		
17	**3-Jan**		No Class		
18	**10-Jan**		Final Project Presentation		

Grading

Grading

Item	Content	Submission	Weight
Lab#1	Tool installation (individual)	Screen shot	2
Lab#2	HLS-FIR (individual)	Report	4
Lab#3	XSIM & GTKWave Simulation - Individual	Report	10
Lab#4-1	Management FW (team)	Github & Report	8
Lab#4-2	Caravel User Project - FIR (team)	Github & Report	8
Lab#5	Caravel FPGA (team)	Github & Report	8
Lab#A-E	Choose 2, each 8 points (team)		0
Lab#A-E	Extra Lab, each 4 points (team)		20
	A: Interrupt Service	Github & Report	
	B: ExMem - User Project Memory	Github & Report	
	C: UART	Github & Report	
	D: WB-SDRAM	Github & Report	
	E: Software Emulation - Bit Banging	Github & Report	
Lab#6	Baseline WLOS (team)	Github & Report	10
Midterm			0
Final Project	WLOS Optimization (team)	Github & Report & ppt	40
Presentation	Selected presentation (extra credit)	ppt	4
StudyJournal	Github & StudyJournal (individual)	Github & StudyJournal.md	4
Soft Skill	Ask question, offer help, sharing	Send link of evidence to TA	2
		Total	120

Logistics

- Register course “SOC Design” as auditor to access course materials
- We will Github as course working area
  - https://github.com/bol-edu/soclab-nthusp23/tree/main
  - Link to StudyJournal.md, and personal Github
- Special Project Course Material deposited in
  - https://github.com/bol-edu/soclab-nthusp23/tree/main/meeting-note

Collaborative Learning checklist

- Accept Slack (channel: soclab) invitation
  - https://boledu.slack.com/archives/C05D406JUSX
  - Show you are in the slack channel (screen shot)
- Subscribe Github/Discussion
  - https://github.com/bol-edu/HLS-SOC-Discussions
  - Show you have subscribe the Github/Discussion （ send screen shot ）
- Create Personal Github (if not created yet.)
  - Send your Github Link with a brief README.md
- Create up the SOCStudy.md
  - Create Hackmd.io account (if not created yet.)
  - Create first document: SOCStudy.md (shared) and send the link

- Submit the Google Form below

https://docs.google.com/forms/d/e/1FAIpQLSe49P6olVLQrXquUw6JrIXCNG3Pc6aNTCtnPYzZcMTHgTnbPw/viewform?usp=sf_link