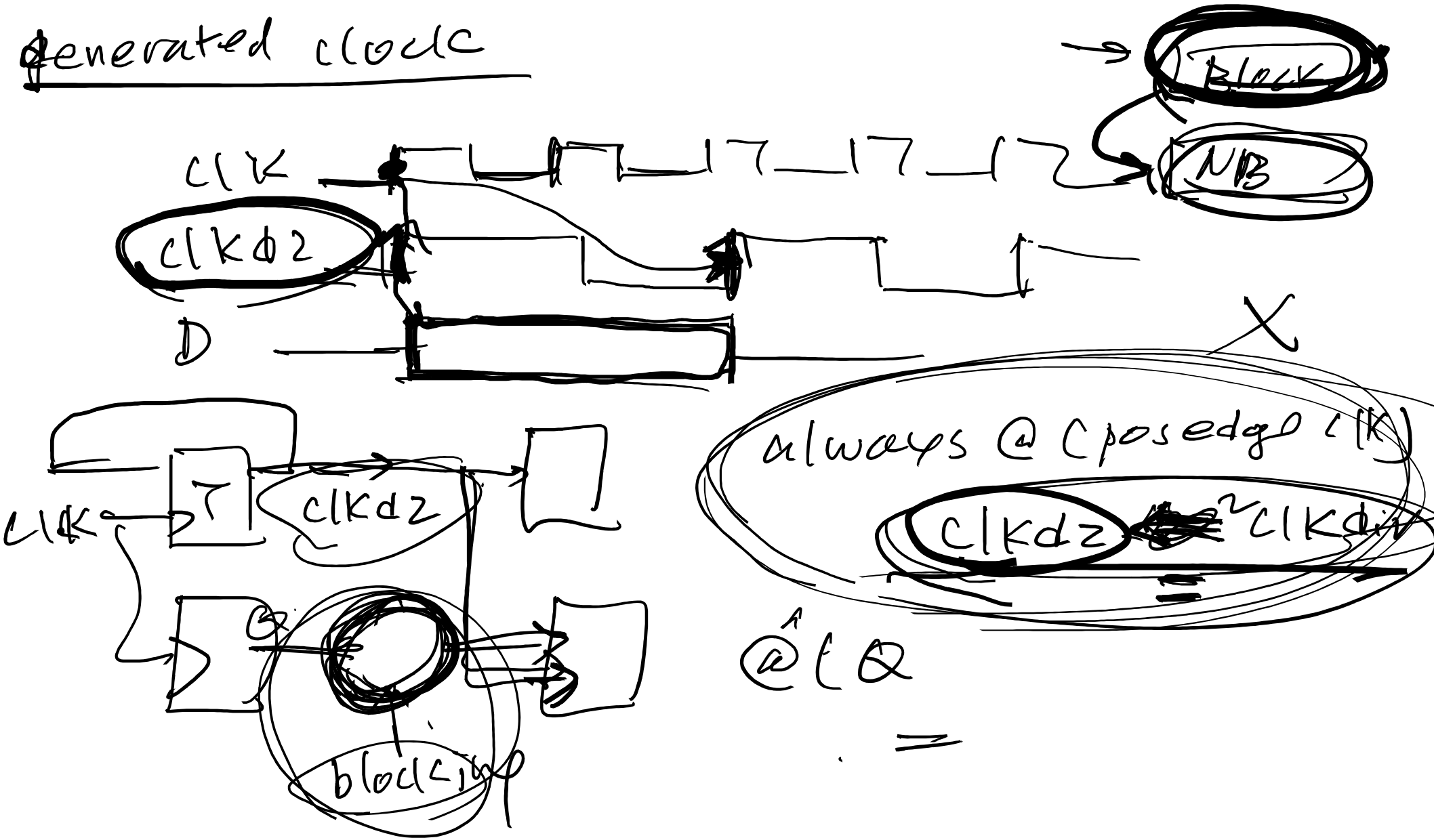
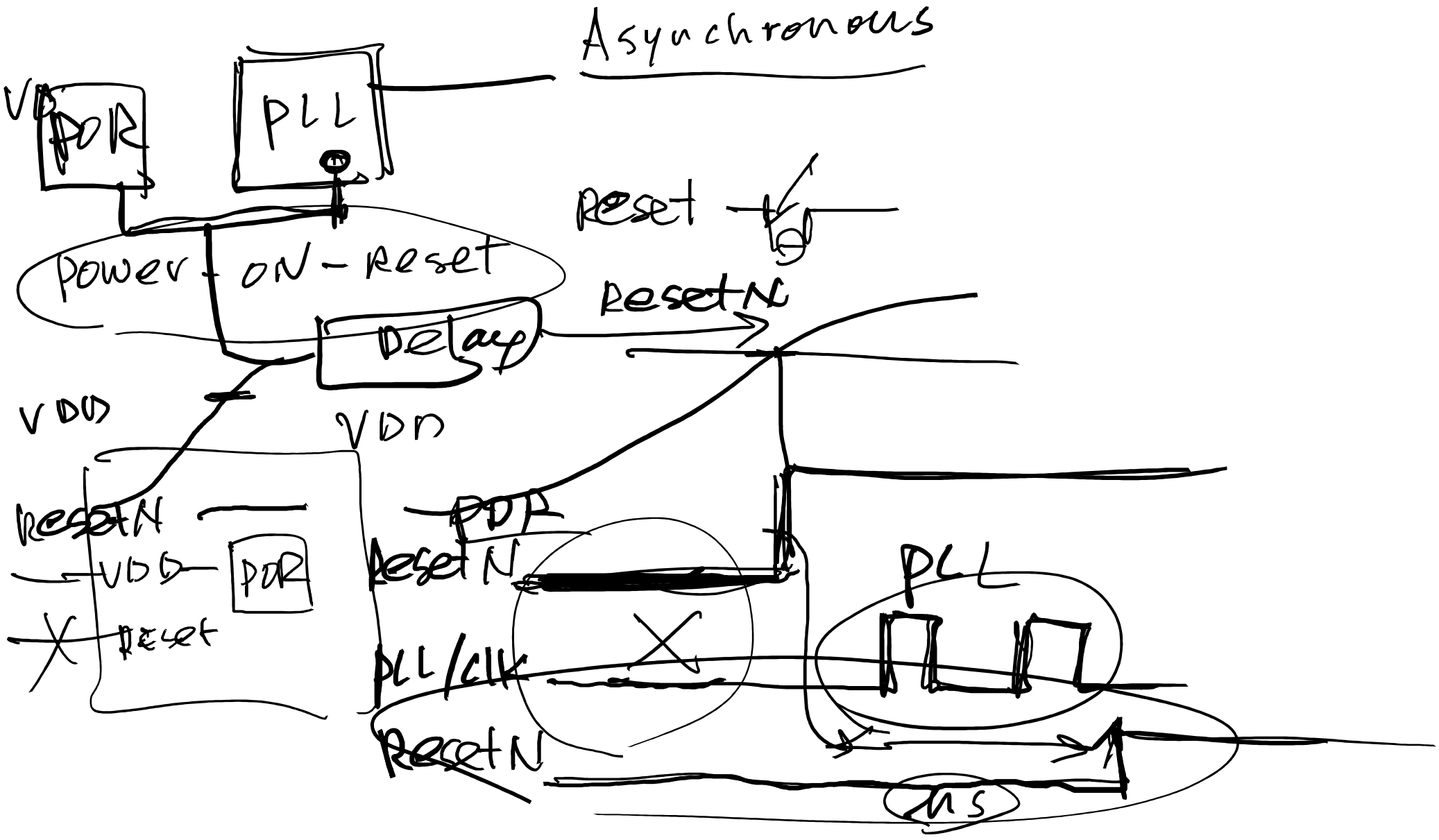
Generated clock




Asynchronous
VDD
POR
PLL
Reset
Power-ON-Reset
ResetN
Delay
VDD
VDD
ResetN
VDD
POR
Reset
POR
ResetN
PLL
PLL/CLK
ResetN
ns

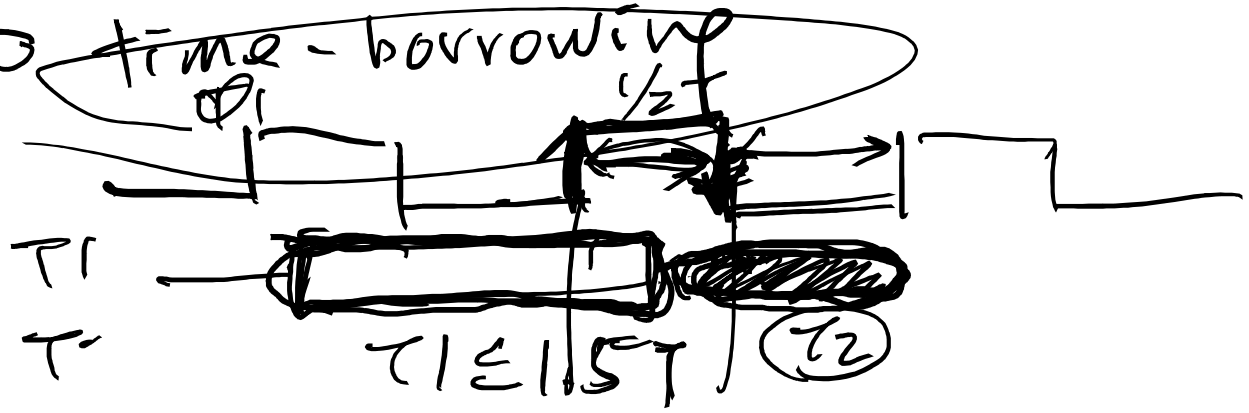
Tp = clock period

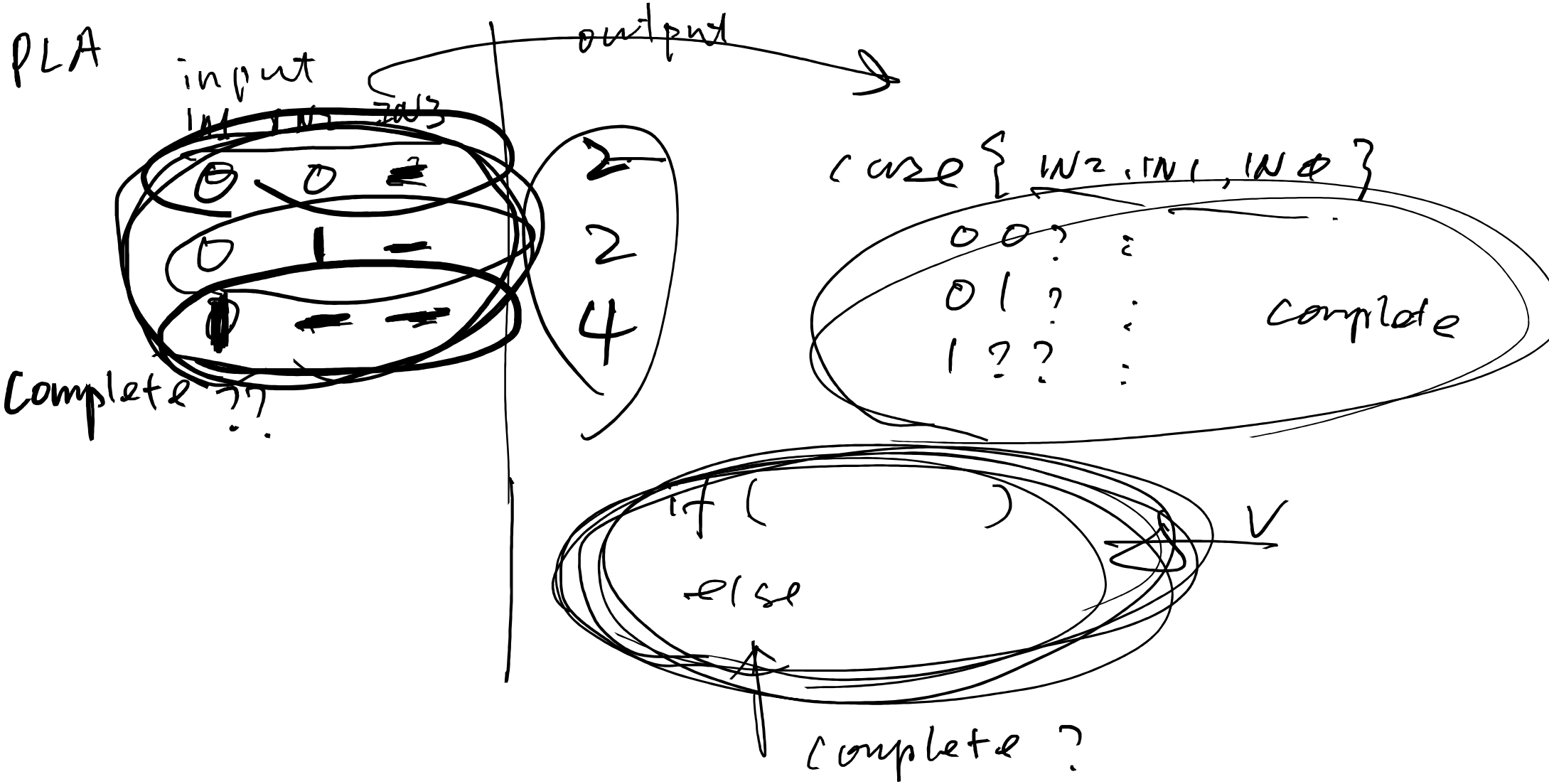
balance delay in each pipeline stage

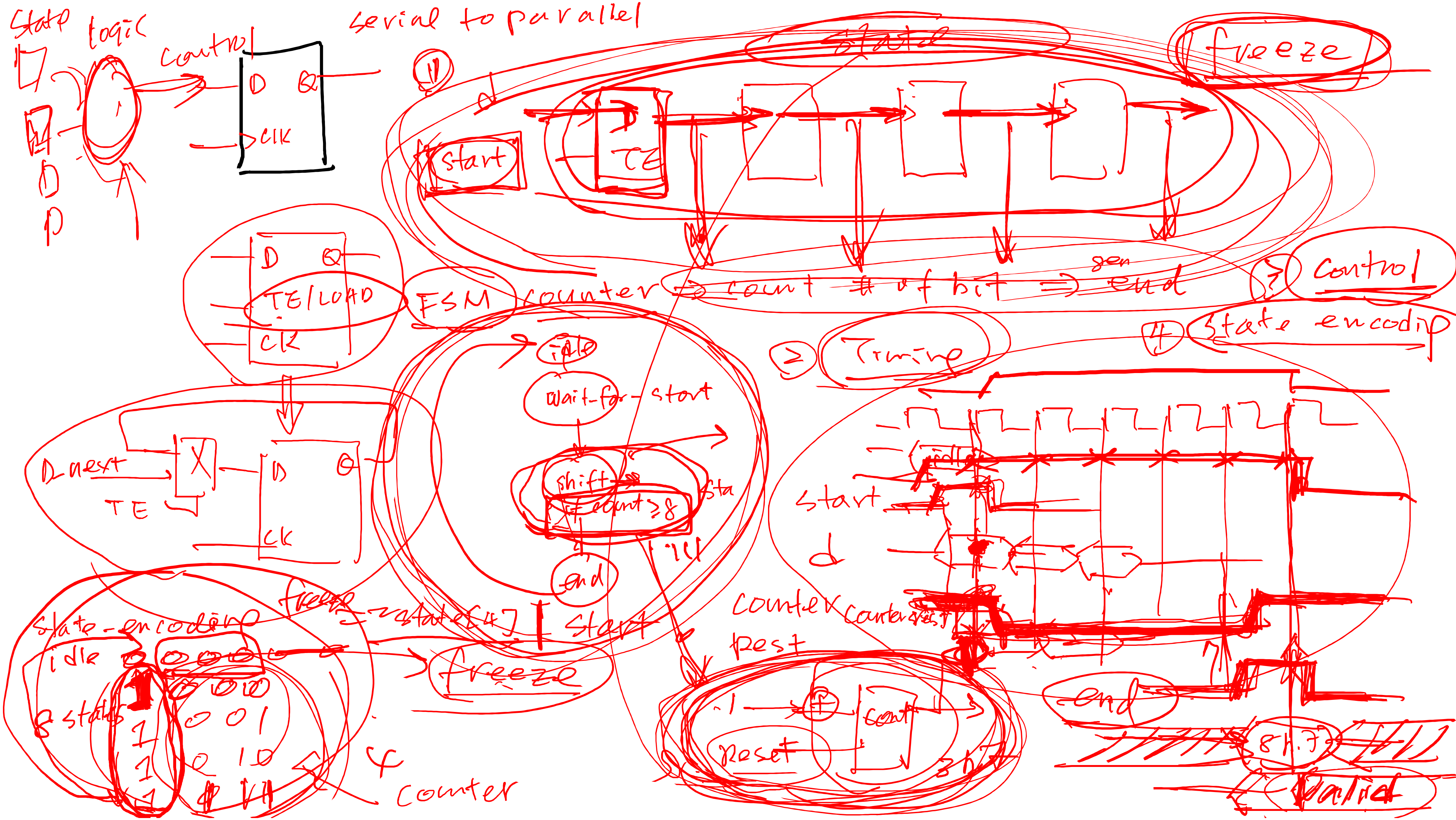
T1 ~ T2 ø

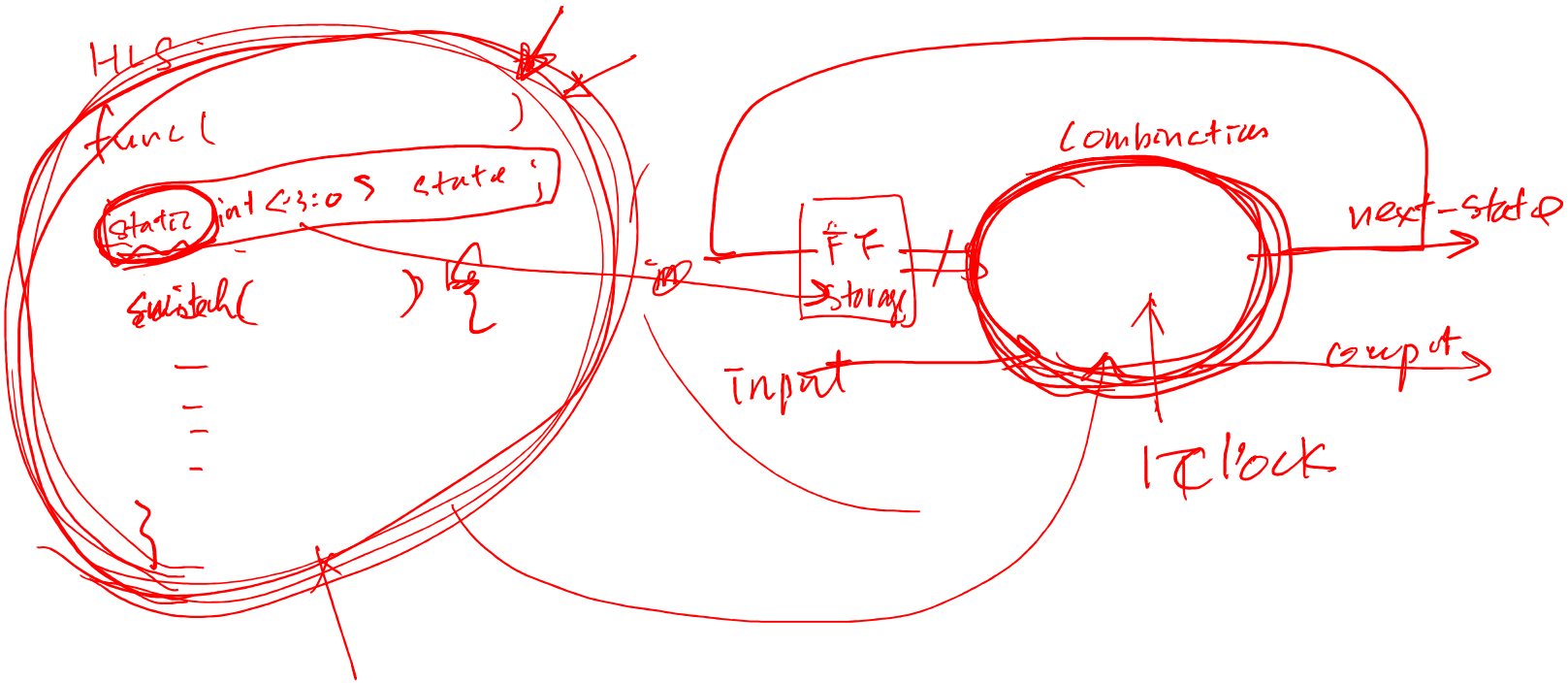
what happen T1 > T2 but T1 + T2 < 2Tp

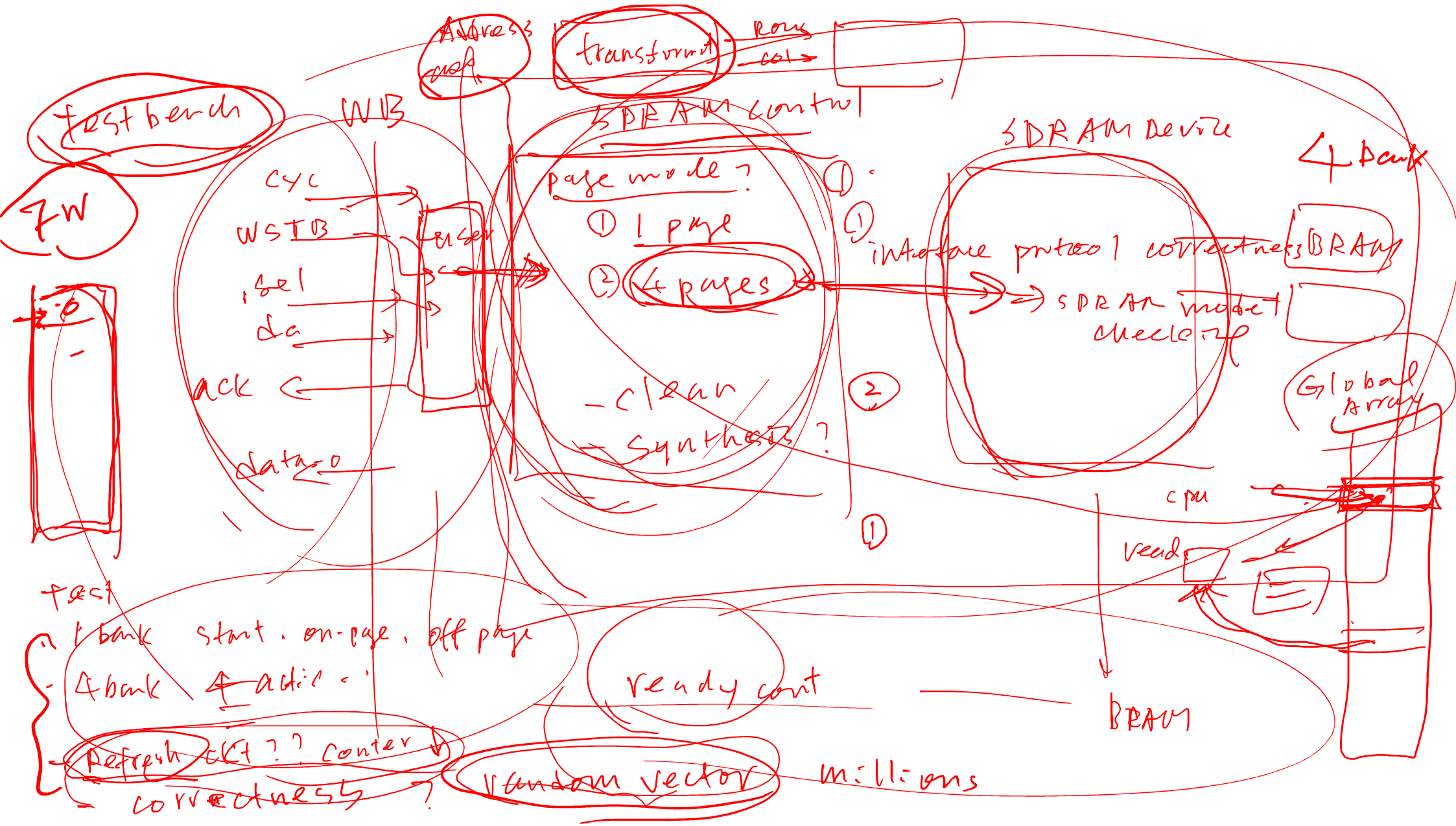
~~time~~ time-borrowing




PLA
input
output
Complete ??
2
2
4
case { IN2 , IN1 , IN0 }
00 ? :
01 ? :
1 ?? :
complete
if ( )
V
else
complete ?


state
logic
control
D
Q
clk
serial to parallel
freeze
start
TE
D
Q
TE/LOAD
CK
FSM
counter
count # of bit
gen end
control
state encoding
Timing
idle
wait-for-start
shift
end
D_next
TE
CK
start
d
counter reset
reset
cont
end
valid
state_encoding
idle
8 states
counter
freeze
state[4]
start


HLS
func(
)
static int<3:0> state;
switch(
)
FF
storage
Combinational
next-state
input
output
clock


testbench
FW
WB
Address
transform
row
col
SDRAM cntr
SDRAM Device
4 bank
cyc
WSTB
sel
da
ack
data_o
page mode ?
① 1 page
② 4 pages
clear
synthesis ?
interface protocol correctness
BRAM
SDRAM model
checking
Global Array
cpu
read
test
1 bank start . on-page . off page
4 bank
Refresh ckt ? ? center
correctness ?
ready cont
random vector
millions
BRAM