A Data System Based on APB Bus Protocol

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1. Overview

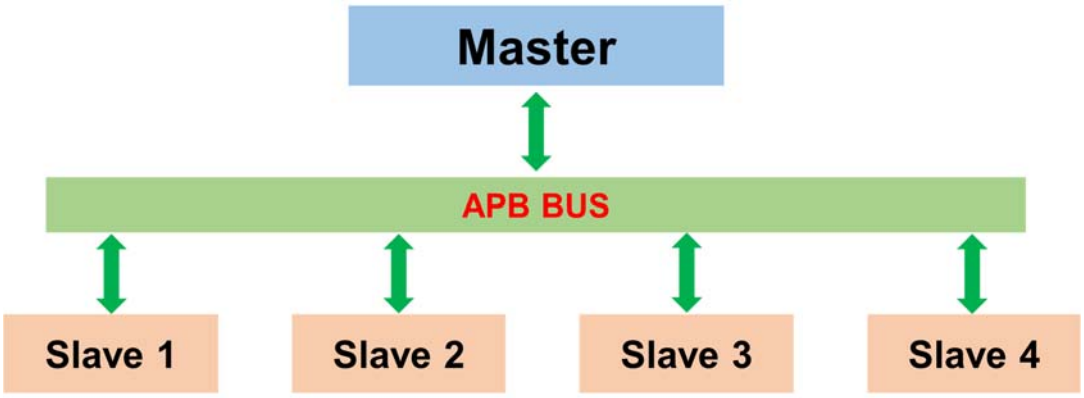
APB is an efficient peripheral data transmission bus introduced by ARM, which can mount multiple slave devices simultaneously on the bus. Master device controls bus signal to select different slave devices for data interaction.

In this design, we include a Master device and four slave devices connected to each other via the APB bus. For simplicity, all slave devices were instantiated from the same underlying design. In practical application, different slave devices can be designed according to specific functions.

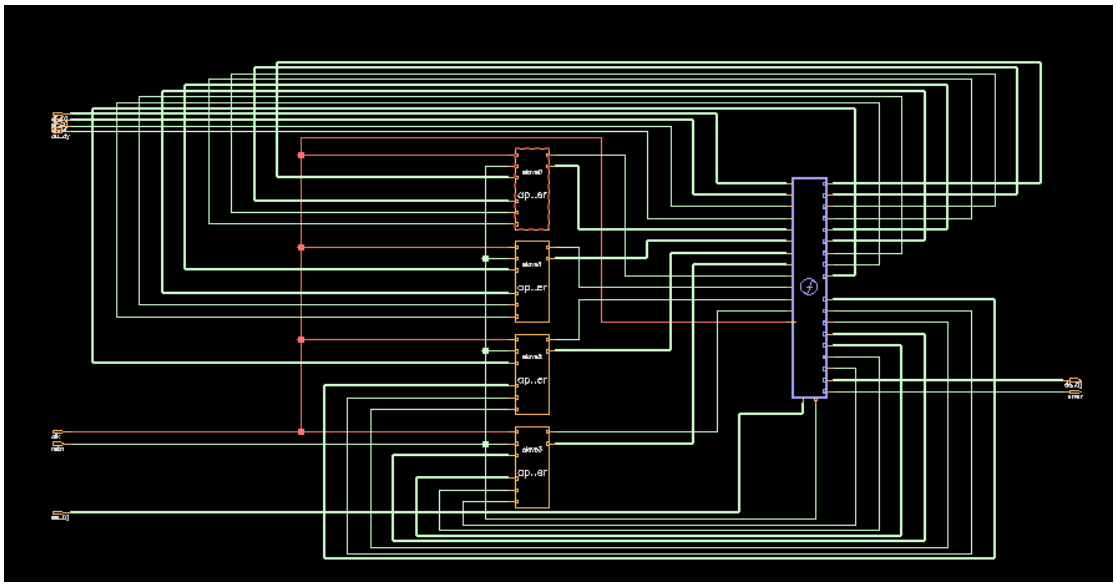
2. APB Protocol

Signal	Source	Description
PCLK	Clock source	Clock. The rising edge of **PCLK** times all transfers on the APB.
PRESETn	System bus equivalent	Reset. The APB reset signal is active LOW. This signal is normally connected directly to the system bus reset signal.
PADDR	APB bridge	Address. This is the APB address bus. It can be up to 32 bits wide and is driven by the peripheral bus bridge unit.
PPROT	APB bridge	Protection type. This signal indicates the normal, privileged, or secure protection level of the transaction and whether the transaction is a data access or an instruction access.
PSELx	APB bridge	Select. The APB bridge unit generates this signal to each peripheral bus slave. It indicates that the slave device is selected and that a data transfer is required. There is a **PSELx** signal for each slave.
PENABLE	APB bridge	Enable. This signal indicates the second and subsequent cycles of an APB transfer.
PWRITE	APB bridge	Direction. This signal indicates an APB write access when HIGH and an APB read access when LOW.
PWDATA	APB bridge	Write data. This bus is driven by the peripheral bus bridge unit during write cycles when **PWRITE** is HIGH. This bus can be up to 32 bits wide.
PSTRB	APB bridge	Write strobes. This signal indicates which byte lanes to update during a write transfer. There is one write strobe for each eight bits of the write data bus. Therefore, **PSTRB[n]** corresponds to **PWDATA[(8n + 7):(8n)]**. Write strobes must not be active during a read transfer.
PREADY	Slave interface	Ready. The slave uses this signal to extend an APB transfer.
PRDATA	Slave interface	Read Data. The selected slave drives this bus during read cycles when **PWRITE** is LOW. This bus can be up to 32-bits wide.
PSLVERR	Slave interface	This signal indicates a transfer failure. APB peripherals are not required to support the **PSLVERR** pin. This is true for both existing and new APB peripheral designs. Where a peripheral does not include this pin then the appropriate input to the APB bridge is tied LOW.

3. System



4. Schematic



5. DC

```
Number of ports:                         1239
Number of nets:                          8434
Number of cells:                         6779
Number of combinational cells:           5406
Number of sequential cells:              1361
Number of macros/black boxes:               0
Number of buf/inv:                       3423
Number of references:                      13

Combinational area:              27570.000000
Buf/Inv area:                    15086.000000
Noncombinational area:           21216.000000
Macro/Black Box area:                0.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:                 48786.000000
```

```
                 Internal         Switching           Leakage            Total
Power Group      Power            Power               Power              Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000             NA   (     N/A)
memory             0.0000           0.0000              0.0000             NA   (     N/A)
black_box          0.0000           0.0000              0.0000             NA   (     N/A)
clock_network      0.0000           0.0000              0.0000             NA   (     N/A)
register           0.1218        4.4038e-02             0.0000             NA   (     N/A)
sequential      5.4303e-07        7.7232e-06             0.0000             NA   (     N/A)
combinational   7.6060e-03           0.7871              0.0000             NA   (     N/A)
--------------------------------------------------------------------------------------------------
Total              0.1294 mW        0.8312 mW           0.0000             NA
```