

## SN74LVC1G17 Single Schmitt-Trigger Buffer

### 1 Features

- Available in Ultra Small 0.64-mm<sup>2</sup> Package (DPW) With 0.5-mm Pitch
- Supports 5-V V<sub>CC</sub> Operation
- Inputs Accept Voltages to 5.5 V
- Max t<sub>pd</sub> of 4.6 ns at 3.3 V
- Low Power Consumption, 10-µA Max I<sub>CC</sub>
- ±24-mA Output Drive at 3.3 V
- I<sub>off</sub> Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- AV Receiver
- Audio Dock: Portable
- Blu-ray Player and Home Theater
- MP3 Player/Recorder
- Personal Digital Assistant (PDA)
- Power: Telecom/Server AC/DC Supply: Single Controller: Analog and Digital
- Solid State Drive (SSD): Client and Enterprise
- TV: LCD/Digital and High-Definition (HDTV)
- Tablet: Enterprise
- Video Analytics: Server
- Wireless Headset, Keyboard, and Mouse

### 3 Description

This single Schmitt-trigger buffer is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC1G17 device contains one buffer and performs the Boolean function Y = A.

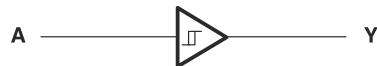
The CMOS device has high output drive while maintaining low static power dissipation over a broad V<sub>CC</sub> operating range.

The SN74LVC1G17 is available in a variety of packages, including the ultra-small DPW package with a body size of 0.8 mm × 0.8mm.

#### Device Information

DEVICE NAME	PACKAGE <sup>(1)</sup>	BODY SIZE
SN74LVC1G17	SOT-23 (5)	2.9mm × 1.6mm
	SC70 (5)	2.0mm × 1.25mm
	X2SON (4)	0.8mm × 0.8mm
	SON (6)	1.45mm × 1.0mm
	SON (6)	1.0mm × 1.0mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

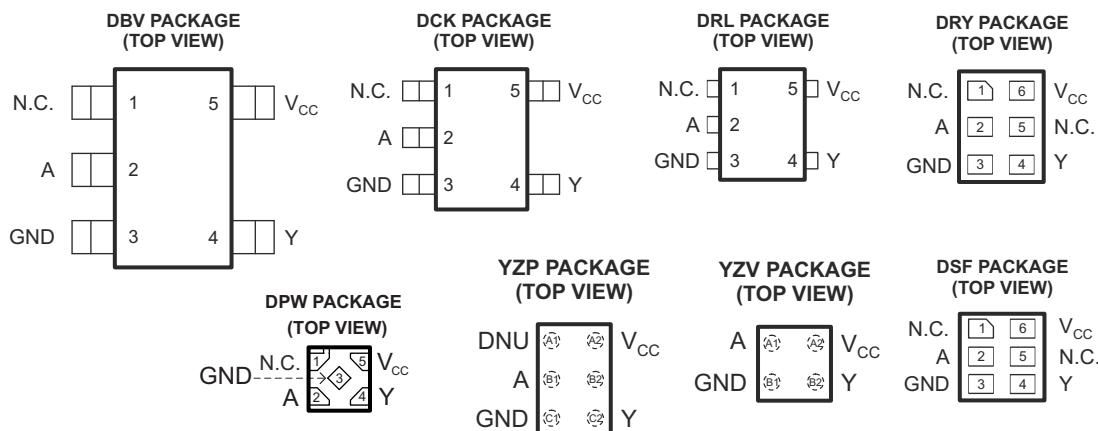
<b>Changes from Revision V (April 2014) to Revision W (September 2020)</b>	<b>Page</b>
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Corrected part number from SN74LVC1G14 to SN74LVC1G17 in the <i>Application Information</i> section.....	11
• Corrected typical application schematic in <i>Typical Application</i> section.....	11

<b>Changes from Revision U (February 2014) to Revision V (April 2014)</b>	<b>Page</b>
• Added Pin Functions table. ....	3
• Added Handling Ratings table. ....	4
• Added Thermal Information table. ....	5
• Added Typical Characteristics. ....	7
• Added Application and Implementation section. ....	11
• Added Power Supply Recommendations section. ....	12
• Added Layout section. ....	13

<b>Changes from Revision T (November 2012) to Revision U (February 2014)</b>	<b>Page</b>
• Added Applications.....	1
• Moved $T_{stg}$ to Handling Ratings table.....	4
• Changed MAX operating free-air temperature from $85^\circ\text{C}$ to $125^\circ\text{C}$ .....	5
• Added $-40^\circ\text{C}$ to $125^\circ\text{C}$ to Electrical Characteristics table.....	6
• Added Switching Characteristics table for $-40^\circ\text{C}$ to $125^\circ\text{C}$ temperature range.....	7

<b>Changes from Revision S (June 2011) to Revision T (November 2012)</b>	<b>Page</b>
• Removed Ordering Information table.....	3

## 5 Pin Configuration and Functions



N.C. – No internal connection  
See mechanical drawings for dimensions.  
DNU – Do not use

## Pin Functions

PIN					DESCRIPTION
NAME	DBV, DCK, DRL, DPW	DRY, DSF	YZP	YZV	
NC	1	1, 5	A1, B2	–	Not connected
A	2	2	B1	A1	Input
GND	3	3	C1	B1	Ground
Y	4	4	C2	B2	Output
V <sub>CC</sub>	5	6	A2	A2	Power terminal

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	6.5	V
V <sub>I</sub>	Input voltage range <sup>(1)</sup>	-0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(1)</sup>	-0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high or low state <sup>(1) (2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current  V <sub>I</sub> < 0		-50	mA
I <sub>OK</sub>	Output clamp current  V <sub>O</sub> < 0		-50	mA
I <sub>O</sub>	Continuous output current		±50	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA

(1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(2) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.

### 6.2 Handling Ratings

		MIN	MAX	UNIT
T <sub>stg</sub>	Storage temperature range	-65	150	°C
V <sub>ESD</sub> <sup>(1)</sup>	Human-Body Model (HBM) <sup>(2)</sup>	0	2	kV
	Charged-Device Model (CDM) <sup>(3)</sup>	0	1	kV

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
- (2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
$V_{CC}$	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
$V_I$	Input voltage		0	5.5	V
$V_O$	Output voltage		0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 1.65\text{ V}$		-4	mA
		$V_{CC} = 2.3\text{ V}$		-8	
		$V_{CC} = 3\text{ V}$		-16	
		$V_{CC} = 4.5\text{ V}$		-24	
$I_{OL}$	Low-level output current	$V_{CC} = 1.65\text{ V}$		4	mA
		$V_{CC} = 2.3\text{ V}$		8	
		$V_{CC} = 3\text{ V}$		16	
		$V_{CC} = 4.5\text{ V}$		24	
$T_A$ Operating free-air temperature			-40	125	°C

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74LVC1G17							UNIT
	DBV	DCK	DRL	DRY	YZP	DPW	YZV	
	5 PINS	5 PINS	5 PINS	6 PINS	5 PINS	4 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	229	280	350	608	130	340	181
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	164	66	121	432	54	215	1
$R_{\theta JB}$	Junction-to-board thermal resistance	62	67	171	446	51	294	39
$\Psi_{JT}$	Junction-to-top characterization parameter	44	2	11	191	1	41	8
$\Psi_{JB}$	Junction-to-board characterization parameter	62	66	169	442	50	294	38
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	–	–	–	198	–	250	–

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics—DC Limit Changes

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	25°C			−40°C TO 85°C			−40°C TO 125°C			UNIT
			MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP	MAX	
V <sub>T+</sub> (Positive-going input threshold voltage)		1.65 V				0.76		1.13	0.76		1.13	V
		2.3 V				1.08		1.56	1.08		1.56	
		3 V				1.48		1.92	1.48		1.92	
		4.5 V				2.19		2.74	2.19		2.74	
		5.5 V				2.65		3.33	2.65		3.33	
V <sub>T−</sub> (Negative-going input threshold voltage)		1.65 V				0.35		0.59	0.35		0.59	V
		2.3 V				0.56		0.88	0.56		0.88	
		3 V				0.89		1.2	0.89		1.2	
		4.5 V				1.51		1.97	1.51		1.97	
		5.5 V				1.88		2.4	1.88		2.4	
ΔV <sub>T</sub> Hysteresis (V <sub>T+</sub> − V <sub>T−</sub> )		1.65 V				0.36		0.64	0.36		0.64	V
		2.3 V				0.45		0.78	0.45		0.78	
		3 V				0.51		0.83	0.51		0.83	
		4.5 V				0.58		0.93	0.58		0.93	
		5.5 V				0.69		1.04	0.69		1.04	
V <sub>OH</sub>	I <sub>OH</sub> = −100 μA	1.65 V to 5.5 V				V <sub>CC</sub> − 0.1			V <sub>CC</sub> − 0.1			V
	I <sub>OH</sub> = −4 mA	1.65 V				1.2			1.2			
	I <sub>OH</sub> = −8 mA	2.3 V				1.9			1.9			
	I <sub>OH</sub> = −16 mA	3 V				2.4			2.4			
	I <sub>OH</sub> = −24 mA					2.3			2.3			
	I <sub>OH</sub> = −32 mA	4.5 V				3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V					0.1			0.1		V
	I <sub>OL</sub> = 4 mA	1.65 V					0.45			0.45		
	I <sub>OL</sub> = 8 mA	2.3 V					0.3			0.3		
	I <sub>OL</sub> = 16 mA	3 V					0.4			0.4		
	I <sub>OL</sub> = 24 mA						0.55			0.55		
	I <sub>OL</sub> = 32 mA	4.5 V					0.55			0.55		
I <sub>I</sub>	A input	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V				±5			±5	μA	
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0				±10			±10	μA	
I <sub>CC</sub>	V <sub>I</sub> = 5.5 V or GND, V <sub>I</sub> = 3.6 V or GND,	I <sub>O</sub> = 0	1.65 V to 5.5 V				10			10	μA	
			3 V to 3.6 V	0.5	1.5							
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> − 0.6 V, Other inputs at V <sub>C</sub> C or GND		3 V to 5.5 V				500			500	μA	
C <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND		3.3 V		4.5						pF	

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## 6.6 Switching Characteristics, $C_L = 15 \text{ pF}$

over recommended operating free-air temperature range,  $C_L = 15 \text{ pF}$  (unless otherwise noted) (see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-40°C TO 85°C								UNIT	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$t_{pd}$	A	Y	2.8	9.9	1.6	5.5	1.5	4.6	0.9	4.4	ns	

## 6.7 Switching Characteristics AC Limit, -40°C TO 85°C

over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$  or  $50 \text{ pF}$  (unless otherwise noted) (see [Figure 7-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-40°C TO 85°C								UNIT	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$t_{pd}$	A	Y	3.8	11	2	6.5	1.8	5.5	1.2	5	ns	

## 6.8 Switching Characteristics AC Limit, -40°C TO 125°C

over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$  or  $50 \text{ pF}$  (unless otherwise noted) (see [Figure 7-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	-40°C TO 125°C								UNIT	
			$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$			
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$t_{pd}$	A	Y	3.8	13	2	8	1.8	6.5	1.2	6	ns	

## 6.9 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8 \text{ V}$	$V_{CC} = 2.5 \text{ V}$	$V_{CC} = 3.3 \text{ V}$	$V_{CC} = 5 \text{ V}$	UNIT
		TYP	TYP	TYP	TYP	
$C_{pd}$	Power dissipation capacitance	f = 10 MHz	20	21	22	26 pF

## 6.10 Typical Characteristics

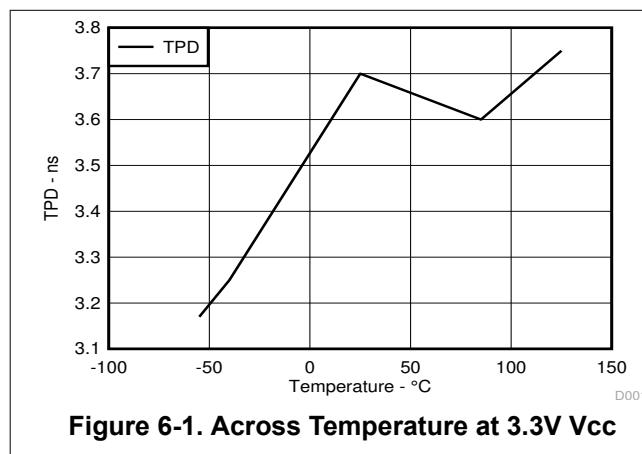


Figure 6-1. Across Temperature at 3.3V Vcc

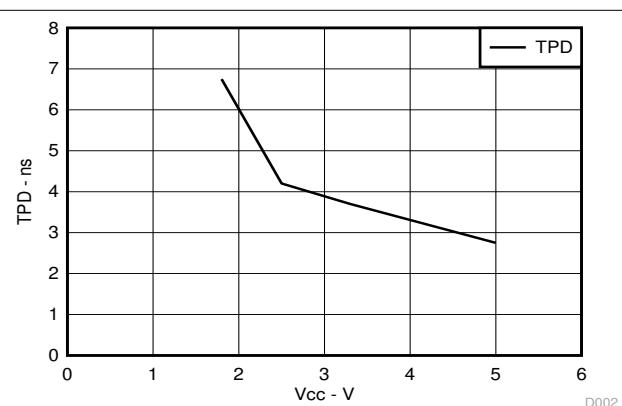
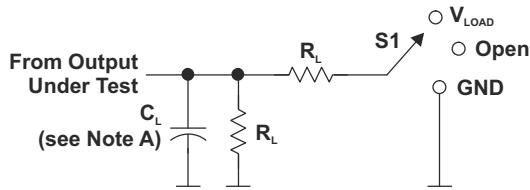


Figure 6-2. Across Vcc at 25°C

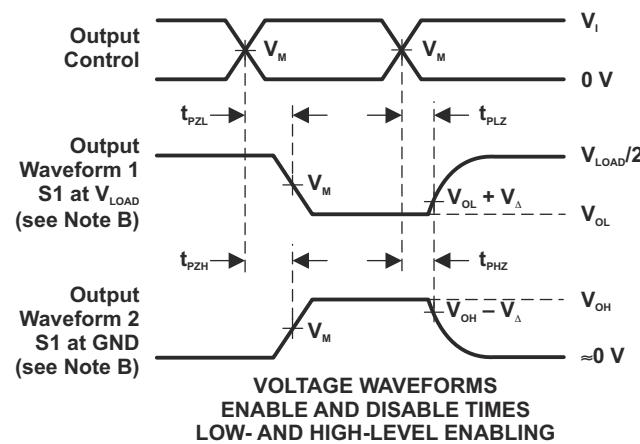
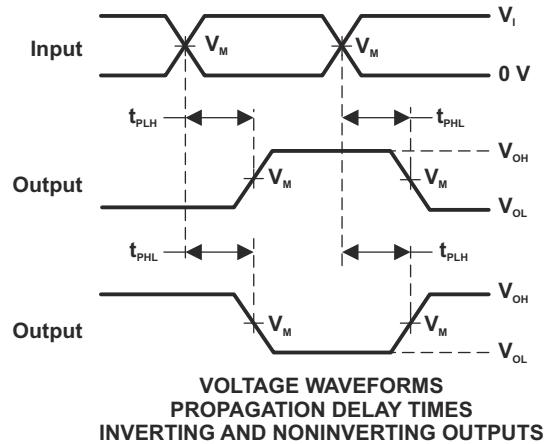
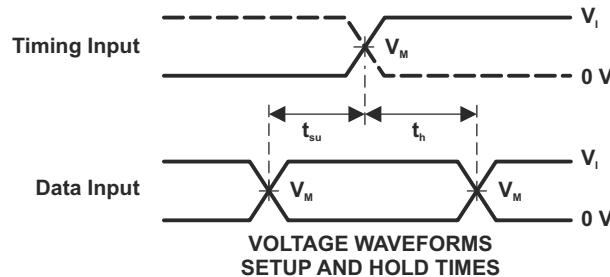
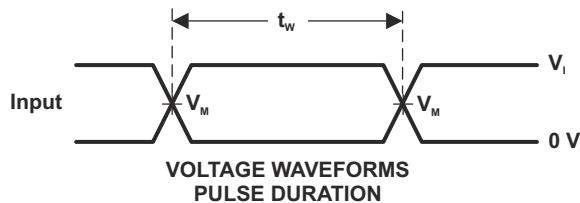
## 7 Parameter Measurement Information



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

LOAD CIRCUIT

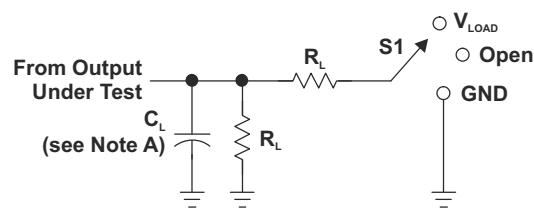
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_\Delta$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	$1\text{ M}\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	$1\text{ M}\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	$1\text{ M}\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	$1\text{ M}\Omega$	0.3 V



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_o = 50\text{ }\Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

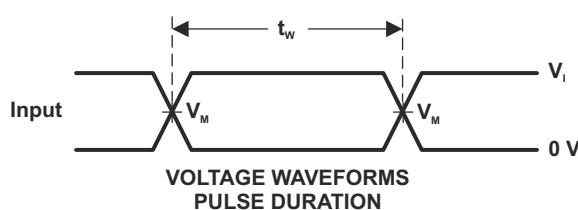
Figure 7-1. Load Circuit and Voltage Waveforms



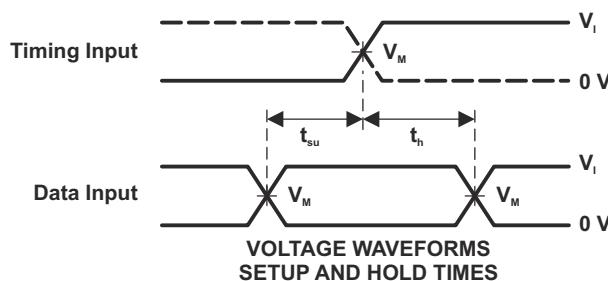
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

#### LOAD CIRCUIT

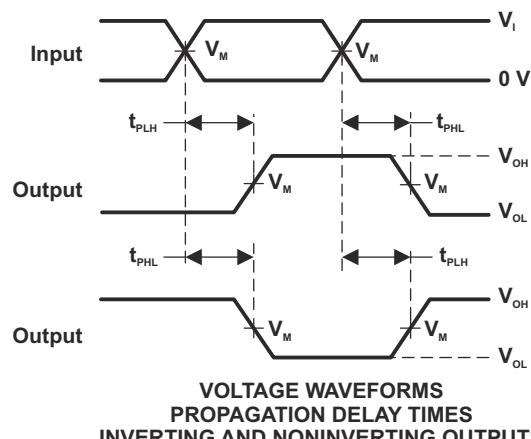
V <sub>CC</sub>	INPUTS		V <sub>M</sub>	V <sub>LOAD</sub>	C <sub>L</sub>	R <sub>L</sub>	V <sub>A</sub>
	V <sub>I</sub>	t <sub>r</sub> /t <sub>f</sub>					
1.8 V ± 0.15 V	V <sub>CC</sub>	≤2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V <sub>CC</sub>	≤2 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V <sub>CC</sub>	≤2.5 ns	V <sub>CC</sub> /2	2 × V <sub>CC</sub>	50 pF	500 Ω	0.3 V



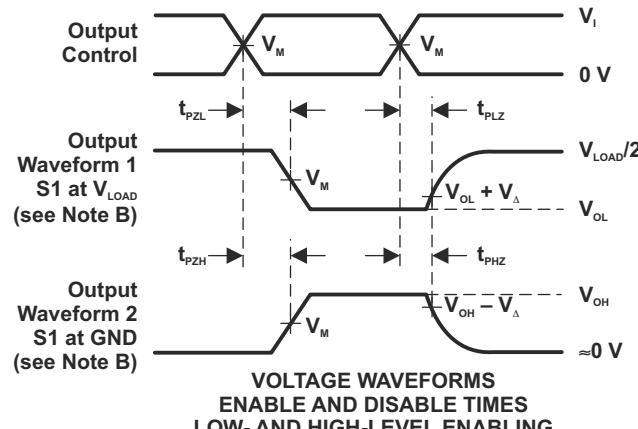
## VOLTAGE WAVEFORMS PULSE DURATION



## VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



## VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



## VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES:

- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_o = 50 \Omega$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZH}$  and  $t_{PZL}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

**Figure 7-2. Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The SN74LVC1G17 device contains one Schmitt trigger buffer and performs the Boolean function  $Y = A$ . The device functions as an independent buffer, but because of Schmitt action, it will have different input threshold levels for a positive-going ( $VT^+$ ) and negative-going signals.

The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

- Wide operating voltage range.
  - Operates From 1.65 V to 5.5 V.
- Allows Down voltage translation.
- Inputs accept voltages to 5.5 V.
- $I_{off}$  feature allows voltages on the inputs and outputs, when  $V_{CC}$  is 0 V.

### 8.4 Device Functional Modes

Table 8-1. Function Table

INPUT A	OUTPUT Y
H	H
L	L

## 9 Applications and Implementation

---

### Note

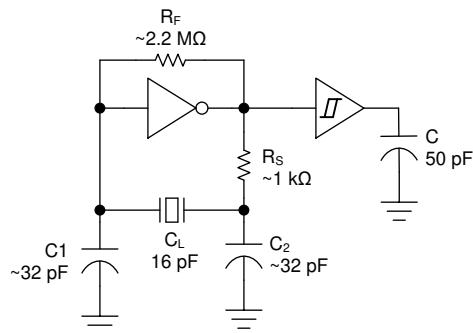
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

---

### 9.1 Application Information

The SN74LVC1G17 is a high drive CMOS device that can be used for a multitude of buffer type functions where the input is slow or noisy. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to  $V_{CC}$ .

### 9.2 Typical Application



#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

##### 1. Recommended Input Conditions

- Rise time and fall time specs. See ( $\Delta t/\Delta V$ ) in the [Recommended Operating Conditions](#) table.
- Specified high and low levels. See ( $V_{IH}$  and  $V_{IL}$ ) in the [Recommended Operating Conditions](#) table.
- Inputs are overvoltage tolerant allowing them to go as high as ( $V_I$  max) in the [Recommended Operating Conditions](#) table at any valid  $V_{CC}$ .

##### 2. Recommend Output Conditions

- Load currents should not exceed ( $I_O$  max) per output and should not exceed (continuous current through  $V_{CC}$  or GND) total current for the part. These limits are located in the [Absolute Max Ratings](#) table.
- Outputs should not be pulled above  $V_{CC}$ .

### 9.2.3 Application Curves

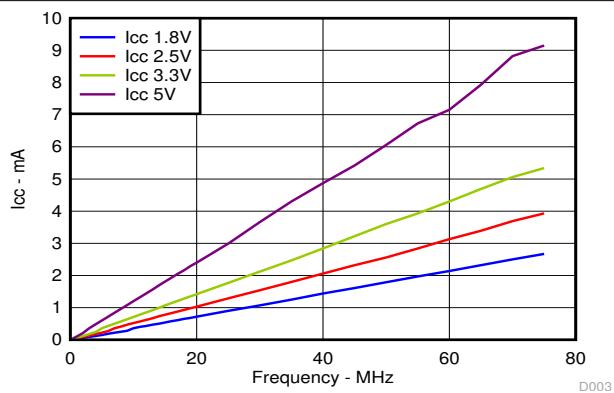


Figure 9-1. ICC vs Frequency

## 10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each Vcc pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply a 0.1- $\mu$ F capacitor is recommended and if there are multiple Vcc pins then a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass caps to reject different frequencies of noise. 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input terminals should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to Gnd or Vcc whichever make more sense or is more convenient.

### 11.2 Layout Example



## 12 Device and Documentation Support

### 12.1 Trademarks

All other trademarks are the property of their respective owners.

### 12.2 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.3 Glossary

#### [TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G17DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(C175, C17F, C17J, C17K, C17R) (C17H, C17P, C17S)	Samples
SN74LVC1G17DBVRE4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C17F	Samples
SN74LVC1G17DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C17F	Samples
SN74LVC1G17DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(C175, C17F, C17J, C17K, C17R) (C17H, C17P, C17S)	Samples
SN74LVC1G17DBVTE4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C17F	Samples
SN74LVC1G17DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C17F	Samples
SN74LVC1G17DCK3	ACTIVE	SC70	DCK	5	3000	RoHS & Non-Green	SNBI	Level-1-260C-UNLIM	-40 to 85	(C7F, C7Z)	Samples
SN74LVC1G17DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(C75, C7F, C7J, C7 K, C7R, C7T) (C7H, C7P, C7S)	Samples
SN74LVC1G17DCKRE4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C75 C7S	Samples
SN74LVC1G17DCKRG4	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C75 C7S	Samples
SN74LVC1G17DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(C75, C7F, C7J, C7 K, C7R, C7T) (C7H, C7P, C7S)	Samples
SN74LVC1G17DCKTE4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C75 C7S	Samples
SN74LVC1G17DCKTG4	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C75 C7S	Samples
SN74LVC1G17DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	S4	Samples
SN74LVC1G17DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	(C77, C7R)	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G17DRLRG4	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAUJAG	Level-1-260C-UNLIM	-40 to 125	(C77, C7R)	Samples
SN74LVC1G17DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C7	Samples
SN74LVC1G17DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	C7	Samples
SN74LVC1G17YZPR	ACTIVE	DSBGA	YZP	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C7N	Samples
SN74LVC1G17YZVR	ACTIVE	DSBGA	YZV	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	C7 (7, N)	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

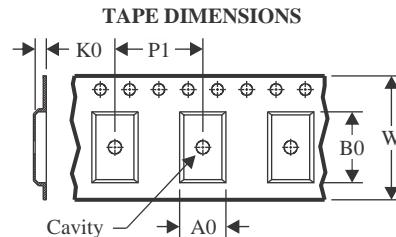
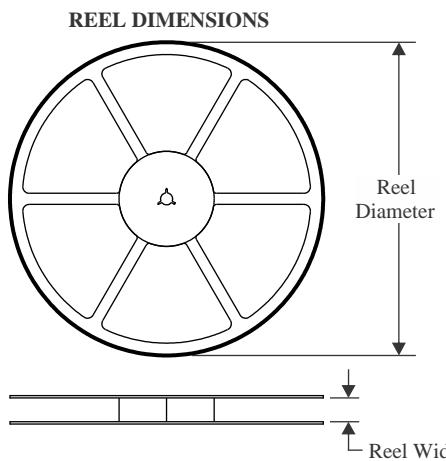
**OTHER QUALIFIED VERSIONS OF SN74LVC1G17 :**

- Automotive : [SN74LVC1G17-Q1](#)
- Enhanced Product : [SN74LVC1G17-EP](#)

NOTE: Qualified Version Definitions:

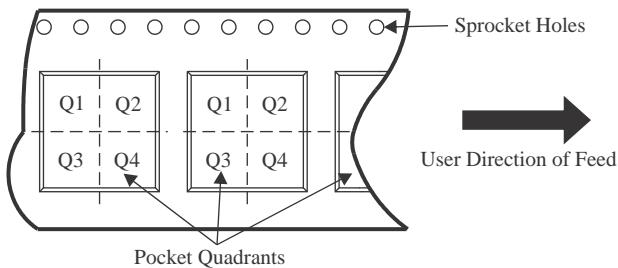
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

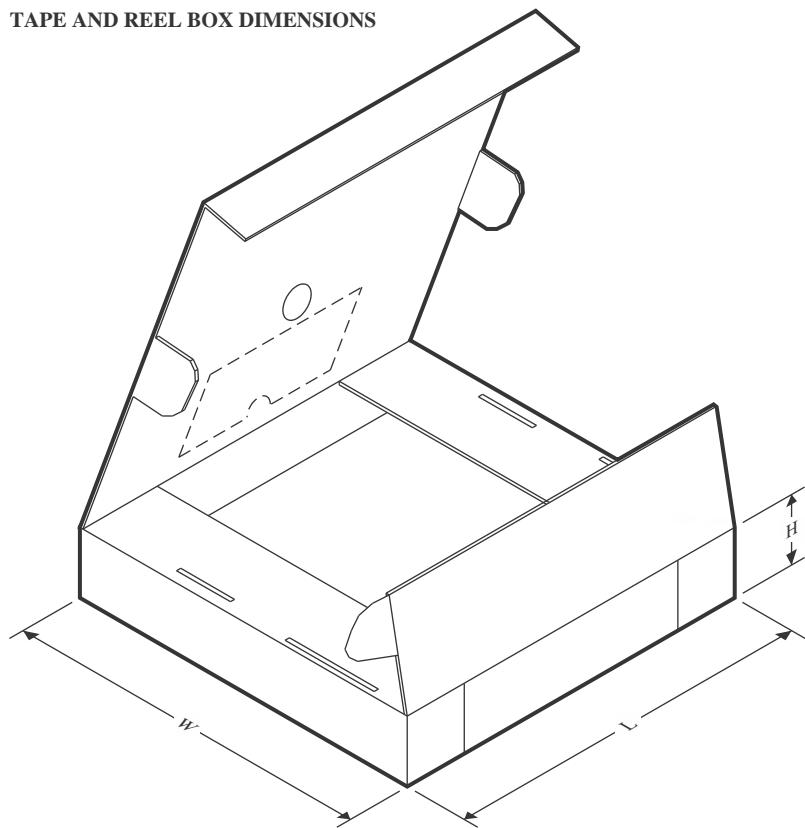
### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G17DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G17DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G17DBVR	SOT-23	DBV	5	3000	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G17DBVRG4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G17DBVT	SOT-23	DBV	5	250	178.0	9.2	3.3	3.23	1.55	4.0	8.0	Q3
SN74LVC1G17DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74LVC1G17DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G17DBVTG4	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74LVC1G17DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G17DCKRG4	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G17DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74LVC1G17DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G17DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74LVC1G17DCKTG4	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74LVC1G17DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74LVC1G17DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G17DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74LVC1G17DSFR	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
SN74LVC1G17YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1
SN74LVC1G17YZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G17DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G17DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74LVC1G17DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G17DBVRG4	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74LVC1G17DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G17DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G17DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74LVC1G17DBVTG4	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74LVC1G17DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G17DCKRG4	SC70	DCK	5	3000	180.0	180.0	18.0
SN74LVC1G17DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G17DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G17DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74LVC1G17DCKTG4	SC70	DCK	5	250	180.0	180.0	18.0
SN74LVC1G17DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74LVC1G17DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74LVC1G17DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74LVC1G17DSFR	SON	DSF	6	5000	184.0	184.0	19.0

---

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G17YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0
SN74LVC1G17YZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0

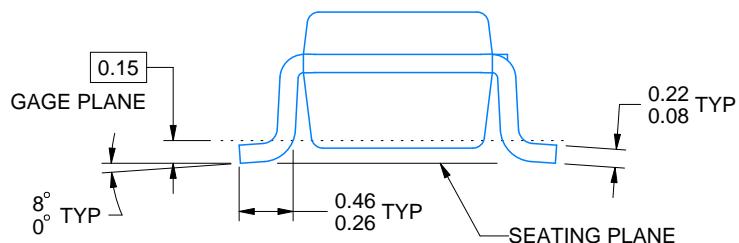
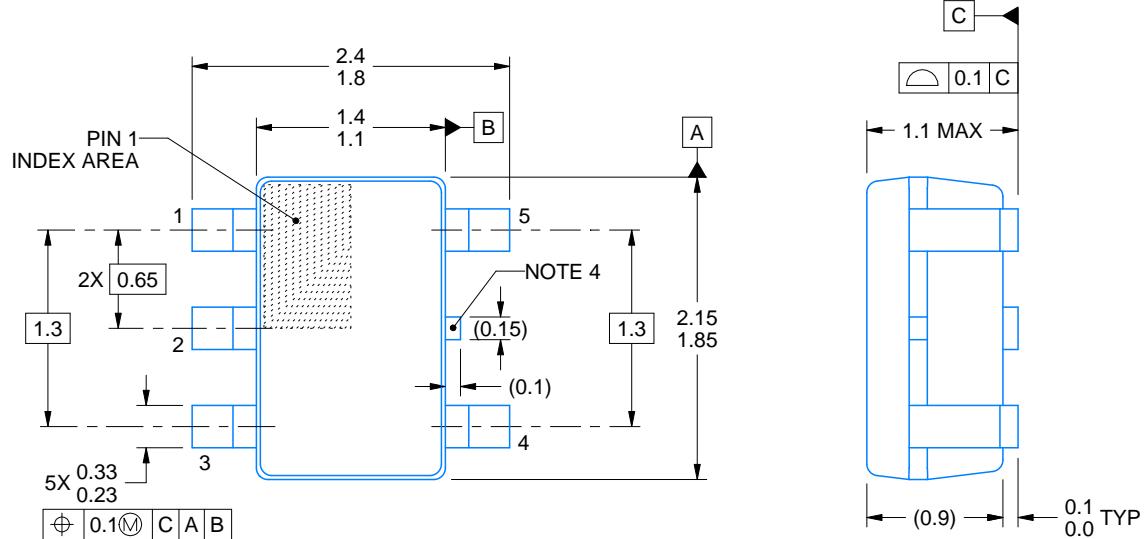
# PACKAGE OUTLINE

DCK0005A



## SOT - 1.1 max height

## SMALL OUTLINE TRANSISTOR



4214834/C 03/2023

## NOTES:

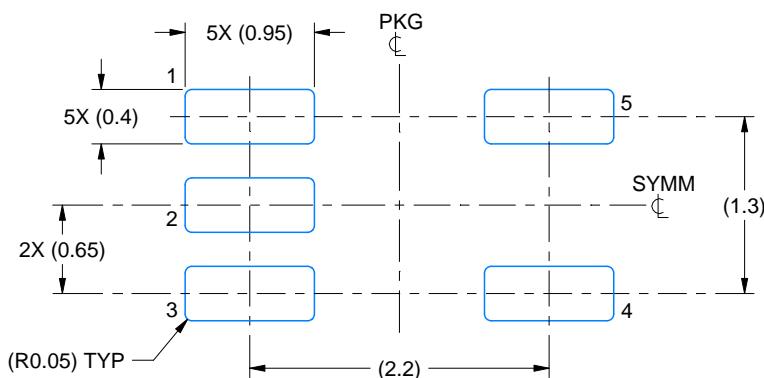
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.
  3. Reference JEDEC MO-203.
  4. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

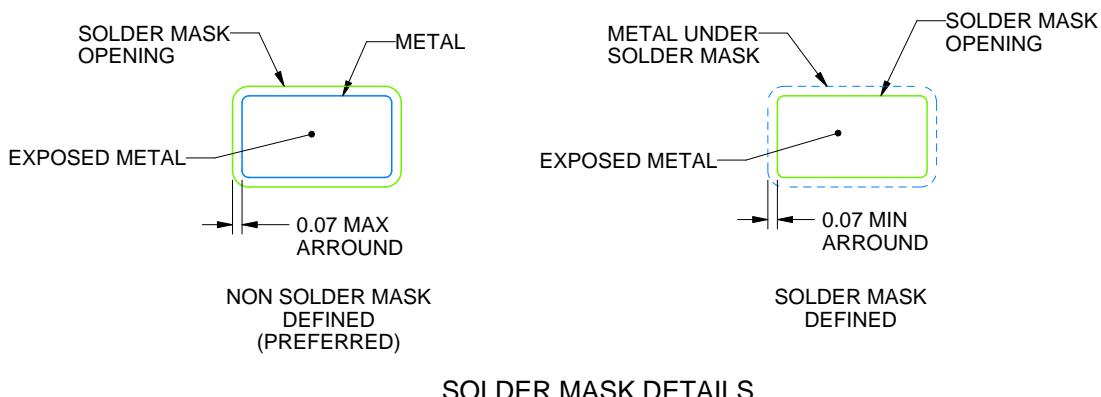
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/C 03/2023

NOTES: (continued)

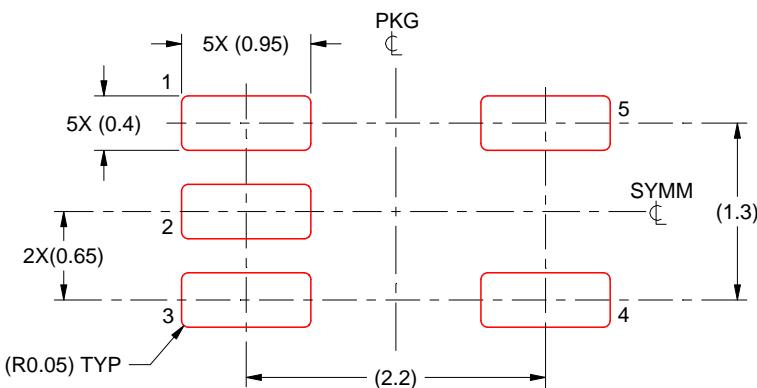
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214834/C 03/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

**DRY 6**

**GENERIC PACKAGE VIEW**

**USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4207181/G

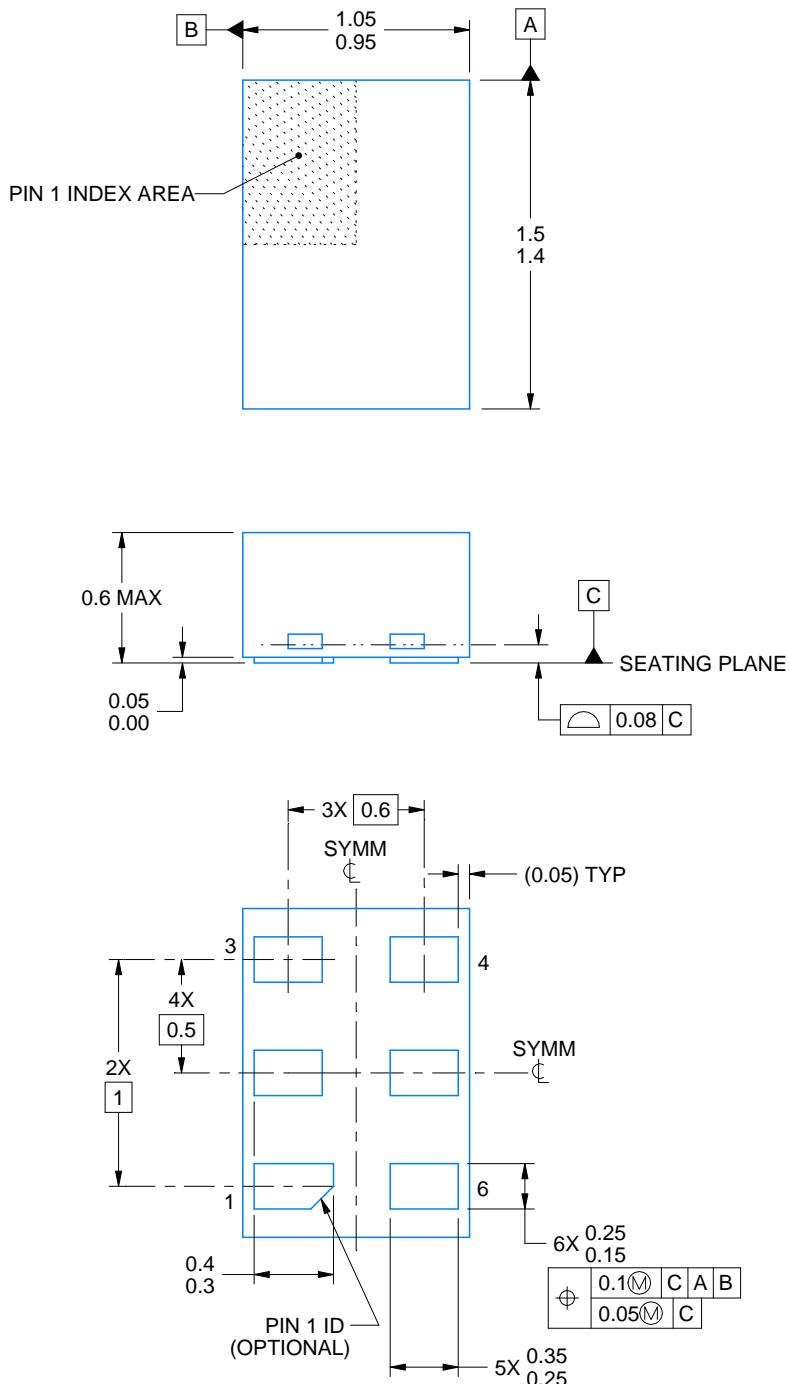
# PACKAGE OUTLINE

**DRY0006A**



## **USON - 0.6 mm max height**

## PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

## NOTES:

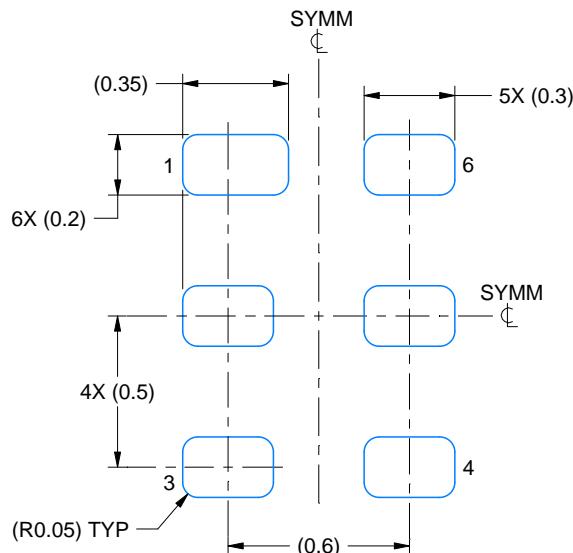
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

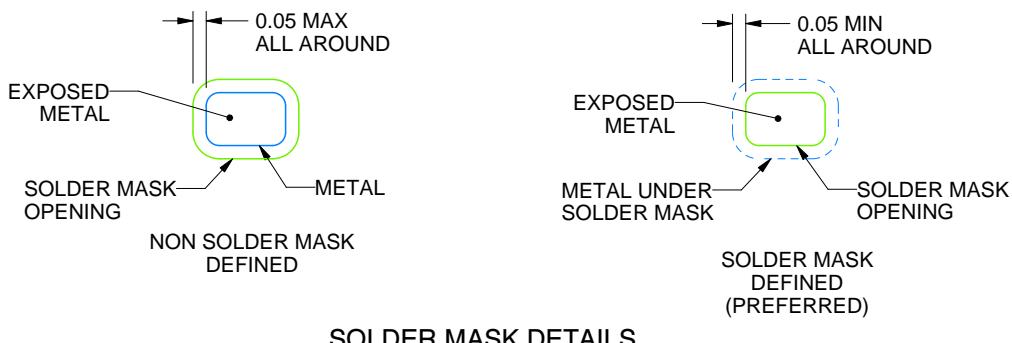
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
1:1 RATIO WITH PKG SOLDER PADS  
EXPOSED METAL SHOWN  
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

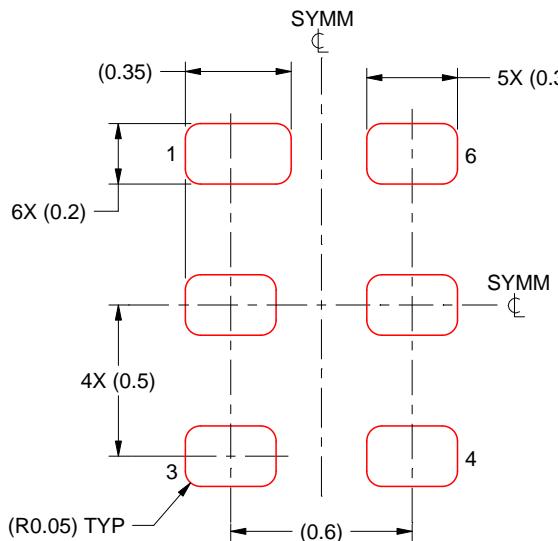
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

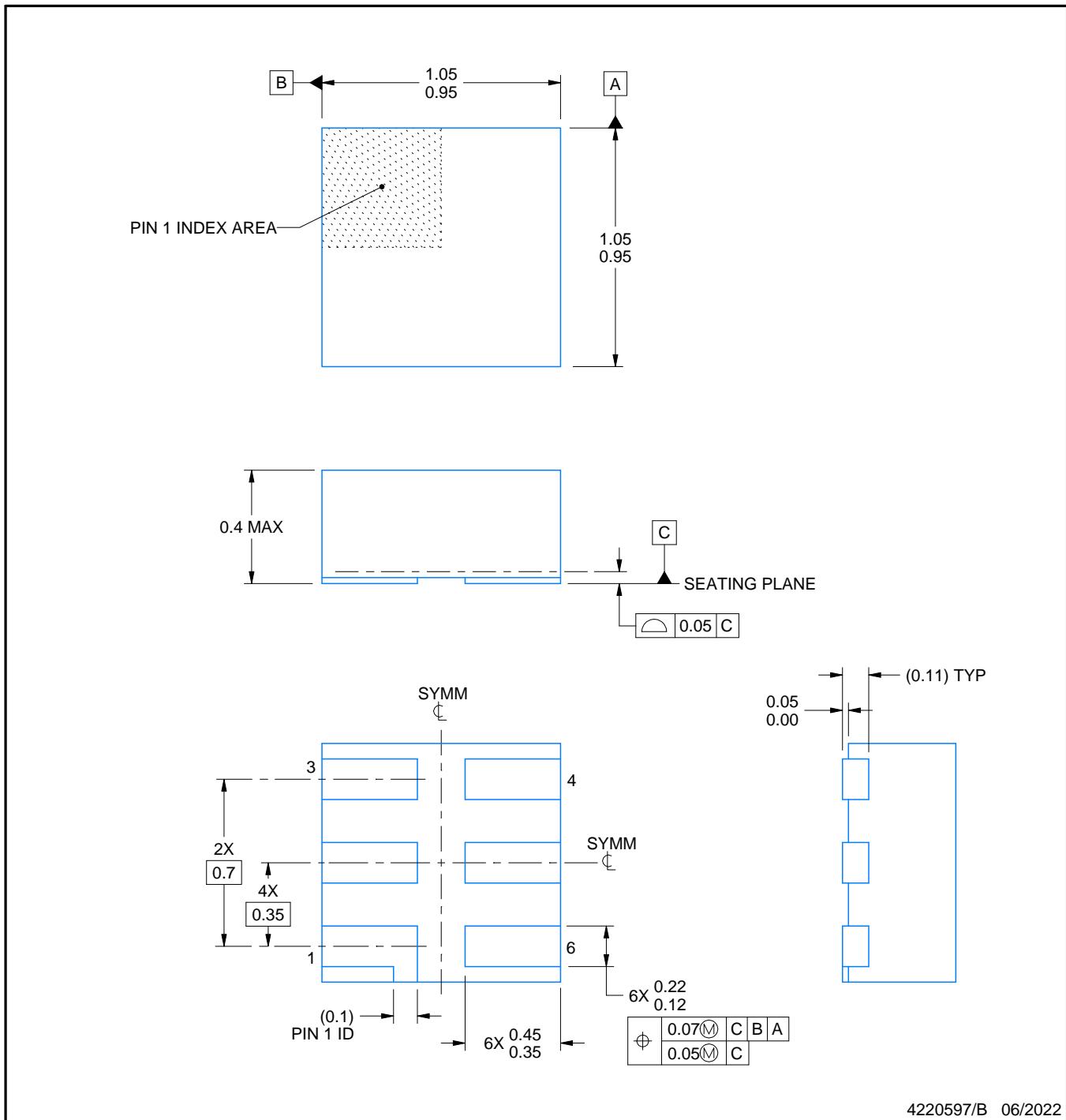
**DSF0006A**



# PACKAGE OUTLINE

## X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220597/B 06/2022

### NOTES:

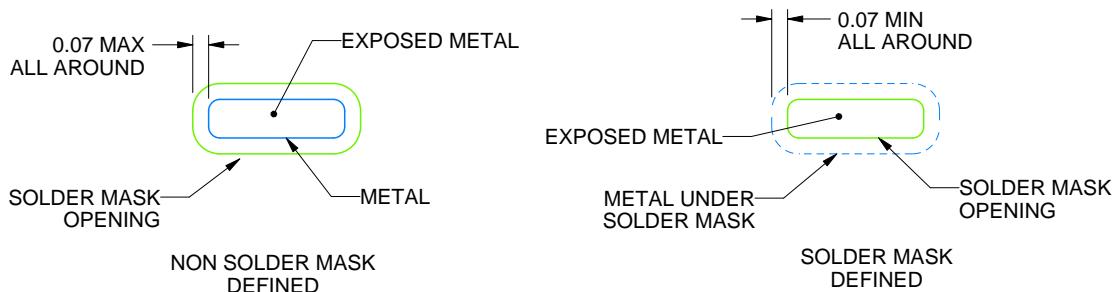
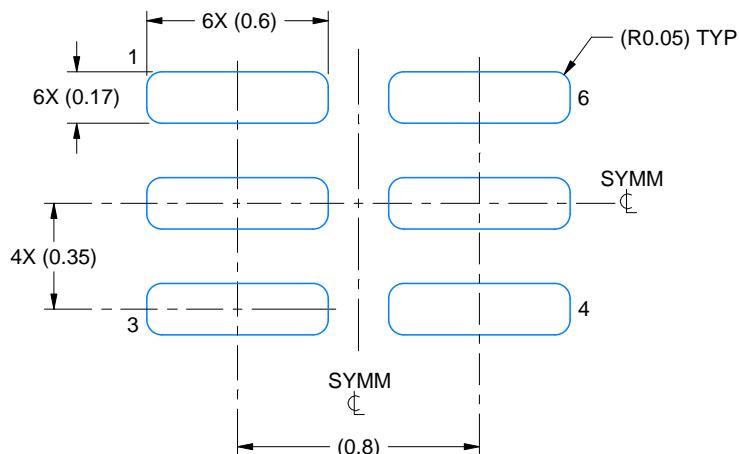
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

# EXAMPLE BOARD LAYOUT

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4220597/B 06/2022

NOTES: (continued)

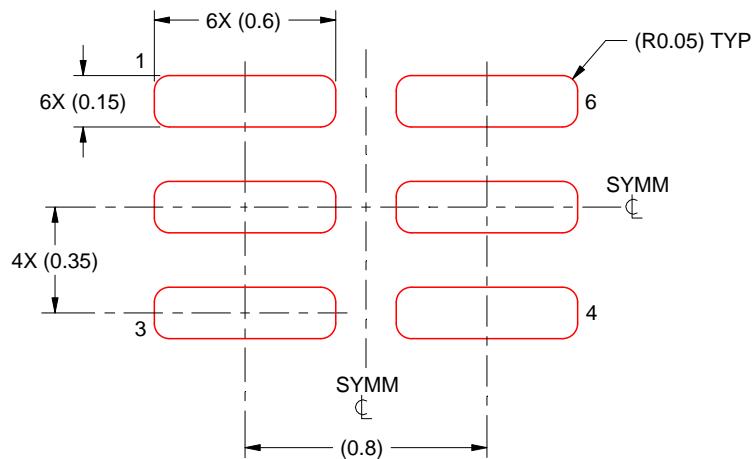
4. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:40X

4220597/B 06/2022

- Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

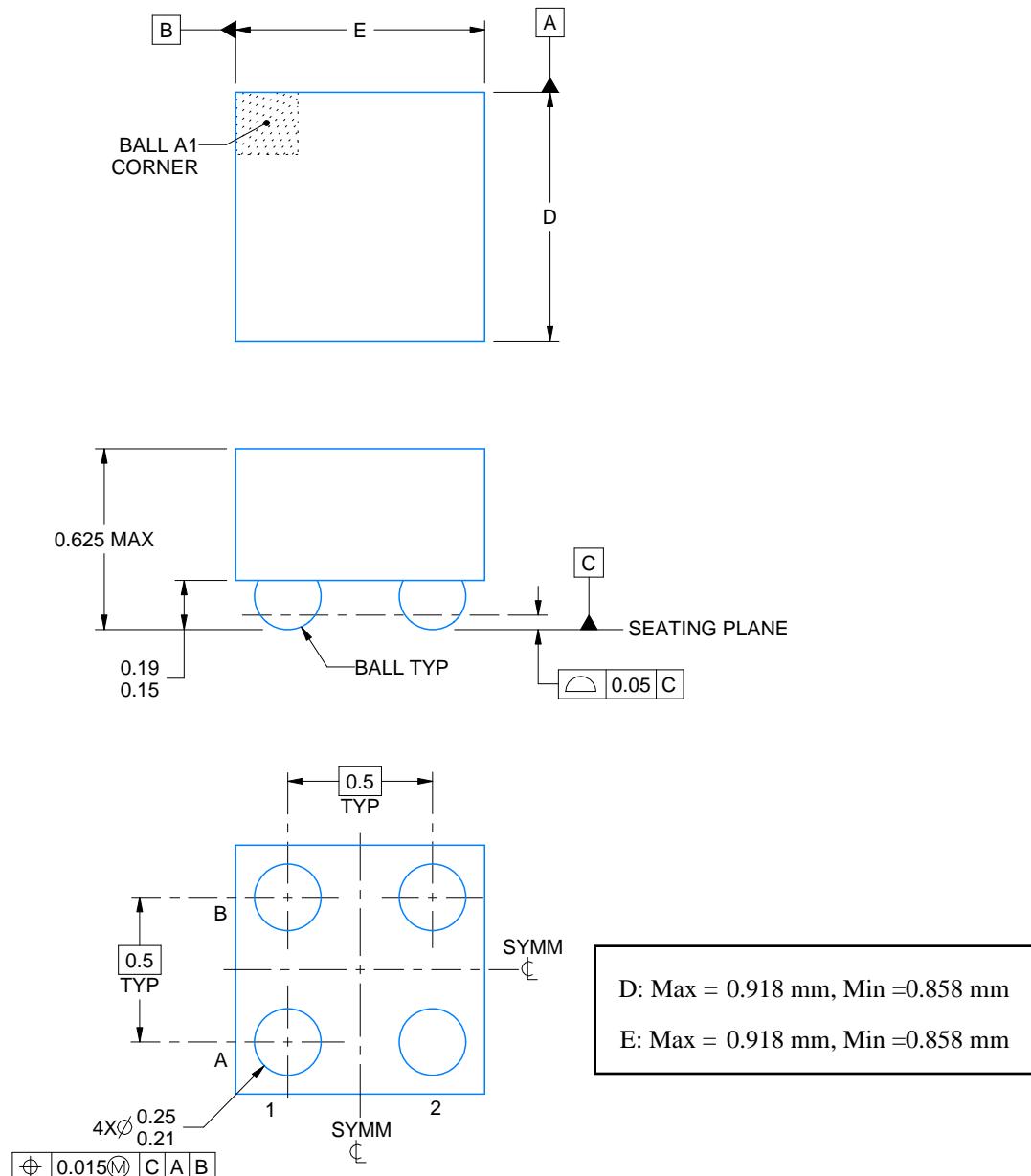


# PACKAGE OUTLINE

YZT0004

## **DSBGA - 0.625 mm max height**

#### DIE SIZE BALL GRID ARRAY



4219477/A 05/2017

## NOTES:

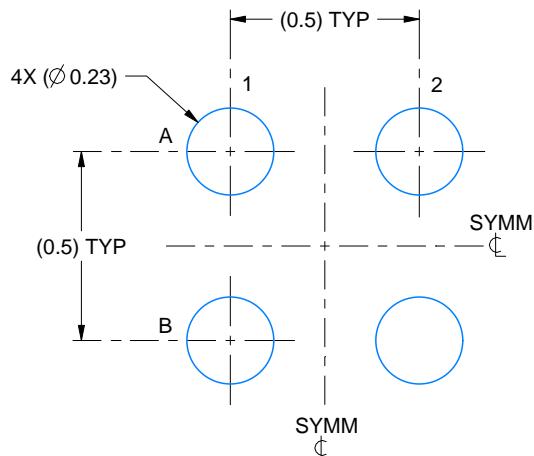
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
  2. This drawing is subject to change without notice.

## **EXAMPLE BOARD LAYOUT**

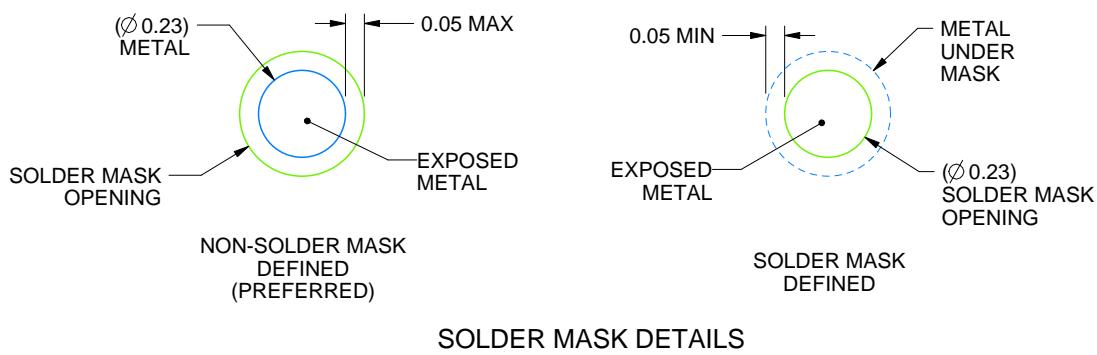
YZT0004

## **DSBGA - 0.625 mm max height**

DIE SIZE BALL GRID ARRAY



**LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:50X**



4219477/A 05/2017

#### NOTES: (continued)

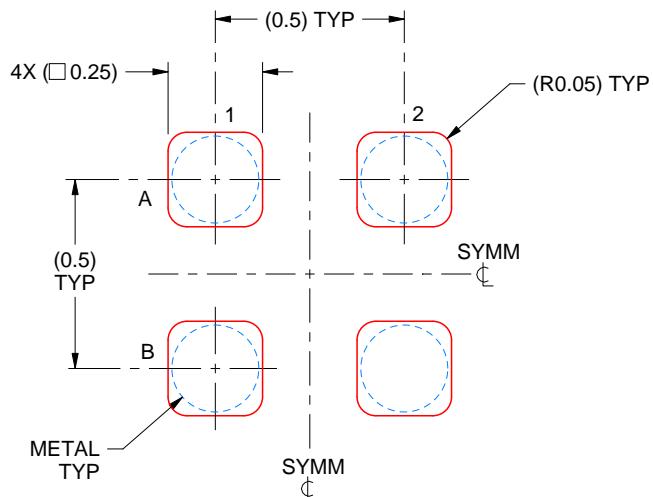
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.  
Refer to Texas Instruments Literature No. SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZT0004

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:50X

4219477/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

**DPW 5**

**GENERIC PACKAGE VIEW**

**X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD

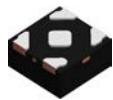


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4211218-3/D

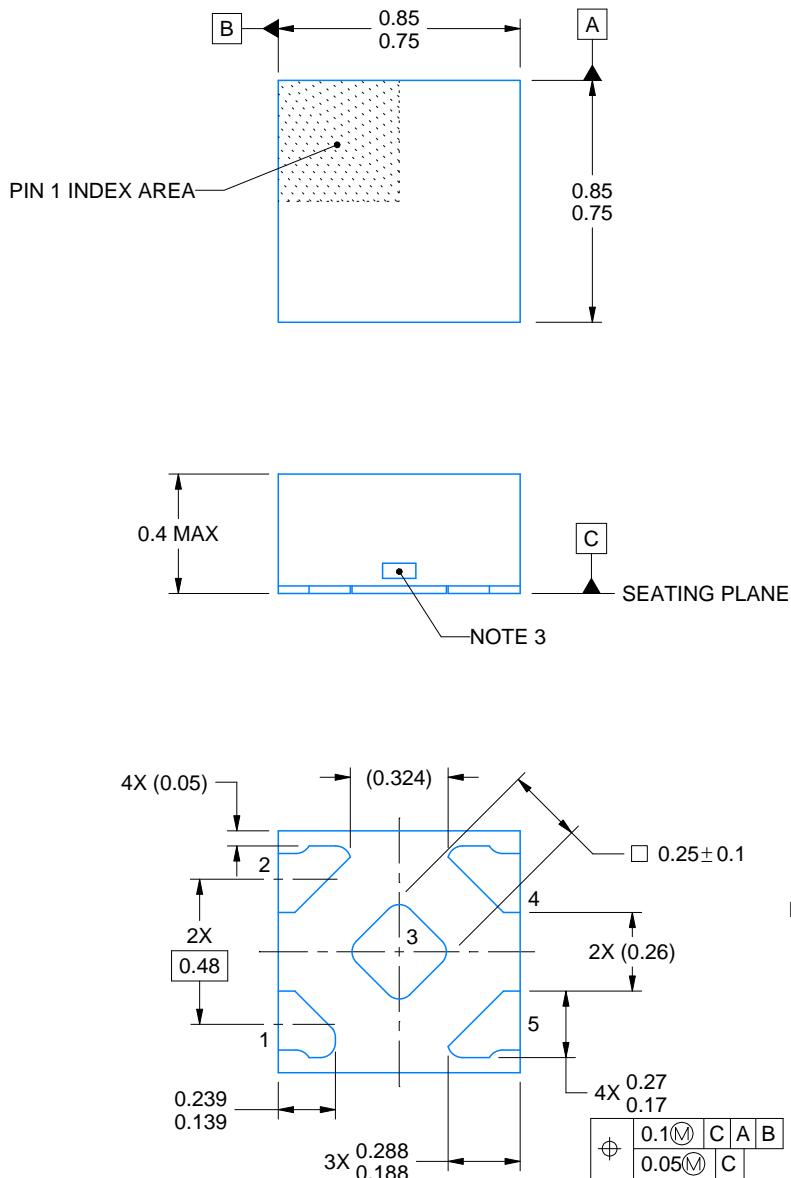
# PACKAGE OUTLINE

**DPW0005A**



**X2SON - 0.4 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



4223102/D 03/2022

NOTES:

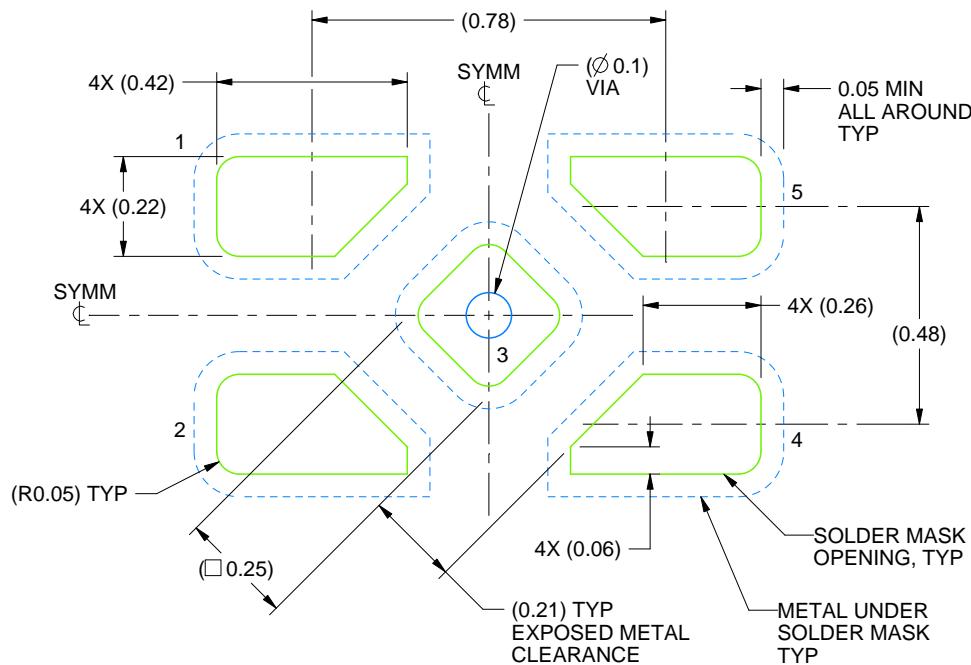
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

## **EXAMPLE BOARD LAYOUT**

**DPW0005A**

## **X2SON - 0.4 mm max height**

## PLASTIC SMALL OUTLINE - NO LEAD



# LAND PATTERN EXAMPLE

## SOLDER MASK DEFINED

### SCALE:60X

4223102/D 03/2022

#### NOTES: (continued)

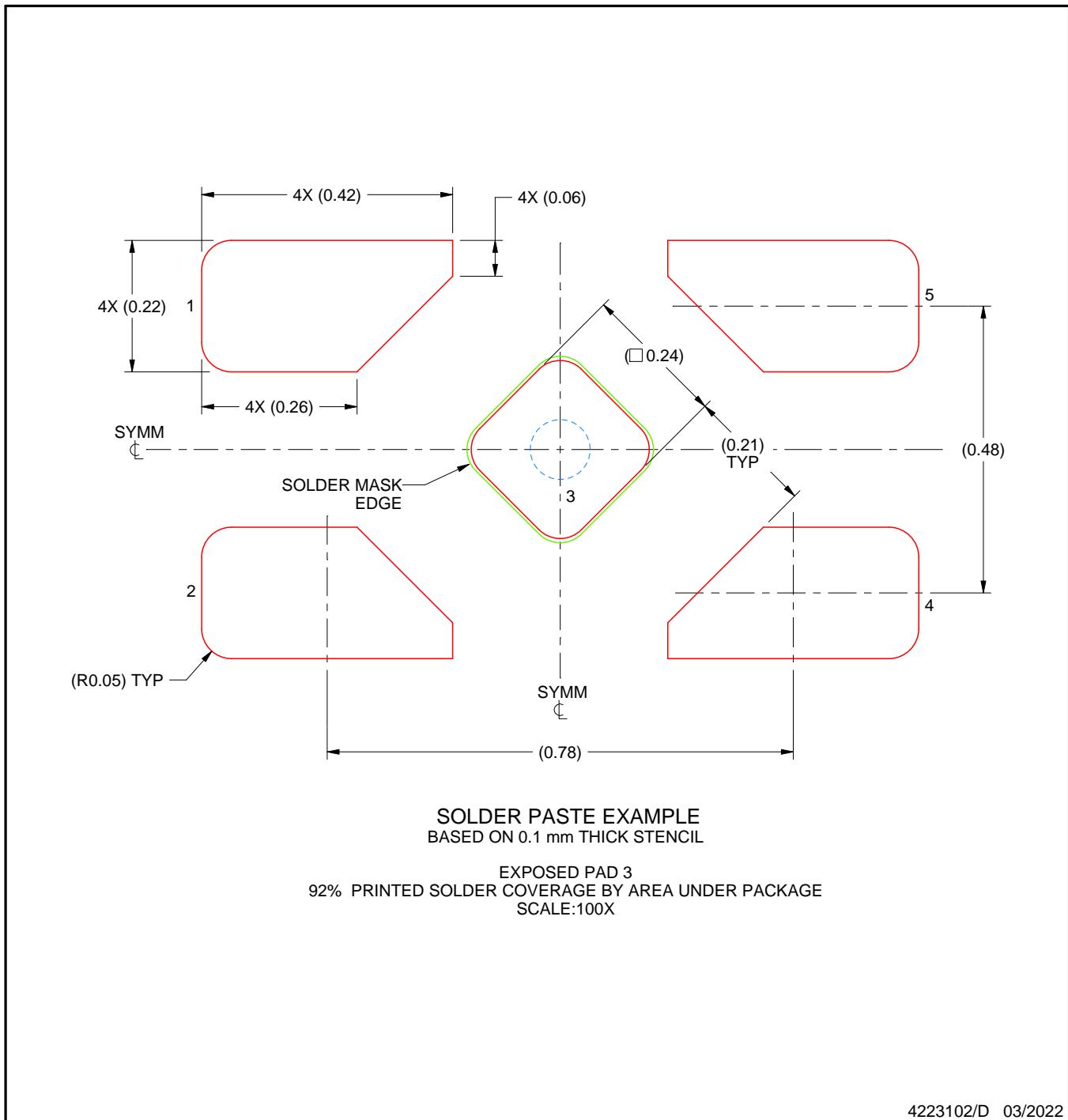
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

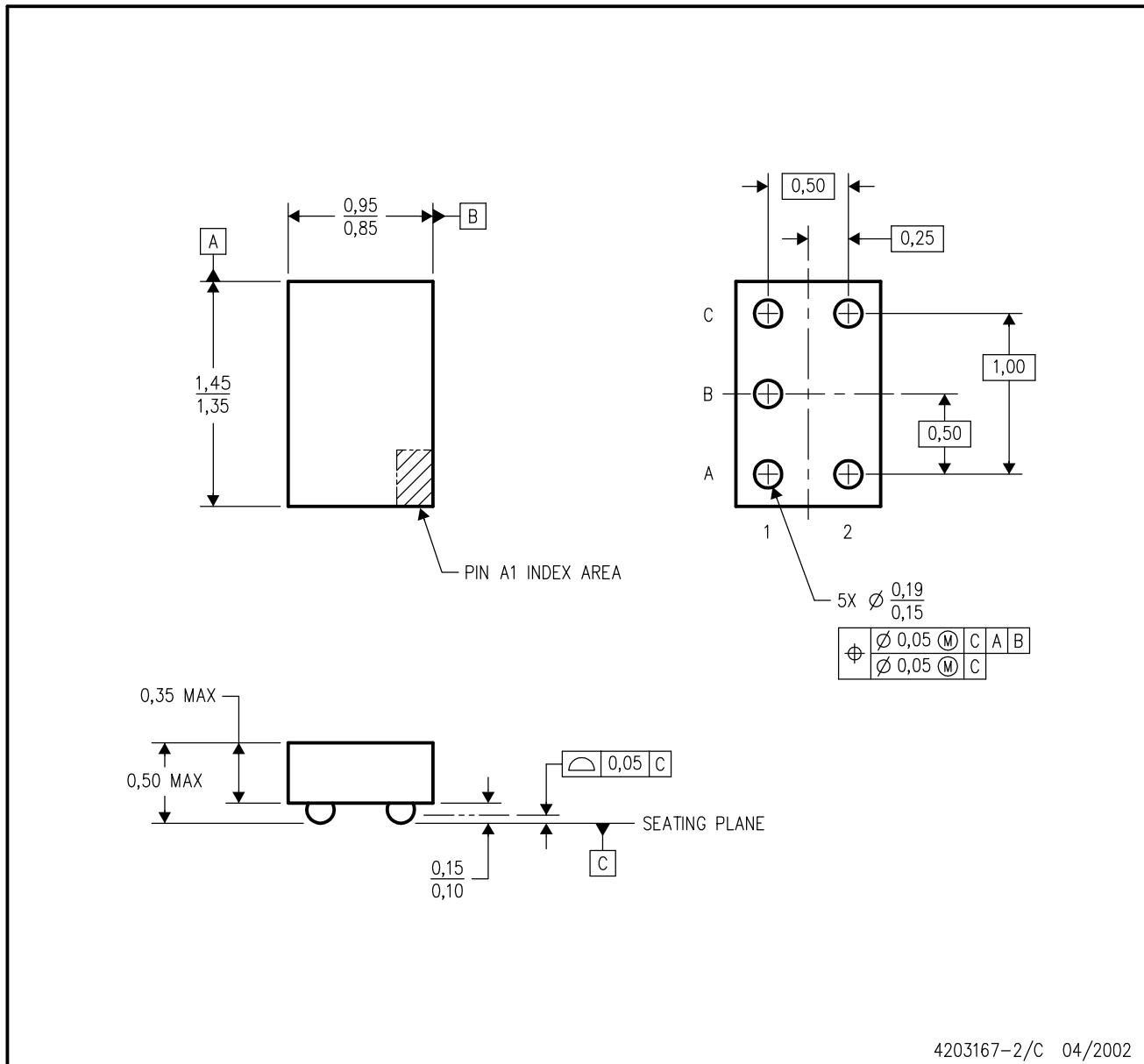


NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## YEA (R-XBGA-N5)

## DIE-SIZE BALL GRID ARRAY



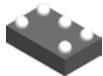
4203167-2/C 04/2002

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - NanoStar™ package configuration.
  - Package complies to JEDEC MO-211 variation EA.
  - This package is tin-lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead-free.

NanoStar is a trademark of Texas Instruments.

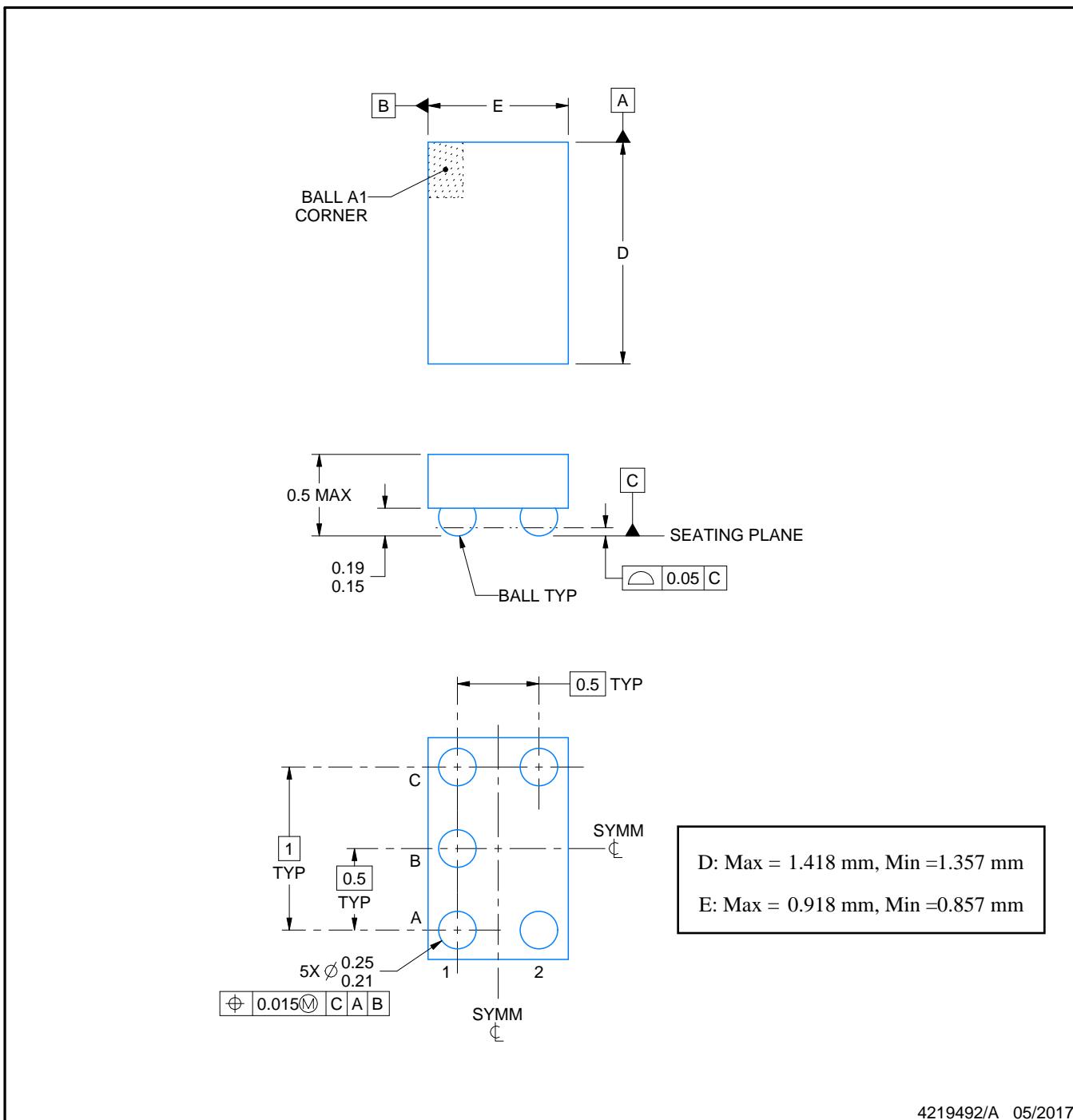
# PACKAGE OUTLINE

**YZP0005**



**DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



4219492/A 05/2017

## NOTES:

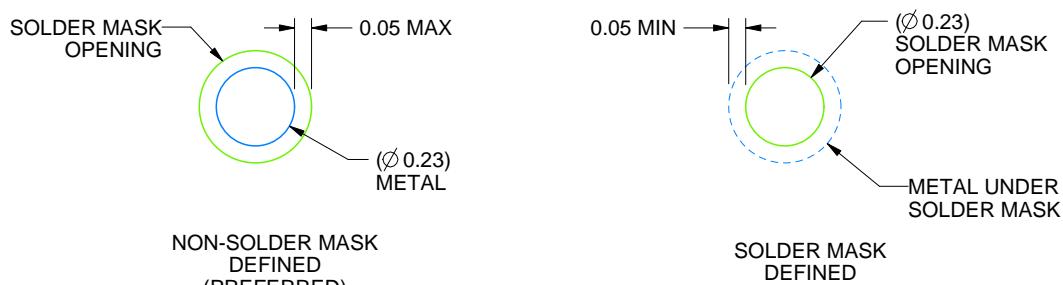
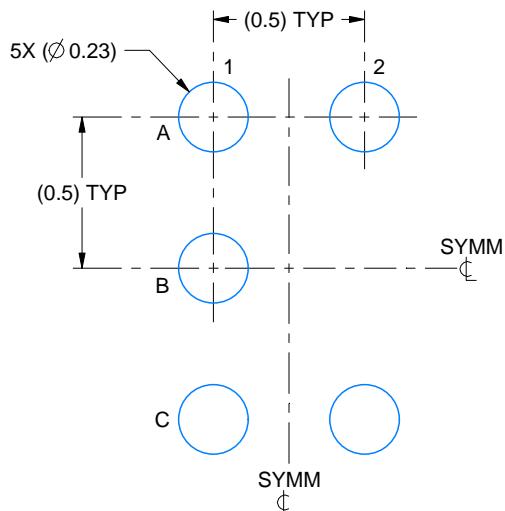
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER MASK DETAILS  
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

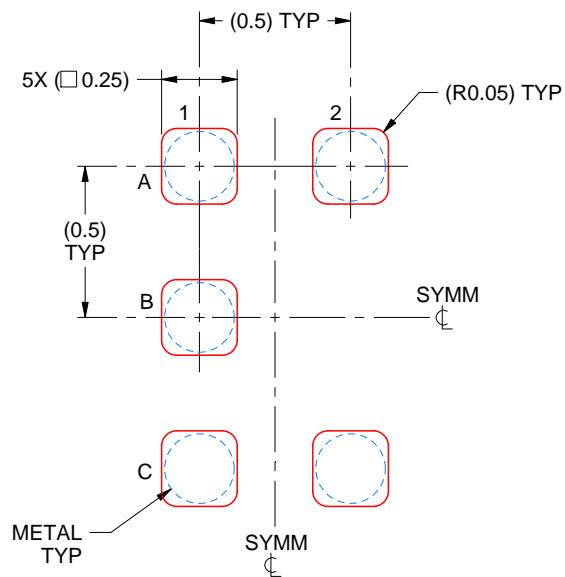
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.  
For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4219492/A 05/2017

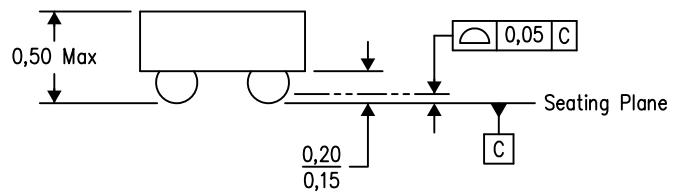
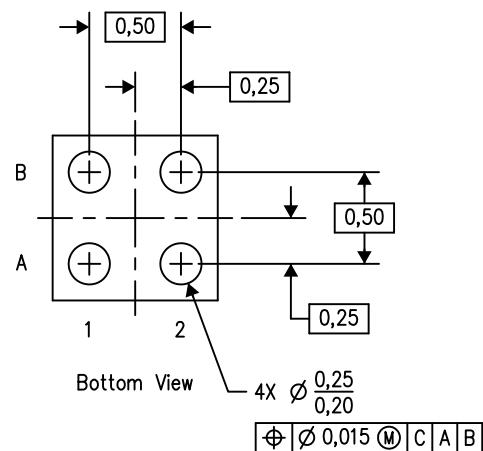
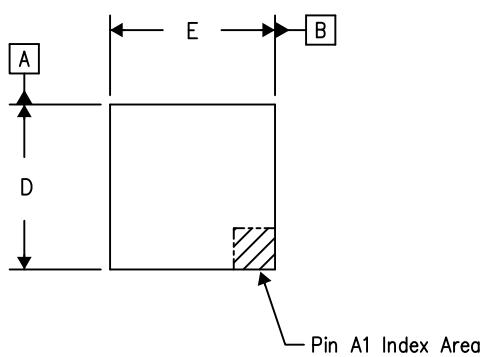
NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## MECHANICAL DATA

YZV (S-XBGA-N4)

DIE-SIZE BALL GRID ARRAY



D: Max = 0.918 mm, Min = 0.858 mm  
E: Max = 0.918 mm, Min = 0.858 mm

4206083/C 07/13

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

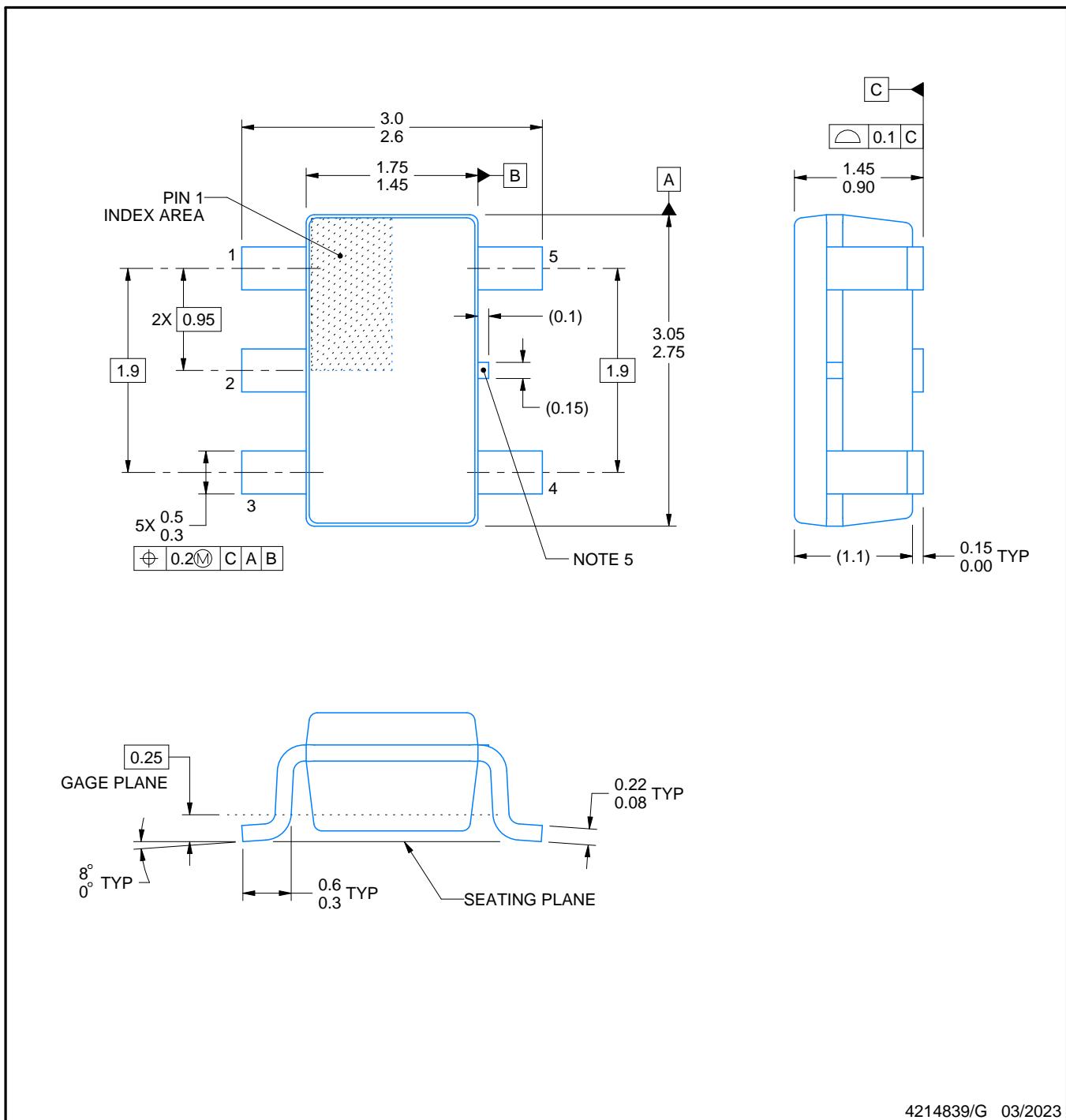
# PACKAGE OUTLINE

**DBV0005A**



**SOT-23 - 1.45 mm max height**

SMALL OUTLINE TRANSISTOR



**NOTES:**

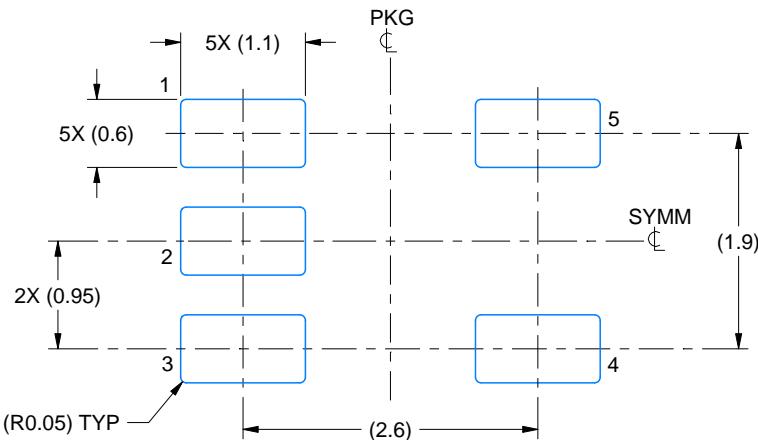
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

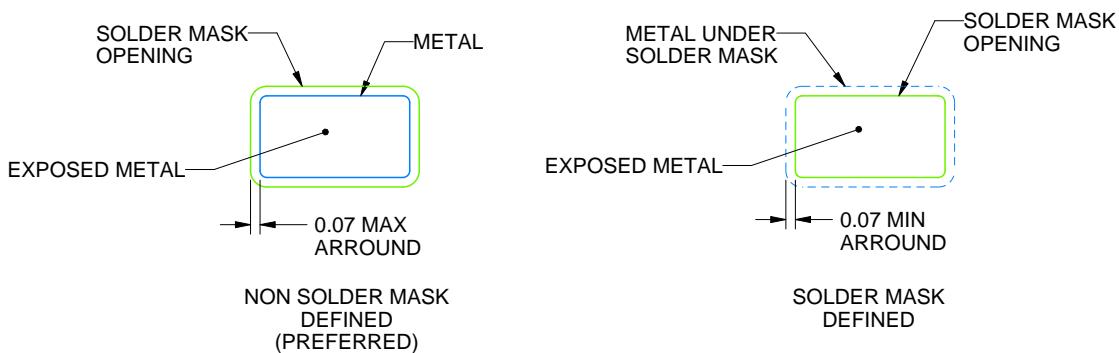
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/G 03/2023

NOTES: (continued)

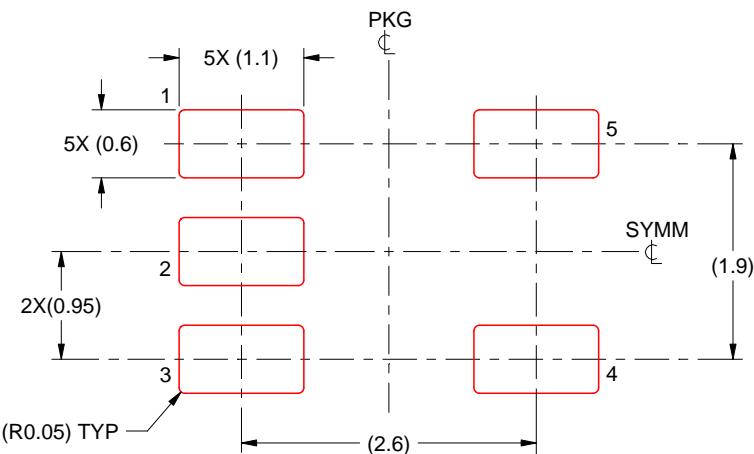
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/G 03/2023

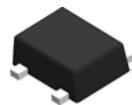
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

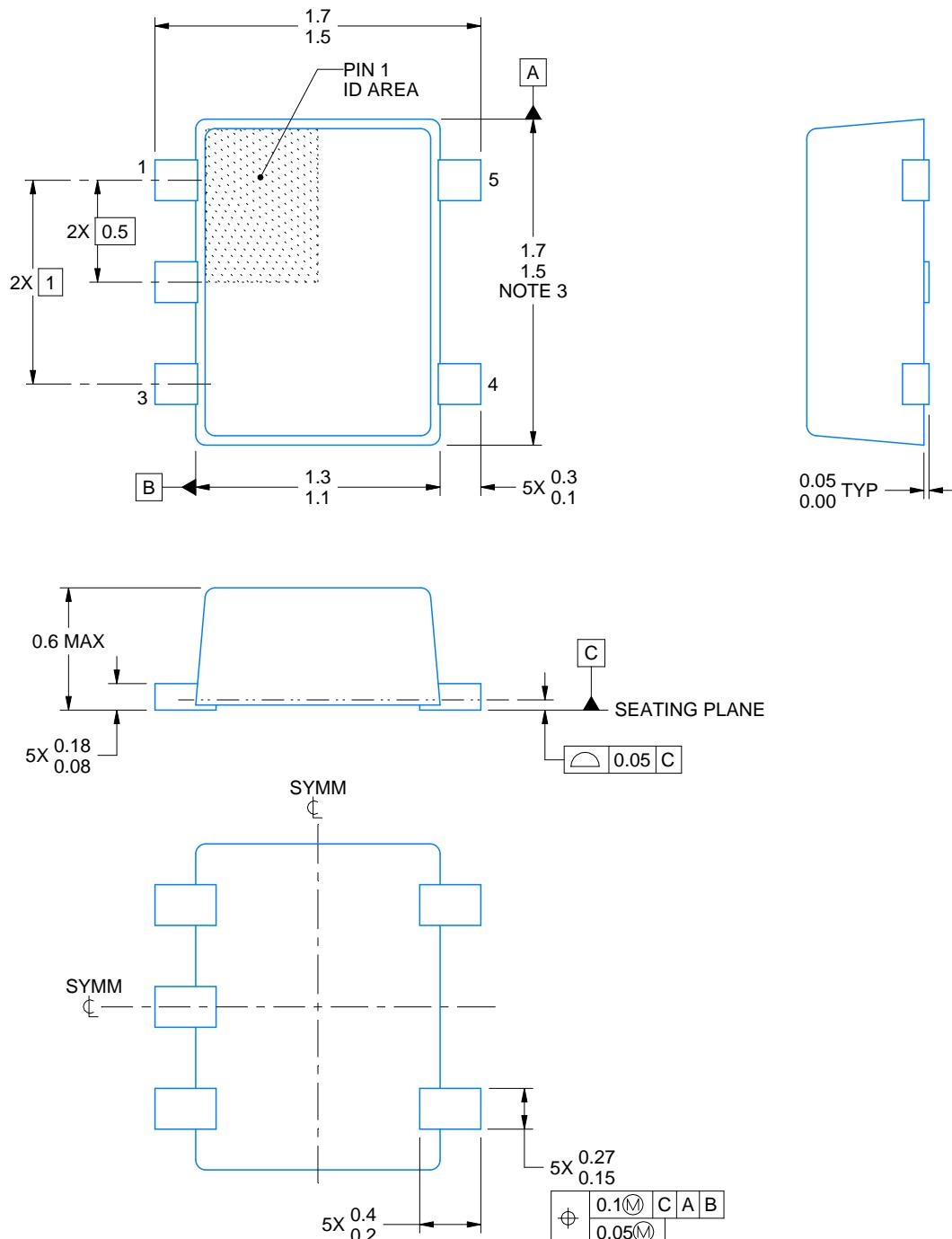
# PACKAGE OUTLINE

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



**DRL0005A**



4220753/B 12/2020

### NOTES:

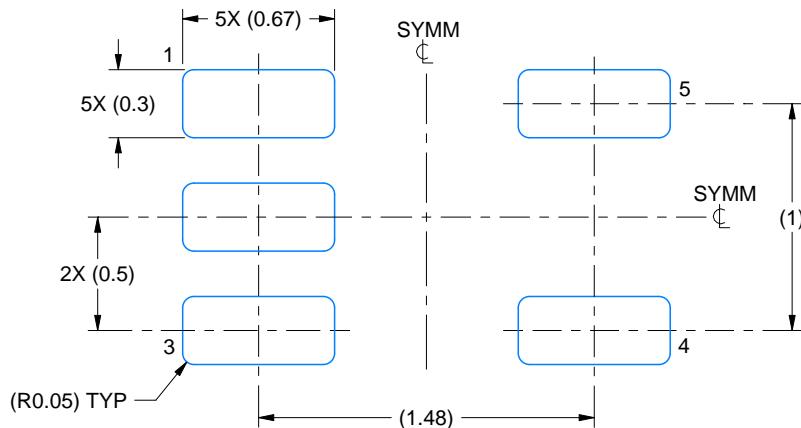
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

# EXAMPLE BOARD LAYOUT

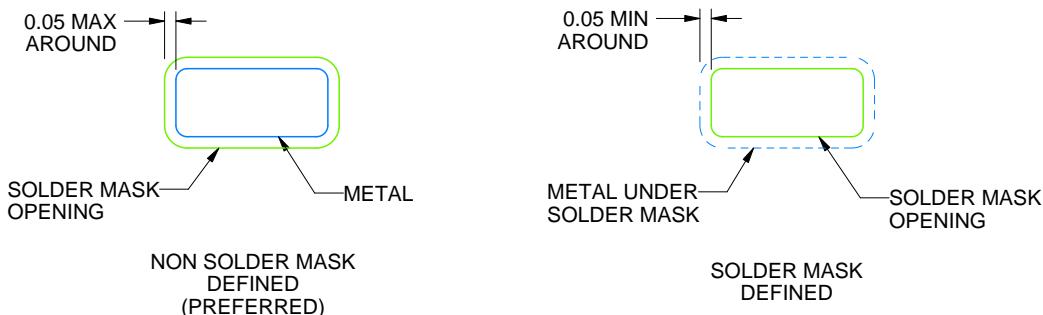
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



4220753/B 12/2020

NOTES: (continued)

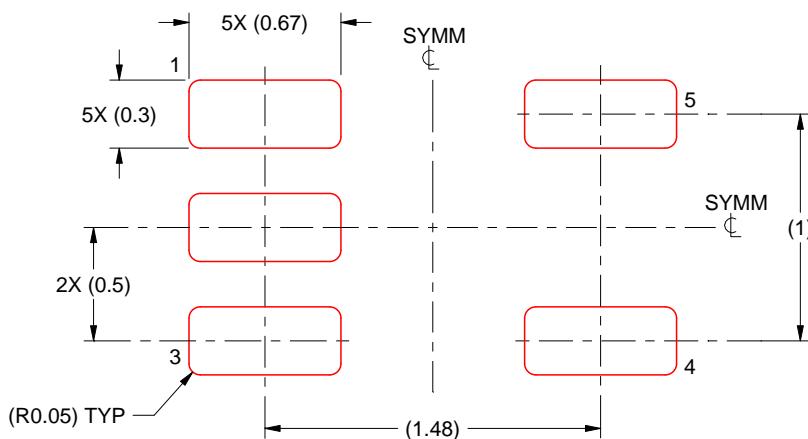
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

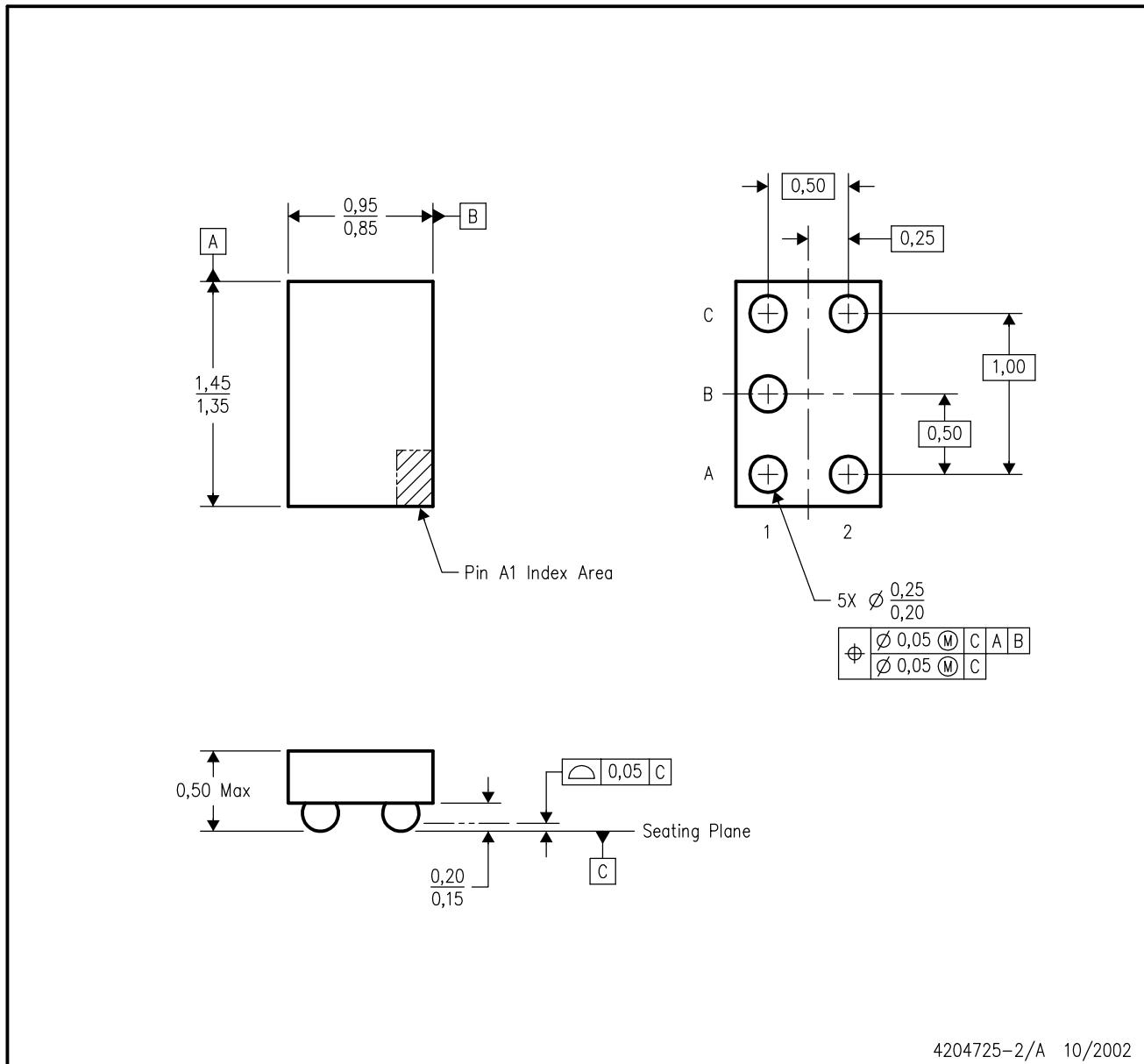
4220753/B 12/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## YEP (R-XBGA-N5)

## DIE-SIZE BALL GRID ARRAY



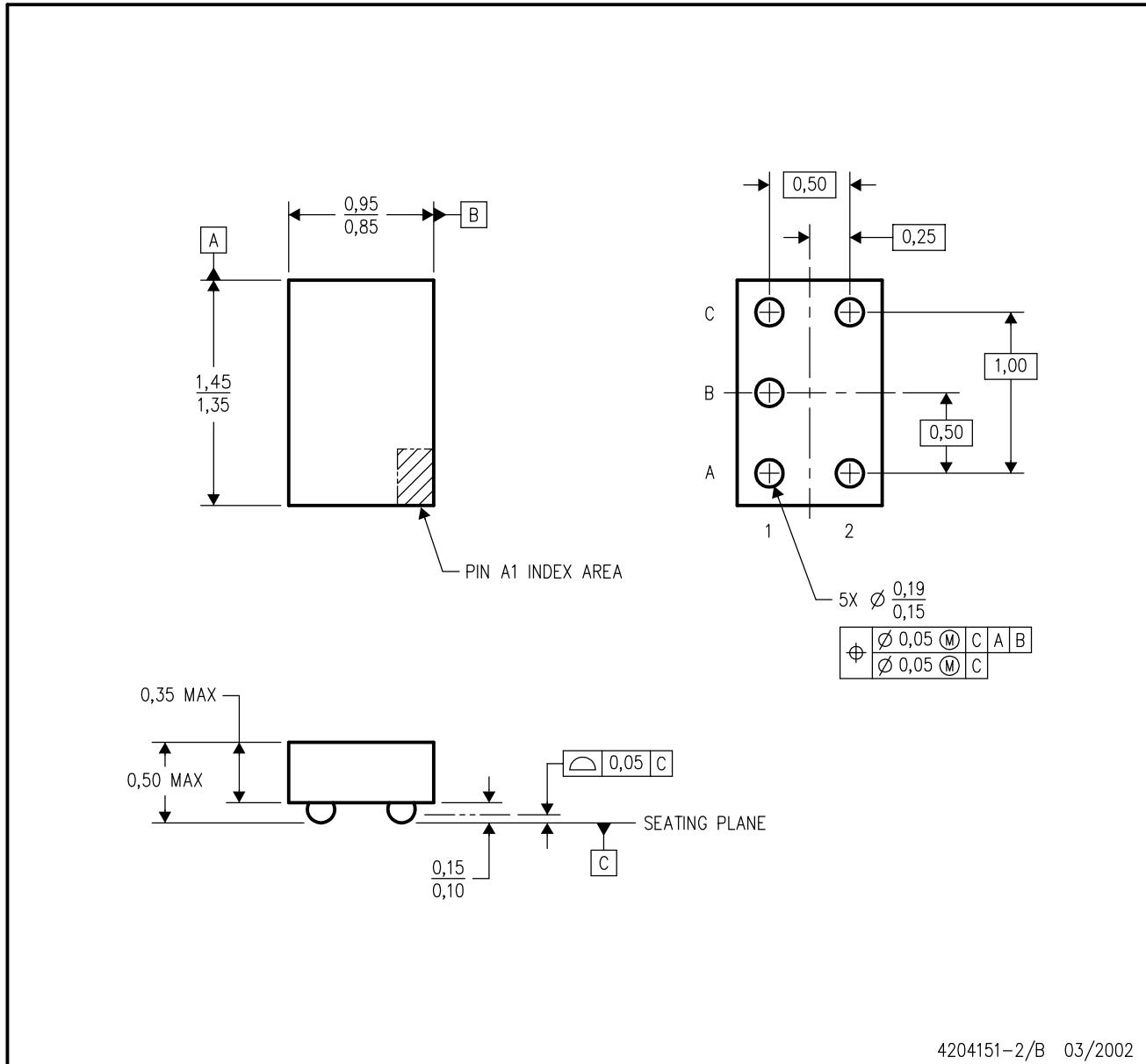
4204725-2/A 10/2002

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - NanoStar™ package configuration.
  - This package is tin-lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead-free.

NanoStar is a trademark of Texas Instruments.

## YZA (R-XBGA-N5)

## DIE-SIZE BALL GRID ARRAY



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - NanoFree™ package configuration.
  - Package complies to JEDEC MO-211 variation EA.
  - This package is lead-free. Refer to the 5 YEA package (drawing 4203167) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

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