

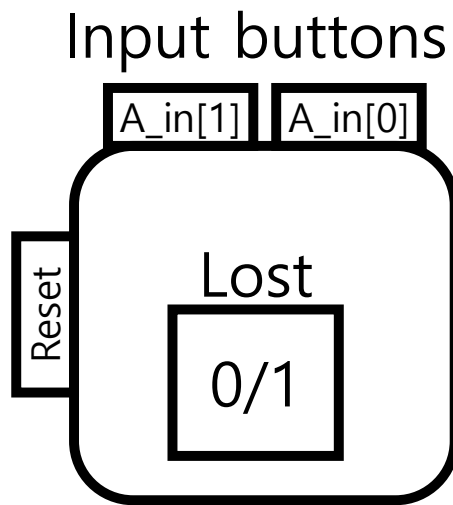
HW#7. Due 11/27 Sat 11:59 PM

- Submit a hand-written pdf for problem 1-3.
- Submit a zipped vhd files for problem 4.
- The name of the zip file should be **your_id.zip**
- The top entity vhd file should be **top_moore.vhd** and **top_mealy.vhd**
 - Use any number of vhd files of any name as submodules
- When naming a signal for any module, avoid using 'reserved words'.
- **Stick to the given port names.** We will use an automatic grader and your answer will be wrong if you use a wrong port name. Case-insensitive.



- (a) Given a JK Flip Flop, design a T (toggle) flip flop. Explain how you derived the answer.
- (b) Given a T (toggle) Flip Flop, design a JK flip flop. Explain how you derived the answer.

3. [FSM - Even/Odd Game]



You founded a startup that makes a gaming toy. The rule for the game is as follows:

- People sit down in a circle.
- After pressing the reset button, the game starts. Each person is given 10-seconds turn to input a 2-bit number using the buttons.
- The first person inputs any number and hold until the end of 10-second period.
- The second person inputs any number and hold until the end of 10-second period.
- **If your previous player inputted an even number, you should input an odd, number, and vice versa.**
- The device outputs '1' if it detects an even-even sequence, or an odd-odd sequence, indicating that the person lost.
- The game goes on even though someone lost, there is no stopping.

The above device is a simple example for an FSM, which detects even-even sequence or an odd-odd sequence out of 2-bit inputs. Assume the following.

- A. The reset is synchronous, active-high.
- B. A clock signal with 10-seconds period is provided.
- C. 'Odd number' means "01" and "11", while 'even number' means "00" and "10".
- D. Output is a single bit signal, '0' for okay, '1' for lost (pattern detected)

- (a) Draw a state diagram of a Moore machine.
- (b) Draw a state transition table for (a).
- (c) Draw a state diagram of a Mealy machine.
- (d) Draw a state transition table for (c).
- (e) After solving problem 4, paste screenshots of the testbench results, and explain that your circuit is correctly working.

4. FSM – VHDL

- (a) Implement the moore machine from problem 3. Write a testbench yourself, and verify that your circuit works.
- (b) Implement the mealy machine from problem 3. Write a testbench yourself, and verify that your circuit works.

Specifications:

- When writing a testbench, you don't have to bother making a 10-second period. It was just an example. Just input a clock of any period.
- You don't have to submit your testbench. We will use our own. In case yours do not work with our testbench, we will ask separately you for partial credits.
- Your circuit must be synthesizable from Quartus.
- The reset is synchronous, active-high.
- The name of the input ports:
 - A_in[1 downto 0]
 - reset, clk
- The name of the output port:
 - lost
- Web searching for general things are fine: e.g., how to write FSM in VHDL, how to write testbench in VHDL, how to implement clock, etc. However, don't copy-and-paste anything.
- If you are not sure about anything, ask us before doing it.