CV

Mathieu Léonardon

Ph.D. in Electronics

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Education

2015 - 2018 **PhD Student in Electronics**,
Université de Bordeaux, *IMS Laboratory*, *France*,
Polytechnique Montréal, *Electrical Engineering Department*, *Canada*

- **Title:** Polar decoding on programmable architectures.
- **Keywords:** Polar Codes, Software decoder, ASIP, Algorithm-Architecture Adequation
- **Teaching:** 45 hours at Bordeaux INP Engineering School
- **Defense date:** December 13, 2018
- **Jury:**

Pr.	Mohamad Sawan	Polytechnique Montréal	President
Pr.	Amer Baghdadi	IMT Atlantique	Member
Pr.	Emmanuel Casseau	Université Rennes 1	Member
Dr.	Olivier Muller	Grenoble INP	Member
Pr.	Charly Poulliat	INP Toulouse	Member
Dr.	Camille Leroux	Bordeaux INP	Supervisor
Pr.	Christophe Jégo	Bordeaux INP	Director
Pr.	Yvon Savaria	Polytechnique Montréal	Director

2012 - 2015 **Engineer Degree**, *Bordeaux INP*, *Talence*, *France*

- Embedded Electronics Systems (SEE), Apprenticeship

2011 - 2012 **University Diploma of Technology**, *IUT Paul Sabatier*, *Toulouse*, *France*

- Physical Measures

Professional Experience

2018 - 2019 **Teaching Assistant**, *Bordeaux INP*, *IMS Laboratory*, *Talence*

- **Supervisors:** Christophe Jégo (IMS), Camille Leroux (IMS)
- **Subject:** Software and hardware implementations of polar decoding algorithms
- **Teaching:** 192 hours at Bordeaux INP Engineering School

2012-2015 **Apprentice Engineer**, *Worldcast Systems*, *Mérignac*

- **Supervisor**: Hervé Garat
- **Main project**: Specification, design and development of a man-machine interface
- **Side project**: Board design and microcontroller programming for FM transmitters

Juillet-Août 2012 **Internship**, *I3S*, *Laroque-d'Olmes*

- **Supervisor:** Nicolas Antini and Franck Dedieu
- **Subject:** Design of an electronic gauge with display for measuring oil volume in tankers with a differential pressure sensor.

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Areas of expertise

Research themes

- *Signal processing*, digital communication chain, multiple access techniques, digital modulation
- *Algorithm-Architecture Adequacy*
- *Channel coding*: polar codes, LDPC codes, Turbocodes, algebraic codes
- *High-performance computing on general purpose processors*: SIMD, SMT, multinodes
- *Dedicated hardware architectures*: Xilinx design flow & Intel FPGA
- *ASIP Architectures*: Tensilica design flow, TCE (TTA-based Co-design Environment)
- *Software engineering*: object-oriented programming, continuous integration, versioning

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Communications

- *Teaching* engineers
- *Writing* scientific articles in French and English
- *Talking* at national and international conferences
- *Languages*: French (mother tongue), English (TOEIC 975) and German (elementary)

Tools

- *Operating systems*: Linux/Unix (preferred), Windows
- *Programming languages*: C/C++ (STL, Pthreads, OpenMP, MPI), JAVA, Python
- *Software*: Matlab, LaTeX, Office, Git, Vivado, Quartus

Publications

- **Manuscript**

[M1] **M. Léonardon**, "Décodage de codes polaires sur des architectures programmables", PhD thesis, Université de Bordeaux and Polytechnique Montréal, 2018.

- **International Journals**

[IJ1] A. Ghaffari, **M. Léonardon**, A. Cassagne, C. Leroux, and Y. Savaria, "Toward High Performance Implementation of 5G SCMA Algorithms", *IEEE Access*, 2018. DOI: 10.1109/ACCESS.2019.2891597.

[IJ2] **M. Léonardon**, A. Cassagne, C. Leroux, C. Jégo, L.-P. Hamelin, and Y. Savaria, "Fast and Flexible Software Polar List Decoders", *Springer Journal of Signal Processing Systems (JSPS)*, 2019. DOI: 10.1007/s11265-018-1430-3.

- **International Conferences**

[IC1] A. Cassagne, O. Hartmann, **M. Léonardon**, T. Tonnellier, G. Delbergue, C. Leroux, R. Tajan, B. Le Gal, C. Jégo, O. Aumage, and D. Barthou, "Fast simulation and prototyping with AFF3CT", in *International Workshop on Signal Processing Systems (SiPS)*, IEEE, 2017.

[IC2] A. Ghaffari, **M. Léonardon**, Y. Savaria, C. Jégo, and C. Leroux, "Improving performance of SCMA MPA decoders using estimation of conditional probabilities", in *International Conference on New Circuits and Systems (NEWCAS)*, 2017. DOI: 10.1109/NEWCAS.2017.8010095.

[IC3] **M. Léonardon**, C. Leroux, D. Binet, J. P. Langlois, C. Jégo, and Y. Savaria, "Custom Low Power Processor for Polar Decoding", in *International Symposium on Circuits and Systems (ISCAS)*, IEEE, 2018. DOI: 10.1109/ISCAS.2018.8351739.

[IC4] **M. Léonardon**, C. Leroux, P. Jääskeläinen, C. Jégo, and Y. Savaria, "Transport Triggered Polar Decoders", in *International Symposium on Turbo Codes and Iterative Information Processing (ISTC)*, IEEE, 2018. DOI: 10.1109/ISTC.2018.8625310.

- **French Conference**

[NC1] A. Cassagne, **M. Léonardon**, O. Hartmann, T. Tonnellier, G. Delbergue, V. Giraud, C. Leroux, R. Tajan, B. Le Gal, C. Jégo, O. Aumage, and D. Barthou, "AFF3CT : un Environnement de Simulation pour le Codage de Canal", in *GdR SoC2*, 2017.

Research

These works have all been realized during my 3-years thesis.

- **Polar Codes**

The main theme of my thesis was the decoding of polar codes. Polar codes are a recently invented class of error-correcting codes that are of interest to researchers and industry, as evidenced by their selection for the coding of control channels in the next generation of mobile telephony (5G). One of the challenges of future mobile networks is the virtualization of digital signal processing, and in particular channel encoding and decoding algorithms. In order to improve network flexibility, these algorithms must be described in software and deployed on programmable architectures. Such a network infrastructure makes it possible to better distribute the computational effort over all nodes and to improve cooperation between cells. These techniques are designed to reduce energy consumption, increase throughput and reduce communication latency. The work presented in the thesis manuscript focused on the software implementation of polar code decoding algorithms and the design of specialized programmable architectures for their execution.

- **Software implementation of decoding algorithms for polar codes on general purpose processors**

One of the main characteristics of a mobile communication chain is the instability of the communication channel. In order to address this instability, adaptive modulation and coding techniques are used in communication standards. These techniques require that decoders support a wide range of codes: they must be generic. The first contribution of this work is the software implementation of generic decoders of "Successive Cancellation List" (SCL) decoding algorithms on general purpose processors [IJ2]. The SIMD units present on modern processors make it possible to exploit the parallelism available in polar code decoding algorithms.

This first contribution involved the definition of two distinct concepts: the genericity and flexibility of a polar code decoder. Flexibility, on the one hand, is the ability of a decoder to adapt to a communications standard. Indeed, the parameters such as the size of a frame, the number of bits of information, the concatenation of a CRC code, the ability to manage punching patterns, are elements defined by the standard. A generic decoder must be able to support this genericity with respect to the encoding scheme. On the other hand, the flexibility of a polar code decoder corresponds to the possibility of adjusting the algorithm and implementation of the decoder in order to propose compromises between data rate and latency, for the same encoding scheme. Parameters that concern flexibility are for example the depth of the list for SCL algorithms, the representation format of integers (quantification) or the management of adaptive algorithmic variants of the SCL algorithm. The proposed decoder aims to be as generic and flexible as possible. The genericity and flexibility of the proposed decoder are superior to all state of the art implementations of list decoding algorithms, which are the algorithms with the best decoding performance.

In addition, algorithmic and implementation improvements are proposed, allowing to increase the performance of bit rates and decoding latency. Despite increased genericity and flexibility, the decoding rates achieved are higher (up to a factor of 5) than those in the literature. A version of the decoders proposed was also ported to ARM. It uses the SIMD NEON instruction set. While lower throughput are achieved, it is shown that power consumption on ARM is reduced compared to implementations on x86 architecture processors. The decoders are all integrated into the AFF3CT software suite (`https://aff3ct.github.io`). The source code is therefore made available to the scientific community and the results are easily reproducible.

- **ASIP decoder of polar codes: Customization of a processor**

The second contribution of my thesis work is the proposal of a new high-performance programmable architecture specialized in the decoding of polar codes [IC3]. It results from the following observation: if the data rates achieved by software decoders are high, especially when considering multi-core

architectures, their weak point is their energy consumption. Therefore, the challenge is to identify architectures that can maintain high flexibility while being more energy efficient. The ASIP (Application Specific Instruction set Processor) family of processors is an efficient and elegant solution.

The approach we first chose is the one proposed by the Cadence / Tensilica tools. A simple RISC processor is the basis of XTensa processors. This base can be configured. We have therefore eliminated the superfluous (floating point computing units, hardware accelerators for multiplication) and added parallel instructions (VLIW: Very Large Instruction Word). The instruction set of XTensa processors can also be extended, in conjunction with the definition of hardware units specialized in the application of interest to us, i. e. the decoding of polar codes. One of the advantages of this solution is that the algorithm is defined in software form, allowing for rapid development.

The consumption and occupied area metrics are then generated by the tool. A simulator is used to execute the algorithm and thus measure the number of cycles required to decode the frames. The results obtained show that this architecture achieves speeds and latencies close to state-of-the-art software implementations on general purpose processors. Energy consumption is reduced by an order of magnitude. Indeed, when considering decoding by successive cancellation of a polar code (1024,512), the energy required per decoded bit is about 10 nJ on general purpose processors versus 1 nJ on the proposed processor.

- **ASIP decoder of polar codes: Full design of a processor**

The third contribution of my thesis work is also a processor architecture with instruction set dedicated to the application. It addresses the same issue: to offer a flexible implementation by increasing throughput, latency and energy consumption performance. It differs from the previous one in that it uses an alternative design methodology. Instead of being based on a RISC architecture, the proposed processor architecture is part of the Transport Triggered Architectures (TTA) class. These architectures are made up of functional units that perform data operations (loading, saving, calculating) and transport buses that connect them. In a traditional processor architecture, the content of the instruction is the operation to be performed with the addresses of the input and output data. In TTA architectures, each bus is assigned an instruction during each cycle. Each instruction contains a source port and a destination port. This is called an exposed data path: the programmer (or compiler) can specify the data path for each instruction. This property allows fine optimizations of the implementation of an algorithm.

A suite of free development tools is available from Tampere University (`http://openasip.org/`). The latter allows to automate a large part of the design of such a processor and also offers a compiler that adapts to the specialized architecture. Thus, just like the previous ASIP, the decoding algorithm is described using a high-level language. The polar code decoder of TTA architecture realized was prototyped on FPGA and its synthesis was realized for an ASIC target in ST FD-SOI technology 28 nm [IC4]. The measured throughput are then higher than those obtained on general purpose processors. The energy consumption is reduced to about 0.1 nJ per decoded bit for a polar code (1024,512) with the successive cancellation decoding algorithm. This corresponds to a reduction of two orders of magnitude compared to the consumption measured on general purpose processors, and a reduction of one order of magnitude compared to ASIP using the Cadence / Tensilica tools.

- **Studies on Sparse Code Multiple Access decoder**

During my stay at Polytechnique Montréal, as part of my thesis work, I became interested in the implementation of a SCMA (Sparse Code Multiple Access) decoder. SCMA is a promising non-orthogonal multiple access technique for future communication standards. Alirezah Ghaffari proposed computational simplifications of the algorithm to accelerate decoding processing. In order to ensure the real performance of this simplification, we have integrated this SCMA decoder into a complete communication chain. It is also integrated into AFF3CT to make the source code available to the community and also to allow the results to be reproduced. This work is described in [IC2]. In a second step, we focused on accelerating the software implementation of these algorithms on general purpose processors, by using SIMD instruction sets [IJ1]. The use of SIMD units in conjunction with

the proposed simplifications allows significant gains in throughput and energy consumption, up to an order of magnitude.

- **Contribution to the AFF3CT project**

Since 2015, I have been contributing to the development of the AFF3CT project (`aff3ct.github.io`). This is a project that offers many software tools related to digital communications. Particular attention is paid to the throughput and latency performance of error-correcting code decoders.

Used as a simulator, it allows Monte Carlo simulations of the entire communication chain. The data are randomly generated, encoded, modulated, noisy, decoded, and the performance is estimated by measuring the Bit Error Rate (BER) and the Frame Error Rate (FER). The simulator's ambition is threefold:

1. **Reproducibility**: it is often difficult to reproduce the results of the literature. Many parameters can be omitted, which prevent a faithful reproduction of the proposed algorithms. This is why a large database of pre-simulated curves with all the necessary parameters is available. As a result, many research projects use AFF3CT as a reference. Being open-source, software descriptions are accessible to everyone.

2. **High-speed simulations**: in order to correctly estimate BER / FER, it is necessary to simulate a hundred erroneous frames for a signal-to-noise ratio value. When the FER to be simulated is low, for example 10^{-7}, about 1 billion frames must be simulated. When the frames are large, simulation times can be extremely long. It is therefore very useful to have high throughput simulations. This is why we use all the available parallelism: data parallelism, by using SIMD instructions, instruction parallelism, with the use of superscalar and multicore architectures, and finally the use of multiple nodes is ensured through the `openmpi` library. This allows very high throughput to be achieved. For example, 63 Gbps are reached for the FA-SCL decoder presented in [IJ2] on the miriel node of the PLAFRIM platform (`https://www.plafrim.fr/en/the-platform/hardware-documentation/`).

3. **Heterogeneity of algorithms**: in the field of error-correcting code decoders, there are very many decoding algorithms. It is therefore often very difficult to make an exhaustive comparison with the existing system. The ambition of AFF3CT is to cover as many algorithmic variants of the literature as possible to facilitate the work of researchers.

AFF3CT can also be used as a library. Thus, any developer can use the elementary bricks available. This possibility is widely used by our industrial partners (Airbus, Thales,...) to integrate AFF3CT blocks into their communication chains, whether for simulation or for real communicating systems (software radio).

Teaching

School	Level	Nb. of hours	Section
ENSEIRB-MATMECA	2015 - 2016	45 h	61
ENSEIRB-MATMECA	2018 - 2019	192 h	61
		237 h	

- **Electronics Design Project**

Person in charge: Mathieu Léonardon

Level : First year ENSEIRB - equivalent L3

Volume : 2 x 25 Hours

Content : The first part of this module is a course on FPGA design flow. The state machines are also presented and some exercises are proposed. This is followed by a project to design a digital architecture. The objectives are:

- design a hardware architecture,
- acquire VHDL skills,
- develop a synthetic mind for the writing of the report,
- acquire skills in project presentation with a defense.

The project is the realization of a Lotto on a Nexys 4 card. The end user must be able to draw 6 numbers at random, without removing them. These numbers are displayed on 7-segment displays.

Keywords: FPGA, VHDL, Digital Electronics

Personal participation: Integrated course, project supervision.

Educational resources created : https://bit.ly/2HLfaXt

- **Reconfigurable architecture**

Person in charge: Mathieu Léonardon

Level : Second year ENSEIRB-MATMECA - equivalent M1

Volume : 1 x 20 Hours

Content: Advanced design on FPGA circuits. Objectives :

- define reconfigurable architectures,
- understand their internal structure,
- understand how they work,
- implementation of advanced techniques,
- acquire skills in project presentation with a small defense.

Keywords: FPGA, VHDL, Digital Electronics

Personal participation: Integrated course, project management.

Educational resources created : https://bit.ly/2U4Ua4o

- **Digital Electronics**

Person in charge: Mathieu Léonardon

Level : First year ENSEIRB-MATMECA - equivalent L3

Volume : 1 x 25 Hours

Content: This module introduces the basics of digital electronics: numeration, Boolean algebra, combinatorial logic as well as sequential logic. Architecture and operation of a finite state machine. Basics of printed circuit board technology.

Keywords: Numbering, Finite state machine, CMOS technology, Digital electronics

Personal Participation: Integrated Course - Supervised works

Educational resources created : https://bit.ly/2U0hgsV

- **Combinatory logic and sequential logic**

Person in charge: Christophe Jégo

Level : First year ENSEIRB-MATMECA - equivalent L3

Volume : 1 x 32 Hours

Content :

- The elementary combinatorial and sequential functions used in digital circuits,
- the modeling of numerical functions using the VHDL language.

At the end of the course, the student must be able to:

- to describe a combinatorial function and represent it with a digital circuit,
- to describe and synthesize a counter, a state machine,
- to identify the critical path of a complex logical function and calculate its maximum operating frequency.

Six four-hour tutorial sessions of four full hours each. Each session is divided into two parts. Themes are dealt with in the first part. In a second part, the defined digital systems are described in the hardware description language VHDL. This approach gradually introduces students to this language.

Keywords: Digital electronics, VHDL, FPGA

Personal participation: Supervision of the practical works and the project

- **Microprocessor project**

Person in charge: Valéry Lebret

Level : First year ENSEIRB-MATMECA - equivalent L3

Volume : 1 x 36 Hours

Content: This course aims to program MICROCHIP PIC microcontrollers, chosen for their ease of implementation due to their low complexity. After a presentation of this family of microcontrollers and their specificities, the activity begins by writing simple programs in assembler language to illustrate the operation of the microcontroller (coding and execution of instructions, access to registers, management of internal resources and inputs/outputs, etc.). An application card integrating a PIC16F84 serves as a support, with software development being carried out using the MPLABX integrated tool chain, which includes a simulator. Programming is then carried out in C language with the purpose of implementing a project (e. g. a quartz clock on an LCD display) using the PICDEM2 development board with a PIC16F877 target (more internal resources, possibility of debugging). The focus is on the limitations encountered on embedded systems when programming in C language (reduced memory space, limited computing power, etc.) as well as on interrupt management.

Keywords: Microcontroller programming, assembly language

Personal participation : Supervision of practical works

- **Computer architecture**

Person in charge: Jérémie Crenne

Level : Second year ENSEIRB-MATMECA - equivalent M1

Volume : 1 x 16 Hours

Content: This course aims to strengthen knowledge by addressing more advanced techniques related to processors and memories. This course is based on the book by J.L. Hennessy and A. Patterson "Computer Architecture, a quantitative approach". RISC and CISC architectures, pipeline architectures, data and control hazards are discussed. The case of the MIPS processor is studied in detail to give students a concrete example of a processor architecture. The purpose of this course is to enable students to understand the most sophisticated multi/many-core systems.

Keywords: Computer architecture, pipeline architectures, multithreading

Personal Involvement : Supervised works

- **Microcomputer project**

Person in charge: Yannick Bornat

Level : Second year ENSEIRB-MATMECA - equivalent M1

Volume : 1 x 42 Hours

Content : All practical works are performed on the AT91SAM7X256 microcontroller. This microcontroller has an ARM7 core, many peripherals and a vectorized and configurable interrupt system. The objective of the course is to use the different hardware resources to design a minimalist operating system that meets the specific needs of microcontrollers for real-time tasks. The concepts cover real-time aspects, communication, data integrity. Students are placed in a situation where their only source of documentation is the manufacturer's technical documents in English.

Keywords: Microcontroller programming, C language, interrupt networks

Personal participation: Supervision of the practical works and the project

- **Object oriented programming. C++ language**

Person in charge: Bertrand Le Gal

Level : Second year ENSEIRB-MATMECA - equivalent M1

Volume : 1 x 15 Hours

Content : This course aims to provide students with the basics of object-oriented programming. The general concepts of object-oriented programming are being introduced. The C++ language is used to illustrate the concepts manipulated. All these concepts are used in a project to illustrate in a practical way the interest of this programming approach.

Keywords: Object oriented programming, C++

Personal participation : Supervision of practical works

Responsabilities

I have been an IEEE member since 2018 and I participate in the review of articles for various journals and conferences in the field of digital systems and signal processing.

- **Revue d'articles de journaux**
  - IEEE Communication Letters
- **Revue d'articles de conférence**
  - IEEE International Symposium on Information Theory: ISIT
  - IEEE Wireless Communications and Networking Conference: WCNC
  - IEEE International Conference on Communications: ICC
  - IEEE Workshop on Signal Processing Systems: SiPS
- **CCT TSI CNES**

In June 2015, I participated in the "Technologies for 5G - Space Segment" day organized by CNES in Toulouse, for a presentation called "Polar codes, algorithms and decoders", during which I was able to exchange with the various speakers.