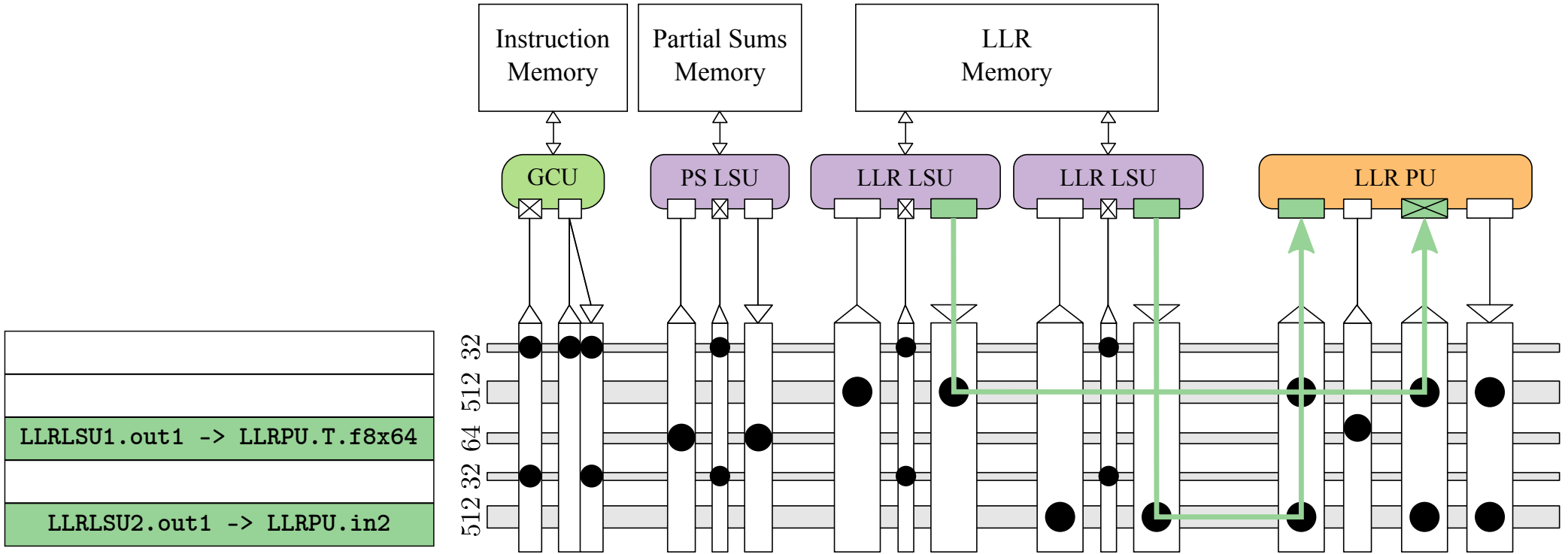
Instruction Memory
Partial Sums Memory
LLR Memory
GCU
PS LSU
LLR LSU
LLR LSU
LLR PU
32
512
64
32
512
LLRLSU1.out1 -> LLRPU.T.f8x64
LLRLSU2.out1 -> LLRPU.in2