The device can be powered off by writing to the POWEROFF bit of the Power Down register. In POWEROFF mode the Control Interface and a small portion of the digital remain active. The analogue VMID reference is disabled. As in STANDBY mode the crystal oscillator and/or CLKOUT pin can be independently controlled. Refer to Table 28.

POWER OFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD	DESCRIPTION
1	0	0	X	X	X	X	X	POWEROFF, but with Crystal Oscillator OS and CLKOUT available
1	1	0	X	X	X	X	X	POWEROFF, but with Crystal Oscillator OS available, CLKOUT not-available
1	1	1	X	X	X	X	X	POWEROFF, Crystal oscillator and CLKOUT not-available.

Table 28 Poweroff Mode

REGISTER MAP

The complete register map is shown in Table 29. The detailed description can be found in Table 30 and in the relevant text of the device description. There are 11 registers with 16 bits per register (7 bit address + 9 bits of data). These can be controlled using either the 2 wire or 3 wire MPU interface.

REGISTER	B 15	B 14	B 13	B 12	B 11	B 10	B 9	B8	B7	B6	B5	B4	B3	B2	B1	B0
R0 (00h)	0	0	0	0	0	0	0	LRIN BOTH	LIN MUTE	0	0	LINVOL				
R1 (02h)	0	0	0	0	0	0	1	RLIN BOTH	RIN MUTE	0	0	RINVOL				
R2 (04h)	0	0	0	0	0	1	0	LRHP BOTH	LZCEN	LHPVOL						
R3 (06h)	0	0	0	0	0	1	1	RLHP BOTH	RZCEN	RHPVOL						
R4 (08h)	0	0	0	0	1	0	0	0	SIDEATT		SIDETONE	DAC SEL	BY PASS	INSEL	MUTE MIC	MIC BOOST
R5 (0Ah)	0	0	0	0	1	0	1	0	0	0	0	HPOR	DAC MU	DEEMPH		ADC HPD
R6 (0Ch)	0	0	0	0	1	1	0	0	PWR OFF	CLK OUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD
R7 (0Eh)	0	0	0	0	1	1	1	0	BCLK INV	MS	LR SWAP	LRP	IWL		FORMAT	
R8 (10h)	0	0	0	1	0	0	0	0	CLKO DIV2	CLKI DIV2	SR				BOSR	USB/ NORM
R9 (12h)	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0	ACTIVE
R15(1Eh)	0	0	0	1	1	1	1	RESET								
	ADDRESS							DATA								

Table 29 Mapping of Program Registers