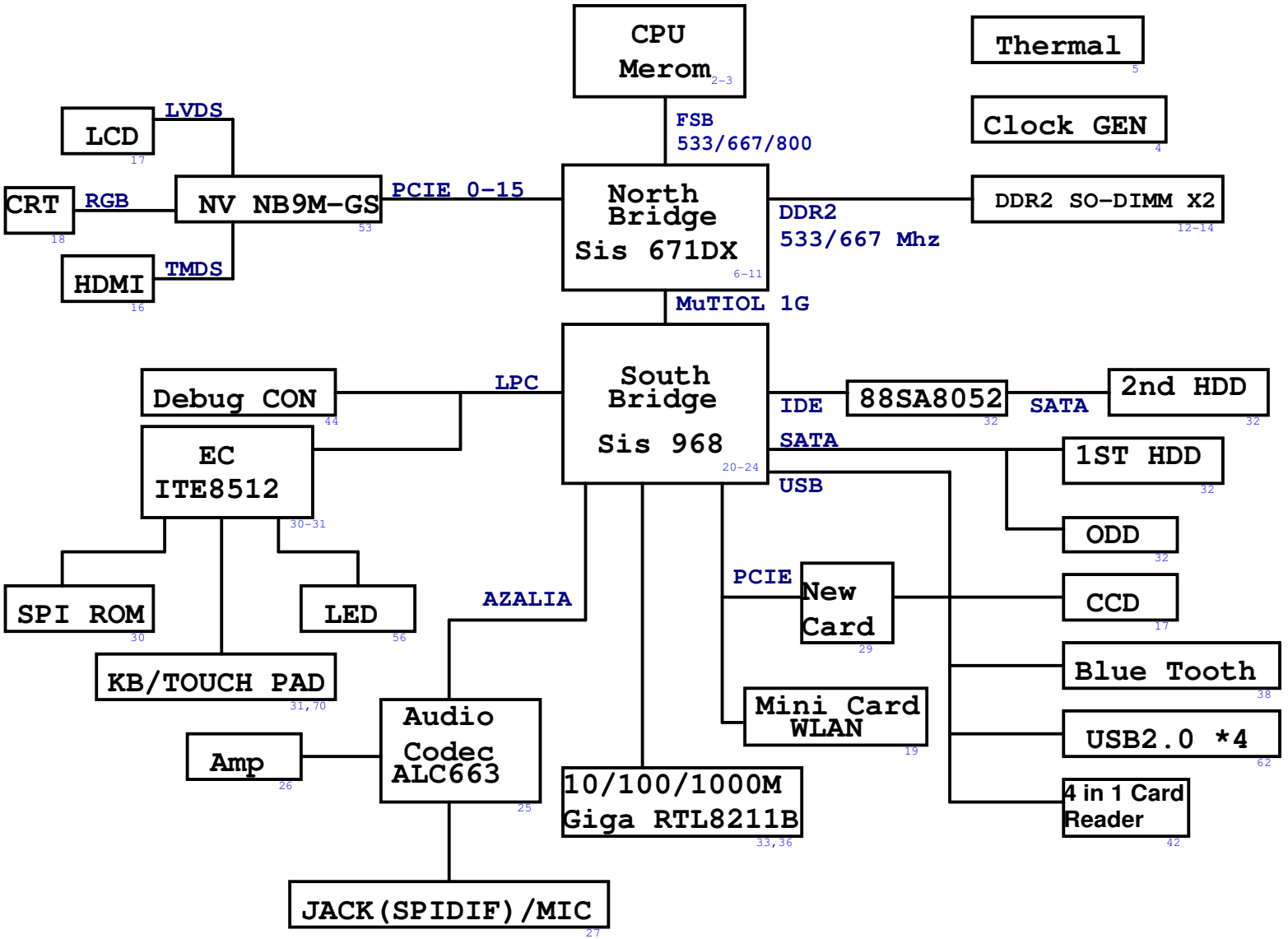
F70SL Main BD. R1.0 BLOCK DIAGRAM



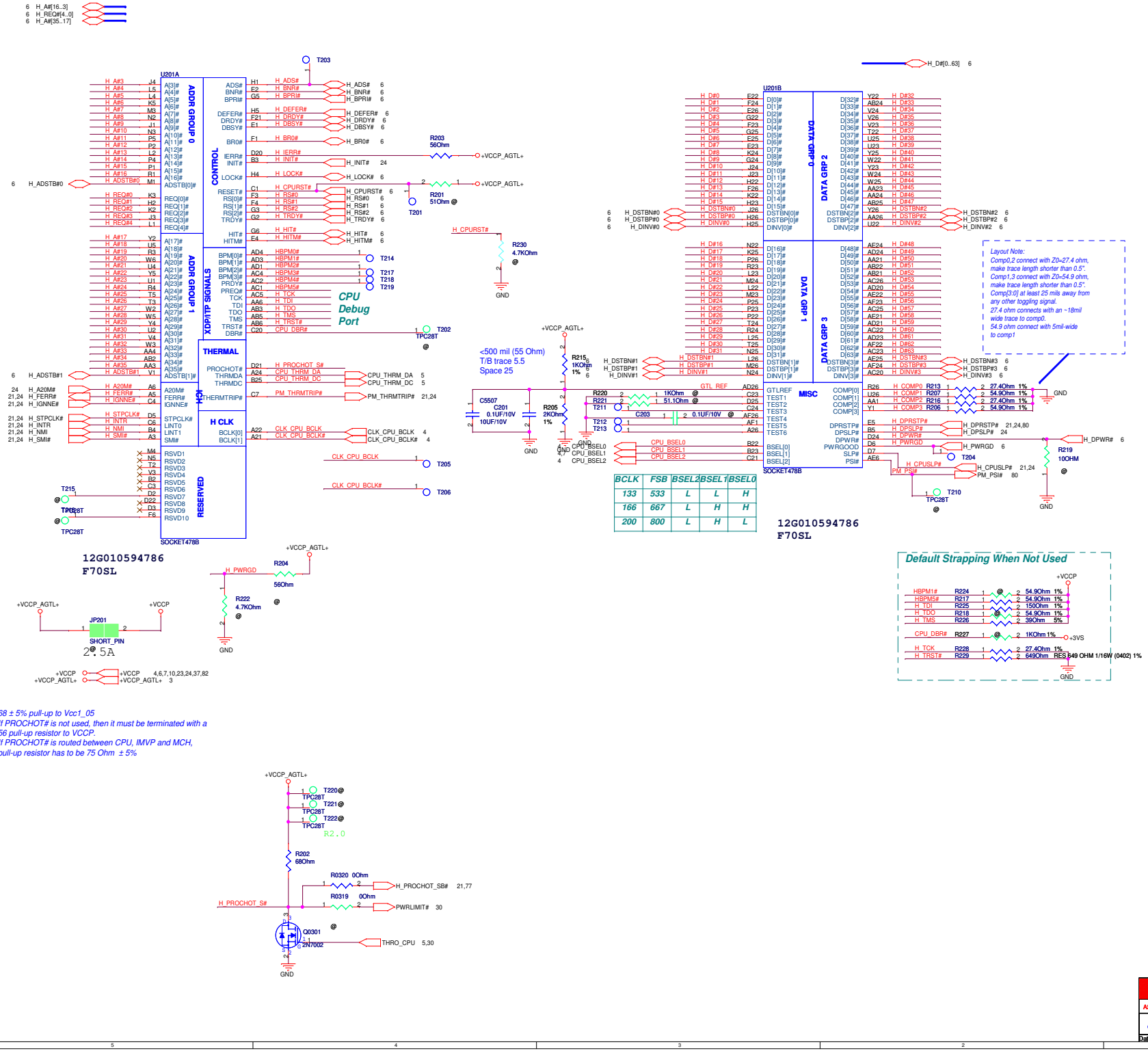
ASUSTeK Computer INC

Title : Block Diagram

Engineer: Miller / Daniel

Size	Project Name	Rev
B	F70SL	1.0

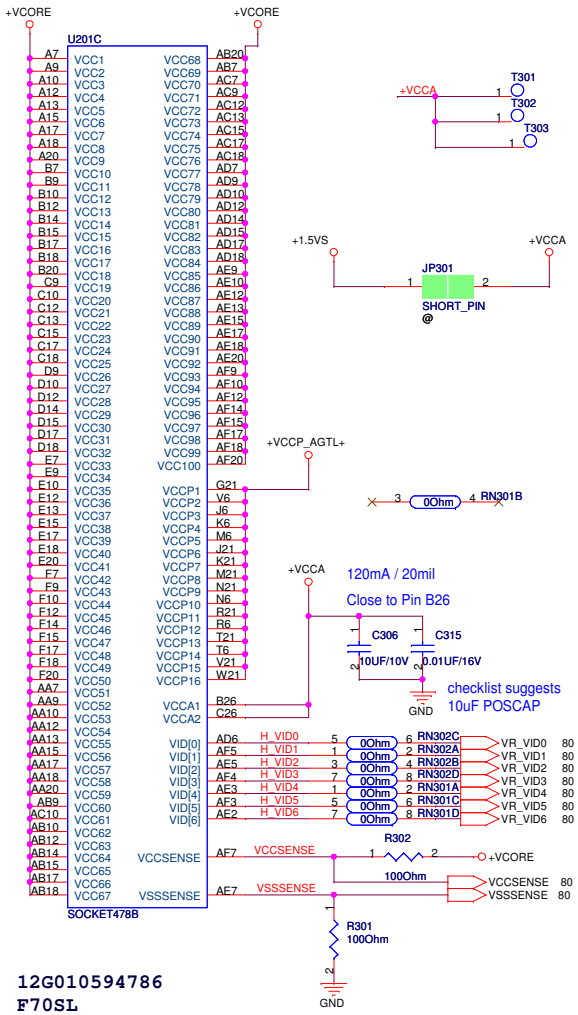
Date: Monday, November 03, 2008 Sheet 1 of 94



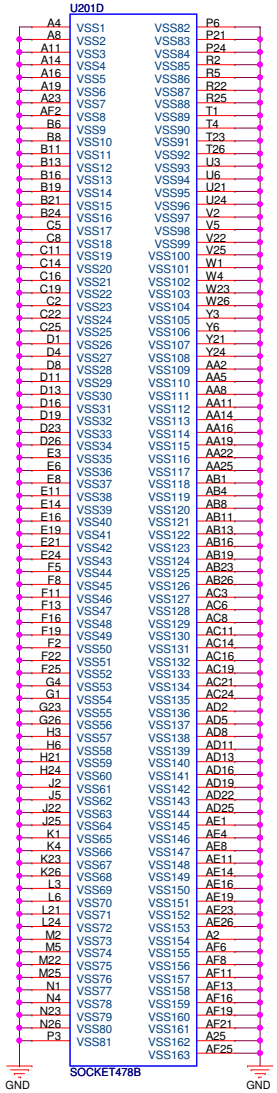
Title :	Merom CPU (1)
ASUSTeK COMPUTER INC	Engineer: Miller / Daniel
Size: C	Project Name: F70SL
Rev: 1.0	
Date: Monday, November 03, 2008	Sheet 2 of 94

YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A



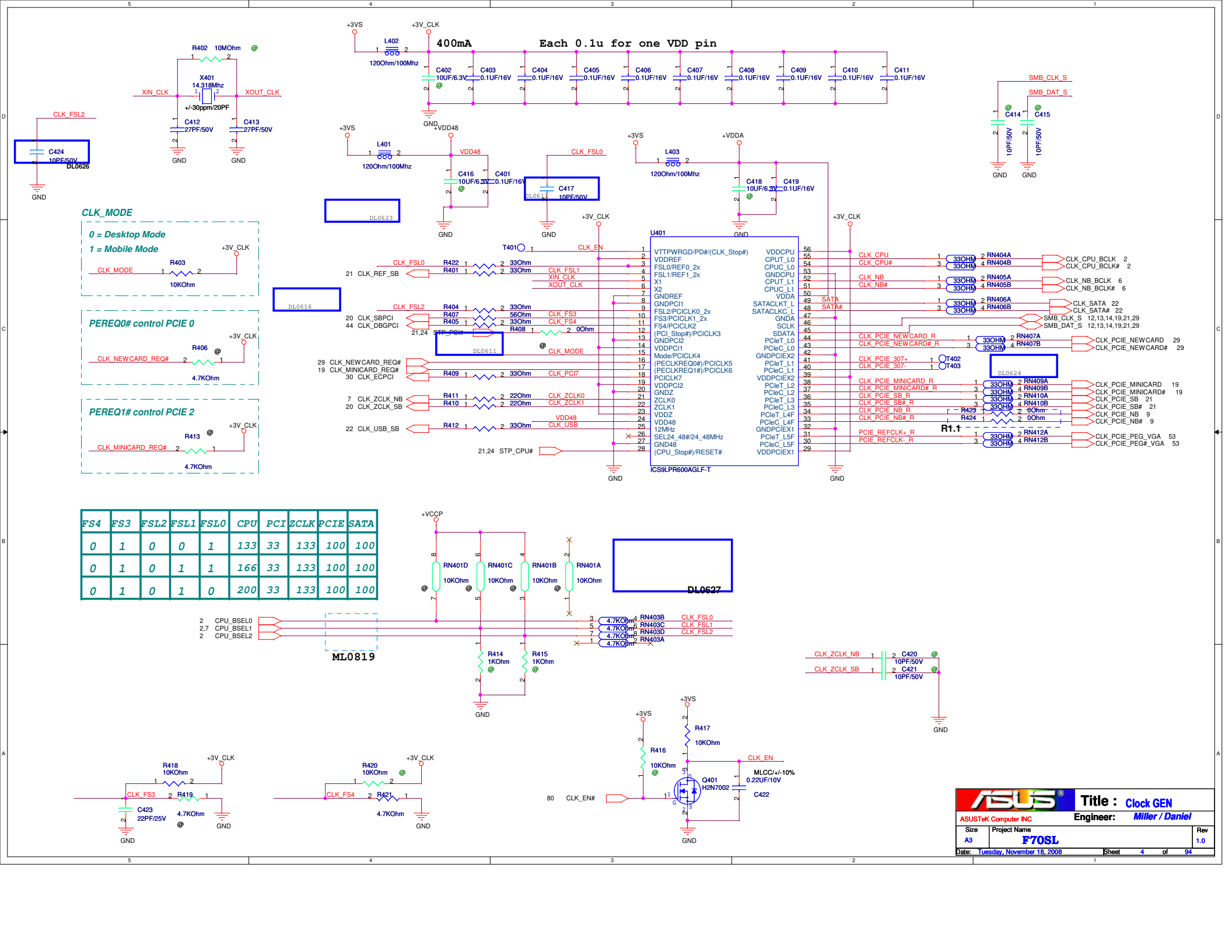
12G010594786
F70SL



12G010594786
F70SL

Layout Note:
VCCSENSE/VSSSENSE lines between the CPU and the VR should have a trace width of 18 mils on 7 mils spacing, with trace impedance of Zo=27.4 Ohm.
The VCCSENSE/VSSSENSE should be length matched to within 25 mils.
These resistors should be placed within 2 inch of the CPU.

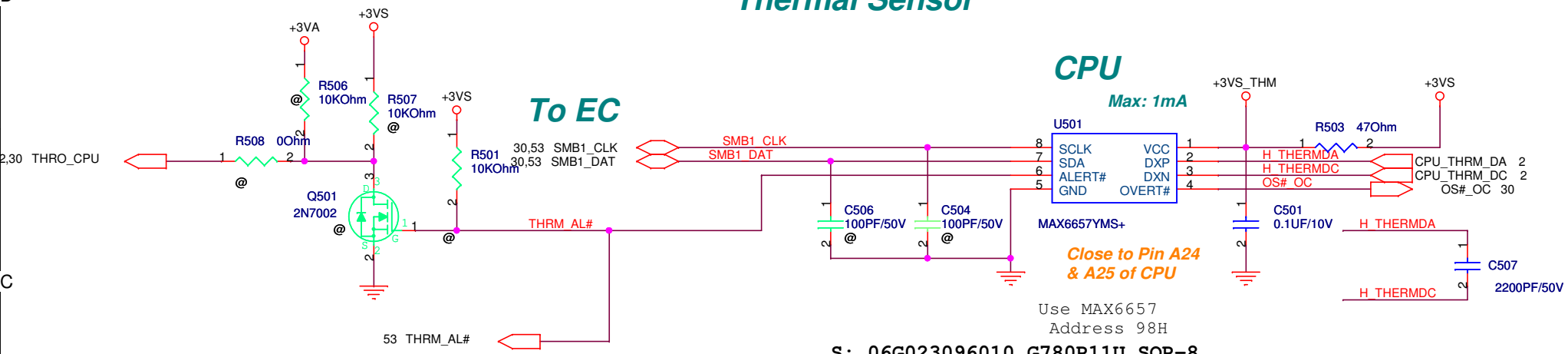
ASUSTeK COMPUTER INC	Title :	Merom CPU (2)
	Engineer:	Miller / Daniel
Size: A3	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 3 of 94	



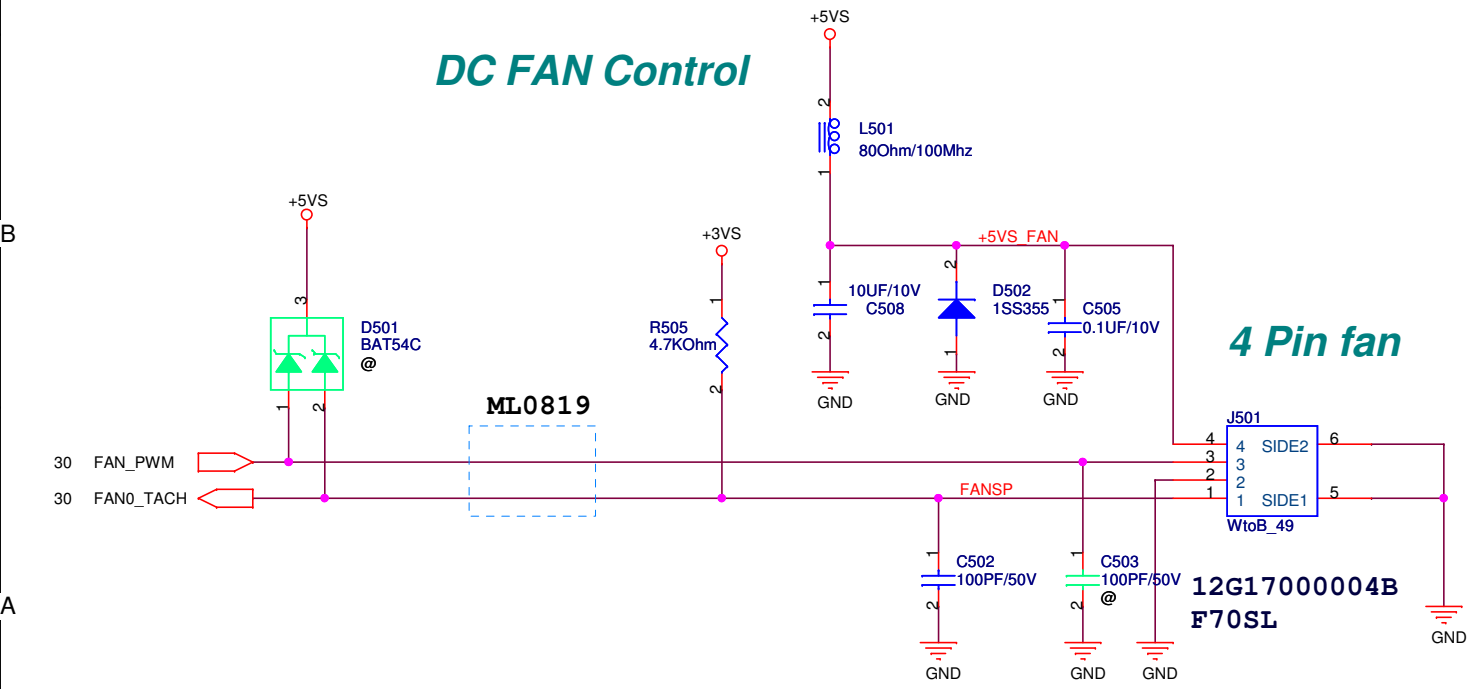
FS4	FS3	FSL2	FSL1	FSL0	CPU	PCI	ZCLK	PCIE	SATA
0	1	0	0	1	133	33	133	100	100
0	1	0	1	1	166	33	133	100	100
0	1	0	1	0	200	33	133	100	100

ASUSTeK Computer INC	Title : Clock GEN	
	Engineer: Miller / Daniel	
Size: A3	Project Name: F70SL	Rev: 1.0
Date: Tuesday, November 18, 2008	Sheet 4 of 94	

Thermal Sensor



DC FAN Control

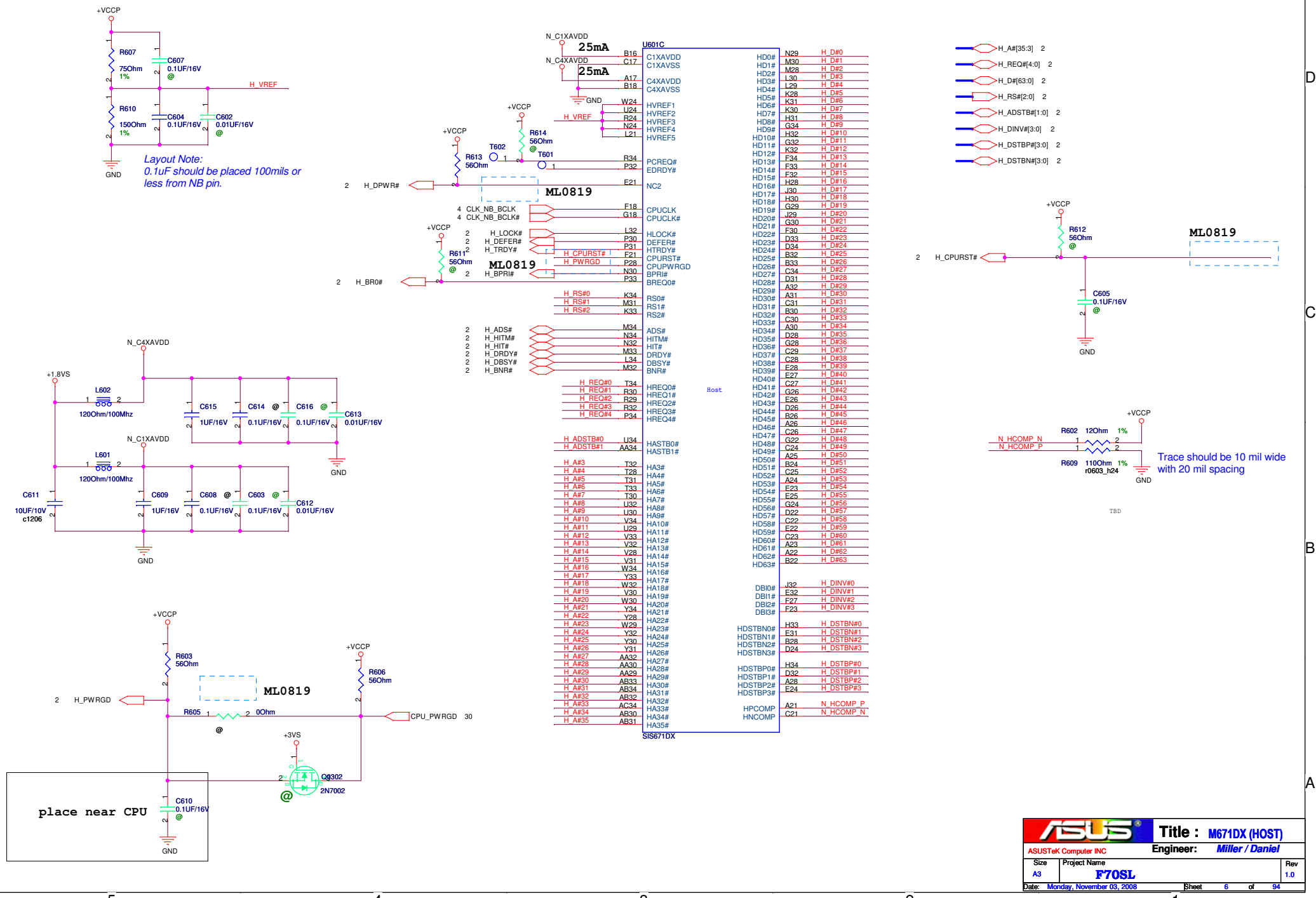


Route H_THERMDA and H_THERMDC on the same layer

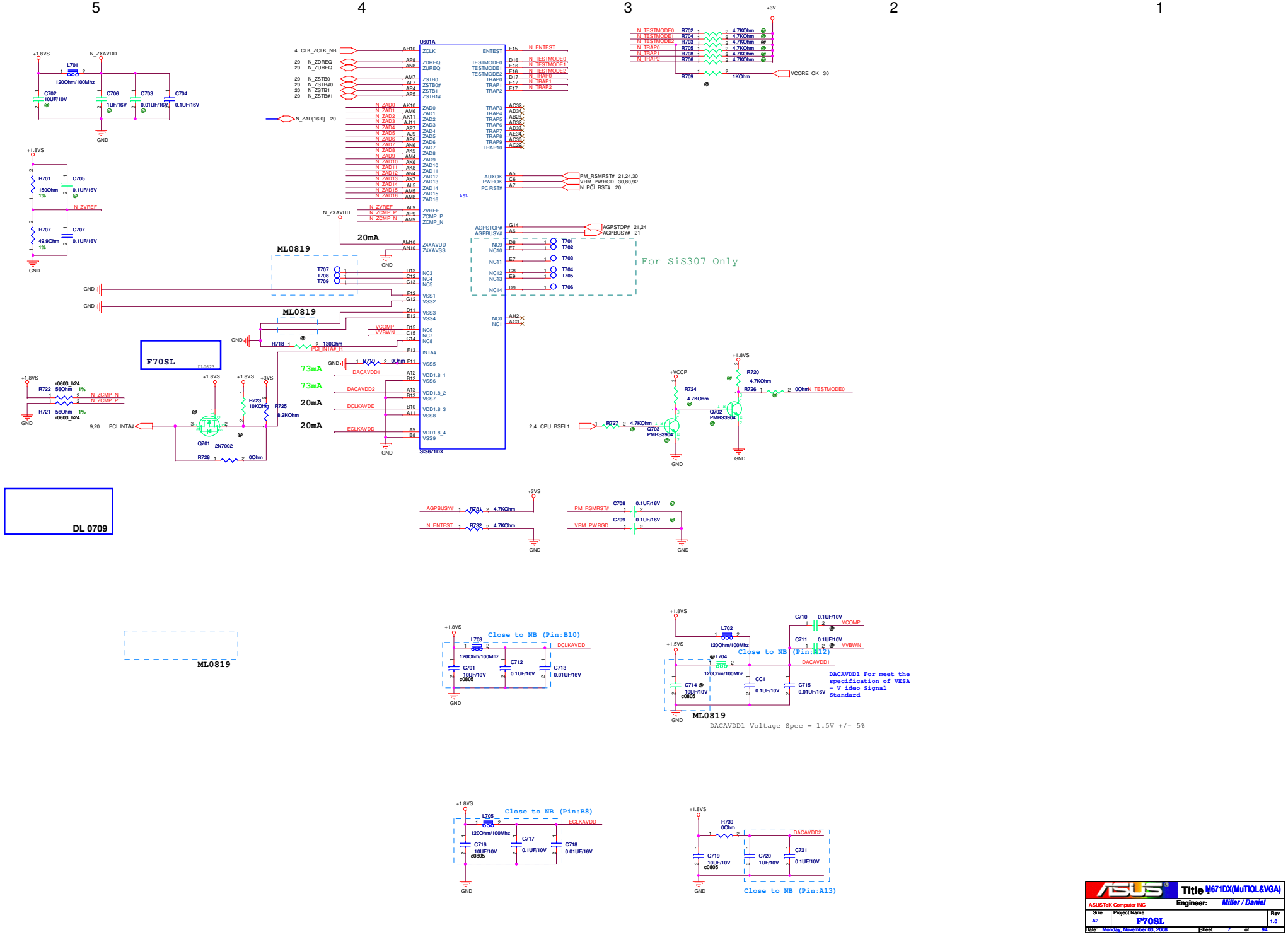
----------OTHER SIGNALS
20 mils
==========GND
10 mils
==========H_THERMDA(10 mils)
10 mils
==========H_THERMDC(10 mils)
10 mils
==========GND
20 mils
----------OTHER SIGNALS

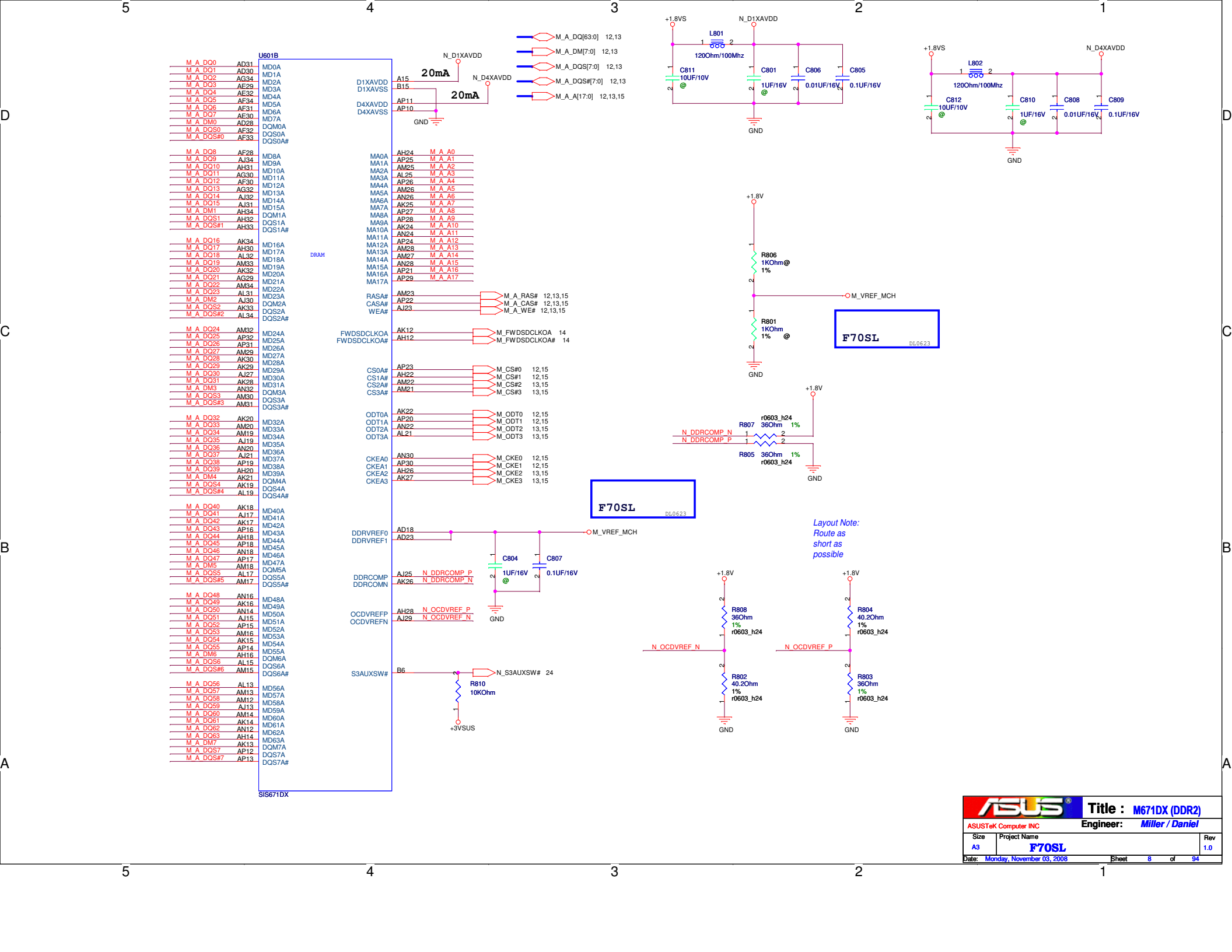
Avoid FSB,Power

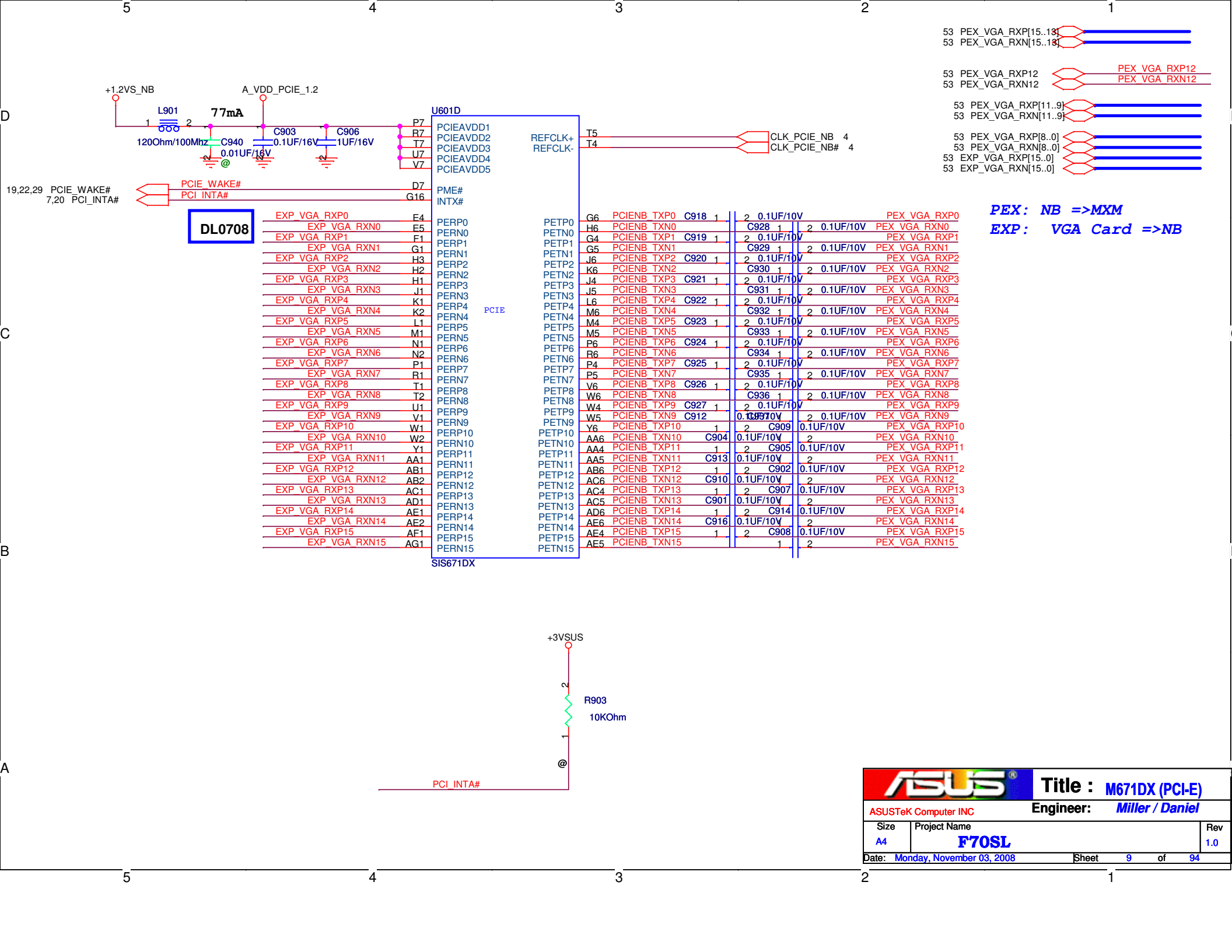
ASUSTeK Computer INC	Title : Thermal Sensor	
	Engineer: Miller / Daniel	
Size: A4	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 5 of 94	



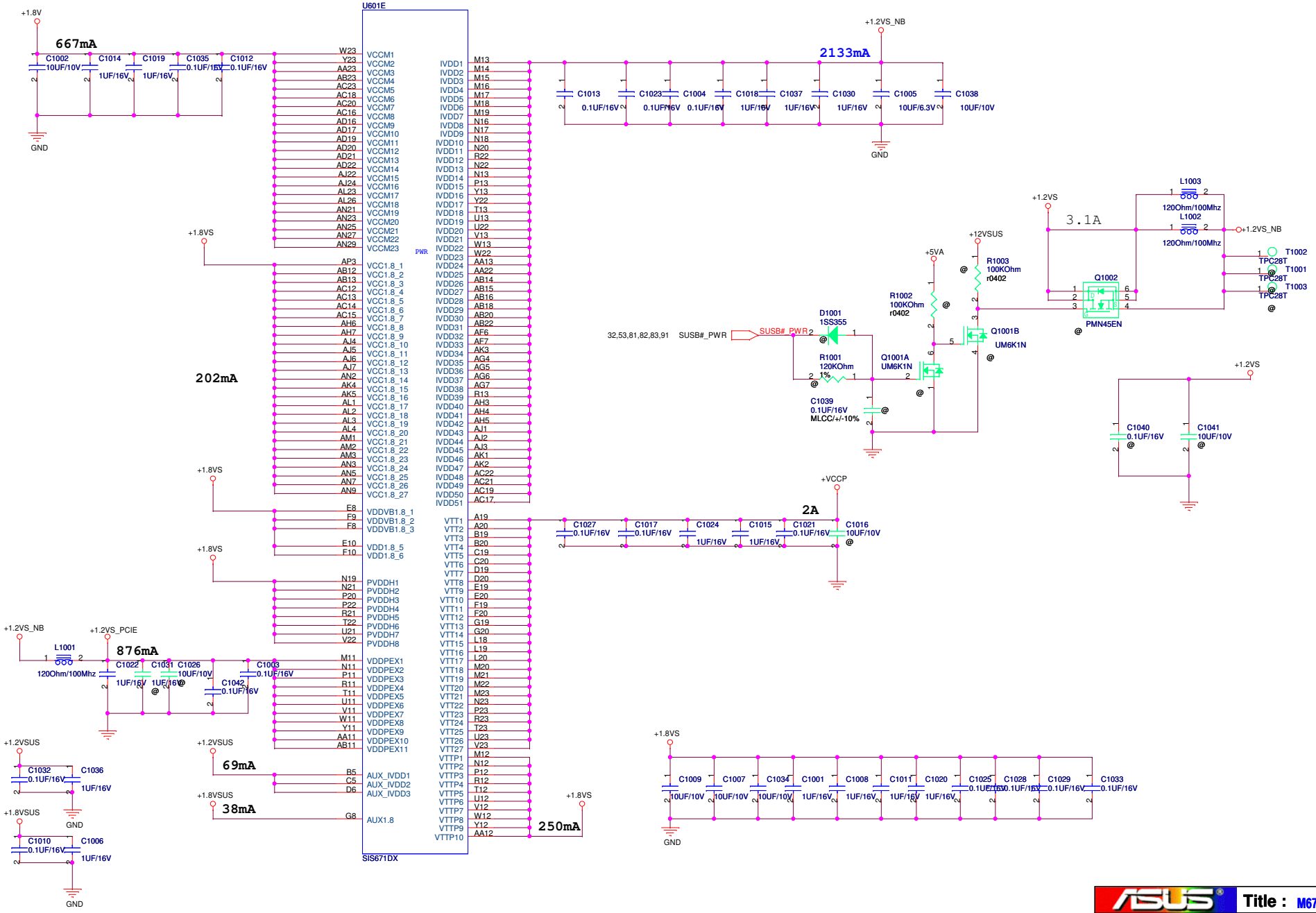
ASUSTeK Computer INC	Title : M671DX (HOST)	
	Engineer: Miller / Daniel	
Size: A3	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 6 of 94	


U601A
SIS671DX
F70SL
ML0819
DL 0709
For SiS307 Only
73mA
73mA
20mA
20mA
20mA
Close to NB (Pin:B10)
Close to NB (Pin:M12)
Close to NB (Pin:B8)
Close to NB (Pin:A13)
DACAVDD1 For meet the specification of VESA - V ideo Signal Standard
DACAVDD1 Voltage Spec = 1.5V +/- 5%
Title : M671DX(MuTIOL&VGA)
ASUSTeK Computer INC
Engineer: Miller / Daniel
Size A2
Project Name F70SL
Rev 1.0
Date: Monday, November 03, 2008
Sheet 7 of 94

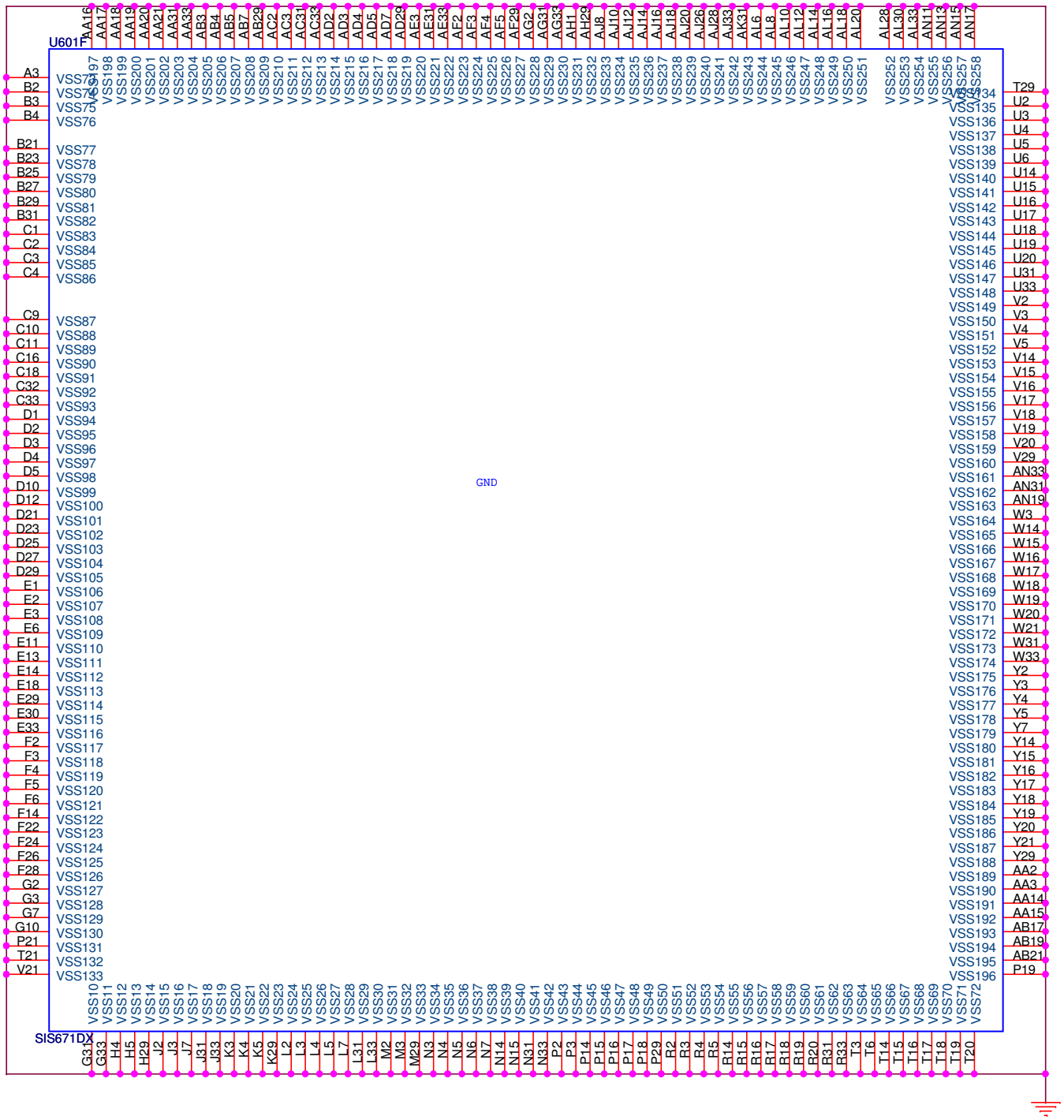

U601B
SIS671DX
DRAM
M_A_DQ[63:0] 12,13
M_A_DM[7:0] 12,13
M_A_DQS[7:0] 12,13
M_A_DQS#[7:0] 12,13
M_A_A[17:0] 12,13,15
N_D1XAVDD
N_D4XAVDD
20mA
20mA
GND
+1.8VS
L801
120Ohm/100Mhz
C811 10UF/10V @
C801 1UF/16V @
C806 0.01UF/16V
C805 0.1UF/16V
L802
120Ohm/100Mhz
C812 10UF/10V @
C810 1UF/16V @
C808 0.01UF/16V
C809 0.1UF/16V
+1.8V
R806 1KOhm@ 1%
R801 1KOhm 1% @
M_VREF_MCH
F70SL
DL0623
N_DDRCOMP_N
N_DDRCOMP_P
R807 36Ohm 1% r0603_h24
R805 36Ohm 1% r0603_h24
Layout Note: Route as short as possible
C804 1UF/16V @
C807 0.1UF/16V
R808 36Ohm 1% r0603_h24
R802 40.2Ohm 1% r0603_h24
R804 40.2Ohm 1% r0603_h24
R803 36Ohm 1% r0603_h24
N_OCDVREF_N
N_OCDVREF_P
R810 10KOhm
+3VSUS
M_A_RAS# 12,13,15
M_A_CAS# 12,13,15
M_A_WE# 12,13,15
M_FWDSDCLKOA 14
M_FWDSDCLKOA# 14
M_CS#0 12,15
M_CS#1 12,15
M_CS#2 13,15
M_CS#3 13,15
M_ODT0 12,15
M_ODT1 12,15
M_ODT2 13,15
M_ODT3 13,15
M_CKE0 12,15
M_CKE1 12,15
M_CKE2 13,15
M_CKE3 13,15
N_S3AUXSW# 24
Title : M671DX (DDR2)
ASUSTeK Computer INC
Engineer: Miller / Daniel
Size A3
Project Name F70SL
Rev 1.0
Date: Monday, November 03, 2008
Sheet 8 of 94



Title : M671DX (PCI-E)		
ASUSTeK Computer INC	Engineer: Miller / Daniel	
Size: A4	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 9 of 94	

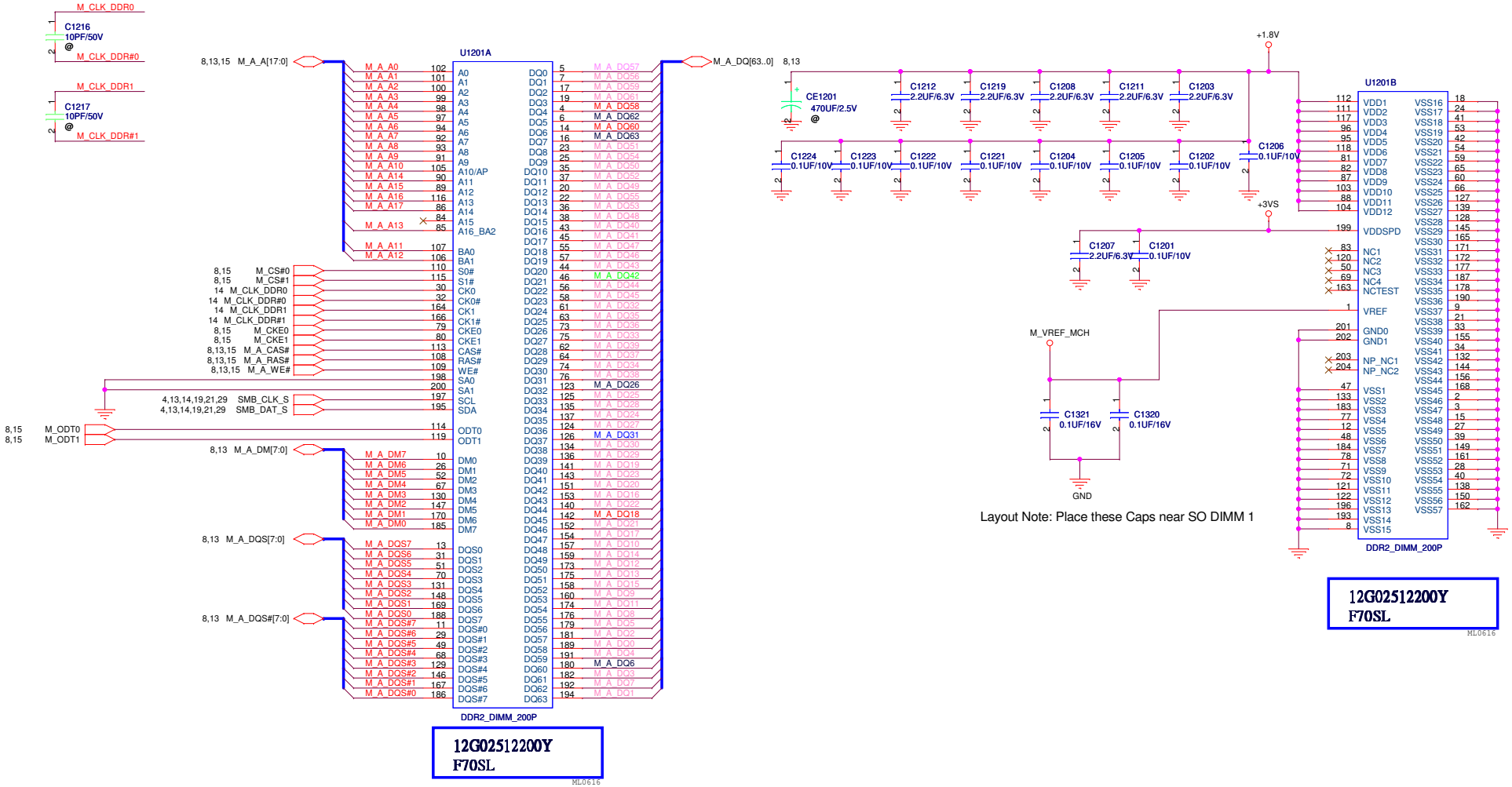


Title :	M671DX (PWR)
ASUSTeK Computer INC	Engineer: Miller / Daniel
Size: A3	Project Name: F70SL
Rev: 1.0	
Date: Monday, November 03, 2008	Sheet 10 of 94



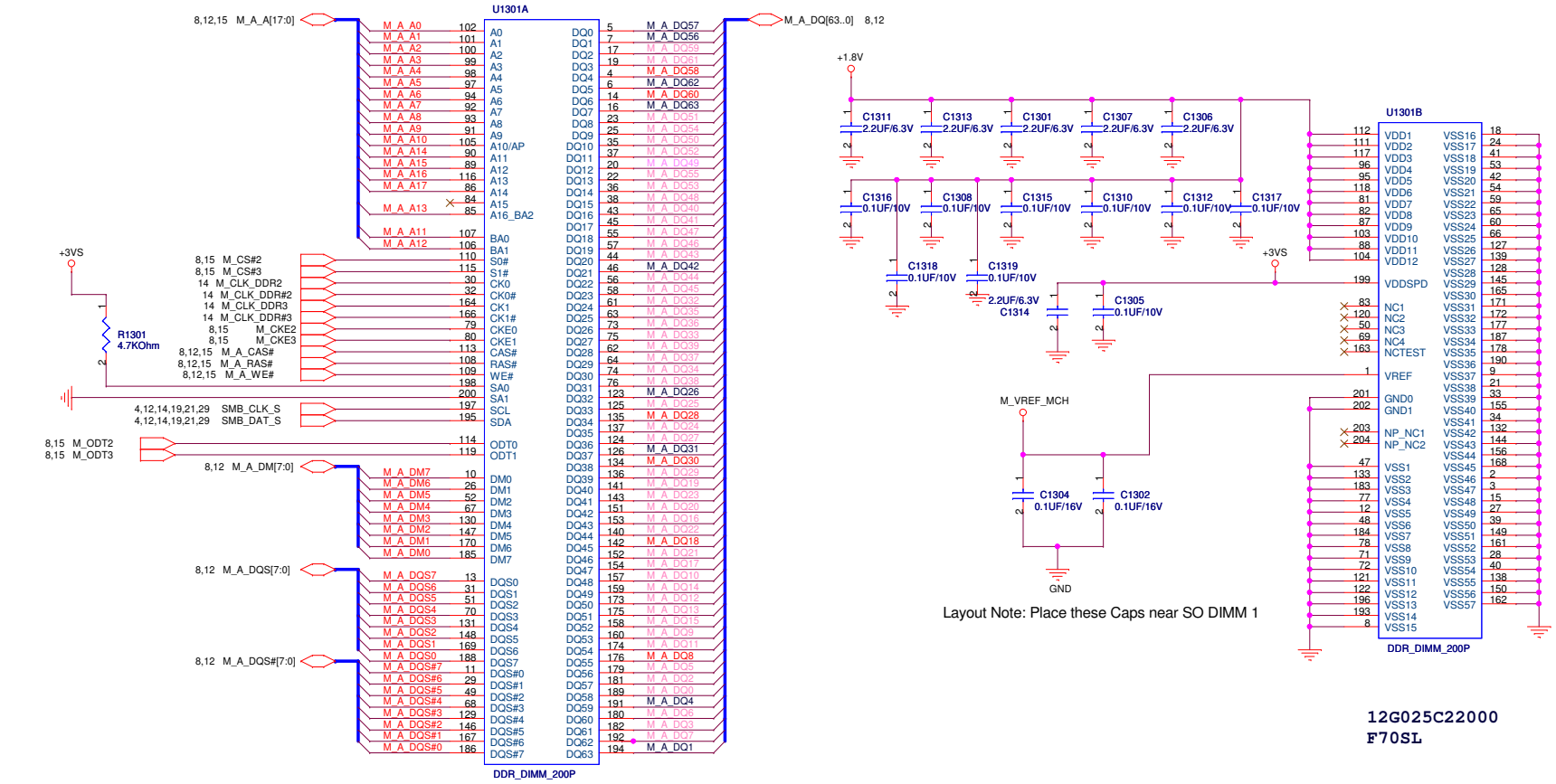
ASUSTeK Computer INC	Title : M671DX (GND)	
	Engineer: Miller / Daniel	
Size: A4	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 11 of 94	

TOP



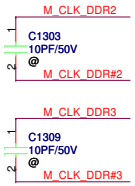
Layout Note: Place these Caps near SO DIMM 1

ASUSTeK Computer INC	Title : DDR2 SO-DIMM1	
	Engineer: Miller / Daniel	
Size: A3	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 12 of 94	



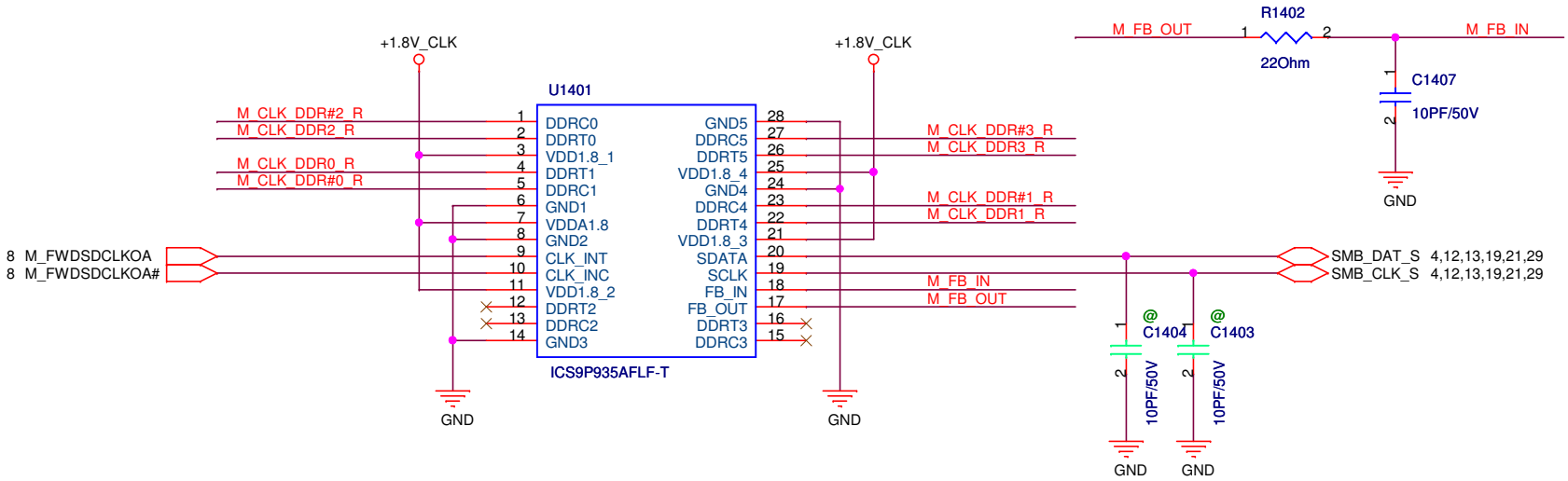
Layout Note: Place these Caps near SO DIMM 1

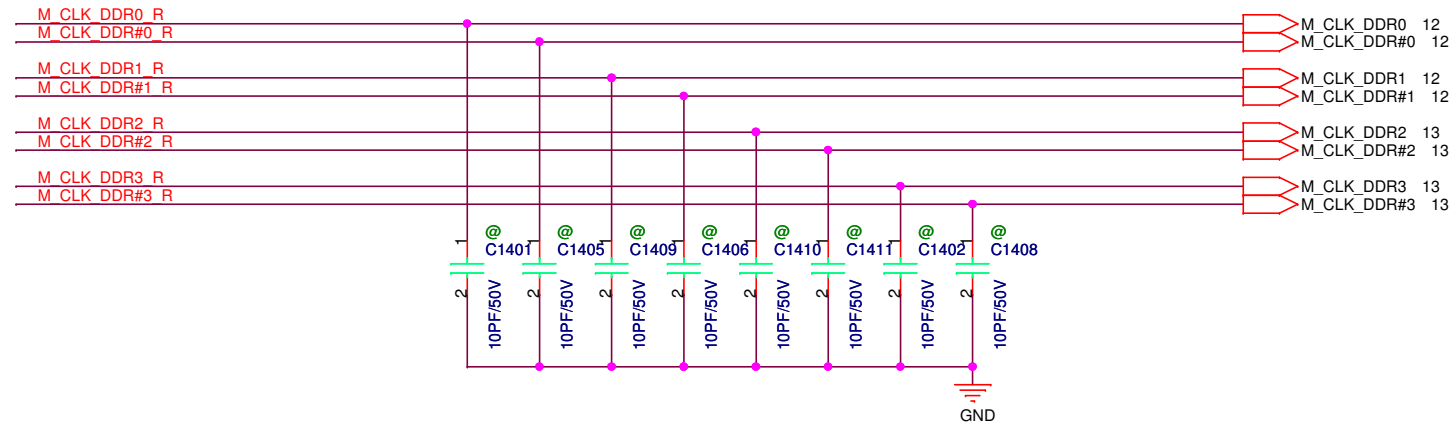
12G025C22000
F70SL

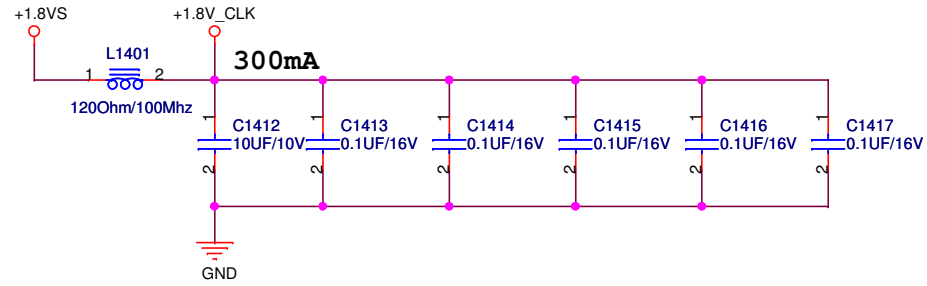


12G025C22000
F70SL

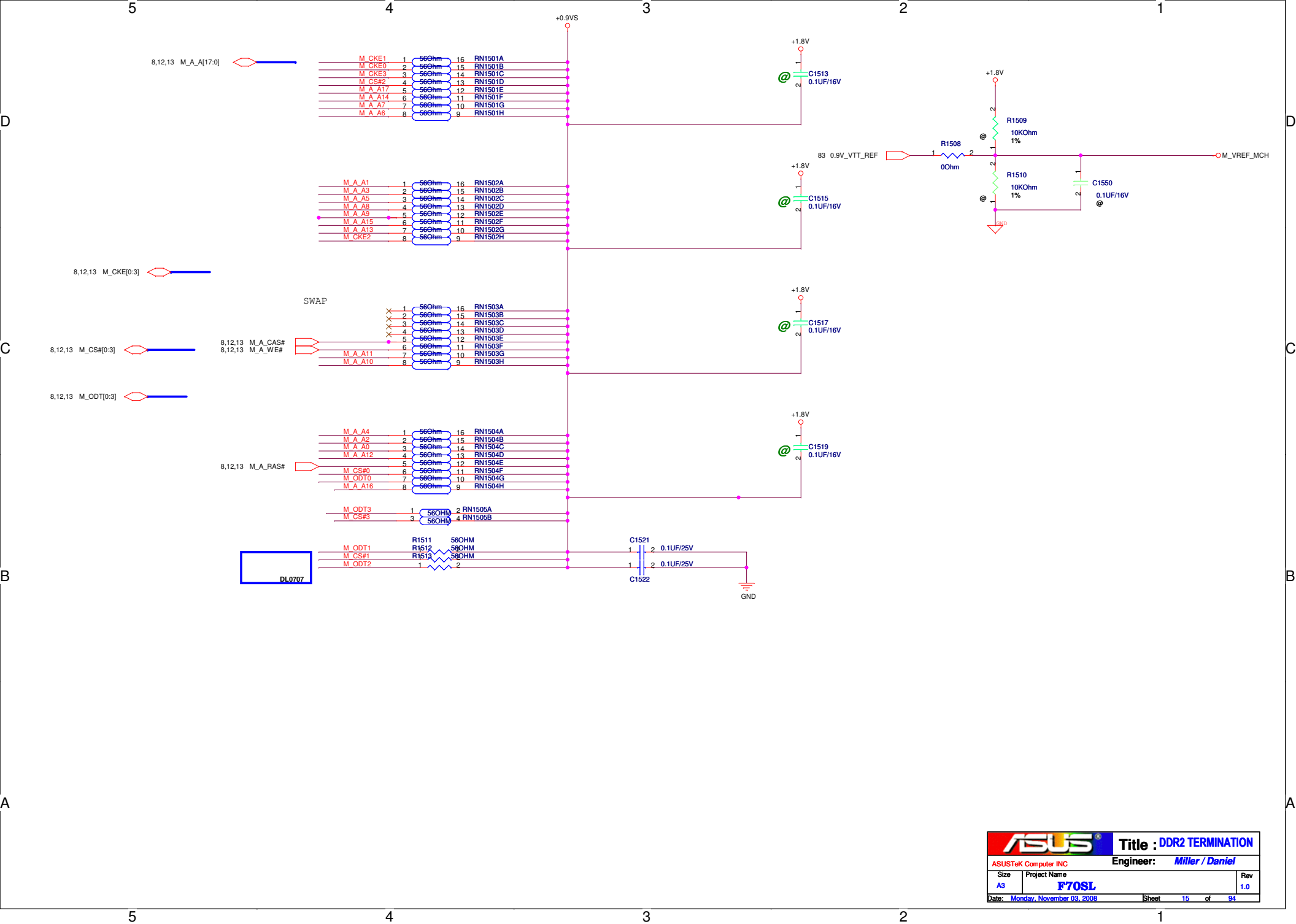
ASUSTeK Computer INC	Title : DDR2 SO-DIMM2	
	Engineer: Miller / Daniel	
Size: A3	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 13 of 94	



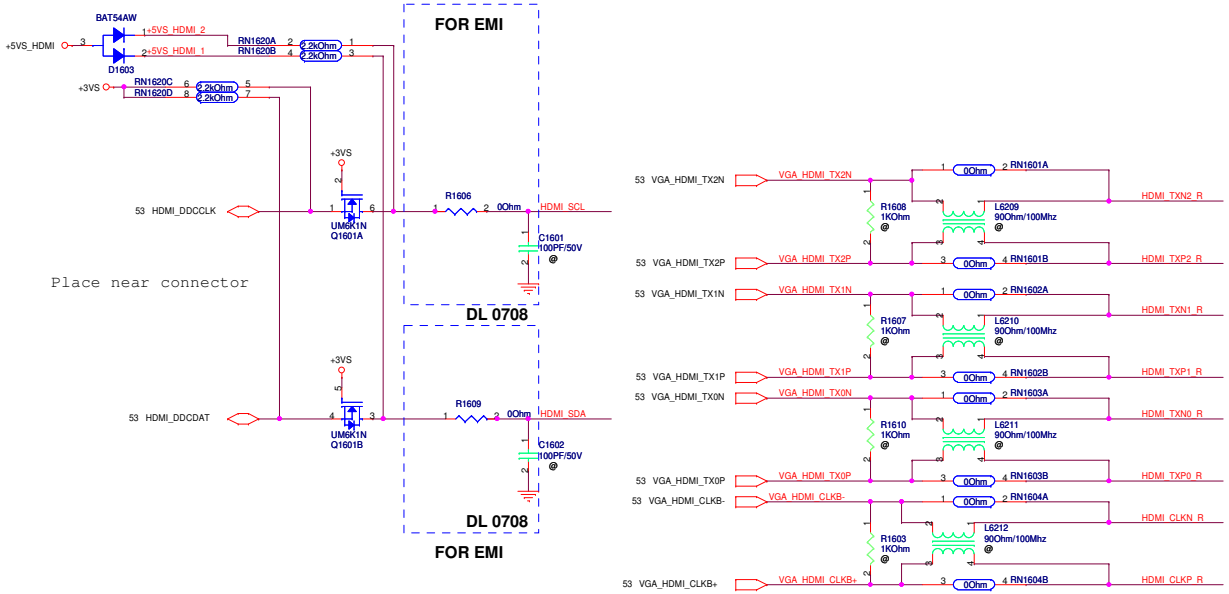




ASUSTeK Computer INC	Title : DDR2 BUFFER	
	Engineer: Miller / Daniel	
Size: A4	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 14 of 94	



ASUSTeK Computer INC	Title : DDR2 TERMINATION	
	Engineer: Miller / Daniel	
Size: A3	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 15 of 94	

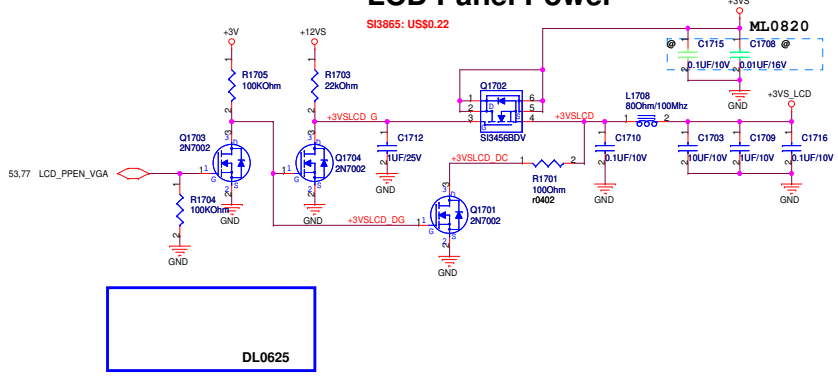


ASUSTeK Computer INC	Title : HDMI		
	Engineer: Miller / Daniel		
Size: C	Project Name: F70SL		Rev: 1.0
Date: Monday, November 03, 2008	Sheet 16 of 94		

LCD Panel Power

3~3.6V
S0-S1 M: 410
mA(Max. 500 mA)

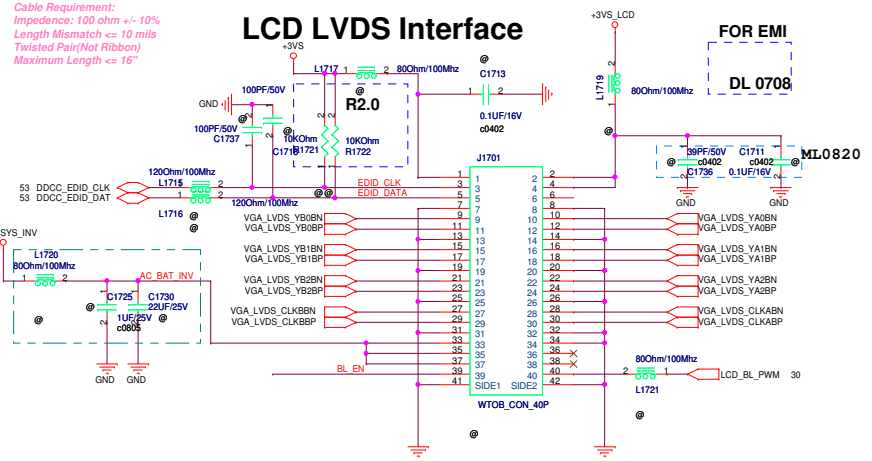
SI3865: US$0.22



DL0625

Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

LCD LVDS Interface

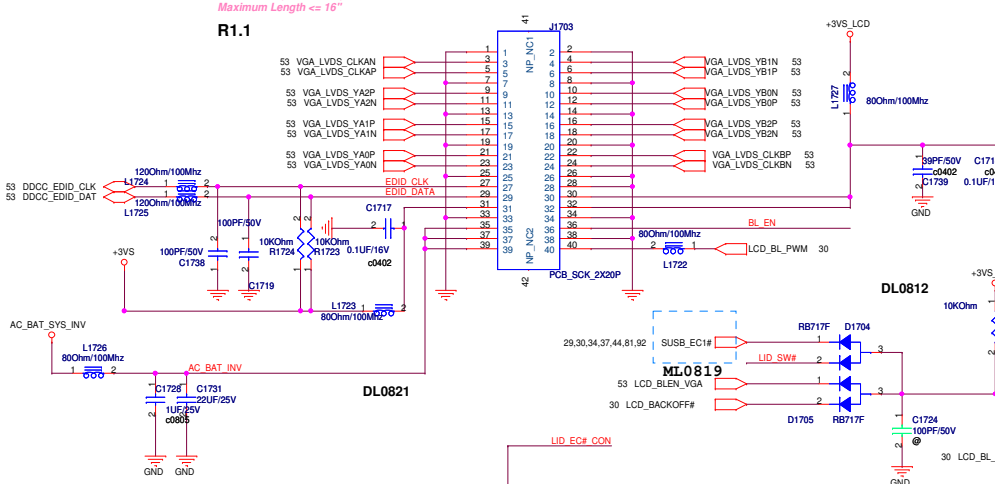


R1.1 12G170010408 F70SL DL0810

B to B Interface

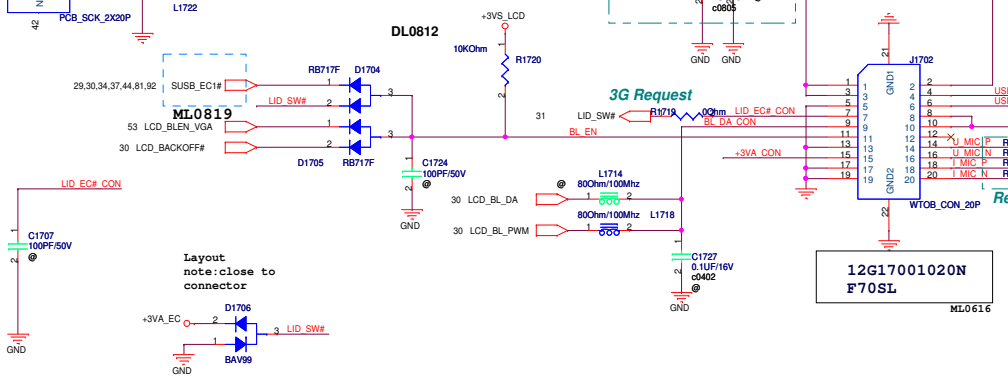
Cable Requirement:
Impedence: 100 ohm +/- 10%
Length Mismatch <= 10 mils
Twisted Pair(Not Ribbon)
Maximum Length <= 16"

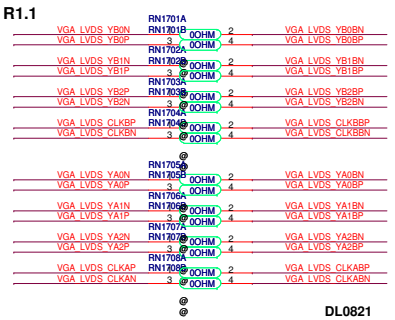
R1.1



DL0821

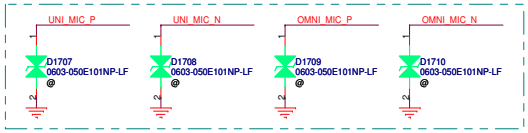
DL0812

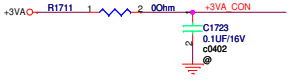




DL0821

Reserved for EMI

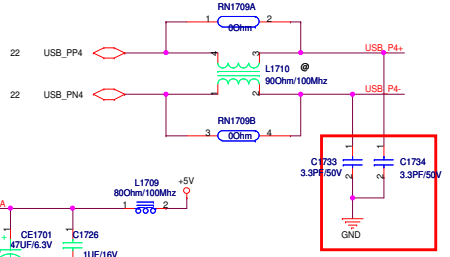


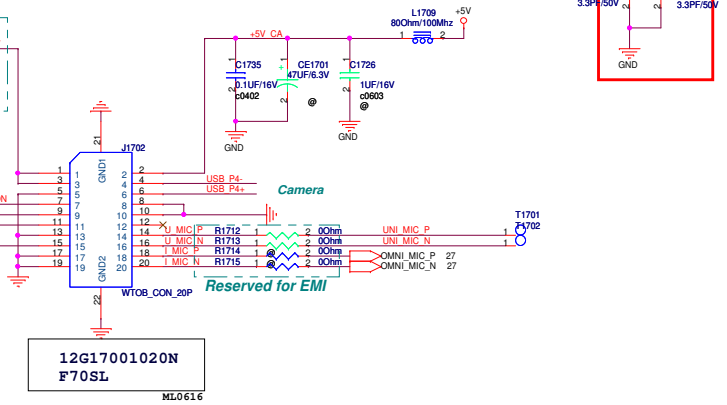


pls add the command choke

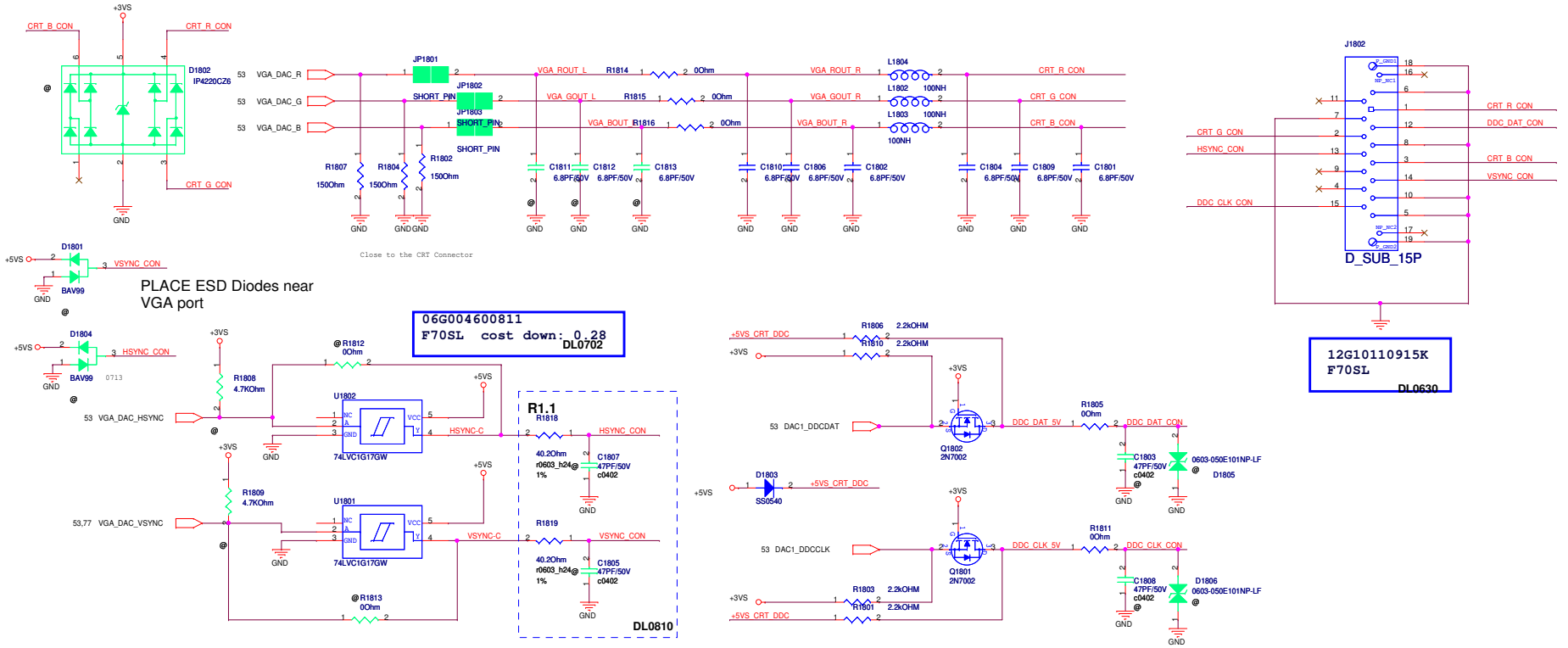
LCD Backlight Control

INVERTER
Interface/Speaker
CONN.

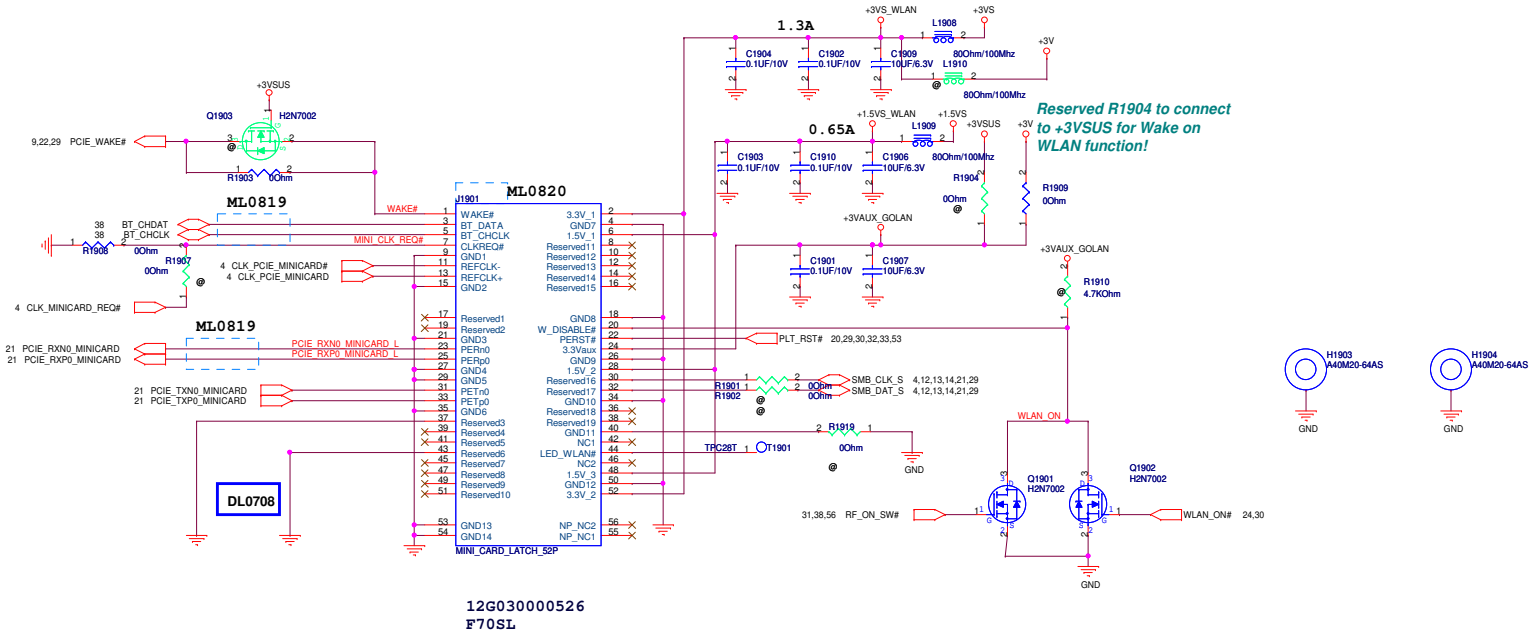




12G17001020N F70SL ML0616



ASUSTeK Computer INC	Title : CRT		
	Engineer: Miller / Daniel		
Size: C	Project Name: F70SL		Rev: 1.0
Date: Monday, November 03, 2008	Sheet 18 of 94		



12G030000526
F70SL

DL0619

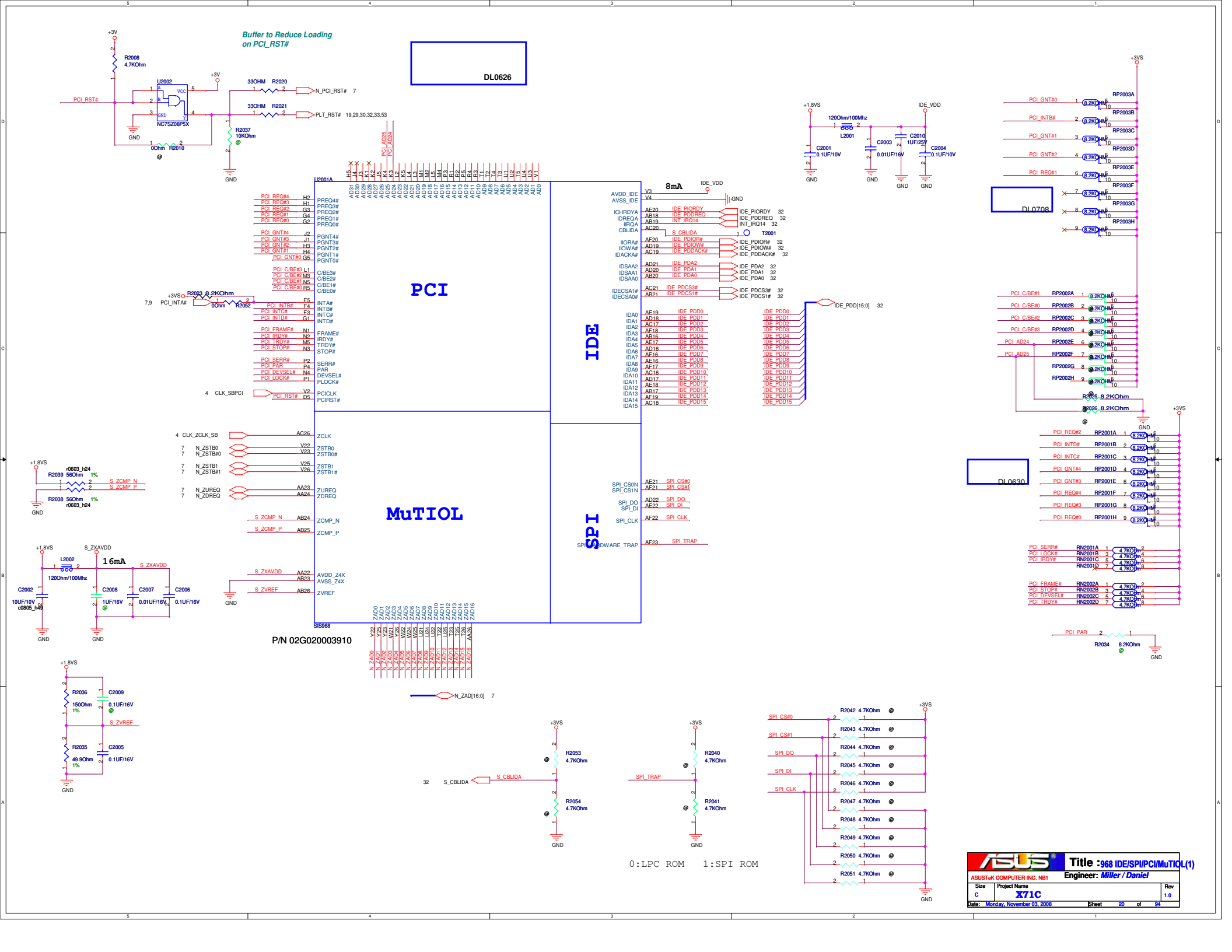
ASUSTeK Computer INC

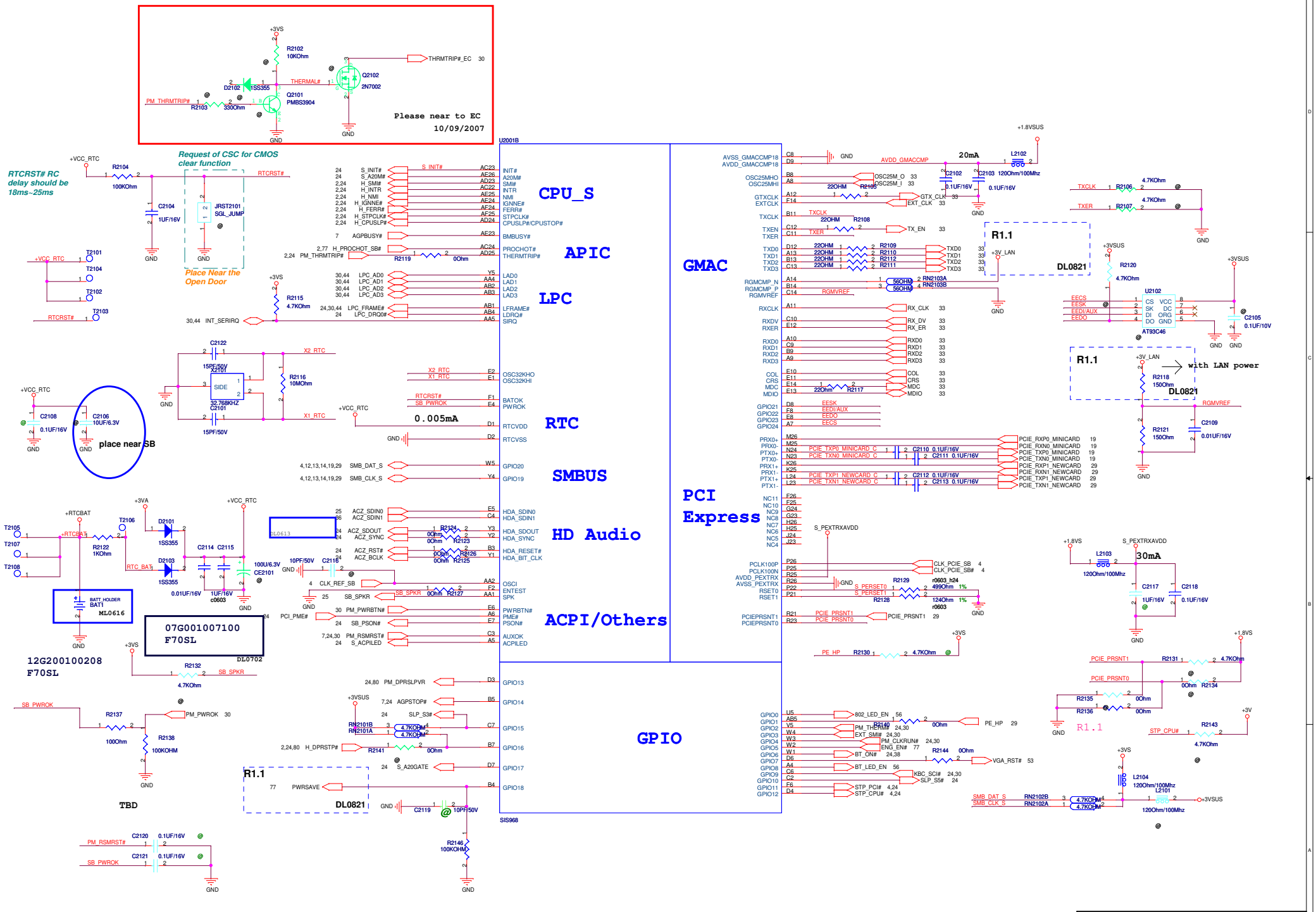
Title : Mini card WLAN/TV Tuner

Engineer: Miller / Daniel

Size	Project Name	Rev
C	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 19 of 94


Buffer to Reduce Loading on PCI_RST#
DL0626
PCI
IDE
MuTIOL
SPI
SIS968
P/N 02G020003910
8mA
16mA
DL0708
DL0630
0:LPC ROM 1:SPI ROM
Title :968 IDE/SPI/PCI/MuTIOL(1)
ASUSTeK COMPUTER INC. NB1
Engineer: Miller / Daniel
Size C
Project Name X71C
Rev 1.0
Date: Monday, November 03, 2008
Sheet 20 of 94



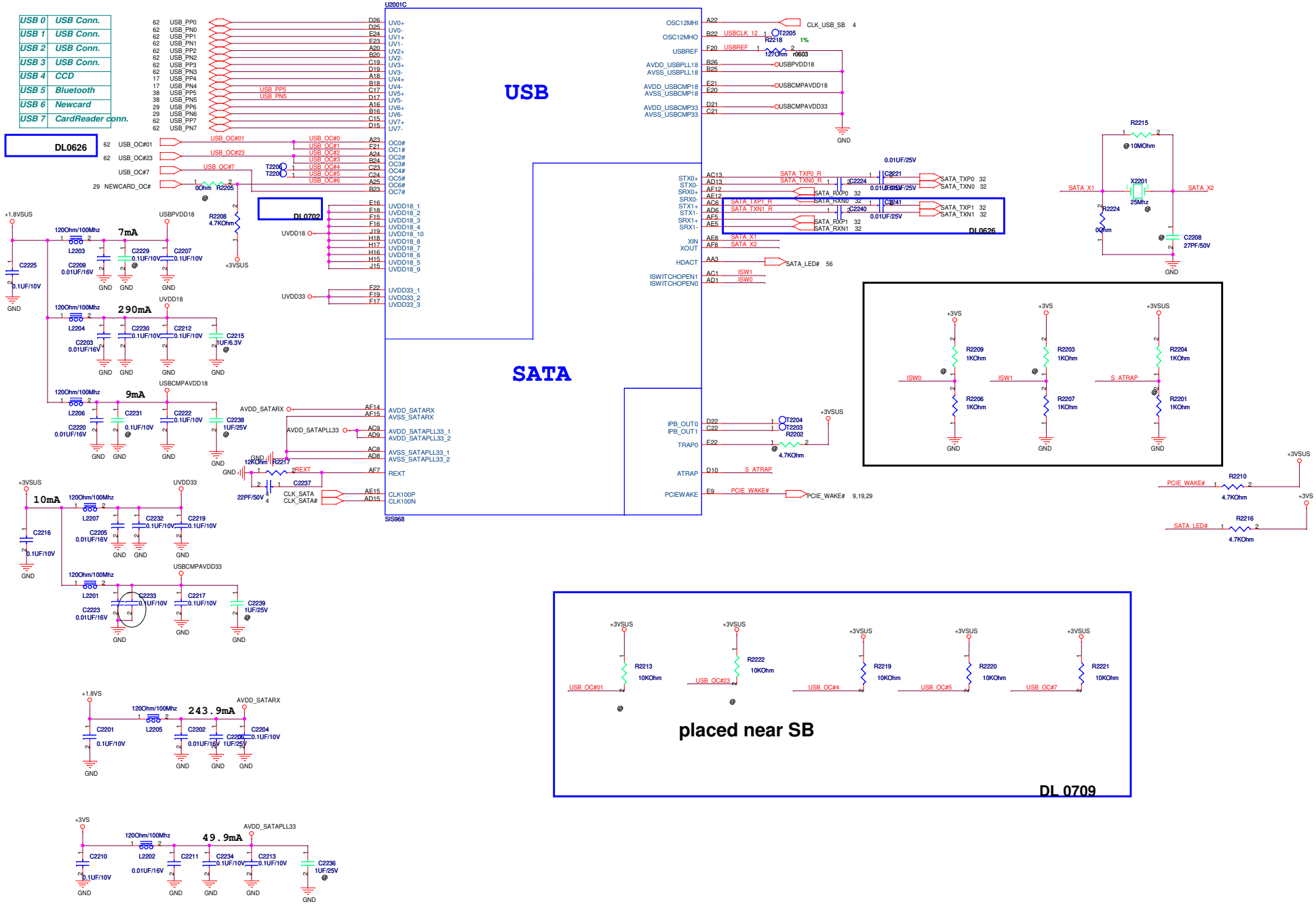
ASUSTeK COMPUTER INC. NB1

Title : 68-PCIE/AUDIO/ACPI/GPIO(2)

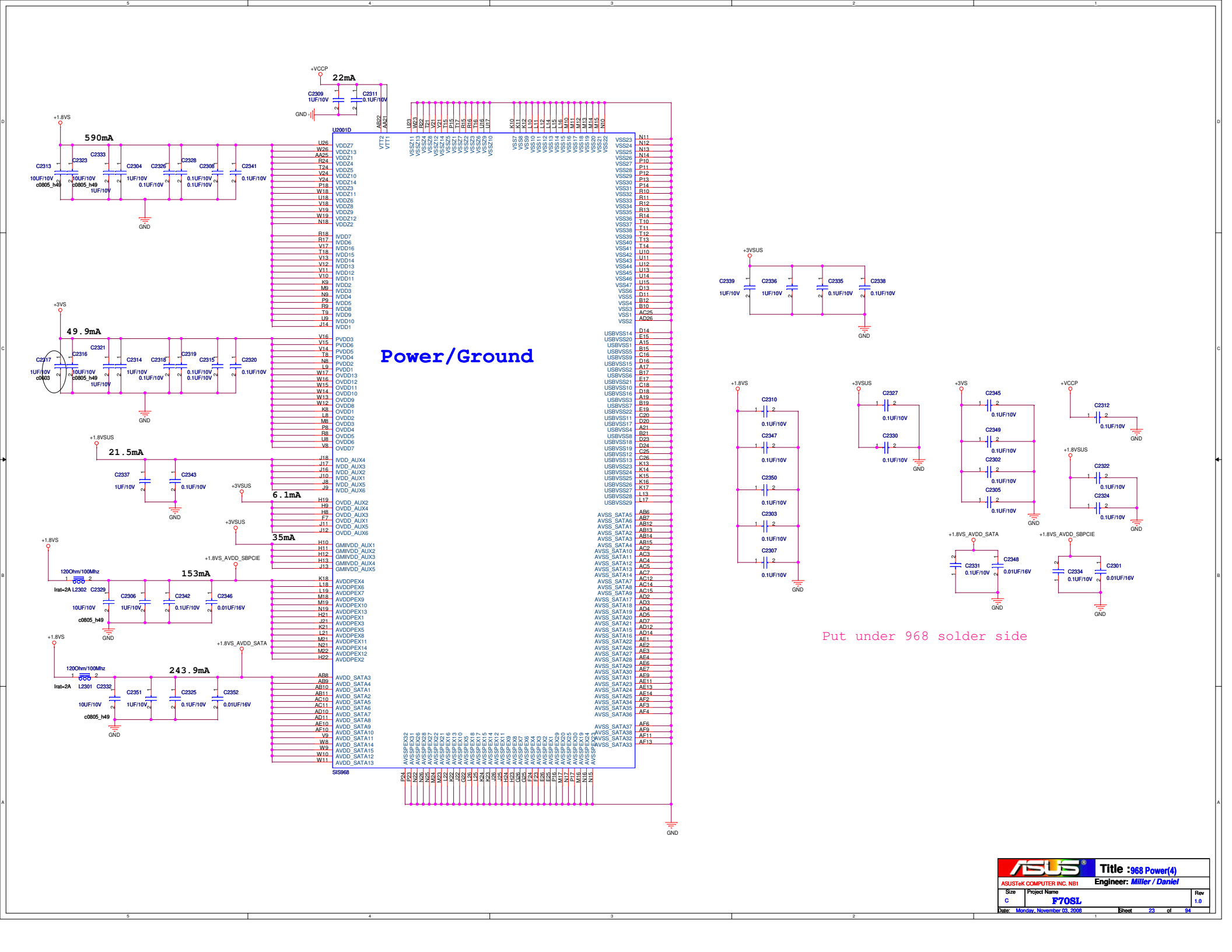
Engineer: Miller / Daniel

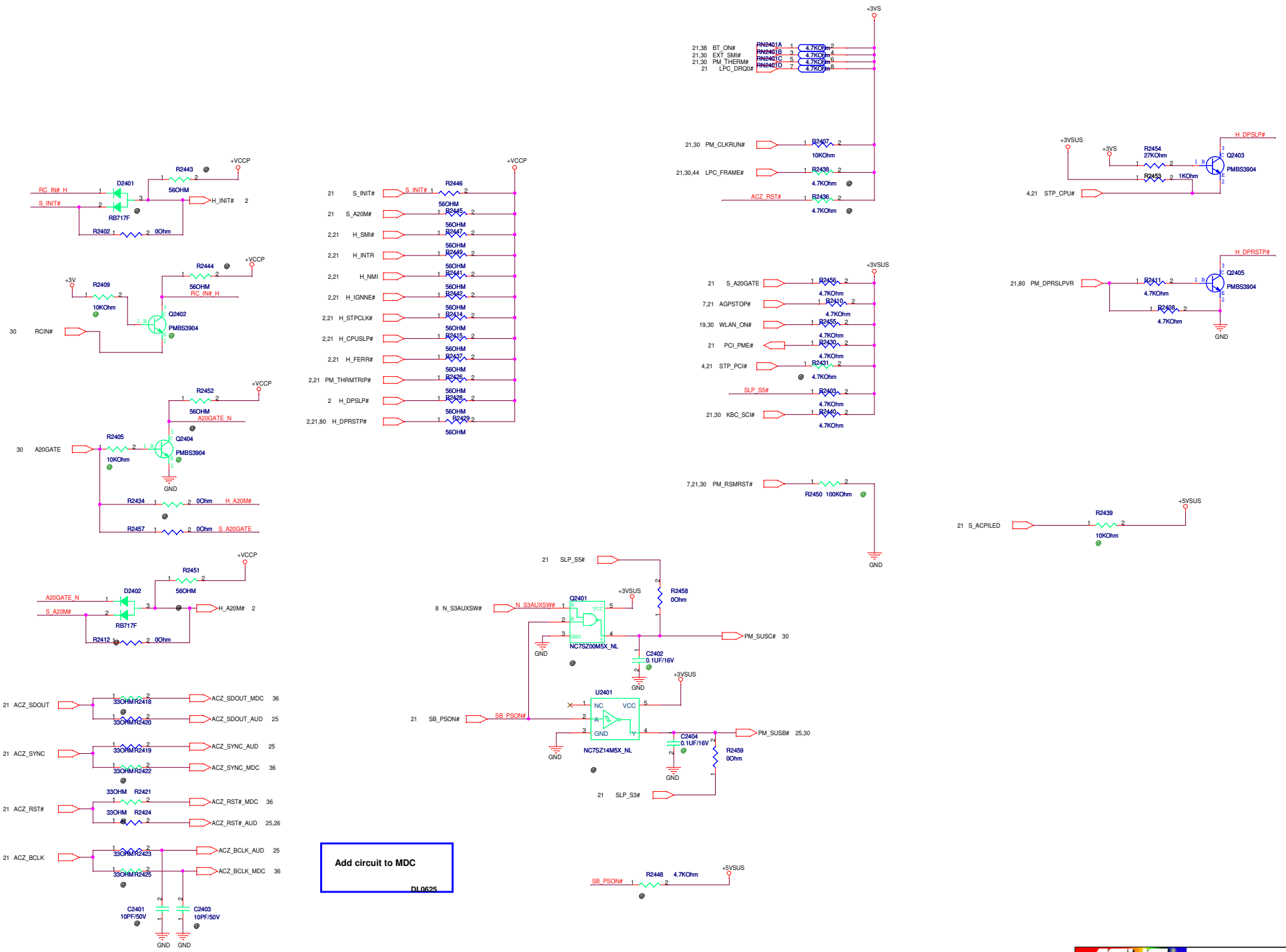
Size	Project Name	Rev
C	F70SL	1.0

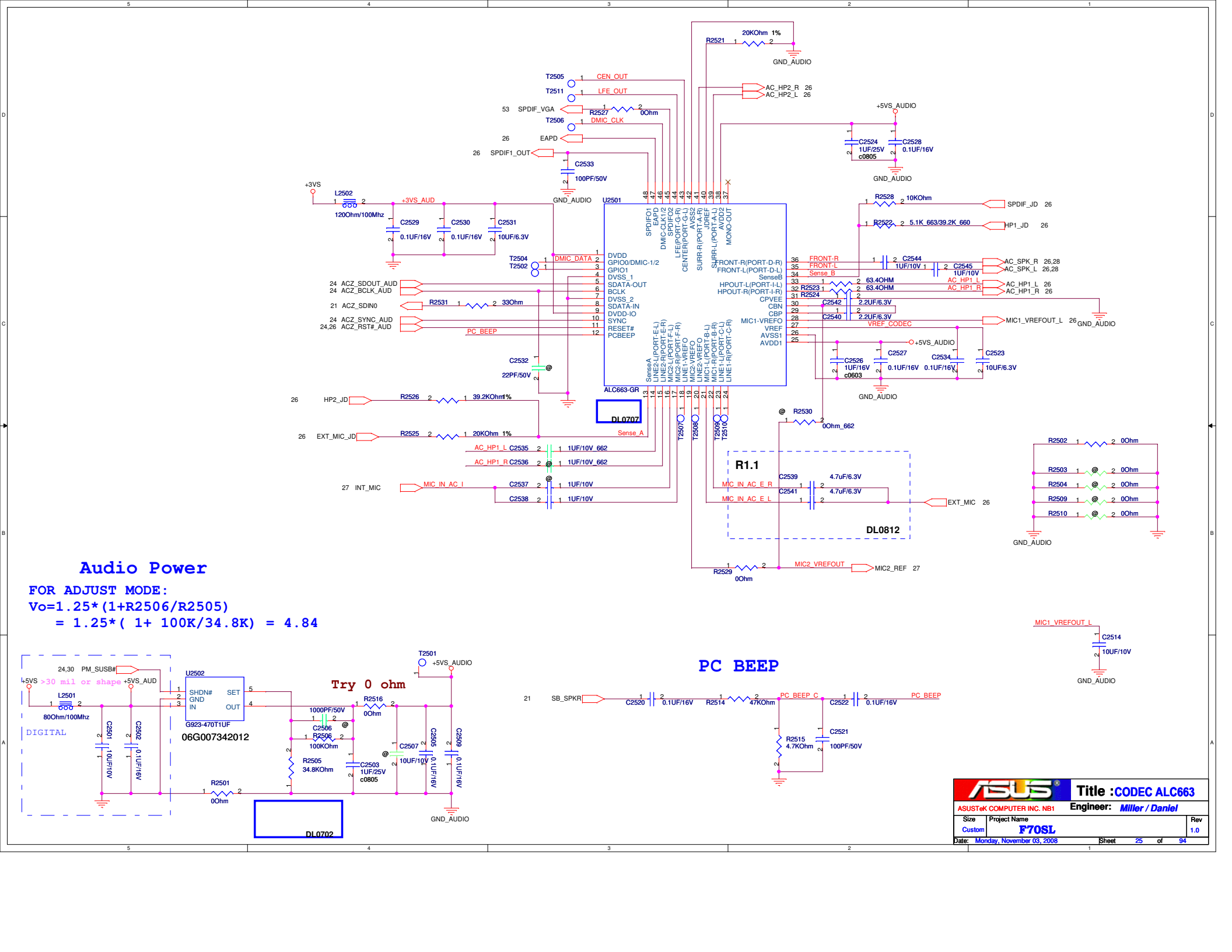
Date: Monday, November 03, 2008 Sheet 21 of 94



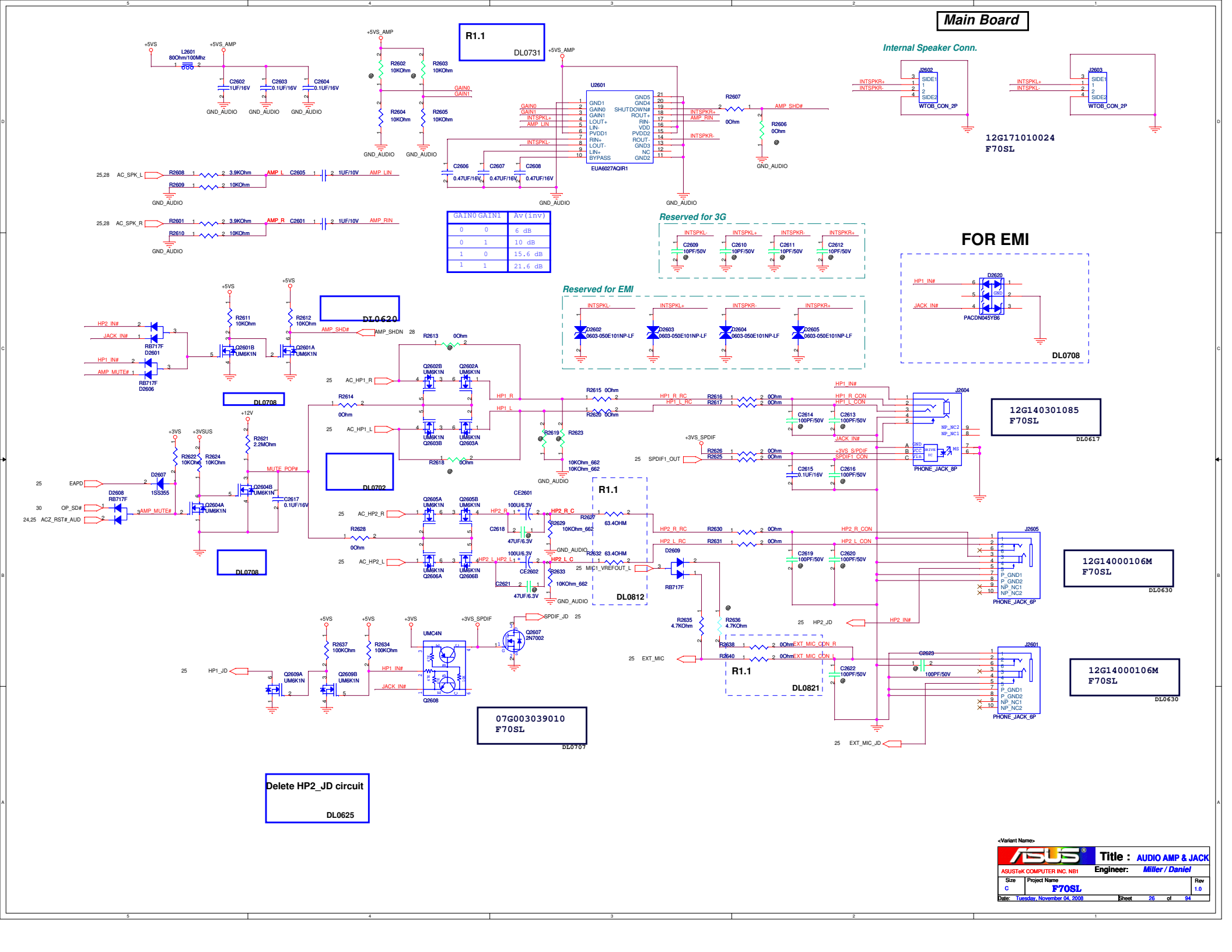
ASUS	Title : 968 USB/SATA(3)
ASUSTeK COMPUTER INC. NB1	Engineer: Miller / Daniel
Size: C	Project Name: F70SL
Rev: 1.0	
Date: Monday, November 03, 2008	Sheet 22 of 94


Power/Ground
U2001D
SIS968
590mA
49.9mA
21.5mA
6.1mA
35mA
153mA
243.9mA
22mA
+1.8VS
+3VS
+3VSUS
+1.8VSUS
+VCCP
+1.8VS_AVDD_SBPCIE
+1.8VS_AVDD_SATA
GND
Put under 968 solder side
Title :968 Power(4)
ASUSTeK COMPUTER INC. NB1
Engineer: Miller / Daniel
Project Name F70SL
Size C
Rev 1.0
Date: Monday, November 03, 2006
Sheet 23 of 94


+3VS
21,38 BT_ON#
21,30 EXT_SMI#
21,30 PM_THERM#
21 LPC_DRQ0#
RN2401A 4.7KOhm
RN2401B 4.7KOhm
RN2401C 4.7KOhm
RN2401D 4.7KOhm
21,30 PM_CLKRUN# R2407 10KOhm
21,30,44 LPC_FRAME# R2438 4.7KOhm @
ACZ_RST# R2436 4.7KOhm @
+3VSUS
+3VS
R2454 27KOhm
R2453 1KOhm
Q2403 PMBS3904
H_DPSLP#
4,21 STP_CPU#
+VCCP
R2443 @ 56OHM
D2401 RB717F
RC_IN# H
S_INIT#
H_INIT# 2
R2402 0Ohm
R2444 @ 56OHM
RC_IN# H
+3V
R2409 10KOhm @
Q2402 PMBS3904
30 RCIN#
21 S_INIT# R2446 56OHM
21 S_A20M# R2445 56OHM
2,21 H_SMI# R2447 56OHM
2,21 H_INTR R2449 56OHM
2,21 H_NMI R2441 56OHM
2,21 H_IGNNE# R2442 56OHM
2,21 H_STPCLK# R2414 56OHM
2,21 H_CPUSLP# R2415 56OHM
2,21 H_FERR# R2437 56OHM
2,21 PM_THRMTRIP# R2426 56OHM
2 H_DPSLP# R2428 56OHM
2,21,80 H_DPRSTP# R2429 56OHM
+3VSUS
21 S_A20GATE R2456 4.7KOhm
7,21 AGPSTOP# R2410 4.7KOhm
19,30 WLAN_ON# R2455 4.7KOhm
21 PCI_PME# R2430 4.7KOhm
4,21 STP_PCI# R2431 4.7KOhm @
SLP_S5# R2403 4.7KOhm
21,30 KBC_SCI# R2440 4.7KOhm
Q2405 PMBS3904
H_DPRSTP#
21,80 PM_DPRSLPVR
R2411 4.7KOhm
R2408 4.7KOhm
GND
+VCCP
R2452 56OHM A20GATE_N @
30 A20GATE
R2405 10KOhm @
Q2404 PMBS3904
GND
R2434 0Ohm H_A20M#
R2457 0Ohm S_A20GATE
7,21,30 PM_RSMRST#
R2450 100KOhm @
GND
+5VSUS
21 S_ACPILED
R2439 10KOhm @
+VCCP
R2451 56OHM
D2402 RB717F
A20GATE_N
S_A20M#
H_A20M# 2
R2412 0Ohm
21 SLP_S5#
8 N_S3AUXSW#
Q2401 NC7SZ00M5X_NL
+3VSUS
R2458 0Ohm
PM_SUSC# 30
C2402 0.1UF/16V @
GND
21 SB_PSON#
U2401 NC7SZ14M5X_NL
C2404 0.1UF/16V @
R2459 0Ohm
PM_SUSB# 25,30
21 SLP_S3#
21 ACZ_SDOUT
33OHM R2418
33OHM R2420
ACZ_SDOUT_MDC 36
ACZ_SDOUT_AUD 25
21 ACZ_SYNC
33OHM R2419
33OHM R2422
ACZ_SYNC_AUD 25
ACZ_SYNC_MDC 36
21 ACZ_RST#
33OHM R2421
33OHM R2424
ACZ_RST#_MDC 36
ACZ_RST#_AUD 25,26
21 ACZ_BCLK
33OHM R2423
33OHM R2425
ACZ_BCLK_AUD 25
ACZ_BCLK_MDC 36
C2401 10PF/50V @
C2403 10PF/50V @
GND GND
Add circuit to MDC
DL0625
SB_PSON#
R2448 4.7KOhm @
+5VSUS
ASUSTeK COMPUTER INC. NB1
Title : 968 Strap(5)
Engineer: Miller / Daniel
Size C
Project Name F70SL
Rev 1.0
Date: Monday, November 03, 2008
Sheet 24 of 84

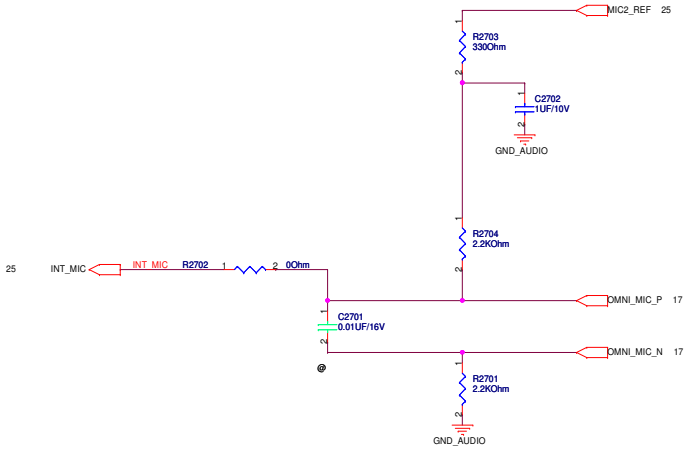

Audio Power
FOR ADJUST MODE:
Vo=1.25*(1+R2506/R2505)
= 1.25*(1+ 100K/34.8K) = 4.84
PC BEEP
Try 0 ohm
ALC663-GR
U2501
U2502
G923-470T1UF
06G007342012
DL0707
DL0812
DL0702
R1.1
DIGITAL
Title :CODEC ALC663
ASUSTeK COMPUTER INC. NB1
Engineer: Miller / Daniel
Project Name F70SL
Rev 1.0
Date: Monday, November 03, 2008
Sheet 25 of 94

Main Board

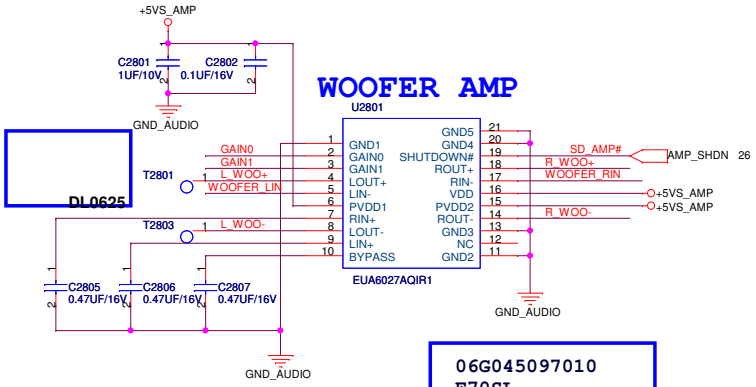


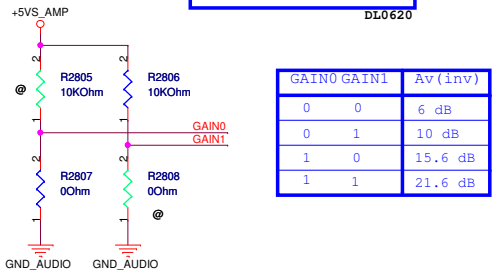
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : AUDIO AMP & JACK	
	Engineer: Miller / Daniel	
Size: C	Project Name: F70SL	Rev: 1.0
Date: Tuesday, November 04, 2008	Sheet 26 of 94	

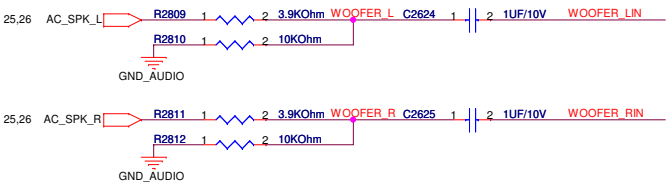


ASUSTeK COMPUTER INC. NB1	Title :	
	Engineer: Miller / Daniel	
Size: C	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 27 of 94	





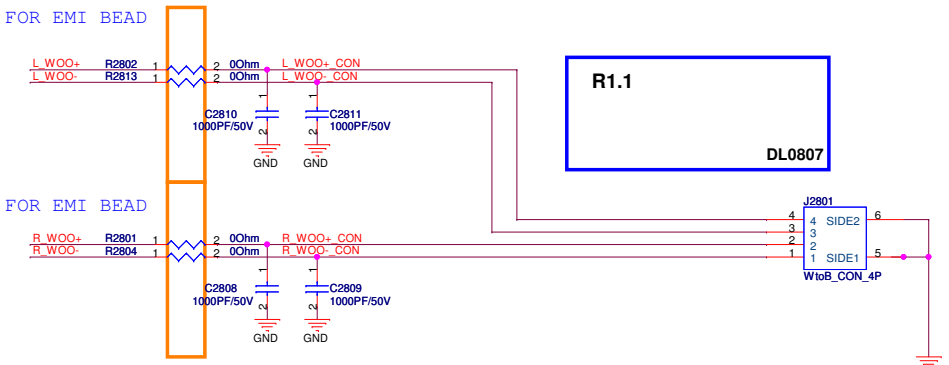
GAIN0	GAIN1	Av(inv)
0	0	6 dB
0	1	10 dB
1	0	15.6 dB
1	1	21.6 dB



R1.1

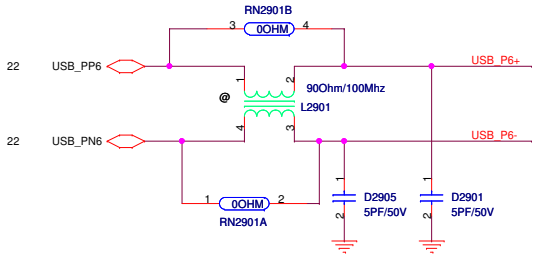
DL0807

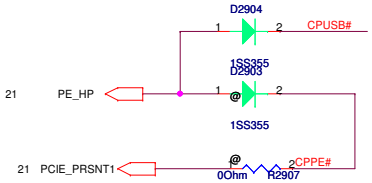
SPEAKER CONNECTOR WOOFER

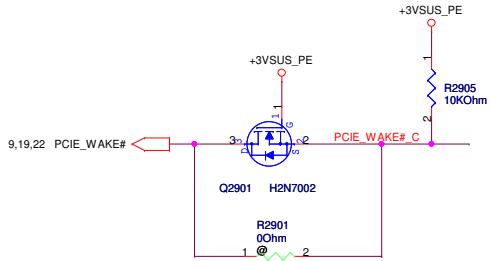


ASUS	Title : Woofer	
ASUSTeK COMPUTER INC. NB1	Engineer: Miller / Daniel	
Size: Custom	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 28 of 94	

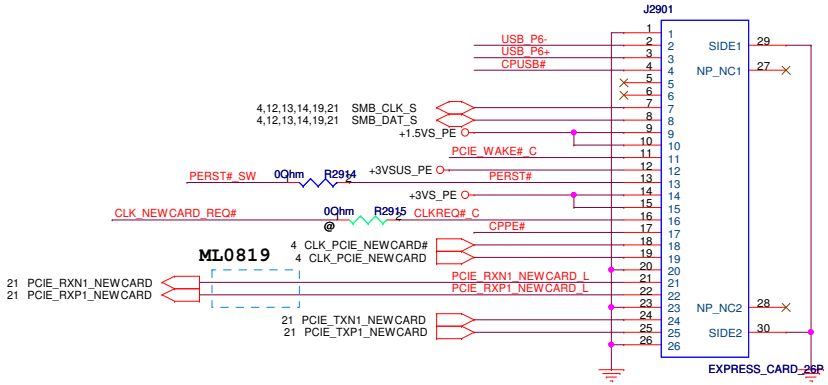
FOR SWAP



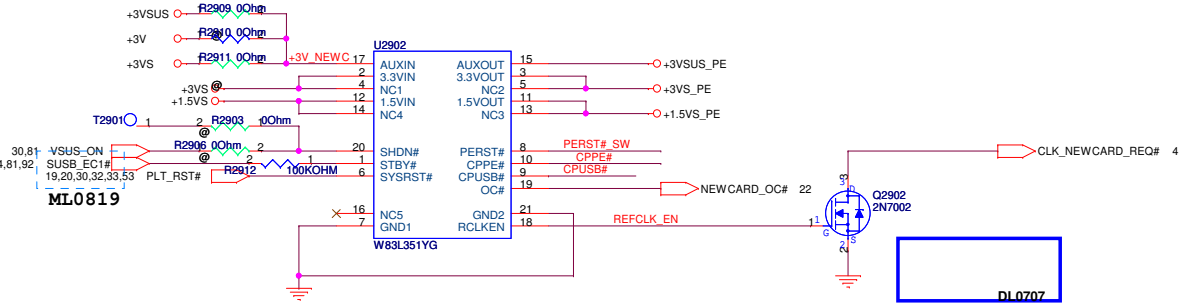




!ExpressCard Standard 1.0:
Change Pin7 from RESERVED to SMBCLK
Change Pin8 from SMBCLK to SMBDATA
Change Pin9 from SMBDATA to +1.5V

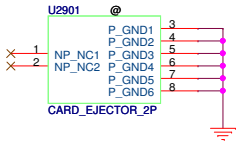


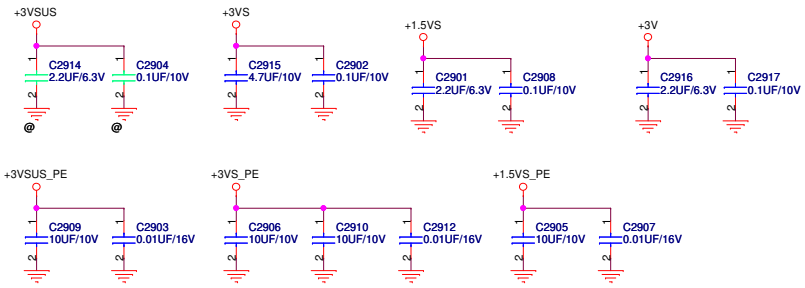
12G161320266
F70SL
DL0619



ML0819

DL0707





<Variant Name>

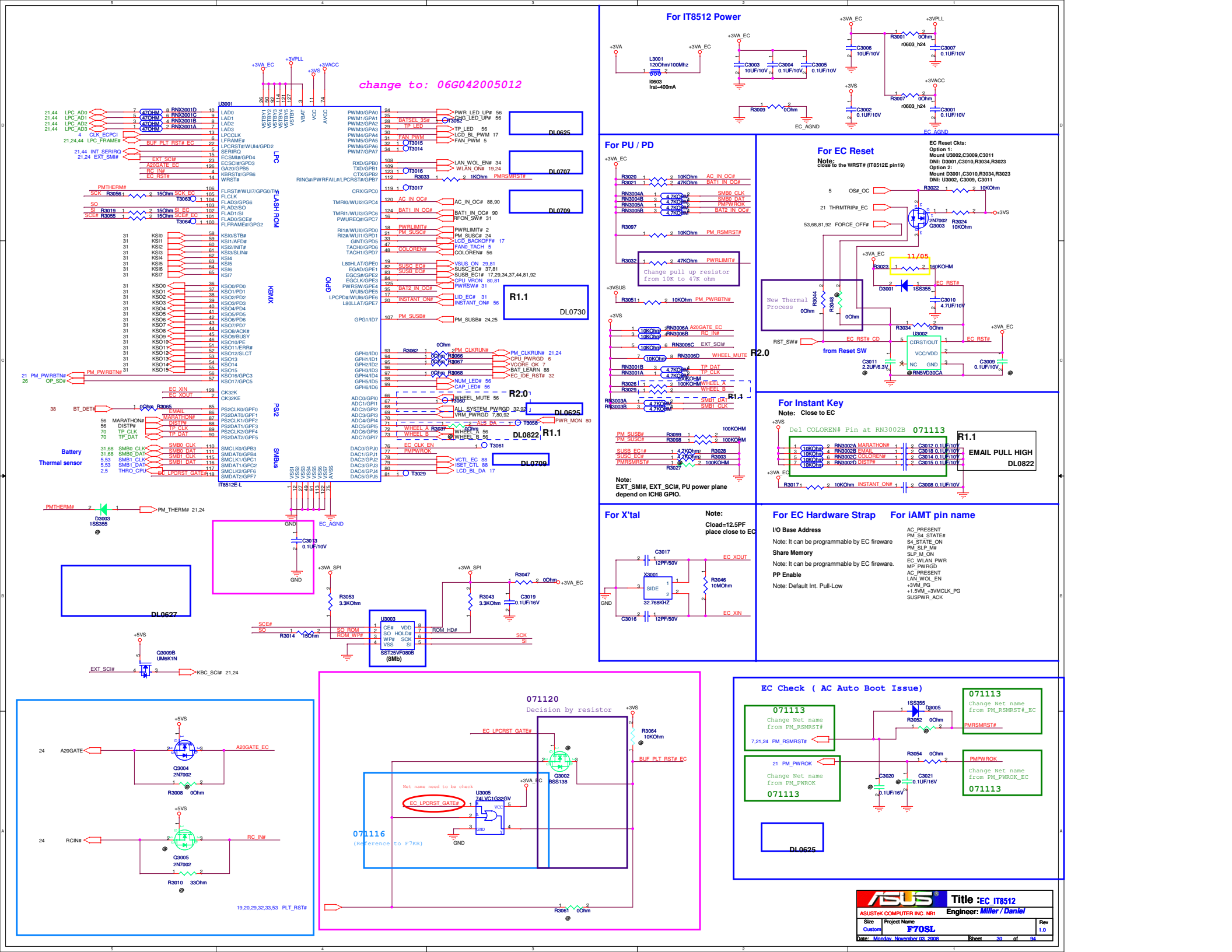
ASUSTeK COMPUTER INC

Title : NEWCARD

Engineer: Miller / Daniel

Size	Project Name	Rev
Custom	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 29 of 94


change to: 06G042005012
U3001
IT8512E-L
LPC
FLASH ROM
KBMX
GPIO
PS2
SMBus
Battery
Thermal sensor
For IT8512 Power
For PU / PD
For EC Reset
For Instant Key
For X'tal
For EC Hardware Strap
For iAMT pin name
EC Reset Ckts:
Option 1:
Mount U3002,C3009,C3011
DNI: D3001,C3010,R3034,R3023
Option 2:
Mount D3001,C3010,R3034,R3023
DNI: U3002, C3009, C3011
Note:
close to the WRST# (IT8512E pin19)
Change pull up resistor from 10K to 47K ohm
Note:
EXT_SMI#, EXT_SCI#, PU power plane depend on ICH8 GPIO.
Note: Close to EC
Del COLOREN# Pin at RN3002B 071113
EMAIL PULL HIGH
DL0822
Note:
Cload=12.5PF
place close to EC
I/O Base Address
Note: It can be programmable by EC fireware
Share Memory
Note: It can be programmable by EC fireware.
PP Enable
Note: Default Int. Pull-Low
AC_PRESENT
PM_S4_STATE#
S4_STATE_ON
PM_SLP_M#
SLP_M_ON
EC_WLAN_PWR
MP_PWRGD
AC_PRESENT
LAN_WOL_EN
+3VM_PG
+1.5VM_+3VMCLK_PG
SUSPWR_ACK
071120
Decision by resistor
071116
(Reference to F7KR)
Net name need to be check
EC Check (AC Auto Boot Issue)
071113
Change Net name from PM_RSMRST#
Change Net name from PM_PWROK
Change Net name from PM_RSMRST#_EC
Change Net name from PM_PWROK_EC
DL0625
DL0627
DL0707
DL0709
DL0730
DL0822
R1.1
R2.0
ASUSTeK COMPUTER INC. NB1
Title :EC_IT8512
Engineer: Miller / Daniel
Project Name
F70SL
Rev
1.0
Date: Monday, November 03, 2008
Sheet 30 of 94

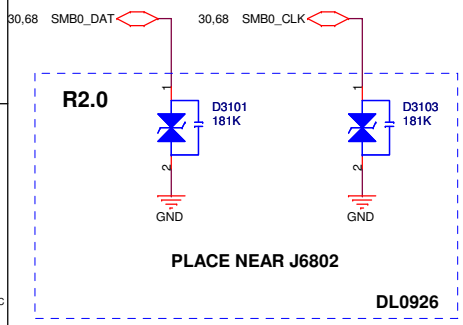
For Battery

Single Battery

BAT1_CNT1#, BAT1_CNT2#,
BAT2_CNT1#, BAT2_CNT2#
don't connect to Battery
Connector.

Dual Battery

BAT1_CNT1#, BAT1_CNT2#,
BAT2_CNT1#, BAT2_CNT2#
must connect to Battery
Connector.

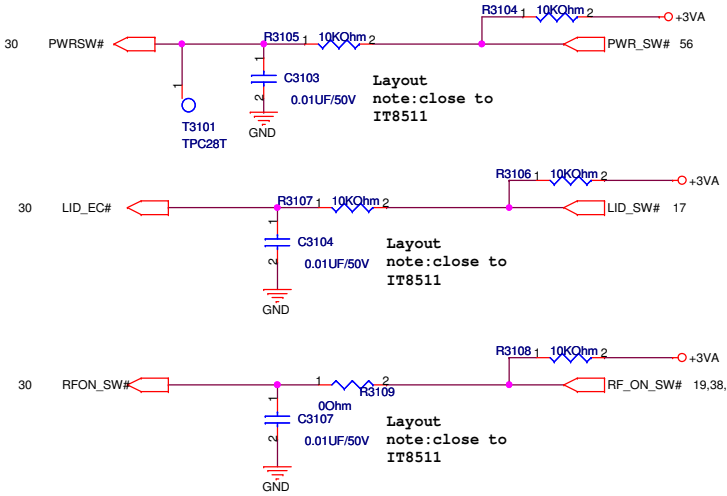


Note:

When we plug in or plug out the battery, it may cause a spike to damage the EC and gas gauge. It needed to add these varistors to protect those pins.

close to connector

For Switch

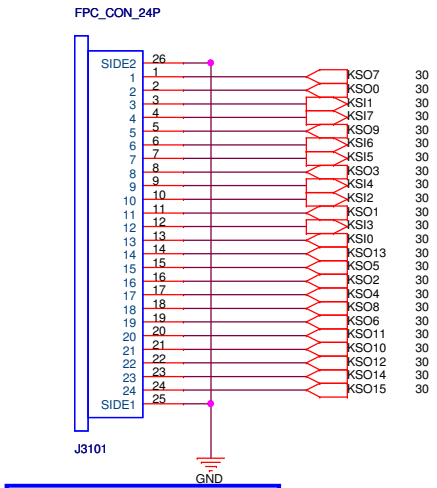


Note:

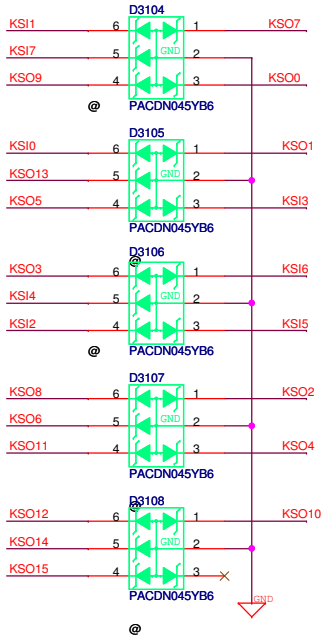
This LID_EC# is a signal from inverter board, it is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. It needed to add bidirectional diode to protect this pin.

For External PS/2 I/F

For Keyboard



EMI recommandation. To protect KBC destroy by ESD. Need put between KB connector and KBC, and close to the connector as possible.



Each IC needs 2 vias to ground.

DL0625

<Variant Name>

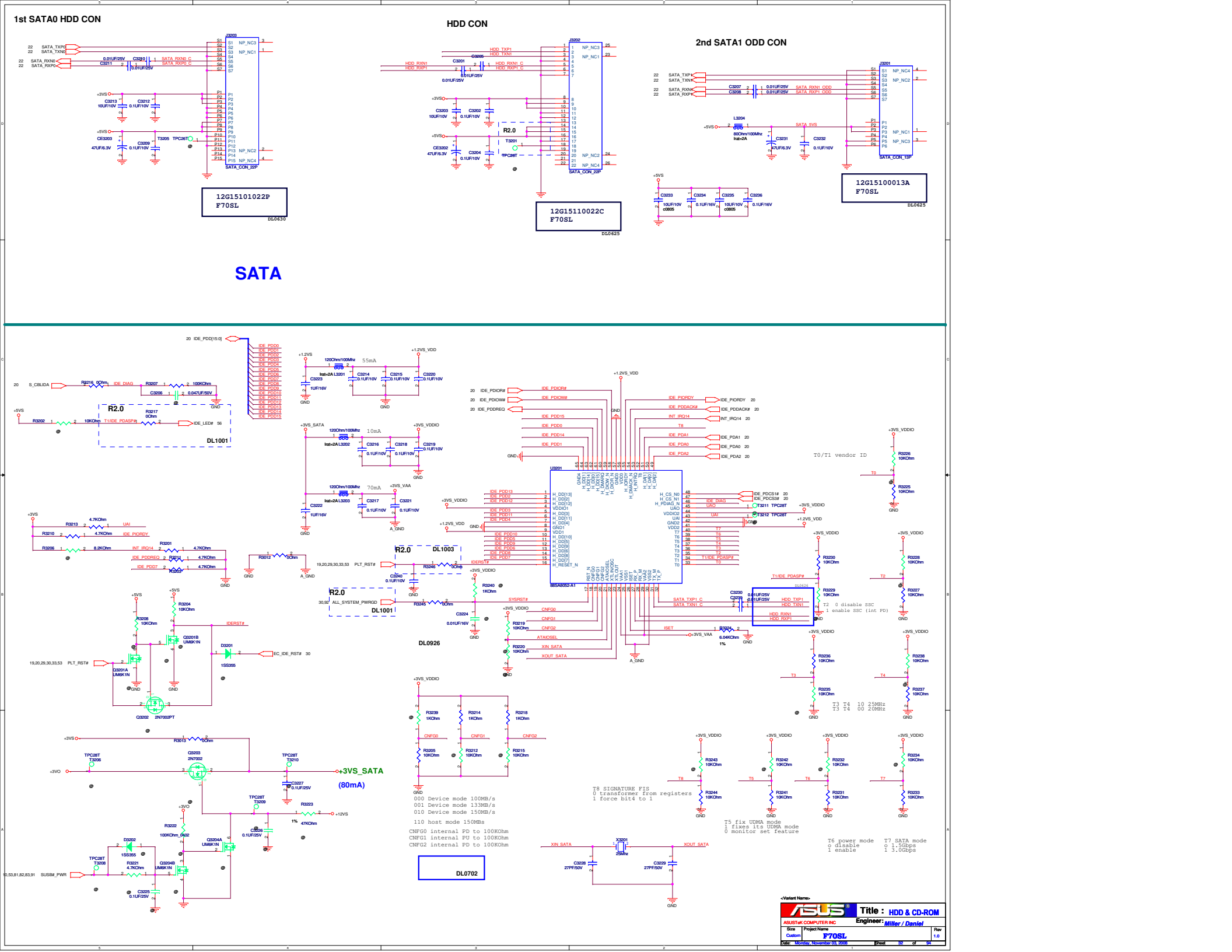
Title : KB&ISA ROM

ASUSTeK COMPUTER INC. NB1

Engineer: Miller / Daniel

Size	Project Name	Rev
Custom	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 31 of 94


1st SATA0 HDD CON
HDD CON
2nd SATA1 ODD CON
12G15101022P
F70SL
DL0630
12G15110022C
F70SL
DL0625
12G15100013A
F70SL
DL0625
SATA
DL1001
DL1003
DL0926
DL0702
R2.0
T0/T1 vendor ID
T8 SIGNATURE FIS
0 transformer from registers
1 force bit4 to 1
000 Device mode 100MB/s
001 Device mode 133MB/s
010 Device mode 150MB/s
110 host mode 150MBs
CNFG0 internal PD to 100KOhm
CNFG1 internal PU to 100KOhm
CNFG2 internal PD to 100KOhm
T5 fix UDMA mode
1 fixes its UDMA mode
0 monitor set feature
T6 power mode
0 disable
1 enable
T7 SATA mode
0 1.5Gbps
1 3.0Gbps
T2 0 disable SSC
1 enable SSC (int PD)
T3 T4 10 25MHz
T3 T4 00 20MHz
+3VS_SATA
(80mA)
Title : HDD & CD-ROM
ASUSTeK COMPUTER INC
Engineer: Miller / Daniel
Project Name F70SL
Rev 1.0
Monday, November 03, 2008
Sheet 32 of 94

Average supply current
VDD33 65mA
AVDD18 103mA
VDD15+AVDD15 241mA

RTL 8211B

RC power-up reset

For wake on LAN function
Stuff R3510, C3504 and Nostuff R3512

Place near to 968

R2.0 EMI DL1001

R2.0 EMI DL1002

ML0820

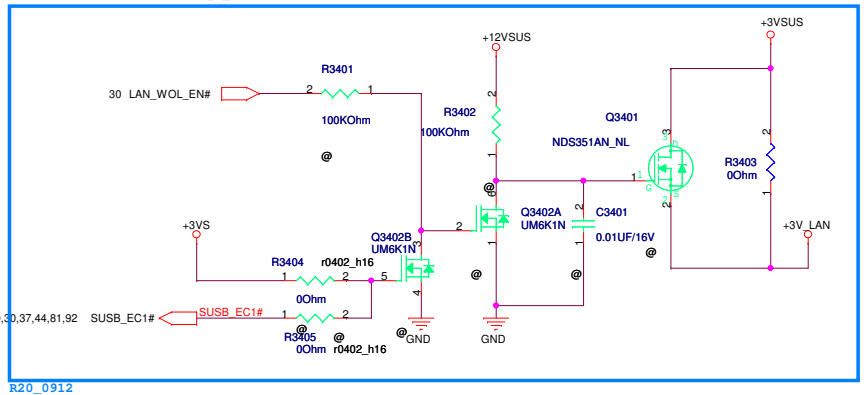
R1.1 DL0731

DL0702

EN-0055974 For Page33 LAN linking slow issue BOM change 20071227
(1)RXDLY pull high
(2)RX_CLK and Data R3327,R3328,R3329,R3330,R3332 and R3331, change to 0 ohm
(3)TXDLY Pull high
(4)Delete C3307

ASUSTECH CO.,LTD.	Title :	Giga LAN RTL8211B
	Engineer:	Miller / Daniel
Size: Custom	Project Name: F70SL	Rev: 1.1
Date: Monday, November 03, 2008	Sheet 33 of 94	

For Energy V4.0



+3VSUS +3VSUS 8,9,19,21,22,23,24,26,29,30,36,81,91

<Variant Name>

ASUSTeK COMPUTER INC	Title : ENERGY STAR	
	Engineer: Miller / Daniel	
Size: Custom	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 34 of 94	

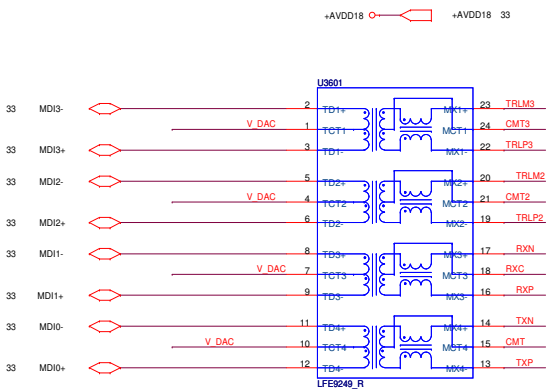
Title : BLANK

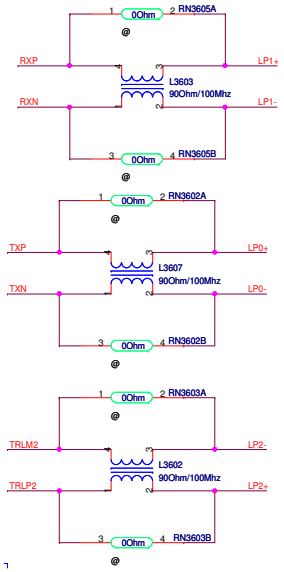
ASUSTeK Computer INC

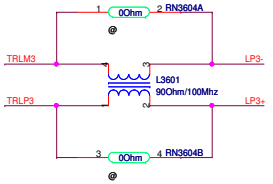
Engineer: Miller / Daniel

Size	Project Name	Rev
B	F70SL	1.0

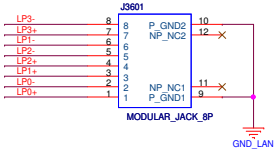
Date: Monday, November 03, 2008 Sheet 35 of 94



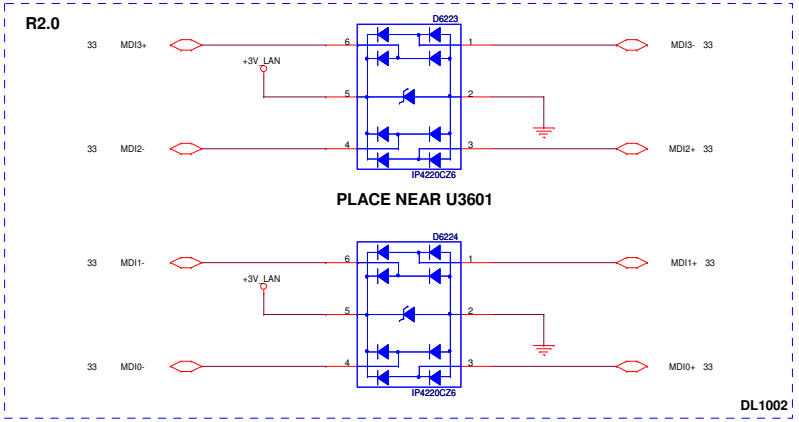


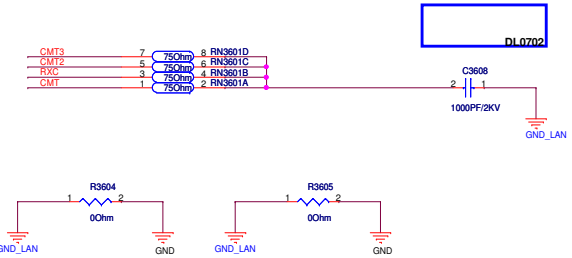


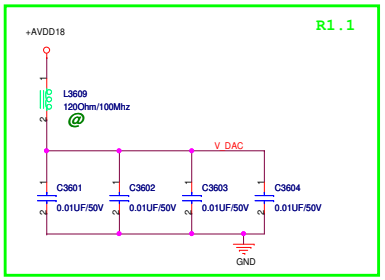
LAN PORT



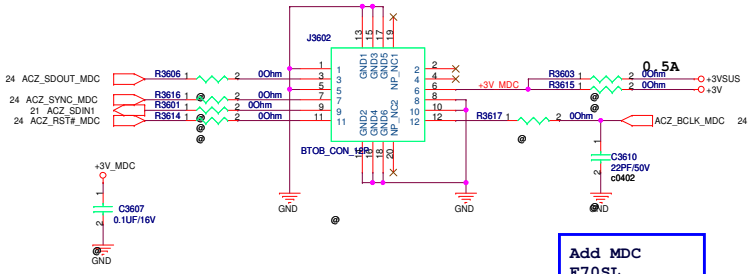
12G14851108M
F70SL
DL0623



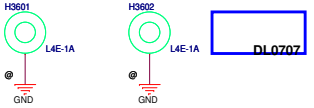




MDC

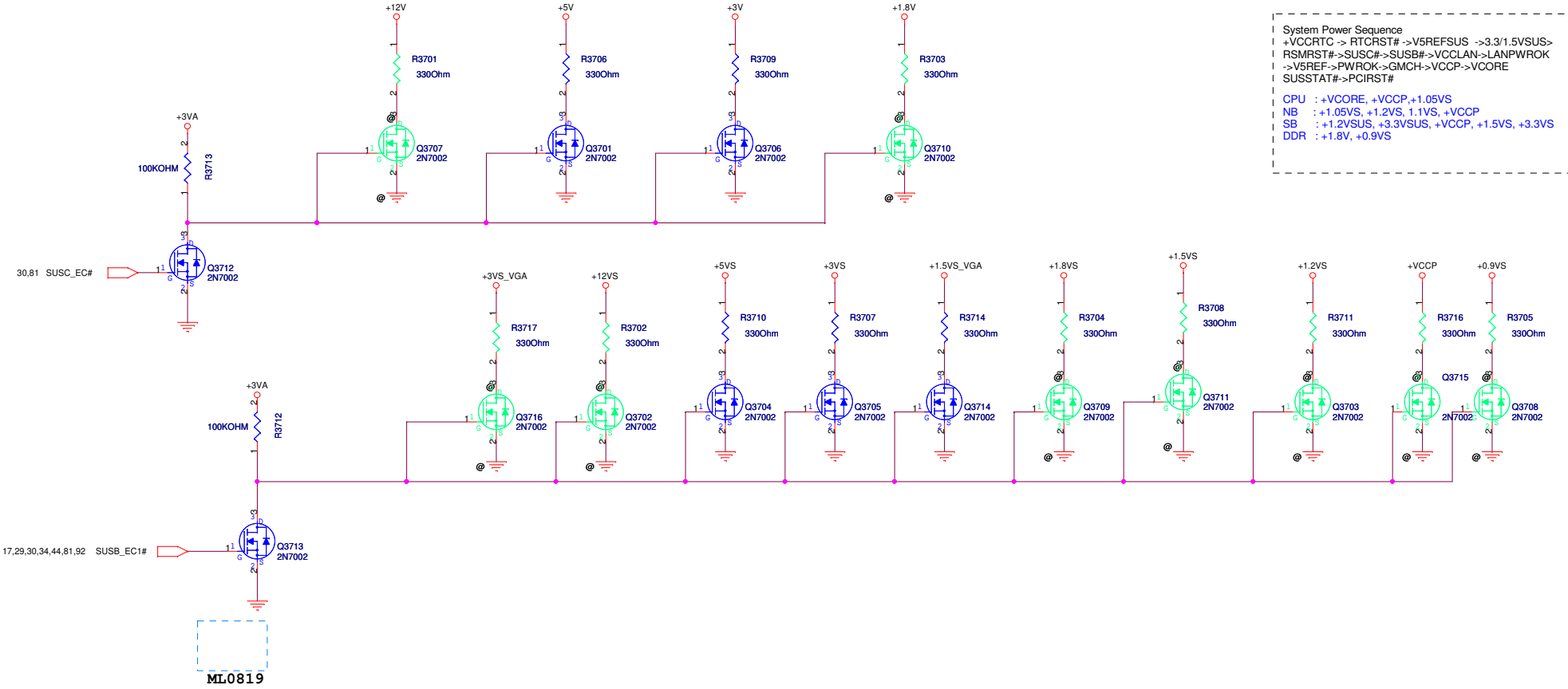


Add MDC
F70SL
DL0625



DL0707

ASUSTeK COMPUTER INC	Title : RJ11+45 & MDC	
	Engineer: Miller / Daniel	
Size: C	Project Name: F70SL	Rev: 1.0
Date: Monday, November 17, 2008	Sheet 38 of 94	



System Power Sequence
+VCCRTC -> RTCRST# ->V5REFSUS ->3.3/1.5VSUS>
RSMRST#->SUSC#->SUSB#->VCCLAN->LANPWROK
->V5REF->PWROK->GMCH->VCCP->VCORE
SUSSTAT#->PCIRST#

CPU : +VCORE, +VCCP,+1.05VS
NB : +1.05VS, +1.2VS, 1.1VS, +VCCP
SB : +1.2VSUS, +3.3VSUS, +VCCP, +1.5VS, +3.3VS
DDR : +1.8V, +0.9VS

<Variant Name>

ASUSTeK COMPUTER INC

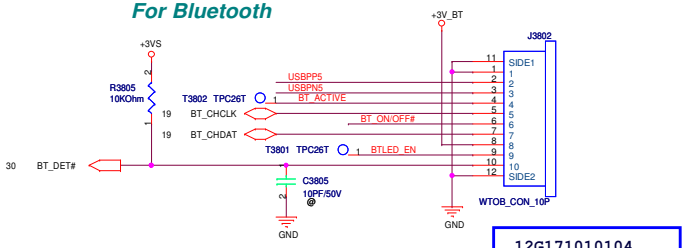
Title : DISCHARGE CKT

Engineer: Miller / Daniel

Size	Project Name	Rev
Custom	F70SL	1.0

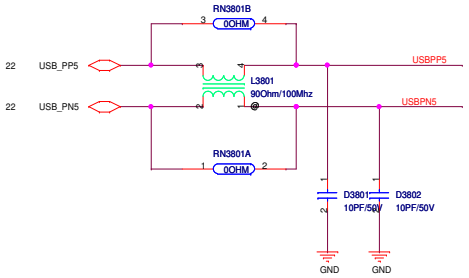
Date: Monday, November 03, 2008 Sheet 37 of 94

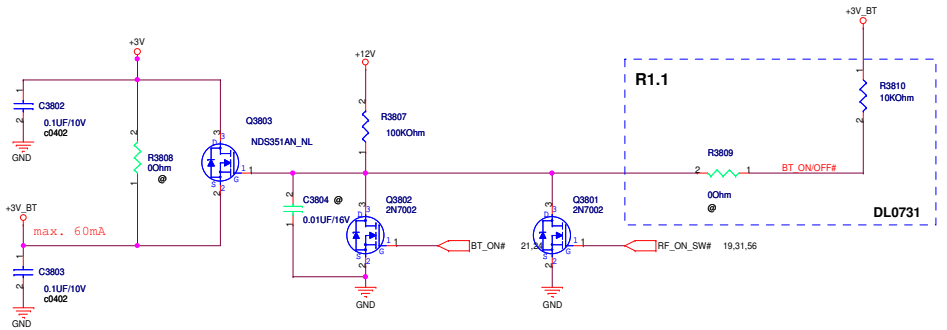
For Bluetooth



12G171010104
F70SL

ML0617





DL0707

<Variant Name>

Title : BT

ASUSTeK COMPUTER INC. NB1

Engineer: Miller / Daniel

Size	Project Name	Rev
C	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 38 of 94

DL0619

<Variant Name>

Title : SWITCH

ASUSTeK COMPUTER INC

Engineer: Miller / Daniel

Size	Project Name	Rev
Custom	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 39 of 94

Delete R5C833

DL0626

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : R5C833(1)	
	Engineer: Miller / Daniel	
Size: Custom	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 40 of 94	

Delete R5C833

DL0626

ASUSTeK COMPUTER INC. NB1	Title : R5C833(2)	
	Engineer: Miller / Daniel	
Size: Custom	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 41 of 94	

ASUSTeK COMPUTER INC. NB1	Title : CardReader Conn.		
	Engineer: Miller / Daniel		
Size: C	Project Name: F70SL		Rev: 1.0
Date: Monday, November 03, 2008	Sheet 42 of 94		

<Variant Name>

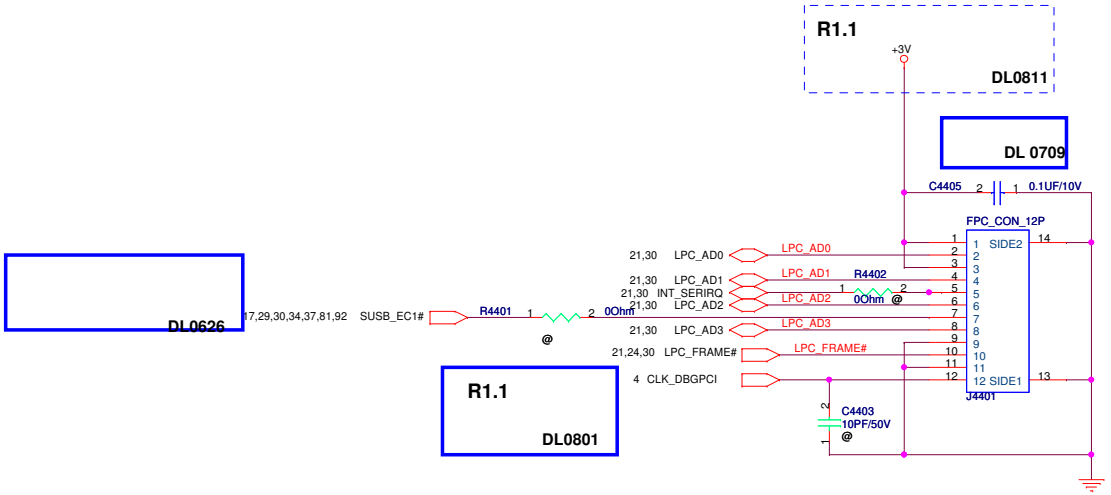
Title N/A

ASUSTeK COMPUTER INC

Engineer: Miller / Daniel

Size	Project Name	Rev
Custom	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 43 of 94



ASUSTeK COMPUTER INC. NB1	Title : debug		
	Engineer: Miller / Daniel		
Size: Custom	Project Name: F70SL		Rev: 1.0
Date: Monday, November 03, 2008	Sheet 44 of 94		

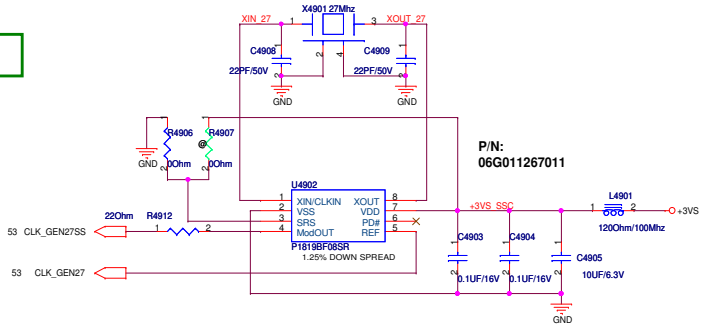
ASUSTeK COMPUTER INC	Title : N/A	
	Engineer: Miller / Daniel	
Size: C	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 45 of 94	

ASUSTeK COMPUTER INC	Title : N/A		
	Engineer: Miller / Daniel		
Size: C	Project Name: F70SL		Rev: 1.0
Date: Monday, November 03, 2008	Sheet 46 of 94		

ASUSTeK COMPUTER INC		Title : N/A	
		Engineer: Miller / Daniel	
Size: C	Project Name: F70SL		Rev: 1.0
Date: Monday, November 03, 2008		Sheet 47 of 94	

ASUSTeK COMPUTER INC		Title : N/A	
		Engineer: Miller / Daniel	
Size: C	Project Name: F70SL		Rev: 1.0
Date: Monday, November 03, 2006		Sheet 48 of 94	

XTAL_IN , XTAL_OUT
3.3V tolerance



ASUSTeK COMPUTER INC	Title : DACs/CLK	
	Engineer: Miller / Daniel	
Size: C	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 49 of 94	

ASUSTeK COMPUTER INC	Title : N/A		
	Engineer: Miller / Daniel		
Size: C	Project Name: F70SL		Rev: 1.0
Date: Monday, November 03, 2008	Sheet 50 of 94		

ASUSTeK COMPUTER INC	Title : N/A		
	Engineer: Miller / Daniel		
Size: C	Project Name: F70SL		Rev: 1.0
Date: Monday, November 03, 2008	Sheet 51 of 94		

DL0611

ASUSTeK COMPUTER INC	Title : N/A		
	Engineer: Miller / Daniel		
Size: C	Project Name: F70SL		Rev: 1.0
Date: Monday, November 03, 2008	Sheet 52 of 94		

PEX: NB =>MXM
EXP: VGA Card =>NB

J5301A

DVI
CRT
VGA
LVDS
IGP
TV-OUT
SMBUS
PEX
OTHER

J5301B
MXM_230P

Pin 218 reserve for ATI HDTV EN#

12G161802308
F70SL

JP0201:
OPEN: FBVTT = VGA card regulator(FBVTT_VGA)
SHORT: FBVTT = MB(+0.9V_VGA)

ML0819

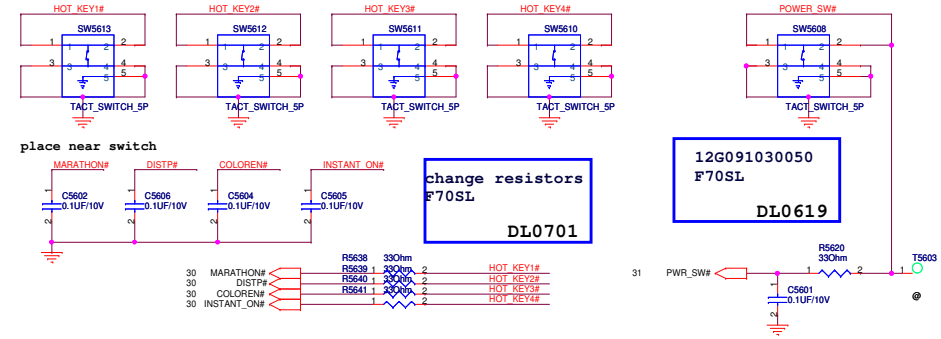
12G161802308
F70SL

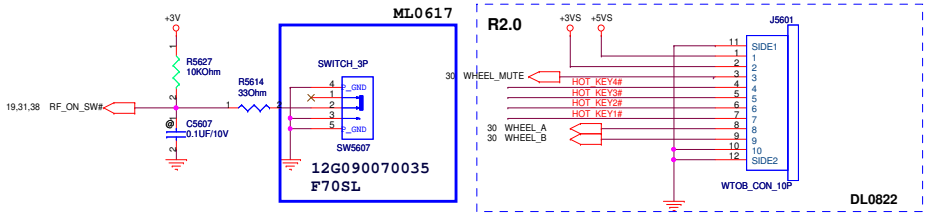
Title :	MXM
ASUSTeK COMPUTER INC. NB1	Engineer: Miller / Daniel
Size: Custom	Project Name: F70SL
Rev: 1.0	
Date: Monday, November 03, 2008	Sheet 53 of 94

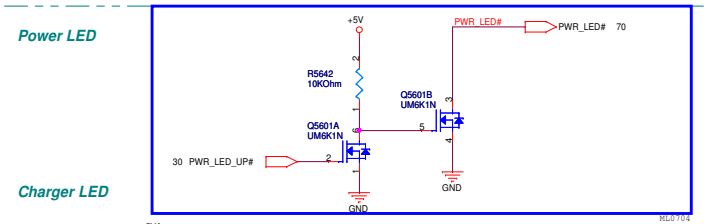
Title :	BLANK
ASUSTeK COMPUTER INC. NB1	Engineer: Miller / Daniel
Size: A	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 54 of 94

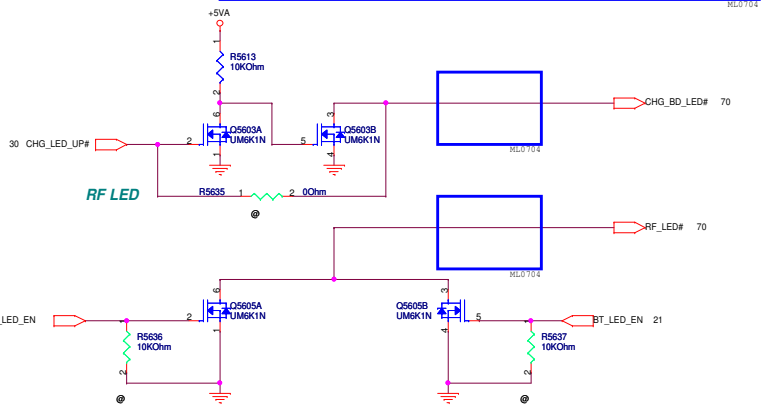
ASUSTeK COMPUTER INC. NB1	Title : SS STRAPS	
	Engineer: Miller / Daniel	
Size: Custom	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 55 of 94	

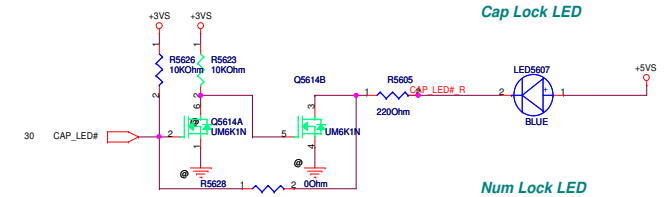
Main Board

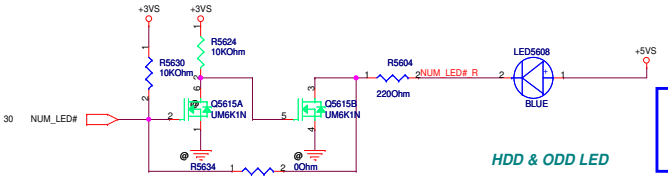


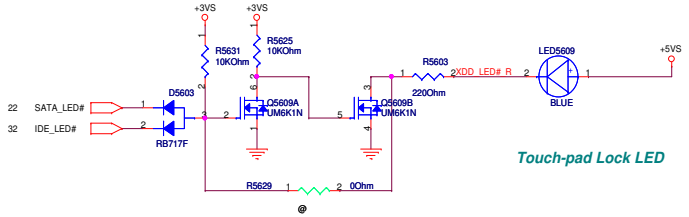


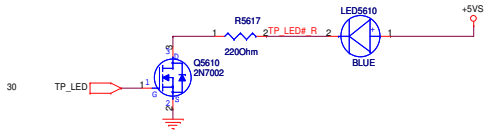












R1.1

DELETE MAIL LED CIRCUIT

DL0810

ASUSTeK COMPUTER INC. NB1	Title : <Title>	
	Engineer: Miller / Daniel	
Size: C	Project Name: F70SL	Rev: 1.0
Date: Tuesday, November 18, 2008	Sheet 56 of 94	

Title :	+1.2VSUS
ASUSTeK COMPUTER INC. NB1	Engineer: Miller / Daniel
Size: A	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 57 of 94

ASUSTeK COMPUTER INC. NB1	Title : NA		
	Engineer: Miller / Daniel		
Size: C	Project Name: X71C		Rev: 1.0
Date: Monday, November 03, 2008	Sheet 58 of 94		

Title :	EMI
ASUSTeK COMPUTER INC. NB1	Engineer: Miller / Daniel
Size: A	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 59 of 94

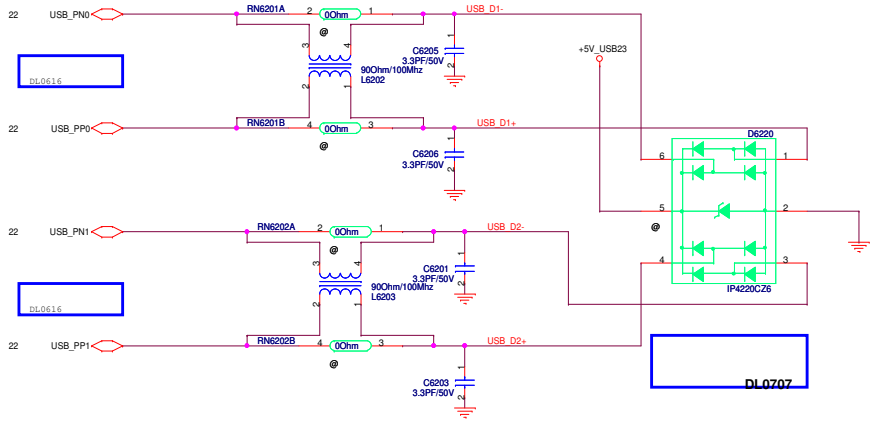
Delete SPIF215A

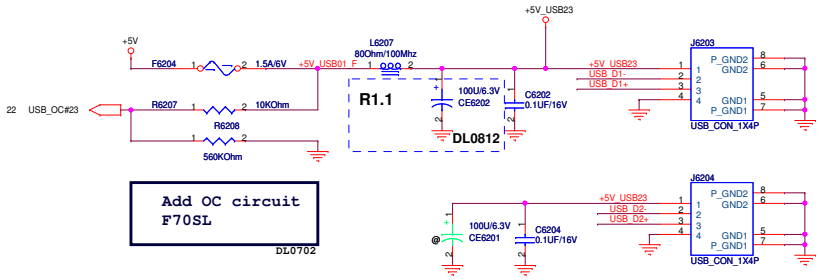
DL0626

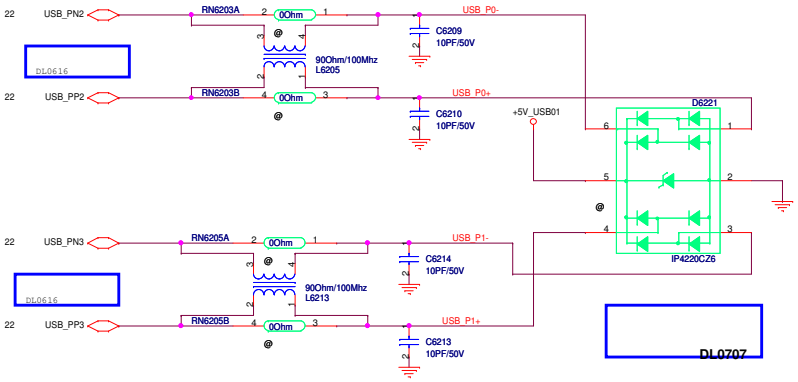
ASUSTeK COMPUTER INC. NB1	Title : USB SATA adapter	
	Engineer: Miller / Daniel	
Size: C	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 60 of 94	

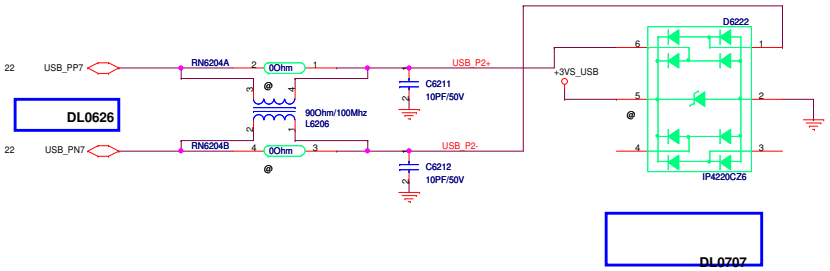
DL0616

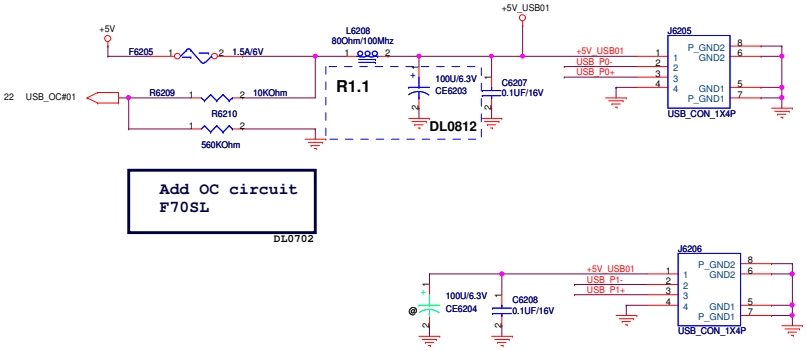
ASUSTeK COMPUTER INC. NB1	Title : USB HUB	
	Engineer: Miller / Daniel	
Size: B	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 61 of 94	





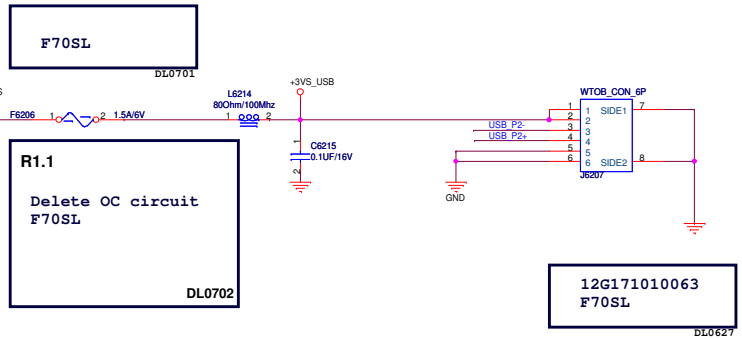






CardReader Connector

DL0626



<Variant Name>

ASUSTeK COMPUTER INC

Title : USB CONN

Engineer: Miller / Daniel

Size	Project Name	Rev
C	F70SL	1.0

Date: Thursday, November 13, 2008 Sheet 62 of 94

Title : BLANK

ASUSTeK COMPUTER INC. NB1

Engineer: Miller / Daniel

Size	Project Name	Rev
C	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 63 of 94

Title :	BLANK
ASUSTeK COMPUTER INC. NB1	Engineer: Miller / Daniel
Size: A	Project Name: F70SL
Rev: 1.0	
Date: Monday, November 03, 2008	Sheet 64 of 94

<Variant Name>

Title :NC

ASUSTeK COMPUTER INC. NB1

Engineer: Miller / Daniel

Size	Project Name	Rev
Custom	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 65 of 94

<Variant Name>

Title : NC

ASUSTeK COMPUTER INC. NB1

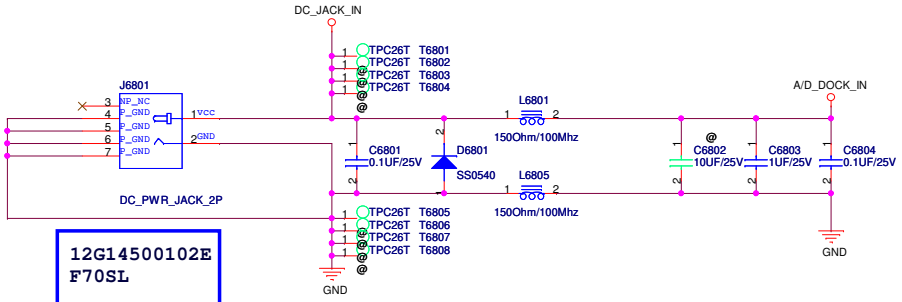
Engineer: Miller / Daniel

Size	Project Name	Rev
Custom	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 66 of 94

Title :	BLANK
ASUSTeK COMPUTER INC. NB1	Engineer: Miller / Daniel
Size: A	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 67 of 94

DC IN



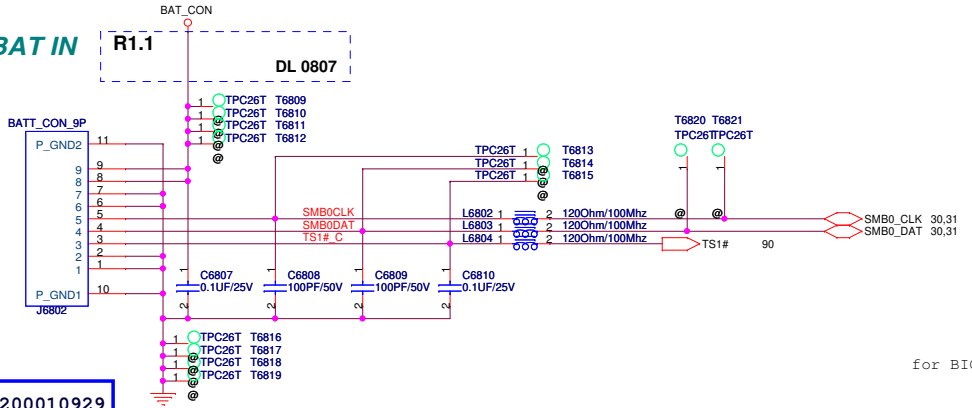
12G14500102E
F70SL

ML0617

BAT IN

R1.1

DL 0807

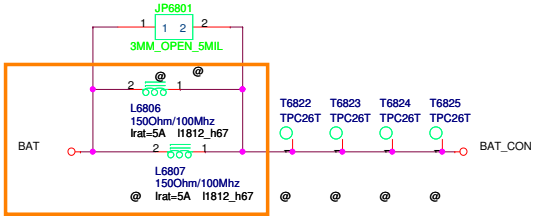


12G200010929
F70SL

DL0630

Add jumper & EMI bead

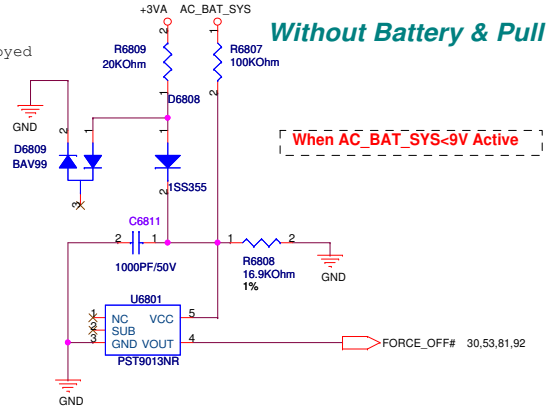
DL0625

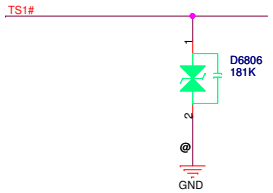


for BIOS is destroyed

1/23

Without Battery & Pull out Adapter





<Variant Name>

ASUSTeK COMPUTER INC. NB1

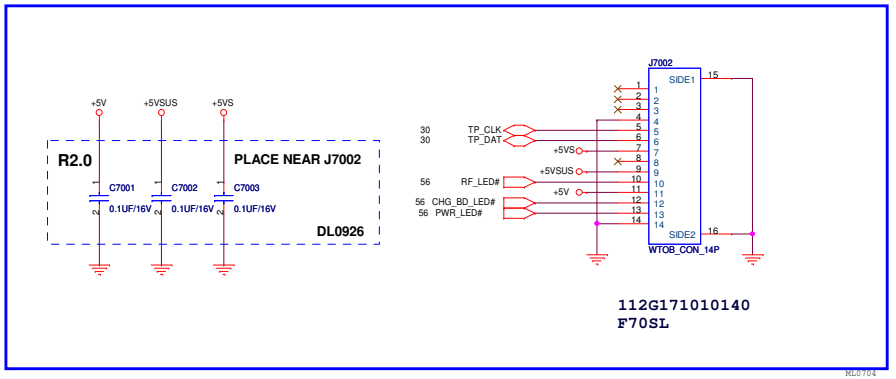
Title : DC & BAT IN

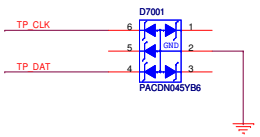
Engineer: Miller / Daniel

Size	Project Name	Rev
Custom	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 68 of 94

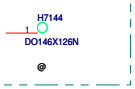
Title :	BLANK
ASUSTeK COMPUTER INC. NB1	Engineer: Miller / Daniel
Size: A	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 69 of 94



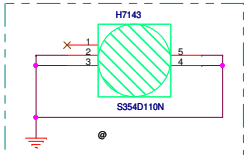


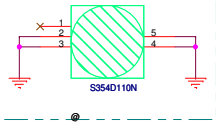
ASUSTeK COMPUTER INC. NB1	Title : TP CON	
	Engineer: Miller / Daniel	
Size: C	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 70 of 94	

Screw Hole A

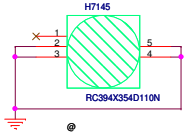


Screw Hole B



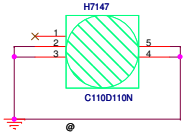


Screw Hole C

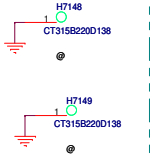


Screw Hole D

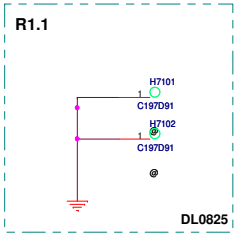
Screw Hole E



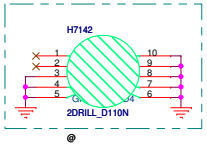
Screw Hole F



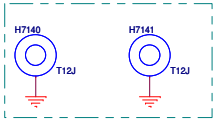
Screw Hole G



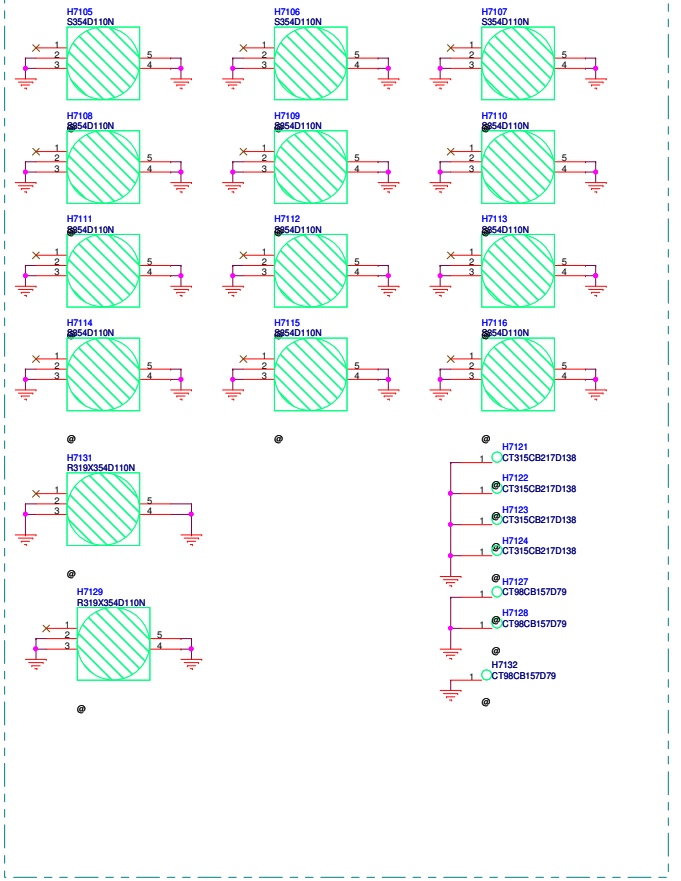
Screw Hole J



NUT 2.5H



F70SL Screw Hole



ASUSTeK COMPUTER INC. NB1	Title : SCREW hole	
	Engineer: Miller / Daniel	
Size: C	Project Name: F70SL	Rev: 1.0
Date: Wednesday, November 19, 2008	Sheet 71 of 94	

Title :	BLANK
ASUSTeK COMPUTER INC. NB1	Engineer: Miller / Daniel
Size: A	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 72 of 94

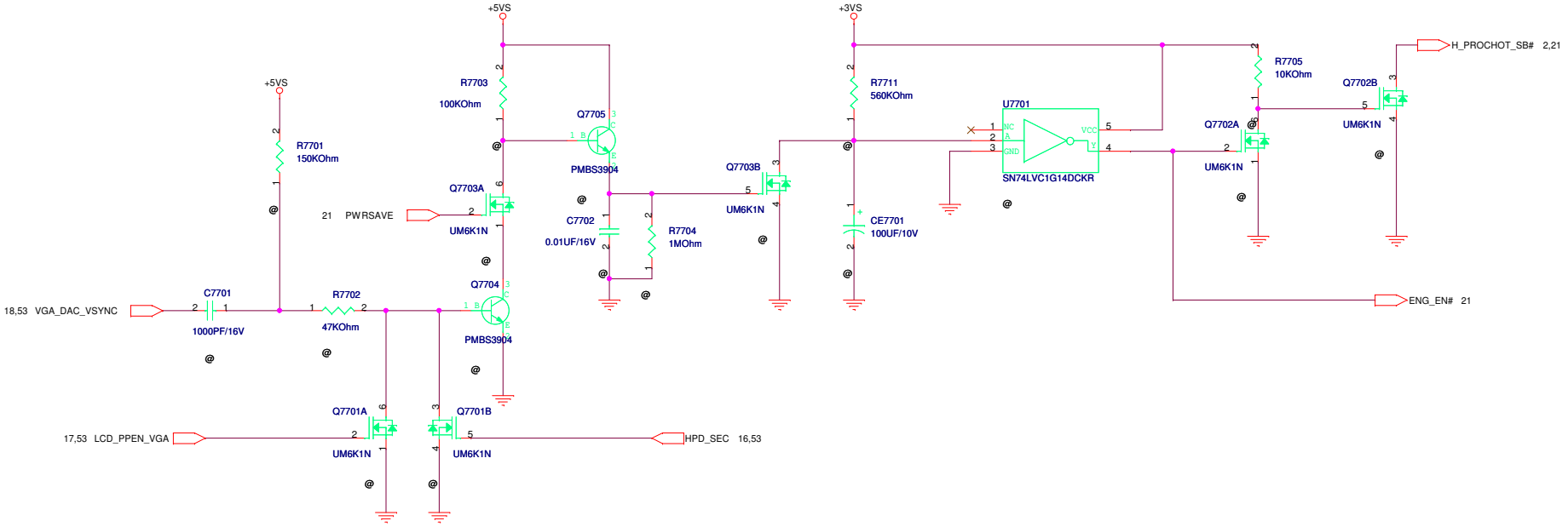
Title :	BLANK
ASUSTeK COMPUTER INC. NB1	Engineer: Miller / Daniel
Size: A	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 73 of 94

1.080926 Add C7001,C7002,C7003,D7001 for EMI on Page 70
2.080926 Add C3238 for EMI on Page 32
3.080926 place D3101,D3103 near J6802 for EMI on Page 31
4.080926 Add C8040 near R8001 for EMI on Page 80
5.080930 Modify Page 32
6.080930 Add wheel_mute pin on Page 56
7.081002 Add R3350,R3351,R3352 for EMI on Page 33

ASUSTeK COMPUTER INC. NB1	Title : BLANK	
	Engineer: Miller / Daniel	
Size: C	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 74 of 94	

Title :	BLANK
ASUSTeK COMPUTER INC. NB1	Engineer: Miller / Daniel
Size: A	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 75 of 94

ASUSTeK COMPUTER INC	Title : Energy Star	
	Engineer: Miller / Daniel	
Size: Custom	Project Name: F70SL	Rev: 2.1
Date: Monday, November 03, 2008	Sheet 76 of 94	



<Variant Name>

Title : Battery Saving

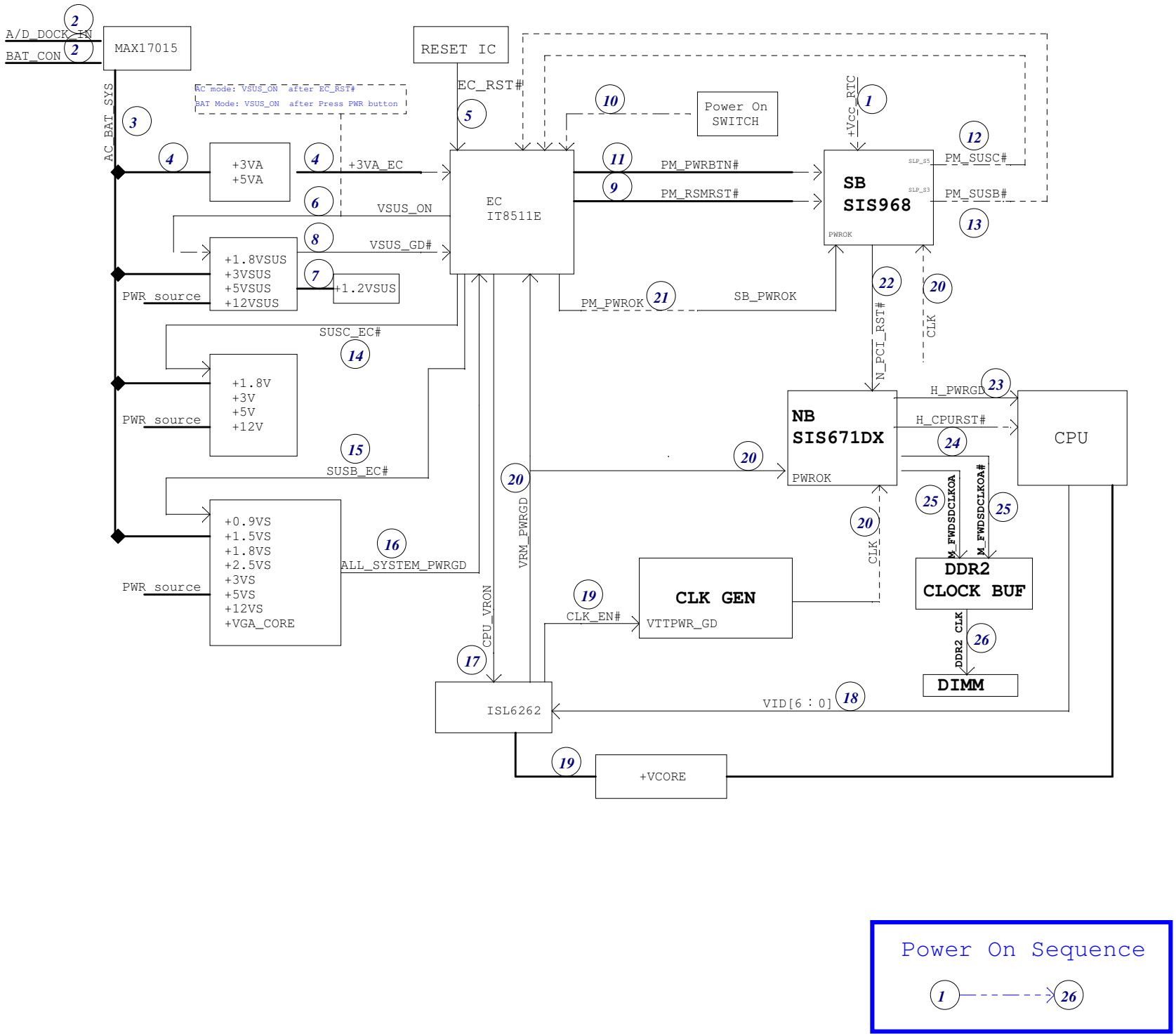
ASUSTeK COMPUTER INC

Engineer: Miller / Daniel

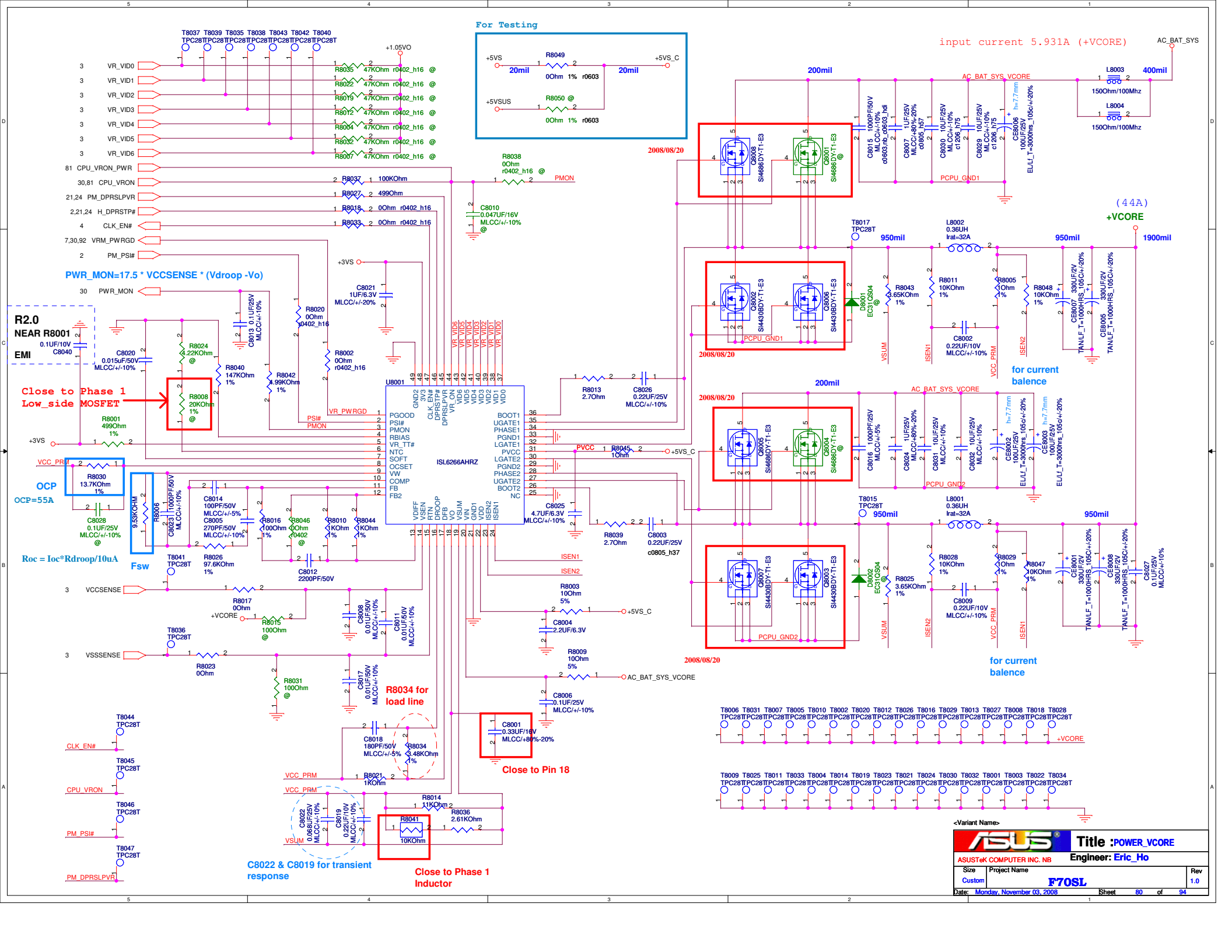
Size	Project Name	Rev
Custom	F70SL	2.1

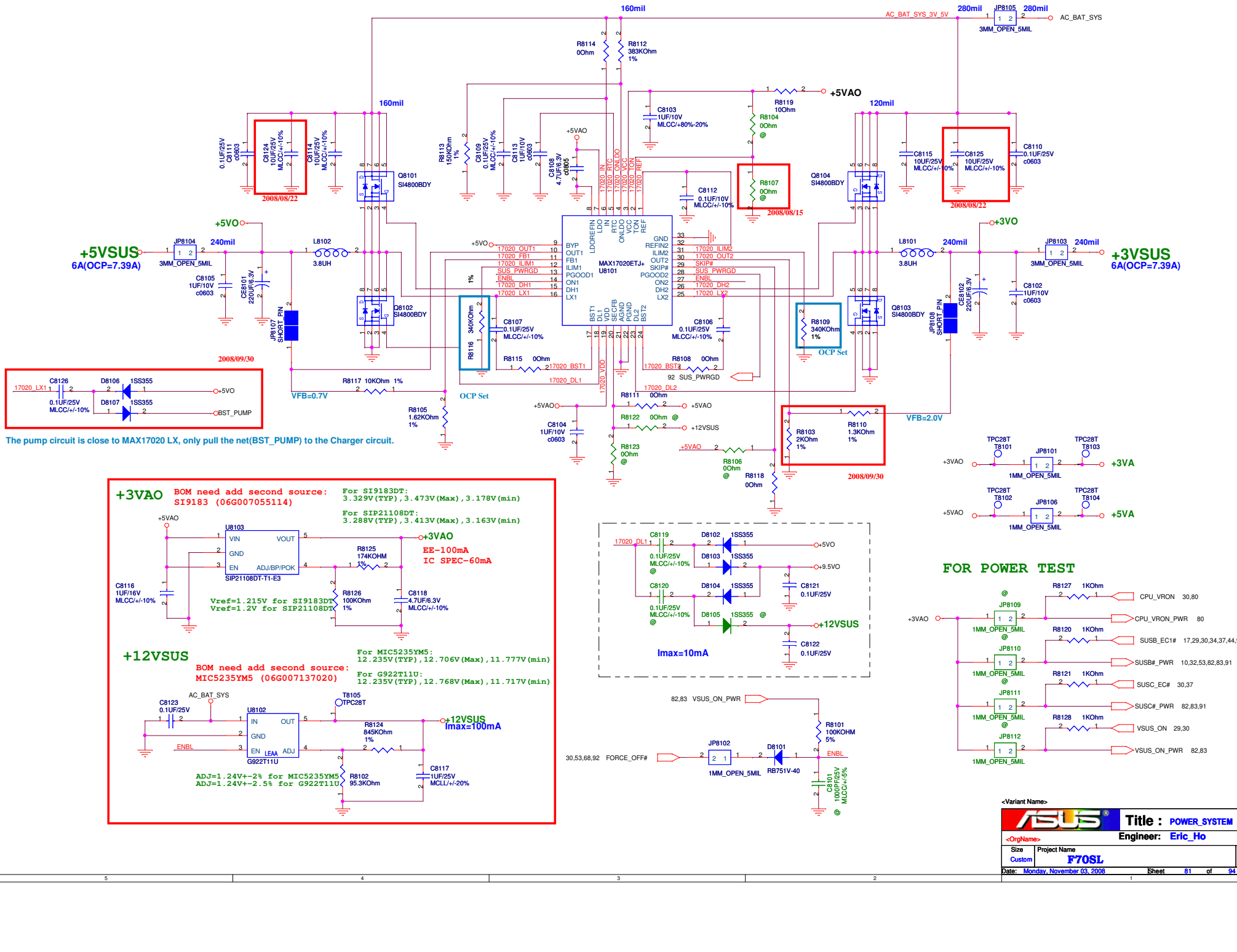
Date: Monday, November 03, 2008 Sheet 77 of 94

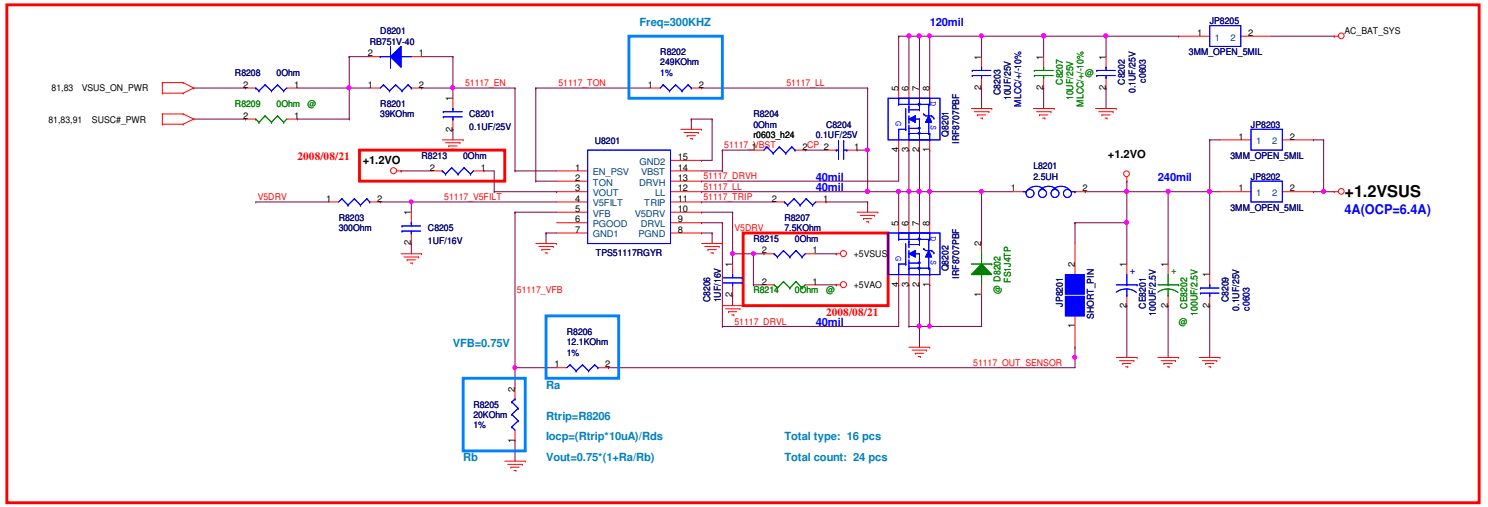
Title :	BLANK
ASUSTeK COMPUTER INC. NB1	Engineer: Miller / Daniel
Size: A	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 78 of 94



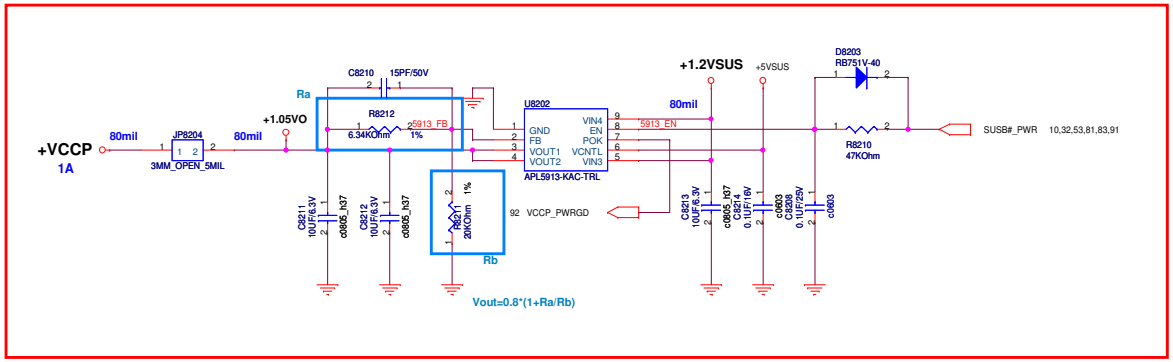
ASUSTeK COMPUTER INC. NB1	Title : Power sequence	
	Engineer: Miller / Daniel	
Size C	Project Name F70SL	Rev 1.0
Date: Monday, November 03, 2008	Sheet 79 of 94	


For Testing
input current 5.931A (+VCORE)
AC_BAT_SYS
+VCORE
(44A)
PWR_MON=17.5 * VCCSENSE * (Vdroop -Vo)
R2.0
NEAR R8001
EMI
Close to Phase 1
Low_side MOSFET
OCP
OCP=55A
Roc = Ioc*Rdroop/10uA
Fsw
R8034 for
load line
Close to Pin 18
Close to Phase 1
Inductor
C8022 & C8019 for transient
response
for current
balence
for current
balence
ISL6266AHRZ
U8001
2008/08/20
Title :POWER_VCORE
ASUSTeK COMPUTER INC. NB
Engineer: Eric_Ho
Project Name
F70SL
Rev
1.0
Monday, November 03, 2008
Sheet 80 of 94


+5VSUS
6A(OCP=7.39A)
+3VSUS
6A(OCP=7.39A)
MAX17020ETJ+
U8101
VFB=0.7V
VFB=2.0V
OCP Set
OCP Set
2008/09/30
2008/08/22
2008/08/15
2008/08/22
2008/09/30
The pump circuit is close to MAX17020 LX, only pull the net(BST_PUMP) to the Charger circuit.
+3VAO
BOM need add second source:
SI9183 (06G007055114)
For SI9183DT:
3.329V(TYP),3.473V(Max),3.178V(min)
For SIP21108DT:
3.288V(TYP),3.413V(Max),3.163V(min)
EE-100mA
IC SPEC-60mA
Vref=1.215V for SI9183DT
Vref=1.2V for SIP21108DT
+12VSUS
BOM need add second source:
MIC5235YM5 (06G007137020)
For MIC5235YM5:
12.235V(TYP),12.706V(Max),11.777V(min)
For G922T11U:
12.235V(TYP),12.768V(Max),11.717V(min)
Imax=100mA
ADJ=1.24V+-2% for MIC5235YM5
ADJ=1.24V+-2.5% for G922T11U
Imax=10mA
FOR POWER TEST
CPU_VRON 30,80
CPU_VRON_PWR 80
SUSB_EC1# 17,29,30,34,37,44,92
SUSB#_PWR 10,32,53,82,83,91
SUSC_EC# 30,37
SUSC#_PWR 82,83,91
VSUS_ON 29,30
VSUS_ON_PWR 82,83
30,53,68,92 FORCE_OFF#
82,83 VSUS_ON_PWR
Title : POWER_SYSTEM
Engineer: Eric_Ho
Project Name F70SL
Date: Monday, November 03, 2008
Sheet 81 of 94

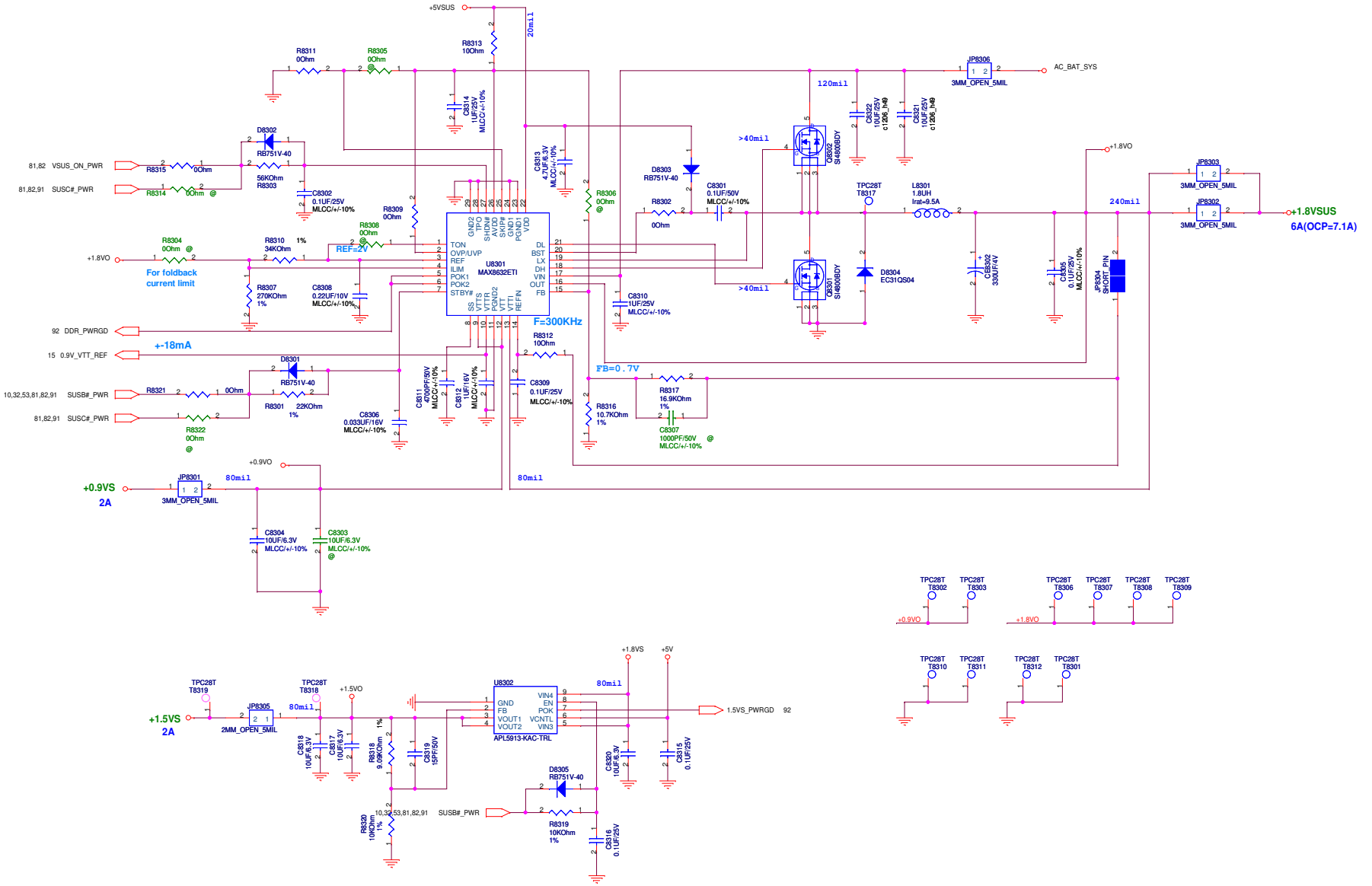


2008/08/15



2008/08/15

ASUS	Title: POWER_I/O_1.2VS & 1.05VS		
<OrgName>	Engineer: Eric_Ho		
Size: C	Project Name: F70SL		Rev: 1.0
Date: Monday, November 03, 2008	Sheet 82 of 94		



ASUS	Title : POWER_I/O_DDR & VTT		
<OrgName>	Engineer: Eric_Ho		
Size: C	Project Name: F70SL		Rev: 1.0
Date: Monday, November 03, 2008	Sheet 83 of 94		

<Variant Name>

Title : N/A

<OrgName>

Engineer: Eric_Ho

Size	Project Name	Rev
Custom	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 84 of 94

<Variant Name>

Title : NA

ASUSTeK COMPUTER INC. NB

Engineer: Eric_Ho

Size	Project Name	Rev
C	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 85 of 94

<Variant Name>

Title : N/A

<OrgName>

Engineer: Eric_Ho

Size	Project Name	Rev
B	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 86 of 94

<Variant Name>

Title : N/A

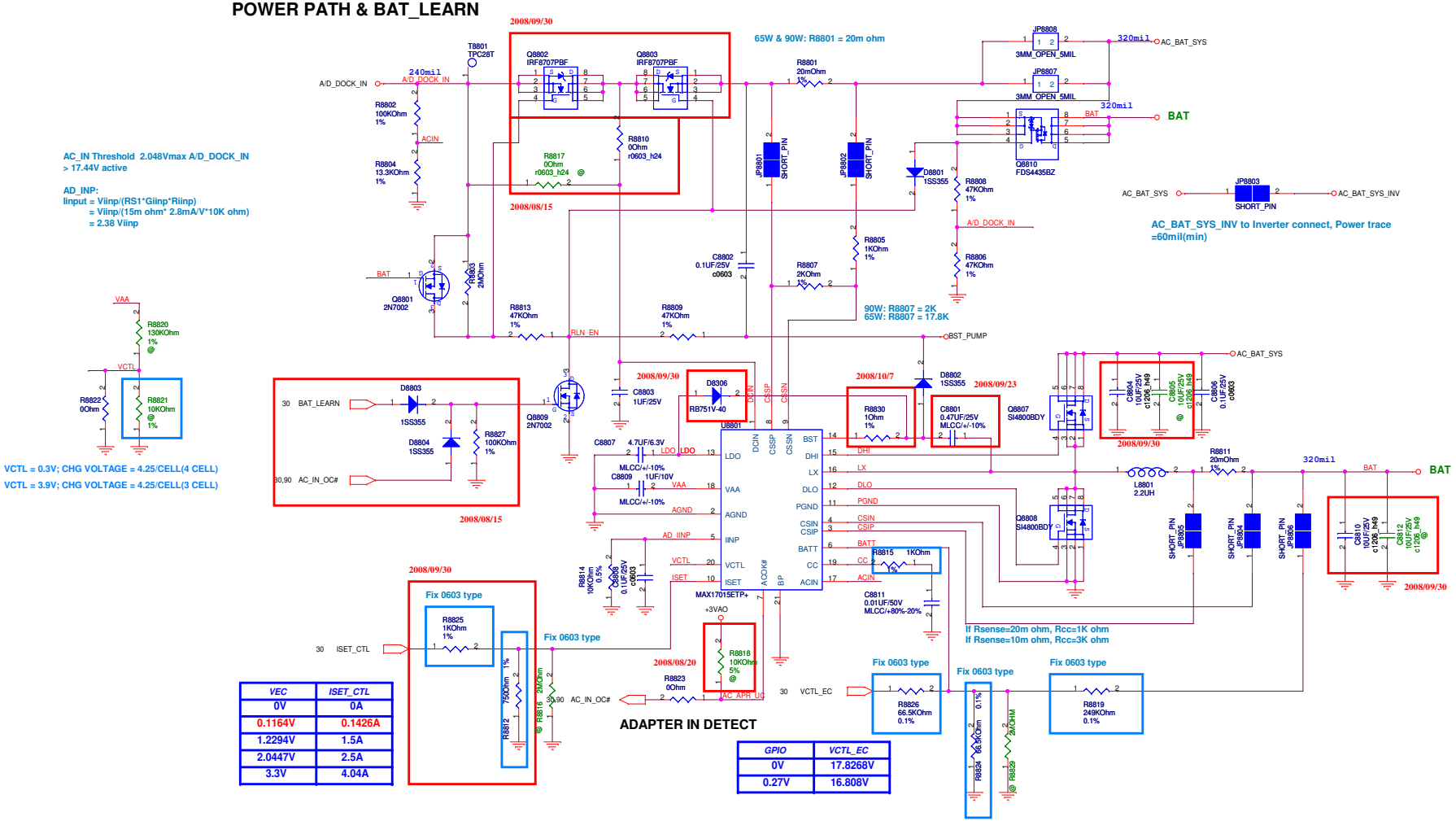
<OrgName>

Engineer: Eric_Ho

Size	Project Name	Rev
Custom	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 87 of 94

POWER PATH & BAT_LEARN



VEC	ISET_CTL
0V	0A
0.1164V	0.1426A
1.2294V	1.5A
2.0447V	2.5A
3.3V	4.04A

ADAPTER IN DETECT

GPIO	VCTL_EC
0V	17.8268V
0.27V	16.808V

<Variant Name>

ASUSTeK COMPUTER INC. NB

Title : POWER_CHARGER

Engineer: Eric_Ho

Size	Project Name	Rev
C	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 88 of 94

<Variant Name>

Title : N/A

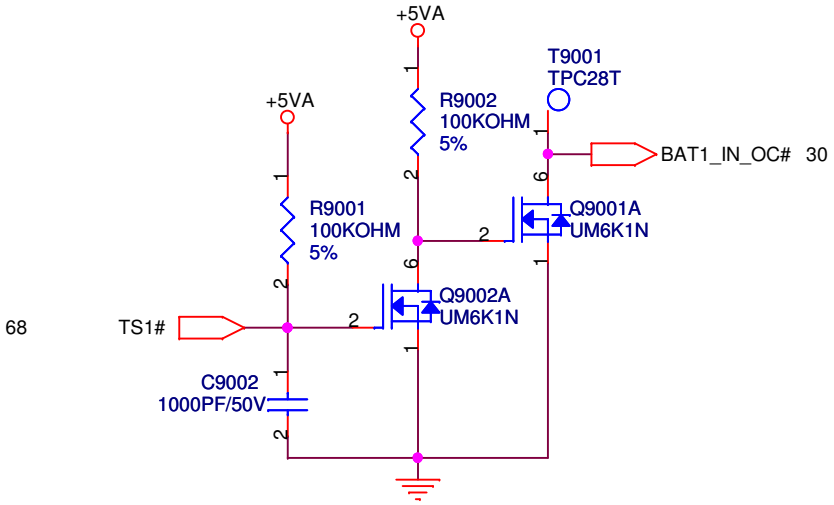
<OrgName>

Engineer: Eric_Ho

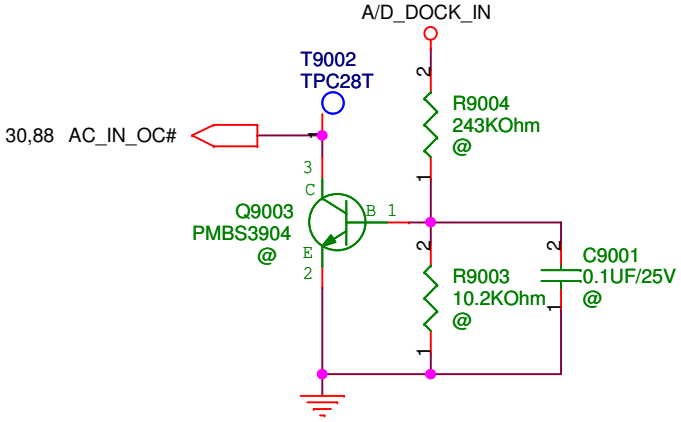
Size	Project Name	Rev
Custom	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 89 of 94

BATTERY IN DETECT



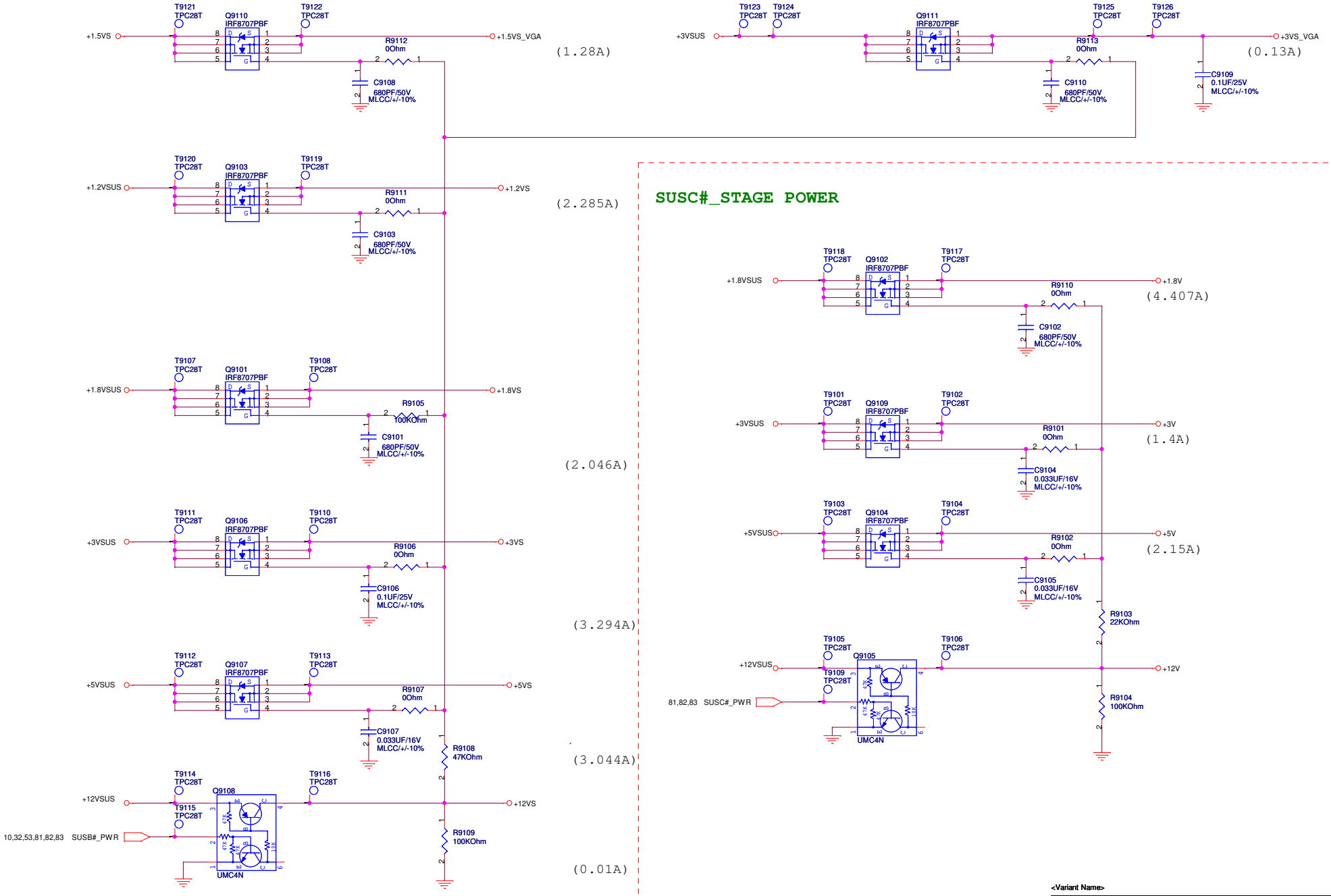
ADAPTER IN DETECT



<Variant Name>

ASUS	Title : POWER_DETECT	
<OrgName>	Engineer: Eric_Ho	
Size: A	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 90 of 94	

SUSB#_STAGE POWER

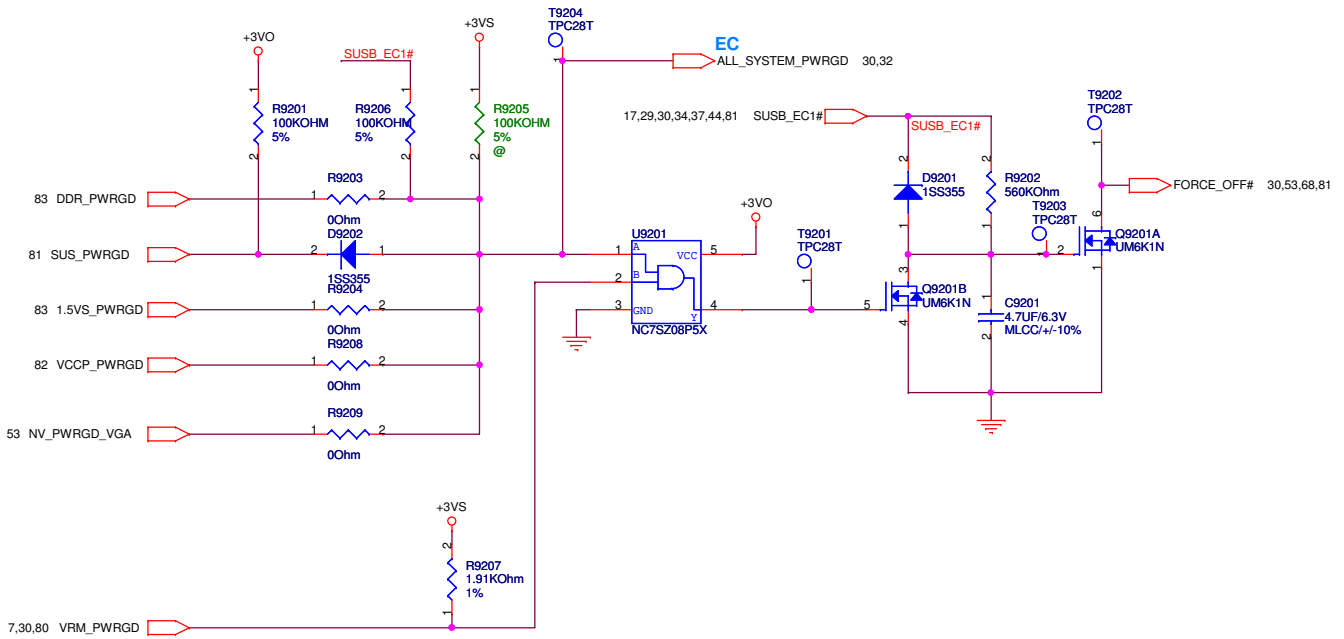


SUSC#_STAGE POWER

<Variant Name>

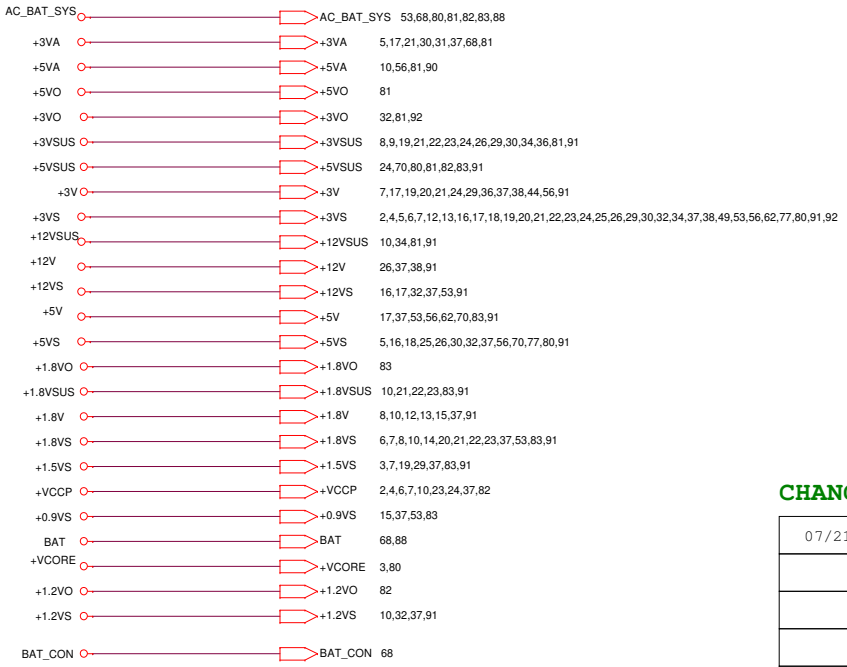
ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer: Eric_Ho	
Size: Custom	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 91 of 94	

POWER GOOD DETECTER



<Variant Name>

<OrgName>	Title : POWER_PROTECT	
	Engineer: Eric_Ho	
Size: B	Project Name: F70SL	Rev: 1.0
Date: Monday, November 03, 2008	Sheet 92 of 94	



CHANGE LIST

07/21 SR	N/A

<Variant Name>

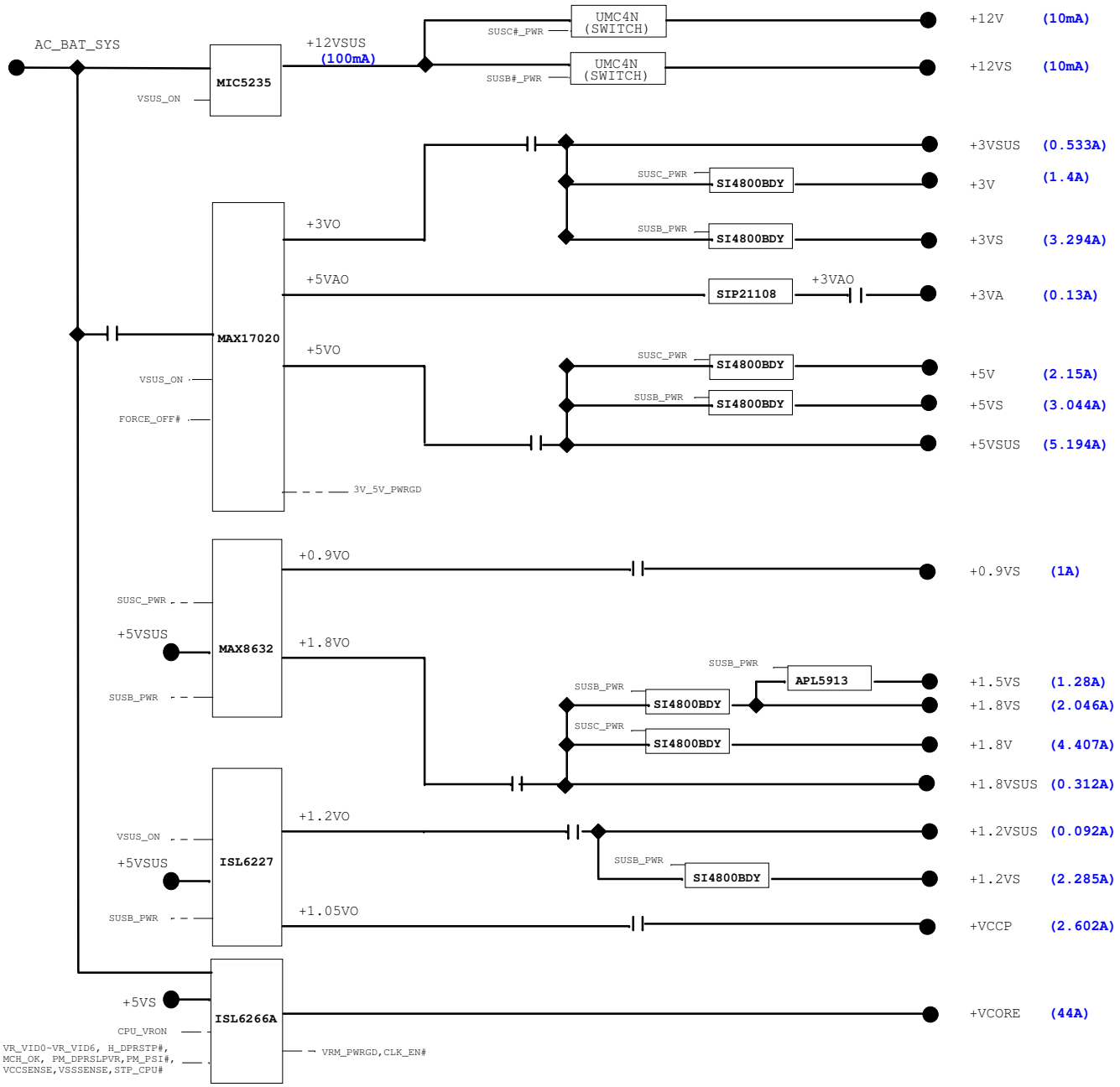
Title :POWER_SIGNAL

<OrgName>

Engineer: Eric_Ho

Size	Project Name	Rev
Custom	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 93 of 94



<Variant Name>

ASUS

Title : POWER_FLOWCHART

<OrgName>

Engineer: Eric_Ho

Size	Project Name	Rev
Custom	F70SL	1.0

Date: Monday, November 03, 2008 Sheet 94 of 94