

## 20V N-Channel Enhancement Mode MOSFET

**VDS= 20V**

**RDS(ON), Vgs@4.5V, Ids@5.0A < 31mΩ**

**RDS(ON), Vgs@2.5V, Ids@4.5A < 37mΩ**

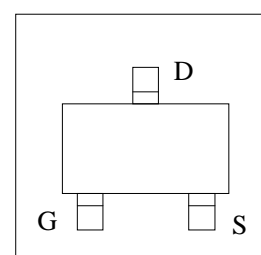
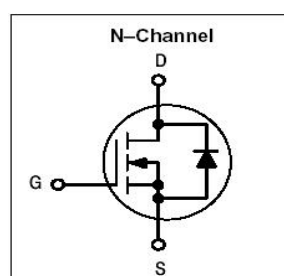
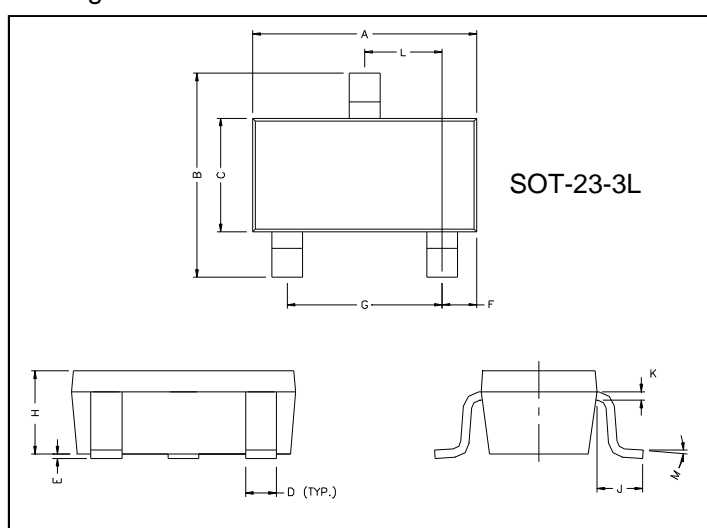
**RDS(ON), Vgs@1.8V, Ids@3.9A < 85mΩ**

### Features

Advanced trench process technology

High Density Cell Design For Ultra Low On-Resistance

### Package Dimensions



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	2.70	3.10	G	1.90	REF.
B	2.65	2.95	H	1.00	1.30
C	1.50	1.70	K	0.10	0.20
D	0.35	0.50	J	0.40	-
E	0	0.10	L	0.85	1.15
F	0.45	0.55	M	0°	10°

### Maximum Ratings and Thermal Characteristics (TA = 25°C unless otherwise noted)

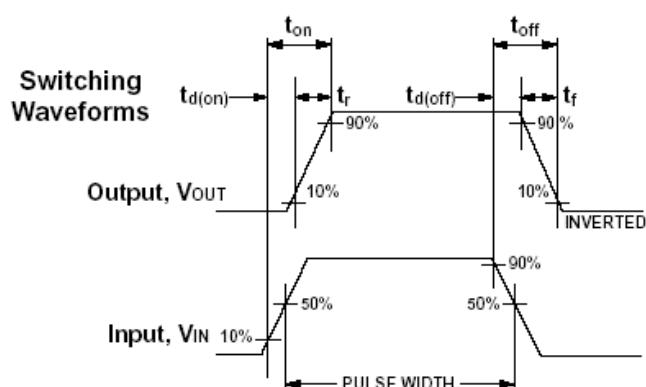
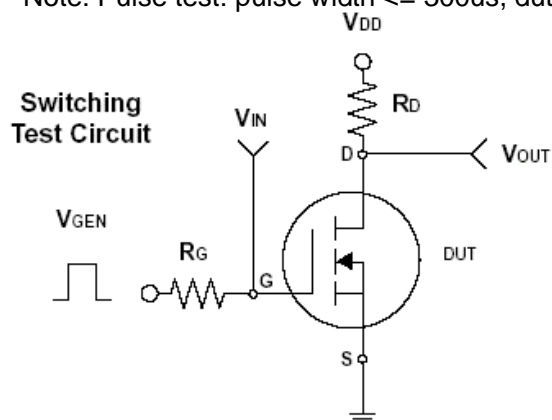
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V <sub>DS</sub>	20	V
Gate-Source Voltage	V <sub>GS</sub>	± 8	
Continuous Drain Current	I <sub>D</sub>	4.9	A
Pulsed Drain Current	I <sub>DM</sub>	15	
Maximum Power Dissipation	P <sub>D</sub>	0.75	W
		0.48	
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to 150	°C
Junction-to-Ambient Thermal Resistance (PCB mounted)	R <sub>θJA</sub>	140	°C/W

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### ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250uA	20			V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 5.0A		21.0	31.0	mΩ
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 2.5V, I <sub>D</sub> = 4.5A		24.0	37.0	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 1.8V, I <sub>D</sub> = 4.0A		50.0	85.0	
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> = 250uA	0.4		1	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20V, V <sub>GS</sub> = 0V			1	uA
Gate Body Leakage	I <sub>GSS</sub>	V <sub>GS</sub> = ± 8V, V <sub>DS</sub> = 0V			± 100	nA
Forward Transconductance	g <sub>fs</sub>	V <sub>DS</sub> = 15V, I <sub>D</sub> = 5.0A		40	—	S
Dynamic						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 10V, I <sub>D</sub> = 5.0A V <sub>GS</sub> = 4.5V		11.2	14	nC
Gate-Source Charge	Q <sub>gs</sub>			1.4		
Gate-Drain Charge	Q <sub>gd</sub>			2.2		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 10V, RL=10Ω I <sub>D</sub> = 1A, V <sub>GEN</sub> = 4.5V R <sub>G</sub> = 6Ω		15	25	ns
Turn-On Rise Time	t <sub>r</sub>			40	60	
Turn-Off Delay Time	t <sub>d(off)</sub>			48	70	
Turn-Off Fall Time	t <sub>f</sub>			31	45	
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 8V, V <sub>GS</sub> = 0V f = 1.0 MHz		500		pF
Output Capacitance	C <sub>oss</sub>			300		
Reverse Transfer Capacitance	C <sub>rss</sub>			140		
Source-Drain Diode						
Max. Diode Forward Current	I <sub>S</sub>				1.7	A
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = 1.8A, V <sub>GS</sub> = 0V			1.2	V

Note: Pulse test: pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$



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Typical Characteristics ( $T_J = 25^\circ\text{C}$  Noted)

