Mux

Design code:

2x1:

```
`timescale 1ns / 1ps
module Mux2to1(
   input a,
   input b,
   input sel,
   output y
   );
   assign y = (a & sel) | (!sel & b);
endmodule
```

4x1:

```
`timescale 1ns / 1ps
module Mux4to1(
   input a, b, c, d, sel1, sel2, sel3,
   output P
   );
   wire P0, P1;
   Mux2to1 uud(.a(a), .b(b), .sel(sel1), .y(P0));
   Mux2to1 uud1(.a(c), .b(d), .sel(sel2), .y(P1));
   Mux2to1 uud2(.a(P0), .b(P1), .sel(sel3), .y(P));
Endmodule
```

8x1:

```
`timescale 1ns / 1ps

module Mux8to1(
   input A, B, C, D, E, F, G, H, sel1, sel2, sel3, sel4, sel5, sel6, sel7,
   output Y
   );
   wire p0, p1;
   Mux4to1 uud1(.a(A), .b(B), .c(C), .d(D), .sel1(sel1), .sel2(sel2), .sel3(sel3), .P(p0));
   Mux4to1 uud2(.a(E), .b(F), .c(G), .d(H), .sel1(sel4), .sel2(sel5), .sel3(sel6), .P(p1));
   Mux2to1 uud3(.a(p0), .b(p1), .sel(sel7), .y(Y));
endmodule
```

Test Bench code:

2x1:

```
`timescale 1ns / 1ps


module Mux2to1(
    input a,
    input b,
    input sel,
    output y
    );
    assign y = (a & sel) | (!sel & b);
endmodule
```

4x1:

```
`timescale 1ns / 1ps


module TestBench4to1;
    reg d3, d2, d1, d0, s2, s1, s0;
    wire y;
    Mux4to1 uud(.a(d0), .b(d1), .c(d2), .d(d3), .sel1(s0), .sel2(s1), .sel3(s2));
    integer i;
    initial begin
```

```
      $display("Mux 4 to 1 tester!");
      d0 = 1'b1; d1 = 1'b0;
      d2 = 1'bx; d3 = 1'b1;
      $display("\tTest case\td3\td2\td1\td0\ts2\ts1\ts0\t|\ty");
      for (i = 0; i < 4; i = i+1)
      begin
         {s2, s1, s0} = i;
         #1 $display("%d\t\t%b\t%b\t%b\t%b\t|\t%b", i, d3, d2, d1, d0, s2, s1, s0, y);
      end
      $finish;
   end
endmodule
```

8to1:

```
`timescale 1ns / 1ps

module TestBench4to1;
   reg d3, d2, d1, d0, s2, s1, s0;
   wire y;
   Mux4to1 uud(.a(d0), .b(d1), .c(d2), .d(d3), .sel1(s0), .sel2(s1), .sel3(s2));
   integer i;
   initial begin
      $display("Mux 4 to 1 tester!");
      d0 = 1'b1; d1 = 1'b0;
      d2 = 1'bx; d3 = 1'b1;
      $display("\tTest case\td3\td2\td1\td0\ts2\ts1\ts0\t|\ty");
      for (i = 0; i < 4; i = i+1)
      begin
         {s2, s1, s0} = i;
         #1 $display("%d\t\t%b\t%b\t%b\t%b\t|\t%b", i, d3, d2, d1, d0, s2, s1, s0, y);
```

```
    end
    $finish;
  end
endmodule
```

Youtube link:

https://youtu.be/rv74RKqrkUY