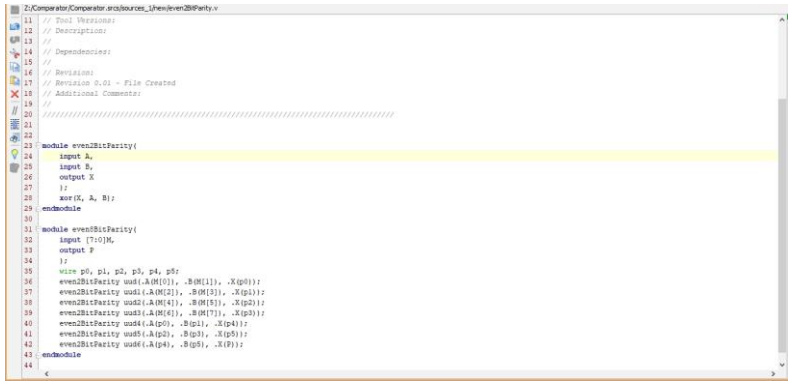
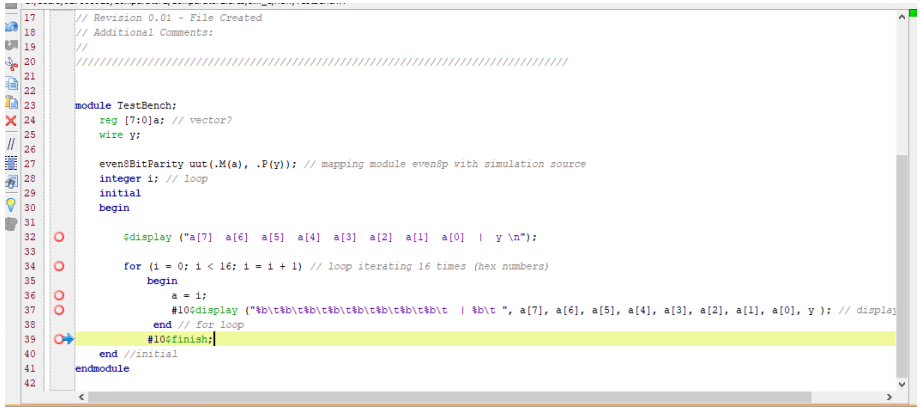
Comparator

Design Code



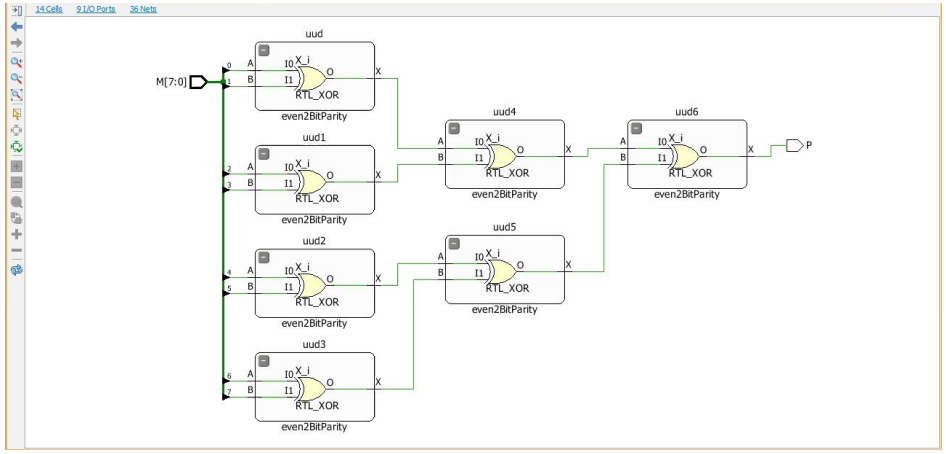
```
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module even2BitParity(
    input A,
    input B,
    output X
    );
    xor(X, A, B);
endmodule

module even8BitParity(
    input [7:0]M,
    output P
    );
    wire p0, p1, p2, p3, p4, p5;
    even2BitParity uut(.A(M[0]), .B(M[1]), .X(p0));
    even2BitParity uut1(.A(M[2]), .B(M[3]), .X(p1));
    even2BitParity uut2(.A(M[4]), .B(M[5]), .X(p2));
    even2BitParity uut3(.A(M[6]), .B(M[7]), .X(p3));
    even2BitParity uut4(.A(p0), .B(p1), .X(p4));
    even2BitParity uut5(.A(p2), .B(p3), .X(p5));
    even2BitParity uut6(.A(p4), .B(p5), .X(P));
endmodule

```

Test Bench

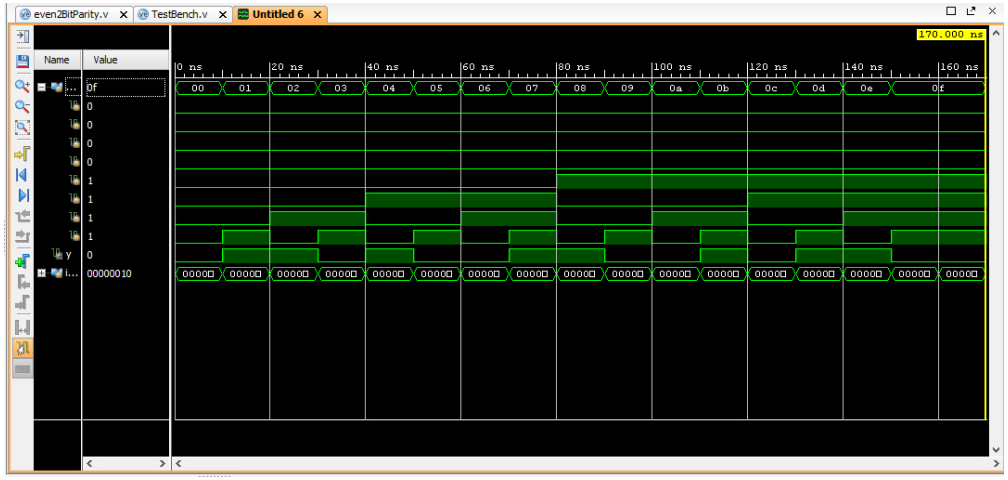


```
    // Revision 0.01 - File Created
    // Additional Comments:
    //
    //////////////////////////////////////////////////////////////////////////////////


    module TestBench;
        reg [7:0]a; // vector?
        wire y;

        even8BitParity uut(.M(a), .P(y)); // mapping module even8p with simulation source
        integer i; // loop
        initial
        begin

            $display ("a[7]  a[6]  a[5]  a[4]  a[3]  a[2]  a[1]  a[0]  |  y \n");

            for (i = 0; i < 16; i = i + 1) // loop iterating 16 times (hex numbers)
                begin
                    a = i;
                    #10$display ("%b\t%b\t%b\t%b\t%b\t%b\t%b\t%b\t  | %b\t ", a[7], a[6], a[5], a[4], a[3], a[2], a[1], a[0], y ); // displa
                end // for loop
                #10$finish;
        end //initial
    endmodule

```

RTL Schematic



Timing Diagram



Youtube link:

https://www.youtube.com/watch?v=js_w9cWSjX8