Name: Matthew Zaldana

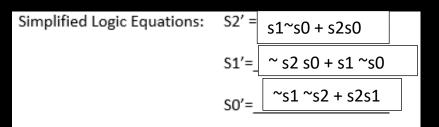
CECS 225 – DD&CA Fall 2020 Assignment #05 Sequential Logic

Due: 29 OCT 2020 (8am)

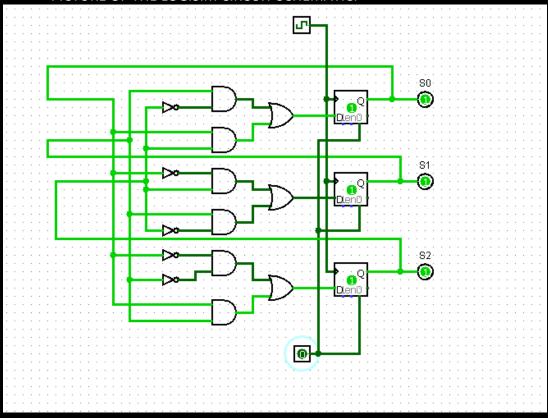
Please download the software Logisim from http://www.cburch.com/logisim/download.html and install in your computer. Then open Logisim. Read the tutorials in the HELP tab if needed.

1. Design and implement a 3-bit sequential logic circuit using D flipflops that will perform a GRAY code count, i.e. a count of 0,1,3,2,4,5,7,6,0,1,3,2 ... Employ an asynchronous RESET to force the counter to 0 when asserted. Set the simulation clock of the counter at 1 Hz and check its operation. Include a picture (not the .circ Logisim code) of the Logisim implementation of your counter in the pdf of this assignment.

| 3-bit Gray Code Counter | | | | | | | | | | | | |
|-------------------------|-----------|-----------|----|--------|-----|-----|--|--|--|--|--|--|
| Logic Table | | | | | | | | | | | | |
| | | Input | t | Output | | | | | | | | |
| # | S2 | S1 | S0 | S2' | S1' | SO' | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | | | | | | |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 | | | | | | |
| 2 | 0 | 1 | 1 | 0 | 1 | 0 | | | | | | |
| 3 | 0 | 1 | 0 | 1 | 1 | 0 | | | | | | |
| 4 | 1 | 1 | 0 | 1 | 1 | 1 | | | | | | |
| 5 | 1 | 1 | 1 | 1 | 0 | 1 | | | | | | |
| 6 | 1 | 0 | 1 | 1 | 0 | 0 | | | | | | |
| 7 | 1 | 0 | 0 | 0 | 0 | 0 | | | | | | |



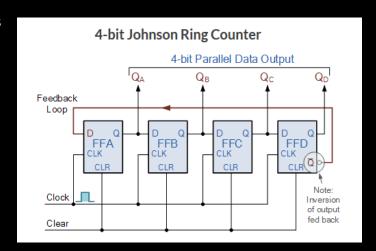
PICTURE OF THE LOGISIM CIRCUIT SCHEMATIC:

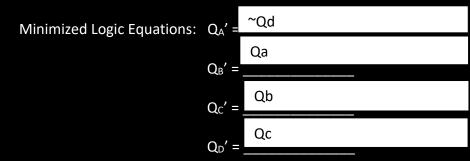


2. Using Logisim, build this counter and determine its 4-bit output and complete the logic table below. Submit a picture of your Logisim logic circuit. The *Clear* input is asserted to reset the counter. The clock frequency for the FFs should be 1 Hz. Find the cycle time of the count before it repeats.

Logic Table for Johnson Counter Cycle time of the count = 8

| eyele time of the country | | | | | | | | | | | | |
|---------------------------|---------------|----------------|---------|-------|---------------------------|--------|------------------|--------|--|--|--|--|
| | Current State | | | | Next State | | | | | | | |
| M | Q_{A} | Q_{B} | Q_{C} | Q_D | $Q_{\text{A}}{}^{\prime}$ | Q_B' | Q_{C}^{\prime} | Q_D' | | | | |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | | | | |
| 8 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | | | | |
| 12 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | | | | |
| 14 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | | | | |
| 15 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | | | | |
| 7 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | | | | |
| 3 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | | | | |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | | | | |
| 2 | 0 | 0 | 1 | 0 | Х | Х | Х | Χ | | | | |
| 4 | 0 | 1 | 0 | 0 | Χ | X | X | Χ | | | | |
| 5 | 0 | 1 | 0 | 1 | Χ | X | X | Χ | | | | |
| 6 | 0 | 1 | 1 | 0 | Х | Х | X | Χ | | | | |
| 9 | 1 | 0 | 0 | 1 | Х | Х | X | Χ | | | | |
| 10 | 1 | 0 | 1 | 0 | Х | Х | X | Χ | | | | |
| 11 | 1 | 0 | 1 | 1 | Х | Х | Х | Χ | | | | |
| 13 | 1 | 1 | 0 | 1 | Χ | X | X | Χ | | | | |





PICTURE OF THE LOGISIM CIRCUIT SCHEMATIC:

