Name: Matthew Zaldana

CECS 225 – DD&CA Fall 2020
LAB #04 Combinational Logic   Due: 24 SEP 2020 (8am)

Please download the software Logisim from http://www.cburch.com/logisim/download.html and install in your computer. Then open Logisim. Read the tutorials in the HELP tab if needed.

1. Design and implement in Logisim a full-adder circuit by completing and implementing the logic using only NAND gates. Using Logisim, input all combinations and verify the full adder truth table.

Inputs				Outputs	
A	B	Ci		S	Co
0	0	0		0	0
0	0	1		1	0
0	1	0		1	0
0	1	1		0	1
1	0	0		1	0
1	0	1		0	1
1	1	0		0	1
1	1	1		1	1
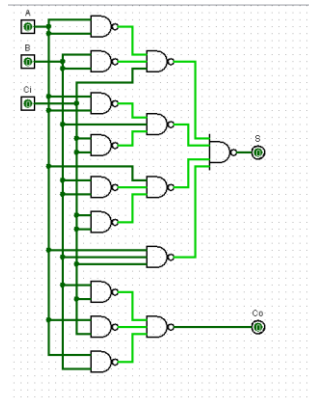
2. Using the full adder circuit, use Logisim to fashion an 8-bit 2's complement ripple adder with a carry flag CF, a zero flag ZF, an overflow flag OF, and a sign flag SF. The zero flag ZF=1 if all bits of result are 0. The overflow flag OF is the XOR of the carry into the msb with the carry out of the msb. The sign flag SF is just the msb of the result. The carry flag CF is the carry out of the msb.
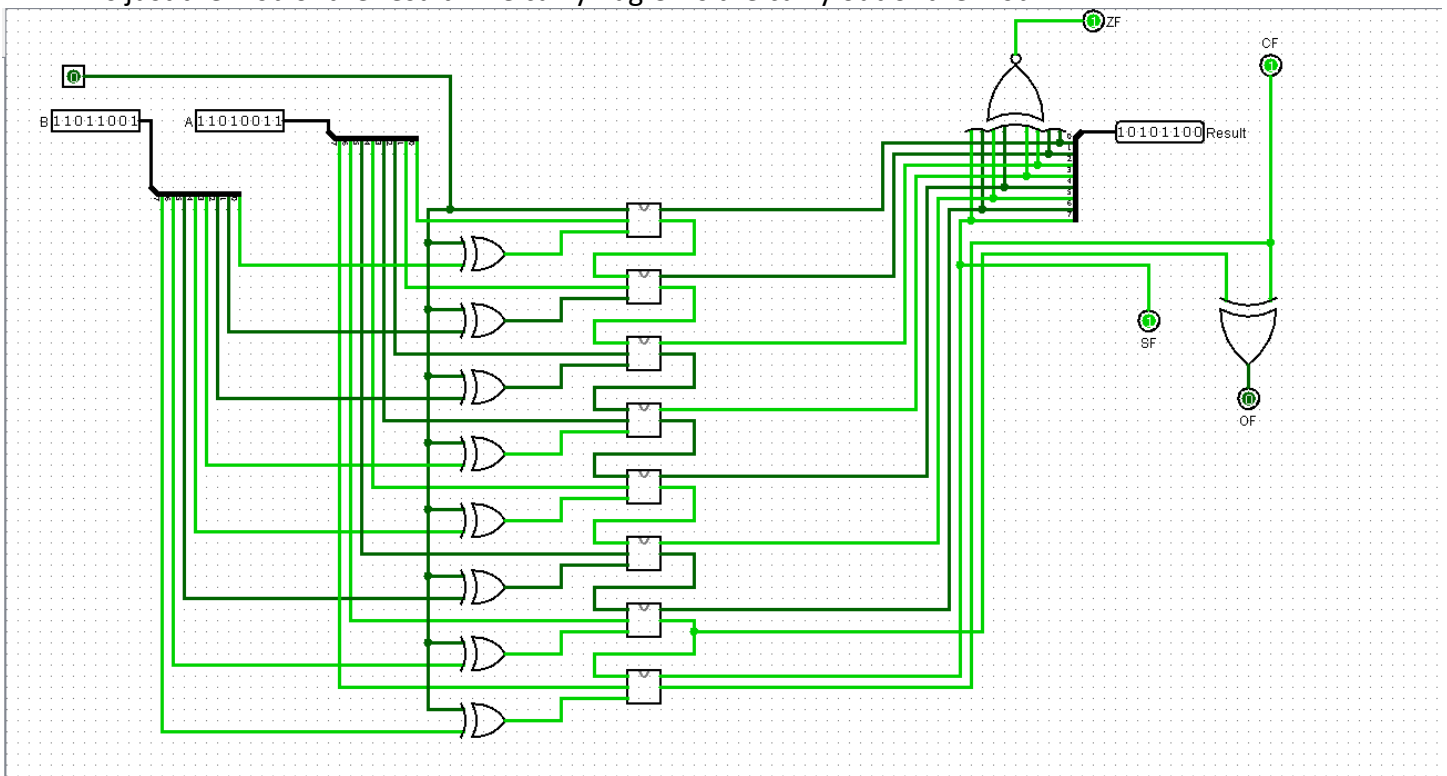
3. Fill out this table using Logisim to find the results. The first row is given as an example of the result and the flag values. An underscore is used to separate groups of four binary bits to make the value more readable. Attach a copy of the Logisim circuit of (2) to this submission. (50 pts)

#	A	B	Operation	8-bit Result	CF	ZF	OF	SF	Range: -128 to +127
0	50	78	A+B	1000_0000 (128)	0	0	1	1	
1	12	55	A+B	0100_0011 (67)	0	0	0	0	
2	-45	39	A-B	1010_1100 (-84)	1	0	0	1	
3	-68	29	A+B	1101_1001 (-39)	0	0	0	1	
4	21	-59	A-B	1101_1010 (218)	0	0	0	1	
5	-80	-79	A+B	0110_0001 (97)	1	0	1	0	
6	127	127	A-B	0000_0000 (0)	1	1	0	0	
7	-01	03	A+B	0000_0010 (2)	1	1	0	0	
8	50	100	A-B	1100_1110 (-50)	0	0	0	1	
9	-95	-90	A+B	0100_0111 (71)	1	0	1	0	
10	0	0	A-B	0000_0000 (0)	0	1	0	0	

Extra Credit:
4. Logisim has the capability of reducing the logic found in a truth table and implementing the logic at the gate logic level. Read the Combinational Analysis section of the User's Guide that is found by clicking the HELP tab. Using this combinational tool, find the SOP logic equations and resulting AND-OR-INVERT circuit for a 7-segment decoder. Please read the text, pp. 79-82 for more information on the decoder circuit. Submit your copy of the Logisim circuit with this submission for extra credit. (10pts)