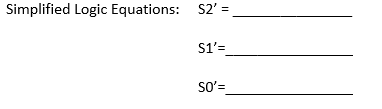
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CECS 225 – DD&CA Fall 2020

Assignment #05 Sequential Logic Due: 29 OCT 2020 (8am)

Please download the software Logisim from <http://www.cburch.com/logisim/download.html> and install in your computer. Then open Logisim. Read the tutorials in the HELP tab if needed.

1. Design and implement a 3-bit sequential logic circuit using D flipflops that will perform a GRAY code count, i.e. a count of 0,1,3,2,4,5,7,6,0,1,3,2 … Employ an asynchronous RESET to force the counter to 0 when asserted. Set the simulation clock of the counter at 1 Hz and check its operation. Include a *picture* (not the ***.circ*** Logisim code) of the Logisim implementation of your counter in the pdf of this assignment.



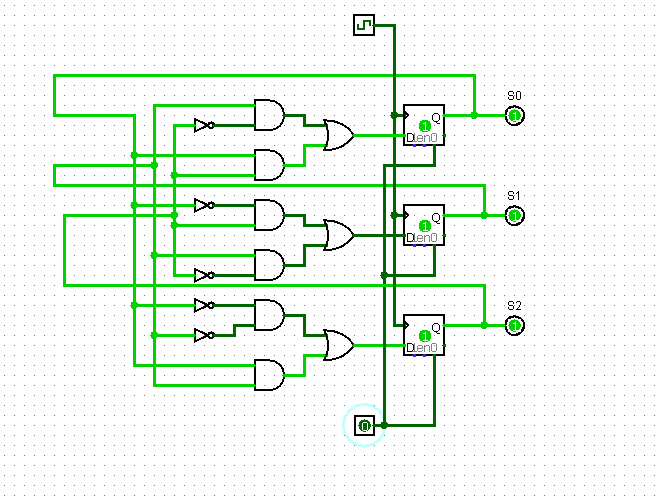
~s1 ~s2 + s2s1 s2

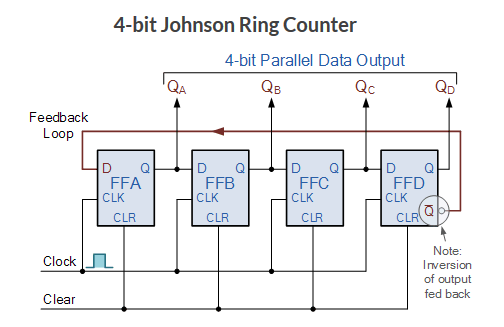
~ s2 s0 + s1 ~s0

s1~s0 + s2s0

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3-bit Gray Code Counter  Logic Table | | | | | | |
|  | Input | | | Output | | |
| # | S2 | S1 | S0 | S2’ | S1’ | S0’ |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| 2 | 0 | 1 | 1 | 0 | 1 | 0 |
| 3 | 0 | 1 | 0 | 1 | 1 | 0 |
| 4 | 1 | 1 | 0 | 1 | 1 | 1 |
| 5 | 1 | 1 | 1 | 1 | 0 | 1 |
| 6 | 1 | 0 | 1 | 1 | 0 | 0 |
| 7 | 1 | 0 | 0 | 0 | 0 | 0 |

PICTURE OF THE LOGISIM CIRCUIT SCHEMATIC:



1. Using Logisim, build this counter and determine its 4-bit output and complete the logic table below. Submit a picture of your Logisim logic circuit. The *Clear* input is asserted to reset the counter. The clock frequency for the FFs should be 1 Hz. Find the cycle time of the count before it repeats.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Logic Table for Johnson Counter  Cycle time of the count = 8 | | | | | | | | |
|  | Current State | | | | Next State | | | |
| M | QA | QB | QC | QD | QA’ | QB’ | QC’ | QD’ |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 8 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| 12 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 14 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 |
| 15 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 7 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 3 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 2 | 0 | 0 | 1 | 0 | x | x | x | x |
| 4 | 0 | 1 | 0 | 0 | x | x | x | x |
| 5 | 0 | 1 | 0 | 1 | x | x | x | x |
| 6 | 0 | 1 | 1 | 0 | x | x | x | x |
| 9 | 1 | 0 | 0 | 1 | x | x | x | x |
| 10 | 1 | 0 | 1 | 0 | x | x | x | x |
| 11 | 1 | 0 | 1 | 1 | x | x | x | x |
| 13 | 1 | 1 | 0 | 1 | x | x | x | x |

~Qd

Minimized Logic Equations: QA’ = \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Qa

QB’ = \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Qb

QC’ = \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Qc

QD’ = \_\_\_\_\_\_\_\_\_\_\_\_\_\_

PICTURE OF THE LOGISIM CIRCUIT SCHEMATIC:

