

Lab 3: Designing Arithmetic and Logic Unit (ALU)

Objective

The objective of this lab is to design an Arithmetic and Logic Unit (ALU) using VHDL. In particular, in this lab the ALU should be defined using the behavioral model. The ALU component is illustrated in Figure 1, and the specification for the instructions to implement are included in Table 1.

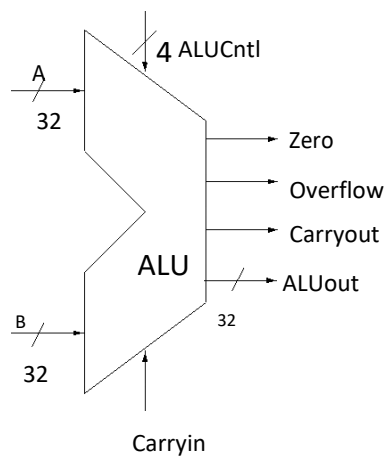


Figure 1: ALU Unit to be developed in this Lab project

Table 1: ALU control Lines and corresponding ALU Operations

ALUCntl	Function
0000	And
0001	Or
0011	Xor
0010	Add
0110	Subtract
1100	Nor

Lab Design

Write a VHDL code to design the ALU component which performs the operations given in Table 1 for the given ALU control signals and two 32-bit inputs **A** and **B**. The result of the operation appears on 32-bit output port **ALUout**. The ALU also computes three flag bits **Zero**, **Carryout**, and **Overflow**.

Testing the Design

- Calculate the ALUout, Zero, Overflow, and Carryout values for the given inputs in Table 2.
- Write a test-bench to test your design for the given inputs of A, B, Carryin, and ALUCntl in Table 2 and compare the results with your calculated values.

Lab Report

Your report should include the following sections:

- Lab objective and your approach in designing the ALU unit
- Calculations of Table 2
- Conclusion

Table 2: Test Vectors for testing the design

#	A_{hex}	B_{hex}	Carryin	ALUCntl	ALUout _{hex}	Zero	Overflow	Carryout
1	FFFFFFFF	00000000	-	0000				
2	98989898	89898989	-	0001				
3	01010101	10101010	-	0011				
4	00000001	FFFFFFFF	0	0010				
5	6389754F	AD5624E6	0	0010				
6	00000001	FFFFFFFF	1	0010				
7	6389754F	AD5624E6	1	0010				
8	FFFFFFFF	FFFFFFFF	1	0010				
9	00000000	00000001	-	0110				
10	F9684783	F998D562	-	0110				
11	9ABCDEDF	9ABCDEFD	-	1100				
12	89BCDE34	C53BD687	1	0010				

Lab Deliverables

Once completed, submit a **ZIPPED** file with the following syntax **Lab3_ALU_Group #Number.zip** through BeachBoard. The submitted file should contain the following components:

- The full project folder.
- alu.vhd (behavioral VHDL model of ALU-unit).
- Your testbench to simulate for the given values in Table 2.
- Your simulation waveform.
- Your lab report including your approach in developing the ALU and the completed Table 2.

In addition, the lab results should be demonstrated in the class. The submission due date is on [August 3rd \(08/03/2021\), 11:59 PM.](#)