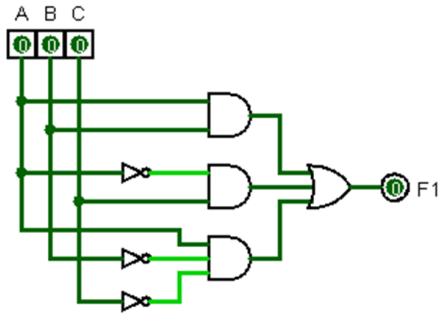
Designing a 4-bit binary Adder-Subtractor using Xilinx Vivado IP Integrator

Part I. (Pre-Lab)

In this part, students will work on developing a digital circuit (Circuit 1) shown below using *behavioral VHDL*. This circuit is also described in detail in course's Intro to VHDL Lecture. For the following design, students should develop a separate behavioral VHDL program and develop a simple testbench to verify the functionality of design.



$$F_1(A,B,C) = A.B + A'.C + A.B'.C'$$

Part II. 4-bit Adder/Subtractor

In this part, based on the knowledge learned from Lab 1 and Intro to VHDL Lecture, you will be using VHDL programming and Xilinx Vivado IP Integrator tool to design a simple 4-bit adder/subtractor.

As we discussed in previous Lab, first, you need to develop the required 1-bit logical components using VHDL, and then use them to construct the larger design (4-bit adder-subtractor) using Vivado IP Integrator. Lastly, you need to develop a testbench to verify your design using the simulation results and generated waveforms.

Lab Deliverables

Submit a zipped file with the following syntax Lab2 Group #Number.zip. The zipped file should include the following files:

- The pre-lab (part I) folder consisting of project folder and files for the tested Circuit (folder containing all the files of your design including Xilinx generated files).
- The full Lab 2-part II project folder for the 4-bit adder-subtractor (folder containing all the files of your design including Xilinx generated files).
- The lab results need to be presented in the lab during the demo session.
- A lab report describing your steps in developing your design. Also, include the snapshot of your design and captured waveform.
- Students need to explain the performed steps in a complete lab report and submit the project folders.
- One submission per group is enough. The lab report should include the group members names.
- The submission due date and demo in the lab is **July 21st (07/21/2021) at 11:59 PM.**