主频和时钟配置实验

**参考文档**：

* 【正点原子】I.MX6U嵌入式Linux驱动开发指南V1.4.pdf
* Allwinner\_V3s\_User\_Manual\_V1.0.pdf
* **V3S时钟系统**
* 系统时钟来源

32.768KHZ无源晶振

24MHZ无源晶振

* 9路PLL时钟源

|  |  |
| --- | --- |
| Module Name | Base Address |
| CCU | 0x01C20000 |

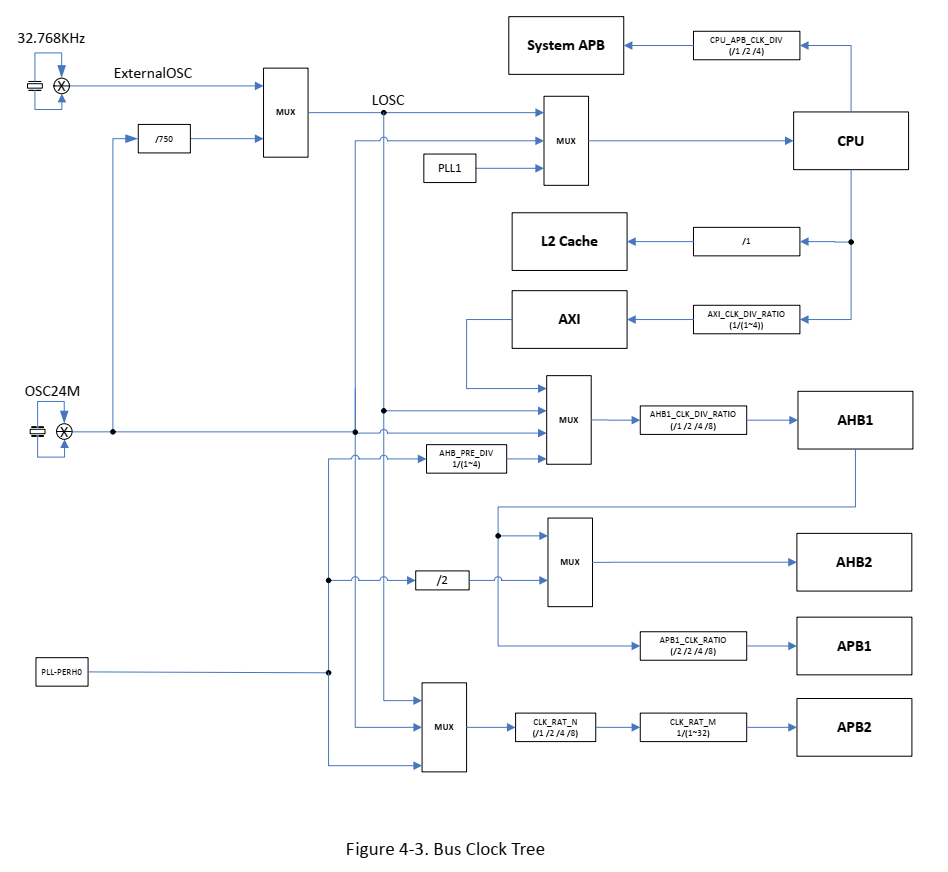
|  |  |  |  |
| --- | --- | --- | --- |
| Register Name | Offset | Description |  |
| **PLL\_CPU\_CTRL\_REG** | 0x0000 | PLL\_CPU Control Register |  |
| PLL\_AUDIO\_CTRL\_REG | 0x0008 | PLL\_AUDIO Control Register |  |
| PLL\_VIDEO\_CTRL\_REG | 0x0010 | PLL\_VIDEO Control Register |  |
| PLL\_VE\_CTRL\_REG | 0x0018 | PLL\_VE Control Register |  |
| PLL\_DDR0\_CTRL\_REG | 0x0020 | PLL\_DDR0 Control Register |  |
| PLL\_PERIPH0\_CTRL\_REG | 0x0028 | PLL\_PERIPH0 Control Register |  |
| PLL\_ISP\_CTRL\_REG | 0x002C | PLL\_ISP Control Register |  |
| PLL\_PERIPH1\_CTRL\_REG | 0x0044 | PLL\_PERIPH1 Control Register |  |
| **PLL\_DDR1\_CTRL\_REG** | 0x004C | PLL\_DDR1 Control Register |  |

说明：

PLL1：支持动态频率修改，只能用于CPU

PLL9：支持动态频率修改

* 时钟树



* UBOOT配置时钟分析

试验：在UBOOT中查9路PLL寄存器的值，结合V3S文档 4.3.5描述，分析当前主频（CPU、外设、总线等等）

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| PLL\_CPU\_CTRL\_REG  Uboot命令：md.l 1c20000 4  返回：0x90001b21 | | | | | | | |
| 位 | 31 | 28 | 24 | 17-16 | 12-8 | 5-4 | 1-0 |
| 对应值 | 1 | 1 | 0 | 00 | 11011 | 10 | 01 |
| 说明 | EN | LOCKED,表示稳定 |  | P | N+1 | K+1 | M+1 |
| 公式：(前值结果>288MHZ时忽略P)  24MHZ \* N \* K / M / P  =24M \* 28 \* 3 / 2 / ?  =1008M / ?  =1008M  PLL1(PLL\_CPU) = 1008MHZ | | | | | | | |

以此类推，得出：

|  |  |  |
| --- | --- | --- |
| PLL\_PERIPH0 | 24M \* N\*K / 2=600MHZ |  |
| PLL\_DDR0 | 24M \* N\*K/M=720M |  |
| PLL\_DDR1 | 24M\*N/M=600M | 禁止状态 |
| CPU\_AXI\_CFG\_REG | SystemAPB  =PLL\_CPU/CPU\_APB\_CLK\_DIV  =1008M/2=504M | 对照时钟树 |
| AXI  =PLL\_CPU/AXI\_CLK\_DIV\_RATIO  =1008M/2=504M |
| AHB1\_APB1\_CFG\_REG | AHB1  =PLL\_PERIHO0/AHB1\_PRE\_DIV/  AHB1\_CLK\_DIV\_RATIO  =600M/3/1=200M | 13-12位选择PLL\_PERIPH0为时钟源 |
| APB1=AHB1/APB1\_CLK\_RATIO  = 200M/2=100M | 参考时钟树，APB1唯一时钟来源是AHB1 |
| AHB2\_CFG\_REG | AHB2=AHB1=200M | 1-0位选择AHB1为时钟源 |
| APB2\_CFG\_REG | OSC24M/CLK\_RAT\_N/CLK\_RAT\_M  =24M / (2^N) / (M+1)=24M | 参考时钟树：25-24位选择OSC24M为时钟源 |