Direct-Coupled Transistor–Transistor Logic: A New High-Performance LSI Gate Family

DAVID E. FULKERSON, MEMBER, IEEE

Abstract—The direct-coupled transistor-transistor logic (DCT^2L) family consists of a multiple-emitter AND gate and a NOR gate similar to direct-coupled transistor logic (DCTL). High speed for low power is obtained by limiting the voltage swing and using a low voltage power supply of about 2 V. Using a conservative, standard Schottky process, the DCT^2L NOR gate has a delay of about 1 ns for 4-mW gate power. A computer-aided analysis shows that this is faster than the basic gates of emitter-function logic (EFL), emitter-coupled logic (ECL), or Schottky transistor-transistor logic (T^2L) with the same process and gate power. This contradicts the common idea that ECL is inherently faster than Schottky-clamped saturating circuits. Several T^2L-compatible DCT^2L circuits have been made. A comparison of actual arithmetic-logic units (ALU) shows that Schottky DCT^2L is smaller and faster than ECL and Schottky T^2L. If we use speed-power-area product as a rough figure of merit, then DCT^2L is about four times better than ECL, and six times better than Schottky T^2L when all three circuit types have comparable speeds and are made on similar processes. The higher speed and density of DCT^2L makes it a better large-scale integration (LSI) concept than the other logic families.

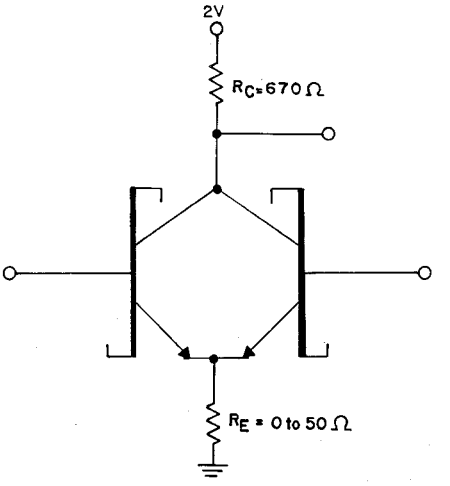

Fig. 1. DCT^2L NOR gate.

I. Introduction

WE HAVE defined and are fabricating a new logic concept that is very useful for high-speed bipolar large-scale integrated (LSI) logic circuits. The logic gates can be fabricated from any standard bipolar process. The use of Schottky diodes significantly increases circuit speed by keeping transistors out of saturation. The gates are smaller in area and they operate faster than conventional high-speed gates such as emitter-coupled logic (ECL), and Schottky transistor-transistor logic (T^2L).

MOS and integrated injection logic [1] (I^2L) are not competitors with direct-coupled transistor-transistor logic (DCT^2L) in the high-speed range because these circuits cannot be conviently operated at gate delays less than 10 ns, while subnanosecond DCT^2L gate delays are easily obtained. On the other hand, DCT^2L is a competitor with slow-speed circuits, since 500 or more DCT^2L gates could be packed in a 150-× 150-mil active area on a T^2L-compatible chip. The main emphasis of this paper, however, will be on applications for gate delays near 1 ns. All performance estimates will be for standard, junction-isolated processes of the type now currently in use by several IC manufacturers. Higher-performance lower-area processes will obviously make DCT^2L faster and smaller.

The new gate family uses a NOR gate similar to the old direct-coupled transistor logic (DCTL) and an AND gate similar to the input transistor used in T^2L. Hence, the logic family is called DCT^2L. The name "direct-coupled T^2L" is also appropriate because every transistor is direct coupled to the next one with no intervening circuits for level shifting or amplifying. Every transistor performs a logic function, which accounts for the simplicity and small size of DCT^2L.

The DCT^2L two-input NOR and AND gates are shown in Figs. 1 and 2 with typical resistor values for a 2-V supply and 4-mW gate power dissipation. It is obviously possible to operate with other supply voltages and other power dissipations. For example, a 20-kΩ collector resistor on either the AND or NOR gate results in a power dissipation of 0.13 mW for a 2-V supply, and 1.1 mW for a 5-V supply. The 0.13-mW NOR gate would have a delay of 5–20 ns, depending on the sophistication of the logic process.

As is well known, DCTL-type NOR gates have a limited fan-out. The fan-out of DCTL can be increased either by adding resistors to the transistor bases (at the cost of speed and area), or by adding a single small-value resistor R_E, as shown in Fig. 1. Even with R_E, however, the maximum fan-out of the NOR gate is only about 5, assuming normal device parameter matching. All possible Boolean logic combinations can be performed by NOR gate alone, but the AND gate of Fig. 2 was added to the NOR gate family for the following reasons.

1) Fan-outs of 10 or more can be easily achieved by restricting large fan-outs to AND gate inputs. As shown in the Appendix, the purpose of the extra feedback emitter in Fig. 2 is to reduce high-state input current to achieve higher fan-out.

2) For logic gates with many inputs, the AND gate is smaller

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The author is with Honeywell Solid State Electronics Center, Plymouth, Minn.

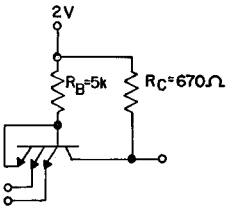

Fig. 2. DCT^2L AND gate.

than the NOR because each input is only one extra emitter rather than another whole Schottky transistor in the same epitaxial region.

3) The AND gate lends logic flexibility, and therefore allows fewer gates to perform a given logic function.

4) Layouts of certain logic configurations are made smaller by routing logic interconnections to AND gate emitters rather than to NOR gate bases.

5) Because it is noninverting, the AND gate is even faster than the NOR for the same power.

The reader will recognize that DCT^2L has some similarities to conventional T^2L, which can also be thought of as AND's and NOR's in a restricted sense. However, a DCT^2L NOR can drive other DCT^2L NOR's without intervening AND buffers, and a DCT^2L AND gate can drive more than one DCT^2L NOR. Conventional T^2L cannot be used in this way. A DCT^2L NOR can also drive several AND's and NOR's simultaneously. Another difference between DCT^2L and conventional T^2L is that the DCT^2L circuit design allows operation at lower supply voltages, and hence a higher speed is possible for a given gate power. Other T^2L-like circuits have been proposed using low-voltage supplies [2], but these circuits are slower than DCT^2L and have the same aforementioned AND-NOR logic restrictions as conventional T^2L.

Another difference between DCT^2L and conventional T^2L is that with DCT^2L the output voltage of both AND and NOR gates goes from approximately (V_{BE}-V_{Sch}) in the low state to V_{BE} in the high state, where V_{Sch} is a Schottky diode forward voltage drop and V_{BE} is a base–emitter forward drop. Thus, the output voltage swing is approximately V_{Sch} (about 0.5 V for aluminum Schottky diodes at room temperature). This low voltage swing partially accounts for the high speed in comparison with other circuits. If a NOR gate drives one or more NOR's (and possibly some AND gates too), then the output high-state clamping mechanism at one V_{BE} is fairly obvious, since R_E (in Fig. 1) has only a small voltage drop across it. If a NOR gate drives only AND gates, then the NOR gate would usually not have a collector pull-up resistor, and the low-state current coming out of the AND's would provide the pull-up current. At input voltages higher than V_{BE}, the AND draws positive input current due to the finite inverse transistor current gain; at input voltages less than V_{BE} the AND gate provides the normal T^2L low-state negative input current. The output of the NOR gate with no collector resistor will automatically clamp at a voltage where the AND gate input current is zero, i.e., at about one V_{BE}. Therefore, the high-state clamping level of a NOR driving only AND's is also one V_{BE}, just as for a NOR driving other NOR's.

A standard DCT^2L chip operating from a single 2-V supply with AND gate input buffers and NOR gate output buffers is compatible with T^2L, but with reduced noise margins. The worst case low-state dc logic "0" input level for an AND-NOR DCT^2L input buffer is 0.6 V for a standard digital process at 100°C junction temperature. The worst case dc logic "0" output level for a DCT^2L NOR output buffer is 0.4 V when sinking 8 mA. Therefore, the worst case noise margin for DCT^2L with a 2-V ± 0.2-V supply is 0.2 V. The noise margin for the high level is about 0.6 V. This type of circuit is also directly compatible with standard ECL when the 2-V supply is defined as the ECL ground, and the DCT^2L ground is defined as −2 V. The −2-V supply is usually already available for resistor terminations in ECL systems.

Both the AND and NOR DCT^2L gates can be driven by standard 5-V diode-transistor logic (DTL) or T^2L gates internal to a chip. Therefore, full T^2L compatibility and noise immunity can be achieved at the inputs simply by including DTL or T^2L gates as input buffers on a DCT^2L chip. T^2L compatibility and noise immunity at the outputs of DCT^2L chips is easily accomplished in several ways, such as using a DCT^2L NOR gate with a supply voltage in the 5-V range, or by driving an on-chip T^2L gate directly by DCT^2L. The internal DCT^2L gates would usually use a lower supply voltage (about 2 V) in order to provide high speed at lower power.

We have designed, made, and tested the following DCT^2L chips.

1) Four different DCT^2L random logic chips of 40, 50, 69, and 100-gate complexity having DCT^2L NOR internal gates and DTL input buffers for T^2L compatibility: these chips use a single 5-V supply. Using a standard process with conservative layout rules (e.g., 0.2 mil × 0.4 mil minimum contact cut), the 100-gate chip contains 89 two and three input DCT^2L NOR's in a 56- × 59-mil area which includes all interconnections, diffused crossunders, and power lines.

2) A test circuit consisting of a string of DCT^2L NOR gates for measuring gate speed: this chip demonstrates internal NOR gate delays of 1.0 ns at 2.0-mW gate power, using the same process as above with transistor f_T's of only 0.6 GHz. The chip uses a single 1.3-V supply.

3) A general-purpose "Master Slice" chip containing 72 unmetallized cells: each cell consists of a five-input DCT^2L AND gate and a two-input DCT^2L NOR gate. DTL and T^2L gates for input and output buffers can be made by using the same components as are used in the AND and NOR gates. The chip is processed up through contact cut and stored. A given logic is implemented by customizing two layers of metal to determine the logic function of individual cells, logic interconnections, and power supply routing. The chip can operate with supplies of 5 V or 2 V or both, with an option for generating the 2-V supply internal to the chip.

4) A DCT^2L arithmetic-logic unit (ALU) which is described in a later section of this paper.

Now that the general DCT^2L concept has been explained, the remainder of the paper will compare DCT^2L to emitter-function logic (EFL) (not to be confused with emitter-follower logic), ECL, and Schottky T^2L. First, the logic families will

be compared by computer-aided transient analysis of individual gates using identical component models. Next, an actual DCT^{2}L ALU will be compared to recent ALU's now in production with ECL and Schottky T^{2}L. An ALU was chosen as a vehicle of comparison because it is a more or less typical modern random-logic chip that is the most complex type commercially available in different logic families.

II. Theoretical Comparison of DCT^{2}L Speed to EFL, ECL, and Schottky T^{2}L

In this section the speed of DCT^{2}L will be computer simulated and compared to speeds of representative LSI gates from the above families. One point of confusion which usually arises from such speed comparisons is that a proposed LSI internal gate is compared to published data on discrete gates of other existing technologies. Since these discrete gates are optimized for high noise immunity and for driving large capacitive loads, their unloaded speed-power relationship does not compare well to gates that have been optimized for driving on-chip loads. However, this study will compare DCT^{2}L to an internal EFL gate and to actual internal ECL and Schottky T^{2}L gates used in recent commercially available high-complexity bipolar IC's. Fig. 3 shows the circuit schematics of the EFL, ECL, and Schottky T^{2}L internal gates considered. These gates will be compared to the DCT^{2}L NOR gate of Fig. 1 with $R_E = 30\ \Omega$. All the gates have 4-mW power dissipation which is defined as nominal room temperature dc power averaged for both inputs high and both inputs low.

The EFL gate of Fig. 3 uses a 2.0-V power supply whereas a previous publication [3] quoted performance at 1.4 V. However, at 1.4 V the power dissipation and speed can be shown to be very dependent on temperature, external power supply variations, and internal power supply voltage drops. Both EFL and DCT^{2}L can operate on a power supply somewhat greater than $1\frac{1}{2}\ V_{BE}$, but 2.0 V was chosen for both in order to have a reasonable control on power and speed. With a 2-V power supply, the increase in resistance with temperature counteracts the decrease in V_{BE} with temperature, thus providing temperature-compensated power for DCT^{2}L. Experimentally, the speed is also nearly constant with temperature because the currents are nearly constant and the voltage swings decrease only slightly.

For all gate simulations, identical component models corresponding to an existing Honeywell process are used. The process is a standard bipolar digital process with two layers of metal and a 4.5-μ 0.35-$\Omega \cdot$ cm epitaxial layer. Fig. 4 shows the minimum-geometry transistor assumed. Fig. 5 shows the mathematical model for that transistor. It is an extended Ebers-Moll model with an f_T of about 0.6 GHz. The model has been used on more than 40 IC's and it accurately predicts dc and transient behavior for transistors operating in the 0.1-10 mA range. Fig. 6 shows the dc model for a Schottky diode, which is made in the same epitaxial layer as the transistor. The placement of the resistors in the model of a Schottky transistor is consistent with the recommendation of Heald and Hodges [4]. All transistors are modeled as in Fig. 5, but with capacitances as shown in Table I for the various transistor types. Capacitances of resistors are modeled as in Fig. 7 assuming 0.3-mil wide base resistors.

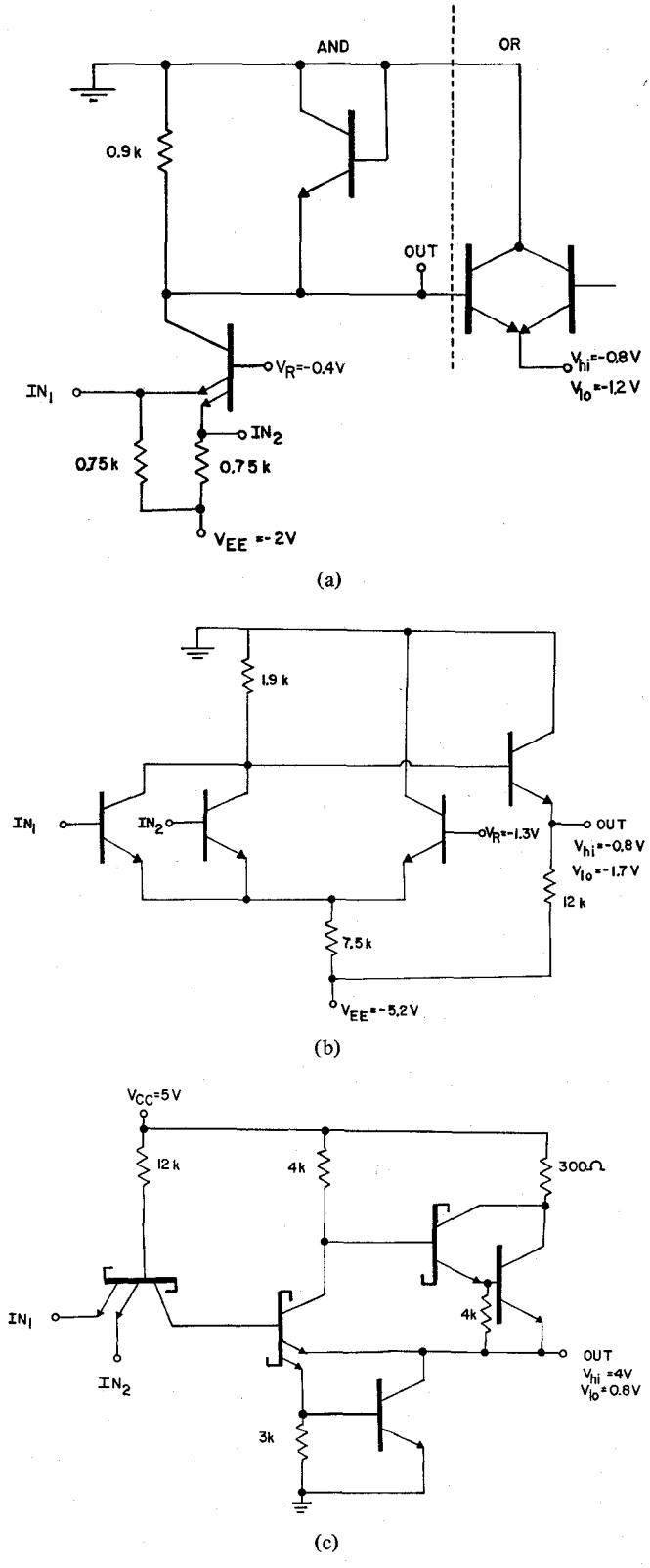

Fig. 3. Circuit schematics for the following 4-mW internal gates: (a) EFL AND, (b) ECL NOR, and (c) Schottky T^{2}L NAND.

The circuits of Fig. 3 were simulated on TESS, which is like an advanced version of SCEPTRE [5]. Table II shows

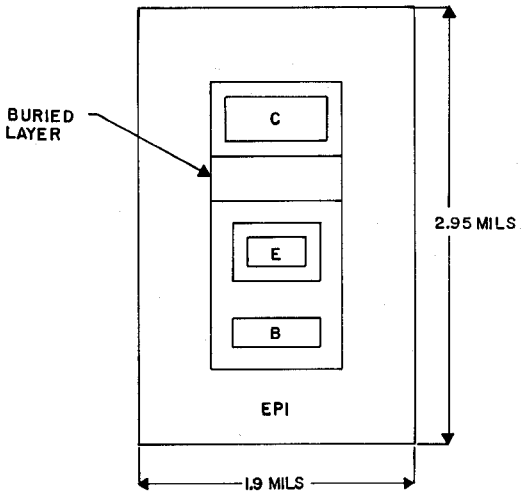

Fig. 4. Minimum-geometry transistor used for computer analysis of all gate types.

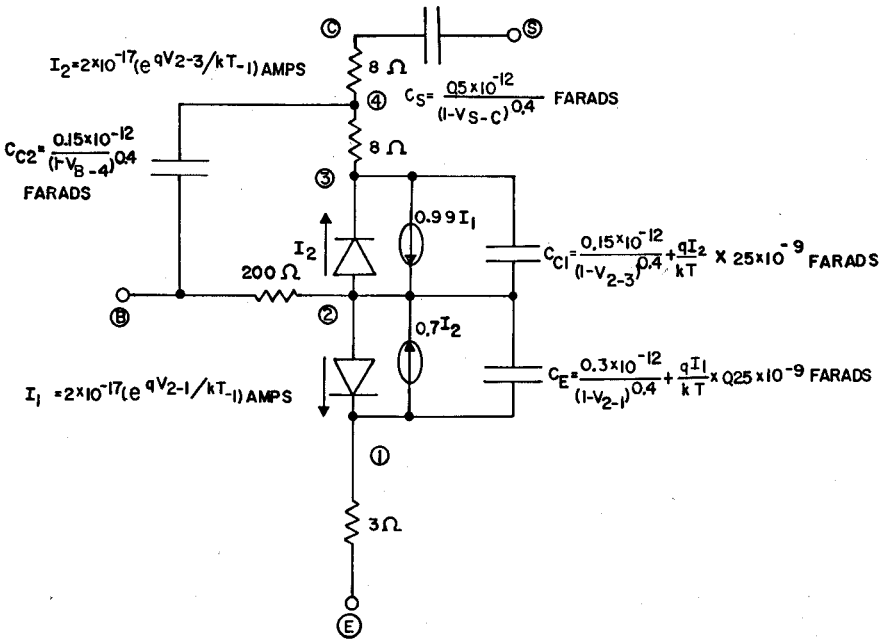

Fig. 5. Computer model for the transistor of Fig. 4.

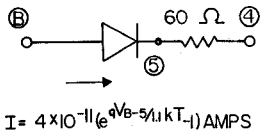

Fig. 6. Computer dc model for a 0.9 × 0.6 mil Schottky diode.

the results of the gate delay calculations for a fan-out of one. Delay was calculated from the input to output thresholds indicated in Table II.

Table II shows that the DCT^{2}L NOR is faster than the other gate types for the same gate power and fabrication process. Although this is a meaningful result, the actual speed-power performance of an LSI chip involves many more complex factors than can be shown in one simple table. These complicating factors include the following.

TABLE I
CAPACITANCES USED IN THE MODELING OF VARIOUS TRANSISTOR TYPES

Transistor	C_{C2} at 0 V (pF)	C_S at 0 V (pF)
1) Standard, as in Figs. 4 and 5	0.15	0.5
2) Two standard transistors in same epi region	0.15	0.7
3) Schottky transistor	0.3	0.6
4) Two Schottky transistors in same epi region	0.3	0.8
5) Double-emitter transistor	0.33	0.6
6) Double-emitter Schottky transistor	0.48	0.7

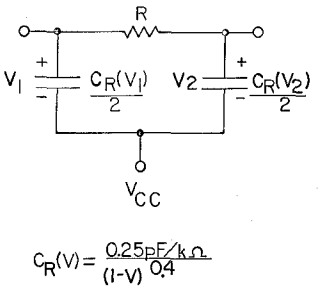

Fig. 7. Computer model for resistors.

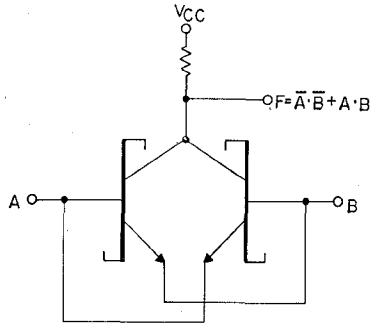

Fig. 8. Gate that performs the coincidence logic function in DCT^{2}L and Schottky T^{2}L.

TABLE II
DELAY CALCULATIONS FOR THE VARIOUS TWO-INPUT GATE TYPES WITH 4-mW GATE POWER AND A FAN-OUT OF ONE

Gate Type	Threshold Voltage (V)	Delay for Input Rising (ns)	Delay for Input Falling (ns)	Average Delay (ns)
1) DCT^{2}L NOR	0.8	1.1	0.9	1.0
2) EFL AND (power is proportional to number of inputs)	−1.2 (input) −0.4 (output)	1.8	1.4	1.6
3) ECL NOR	−1.3	2.7	1.4	2.0
4) Schottky T^{2}L NAND	1.3	8.0	5.0	6.5

1) All of the gate families consist of more than the simple gates considered. For example, EFL also has an OR gate. DCT^{2}L has an AND gate with a delay of 0.5 ns at 4 mW, which is faster than the DCT^{2}L NOR. Both DCT^{2}L and Schottky T^{2}L can use the "coincidence" gate of Fig. 8 and other special gates. ECL uses "series gating" and "collector dotting" to improve speed-power performance.

2) Table II shows only typical delays, whereas a more detailed analysis would take into account variations in processing, supply voltage, and temperature.

3) Table II shows only the delay for a fan-out of one, whereas an LSI chip will have various fan-outs depending on the logic design.

4) The delay calculations were done for only two inputs. The EFL AND gate power is proportional to the number of inputs, which is not true of the other gate types.

5) ECL gates have the OR output also available if a resistor is added to the collector of the reference transistor in Fig. 3(b). An extra emitter follower (which requires extra power) must also be added to use this output. The OR output adds logic flexibility to the circuit set.

6) ECL chips usually have an on-chip voltage reference generator which consumes extra power.

7) If a system interfaces with T^{2}L, which is the most common form of logic, then the extra cost and performance of buffer circuits must be considered. Interfacing with T^{2}L is difficult for EFL and ECL, but straightforward for DCT^{2}L because T^{2}L can drive DCT^{2}L directly inside a chip.

Another important factor in LSI design is the area consumed by a gate. Comparing the circuit diagrams of Figs. 1, 2, and 3, it is obvious that DCT^{2}L takes little area because the circuits are simple and particularly well suited for dense layout in bipolar processes. The two transistors in the DCT^{2}L NOR gate are made in the same epitaxial region, the collector resistor can be made out of the same epitaxial layer as the collector, and the emitter resistor can be made from an n+ emitter diffusion placed directly into the isolation diffusion, thus saving area. Chip area depends on other subtle factors which are hard to assess at the gate level rather than the chip level. For example, the ease of interconnecting the gates is a factor. Gates such as EFL and ECL, which require routing of a separate reference supply, will significantly complicate a layout and add extra area. Circuits that require small ground voltage drops, and therefore wide power lines, also take up more area.

The EFL, ECL, and Schottky T^{2}L gate types were used in the comparison because these gates are fairly well known and represent a cross section of design philosophies. The reader will recognize that DCT^{2}L could be compared to many other gate types as well. For example, "nonthreshold logic" [6] is a logic circuit requiring a special voltage regulator. Gate delay is about 3 ns at 4 mW, so its performance is in the range of the other gates considered.

III. A COMPARISON OF A DCT^{2}L ALU TO SIMILAR CIRCUITS IN ECL AND SCHOTTKY T^{2}L

Because of the above-mentioned difficulties in judging chip speed, power, and area when looking only at the gate level, we will compare an actual DCT^{2}L ALU chip to existing ALU's in the ECL and Schottky T^{2}L families. Such a chip was not available in EFL. Fig. 9 shows the logic diagram of the DCT^{2}L ALU. The logic diagrams of the other ALU's are virtually identical except for different logic implementations inherent in the logic forms. All of these ALU's are considered state of the art logic representations which use several logic tricks such as extensive use of series gating for ECL. The ECL ALU is the MC10181. The Schottky T^{2}L ALU is the 74S181.

The DCT^{2}L ALU uses only NOR and AND gates with a single 2-V supply. The ALU is part of a compatible DCT^{2}L chip family. The inputs of the ALU can be driven by T^{2}L if desired. The input noise margin is less than for T^{2}L because the input threshold is only 0.75 V at room temperature. The output of this ALU is simply a 200-Ω resistor pull-up

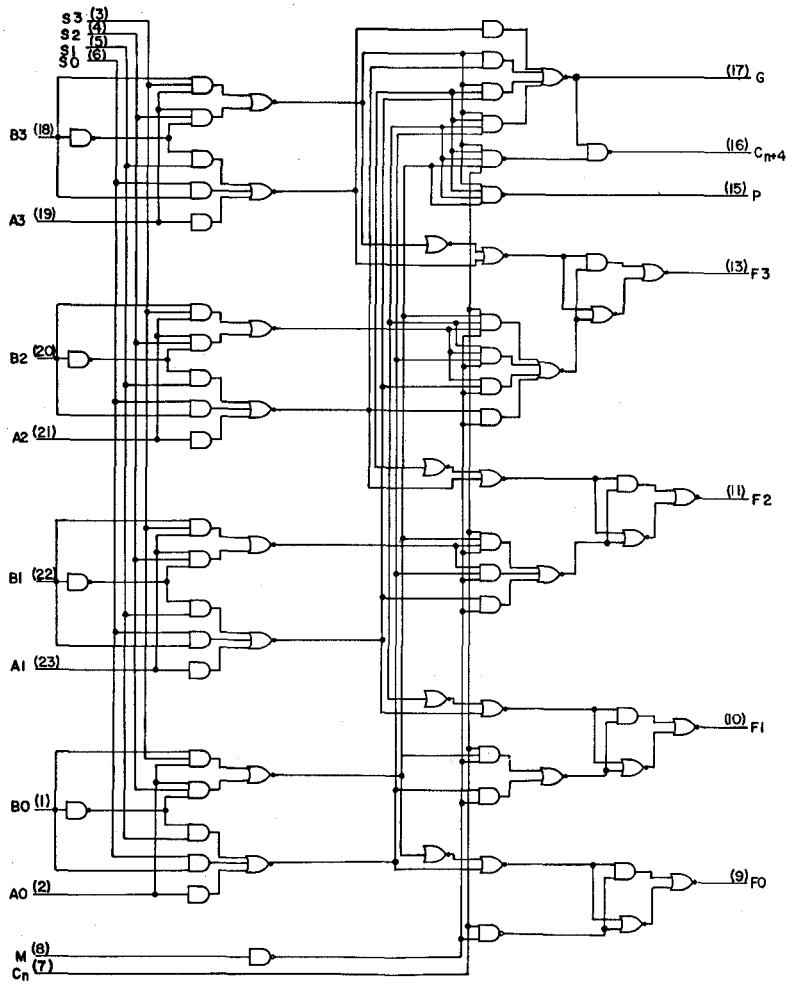

Fig. 9. Logic diagram of the DCT^{2}L ALU.

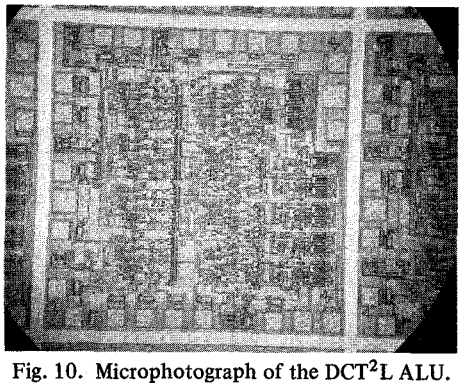

Fig. 10. Microphotograph of the DCT^{2}L ALU.

TABLE III
TYPICAL PROPAGATION DELAYS FOR THE DCT^{2}L ALU

Path	Delay for Input Rising (ns)	Delay for Input Falling (ns)
Any A_i to any F_i	7.0	7.5
Any A_i to P	4.3	5.4
Any A_i to G	6.7	4.9
C_n to C_{n+4}	3.8	6.6

TABLE IV
A COMPARISON OF THE DCT^{2}L ALU TO THE ECL AND SCHOTTKY T^{2}L ALU'S

Circuit Type	Typical dc Power Dissipation (mW)	Chip Area (mils^2)	Minimum Transistor Area (mils^2)	Typical Average Delay (ns)	Transistor f_T (GHz)
1) DCT^{2}L	350	5700	5.6	5.8	0.6
2) ECL	730	7200	3.9	4.4	2
3) Schottky T^{2}L	700	6300	3.6	8.6	1

to 2 V. A higher output high level can be achieved by adding an external pull-up resistor to 5 V to drive T^{2}L if desired.

Fig. 10 shows a picture of the DCT^{2}L ALU. It is 75 X 76 mils. Table III lists the more important typical propagation delays for the DCT^{2}L ALU. Table IV summarizes the more important features of the DCT^{2}L, ECL, and Schottky T^{2}L ALU's. The ECL power includes chip power due to 75-Ω resistor terminations, but does not include the power in the terminating resistors themselves. The average delay for each ALU was calculated by averaging the delays in Table III. Table IV gives minimum transistor areas for each process type. Note that the DCT^{2}L chip is the smallest, even though its process geometries are larger. Also shown in Table IV are the approximate transistor f_T's for each circuit. The DCT^{2}L ALU would be at least as fast as the

TABLE V
A CRUDE FIGURE OF MERIT: THE SPEED-POWER-AREA PRODUCT FOR THE VARIOUS ALU'S

Chip Type	Speed × Power × Area (pJ-mils^2)
1) DCT^{2}L	1.2×10^7 (0.6×10^7 for the ECL process)
2) ECL	2.3×10^7
3) Schottky T^{2}L	3.8×10^7

ECL ALU if its f_T and device area were the same as the ECL process, and if it had two base diffusions to reduce r_b' as in ECL. This speed would be achieved with less than half of the ECL circuit's power, as shown in Table IV. Another ECL ALU similar in design to the one in Table IV was made on the same process as the DCT^{2}L ALU. This new ECL ALU was about the same speed as the DCT^{2}L version, but it required three times the power and $2\frac{1}{2}$ times the area of the DCT^{2}L ALU.

A crude figure of merit for complex chips in the same speed range is the speed-power-area product, which should be as small as possible. Table V lists this figure of merit for the ALU's of Table IV. The DCT^{2}L ALU is seen to be about twice as good as the ECL ALU and three times better than the Schottky T^{2}L ALU. If the ECL process were used for DCT^{2}L, then DCT^{2}L would be about four times better than ECL and six times better than Schottky T^{2}L, according to this figure of merit.

IV. CONCLUSIONS

The DCT^{2}L family of AND and NOR gates is particularly well suited for applications requiring T^{2}L compatibility. The same T^{2}L-compatible chip can also interface directly with ECL. For the same power, the basic DCT^{2}L NOR gate is faster than the basic gates of the EFL, ECL, and Schottky T^{2}L families. Comparison of ALU circuits shows that the DCT^{2}L circuit consumes significantly less power for the same speed, and is smaller than ECL and Schottky T^{2}L circuits made on similar processes. Furthermore, the practicality of DCT^{2}L has been demonstrated on several other logic circuits. The demonstrated performance of DCT^{2}L contradicts the nearly universally accepted notion that ECL is inherently faster than Schottky-clamped saturating circuits. Because of its higher speed and smaller area, DCT^{2}L appears to be the best of the high-speed LSI concepts.

APPENDIX
DERIVATION OF HIGH-STATE INPUT CURRENT FOR THE DCT^{2}L AND GATE

The following is a derivation showing how the extra emitter in Fig. 2 reduces the high-state input current, which is a common problem in T^{2}L-like circuits. Fig. 11 shows the Ebers-Moll model for the AND gate of Fig. 2. Parasitic vertical p-n-p gain is assumed to be negligible. There are n multiple-emitter inputs with one input high. k is the ratio of the area of the feedback emitter to the area of each of the input emitters. α_i is the inverse common-base current gain when all emitters are tied together and act as a collector.

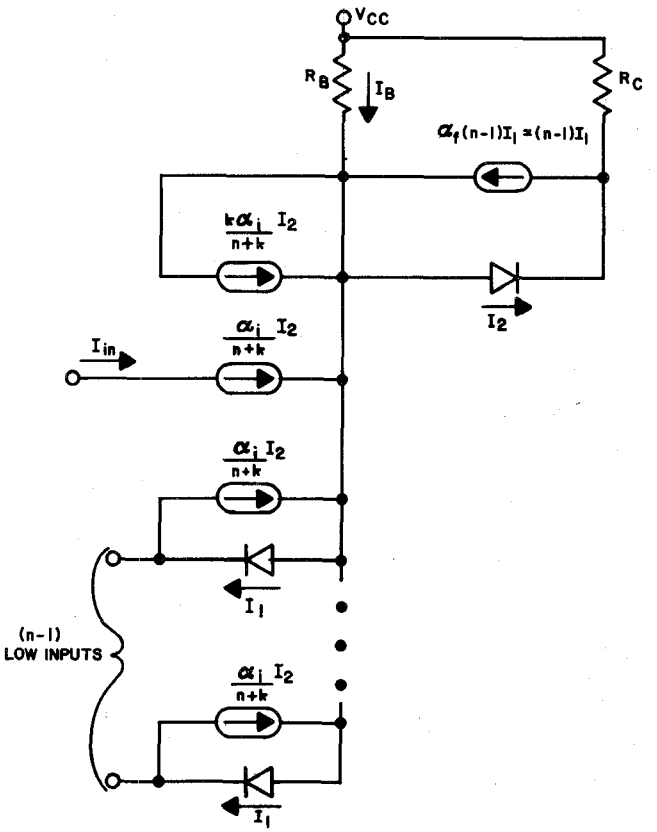

Fig. 11. Ebers-Moll model for the AND gate of Fig. 2.

Summing currents and solving for the high-state input current we obtain

$$I_{in} = \frac{\beta_i I_B}{n + (\beta_i + 1)k} \tag{1}$$

where β_i is defined by the usual equation

$$\beta_i = \frac{\alpha_i}{1 - \alpha_i}. \tag{2}$$

If there is no feedback emitter, which is the same as having $k = 0$, then (1) shows that

$$I_{in} = \frac{\beta_i I_B}{n}. \tag{3}$$

This is a larger input current than for a finite k. On the other hand, if $k \neq 0$ and $\beta_i \gg 1$, (1) reduces to

$$I_{in} = \frac{I_B}{k}. \tag{4}$$

Equations (3) and (4) show that when β_i is large, the high-state input current will be significantly reduced by including an extra emitter fed back to the base.

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David E. Fulkerson (S'66–M'67) was born in Mora, Minn., on April 3, 1941. He received the B.S., M.S., and Ph.D. degrees from the University of Minnesota, Minneapolis, in 1963, 1965, and 1967, respectively.

From December, 1966, to March, 1967, he was an Assistant Professor in the Department of Electrical Engineering, University of Minnesota. He is presently working on integrated-circuit development and research at the Solid State Electronics Center, Honeywell, Inc., Plymouth, Minn.

Dr. Fulkerson is a member of Tau Beta Pi and Eta Kappa Nu.

Low Power CML IC Crosspoint Switch Matrix for Space Division Digital Switching Networks

MANABU SUNAZAWA, MASAHARU KAWAKAMI, NAOAKI NARUMI, KOHJI ISHIKAWA, TOSHIYUKI HANI, HIROMU IWAMOTO, AND KOUICHI FUJITA

Abstract—**A CML IC crosspoint switch matrix for space division digital switching networks is described.**

This crosspoint switch matrix is constructed from CML gates for digitized video signals and p-n-p n-p-n transistor type holding circuits that hold the ON or OFF state of the CML gates. This holding circuit cuts off the power of the unselected crosspoints to reduce the total power dissipation of the switch matrix circuit.

The CML IC crosspoint switch, with a 4 × 4 matrix size, is fabricated on a single chip.

Dynamic test of the subsystem, in which fabricated switch matrices are connected in cascade stages, has indicated that it is applicable to high speed space division digital switching networks.

I. Introduction

INTEREST in new types of communication services, such as video communications and facsimile transmission, in addition to conventional telephone communications, has been considerably stimulated by the rapid progress in the area of communications. Because video communication deals with a much higher frequency bandwidth than telephone communication, stress should be placed on the reduction of noise, e.g., crosstalk, to prevent degrading transmission quality. Therefore, digital transmission, which has good noise immunity characteristics, has been considered and space division digital switching systems have been proposed as methods for realizing economic and high performance video communication systems. The only factor lacking has been electronic crosspoint switches suitable for exchanging digitized video signals in a space division switching network.

Various kinds of crosspoint switches, such as the electromechanical crossbar switch, the p-n-p-n IC switch, and the MOS IC switch [2], have been considered for digital switching use. However, these are analog mode switches which have no pulse waveform regeneration function. Accordingly, if these analog mode switches are connected in cascade stages, the output pulse waveform of the last stage is distorted by impedance mismatch, crosstalk noise, etc.

Ideally, in an MOS IC switch with a nonlinear limiter amplifier that has a threshold characteristic involving a pulse waveform regeneration function, the above mentioned problem does not occur. But the MOS IC switch has comparatively large pulse width fluctuation because of large ON resistance deviations of the MOS transistor. This factor influences the threshold stability of the amplifier.

On the other hand, the electronic crosspoint switch, constructed from logic circuits, is a digital mode switch which has a pulse waveform regeneration function, and pulse waveform distortion and pulse width fluctuation problems mentioned above need not be taken into consideration.

For these reasons, many investigations have been made on logic circuits with the progress of semiconductor integrated circuit and digital electronic circuit technology for a background.

Digital mode switches for a space division digital switching system can be easily constructed, using logic circuits for cross-

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M. Sunazawa, M. Kawakami, N. Narumi, and K. Ishikawa are with the Musashino Electrical Communication Laboratory, Nippon Telegraph and Telephone Public Corporation, Tokyo, Japan.

T. Hani, H. Iwamoto, and K. Fujita are with Fujitsu Limited, Kawasaki-shi, Japan.