ETROC1 Array Design Note

This document aims to provide information for ETROC1 Array chip test.

Author: Wei Zhang
Co-author: Datao, Quan Sun, Tiankuan Liu

Version 0.1: Feb 21, 2020

Email: wzhang@mails.ccnu.edu.cn

Contents

1 Pin Assignment **1**

2 ETROC1 Array Chip block diagram **3**

3 I2C Interface **4**

1 Pin Assignment

The ETROC1 Array chip has 50 pads that can be divided into three types: general IO pads, differential IO pads, and power IO pads, respectively. The 50 pads are located on the bottom side of the ETROC1 chip. The below table listed the detail pad information of the ETROC1 Array chip.

Table 1: ETROC1 Array Chip I2C Register Map

NO.	Name	Location (x,y)	Type	Description
1	vdd_IO_A	(1020, 127.79)	Power	Power supply of the Tx and the Rx, 1.2 V
2	vss_IO_A	(1130, 127.79)	Ground	Ground of the Tx and Rx, 0 V
3	CLK1P28GI_P_A	(1240, 127.79)	Digital In	Positive input of the 1.28 GHz clock or the 320 MHz clock
4	CLK1P28GI_N_A	(1350, 127.79)	Digital In	Negative input of the 1.28 GHz clock or the 320 MHz clock
5	CLK320MI_P_A	(1460, 127.79)	Digital In	Positive input of the 320 MHz clock
6	CLK320MI_N_A	(1570, 127.79)	Digital In	Negative input of the 320 MHz clock
7	CLK40MI_P_A	(1680, 127.79)	Digital In	Positive input of the 40 MHz clock
8	CLK40MI_N_A	(1790, 127.79)	Digital In	Negative input of the 40 MHz clock
9	QInj_P_A	(1900, 127.79)	Digital In	Positive input of the charge injection trigger
10	QInj_N_A	(2010, 127.79)	Digital In	Negative input of the charge injection trigger
11	CLKTO_P_A	(2120, 127.79)	Digital Out	Positive Output of the test clock, either 40 MHz clock or 320 MHz pulse
12	CLKTO_N_A	(2230, 127.79)	Digital Out	Negative Output of the test clock, either 40 MHz clock or 320 MHz pulse
13	DOut_P_A	(2340, 127.79)	Digital Out	Positive data output of the array, for either DMRO or SRO
14	DOut_N_A	(2450, 127.79)	Digital Out	Negative data output of the array, for either DMRO or SRO
15	vdd_IO_A	(2560, 127.79)	Power	Power supply of the Tx and the Rx, 1.2 V
16	vss_IO_A	(2670, 127.79)	Ground	Ground of the Tx and Rx, 0 V
17	vdd_Discri_A	(2780, 127.79)	Power	Power supply of the discriminator, 1.2 V
18	vss_Discri_A	(2890, 127.79)	Ground	Ground of the discriminator, 0 V
19	vdd_PA_A	(3000, 127.79)	Power	Power supply of the pre-amplifier, 1.2 V
20	vss_PA_A	(3110, 127.79)	Ground	Ground of the pre-amplifier, 0 V
21	VRef_A	(3220, 127.79)	Analog Input	1 V reference voltage input
22	vdd_PA_A	(3330, 127.79)	Power	Power supply of the pre-amplifier, 1.2 V
23	vss_PA_A	(3440, 127.79)	Ground	Ground of the pre-amplifier, 0 V
24	VTHInOut_A	(3550, 127.79)	Analog Inout	Threshold voltage of the discriminator
25	vdd_PA_A	(3660, 127.79)	Power	Power supply of the pre-amplifier, 1.2 V
26	vss_PA_A	(3770, 127.79)	Ground	Ground of the pre-amplifier, 0 V
27	vdd_QInj_A	(3880, 127.79)	Power	Power supply of the charge injection, 1.2 V
28	vss_QInj_A	(3990, 127.79)	Ground	Ground of the charge injection, 0 V
29	vdd_CLK_A	(4100, 127.79)	Power	Power supply of the clock generation circuits, 1.2 V
30	vss_CLK_A	(4210, 127.79)	Ground	Ground of the clock generation circuits, 0 V
31	vdd_Discri_A	(4320, 127.79)	Power	Power supply of the discriminator, 1.2 V
32	vss_Discri_A	(4430, 127.79)	Ground	Ground of the discriminator, 0 V
33	vdd_Dig_A	(4540, 127.79)	Power	Power supply of the digital circuit, 1.2 V
34	vss_Dig_A	(4650, 127.79)	Ground	Ground of the digital circuit, 0 V
35	BC0_A	(4760, 127.79)	Digital input	Bunch crossing zero
36	L1ACC_A	(4870, 127.79)	Digital input	Level-1 acceptance
37	RSTN_A	(4980, 127.79)	Digital input	Reset for I2C/SRO/Controller/DMRO
38	DiscriOut_A	(5090, 127.79)	Digital output	Discriminator output of the array

39	A0_A	(5200, 127.79)	Digital input	I2C address low bit for the slave A
40	A1_A	(5310, 127.79)	Digital input	I2C address high bit for the slave A
41	vdd_Dig_A	(5420, 127.79)	Power	Power supply of the digital circuit, 1.2 V
42	vss_Dig_A	(5530, 127.79)	Ground	Ground of the digital circuit, 0 V
43	SCL_A_A	(5640, 127.79)	Digital input	I2C clock for the slave A
44	SDA_A_A	(5750, 127.79)	Digital input	I2C data for the slave A
45	A0_B_A	(5860, 127.79)	Digital input	I2C address low bit for the slave B
46	A1_B_A	(5970, 127.79)	Digital input	I2C address low bit for the slave B
47	SCL_B_A	(6080, 127.79)	Digital input	I2C clock for the slave B
48	SDA_A_A	(6190, 127.79)	Digital input	I2C data for the slave B
49	vdd_Dig_A	(6300, 127.79)	Power	Power supply of the digital circuit, 1.2 V
50	vss_Dig_A	(6410, 127.79)	Ground	Ground of the digital circuit, 0 V

The layout of ETROC1 Array chip is shown as Figure 1. The **vdd_IO** pad is named as the pin 1. From the anti-clockwise direction, the pad number is increasing with the step 1.

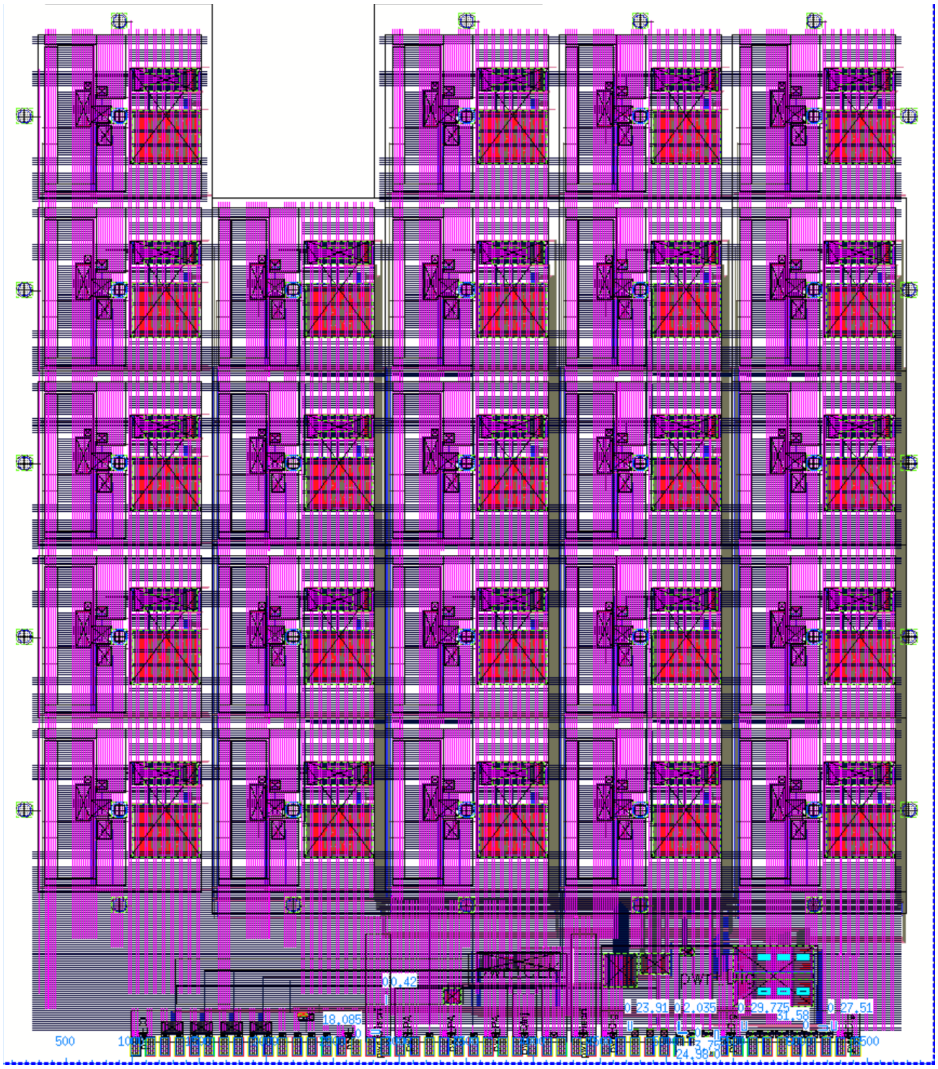

Figure 1: ETROC1 Array Chip Layout

2 ETROC1 Array Chip block diagram

3 I2C Interface

A generic I2C slave is used twice in ETROC1. Each slave provides 32 bytes for reading and 16 bytes for writing by ETROC1. A 4-bit chip ID and a 4-bit chip reversion are available as well. The registers in the I2C slave are triplicated to mitigate SEU. The registers in two slaves are named REG_A and REG_B, respectively. Their addresses are 7'b00000A1_AA0_A and 7'b11111A1_BA0_B, respectively. Note that the address of 7'b0000000 should be avoided for the slave A.

Table 2: ETROC1 Array Chip I2C Register Map

NO.	Name	Reg name	Description	Default value	Default value
1	CLSel[1:0]	Reg_A_00[1:0]	selection of load capacitance of the preamp first stage, 2'b00 $--> 0$ fC, 2'b01 $--> 80$ fC, 2'b10 $--> 80$ fC, 2'b11 $--> 160$ fC	2'b00	0xf8
2	RfSel[1:0]	Reg_A_00[3:2]	Feedback resistance selection, 2'b00 $--> 10\,\mathrm{kOhm}$, 2'b01 $--> 10\,\mathrm{kOhm}$, 2'b10 $--> 5.7\,\mathrm{kOhm}$, 2'b11 $--> 4.4\,\mathrm{kOhm}$	2'b10	
3	HysSel[3:0]	Reg_A_00[7:4]	Hysteresis voltage selection, 4'b0000 $-->$ Vhys1, 4'b0001 $-->$ Vhys2, 4'b0011 $-->$ Vhys3, 4'b0111 $-->$ Vhys4, 4'b1111 $-->$ Vhys5; $Vhys1 > Vhys2 > Vhys3 > Vhys4 = Vhys5 = 0$; shared by all the pixels	4'b1111	
4	IBSel[2:0]	Reg_A_01[2:0]	Bias current selection of the input transistor in the preamp, 3'b000 $-->$ I1, 3'b000, 3'b010, 3'b100 $-->$ I2, 3'b011, 3'b110, 3'b101 $-->$ I3, 3'b111 $-->$ I4; $I1 > I2 > I3 > I4$, shared by all pixels	3'b111	0x37
5	QSel[4:0]	Reg_A_00[7:3]	selection of injected charge, from 1 fC (5'b00000) to 32 fC (5'b11111), Typical charge from LGAD sensor is 7 fC (5'b00110); shared by all the pixels	5'b00110	
6	DIS_VTHInOut[7:0]	Reg_A_02[7:0]	Disable threshold voltage input/output of the specified pixel, active high. Each bit controls a pixel according the pixel index map. Only one of threshold can be enable at a time. For example, DIS_VTHInOut = 16'h4000	8'b11111111	0xff
7	DIS_VTHInOut[15:8]	Reg_A_03[7:0]	Disable threshold voltage input/output of the specified pixel, active high. Each bit controls a pixel according the pixel index map. Only one of threshold can be enable at a time. For example, DIS_VTHInOut = 16'h4000	8'b11111111	0xff
8	EN_DiscriOut[7:0]	Reg_A_04[7:0]	Enable the discriminator output, active high. Each bit in EN_DiscriOut[7:4] represents the row, and each bit in EN_DiscriOut[3:0] represents the column. Users can enable the discriminator output from a specified pixel. Only one row can be specified at a time. That means no more than one bit in EN_DiscriOut[7:4] can be set to 1'b1 at a time. When more than one bit is set to 1'b1, or all bits are set to 0 in EN_DiscriOut[3:0], the discriminator output is disable	8'b00010001	0x11
9	EN_QInj[7:0]	Reg_A_05[7:0]	Enable the charge injection of the specified pixel, active high. Each bit controls a pixel. Users can specify non or more pixel to enable the charge injection	8'b00000001	0x01
10	EN_QInj[15:8]	Reg_A_06[7:0]	Enable the charge injection of the specified pixel, active high. Each bit controls a pixel. Users can specify non or more pixel to enable the charge injection	8'b00000000	0x00

11	OE_DMRO_Row[3:0]	Reg_A_07[3:0]	Output enable of DMRO in rows. Each bit represents a row. Only one row can be enabled for output at a time. For example: 4'0000 : no DMRO output enable. 4'b0001 : the row 0 of DMRO output is enable. 4'b0100 : the row 2 of DMRO output is enable. 4'b1010 is invalid.	4'b0001	0x01
12	DMRO_COL[1:0]	Reg_A_07[5:4]	Select DMRO output from a specified column. 2'b00 : column 0 is selected; 2'b01 : column 1 is selected; 2'b10 : column 2 is selected; 2'b11 : column 3 is selected.	2'b00	
13	RO_SEL	Reg_A_07[6]	Select readout mode from either SRO or DMRO. 1'b0 : DMRO enabled; 1'b1 : SRO enabled.	1'b0	
14	PD_DACDiscri[7:0]	Reg_A_08[7:0]	Power down the DAC and the discriminator in pixels, active high. Each bit controls a pixel. Users can specify non or more pixels to control	8'b00000000	0x00
15	PD_DACDiscri[15:8]	Reg_A_09[7:0]	Power down the DAC and the discriminator in pixels, active high. Each bit controls a pixel. Users can specify non or more pixels to control	8'b00000000	0x00
16	VTHIn[7:0]	Reg_A_0A[7:0]	Threshold voltage input	8'b00000000	0x00
17	VTHIn[15:8]	Reg_A_0B[7:0]	Threshold voltage input	8'b00000010	0x02
18	VTHIn[23:16]	Reg_A_0C[7:0]	Threshold voltage input	8'b00001000	0x08
19	VTHIn[31:24]	Reg_A_0D[7:0]	Threshold voltage input	8'b00100000	0x20
20	VTHIn[39:32]	Reg_A_0E[7:0]	Threshold voltage input	8'b10000000	0x80
21	VTHIn[47:40]	Reg_A_0F[7:0]	Threshold voltage input	8'b00000000	0x00
22	VTHIn[55:48]	Reg_A_10[7:0]	Threshold voltage input	8'b00000010	0x02
23	VTHIn[63:56]	Reg_A_11[7:0]	Threshold voltage input	8'b00001000	0x08
24	VTHIn[71:64]	Reg_A_12[7:0]	Threshold voltage input	8'b00100000	0x20
25	VTHIn[79:72]	Reg_A_13[7:0]	Threshold voltage input	8'b10000000	0x80
26	VTHIn[87:80]	Reg_A_14[7:0]	Threshold voltage input	8'b00000000	0x00
27	VTHIn[95:88]	Reg_A_15[7:0]	Threshold voltage input	8'b00000010	0x02
28	VTHIn[103:96]	Reg_A_16[7:0]	Threshold voltage input	8'b00001000	0x08
29	VTHIn[111:104]	Reg_A_17[7:0]	Threshold voltage input	8'b00100000	0x20
30	VTHIn[119:112]	Reg_A_18[7:0]	Threshold voltage input	8'b10000000	0x80
31	VTHIn[127:120]	Reg_A_19[7:0]	Threshold voltage input	8'b00000000	0x00
32	VTHIn[135:128]	Reg_A_1A[7:0]	Threshold voltage input	8'b00000010	0x02
33	VTHIn[143:136]	Reg_A_1B[7:0]	Threshold voltage input	8'b00001000	0x08
34	VTHIn[151:144]	Reg_A_1C[7:0]	Threshold voltage input	8'b00100000	0x20
35	VTHIn[159:152]	Reg_A_1D[7:0]	Threshold voltage input	8'b10000000	0x80
36	ROI[7:0]	Reg_A_1E[7:0]	Region of interest. low 8 bit vector specifies which pixels are enabled for readout	8'b11111111	0xff
37	ROI[15:8]	Reg_A_1F[7:0]	Region of interest. high 8 bit vector specifies which pixels are enabled for readout	8'b11111111	0xff
38	TDC_autoReset	Reg_B_00[0]	TDC autoReset mode	1'b0	0x1C
39	TDC_enableMon	Reg_B_00[1]	Delay Line raw data output enable	1'b0	
40	TDC_enable	Reg_B_00[2]	Enable TDC	1'b1	
41	TDC_polaritySel	Reg_B_00[3]	TDC Controller signal polarity select	1'b1	
42	TDC_resetn	REG_B_00[4]	TDC reset, low active	1'b1	
43	TDC_selRawCode	REG_B_00[5]	Select TDC raw code, always "0"	1'b0	

44	TDC_testMode	REG_B_00[6]	TDC test mode select	1'b0	
45	TDC_timeStampMode	REG_B_00[7]	TDC Calibration data timeStamp mode	1'b0	
46	TDC_level[2:0]	REG_B_01[2:0]	TDC Encoder bubble tolerance	3'b001	0x01
47	TDC_offset[6:0]	REG_B_02[6:0]	TDC ripple counter window offset	7'b0000000	0x00
48	dllEnable	REG_B_03[0]	Enable loop control of DLL	1'b1	0x09
49	dllForceDown	REG_B_03[1]	Force to pull down the output of the phase detector, high active	1'b0	
50	dllCapReset	REG_B_03[2]	Reset the control voltage of DLL to power supply, high active	1'b0	
51	dllCPCurrent[3:0]	REG_B_03[6:3]	Charge pump current control, ranging from 1 to 15 uA	4'b0001	
52	PhaseAdj[7:0]	REG_B_04[7:0]	Phase control bits, PhaseAdj[7:3] for coarse, [2:0] for fine	8'b00000000	0x00
53	RefStrSel[7:0]	REG_B_05[7:0]	TDC reference strobe selection	8'b00000011	0x03
55	DMRO_ENScr	REG_B_06[0]	DMRO Enable Scrambler, high active	1'b1	0x41
56	DMRO_revclk	REG_B_06[1]	DMRO 40 MHz clock reverse	1'b0	
57	DMRO_reverse	REG_B_06[2]	DMRO reverse output data, high active	1'b0	
58	DMRO_testMode	REG_B_06[3]	DMRO test mode select	1'b0	
59	TestCLK0	REG_B_06[4]	TestCLK0=1, the phase shifter is bypassed	1'b0	
60	TestCLK1	REG_B_06[5]	TestCLK1=1, the reference strobe generator is bypassed	1'b0	
61	CLKOutSel	REG_B_06[6]	Select output from either 40 MHz clock or TDC reference strobe	1'b1	
62	Clk1G28_equ[1:0]	REG_B_07[1:0]	Equalization strength of the Rx for 1.28 GHz	2'b00	0x38
63	Clk1G28_invertData	REG_B_07[2]	1.28 GHz clock input Rx data invert	1'b0	
64	Clk1G28_enTermination	REG_B_07[3]	Enable 1.28 GHz clock input Rx termination	1'b1	
65	Clk1G28_setCommMode	REG_B_07[4]	Set 1.28 GHz clock input Rx common mode	1'b1	
66	Clk1G28_enableRx	REG_B_07[5]	Enable 1.28 GHz clock input Rx	1'b1	
67	Clk320M_equ[1:0]	REG_B_08[1:0]	Equalization strength of the Rx for 320 MHz	2'b00	0x18
68	Clk320M_invertData	REG_B_08[2]	320 MHz clock input Rx data invert	1'b0	
69	Clk320M_enTermination	REG_B_08[3]	Enable 320 MHz clock input Rx termination	1'b1	
70	Clk320M_setCommMode	REG_B_08[4]	Set 320 MHz clock input Rx common mode	1'b1	
71	Clk320M_enableRx	REG_B_08[5]	Enable 320 MHz clock input Rx	1'b0	
72	Clk40M_equ[1:0]	REG_B_09[1:0]	Equalization strength of the Rx for 40 MHz	2'b00	0x18
73	Clk40M_invertData	REG_B_09[2]	40 MHz clock input Rx data invert	1'b0	
74	Clk40M_enTermination	REG_B_09[3]	Enable 40 MHz clock input Rx termination	1'b1	
75	Clk40M_setCommMode	REG_B_09[4]	Set 40 MHz clock input Rx common mode	1'b1	
76	Clk40M_enableRx	REG_B_09[5]	Enable 40 MHz clock input Rx	1'b0	
77	QInj_equ[1:0]	REG_B_0A[1:0]	Equalization strength of the Rx for QInj	2'b00	0x38
78	QInj_invertData	REG_B_0A[2]	QInj input Rx data invert	1'b0	
79	QInj_enTermination	REG_B_0A[3]	Enable QInj input Rx termination	1'b1	
80	QInj_setCommMode	REG_B_0A[4]	Set QInj input Rx common mode	1'b1	
81	QInj_enableRx	REG_B_0A[5]	Enable QInj input Rx	1'b1	
82	CLKTO_AmplSel[2:0]	REG_B_0B[2:0]	CLKTO CML driver amplitude selection	3'b111	0x77
83	CLKTO_disBIAS[3]	REG_B_0B[3]	Disable CLKTO CML Driver Bias, high active	1'b0	
84	Dataout_AmplSel[2:0]	REG_B_0B[6:4]	Dataout output CML driver amplitude selection	3'b111	
85	Dataout_disBIAS[3]	REG_B_0B[7]	Disable Dataout CML Driver Bias, high active	1'b0	