ETROC1 Single Pixel Design Note

This document aims to provide information for ETROC1 single pixel chip test.

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1 Pin Assignment

The ETROC1 Single Pixel chip has 34 pads that can be divided into three types: general IO pads, differential IO pads, and power IO pads, respectively. The 34 pads are located on the top side of the ETROC1 chip. The below table listed the detail pad information of the ETROC1 Single Pixel chip.

Table 1: ETROC1 Single Pixel Chip pads information

NO.	Name	Location (x,y)	Type	Description
1	RSTN_S	(4015.09, 8872.21)	Digital In	I2C Reset signal
2	SCL_S	(3905.09, 8872.21)	Digital In	I2C write/read clock
3	SDA_S	(3795.09, 8872.21)	Digital In/Out	I2C write/read data
4	CLKTO_N_S	(3685.09, 8872.21)	Digital Out	Negative output of the test clock, 40M or 320M clock
5	CLKTO_P_S	(3575.09, 8872.21)	Digital Out	Positive output of the test clock, 40M or 320M clock
6	VDD_Dig_S	(3465.09, 8872.21)	Power supply	Power supply of the digital circuit, $1.2\,\mathrm{V}$
7	VSS_Dig_S	(3355.09, 8872.21)	Gound	Ground for the digital circuit, $0\,\mathrm{V}$
8	DOut_N_S	(3245.09, 8872.21)	Digital Out	$1.28\,\mathrm{Gbps}$ data output, negative
9	DOut_P_S	(3135.09, 8872.21)	Digital Out	$1.28\,\mathrm{Gbps}$ data output, positive
10	QInj_N_S	(3025.09, 8872.21)	Digital In	Negative input of the charge injection trigger
11	QInj_P_S	(2915.09, 8872.21)	Digital In	Positive input of the charge injection trigger
12	CLK40MI_N_S	(2805.09, 8872.21)	Digital In	Negative input of the $40\,\mathrm{MHz}$ clock
13	CLK40MI_P_S	(2695.09, 8872.21)	Digital In	Positive input of the $40\,\mathrm{MHz}$ clock
14	CLK320MI_N_S	(2585.09, 8872.21)	Digital In	Negative input of the $320\,\mathrm{MHz}$ clock
15	CLK320MI_P_S	(2475.09, 8872.21)	Digital In	Positive input of the $320\,\mathrm{MHz}$ clock
16	CLK1P28GI_N_S	(2365.09, 8872.21)	Digital In	Negative input of the $1.28\,\mathrm{GHz}$ clock
17	CLK1P28GI_P_S	(2255.09, 8872.21)	Digital In	Positive input of the $1.28\,\mathrm{GHz}$ clock
18	VDD_Dig_S	(2145.09, 8872.21)	Power supply	Power supply of the digital circuit, $1.2\,\mathrm{V}$
19	VSS_Dig_S	(2035.09, 8872.21)	Gound	Ground for the digital circuit, $0\,\mathrm{V}$
20	DiscriOut_S	(1925.09, 8872.21)	Digital Out	I2C module serial data
21	PAIn_S	(1815.09, 8872.21)	Analog In	Input of the preamp
22	PAIn_S	(1705.09, 8872.21)	Analog In	Input of the preamp
23	VDD_PA_S	(1595.09, 8872.21)	Power supply	Power supply for preamp, $1.2\,\mathrm{V}$
24	VSS_PA_S	(1485.09, 8872.21)	Ground	Ground for GRO module
25	VTHInOut_S	(1375.09, 8872.21)	Analog Out	DAC analog output
26	VRef_S	(1265.09, 8872.21)	Analog In	$1\,\mathrm{V}$ voltage reference input
27	AOut_S	(1155.09, 8872.21)	Analog Out	Output of the analog buffer
28	VDD_Buf_S	(1045.09, 8872.21)	Power supply	Power supply for analog buffer, $1.5\,\mathrm{V}$
29	VSS_Buf_S	(935.09, 8872.21)	Ground	Ground for analog buffer, $0\,\mathrm{V}$
30	QV_S	(825.09, 8872.21)	Analog In/Out	Charge injection input/output
31	VDD_QInj_S	(715.09, 8872.21)	Power supply	Power supply for charge injection, $1.2\,\mathrm{V}$
32	VSS_QInj_S	(605.09, 8872.21)	Ground	Ground for analog buffer, $0\,\mathrm{V}$
33	VDD_Discri_S	(495.09, 8872.21)	Power supply	Power supply for discriminator, $1.2\,\mathrm{V}$
34	VSS_Discri_S	(385.09, 8872.21)	Ground	Ground for discriminator, $0\,\mathrm{V}$

The layout of ETROC1 Single Pixel chip is shown as Figure 1. The **RSTN** pad is named as the pin 1. From the anti-clockwise direction, the pad number is increasing with the step 1.

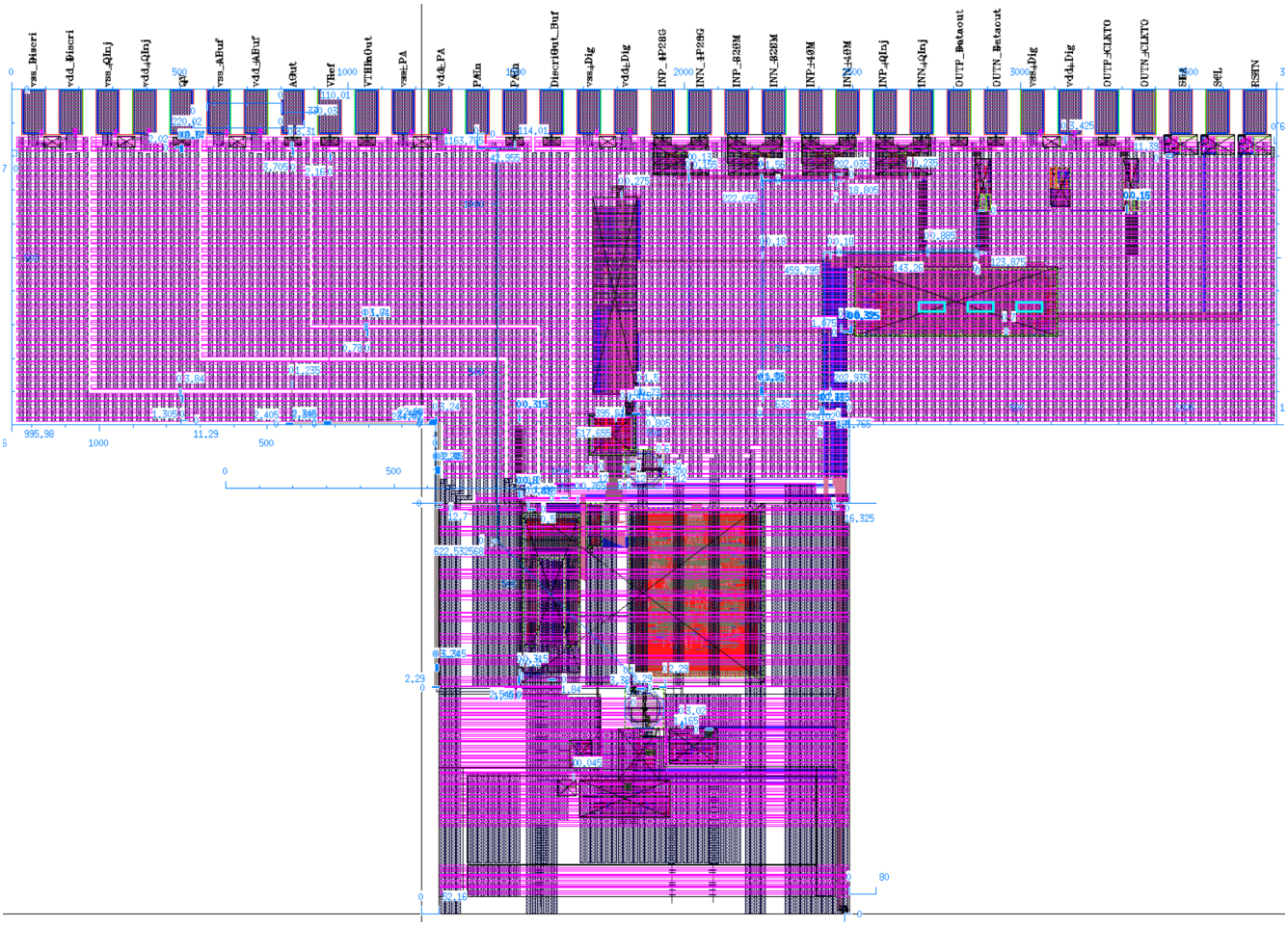

Figure 1: Single Pixel Chip Layout

2 I2C Interface

The ETROC1 Single Pixel chip employs an I2C interface as slow control. The slave provides 32 bytes for writing and 16 bytes for reading by ETROC1. A 4-bit chip ID and a 4-bit chip reversion are available as well. The registers in the I2C are triplicated to mitigate SEU. The slave address is 7'b1001110 (**0x4E**).

Table 2: ETROC1 Single Pixel Chip I2C Register Map

NO.	Name	Reg name	Description	Default value	Default value
1	TDC_autoReset	Reg_00[0]	TDC autoReset mode	1'b0	0x1C
2	TDC_enableMon	REG_00[1]	Delay Line raw data output enable	1'b0	
3	TDC_enable	REG_00[2]	Enable TDC	1'b1	
4	TDC_polaritySel	REG_00[3]	TDC Controller signal polarity select	1'b1	
5	TDC_resetn	REG_00[4]	TDC reset, low active	1'b1	
6	TDC_selRawCode	REG_00[5]	Select TDC raw code, always "0"	1'b0	
7	TDC_testMode	REG_00[6]	TDC test mode select	1'b0	
8	TDC_timeStampMode	REG_00[7]	TDC Calibration data timeStamp mode	1'b0	
9	TDC_level[2:0]	REG_01[2:0]	TDC Encoder bubble tolerance	3'b001	0x01
10	TDC_offset[6:0]	REG_02[6:0]	TDC ripple counter window offset	7'b0000000	0x09
11	dllEnable	REG_03[0]	Enalbe loop control of DLL	1'b1	0x00
12	dllForceDown	REG_03[1]	Force to pull down the output of the phase detector, high active	1'b0	
13	dllCapReset	REG_03[2]	Reset the control voltage of DLL to power supply, high active	1'b0	
14	dllCPCurrent[3:0]	REG_03[6:3]	Charge pump current control, ranging from 1 to 15 uA	4'b0001	
15	PhaseAdj[7:0]	REG_04[7:0]	Phase control bits, PhaseAdj[7:3] for coarse, [2:0] for fine	7'b0000000	0x00
16	RefStrSel[7:0]	REG_05[7:0]	TDC reference strobe selection	8'b00000011	0x03
17	DMRO_resetn	REG_06[0]	DMRO reset, low active	1'b1	0x83
18	DMRO_ENScr	REG_06[1]	DMRO Enable Scrambler, high active	1'b1	
19	DMRO_reclk	REG_06[2]	DMRO 40 MHz clock reverse	1'b0	
20	DMRO_reverse	REG_06[3]	DMRO reverse output data, high active	1'b0	
21	DMRO_testMode	REG_06[4]	DMRO test mode select	1'b0	
22	TestCLK0	REG_06[5]	TestCLK=1, the phase shifter is bypassed	1'b0	
23	TestCLK1	REG_06[6]	TestCLK=1, the reference strobe generator is bypassed	1'b0	
24	CLKOutSel	REG_06[7]	Select output from either 40 MHz clock or TDC reference strobe	1'b1	
25	Clk1G28_equ[1:0]	REG_07[1:0]	Equalization strength of the Rx for 1.28 GHz	2'b00	0x38
26	Clk1G28_invertData	REG_07[2]	1.28 GHz clock input Rx data invert	1'b0	
27	Clk1G28_enTermination	REG_07[3]	Enable 1.28 GHz clock input Rx termination	1'b1	
28	Clk1G28_setCommMode	REG_07[4]	Set 1.28 GHz clock input Rx common mode	1'b1	
29	Clk1G28_enableRx	REG_07[5]	Enable 1.28 GHz clock input Rx	1'b1	
30	Clk320M_equ[1:0]	REG_08[1:0]	Equalization strength of the Rx for 320 MHz	2'b00	0x38
31	Clk320M_invertData	REG_08[2]	320 MHz clock input Rx data invert	1'b0	
32	Clk320M_enTermination	REG_08[3]	Enable 320 MHz clock input Rx termination	1'b1	
33	Clk320M_setCommMode	REG_08[4]	Set 320 MHz clock input Rx common mode	1'b1	
34	Clk320M_enableRx	REG_08[5]	Enable 320 MHz clock input Rx	1'b1	

35	Clk40M_equ[1:0]	REG_09[1:0]	Equalization strength of the Rx for 40 MHz	2'b00	0x38
36	Clk40M_invertData	REG_09[2]	40 MHz clock input Rx data invert	1'b0	
37	Clk40M_enTermination	REG_09[3]	Enable 40 MHz clock input Rx termination	1'b1	
38	Clk40M_setCommMode	REG_09[4]	Set 40 MHz clock input Rx common mode	1'b1	
39	Clk40M_enableRx	REG_09[5]	Enable 40 MHz clock input Rx	1'b1	
40	QInj_equ[1:0]	REG_0A[1:0]	Equalization strength of the Rx for QInj	2'b00	0x38
41	QInj_invertData	REG_0A[2]	QInj input Rx data invert	1'b0	
42	QInj_enTermination	REG_0A[3]	Enable QInj input Rx termination	1'b1	
43	QInj_setCommMode	REG_0A[4]	Set QInj input Rx common mode	1'b1	
44	QInj_enableRx	REG_0A[5]	Enable QInj input Rx	1'b1	
45	CLKTO_AmplSel[2:0]	REG_0B[2:0]	CLKTO CML driver amplitude selection	3'b111	0x77
46	CLKTO_disBIAS[3]	REG_0B[3]	Disable CLKTO CML Driver Bias, high active	1'b0	
47	Dataout_AmplSel[2:0]	REG_0B[6:4]	Dataout output CML driver amplitude selection	3'b111	
48	Dataout_disBIAS[3]	REG_0B[7]	Disable Dataout CML Driver Bias, high active	1'b0	
49	CLSel[1:0]	REG_0C[1:0]	Select of load capacitance of the preamp first stage, 2'b00 $->$ 0 fC, 2'b01 $->$ 80 fC, 2'b10 $->$ 80 fC, 2'b11 $->$ 160 fC	2'b00	0xf8
50	RfSel[1:0]	REG_0C[3:2]	Feedback resistance selection, 2'b00 $->$ 20 kOhm, 2'b01 $->$ 10 kOhm, 2'b10 $->$ 5.7 kOhm, 2 b11 $->$ 4.4 kOhm	2'b10	
51	HysSel[3:0]	REG_0C[7:4]	Hysteresis voltage selection, 4'b0000 $->$ Vhys1, 4'b0001 $->$ Vhys2, 4'b0011 $->$ Vhys3, 4'b0111 $->$ Vhys4, 4'b1111 $->$ Vhys5, Vhys1>Vhys2>VHys3>Vhys4>Vhys5=0	4'b1111	
52	IBSel[2:0]	REG_0D[2:0]	Bias current selection of the input transistor in the preamp, 3'b000 $->$ I1, 3'b001, 3'b010, 3'b100 $->$ I2, 3'b011, 3'b110, 3'b101 $->$ I3, 3'b111 $->$ I4; I1>I2>I3>I4	3'b111	0x37
53	QSel[4:0]	REG_0D[7:3]	Select injected charge, from 1 fC (5'b00000) to 32 fC (5'b11111), Typical charge from LGAD sensor is 7 fC (7'b0000110)	5'b00110	
54	VTHIn[7:0]	REG_0E[7:0]	Threshold voltage input of Discriminator	8'b00000000	0x00
55	VTHIn[9:8]	REG_0F[1:0]	Threshold voltage input of Discriminator	2'b10	0x56
56	EN_QInj	REG_0F[2]	Enable the charge injection	1'b1	
57	EN_DiscriOut	REG_0F[3]	Enable Discriminator Output	1'b0	
58	Dis_VTHInOut	REG_0F[4]	Disable VTHIn Output	1'b1	
59	PD_DACDiscri	REG_0F[5]	Power down the DAC	1'b0	
60	OE_DMRO	REG_0F[6]	Output enable of DMRO	1'b1	