混合信号微控制器

查询样品: MSP430F5638, MSP430F5637, MSP430F5636, MSP430F5635, MSP430F5634, MSP430F5633, MSP430F5632, MSP430F5631, MSP430F5630

特性

- 低电源电压范围: **1.8V** 至 **3.6V**
- 超低功耗
  - 激活模式 **(AM)**:
    所有系统时钟激活:
    在 **8MHz**，**3.0V** 时为 **270μA/MHz**，闪存程序执行（典型值）
  - 待机模式 **(LPM3)**:
    带有晶振的看门狗且电源监控器可用、完全 **RAM** 保持、快速唤醒:
    2.2V 时为 **1.8μA**，**3.0V** 时为 **2.1μA**（典型值）
  - 关断 **RTC** 模式 **(LPM 3.5)**:
    关断模式，带有晶振的有源实时时钟:
    3.0V 时为 **1.1μA**（典型值）
  - 关断模式 **(LPM4.5)**:
    3.0V 时为 **0.3μA**（典型值）
- 在 **3 μs** 内从待机模式唤醒（典型值）
- **16** 位精简指令集 **(RISC)** 架构、扩展内存、高达 **20MHz** 的系统时钟
- 灵活的电源管理系统
  - 具有可编程经稳压内核电源电压的完全集成低压降稳压器 **(LDO)**
  - 电源电压监控、监视、和临时限电
- 统一时钟系统
  - 针对频率稳定的锁频环路 **(FLL)** 控制环路
  - 低功耗低频内部时钟源 **(VLO)**
  - 低频修整内部参照源 **(REFO)**
  - **32kHz** 晶体 **(XT1)**
  - 高达 **32MHz** 的高频晶振 **(XT2)**
- 四个 配有 **3**，**5** 或者 **7** 个捕捉/比较寄存器的 **16** 位寄存器
- **2** 个通用串行通信接口
  - **USCI_A0** 和 **USCI_A1** 每个都支持:
    - 增强型 **UART** 支持自动波特率检测
    - **IrDA** 编码器和解码器
    - 同步 **SPI**
  - **USCI_B0** 和 **USCI_B1**每个支持:
    - **I^2C**
    - 同步串行外设接口 **(SPI)**
- 全速通用串行总线 **(USB)**
  - 集成的 **USB -** 物理层 **(PHY)**
  - 集成 **3.3V** 和 **1.8V USB** 电源系统
  - 集成 **USB-** 锁相环 **(PLL)**
  - **8** 输入和 **8** 输出端点
- 具有内部共用基准、采样保持、和自动扫描功能的 **12** 位模数转换器 **(ADC)**
- 具有同步功能的双通道 **12** 位数模转换器 **(DAC)**
- 电压比较器
- 支持 **32** 位运算的硬件乘法器
- 串行板上编程，无需外部编程电压
- **6** 通道内部直接内存访问 **(DMA)**
- 具有电源电压后备开关的实时时钟模块
- 系列成员汇总于表 **1**
- 要获得完整的模块说明，请参阅《***MSP430x5xx*** *和* ***MSP430x6xx*** *系列产品用户指南》* **(**文献号：**SLAU208)**

应用范围

- 模拟和数字传感器系统
- 数字电机控制
- 遥控
- 恒温器
- 数字定时器
- 手持仪表

说明

德州仪器 （TI） MSP430™ 系列超低功率微控制器包含几个器件，这些器件特有针对多种应用的多种外设集。 这种架构与 5 种低功耗模式相组合，专为在便携式测量应用中延长电池使用寿命而优化。 该器件具有一个强大的 16 位 RISC CPU，16 位寄存器和有助于获得最大编码效率的常数发生器。 此数控振荡器 (DCO) 可在 3 µs（典型值）内实现从低功率模式唤醒至激活模式。

MSP430F563x 系列是配置有一个高性能 12 位模数转换器 (ADC)，比较器，两个通用串行通信接口 (USCI)，USB 2.0，一个硬件乘法器，DMA，四个 16 位定时器，一个带有报警功能的实时时钟和多达 74 个 I/O 引脚的微控制器。

这个器件的典型应用包括模拟和数字传感器系统、数字电机控制、遥控、恒温器、数字定时器、手持仪表。

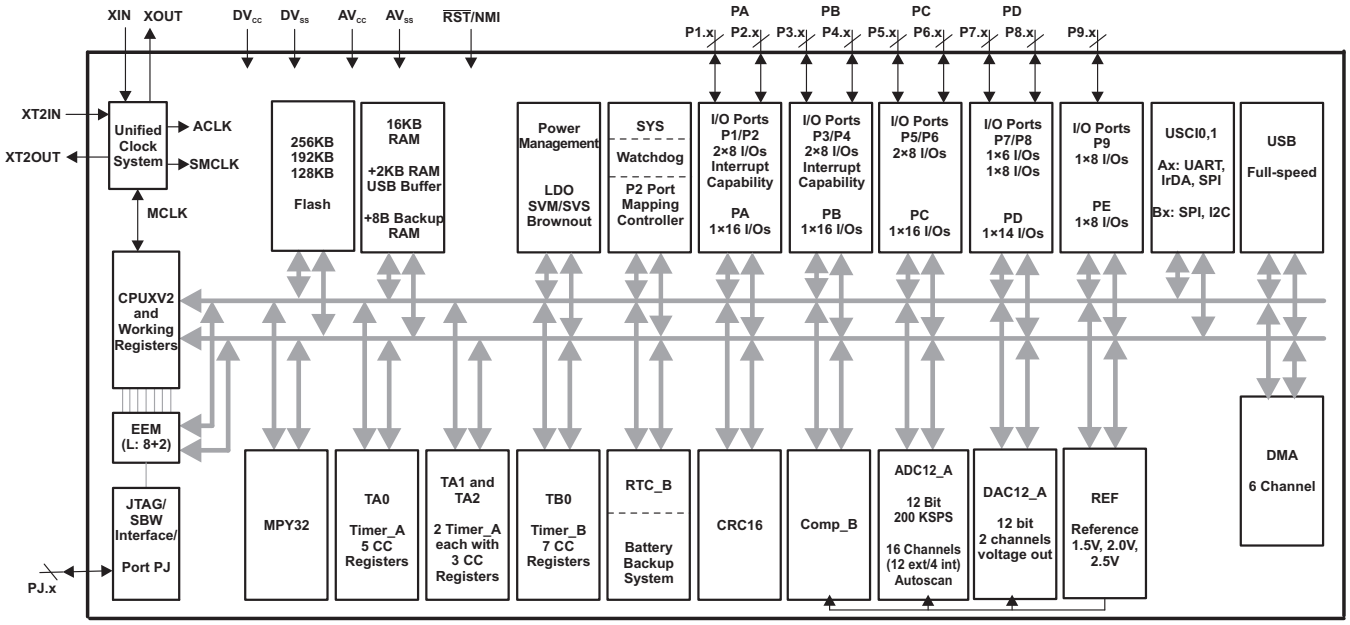
表 1总结了可用的产品成员。

表 1. 系列产品(1)(2)

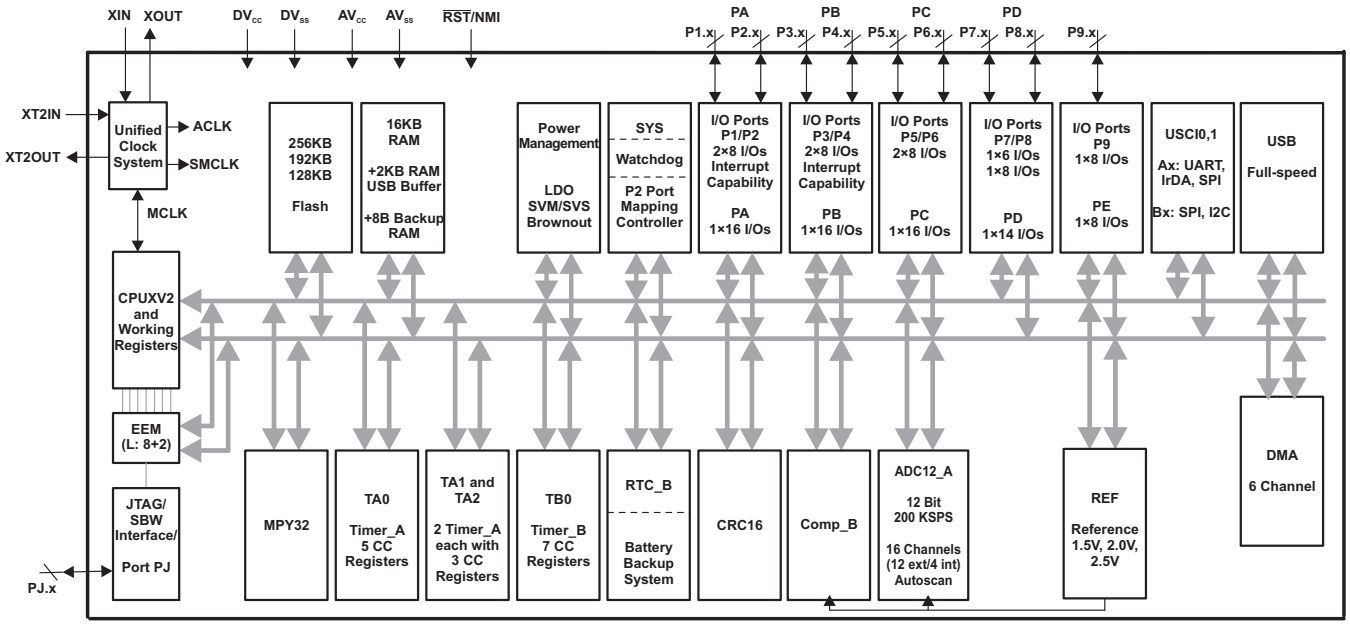
器件	闪存 (KB)	SRAM (KB)(3)	Timer_A(4)	Timer_B(5)	USCI		ADC12_A (Ch)	DAC12_A (Ch)	Comp_B (Ch)	I/O	封装类型
					通道 A：UART，IrDA，SPI	通道 B：SPI，I^2C					
MSP430F5638	256	16+2	5, 3, 3	7	2	2	12 个外部通道，4 个内部通道	2	12	74	100 PZ，113 ZQW
MSP430F5637	192	16+2	5, 3, 3	7	2	2	12 个外部通道，4 个内部通道	2	12	74	100 PZ，113 ZQW
MSP430F5636	128	16+2	5, 3, 3	7	2	2	12 个外部通道，4 个内部通道	2	12	74	100 PZ，113 ZQW
MSP430F5635	256	16+2	5, 3, 3	7	2	2	12 个外部通道，4 个内部通道	-	12	74	100 PZ，113 ZQW
MSP430F5634	192	16+2	5, 3, 3	7	2	2	12 个外部通道，4 个内部通道	-	12	74	100 PZ，113 ZQW
MSP430F5633	128	16+2	5, 3, 3	7	2	2	12 个外部通道，4 个内部通道	-	12	74	100 PZ，113 ZQW
MSP430F5632	256	16+2	5, 3, 3	7	2	2	-	-	12	74	100 PZ，113 ZQW
MSP430F5631	192	16+2	5, 3, 3	7	2	2	-	-	12	74	100 PZ，113 ZQW
MSP430F5630	128	16+2	5, 3, 3	7	2	2	-	-	12	74	100 PZ，113 ZQW

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者浏览 TI 网站 www.ti.com进行查询。
(2) 封装图示，标准包装数量，散热数据，符号以及印刷电路板 (PCB) 设计指南可从www.ti.com/packaging中获得。
(3) 列出的额外 2KB USB SRAM 在 USB 未使用时可被用作通用 SRAM。
(4) 序列中的每个数代表 Timer_A 的一个例示，并反映出其可使用的捕获/比较寄存器及脉宽调制 (PWM) 输出发生器的相关数量。 例如：一个 (3，5) 数列将代表 Timer_A 的两个例示，第一个例示和第二个例示分别具有 3 个和 5 个捕获/比较寄存器和 PWM 输出发生器。
(5) 序列中的每个数代表 Timer_B 的一个例示，并反映出其可使用的捕获/比较寄存器及 PWM 输出发生器的相关数量。 例如：一个 (3，5) 数列将代表 Timer_B 的两个例示，第一个例示和第二个例示分别具有 3 个和 5 个捕获/比较寄存器和 PWM 输出发生器。

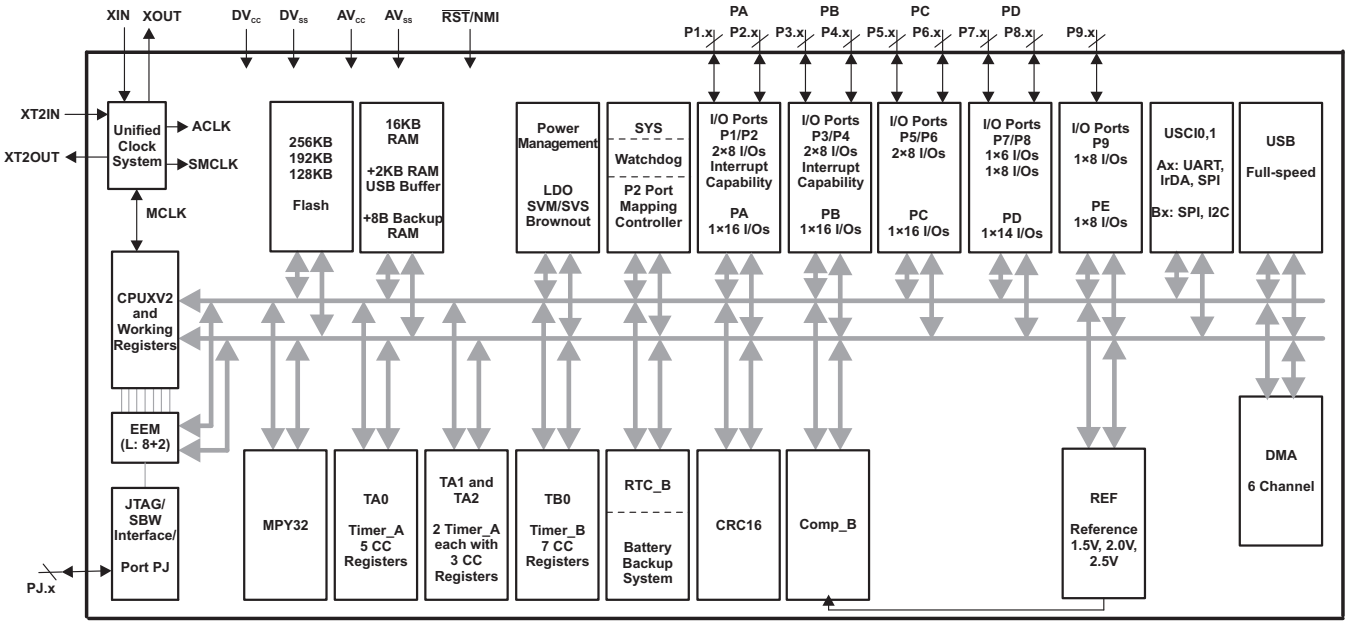
Functional Block Diagram, MSP430F5638, MSP430F5637, MSP430F5636



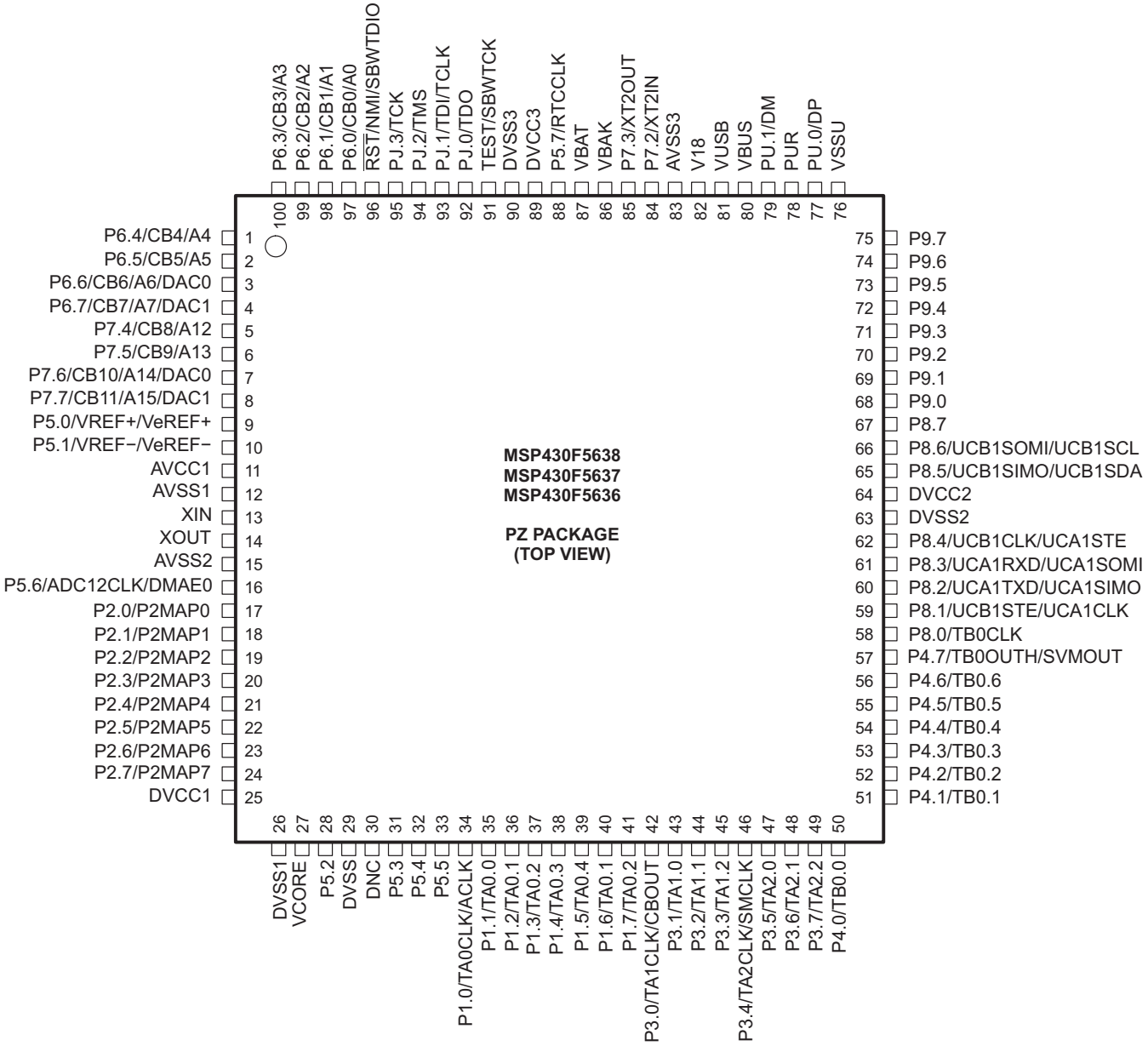
Functional Block Diagram, MSP430F5635, MSP430F5634, MSP430F5633



Functional Block Diagram, MSP430F5632, MSP430F5631, MSP430F5630

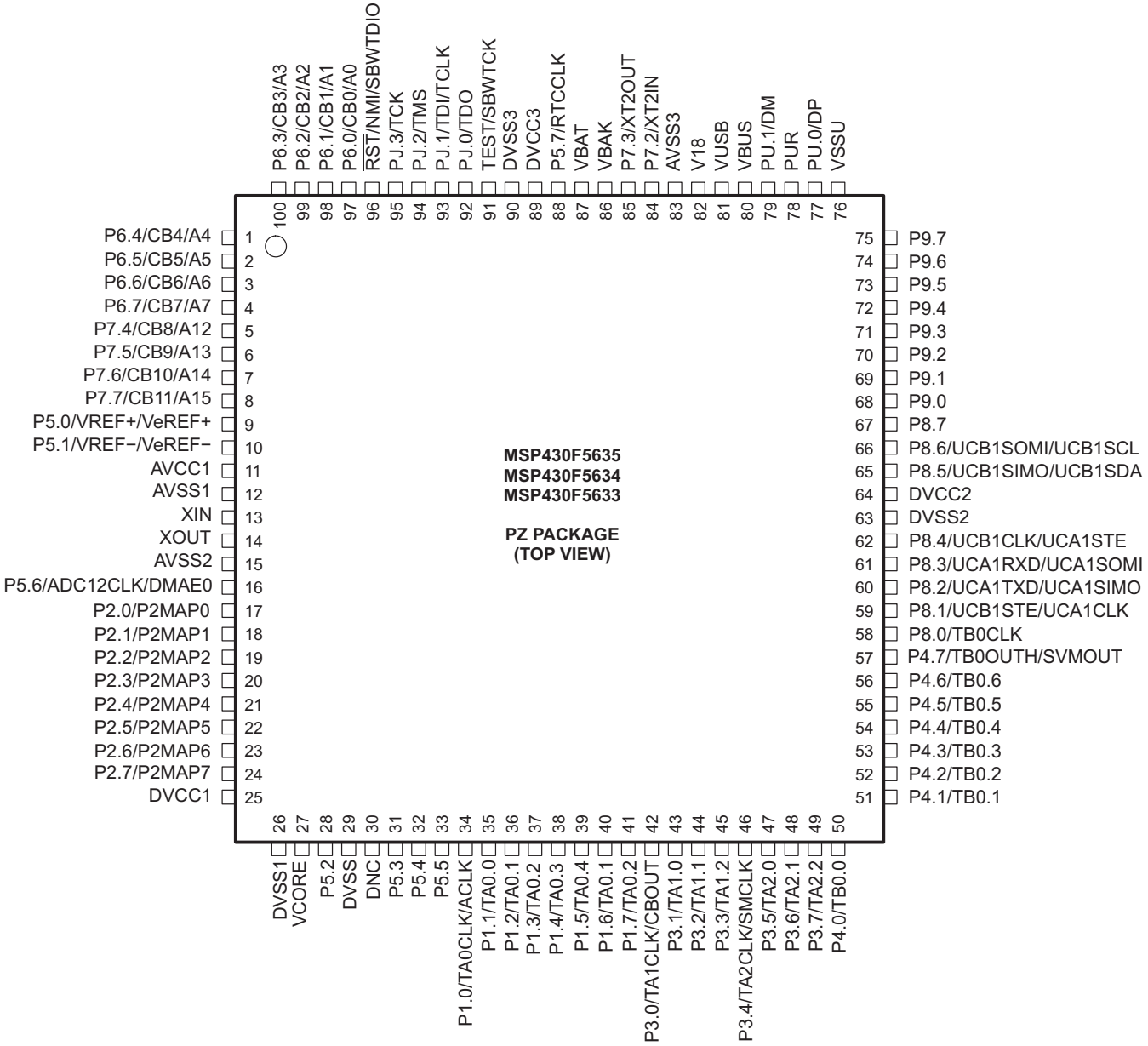


Pin Designation, MSP430F5638IPZ, MSP430F5637IPZ, MSP430F5636IPZ



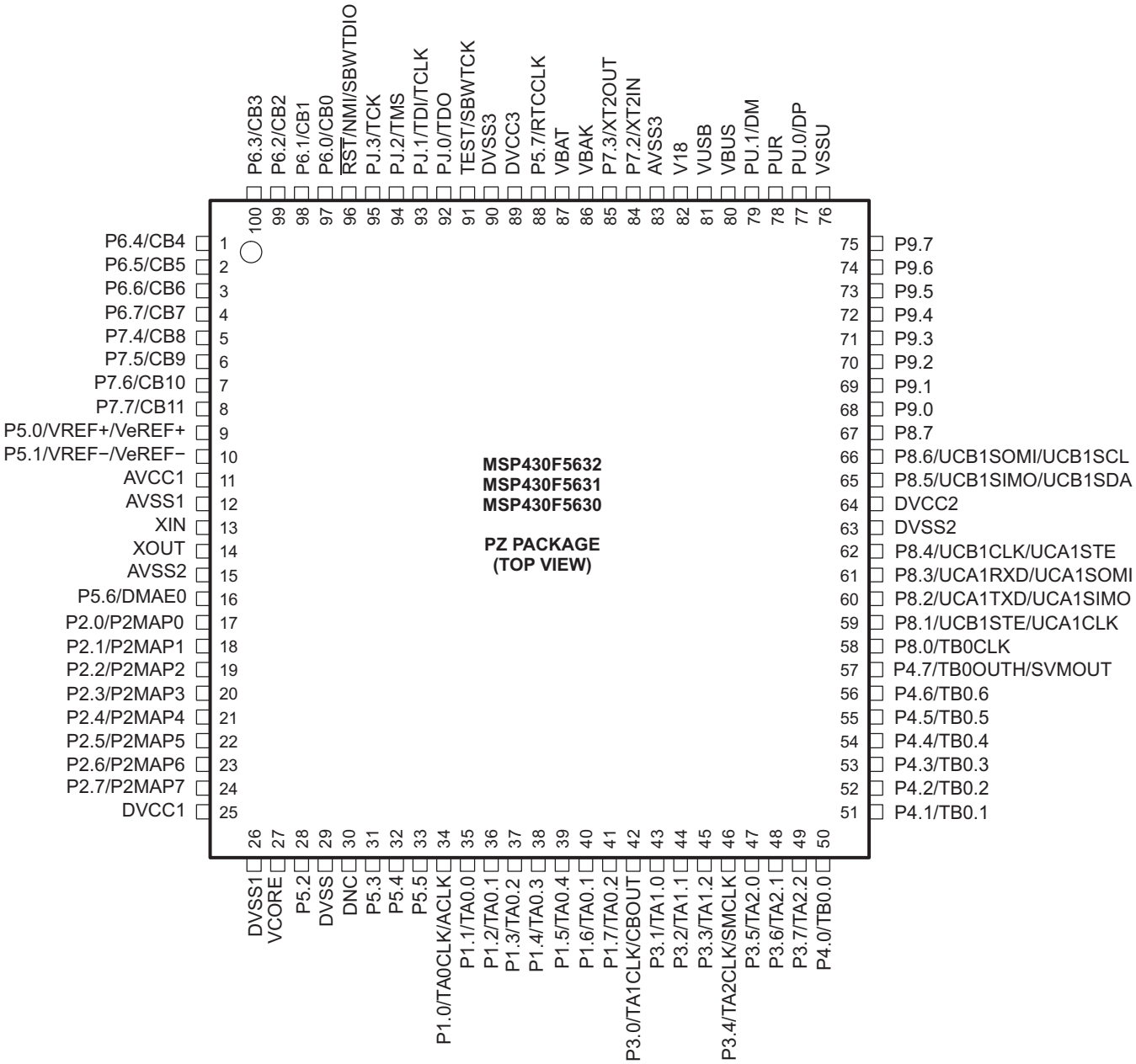
NOTE: DNC = Do not connect

Pin Designation, MSP430F5635IPZ, MSP430F5634IPZ, MSP430F5633IPZ



NOTE: DNC = Do not connect

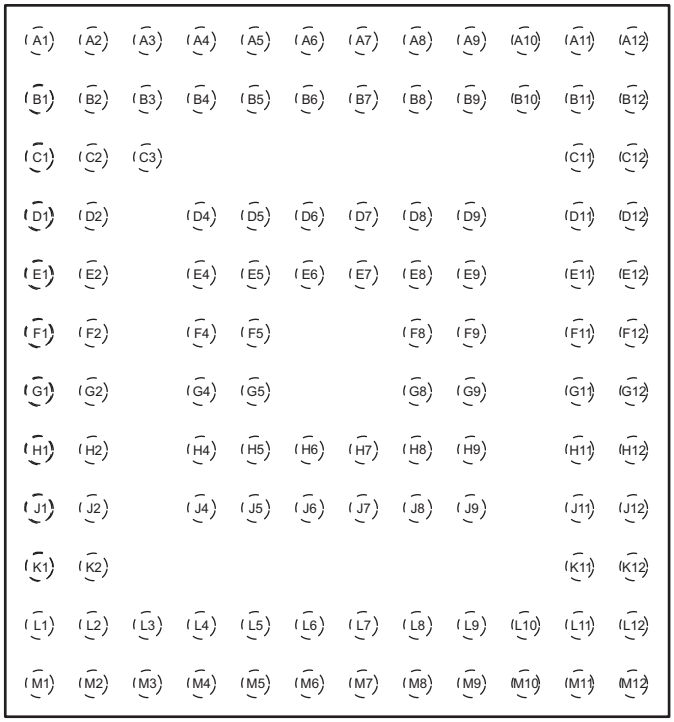
Pin Designation, MSP430F5632IPZ, MSP430F5631IPZ, MSP430F5630IPZ



NOTE: DNC = Do not connect

Pin Designation, MSP430F5638IZQW, MSP430F5637IZQW, MSP430F5636IZQW, MSP430F5635IZQW, MSP430F5634IZQW, MSP430F5633IZQW, MSP430F5632IZQW, MSP430F5631IZQW, MSP430F5630IZQW

ZQW PACKAGE
(TOP VIEW)



NOTE: For terminal assignments, see Table 2

Table 2. Terminal Functions

TERMINAL			I/O(1)	DESCRIPTION
NAME	NO.			
	PZ	ZQW		
P6.4/CB4/A4	1	A1	I/O	General-purpose digital I/O Comparator_B input CB4 Analog input A4 – ADC(not available on F5632, F5631, F5630 devices)
P6.5/CB5/A5	2	B2	I/O	General-purpose digital I/O Comparator_B input CB5 Analog input A5 – ADC(not available on F5632, F5631, F5630 devices)
P6.6/CB6/A6/DAC0	3	B1	I/O	General-purpose digital I/O Comparator_B input CB6 Analog input A6 – ADC (not available on F5632, F5631, F5630 devices) DAC12.0 output (not available on F5635, F5634, F5633, F5632, F5631, F5630 devices)
P6.7/CB7/A7/DAC1	4	C2	I/O	General-purpose digital I/O Comparator_B input CB7 Analog input A7 – ADC (not available on F5632, F5631, F5630 devices) DAC12.1 output (not available on F5635, F5634, F5633, F5632, F5631, F5630 devices)
P7.4/CB8/A12	5	C1	I/O	General-purpose digital I/O Comparator_B input CB8 Analog input A12 –ADC (not available on F5632, F5631, F5630 devices)
P7.5/CB9/A13	6	C3	I/O	General-purpose digital I/O Comparator_B input CB9 Analog input A13 – ADC (not available on F5632, F5631, F5630 devices)
P7.6/CB10/A14/DAC0	7	D2	I/O	General-purpose digital I/O Comparator_B input CB10 Analog input A14 – ADC (not available on F5632, F5631, F5630 devices) DAC12.0 output (not available on F5635, F5634, F5633, F5632, F5631, F5630 devices)
P7.7/CB11/A15/DAC1	8	D1	I/O	General-purpose digital I/O Comparator_B input CB11 Analog input A15 – ADC (not available on F5632, F5631, F5630 devices) DAC12.1 output (not available on F5635, F5634, F5633, F5632, F5631, F5630 devices)
P5.0/VREF+/VeREF+	9	D4	I/O	General-purpose digital I/O Output of reference voltage to the ADC Input for an external reference voltage to the ADC
P5.1/VREF-/VeREF-	10	E4	I/O	General-purpose digital I/O Negative terminal for the ADC's reference voltage for both sources, the internal reference voltage, or an external applied reference voltage
AVCC1	11	E1, E2		Analog power supply
AVSS1	12	F2		Analog ground supply
XIN	13	F1	I	Input terminal for crystal oscillator XT1
XOUT	14	G1	O	Output terminal of crystal oscillator XT1
AVSS2	15	G2		Analog ground supply

(1) I = input, O = output, N/A = not available on this package offering

Table 2. Terminal Functions (continued)

TERMINAL			I/O(1)	DESCRIPTION
NAME	NO.			
	PZ	ZQW		
P5.6/ADC12CLK/DMAE0	16	H1	I/O	General-purpose digital I/O Conversion clock output ADC (not available on F5632, F5631, F5630 devices) DMA external trigger input
P2.0/P2MAP0	17	G4	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_B0 SPI slave transmit enable; USCI_A0 clock input/output
P2.1/P2MAP1	18	H2	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_B0 SPI slave in/master out; USCI_B0 I2C data
P2.2/P2MAP2	19	J1	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_B0 SPI slave out/master in; USCI_B0 I2C clock
P2.3/P2MAP3	20	H4	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_B0 clock input/output; USCI_A0 SPI slave transmit enable
P2.4/P2MAP4	21	J2	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_A0 UART transmit data; USCI_A0 SPI slave in/master out
P2.5/P2MAP5	22	K1	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: USCI_A0 UART receive data; USCI_A0 slave out/master in
P2.6/P2MAP6	23	K2	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: no secondary function
P2.7/P2MAP7	24	L2	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: no secondary function
DVCC1	25	L1		Digital power supply
DVSS1	26	M1		Digital ground supply
VCORE(2)	27	M2		Regulated core power supply (internal use only, no external current loading)
P5.2	28	L3	I/O	General-purpose digital I/O
DVSS	29	M3		Digital ground supply
DNC	30	J4		Do not connect. It is strongly recommended to leave this terminal open.
P5.3	31	L4	I/O	General-purpose digital I/O
P5.4	32	M4	I/O	General-purpose digital I/O
P5.5	33	J5	I/O	General-purpose digital I/O
P1.0/TA0CLK/ACLK	34	L5	I/O	General-purpose digital I/O with port interrupt Timer TA0 clock signal TACLK input ACLK output (divided by 1, 2, 4, 8, 16, or 32)
P1.1/TA0.0	35	M5	I/O	General-purpose digital I/O with port interrupt Timer TA0 CCR0 capture: CCI0A input, compare: Out0 output BSL transmit output
P1.2/TA0.1	36	J6	I/O	General-purpose digital I/O with port interrupt Timer TA0 CCR1 capture: CCI1A input, compare: Out1 output BSL receive input
P1.3/TA0.2	37	H6	I/O	General-purpose digital I/O with port interrupt Timer TA0 CCR2 capture: CCI2A input, compare: Out2 output
P1.4/TA0.3	38	M6	I/O	General-purpose digital I/O with port interrupt Timer TA0 CCR3 capture: CCI3A input compare: Out3 output

(2) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C_{VCORE}.

Table 2. Terminal Functions (continued)

TERMINAL			I/O(1)	DESCRIPTION
NAME	NO.			
	PZ	ZQW		
P1.5/TA0.4	39	L6	I/O	General-purpose digital I/O with port interrupt Timer TA0 CCR4 capture: CCI4A input, compare: Out4 output
P1.6/TA0.1	40	J7	I/O	General-purpose digital I/O with port interrupt Timer TA0 CCR1 capture: CCI1B input, compare: Out1 output
P1.7/TA0.2	41	M7	I/O	General-purpose digital I/O with port interrupt Timer TA0 CCR2 capture: CCI2B input, compare: Out2 output
P3.0/TA1CLK/CBOUT	42	L7	I/O	General-purpose digital I/O with port interrupt Timer TA1 clock input Comparator_B output
P3.1/TA1.0	43	H7	I/O	General-purpose digital I/O with port interrupt Timer TA1 capture CCR0: CCI0A/CCI0B input, compare: Out0 output
P3.2/TA1.1	44	M8	I/O	General-purpose digital I/O with port interrupt Timer TA1 capture CCR1: CCI1A/CCI1B input, compare: Out1 output
P3.3/TA1.2	45	L8	I/O	General-purpose digital I/O with port interrupt Timer TA1 capture CCR2: CCI2A/CCI2B input, compare: Out2 output
P3.4/TA2CLK/SMCLK	46	J8	I/O	General-purpose digital I/O with port interrupt Timer TA2 clock input SMCLK output
P3.5/TA2.0	47	M9	I/O	General-purpose digital I/O with port interrupt Timer TA2 capture CCR0: CCI0A/CCI0B input, compare: Out0 output
P3.6/TA2.1	48	L9	I/O	General-purpose digital I/O with port interrupt Timer TA2 capture CCR1: CCI1A/CCI1B input, compare: Out1 output
P3.7/TA2.2	49	M10	I/O	General-purpose digital I/O with port interrupt Timer TA2 capture CCR2: CCI2A/CCI2B input, compare: Out2 output
P4.0/TB0.0	50	J9	I/O	General-purpose digital I/O with port interrupt Timer TB0 capture CCR0: CCI0A/CCI0B input, compare: Out0 output
P4.1/TB0.1	51	M11	I/O	General-purpose digital I/O with port interrupt Timer TB0 capture CCR1: CCI1A/CCI1B input, compare: Out1 output
P4.2/TB0.2	52	L10	I/O	General-purpose digital I/O with port interrupt Timer TB0 capture CCR2: CCI2A/CCI2B input, compare: Out2 output
P4.3/TB0.3	53	M12	I/O	General-purpose digital I/O with port interrupt Timer TB0 capture CCR3: CCI3A/CCI3B input, compare: Out3 output
P4.4/TB0.4	54	L12	I/O	General-purpose digital I/O with port interrupt Timer TB0 capture CCR4: CCI4A/CCI4B input, compare: Out4 output
P4.5/TB0.5	55	L11	I/O	General-purpose digital I/O with port interrupt Timer TB0 capture CCR5: CCI5A/CCI5B input, compare: Out5 output
P4.6/TB0.6	56	K11	I/O	General-purpose digital I/O with port interrupt Timer TB0 capture CCR6: CCI6A/CCI6B input, compare: Out6 output
P4.7/TB0OUTH/SVMOUT	57	K12	I/O	General-purpose digital I/O with port interrupt Timer TB0: Switch all PWM outputs high impedance SVM output
P8.0/TB0CLK	58	J11	I/O	General-purpose digital I/O Timer TB0 clock input

Table 2. Terminal Functions (continued)

TERMINAL			I/O(1)	DESCRIPTION
NAME	NO.			
	PZ	ZQW		
P8.1/UCB1STE/UCA1CLK	59	J12	I/O	General-purpose digital I/O USCI_B1 SPI slave transmit enable; USCI_A1 clock input/output
P8.2/UCA1TXD/UCA1SIMO	60	H11	I/O	General-purpose digital I/O USCI_A1 UART transmit data; USCI_A1 SPI slave in/master out
P8.3/UCA1RXD/UCA1SOMI	61	H12	I/O	General-purpose digital I/O USCI_A1 UART receive data; USCI_A1 SPI slave out/master in
P8.4/UCB1CLK/UCA1STE	62	G11	I/O	General-purpose digital I/O USCI_B1 clock input/output; USCI_A1 SPI slave transmit enable
DVSS2	63	G12		Digital ground supply
DVCC2	64	F12		Digital power supply
P8.5/UCB1SIMO/UCB1SDA	65	F11	I/O	General-purpose digital I/O USCI_B1 SPI slave in/master out; USCI_B1 I2C data
P8.6/UCB1SOMI/UCB1SCL	66	G9	I/O	General-purpose digital I/O USCI_B1 SPI slave out/master in; USCI_B1 I2C clock
P8.7	67	E12	I/O	General-purpose digital I/O
P9.0	68	E11	I/O	General-purpose digital I/O
P9.1	69	F9	I/O	General-purpose digital I/O
P9.2	70	D12	I/O	General-purpose digital I/O
P9.3	71	D11	I/O	General-purpose digital I/O
P9.4	72	E9	I/O	General-purpose digital I/O
P9.5	73	C12	I/O	General-purpose digital I/O
P9.6	74	C11	I/O	General-purpose digital I/O
P9.7	75	D9	I/O	General-purpose digital I/O
VSSU	76	B11 and B12		USB PHY ground supply
PU.0/DP	77	A12	I/O	General-purpose digital I/O - controlled by USB control register USB data terminal DP
PUR	78	B10	I/O	USB pullup resistor pin (open drain). The voltage level at the PUR pin is used to invoke the default USB BSL. Recommended 1-MΩ resistor to ground. See USB BSL for more information.
PU.1/DM	79	A11	I/O	General-purpose digital I/O - controlled by USB control register USB data terminal DM
VBUS	80	A10		USB LDO input (connect to USB power source)
VUSB	81	A9		USB LDO output
V18	82	B9		USB regulated power (internal use only, no external current loading)
AVSS3	83	A8		Analog ground supply
P7.2/XT2IN	84	B8	I/O	General-purpose digital I/O Input terminal for crystal oscillator XT2
P7.3/XT2OUT	85	B7	I/O	General-purpose digital I/O Output terminal of crystal oscillator XT2
VBAK	86	A7		Capacitor for backup subsystem. Do not load this pin externally. For capacitor values, see C_{BAK} in Recommended Operating Conditions.

Table 2. Terminal Functions (continued)

TERMINAL			I/O(1)	DESCRIPTION
NAME	NO.			
	PZ	ZQW		
VBAT	87	D8		Backup or secondary supply voltage. If backup voltage is not supplied, connect to DVCC externally.
P5.7/RTCCLK	88	D7	I/O	General-purpose digital I/O RTCCLK output
DVCC3	89	A6		Digital power supply
DVSS3	90	A5		Digital ground supply
TEST/SBWTCK	91	B6	I	Test mode pin; selects digital I/O on JTAG pins Spy-bi-wire input clock
PJ.0/TDO	92	B5	I/O	General-purpose digital I/O Test data output port
PJ.1/TDI/TCLK	93	A4	I/O	General-purpose digital I/O Test data input or test clock input
PJ.2/TMS	94	E7	I/O	General-purpose digital I/O Test mode select
PJ.3/TCK	95	D6	I/O	General-purpose digital I/O Test clock
$\overline{\text{RST}}$/NMI/SBWTDIO	96	A3	I/O	Reset input (active low)(3) Non-maskable interrupt input Spy-bi-wire data input/output
P6.0/CB0/A0	97	B4	I/O	General-purpose digital I/O Comparator_B input CB0 Analog input A0 – ADC (not available on F5632, F5631, F5630 devices)
P6.1/CB1/A1	98	B3	I/O	General-purpose digital I/O Comparator_B input CB1 Analog input A1 – ADC (not available on F5632, F5631, F5630 devices)
P6.2/CB2/A2	99	A2	I/O	General-purpose digital I/O Comparator_B input CB2 Analog input A2 – ADC (not available on F5632, F5631, F5630 devices)
P6.3/CB3/A3	100	D5	I/O	General-purpose digital I/O Comparator_B input CB3 Analog input A3 – ADC (not available on F5632, F5631, F5630 devices)
Reserved	N/A	E5, E6, E8, F4, F5, F8, G5, G8, H5, H8, H9		Reserved. It is recommended to connect to ground (DVSS, AVSS).

(3) When this pin is configured as reset, the intermal pullup resistor is enabled by default.

Development Tools Support

All MSP430™ microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at www.ti.com/msp430tools.

Hardware Features

See the *Code Composer Studio for MSP430 User's Guide* (SLAU157) for details on the available features.

MSP430 Architecture	4-Wire JTAG	2-Wire JTAG	Break-points (N)	Range Break-points	Clock Control	State Sequencer	Trace Buffer	LPMx.5 Debugging Support
MSP430Xv2	Yes	Yes	8	Yes	Yes	Yes	Yes	No

Recommended Hardware Options

Target Socket Boards

The target socket boards allow easy programming and debugging of the device using JTAG. They also feature header pin outs for prototyping. Target socket boards are orderable individually or as a kit with the JTAG programmer and debugger included. The following table shows the compatible target boards and the supported packages.

Package	Target Board and Programmer Bundle	Target Board Only
100-pin LQFP (PZ)	MSP-FET430U100USB	MSP-TS430PZ100USB

Experimenter Boards

Experimenter Boards and Evaluation kits are available for some MSP430 devices. These kits feature additional hardware components and connectivity for full system evaluation and prototyping. See www.ti.com/msp430tools for details.

Debugging and Programming Tools

Hardware programming and debugging tools are available from TI and from its third party suppliers. See the full list of available tools at www.ti.com/msp430tools.

Production Programmers

The production programmers expedite loading firmware to devices by programming several devices simultaneously.

Part Number	PC Port	Features	Provider
MSP-GANG	Serial and USB	Program up to eight devices at a time. Works with PC or standalone.	Texas Instruments

Recommended Software Options

Integrated Development Environments

Software development tools are available from TI or from third parties. Open source solutions are also available.

This device is supported by Code Composer Studio™ IDE (CCS).

MSP430Ware

MSP430Ware is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware also includes a high-level API called MSP430 Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware is available as a component of CCS or as a standalone package.

TI-RTOS

TI-RTOS is a complete real-time operating system for the MSP430 microcontrollers. It combines a real-time multitasking kernel SYS/BIOS with additional middleware components. TI-RTOS is available free of charge and provided with full source code.

MSP430 USB Developer's Package

MSP430 USB Developer's Package is an easy-to-use USB stack implementation for the MSP430 microcontrollers.

Command-Line Programmer

MSP430 Flasher is an open-source, shell-based interface for programming MSP430 microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP430 Flasher can be used to download binary files (.txt or .hex) files directly to the MSP430 Flash without the need for an IDE.

Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E Community

TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

Device and Development Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP430™ MCU devices and support tools. Each MSP430™ MCU commercial family member has one of two prefixes: MSP or XMS (for example, MSP430F5259). Texas Instruments recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

Support tool development evolutionary flow:

MSPX – Development-support product that has not yet completed Texas Instruments internal qualification testing.

MSP – Fully-qualified development-support product

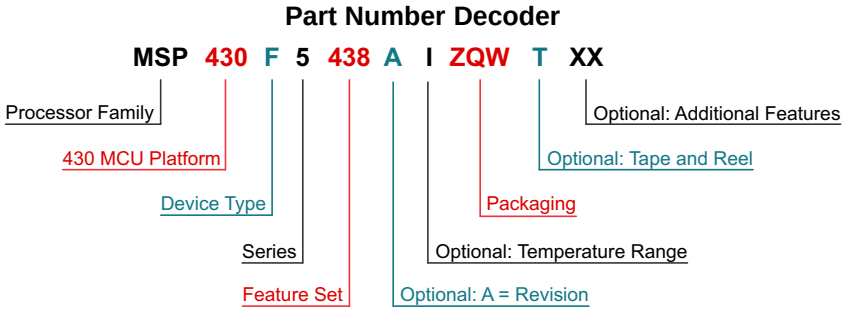
XMS devices and MSPX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZP) and temperature range (for example, T). Figure 1 provides a legend for reading the complete device name for any family member.



Processor Family	CC = Embedded RF Radio MSP = Mixed Signal Processor XMS = Experimental Silicon	
430 MCU Platform	TI's Low Power Microcontroller Platform	
Device Type	**Memory Type** C = ROM F = Flash FR = FRAM G = Flash (Value Line) L = No Nonvolatile Memory	**Specialized Application** AFE = Analog Front End BT = Preprogrammed with Bluetooth BQ = Contactless Power CG = ROM Medical FE = Flash Energy Meter FG = Flash Medical FW = Flash Electronic Flow Meter
Series	1 Series = Up to 8 MHz 2 Series = Up to 16 MHz 3 Series = Legacy 4 Series = Up to 16 MHz w/ LCD	5 Series = Up to 25 MHz 6 Series = Up to 25 MHz w/ LCD 0 = Low Voltage Series
Feature Set	Various Levels of Integration Within a Series	
Optional: A = Revision	N/A	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = -40°C to 85°C T = -40°C to 105°C	
Packaging	www.ti.com/packaging	
Optional: Tape and Reel	T = Small Reel (7 inch) R = Large Reel (11 inch) No Markings = Tube or Tray	
Optional: Additional Features	*-EP = Enhanced Product (-40°C to 105°C) *-HT = Extreme Temperature Parts (-55°C to 150°C)	

Figure 1. Device Nomenclature

Short-Form Description

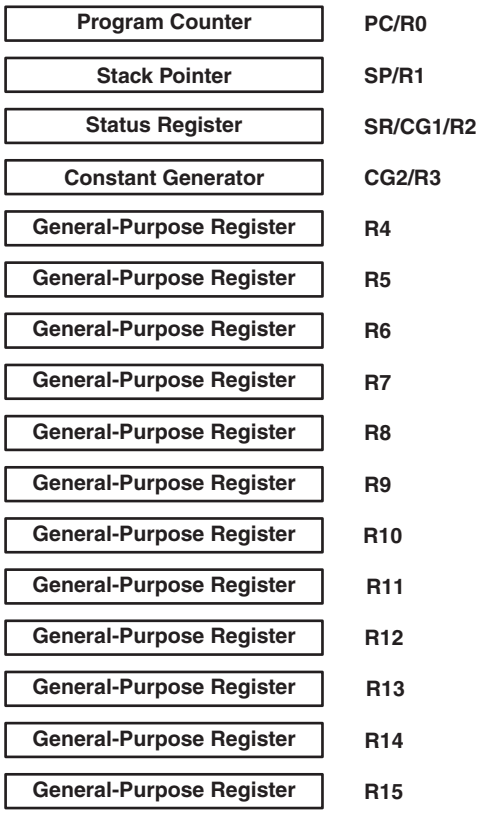
CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. Table 3 shows examples of the three types of instruction formats; Table 4 shows the address modes.

Table 3. Instruction Word Formats

INSTRUCTION WORD FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC → (TOS), R8 → PC
Relative jump, un/conditional	JNE	Jump-on-equal bit = 0

Table 4. Address Mode Descriptions

ADDRESS MODE	S(1)	D(1)	SYNTAX	EXAMPLE	OPERATION
Register	+	+	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	+	+	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	+	+	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	+	+	MOV &MEM, &TCDAT		M(MEM) → M(TCDAT)
Indirect	+		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect auto-increment	+		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	+		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source, D = destination

Operating Modes

The MSP430 has one active mode and seven software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following seven operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc generator is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 3.5 (LPM3.5)
  - Internal regulator disabled
  - No data retention
  - RTC enabled and clocked by low-frequency oscillator
  - Wakeup from $\overline{\text{RST}}$/NMI, RTC_B, P1, P2, P3, and P4
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No data retention
  - Wakeup from $\overline{\text{RST}}$/NMI, RTC_B, P1, P2, P3, and P4

Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 5. Interrupt Sources, Flags, and Vectors of MSP430F563x Configurations

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-Up, External Reset Watchdog Timeout, Key Violation Flash Memory Key Violation	WDTIFG, KEYV (SYSRSTIV)(1)(2)	Reset	0FFFEh	63, highest
System NMI PMM Vacant Memory Access JTAG Mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV)(1)	(Non)maskable	0FFFCh	62
User NMI NMI Oscillator Fault Flash Memory Access Violation	NMIIFG, OFIFG, ACCVIFG, BUSIFG (SYSUNIV)(1)(2)	(Non)maskable	0FFFAh	61
Comp_B	Comparator B interrupt flags (CBIV)(1)(3)	Maskable	0FFF8h	60
Timer TB0	TB0CCR0 CCIFG0(3)	Maskable	0FFF6h	59
Timer TB0	TB0CCR1 CCIFG1 to TB0CCR6 CCIFG6, TB0IFG (TBIV)(1) (3)	Maskable	0FFF4h	58
Watchdog Interval Timer Mode	WDTIFG	Maskable	0FFF2h	57
USCI_A0 Receive or Transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV)(1)(3)	Maskable	0FFF0h	56
USCI_B0 Receive or Transmit	UCB0RXIFG, UCB0TXIFG (UCB0IV)(1)(3)	Maskable	0FFEEh	55
ADC12_A(4)	ADC12IFG0 to ADC12IFG15 (ADC12IV)(1)(3)	Maskable	0FFECh	54
Timer TA0	TA0CCR0 CCIFG0(3)	Maskable	0FFEAh	53
Timer TA0	TA0CCR1 CCIFG1 to TA0CCR4 CCIFG4, TA0IFG (TA0IV)(1)(3)	Maskable	0FFE8h	52
USB_UBM	USB interrupts (USBIV)(1)(3)	Maskable	0FFE6h	51
DMA	DMA0IFG, DMA1IFG, DMA2IFG, DMA3IFG, DMA4IFG, DMA5IFG (DMAIV)(1)(3)	Maskable	0FFE4h	50
Timer TA1	TA1CCR0 CCIFG0(3)	Maskable	0FFE2h	49
Timer TA1	TA1CCR1 CCIFG1 to TA1CCR2 CCIFG2, TA1IFG (TA1IV)(1)(3)	Maskable	0FFE0h	48
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV)(1) (3)	Maskable	0FFDEh	47
USCI_A1 Receive or Transmit	UCA1RXIFG, UCA1TXIFG (UCA1IV)(1)(3)	Maskable	0FFDCh	46
USCI_B1 Receive or Transmit	UCB1RXIFG, UCB1TXIFG (UCB1IV)(1)(3)	Maskable	0FFDAh	45
I/O Port P2	P2IFG.0 to P2IFG.7 (P2IV)(1) (3)	Maskable	0FFD8h	44
Reserved	Reserved	Maskable	0FFD6h	43
RTC_B	RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG, RTCOFIFG (RTCIV)(1)(3)	Maskable	0FFD4h	42
DAC12_A(5)	DAC12_0IFG, DAC12_1IFG(1)(3)	Maskable	0FFD2h	41
Timer TA2	TA2CCR0 CCIFG0(3)	Maskable	0FFD0h	40
Timer TA2	TA2CCR1 CCIFG1 to TA2CCR2 CCIFG2, TA2IFG (TA2IV)(1)(3)	Maskable	0FFCEh	39
I/O Port P3	P3IFG.0 to P3IFG.7 (P3IV)(1)(3)	Maskable	0FFCCh	38
I/O Port P4	P4IFG.0 to P4IFG.7 (P4IV)(1)(3)	Maskable	0FFCAh	37

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.
(Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(3) Interrupt flags are located in the module.
(4) Only on devices with peripheral module ADC12_A, otherwise reserved.
(5) Only on devices with peripheral module DAC12_A, otherwise reserved.

Table 5. Interrupt Sources, Flags, and Vectors of MSP430F563x Configurations (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Reserved	Reserved(6)		0FFC8h	36
			⋮	⋮
			0FF80h	0, lowest

(6) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatability with other devices, it is recommended to reserve these locations.

Memory Organization

Table 6. Memory Organization(1)(2)

		MSP430F5636 MSP430F5633 MSP430F5630	MSP430F5637 MSP430F5634 MSP430F5631	MSP430F5638 MSP430F5635 MSP430F5632
Memory (flash) Main: interrupt vector	Total Size	128KB 00FFFFh–00FF80h	192KB 00FFFFh–00FF80h	256KB 00FFFFh–00FF80h
Main: code memory	Bank 3	N/A	N/A	64 KB 047FFF-038000h
	Bank 2	N/A	64 KB 037FFF-028000h	64 KB 037FFF-028000h
	Bank 1	64 KB 027FFF-018000h	64 KB 027FFF-018000h	64 KB 027FFF-018000h
	Bank 0	64 KB 017FFF-008000h	64 KB 017FFF-008000h	64 KB 017FFF-008000h
RAM	Sector 3	4 KB 0063FFh–005400h	4 KB 0063FFh–005400h	4 KB 0063FFh–005400h
	Sector 2	4 KB 0053FFh–004400h	4 KB 0053FFh–004400h	4 KB 0053FFh–004400h
	Sector 1	4 KB 0043FFh–003400h	4 KB 0043FFh–003400h	4 KB 0043FFh–003400h
	Sector 0	4 KB 0033FFh–002400h	4 KB 0033FFh–002400h	4 KB 0033FFh–002400h
USB RAM(3)	Size RAM	2KB 0023FFh-001C00h	2KB 0023FFh-001C00h	2KB 0023FFh-001C00h
Information memory (flash)	Info A	128 B 0019FFh–001980h	128 B 0019FFh–001980h	128 B 0019FFh–001980h
	Info B	128 B 00197Fh–001900h	128 B 00197Fh–001900h	128 B 00197Fh–001900h
	Info C	128 B 0018FFh–001880h	128 B 0018FFh–001880h	128 B 0018FFh–001880h
	Info D	128 B 00187Fh–001800h	128 B 00187Fh–001800h	128 B 00187Fh–001800h
Bootstrap loader (BSL) memory (flash)	BSL 3	512 B 0017FFh–001600h	512 B 0017FFh–001600h	512 B 0017FFh–001600h
	BSL 2	512 B 0015FFh–001400h	512 B 0015FFh–001400h	512 B 0015FFh–001400h
	BSL 1	512 B 0013FFh–001200h	512 B 0013FFh–001200h	512 B 0013FFh–001200h
	BSL 0	512 B 0011FFh–001000h	512 B 0011FFh–001000h	512 B 0011FFh–001000h
Peripherals	Size	4KB 000FFFh–000000h	4KB 000FFFh–000000h	4KB 000FFFh–000000h

(1) N/A = Not available.
(2) Backup RAM is accessed via the control registers BAKMEM0, BAKMEM1, BAKMEM2, and BAKMEM3.
(3) USB RAM can be used as general purpose RAM when not used for USB operation.

Bootstrap Loader (BSL)

The BSL enables users to program the flash memory or RAM using various serial interfaces. Access to the device memory via the BSL is protected by an user-defined password. For complete description of the features of the BSL and its implementation, see *MSP430 Programming Via the Bootstrap Loader (BSL)* (SLAU319).

USB BSL

All devices come pre-programmed with the USB BSL. Use of the USB BSL requires external access to the six pins shown in Table 7. In addition to these pins, the application must support external components necessary for normal USB operation; for example, the proper crystal on XT2IN and XT2OUT or proper decoupling.

Table 7. USB BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
PU.0/DP	USB data terminal DP
PU.1/DM	USB data terminal DM
PUR	USB pullup resistor terminal
VBUS	USB bus power supply
VSSU	USB ground supply

NOTE

The default USB BSL evaluates the logic level of the PUR pin after a BOR reset. If it is pulled high externally, then the BSL is invoked. Therefore, unless the application is invoking the BSL, it is important to keep PUR pulled low after a BOR reset, even if BSL or USB is never used. Applying a 1-MΩ resistor to ground is recommended.

UART BSL

A UART BSL is also available that can be programmed by the user into the BSL memory by replacing the pre-programmed, factory supplied, USB BSL. Use of the UART BSL requires external access to the six pins shown in Table 8.

Table 8. UART BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P1.1	Data transmit
P1.2	Data receive
VCC	Power supply
VSS	Ground supply

JTAG Operation

JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}$/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in Table 9. For further details on interfacing to development tools and device programmers, see the *MSP430(tm) Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

Table 9. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/TCK	IN	JTAG clock input
PJ.2/TMS	IN	JTAG state control
PJ.1/TDI/TCLK	IN	JTAG data input, TCLK input
PJ.0/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
$\overline{\text{RST}}$/NMI/SBWTDIO	IN	External reset
VCC		Power supply
VSS		Ground supply

Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in Table 10. For further details on interfacing to development tools and device programmers, see the *MSP430(tm) Hardware Tools User's Guide* (SLAU278). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* (SLAU320).

Table 10. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
$\overline{\text{RST}}$/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input/output
VCC		Power supply
VSS		Ground supply

Flash Memory (Link to User's Guide)

The flash memory can be programmed via the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

RAM Memory (Link to User's Guide)

The RAM memory is made up of n sectors. Each sector can be completely powered down to save leakage, however all data is lost. Features of the RAM memory include:

- RAM memory has n sectors. The size of a sector can be found in Memory Organization.
- Each sector 0 to n can be complete disabled, however data retention is lost.
- Each sector 0 to n automatically enters low power retention mode when possible.
- For devices that contain USB memory, the USB memory can be used as normal RAM if USB is not required.

Backup RAM Memory

The backup RAM provides a limited number of bytes of RAM that are retained during LPMx.5 and during operation from a backup supply if the Battery Backup System module is implemented.

There are 8 bytes of Backup RAM available on MSP430F563x. It can be wordwise accessed via the control registers BAKMEM0, BAKMEM1, BAKMEM2, and BAKMEM3.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

Digital I/O (Link to User's Guide)

There are up to nine 8-bit I/O ports implemented: P1 through P6, P8, and P9 are complete, P7 contains six individual I/O ports, and PJ contains four individual I/O ports.

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Programmable drive strength on all ports.
- Edge-selectable interrupt input capability for all the eight bits of ports P1, P2, P3, and P4.
- Read/write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P9) or word-wise in pairs (PA through PD).

Port Mapping Controller (Link to User's Guide)

The port mapping controller allows the flexible and reconfigurable mapping of digital functions to port P2.

Table 11. Port Mapping, Mnemonics and Functions

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
0	PM_NONE	None	DV_{SS}
1	PM_CBOUT	-	Comparator_B output
	PM_TB0CLK	Timer TB0 clock input	-
2	PM_ADC12CLK	-	ADC12CLK
	PM_DMAE0	DMAE0 Input	-
3	PM_SVMOUT	-	SVM output
	PM_TB0OUTH	Timer TB0 high impedance input TB0OUTH	-
4	PM_TB0CCR0B	Timer TB0 CCR0 capture input CCI0B	Timer TB0: TB0.0 compare output Out0
5	PM_TB0CCR1B	Timer TB0 CCR1 capture input CCI1B	Timer TB0: TB0.1 compare output Out1
6	PM_TB0CCR2B	Timer TB0 CCR2 capture input CCI2B	Timer TB0: TB0.2 compare output Out2
7	PM_TB0CCR3B	Timer TB0 CCR3 capture input CCI3B	Timer TB0: TB0.3 compare output Out3
8	PM_TB0CCR4B	Timer TB0 CCR4 capture input CCI4B	Timer TB0: TB0.4 compare output Out4
9	PM_TB0CCR5B	Timer TB0 CCR5 capture input CCI5B	Timer TB0: TB0.5 compare output Out5
10	PM_TB0CCR6B	Timer TB0 CCR6 capture input CCI6B	Timer TB0: TB0.6 compare output Out6
11	PM_UCA0RXD	USCI_A0 UART RXD (Direction controlled by USCI - input)	
	PM_UCA0SOMI	USCI_A0 SPI slave out master in (direction controlled by USCI)	
12	PM_UCA0TXD	USCI_A0 UART TXD (Direction controlled by USCI - output)	
	PM_UCA0SIMO	USCI_A0 SPI slave in master out (direction controlled by USCI)	
13	PM_UCA0CLK	USCI_A0 clock input/output (direction controlled by USCI)	
	PM_UCB0STE	USCI_B0 SPI slave transmit enable (direction controlled by USCI - input)	
14	PM_UCB0SOMI	USCI_B0 SPI slave out master in (direction controlled by USCI)	
	PM_UCB0SCL	USCI_B0 I2C clock (open drain and direction controlled by USCI)	
15	PM_UCB0SIMO	USCI_B0 SPI slave in master out (direction controlled by USCI)	
	PM_UCB0SDA	USCI_B0 I2C data (open drain and direction controlled by USCI)	
16	PM_UCB0CLK	USCI_B0 clock input/output (direction controlled by USCI)	
	PM_UCA0STE	USCI_A0 SPI slave transmit enable (direction controlled by USCI - input)	
17	PM_MCLK	-	MCLK
18	Reserved	Reserved for test purposes. Do not use this setting.	

Table 11. Port Mapping, Mnemonics and Functions (continued)

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
19	Reserved	Reserved for test purposes. Do not use this setting.	
20-30	Reserved	None	DVSS
31 (0FFh)(1)	PM_ANALOG	Disables the output driver and the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals.	

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide and the upper bits are ignored, which results in a read out value of 31.

Table 12. Default Mapping

PIN	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
P2.0/P2MAP0	PM_UCB0STE, PM_UCA0CLK	USCI_B0 SPI slave transmit enable (direction controlled by USCI - input), USCI_A0 clock input/output (direction controlled by USCI)	
P2.1/P2MAP1	PM_UCB0SIMO, PM_UCB0SDA	USCI_B0 SPI slave in master out (direction controlled by USCI), USCI_B0 I2C data (open drain and direction controlled by USCI)	
P2.2/P2MAP2	PM_UCB0SOMI, PM_UCB0SCL	USCI_B0 SPI slave out master in (direction controlled by USCI), USCI_B0 I2C clock (open drain and direction controlled by USCI)	
P2.3/P2MAP3	PM_UCB0CLK, PM_UCA0STE	USCI_B0 clock input/output (direction controlled by USCI), USCI_A0 SPI slave transmit enable (direction controlled by USCI - input)	
P2.4/P2MAP4	PM_UCA0TXD, PM_UCA0SIMO	USCI_A0 UART TXD (direction controlled by USCI - output), USCI_A0 SPI slave in master out (direction controlled by USCI)	
P2.5/P2MAP5	PM_UCA0RXD, PM_UCA0SOMI	USCI_A0 UART RXD (direction controlled by USCI - input), USCI_A0 SPI slave out master in (direction controlled by USCI)	
P2.6/P2MAP6	PM_NONE	-	DVSS
P2.7/P2MAP7	PM_NONE	-	DVSS

Oscillator and System Clock (Link to User's Guide)

The clock system in the MSP430F563x family of devices is supported by the Unified Clock System (UCS) module that includes support for a 32-kHz watch crystal oscillator (in XT1 LF mode; XT1 HF mode is not supported), an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), an integrated internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator XT2. The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the watch crystal frequency. The internal DCO provides a fast turn-on clock source and stabilizes in 3 µs (typical). The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32-kHz watch crystal (XT1), a high-frequency crystal (XT2), the internal low-frequency oscillator (VLO), the trimmed low-frequency oscillator (REFO), or the internal digitally-controlled oscillator DCO.
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

Power Management Module (PMM) (Link to User's Guide)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS and SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

Hardware Multiplier (MPY) (Link to User's Guide)

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations.

Real-Time Clock (RTC_B) (Link to User's Guide)

The RTC_B module can be configured for real-time clock (RTC) or calendar mode providing seconds, minutes, hours, day of week, day of month, month, and year. Calendar mode integrates an internal calendar which compensates for months with less than 31 days and includes leap year correction. The RTC_B also supports flexible alarm functions and offset-calibration hardware. The implementation on this device supports operation in LPM3.5 mode and operation from a backup supply.

Watchdog Timer (WDT_A) (Link to User's Guide)

The primary function of the watchdog timer (WDT_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

System Module (SYS) (Link to User's Guide)

The SYS module handles many of the system functions within the device. These include power-on reset and power-up clear handling, NMI source selection and management, reset interrupt vector generators, bootstrap loader entry mechanisms, and configuration management (device descriptors). SYS also includes a data exchange mechanism via JTAG called a JTAG mailbox that can be used in the application.

Table 13. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	INTERRUPT EVENT	WORD ADDRESS	OFFSET	PRIORITY
SYSRSTIV, System Reset	No interrupt pending	019Eh	00h	
	Brownout (BOR)		02h	Highest
	RST/NMI (BOR)		04h	
	DoBOR (BOR)		06h	
	LPM3.5 or LPM4.5 wakeup (BOR)		08h	
	Security violation (BOR)		0Ah	
	SVSL (POR)		0Ch	
	SVSH (POR)		0Eh	
	SVML_OVP (POR)		10h	
	SVMH_OVP (POR)		12h	
	DoPOR (POR)		14h	
	WDT timeout (PUC)		16h	
	WDT key violation (PUC)		18h	
	KEYV flash key violation (PUC)		1Ah	
	Reserved		1Ch	
	Peripheral area fetch (PUC)		1Eh	
	PMM key violation (PUC)		20h	
	Reserved		22h to 3Eh	Lowest

Table 13. System Module Interrupt Vector Registers (continued)

INTERRUPT VECTOR REGISTER	INTERRUPT EVENT	WORD ADDRESS	OFFSET	PRIORITY
SYSSNIV, System NMI	No interrupt pending	019Ch	00h	
	SVMLIFG		02h	Highest
	SVMHIFG		04h	
	DLYLIFG		06h	
	DLYHIFG		08h	
	VMAIFG		0Ah	
	JMBINIFG		0Ch	
	JMBOUTIFG		0Eh	
	SVMLVLRIFG		10h	
	SVMHVLRIFG		12h	
	Reserved		14h to 1Eh	Lowest
SYSUNIV, User NMI	No interrupt pending	019Ah	00h	
	NMIFG		02h	Highest
	OFIFG		04h	
	ACCVIFG		06h	
	BUSIFG		08h	
	Reserved		0Ah to 1Eh	Lowest
SYSBERRIV, Bus Error	No interrupt pending	0198h	00h	
	USB wait state timeout		02h	Highest
	Reserved		04h to 1Eh	Lowest

DMA Controller (Link to User's Guide)

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC12_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

The USB timestamp generator also uses the channel 0, 1, and 2 DMA trigger assignments described in Table 14.

Table 14. DMA Trigger Assignments(1)

Trigger	Channel					
	0	1	2	3	4	5
0	DMAREQ					
1	TA0CCR0 CCIFG					
2	TA0CCR2 CCIFG					
3	TA1CCR0 CCIFG					
4	TA1CCR2 CCIFG					
5	TA2CCR0 CCIFG					
6	TA2CCR2 CCIFG					
7	TBCCR0 CCIFG					
8	TBCCR2 CCIFG					
9	Reserved					
10	Reserved					
11	Reserved					
12	Reserved					
13	Reserved					
14	Reserved					
15	Reserved					
16	UCA0RXIFG					
17	UCA0TXIFG					
18	UCB0RXIFG					
19	UCB0TXIFG					
20	UCA1RXIFG					
21	UCA1TXIFG					
22	UCB1RXIFG					
23	UCB1TXIFG					
24	ADC12IFGx(2)					
25	DAC12_0IFG(3)					
26	DAC12_1IFG(3)					
27	USB FNRXD					
28	USB ready					
29	MPY ready					
30	DMA5IFG	DMA0IFG	DMA1IFG	DMA2IFG	DMA3IFG	DMA4IFG
31	DMAE0					

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers will not cause any DMA trigger event when selected.
(2) Only on devices with peripheral module ADC12_A. Reserved on devices without ADC.
(3) Only on devices with peripheral module DAC12_A. Reserved on devices without DAC.

Universal Serial Communication Interface (USCI) (Links to User's Guide: UART Mode, SPI Mode, I2C Mode)

The USCI modules are used for serial data communication. The USCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA. Each USCI module contains two portions, A and B.

The USCI_An module provides support for SPI (3 or 4 pin), UART, enhanced UART, or IrDA.

The USCI_Bn module provides support for SPI (3 or 4 pin) or I2C.

The MSP430F563x series includes two complete USCI modules (n = 0 to 1).

Timer TA0 (Link to User's Guide)

Timer TA0 is a 16-bit timer/counter (Timer_A type) with five capture/compare registers. It can support multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 15. Timer TA0 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PZ	ZQW						PZ	ZQW
34-P1.0	L5-P1.0	TA0CLK	TACLK	Timer	NA	NA		
		ACLK	ACLK					
		SMCLK	SMCLK					
34-P1.0	L5-P1.0	TA0CLK	$\overline{\text{TACLK}}$					
35-P1.1	M5-P1.1	TA0.0	CCI0A	CCR0	TA0	TA0.0	35-P1.1	M5-P1.1
		DV_{SS}	CCI0B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
36-P1.2	J6-P1.2	TA0.1	CCI1A	CCR1	TA1	TA0.1	36-P1.2	J6-P1.2
40-P1.6	J7-P1.6	TA0.1	CCI1B				40-P1.6	J7-P1.6
		DV_{SS}	GND				ADC12_A (internal)(1) ADC12SHSx = {1}	
		DV_{CC}	V_{CC}					
37-P1.3	H6-P1.3	TA0.2	CCI2A	CCR2	TA2	TA0.2	37-P1.3	H6-P1.3
41-P1.7	M7-P1.7	TA0.2	CCI2B				41-P1.7	M7-P1.7
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
38-P1.4	M6-P1.4	TA0.3	CCI3A	CCR3	TA3	TA0.3	38-P1.4	M6-P1.4
		DV_{SS}	CCI3B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
39-P1.5	L6-P1.5	TA0.4	CCI4A	CCR4	TA4	TA0.4	39-P1.5	L6-P1.5
		DV_{SS}	CCI4B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

(1) Only on devices with peripheral module ADC12_A.

Timer TA1 (Link to User's Guide)

Timer TA1 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. It supports multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 16. Timer TA1 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PZ	ZQW						PZ	ZQW
42-P3.0	L7-P3.0	TA1CLK	TACLK	Timer	NA	NA		
		ACLK	ACLK					
		SMCLK	SMCLK					
42-P3.0	L7-P3.0	TA1CLK	$\overline{\text{TACLK}}$					
43-P3.1	H7-P3.1	TA1.0	CCI0A	CCR0	TA0	TA1.0	43-P3.1	H7-P3.1
		DV_{SS}	CCI0B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
44-P3.2	M8-P3.2	TA1.1	CCI1A	CCR1	TA1	TA1.1	44-P3.2	M8-P3.2
		CBOUT (internal)	CCI1B				DAC12_A[1] DAC12_0, DAC12_1 (internal)	
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
45-P3.3	L8-P3.3	TA1.2	CCI2A	CCR2	TA2	TA1.2	45-P3.3	L8-P3.3
		ACLK (internal)	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

(1) Only on devices with peripheral module DAC12_A.

Timer TA2 (Link to User's Guide)

Timer TA2 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. It supports multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 17. Timer TA2 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PZ	ZQW						PZ	ZQW
46-P3.4	J8-P3.4	TA2CLK	TACLK	Timer	NA	NA		
		ACLK	ACLK					
		SMCLK	SMCLK					
46-P3.4	J8-P3.4	TA2CLK	$\overline{\text{TACLK}}$					
47-P3.5	M9-P3.5	TA2.0	CCI0A	CCR0	TA0	TA2.0	47-P3.5	M9-P3.5
		DV_{SS}	CCI0B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
48-P3.6	L9-P3.6	TA2.1	CCI1A	CCR1	TA1	TA2.1	48-P3.6	L9-P3.6
		CBOUT (internal)	CCI1B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
49-P3.7	M10-P3.7	TA2.2	CCI2A	CCR2	TA2	TA2.2	49-P3.7	M10-P3.7
		ACLK (internal)	CCI2B					
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

Timer TB0 (Link to User's Guide)

Timer TB0 is a 16-bit timer/counter (Timer_B type) with seven capture/compare registers. It supports multiple capture/compares, PWM outputs, and interval timing. It also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 18. Timer TB0 Signal Connections

INPUT PIN NUMBER		DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL	OUTPUT PIN NUMBER	
PZ	ZQW						PZ	ZQW
58-P8.0 P2MAPx(1)	J11-P8.0 P2MAPx(1)	TB0CLK	TB0CLK	Timer	NA	NA		
		ACLK	ACLK					
		SMCLK	SMCLK					
58-P8.0 P2MAPx(1)	J11-P8.0 P2MAPx(1)	TB0CLK	$\overline{\text{TB0CLK}}$					
50-P4.0	J9-P4.0	TB0.0	CCI0A	CCR0	TB0	TB0.0	50-P4.0	J9-P4.0
P2MAPx(1)	P2MAPx(1)	TB0.0	CCI0B				P2MAPx(1)	P2MAPx(1)
		DV_{SS}	GND				ADC12 (internal) (2) ADC12SHSx = {2}	
		DV_{CC}	V_{CC}					
51-P4.1	M11-P4.1	TB0.1	CCI1A	CCR1	TB1	TB0.1	51-P4.1	M11-P4.1
P2MAPx(1)	P2MAPx(1)	TB0.1	CCI1B				P2MAPx(1)	P2MAPx(1)
		DV_{SS}	GND				ADC12 (internal) (2) ADC12SHSx = {3}	
		DV_{CC}	V_{CC}					
52-P4.2	L10-P4.2	TB0.2	CCI2A	CCR2	TB2	TB0.2	52-P4.2	L10-P4.2
P2MAPx(1)	P2MAPx(1)	TB0.2	CCI2B				P2MAPx(1)	P2MAPx(1)
		DV_{SS}	GND				DAC12_A(3) DAC12_0, DAC12_1 (internal)	
		DV_{CC}	V_{CC}					
53-P4.3	M12-P4.3	TB0.3	CCI3A	CCR3	TB3	TB0.3	53-P4.3	M12-P4.3
P2MAPx(1)	P2MAPx(1)	TB0.3	CCI3B				P2MAPx(1)	P2MAPx(1)
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
54-P4.4	L12-P4.4	TB0.4	CCI4A	CCR4	TB4	TB0.4	54-P4.4	L12-P4.4
P2MAPx(1)	P2MAPx(1)	TB0.4	CCI4B				P2MAPx(1)	P2MAPx(1)
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
55-P4.5	L11-P4.5	TB0.5	CCI5A	CCR5	TB5	TB0.5	55-P4.5	L11-P4.5
P2MAPx(1)	P2MAPx(1)	TB0.5	CCI5B				P2MAPx(1)	P2MAPx(1)
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					
56-P4.6	K11-P4.6	TB0.6	CCI6A	CCR6	TB6	TB0.6	56-P4.6	K11-P4.6
P2MAPx(1)	P2MAPx(1)	TB0.6	CCI6B				P2MAPx(1)	P2MAPx(1)
		DV_{SS}	GND					
		DV_{CC}	V_{CC}					

(1) Timer functions selectable via the port mapping controller.
(2) Only on devices with peripheral module ADC12_A.
(3) Only on devices with peripheral module DAC12_A.

Comparator_B (Link to User's Guide)

The primary function of the Comparator_B module is to support precision slope analog-to-digital conversions, battery voltage supervision, and monitoring of external analog signals.

ADC12_A (Link to User's Guide)

The ADC12_A module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without any CPU intervention.

DAC12_A (Link to User's Guide)

The DAC12_A module is a 12-bit R-ladder voltage-output DAC. The DAC12_A may be used in 8-bit or 12-bit mode, and may be used in conjunction with the DMA controller. When multiple DAC12_A modules are present, they may be grouped together for synchronous operation.

CRC16 (Link to User's Guide)

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

REF Voltage Reference (Link to User's Guide)

The reference module (REF) is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device.

USB Universal Serial Bus (Link to User's Guide)

The USB module is a fully integrated USB interface that is compliant with the USB 2.0 specification. The module supports full-speed operation of control, interrupt, and bulk transfers. The module includes an integrated LDO, PHY, and PLL. The PLL is highly flexible and can support a wide range of input clock frequencies. USB RAM, when not used for USB communication, can be used by the system.

Embedded Emulation Module (EEM) (Link to User's Guide)

The Embedded Emulation Module (EEM) supports real-time in-system debugging. The L version of the EEM implemented on these devices has the following features:

- Eight hardware triggers or breakpoints on memory access
- Two hardware triggers or breakpoints on CPU register write access
- Up to ten hardware triggers can be combined to form complex triggers or breakpoints
- Two cycle counters
- Sequencer
- State storage
- Clock control on module level

Peripheral File Map

Table 19. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE(1)
Special Functions (see Table 20)	0100h	000h-01Fh
PMM (see Table 21)	0120h	000h-010h
Flash Control (see Table 22)	0140h	000h-00Fh
CRC16 (see Table 23)	0150h	000h-007h
RAM Control (see Table 24)	0158h	000h-001h
Watchdog (see Table 25)	015Ch	000h-001h
UCS (see Table 26)	0160h	000h-01Fh
SYS (see Table 27)	0180h	000h-01Fh
Shared Reference (see Table 28)	01B0h	000h-001h
Port Mapping Control (see Table 29)	01C0h	000h-003h
Port Mapping Port P2 (see Table 29)	01D0h	000h-007h
Port P1/P2 (see Table 30)	0200h	000h-01Fh
Port P3/P4 (see Table 31)	0220h	000h-01Fh
Port P5/P6 (see Table 32)	0240h	000h-00Bh
Port P7/P8 (see Table 33)	0260h	000h-00Bh
Port P9 (see Table 34)	0280h	000h-00Bh
Port PJ (see Table 35)	0320h	000h-01Fh
Timer TA0 (see Table 36)	0340h	000h-02Eh
Timer TA1 (see Table 37)	0380h	000h-02Eh
Timer TB0 (see Table 38)	03C0h	000h-02Eh
Timer TA2 (see Table 39)	0400h	000h-02Eh
Battery Backup (see Table 40)	0480h	000h-01Fh
RTC_B (see Table 41)	04A0h	000h-01Fh
32-bit Hardware Multiplier (see Table 42)	04C0h	000h-02Fh
DMA General Control (see Table 43)	0500h	000h-00Fh
DMA Channel 0 (see Table 43)	0510h	000h-00Ah
DMA Channel 1 (see Table 43)	0520h	000h-00Ah
DMA Channel 2 (see Table 43)	0530h	000h-00Ah
DMA Channel 3 (see Table 43)	0540h	000h-00Ah
DMA Channel 4 (see Table 43)	0550h	000h-00Ah
DMA Channel 5 (see Table 43)	0560h	000h-00Ah
USCI_A0 (see Table 44)	05C0h	000h-01Fh
USCI_B0 (see Table 45)	05E0h	000h-01Fh
USCI_A1 (see Table 46)	0600h	000h-01Fh
USCI_B1 (see Table 47)	0620h	000h-01Fh
ADC12_A (see Table 48)	0700h	000h-03Fh
DAC12_A (see Table 49)	0780h	000h-01Fh
Comparator_B (see Table 50)	08C0h	000h-00Fh
USB configuration (see Table 51)	0900h	000h-014h
USB control (see Table 52)	0920h	000h-01Fh

(1) For a detailed description of the individual control register offset addresses, see the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

Table 20. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 21. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM Control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
SVS high side control	SVSMHCTL	04h
SVS low side control	SVSMLCTL	06h
PMM interrupt flags	PMMIFG	0Ch
PMM interrupt enable	PMMIE	0Eh
PMM power mode 5 control	PM5CTL0	10h

Table 22. Flash Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Flash control 1	FCTL1	00h
Flash control 3	FCTL3	04h
Flash control 4	FCTL4	06h

Table 23. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC result	CRC16INIRES	04h

Table 24. RAM Control Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM control 0	RCCTL0	00h

Table 25. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

Table 26. UCS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 0	UCSCTL0	00h
UCS control 1	UCSCTL1	02h
UCS control 2	UCSCTL2	04h
UCS control 3	UCSCTL3	06h
UCS control 4	UCSCTL4	08h
UCS control 5	UCSCTL5	0Ah
UCS control 6	UCSCTL6	0Ch
UCS control 7	UCSCTL7	0Eh
UCS control 8	UCSCTL8	10h

Table 27. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootstrap loader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus Error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

Table 28. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

Table 29. Port Mapping Registers (Base Address of Port Mapping Control: 01C0h, Port P2: 01D0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port mapping password register	PMAPPWD	00h
Port mapping control register	PMAPCTL	02h
Port P2.0 mapping register	P2MAP0	00h
Port P2.1 mapping register	P2MAP1	01h
Port P2.2 mapping register	P2MAP2	02h
Port P2.3 mapping register	P2MAP3	03h
Port P2.4 mapping register	P2MAP4	04h
Port P2.5 mapping register	P2MAP5	05h
Port P2.6 mapping register	P2MAP6	06h
Port P2.7 mapping register	P2MAP7	07h

Table 30. Port P1/P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pullup/pulldown enable	P1REN	06h
Port P1 drive strength	P1DS	08h
Port P1 selection	P1SEL	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pullup/pulldown enable	P2REN	07h
Port P2 drive strength	P2DS	09h

Table 30. Port P1/P2 Registers (Base Address: 0200h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P2 selection	P2SEL	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 31. Port P3/P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 pullup/pulldown enable	P3REN	06h
Port P3 drive strength	P3DS	08h
Port P3 selection	P3SEL	0Ah
Port P3 interrupt vector word	P3IV	0Eh
Port P3 interrupt edge select	P3IES	18h
Port P3 interrupt enable	P3IE	1Ah
Port P3 interrupt flag	P3IFG	1Ch
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 pullup/pulldown enable	P4REN	07h
Port P4 drive strength	P4DS	09h
Port P4 selection	P4SEL	0Bh
Port P4 interrupt vector word	P4IV	1Eh
Port P4 interrupt edge select	P4IES	19h
Port P4 interrupt enable	P4IE	1Bh
Port P4 interrupt flag	P4IFG	1Dh

Table 32. Port P5/P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 pullup/pulldown enable	P5REN	06h
Port P5 drive strength	P5DS	08h
Port P5 selection	P5SEL	0Ah
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 pullup/pulldown enable	P6REN	07h
Port P6 drive strength	P6DS	09h
Port P6 selection	P6SEL	0Bh

Table 33. Port P7/P8 Registers (Base Address: 0260h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P7 input	P7IN	00h
Port P7 output	P7OUT	02h
Port P7 direction	P7DIR	04h
Port P7 pullup/pulldown enable	P7REN	06h
Port P7 drive strength	P7DS	08h
Port P7 selection	P7SEL	0Ah
Port P8 input	P8IN	01h
Port P8 output	P8OUT	03h
Port P8 direction	P8DIR	05h
Port P8 pullup/pulldown enable	P8REN	07h
Port P8 drive strength	P8DS	09h
Port P8 selection	P8SEL	0Bh

Table 34. Port P9 Register (Base Address: 0280h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P9 input	P9IN	00h
Port P9 output	P9OUT	02h
Port P9 direction	P9DIR	04h
Port P9 pullup/pulldown enable	P9REN	06h
Port P9 drive strength	P9DS	08h
Port P9 selection	P9SEL	0Ah

Table 35. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ pullup/pulldown enable	PJREN	06h
Port PJ drive strength	PJDS	08h

Table 36. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
Capture/compare control 3	TA0CCTL3	08h
Capture/compare control 4	TA0CCTL4	0Ah
TA0 counter register	TA0R	10h
Capture/compare register 0	TA0CCR0	12h
Capture/compare register 1	TA0CCR1	14h
Capture/compare register 2	TA0CCR2	16h
Capture/compare register 3	TA0CCR3	18h
Capture/compare register 4	TA0CCR4	1Ah
TA0 expansion register 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 37. TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
Capture/compare control 2	TA1CCTL2	06h
TA1 counter register	TA1R	10h
Capture/compare register 0	TA1CCR0	12h
Capture/compare register 1	TA1CCR1	14h
Capture/compare register 2	TA1CCR2	16h
TA1 expansion register 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

Table 38. TB0 Registers (Base Address: 03C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
Capture/compare control 3	TB0CCTL3	08h
Capture/compare control 4	TB0CCTL4	0Ah
Capture/compare control 5	TB0CCTL5	0Ch
Capture/compare control 6	TB0CCTL6	0Eh
TB0 register	TB0R	10h
Capture/compare register 0	TB0CCR0	12h
Capture/compare register 1	TB0CCR1	14h
Capture/compare register 2	TB0CCR2	16h
Capture/compare register 3	TB0CCR3	18h
Capture/compare register 4	TB0CCR4	1Ah
Capture/compare register 5	TB0CCR5	1Ch
Capture/compare register 6	TB0CCR6	1Eh
TB0 expansion register 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

Table 39. TA2 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
Capture/compare control 2	TA2CCTL2	06h
TA2 counter register	TA2R	10h
Capture/compare register 0	TA2CCR0	12h
Capture/compare register 1	TA2CCR1	14h
Capture/compare register 2	TA2CCR2	16h
TA2 expansion register 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

Table 40. Battery Backup Registers (Base Address: 0480h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Battery Backup Memory 0	BAKMEM0	00h
Battery Backup Memory 1	BAKMEM1	02h
Battery Backup Memory 2	BAKMEM2	04h
Battery Backup Memory 3	BAKMEM3	06h
Battery Backup Control	BAKCTL	1Ch
Battery Charger Control	BAKCHCTL	1Eh

Table 41. Real-Time Clock Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control register 0	RTCCTL0	00h
RTC control register 1	RTCCTL1	01h
RTC control register 2	RTCCTL2	02h
RTC control register 3	RTCCTL3	03h
RTC prescaler 0 control register	RTCPS0CTL	08h
RTC prescaler 1 control register	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds	RTCSEC	10h
RTC minutes	RTCMIN	11h
RTC hours	RTCHOUR	12h
RTC day of week	RTCDOW	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year low	RTCYEARL	16h
RTC year high	RTCYEARH	17h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh
Binary-to-BCD conversion register	BIN2BCD	1Ch
BCD-to-binary conversion register	BCD2BIN	1Eh

Table 42. 32-bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension register	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h

Table 42. 32-bit Hardware Multiplier Registers (Base Address: 04C0h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control register 0	MPY32CTL0	2Ch

Table 43. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h, DMA Channel 3: 0540h, DMA Channel 4: 0550h, DMA Channel 5: 0560h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA General Control: DMA module control 0	DMACTL0	00h
DMA General Control: DMA module control 1	DMACTL1	02h
DMA General Control: DMA module control 2	DMACTL2	04h
DMA General Control: DMA module control 3	DMACTL3	06h
DMA General Control: DMA module control 4	DMACTL4	08h
DMA General Control: DMA interrupt vector	DMAIV	0Ah
DMA Channel 0 control	DMA0CTL	00h
DMA Channel 0 source address low	DMA0SAL	02h
DMA Channel 0 source address high	DMA0SAH	04h
DMA Channel 0 destination address low	DMA0DAL	06h
DMA Channel 0 destination address high	DMA0DAH	08h
DMA Channel 0 transfer size	DMA0SZ	0Ah
DMA Channel 1 control	DMA1CTL	00h
DMA Channel 1 source address low	DMA1SAL	02h
DMA Channel 1 source address high	DMA1SAH	04h
DMA Channel 1 destination address low	DMA1DAL	06h
DMA Channel 1 destination address high	DMA1DAH	08h
DMA Channel 1 transfer size	DMA1SZ	0Ah
DMA Channel 2 control	DMA2CTL	00h
DMA Channel 2 source address low	DMA2SAL	02h
DMA Channel 2 source address high	DMA2SAH	04h
DMA Channel 2 destination address low	DMA2DAL	06h
DMA Channel 2 destination address high	DMA2DAH	08h
DMA Channel 2 transfer size	DMA2SZ	0Ah
DMA Channel 3 control	DMA3CTL	00h
DMA Channel 3 source address low	DMA3SAL	02h
DMA Channel 3 source address high	DMA3SAH	04h
DMA Channel 3 destination address low	DMA3DAL	06h
DMA Channel 3 destination address high	DMA3DAH	08h
DMA Channel 3 transfer size	DMA3SZ	0Ah
DMA Channel 4 control	DMA4CTL	00h
DMA Channel 4 source address low	DMA4SAL	02h

Table 43. DMA Registers (Base Address DMA General Control: 0500h, DMA Channel 0: 0510h, DMA Channel 1: 0520h, DMA Channel 2: 0530h, DMA Channel 3: 0540h, DMA Channel 4: 0550h, DMA Channel 5: 0560h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA Channel 4 source address high	DMA4SAH	04h
DMA Channel 4 destination address low	DMA4DAL	06h
DMA Channel 4 destination address high	DMA4DAH	08h
DMA Channel 4 transfer size	DMA4SZ	0Ah
DMA Channel 5 control	DMA5CTL	00h
DMA Channel 5 source address low	DMA5SAL	02h
DMA Channel 5 source address high	DMA5SAH	04h
DMA Channel 5 destination address low	DMA5DAL	06h
DMA Channel 5 destination address high	DMA5DAH	08h
DMA Channel 5 transfer size	DMA5SZ	0Ah

Table 44. USCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 0	UCA0CTL0	00h
USCI control 1	UCA0CTL1	01h
USCI baud rate 0	UCA0BR0	06h
USCI baud rate 1	UCA0BR1	07h
USCI modulation control	UCA0MCTL	08h
USCI status	UCA0STAT	0Ah
USCI receive buffer	UCA0RXBUF	0Ch
USCI transmit buffer	UCA0TXBUF	0Eh
USCI LIN control	UCA0ABCTL	10h
USCI IrDA transmit control	UCA0IRTCTL	12h
USCI IrDA receive control	UCA0IRRCTL	13h
USCI interrupt enable	UCA0IE	1Ch
USCI interrupt flags	UCA0IFG	1Dh
USCI interrupt vector word	UCA0IV	1Eh

Table 45. USCI_B0 Registers (Base Address: 05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 0	UCB0CTL0	00h
USCI synchronous control 1	UCB0CTL1	01h
USCI synchronous bit rate 0	UCB0BR0	06h
USCI synchronous bit rate 1	UCB0BR1	07h
USCI synchronous status	UCB0STAT	0Ah
USCI synchronous receive buffer	UCB0RXBUF	0Ch
USCI synchronous transmit buffer	UCB0TXBUF	0Eh
USCI I2C own address	UCB0I2COA	10h
USCI I2C slave address	UCB0I2CSA	12h
USCI interrupt enable	UCB0IE	1Ch
USCI interrupt flags	UCB0IFG	1Dh
USCI interrupt vector word	UCB0IV	1Eh

Table 46. USCI_A1 Registers (Base Address: 0600h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI control 0	UCA1CTL0	00h
USCI control 1	UCA1CTL1	01h
USCI baud rate 0	UCA1BR0	06h
USCI baud rate 1	UCA1BR1	07h
USCI modulation control	UCA1MCTL	08h
USCI status	UCA1STAT	0Ah
USCI receive buffer	UCA1RXBUF	0Ch
USCI transmit buffer	UCA1TXBUF	0Eh
USCI LIN control	UCA1ABCTL	10h
USCI IrDA transmit control	UCA1IRTCTL	12h
USCI IrDA receive control	UCA1IRRCTL	13h
USCI interrupt enable	UCA1IE	1Ch
USCI interrupt flags	UCA1IFG	1Dh
USCI interrupt vector word	UCA1IV	1Eh

Table 47. USCI_B1 Registers (Base Address: 0620h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USCI synchronous control 0	UCB1CTL0	00h
USCI synchronous control 1	UCB1CTL1	01h
USCI synchronous bit rate 0	UCB1BR0	06h
USCI synchronous bit rate 1	UCB1BR1	07h
USCI synchronous status	UCB1STAT	0Ah
USCI synchronous receive buffer	UCB1RXBUF	0Ch
USCI synchronous transmit buffer	UCB1TXBUF	0Eh
USCI I2C own address	UCB1I2COA	10h
USCI I2C slave address	UCB1I2CSA	12h
USCI interrupt enable	UCB1IE	1Ch
USCI interrupt flags	UCB1IFG	1Dh
USCI interrupt vector word	UCB1IV	1Eh

Table 48. ADC12_A Registers (Base Address: 0700h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Control register 0	ADC12CTL0	00h
Control register 1	ADC12CTL1	02h
Control register 2	ADC12CTL2	04h
Interrupt-flag register	ADC12IFG	0Ah
Interrupt-enable register	ADC12IE	0Ch
Interrupt-vector-word register	ADC12IV	0Eh
ADC memory-control register 0	ADC12MCTL0	10h
ADC memory-control register 1	ADC12MCTL1	11h
ADC memory-control register 2	ADC12MCTL2	12h
ADC memory-control register 3	ADC12MCTL3	13h
ADC memory-control register 4	ADC12MCTL4	14h
ADC memory-control register 5	ADC12MCTL5	15h
ADC memory-control register 6	ADC12MCTL6	16h
ADC memory-control register 7	ADC12MCTL7	17h
ADC memory-control register 8	ADC12MCTL8	18h

Table 48. ADC12_A Registers (Base Address: 0700h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC memory-control register 9	ADC12MCTL9	19h
ADC memory-control register 10	ADC12MCTL10	1Ah
ADC memory-control register 11	ADC12MCTL11	1Bh
ADC memory-control register 12	ADC12MCTL12	1Ch
ADC memory-control register 13	ADC12MCTL13	1Dh
ADC memory-control register 14	ADC12MCTL14	1Eh
ADC memory-control register 15	ADC12MCTL15	1Fh
Conversion memory 0	ADC12MEM0	20h
Conversion memory 1	ADC12MEM1	22h
Conversion memory 2	ADC12MEM2	24h
Conversion memory 3	ADC12MEM3	26h
Conversion memory 4	ADC12MEM4	28h
Conversion memory 5	ADC12MEM5	2Ah
Conversion memory 6	ADC12MEM6	2Ch
Conversion memory 7	ADC12MEM7	2Eh
Conversion memory 8	ADC12MEM8	30h
Conversion memory 9	ADC12MEM9	32h
Conversion memory 10	ADC12MEM10	34h
Conversion memory 11	ADC12MEM11	36h
Conversion memory 12	ADC12MEM12	38h
Conversion memory 13	ADC12MEM13	3Ah
Conversion memory 14	ADC12MEM14	3Ch
Conversion memory 15	ADC12MEM15	3Eh

Table 49. DAC12_A Registers (Base Address: 0780h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DAC12_A channel 0 control register 0	DAC12_0CTL0	00h
DAC12_A channel 0 control register 1	DAC12_0CTL1	02h
DAC12_A channel 0 data register	DAC12_0DAT	04h
DAC12_A channel 0 calibration control register	DAC12_0CALCTL	06h
DAC12_A channel 0 calibration data register	DAC12_0CALDAT	08h
DAC12_A channel 1 control register 0	DAC12_1CTL0	10h
DAC12_A channel 1 control register 1	DAC12_1CTL1	12h
DAC12_A channel 1 data register	DAC12_1DAT	14h
DAC12_A channel 1 calibration control register	DAC12_1CALCTL	16h
DAC12_A channel 1 calibration data register	DAC12_1CALDAT	18h
DAC12_A interrupt vector word	DAC12IV	1Eh

Table 50. Comparator_B Registers (Base Address: 08C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Comp_B control register 0	CBCTL0	00h
Comp_B control register 1	CBCTL1	02h
Comp_B control register 2	CBCTL2	04h
Comp_B control register 3	CBCTL3	06h
Comp_B interrupt register	CBINT	0Ch
Comp_B interrupt vector word	CBIV	0Eh

Table 51. USB Configuration Registers (Base Address: 0900h)

REGISTER DESCRIPTION	REGISTER	OFFSET
USB key/ID	USBKEYID	00h
USB module configuration	USBCNF	02h
USB PHY control	USBPHYCTL	04h
USB power control	USBPWRCTL	08h
USB power voltage setting	USBPWRVSR	0Ah
USB PLL control	USBPLLCTL	10h
USB PLL divider	USBPLLDIV	12h
USB PLL interrupts	USBPLLIR	14h

Table 52. USB Control Registers (Base Address: 0920h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Input endpoint#0 configuration	IEPCNF_0	00h
Input endpoint #0 byte count	IEPCNT_0	01h
Output endpoint#0 configuration	OEPCNF_0	02h
Output endpoint #0 byte count	OEPCNT_0	03h
Input endpoint interrupt enables	IEPIE	0Eh
Output endpoint interrupt enables	OEPIE	0Fh
Input endpoint interrupt flags	IEPIFG	10h
Output endpoint interrupt flags	OEPIFG	11h
USB interrupt vector	USBIV	12h
USB maintenance	MAINT	16h
Time stamp	TSREG	18h
USB frame number	USBFN	1Ah
USB control	USBCTL	1Ch
USB interrupt enables	USBIE	1Dh
USB interrupt flags	USBIFG	1Eh
Function address	FUNADR	1Fh

Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

Voltage applied at V_{CC} to V_{SS}	–0.3 V to 4.1 V
Voltage applied to any pin (excluding VCORE, VBUS, V18)(2)	–0.3 V to V_{CC} + 0.3 V
Diode current at any device pin	±2 mA
Storage temperature range, T_{stg}(3)	–55°C to 150°C
Maximum junction temperature, T_J	95°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. VCORE is for internal device use only. No external dc loading or voltage should be applied.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Thermal Packaging Characteristics

PARAMETER			VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance, still air(1)	QFP (PZ)	122	°C/W
		BGA (ZQW)	108	
$\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance(2)	QFP (PZ)	83	°C/W
		BGA (ZQW)	72	
θ_{JB}	Junction-to-board thermal resistance(3)	QFP (PZ)	98	°C/W
		BGA (ZQW)	76	

(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

Recommended Operating Conditions

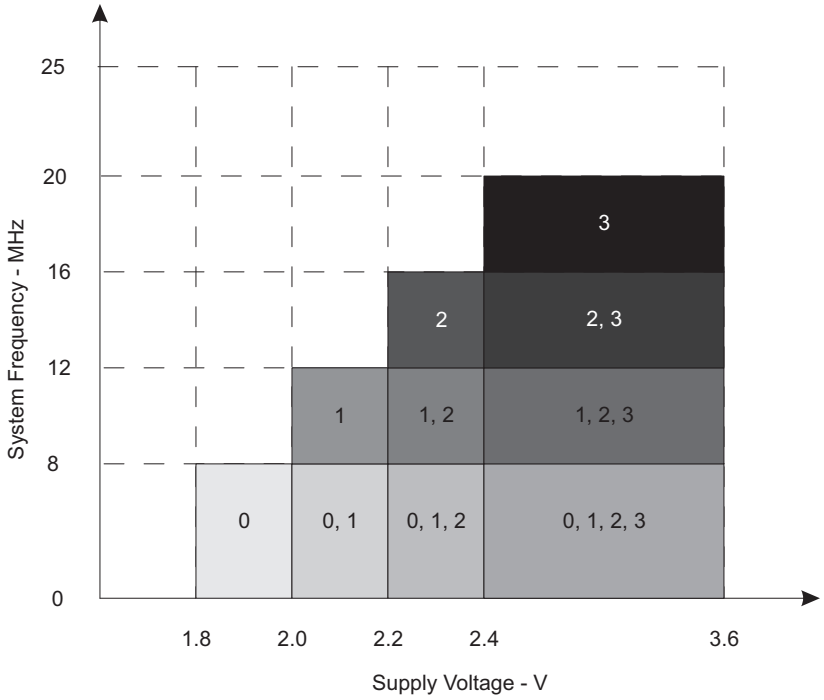
			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming (AVCC1 = DVCC1 = DVCC2 = DVCC3 = DV_{CC} = V_{CC})(1)(2)	PMMCOREVx = 0	1.8		3.6	V
		PMMCOREVx = 0, 1	2.0		3.6	
		PMMCOREVx = 0, 1, 2	2.2		3.6	
		PMMCOREVx = 0, 1, 2, 3	2.4		3.6	
$V_{CC,USB}$	Supply voltage during USB operation, USB PLL disabled (USB_EN = 1, UPLLEN = 0)	PMMCOREVx = 0	1.8		3.6	V
		PMMCOREVx = 0, 1	2.0		3.6	
		PMMCOREVx = 0, 1, 2	2.2		3.6	
		PMMCOREVx = 0, 1, 2, 3	2.4		3.6	
	Supply voltage during USB operation, USB PLL enabled(3) (USB_EN = 1, UPLLEN = 1)	PMMCOREVx = 2	2.2		3.6	
		PMMCOREVx = 2, 3	2.4		3.6	
V_{SS}	Supply voltage (AVSS1 = AVSS2 = AVSS3 = DVSS1 = DVSS2 = DVSS3 = V_{SS})			0		V
$V_{BAT,RTC}$	Backup-supply voltage with RTC operational	T_A = 0°C to 85°C	1.55		3.6	V
		T_A = –40°C to 85°C	1.70		3.6	
$V_{BAT,MEM}$	Backup-supply voltage with backup memory retained.	T_A = –40°C to 85°C	1.20		3.6	V
T_A	Operating free-air temperature	I version	–40		85	°C
T_J	Operating junction temperature	I version	–40		85	°C
C_{BAK}	Capacitance at pin VBAK		1	4.7	10	nF

(1) It is recommended to power AV_{CC} and DV_{CC} from the same source. A maximum difference of 0.3 V between AV_{CC} and DV_{CC} can be tolerated during power up and operation.
(2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the PMM, SVS High Side threshold parameters for the exact values and further details.
(3) USB operation with USB PLL enabled requires PMMCOREVx ≥ 2 for proper operation.

Recommended Operating Conditions (continued)

			MIN	NOM	MAX	UNIT
C_{VCORE}	Capacitor at VCORE			470		nF
C_{DVCC}/C_{VCORE}	Capacitor ratio of DVCC to VCORE		10			
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)(4)(5) (see Figure 2)	PMMCOREVx = 0, 1.8 V ≤ V_{CC} ≤ 3.6 V (default condition)	0		8.0	MHz
		PMMCOREVx = 1, 2 V ≤ V_{CC} ≤ 3.6 V	0		12.0	
		PMMCOREVx = 2, 2.2 V ≤ V_{CC} ≤ 3.6 V	0		16.0	
		PMMCOREVx = 3, 2.4 V ≤ V_{CC} ≤ 3.6 V	0		20.0	
f_{SYSTEM_USB}	Minimum processor frequency for USB operation		1.5			MHz
USB_wait	Wait state cycles during USB operation			16		cycles

(4) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse duration of the specified maximum frequency.
(5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.



The numbers within the fields denote the supported PMMCOREVx settings.

Figure 2. Frequency vs Supply Voltage

Electrical Characteristics

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)(1)(2)(3)

PARAMETER	EXECUTION MEMORY	V_{CC}	PMMCOREVx	FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$)								UNIT
				1 MHz		8 MHz		12 MHz		20 MHz		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, Flash}$	Flash	3 V	0	0.32	0.36	2.1	2.4					mA
			1	0.36		2.4		3.6	4.0			
			2	0.37		2.5		3.8				
			3	0.39		2.7		4.0		6.6		
$I_{AM, RAM}$	RAM	3 V	0	0.18	0.21	1.0	1.2					mA
			1	0.20		1.2		1.7	1.9			
			2	0.22		1.3		2.0				
			3	0.23		1.4		2.1		3.6		

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Characterized with program executing typical data processing. USB disabled (VUSBEN = 0, SLDOEN = 0).
f_{ACLK} = 32786 Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0.

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER		V_{CC}	PMMCOREVx	-40°C		25°C		60°C		85°C		UNIT
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0,1MHz}$	Low-power mode 0(3)(4)	2.2 V	0	71		75	87	81		85	99	µA
		3 V	3	78		83	98	89		94	108	
I_{LPM2}	Low-power mode 2(5)(4)	2.2 V	0	6.3		6.7	9.9	9.0		11	16	µA
		3 V	3	6.6		7.0	11	10		12	18	
$I_{LPM3,XT1LF}$	Low-power mode 3, crystal mode(6)(4)	2.2 V	0	1.6		1.8	2.4	4.7		6.5	10.5	µA
			1	1.6		1.9		4.8		6.6		
			2	1.7		2.0		4.9		6.7		
		3 V	0	1.9		2.1	2.7	5.0		6.8	10.8	
			1	1.9		2.1		5.1		7.0		
			2	2.0		2.2		5.2		7.1		
			3	2.0		2.2	2.9	5.4		7.3	12.6	
$I_{LPM3,VLO,WDT}$	Low-power mode 3, VLO mode, Watchdog enabled(7)(4)	3 V	0	0.9		1.2	1.9	4.0		5.9	10.3	µA
			1	0.9		1.2		4.1		6.0		
			2	1.0		1.3		4.2		6.1		
			3	1.0		1.3	2.2	4.3		6.3	11.3	
I_{LPM4}	Low-power mode 4(8)(4)	3 V	0	0.9		1.1	1.8	3.9		5.8	10	µA
			1	0.9		1.1		4.0		5.9		
			2	1.0		1.2		4.1		6.1		
			3	1.0		1.2	2.1	4.2		6.2	11	
$I_{LPM3.5,RTC,VCC}$	Low-power mode 3.5 (LPM3.5) current with active RTC into primary supply pin DV_{CC} (9)	3 V				0.5				0.8	1.4	µA
$I_{LPM3.5,RTC,VBAT}$	Low-power mode 3.5 (LPM3.5) current with active RTC into backup supply pin VBAT(10)	3 V				0.6				0.8	1.4	µA
$I_{LPM3.5,RTC,TOT}$	Total low-power mode 3.5 (LPM3.5) current with active RTC(11)	3 V		1.0		1.1		1.3		1.6	2.8	µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal CC4V-T1A SMD crystal with a load capacitance of 9 pF. The internal and external load capacitance are chosen to closely match the required 9 pF.
(3) Current for watchdog timer clocked by SMCLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz
USB disabled (VUSBEN = 0, SLDOEN = 0).
(4) Current for brownout included. Low side supervisor and monitors disabled (SVS_L, SVM_L). High side supervisor and monitor disabled (SVS_H, SVM_H). RAM retention enabled.
(5) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz; DCO setting = 1 MHz operation, DCO bias generator enabled.
USB disabled (VUSBEN = 0, SLDOEN = 0).
(6) Current for watchdog timer clocked by ACLK and RTC clocked by LFXT1 (32768 Hz) included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
USB disabled (VUSBEN = 0, SLDOEN = 0).
(7) Current for watchdog timer clocked by VLO included.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
USB disabled (VUSBEN = 0, SLDOEN = 0).
(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4); f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz
USB disabled (VUSBEN = 0, SLDOEN = 0).
(9) V_{VBAT} = V_{CC} - 0.2 V, f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32768 Hz, PMMREGOFF = 1, RTC in backup domain active
(10) V_{VBAT} = V_{CC} - 0.2 V, f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32768 Hz, PMMREGOFF = 1, RTC in backup domain active, no current drawn on VBAK
(11) f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32768 Hz, PMMREGOFF = 1, RTC in backup domain active, no current drawn on VBAK

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER		V_{CC}	PMMCOREVx	-40°C		25°C		60°C		85°C		UNIT
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM4.5}$	Low-power mode 4.5 (LPM4.5)(12)	3 V		0.2		0.3	0.6	0.7		0.9	1.4	µA

(12) Internal regulator disabled. No data retention.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1, PMMREGOFF = 1 (LPM4.5); $f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz

Schmitt-Trigger Inputs – General Purpose I/O(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		1.8 V	0.80		1.40	V
			3 V	1.50		2.10	
V_{IT-}	Negative-going input threshold voltage		1.8 V	0.45		1.00	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} – V_{IT-}$)		1.8 V	0.3		0.8	V
			3 V	0.4		1.0	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
C_I	Input capacitance	$V_{IN} = V_{SS}$ or V_{CC}			5		pF

(1) Same parametrics apply to clock input pin when crystal bypass mode is used on XT1 (XIN) or XT2 (XT2IN).

Inputs – Ports P1, P2, P3, and P4(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing(2)	Port P1, P2, P3, P4: P1.x to P4.x, External trigger pulse duration to set interrupt flag	2.2 V, 3 V	20		ns

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

Leakage Current – General Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	(1)(2)	1.8 V, 3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

Outputs – General Purpose I/O (Full Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)} = –3$ mA(1)	1.8 V	$V_{CC} – 0.25$	V_{CC}	V
		$I_{(OHmax)} = –10$ mA(2)		$V_{CC} – 0.60$	V_{CC}	
		$I_{(OHmax)} = –5$ mA(1)	3 V	$V_{CC} – 0.25$	V_{CC}	
		$I_{(OHmax)} = –15$ mA(2)		$V_{CC} – 0.60$	V_{CC}	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

Outputs – General Purpose I/O (Full Drive Strength) (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 3 mA(1)	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 10 mA(2)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 5 mA(1)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 15 mA(2)		V_{SS}	V_{SS} + 0.60	

Outputs – General Purpose I/O (Reduced Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA(2)	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –3 mA(3)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –2 mA(2)	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA(3)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA(2)	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA(3)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA(2)	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA(3)		V_{SS}	V_{SS} + 0.60	

(1) Selecting reduced drive strength may reduce EMI.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(3) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

Output Frequency – Ports P1, P2, and P3

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	P3.4/TA2CLK/SMCLK/S27 C_L = 20 pF, R_L = 1 kΩ(1) or 3.2 kΩ(2)(3)	V_{CC} = 1.8 V PMMCOREVx = 0		8	MHz
			V_{CC} = 3 V PMMCOREVx = 3		20	
f_{Port_CLK}	Clock output frequency	P1.0/TA0CLK/ACLK/S39 P3.4/TA2CLK/SMCLK/S27 P2.0/P2MAP0 (P2MAP0 = PM_MCLK) C_L = 20 pF(3)	V_{CC} = 1.8 V PMMCOREVx = 0		8	MHz
			V_{CC} = 3 V PMMCOREVx = 3		20	

(1) Full drive strength of port: A resistive divider with 2 × 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(2) Reduced drive strength of port: A resistive divider with 2 × 1.6 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
(3) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Typical Characteristics – Outputs, Reduced Drive Strength (PxDS.y = 0)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

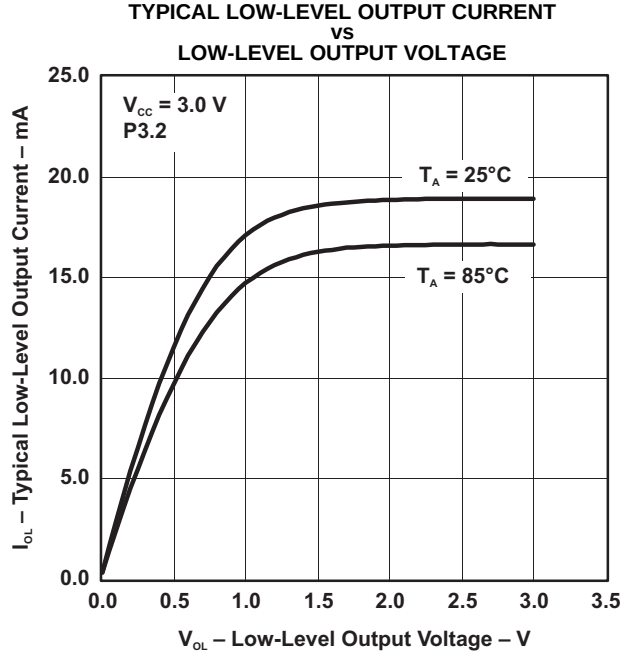


Figure 3.

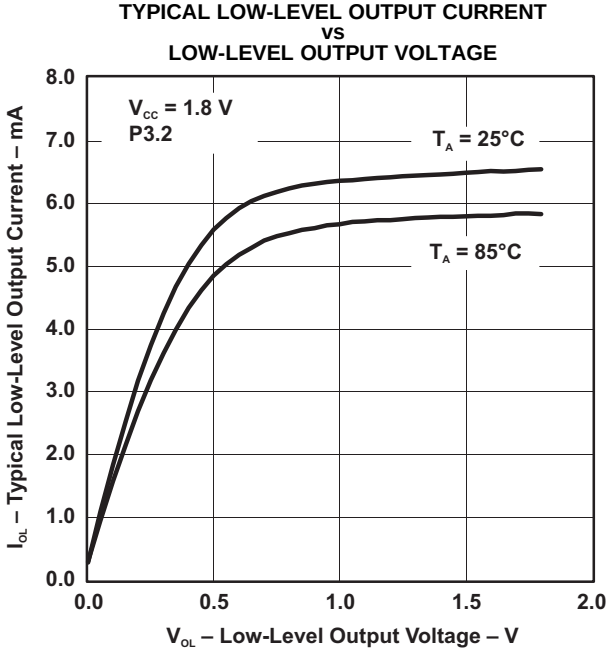


Figure 4.

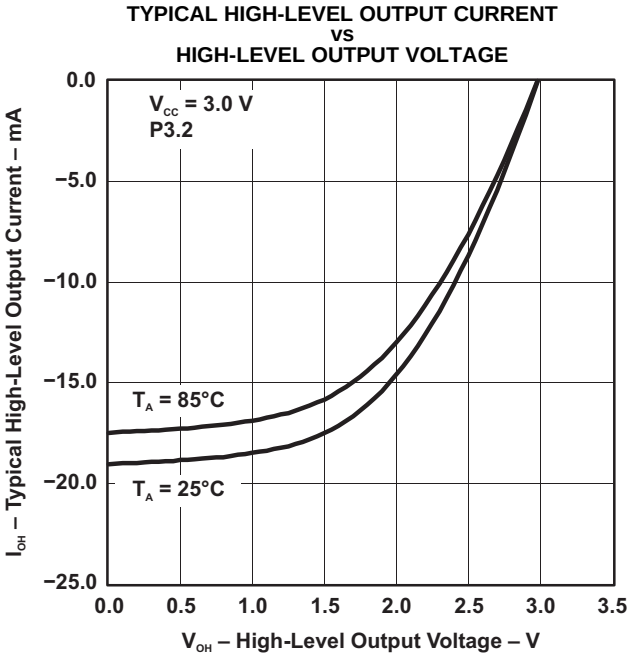


Figure 5.

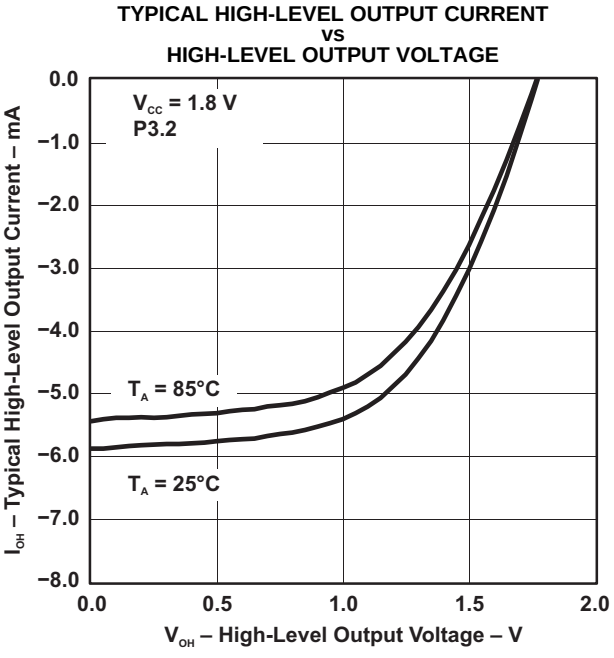


Figure 6.

Typical Characteristics – Outputs, Full Drive Strength (PxDS.y = 1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

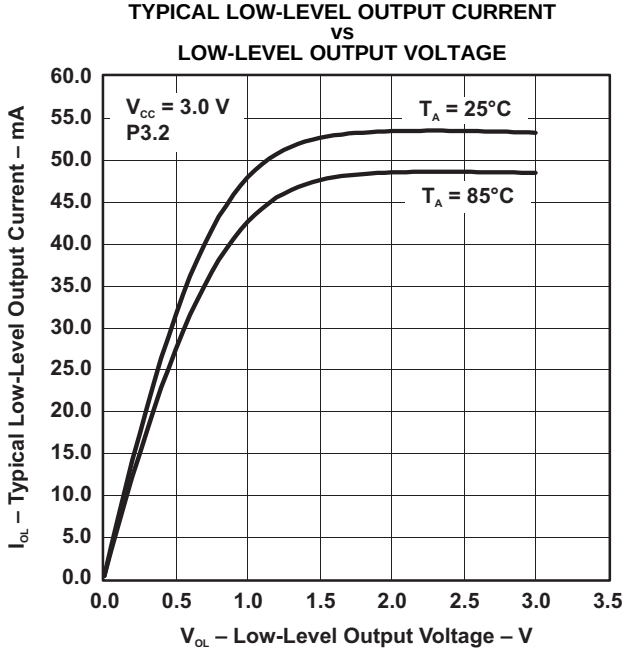


Figure 7.

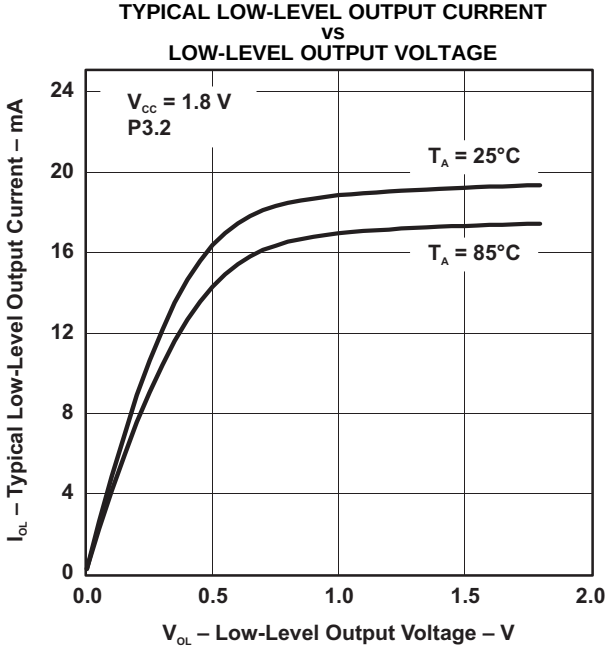


Figure 8.

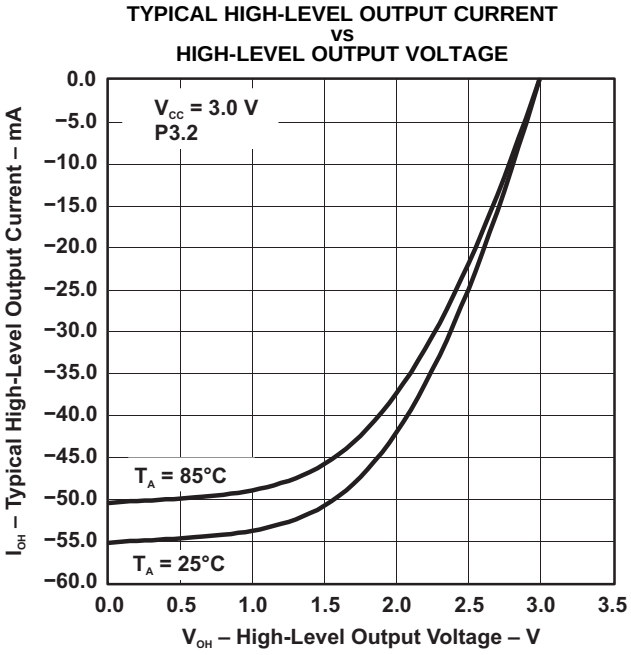


Figure 9.

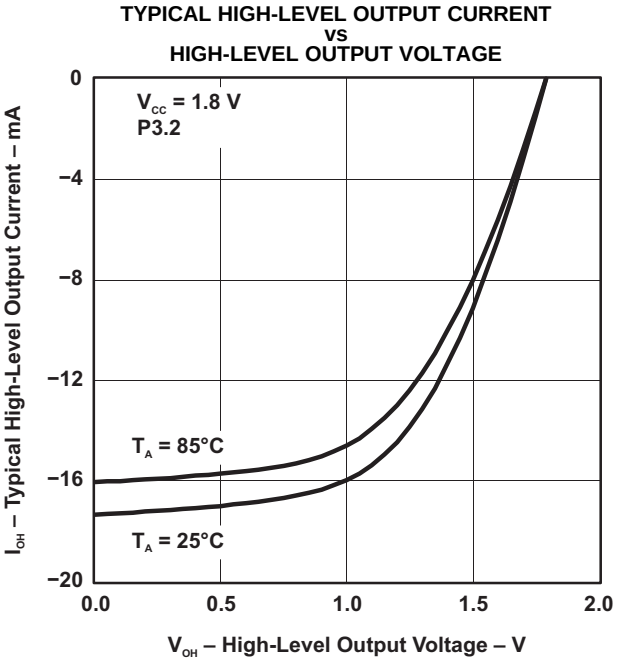


Figure 10.

Crystal Oscillator, XT1, Low-Frequency Mode(1)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$\Delta I_{DVCC,LF}$	Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C	3 V		0.075		µA
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C			0.170		
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C			0.290		
$f_{XT1,LF0}$	XT1 oscillator crystal frequency, LF mode	XTS = 0, XT1BYPASS = 0			32768		Hz
$f_{XT1,LF,SW}$	XT1 oscillator logic-level square-wave input frequency, LF mode	XTS = 0, XT1BYPASS = 1(2) (3)		10	32.768	50	kHz
OA_{LF}	Oscillation allowance for LF crystals(4)	XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, LF mode(5)	XTS = 0, XCAPx = 0(6)			2		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			12.0		
	Duty cycle, LF mode	XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz		30		70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode(7)	XTS = 0(8)		10		10000	Hz
$t_{START,LF}$	Startup time, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 6 pF	3 V		1000		ms
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C, $C_{L,eff}$ = 12 pF			500		

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
  (a) Keep the trace between the device and the crystal as short as possible.
  (b) Design a good ground plane around the oscillator pins.
  (c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
  (d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
  (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
  (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.

(2) When XT1BYPASS is set, XT1 circuit is automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet.

(3) Maximum frequency of operation of the entire device cannot be exceeded.

(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVEx settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
  (a) For XT1DRIVEx = 0, $C_{L,eff} \le 6$ pF.
  (b) For XT1DRIVEx = 1, 6 pF $\le C_{L,eff} \le$ 9 pF.
  (c) For XT1DRIVEx = 2, 6 pF $\le C_{L,eff} \le$ 10 pF.
  (d) For XT1DRIVEx = 3, $C_{L,ef\ f} \ge 6$ pF.

(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
  Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.

(6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.

(8) Measured with logic-level input frequency but also applies to operation with crystals.

Crystal Oscillator, XT2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{DVCC,XT2}$	XT2 oscillator crystal current consumption	f_{OSC} = 4 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 0, T_A = 25°C	3 V		200		µA
		f_{OSC} = 12 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 1, T_A = 25°C			260		
		f_{OSC} = 20 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 2, T_A = 25°C			325		
		f_{OSC} = 32 MHz, XT2OFF = 0, XT2BYPASS = 0, XT2DRIVEx = 3, T_A = 25°C			450		
$f_{XT2,HF0}$	XT2 oscillator crystal frequency, mode 0	XT2DRIVEx = 0, XT2BYPASS = 0(3)		4		8	MHz
$f_{XT2,HF1}$	XT2 oscillator crystal frequency, mode 1	XT2DRIVEx = 1, XT2BYPASS = 0(3)		8		16	MHz
$f_{XT2,HF2}$	XT2 oscillator crystal frequency, mode 2	XT2DRIVEx = 2, XT2BYPASS = 0(3)		16		24	MHz
$f_{XT2,HF3}$	XT2 oscillator crystal frequency, mode 3	XT2DRIVEx = 3, XT2BYPASS = 0(3)		24		32	MHz
$f_{XT2,HF,SW}$	XT2 oscillator logic-level square-wave input frequency	XT2BYPASS = 1(4) (3)		0.7		32	MHz
OA_{HF}	Oscillation allowance for HF crystals(5)	XT2DRIVEx = 0, XT2BYPASS = 0, $f_{XT2,HF0}$ = 6 MHz, $C_{L,eff}$ = 15 pF			450		Ω
		XT2DRIVEx = 1, XT2BYPASS = 0, $f_{XT2,HF1}$ = 12 MHz, $C_{L,eff}$ = 15 pF			320		
		XT2DRIVEx = 2, XT2BYPASS = 0, $f_{XT2,HF2}$ = 20 MHz, $C_{L,eff}$ = 15 pF			200		
		XT2DRIVEx = 3, XT2BYPASS = 0, $f_{XT2,HF3}$ = 32 MHz, $C_{L,eff}$ = 15 pF			200		
$t_{START,HF}$	Startup time	f_{OSC} = 6 MHz XT2BYPASS = 0, XT2DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 15 pF	3 V		0.5		ms
		f_{OSC} = 20 MHz XT2BYPASS = 0, XT2DRIVEx = 3, T_A = 25°C, $C_{L,eff}$ = 15 pF			0.3		
$C_{L,eff}$	Integrated effective load capacitance, HF mode(6) (1)				1		pF
	Duty cycle	Measured at ACLK, $f_{XT2,HF2}$ = 20 MHz		40	50	60	%
$f_{Fault,HF}$	Oscillator fault frequency(7)	XT2BYPASS = 1(8)		30		300	kHz

(1) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
(2) To improve EMI on the XT2 oscillator the following guidelines should be observed.
  (a) Keep the traces between the device and the crystal as short as possible.
  (b) Design a good ground plane around the oscillator pins.
  (c) Prevent crosstalk from other clock or data lines into oscillator pins XT2IN and XT2OUT.
  (d) Avoid running PCB traces underneath or adjacent to the XT2IN and XT2OUT pins.
  (e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XT2IN and XT2OUT pins.
  (f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
(3) Maximum frequency of operation of the entire device cannot be exceeded.
(4) When XT2BYPASS is set, the XT2 circuit is automatically powered down.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals.
(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
  Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(8) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at ACLK	1.8 V to 3.6 V	6	9.4	14	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at ACLK(1)	1.8 V to 3.6 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at ACLK(2)	1.8 V to 3.6 V		4		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40	50	60	%

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO oscillator current consumption	T_A = 25°C	1.8 V to 3.6 V		3		µA
f_{REFO}	REFO frequency calibrated	Measured at ACLK	1.8 V to 3.6 V		32768		Hz
	REFO absolute tolerance calibrated	Full temperature range	1.8 V to 3.6 V			±3.5	%
		T_A = 25°C	3 V			±1.5	%
df_{REFO}/d_T	REFO frequency temperature drift	Measured at ACLK(1)	1.8 V to 3.6 V		0.01		%/°C
df_{REFO}/dV_{CC}	REFO frequency supply voltage drift	Measured at ACLK(2)	1.8 V to 3.6 V		1.0		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40	50	60	%
t_{START}	REFO startup time	40%/60% duty cycle	1.8 V to 3.6 V		25		µs

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO(0,0)}$	DCO frequency (0, 0)	DCORSELx = 0, DCOx = 0, MODx = 0	0.07		0.20	MHz
$f_{DCO(0,31)}$	DCO frequency (0, 31)	DCORSELx = 0, DCOx = 31, MODx = 0	0.70		1.70	MHz
$f_{DCO(1,0)}$	DCO frequency (1, 0)	DCORSELx = 1, DCOx = 0, MODx = 0	0.15		0.36	MHz
$f_{DCO(1,31)}$	DCO frequency (1, 31)	DCORSELx = 1, DCOx = 31, MODx = 0	1.47		3.45	MHz
$f_{DCO(2,0)}$	DCO frequency (2, 0)	DCORSELx = 2, DCOx = 0, MODx = 0	0.32		0.75	MHz
$f_{DCO(2,31)}$	DCO frequency (2, 31)	DCORSELx = 2, DCOx = 31, MODx = 0	3.17		7.38	MHz
$f_{DCO(3,0)}$	DCO frequency (3, 0)	DCORSELx = 3, DCOx = 0, MODx = 0	0.64		1.51	MHz
$f_{DCO(3,31)}$	DCO frequency (3, 31)	DCORSELx = 3, DCOx = 31, MODx = 0	6.07		14.0	MHz
$f_{DCO(4,0)}$	DCO frequency (4, 0)	DCORSELx = 4, DCOx = 0, MODx = 0	1.3		3.2	MHz
$f_{DCO(4,31)}$	DCO frequency (4, 31)	DCORSELx = 4, DCOx = 31, MODx = 0	12.3		28.2	MHz
$f_{DCO(5,0)}$	DCO frequency (5, 0)	DCORSELx = 5, DCOx = 0, MODx = 0	2.5		6.0	MHz
$f_{DCO(5,31)}$	DCO frequency (5, 31)	DCORSELx = 5, DCOx = 31, MODx = 0	23.7		54.1	MHz
$f_{DCO(6,0)}$	DCO frequency (6, 0)	DCORSELx = 6, DCOx = 0, MODx = 0	4.6		10.7	MHz
$f_{DCO(6,31)}$	DCO frequency (6, 31)	DCORSELx = 6, DCOx = 31, MODx = 0	39.0		88.0	MHz
$f_{DCO(7,0)}$	DCO frequency (7, 0)	DCORSELx = 7, DCOx = 0, MODx = 0	8.5		19.6	MHz
$f_{DCO(7,31)}$	DCO frequency (7, 31)	DCORSELx = 7, DCOx = 31, MODx = 0	60		135	MHz
$S_{DCORSEL}$	Frequency step between range DCORSEL and DCORSEL + 1	$S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$	1.2		2.3	ratio
S_{DCO}	Frequency step between tap DCO and DCO + 1	$S_{DCO} = f_{DCO(DCORSEL,DCO+1)}/f_{DCO(DCORSEL,DCO)}$	1.02		1.12	ratio
	Duty cycle	Measured at SMCLK	40	50	60	%
df_{DCO}/dT	DCO frequency temperature drift	f_{DCO} = 1 MHz,		0.1		%/°C
df_{DCO}/dV_{CC}	DCO frequency voltage drift	f_{DCO} = 1 MHz		1.9		%/V

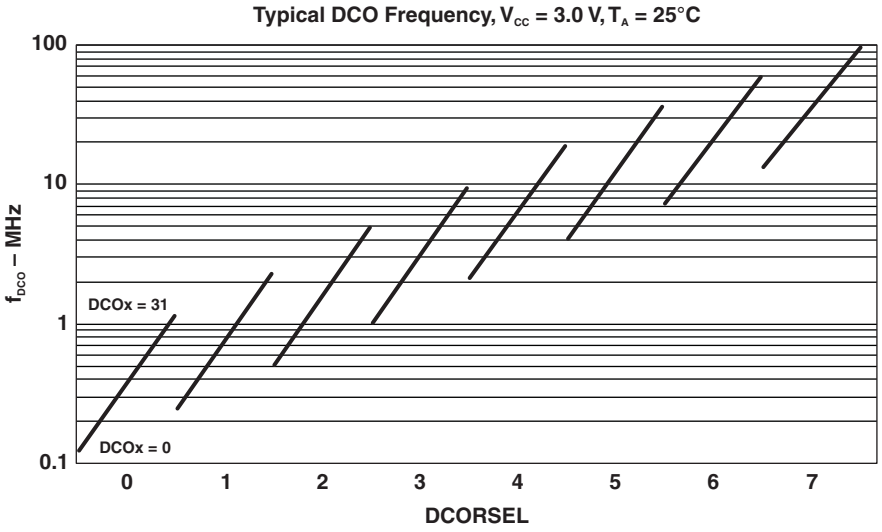


Figure 11. Typical DCO frequency

PMM, Brown-Out Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V(DV_{CC}\_BOR\_IT-)$	BOR_H on voltage, DV_{CC} falling level	$\lvert dDV_{CC}/d_t \rvert < 3$ V/s			1.45	V
$V(DV_{CC}\_BOR\_IT+)$	BOR_H off voltage, DV_{CC} rising level	$\lvert dDV_{CC}/d_t \rvert < 3$ V/s	0.80	1.30	1.50	V
$V(DV_{CC}\_BOR\_hys)$	BOR_H hysteresis		60		250	mV
t_{RESET}	Pulse length required at $\overline{RST}$/NMI pin to accept a reset		2			µs

PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CORE3}(AM)	Core voltage, active mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V, 0 mA ≤ I(V_{CORE}) ≤ 21 mA		1.90		V
V_{CORE2}(AM)	Core voltage, active mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V, 0 mA ≤ I(V_{CORE}) ≤ 21 mA		1.80		V
V_{CORE1}(AM)	Core voltage, active mode, PMMCOREV = 1	2 V ≤ DV_{CC} ≤ 3.6 V, 0 mA ≤ I(V_{CORE}) ≤ 17 mA		1.60		V
V_{CORE0}(AM)	Core voltage, active mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V, 0 mA ≤ I(V_{CORE}) ≤ 13 mA		1.40		V
V_{CORE3}(LPM)	Core voltage, low-current mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V, 0 µA ≤ I(V_{CORE}) ≤ 30 µA		1.94		V
V_{CORE2}(LPM)	Core voltage, low-current mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V, 0 µA ≤ I(V_{CORE}) ≤ 30 µA		1.84		V
V_{CORE1}(LPM)	Core voltage, low-current mode, PMMCOREV = 1	2 V ≤ DV_{CC} ≤ 3.6 V, 0 µA ≤ I(V_{CORE}) ≤ 30 µA		1.64		V
V_{CORE0}(LPM)	Core voltage, low-current mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V, 0 µA ≤ I(V_{CORE}) ≤ 30 µA		1.44		V

PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSH)}$	SVS current consumption	SVSHE = 0, DV_{CC} = 3.6 V		0		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 0		200		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 1		2.0		µA
$V_{(SVSH\_IT-)}$	SVS_H on voltage level(1)	SVSHE = 1, SVSHRVL = 0	1.59	1.64	1.69	V
		SVSHE = 1, SVSHRVL = 1	1.79	1.84	1.91	
		SVSHE = 1, SVSHRVL = 2	1.98	2.04	2.11	
		SVSHE = 1, SVSHRVL = 3	2.10	2.16	2.23	
$V_{(SVSH\_IT+)}$	SVS_H off voltage level(1)	SVSHE = 1, SVSMHRRL = 0	1.62	1.74	1.81	V
		SVSHE = 1, SVSMHRRL = 1	1.88	1.94	2.01	
		SVSHE = 1, SVSMHRRL = 2	2.07	2.14	2.21	
		SVSHE = 1, SVSMHRRL = 3	2.20	2.26	2.33	
		SVSHE = 1, SVSMHRRL = 4	2.32	2.40	2.48	
		SVSHE = 1, SVSMHRRL = 5	2.56	2.70	2.84	
		SVSHE = 1, SVSMHRRL = 6	2.85	3.00	3.15	
		SVSHE = 1, SVSMHRRL = 7	2.85	3.00	3.15	

(1) The SVS_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208) on recommended settings and usage.

PMM, SVS High Side (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd(SVSH)}$	SVS_H propagation delay	SVSHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVSHFP = 1		2.5		µs
		SVSHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVSHFP = 0		20		
$t_{(SVSH)}$	SVS_H on/off delay time	SVSHE = 0→1, SVSHFP = 1		12.5		µs
		SVSHE = 0→1, SVSHFP = 0		100		
dV_{DVCC}/dt	DV_{CC} rise time		0		1000	V/s

PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVMH)}$	SVM_H current consumption	SVMHE = 0, DVCC = 3.6 V		0		nA
		SVMHE = 1, DVCC = 3.6 V, SVMHFP = 0		200		nA
		SVMHE = 1, DVCC = 3.6 V, SVMHFP = 1		2.0		µA
$V_{(SVMH)}$	SVM_H on or off voltage level[1]	SVMHE = 1, SVSMHRRL = 0	1.65	1.74	1.86	V
		SVMHE = 1, SVSMHRRL = 1	1.85	1.94	2.02	
		SVMHE = 1, SVSMHRRL = 2	2.02	2.14	2.22	
		SVMHE = 1, SVSMHRRL = 3	2.18	2.26	2.35	
		SVMHE = 1, SVSMHRRL = 4	2.32	2.40	2.48	
		SVMHE = 1, SVSMHRRL = 5	2.56	2.70	2.84	
		SVMHE = 1, SVSMHRRL = 6	2.85	3.00	3.15	
		SVMHE = 1, SVSMHRRL = 7	2.85	3.00	3.15	
		SVMHE = 1, SVMHOVPE = 1		3.75		
$t_{pd(SVMH)}$	SVM_H propagation delay	SVMHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVMHFP = 1		2.5		µs
		SVMHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVMHFP = 0		20		µs
$t_{(SVMH)}$	SVM_H on or off delay time	SVMHE = 0→1, SVSMFP = 1		12.5		µs
		SVMHE = 0→1, SVMHFP = 0		100		µs

(1) The SVM_H settings available depend on the VCORE (PMMCOREVx) setting. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208) on recommended settings and usage.

PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSL)}$	SVS_L current consumption	SVSLE = 0, PMMCOREV = 2		0		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 0		200		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 1		2.0		µA
$t_{pd(SVSL)}$	SVS_L propagation delay	SVSLE = 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		2.5		µs
		SVSLE = 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		20		
$t_{(SVSL)}$	SVS_L on/off delay time	SVSLE = 0→1, SVSLFP = 1		12.5		µs
		SVSLE = 0→1, SVSLFP = 0		100		

PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVML)}$	SVM_L current consumption	SVMLE = 0, PMMCOREV = 2		0		nA
		SVMLE = 1, PMMCOREV = 2, SVMLFP = 0		200		nA
		SVMLE = 1, PMMCOREV = 2, SVMLFP = 1		2.0		µA

PMM, SVM Low Side (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{pd(SVML)}$	SVM_L propagation delay	SVMLE = 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		2.5		µs
		SVMLE = 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		20		
$t_{(SVML)}$	SVM_L on/off delay time	SVMLE = 0→1, SVMLFP = 1		12.5		µs
		SVMLE = 0→1, SVMLFP = 0		100		

Wake-Up From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{WAKE-UP-FAST}$	Wake-up time from LPM2, LPM3, or LPM4 to active mode(1)	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1	f_{MCLK} ≥ 4 MHz		3	6.5	µs
			1 MHz < f_{MCLK} < 4 MHz		4	8.0	
$t_{WAKE-UP-SLOW}$	Wake-up time from LPM2, LPM3 or LPM4 to active mode(2)	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0			150	165	µs
$t_{WAKE-UP-LPM5}$	Wake-up time from LPM3.5 or LPM4.5 to active mode(3)				2	3	ms
$t_{WAKE-UP-RESET}$	Wake-up time from $\overline{RST}$ or BOR event to active mode(3)				2	3	ms

(1) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low-side supervisor (SVS_L) and low side monitor (SVM_L). Fastest wakeup times are possible with $SVS_L$and SVM_L in full performance mode or disabled when operating in AM, LPM0, and LPM1. Various options are available for $SVS_L$and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

(2) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low-side supervisor (SVS_L) and low side monitor (SVM_L). In this case, the $SVS_L$and SVM_L are in normal mode (low current) mode when operating in AM, LPM0, and LPM1. Various options are available for $SVS_L$and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

(3) This value represents the time from the wakeup event to the reset vector execution.

Timer_A, Timers TA0, TA1, and TA2

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ± 10%	1.8 V, 3 V			20	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs, Minimum pulse duration required for capture	1.8 V, 3 V	20			ns

Timer_B, Timer TB0

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TB}	Timer_B input clock frequency	Internal: SMCLK, ACLK External: TBCLK Duty cycle = 50% ± 10%	1.8 V, 3 V			20	MHz
$t_{TB,cap}$	Timer_B capture timing	All capture inputs, Minimum pulse duration required for capture	1.8 V, 3 V	20			ns

Battery Backup

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
I_{VBAT}	Current into VBAT terminal in case no primary battery is connected.	VBAT = 1.7 V, DVCC not connected, RTC running	T_A = -40°C			0.43		µA
			T_A = 25°C			0.52		
			T_A = 60°C			0.58		
			T_A = 85°C			0.64		
		VBAT = 2.2 V, DVCC not connected, RTC running	T_A = -40°C			0.50		µA
			T_A = 25°C			0.59		
			T_A = 60°C			0.64		
			T_A = 85°C			0.71		
		VBAT = 3 V, DVCC not connected, RTC running	T_A = -40°C			0.68		µA
			T_A = 25°C			0.75		
			T_A = 60°C			0.79		
			T_A = 85°C			0.86		
V_{SWITCH}	Switch-over level (V_{CC} to VBAT)	C_{VCC} = 4.7 µF	General			V_{SVSH_IT-}		V
			SVSHRL = 0		1.59		1.69	
			SVSHRL = 1		1.79		1.91	
			SVSHRL = 2		1.98		2.11	
			SVSHRL = 3		2.10		2.23	
R_{ON_VBAT}	On-resistance of switch between VBAT and VBAK	V_{BAT} = 1.8 V		0 V		0.35	1	kΩ
V_{BAT3}	VBAT to ADC input channel 12: V_{BAT} divide, $V_{BAT3} \neq V_{BAT}$ /3			1.8 V		0.6	±5%	V
				3 V		1.0	±5%	
				3.6 V		1.2	±5%	
$t_{Sample,VBAT3}$	VBAT to ADC: Sampling time required if VBAT3 selected	ADC12ON = 1, Error of conversion result ≤ 1 LSB			1000			ns
V_{CHVx}	Charger end voltage	CHVx = 2			2.65	2.7	2.9	V
R_{CHARGE}	Charge limiting resistor		CHCx = 1				5	kΩ
			CHCx = 2				10	
			CHCx = 3				20	

USCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)					1	MHz
t_τ	UART receive deglitch time(1)		2.2 V	50		600	ns
			3 V	50		600	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

USCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)
(see Figure 12 and)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	SMCLK, ACLK, Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
$t_{SU,MI}$	SOMI input data setup time	PMMCOREV = 0	1.8 V	55			ns
			3 V	38			
		PMMCOREV = 3	2.4 V	30			ns
			3 V	25			
$t_{HD,MI}$	SOMI input data hold time	PMMCOREV = 0	1.8 V	0			ns
			3 V	0			
		PMMCOREV = 3	2.4 V	0			ns
			3 V	0			
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF, PMMCOREV = 0	1.8 V			20	ns
			3 V			18	
		UCLK edge to SIMO valid, C_L = 20 pF, PMMCOREV = 3	2.4 V			16	ns
			3 V			15	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF, PMMCOREV = 0	1.8 V	-10			ns
			3 V	-8			
		C_L = 20 pF, PMMCOREV = 3	2.4 V	-10			ns
			3 V	-8			

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(USCI)} + t_{SU,SI(Slave)}, t_{SU,MI(USCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 12 and .
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 12 and .

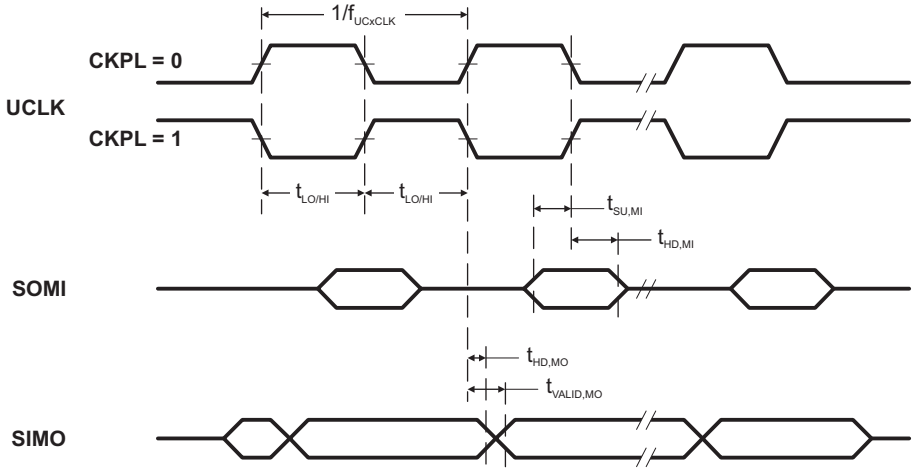


Figure 12. SPI Master Mode, CKPH = 0

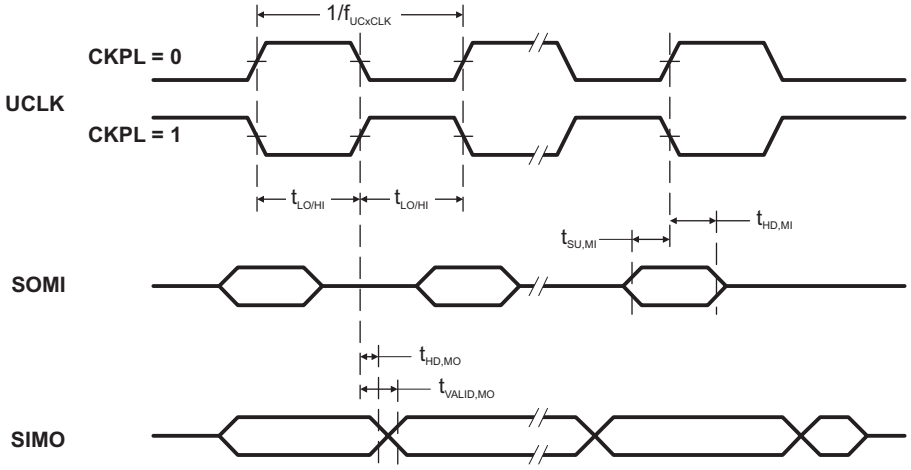


Figure 13. SPI Master Mode, CKPH = 1

USCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)
(see Figure 14 and Figure 15)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE low to clock	PMMCOREV = 0	1.8 V	11			ns
			3 V	8			
		PMMCOREV = 3	2.4 V	7			ns
			3 V	6			
$t_{STE,LAG}$	STE lag time, Last clock to STE high	PMMCOREV = 0	1.8 V	3			ns
			3 V	3			
		PMMCOREV = 3	2.4 V	3			ns
			3 V	3			
$t_{STE,ACC}$	STE access time, STE low to SOMI data out	PMMCOREV = 0	1.8 V			66	ns
			3 V			50	
		PMMCOREV = 3	2.4 V			36	ns
			3 V			30	
$t_{STE,DIS}$	STE disable time, STE high to SOMI high impedance	PMMCOREV = 0	1.8 V			30	ns
			3 V			23	
		PMMCOREV = 3	2.4 V			16	ns
			3 V			13	
$t_{SU,SI}$	SIMO input data setup time	PMMCOREV = 0	1.8 V	5			ns
			3 V	5			
		PMMCOREV = 3	2.4 V	2			ns
			3 V	2			
$t_{HD,SI}$	SIMO input data hold time	PMMCOREV = 0	1.8 V	5			ns
			3 V	5			
		PMMCOREV = 3	2.4 V	5			ns
			3 V	5			
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF, PMMCOREV = 0	1.8 V			76	ns
			3 V			60	
		UCLK edge to SOMI valid, C_L = 20 pF, PMMCOREV = 3	2.4 V			44	ns
			3 V			40	
$t_{HD,SO}$	SOMI output data hold time(3)	C_L = 20 pF, PMMCOREV = 0	1.8 V	18			ns
			3 V	12			
		C_L = 20 pF, PMMCOREV = 3	2.4 V	10			ns
			3 V	8			

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(USCI)}, t_{SU,MI(Master)} + t_{VALID,SO(USCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in Figure 14 and Figure 15.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in Figure 14 and Figure 15.

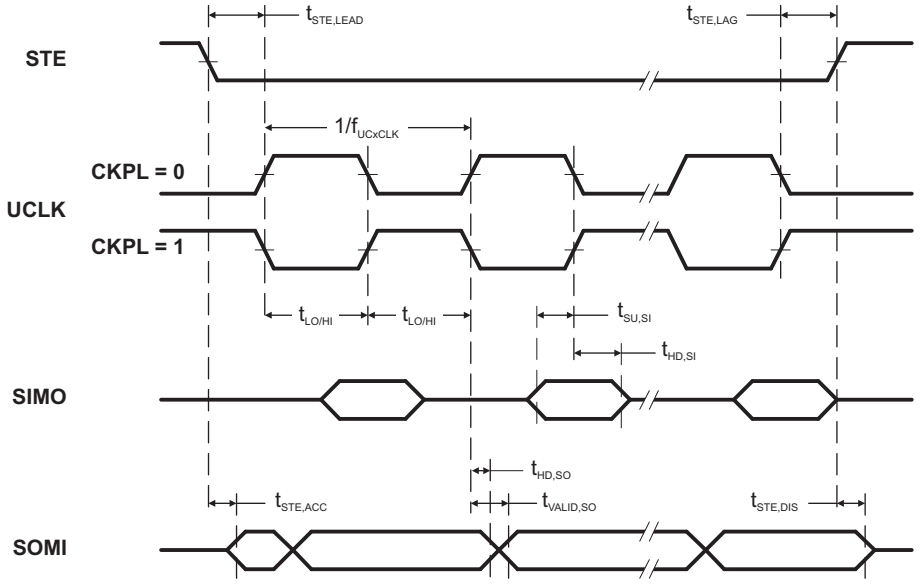


Figure 14. SPI Slave Mode, CKPH = 0

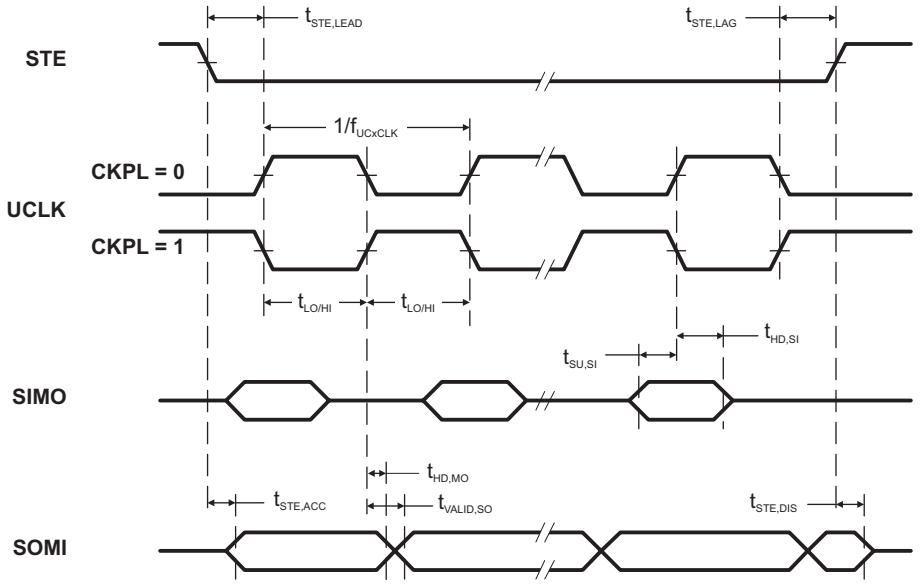


Figure 15. SPI Slave Mode, CKPH = 1

USCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 16)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{USCI}	USCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2.2 V, 3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	$f_{SCL} \le 100$ kHz	2.2 V, 3 V	4.0			µs
		$f_{SCL} > 100$ kHz		0.6			
$t_{SU,STA}$	Setup time for a repeated START	$f_{SCL} \le 100$ kHz	2.2 V, 3 V	4.7			µs
		$f_{SCL} > 100$ kHz		0.6			
$t_{HD,DAT}$	Data hold time		2.2 V, 3 V	0			ns
$t_{SU,DAT}$	Data setup time		2.2 V, 3 V	250			ns
$t_{SU,STO}$	Setup time for STOP	$f_{SCL} \le 100$ kHz	2.2 V, 3 V	4.0			µs
		$f_{SCL} > 100$ kHz		0.6			
t_{SP}	Pulse width of spikes suppressed by input filter		2.2 V	50		600	ns
			3 V	50		600	

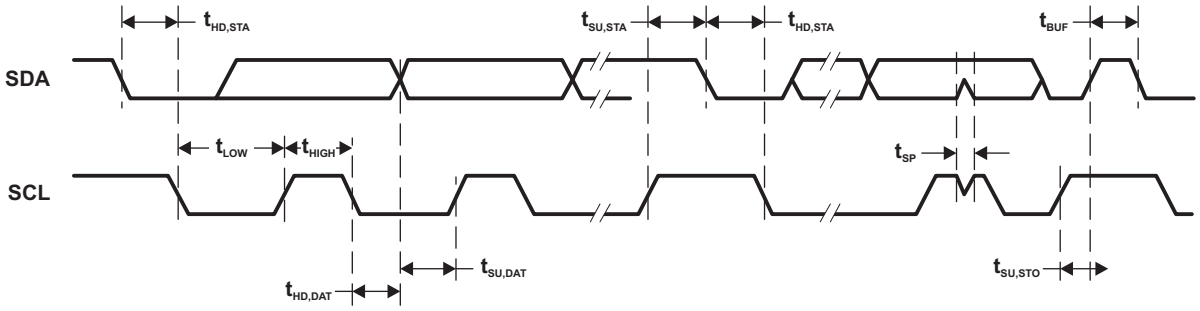


Figure 16. I2C Mode Timing

12-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AVCC and DVCC are connected together, AVSS and DVSS are connected together, V(AVSS) = V(DVSS) = 0 V		2.2		3.6	V
$V_{(Ax)}$	Analog input voltage range(2)	All ADC12 analog input pins Ax		0		AV_{CC}	V
I_{ADC12_A}	Operating supply current into AV_{CC} terminal(3)	$f_{ADC12CLK}$ = 5 MHz(4)	2.2 V		150	200	µA
			3 V		150	250	
C_I	Input capacitance	Only one terminal Ax can be selected at one time	2.2 V		20	25	pF
R_I	Input MUX ON resistance	0 V ≤ VIN ≤ V(AVCC)		10	200	1900	Ω

(1) The leakage current is specified by the digital I/O input leakage.
(2) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. If the reference voltage is supplied by an external source or if the internal voltage is used and REFOUT = 1, then decoupling capacitors are required. See REF, External Reference and REF, Built-In Reference.
(3) The internal reference supply current is not included in current consumption parameter I_{ADC12}.
(4) ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0

12-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$	ADC conversion clock	For specified performance of ADC12 linearity parameters using an external reference voltage or AVCC as reference(1)	2.2 V, 3 V	0.45	4.8	5.0	MHz
		For specified performance of ADC12 linearity parameters using the internal reference(2)		0.45	2.4	4.0	
		For specified performance of ADC12 linearity parameters using the internal reference(3)		0.45	2.4	2.7	
$f_{ADC12OSC}$	Internal ADC12 oscillator(4)	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V, 3 V	4.2	4.8	5.4	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, ADC12OSC used for ADC conversion clock	2.2 V, 3 V	2.4		3.1	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK or SMCLK, ADC12SSEL ≠ 0			(5)		
t_{Sample}	Sampling time	R_S = 400 Ω, R_I = 200 Ω, C_I = 20 pF, $\tau = [R_S + R_I] \times C_I$(6)	2.2 V, 3 V	1000			ns

(1) REFOUT = 0, external reference voltage: SREF2 = 0, SREF1 = 1, SREF0 = 0. AVCC as reference voltage: SREF2 = 0, SREF1 = 0, SREF0 = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC. For other clock sources, the specified performance of the ADC12 linearity is ensured with $f_{ADC12CLK}$ maximum of 5 MHz.
(2) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 1
(3) SREF2 = 0, SREF1 = 1, SREF0 = 0, ADC12SR = 0, REFOUT = 0. The specified performance of the ADC12 linearity is ensured when using the ADC12OSC divided by 2.
(4) The ADC12OSC is sourced directly from MODOSC inside the UCS.
(5) 13 × ADC12DIV × $1/f_{ADC12CLK}$
(6) Approximately ten Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, R_S = external source resistance

12-Bit ADC, Linearity Parameters Using an External Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error(1)	1.4 V ≤ dVREF ≤ 1.6 V(2)	2.2 V, 3 V			±2	LSB
		1.6 V < dVREF (2)				±1.7	
E_D	Differential linearity error(1)	(2)	2.2 V, 3 V			±1	LSB
E_O	Offset error(3)	dVREF ≤ 2.2 V(2)	2.2 V, 3 V		±3	±5.6	LSB
		dVREF > 2.2 V(2)	2.2 V, 3 V		±1.5	±3.5	
E_G	Gain error(3)	(2)	2.2 V, 3 V		±1	±2.5	LSB
E_T	Total unadjusted error	dVREF ≤ 2.2 V(2)	2.2 V, 3 V		±3.5	±7.1	LSB
		dVREF > 2.2 V(2)	2.2 V, 3 V		±2	±5	

(1) Parameters are derived using the histogram method.
(2) The external reference voltage is selected by: SREF2 = 0 or 1, SREF1 = 1, SREF0 = 0. dVREF = V_{R+} - V_{R-}. V_{R+} < AVCC. V_{R-} > AVSS. Unless otherwise mentioned, dVREF > 1.5 V. Impedance of the external reference voltage R < 100 Ω, and two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF+/VREF- to decouple the dynamic current. See also the *MSP430F5xx and MSP430F6xx Family User's Guide* (SLAU208).
(3) Parameters are derived using a best fit curve.

12-Bit ADC, Linearity Parameters Using AVCC as Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error(1)	See (2)	2.2 V, 3 V			±1.7	LSB
E_D	Differential linearity error(1)	See (2)	2.2 V, 3 V			±1	LSB

(1) Parameters are derived using the histogram method.
(2) AVCC as reference voltage is selected by: SREF2 = 0, SREF1 = 0, SREF0 = 0.

12-Bit ADC, Linearity Parameters Using AVCC as Reference Voltage (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_O	Offset error(3)	See (2)	2.2 V, 3 V		±1	±2	LSB
E_G	Gain error(3)	See (2)	2.2 V, 3 V		±2	±4	LSB
E_T	Total unadjusted error	See (2)	2.2 V, 3 V		±2	±5	LSB

(3) Parameters are derived using a best fit curve.

12-Bit ADC, Linearity Parameters Using the Internal Reference Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error(2)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V			±1.7	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz				±2.5	
E_D	Differential linearity error(2)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V	-1		+1.5	LSB
		ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 2.7 MHz				±1	
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz		-1		+2.5	
E_O	Offset error(3)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±2	±4	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz			±2	±4	
E_G	Gain error(3)	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±1	±2.5	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz				±1%(4)	VREF
E_T	Total unadjusted error	ADC12SR = 0, REFOUT = 1	$f_{ADC12CLK}$ ≤ 4.0 MHz	2.2 V, 3 V		±2	±5	LSB
		ADC12SR = 0, REFOUT = 0	$f_{ADC12CLK}$ ≤ 2.7 MHz				±1%(4)	VREF

(1) The external reference voltage is selected by: SREF2 = 0, SREF1 = 0, SREF0 = 1. dVREF = V_{R+} - V_{R-}.
(2) Parameters are derived using the histogram method.
(3) Parameters are derived using a best fit curve.
(4) The gain error and the total unadjusted error are dominated by the accuracy of the integrated reference module absolute accuracy. In this mode the reference voltage used by the ADC12_A is not available on a pin.

12-Bit ADC, Temperature Sensor and Built-In V_{MID}

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{SENSOR}	See (1)	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		680		mV
			3 V		680		
TC_{SENSOR}		ADC12ON = 1, INCH = 0Ah	2.2 V		2.25		mV/°C
			3 V		2.25		
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected(2)(3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	100			µs
			3 V	100			
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, V_{MID} is approximately 0.5 × V_{AVCC}	2.2 V	1.06	1.1	1.14	V
			3 V	1.46	1.5	1.54	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected(4)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V, 3 V	1000			ns

(1) The temperature sensor is provided by the REF module. See the REF module parametric, I_{REF+}, regarding the current consumption of the temperature sensor.
(2) The temperature sensor offset can be significant. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor. The TLV structure contains calibration values for 30°C ± 3°C and 85°C ± 3°C for each of the available reference voltage levels. The sensor voltage can be computed as V_{SENSE} = TC_{SENSOR} × (Temperature,°C) + V_{SENSOR}, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy. See also the *MSP430F5xx and MSP430F6xx Family User's Guide* (SLAU208).
(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(4) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

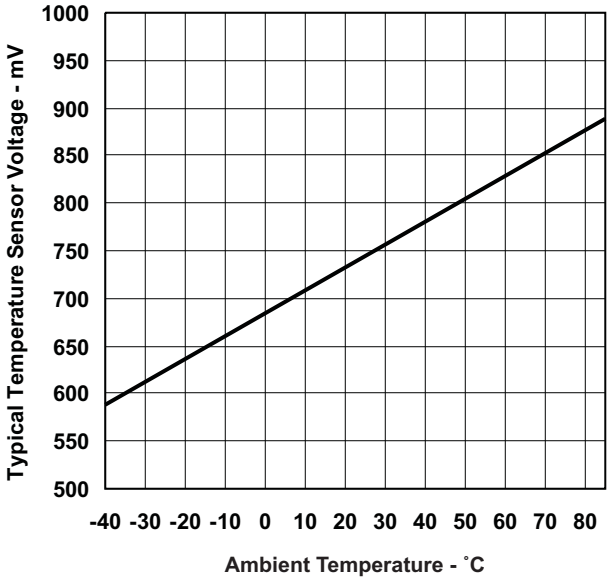


Figure 17. Typical Temperature Sensor Voltage

REF, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (2)		1.4		AV_{CC}	V
V_{REF-}/V_{eREF-}	Negative external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (3)		0		1.2	V
$V_{eREF+} - V_{REF-}/V_{eREF-}$	Differential external reference voltage input	$V_{eREF+} > V_{REF-}/V_{eREF-}$ (4)		1.4		AV_{CC}	V
I_{VeREF+}, $I_{VREF-/VeREF-}$	Static input current	1.4 V ≤ V_{eREF+} ≤ V_{AVCC} , V_{eREF-} = 0 V, $f_{ADC12CLK}$ = 5 MHz, ADC12SHTx = 1h, Conversion rate 200 ksps	2.2 V, 3 V	-26		26	µA
		1.4 V ≤ V_{eREF+} ≤ V_{AVCC} , V_{eREF-} = 0 V, $f_{ADC12CLK}$ = 5 MHZ, ADC12SHTx = 8h, Conversion rate 20 ksps	2.2 V, 3 V	-1.2		+1.2	µA
$C_{VREF+/-}$	Capacitance at $V_{REF+/-}$ terminal(5)			10			µF

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_i, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(5) Two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_A. See also the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REFVSEL = {2} for 2.5 V, REFON = REFOUT = 1 , I_{VREF+} = 0 A		3 V		2.5	±1%	V
		REFVSEL = {1} for 2 V, REFON = REFOUT = 1, I_{VREF+} = 0 A		3 V		2.0	±1%	
		REFVSEL = {0} for 1.5 V, REFON = REFOUT = 1, I_{VREF+} = 0 A		2.2 V, 3 V		1.5	±1%	
$AV_{CC(min)}$	AV_{CC} minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.5 V			2.2			V
		REFVSEL = {1} for 2 V			2.3			
		REFVSEL = {2} for 2.5 V			2.8			
I_{REF+}	Operating supply current into AV_{CC} terminal (2) (3)	ADC12SR = 1(4), REFON = 1, REFOUT = 0, REFBURST = 0		3 V		70	100	µA
		ADC12SR = 1(4), REFON = 1, REFOUT = 1, REFBURST = 0		3 V		0.45	0.75	mA
		ADC12SR = 0(4), REFON = 1, REFOUT = 0, REFBURST = 0		3 V		210	310	µA
		ADC12SR = 0(4), REFON = 1, REFOUT = 1, REFBURST = 0		3 V		0.95	1.7	mA
$I_{L(VREF+)}$	Load-current regulation, V_{REF+} terminal(5)	REFVSEL = {0, 1, 2} I_{VREF+} = +10 µA / -1000 µA AV_{CC} = $AV_{CC(min)}$ for each reference level, REFVSEL = {0, 1, 2}, REFON = REFOUT = 1				1500	2500	µV/mA
C_{VREF+}	Capacitance at V_{REF+} terminal	REFON = REFOUT = 1, (6) 0 mA ≤ I_{VREF+} ≤ I_{VREF+}(max)		2.2 V, 3 V	20		100	pF
TC_{REF+}	Temperature coefficient of built-in reference(7)	I_{VREF+} is a constant in the range of 0 mA ≤ I_{VREF+} ≤ –1 mA	REFOUT = 0	2.2 V, 3 V		20		ppm/°C
TC_{REF+}	Temperature coefficient of built-in reference(7)	I_{VREF+} is a constant in the range of 0 mA ≤ I_{VREF+} ≤ –1 mA	REFOUT = 1	2.2 V, 3 V		20	50	ppm/°C
PSRR_DC	Power supply rejection ratio (dc)	AV_{CC} = $AV_{CC(min)}$ - $AV_{CC(max)}$, T_A = 25°C, REFVSEL = {0, 1, 2}, REFON = 1, REFOUT = 0 or 1				120	300	µV/V
PSRR_AC	Power supply rejection ratio (ac)	AV_{CC} = $AV_{CC(min)}$ - $AV_{CC(max)}$, T_A = 25°C, REFVSEL = {0, 1, 2}, REFON = 1, REFOUT = 0 or 1				1		mV/V

(1) The reference is supplied to the ADC by the REF module and is buffered locally inside the ADC. The ADC uses two internal buffers, one smaller and one larger for driving the V_{REF+} terminal. When REFOUT = 1, the reference is available at the V_{REF+} terminal, as well as, used as the reference for the conversion and utilizes the larger buffer. When REFOUT = 0, the reference is only used as the reference for the conversion and utilizes the smaller buffer.
(2) The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC12ON control bit, unless a conversion is active. REFOUT = 0 represents the current contribution of the smaller buffer. REFOUT = 1 represents the current contribution of the larger buffer without external load.
(3) The temperature sensor is provided by the REF module. Its current is supplied via terminal AVCC and is equivalent to I_{REF+} with REFON = 1 and REFOUT = 0.
(4) For devices without the ADC12, the parametric with ADC12SR = 0 are applicable.
(5) Contribution only due to the reference and buffer including package. This does not include resistance due to PCB traces or other external factors.
(6) Two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC12_A. See also the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).
(7) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C)/(85°C – (–40°C)).

REF, Built-In Reference (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{SETTLE}	Settling time of reference voltage(8)	$AV_{CC} = AV_{CC(min)}$ - $AV_{CC(max)}$, REFVSEL = {0, 1, 2}, REFOUT = 0, REFON = 0 → 1			75		µs
		$AV_{CC} = AV_{CC(min)}$ - $AV_{CC(max)}$, $C_{VREF} = C_{VREF}$(max), REFVSEL = {0, 1, 2}, REFOUT = 1, REFON = 0 → 1			75		

(8) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load when REFOUT = 1.

12-Bit DAC, Supply Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS} = 0$ V		2.20		3.60	V
I_{DD}	Supply current, single DAC channel(1) (2)	DAC12AMPx = 2, DAC12IR = 0, DAC12OG = 1, DAC12_xDAT = 0800h, VeREF+ = VREF+ = 1.5 V	3 V		65	110	µA
		DAC12AMPx = 2, DAC12IR = 1, DAC12_xDAT = 0800h, VeREF+ = VREF+ = AV_{CC}	2.2 V, 3 V		125	165	
		DAC12AMPx = 5, DAC12IR = 1, DAC12_xDAT = 0800h, VeREF+ = VREF+ = AV_{CC}			250	350	
		DAC12AMPx = 7, DAC12IR = 1, DAC12_xDAT = 0800h, VeREF+ = VREF+ = AV_{CC}			750	1100	
PSRR	Power supply rejection ratio(3) (4)	DAC12_xDAT = 800h, VeREF+ = 1.5 V, ΔAV_{CC} = 100 mV	2.2 V		70		dB
		DAC12_xDAT = 800h, VeREF+ = 1.5 V or 2.5 V, ΔAV_{CC} = 100 mV	3 V		70		

(1) No load at the output pin, DAC12_0 or DAC12_1, assuming that the control bits for the shared pins are set properly.
(2) Current into reference terminals not included. If DAC12IR = 1 current flows through the input divider; see Reference Input specifications.
(3) PSRR = 20 log (ΔAV_{CC} / ΔV_{DAC12_xOUT})
(4) The internal reference is not used.

12-Bit DAC, Linearity Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 18)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
	Resolution	12-bit monotonic		12			bits
INL	Integral nonlinearity(1)	VeREF+ = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V		±2	±4(2)	LSB
		VeREF+ = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V		±2	±4	
DNL	Differential nonlinearity(1)	VeREF+ = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V		±0.4	±1(2)	LSB
		VeREF+ = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V		±0.4	±1	

(1) Parameters calculated from the best-fit curve from 0x0F to 0xFFF. The best-fit curve method is used to deliver coefficients "a" and "b" of the first-order equation: y = a + bx. $V_{DAC12\_xOUT} = E_O + (1 + E_G) \times (VeREF+/4095) \times DAC12\_xDAT$, DAC12IR = 1.
(2) This parameter is not production tested.

12-Bit DAC, Linearity Specifications (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 18)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
E_O	Offset voltage	Without calibration (1) (3)	VeREF+ = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V			±21 (2)	mV
			VeREF+ = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V			±21	
		With calibration (1) (3)	VeREF+ = 1.5 V, DAC12AMPx = 7, DAC12IR = 1	2.2 V			±1.5 (2)	
			VeREF+ = 2.5 V, DAC12AMPx = 7, DAC12IR = 1	3 V			±1.5	
$d_{E(O)}/d_T$	Offset error temperature coefficient (1)	With calibration		2.2 V, 3 V		±10		µV/°C
E_G	Gain error	VeREF+ = 1.5 V		2.2 V			±2.5	%FSR
		VeREF+ = 2.5 V		3 V			±2.5	
$d_{E(G)}/d_T$	Gain temperature coefficient (1)			2.2 V, 3 V		10		ppm of FSR/ °C
t_{Offset_Cal}	Time for offset calibration (4)	DAC12AMPx = 2		2.2 V, 3 V			165	ms
		DAC12AMPx = 3, 5					66	
		DAC12AMPx = 4, 6, 7					16.5	

(3) The offset calibration works on the output operational amplifier. Offset Calibration is triggered setting bit DAC12CALON
(4) The offset calibration can be done if DAC12AMPx = {2, 3, 4, 5, 6, 7}. The output operational amplifier is switched off with DAC12AMPx = {0, 1}. It is recommended that the DAC12 module be configured prior to initiating calibration. Port activity during calibration may effect accuracy and is not recommended.

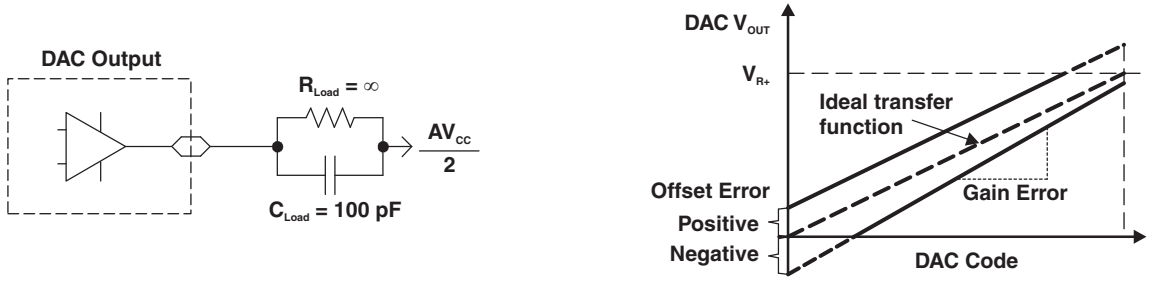


Figure 18. Linearity Test Load Conditions and Gain/Offset Definition

12-Bit DAC, Output Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_O	Output voltage range(1) (see Figure 19)	No load, VeREF+ = AV_{CC}, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7	2.2 V, 3 V	0		0.005	V
		No load, VeREF+ = AV_{CC}, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC} – 0.05		AV_{CC}	
		R_{Load} = 3 kΩ, VeREF+ = AV_{CC}, DAC12_xDAT = 0h, DAC12IR = 1, DAC12AMPx = 7		0		0.1	
		R_{Load} = 3 kΩ, VeREF+ = AV_{CC}, DAC12_xDAT = 0FFFh, DAC12IR = 1, DAC12AMPx = 7		AV_{CC} – 0.13		AV_{CC}	
$C_{L(DAC12)}$	Maximum DAC12 load capacitance		2.2 V, 3 V			100	pF
$I_{L(DAC12)}$	Maximum DAC12 load current	DAC12AMPx = 2, DAC12xDAT = 0FFFh, $V_{O/P(DAC12)}$ > AV_{CC} – 0.3	2.2 V, 3 V	–1			mA
		DAC12AMPx = 2, DAC12xDAT = 0h, $V_{O/P(DAC12)}$ < 0.3 V				1	
$R_{O/P(DAC12)}$	Output resistance (see Figure 19)	R_{Load} = 3 kΩ, VO/P(DAC12) < 0.3 V, DAC12AMPx = 2, DAC12_xDAT = 0h	2.2 V, 3 V		150	250	Ω
		R_{Load} = 3 kΩ, $V_{O/P(DAC12)}$ > AV_{CC} – 0.3 V, DAC12_xDAT = 0FFFh			150	250	
		R_{Load} = 3 kΩ, 0.3 V ≤ $V_{O/P(DAC12)}$ ≤ AV_{CC} – 0.3 V				6	

(1) Data is valid after the offset calibration of the output amplifier.

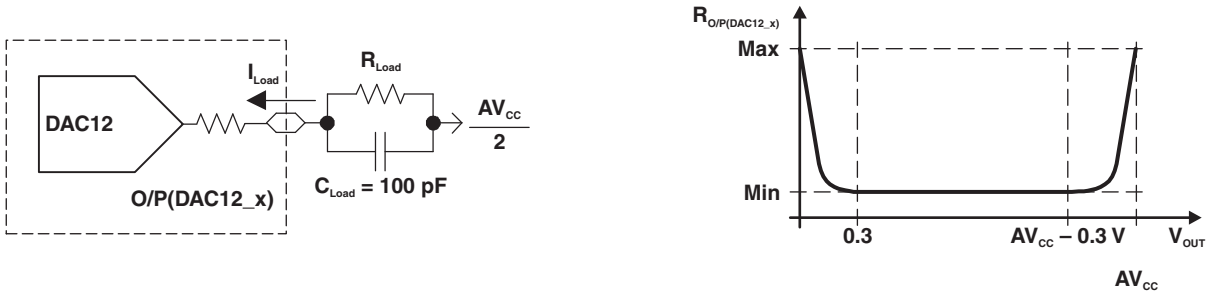


Figure 19. DAC12_x Output Resistance Tests

12-Bit DAC, Reference Input Specifications

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
VeREF+	Reference input voltage range	DAC12IR = 0 (1) (2)	2.2 V, 3 V		AV_{CC} / 3	AV_{CC} + 0.2	V
		DAC12IR = 1 (3) (4)			AV_{CC}	AV_{CC} + 0.2	
$Ri_{(VREF+)}$, $Ri_{(VeREF+)}$	Reference input resistance (5)	DAC12_0 IR = DAC12_1 IR = 0	2.2 V, 3 V	20			MΩ
		DAC12_0 IR = 1, DAC12_1 IR = 0			48		kΩ
		DAC12_0 IR = 0, DAC12_1 IR = 1			48		
		DAC12_0 IR = DAC12_1 IR = 1, DAC12_0 SREFx = DAC12_1 SREFx (6)			24		

(1) For a full-scale output, the reference input voltage can be as high as 1/3 of the maximum output voltage swing (AVCC).
(2) The maximum voltage applied at reference input voltage terminal VeREF+ = $[AV_{CC} – V_{E(O)}] / [3 × (1 + E_G)]$.
(3) For a full-scale output, the reference input voltage can be as high as the maximum output voltage swing (AVCC).
(4) The maximum voltage applied at reference input voltage terminal VeREF+ = $[AV_{CC} – V_{E(O)}] / (1 + E_G)$.
(5) This impedance depends on tradeoff in power savings. Current devices have 48 kΩ for each channel when divide is enabled. Can be increased if performance can be maintained.
(6) When DAC12IR = 1 and DAC12SREFx = 0 or 1 for both channels, the reference input resistive dividers for each DAC are in parallel reducing the reference input resistance.

12-Bit DAC, Dynamic Specifications

$V_{REF} = V_{CC}$, DAC12IR = 1 (see Figure 20 and Figure 21), over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
t_{ON}	DAC12 on time	DAC12_xDAT = 800h, $Error_{V(O)}$ < ±0.5 LSB (1) (see Figure 20)	DAC12AMPx = 0 → {2, 3, 4}	2.2 V, 3 V		60	120	µs
			DAC12AMPx = 0 → {5, 6}			15	30	
			DAC12AMPx = 0 → 7			6	12	
$t_{S(FS)}$	Settling time, full scale	DAC12_xDAT = 80h → F7Fh → 80h	DAC12AMPx = 2	2.2 V, 3 V		100	200	µs
			DAC12AMPx = 3, 5			40	80	
			DAC12AMPx = 4, 6, 7			15	30	
$t_{S(C-C)}$	Settling time, code to code	DAC12_xDAT = 3F8h → 408h → 3F8h, BF8h → C08h → BF8h	DAC12AMPx = 2	2.2 V, 3 V		5		µs
			DAC12AMPx = 3, 5			2		
			DAC12AMPx = 4, 6, 7			1		
SR	Slew rate	DAC12_xDAT = 80h → F7Fh → 80h (2)	DAC12AMPx = 2	2.2 V, 3 V	0.05	0.35		V/µs
			DAC12AMPx = 3, 5		0.35	1.10		
			DAC12AMPx = 4, 6, 7		1.50	5.20		
	Glitch energy	DAC12_xDAT = 800h → 7FFh → 800h	DAC12AMPx = 7	2.2 V, 3 V		35		nV-s

(1) R_{Load} and C_{Load} connected to AV_{SS} (not $AV_{CC}/2$) in Figure 20.
(2) Slew rate applies to output voltage steps ≥ 200 mV.

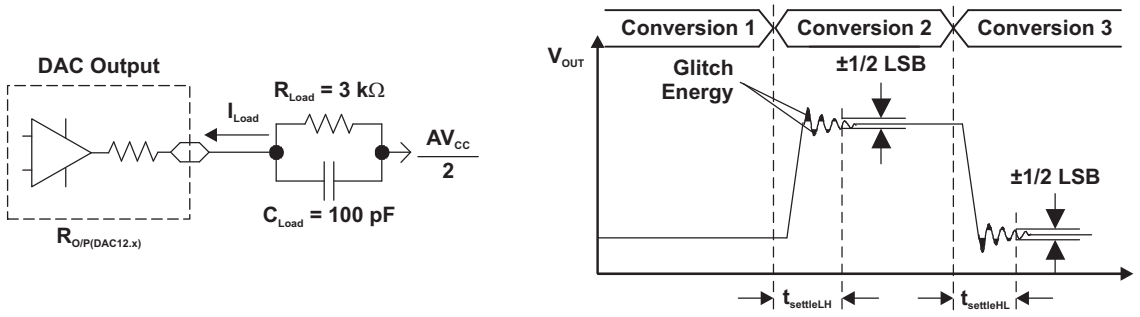


Figure 20. Settling Time and Glitch Energy Testing

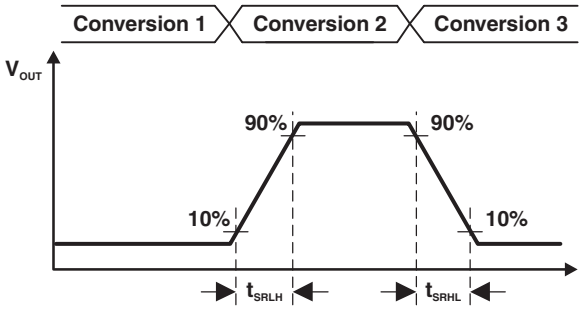


Figure 21. Slew Rate Testing

12-Bit DAC, Dynamic Specifications (Continued)

over recommended ranges of supply voltage and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
BW_{-3dB}	3-dB bandwidth, V_{DC} = 1.5 V, V_{AC} = 0.1 V_{PP} (see Figure 22)	DAC12AMPx = {2, 3, 4}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h	2.2 V, 3 V	40			kHz
		DAC12AMPx = {5, 6}, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		180			
		DAC12AMPx = 7, DAC12SREFx = 2, DAC12IR = 1, DAC12_xDAT = 800h		550			
	Channel-to-channel crosstalk(1) (see Figure 23)	DAC12_0DAT = 800h, No load, DAC12_1DAT = 80h ↔ F7Fh, R_{Load} = 3 kΩ, f_{DAC12_0OUT} = 10 kHz at 50/50 duty cycle	2.2 V, 3 V		–80		dB
		DAC12_0DAT = 80h ↔ F7Fh, R_{Load} = 3 kΩ, DAC12_1DAT = 800h, No load, f_{DAC12_0OUT} = 10 kHz at 50/50 duty cycle			–80		

(1) R_{Load} = 3 kΩ, C_{Load} = 100 pF

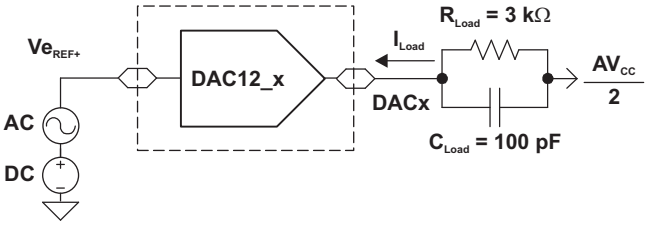


Figure 22. Test Conditions for 3-dB Bandwidth Specification

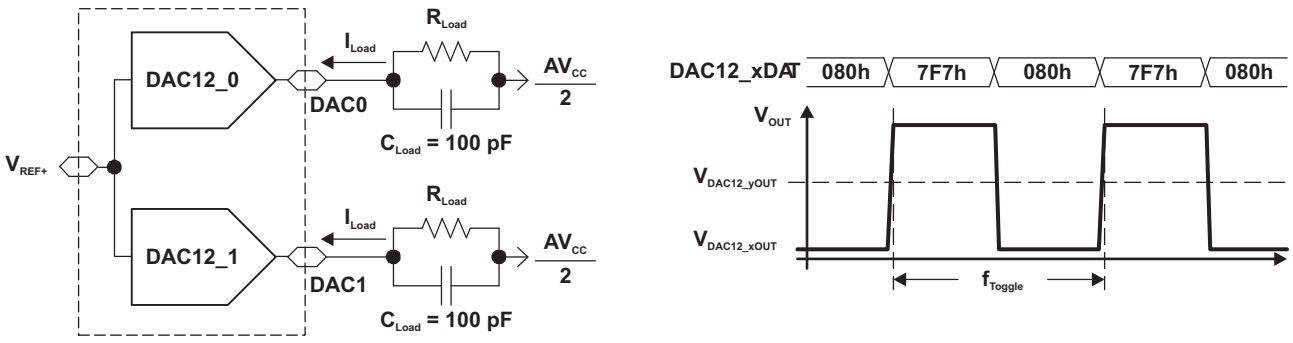


Figure 23. Crosstalk Test Conditions

Comparator_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			1.8		3.6	V
I_{AVCC_COMP}	Comparator operating supply current into AVCC terminal, Excludes reference resistor ladder	CBPWRMD = 00	1.8 V			40	µA
			2.2 V		30	50	
			3 V		40	65	
		CBPWRMD = 01	2.2 V, 3 V		10	30	
		CBPWRMD = 10	2.2 V, 3 V		0.1	0.5	
I_{AVCC_REF}	Quiescent current of local reference voltage amplifier into AVCC terminal	CBREFACC = 1, CBREFLx = 01				22	µA
V_{IC}	Common mode input range			0		V_{CC} - 1	V
V_{OFFSET}	Input offset voltage	CBPWRMD = 00				±20	mV
		CBPWRMD = 01, 10				±10	
C_{IN}	Input capacitance				5		pF
R_{SIN}	Series input resistance	ON - switch closed			3	4	kΩ
		OFF - switch opened		50			MΩ
t_{PD}	Propagation delay, response time	CBPWRMD = 00, CBF = 0				450	ns
		CBPWRMD = 01, CBF = 0				600	ns
		CBPWRMD = 10, CBF = 0				50	µs
$t_{PD,filter}$	Propagation delay with filter active	CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 00		0.35	0.6	1.0	µs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 01		0.6	1.0	1.8	µs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 10		1.0	1.8	3.4	µs
		CBPWRMD = 00, CBON = 1, CBF = 1, CBFDLY = 11		1.8	3.4	6.5	µs
t_{EN_CMP}	Comparator enable time, settling time	CBON = 0 to CBON = 1 CBPWRMD = 00, 01, 10			1	2	µs
t_{EN_REF}	Resistor reference enable time	CBON = 0 to CBON = 1			0.3	1.5	µs
V_{CB_REF}	Reference voltage for a given tap	VIN = reference into resistor ladder, n = 0 to 31		VIN × (n+0.5) / 32	VIN × (n+1) / 32	VIN × (n+1.5) / 32	V

Ports PU.0 and PU.1

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	V_{USB} = 3.3 V ± 10%, I_{OH} = -25 mA		2.4			V
V_{OL}	Low-level output voltage	V_{USB} = 3.3 V ± 10%, I_{OL} = 25 mA				0.4	V
V_{IH}	High-level input voltage	V_{USB} = 3.3 V ± 10%		2.0			V
V_{IL}	Low-level input voltage	V_{USB} = 3.3 V ± 10%				0.8	V

USB Output Ports DP and DM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	D+, D- single ended	USB 2.0 load conditions	2.8		3.6	V
V_{OL}	D+, D- single ended	USB 2.0 load conditions	0		0.3	V
$Z_{(DRV)}$	D+, D- impedance	Including external series resistor of 27 Ω	28		44	Ω
t_{RISE}	Rise time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4		20	ns
t_{FALL}	Fall time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+	4		20	ns

USB Input Ports DP and DM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(CM)}$	Differential input common mode range		0.8		2.5	V
$Z_{(IN)}$	Input impedance		300			kΩ
V_{CRS}	Crossover voltage		1.3		2.0	V
V_{IL}	Static SE input logic low level				0.8	V
V_{IH}	Static SE input logic high level		2.0			V
VDI	Differential input voltage				0.2	V

USB-PWR (USB Power System)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{LAUNCH}	V_{BUS} detection threshold				3.75	V
V_{BUS}	USB bus voltage	Normal operation	3.76		5.5	V
V_{USB}	USB LDO output voltage			3.3	±9%	V
V_{18}	Internal USB voltage(1)			1.8		V
I_{USB_EXT}	Maximum external current from VUSB terminal(2)	USB LDO is on			12	mA
I_{DET}	USB LDO current overload detection(3)		60		100	mA
$I_{SUSPEND}$	Operating supply current into VBUS terminal.(4)	USB LDO is on, USB PLL disabled			250	µA
C_{BUS}	VBUS terminal recommended capacitance			4.7		µF
C_{USB}	VUSB terminal recommended capacitance			220		nF
C_{18}	V18 terminal recommended capacitance			220		nF
t_{ENABLE}	Settling time V_{USB} and V_{18}	Within 2%, recommended capacitances			2	ms
R_{PUR}	Pullup resistance of PUR terminal		70	110	150	Ω

(1) This voltage is for internal use only. No external dc loading should be applied.
(2) This represents additional current that can be supplied to the application from the VUSB terminal beyond the needs of the USB operation.
(3) A current overload is detected when the total current supplied from the USB LDO, including I_{USB_EXT}, exceeds this value.
(4) Does not include current contribution of Rpu and Rpd as outlined in the USB specification.

USB-PLL (USB Phase-Locked Loop)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{PLL}	Operating supply current					7	mA
f_{PLL}	PLL frequency				48		MHz
f_{UPD}	PLL reference frequency			1.5		3	MHz
t_{LOCK}	PLL lock time					2	ms
t_{Jitter}	PLL jitter				1000		ps

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$DV_{CC(PGM/ERASE)}$	Program and erase supply voltage		1.8		3.6	V
I_{PGM}	Average supply current from DVCC during program			3	5	mA
I_{ERASE}	Average supply current from DVCC during erase			6	11	mA
I_{MERASE}, I_{BANK}	Average supply current from DVCC during mass erase or bank erase			6	11	mA
t_{CPT}	Cumulative program time	See (1)			16	ms
	Program and erase endurance		10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C	100			years
t_{Word}	Word or byte program time	See (2)	64		85	µs
$t_{Block, 0}$	Block program time for first byte or word	See (2)	49		65	µs
$t_{Block, 1–(N–1)}$	Block program time for each additional byte or word, except for last byte or word	See (2)	37		49	µs
$t_{Block, N}$	Block program time for last byte or word	See (2)	55		73	µs
$t_{Seg\ Erase}$	Erase time for segment, mass erase, and bank erase when available	See (2)	23		32	ms
$f_{MCLK,MGR}$	MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4.MGR1 = 1)		0		1	MHz

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.
(2) These values are hardwired into the flash controller's state machine.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.2 V, 3 V	0.025		15	µs
$t_{SBW, En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1)	2.2 V, 3 V			1	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	µs
f_{TCK}	TCK input frequency (4-wire JTAG) (2)	2.2 V	0		5	MHz
		3 V	0		10	MHz
$R_{internal}$	Internal pulldown resistance on TEST	2.2 V, 3 V	45	60	80	kΩ

(1) Tools that access the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

INPUT/OUTPUT SCHEMATICS

Port P1, P1.0 to P1.7, Input/Output With Schmitt Trigger

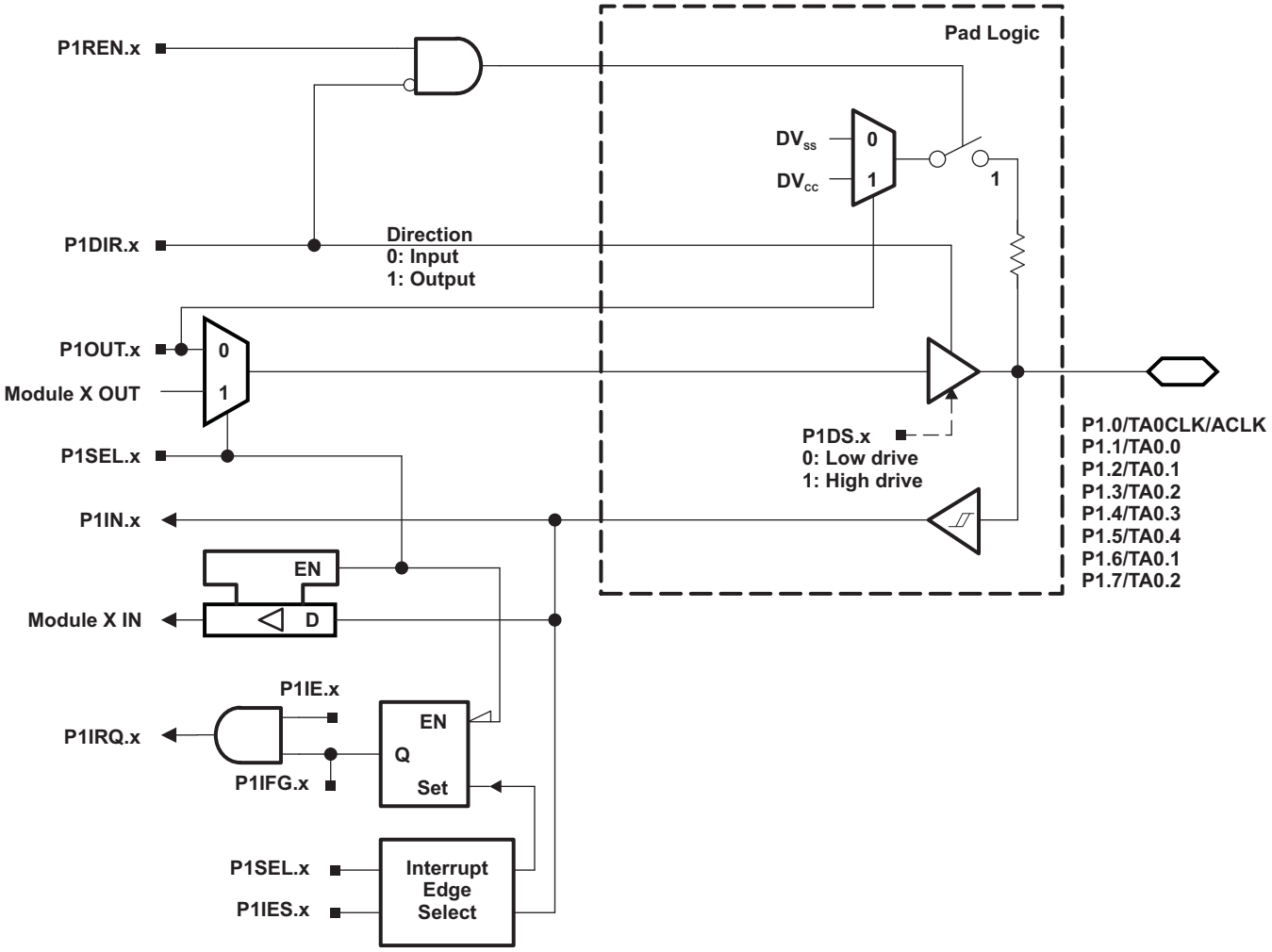


Table 53. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P1DIR.x	P1SEL.x
P1.0/TA0CLK/ACLK	0	P1.0 (I/O)	I: 0; O: 1	0
		Timer TA0.TA0CLK	0	1
		ACLK	1	1
P1.1/TA0.0	1	P1.1 (I/O)	I: 0; O: 1	0
		Timer TA0.CCI0A capture input	0	1
		Timer TA0.0 output	1	1
P1.2/TA0.1	2	P1.2 (I/O)	I: 0; O: 1	0
		Timer TA0.CCI1A capture input	0	1
		Timer TA0.1 output	1	1
P1.3/TA0.2	3	P1.3 (I/O)	I: 0; O: 1	0
		Timer TA0.CCI2A capture input	0	1
		Timer TA0.2 output	1	1
P1.4/TA0.3	4	P1.4 (I/O)	I: 0; O: 1	0
		Timer TA0.CCI3A capture input	0	1
		Timer TA0.3 output	1	1
P1.5/TA0.4	5	P1.5 (I/O)	I: 0; O: 1	0
		Timer TA0.CCI4A capture input	0	1
		Timer TA0.4 output	1	1
P1.6/TA0.1	6	P1.6 (I/O)	I: 0; O: 1	0
		Timer TA0.CCI1B capture input	0	1
		Timer TA0.1 output	1	1
P1.7/TA0.2	7	P1.7 (I/O)	I: 0; O: 1	0
		Timer TA0.CCI2B capture input	0	1
		Timer TA0.2 output	1	1

Port P2, P2.0 to P2.7, Input/Output With Schmitt Trigger

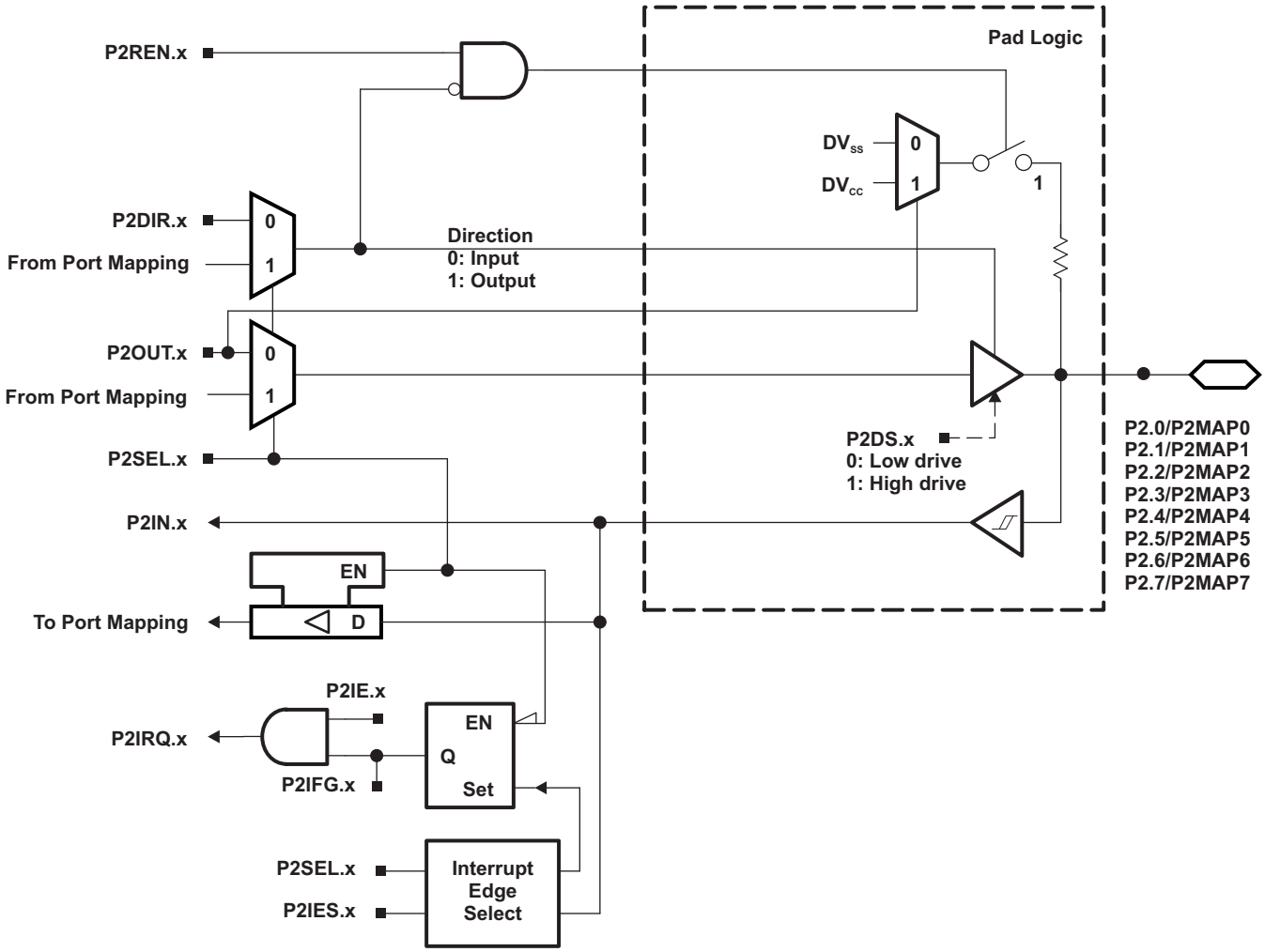


Table 54. Port P2 (P2.0 to P2.7) Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P2DIR.x	P2SEL.x	P2MAPx
P2.0/P2MAP0	0	P2.0 (I/O)	I: 0; O: 1	0	
		Mapped secondary digital function	X	1	≤ 19
P2.1/P2MAP1	1	P2.1 (I/O)	I: 0; O: 1	0	
		Mapped secondary digital function	X	1	≤ 19
P2.2/P2MAP2	2	P2.2 (I/O)	I: 0; O: 1	0	
		Mapped secondary digital function	X	1	≤ 19
P2.3/P2MAP3	3	P2.3 (I/O)	I: 0; O: 1	0	
		Mapped secondary digital function	X	1	≤ 19
P2.4/P2MAP4	4	P2.4 (I/O)	I: 0; O: 1	0	
		Mapped secondary digital function	X	1	≤ 19
P2.5/P2MAP5	5	P2.5 (I/O	I: 0; O: 1	0	
		Mapped secondary digital function	X	1	≤ 19
P2.6/P2MAP6	6	P2.6 (I/O)	I: 0; O: 1	0	
		Mapped secondary digital function	X	1	≤ 19
P2.7/P2MAP7	7	P2.7 (I/O)	I: 0; O: 1	0	
		Mapped secondary digital function	X	1	≤ 19

(1) X = Don't care

Port P3, P3.0 to P3.7, Input/Output With Schmitt Trigger

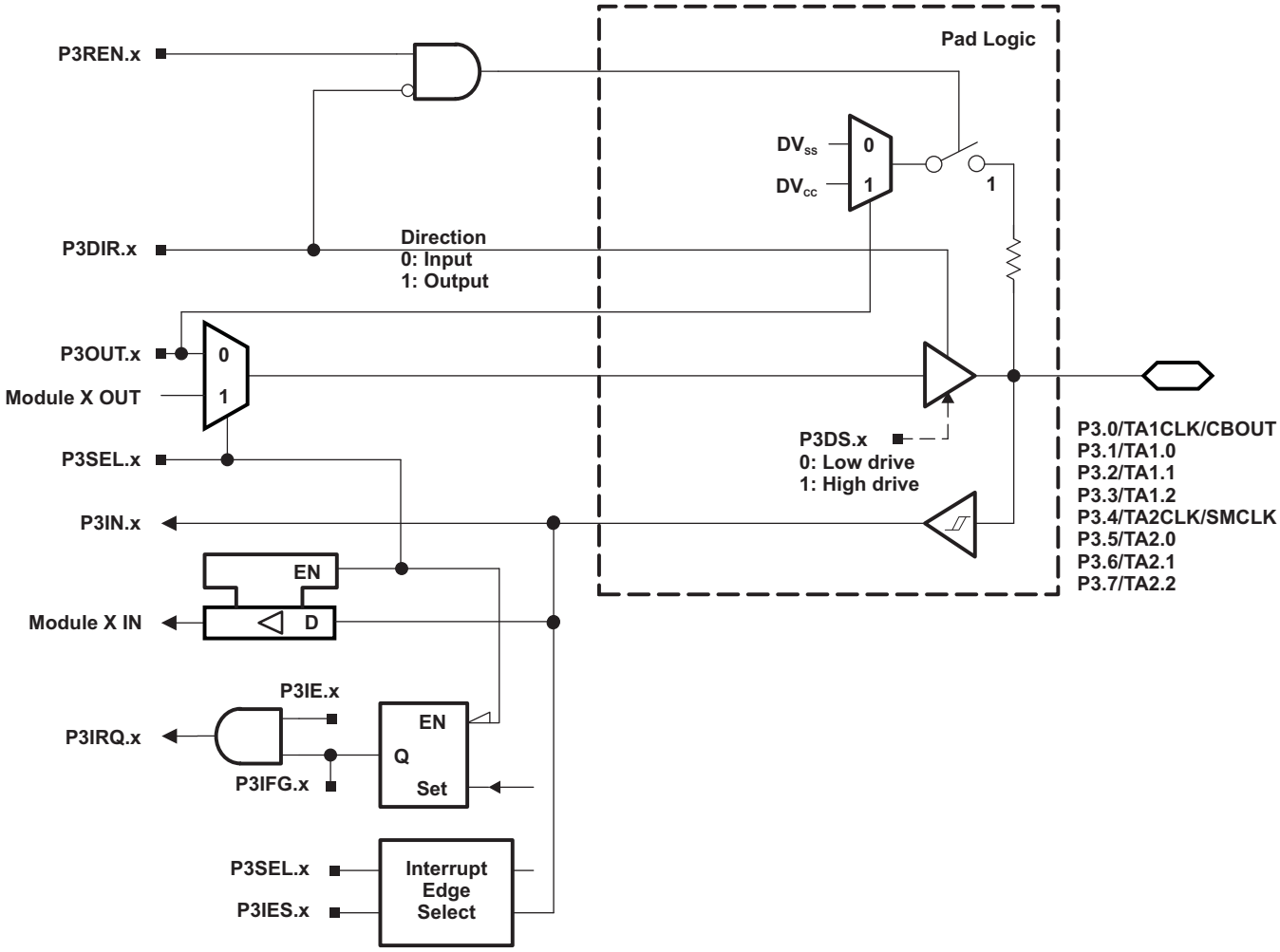


Table 55. Port P3 (P3.0 to P3.7) Pin Functions

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P3DIR.x	P3SEL.x
P3.0/TA1CLK/CBOUT	0	P3.0 (I/O)	I: 0; O: 1	0
		Timer TA1.TA1CLK	0	1
		CBOUT	1	1
P3.1/TA1.0	1	P3.1 (I/O)	I: 0; O: 1	0
		Timer TA1.CCI0A capture input	0	1
		Timer TA1.0 output	1	1
P3.2/TA1.1	2	P3.2 (I/O)	I: 0; O: 1	0
		Timer TA1.CCI1A capture input	0	1
		Timer TA1.1 output	1	1
P3.3/TA1.2	3	P3.3 (I/O)	I: 0; O: 1	0
		Timer TA1.CCI2A capture input	0	1
		Timer TA1.2 output	1	1
P3.4/TA2CLK/SMCLK	4	P3.4 (I/O)	I: 0; O: 1	0
		Timer TA2.TA2CLK	0	1
		SMCLK	1	1
P3.5/TA2.0	5	P3.5 (I/O)	I: 0; O: 1	0
		Timer TA2.CCI0A capture input	0	1
		Timer TA2.0 output	1	1
P3.6/TA2.1	6	P3.6 (I/O)	I: 0; O: 1	0
		Timer TA2.CCI1A capture input	0	1
		Timer TA2.1 output	1	1
P3.7/TA2.2	7	P3.7 (I/O)	I: 0; O: 1	0
		Timer TA2.CCI2A capture input	0	1
		Timer TA2.2 output	1	1

Port P4, P4.0 to P4.7, Input/Output With Schmitt Trigger

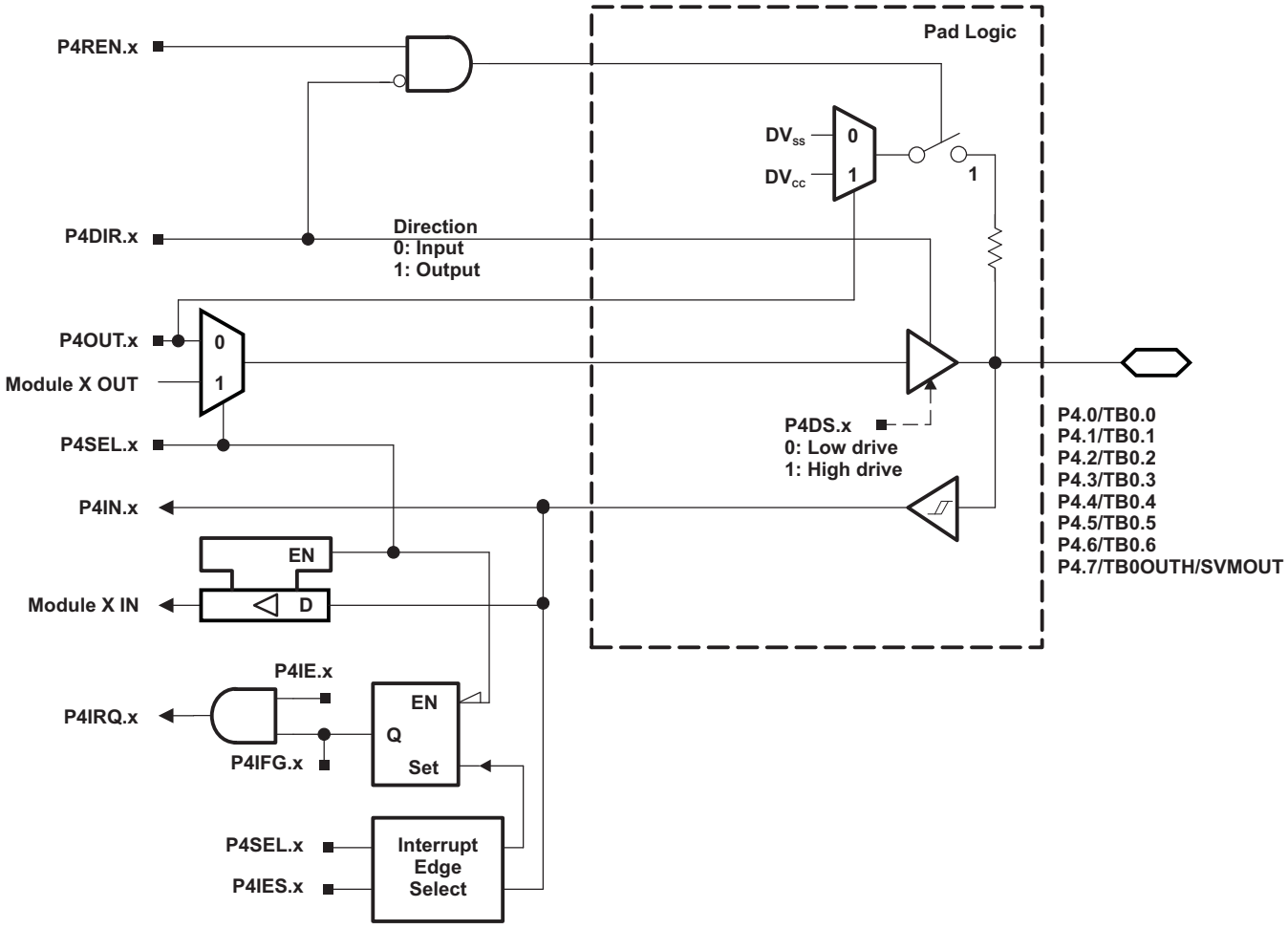


Table 56. Port P4 (P4.0 to P4.7) Pin Functions

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P4DIR.x	P4SEL.x
P4.0/TB0.0	0	P4.0 (I/O)	I: 0; O: 1	0
		Timer TB0.CCI0A capture input	0	1
		Timer TB0.0 output(1)	1	1
P4.1/TB0.1	1	P4.1 (I/O)	I: 0; O: 1	0
		Timer TB0.CCI1A capture input	0	1
		Timer TB0.1 output(1)	1	1
P4.2/TB0.2	2	P4.2 (I/O)	I: 0; O: 1	0
		Timer TB0.CCI2A capture input	0	1
		Timer TB0.2 output(1)	1	1
P4.3/TB0.3	3	P4.3 (I/O)	I: 0; O: 1	0
		Timer TB0.CCI3A capture input	0	1
		Timer TB0.3 output(1)	1	1
P4.4/TB0.4	4	P4.4 (I/O)	I: 0; O: 1	0
		Timer TB0.CCI4A capture input	0	1
		Timer TB0.4 output(1)	1	1
P4.5/TB0.5	5	P4.5 (I/O)	I: 0; O: 1	0
		Timer TB0.CCI5A capture input	0	1
		Timer TB0.5 output(1)	1	1
P4.6/TB0.6	6	P4.6 (I/O)	I: 0; O: 1	0
		Timer TB0.CCI6A capture input	0	1
		Timer TB0.6 output(1)	1	1
P4.7/TB0OUTH/ SVMOUT	7	P4.7 (I/O)	I: 0; O: 1	0
		Timer TB0.TB0OUTH	0	1
		SVMOUT	1	1

(1) Setting TB0OUTH causes all Timer_B configured outputs to be set to high impedance.

Port P5, P5.0 and P5.1, Input/Output With Schmitt Trigger

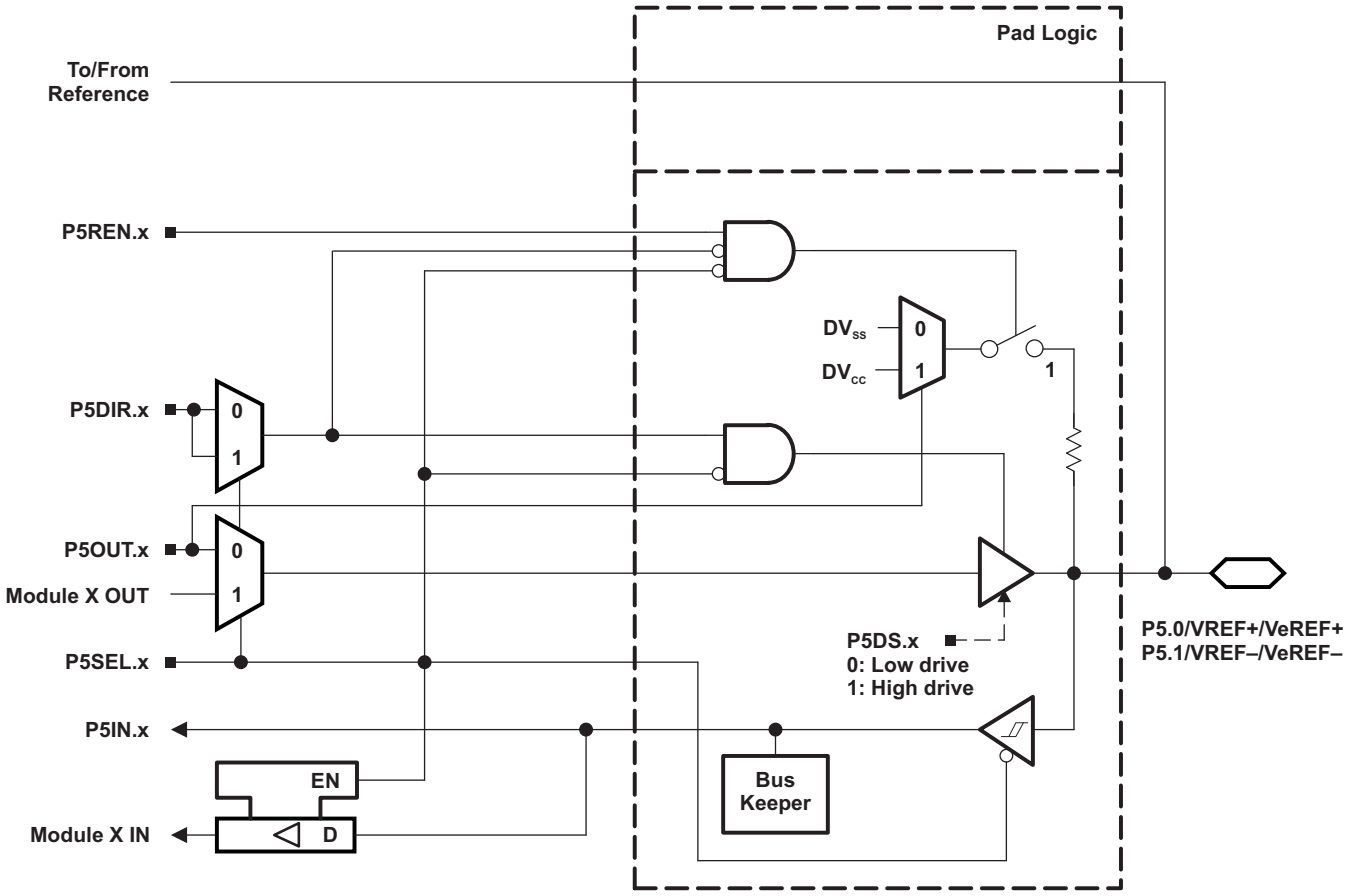


Table 57. Port P5 (P5.0 and P5.1) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P5DIR.x	P5SEL.x	REFOUT
P5.0/VREF+/VeREF+	0	P5.0 (I/O)(2)	I: 0; O: 1	0	X
		VeREF+(3)	X	1	0
		VREF+(4)	X	1	1
P5.1/VREF–/VeREF–	1	P5.1 (I/O)(2)	I: 0; O: 1	0	X
		VeREF–(5)	X	1	0
		VREF–(6)	X	1	1

(1) X = Don't care
(2) Default condition
(3) Setting the P5SEL.0 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF+ and used as the reference for the ADC12_A, Comparator_B, or DAC12_A.
(4) Setting the P5SEL.0 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The ADC12_A, VREF+ reference is available at the pin.
(5) Setting the P5SEL.1 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. An external voltage can be applied to VeREF- and used as the reference for the ADC12_A, Comparator_B, or DAC12_A.
(6) Setting the P5SEL.1 bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals. The ADC12_A, VREF– reference is available at the pin.

Port P5, P5.2 to P5.7, Input/Output With Schmitt Trigger

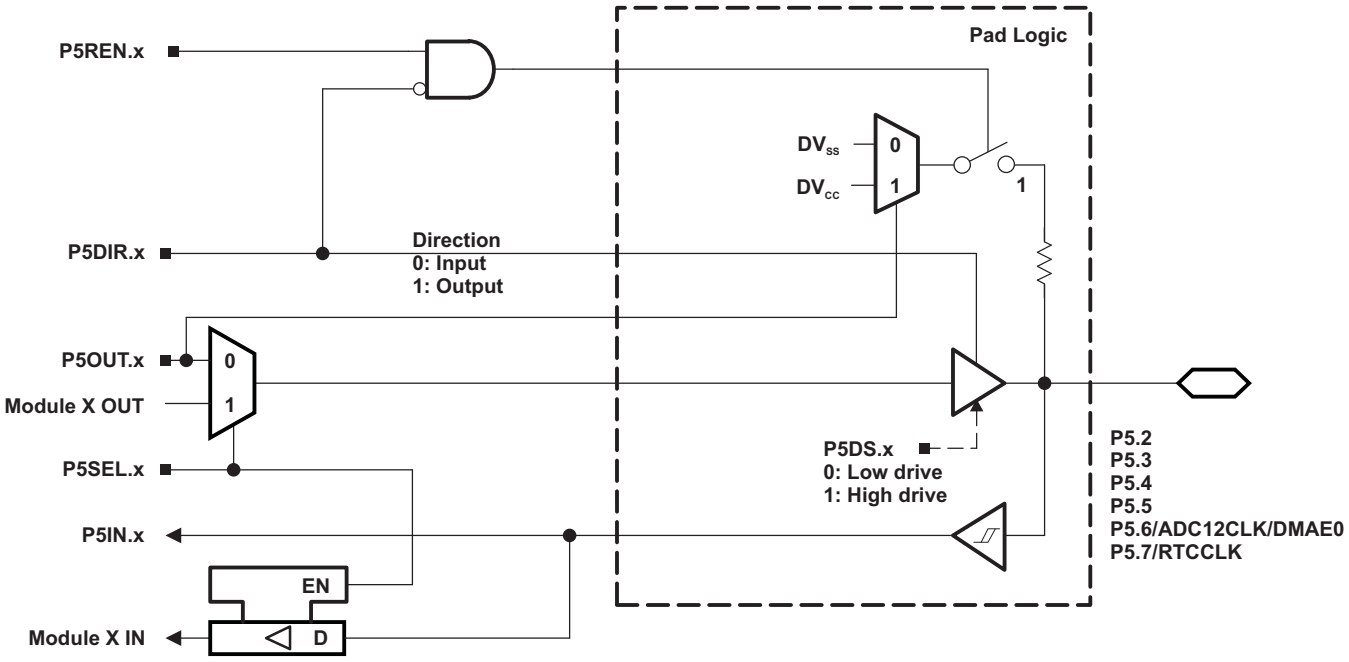


Table 58. Port P5 (P5.2 to P5.7) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P5DIR.x	P5SEL.x
P5.2	2	P5.2 (I/O)	I: 0; O: 1	0
P5.3	3	P5.3 (I/O)	I: 0; O: 1	0
P5.4	4	P5.4 (I/O)	I: 0; O: 1	0
P5.5	5	P5.5 (I/O)	I: 0; O: 1	0
P5.6/ADC12CLK/DMAE0	6	P5.6 (I/O)	I: 0; O: 1	0
		ADC12CLK	1	1
		DMAE0	0	1
P5.7/RTCCLK	7	P5.7 (I/O)	I: 0; O: 1	0
		RTCCLK	1	1

Port P6, P6.0 to P6.7, Input/Output With Schmitt Trigger

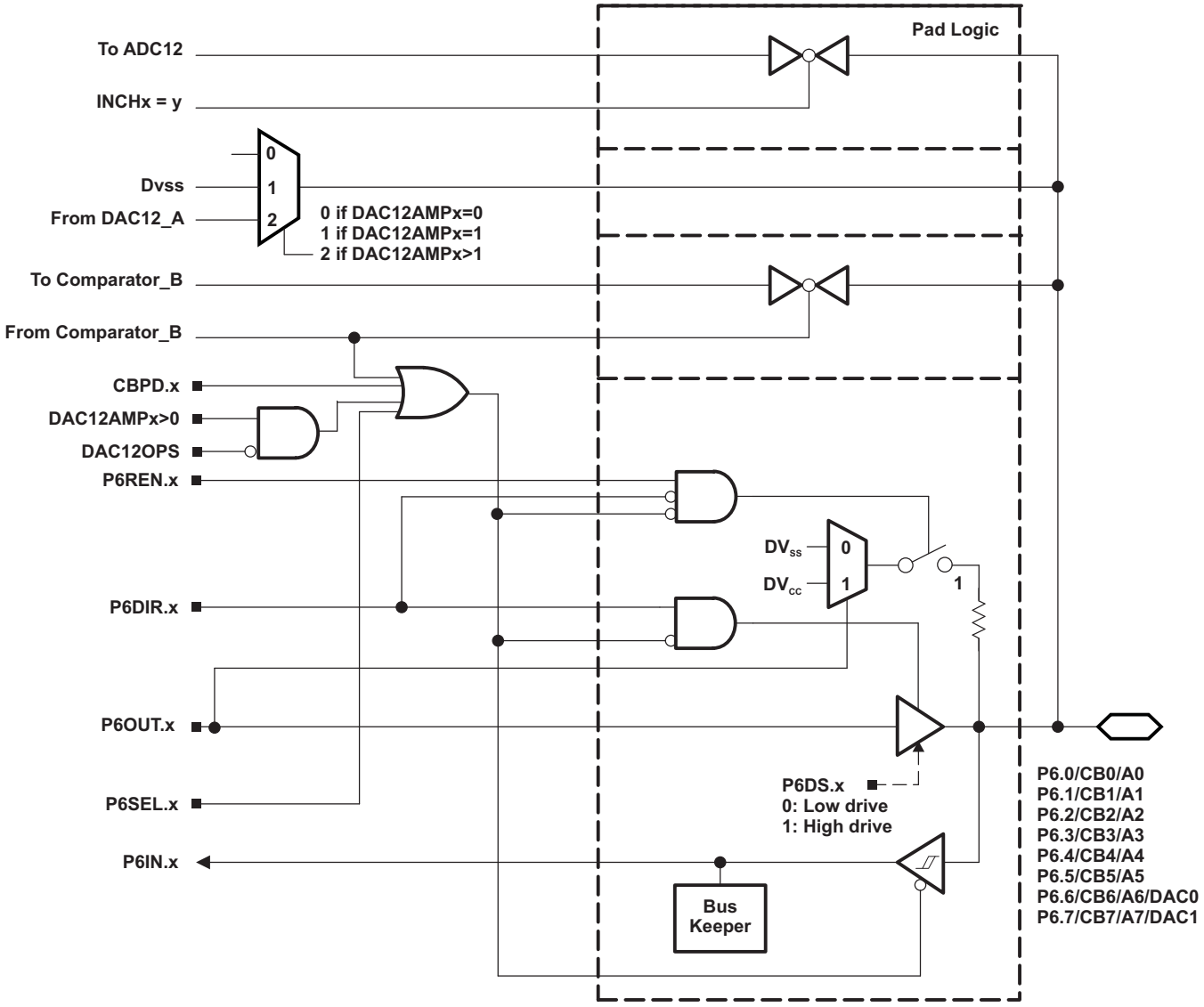
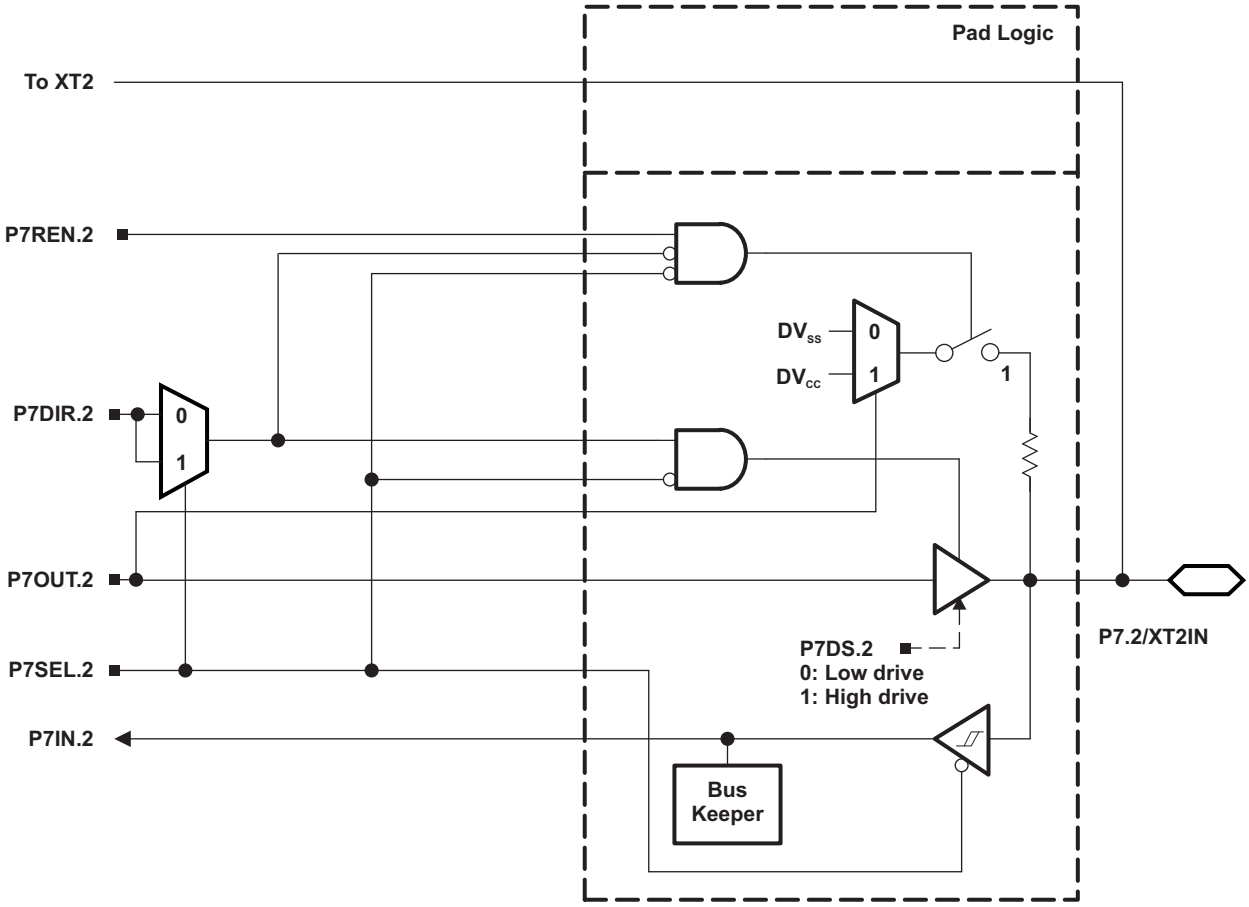


Table 59. Port P6 (P6.0 to P6.7) Pin Functions

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)				
			P6DIR.x	P6SEL.x	CBPD.x	DAC12OPS	DAC12AMPx
P6.0/CB0/A0	0	P6.0 (I/O)	I: 0; O: 1	0	0	n/a	n/a
		CB0	X	X	1	n/a	n/a
		A0(2) (3)	X	1	X	n/a	n/a
P6.1/CB1/A1	1	P6.1 (I/O)	I: 0; O: 1	0	0	n/a	n/a
		CB1	X	X	1	n/a	n/a
		A1(2) (3)	X	1	X	n/a	n/a
P6.2/CB2/A2	2	P6.2 (I/O)	I: 0; O: 1	0	0	n/a	n/a
		CB2	X	X	1	n/a	n/a
		A2(2) (3)	X	1	X	n/a	n/a
P6.3/CB3/A3	3	P6.3 (I/O)	I: 0; O: 1	0	0	n/a	n/a
		CB3	X	X	1	n/a	n/a
		A3(2) (3)	X	1	X	n/a	n/a
P6.4/CB4/A4	4	P6.4 (I/O)	I: 0; O: 1	0	0	n/a	n/a
		CB4	X	X	1	n/a	n/a
		A4(2) (3)	X	1	X	n/a	n/a
P6.5/CB5/A5	5	P6.5 (I/O)	I: 0; O: 1	0	0	n/a	n/a
		CB5	X	X	1	n/a	n/a
		A5(4) (2) (3)	X	1	X	n/a	n/a
P6.6/CB6/A6/DAC0	6	P6.6 (I/O)	I: 0; O: 1	0	0	X	0
		CB6	X	X	1	X	0
		A6(2) (3)	X	1	X	X	0
		DAC0	X	X	X	0	>1
P6.7/CB7/A7/DAC1	7	P6.7 (I/O)	I: 0; O: 1	0	0	X	0
		CB7	X	X	1	X	0
		A7(2) (3)	X	1	X	X	0
		DAC1	X	X	X	0	>1

(1) X = Don't care
(2) Setting the P6SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) The ADC12_A channel Ax is connected internally to AV_{SS} if not selected via the respective INCHx bits.
(4) X = Don't care

Port P7, P7.2, Input/Output With Schmitt Trigger



Port P7, P7.3, Input/Output With Schmitt Trigger

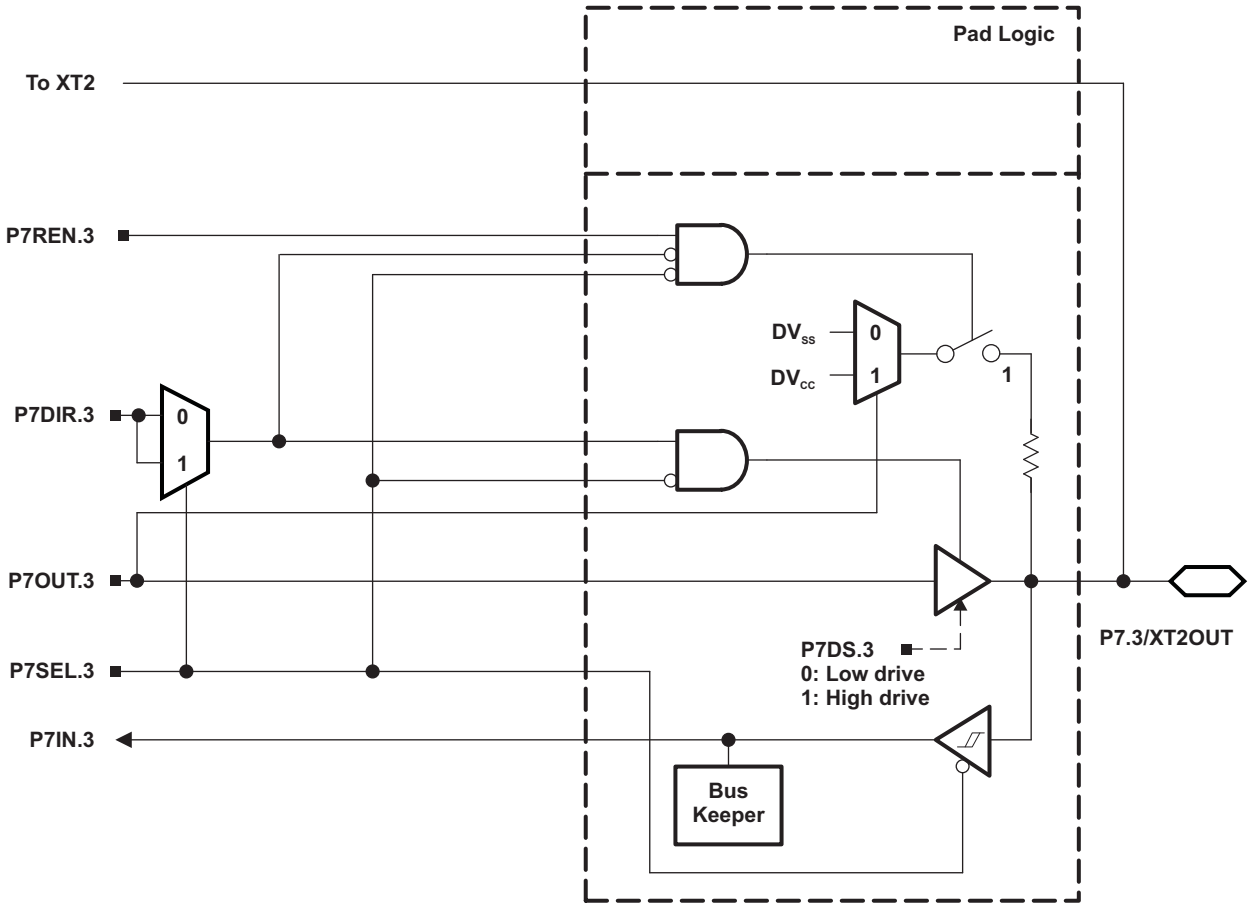


Table 60. Port P7 (P7.2 and P7.3) Pin Functions

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)			
			P7DIR.x	P7SEL.2	P7SEL.3	XT2BYPASS
P7.2/XT2IN	2	P7.2 (I/O)	I: 0; O: 1	0	X	X
		XT2IN crystal mode(2)	X	1	X	0
		XT2IN bypass mode(2)	X	1	X	1
P7.3/XT2OUT	3	P7.3 (I/O)	I: 0; O: 1	0	X	X
		XT2OUT crystal mode(3)	X	1	X	0
		P7.3 (I/O)(3)	X	1	X	1

(1) X = Don't care
(2) Setting P7SEL.2 causes the general-purpose I/O to be disabled. Pending the setting of XT2BYPASS, P7.2 is configured for crystal mode or bypass mode.
(3) Setting P7SEL.2 causes the general-purpose I/O to be disabled in crystal mode. When using bypass mode, P7.3 can be used as general-purpose I/O.

Port P7, P7.4 to P7.7, Input/Output With Schmitt Trigger

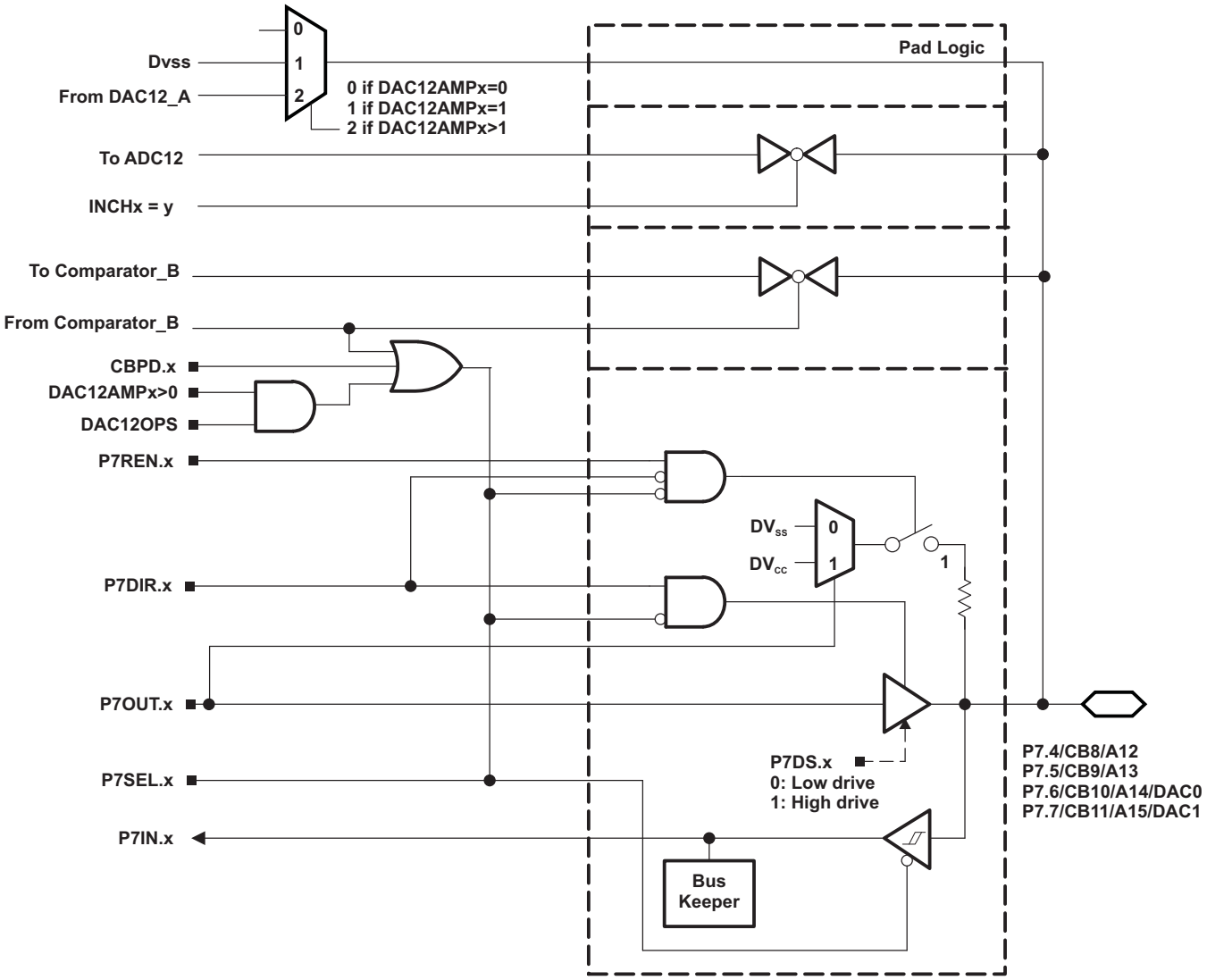


Table 61. Port P7 (P7.4 to P7.7) Pin Functions

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)				
			P7DIR.x	P7SEL.x	CBPD.x	DAC12OPS	DAC12AMPx
P7.4/CB8/A12	4	P7.4 (I/O)	I: 0; O: 1	0	0	n/a	n/a
		Comparator_B input CB8	X	X	1	n/a	n/a
		A12(2) (3)	X	1	X	n/a	n/a
P7.5/CB9/A13	5	P7.5 (I/O)	I: 0; O: 1	0	0	n/a	n/a
		Comparator_B input CB9	X	X	1	n/a	n/a
		A13(2) (3)	X	1	X	n/a	n/a
P7.6/CB10/A14/DAC0	6	P7.6 (I/O)	I: 0; O: 1	0	0	X	0
		Comparator_B input CB10	X	X	1	X	0
		A14(2) (3)	X	1	X	X	0
		DAC12_A output DAC0	X	X	X	1	>1
P7.7/CB11/A15/DAC1	7	P7.7 (I/O)	I: 0; O: 1	0	0	X	0
		Comparator_B input CB11	X	X	1	X	0
		A15(2) (3)	X	1	X	X	0
		DAC12_A output DAC1	X	X	X	1	>1

(1) X = Don't care
(2) Setting the P7SEL.x bit disables the output driver as well as the input Schmitt trigger to prevent parasitic cross currents when applying analog signals.
(3) The ADC12_A channel Ax is connected internally to AV_{SS} if not selected via the respective INCHx bits.

Port P8, P8.0 to P8.7, Input/Output With Schmitt Trigger

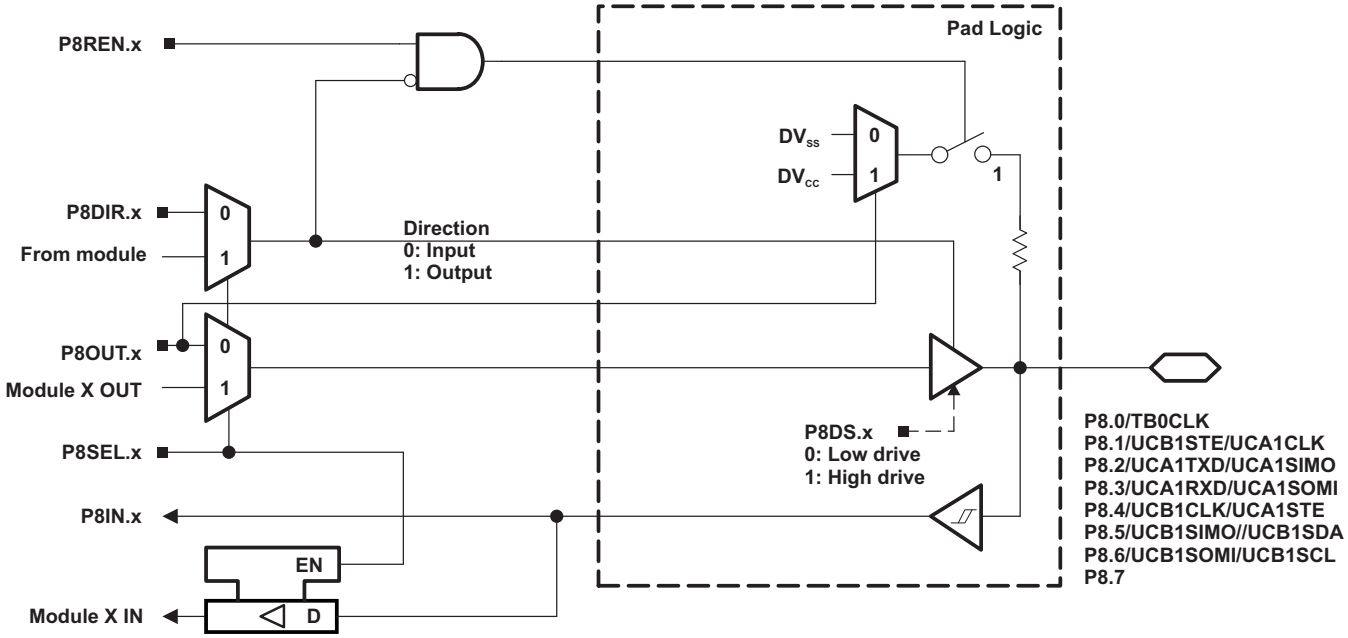


Table 62. Port P8 (P8.0 to P8.7) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)	
			P8DIR.x	P8SEL.x
P8.0/TB0CLK	0	P8.0 (I/O)	I: 0; O: 1	0
		Timer TB0.TB0CLK clock input	0	1
P8.1/UCB1STE/UCA1CLK	1	P8.1 (I/O)	I: 0; O: 1	0
		UCB1STE/UCA1CLK	X	1
P8.2/UCA1TXD/UCA1SIMO	2	P8.2 (I/O)	I: 0; O: 1	0
		UCA1TXD/UCA1SIMO	X	1
P8.3/UCA1RXD/UCA1SOMI	3	P8.3 (I/O)	I: 0; O: 1	0
		UCA1RXD/UCA1SOMI	X	1
P8.4/UCB1CLK/UCA1STE	4	P8.4 (I/O)	I: 0; O: 1	0
		UCB1CLK/UCA1STE	X	1
P8.5/UCB1SIMO/UCB1SDA	5	P8.5 (I/O)	I: 0; O: 1	0
		UCB1SIMO/UCB1SDA	X	1
P8.6/UCB1SOMI/UCB1SCL	6	P8.6 (I/O)	I: 0; O: 1	0
		UCB1SOMI/UCB1SCL	X	1
P8.7	7	P8.7 (I/O)	I: 0; O: 1	0

(1) X = Don't care

Port P9, P9.0 to P9.7, Input/Output With Schmitt Trigger

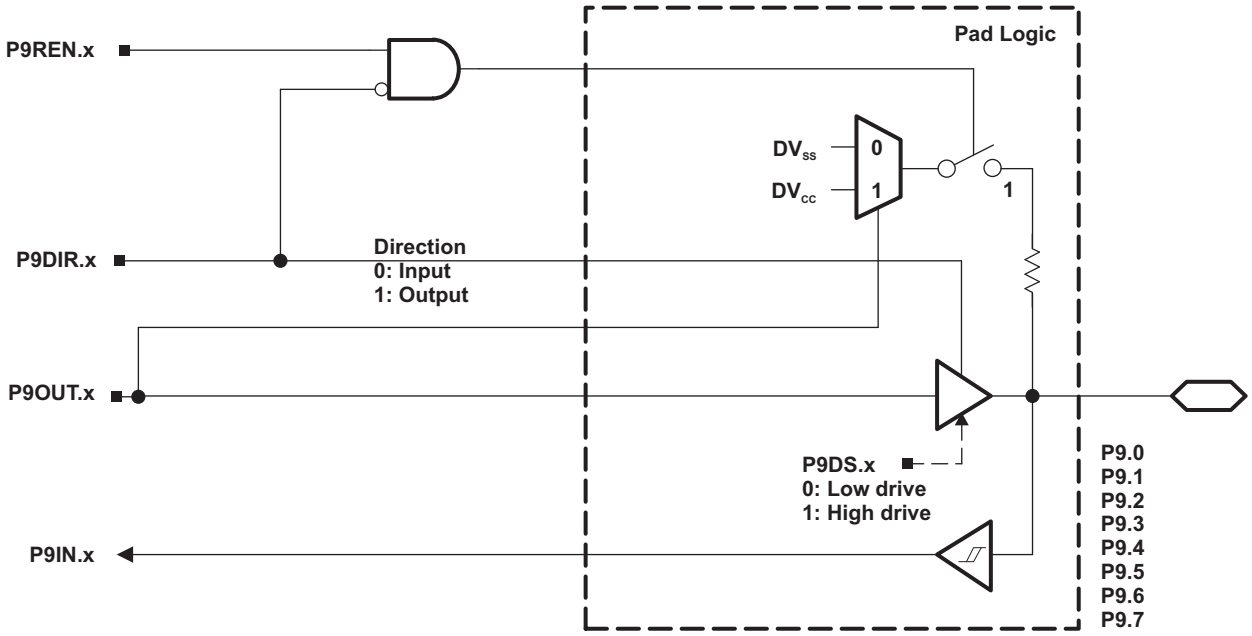


Table 63. Port P9 (P9.0 to P9.7) Pin Functions

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P9DIR.x	P9SEL.x
P9.0	0	P9.0 (I/O)	I: 0; O: 1	0
P9.1	1	P9.1 (I/O)	I: 0; O: 1	0
P9.2	2	P9.2 (I/O)	I: 0; O: 1	0
P9.3	3	P9.3 (I/O)	I: 0; O: 1	0
P9.4	4	P9.4 (I/O)	I: 0; O: 1	0
P9.5	5	P9.5 (I/O)	I: 0; O: 1	0
P9.6	6	P9.6 (I/O)	I: 0; O: 1	0
P9.7	7	P9.7 (I/O)	I: 0; O: 1	0

Port PU.0/DP, PU.1/DM, PUR USB Ports

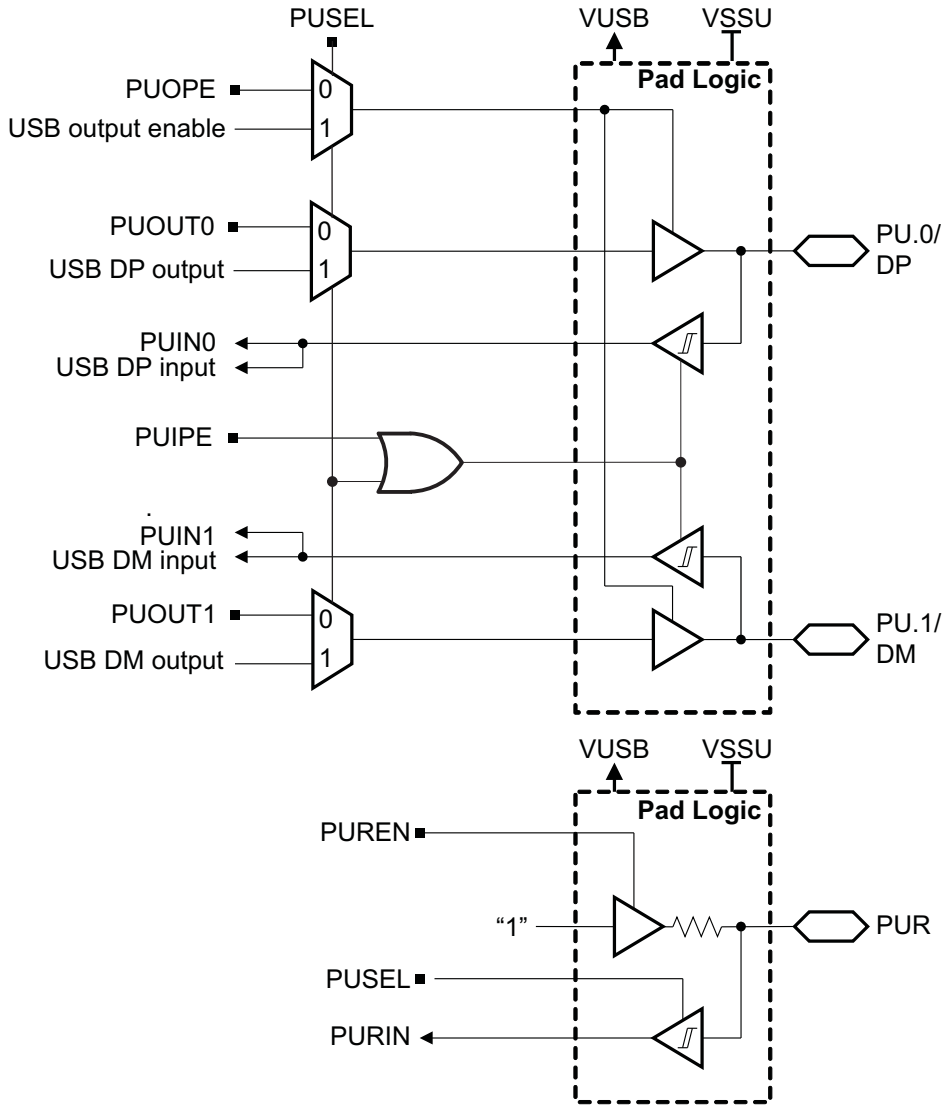


Table 64. Port PU.0/DP, PU.1/DM Output Functions

CONTROL BITS				PIN NAME		FUNCTION
PUSEL	PUDIR	PUOUT1	PUOUT0	PU.1/DM	PU.0/DP	
0	0	X	X	Hi-Z	Hi-Z	Outputs off
0	1	0	0	0	0	Outputs enabled
0	1	0	1	0	1	Outputs enabled
0	1	1	0	1	0	Outputs enabled
0	1	1	1	1	1	Outputs enabled
1	X	X	X	DM	DP	Direction set by USB module

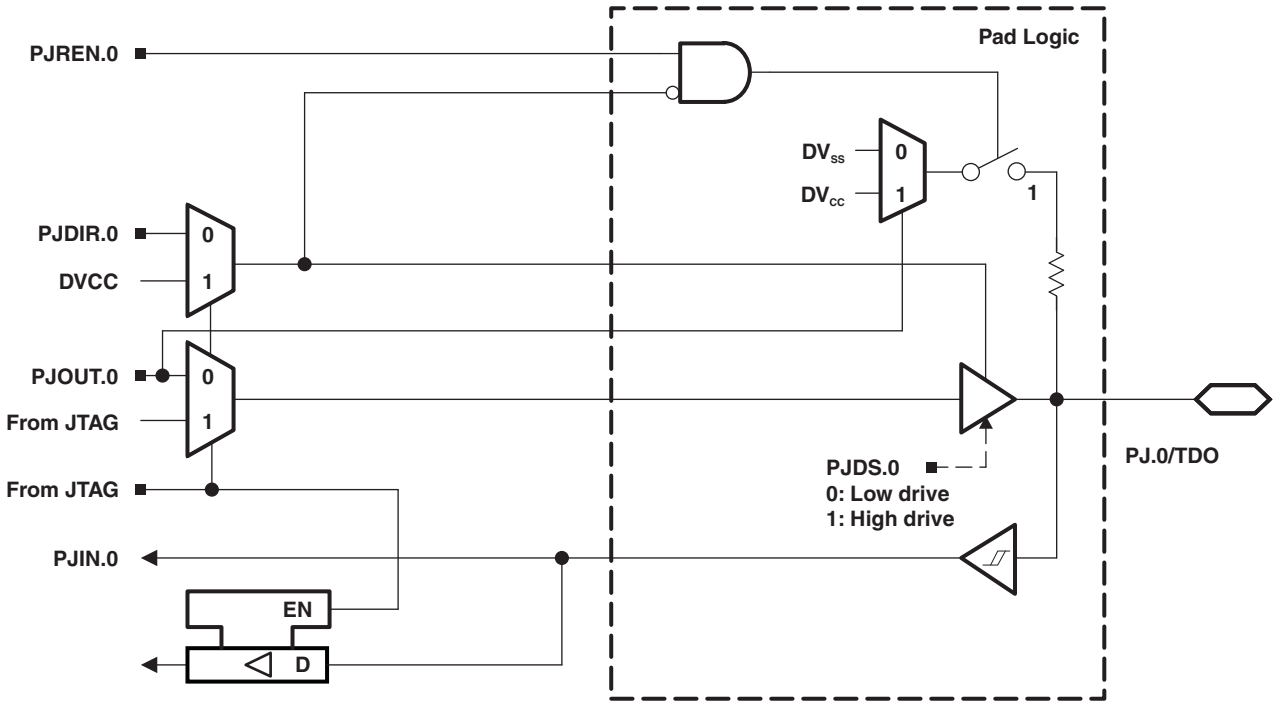
Table 65. Port PUR Input Functions

CONTROL BITS		FUNCTION
PUSEL	PUREN	
0	0	Input disabled Pullup disabled

Table 65. Port PUR Input Functions (continued)

CONTROL BITS		FUNCTION
PUSEL	PUREN	
0	1	Input disabled Pullup enabled
1	0	Input enabled Pullup disabled
1	1	Input enabled Pullup enabled

Port J, J.0 JTAG pin TDO, Input/Output With Schmitt Trigger or Output



Port J, J.1 to J.3 JTAG pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

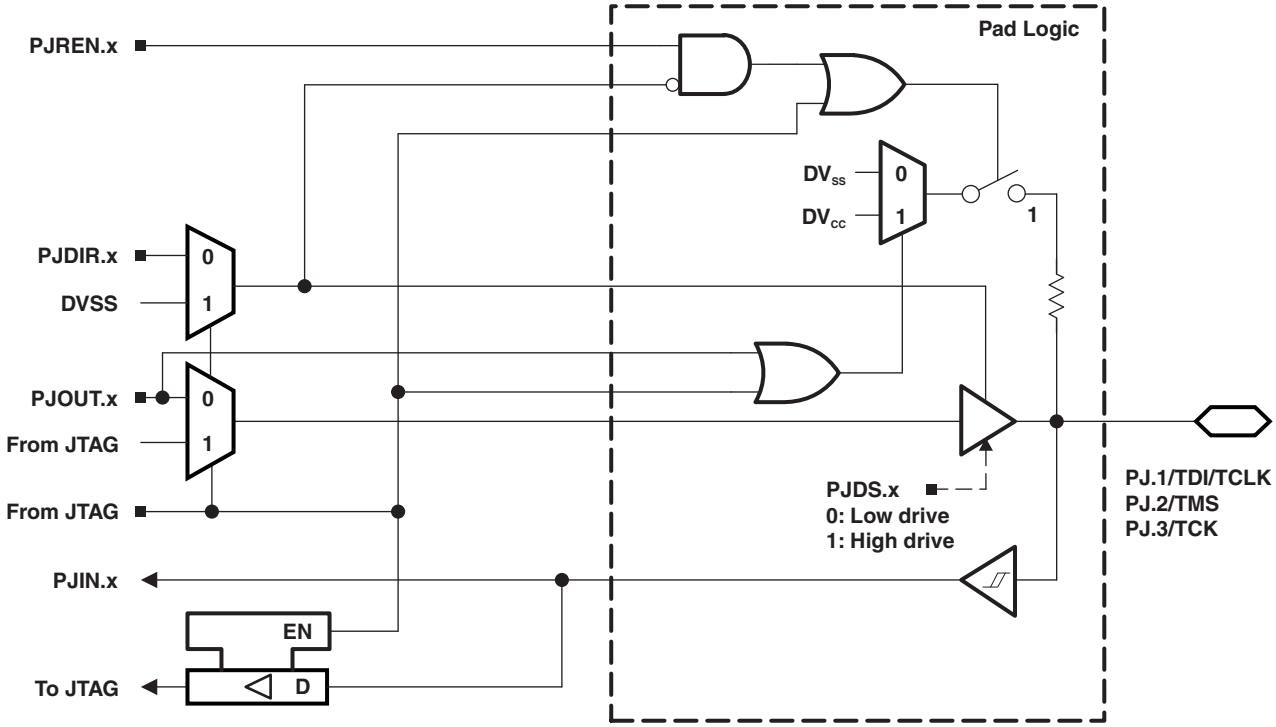


Table 66. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS/ SIGNALS[1]
			PJDIR.x
PJ.0/TDO	0	PJ.0 (I/O)[2]	I: 0; O: 1
		TDO[3]	X
PJ.1/TDI/TCLK	1	PJ.1 (I/O)[2]	I: 0; O: 1
		TDI/TCLK[3] [4]	X
PJ.2/TMS	2	PJ.2 (I/O)[2]	I: 0; O: 1
		TMS[3] [4]	X
PJ.3/TCK	3	PJ.3 (I/O)[2]	I: 0; O: 1
		TCK[3] [4]	X

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

DEVICE DESCRIPTORS

Table 67 list the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

Table 67. MSP430F563x Device Descriptor Table(1)

	Description	Address	Size bytes	F5638	F5637	F5636	F5635	F5634	F5633	F5632	F5631	F5630
				Value	Value	Value	Value	Value	Value	Value	Value	Value
Info Block	Info length	01A00h	1	06h	06h	06h	06h	06h	06h	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h	06h	06h	06h	06h	06h	06h
	CRC value	01A02h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	Device ID	01A04h	2	8014h	8012h	8010h	800Eh	8044h	8042h	8040h	803Eh	803Ch
	Hardware revision	01A06h	1	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	Firmware revision	01A07h	1	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
Die Record	Die Record Tag	01A08h	1	08h	08h	08h	08h	08h	08h	08h	08h	08h
	Die Record length	01A09h	1	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah
	Lot/Wafer ID	01A0Ah	4	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	Die X position	01A0Eh	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	Die Y position	01A10h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	Test results	01A12h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
ADC12 Calibration	ADC12 Calibration Tag	01A14h	1	11h	11h	11h	11h	11h	11h	11h	11h	11h
	ADC12 Calibration length	01A15h	1	10h	10h	10h	10h	10h	10h	10h	10h	10h
	ADC Gain Factor	01A16h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC Offset	01A18h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 1.5-V Reference Temp. Sensor 30°C	01A1Ah	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 1.5-V Reference Temp. Sensor 85°C	01A1Ch	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.0-V Reference Temp. Sensor 30°C	01A1Eh	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.0-V Reference Temp. Sensor 85°C	01A20h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.5-V Reference Temp. Sensor 30°C	01A22h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.5-V Reference Temp. Sensor 85°C	01A24h	2	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit	per unit

(1) NA = Not applicable

REVISION HISTORY

REVISION	COMMENTS
SLAS650	Product Preview release
SLAS650A	Updated Product Preview including electrical specifications
SLAS650B	Production Data release
SLAS650C	Changed description of ACLK and PUR in Terminal Functions. Changed typos to Interrupt Flag names on Timer TA2 rows in Table 5. Changed SYSRSTIV, System Reset offset 1Ch to Reserved in Table 13. Corrected names of SVMLVLRIFG and SVMHVLRIFG bits in Table 13. Corrected right-most column in Table 6. Added note regarding evaluation of PUR in USB BSL. Changed notes on REF, Built-In Reference. Changed $t_{SENSOR(sample)}$ MIN to 100 µs in 12-Bit ADC, Temperature Sensor and Built-In VMID. Changed note (2) in 12-Bit ADC, Temperature Sensor and Built-In VMID. Editorial changes throughout.
SLAS650D	Table 2, Added note regarding pullup resistor to $\overline{\text{RST}}$/NMI/SBWTDIO pin. Added 应用范围, Development Tools Support, and Device and Development Tool Nomenclature. Digital I/O (Link to User's Guide), Changed the description of the number of I/Os in each port. Table 21, Added PM5CTL0 register. 12-Bit DAC, Supply Specifications, Fixed typo in I_{DD} Test Conditions (changed from DAC12IOG to DAC12OG). USB Input Ports DP and DM, Corrected V_{IL} and V_{IH} limits. Flash Memory, Changed I_{ERASE} and I_{MERASE}, I_{BANK} limits.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F5630IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5630	Samples
MSP430F5630IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5630	Samples
MSP430F5630IZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5630	Samples
MSP430F5630IZQWT	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5630	Samples
MSP430F5631IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5631	Samples
MSP430F5631IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5631	Samples
MSP430F5631IZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5631	Samples
MSP430F5631IZQWT	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5631	Samples
MSP430F5632IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5632	Samples
MSP430F5632IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5632	Samples
MSP430F5632IZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5632	Samples
MSP430F5632IZQWT	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5632	Samples
MSP430F5633IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5633	Samples
MSP430F5633IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5633	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F5633IZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5633	Samples
MSP430F5633IZQWT	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5633	Samples
MSP430F5634IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5634	Samples
MSP430F5634IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5634	Samples
MSP430F5634IZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5634	Samples
MSP430F5634IZQWT	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5634	Samples
MSP430F5635IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5635	Samples
MSP430F5635IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5635	Samples
MSP430F5635IZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5635	Samples
MSP430F5635IZQWT	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5635	Samples
MSP430F5636IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5636	Samples
MSP430F5636IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5636	Samples
MSP430F5636IZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5636	Samples
MSP430F5636IZQWT	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5636	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F5637IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5637	Samples
MSP430F5637IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5637	Samples
MSP430F5637IZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5637	Samples
MSP430F5637IZQWT	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5637	Samples
MSP430F5638IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5638	Samples
MSP430F5638IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		M430F5638	Samples
MSP430F5638IZQWR	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5638	Samples
MSP430F5638IZQWT	ACTIVE	BGA MICROSTAR JUNIOR	ZQW	113	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR		M430F5638	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

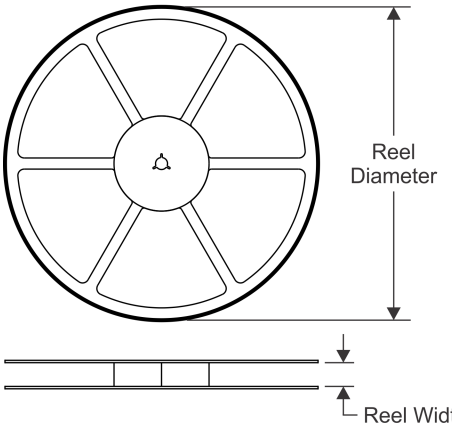
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

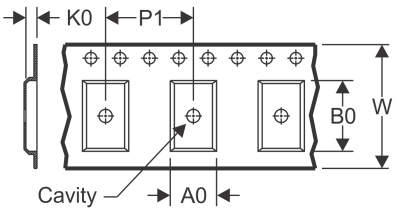
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

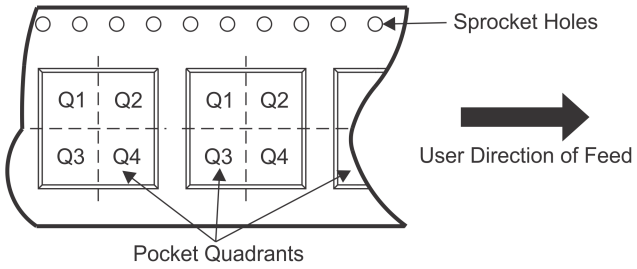


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



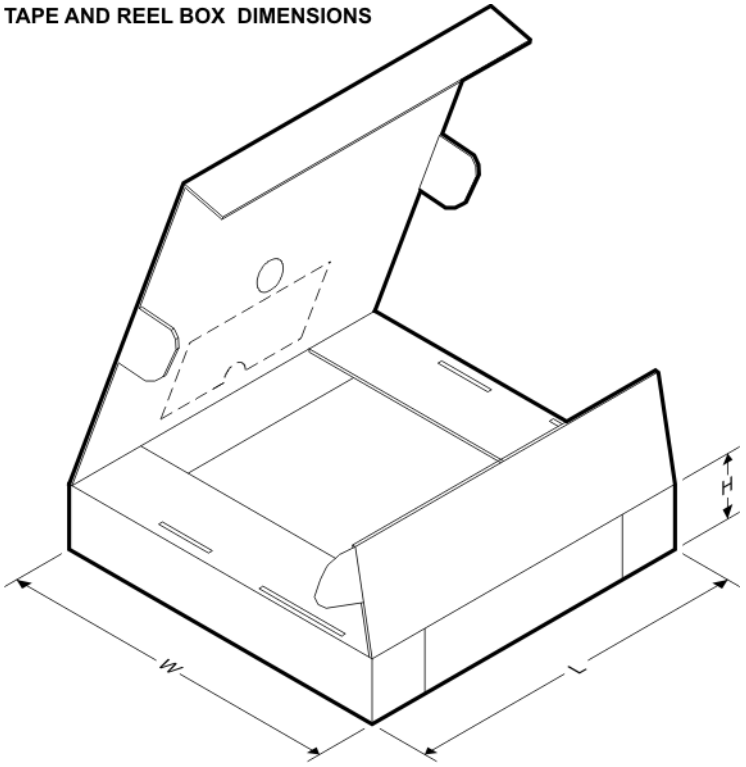
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F5630IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430F5630IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F5630IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F5631IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430F5631IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F5631IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F5632IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430F5632IZQWR	BGA MICROSTAR JUNI	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	OR											
MSP430F5632IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F5633IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430F5633IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F5633IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F5634IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F5634IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F5635IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430F5635IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F5635IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F5636IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F5636IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F5637IPZR	LQFP	PZ	100	1000	330.0	24.4	17.0	17.0	2.1	20.0	24.0	Q2
MSP430F5637IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F5637IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F5638IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1
MSP430F5638IZQWT	BGA MICROSTA	ZQW	113	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
	R JUNIOR											

TAPE AND REEL BOX DIMENSIONS

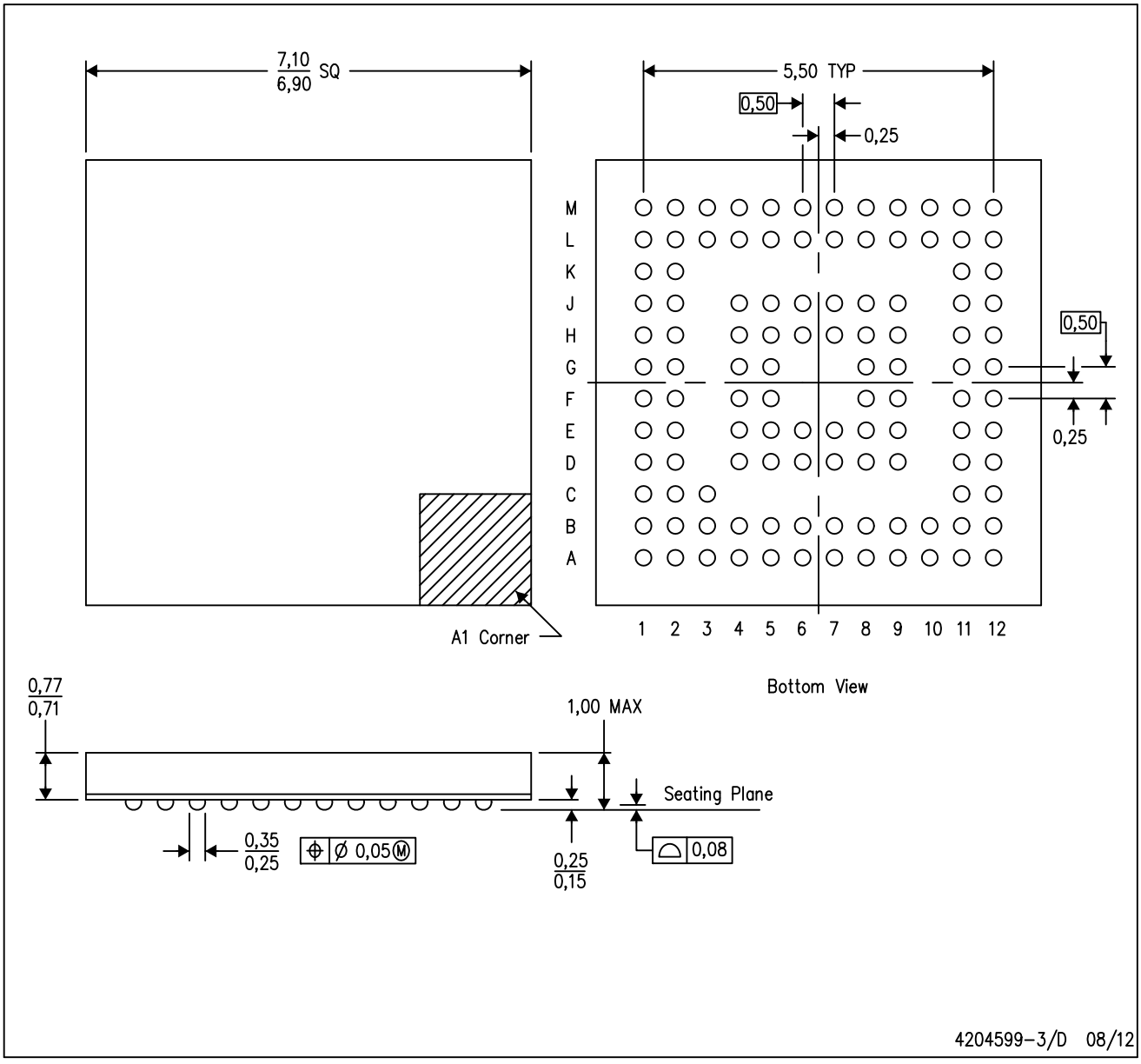


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F5630IPZR	LQFP	PZ	100	1000	367.0	367.0	45.0
MSP430F5630IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430F5630IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	336.6	336.6	28.6
MSP430F5631IPZR	LQFP	PZ	100	1000	367.0	367.0	45.0
MSP430F5631IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430F5631IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	336.6	336.6	28.6
MSP430F5632IPZR	LQFP	PZ	100	1000	367.0	367.0	45.0
MSP430F5632IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430F5632IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	336.6	336.6	28.6
MSP430F5633IPZR	LQFP	PZ	100	1000	367.0	367.0	45.0
MSP430F5633IZQWR	BGA MICROSTAR	ZQW	113	2500	336.6	336.6	28.6

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
	JUNIOR						
MSP430F5633IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	336.6	336.6	28.6
MSP430F5634IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430F5634IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	336.6	336.6	28.6
MSP430F5635IPZR	LQFP	PZ	100	1000	367.0	367.0	45.0
MSP430F5635IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430F5635IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	336.6	336.6	28.6
MSP430F5636IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430F5636IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	336.6	336.6	28.6
MSP430F5637IPZR	LQFP	PZ	100	1000	367.0	367.0	45.0
MSP430F5637IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430F5637IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	336.6	336.6	28.6
MSP430F5638IZQWR	BGA MICROSTAR JUNIOR	ZQW	113	2500	336.6	336.6	28.6
MSP430F5638IZQWT	BGA MICROSTAR JUNIOR	ZQW	113	250	336.6	336.6	28.6

ZQW (S–PBGA–N113) PLASTIC BALL GRID ARRAY

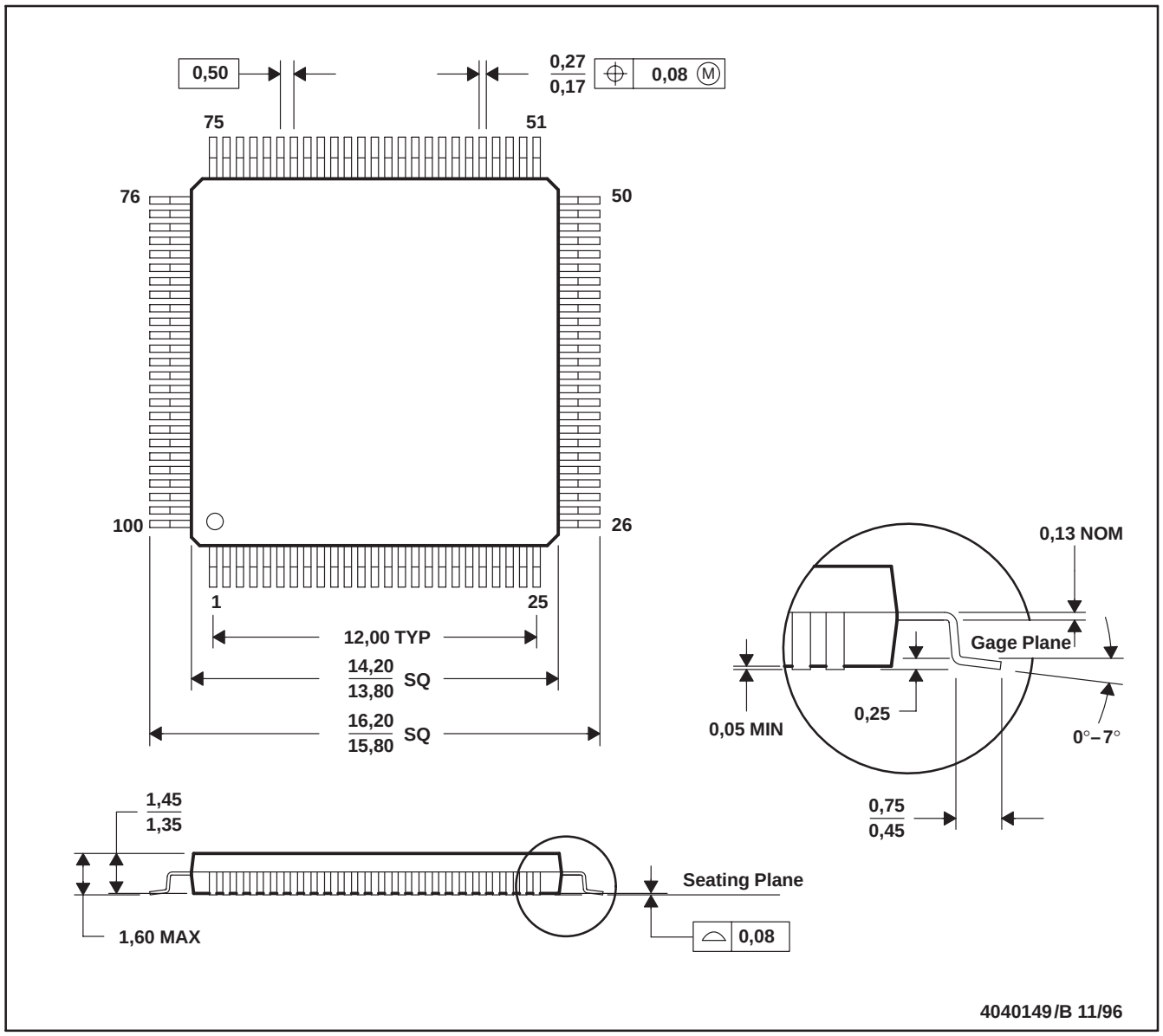


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a Pb–free solder ball design.

MicroStar Junior is a trademark of Texas Instruments.

MTQF013A – OCTOBER 1994 – REVISED DECEMBER 1996

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

重要声明

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