//
Seongwoo Choi
scho29@ucsc.edu
CMPE - 012
#1368039
M/W 2:00PM - 4:00PM
//

Title:
Memories

Purpose:
The purpose of the laboratory assignment 3 is to use MultiMedia Logic to create a sequential logic and learn about basic storage using LC-3, and the D-Latch, and modify it to support a reset signal.

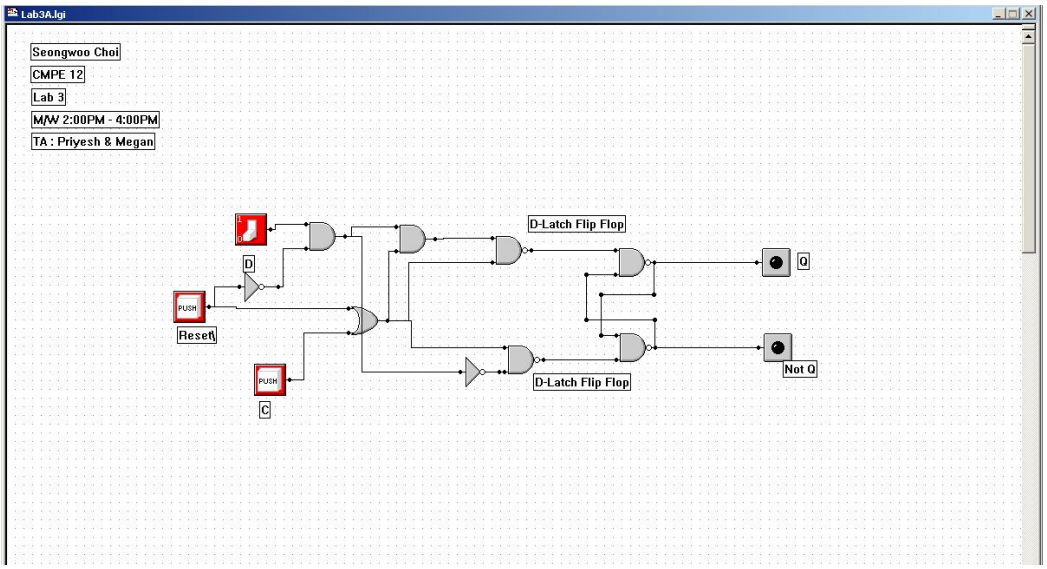
Procedure:
The methodology of using MultiMedia Logic software to build a basic storage using LC-3, and the D-Latch. First, scheme through the lab 3 document and then download a D-Latch file from the server. Second, create a schematic page and modify the D-Latch and then create a reset signal in the D-Latch. For part B, download the files for part B. There is a PDF that explains how Part B should look like. 7-segment display is introduced and create two switches in total. One switch for Read/Write, and another switch for address select. There are two buttons in the part B. One button is for clock/control input and another button is used for resetting the values that are displayed on latches. Those display latches return to 0.

Algorithm and Other Data:
This is the truth table that was used for the lab 3 assignment.

S	**CLK**	**RESET**	**Z**
0	0	0	S
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	S
1	0	1	0

1	1	0	1
1	1	1	0

This is a diagram of modified D-Latch:



When the D switch is on the Q Led flashes and then when the user pushes the C button, the Not Q Led flashes. The reset button makes every LED to go off.

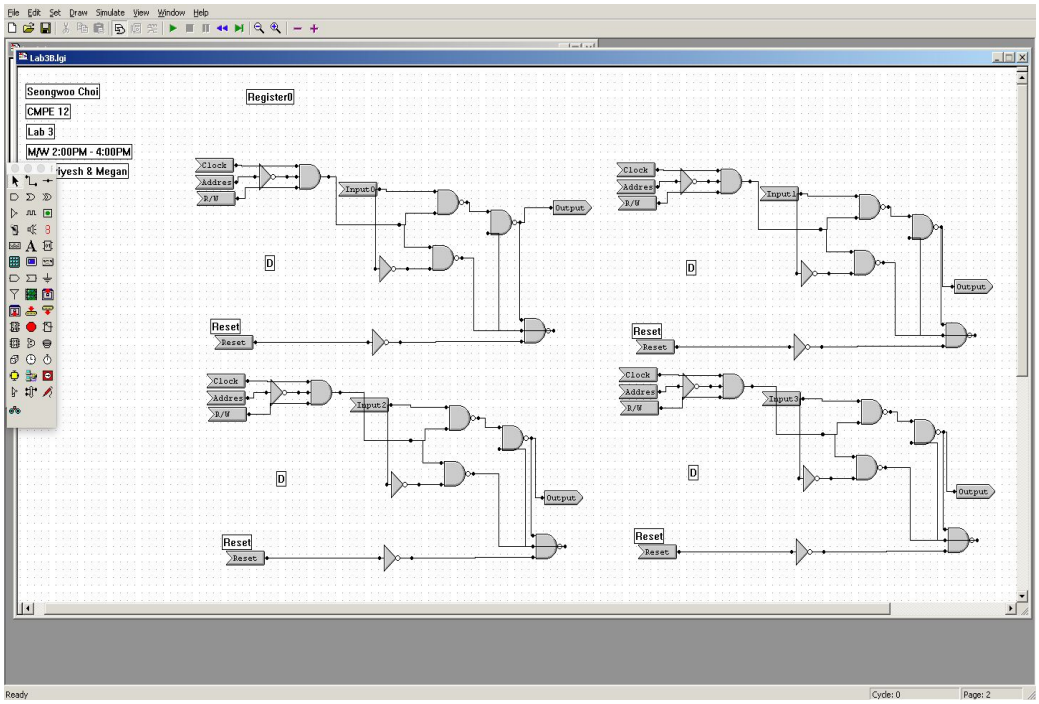
What went wrong or what were the challenges?
In part A, the challenge was to observe and figure out how to implement the D-latch that was provided from the server, and modify a logic to reset the D-latch. For part B, the challenge was to figure out how to store the value in one latch and keep it there until another value was stored to another latch without making the first one to go back to 0 value.

Other Information:
read/write of one "word" of the register file at a time.
What is the word size?
the word size is 4 bits.
Address space?
The address space for one register is 1. Three register is 3.
How about the addressability?
Addressability is 4 bits.

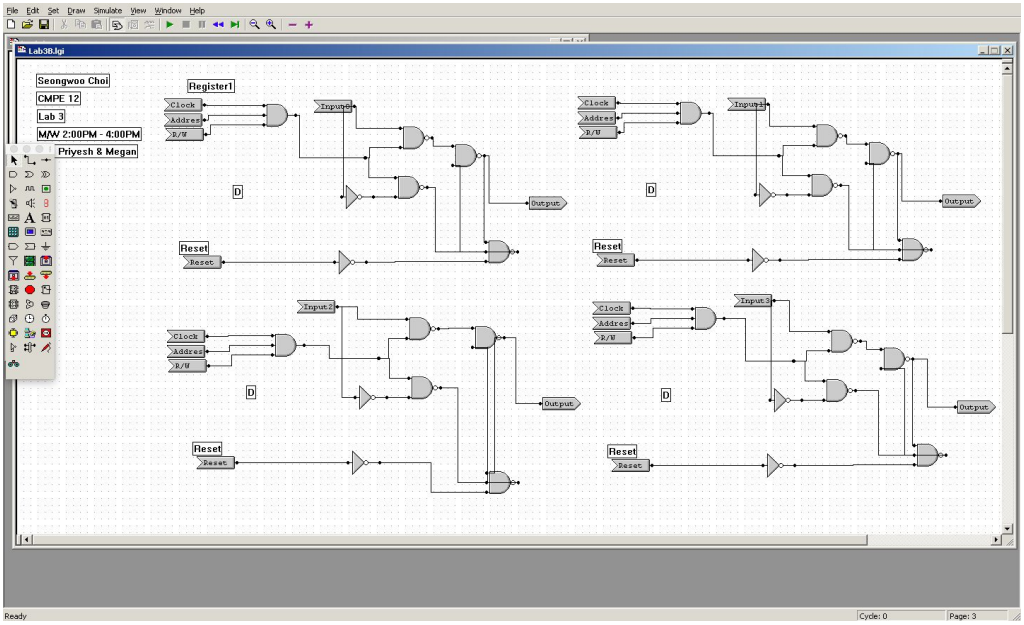
Explain the over flow of data through the circuit.

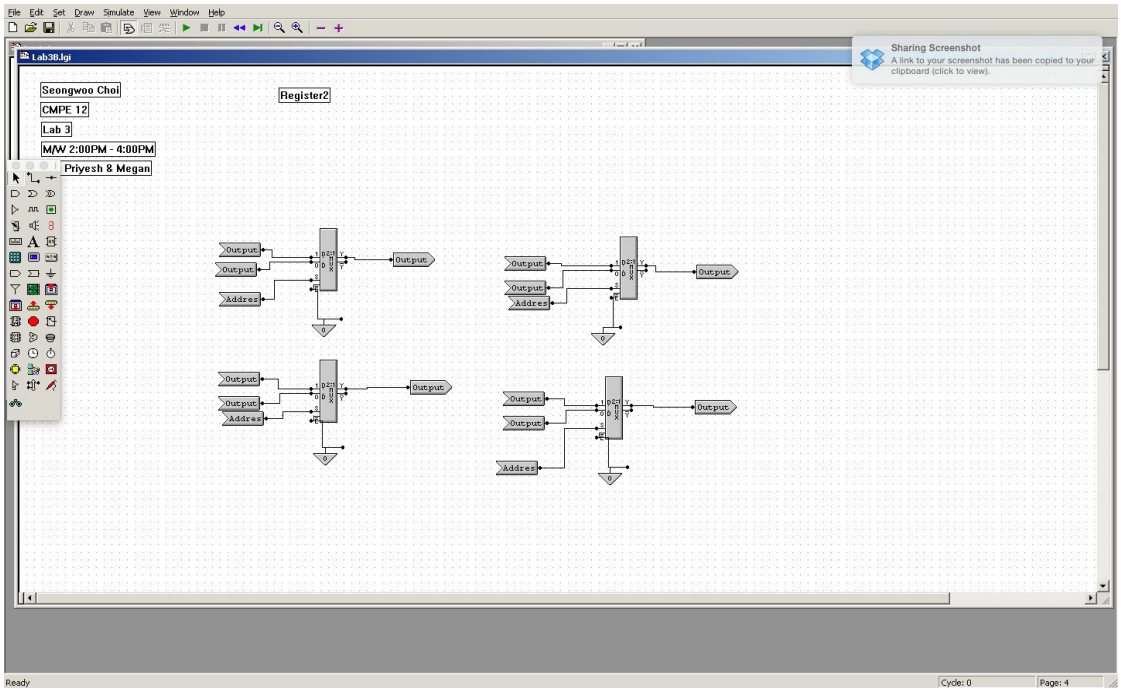
The main overflow of data through the circuit was that the D-Latch should store the value of the user input from the 7-segment display. For example, if an user chooses A from the 7-segment display, the first latch should store that value. Also, it is necessary that the switch for Read/Write supposed to indicate 1. When a clock button is pressed, then there will ‘A’ on the first latch. If the user turns the switch for Address on, then the second latch storage activates. The user chooses a value to store in the second latch, then when the user presses the clock button, the second latch stores the value that the user selected.

This diagram shows that the register0. The AND gate takes the inputs of Address, Clock and

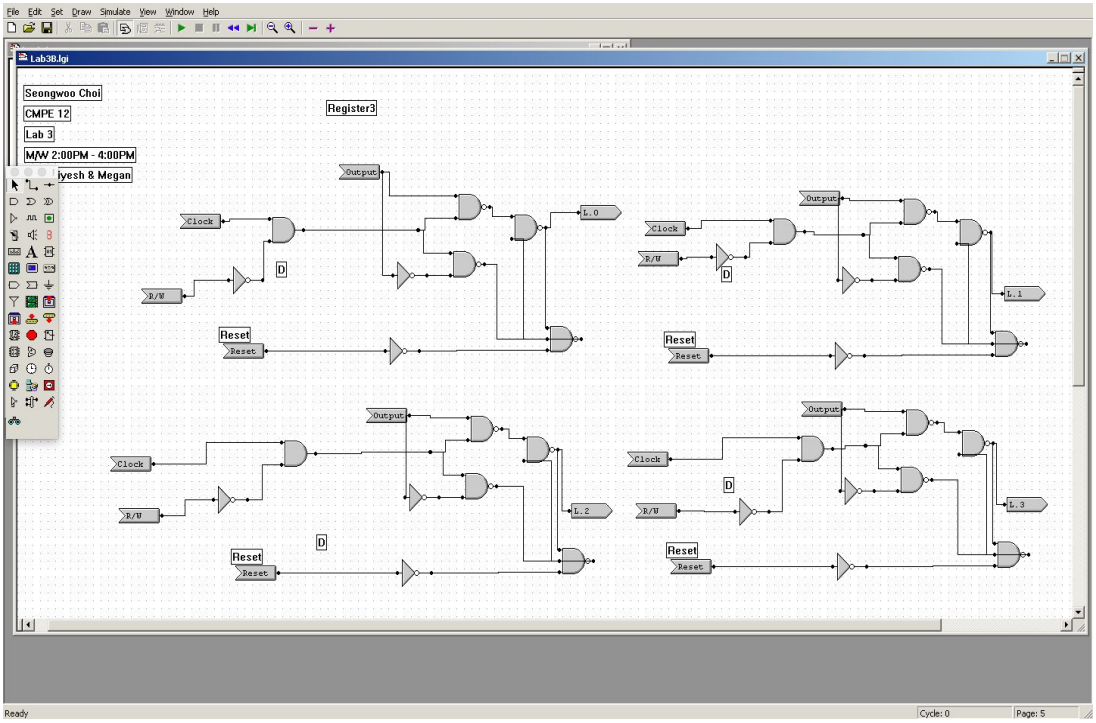


R/W. Address is connected to the inverter.





This diagram shows that the outputs from Register 0 and Register 1 are collected and these become inputs on these four multiplexers. Each multiplexer has 1 and 0 values. On 1 values, inputs are from Register 1, which are output5, 6, 7, and 8.



This is another register diagram that takes the inputs from the multiplexers and store the values. Afterward, those go into the third latch.

Conclusion:

In comparing to the previous labs, this lab was very challenging because this made me to spend a lot of time to work on it. It was a time consuming procedure to figure out how D-latches work. Especially, it required me to understand how registers work and how register can store the value. Overall, this was very challenging, but worth it. The first part of the lab was easy to figure out, but the second part was very hard to understand and a basic storage was hard.