CMPE 110 Computer Architecture
Fall 2015, Homework #4 Solution

Computer Engineering
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Question 1. Cache Coherence Transactions (14 points)

Solution.

	Core	Request Type	Address	C0 L1 State	C1 L1 State	C2 L1 State	C3 L1 State
1	0	Load	`0x00ffabc0`	E	-	-	-
2	0	Store	`0x00ffabc8`	M	-	-	-
3	1	Load	`0x00ffabd4`	S	S	-	-
4	1	Store	`0x00ffabd8`	I	M	-	-
5	1	Load	`0x00afabc0`	-	E	-	-
6	2	Load	`0x00afabc8`	-	S	S	-
7	1	Load	`0x00bfabf0`	-	E	-	-
8	0	Load	`0x00ffabc0`	E	-	-	-

Question 2. Cache Coherence Protocols (15 points)

Solution.

Question 2.A VI Protocol (5 points)

	Core	Request Type	C0 Cache Line State	C1 Cache Line State	C2 Cache Line State	C3 Cache Line State
1	0	Read x	V	-	-	-
2	1	Read x	I	V	-	-
3	2	Read x	I	I	V	-
4	3	Write x	I	I	I	V
5	1	Read x	I	V	I	I

Question 2.B MSI Protocol (5 points)

	Core	Request Type	C0 Cache Line State	C1 Cache Line State	C2 Cache Line State	C3 Cache Line State
1	0	Read x	S	-	-	-
2	1	Read x	S	S	-	-
3	2	Read x	S	S	S	-
4	3	Write x	I	I	I	M
5	1	Read x	I	S	I	S

Question 2.C MESI Protocol (5 points)

	Core	Request Type	C0 Cache Line State	C1 Cache Line State	C2 Cache Line State	C3 Cache Line State
1	0	Read x	E	-	-	-
2	1	Read x	S	S	-	-
3	2	Read x	S	S	S	-
4	3	Write x	I	I	I	M
5	1	Read x	I	S	I	S

Question 3. Virtual Memory (7 points)

Solution.

- What is the number of pages in the virtual address space?

  A 40-bit address can address 2^{40} bytes in a byte-addressable machine. The size of a page is 16K, (2^{14}), number of pages is $\frac{2^{40}}{2^{14}} = 2^{26}$.

- What is the maximum size of addressable physical memory in the system?

  With 4 byte entries, we can reference 2^{32} pages. Each page is 2^{14} bytes long, the max addressable physical memory size is $2^{32} \times 2^{14} = 2^{47}$ Bytes, assuming no protection bits.

- If an average process size is 8 GB, what would be the size of a one-level page table? A two-level page table?

  - 1-level Page Table:

    We have 2^{26} pages in each virtual address space and use 4 bytes per page table entry, the size of the page table is $2^{26} \times 2^2 = 2^{28}$. This is $\frac{1}{64}$ of the processes' memory (256 MB).

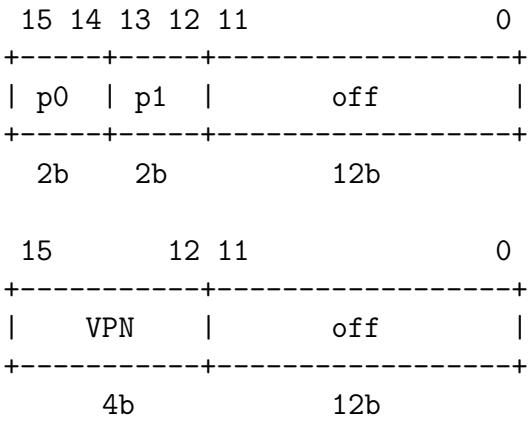
  - 2-level Page Table:

    Address will be divided as 13 | 13 | 14. Process size is 8GB = 2^{33}. Page size is 2^{14}, which means we have $\frac{2^{33}}{2^{14}} = 2^{19}$ pages. Bottom level holds 2^{19} references, with each holding 2^{13} entries which means we need $\frac{2^{19}}{2^{13}} = 2^6$ tables. Total size is $(1 \times 2^{13} \times 4) + (2^6 \times 2^{13} \times 4) = 32768 + 2097152 = 2129920$ Bytes or 2.03125 MB which is much less than 1-level paging.

Question 4. Page-Based Memory Translation (28 points)

Solution.

4.A Two-Level Page Tables (14 points)



Page offset is 12 bits, index into L1 and L2 page tables are both two bits, and the VPN is four bits. Address mappings shown above.

	Page-Table Entry	
Paddr of PTE	**Valid**	**Paddr**
0xffffc	1	0xfffe0
0xffff8	0	
0xffff4	0	
0xffff0	1	0xfffb0
0xfffec	1	0x05000
0xfffe8	1	0x07000
0xfffe4	0	
0xfffe0	0	
0xfffdc	0	
0xfffd8	0	
0xfffd4	0	
0xfffd0	0	
0xfffcc	0	
0xfffc8	0	
0xfffc4	0	
0xfffc0	0	
0xfffbc	1	0x01000
0xfffb8	1	0x04000
0xfffb4	1	0x00000
0xfffb0	0	

Contents of Physical Memory with Page Tables

Question 4.B Translation-Lookaside Buffer (14 points)

Transaction Address	VPN	Page Offset	m/h	Total Num Mem Accesses	TLB Way 0		TLB Way 1	
					VPN	PPN	VPN	PPN
0xeff4	0xe	0xff4	m	3	–	–	–	–
0x2ff0	0x2	0xff0	m	3	0xe	0x07		
0xeff8	0xe	0xff8	h	1			0x2	0x04
0x2ff4	0x2	0xff4	h	1				
0xeffc	0xe	0xffc	h	1				
0x2ff8	0x2	0xff8	h	1				
0xf000	0xf	0x000	m	3				
0x2ffc	0x2	0xffc	h	1	0xf	0x05		
0xf004	0xf	0x004	h	1				
0x3000	0x3	0x000	m	3				
0xf008	0xf	0x008	h	1			0x3	0x01
0x3004	0x3	0x004	h	1				
0xf00c	0xf	0x00c	h	1				
0x3008	0x3	0x008	h	1				
Number of Misses =		4						
Miss Rate =		0.29						

TLB Contents Over Time