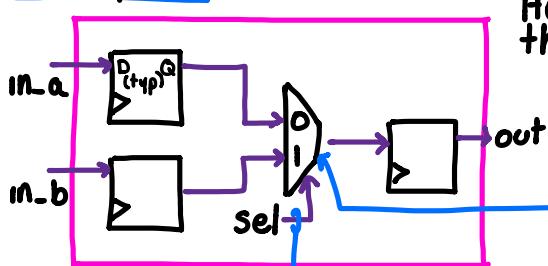


### Datapath



How does data travel through a system?

this MUX controls the data flow

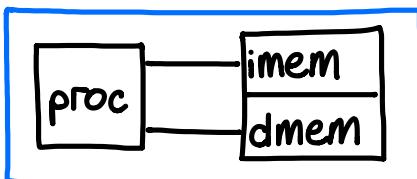
sel is ctrl signal

all flip flops are positive edge triggered

clk ! falling / negative edge

this is the positive or rising edge

computer architects simulate circuits utilizing hardware description languages like Verilog

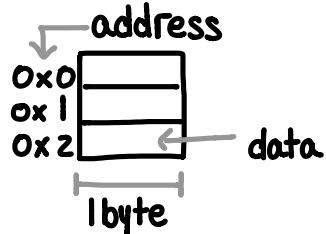


which instr do I want next?

PC → imem → 16 bit instruction

PC  
0x0  
0x2  
0x4  
instr  
add  
Sub  
beq

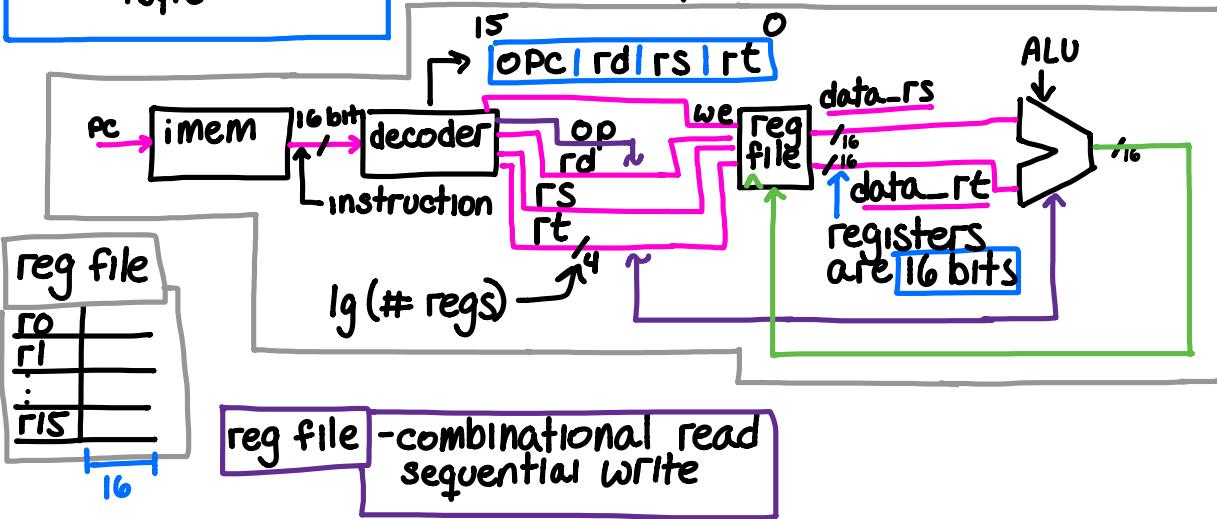
### memory diagram

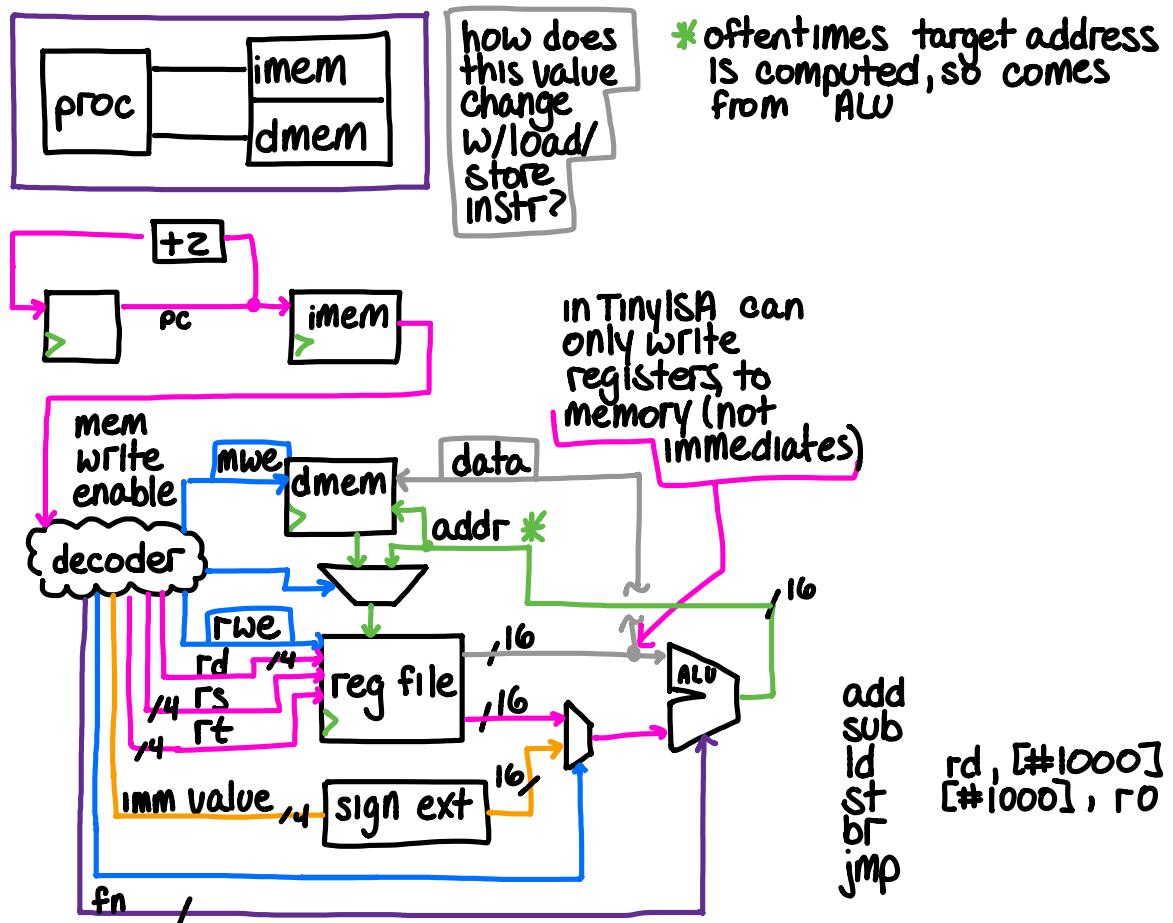
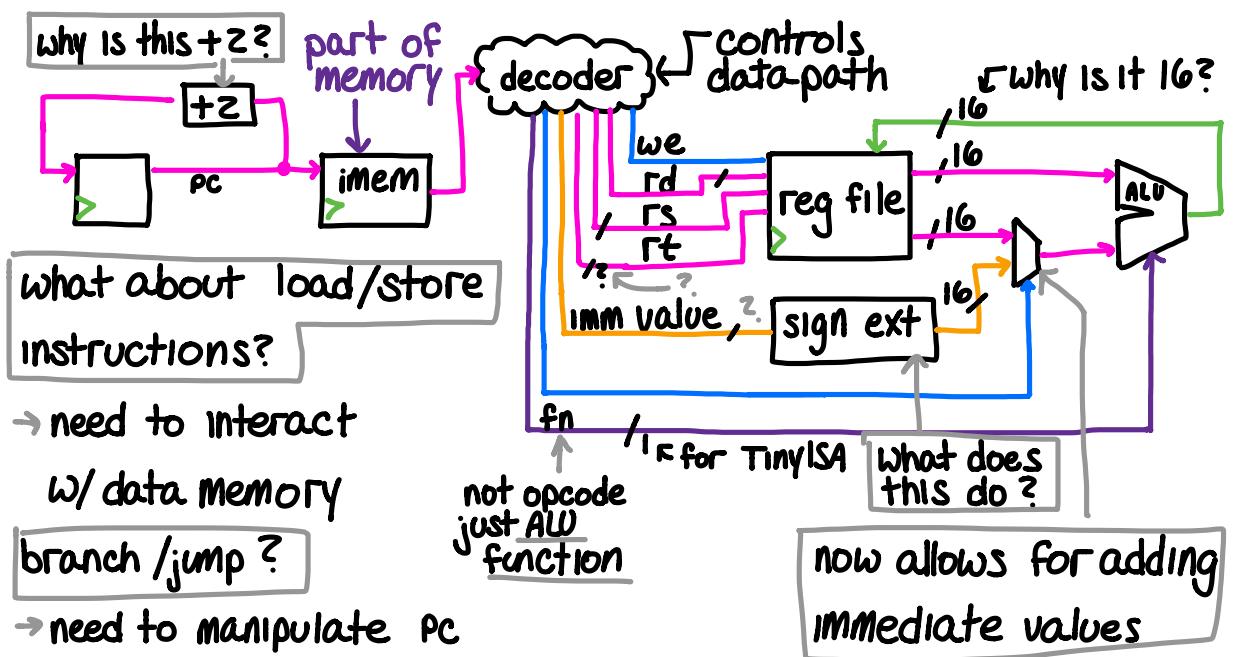


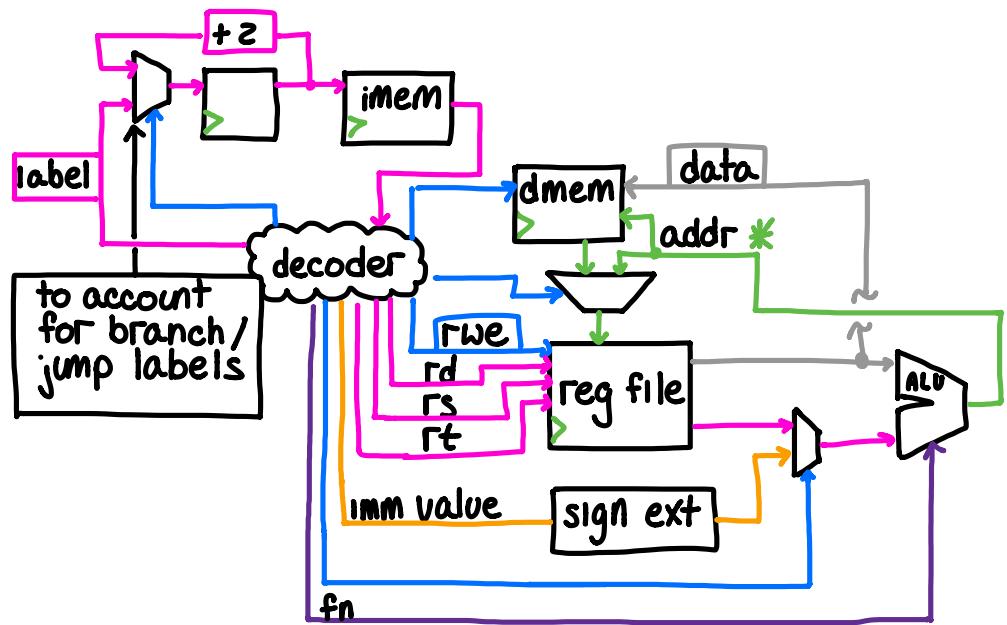
why are we incrementing by 2? what does this tell us about the ISA?

let's build a processor!

basic assembly  
→ add → branch  
→ sub → jmp





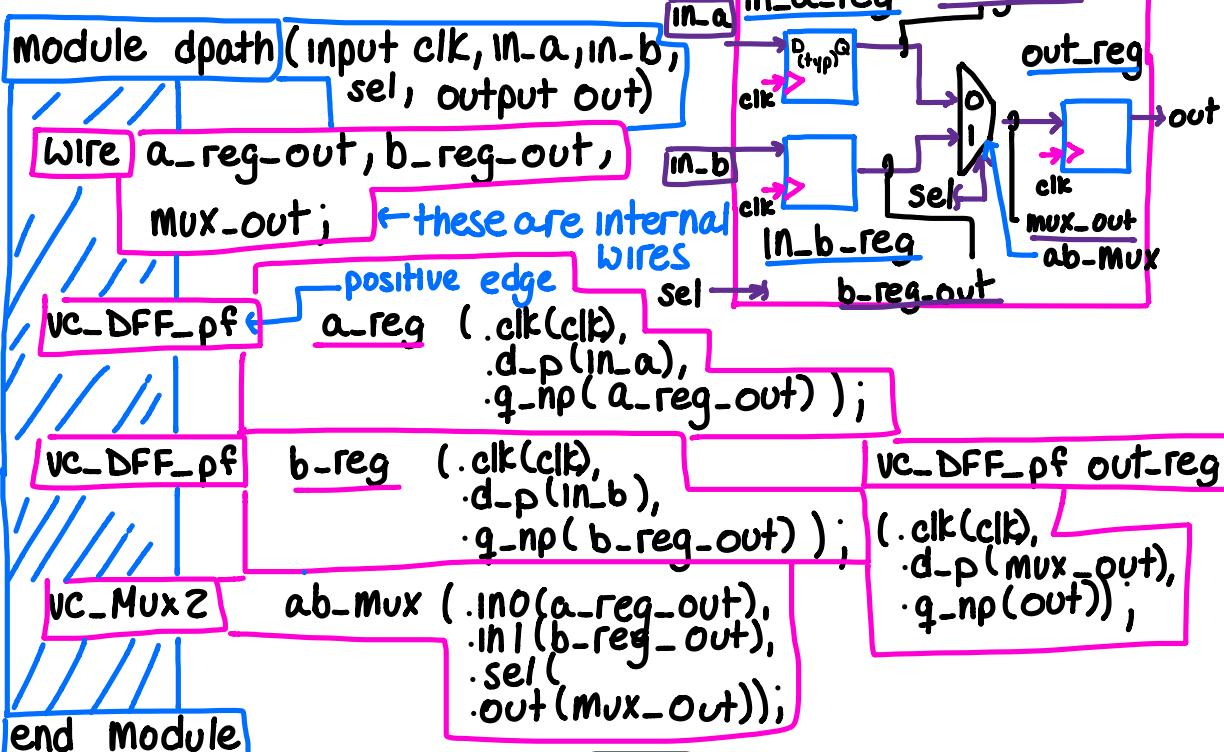


How to convert a circuit diagram to verilog:

code

'include "vc\_StateElements.v" ← contains flip flop block

'include "vc\_Muxes.v"



order of components doesn't matter

incremental design- break down problem into smaller blocks

to make wires into busses:

wire [31:0] wire\_name

VC\_DFF\_pf #(32) out\_reg (...)