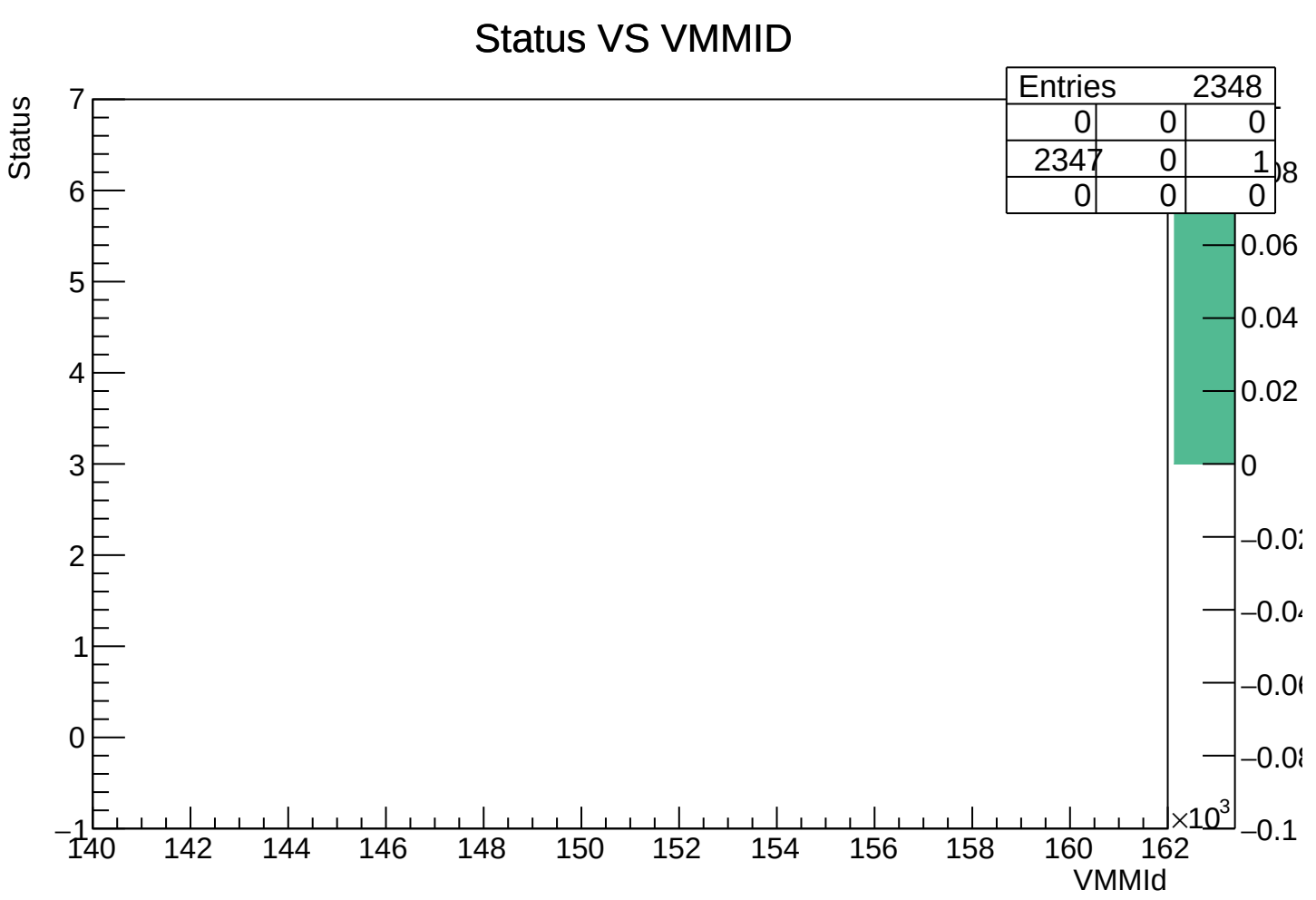
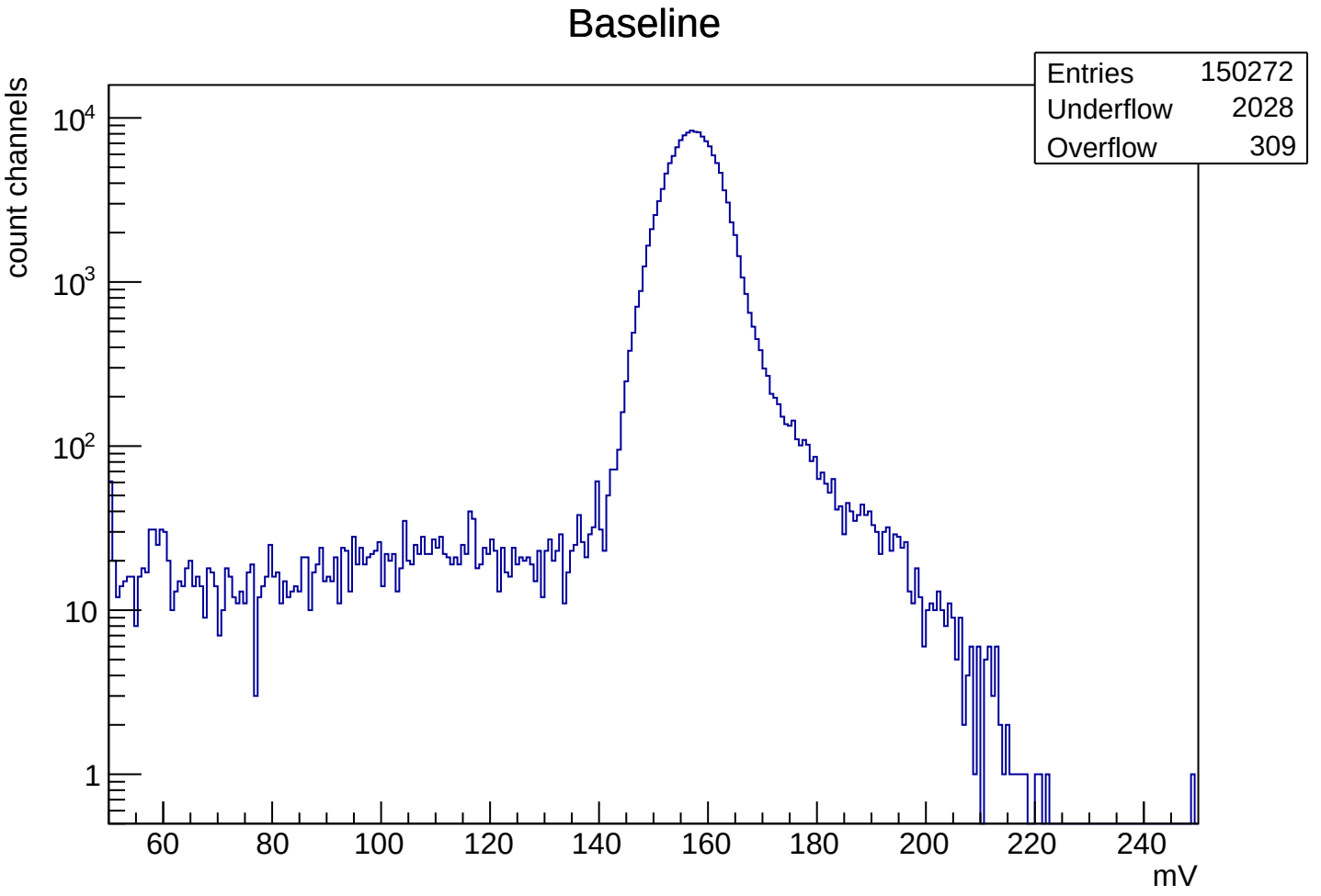
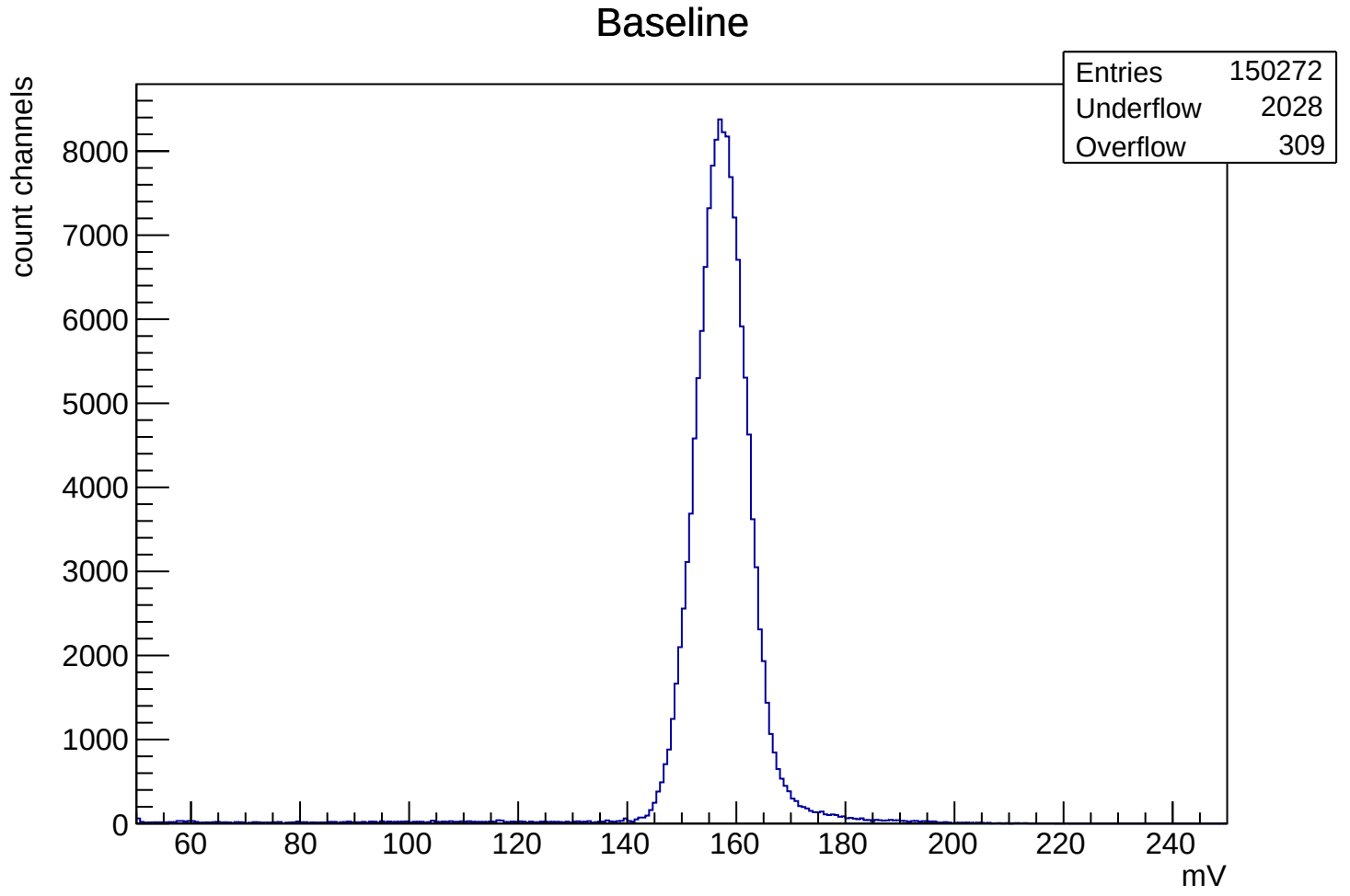
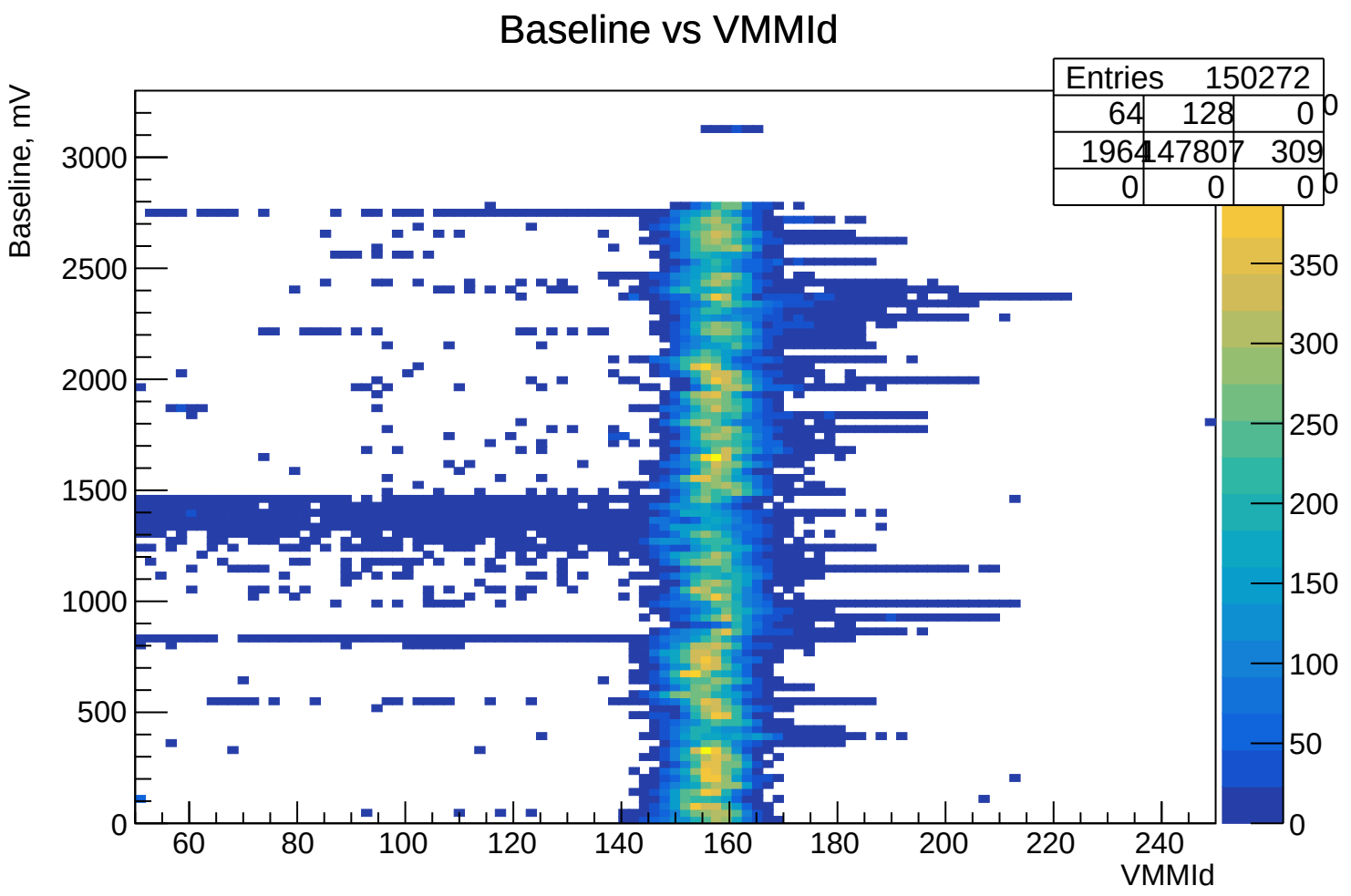
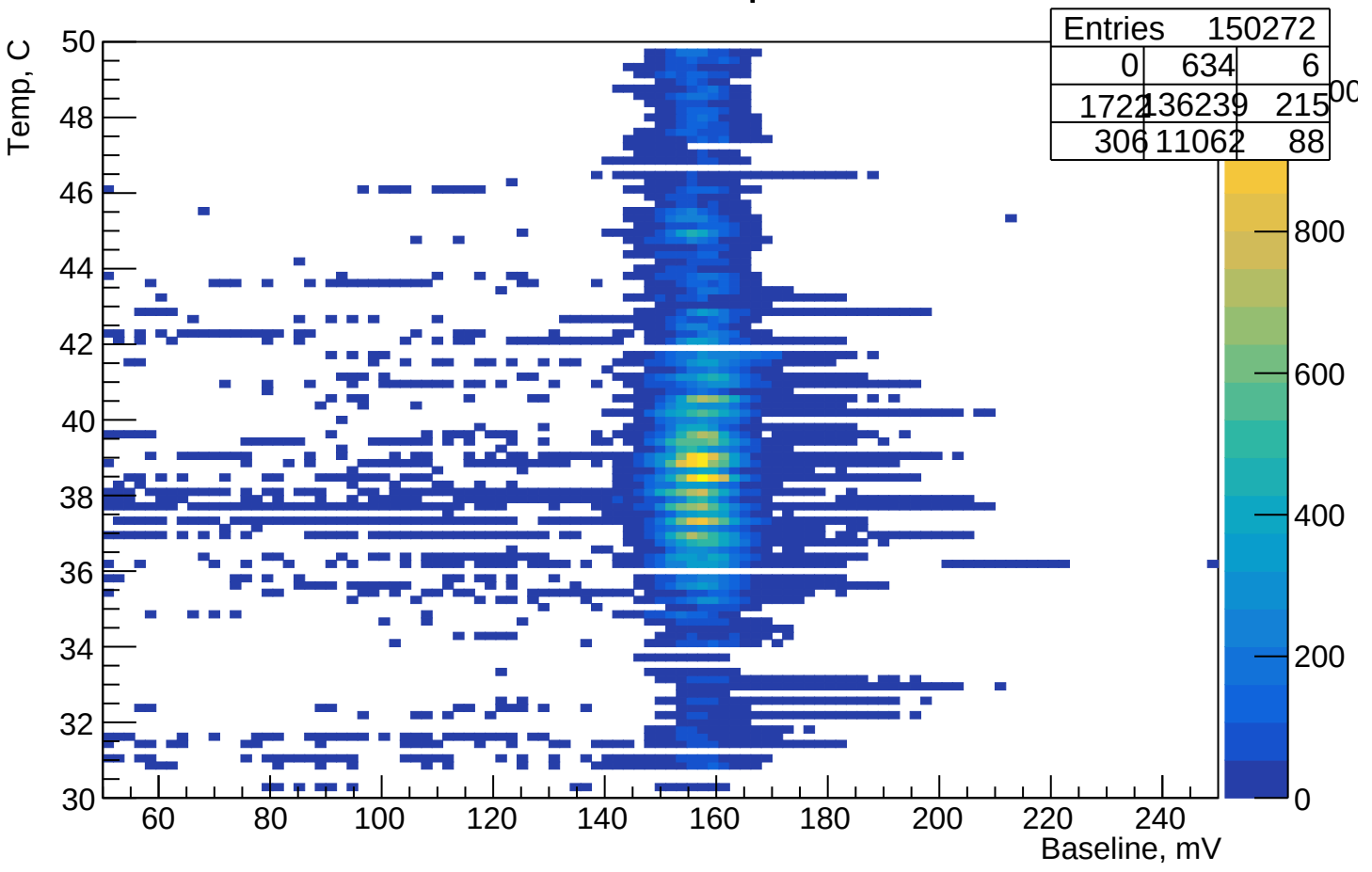
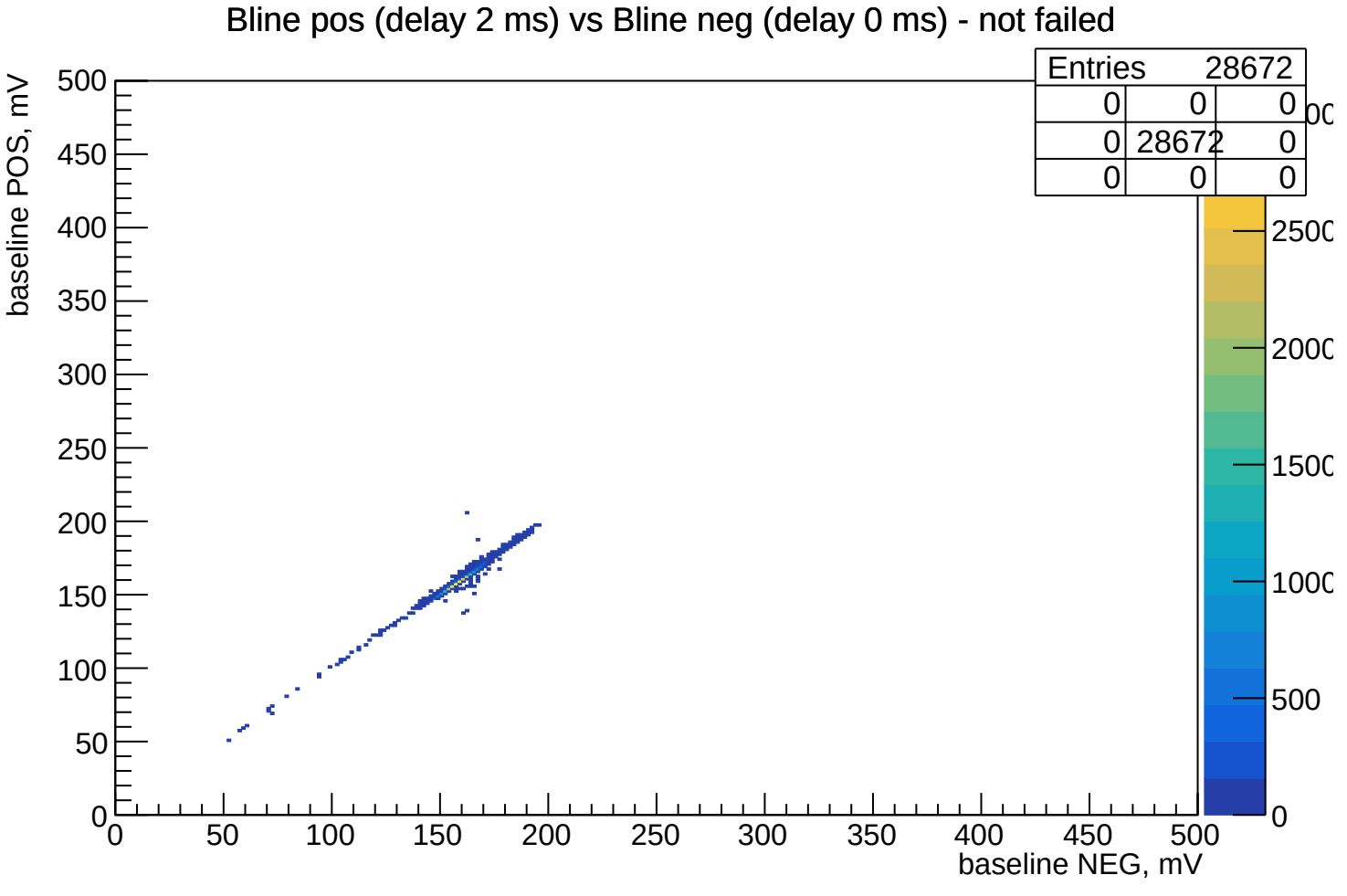

Status VS VMMID
Entries 2348
0 0 0
2347 0 1
0 0 0
Status
VMMId
×10^3
7
6
5
4
3
2
1
0
−1
140
142
144
146
148
150
152
154
156
158
160
162
0.06
0.04
0.02
0
−0.1

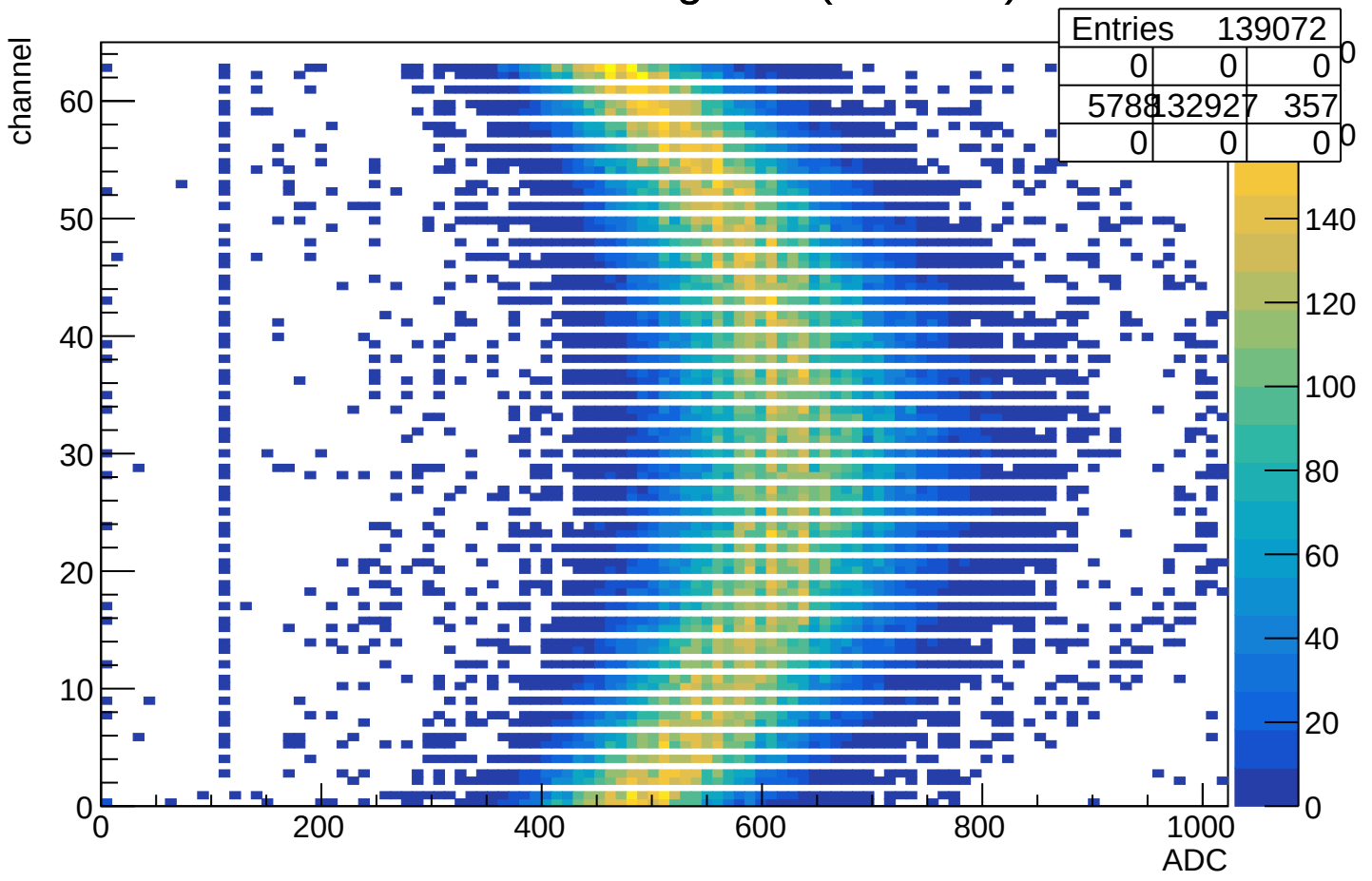

Baseline
Entries 150272
Underflow 2028
Overflow 309
count channels
10^4
10^3
10^2
10
1
60
80
100
120
140
160
180
200
220
240
mV

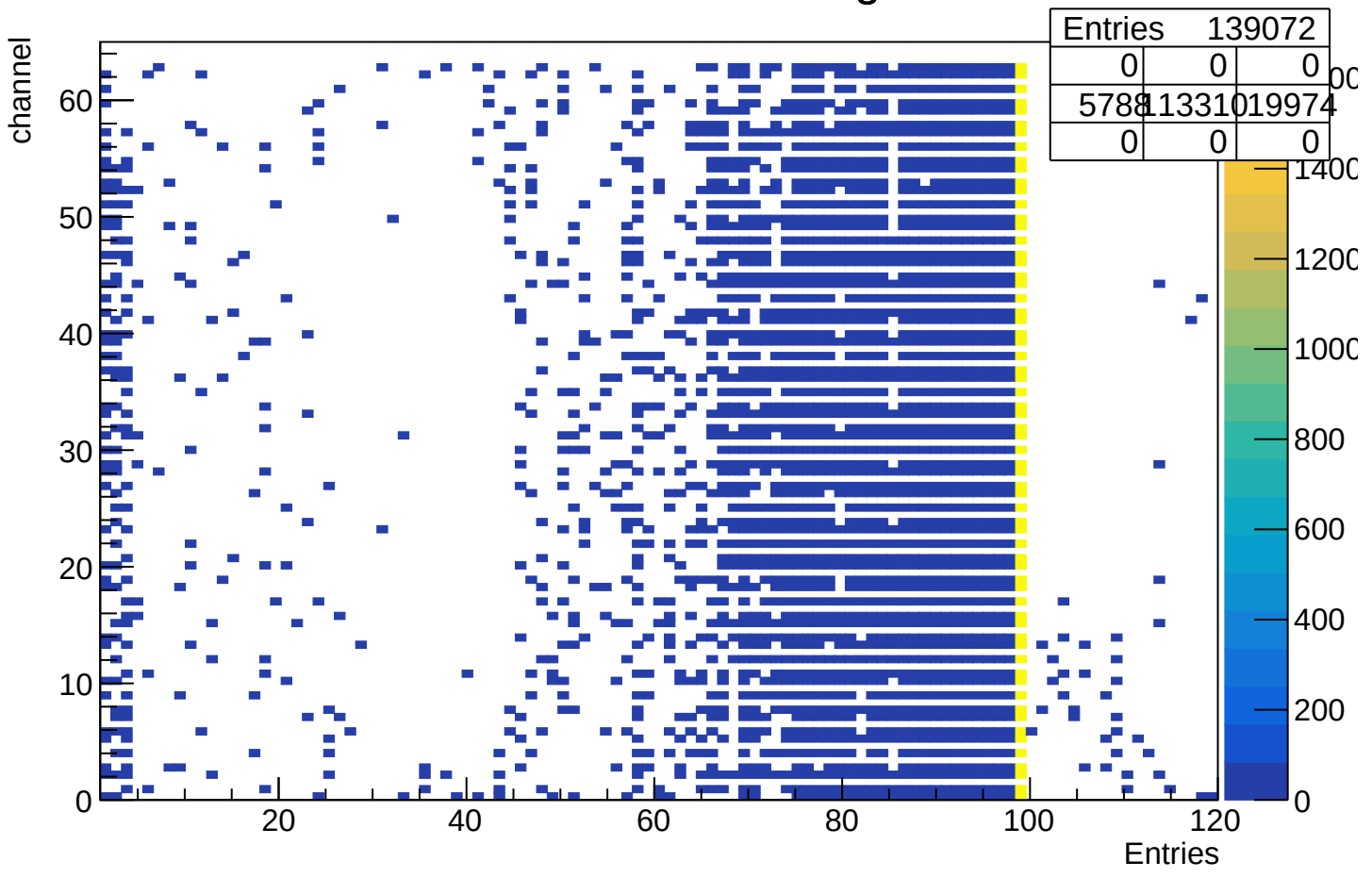

Baseline
Entries 150272
Underflow 2028
Overflow 309
count channels
0
1000
2000
3000
4000
5000
6000
7000
8000
60
80
100
120
140
160
180
200
220
240
mV

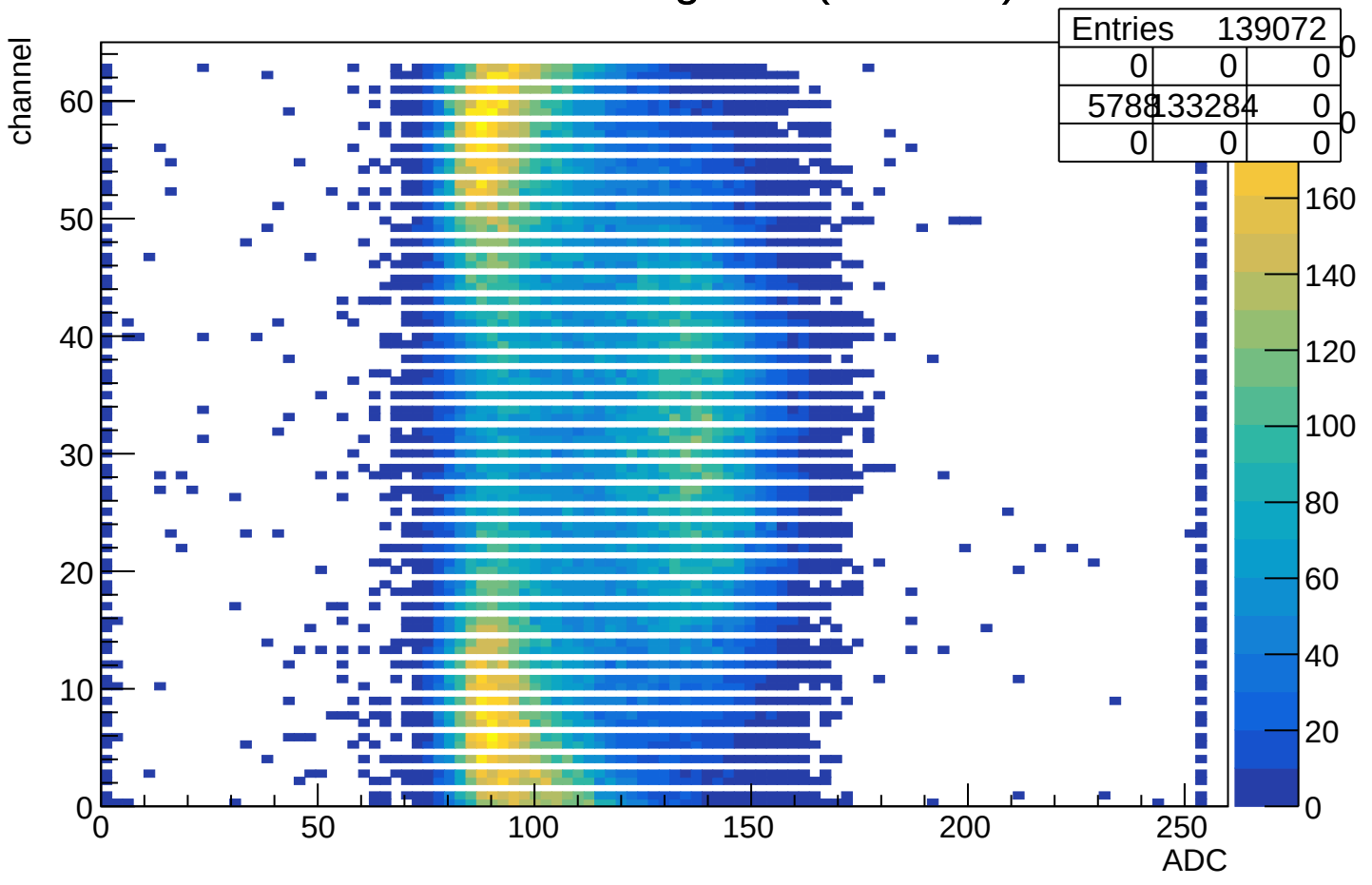

Baseline vs VMMId
Entries 150272
64 128 0
19641478077 309
0 0 0
Baseline, mV
3000
2500
2000
1500
1000
500
0
60
80
100
120
140
160
180
200
220
240
VMMId
350
300
250
200
150
100
50
0

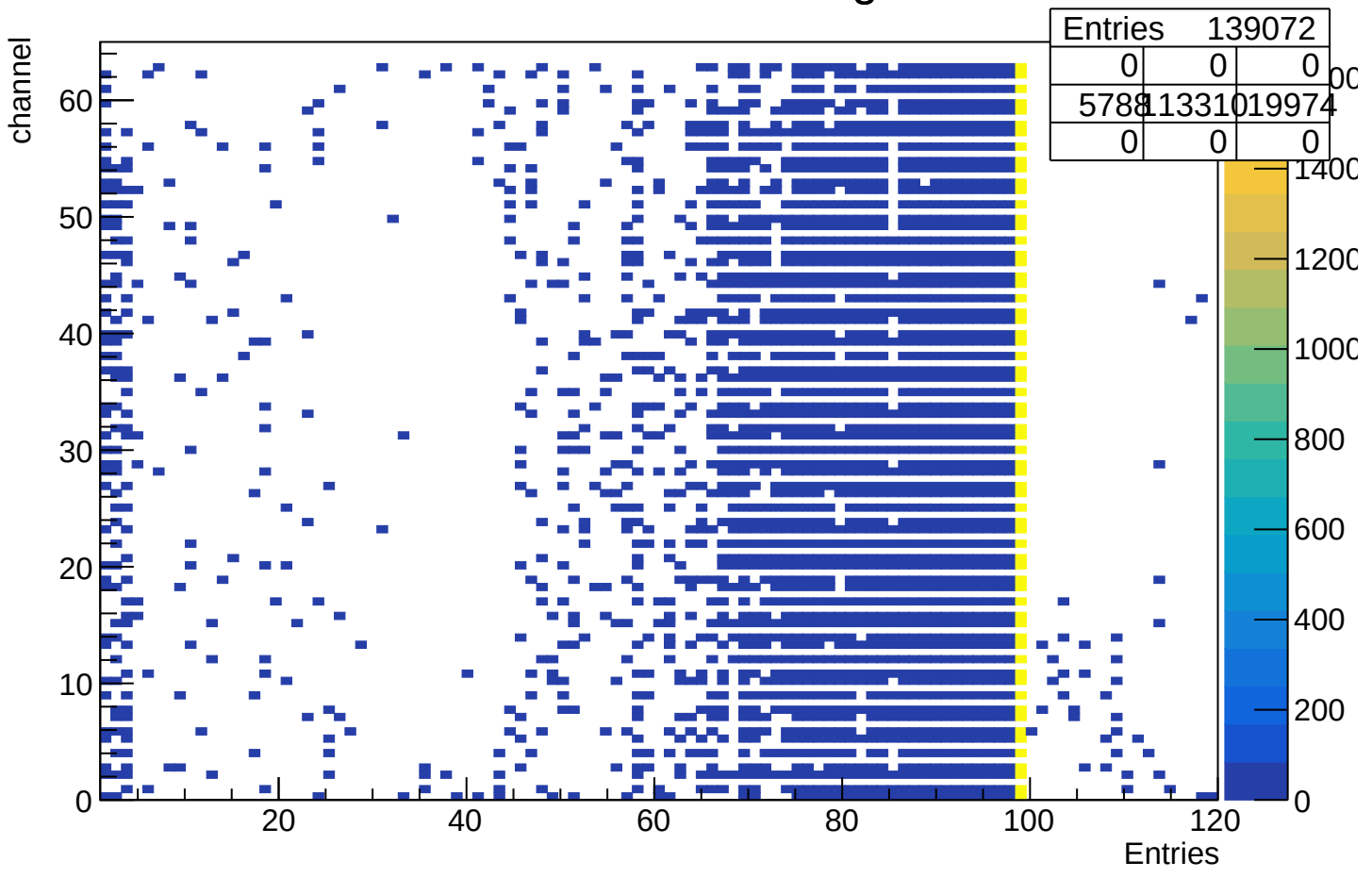

Baseline vs tempreture
Entries 150272
0 634 6
1722 136239 215
306 11062 88
Temp, C
50
48
46
44
42
40
38
36
34
32
30
60
80
100
120
140
160
180
200
220
240
Baseline, mV
800
600
400
200
0

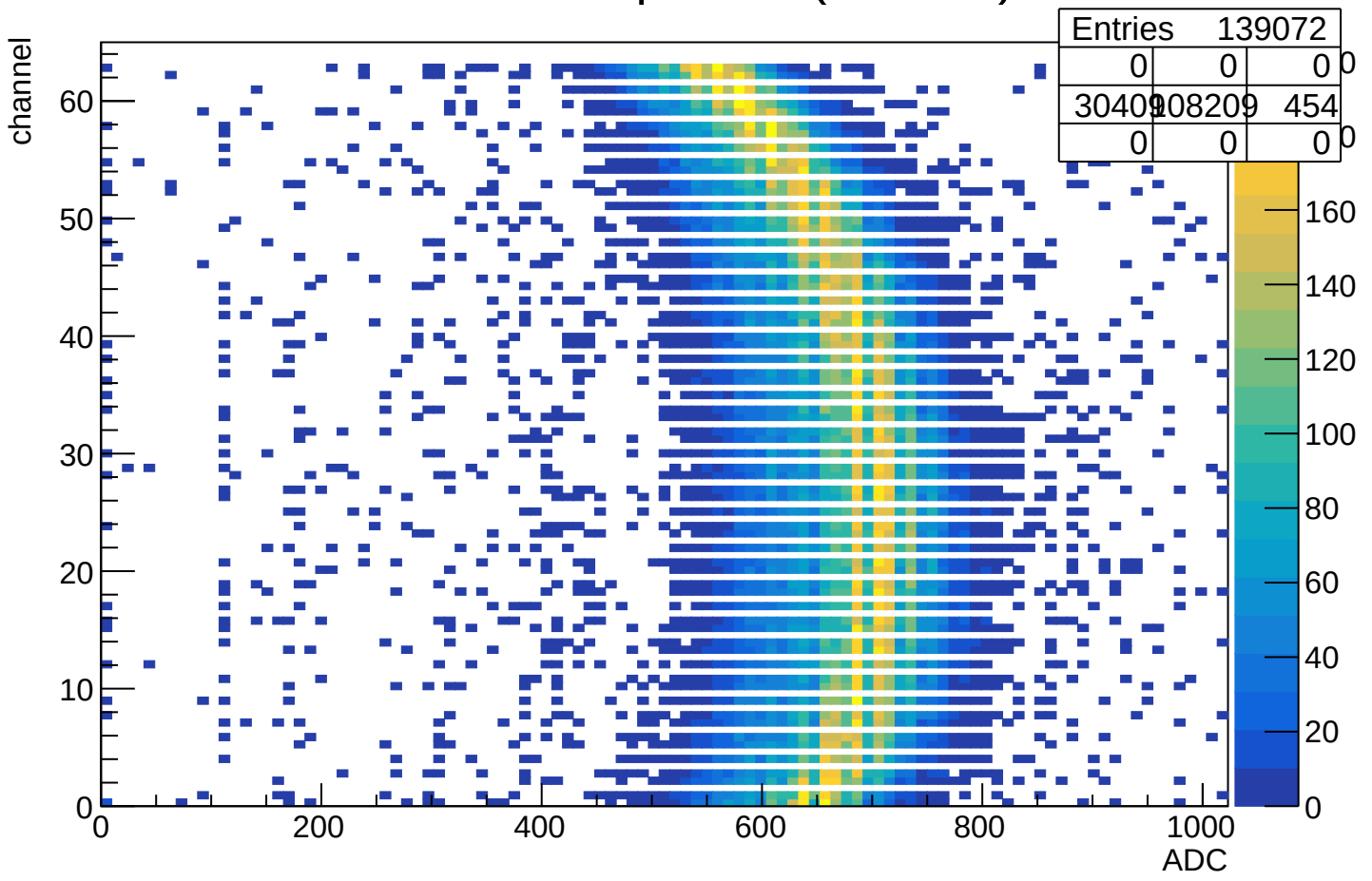

Bline pos (delay 2 ms) vs Bline neg (delay 0 ms) - not failed
Entries 28672
baseline POS, mV
baseline NEG, mV
0
50
100
150
200
250
300
350
400
450
500
2500
2000
1500
1000
500

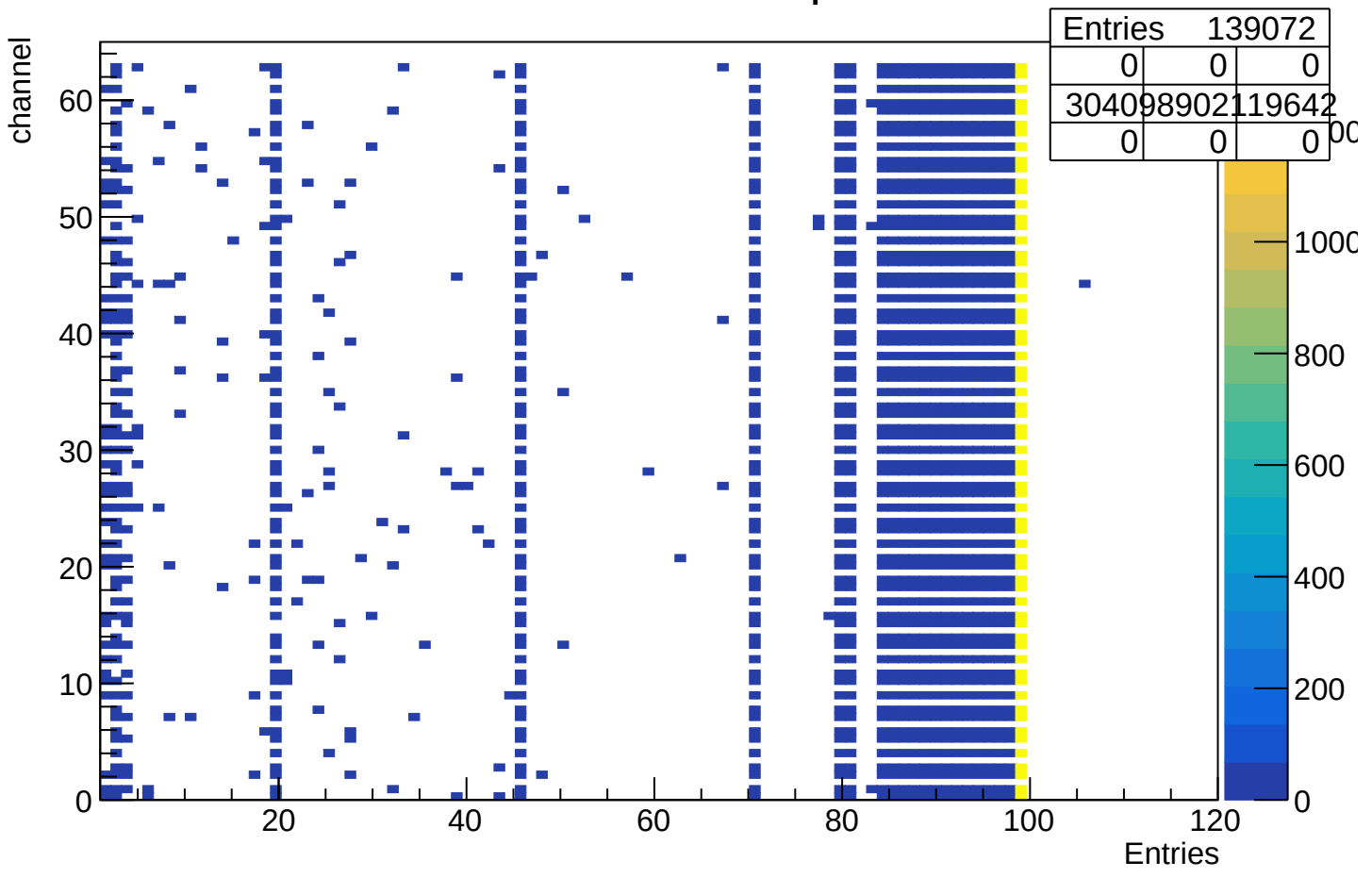

PDO mean L0 negative (all VMM)
Entries 139072
0 0 0
5788 132927 357
0 0 0
channel
ADC
0
10
20
30
40
50
60
0
200
400
600
800
1000
0
20
40
60
80
100
120
140

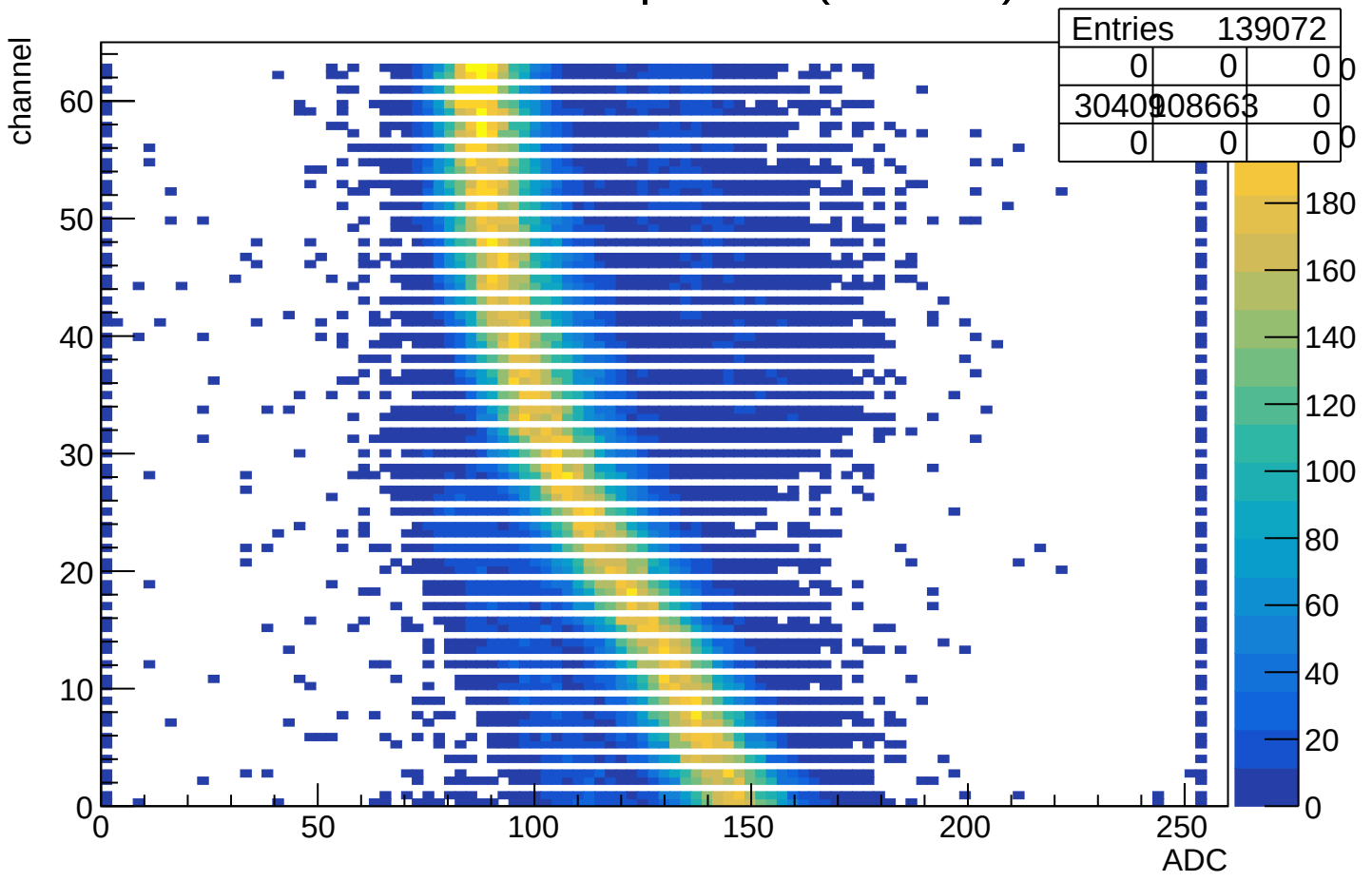

PDO entries mean L0 negative
Entries 139072
0 0 0
5788 1133 19974
0 0 0
channel
0
10
20
30
40
50
60
20
40
60
80
100
120
Entries
200
400
600
800
1000
1200
1400

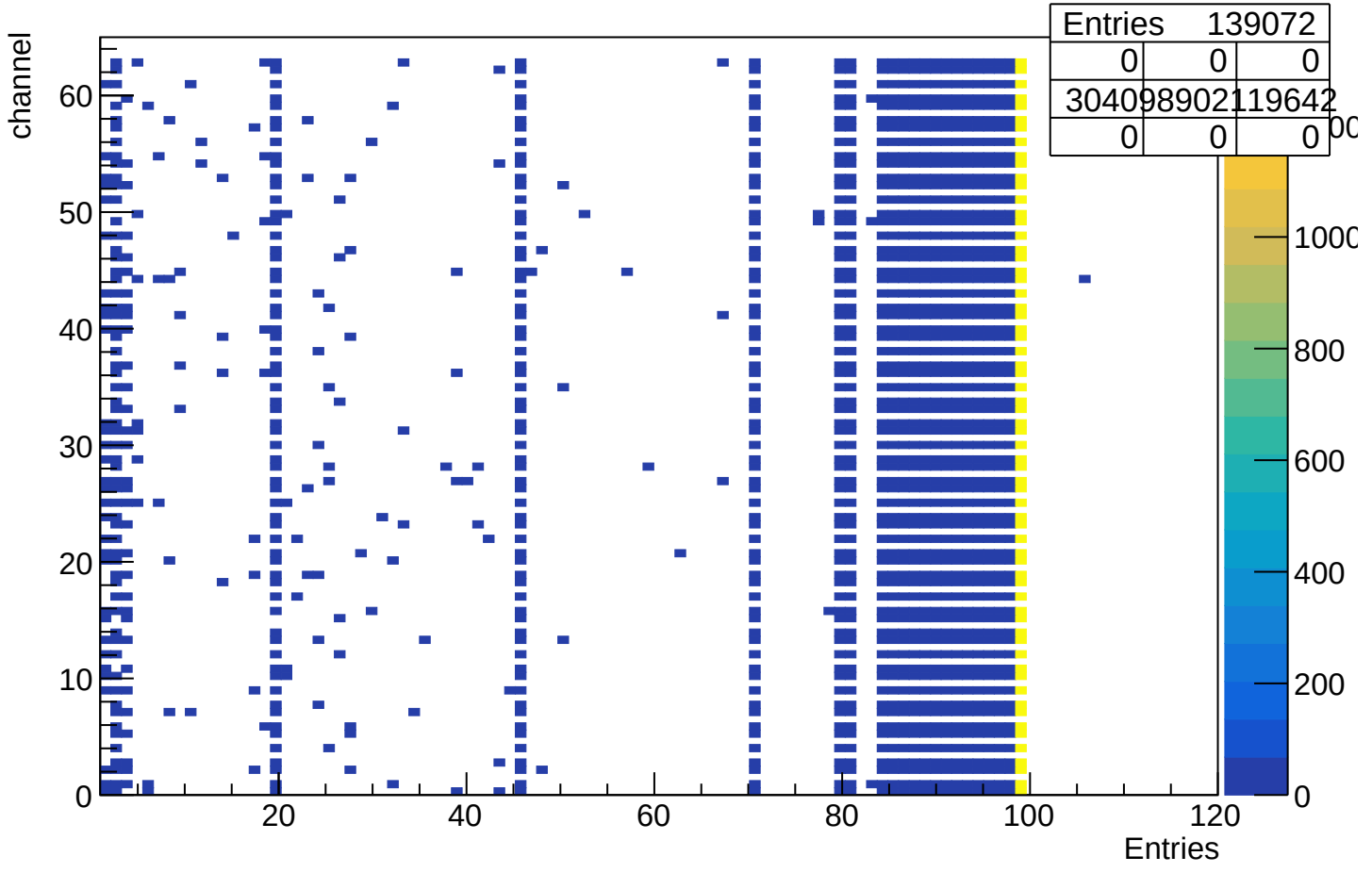

TDO mean L0 negative (all VMM)
Entries 139072
0 0 0
5788 133284 0
0 0 0
channel
0
10
20
30
40
50
60
0
50
100
150
200
250
ADC
0
20
40
60
80
100
120
140
160

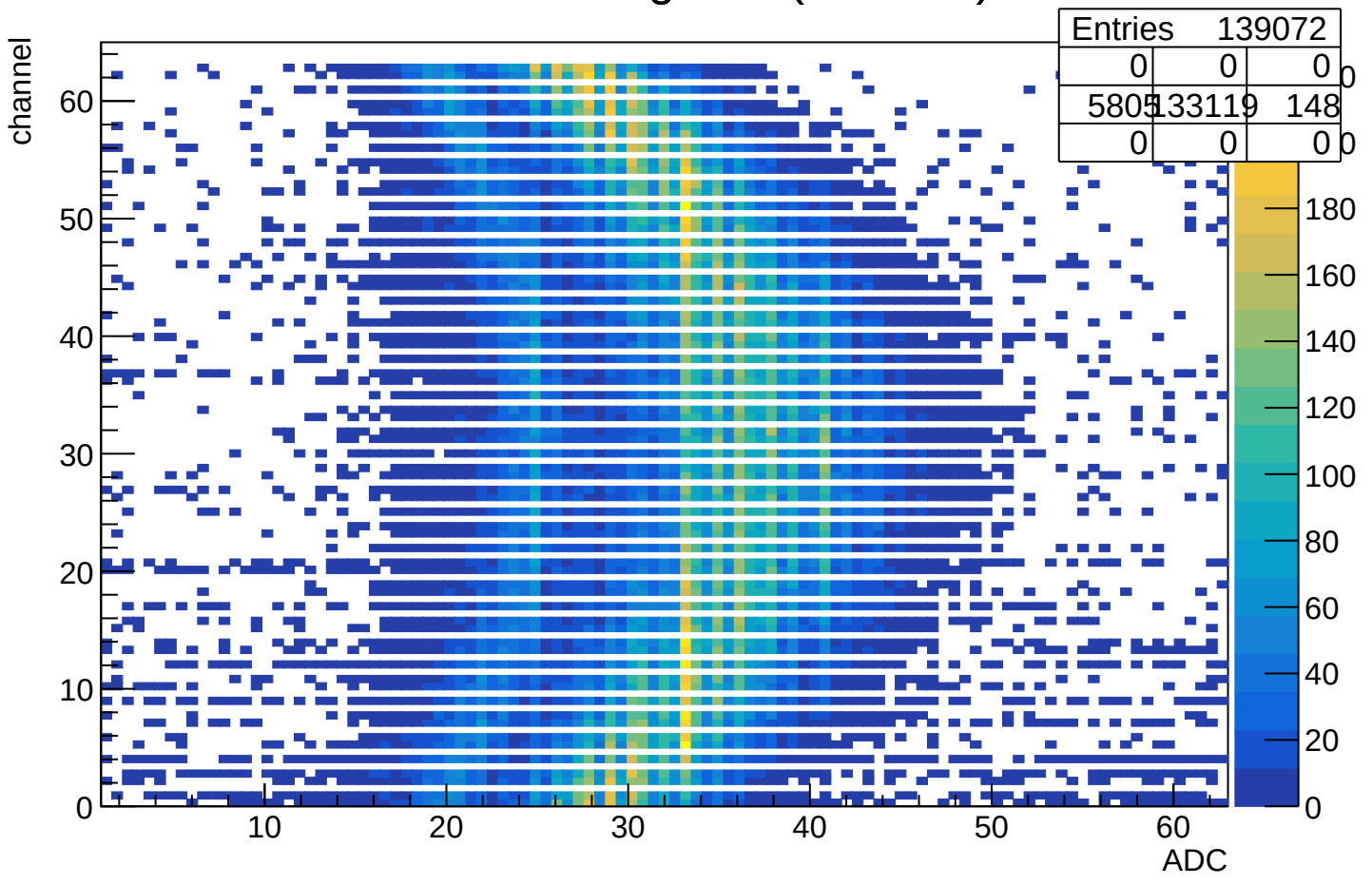

TDO entries mean L0 negative
Entries 139072
0 0 0
5788 11331 19974
0 0 0
channel
Entries
0
10
20
30
40
50
60
20
40
60
80
100
120
0
200
400
600
800
1000
1200
1400

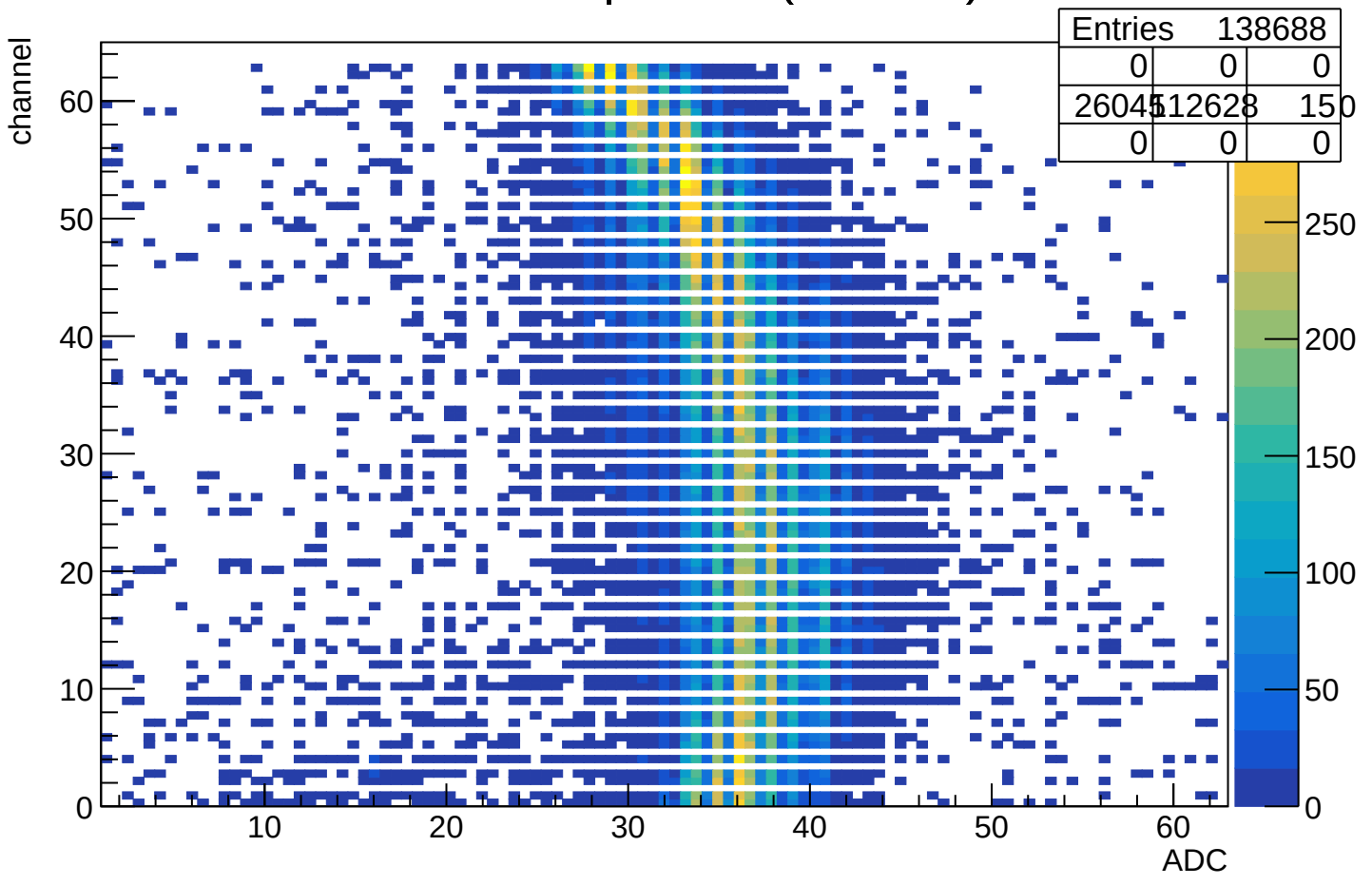

PDO mean L0 positive (all VMM)
Entries 139072
0 0 0 0
3040 108209 454
0 0 0 0
channel
0
10
20
30
40
50
60
0
200
400
600
800
1000
ADC
0
20
40
60
80
100
120
140
160

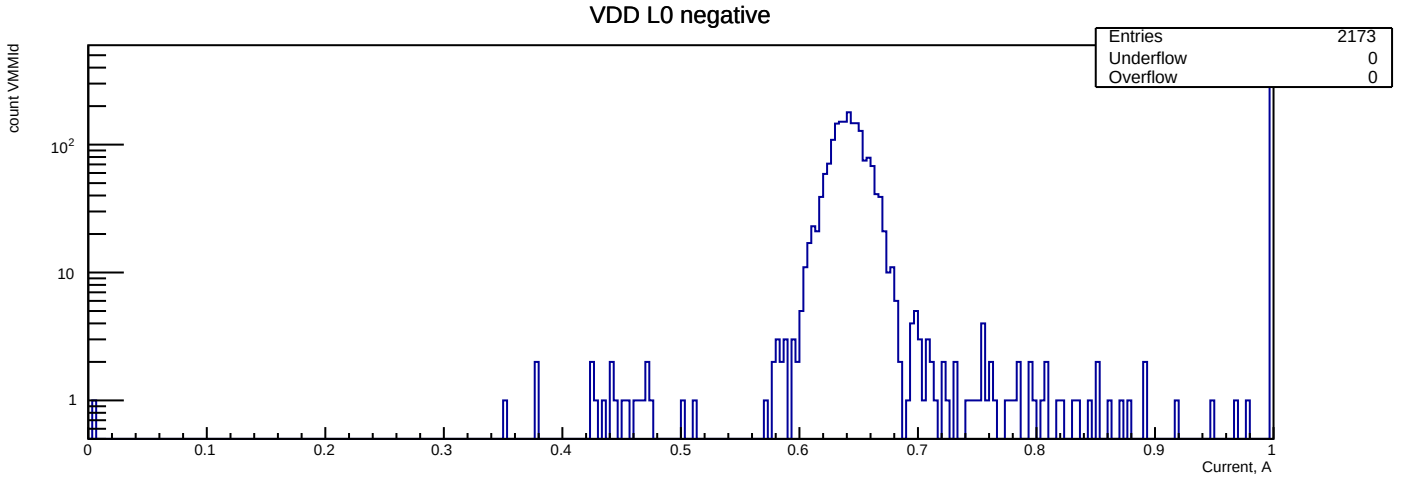

PDO entries mean L0 positive
Entries 139072
0 0 0
3040989021196420 0 0
channel
Entries
0
10
20
30
40
50
60
20
40
60
80
100
120
200
400
600
800
1000

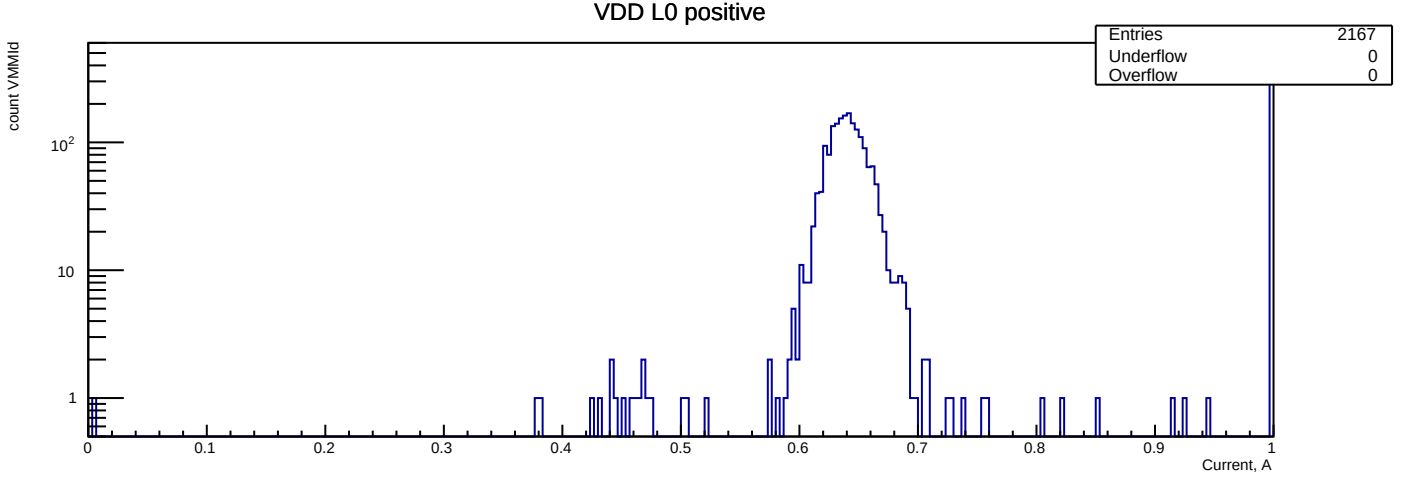

TDO mean L0 positive (all VMM)
Entries 139072
channel
ADC
0
50
100
150
200
250
10
20
30
40
60
180
160
140
120
100
80
60
40
20

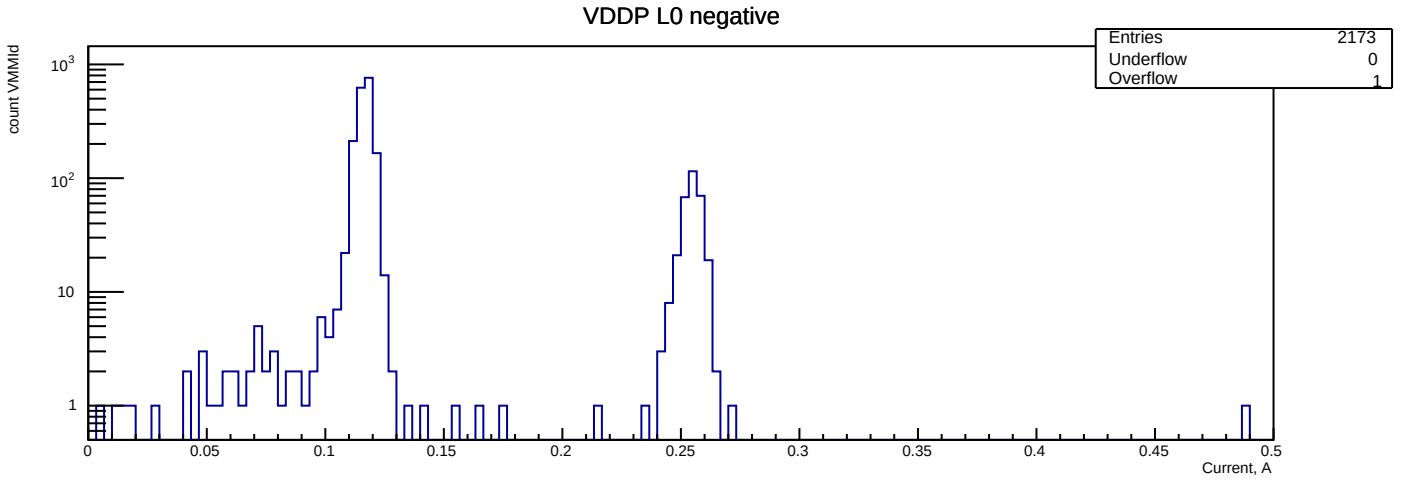

TDO entries mean L0 positive
Entries 139072
0 0 0
3040989021196 42
0 0 0
channel
0
10
20
30
40
50
60
20
40
60
80
100
120
Entries
200
400
600
800
1000

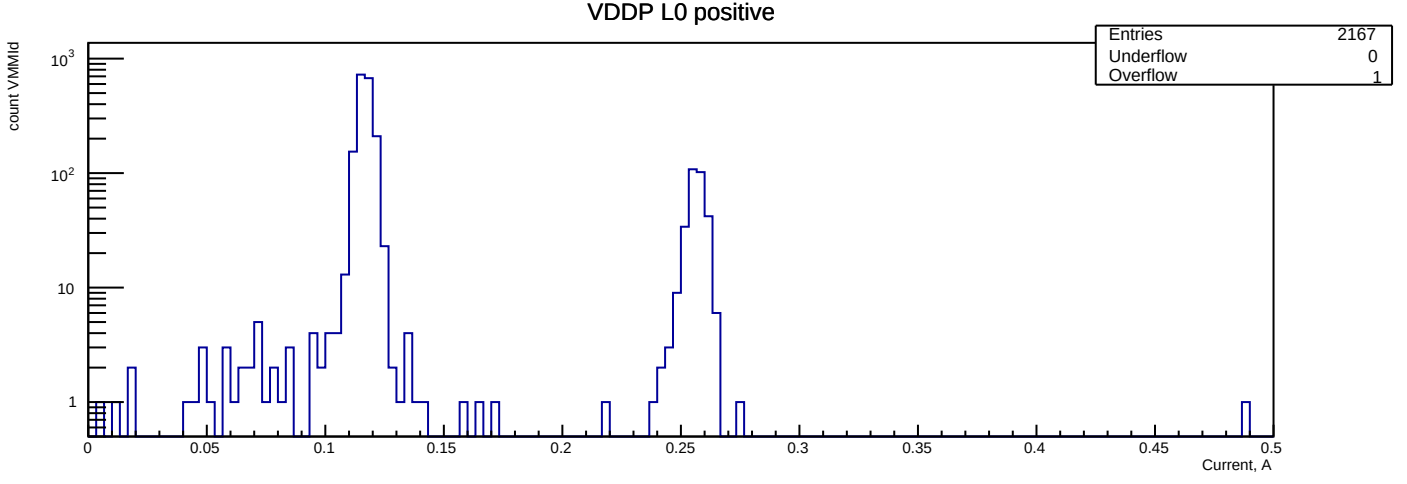

DDO mean negative (all VMM)
Entries 139072
0 0 0
5805 133119 148
0 0 0
channel
0
10
20
30
40
50
60
ADC
10
20
30
40
50
60
0
20
40
60
80
100
120
140
160
180

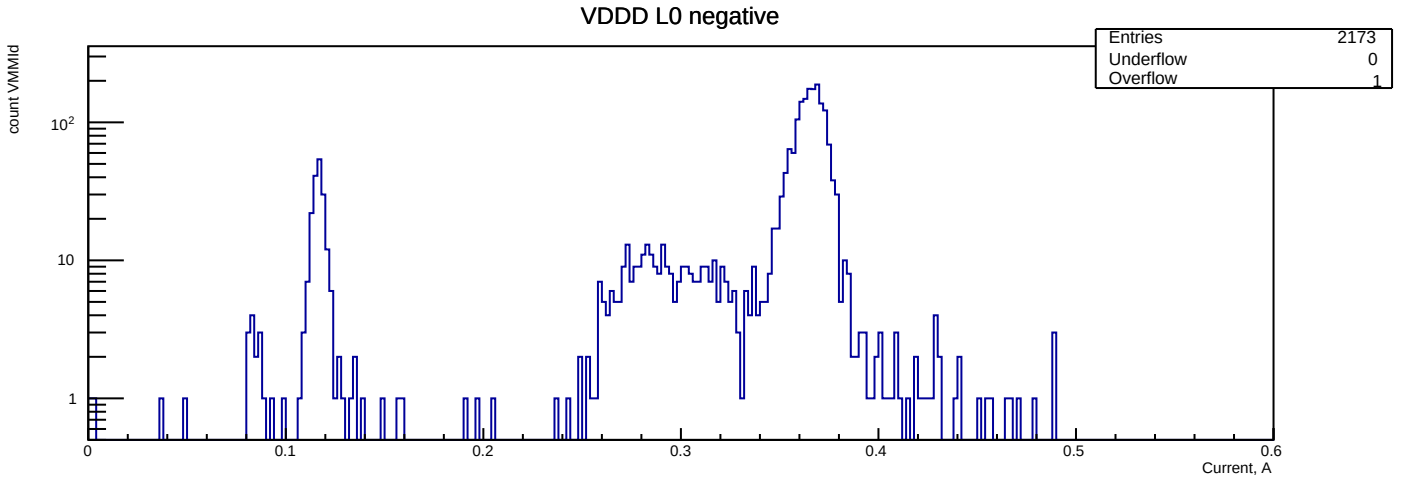

DDO mean positive (all VMM)
Entries 138688
0 0 0
26045 112628 150
0 0 0
channel
ADC
0
10
20
30
40
50
60
0
50
100
150
200
250

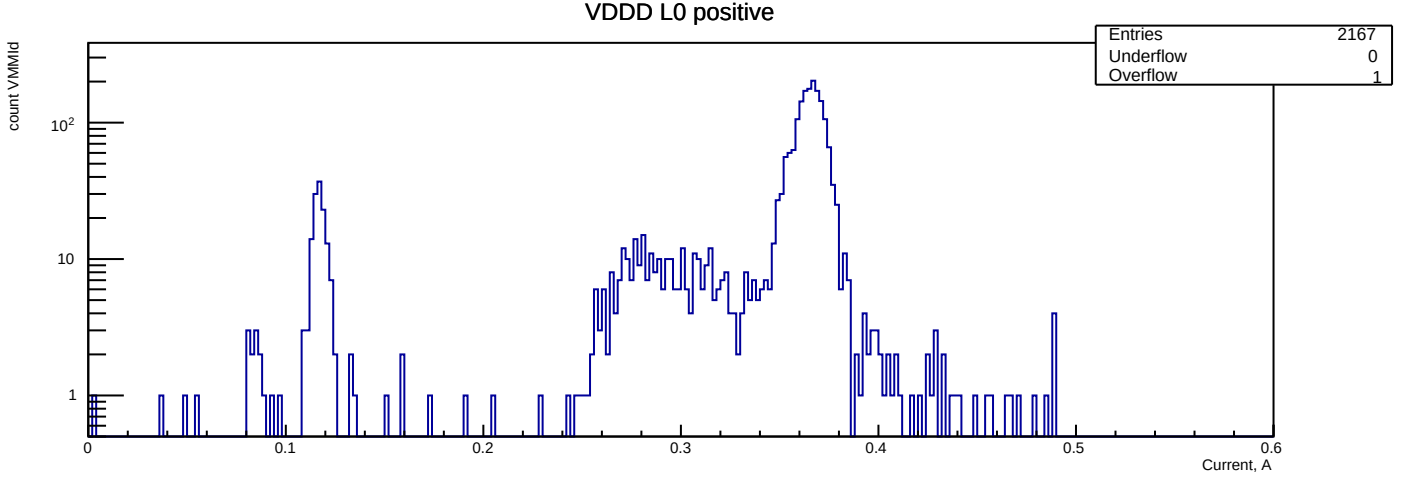

VDD L0 negative
Entries 2173
Underflow 0
Overflow 0
count VMMId
10^2
10
1
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Current, A

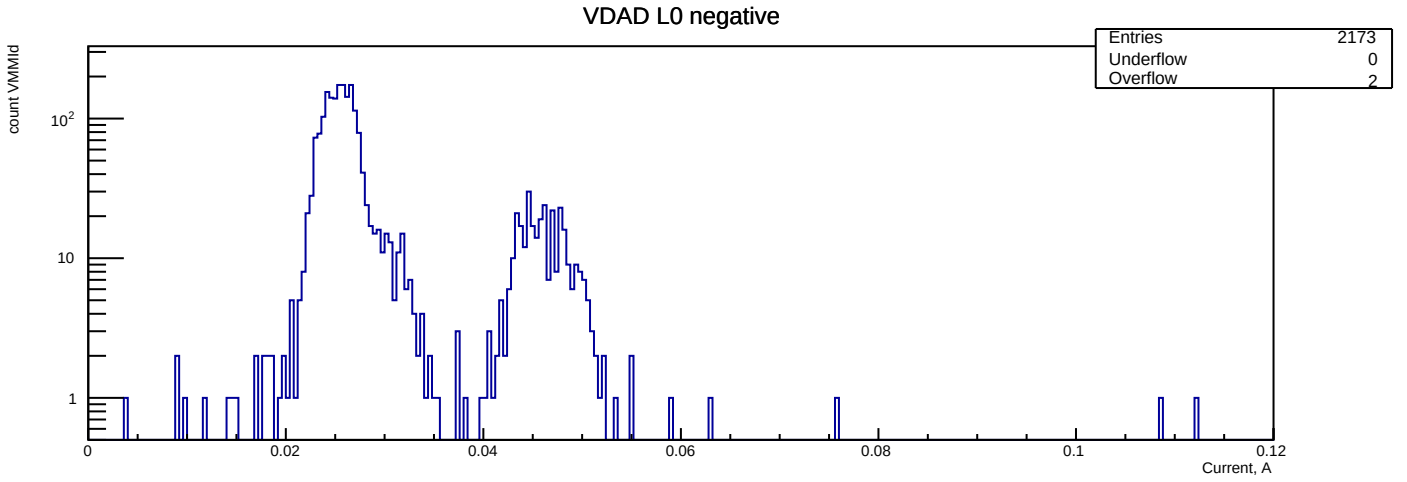

VDD L0 positive
Entries 2167
Underflow 0
Overflow 0
count VMMId
10^2
10
1
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Current, A

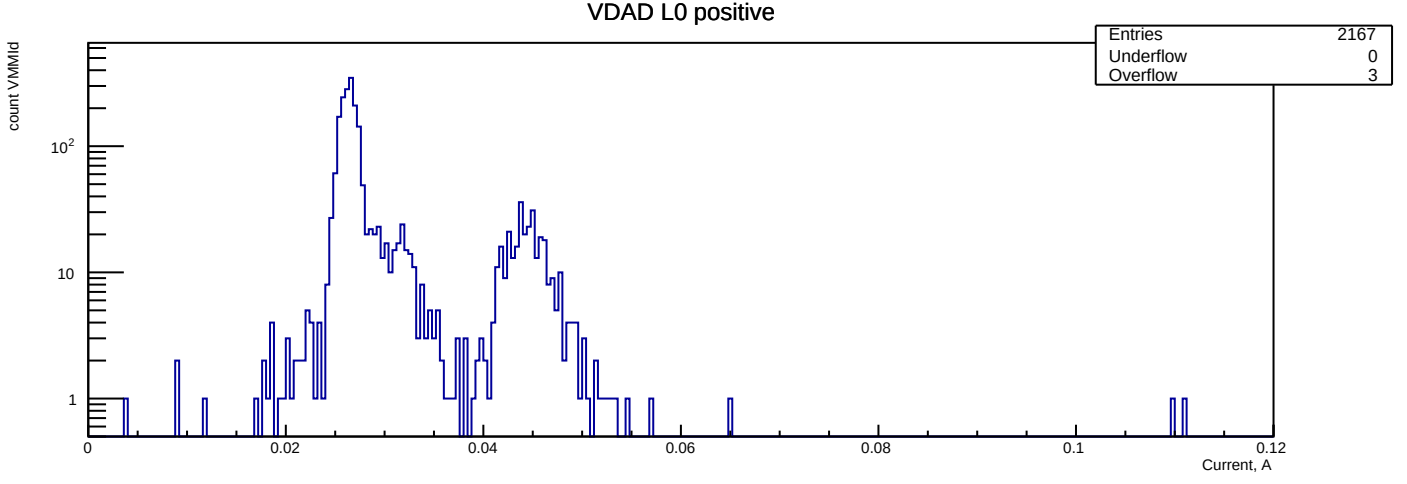

VDDP L0 negative
Entries 2173
Underflow 0
Overflow 1
count VMMId
10^3
10^2
10
1
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
Current, A

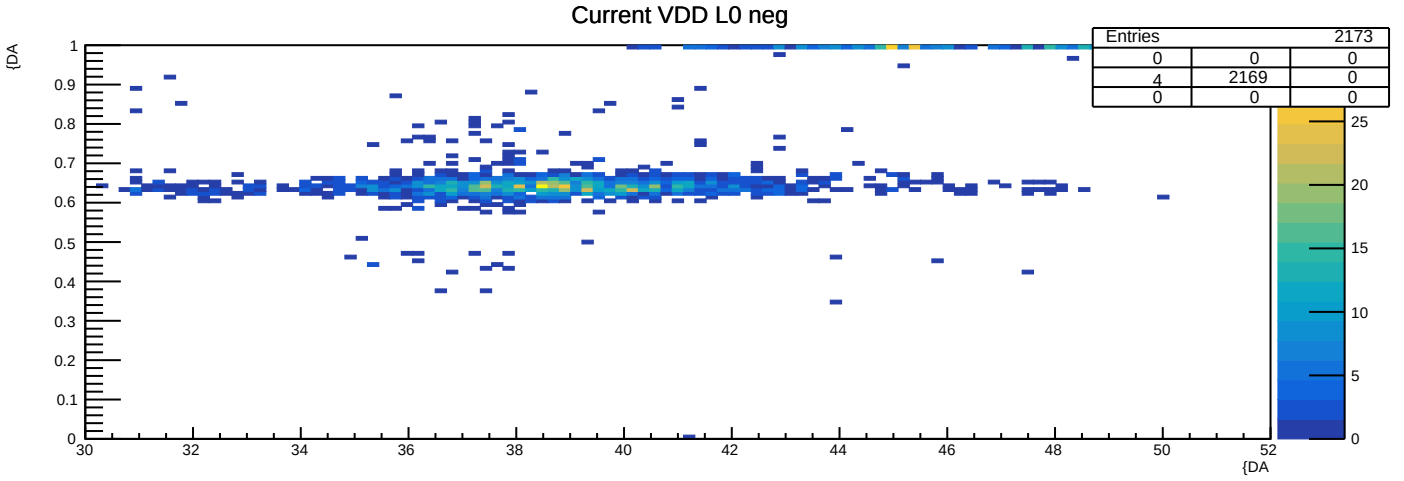

VDDP L0 positive
Entries 2167
Underflow 0
Overflow 1
count VMMId
10^3
10^2
10
1
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
Current, A

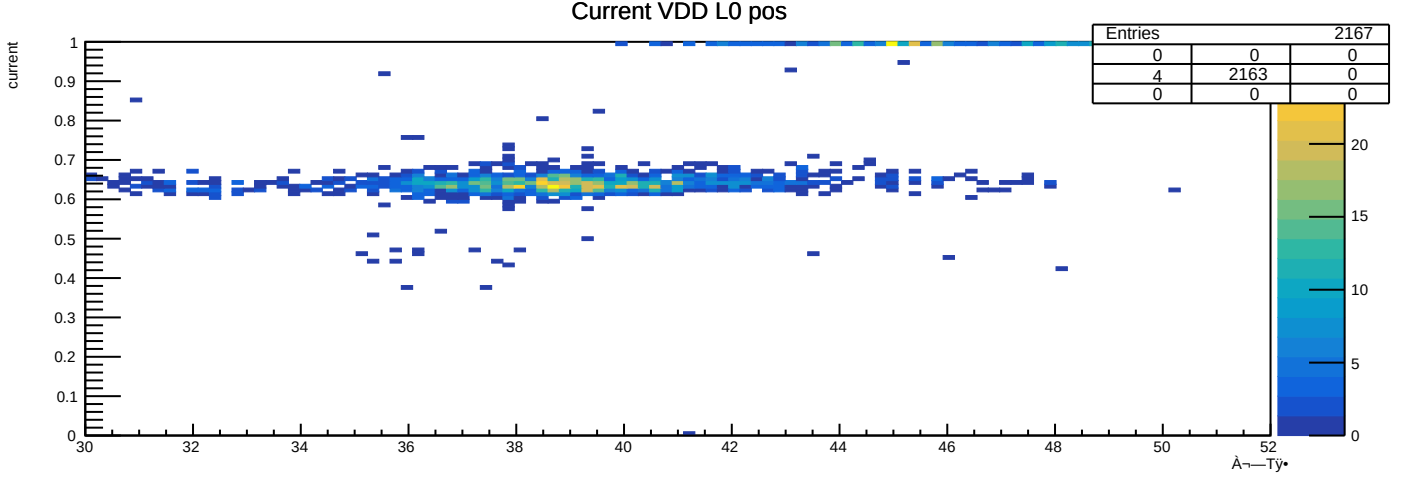

VDDD L0 negative
Entries 2173
Underflow 0
Overflow 1
count VMMId
10^2
10
1
0
0.1
0.2
0.3
0.4
0.5
0.6
Current, A

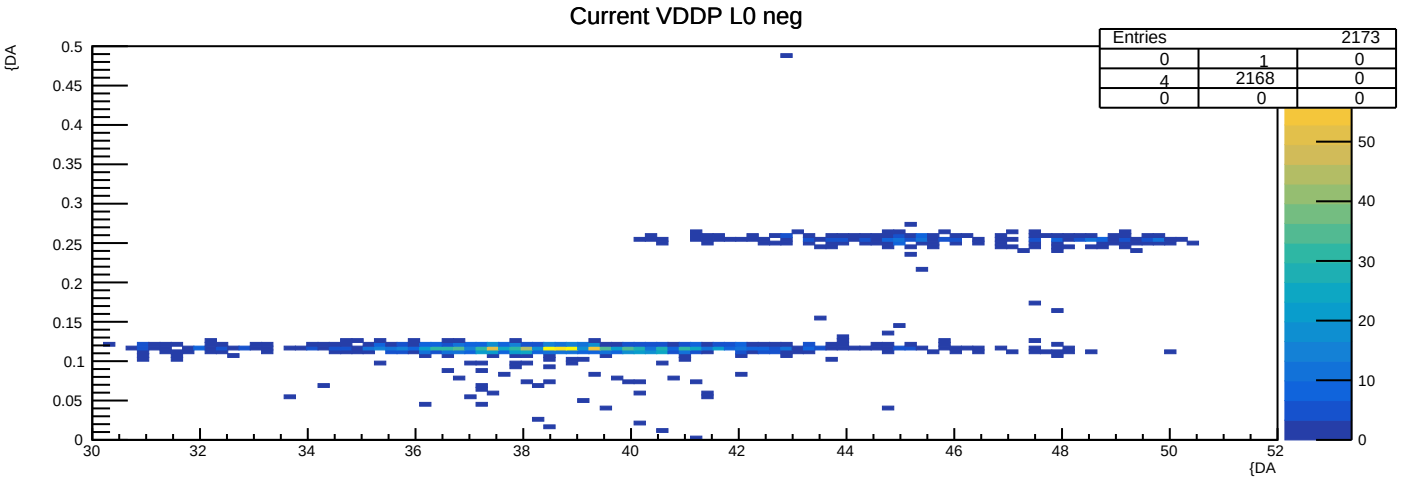

VDDD L0 positive
Entries 2167
Underflow 0
Overflow 1
count VMMId
10^2
10
1
0
0.1
0.2
0.3
0.4
0.5
0.6
Current, A

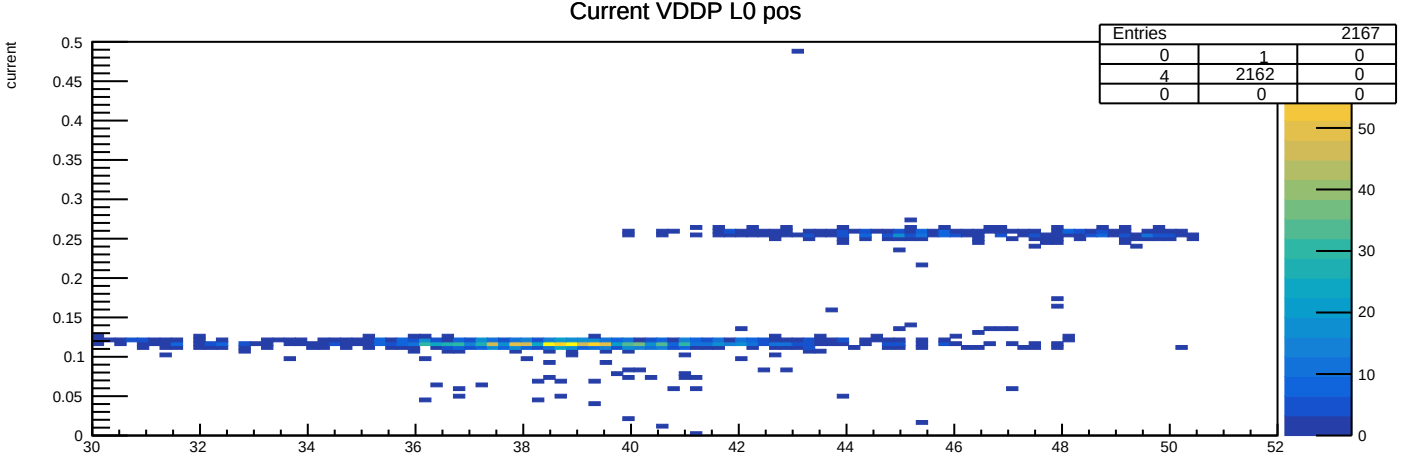

VDAD L0 negative
Entries 2173
Underflow 0
Overflow 2
count VMMId
10^2
10
1
0
0.02
0.04
0.06
0.08
0.1
0.12
Current, A

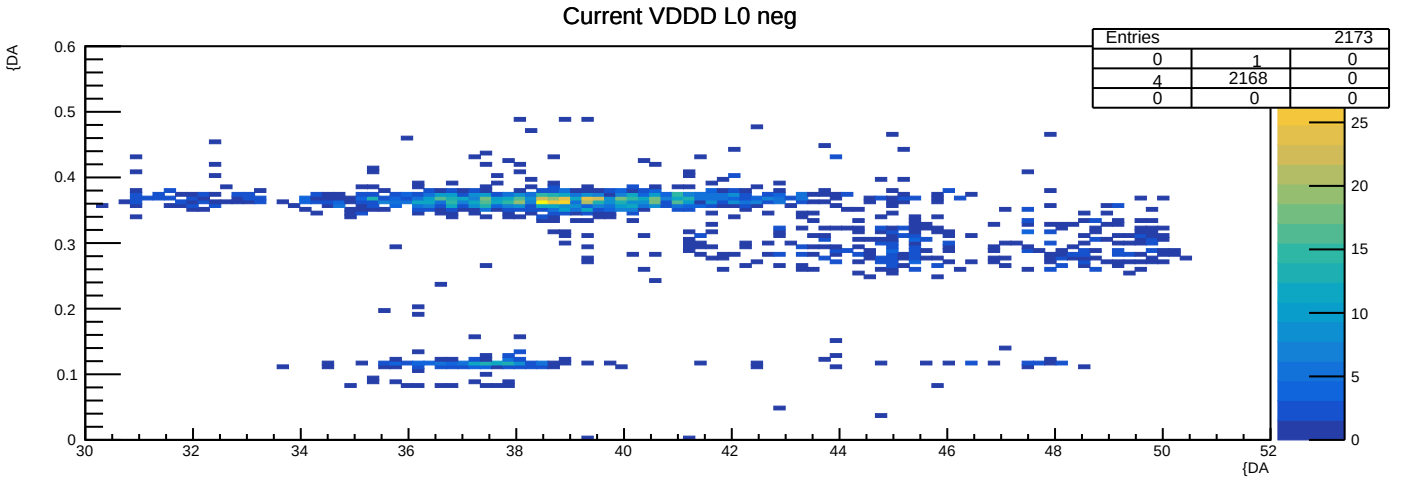

VDAD L0 positive
Entries 2167
Underflow 0
Overflow 3
count VMMId
10^2
10
1
0
0.02
0.04
0.06
0.08
0.1
0.12
Current, A

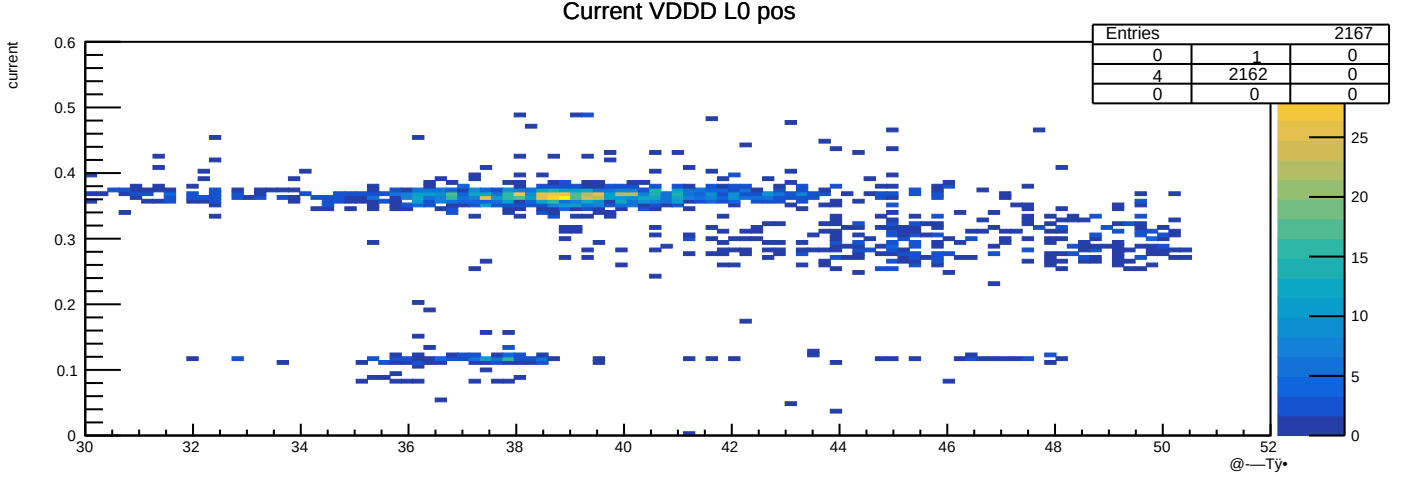

Current VDD L0 neg
{DA
Entries 2173
0 0 0
4 2169 0
0 0 0
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
30
32
34
36
38
40
42
44
46
48
50
52
{DA
25
20
15
10
5
0

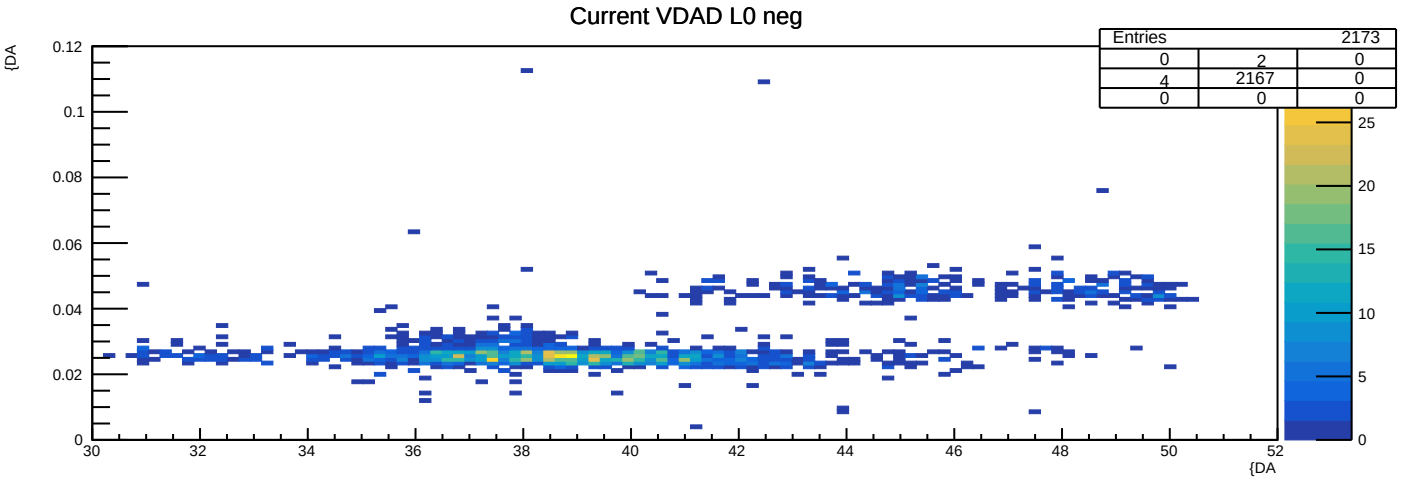

Current VDD L0 pos
current
Entries 2167
0 0 0
4 2163 0
0 0 0
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
30
32
34
36
38
40
42
44
46
48
50
52
Å¬—Tÿ•
20
15
10
5
0

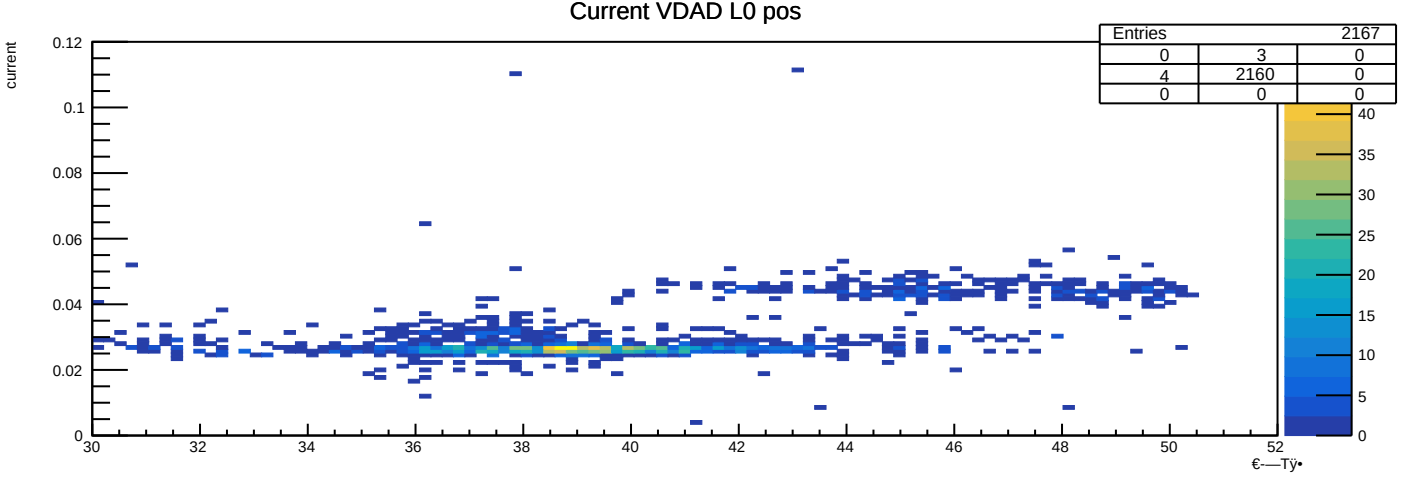

Current VDDP L0 neg
Entries 2173
0 1 0
4 2168 0
0 0 0
{DA
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
30
32
34
36
38
40
42
44
46
48
50
52
{DA
50
40
30
20
10
0

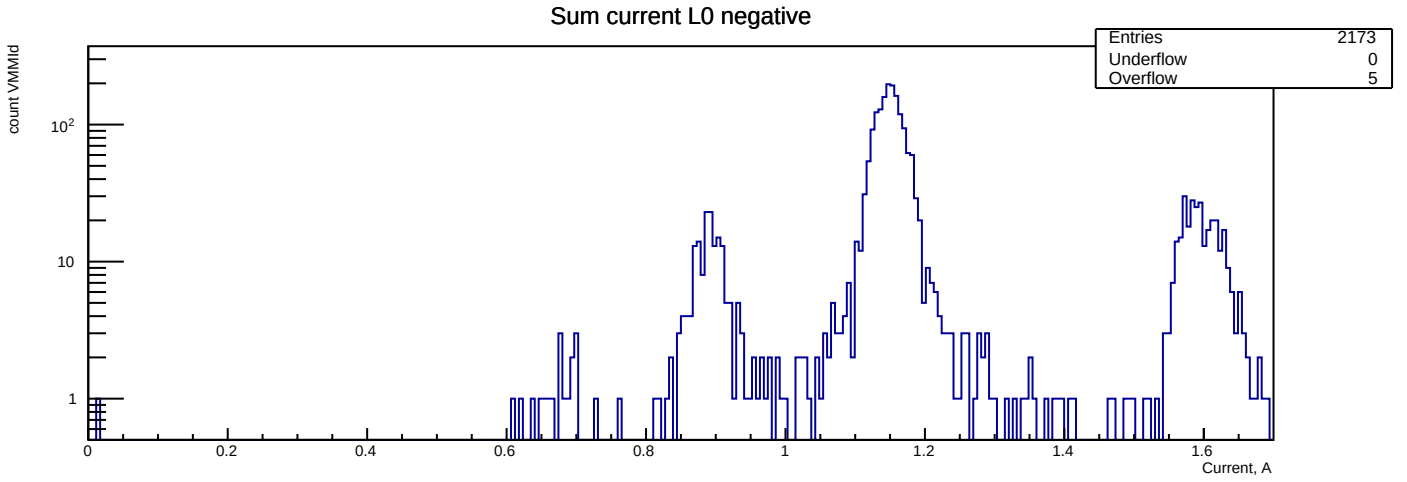

Current VDDP L0 pos
Entries 2167
0 1 0
4 2162 0
0 0 0
current
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
30
32
34
36
38
40
42
44
46
48
50
52
50
40
30
20
10
0

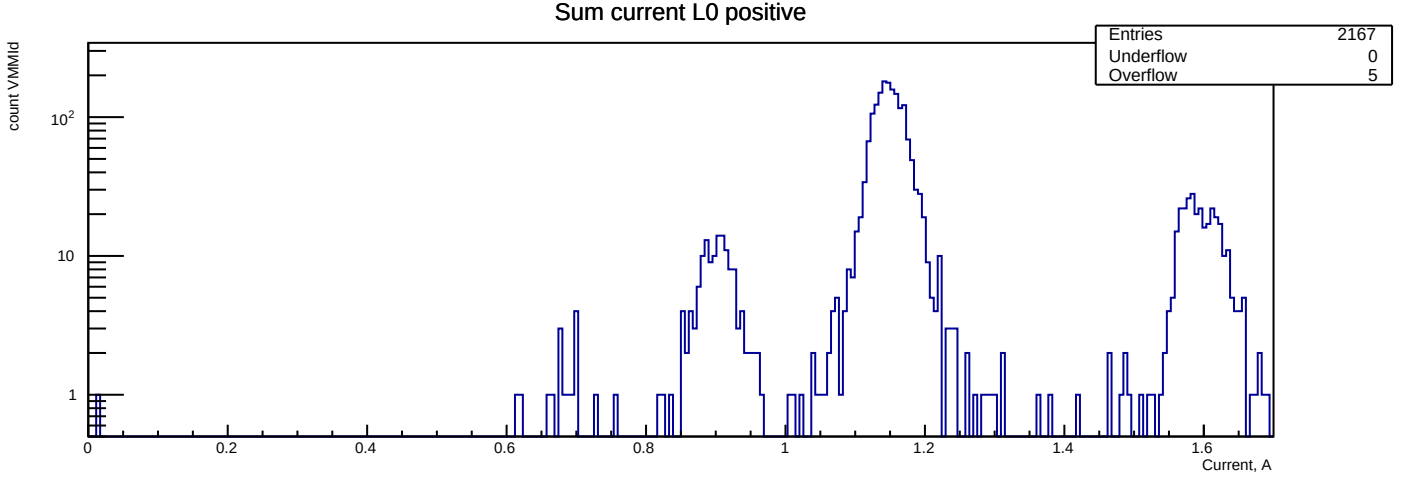

Current VDDD L0 neg
Entries 2173
0 1 0
4 2168 0
0 0 0
{DA
{DA

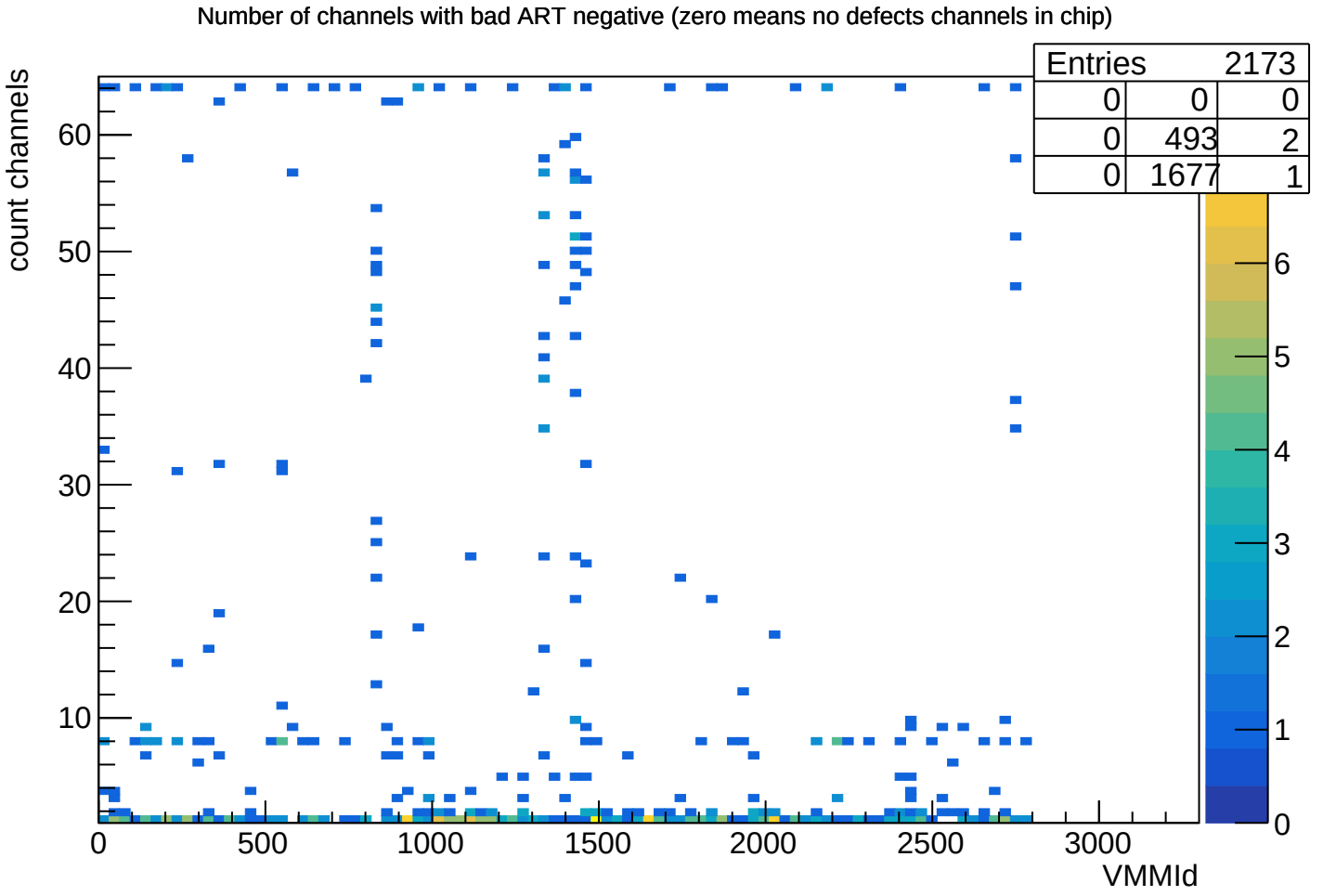

Current VDDD L0 pos
Entries 2167
0 1 0
4 2162 0
0 0 0
current
@—Tÿ•

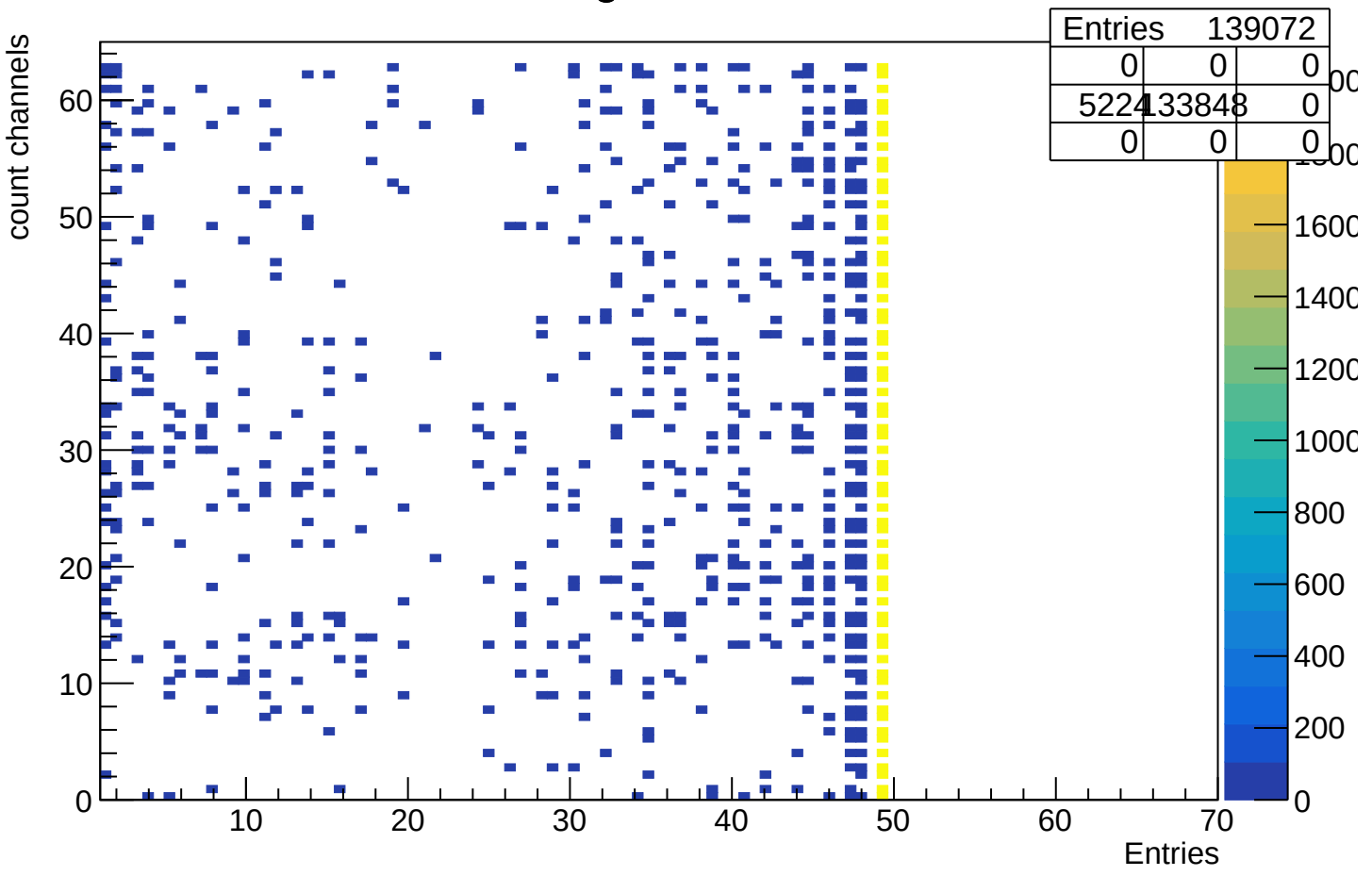

Current VDAD L0 neg
Entries 2173
0 2 0
4 2167 0
0 0 0
{DA
0.12
0.1
0.08
0.06
0.04
0.02
0
30 32 34 36 38 40 42 44 46 48 50 52
{DA
25 20 15 10 5 0

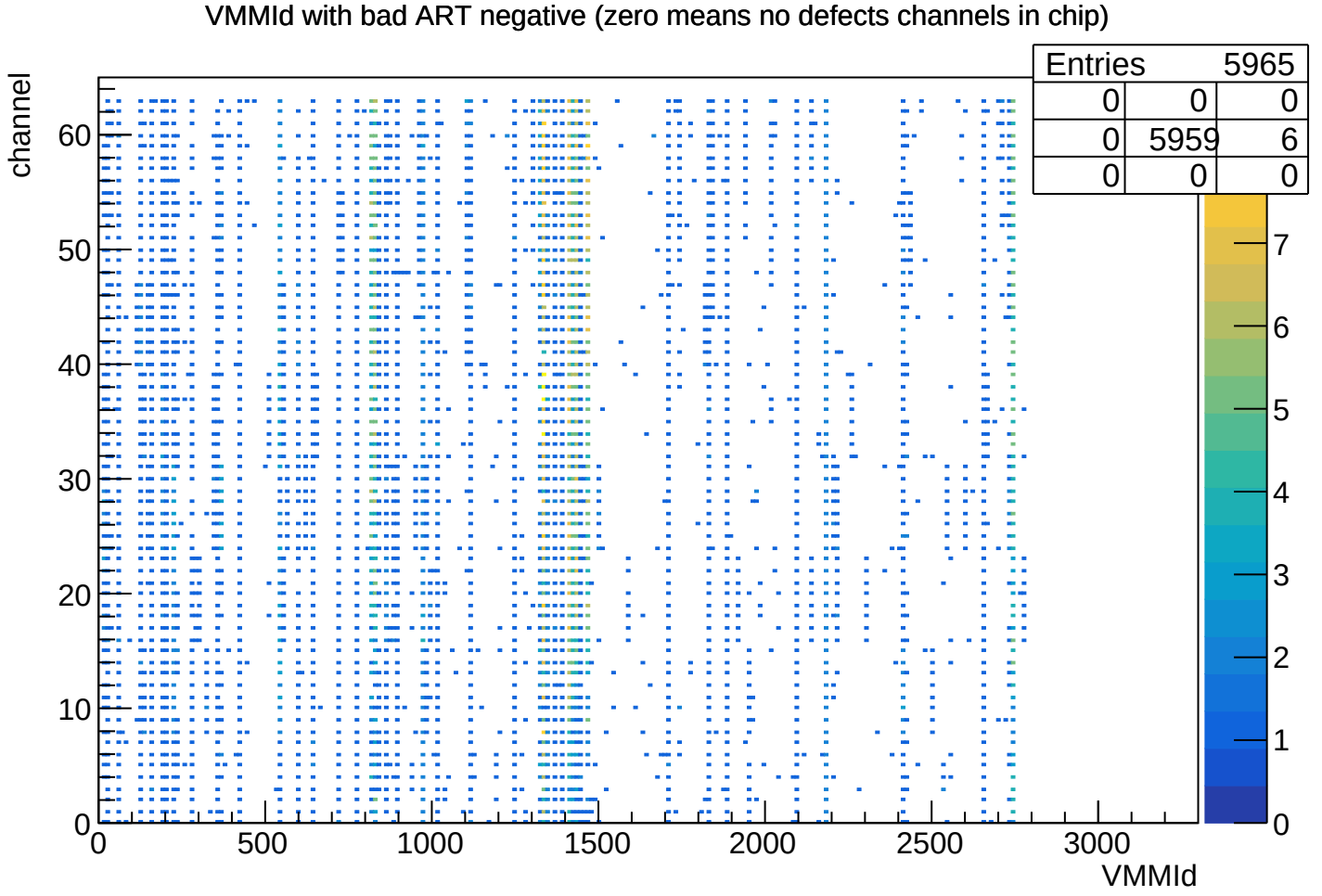

Current VDAD L0 pos
Entries 2167
0 3 0
4 2160 0
0 0 0
current
0.12
0.1
0.08
0.06
0.04
0.02
0
30 32 34 36 38 40 42 44 46 48 50 52
€-—Tÿ•
40 35 30 25 20 15 10 5 0

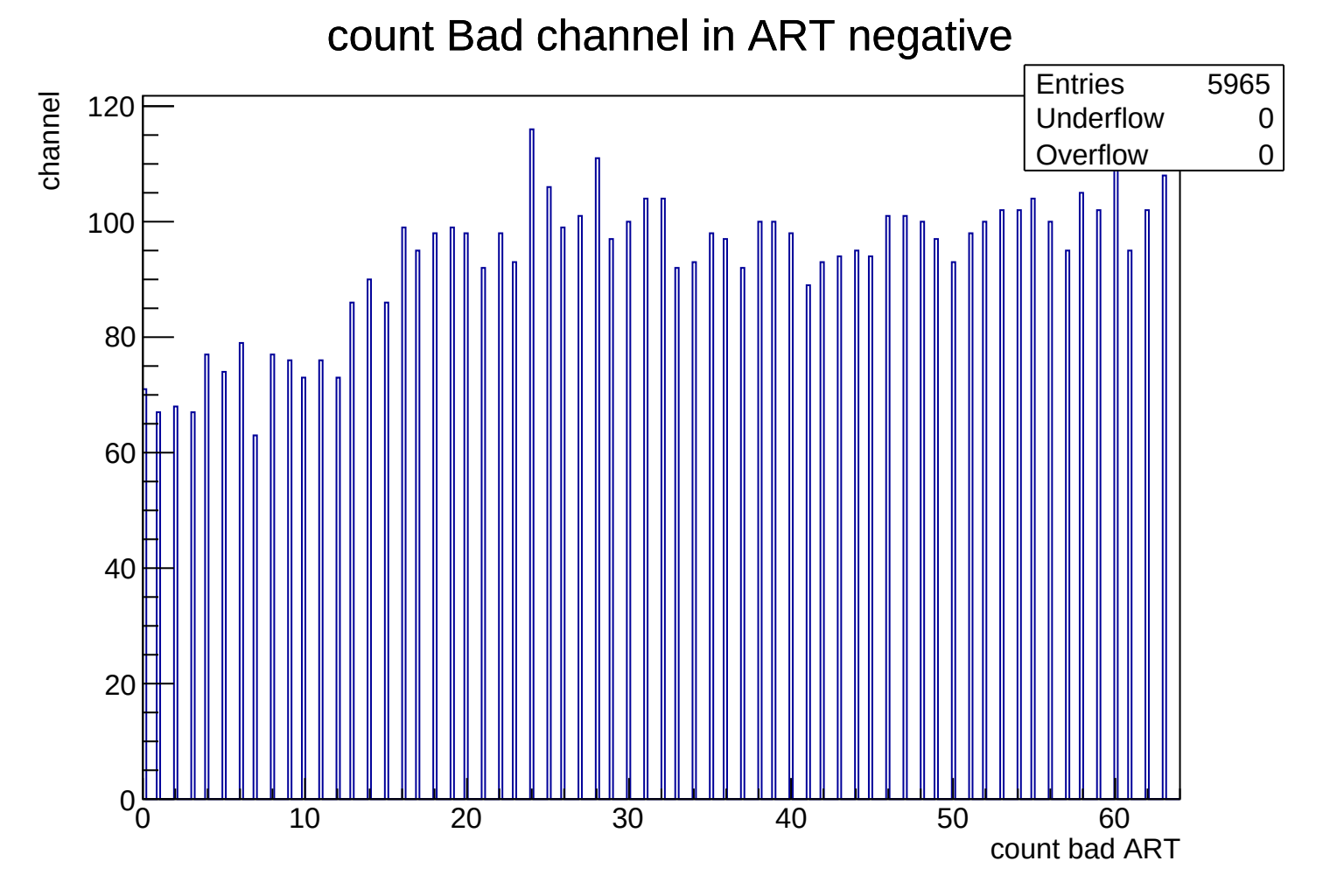

Sum current L0 negative
Entries 2173
Underflow 0
Overflow 5
count VMMId
10^2
10
1
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Current, A

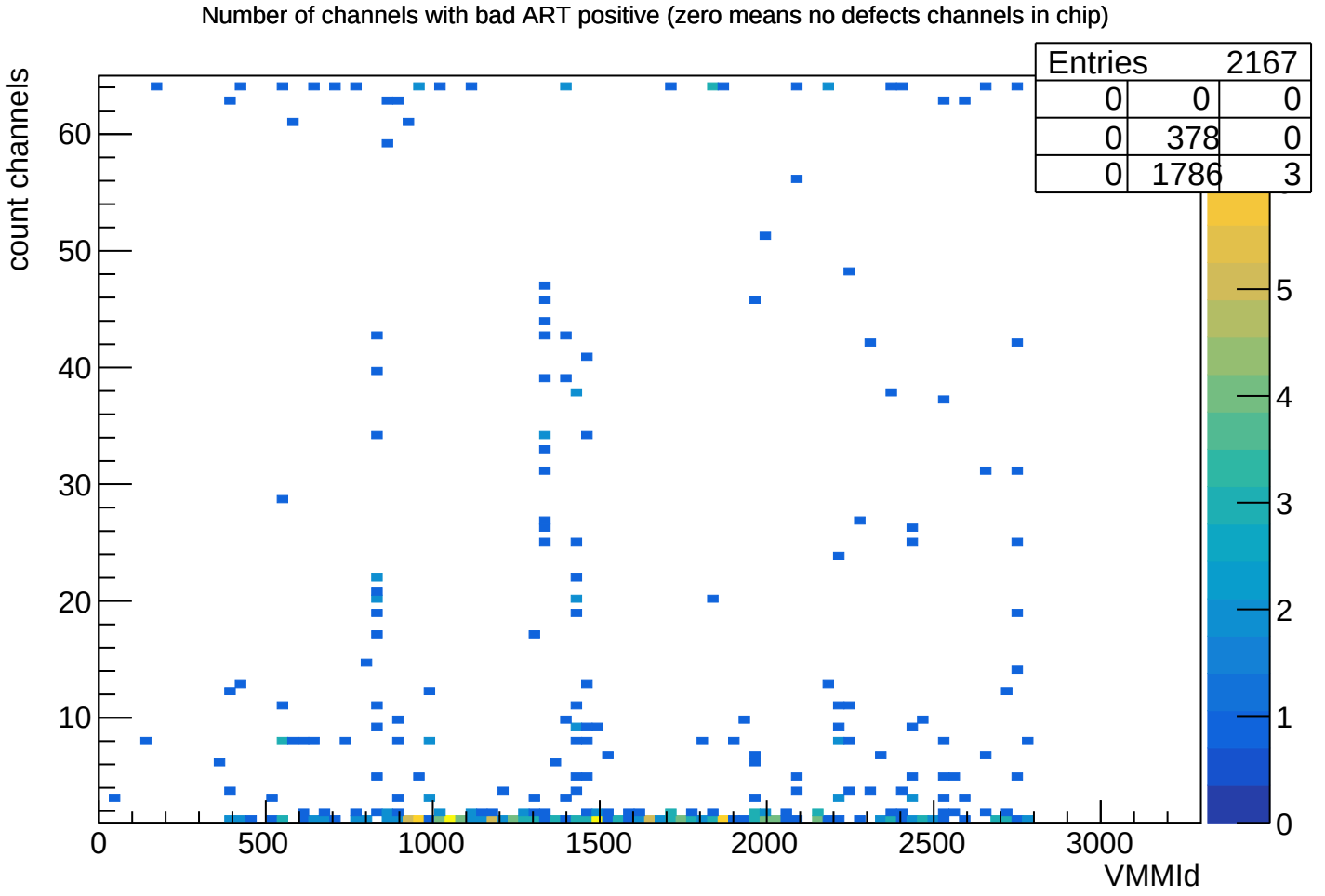

Sum current L0 positive
Entries 2167
Underflow 0
Overflow 5
count VMMId
10^2
10
1
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Current, A

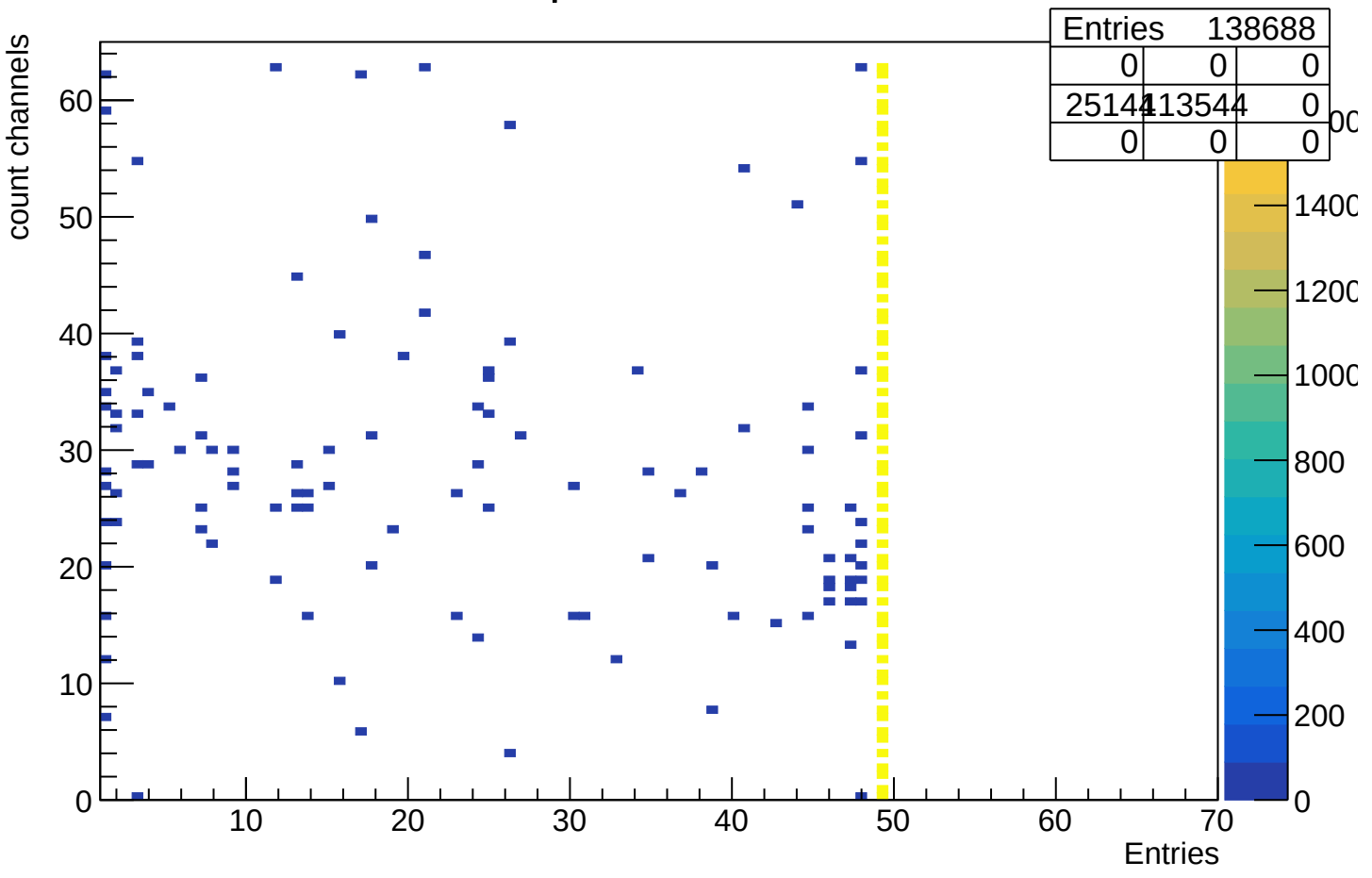

Number of channels with bad ART negative (zero means no defects channels in chip)
Entries 2173
0 0 0
0 493 2
0 1677 1
count channels
60
50
40
30
20
10
0
500
1000
1500
2000
2500
3000
VMMId
6
5
4
3
2
1
0

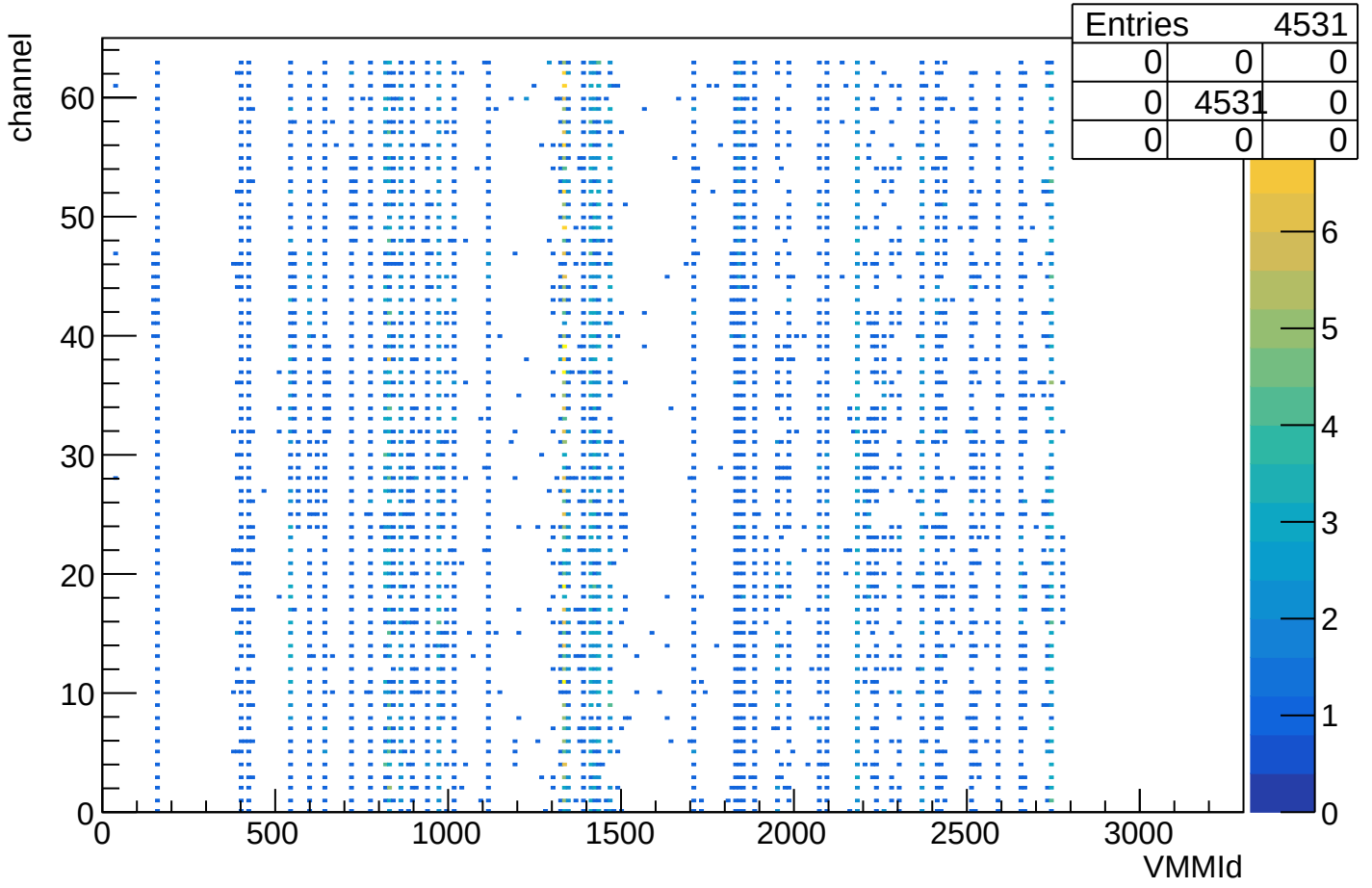

ART negative entries
Entries 139072
0 0 0
5224 133848 0
0 0 0
count channels
0
10
20
30
40
50
60
10
20
30
40
50
60
70
Entries
0
200
400
600
800
1000
1400
1600

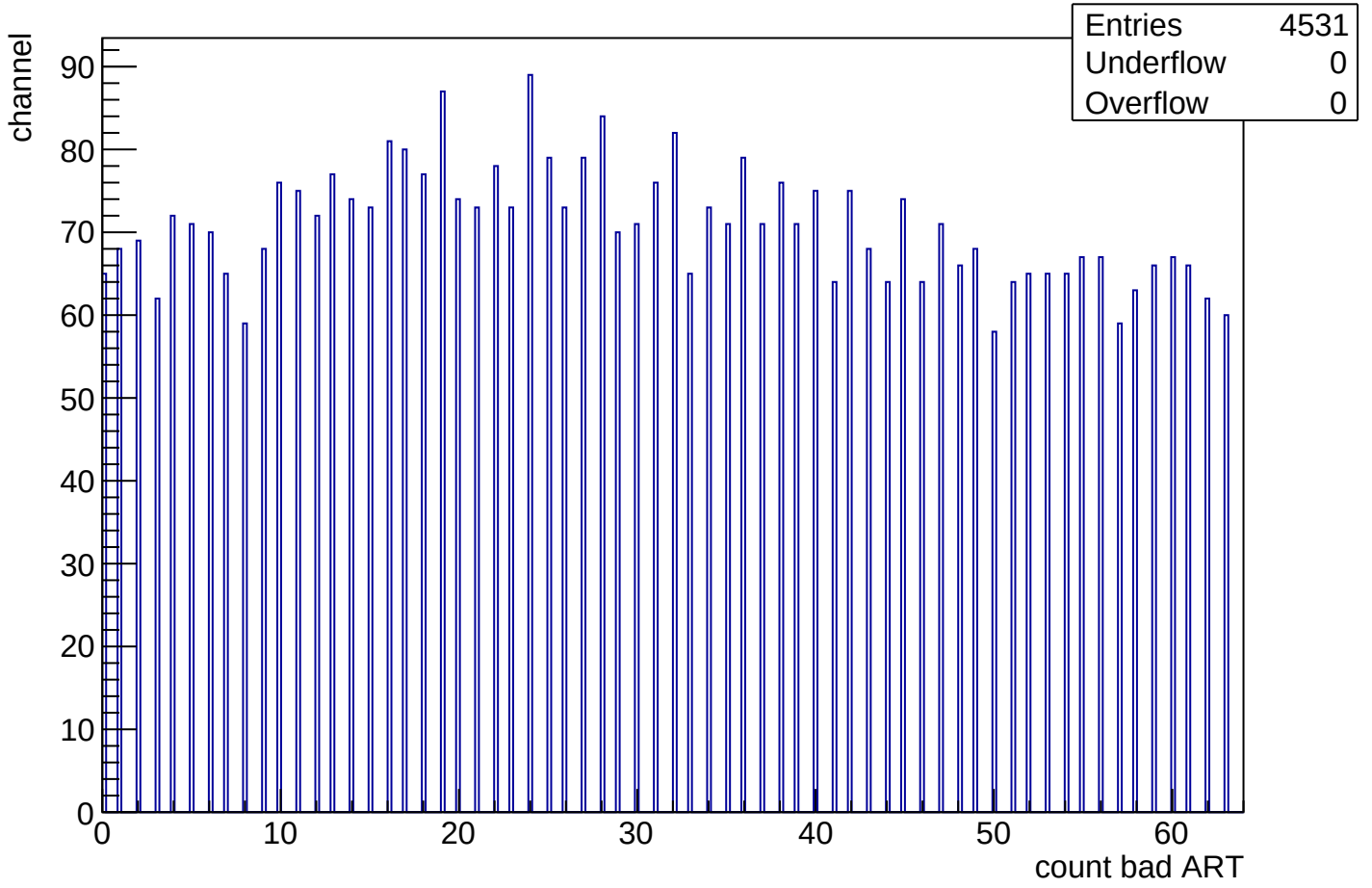

VMMId with bad ART negative (zero means no defects channels in chip)
Entries 5965
0 0 0
0 5959 6
0 0 0
channel
0
10
20
30
40
50
60
0
500
1000
1500
2000
2500
3000
VMMId
0
1
2
3
4
5
6
7

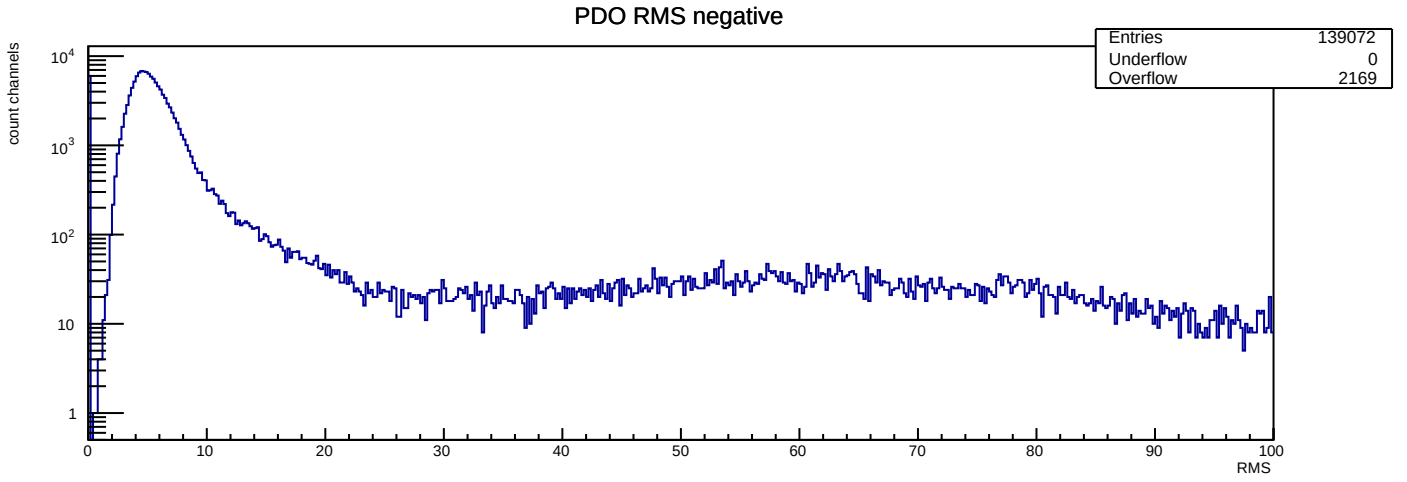

count Bad channel in ART negative
Entries 5965
Underflow 0
Overflow 0
channel
120
100
80
60
40
20
0
0
10
20
30
40
50
60
count bad ART

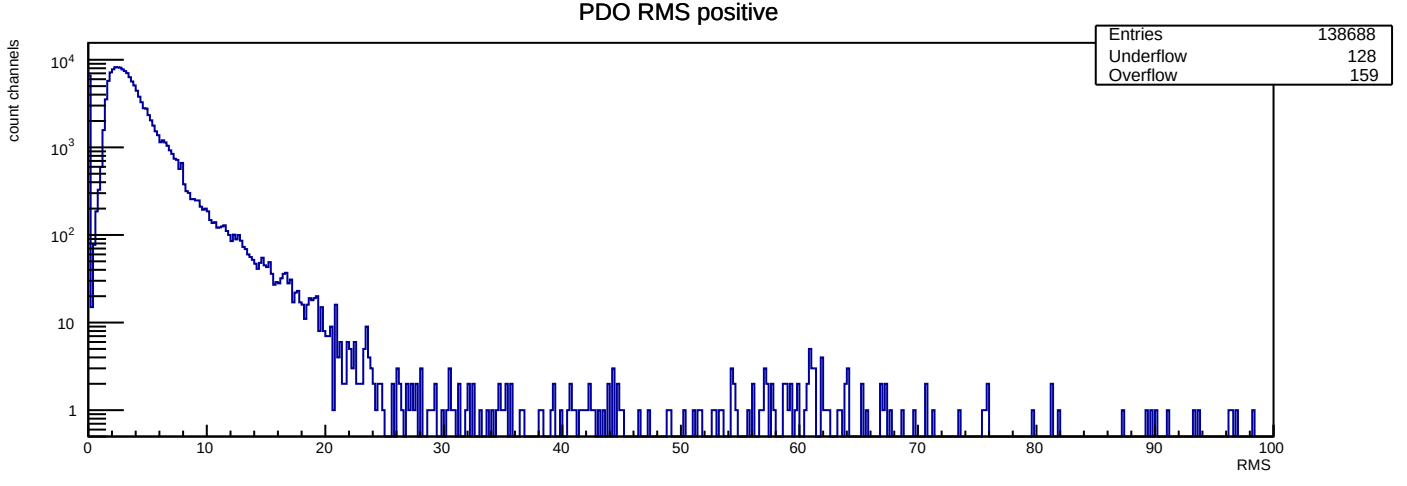

Number of channels with bad ART positive (zero means no defects channels in chip)
Entries 2167
0 0 0
0 378 0
0 1786 3
count channels
60
50
40
30
20
10
0
500
1000
1500
2000
2500
3000
VMMId
5
4
3
2
1
0

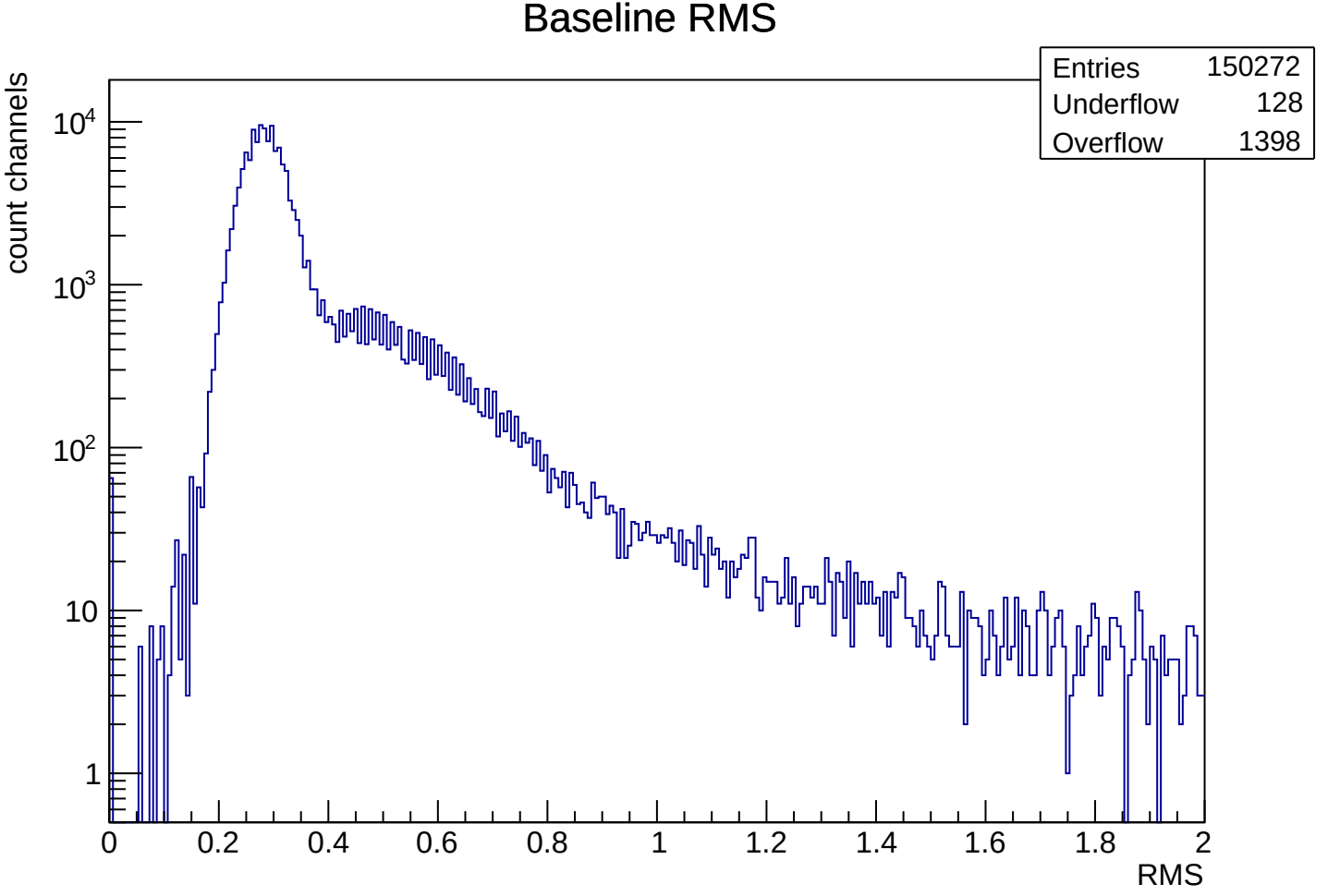

ART positive entries
Entries 138688
count channels
Entries
0
10
20
30
40
50
60
70
200
400
600
800
1000
1200
1400

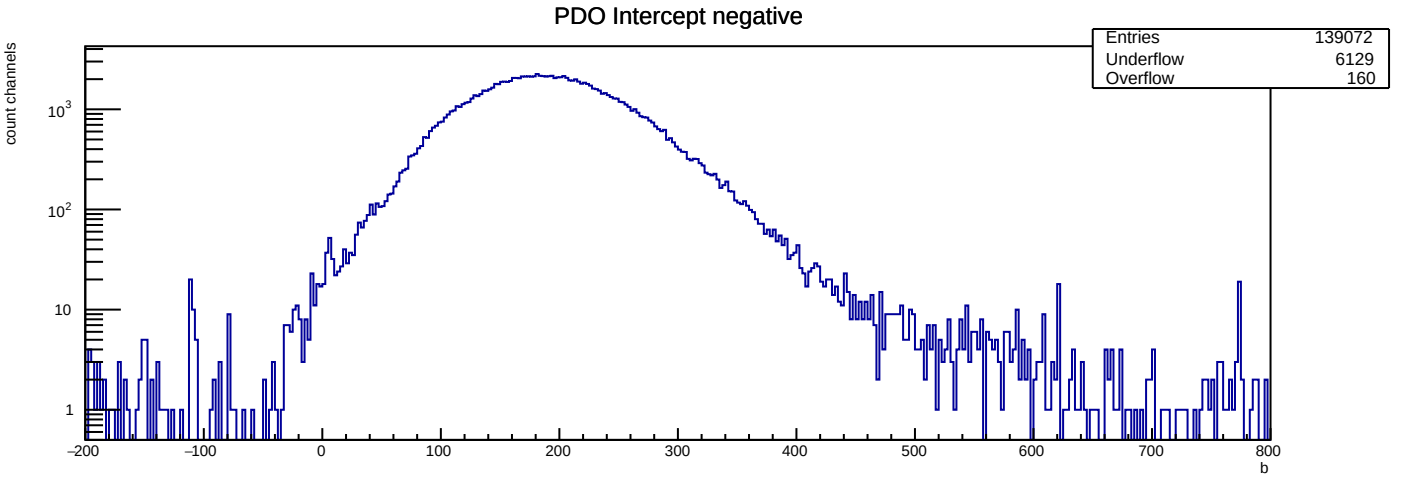

VMMId with bad ART positive (zero means no defects channels in chip)
Entries 4531
0 0 0
0 4531 0
0 0 0
channel
0
10
20
30
40
50
60
0
500
1000
1500
2000
2500
3000
VMMId
0
1
2
3
4
5
6

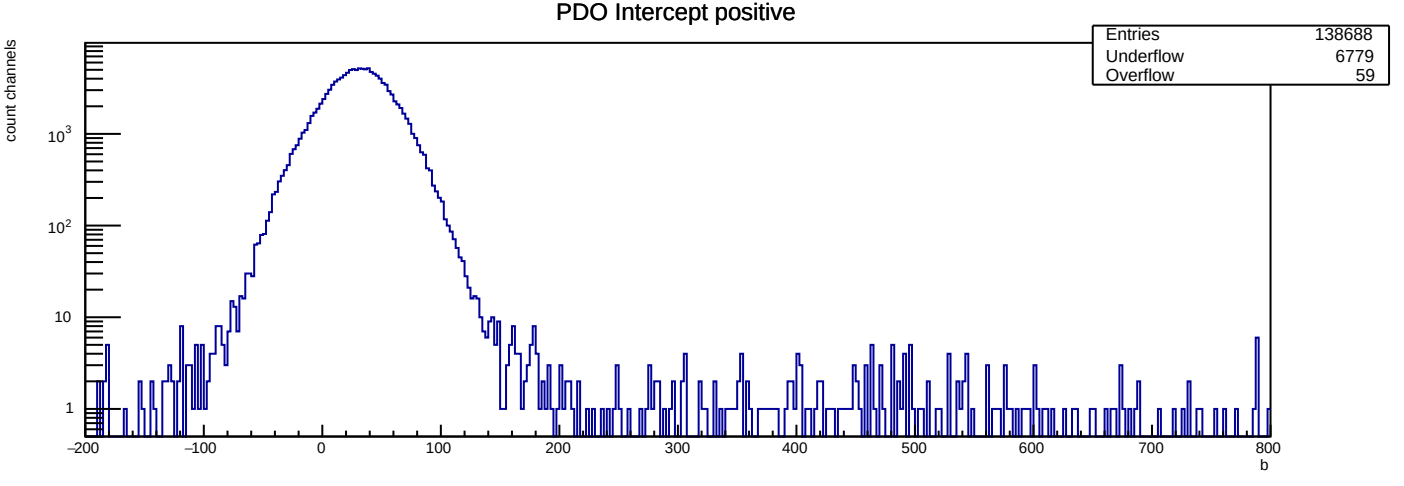

count Bad channel in ART positive
Entries 4531
Underflow 0
Overflow 0
channel
0
10
20
30
40
50
60
70
80
90
0
10
20
30
40
50
60
count bad ART

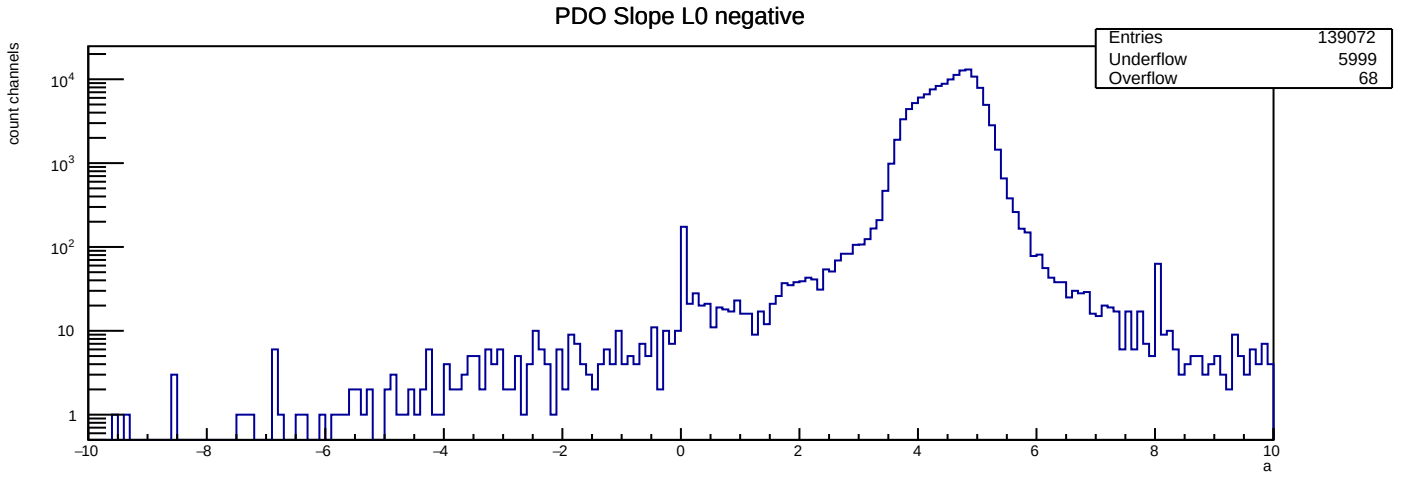

PDO RMS negative
Entries 139072
Underflow 0
Overflow 2169
count channels
RMS

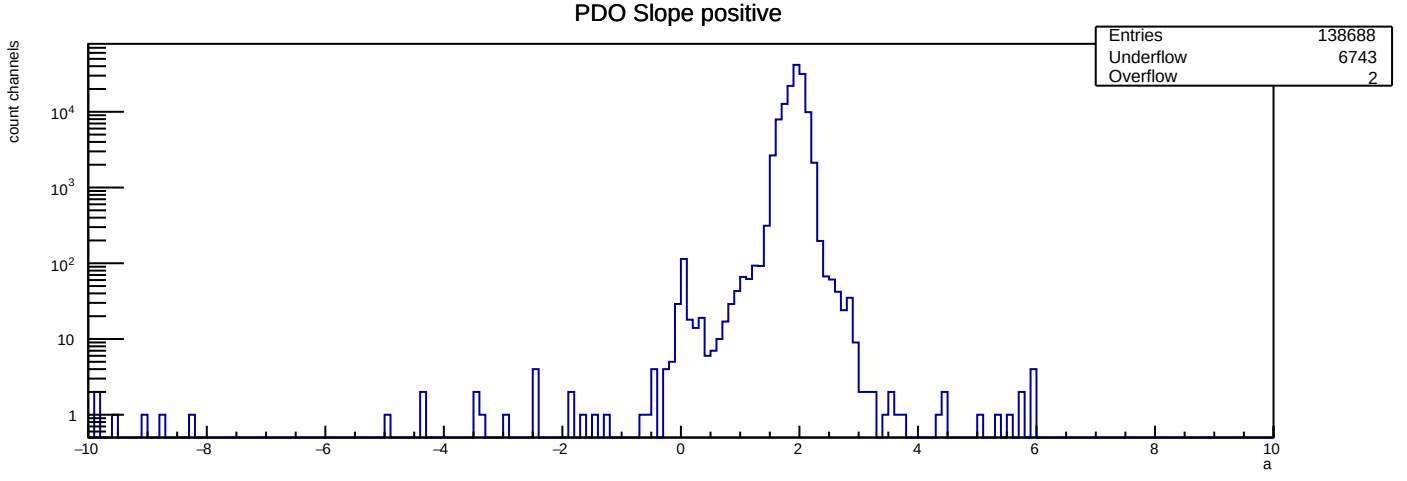

PDO RMS positive
Entries 138688
Underflow 128
Overflow 159
count channels
RMS

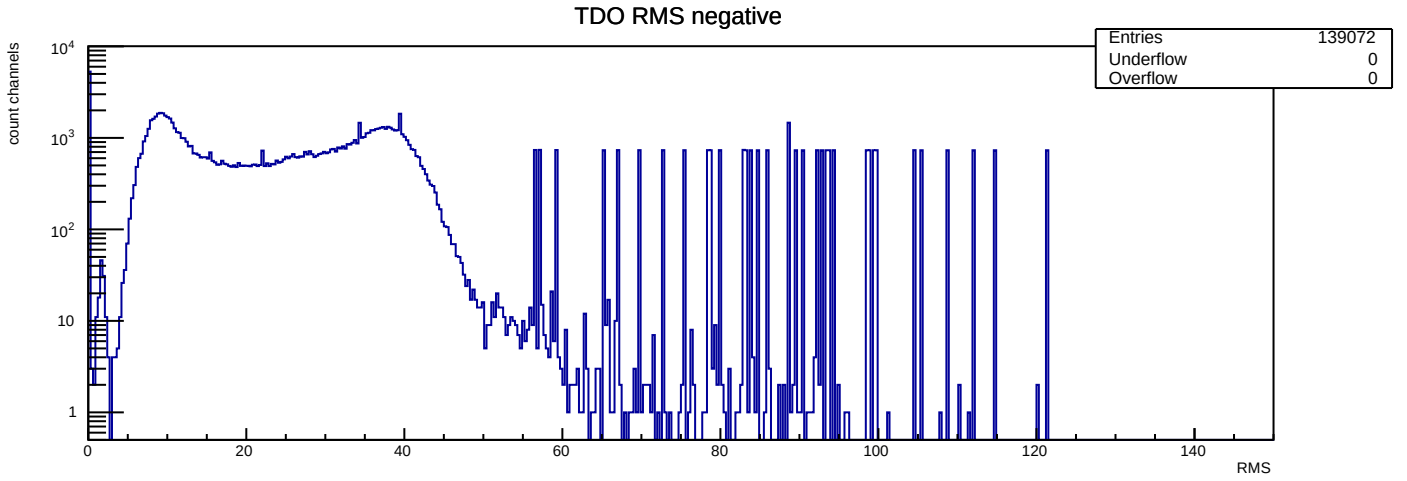

Baseline RMS
Entries 150272
Underflow 128
Overflow 1398
count channels
10^4
10^3
10^2
10
1
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
RMS

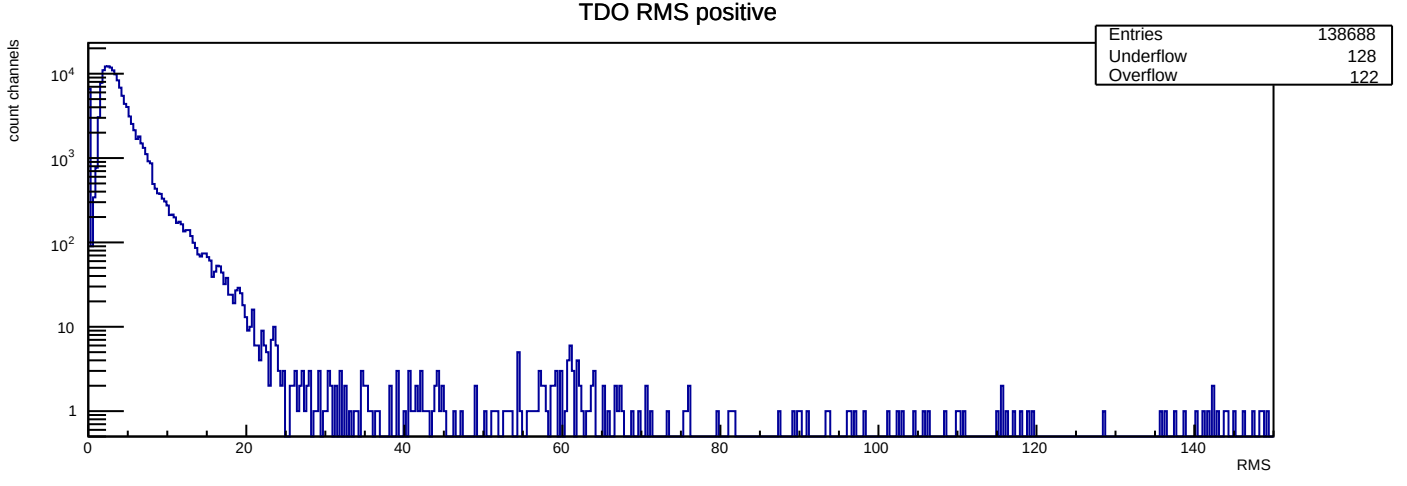

PDO Intercept negative
Entries 139072
Underflow 6129
Overflow 160
count channels
10^3
10^2
10
1
–200
–100
0
100
200
300
400
500
600
700
800
b

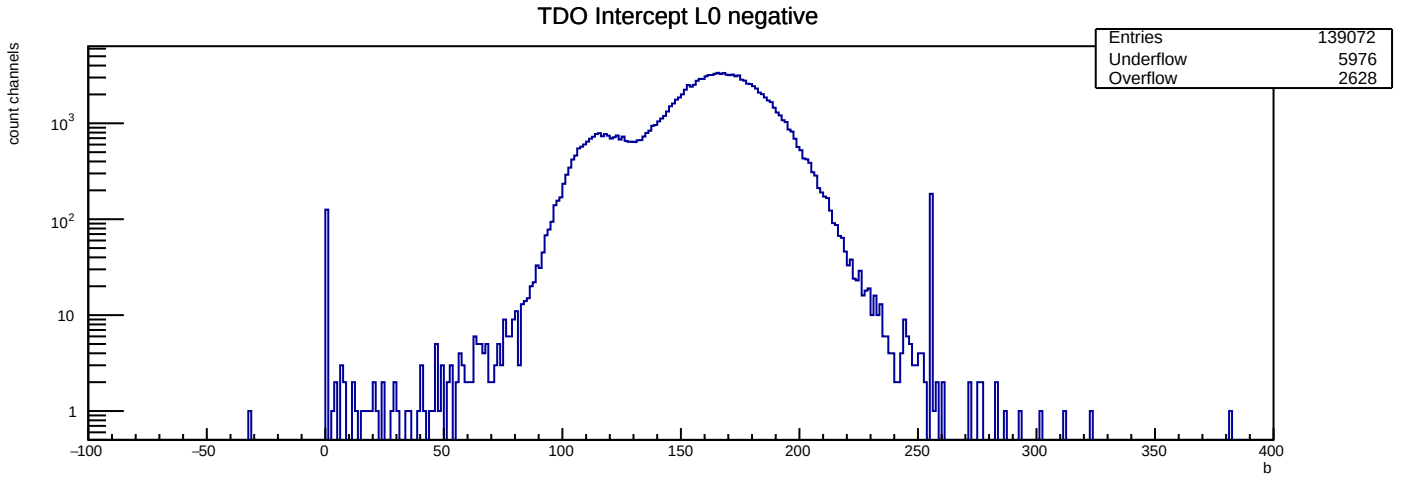

PDO Intercept positive
Entries 138688
Underflow 6779
Overflow 59
count channels
10^3
10^2
10
1
–200
–100
0
100
200
300
400
500
600
700
800
b

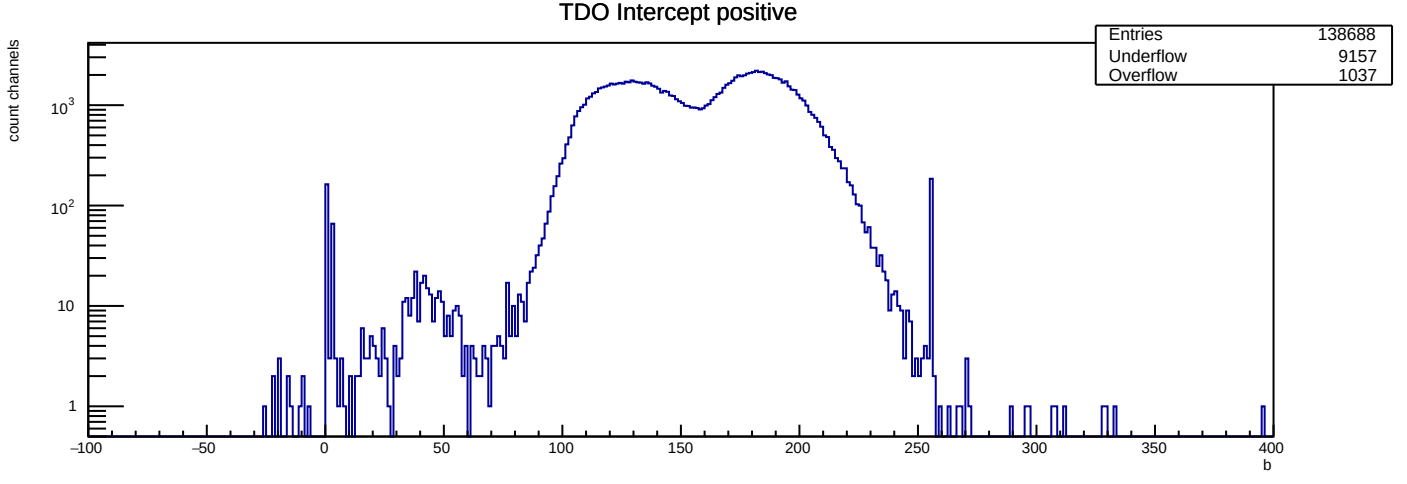

PDO Slope L0 negative
Entries 139072
Underflow 5999
Overflow 68
count channels
10^4
10^3
10^2
10
1
–10
–8
–6
–4
–2
0
2
4
6
8
10
a

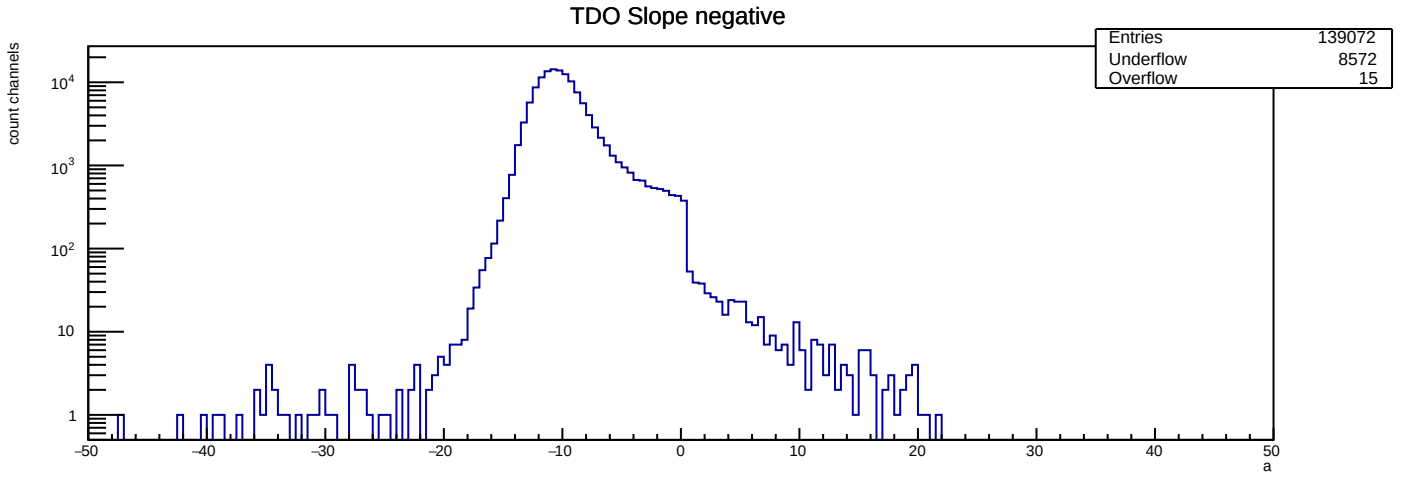

PDO Slope positive
Entries 138688
Underflow 6743
Overflow 2
count channels
10^4
10^3
10^2
10
1
–10
–8
–6
–4
–2
0
2
4
6
8
10
a

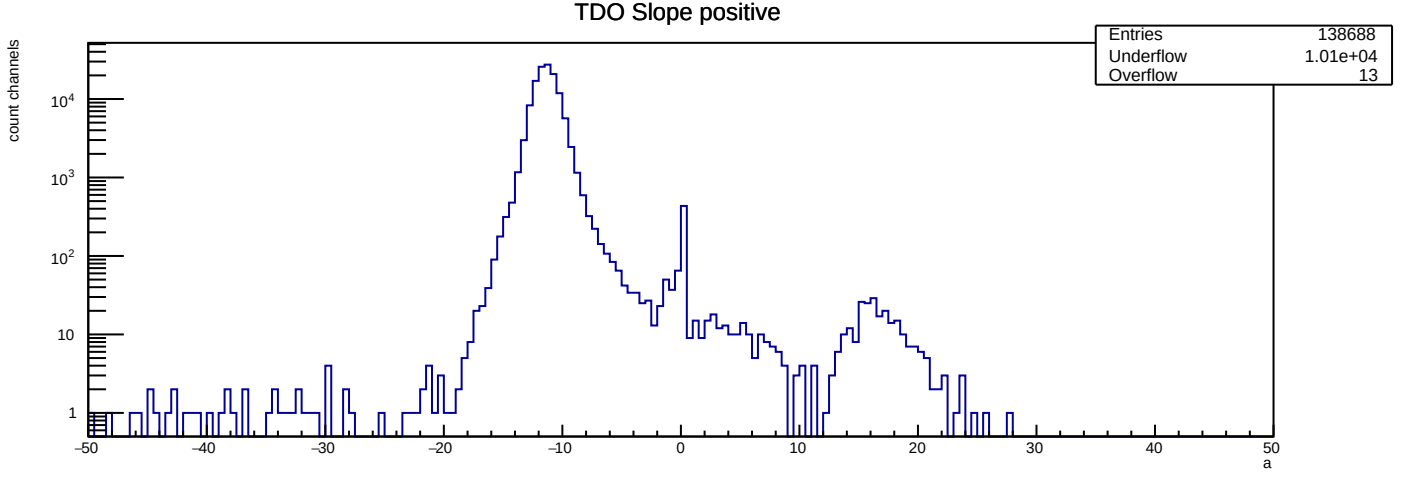

TDO RMS negative
Entries 139072
Underflow 0
Overflow 0
count channels
RMS


TDO RMS positive
Entries 138688
Underflow 128
Overflow 122
count channels
RMS


TDO Intercept L0 negative
Entries 139072
Underflow 5976
Overflow 2628
count channels
10^3
10^2
10
1
–100
–50
0
50
100
150
200
250
300
350
400
b


TDO Intercept positive
Entries 138688
Underflow 9157
Overflow 1037
count channels
10^3
10^2
10
1
–100
–50
0
50
100
150
200
250
300
350
400
b


TDO Slope negative
Entries 139072
Underflow 8572
Overflow 15
count channels
10^4
10^3
10^2
10
1
−50 −40 −30 −20 −10 0 10 20 30 40 50
a


TDO Slope positive
Entries 138688
Underflow 1.01e+04
Overflow 13
count channels
10^4
10^3
10^2
10
1
−50 −40 −30 −20 −10 0 10 20 30 40 50
a