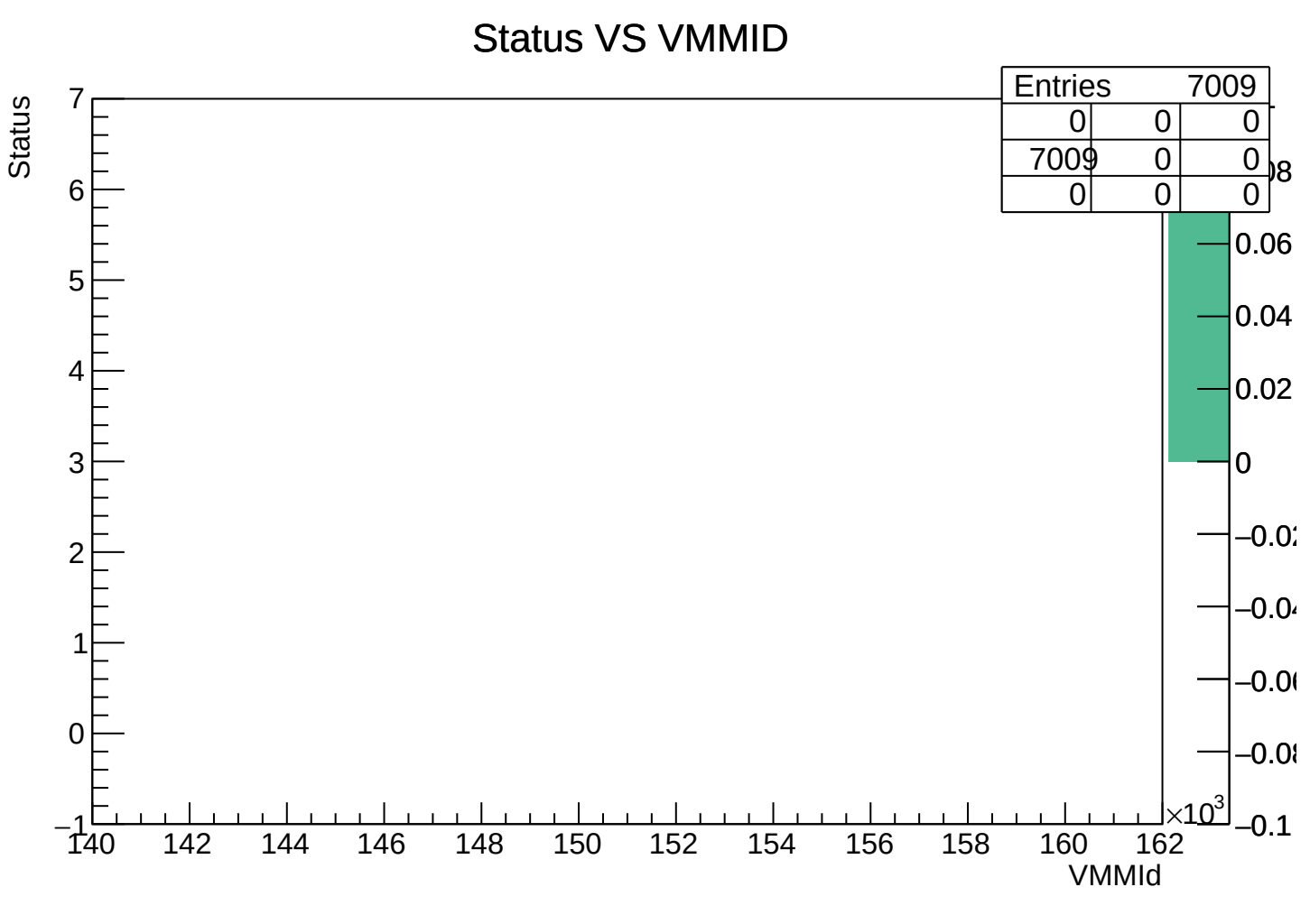
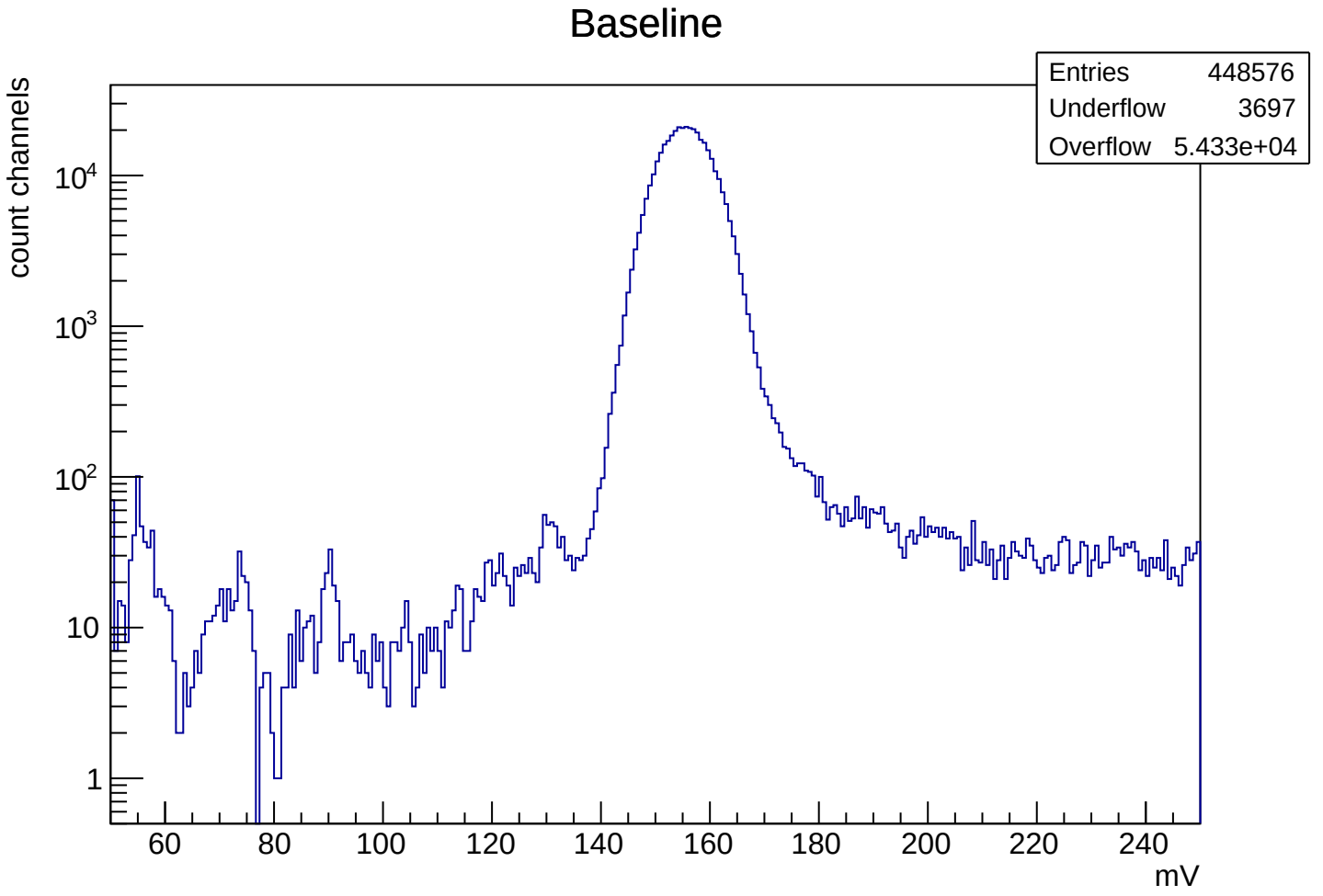
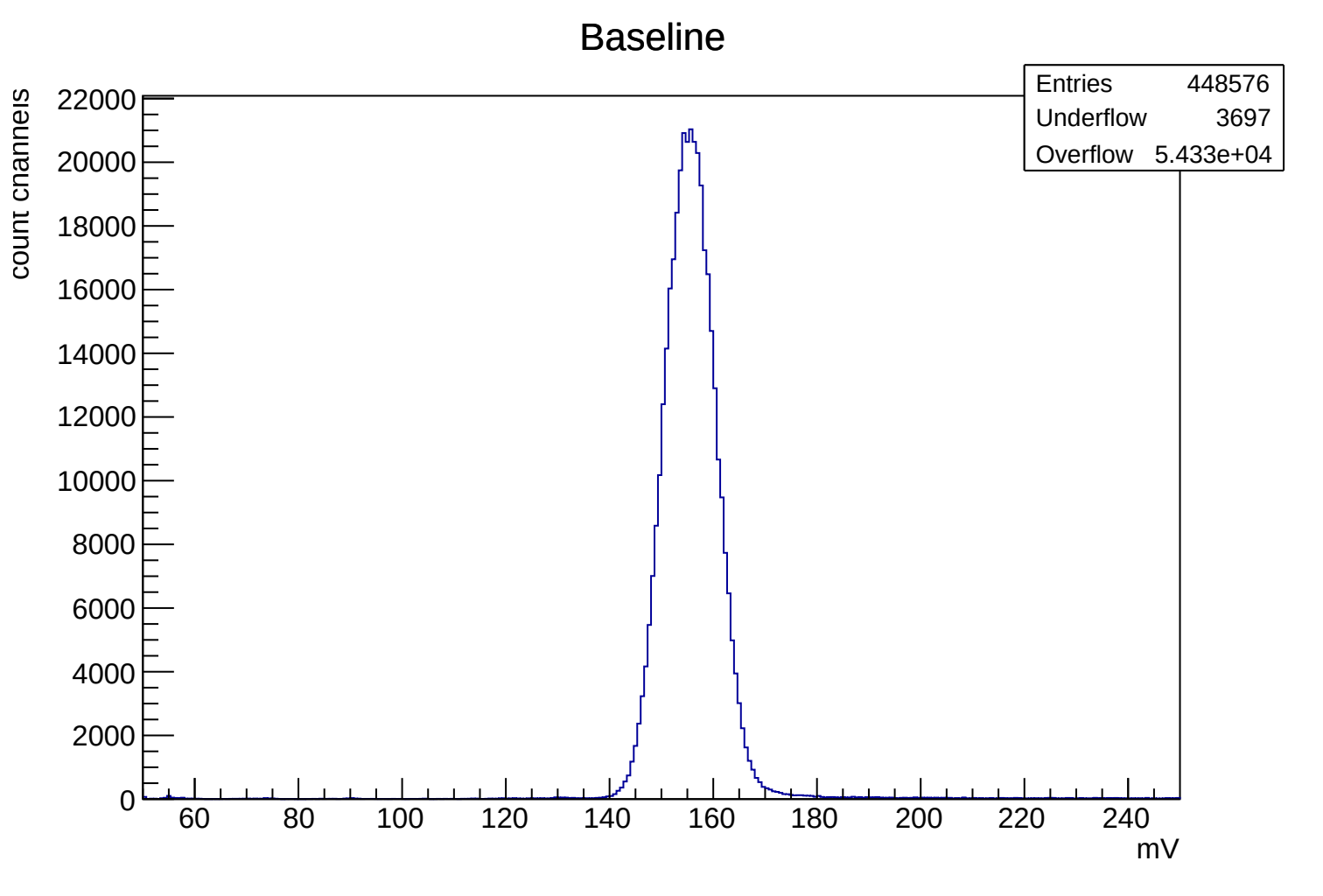
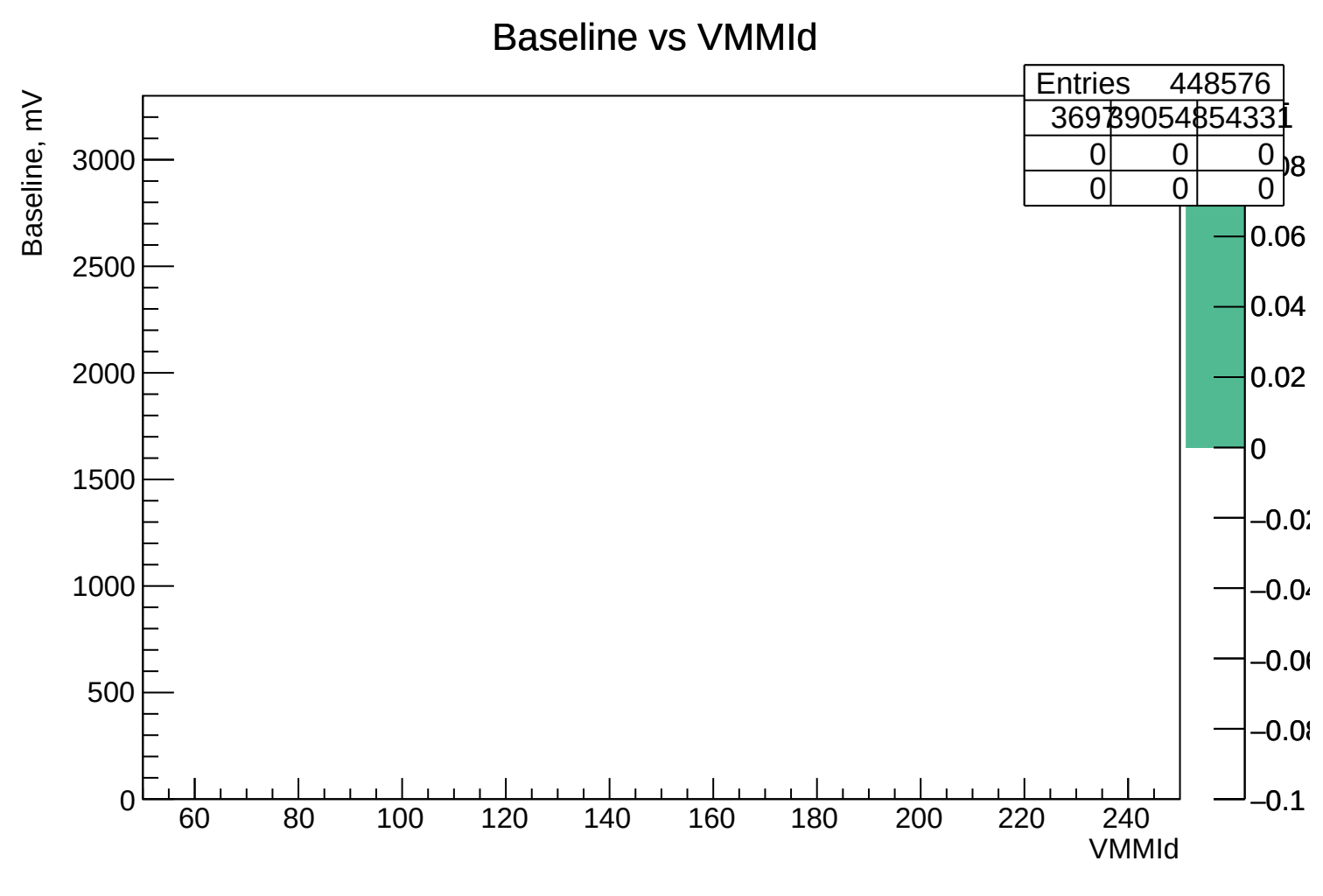
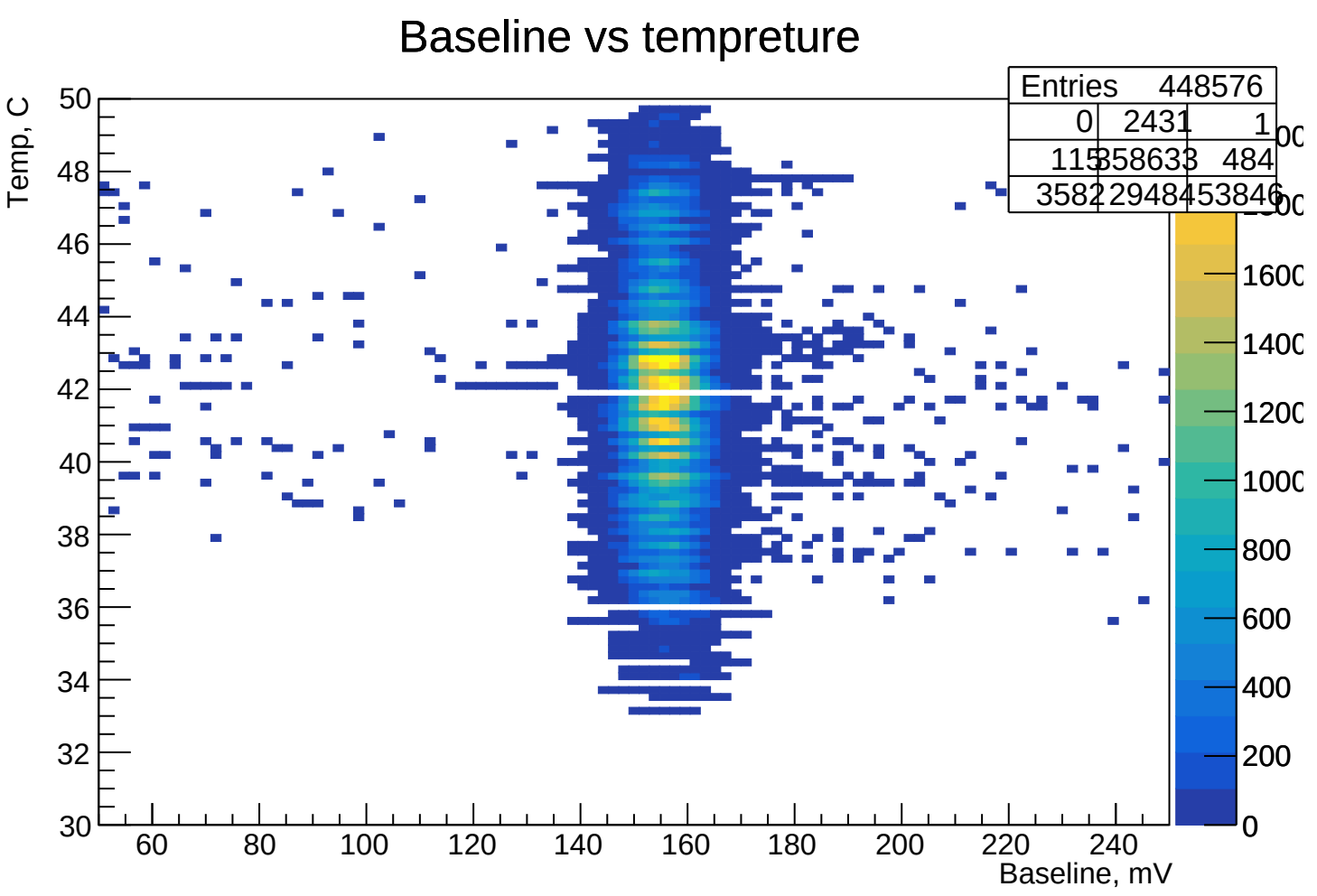
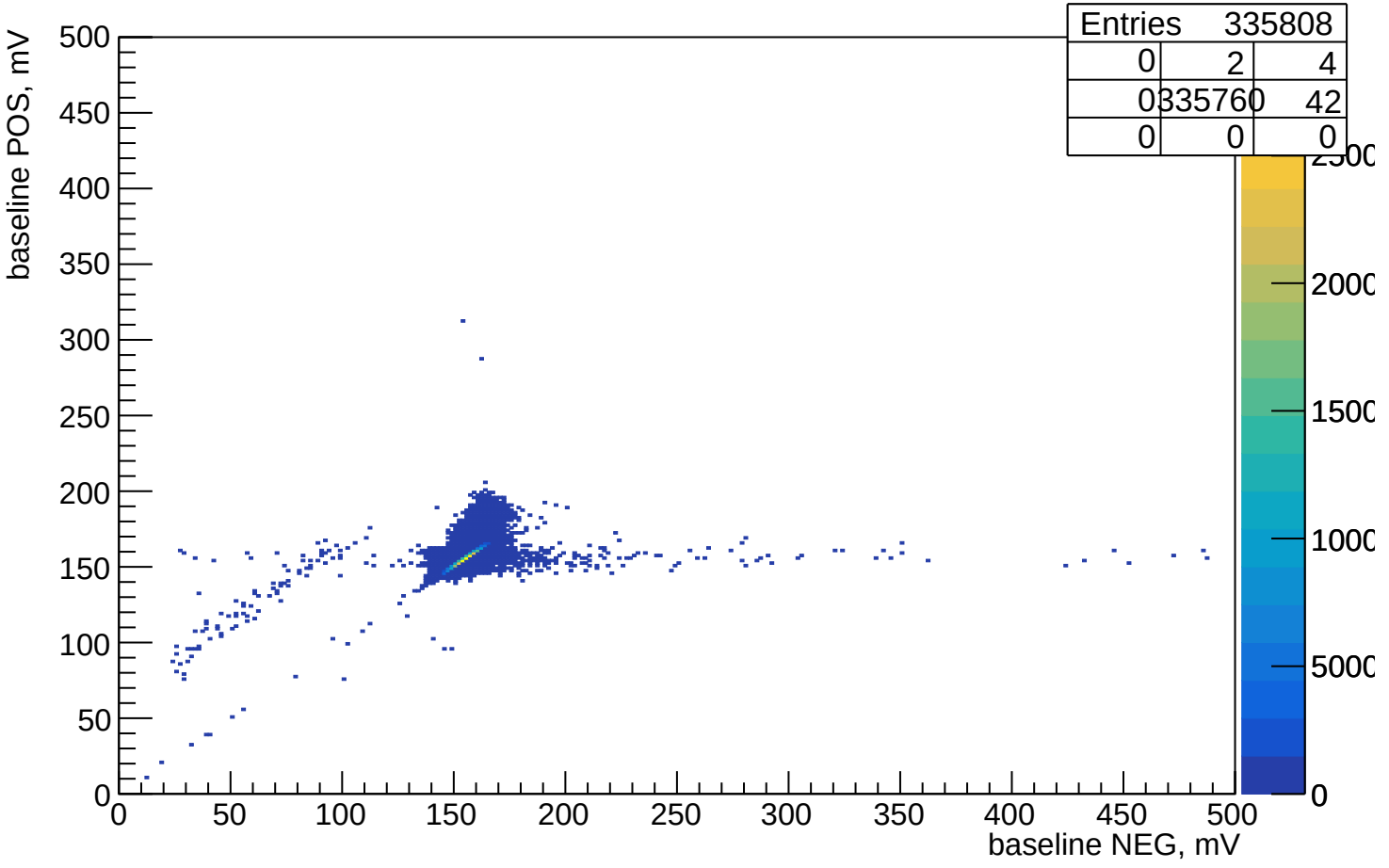

Status VS VMMID
Entries 7009
0 0 0
7009 0 0
0 0 0
Status
VMMId
×10^3
7
6
5
4
3
2
1
0
−1
140
142
144
146
148
150
152
154
156
158
160
162
0.06
0.04
0.02
0
−0.1

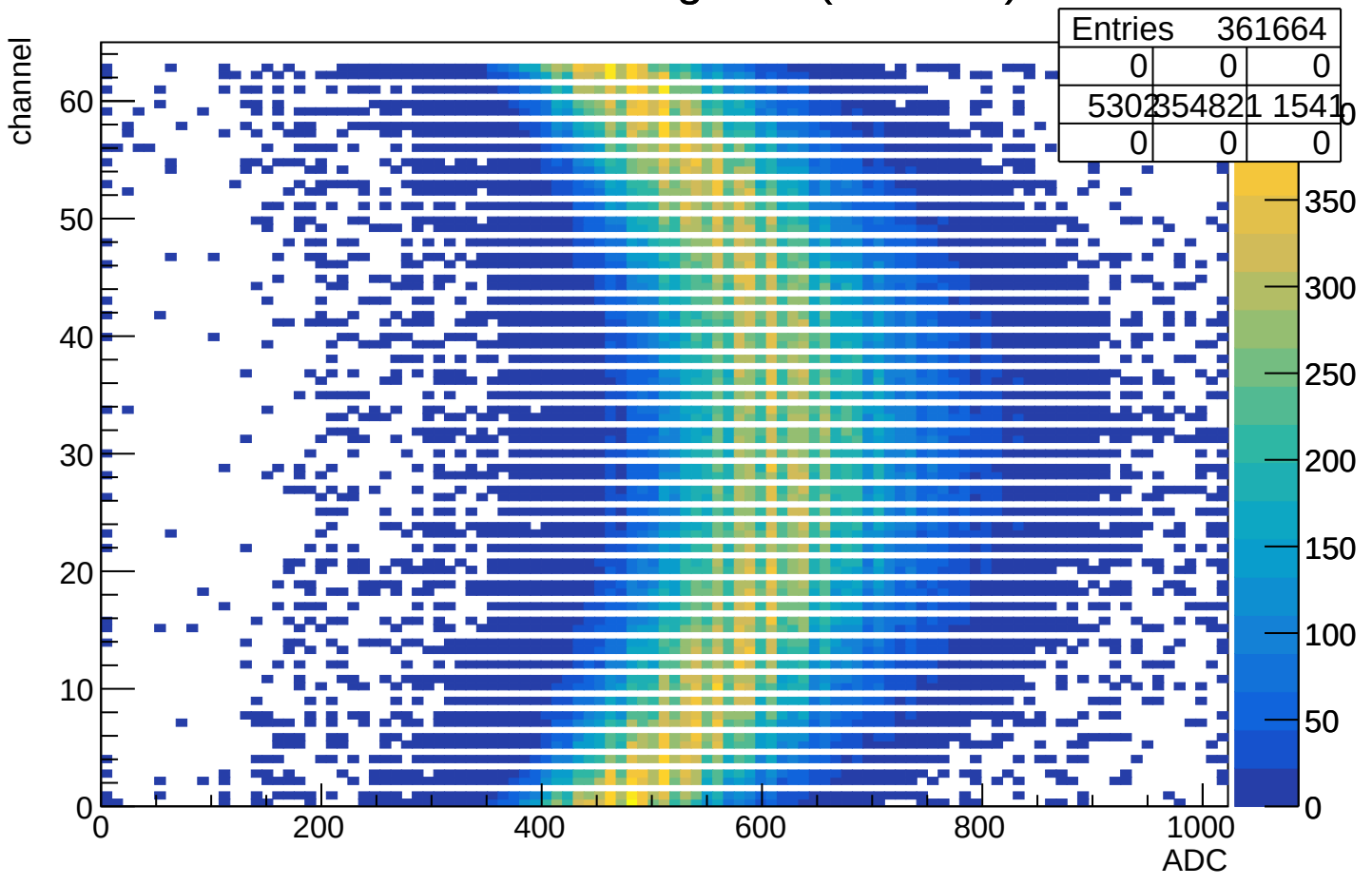

Baseline
Entries 448576
Underflow 3697
Overflow 5.433e+04
count channels
10^4
10^3
10^2
10
1
60
80
100
120
140
160
180
200
220
240
mV

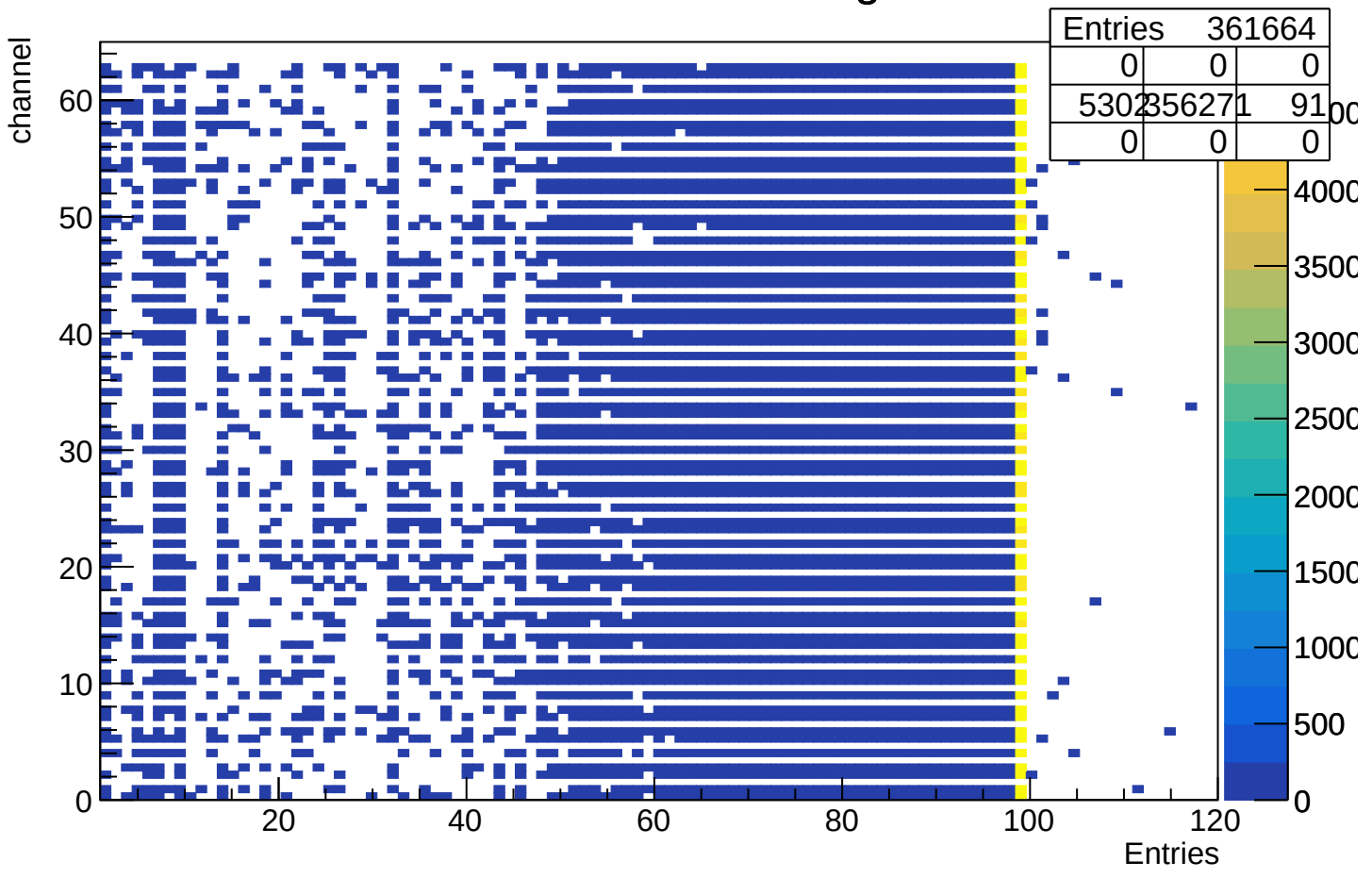

Baseline
Entries 448576
Underflow 3697
Overflow 5.433e+04
count channels
22000
20000
18000
16000
14000
12000
10000
8000
6000
4000
2000
0
60
80
100
120
140
160
180
200
220
240
mV

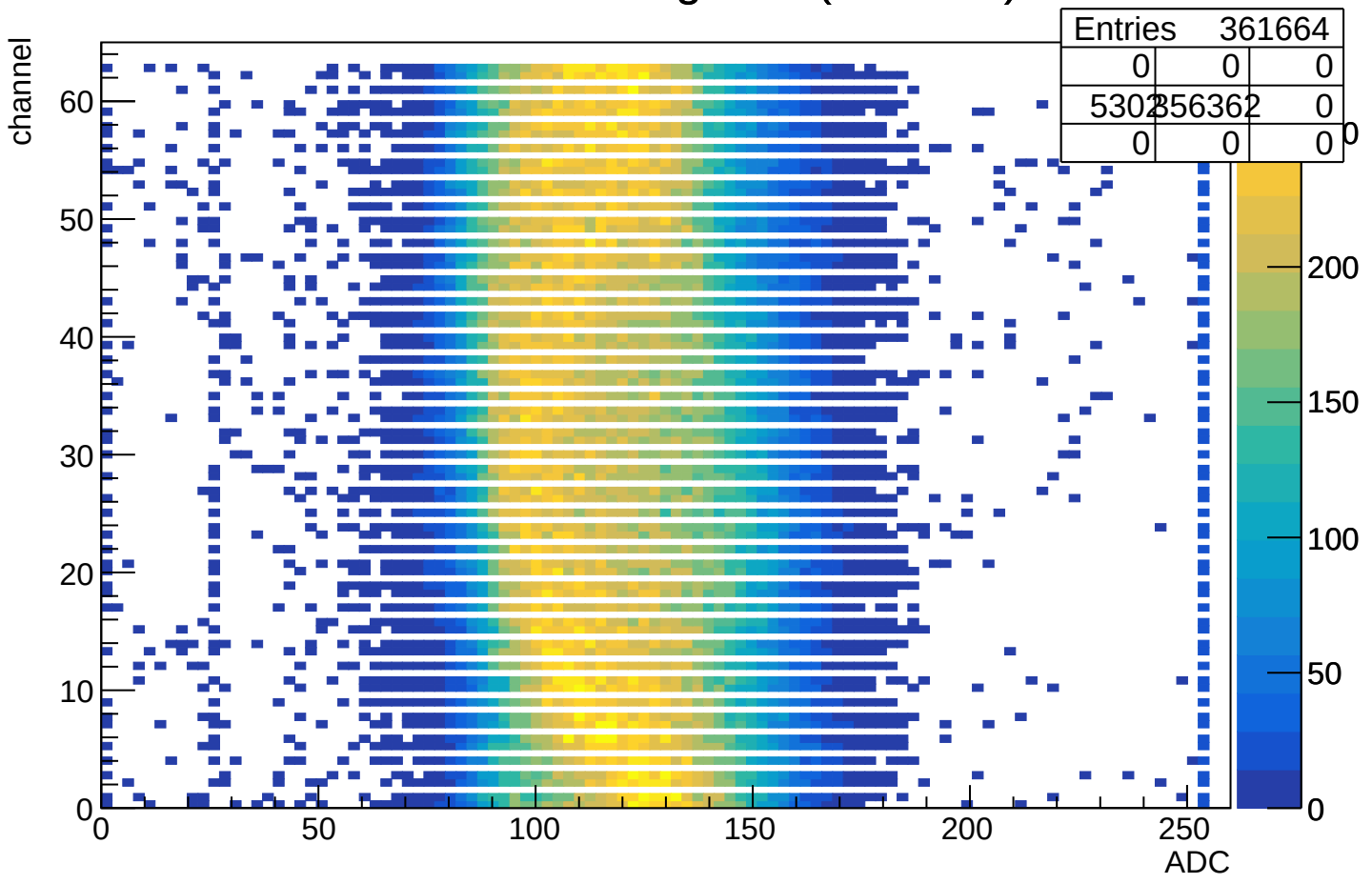

Baseline vs VMMId
Entries 448576
Baseline, mV
3000
2500
2000
1500
1000
500
0
60
80
100
120
140
160
180
200
220
240
VMMId
0.06
0.04
0.02
0
–0.1

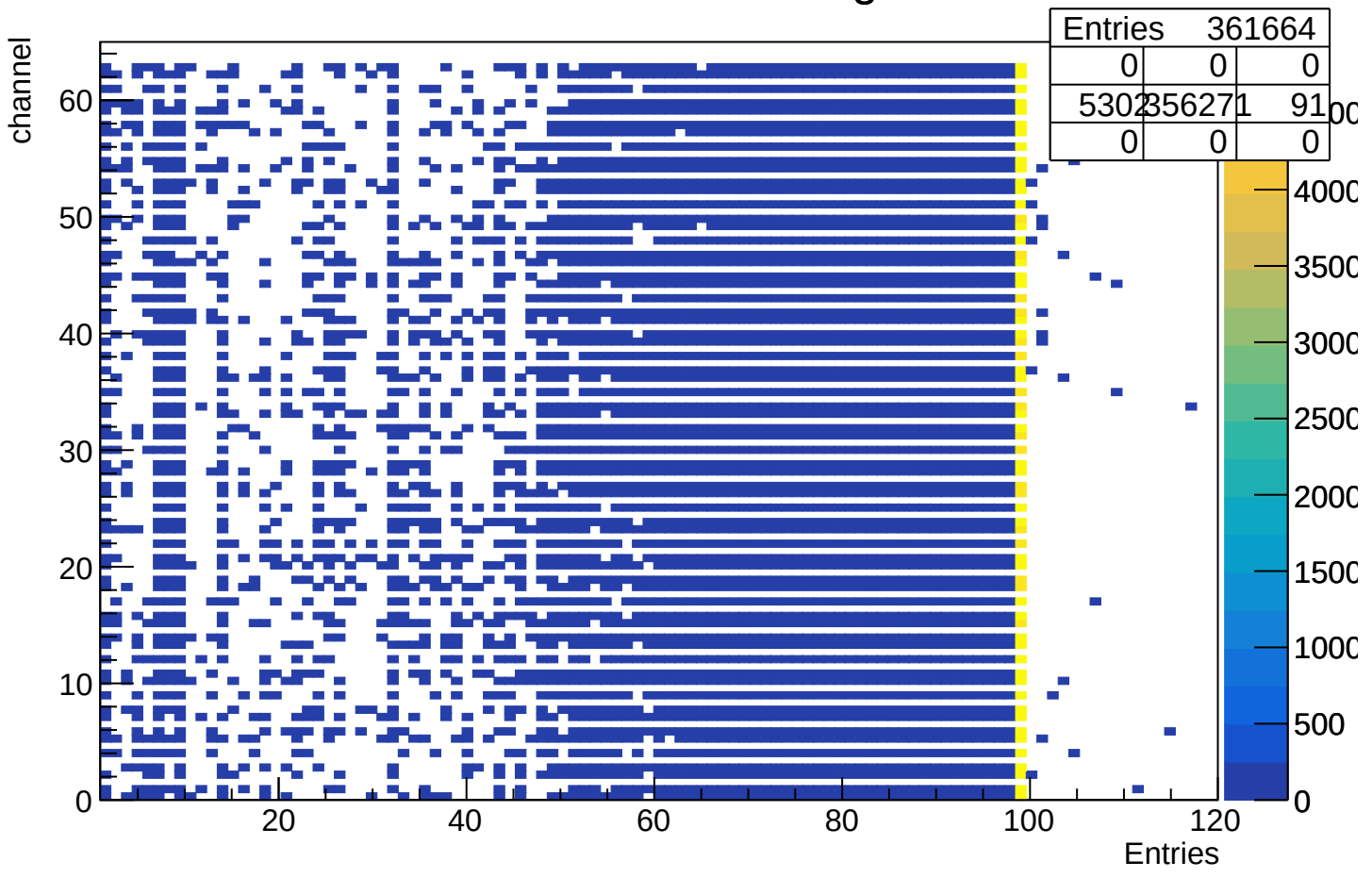

Baseline vs tempreture
Entries 448576
0 2431 1
115 358633 484
3582 29484 53846
Temp, C
50
48
46
44
42
40
38
36
34
32
30
60
80
100
120
140
160
180
200
220
240
Baseline, mV
1600
1400
1200
1000
800
600
400
200
0

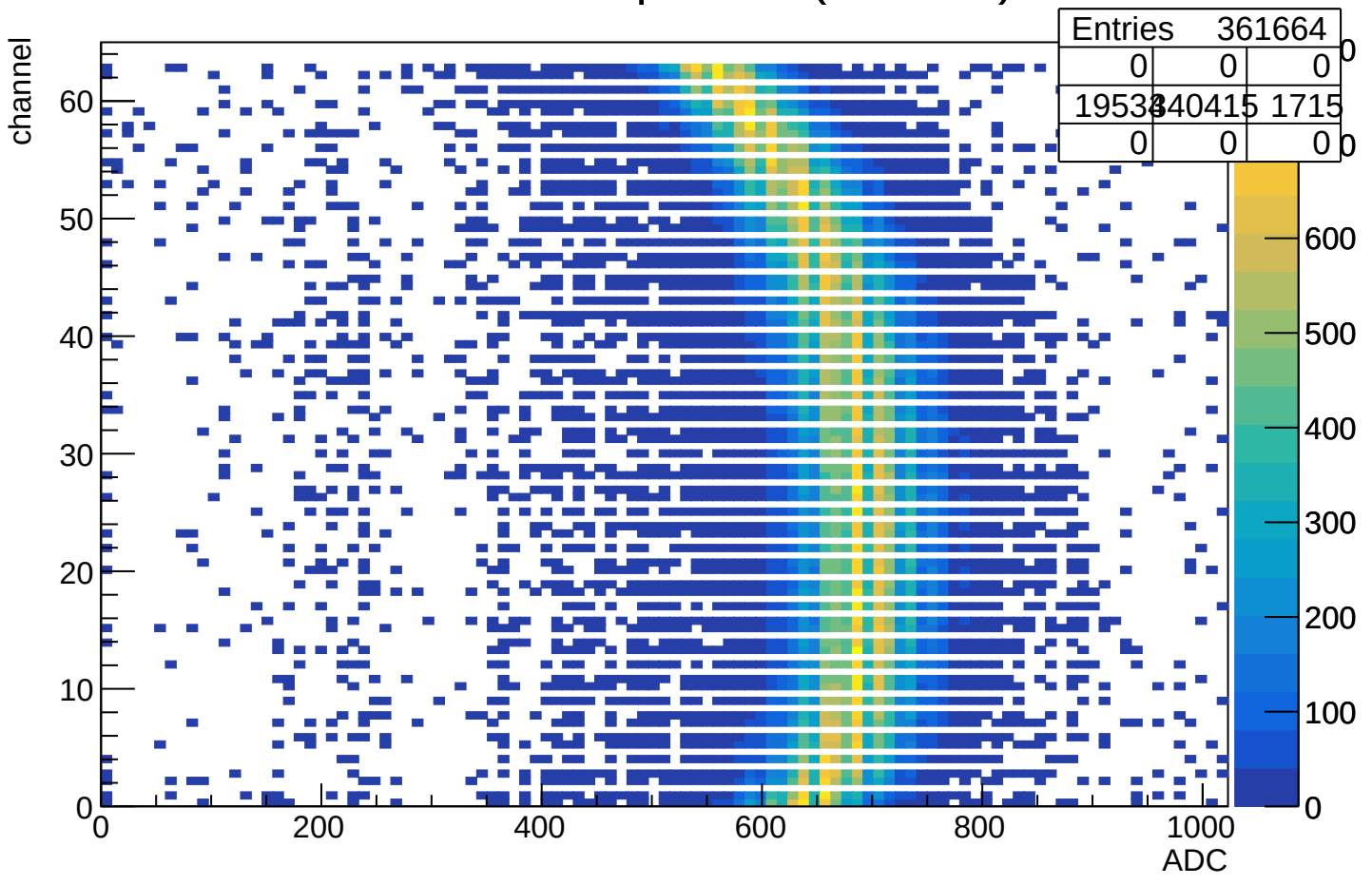

Bline pos (delay 2 ms) vs Bline neg (delay 0 ms) - not failed
Entries 335808
0 2 4
0 335760 42
0 0 0
baseline POS, mV
baseline NEG, mV
0
50
100
150
200
250
300
350
400
450
500
2000
1500
1000
5000

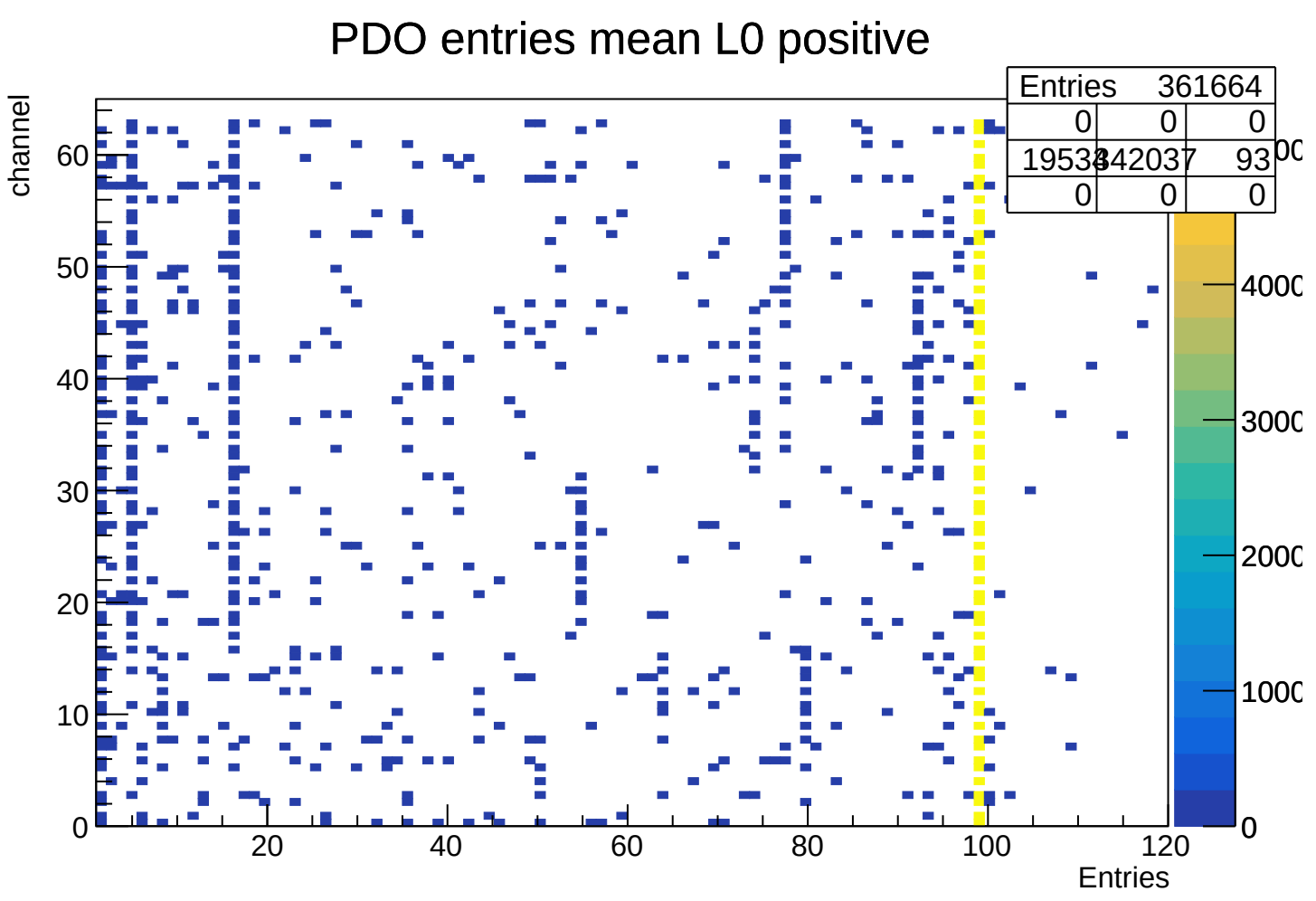

PDO mean L0 negative (all VMM)
Entries 361664
0 0 0
5302 354821 1541
0 0 0
channel
0
10
20
30
40
50
60
0
200
400
600
800
1000
ADC
0
50
100
150
200
250
300
350

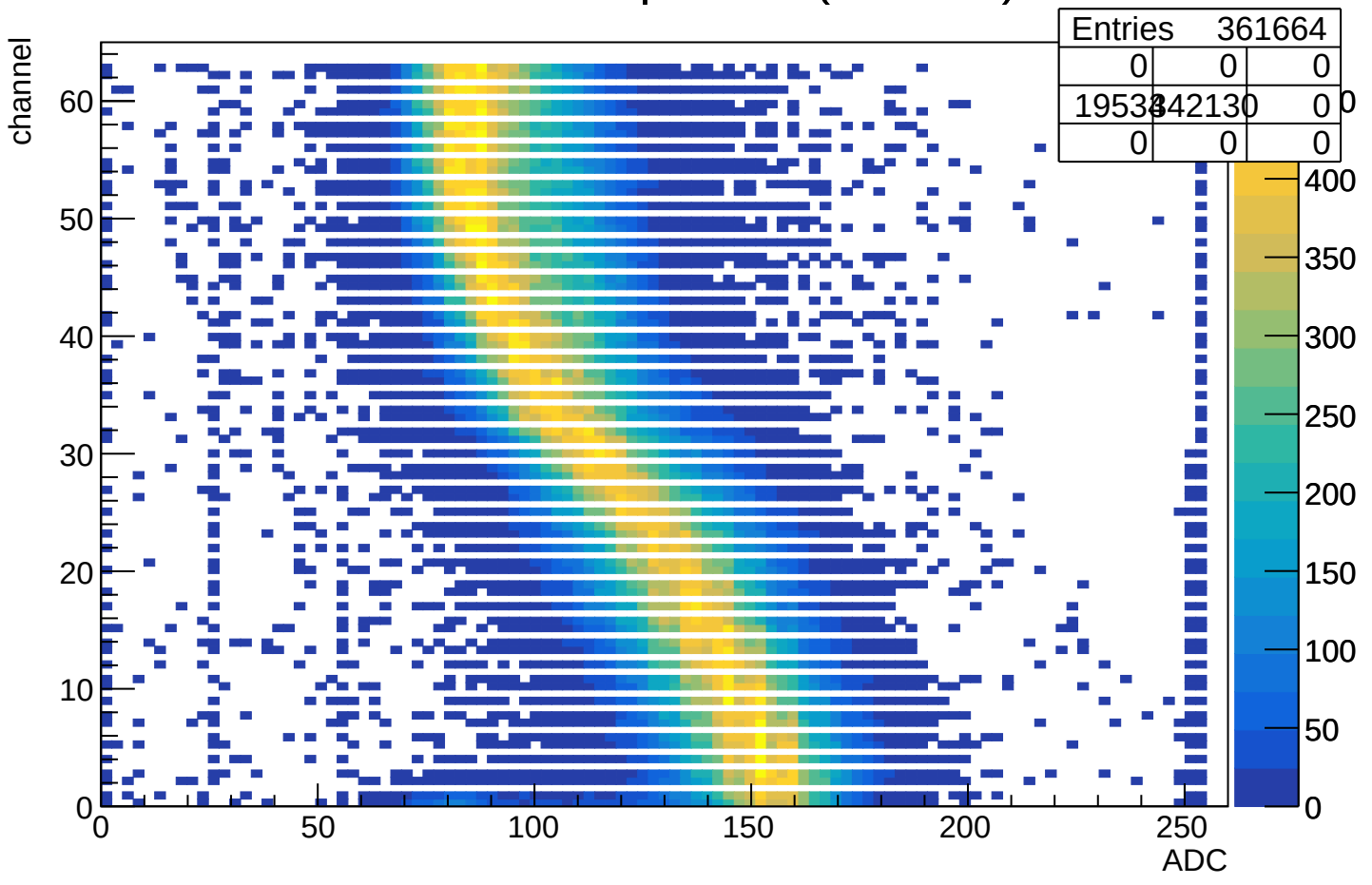

PDO entries mean L0 negative
Entries 361664
0 0 0
5302356271 91
0 0 0
channel
0
10
20
30
40
50
60
20
40
60
80
100
120
Entries
4000
3500
3000
2500
2000
1500
1000
500
0

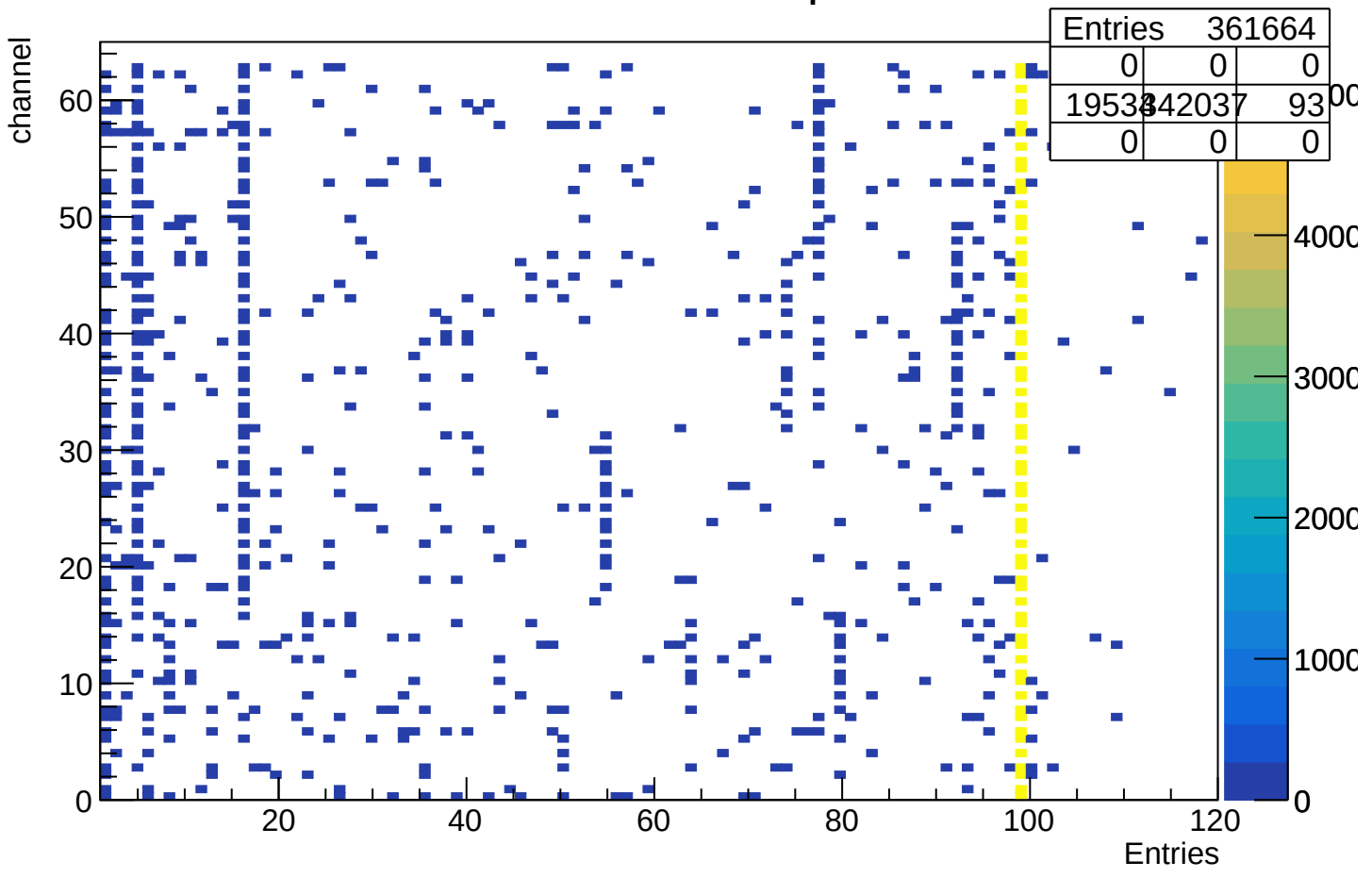

TDO mean L0 negative (all VMM)
Entries 361664
0 0 0
5302356362 0
0 0 0
channel
0
10
20
30
40
50
60
0
50
100
150
200
250
ADC
0
50
100
150
200

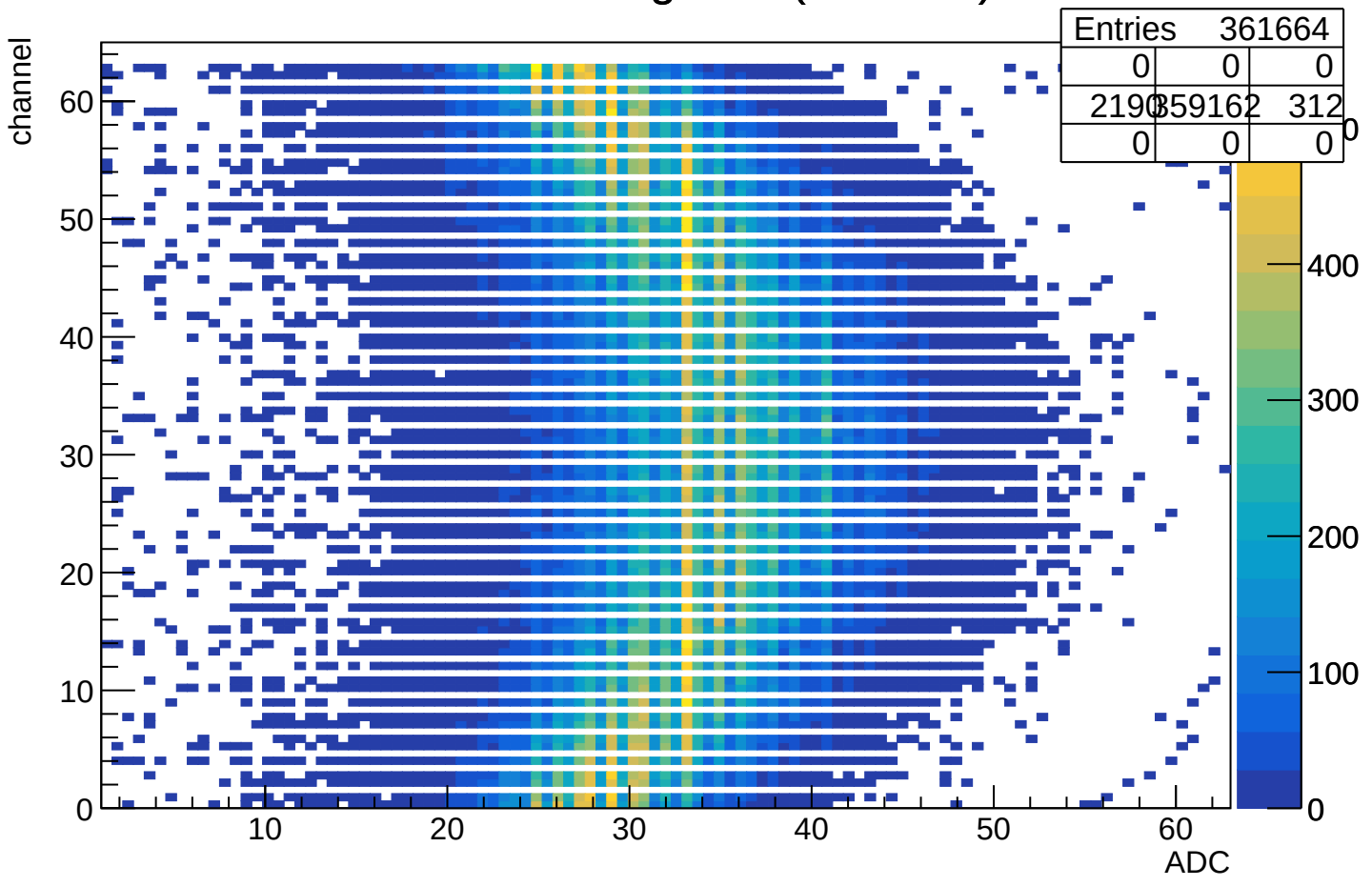

TDO entries mean L0 negative
Entries 361664
0 0 0
5302356271 91
0 0 0
channel
0
10
20
30
40
50
60
20
40
60
80
100
120
Entries
4000
3500
3000
2500
2000
1500
1000
500
0

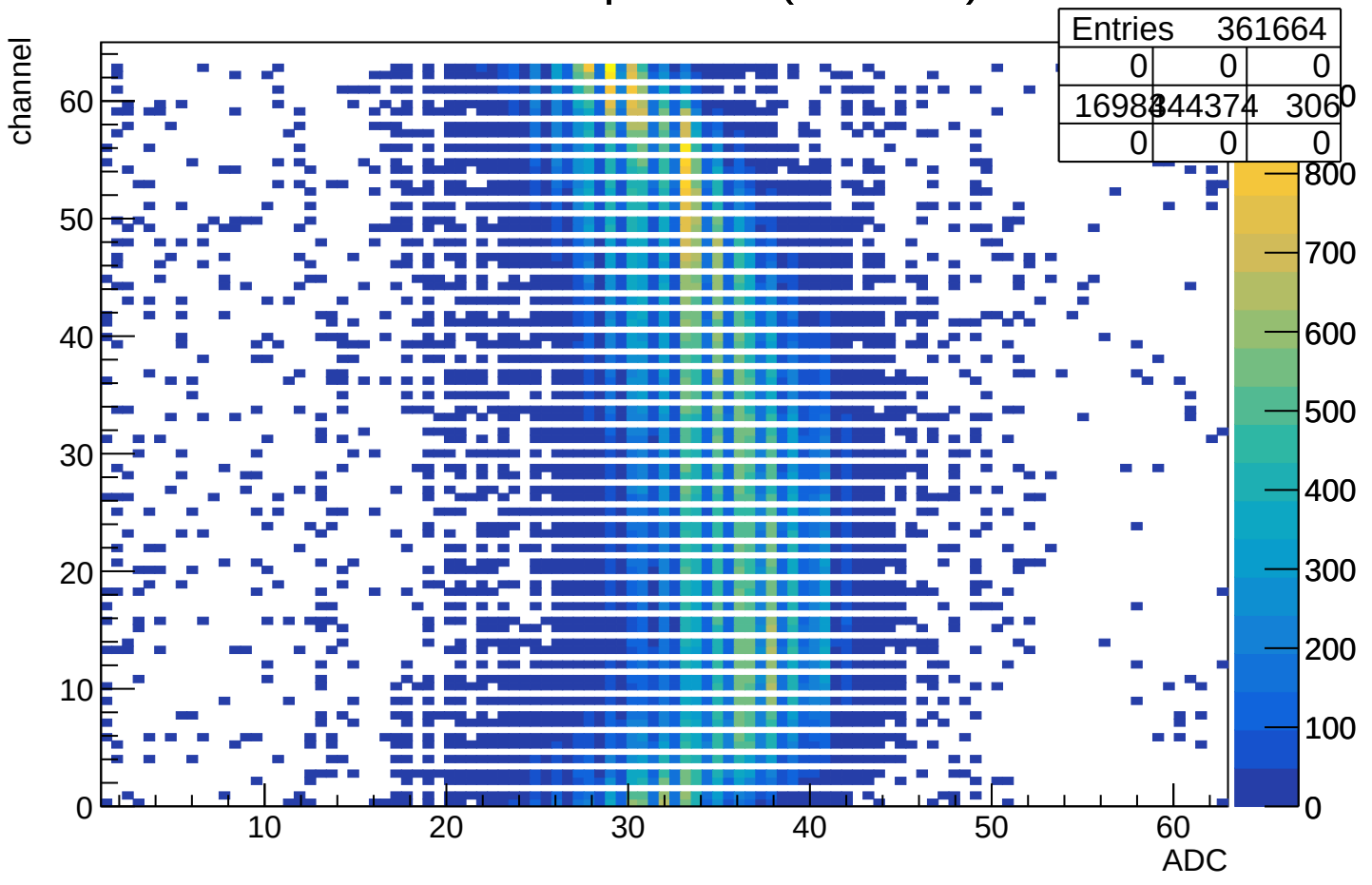

PDO mean L0 positive (all VMM)
Entries 361664
channel
ADC
0
200
400
600
800
1000
10
20
30
40
50
60
100
300
500

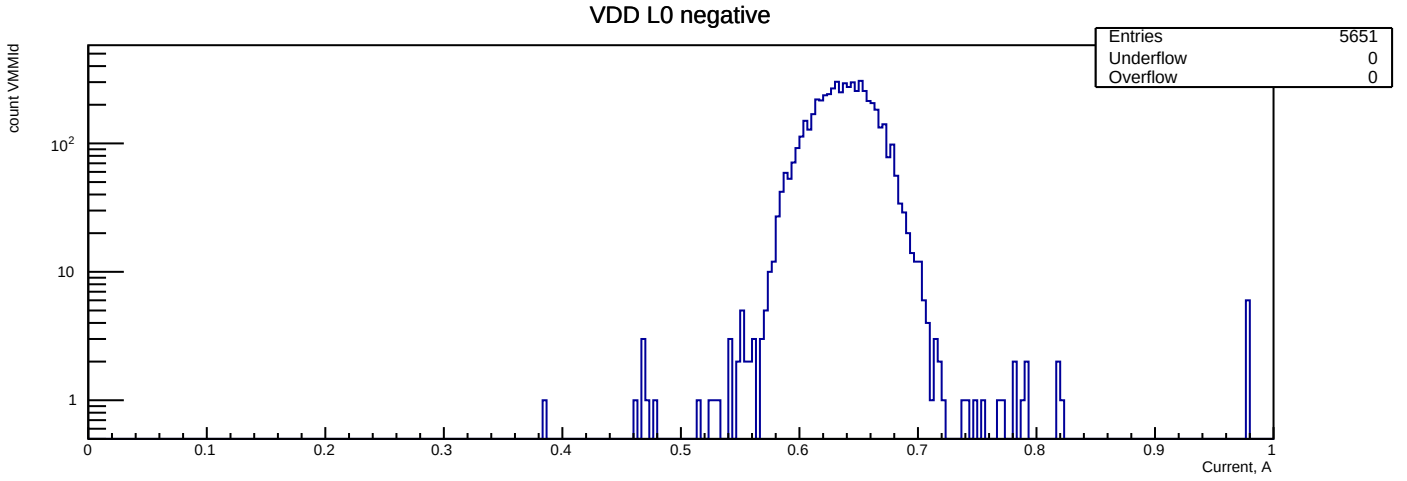

PDO entries mean L0 positive
Entries 361664
channel
Entries
0
10
20
30
40
50
60
20
40
60
80
100
120
1000
2000
3000
4000

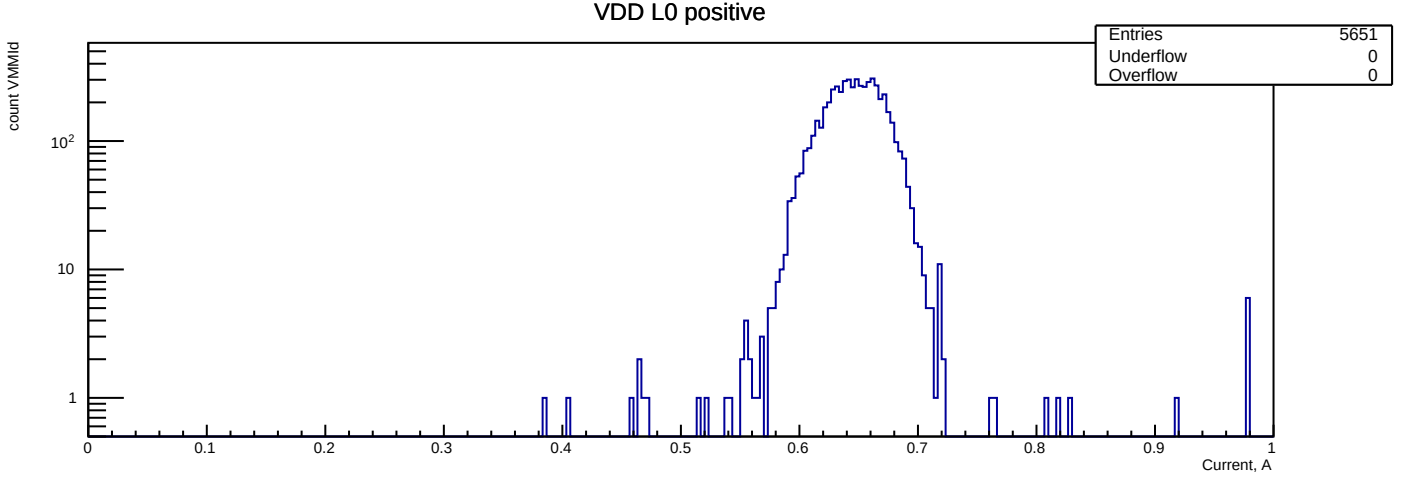

TDO mean L0 positive (all VMM)
Entries 361664
0 0 0
19538 342130 0
0 0 0
channel
ADC
0
10
20
30
40
50
60
0
50
100
150
200
250
0
50
100
150
200
250
300
350
400

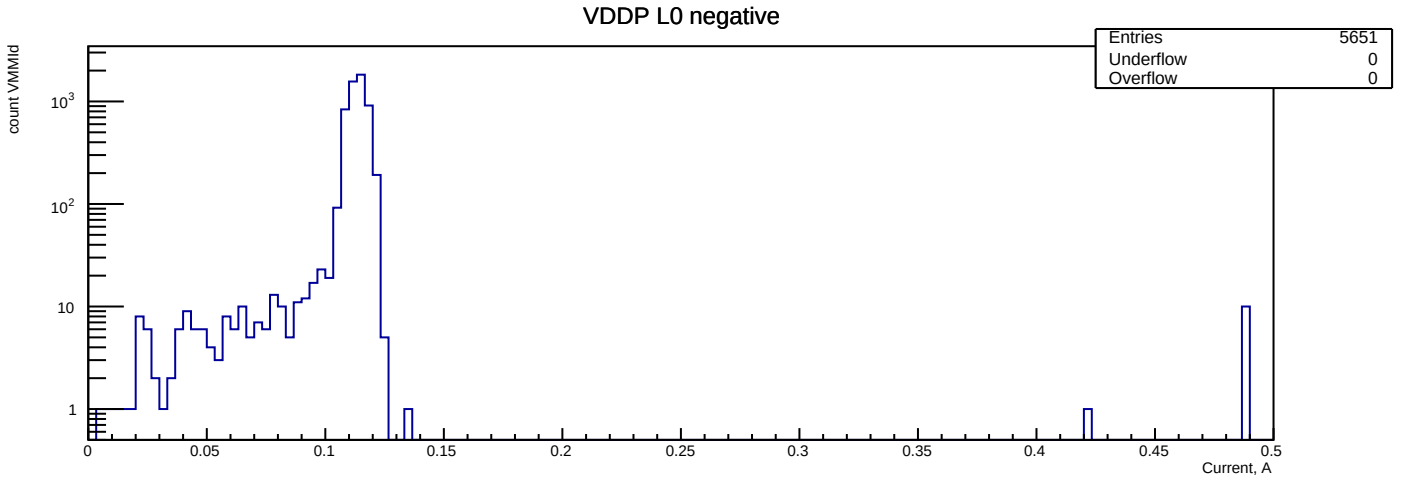

TDO entries mean L0 positive
Entries 361664
0 0 0
19538 342037 93
0 0 0
channel
0
10
20
30
40
50
60
20
40
60
80
100
120
Entries
0
1000
2000
3000
4000

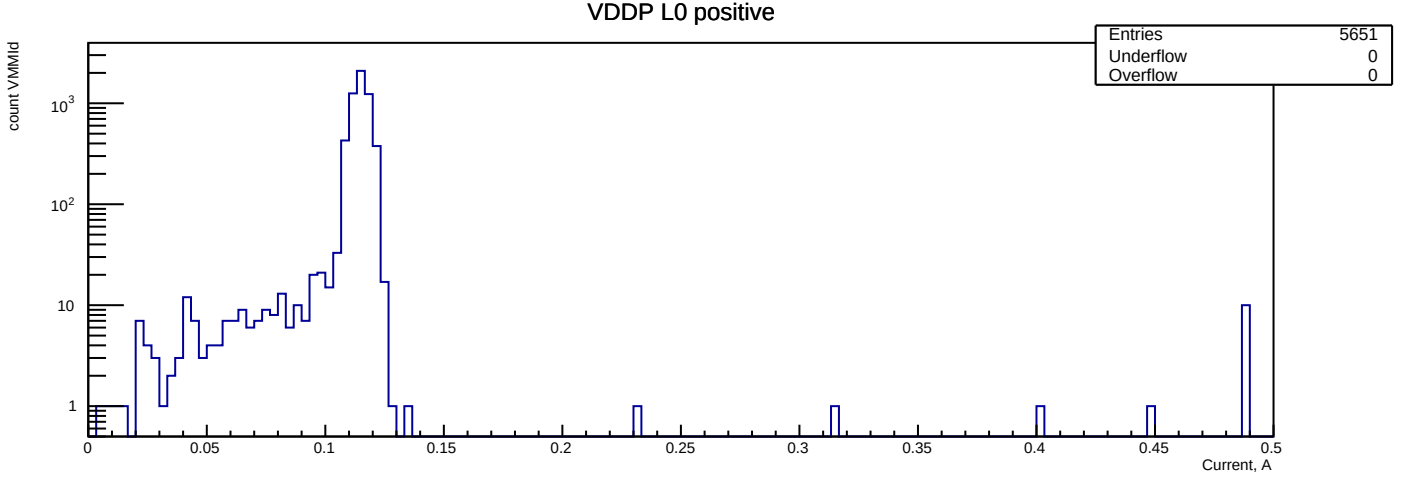

DDO mean negative (all VMM)
Entries 361664
channel
ADC
0
10
20
30
40
50
60
100
200
300
400

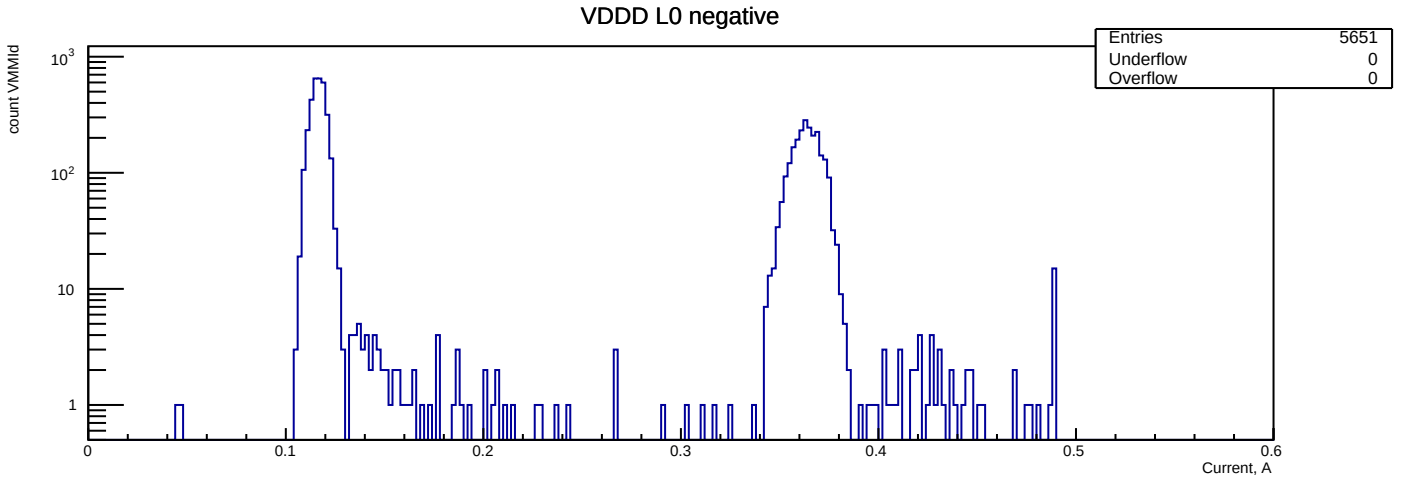

DDO mean positive (all VMM)
Entries 361664
channel
ADC
0
10
20
30
40
50
60
100
200
300
400
500
600
700
800

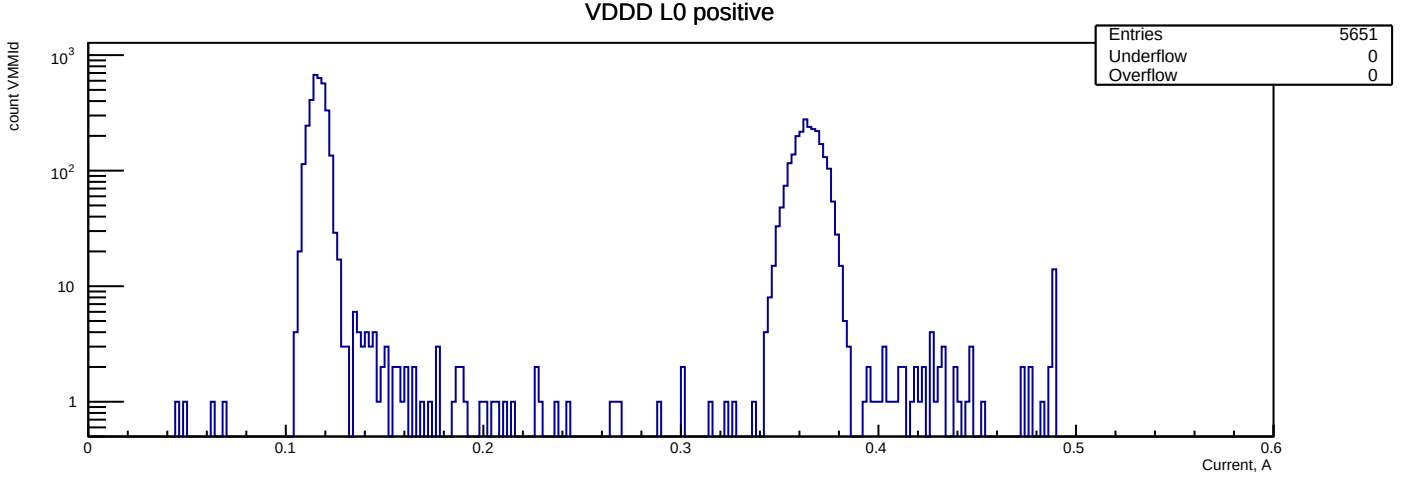

VDD L0 negative
Entries 5651
Underflow 0
Overflow 0
count VMMId
10^2
10
1
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Current, A

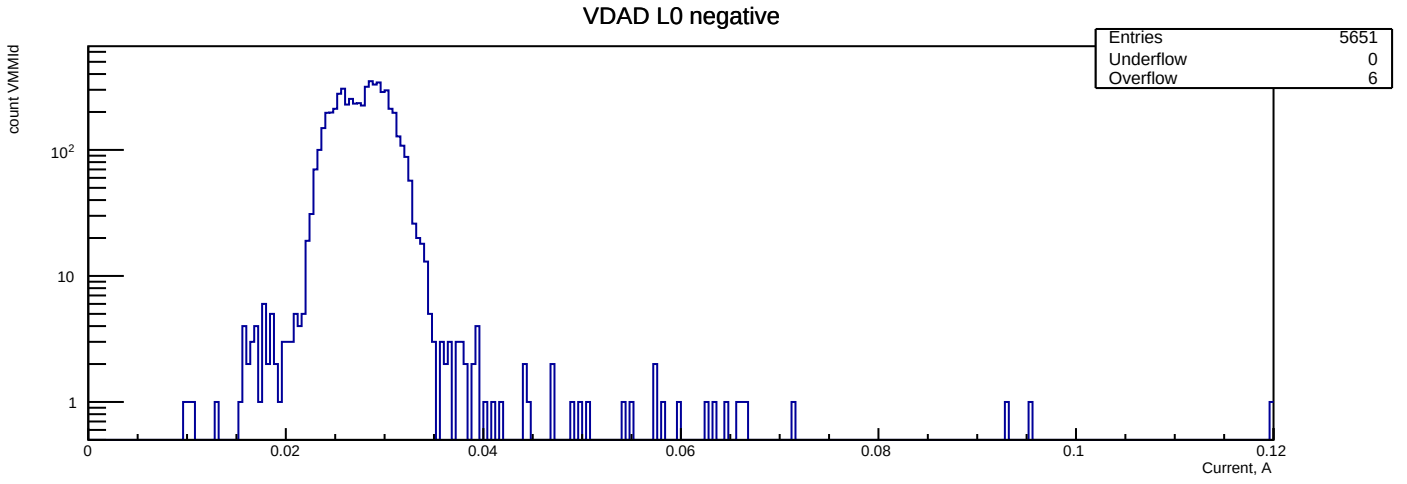

VDD L0 positive
Entries 5651
Underflow 0
Overflow 0
count VMMId
10^2
10
1
0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1
Current, A

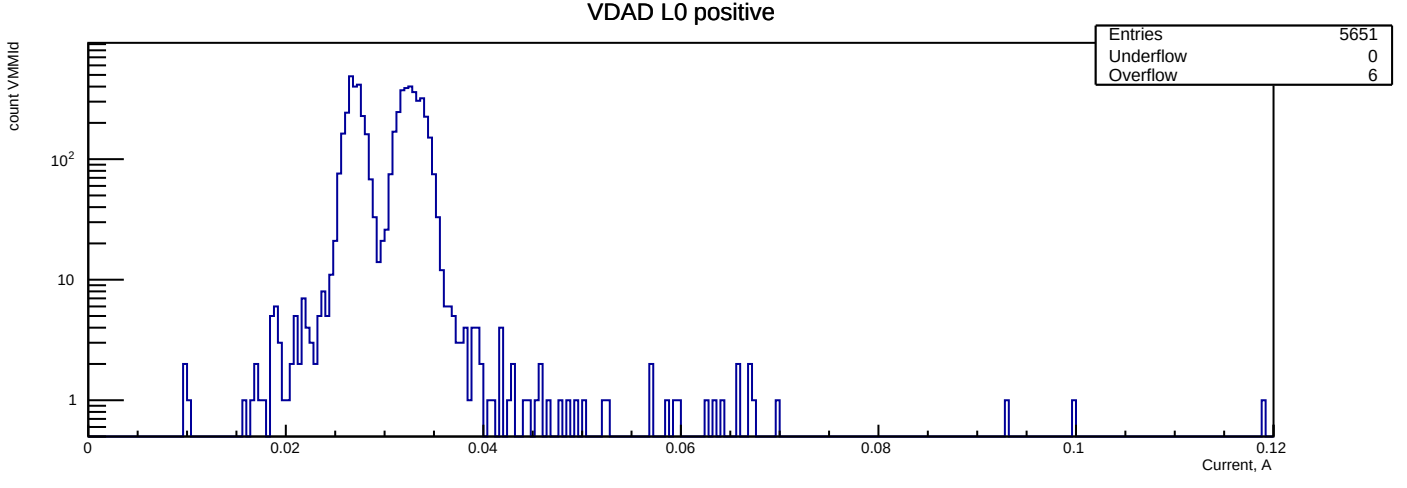

VDDP L0 negative
Entries 5651
Underflow 0
Overflow 0
count VMMId
10^3
10^2
10
1
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
Current, A

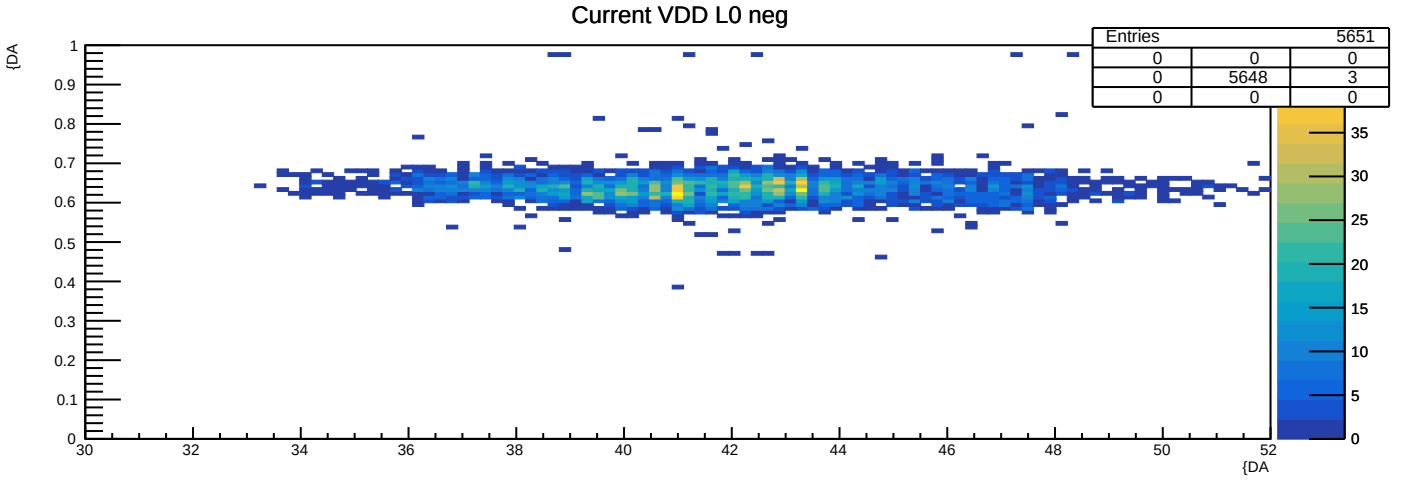

VDDP L0 positive
Entries 5651
Underflow 0
Overflow 0
count VMMId
10^3
10^2
10
1
0
0.05
0.1
0.15
0.2
0.25
0.3
0.35
0.4
0.45
0.5
Current, A

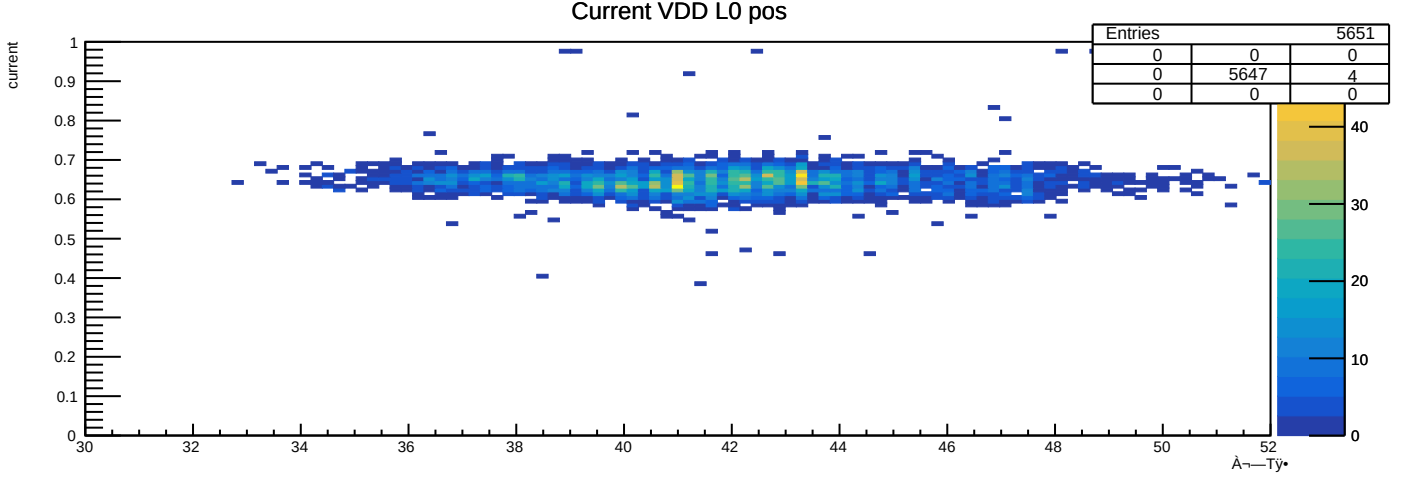

VDDD L0 negative
Entries 5651
Underflow 0
Overflow 0
count VMMId
10^3
10^2
10
1
0
0.1
0.2
0.3
0.4
0.5
0.6
Current, A

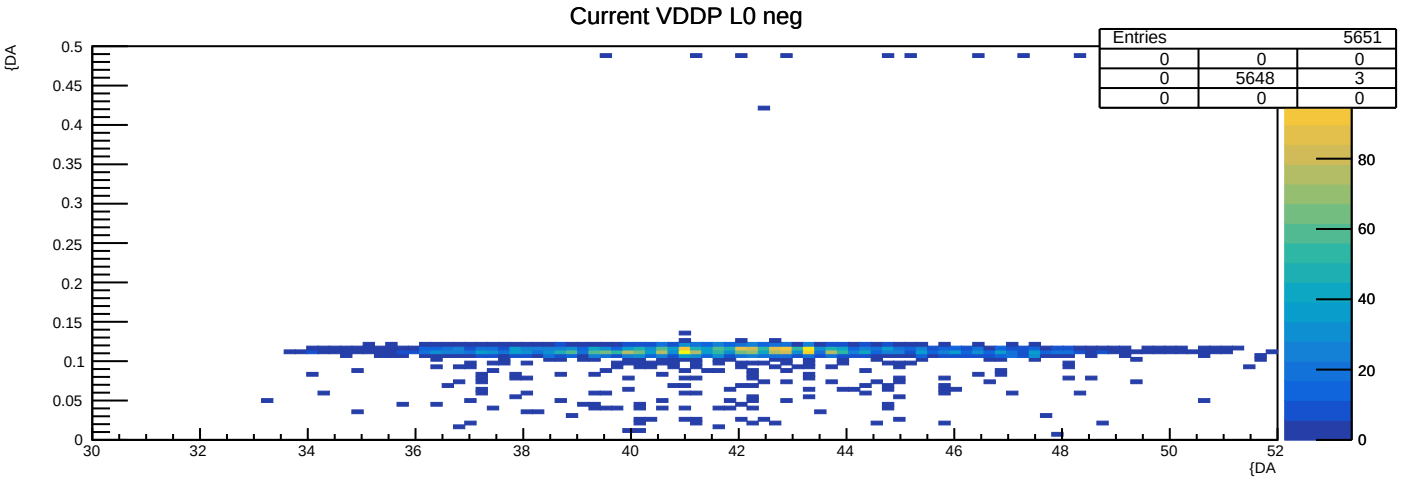

VDDD L0 positive
Entries 5651
Underflow 0
Overflow 0
count VMMId
10^3
10^2
10
1
0
0.1
0.2
0.3
0.4
0.5
0.6
Current, A

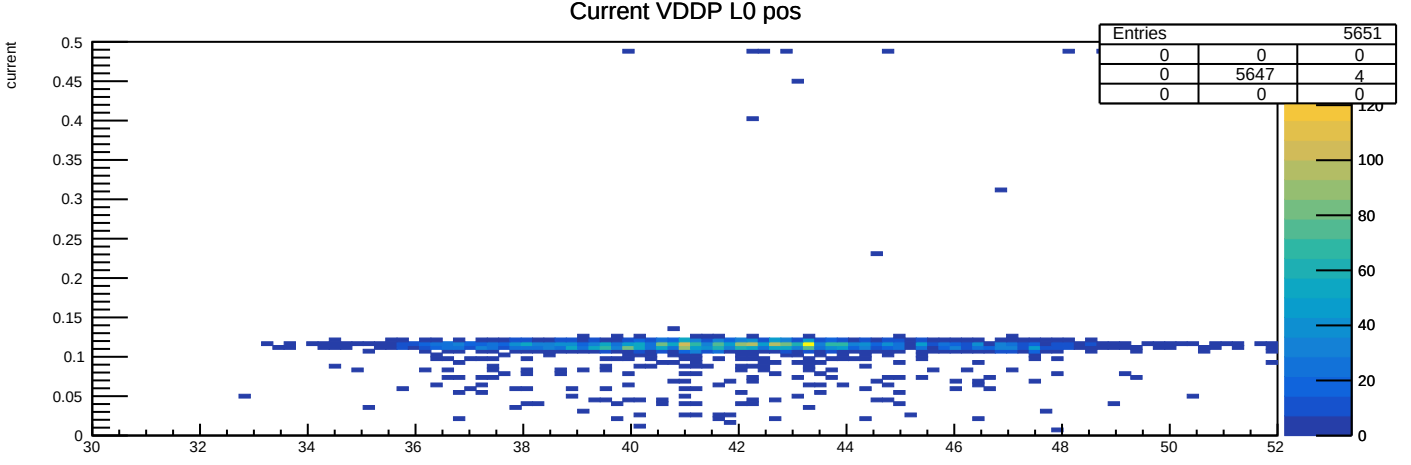

VDAD L0 negative
Entries 5651
Underflow 0
Overflow 6
count VMMId
10^2
10
1
0
0.02
0.04
0.06
0.08
0.1
0.12
Current, A

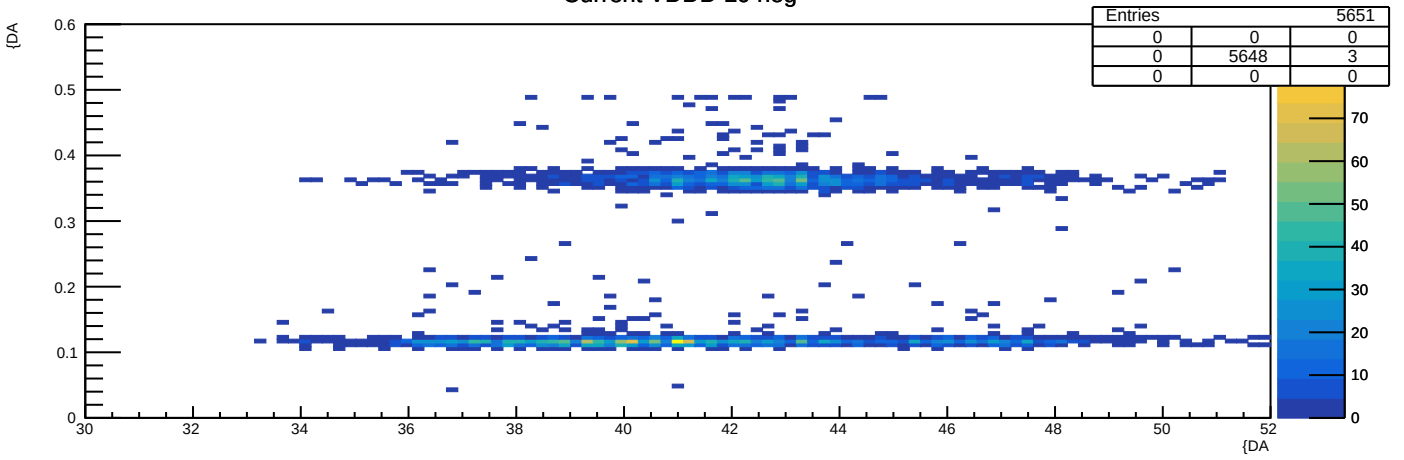

VDAD L0 positive
Entries 5651
Underflow 0
Overflow 6
count VMMId
10^2
10
1
0
0.02
0.04
0.06
0.08
0.1
0.12
Current, A

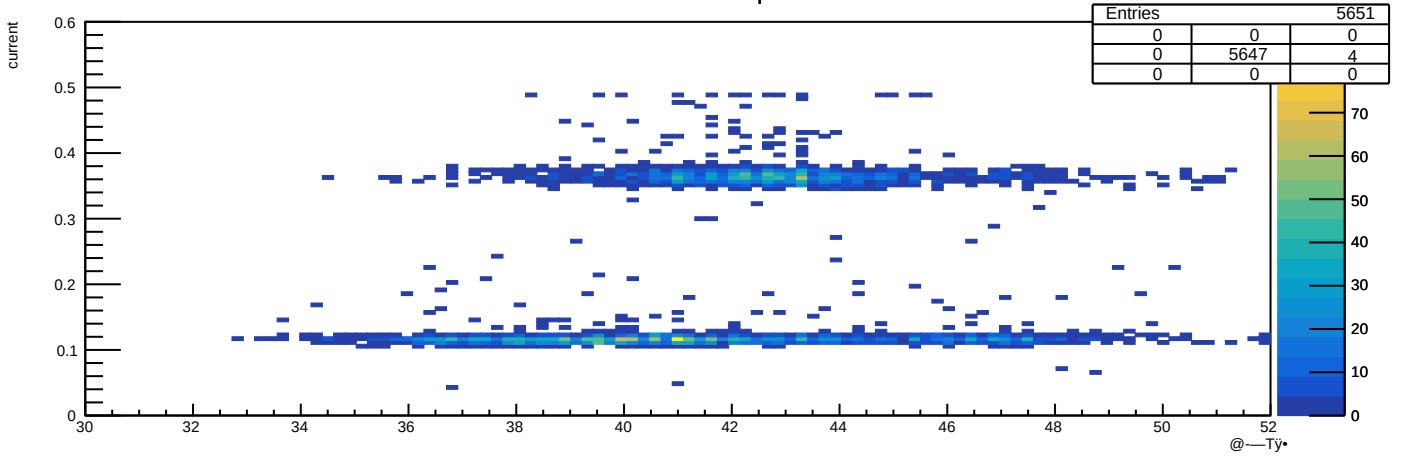

Current VDD L0 neg
Entries 5651
0 0 0
0 5648 3
0 0 0
{DA
{DA

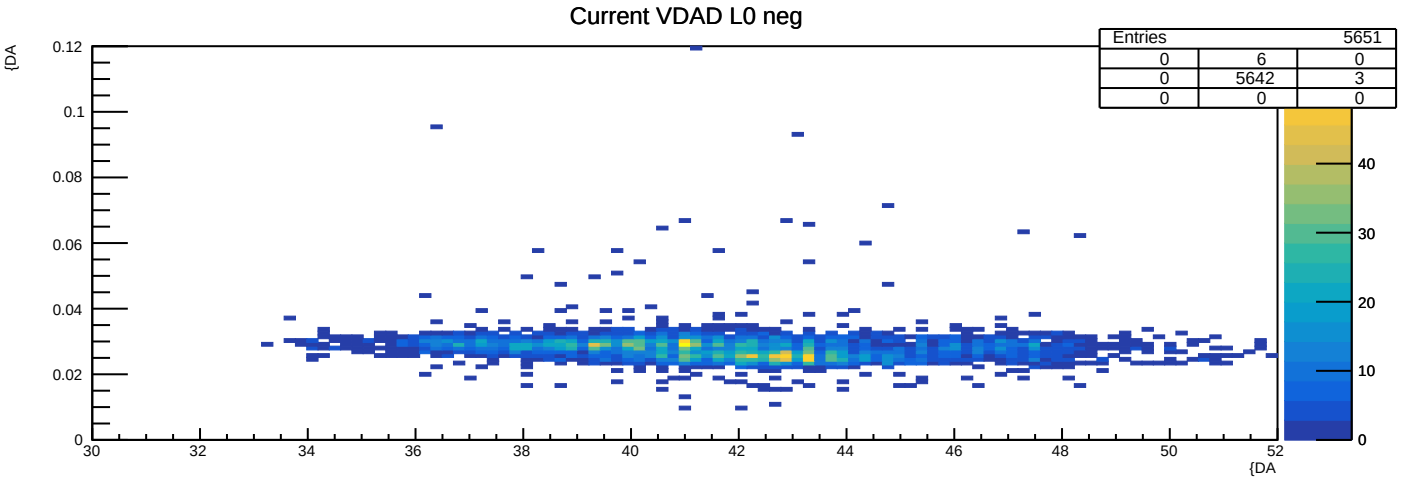

Current VDD L0 pos
Entries 5651
0 0 0
0 5647 4
0 0 0
current
À¬—Tÿ•

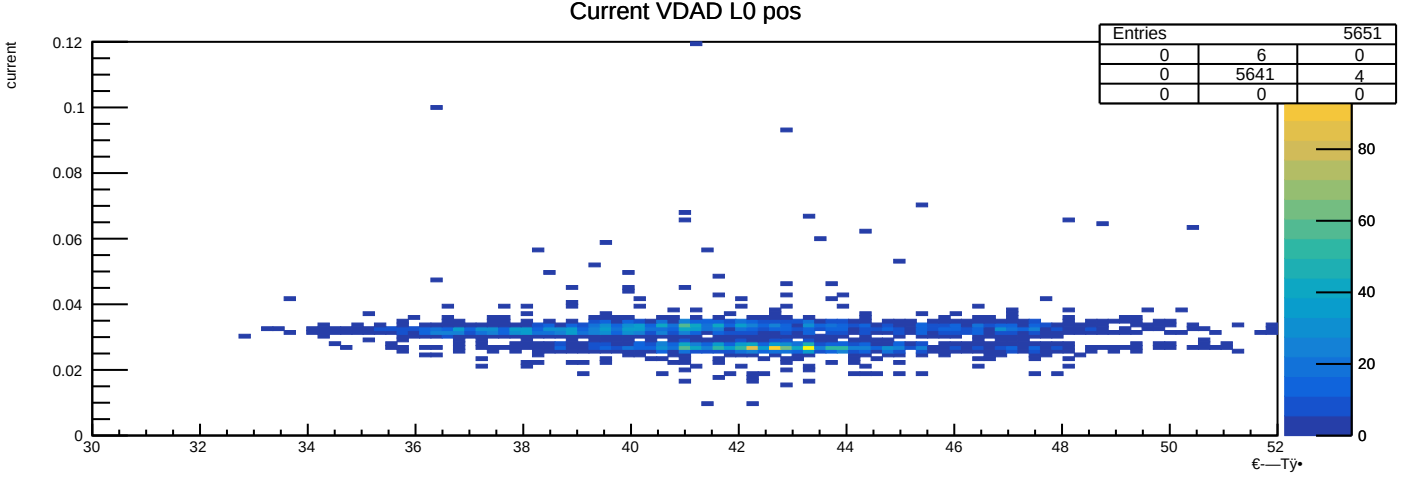

Current VDDP L0 neg
Entries 5651
0 0 0
0 5648 3
0 0 0
{DA
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
30
32
34
36
38
40
42
44
46
48
50
52
{DA
80
60
40
20
0

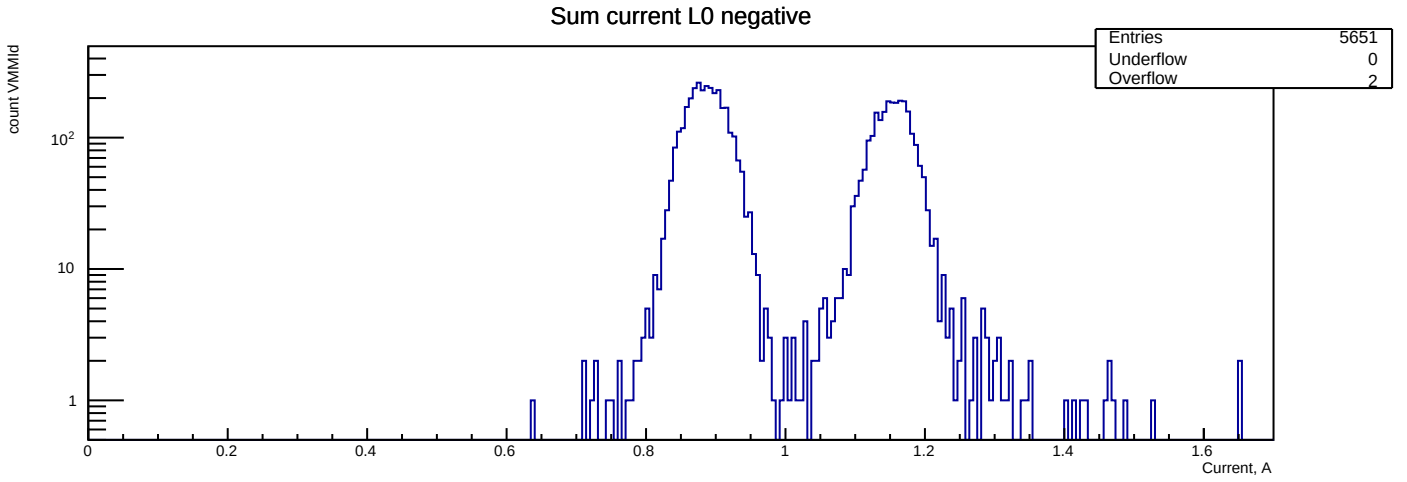

Current VDDP L0 pos
Entries 5651
0 0 0
0 5647 4
0 0 0
current
0.5
0.45
0.4
0.35
0.3
0.25
0.2
0.15
0.1
0.05
0
30
32
34
36
38
40
42
44
46
48
50
52
120
100
80
60
40
20
0

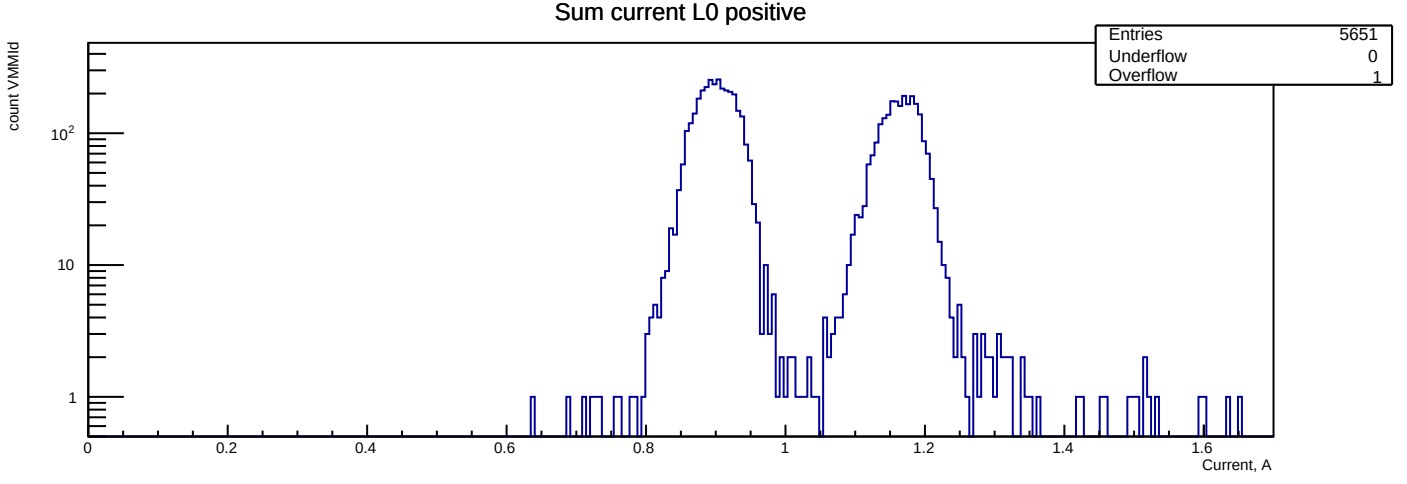

Current VDDD L0 neg
Entries 5651
0 0 0
0 5648 3
0 0 0
{DA
{DA

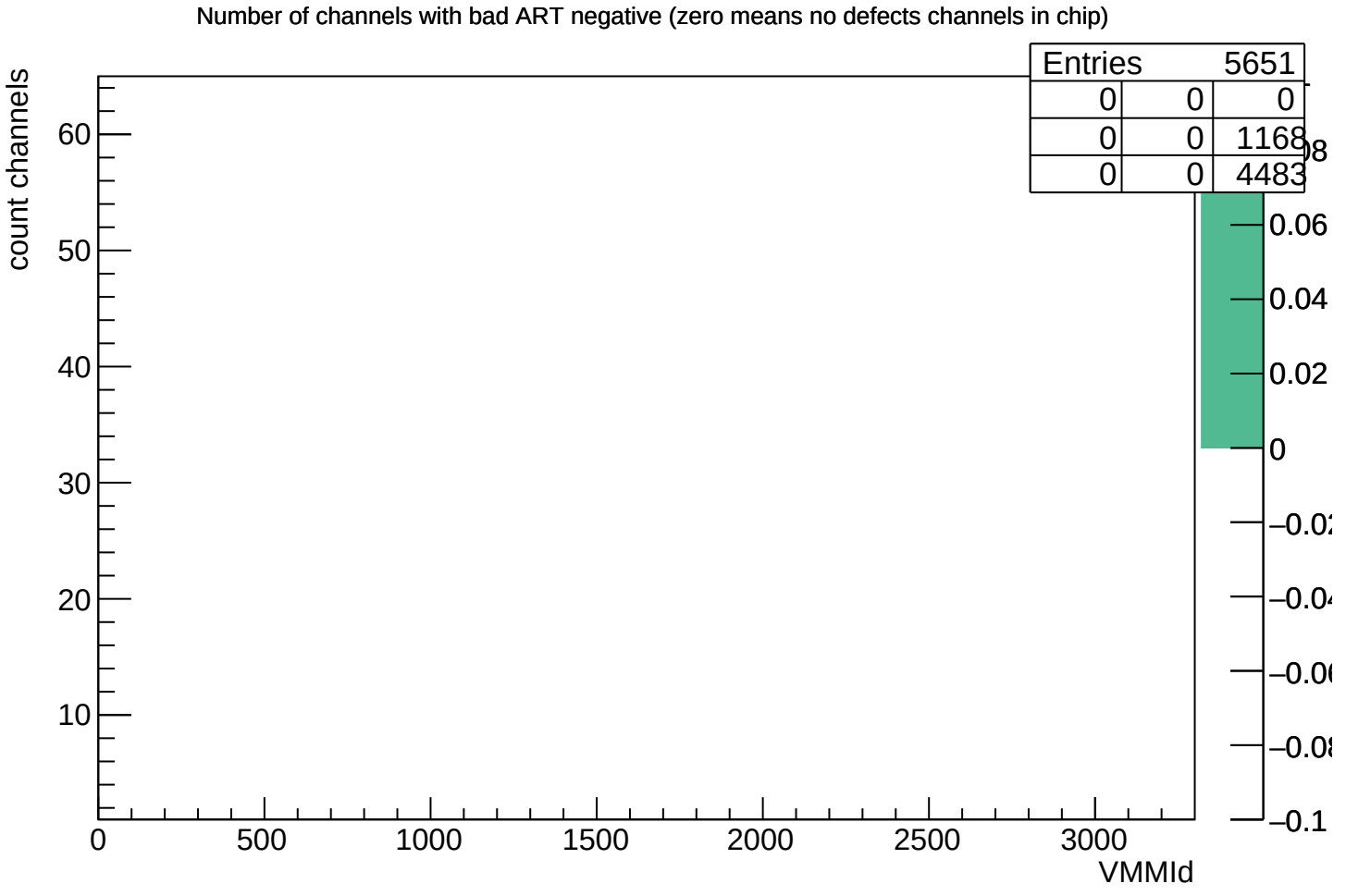

Current VDDD L0 pos
Entries 5651
0 0 0
0 5647 4
0 0 0
current
@—Tÿ•

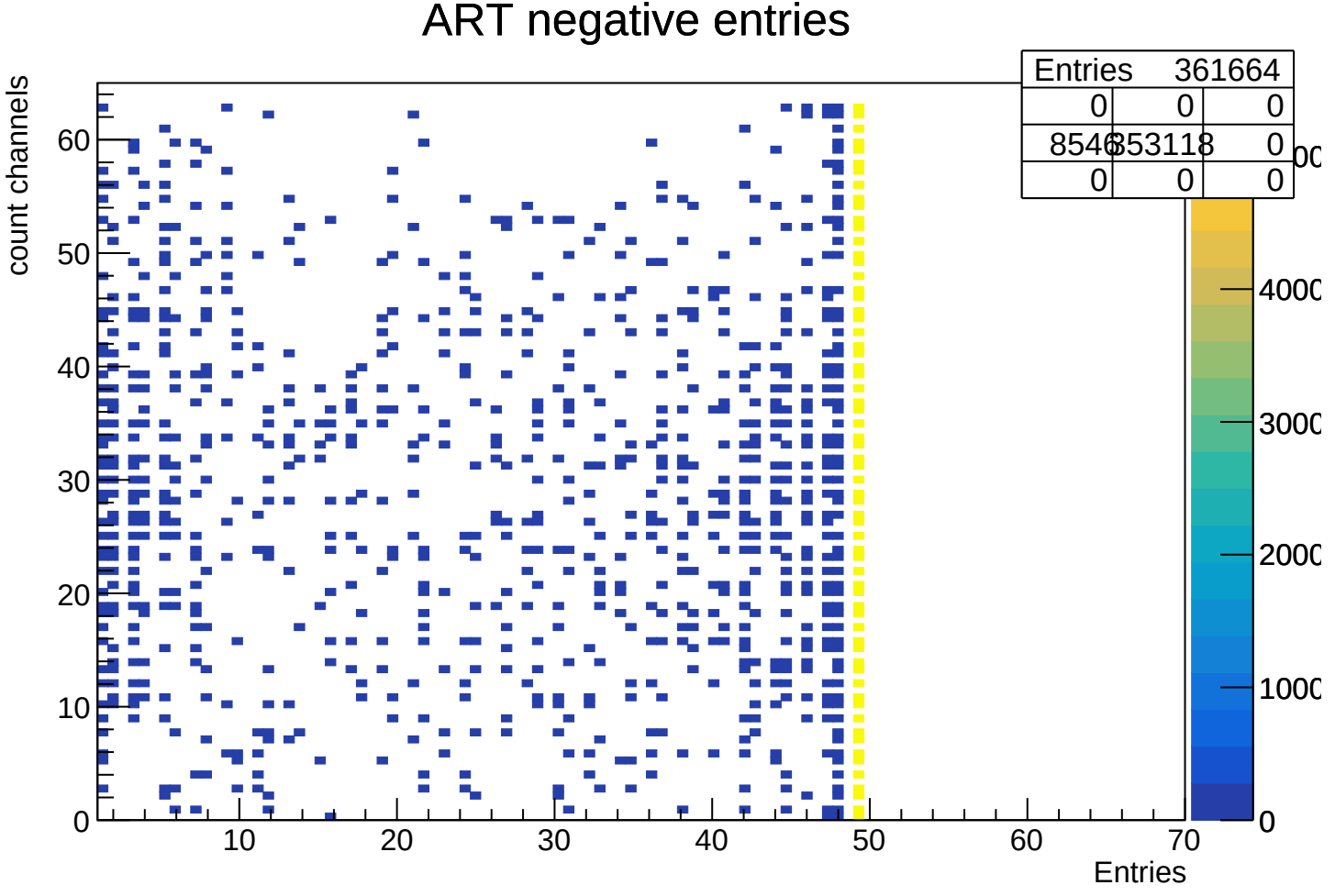

Current VDAD L0 neg
Entries 5651
0 6 0
0 5642 3
0 0 0
{DA
0.12
0.1
0.08
0.06
0.04
0.02
0
30
32
34
36
38
40
42
44
46
48
50
52
{DA
40
30
20
10
0

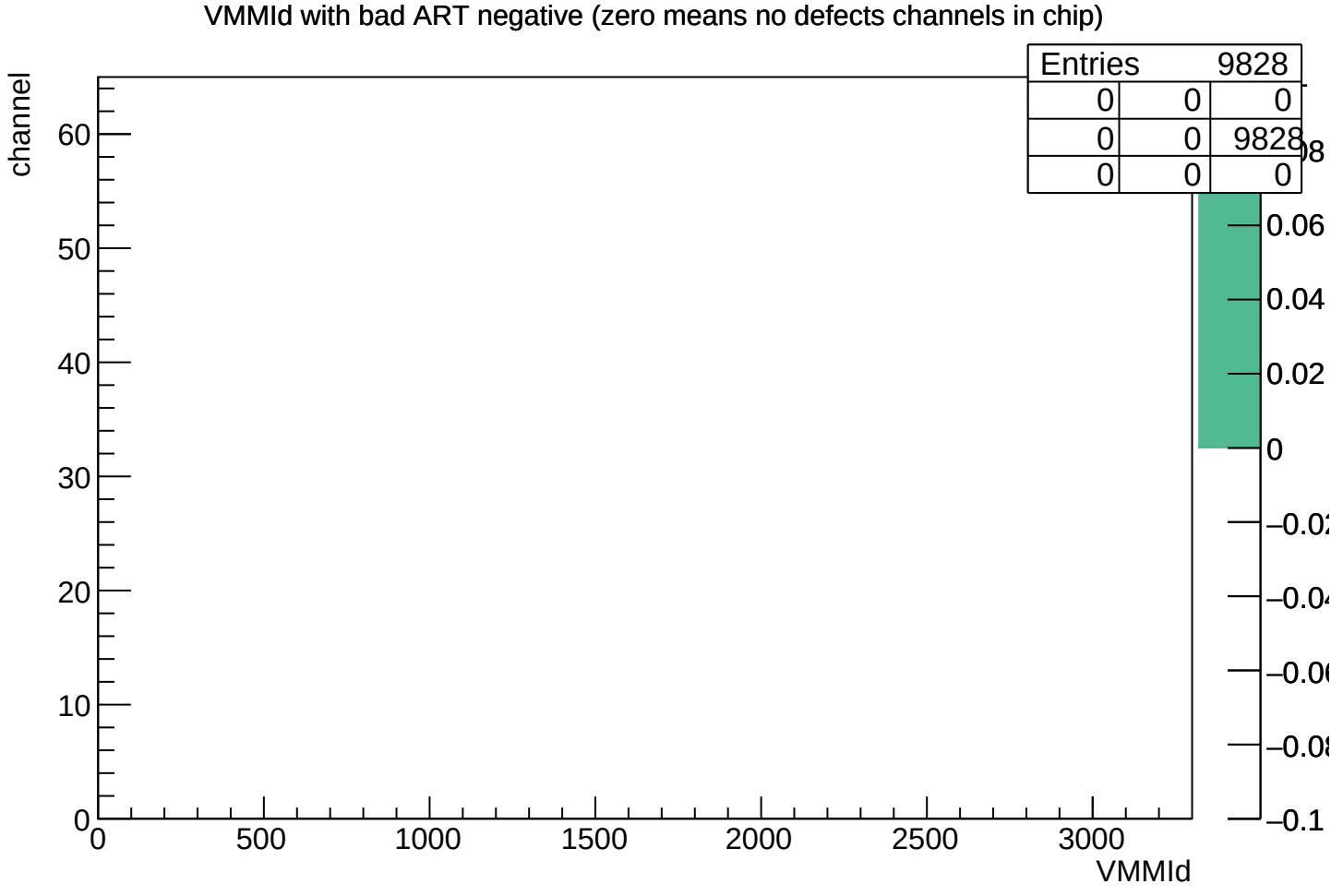

Current VDAD L0 pos
Entries 5651
0 6 0
0 5641 4
0 0 0
current
0.12
0.1
0.08
0.06
0.04
0.02
0
30
32
34
36
38
40
42
44
46
48
50
52
€-—Tÿ•
80
60
40
20
0

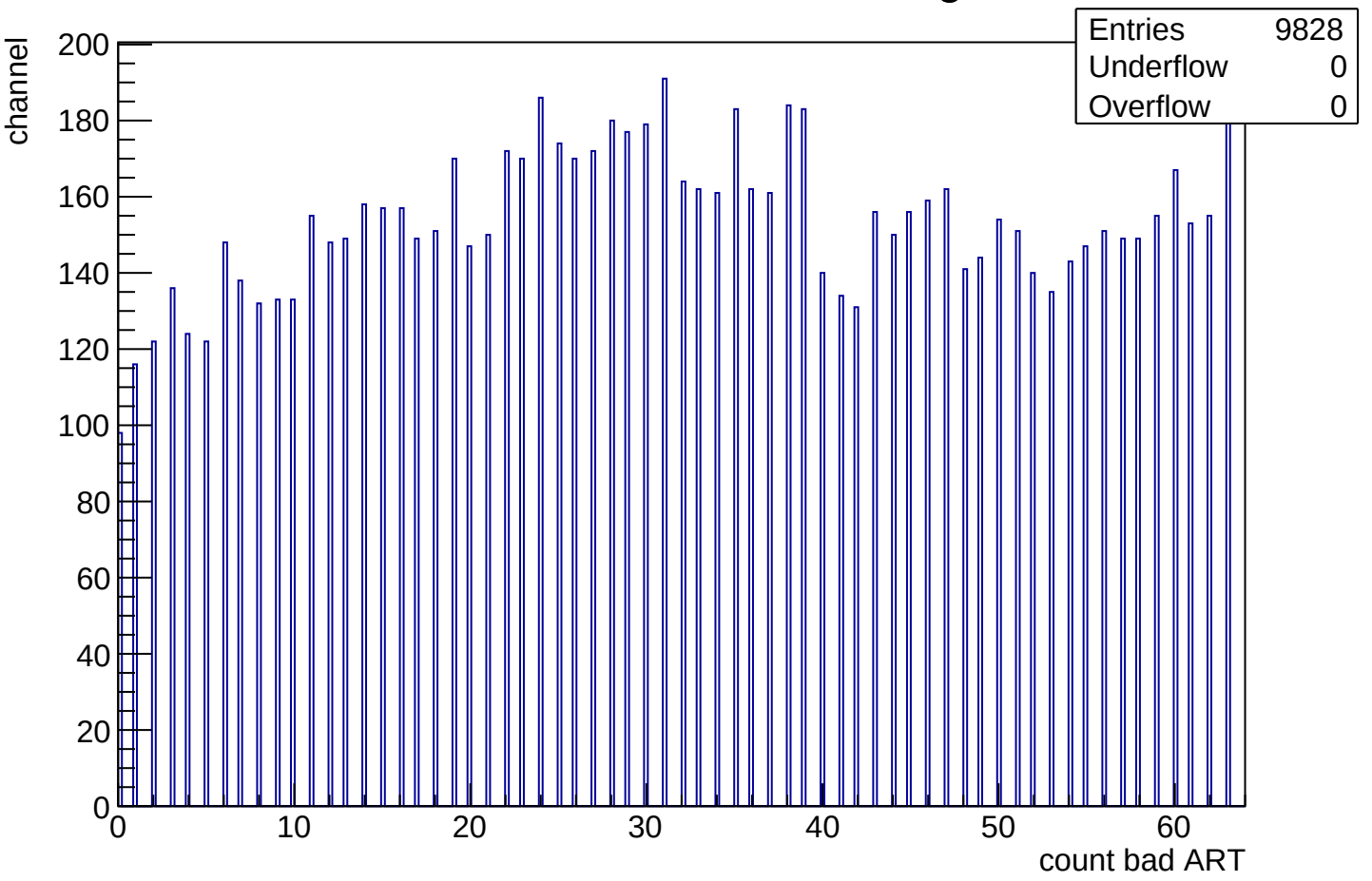

Sum current L0 negative
Entries 5651
Underflow 0
Overflow 2
count VMMId
10^2
10
1
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Current, A

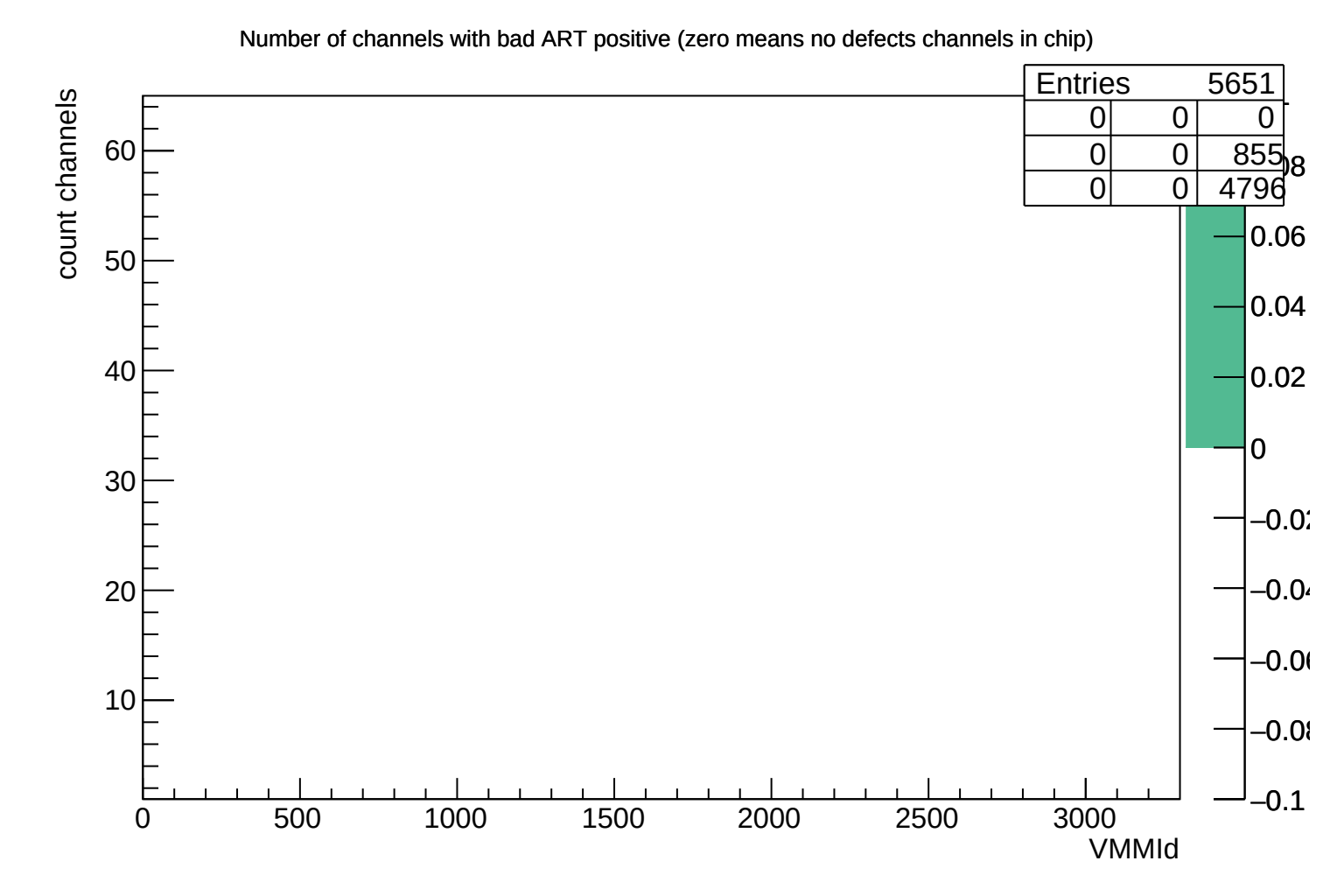

Sum current L0 positive
Entries 5651
Underflow 0
Overflow 1
count VMMId
10^2
10
1
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Current, A

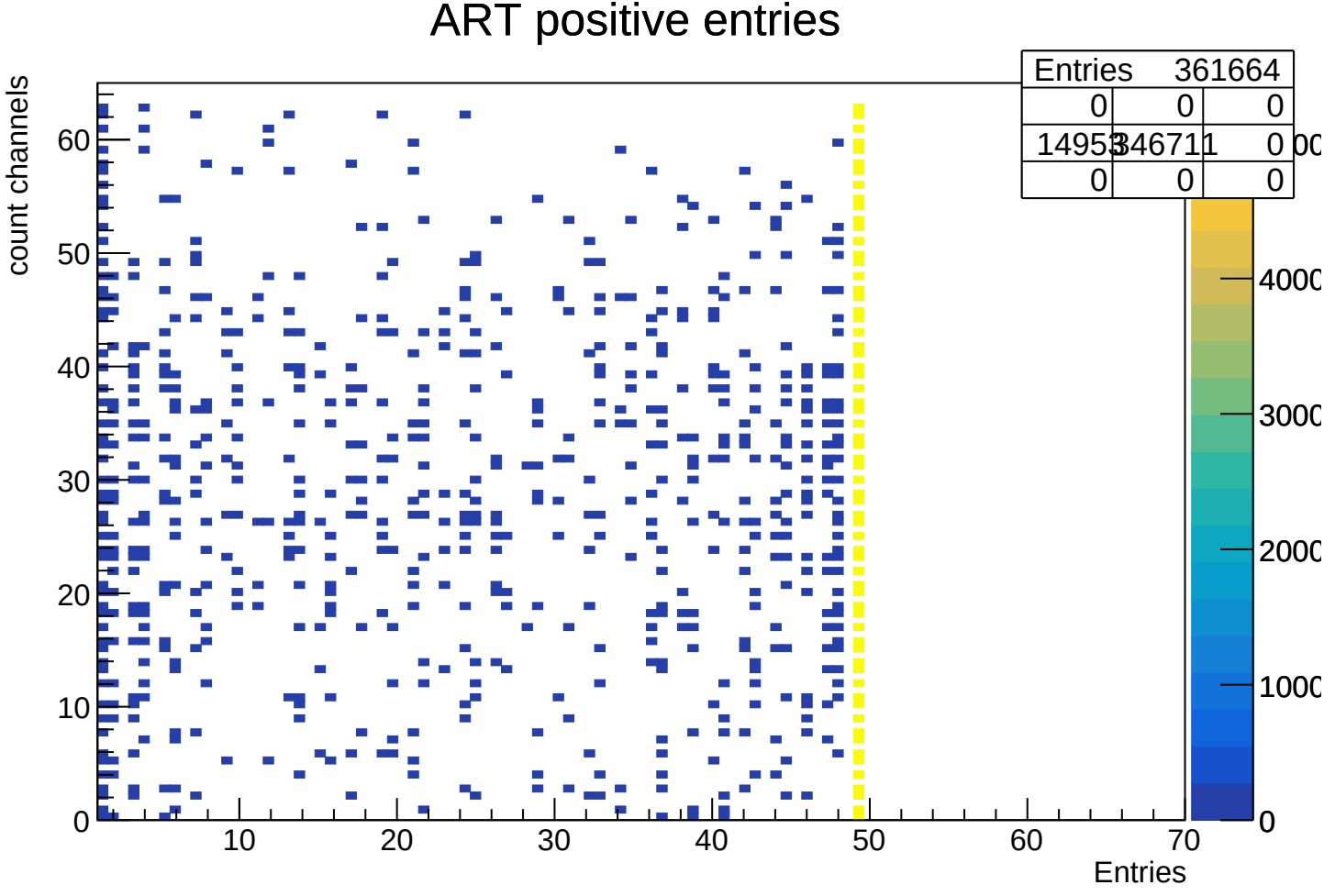

Number of channels with bad ART negative (zero means no defects channels in chip)
Entries 5651
0 0 0
0 0 1168
0 0 4483
count channels
60
50
40
30
20
10
0
500
1000
1500
2000
2500
3000
VMMId
0.06
0.04
0.02
0
–0.1

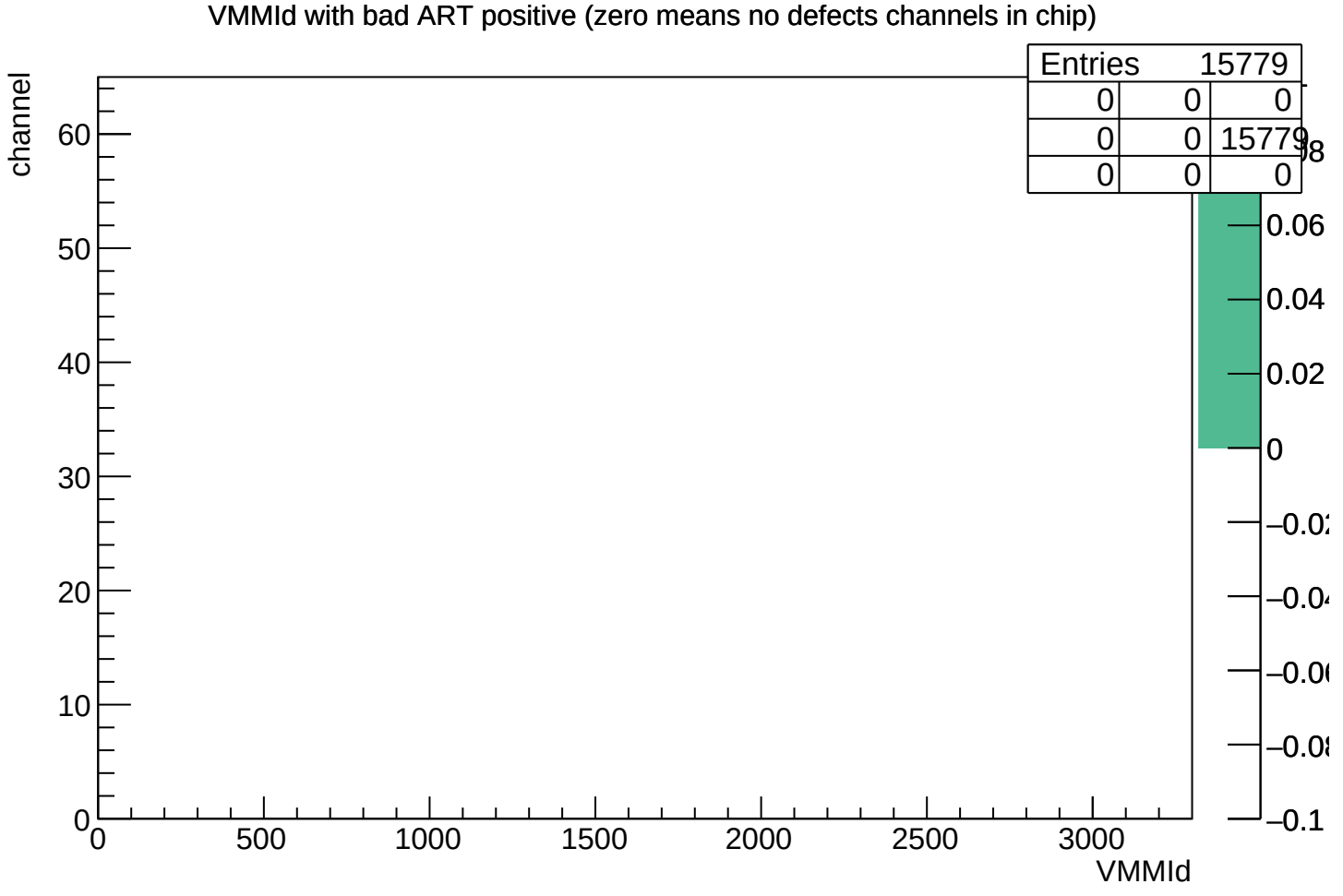

ART negative entries
Entries 361664
0 0 0
8546 53118 0
0 0 0
count channels
0
10
20
30
40
50
60
10
20
30
40
50
60
70
Entries
0
1000
2000
3000
4000

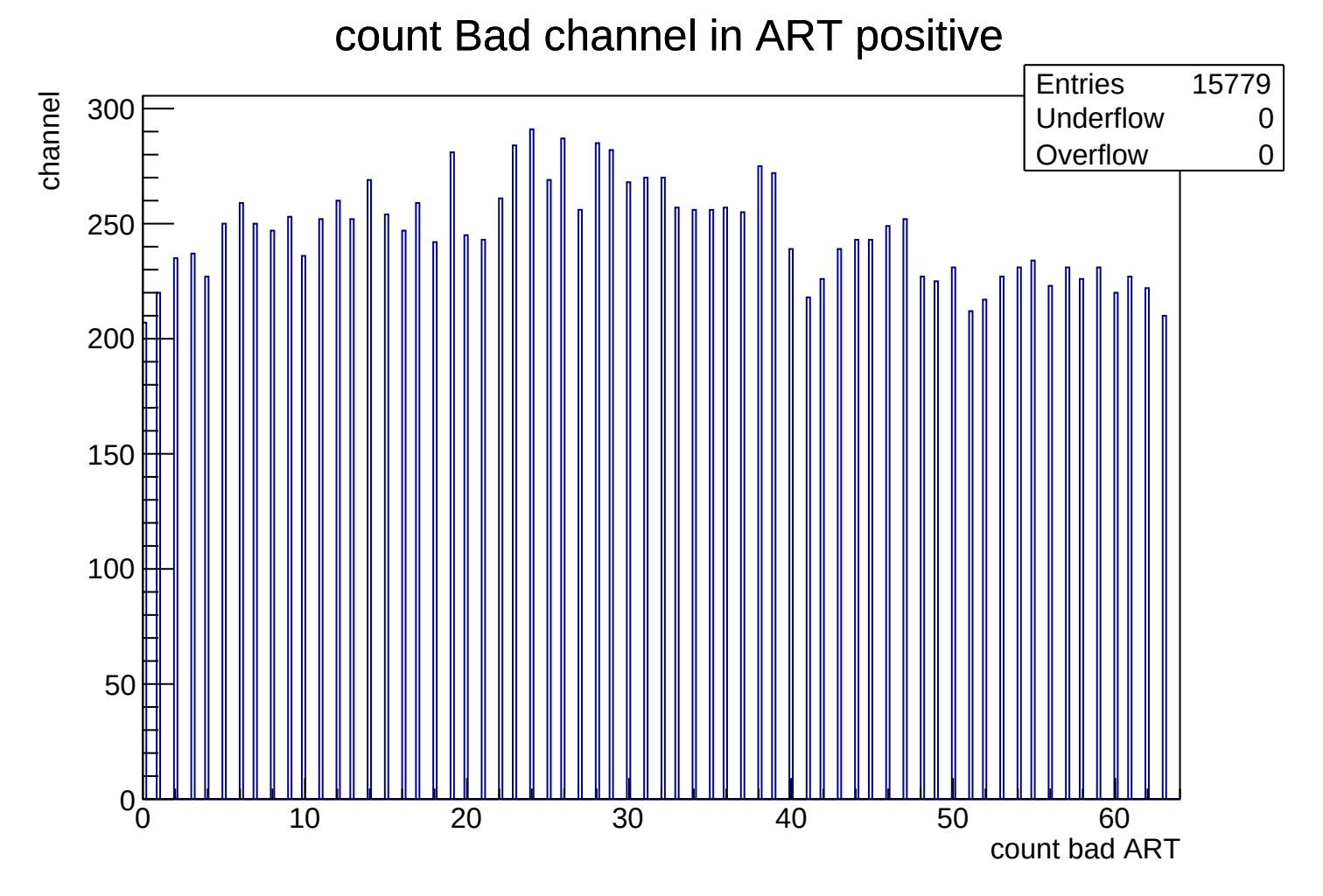

VMMId with bad ART negative (zero means no defects channels in chip)
Entries 9828
channel
VMMId
0
10
20
30
40
50
60
500
1000
1500
2000
2500
3000
0.06
0.04
0.02
0
–0.1

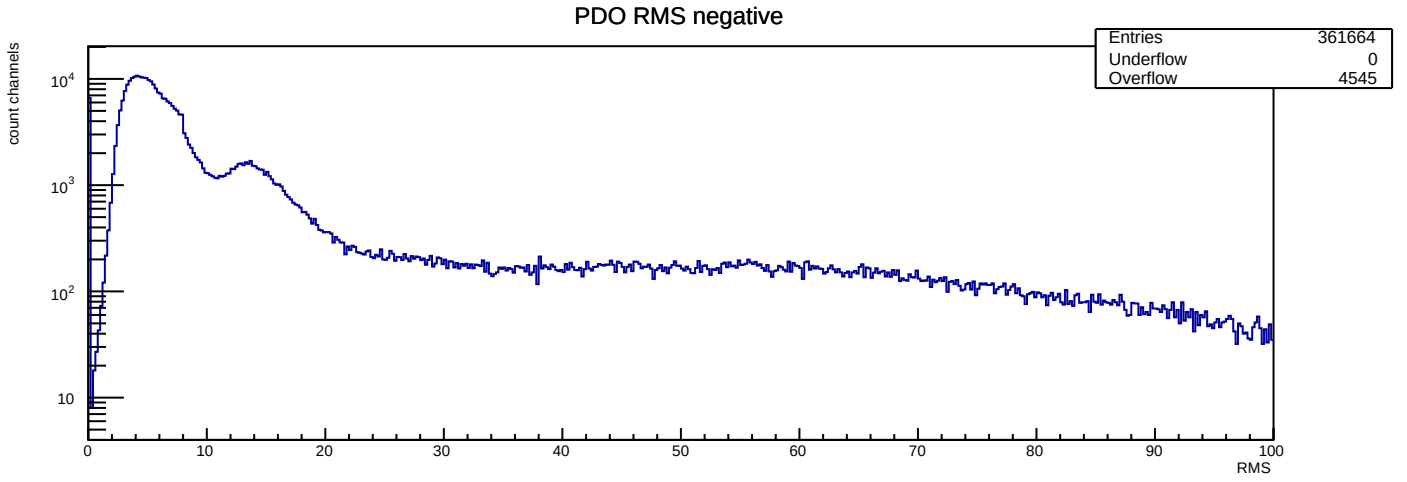

count Bad channel in ART negative
Entries 9828
Underflow 0
Overflow 0
channel
200
180
160
140
120
100
80
60
40
20
0
0
10
20
30
40
50
60
count bad ART

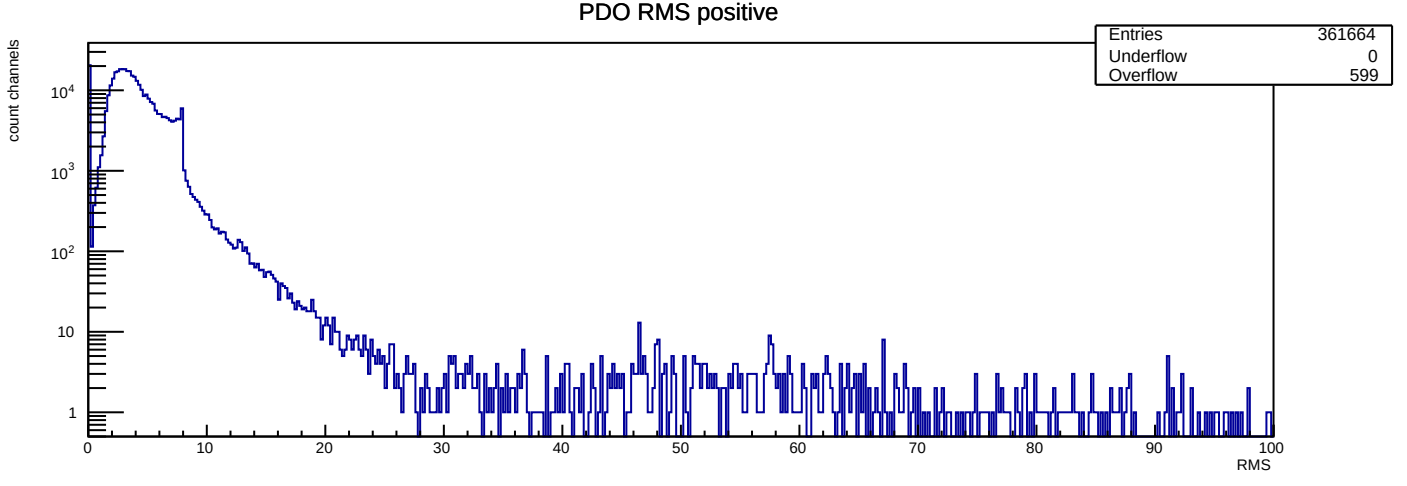

Number of channels with bad ART positive (zero means no defects channels in chip)
Entries 5651
0 0 0
0 0 855
0 0 4796
count channels
60
50
40
30
20
10
0
500
1000
1500
2000
2500
3000
VMMId
0.06
0.04
0.02
0
–0.1

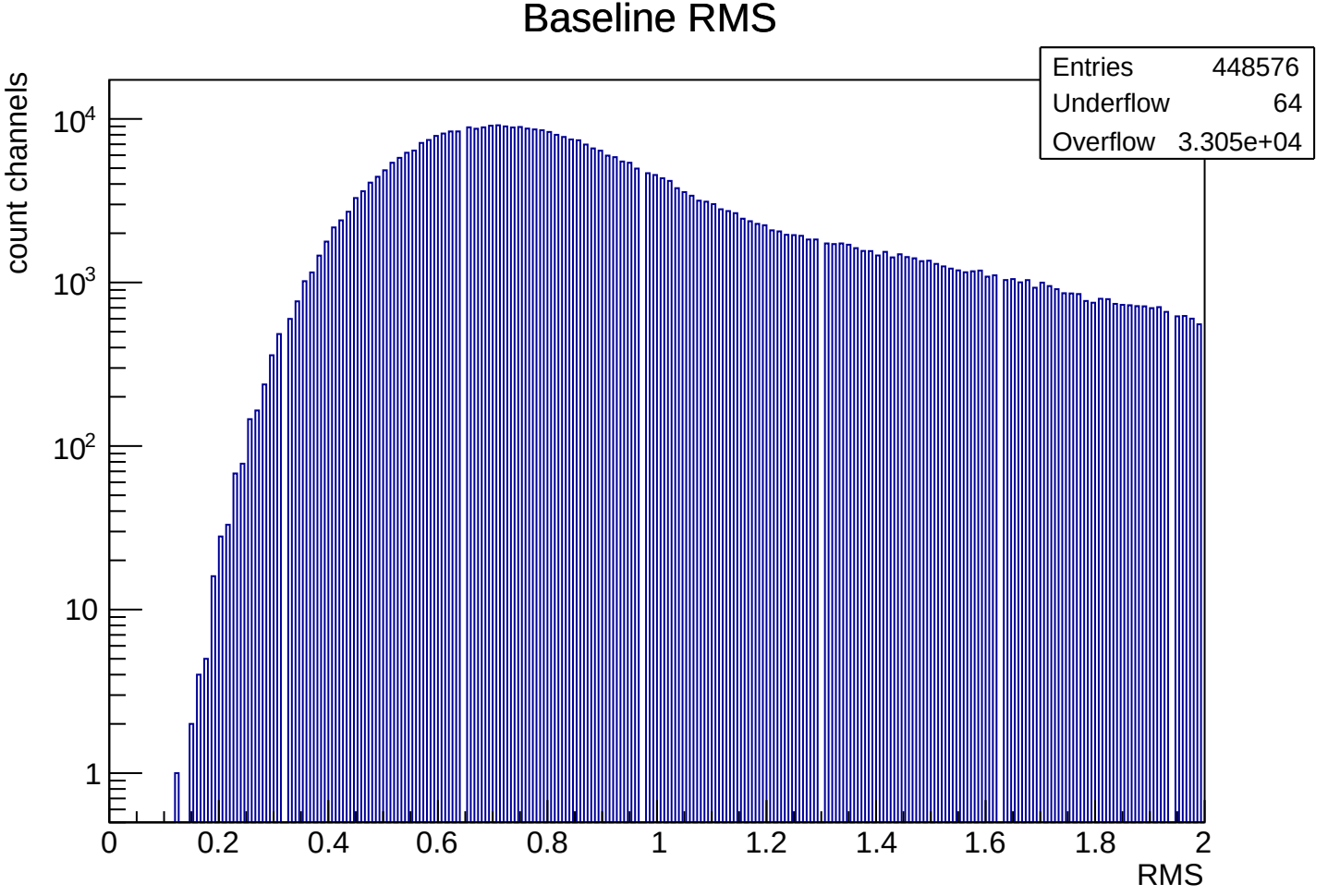

ART positive entries
Entries 361664
0 0 0
1495 346711 0
0 0 0
count channels
0
10
20
30
40
50
60
10
20
30
40
50
60
70
Entries
0
1000
2000
3000
4000

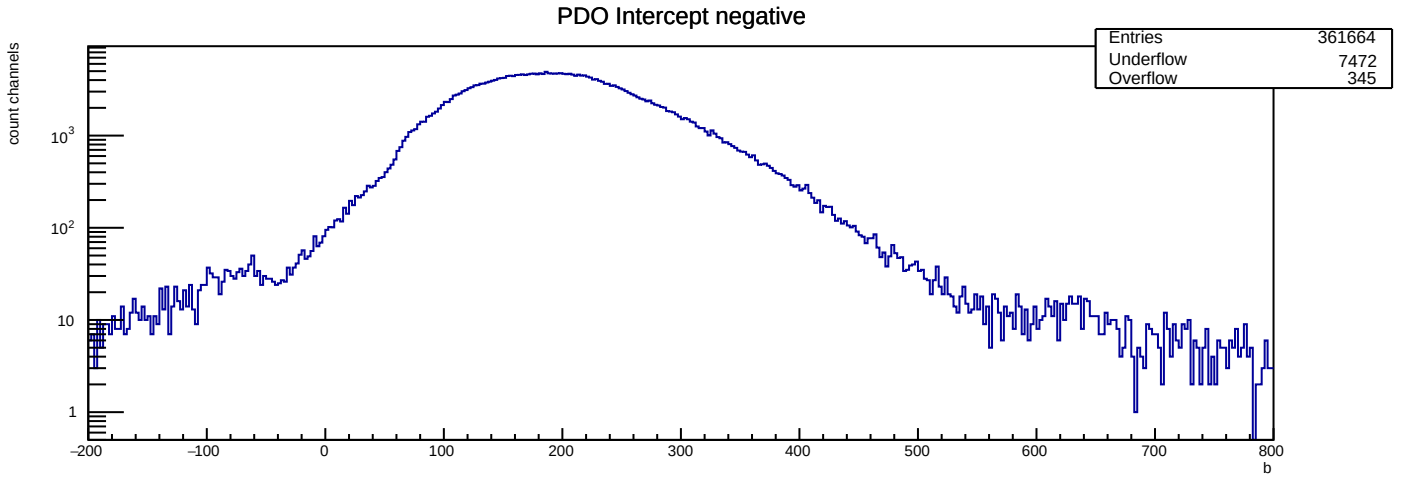

VMMId with bad ART positive (zero means no defects channels in chip)
Entries 15779
channel
VMMId
0
10
20
30
40
50
60
500
1000
1500
2000
2500
3000
0.06
0.04
0.02
0
–0.1

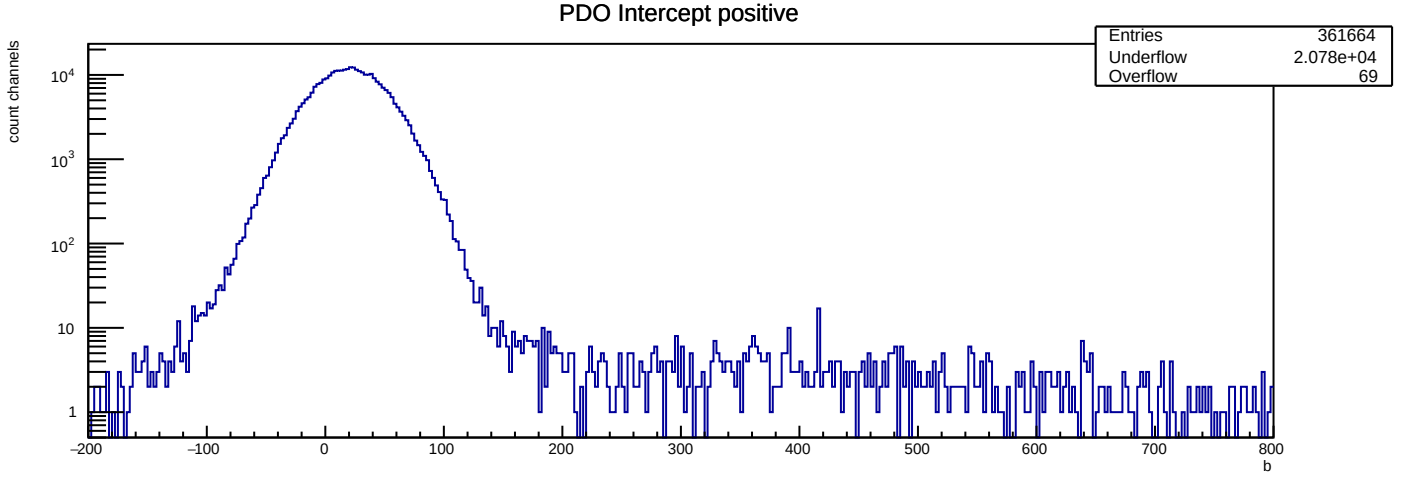

count Bad channel in ART positive
Entries 15779
Underflow 0
Overflow 0
channel
300
250
200
150
100
50
0
0
10
20
30
40
50
60
count bad ART

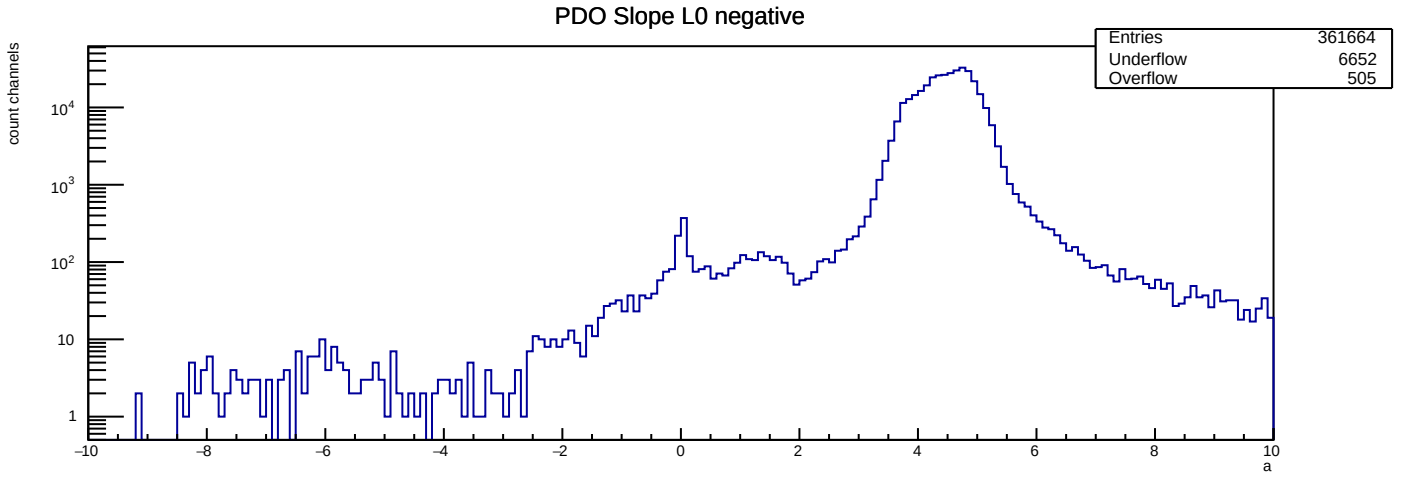

PDO RMS negative
Entries 361664
Underflow 0
Overflow 4545
count channels
RMS

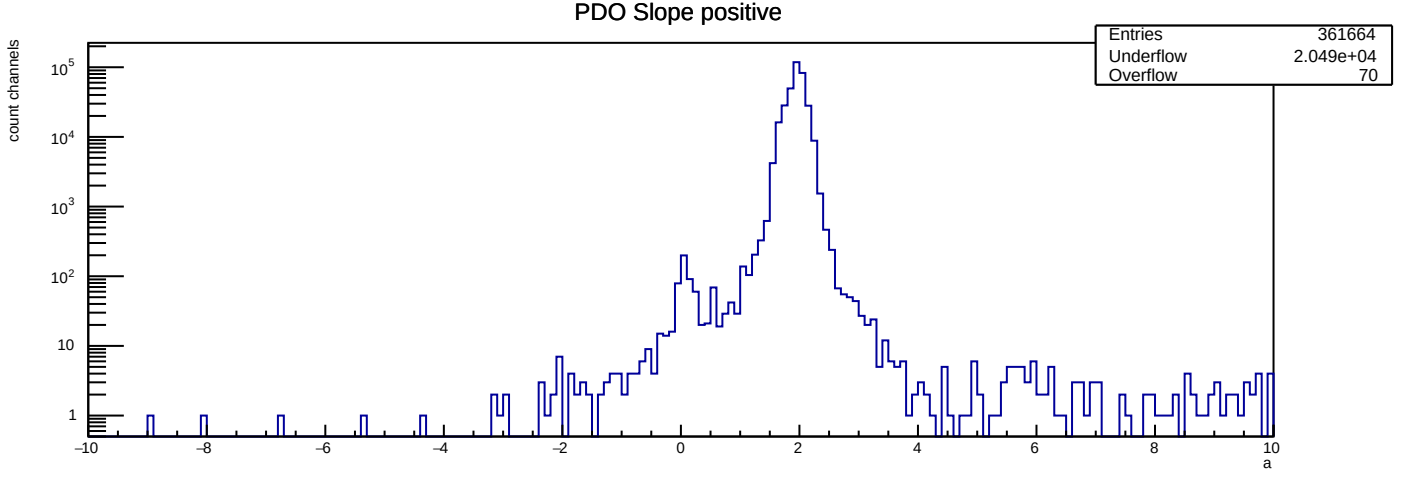

PDO RMS positive
Entries 361664
Underflow 0
Overflow 599
count channels
RMS

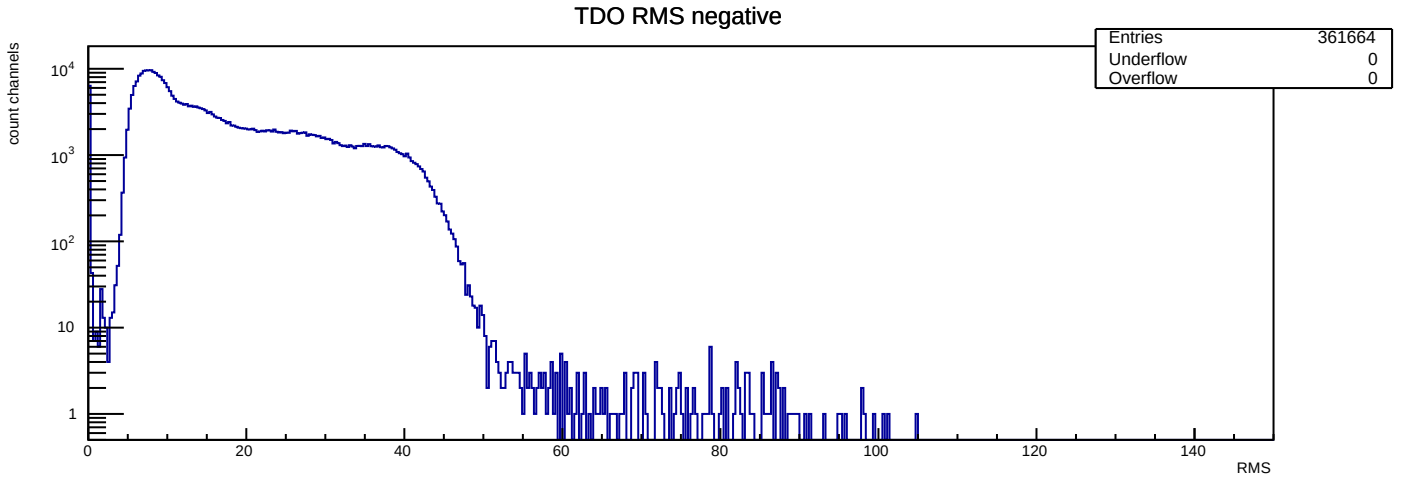

Baseline RMS
Entries 448576
Underflow 64
Overflow 3.305e+04
count channels
10^4
10^3
10^2
10
1
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
1.8
2
RMS

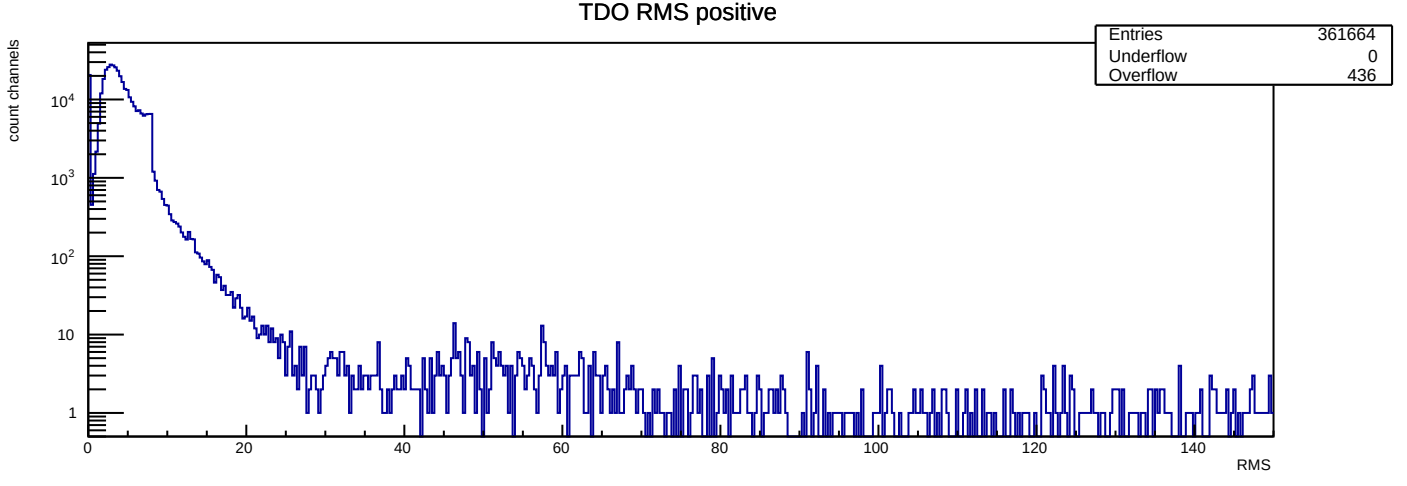

PDO Intercept negative
Entries 361664
Underflow 7472
Overflow 345
count channels
10^3
10^2
10
1
–200
–100
0
100
200
300
400
500
600
700
800
b

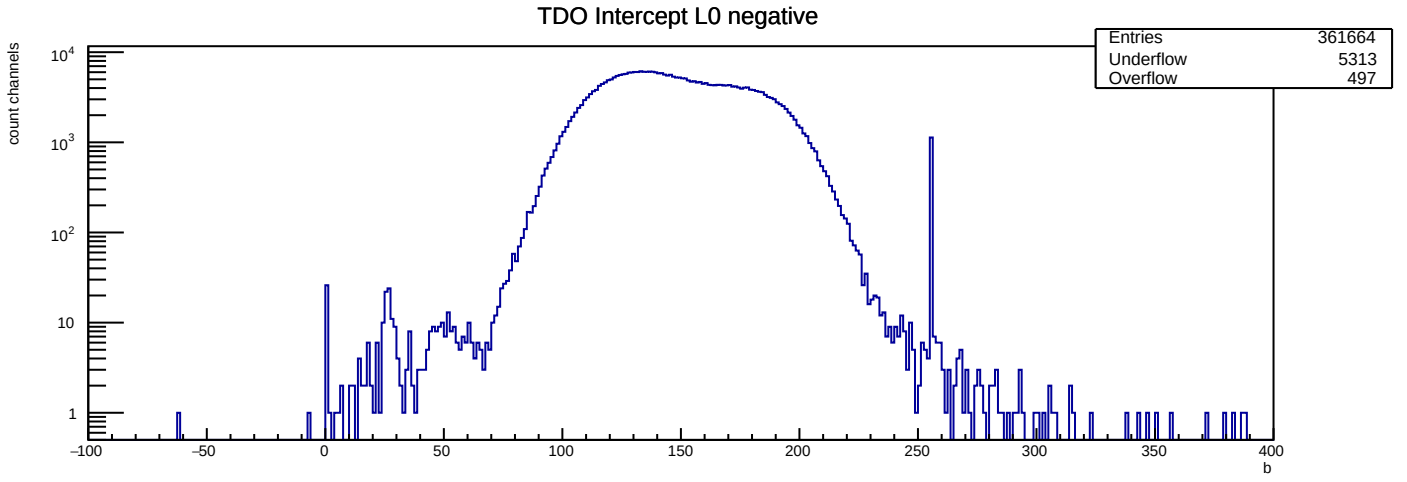

PDO Intercept positive
Entries 361664
Underflow 2.078e+04
Overflow 69
count channels
10^4
10^3
10^2
10
1
–200
–100
0
100
200
300
400
500
600
700
800
b

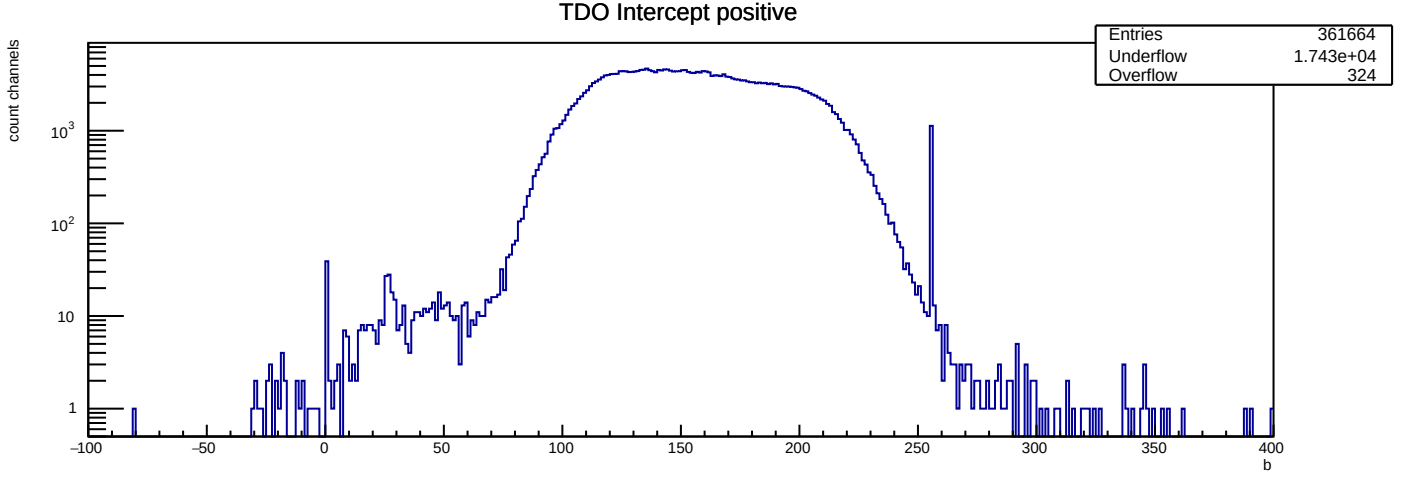

PDO Slope L0 negative
Entries 361664
Underflow 6652
Overflow 505
count channels
10^4
10^3
10^2
10
1
–10
–8
–6
–4
–2
0
2
4
6
8
10
a

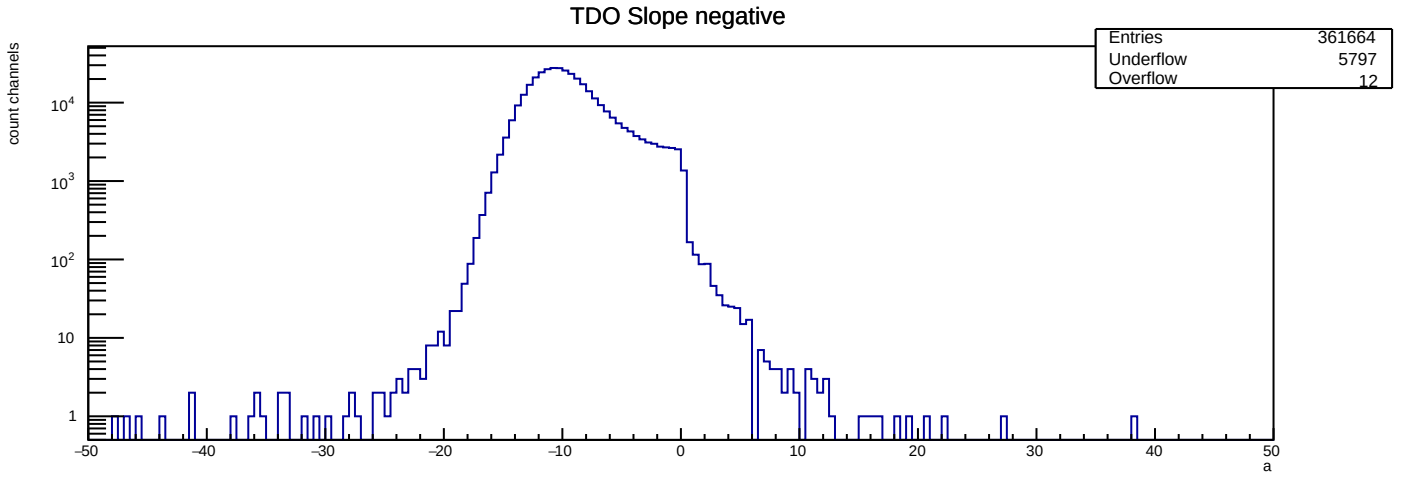

PDO Slope positive
Entries 361664
Underflow 2.049e+04
Overflow 70
count channels
10^5
10^4
10^3
10^2
10
1
–10
–8
–6
–4
–2
0
2
4
6
8
10
a

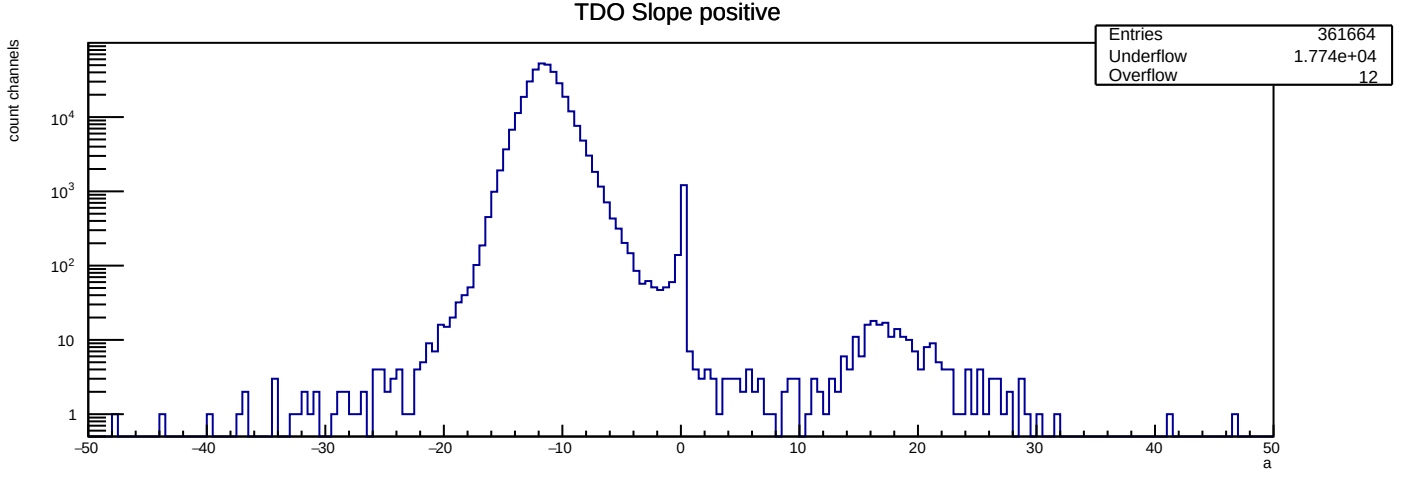

TDO RMS negative
Entries 361664
Underflow 0
Overflow 0
count channels
10^4
10^3
10^2
10
1
0
20
40
60
80
100
120
140
RMS


TDO RMS positive
Entries 361664
Underflow 0
Overflow 436
count channels
10^4
10^3
10^2
10
1
0
20
40
60
80
100
120
140
RMS


TDO Intercept L0 negative
Entries 361664
Underflow 5313
Overflow 497
count channels
b


TDO Intercept positive
Entries 361664
Underflow 1.743e+04
Overflow 324
count channels
b


TDO Slope negative
Entries 361664
Underflow 5797
Overflow 12
count channels
10^4
10^3
10^2
10
1
−50 −40 −30 −20 −10 0 10 20 30 40 50
a


TDO Slope positive
Entries 361664
Underflow 1.774e+04
Overflow 12
count channels
10^4
10^3
10^2
10
1
−50 −40 −30 −20 −10 0 10 20 30 40 50
a