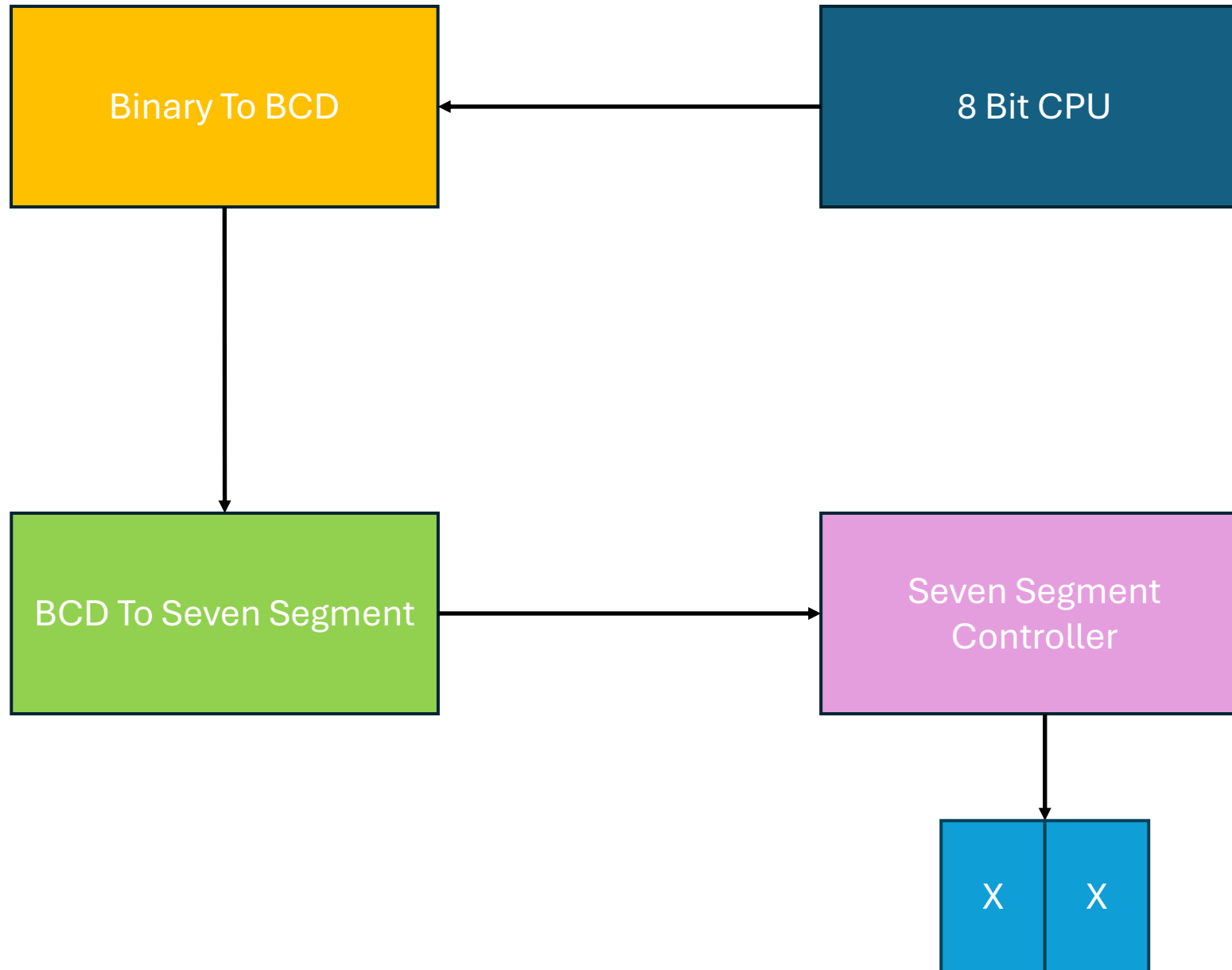
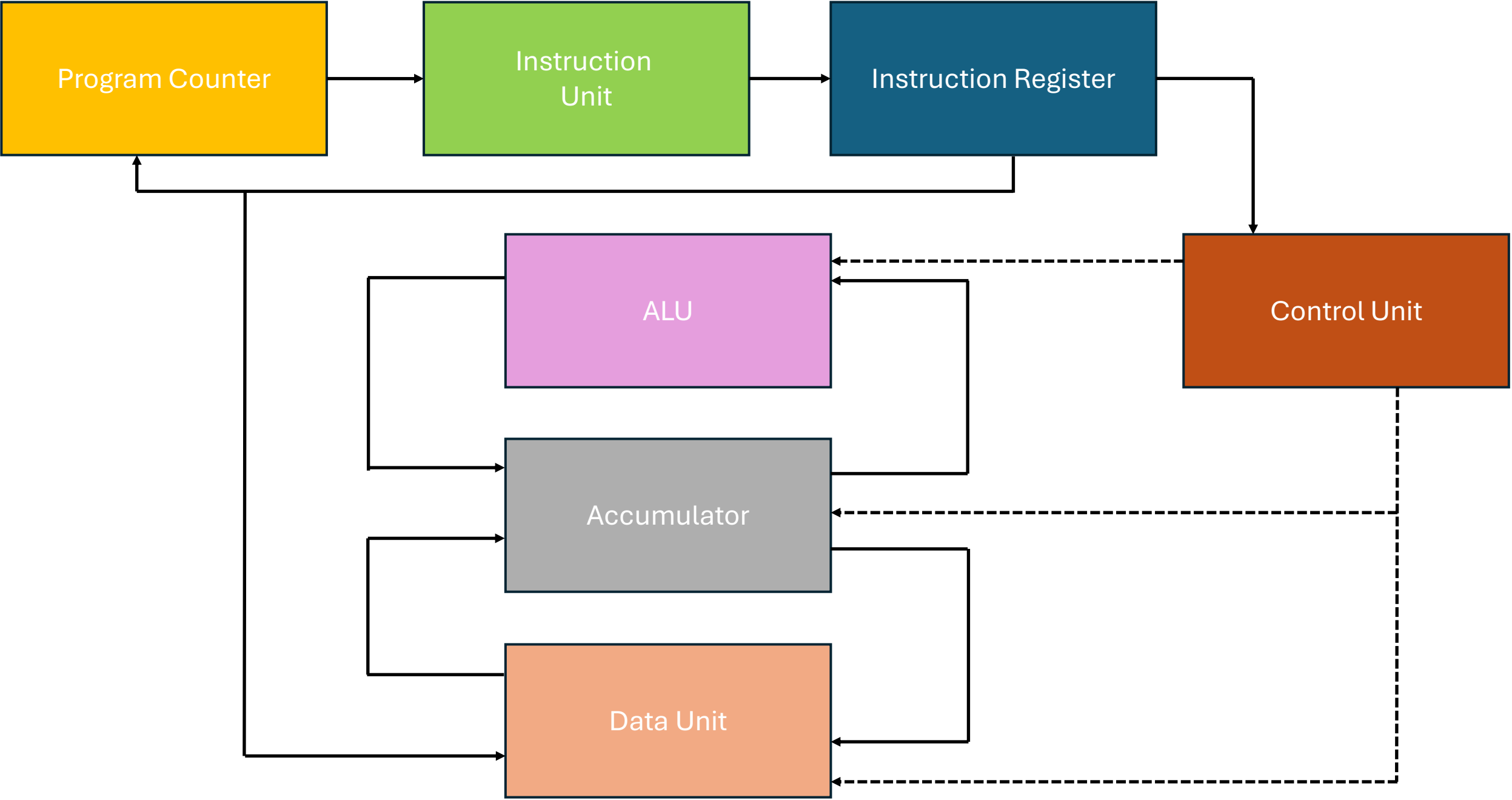
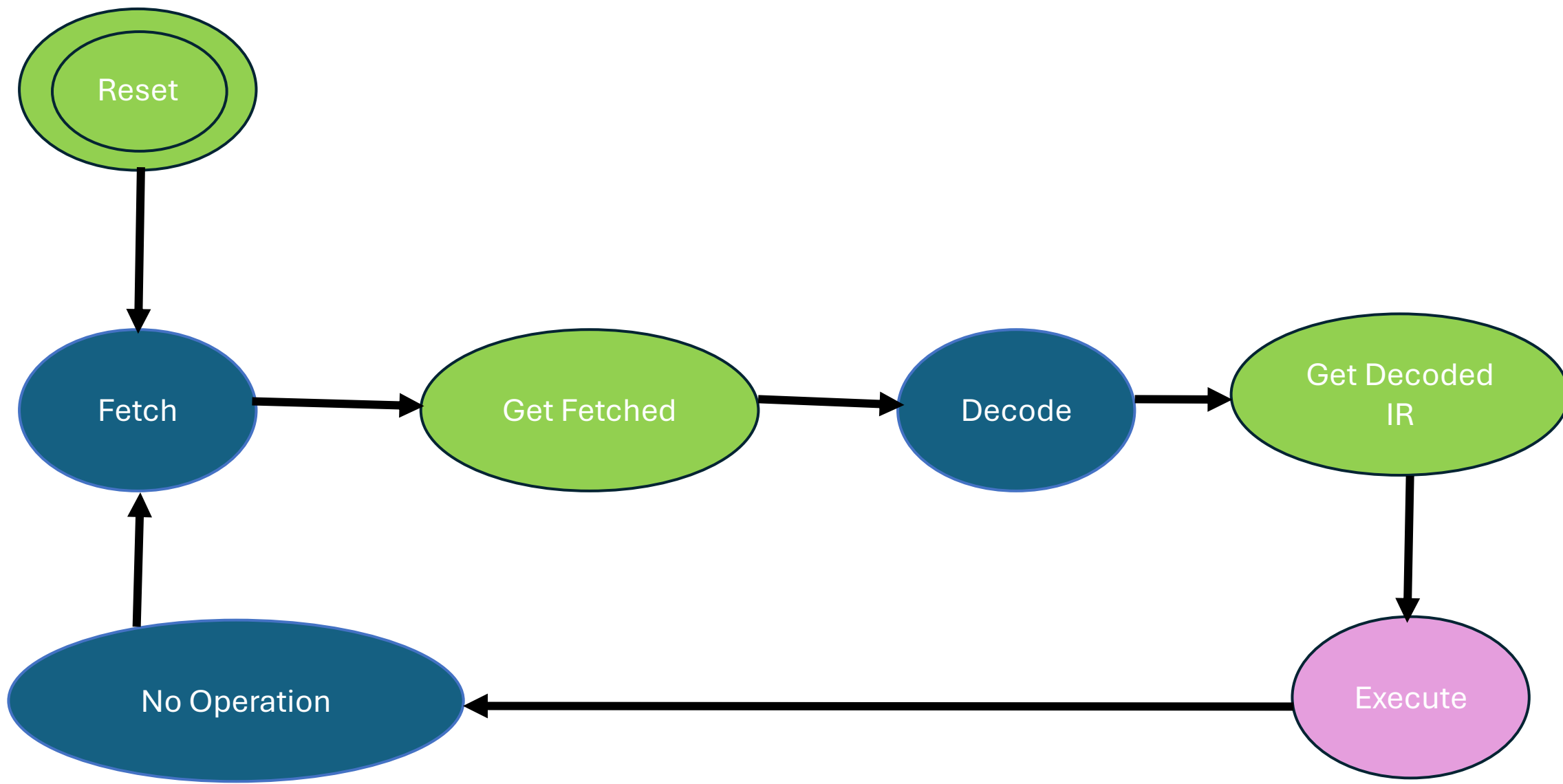


8 BIT Harvard CPU

- Hardware Engineering







| Instruction | OpCode |
|-----------------------|--------|
| LOAD | 100 |
| STORE | 001 |
| SUM | 010 |
| SUB | 011 |
| AND | 111 |
| OR | 101 |
| JUMP If No Carry Flag | 110 |
| No Operation | 000 |

Example with Testbench

CASE(pcAddress) IS

WHEN "00000000" => instruction<="00000000";

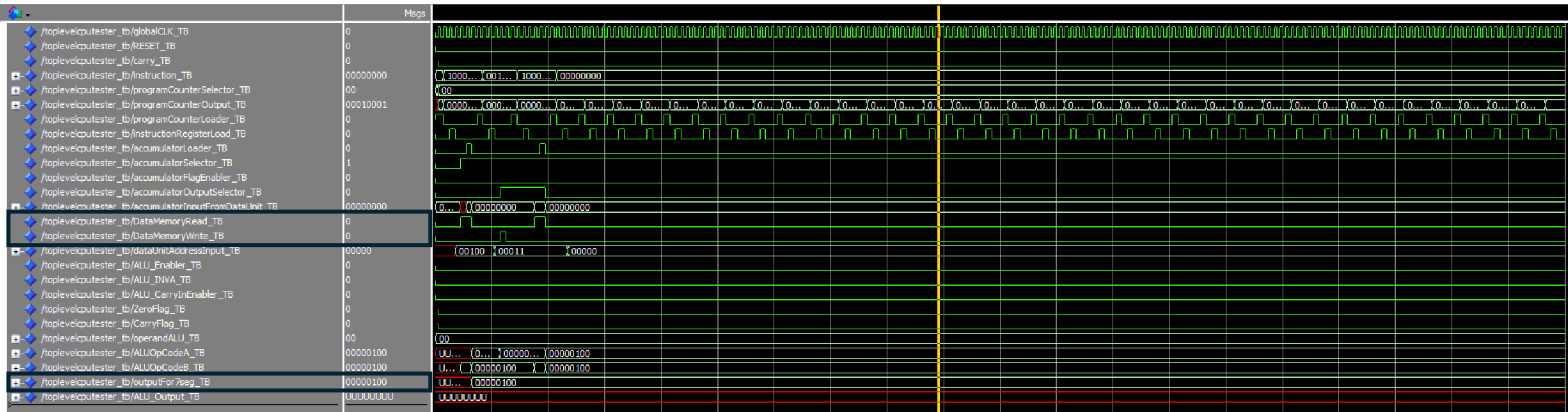
WHEN "00000001" => instruction<="10000100"; --Load

WHEN "00000010" => instruction<="00100011"; --Store

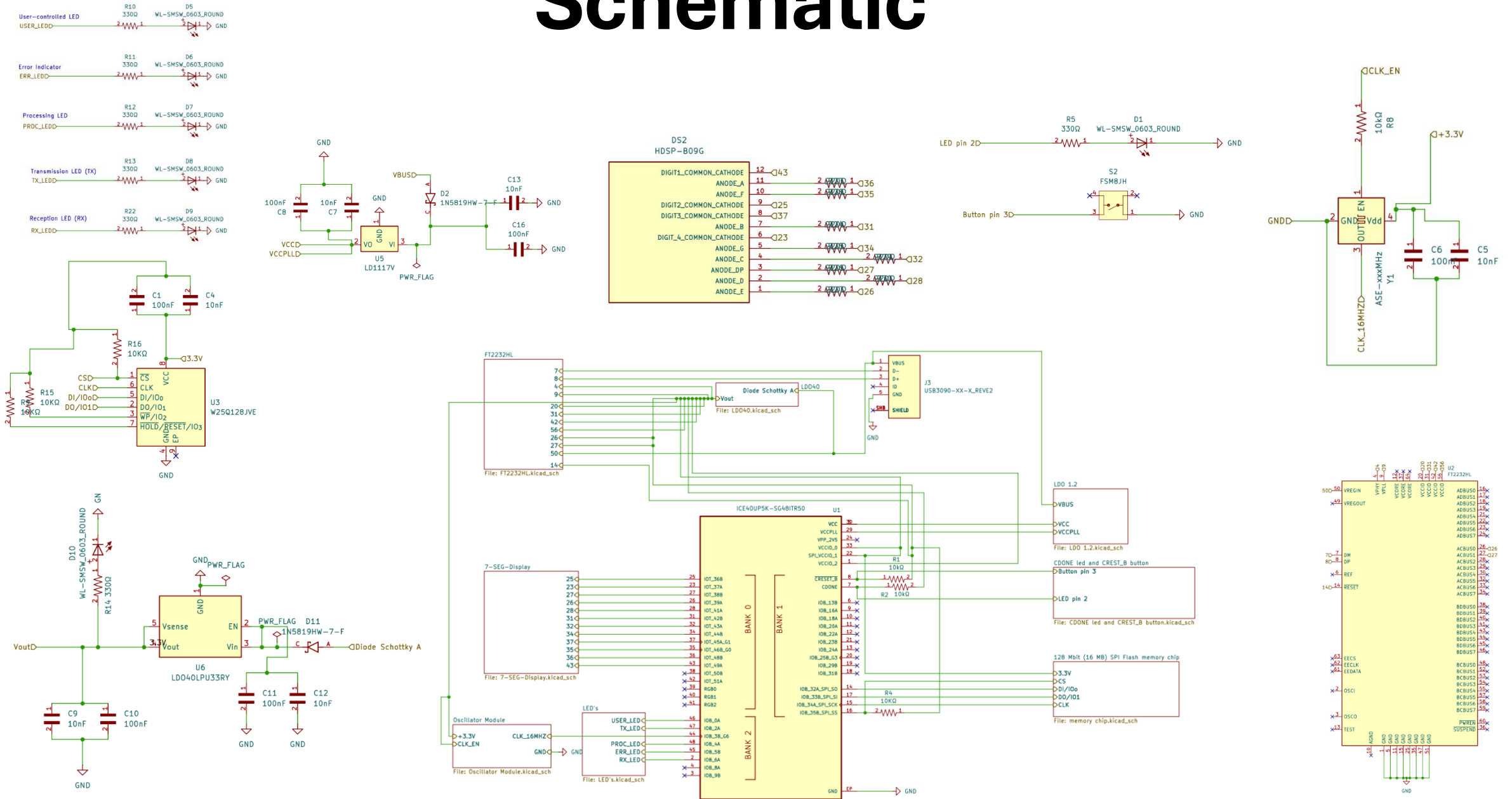
WHEN "00000011" => instruction<="10000011"; --Load

WHEN OTHERS => instruction <= "00000000"; -- No Operation

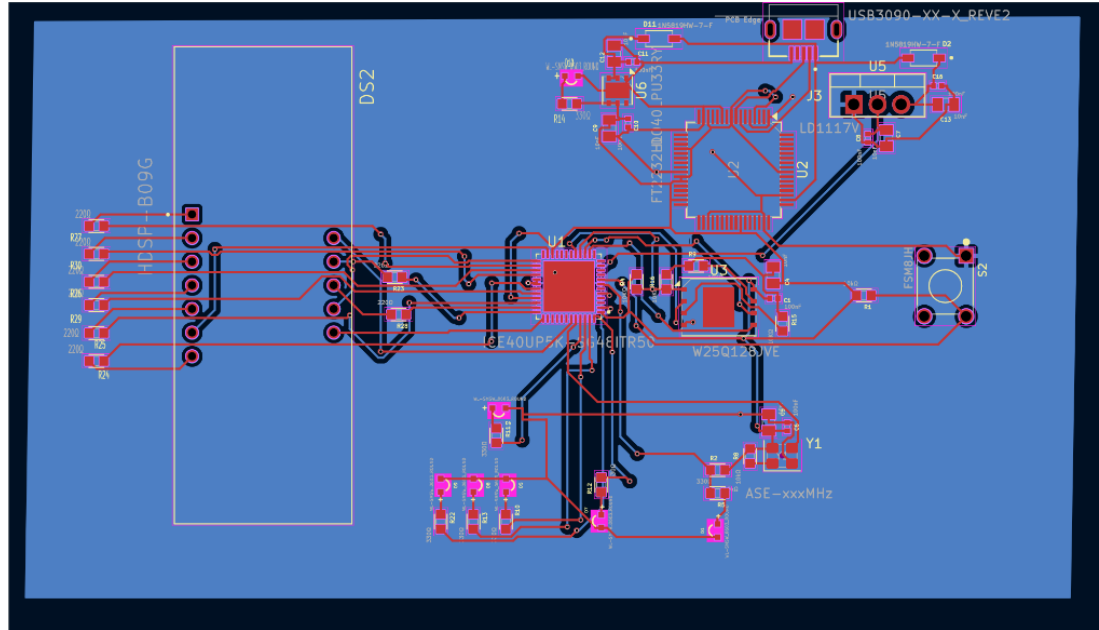
END CASE;



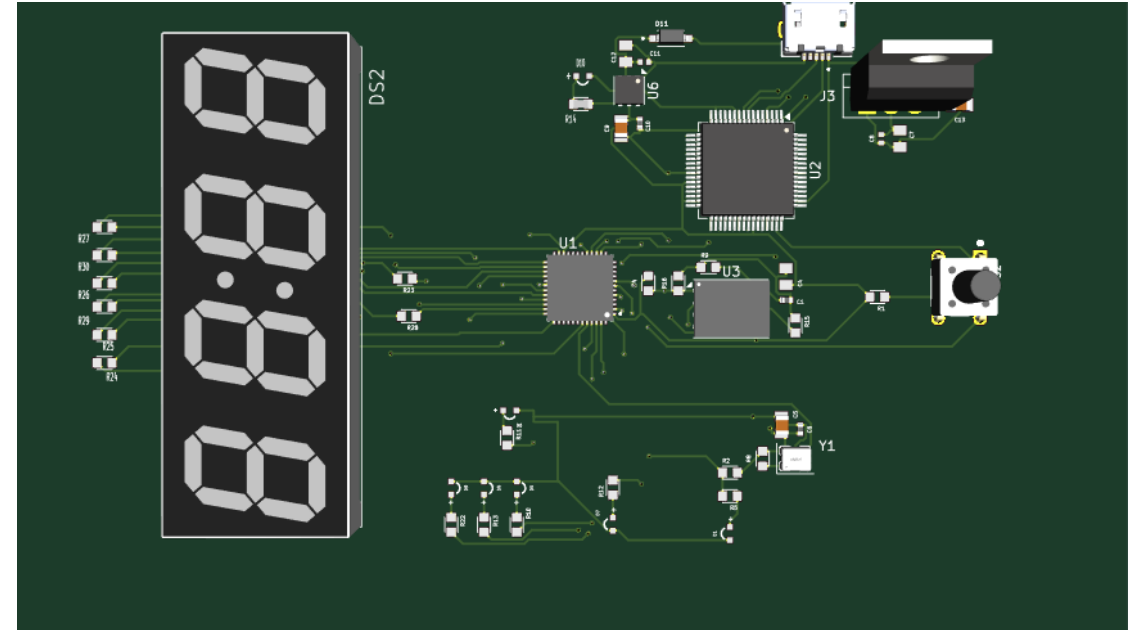
Schematic



LAYOUT



3D view



Physical Stackup

Copper layers: 2 ☐ Impedance controlled Add Dielectric Layer... Remove Dielectric Layer...

| Layer | Id | Type | Material | Thickness | Color | Epsilon R | Loss Tan |
|--------------|---------------------|---------------|----------|-----------|---------------|-----------|----------|
| F.Silkscreen | Top Silk Screen | Not specified | | | Not specified | | |
| F.Paste | Top Solder Paste | | | | | | |
| F.Mask | Top Solder Mask | Not specified | | 0.01 mm | Not specified | 3.3 | 0 |
| F.Cu | Copper | | | 0.035 mm | | | |
| Dielectric 1 | Core | FR4 | | 1.51 mm | Not specified | 4.5 | 0.02 |
| B.Cu | Copper | | | 0.035 mm | | | |
| B.Mask | Bottom Solder Mask | Not specified | | 0.01 mm | Not specified | 3.3 | 0 |
| B.Paste | Bottom Solder Paste | | | | | | |
| B.Silkscreen | Bottom Silk Screen | Not specified | | | Not specified | | |

Net Classes

| Netclasses | | | | | | | | | |
|------------|-----------|-------------|----------|----------|-----------|-----------|----------|---------|--|
| Name | Clearance | Track Width | Via Size | Via Hole | µVia Size | uVia Hole | DP Width | DP Gap | |
| SEG* | 0.17 mm | 0.25 mm | 0.6 mm | 0.3 mm | 0.3 mm | 0.1 mm | 0.2 mm | 0.25 mm | |
| DIGIT* | 0.17 mm | 0.25 mm | 0.6 mm | 0.3 mm | 0.3 mm | 0.1 mm | 0.2 mm | 0.25 mm | |
| 1.2 | 0.17 mm | 0.5 mm | 0.6 mm | 0.3 mm | 0.3 mm | 0.1 mm | 0.2 mm | 0.25 mm | |
| GPIO_* | 0.17 mm | 0.25 mm | 0.6 mm | 0.3 mm | 0.3 mm | 0.1 mm | 0.2 mm | 0.25 mm | |
| v* | 0.17 mm | 0.5 mm | 0.6 mm | 0.3 mm | 0.3 mm | 0.1 mm | 0.2 mm | 0.25 mm | |
| 3.3V | 0.17 mm | 0.5 mm | 0.6 mm | 0.3 mm | 0.3 mm | 0.1 mm | 0.2 mm | 0.25 mm | |
| Default | 0.17 mm | 0.25 mm | 0.6 mm | 0.3 mm | 0.3 mm | 0.1 mm | 0.2 mm | 0.25 mm | |

Constraints

Copper

Minimum clearance:

0.15

mm

Minimum track width:

0.2

mm

Minimum connection width:

0.15

mm

Minimum annular width:

0.1

mm

Minimum via diameter:

0.5

mm

Copper to hole clearance:

0.25

mm

Copper to edge clearance:

0.5

mm

Holes

Minimum through hole:

0.3

mm

Hole to hole clearance:

0.25

mm

uVias

Minimum uVia diameter:

0.2

mm

Minimum uVia hole:

0.1

mm

Silkscreen

Minimum item clearance:

0

mm

Arc/Circle Approximated by Segments

Maximum allowed deviation:

0.005

mm

Note: zone filling can be slow when < 0.005 mm.

Zone Fill Strategy

☐ Allow fillets/chamfers outside zone outline

Minimum thermal relief spoke count:

2

Length Tuning

☒ Include stackup height in track length calculations

ther Board...

OK

Cancel

Tools:

- Xilinx Vivado
- Modelsim
- KiCAD