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-- EXAM QUESTION 1 --
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LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;
USE ieee.std_logic_unsigned.ALL;

ENTITY data_flow IS
    PORT (
        clock : IN std_logic;
        reset : IN std_logic;
        x0, x1, x2, x3, x4, x5, x6, x7, x8, x9 : IN std_logic_vector(7 DOWNTO
0);
        h0, h1, h2, h3, h4, h5, h6, h7, h8, h9 : IN std_logic_vector(7 DOWNTO
0);
        y : OUT std_logic_vector(7 DOWNTO 0)
    );
END data_flow;
ARCHITECTURE arch OF data_flow IS
    SIGNAL temp_output : std_logic_vector(7 DOWNTO 0) := (OTHERS => '0');

    FUNCTION CALCULATE(x : std_logic_vector; h : std_logic_vector; sum : std_l
ogic_vector) RETURN std_logic_vector IS
        VARIABLE result : std_logic_vector(15 DOWNTO 0);
        VARIABLE x_in : std_logic_vector(7 DOWNTO 0);
        VARIABLE h_in : std_logic_vector(7 DOWNTO 0);
        VARIABLE sum_in : std_logic_vector(7 DOWNTO 0);
    BEGIN

        x_in := std_logic_vector(unsigned(x));
        h_in := std_logic_vector(unsigned(h));
        sum_in := std_logic_vector(unsigned(sum));
        result := sum_in + (x_in * h_in);

        RETURN std_logic_vector(result(7 DOWNTO 0));
    END FUNCTION CALCULATE;

BEGIN

    PROCESS (clock, reset)
    BEGIN
        IF (reset = '1') THEN
            temp_output <= (OTHERS => '0');
        ELSIF rising_edge(clock) THEN
            temp_output <= CALCULATE(x0, h0, temp_output);
            temp_output <= CALCULATE(x1, h1, temp_output);
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            temp_output <= CALCULATE(x2, h2, temp_output);
            temp_output <= CALCULATE(x3, h3, temp_output);
            temp_output <= CALCULATE(x4, h4, temp_output);
            temp_output <= CALCULATE(x5, h5, temp_output);
            temp_output <= CALCULATE(x6, h6, temp_output);
            temp_output <= CALCULATE(x7, h7, temp_output);
            temp_output <= CALCULATE(x8, h8, temp_output);
            temp_output <= CALCULATE(x9, h9, temp_output);
        END IF;
    END PROCESS;
    y <= temp_output;

END arch;
```