# EE-1193: Introduction to HDL ASSIGNMENTS

**CONTINUOUS EVALUATION CRITERION:**

**Equal weightage would be given to the following for each assignment:**

**1. Writing the HDL for the intended design, 2. Writing the Test Bench, 3. Simulation the design and the test bench**

1. **CLASS-ASSGN:** Design a system which receives 4-bit 8 data samples sequentially and output even sequenced data from the third data point onwards. Verify the design functionally by writing a test-bench at least for two sets of 4-bit 8 data samples. You need to simulate the entire design using the test bench.

2. **TAKE-HOME:** Design a system which receives 4-bit 8 data samples sequentially and output odd sequenced data from the fourth data point onwards. Verify the design functionally by writing a test-bench at least for two sets of 4-bit 8 data samples. You need to simulate the entire design using the test bench.

3. **CLASS-ASSGN:** Design a system which receives 16-bit data sequentially and output even and odd sequenced data from the fourth data point onwards. Verify the design functionally by writing a test-bench at least for two sets of 16-bit data. You need to simulate the entire design using the test bench.

4. **CLASS-ASSGN:** Compute $e^x$ for a 4-bit sequential data without using division (division architecture or repeated subtraction). Verify the design functionally by writing a test-bench. You need to simulate the entire design using the test bench.

5. **CLASS-ASSGN:** Compute $\sin x$ for a 16-bit sequential data without using division (division architecture or repeated subtraction). Verify the design functionally by writing a test-bench. You need to simulate the entire design using the test bench.

6. **TAKE-HOME:** Compute $\log_e$ (x) for a 16-bit sequential data without using division (division architecture or repeated subtraction). Verify the design functionally by writing a test-bench. You need to simulate the entire design using the test bench.