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--------------------------------------------------------------------------------
-- QUESTION 2 --
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LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;
USE ieee.std_logic_unsigned.ALL;

ENTITY select_odd IS
    PORT (
        clock : IN std_logic;
        reset : IN std_logic;
        input : IN std_logic_vector(3 DOWNTO 0);
        counter : OUT std_logic_vector(2 DOWNTO 0);
        output : OUT std_logic_vector(3 DOWNTO 0)
    );
END select_odd;

ARCHITECTURE arch OF select_odd IS
    SIGNAL t_count : std_logic_vector(2 DOWNTO 0);
    CONSTANT START_POINT : std_logic_vector(2 DOWNTO 0) := "100";

BEGIN

    PROCESS (clock, reset)
    BEGIN
        IF (reset = '1') THEN
            t_count <= "000";
        ELSIF rising_edge(clock) THEN
            t_count <= t_count + 1;
        END IF;
    END PROCESS;
    counter <= t_count;

    PROCESS (input)
    BEGIN
        IF (reset = '1') THEN
            output <= "0000";
        ELSIF (t_count(0) = '0' AND t_count >= START_POINT) THEN
            output <= input;
        ELSE
            output <= "0000";
        END IF;
    END PROCESS;
END arch;
```