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--------------------------------------------------------------------------------
-- TEST BENCH --
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LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.NUMERIC_STD.ALL;

ENTITY exponent_tb IS
END exponent_tb;

ARCHITECTURE Sequential OF exponent_tb IS

    COMPONENT exponent IS
        PORT (
            A : IN std_logic_vector(3 DOWNTO 0);
            S : OUT std_logic_vector(31 DOWNTO 0)
        );
    END COMPONENT;

    --Inputs
    SIGNAL A : std_logic_vector(3 DOWNTO 0);

    --Output
    SIGNAL S : std_logic_vector(31 DOWNTO 0);

BEGIN
    dut : exponent
    PORT MAP(
        A => A,
        S => S
    );

    -- Stimulus process
    stim_proc : PROCESS
    BEGIN
        A <= "0000";
        WAIT FOR 100 ns;
        A <= "0001";
        WAIT FOR 100 ns;
        A <= "0010";
        WAIT FOR 100 ns;
        A <= "0011";
        WAIT FOR 100 ns;
        A <= "0100";
        WAIT FOR 100 ns;
        A <= "0101";
        WAIT FOR 100 ns;
```

```
        A <= "0110";
        WAIT FOR 100 ns;
        A <= "0111";
        WAIT FOR 100 ns;
        A <= "1000";
        WAIT FOR 100 ns;
        A <= "1001";
        WAIT FOR 100 ns;
        A <= "1010";
        WAIT FOR 100 ns;
        A <= "1011";
        WAIT FOR 100 ns;
        A <= "1100";
        WAIT FOR 100 ns;
        A <= "1101";
        WAIT FOR 100 ns;
        A <= "1111";
        WAIT;
    END PROCESS;

END;
```