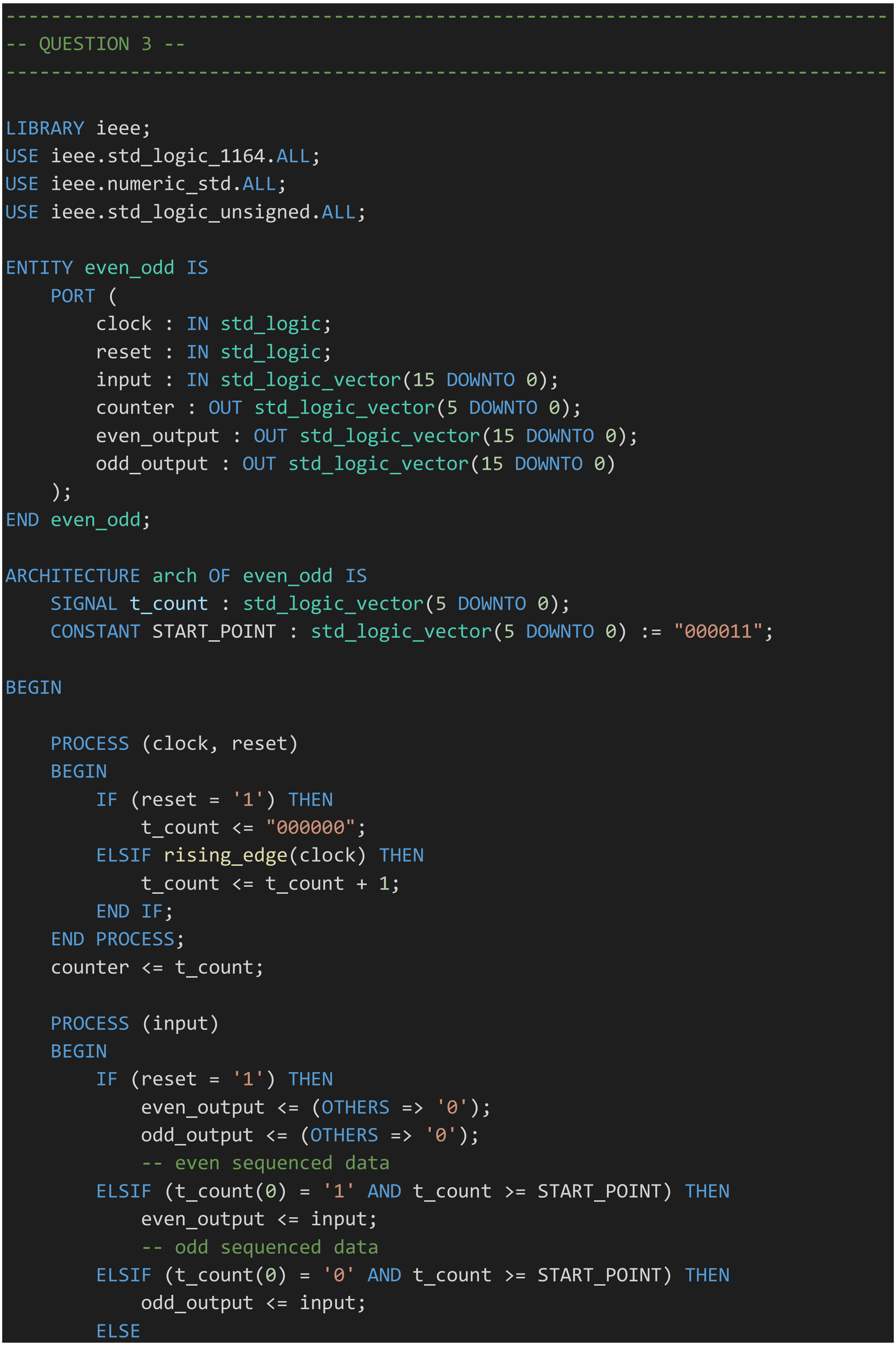

```
------------------------------------------------------------------------------
-- QUESTION 3 --
------------------------------------------------------------------------------

LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;
USE ieee.std_logic_unsigned.ALL;

ENTITY even_odd IS
    PORT (
        clock : IN std_logic;
        reset : IN std_logic;
        input : IN std_logic_vector(15 DOWNTO 0);
        counter : OUT std_logic_vector(5 DOWNTO 0);
        even_output : OUT std_logic_vector(15 DOWNTO 0);
        odd_output : OUT std_logic_vector(15 DOWNTO 0)
    );
END even_odd;

ARCHITECTURE arch OF even_odd IS
    SIGNAL t_count : std_logic_vector(5 DOWNTO 0);
    CONSTANT START_POINT : std_logic_vector(5 DOWNTO 0) := "000011";

BEGIN

    PROCESS (clock, reset)
    BEGIN
        IF (reset = '1') THEN
            t_count <= "000000";
        ELSIF rising_edge(clock) THEN
            t_count <= t_count + 1;
        END IF;
    END PROCESS;
    counter <= t_count;

    PROCESS (input)
    BEGIN
        IF (reset = '1') THEN
            even_output <= (OTHERS => '0');
            odd_output <= (OTHERS => '0');
            -- even sequenced data
        ELSIF (t_count(0) = '1' AND t_count >= START_POINT) THEN
            even_output <= input;
            -- odd sequenced data
        ELSIF (t_count(0) = '0' AND t_count >= START_POINT) THEN
            odd_output <= input;
        ELSE
```

```vhdl
            even_output <= (OTHERS => '0');
            odd_output <= (OTHERS => '0');
        END IF;
    END PROCESS;
END arch;
```