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--------------------------------------------------------------------------------
-- TEST BENCH --
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LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.numeric_std.ALL;
USE ieee.std_logic_unsigned.ALL;

ENTITY even_odd_tb IS
END even_odd_tb;

ARCHITECTURE tb_arch OF even_odd_tb IS

    COMPONENT even_odd
        PORT (
            clock : IN std_logic;
            reset : IN std_logic;
            input : IN std_logic_vector(15 DOWNTO 0);
            counter : OUT std_logic_vector(5 DOWNTO 0);
            even_output : OUT std_logic_vector(15 DOWNTO 0);
            odd_output : OUT std_logic_vector(15 DOWNTO 0)
        );
    END COMPONENT;

    --Inputs
    SIGNAL clock : std_logic := '0';
    SIGNAL reset : std_logic := '0';
    SIGNAL input : std_logic_vector (15 DOWNTO 0);

    --Outputs
    SIGNAL counter : std_logic_vector(5 DOWNTO 0);
    SIGNAL even_output : std_logic_vector(15 DOWNTO 0);
    SIGNAL odd_output : std_logic_vector(15 DOWNTO 0);

    -- Clock period definitions
    CONSTANT clock_period : TIME := 100 ns;

BEGIN

    -- Instantiate the Design Under Test (DUT)
    dut : even_odd
    PORT MAP
    (
        clock => clock,
        reset => reset,
        input => input,
        counter => counter,
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        even_output => even_output,
        odd_output => odd_output
    );

    -- Clock process definitions
    clock_process : PROCESS
    BEGIN
        clock <= '1';
        WAIT FOR clock_period/2;
        clock <= '0';
        WAIT FOR clock_period/2;
    END PROCESS;

    -- Stimulus process
    stim_proc : PROCESS
    BEGIN
        reset <= '1';
        WAIT FOR clock_period * 2;

        -- Data set 1
        reset <= '0';
        input <= "0100000000000000";
        WAIT FOR clock_period;
        input <= "0000000000011100";
        WAIT FOR clock_period;
        input <= "0100001000001111";
        WAIT FOR clock_period;
        input <= "0000000000000000";
        WAIT FOR clock_period;
        input <= "0000000000000001";
        WAIT FOR clock_period;
        input <= "0000000000011111";
        WAIT FOR clock_period;
        input <= "0000000000010011";
        WAIT FOR clock_period;
        input <= "0000000001000000";
        WAIT FOR clock_period;
        input <= "0000000000000111";
        WAIT FOR clock_period;
        input <= "0000000000000011";
        WAIT FOR clock_period;
        input <= "0000000000010011";
        WAIT FOR clock_period;
        input <= "0000000000000001";
        WAIT FOR clock_period;
        reset <= '1';
        WAIT FOR clock_period;
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        -- Data set 2
        reset <= '0';
        input <= "0100000000000000";
        WAIT FOR clock_period;
        input <= "0000000000000000";
        WAIT FOR clock_period;
        input <= "0100001000000001";
        WAIT FOR clock_period;
        input <= "1000000000000000";
        WAIT FOR clock_period;
        input <= "0000000000000001";
        WAIT FOR clock_period;
        input <= "0000000000010000";
        WAIT FOR clock_period;
        input <= "0011111111000000";
        WAIT FOR clock_period;
        input <= "0000001000000111";
        WAIT FOR clock_period;
        input <= "0011100000010011";
        WAIT FOR clock_period;
        input <= "0000000000011101";
        WAIT FOR clock_period;
        reset <= '1';
        WAIT;

    END PROCESS;

END;
```