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-- TEST BENCH --  
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LIBRARY ieee;  
USE ieee.std_logic_1164.ALL;  
USE ieee.numeric_std.ALL;  
USE ieee.std_logic_unsigned.ALL;  
  
ENTITY select_even_tb IS  
END select_even_tb;  
  
ARCHITECTURE tb_arch OF select_even_tb IS  
  
    COMPONENT select_even  
        PORT (  
            clock : IN std_logic;  
            reset : IN std_logic;  
            input : IN std_logic_vector(3 DOWNTO 0);  
            counter : OUT std_logic_vector(2 DOWNTO 0);  
            output : OUT std_logic_vector(3 DOWNTO 0)  
        );  
    END COMPONENT;  
  
    --Inputs  
    SIGNAL clock : std_logic := '1';  
    SIGNAL reset : std_logic := '1';  
    SIGNAL input : std_logic_vector (3 DOWNTO 0);  
  
    --Outputs  
    SIGNAL counter : std_logic_vector(2 DOWNTO 0);  
    SIGNAL output : std_logic_vector(3 DOWNTO 0);  
    -- Clock period definitions  
    CONSTANT clock_period : TIME := 100 ns;  
  
BEGIN  
  
    -- Instantiate the Design Under Test (DUT)  
    dut : select_even  
    PORT MAP  
    (  
        clock => clock,  
        reset => reset,  
        input => input,  
        counter => counter,  
        output => output  
    );
```

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-- Clock process definitions
clock_process : PROCESS
BEGIN
    clock <= '1';
    WAIT FOR clock_period/2;
    clock <= '0';
    WAIT FOR clock_period/2;
END PROCESS;

-- Stimulus process
stim_proc : PROCESS
BEGIN
    reset <= '1';
    WAIT FOR clock_period;

    -- Data set 1
    reset <= '0';
    input <= "1000";
    WAIT FOR clock_period;
    input <= "0001";
    WAIT FOR clock_period;
    input <= "0010";
    WAIT FOR clock_period;
    input <= "0011";
    WAIT FOR clock_period;
    input <= "0100";
    WAIT FOR clock_period;
    input <= "0101";
    WAIT FOR clock_period;
    input <= "0110";
    WAIT FOR clock_period;
    input <= "0111";
    WAIT FOR clock_period;
    reset <= '1';
    WAIT FOR clock_period;

    -- Data set 2
    reset <= '0';
    input <= "1000";
    WAIT FOR clock_period;
    input <= "0011";
    WAIT FOR clock_period;
    input <= "1010";
    WAIT FOR clock_period;
    input <= "1011";
    WAIT FOR clock_period;
    input <= "0110";
    WAIT FOR clock_period;

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    input <= "0001";  
    WAIT FOR clock_period;  
    input <= "0100";  
    WAIT FOR clock_period;  
    input <= "1111";  
    WAIT FOR clock_period;  
    reset <= '1';  
  
    WAIT;  
END PROCESS;  
  
END;
```