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----------------------------------------------------------------------------------
-- TEST BENCH --
----------------------------------------------------------------------------------
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
USE IEEE.NUMERIC_STD.ALL;

-- Input 16 bit signal is a fixed point number of the form:
-- 00.00000000000000
-- 2 bits before decimal: Integral part
-- 14 bits after decimal: Fractional part

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- NOTE: the input range lies in [0, 2] due to the nature of ln(x)'s taylor exp
ansions

ENTITY log_tb IS
END log_tb;

ARCHITECTURE Sequential OF log_tb IS

    COMPONENT log IS
        PORT (
            A : IN std_logic_vector(15 DOWNTO 0);
            S : OUT std_logic_vector(31 DOWNTO 0)
        );
    END COMPONENT;

    --Input
    SIGNAL A : std_logic_vector(15 DOWNTO 0);

    --Output
    SIGNAL S : std_logic_vector(31 DOWNTO 0);

BEGIN
    dut : log
    PORT MAP(
        A => A,
        S => S
    );

    -- Stimulus process
    stim_proc : PROCESS
    BEGIN
        A <= "0001000000000000"; -- 0.25
        WAIT FOR 100 ns;
        A <= "0010000000000000"; -- 0.5
        WAIT FOR 100 ns;
```

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        A <= "0011000000000000"; -- 0.75
        WAIT FOR 100 ns;
        A <= "0100000000000000"; -- 1
        WAIT FOR 100 ns;
        A <= "0101000000000000"; -- 1.25
        WAIT FOR 100 ns;
        A <= "0110000000000000"; -- 1.5
        WAIT FOR 100 ns;
        A <= "0111000000000000"; -- 1.75
        WAIT FOR 100 ns;
        A <= "1000000000000000"; -- 2
        WAIT;
    END PROCESS;

END;
```