

```
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-- QUESTION 2 TEST BENCH --  
-----
```

```
LIBRARY ieee;  
USE ieee.std_logic_1164.ALL;  
USE ieee.numeric_std.ALL;  
USE ieee.std_logic_unsigned.ALL;
```

```
ENTITY control_flow_tb IS  
END control_flow_tb;
```

```
ARCHITECTURE tb_arch OF control_flow_tb IS
```

```
    COMPONENT control_flow  
        PORT (  
            clock : IN std_logic;  
            reset : IN std_logic;  
            x0, x1, x2, x3, x4, x5, x6, x7, x8, x9 : IN std_logic_vector(7 DOWNTO 0);  
            h0, h1, h2, h3, h4, h5, h6, h7, h8, h9 : IN std_logic_vector(7 DOWNTO 0);  
            y : OUT std_logic_vector(7 DOWNTO 0)  
        );  
    END COMPONENT;
```

```
    --Inputs  
    SIGNAL clock : std_logic := '1';  
    SIGNAL reset : std_logic := '1';  
    SIGNAL x0, x1, x2, x3, x4, x5, x6, x7, x8, x9 : std_logic_vector (7 DOWNTO 0);  
    SIGNAL h0, h1, h2, h3, h4, h5, h6, h7, h8, h9 : std_logic_vector (7 DOWNTO 0);
```

```
    --Outputs  
    SIGNAL y : std_logic_vector(7 DOWNTO 0);
```

```
    -- Clock period definitions  
    CONSTANT clock_period : TIME := 100 ns;
```

```
BEGIN
```

```
    -- Instantiate the Design Under Test (DUT)  
    dut : control_flow  
    PORT MAP  
    (  
        clock,  
        reset,
```

```
    x0, x1, x2, x3, x4, x5, x6, x7, x8, x9,  
    h0, h1, h2, h3, h4, h5, h6, h7, h8, h9,  
    y  
);
```

```
-- Clock process definitions
```

```
clock_process : PROCESS  
BEGIN  
    clock <= '1';  
    WAIT FOR clock_period/2;  
    clock <= '0';  
    WAIT FOR clock_period/2;  
END PROCESS;
```

```
-- Stimulus process
```

```
stim_proc : PROCESS  
BEGIN  
    reset <= '1';  
    WAIT FOR clock_period;
```

```
    -- Data set 1
```

```
    reset <= '0';  
    x0 <= "00000000";  
    x1 <= "00000001";  
    x2 <= "00000010";  
    x3 <= "00000011";  
    x4 <= "00000100";  
    x5 <= "00000101";  
    x6 <= "00000110";  
    x7 <= "00000111";  
    x8 <= "00001000";  
    x9 <= "00001001";
```

```
    h0 <= "00000001";  
    h1 <= "00000001";  
    h2 <= "00000001";  
    h3 <= "00000001";  
    h4 <= "00000001";  
    h5 <= "00000001";  
    h6 <= "00000001";  
    h7 <= "00000001";  
    h8 <= "00000001";  
    h9 <= "00000001";
```

```
    WAIT FOR clock_period;  
    reset <= '1';  
    WAIT;  
END PROCESS;
```

END;