REGISTER (CPU)

ADDRESS : 4200H
NAME   : NMITIMEN
CONTENTS : ENABLE FLAG FOR V-BLANK. TIMER INTERRUPT & JOY CONTROLLER READ

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
NM I Enable		TIMER ENABLE V-EN	H-EN					JOY-C ENABLE

4 2 0 0 H

└─ JOY CONTROLLER ENABLE
  ┌ 0 : Disable Automatic reading of the Joy Controller
  └ 1 : Enable Automatic reading of the Joy Controller

※ Reading the data can be started at the beginning of V-Blank period, but
  it takes about for 3 or 4 scanning period until completion of reading.

└─ TIMER ENABLE
  ┌ V-EN : V-COUNT TIMER ENABLE
  └ H-EN : H-COUNT TIMER ENABLE

H EN	V EN	FUNCTION
0	0	Disable BOTH H & V
0	1	Enable H only. IRQ is applied by H-count timer value designated.
1	0	Enable V only. IRQ is applied by V-count timer value designated.
1	1	Enable both H & V. IRQ is applied by both H and V count timer value designated.

└─ NMI ENABLE : Enable NMI at the point when V-blank begins
    (When power is turned on or the reset signal is applied. it will be "0".)

  ┌ 0 : NMI DISABLE
  └ 1 : NMI ENABLE

ADDRESS : 4201H
NAME   : WRIO
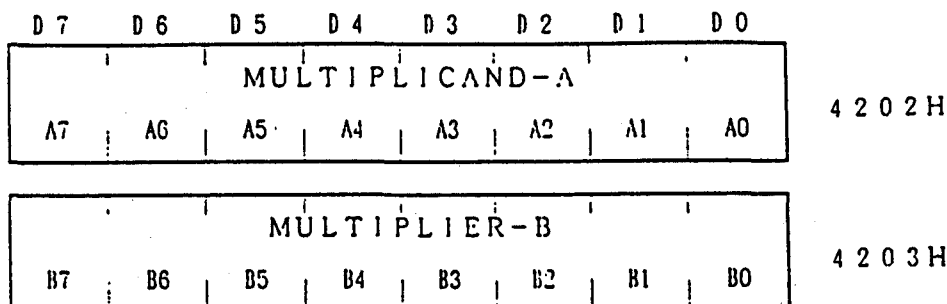CONTENTS : PROGRAMABLE I/C PORT (OUT-PORT)

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
			I/O PORT				
D7	D6	D5	D4	D3	D2	D1	D0

4 2 0 1 H

• This is a Programable I/O port (OUT-PORT). The written data will be output directly from the
   OUT-PORT.

• When this is used as a INPORT. "1" should be written to the particular bit which will be used
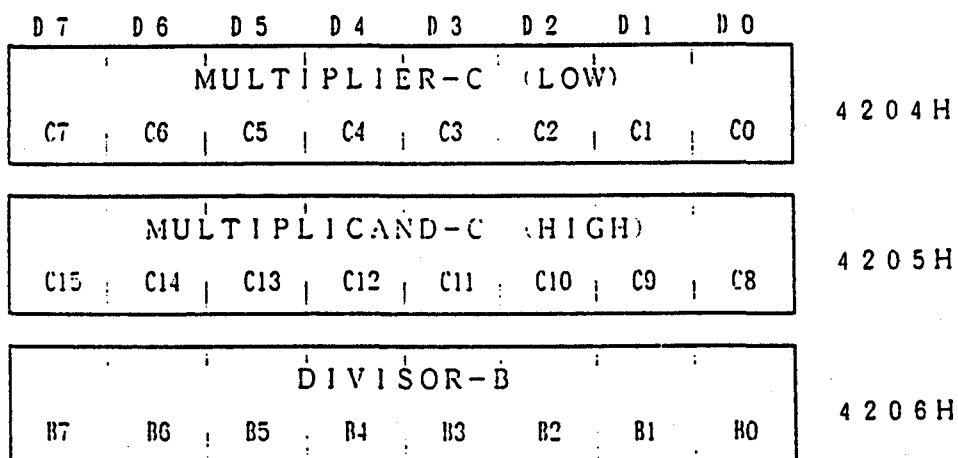   as a IN-PORT. The input data can be read by register <4213H>.

ADDRESS : 4202H / 4203H
NAME : WRMPYA / WRMPYB
CONTENTS : MULTIPLIER & MULTIPLICAND BY MULTIPLICATION

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
MULTIPLICAND-A								4 2 0 2 H
A7	A6	A5	A4	A3	A2	A1	A0	

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
MULTIPLIER-B								4 2 0 3 H
B7	B6	B5	B4	B3	B2	B1	B0	

- This is a register, which can set a Multiplicand (A) and a multiplier (B) for Absolute Multiplication of A (8-BIT) $\times$ B (8-BIT) = C (16-BIT)

- A PRODUCT (C) can be read by registers <4216H><4217H>.

- Set in the order of (A) and (B). The operation will start as soon as (B) has been set, and it will be completed right after 8-machine cycle period.

- Once the data of the A-REGISTER is set, it will not be destoroyed until new data is set.

ADDRESS : 4204H / 4205H / 4206H
NAME : WRDIVL / WRDIVH / WRDIVB
CONTENTS : DIVISOR & DIVIDEND BY DIVIDE

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
MULTIPLIER-C (LOW)								4 2 0 4 H
C7	C6	C5	C4	C3	C2	C1	C0	

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
MULTIPLICAND-C (HIGH)								4 2 0 5 H
C15	C14	C13	C12	C11	C10	C9	C8	

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
DIVISOR-B								4 2 0 6 H
B7	B6	B5	B4	B3	B2	B1	B0	

- This is a register, which can set a Dividend (C) and a Divisor (B) for Absolute Divide of C (16-BIT) $\div$ B (8-BIT) = A (16-BIT)

- The divisor (A) can be read by registers <4214H><4215H>. And the remainder can also be read by registers <4216H><4217H>.

- Set in the order of (C) and (B). The operation will start as soon as (B) has been set, and it will be completed right after 16-machine cycle period.

- Once the data of the A-REGISTER is set, it will not be destoroyed until new data is set.
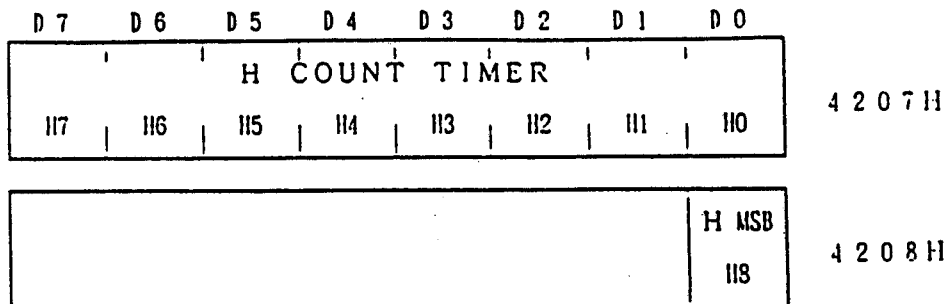
ADDRESS : 4207H / 4208H
NAME   : HTIMEL / HTIMEH
CONTENTS : H-COUNT TIMER SETTINGS

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
			H COUNT TIMER					
H7	H6	H5	H4	H3	H2	H1	H0	4207H

							H MSB	
							H8	4208H

· This is a register, which can set the H-COUNT TIMER value.

· The setting value should be from 0 through 339, which is counted from the far left on the screen.

· When the coordinate counter becomes the count value set, the IRQ will be applied.
  And at the same time, "1" will be written to "timer IRQ" of register <4211H>. READ RESET:
  Enable/Disable of the interrupt will be determined by setting register <4200H>.

※ This countinuous counter is reset every scanning line, therefore once the count value is set,
  it is possible to apply the IRQ every time the scanning line comes to the same horizontal
  position on the screen.

ADDRESS : 4209H /420AH
NAME   : VTIMEL / VTIMEH
CONTENTS : V-COUNT TIMER SETTINGS

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
			V-COUNT TIMER					
V7	V6	V5	V4	V3	V2	V1	V0	4209H

							V MSB	
							V8	420AH
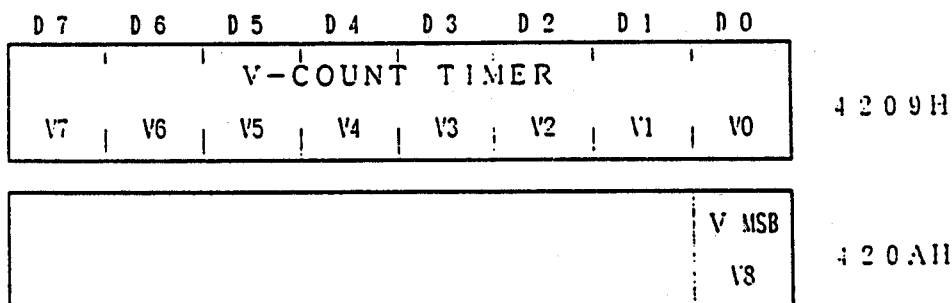
· This is a register, which can set the V-COUNT TIMER value.

  The setting value should be from 0 through 261(262), which is counted from the far top on the screen.
  [This line number described is different from the actual line number on the screen.]

· When the coordinate counter becomes the count value set, the IRQ will be applied.
  And at the same time, "1" will be written to "timer IRQ" of register <4211H>. READ RESET:
  Enable/Disable of the interrupt will be determined by setting register <4200H>.

※ This is a countinuous counter same as H-counter, and it will be reset every time 262(263) lines
  are scanned. Once the count value is set, it is possible to apply the IRQ every time the scanning
  line comes to the same vertical line on the screen.

ADDRESS : 420BH
NAME : MDMAEN
CONTENTS : CHANNEL DESIGNATION FOR GENERAL PURPOSE DMA & TRIGGER (START)

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
GENERAL PURPOSE DMA ENABLE FLAG							
CH7 EN	CH6 EN	CH5 EN	CH4 EN	CH3 EN	CH2 EN	CH1 EN	CH0 EN

4 2 0 B H

- The General purpose DMA consists of 8-channels in total (CH0～CH7).

- This register is used to designate the channel out of 8-channels (8-channels maximum).

- The channel which should be used can be designated by writing "1" to the bit of this channel.
  As soon as "1" is written to the bit (after a few cycles passed), the general purpose DMA transfer will be started.

- When the general purpose DMA of the designated channel is completed, the flag will be cleared.

NOTE : Because the data area (register <4300H> ～) of each channel is held in common with the data of each H-DMA channel, the channel designated by the H-DMA channel designation register <420CH> can not be used.
(It is prohibited to write "1" to the bit of the channel)
Therefore, 8-channels (CH0～CH7) should be assigned by the H-DMA and the general purpose DMA.

NOTE : If the H-Blank comes during the operation of the general purpose DMA and the H-DMA is started, the general purpose DMA will be discontinued in the middle, and re-started right after the H-DMA is complete.

NOTE : If 2 or more channels are designated, the DMA transfer will be performed continuously according to the priority order described by Appendix-1.
And also, the CPU stops operation until all the general purpose DMA are completed.

ADDRESS : 420CH
NAME : HDMAEN
CONTENTS : CHANNEL DESIGNATION FOR H-DMA

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
H-DMA ENABLE FLAG							
CH7 EN	CH6 EN	CH5 EN	CH4 EN	CH3 EN	CH2 EN	CH1 EN	CH0 EN

4 2 0 C H

- The H-DMA consists of 8-channels in total (CH0～CH7).

- This register is used to designate the channel out of 8-channels (8-channels maximum).

- The channel which should be used can be designated by writing "1" to the bit of this channel.
  As soon as H-Blank begins (after a few cycles passed), the H-DMA transfer will be started.

NOTE : Once this flag is set, it will not be destroyed (cleared) until new data is set.
Therefore, the initial settings are done automatically every field, and the same transfer pattern will be repeated.
And also, the flag is set out of V-BLANK period, the DMA transfer will be performed properly from next screen frame.

ADDRESS : 420DH
NAME : MEMSEL
CONTENTS : ACCESS CYCLE DESIGNATION IN MEMORY ② AREA

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
							2. 68 / 3. 58	4 2 0 D H

ACCESS CYCLE DESIGNATION IN MEMORY② AREA

       0 : 2. 68MHz access cycle

       1 : 3. 58MHz access cycle (Only when the high speed memory is used)

- MEMORY ② shows the address (8000H ～ FFFFH) of the bank (80H～ BFH) and all the address of the bank (COH ～ FFH).

- When power is turnes on or the reset signal is applied. it becomes "0".

ADDRESS : 4210H
NAME : ↑RDNMI
CONTENTS : NMI FLAG BY V-BLANK & VERSION NUMBER

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
BLANK NMI				5 Λ 2 2 VERSION NUMBER			

4 2 1 0 H

└── NMI FLAG BY V-BLANK : When "1" is written to "NMI ENABLE" of register <4200H>, this flag will
show NMI status.
┌ 0 : NMI status is "Disable"
└ 1 : NMI status is "Enable"

※ "1" is set to this flag at beginning of V-Blank, and "0" is set at end of V-Blank.
Also, it can be set by reading this register.

NOTE : It is necessary to reset by reading this flag during NMI processing. (See Appendix-3)

ADDRESS : 4211H
NAME : ↑TIMEUP
CONTENTS : IRQ FLAG BY H/V COUNT TIMER

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
TIMER IRQ							

4 2 1 1 H

└── IRQ FLAG BY H/V COUNT TIMER
: (In case the Timer Enable is set by "Timer Enable" of register <4200H>:)
as soon as H/V counte timer becomes the count value set, IRQ will be applied and
"1" will be set to this flag.
This flag is "READ-RESET".

※ Even if V-EN="0" and H-EN="0" are set by "Timer Enable" of register <4200H>, this flag will be
reset.
┌ 0 : Either H/V count Timer is in active or disable
└ 1 : H/V Count Timer is Time-Up

ADDRESS : 4212H
NAME : ↑HVBJOY
CONTENTS : H/V BLANK FLAG & JOY CONTROLLER ENABLE FLAG

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
V BLANK	H BLANK						JOY-C ENABLE

4 2 1 2 H

JOY CONTROLLER ENABLE FLAG
: This flag shows the timing to read
the data of the Joy Controller.
(However. it is limited to the case
which the "JOY-C ENABLE" of register
<4200H> is set to "1".)

0 : This is a period that the Joy Controller is
not reading the data or the Joy Controller
is disabled.
(In case "0" is set to "JOY-C ENABLE"
of register <4200H>)

1 : This is a period that the Joy Controller
is reading the data.

H-BLANK PERIOD FLAG : It shows whether the scanning is in the H-Blank period or not.
0 : Out of H-BLANK period
1 : In H-BLANK period

V-BLANK PERIOD FLAG : It shows whether the scanning is in the period of V-Blank or not.
0 : Out of V-BLANK period
1 : In V-BLANK period

ADDRESS : 4213H
NAME : ↑RDIO
CONTENTS : PROGRAMABLE I/O PORT (IN-PORT)

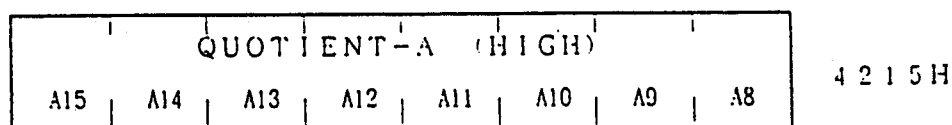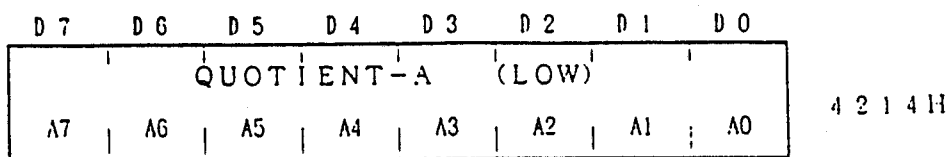| D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
			I/O	PORT			
D7	DG	D5	D4	D3	D2	D1	D0

4 2 1 3 H

• This is a Programable I O port (IN-PORT). The data which is set to the IN-PORT should be read
directly.

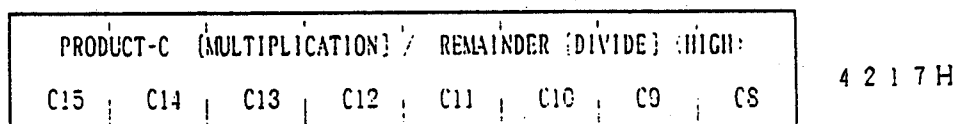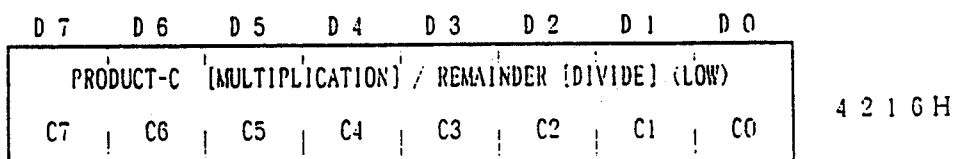• The bit which "1" is written by register <4201H> is used as the IN-PORT.

ADDRESS : 4214H / 4215H
NAME : ‡RDDIVL / ‡RDDIVH
CONTENTS : QUOTIENT OF DIVIDE RESULT

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
QUOTIENT-A (LOW)								4 2 1 4 H
A7	A6	A5	A4	A3	A2	A1	A0	

QUOTIENT-A (HIGH)								4 2 1 5 H
A15	A14	A13	A12	A11	A10	A9	A8	

- This is a Quotient (A), which is a result for Absolute Divide of
  " C (16-BIT) ÷ B (8-BIT) = A (16-BIT)"

- Dividend (C) and Divisor (B) are set by registers <4204H> <4205H> <4206H>.

ADDRESS : 4216H / 4217H
NAME : ‡RDMPYL / ‡RDMPYH
CONTENTS : PRODUCT OF MULTIPLICATION RESULT OR REMAINDER OF DIVIDE RESULT

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
PRODUCT-C [MULTIPLICATION] / REMAINDER [DIVIDE] (LOW)								4 2 1 6 H
C7	C6	C5	C4	C3	C2	C1	C0	

PRODUCT-C [MULTIPLICATION] / REMAINDER [DIVIDE] (HIGH)								4 2 1 7 H
C15	C14	C13	C12	C11	C10	C9	C8	

① IN CASE OF MULTIPLICATION
  - This is a Product (C) which is a result for Absolute Multiplication of
    " A (8-BIT) × B (8-BIT) = C (16-BIT)"

  - A Multiplicand (A) and a Multiplier (B) are set by registers <4202H> <4203H>.

② IN CASE OF DIVIDE
  - This is a Remainder which is a result for the Absolute Divide of
    " C (16-BIT) ÷ B (8-BIT) = A (16-BIT) · · · REMAINDER (8 or 16-Bit)"

  - A Dividend (C) and a Divisor (B) are set by the registers <4204H> <4205H> <4206H>.

ADDRESS : 4218H / 4219H / 421AH / 421BH / 421CH / 421DH / 421EH / 421FH
NAME : JOY1L / JOY1H / JOY2L / JOY2H / JOY3L / JOY3H / JOY4L / JOY4H
CONTENTS : DATA FOR JOY CONTROLLER I. II. III. & IV

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
JOY CONTROLLER-I (LOW)								4 2 1 8 H
X BUTTON	Y BUTTON	TL BUTTON	TR BUTTON					
JOY CONTROLLER-I (HIGH)								4 2 1 9 H
A BUTTON	B BUTTON	SELECT BUTTON	START BUTTON	UP	DOWN	LEFT	RIGHT (JOY PAD)	
JOY CONTROLLER-II (LOW)								4 2 1 A H
X BUTTON	Y BUTTON	TL BUTTON	TR BUTTON					
JOY CONTROLLER-II (HIGH)								4 2 1 B H
A BUTTON	B BUTTON	SELECT BUTTON	START BUTTON	UP	DOWN	LEFT	RIGHT (JOY PAD)	
JOY CONTROLLER-III (LOW)								4 2 1 C H
JOY CONTROLLER-III (HIGH)								4 2 1 D H
A BUTTON	B BUTTON	SELECT BUTTON	START BUTTON	UP	DOWN	LEFT	RIGHT (JOY PAD)	
JOY CONTROLLER-IV (LOW)								4 2 1 E H
JOY CONTROLLER-IV (HIGH)								4 2 1 F H
A BUTTON	B BUTTON	SELECT BUTTON	START BUTTON	UP	DOWN	LEFT	RIGHT (JOY PAD)	

EXPANDED CONNECTOR

• Registers <4016H> <4017H> can be used the same as the Family Computer.

	D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	PORT
4 0 1 6 H RD									4016H D0 : Data for Controller I / 4016H D1 : Data for Controller III
4 0 1 6 H WR									OUT0. OUT1. OUT2
4 0 1 7 H RD									4017H D0 : Data for Controller II / 4017H D1 : Data for Controller IV

NOTE : Whether the standard joy controllers are connected to the SFX unit or not can be reffered
by reading 17th bit of 4016H and 4017H. (See page-22)
0 : connected

1 : not connected

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
CH	CH		A BUS ADDRESS		CH TRANSFER WORD SELECT		
*	TYPE		INC/DEC	FIXED	D2	D1	D0

4 3 × 0 H

└── DMA TRANSFER WORD SELECT

*: Transfer Origination

GENERAL PURPOSE DMA : B-ADDRESS CHANGE METHOD DESIGNATION PER CHANNEL

D2	D1	D0	ADRESS TO BE WRITTEN	
0	0	0	1-ADDRESS	
0	0	1	2-ADDRESS (VRAM etc.)	L. H
0	1	0	1-ADDRESS	
0	1	1	2-ADDRESS (WRITE TWICE)	L. L. H. H
1	0	0	4-ADDRESS	L. H. L. H

H-DMA : The number of byte to be transfered per line and write method designation

D2	D1	D0	＝ OF BYTE TO BE TRANSFERED	ADRESS TO BE WRITTEN	
0	0	0	1 - BYTE	1-ADDRESS	(1)
0	0	1	2 - BYTE	2-ADDRESS (VRAM etc.)	L. H	(2)
0	1	0	3 - BYTE	WITE TWICE	L. L	(1)
0	1	1	4 - BYTE	2-ADDRESS. WRITE TWICE	L. L. H. H	(2)
1	0	0	4 - BYTE	4-ADDRESS	L. H. L. H	(4)

└── FIXED ADDRESS FOR A-BUS & AUTOMATIC INCREMENT/DECREMENT SELECT
[IN CASE OF GENERAL PURPOSE DMA]

D3 ⌈ 0 : AUTOMATIC ADDRESS INCREMENT/DECREMENT
   ⌊ 1 : FIXED ADDRESS <To be used when clearing VRAM etc.

D4 ⌈ 0 : AUTOMATIC INCREMENT
   ⌊ 1 : AUTOMATIC DECREMENT   [In case ˜0˜ is written to D3

└── TYPE DESIGNATION [H-DMA ONLY] : Addressing mode designation when accessing the data
                                                    See Appendix-2
   ⌈ 0 : ABSOLUTE ADDRESSING
   ⌊ 1 : INDIRECT ADDRESSING

└── TRANSFER ORIGINATION DESIGNATION : Transfer Direction A Bus—B Bus, B Bus—A Bus Designation
                                                    (See Appendix-1)
   ⌈ 0 : A-BUS — B-BUS (CPU MEMORY — PPU)
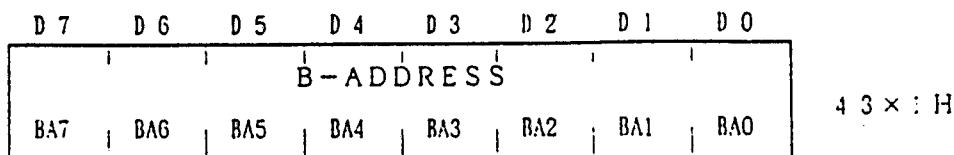   ⌊ 1 : B-BUS —A-BUS (PPU — CPU MEMORY)

※ For example. in case the DMA transfer is performed from CPU memory to PPU. ˜0˜ should be written.

NAME :
CONTENTS : B-BUS ADDRESS FOR DMA

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
			B-ADDRESS				
BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0

4 3 × 1 H

- This is a register, which can set the address of B-bus.

- Whether this is the address of the "Transfer Desitination" or the address of the "Transfer Origination" can be determined by D7 (Transfer Origination) of register <4300H>.

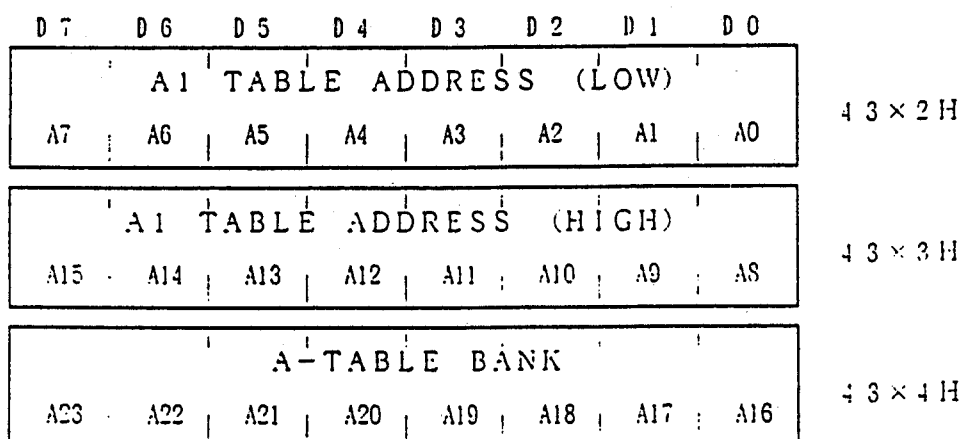   Direction can be designated by "Transfer Origination"
A-BUS ─────────────────────────────────────── B-BUS
                                                  Actual address is 0021XXH.
                                                  (XX : value by this register)

※   When the H-DMA is performed, it will be the address of the "Transfer Desitination".

NAME :
CONTENTS : TABLE ADDRESS OF A-BUS FOR DMA <A1 TABLE ADDRESS>

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
	A1 TABLE ADDRESS (LOW)						
A7	A6	A5	A4	A3	A2	A1	A0

4 3 × 2 H

A1 TABLE ADDRESS (HIGH)							
A15	A14	A13	A12	A11	A10	A9	A8

4 3 × 3 H

A-TABLE BANK							
A23	A22	A21	A20	A19	A18	A17	A16

4 3 × 4 H

- This is a register, which can set the address of A-bus.

- Whether this is the address of the "Transfer Desitination" or the address of the "Transfer Origination" can be determined by D7 (Transfer Origination) of register <4300H>.
  "0" should be written to D7 except a special case.

- In the H-DMA mode, the address of the transfer origination is designated except a special case. Therefore, for the CPU area designated by this address, the data (Appendix-2) must be set by the absolute addressing mode or the indirect addressing mode.

- This address becomes the basic address on the A-Bus during DMA transfer period, and the address will be increased or decreased based on this address.
  (When the general purpose DMA is performed, it will be decreased.)

NAME   :
CONTENTS : DATA ADDRESS STORE BY H-DMA
           & NUMBER OF BYTE TO BE TRANSFERED SETTINGS BY GENERAL PURPOSE DMA

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
DATA ADDRESS (LOW)							
DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
NUMBER OF BYTE TO BE TRANSFERED (LOW)							
B7	B6	B5	B4	B3	B2	B1	B0

(In case of H-DMA;

  4 3 × 5 H

(In case of General Purpose DMA)

DATA ADDRESS (HIGH)							
DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
NUMBER OF BYTE TO BE TRANSFERED (HIGH)							
B15	B14	B13	B12	B11	B10	B9	B8

(In case of H-DMA:

  4 3 × 6 H

(In case of General Purpose DMA:

DATA BANK							
DA23	DA22	DA21	DA20	DA19	DA18	DA17	DA16

(In case of H-DMA:

  4 3 × 7 H

- IN CASE OF H-DMA
    This is a register which the indirect address will be stored automatically in the Indirect
    addressing mode.
    The indirect address means the Data Address described on Appendix-2.
    It is not necessary to read or write directly by the CPU except in special cases.

- IN CASE OF GENERAL PURPOSE DMA
    This is the register, which can set the number of byte to transfer or to be transfered.
    However, the number of Byte (0000H) means 10000H.

ADDRESS   : 43X8H / 43X9H (X : CHANNEL NUMBER ‹0 ~7›)
NAME   :
CONTENTS : TABLE ADDRESS OF A-BUS BY DMA ‹A2 Table Address›

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
A 2	TABLE	ADDRESS		(LOW)			
A7	A6	A5	A4	A3	A2	A1	A0

43×8H

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
A 2	TABLE	ADDRESS		(HIGH)			
A15	A14	A13	A12	A11	A10	A9	A8

43×9H

- This is the address, which is used to access the CPU and RAM, and it will be increased automatically. (See Appendix-2)

- The data of this register is used as the basic address which is the address set by the "A1 Table Address". Afterwards, because it will be increased (or decreased) automatically, it is necessary to set the address into this register by the CPU directly.

  > However, if the data which is transfered needs to be changed by force, it can be done by setting the CPU memory address to this register.
  > And also, the address of the CPU which is accessed currently will be changed by reading this register.

  H-DMA ONLY

ADDRESS   : 43XAH (X : CHANNEL NUMBER ‹0 ~7›)
NAME   :
CONTENTS : THE NUMBER OF LINE TO BE TRANSFERED BY H-DMA

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
CON-			NUMBER	OF	LINE		
TINUE	L6	L5	L4	L3	L2	L1	L0

43×AH

- This is a register which shows number of line for H-DMA transfer. (See Appendix-2)

- The number of line written to the CPU memory will be the basic number of line, it is not necessary to set the address into this register by the CPU directly.

SUPER FAMICOM DOCUMENTATION
SFX03X

REGISTER (CPU)
APPENDIX

GENERAL PURPOSE DMA

(i) TRANSFER METHOD

A-BUS   B-BUS

| CPU
RAM · ROM | ←——→ | PPU |
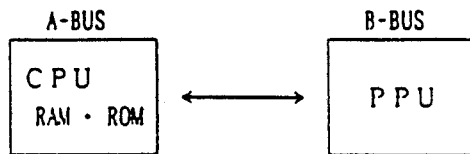
(ii) DATA FORMAT

TYPICAL DATA BANK

(iii) TRIGGER (START)

GENERAL PURPOSE DMA ENABLE FLAG

H-DMA

(i) TRANSFER METHOD

A-BUS   B-BUS

| CPU
RAM · ROM | ——→
←········ | PPU |
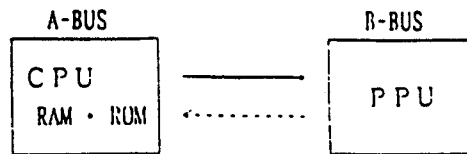
(ii) DATA FORMAT (See Appendix-3 & 4)

⌐ TYPE 0 : Absolute addressing
└ TYPE 1 : Indirect Addressing

⌐ C "0" : If the data is same as the data of
           previous line. the data will not be
           transfered. (Data Compression)

└ C "1" : A pair of data per horizontal line

(iii) TRIGGER (START)

H-BLANK

```
PRIORITY
·H-DMA>GENERAL PURPOSE DMA
·ch0 > ch 1 > · · · > ch 7
 in the same DMA (General purpose DMA or H-DMA)
```

H COORDINATE   H-BLANK

0 ——————————————————— 255 ———————————————— 341

V C O O R D I N A T E

| TABLE PROCESS | H-DMA CH0~CH7   TABLE |

| GENERAL PURPOSE DMA

ROM———CPU RAM etc. | CPU RAM —— PPU |

DISPLAY AREA

224

GENERAL PURPOSE DMA
        CPU RAM———VRAM etc.

262

V-BLANK
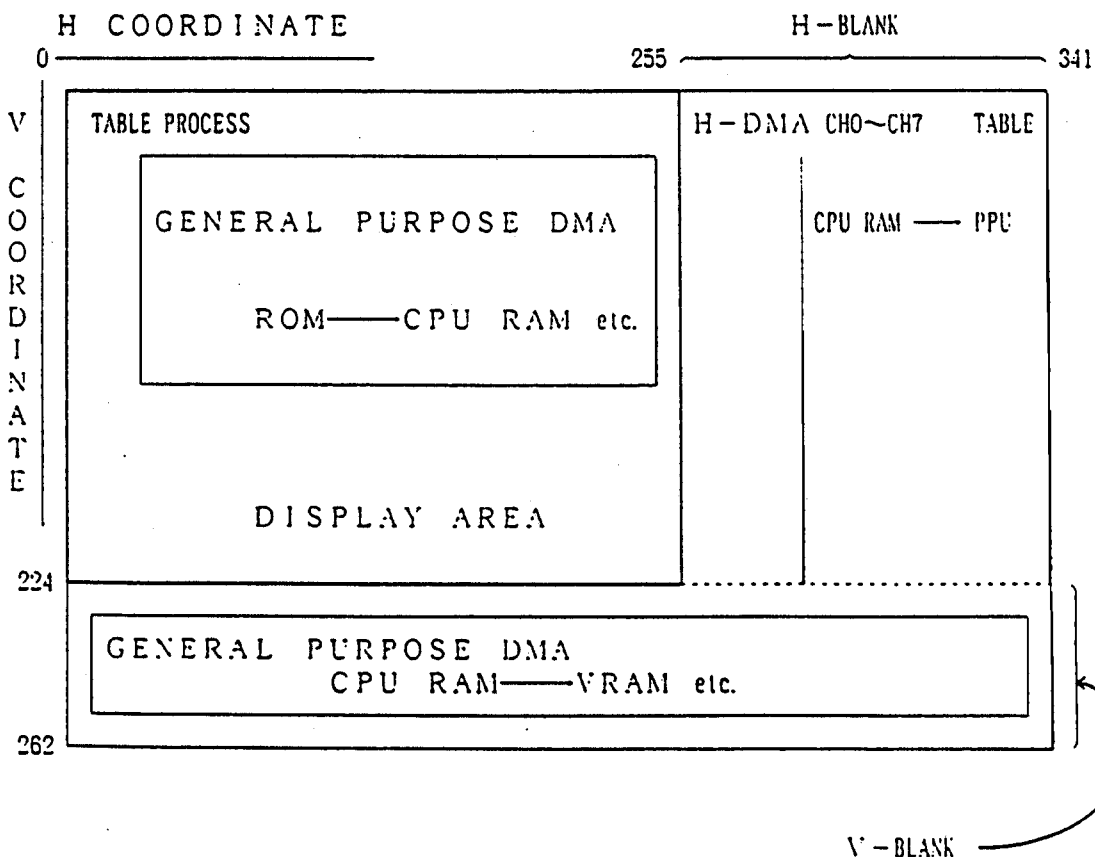
ABSOLUTE ADDRESSING (TYPE-0) ····· This is a mode to transfer the data of the address designated by the TABLE ADDRESS.

CPU RAM

D7   DO

A1 TABLE ADDRESS | C | # OF LINES : 100
A2 TABLE ADDRESS | DATA - 1 (LOW)
                 | DATA - 1 (HIGH)
                 | DATA - 2 (LOW)

SETTING MODE (EXAMPLE-1)
- C="1" : A pair of data per H-line
- NUMBER OF LINES : 100
- TRANSFER WORD SELECT : 1 (2-BYTE L.H)
        (200-Byte data in total)

                 | DATA - 100 (HIGH)
A1 TABLE ADDRESS | C | # OF LINES : 100
A2 TABLE ADDRESS | Data
                 | Data
                 | Data
                 | Data
                 | C | # OF LINES : 0

SETTING MODE (EXAMPLE-2)
- C="0" : Same data as previous line
- NUMBER OF LINES : 100
- TRANSFER WORD SELECT : 4 (4-Byte L.H.L.H)
        (4-Byte data in total)

—— # of line (0) settings : It indicates that the data for the DMA transfer has gone.

INDIRECT ADDRESSING (TYPE-1) ····· This is a mode to transfer the data of the address designated by the Data Address, which is stored to the address designated by the Table Address.

CPU RAM (TABLE MEMORY)   CPU RAM (TABLE MEMORY)

D7   DO   D7   DO

A1 TABLE ADDRESS | C | NUMBER OF LINES
A2 TABLE ADDRESS | Data Address (LOW)
                 | Data Address (HIGH)   } TOP ADDRESS
                 | C | NUMBER OF LINES
                 | Data Address (LOW)   } TOP ADDRESS
                 | Data Address (HIGH)

SETTING MODE (EXAMPLE-1)
- C="1" : A pair of data per H-line
- # OF LINES : 100
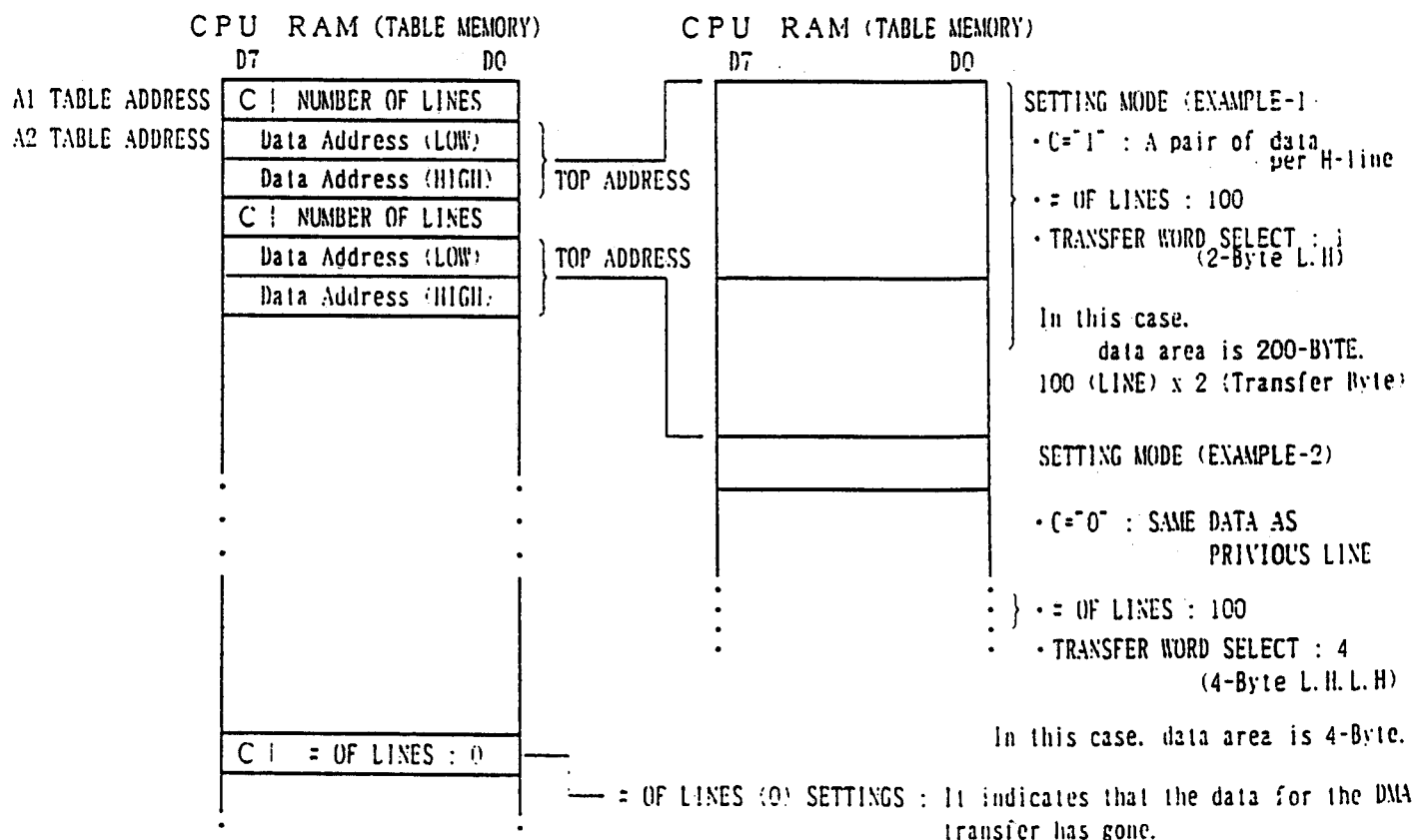- TRANSFER WORD SELECT : 1 (2-Byte L.H)

In this case,
    data area is 200-BYTE.
100 (LINE) x 2 (Transfer Byte)

SETTING MODE (EXAMPLE-2)

- C="0" : SAME DATA AS PREVIOUS LINE
- } # OF LINES : 100
- TRANSFER WORD SELECT : 4
        (4-Byte L.H.L.H)

In this case, data area is 4-Byte.

                 | C | # OF LINES : 0

—— # OF LINES (0) SETTINGS : It indicates that the data for the DMA transfer has gone.

DETECT BEGINNING OF V-BLANK

V-BLANK(END) ———————————— READ <4210H>

D7 of <4200H> { 0 : Disable NMI signal (Always)
"NMI Enable" { 1 : Depend on "Blank NMI" Flag

RESET

SET | BLANK NMI | OUTPUT
V-BLANK(START) ————— | FLAG | ————————→ NMI SIGNAL

D7 of <4210H> { 0 : Disable
"Blank NMI" { 1 : Enable
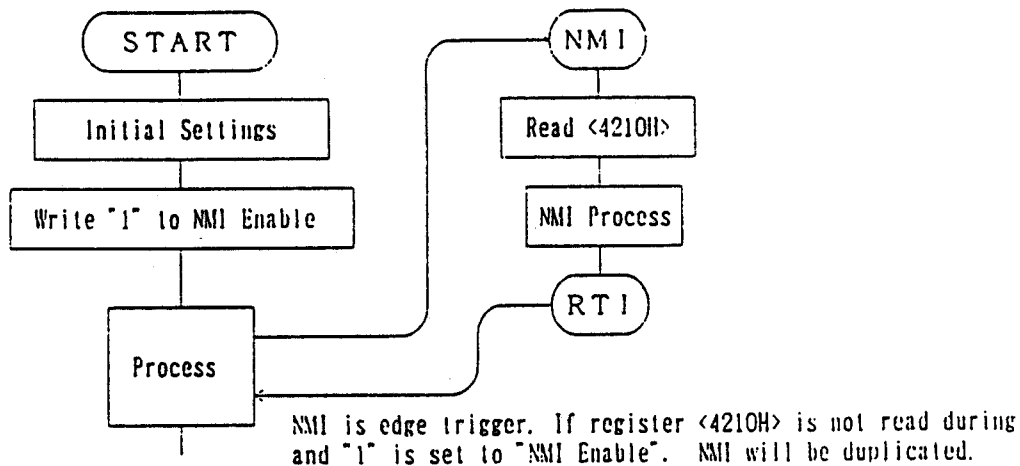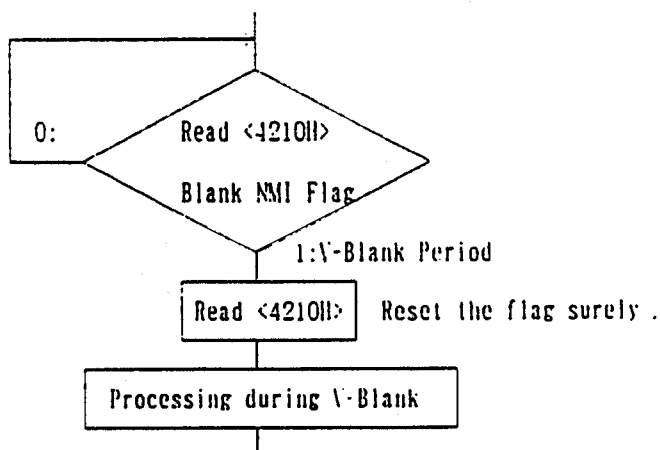
The "Blank NMI" flag of register <4210H> will be set at beginning of V-Blank and will be reset at end of V-Blank. Also, it can be reset by reading register <4210H>.

<EXAMPLE>

1. In case of detecting the beeginning of V-Blank by NMI:

```
   ( START )                          ( NMI )
       |                                 |
 [ Initial Settings ]            [ Read <4210H> ]
       |                                 |
 [ Write "1" to NMI Enable ]     [ NMI Process ]
       |                                 |
                                      ( RTI )
 [ Process ]
       |
```

NMI is edge trigger. If register <4210H> is not read during and "1" is set to "NMI Enable". NMI will be duplicated.

2. In case of detecting the beginning of V-Blank by the flag

```
           |
    0: < Read <4210H>
         Blank NMI Flag >
           |  1:V-Blank Period
    [ Read <4210H> ]  Reset the flag surely.
           |
    [ Processing during V-Blank ]
           |
```

SUMMARY OF REGISTERS

REGISTERS (WRITE) S-PPU

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
2100H	Blanking			Fade IN/OUT (0~15)				
2101H	OBJ Size Select		OBJ Name Select		OBJ Name Base Address			
2102H	OAM Address							
2103H	OAM Priority Rotation							OAM Address MSB
2104H	OAM Data (Low High)							
2105H	BG4	BG3	BG2	BG1 (16 x 16 Size)	BG3 Priority	BG Mode (0~7)		
2106H	Mosaic Size				BG4	Mosaic Enable BG3	BG2	BG1
2107H	BG1 SC Base Address						BG1 SC Size	
2108H	BG2 SC Base Address						BG2 SC Size	
2109H	BG3 SC Base Address						BG3 SC Size	
210AH	BG4 SC Base Address						BG4 SC Size	
210BH	BG2 Name Base Address				BG1 Name Base Address			
210CH	BG4 Name Base Address				BG3 Name Base Address			
210DH	BG1 H-Offset (Low High)							
210EH	BG1 V-Offset (Low High)							
210FH	BG2 H-Offset (Low High)							
2110H	BG2 V-Offset (Low High)							
2111H	BG3 H-Offset (Low High)							
2112H	BG3 V-Offset (Low High)							
2113H	BG4 H-Offset (Low High)							
2114H	BG4 V-Offset (Low High)							
2115H	H/L Inc			V-RAM Address Sequence Mode / Full Graphic / SC Increment				
2116H	V-RAM Address (Low)							
2117H	V-RAM Address (High)							
2118H	V-RAM Data (Low)							
2119H	V-RAM Data (High)							
211AH	Screen Over						Screen Flip V H	

REGISTERS (WRITE) S-PPU

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
211BH	Matrix Parameter A (Low High)							
211CH	Matrix Parameter B (Low High)							
211DH	Matrix Parameter C (Low High)							
211EH	Matrix Parameter D (Low High)							
211FH	Center Position X (Low High)							
2120H	Center Position Y (Low High)							
2121H	CG-RAM Address							
2122H	CG-RAM Data (Low High)							
2123H	W2 EN	IN/OUT	W1 EN	IN/OUT	W2 EN	IN/OUT	W1 EN	IN/OUT
2124H	W2 EN	IN/OUT	W1 EN	IN/OUT	W2 EN	IN/OUT	W1 EN	IN/OUT
2125H	W2 EN	IN/OUT	W1 EN	IN/OUT	W2 EN	IN/OUT	W1 EN	IN/OUT
2126H	Window H0 Position (0~255)							
2127H	Window H1 Position (0~255)							
2128H	Window H2 Position (0~255)							
2129H	Window H3 Position (0~255)							
212AH	BG4		BG3		BG2		BG1	
212BH						Color	OBJ	
212CH				OBJ	BG4	BG3	BG2	B
212DH				OBJ	BG4	BG3	BG2	A
212EH				OBJ	BG4	BG3	BG2	B
212FH				OBJ	BG4	BG3	BG2	B
2130H	Main SF (A)		Sub SF (B)				CG ADD Enable	Dir Sel
2131H	ADD/SUB 1/2 Enable	Back	OBJ	BG4	BG3	BG2	B	
2132H	Blue	Green	Red		Color Brilliance Data			
2133H	EXT. Sync	EXT. Input			Pseudo 512	224/239	OBJ-V	Interlace Select
2134H	MPY (Low)							
2135H	MPY (Mid)							
2136H	MPY (High)							

REGISTER (READ) S-PPU

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
213TH	Soft Latch for H/V Counter							
2139H	OAM Data (Low High)							
213CH	V-RAM Data (Low)							
213VH	V-RAM Data (High)							
213BH	CG Data (Low High)							
213CH	Output Data of H-Counter (Low High)							
213DH	Output Data of V-Counter (Low High)							
213EH	Time Over	Range Over	Master /Slave		5C77 Version Number			
213FH	Field	EXT Latch		NTSC/PAL	5C78 Version Number			
2140H	APU I/O Port							
2141H	APU I/O Port							
2142H	APU I/O Port							
2143H	APU I/O Port							

REGISTERS (WRITE) S-CPU

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
4200H	NMI Enable		Timer Enable V-EN H-EN					Joy-C Enable
4201H	I/O Port							
4202H	Multiplicand-A							
4203H	Multiplier-B							
4204H	Dividend-C (Low)							
4205H	Dividend-C (High)							
4206H	Divisor-B							
4207H	V-Counter Timer							
4208H								H-IGB
4209H	V-Counter Timer							
420AH								V-ASB
420BH	General Purpose DMA (Enable Flag) 07 EN, 06 EN, 05 EN, 04 EN, 03 EN, 02 EN, 01 EN, 00 EN							
420CH	H-DMA (Enable Flag) 07 EN, 06 EN, 05 EN, 04 EN, 03 EN, 02 EN, 01 EN, 00 EN							
420DH								2.68 / 3.58

REGISTERS (READ) S-CPU

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
4210H	Blank NMI					SC22 Version Number		
4211H	Timer IRQ							
4212H	V-Blank	H-Blank						
4213H	I/O Port							
4214H	Quotient (Low)							
4215H	Quotient (High)							
4216H	Product-C / Remainder (Low)							
4217H	Product-C / Remainder (High)							
4218H	Joy Controller I (Low)							
4219H	Joy Controller I (High)							
421AH	Joy Controller II (Low)							
421BH	Joy Controller II (High)							
421CH	Joy Controller III (Low)							
421DH	Joy Controller III (High)							
421EH	Joy Controller IV (Low)							
421FH	Joy Controller IV (High)							

REGISTERS (WRITE) S-CPU

CX : Channel <0

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
43X0H	CIX * T-Org	CIX Type		A-Bus Address INC/DEC Fixed			CIX Transfer Word Sel	
43X1H	CIX B-Address							
43X2H	CIX A1 Table Address (Low)							
43X3H	CIX A1 Table Address (High)							
43X4H	CIX A-Table Bank							
43X5H	CIX Data Address (H-DMA) / Number of Byte to be transferred (General purpose DMA)							
43X6H	CIX Data Address (H-DMA) / Number of Byte to be transferred (General purpose DMA)							
43X7H	CIX Data Bank (H-DMA)							
43X8H	CIX A2 Table Address (Low)							
43X9H	CIX A2 Table Address (High)							
43XAH	Continue		Number of Line					

Note : T-Org means the "Transfer Origination".
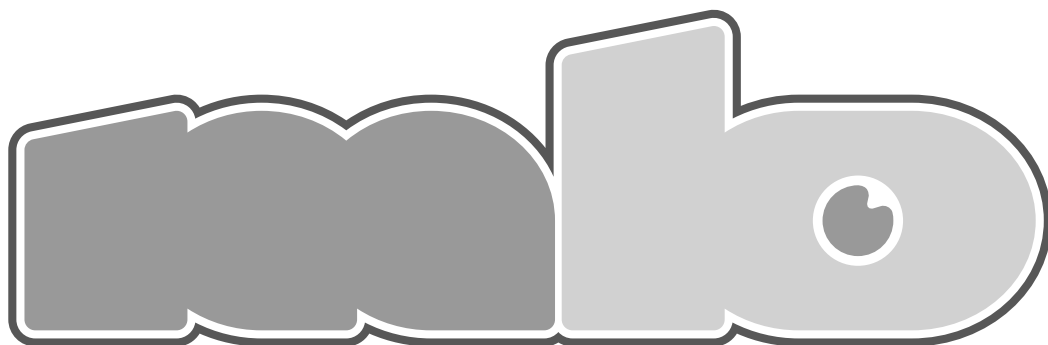
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