SUPER FAMICOM DOCUMENTATION

SFX01

SOFTWARE MANUAL

A I.000.000 BOYS A.K.A MEGABOYS PRODUCE

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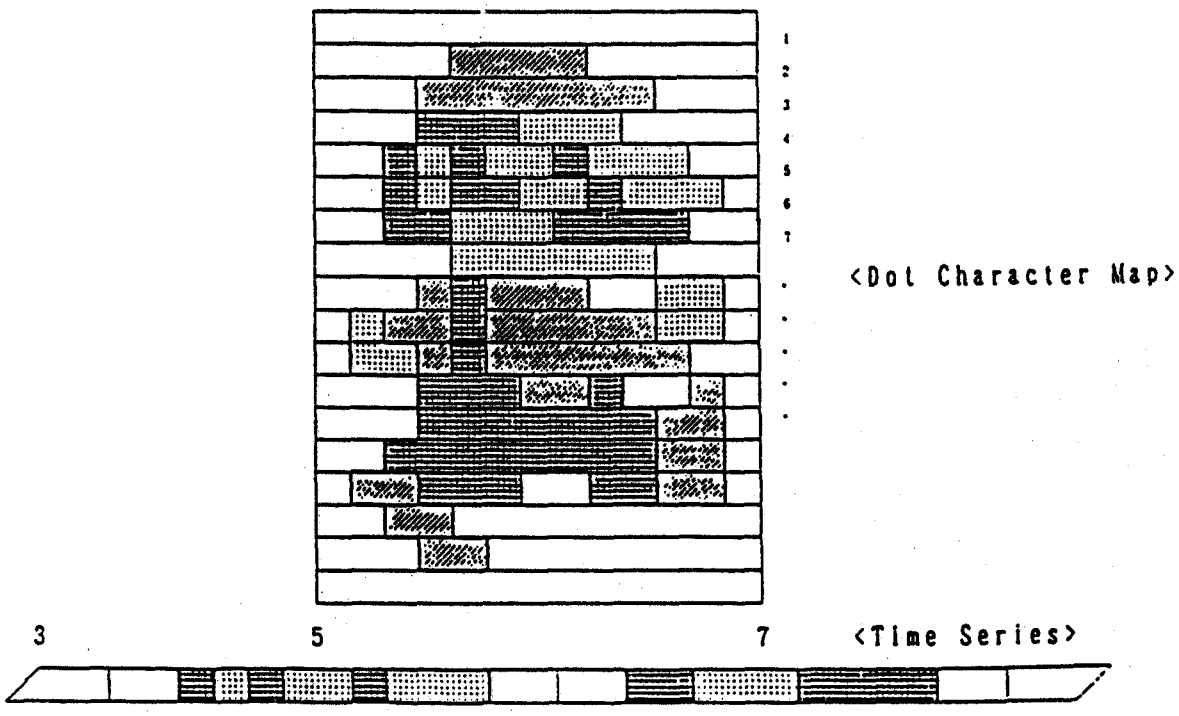
§ 1 INTRODUCTION

Thank you for your interest in developing software for the Super Famicom (SFX). We would like to explain briefly the basic information concerning the home television system. Even if you have been engaged in developing software for the Family Computer (Famicom), please read once for your review.

1. PICTURE IMAGE ON TELEVISION SYSTEM

The picture on a color television system consists of 525 holizontal lines with each line having the color stripes. The broadcasting station breakdowns the picture into lines as shown on Fig.1.
The odd number lines are converted to electric signal from the top to the bottom on the screen, and then, the remaining even number lines will be converted from the top to the bottom in the same way.
The method which traces every two lines is called the "INTERLACE".
For the television system, the electric signal which has been sent is converted to the light signal, and it will traces on the TV screen according to the order above.
The light traces on the screen is called the "scanning", and the period for scanning the odd number line is called the "1st field", and the period for scanning the even number line is called the "2nd field".
A period for scanning on the screen is called "one frame", and this is a period combined of the 1st field and the 2nd field in case of the TV broadcasting. Because of 1/60 sec (one field) and 1/30 sec (one frame), a certain portion on the screen is radiated only every 1/30 sec. However, because of the afterimage of human eyes and the afterglow of the CRT, it does not seem to flicker.



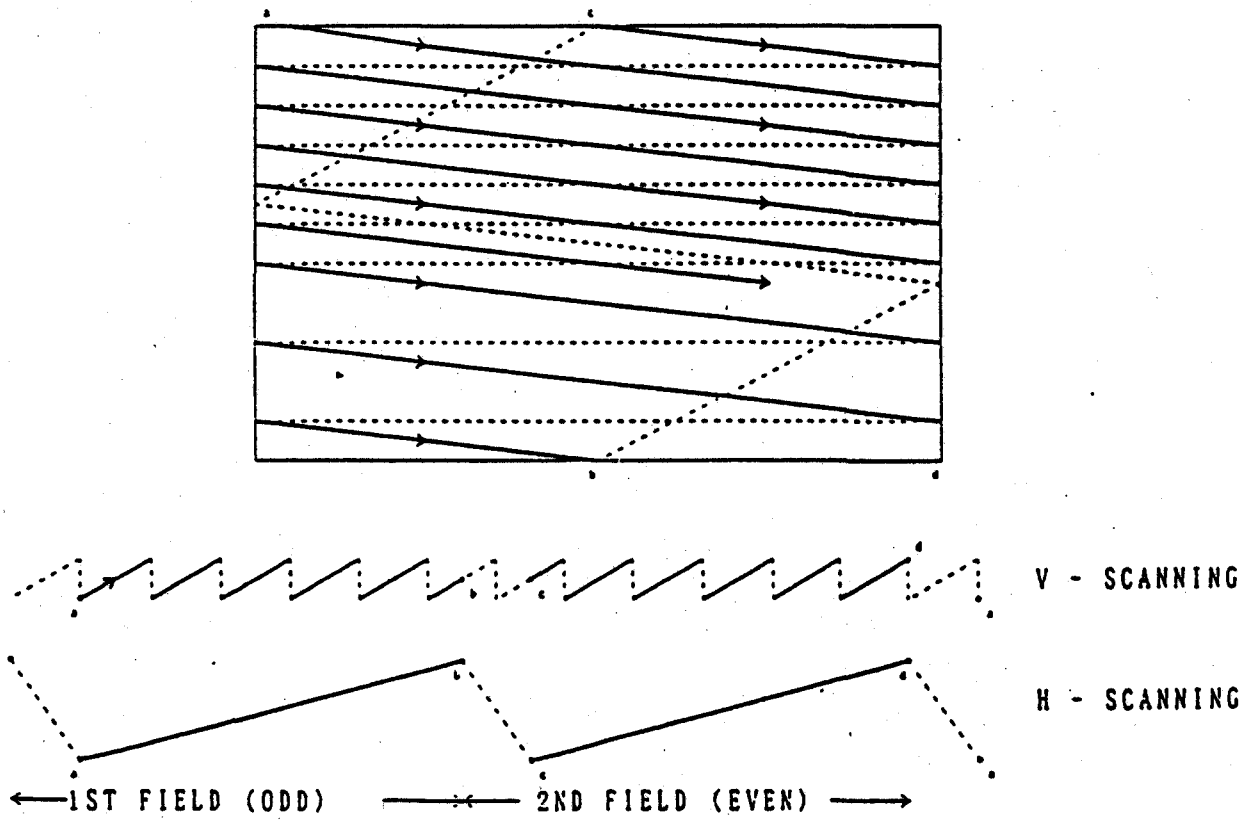
[Fig.1] Scanning Process

2 . SFX DISPLAY

The picture display on the SFX has two modes. One is the Interlace mode based on the television system, and the other is Non-Interlace mode which one frame takes 1/60 second. In the Non-Interlace mode, same position is scanned every field, therefore, lines of a frame are only 262, which means, half of the Interlace mode.
Furthermore, there seems to be no flickering compared to the Interlace mode, since one point on the screen radiates every 1/60 second.

3. BLANK

The screen is scanned from the left to the right and from the top to the bottom on the screen (See Fig.2). After scanning from the left to the right, it sould move back to the left without radiating, and after scanning from the top to the bottom, it should move back to the top without radiating.
It takes a certain amount of time for the scanning.
The former is called H-Blank, and the later is called V-blank.
The Famicom and the SFX use this Blank efficiently to display various movement of the characters.



[Fig.2] SCANNING PATTERN FOR INTERLACE

§ 2 OBJ (OBJECT)

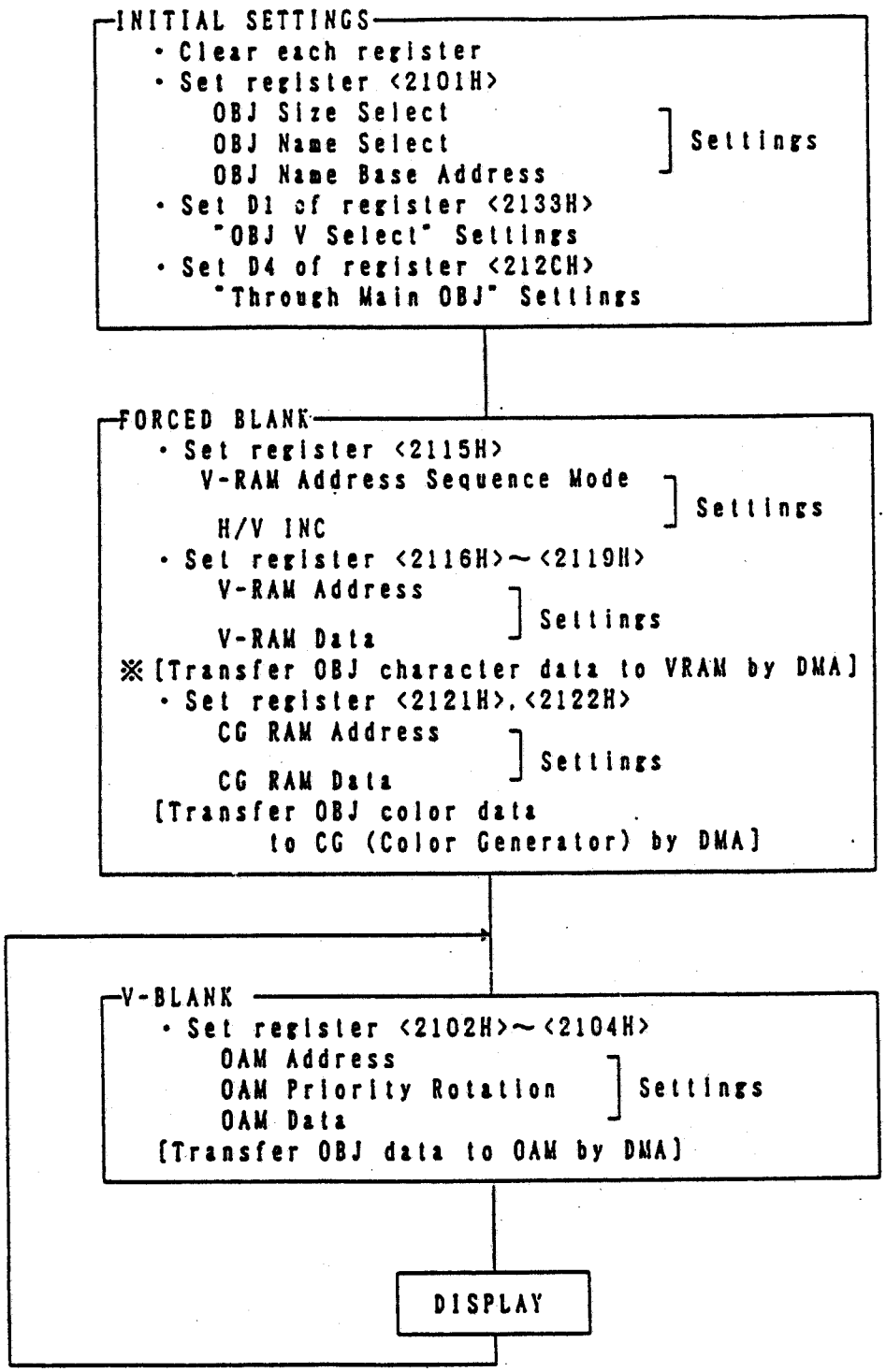
1. OUTLINE

This function can display the Object on a certain position on the screen. The characters, such as the UFO or the missile of a space game, look like they are active in moving this position.
If the character's picture is replaced at the same time the point is moved, animation effects can occur, such as "Mario" character looking like it's walking.

2. FUNCTION

The maximum number of OBJs that can be displayed on the screen is 128 and there are four sizes. However, two sizes can be selected in one frame and one size should be selected for each OBJ.
There are 8 color palettes in the whole OBJs, and one palette should be selected for each OBJ. One color palette has 16 color codes out of 32768 colors, therefore, each OBJ is the picture drawn by 16 colors. Each 128 OBJs has its own priority order, which will decide the display priority if 2 or more OBJs are overlapped.
Furthermore, there is the Flip function of up-down, and left-right, BG priority order and the priority order shifting function.

3. SETTING EXAMPLE



CAUTION ! : It is prohibited to write "100H" to the "OAM H-position (9-bit)". (See PPU Appendix-4)

§ 3 BG (BACKGROUND)

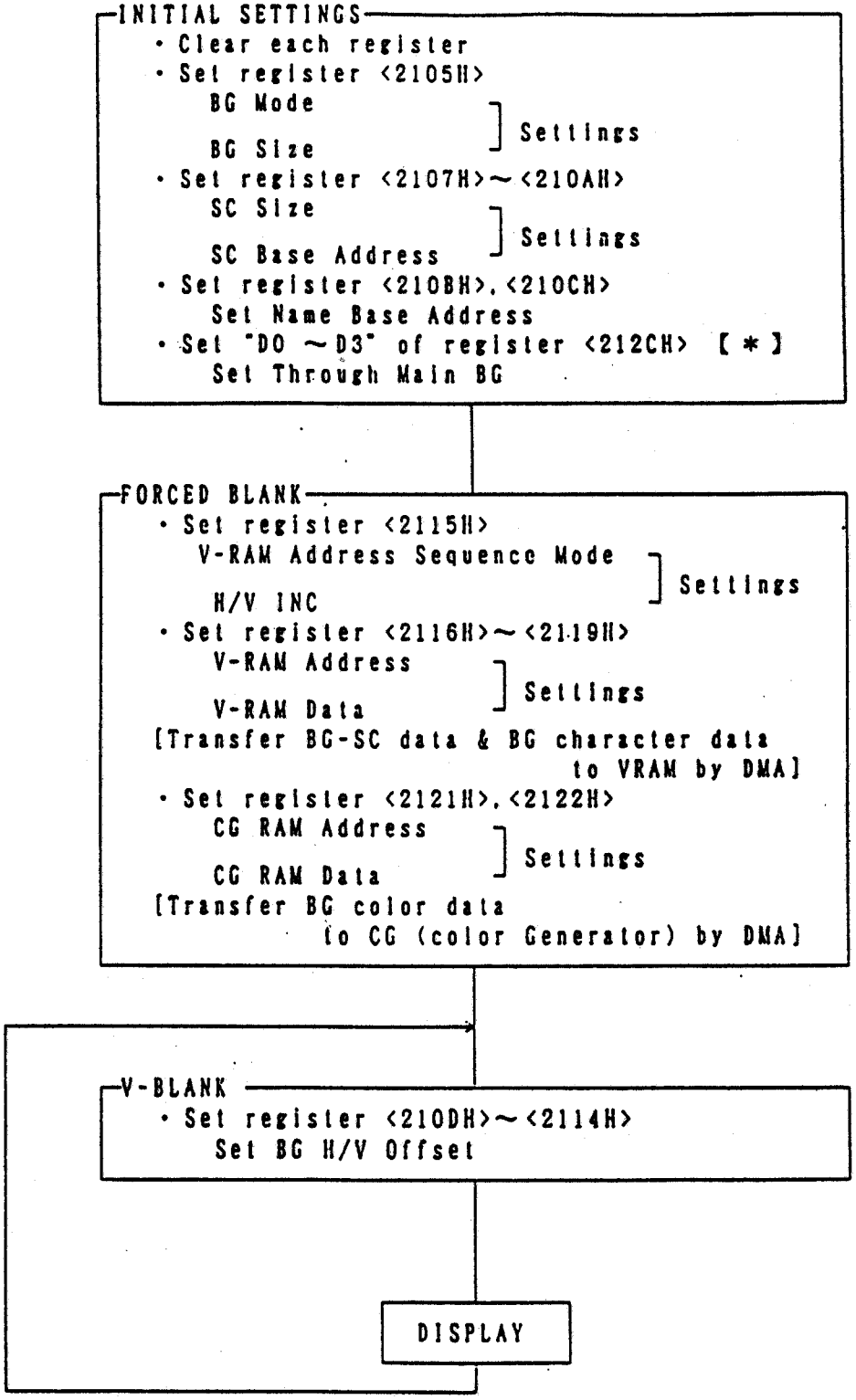
1. OUTLINE

The background for OBJ, such as Mario, can be displayed on the screen, and it can be scrolled to the up, the down, the left and the right, and it helps for the game effect.

2. FUNCTION

There are 8 kinds of BG mode.
In BG mode-0 through 6, there is a difference depending on the combination of the number of the screen, the numbers of the cell color, the resolution and the offset function.
There are 4 screens provided, and the number of the cell colors are from 4 to 256. There are 4 kinds of the resolution selected from 256-dot x 224-dot, 512-dot x 224-dot, or 512-dot x 448-dot.
The character size can be set as "8-dot x 8-dot" or "16-dot x 16-dot" on each screen.
The offset value (scroll coordinate) can be set on each BG screen, and also, the offset value can be changed every horizontal character unit depending on the mode, so that the vertical partial scroll can be made.
8 palettes can be used per character, and H-Flip or V Flip is available per character, and also, the priority order of BG and OBJ can be changed per character. (See "PPU Appendix-16")
Mode-7 has a screen, which can rotate, enlarge or reduce.
There are other functions for BG, such as the mosaic, the window, the fixed color addition/subtraction, the screen addition/subtraction, and the H-Pseudo 512.

3. SETTING EXAMPLE



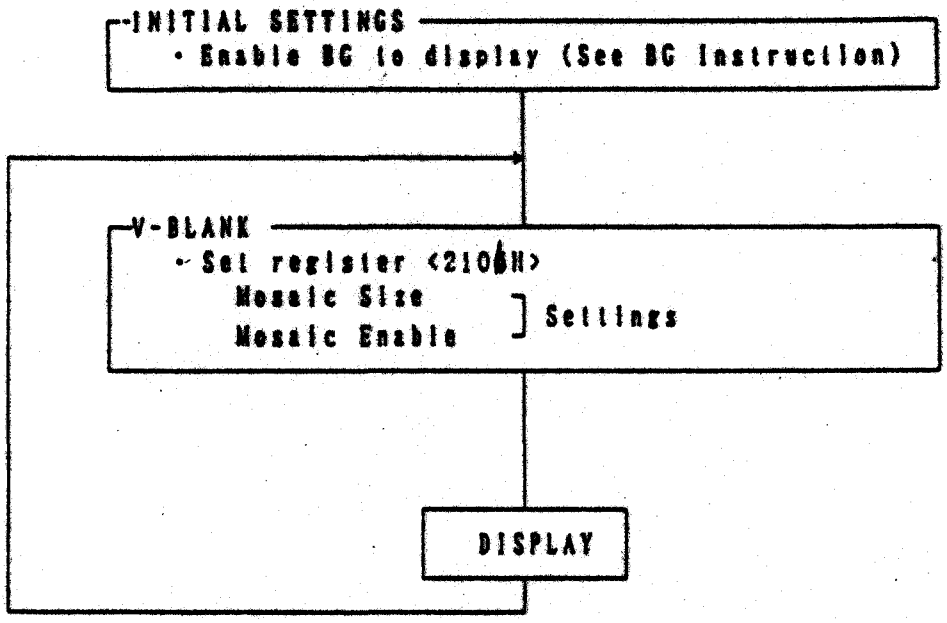
[*] In case of BG MODE 5 or 6, "Through Sub BG" of register <212DH> should also be set. (Refer to § 7)

§ 4 MOSAIC

1. OUTLINE
   This function is to change BG screen to mosaic design and shade off a picture. (See "PPU Appendix-6")

2. FUNCTION
   A picture element of mosaic design can be changed to 15 sizes and BG screen to be a mosaic design can be selected.

3. SETTING EXAMPLE



§ 5 ROTATION/ENLARGEMENT/REDUCTION (BG MODE-7)

1. OUTLINE

In the BG mode-7, this function can add to the BG screen more animation effects by rotation, enlargement or reduction in addition to scroll function

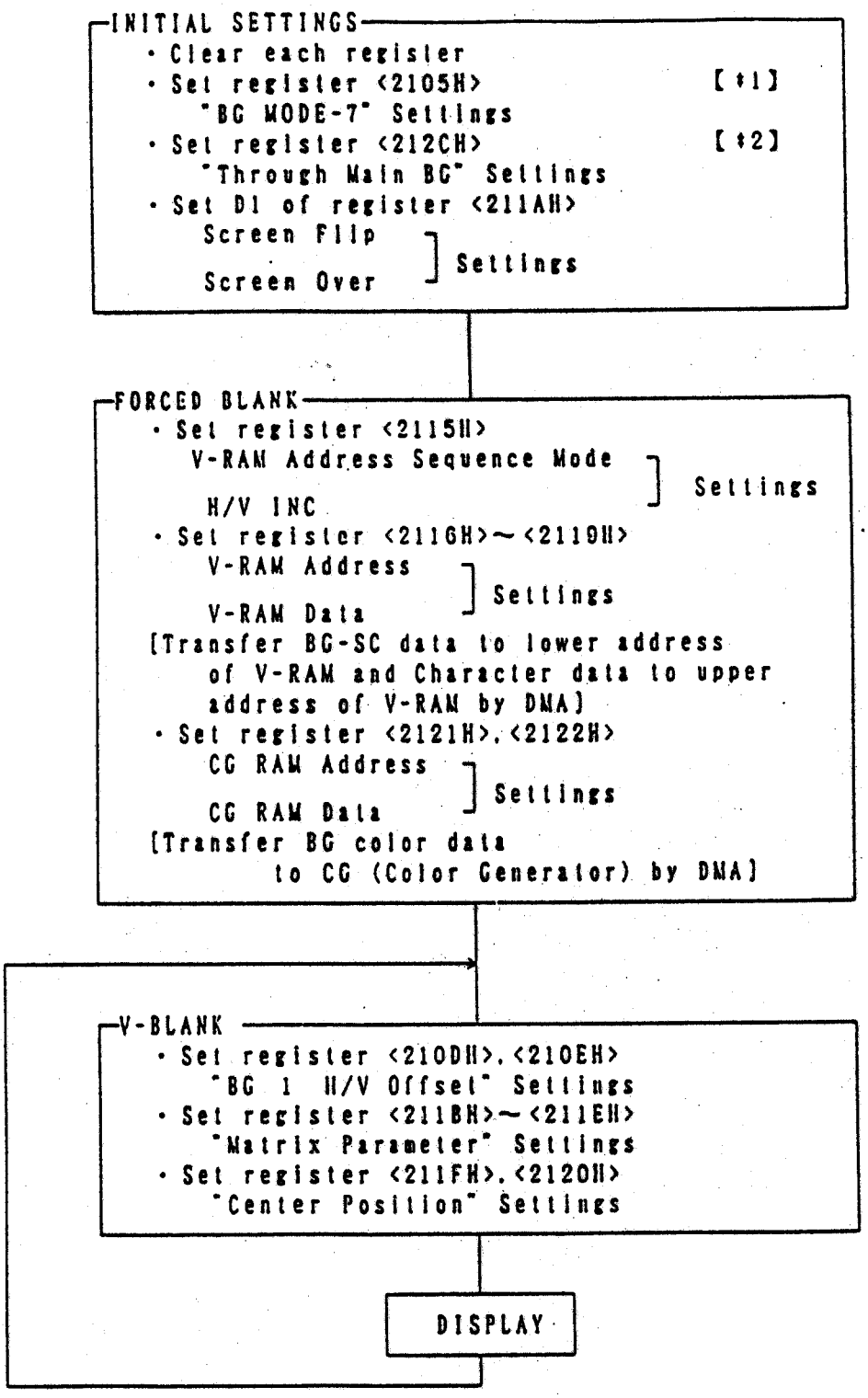
2. FUNCTION

There are 256 characters numbers (8-dot x 8-dot size).
Each dot can be one of 256 colors from a selection of 32,768 colors.
On EXTBG mode, each dot can be one of 128 colors from a selection of 32,768 colors, and each dot can have priority order.
This function is possible to scroll up, down, left and right.
The center coordinate of rotation, enlargement and reduction can be set at either outside or inside of the display area.
The rotation angle, vertical magnification, and horizontal magnification values are changeable. Also, hollizontal flip and vertical flip on the display area are possible.
In case the display area goes beyond the screen area, one of three choices, which are the back drop color, a single character (CHR# 0) or repetetion (wrap) of the screen area, can be selected in order to display the excess portion.

EXTBG MODE : EXTBG mode is originally provided as a function for the purpose of the LSI BG expand.
For the SFX, it is used as rotation, enlargement and reduction with priority order.
Also, it can be used as 2nd screen on mode-7.

(See Page 61)

3. SETTING SAMPLE



[*1] On EXTBG mode. EXT. Input of register <2133H> needs to be set.
[*2] Normally, BG1 should be set. But BG2 should be set on EXTBG mode.

§ 6 WINDOW (WINDOW MASK)

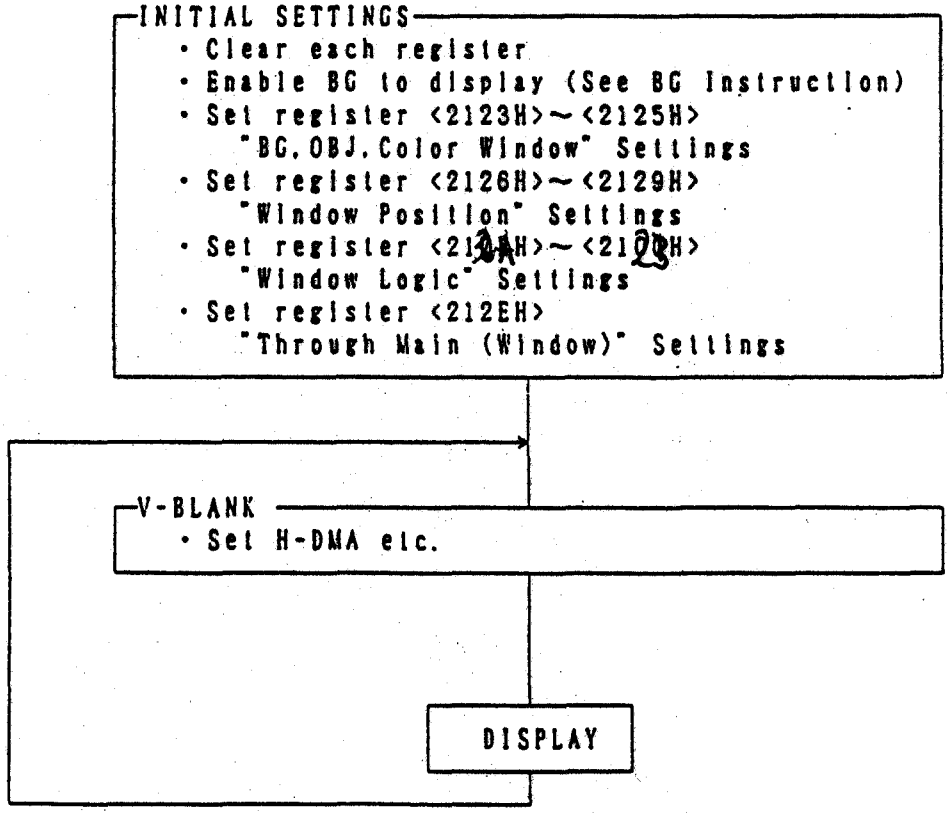
1. OUTLINE

This function limits the display area on the TV screen for BG and OBJ.
The window can be set on the TV screen, and BG and OBJ can be displayed inside (or outside) of this area

2. FUNCTION

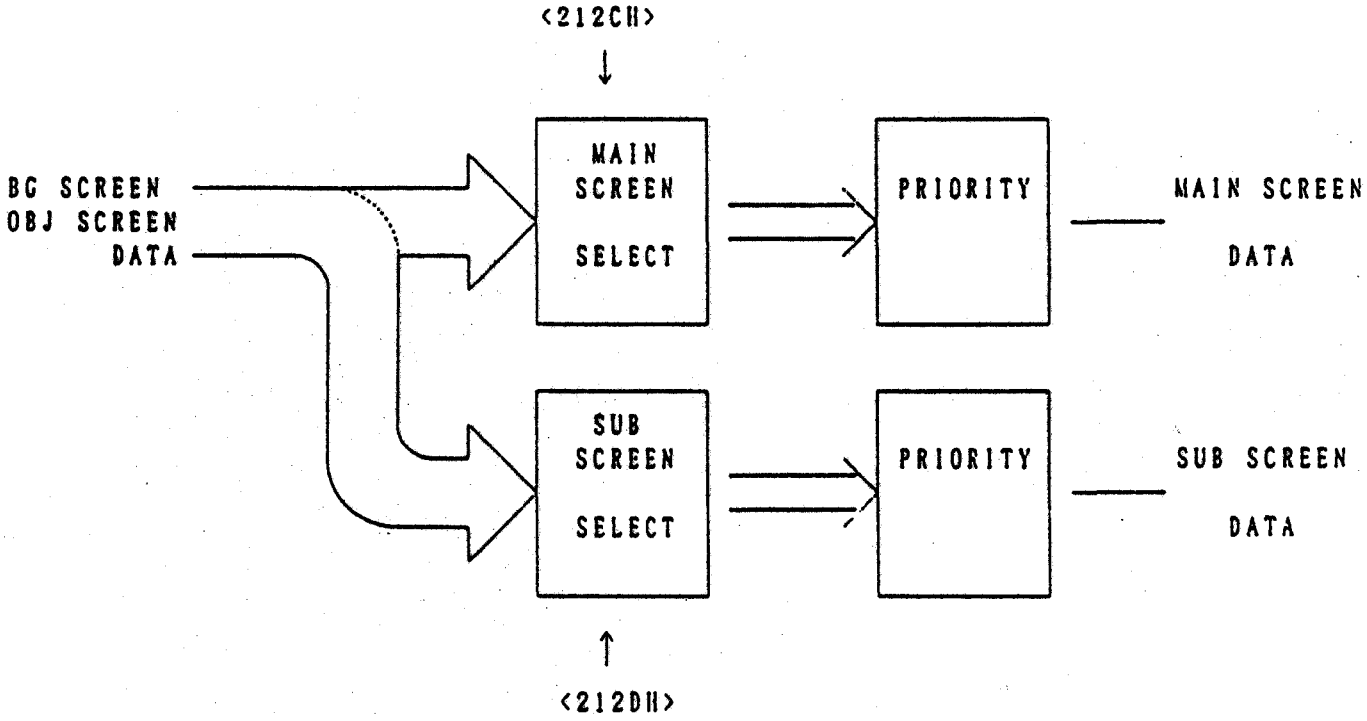
There are 2 windows. Each window can be either BG screen or OBJ, and can be either internal or external mask.
Furthermore, 4 types of window mask logic (OR, AND XOR & NXOR) can be selected each BG and each OBJ by using 2 kinds of the windows at the same time. (See Page-57)
Moreover, if this function is combined with the function of H-DMA, various shapes of the window will be formed, such as a round shape, a heart shape or a star shape.
It is also possible to use this function combined with the screen addition/subtraction and the fixed color addition.

3. SETTING EXAMPLE



§ 7 MAIN / SUB SCREEN

In case of displaying several BG and OBJ screens, the picture to be displayed in the overlapped portion is decided by two paths.
One of them is called the main screen, and the other is called the sub screen.
The screen to be used for the main and the sub screen can be selected by registers <212CH> and <212DH> select.
Furthermore, the data for the main and the sub screen to be displayed is made according to the priority order.
Unless screen the addition/subtraction is done as follows, the "main sw" of the "color window" in register <2130H> is normally on, and the "sub sw" is normally off so that only the main screen is displayed.
(See Appendix-20)



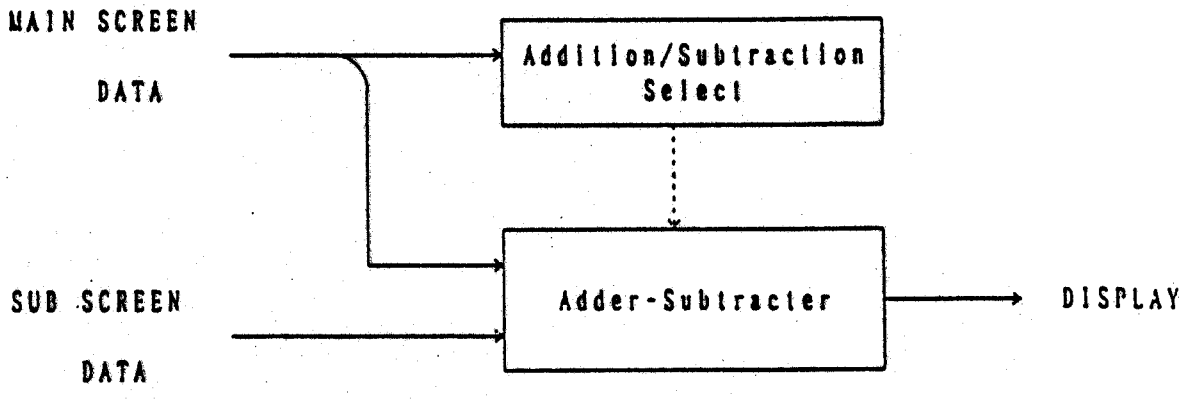
§ 7.1 SCREEN ADDITION/SUBTRACTION

1. OUTLINE

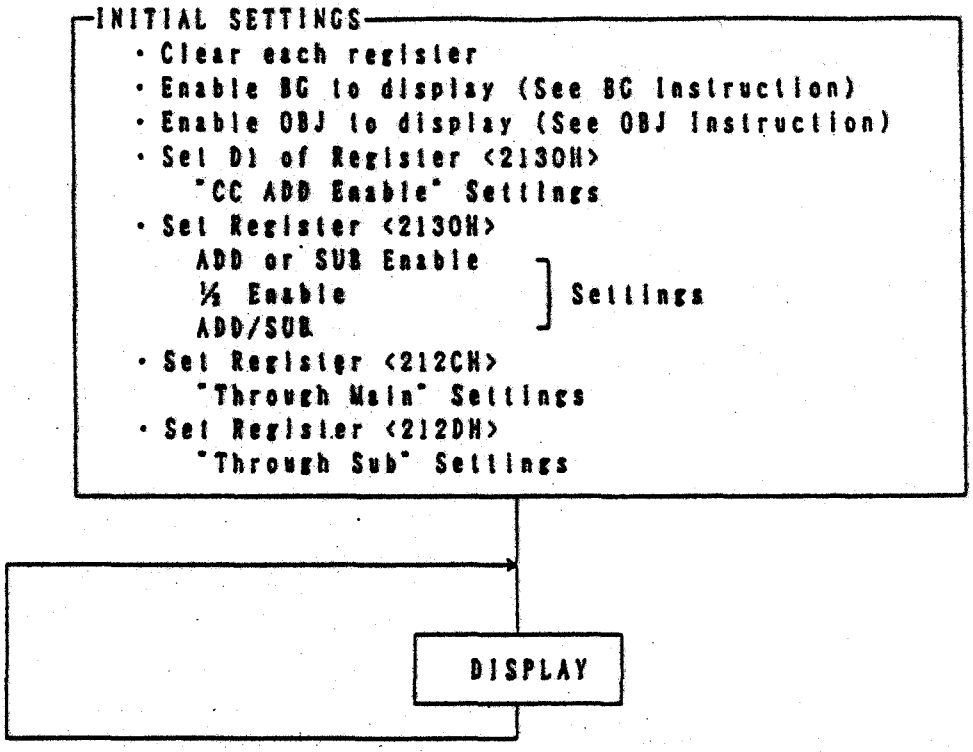
This function is the addition (Overlapping Light) or the subtraction (lense Filter) for the main screen and the sub screen in order to have the effect of transparency.

2. FUNCTION

This function indicates the result after the addition or the subtraction of RGB data on the main screen and sub screen.
This function can also select BG screen or OBJ data on the main screen to be added to or subtracted from the sub screen similar to the Fig. below.
However, when there is no screen data on the sub screen (screen is clear), the color constant explained on page 15 will be added or subtracted.
When the result added or subtracted on each RGB is over 31, the value becomes 31, also, when the value added or subtracted on each RGB is under 0, the value becomes 0.
Please do not use this function on BG mode 5 or 6.



3. SETTING EXAMPLE



NOTE : When the main screen data is the OBJ, it will be added to or subtracted from the sub screen data only for the OBJ of the palette code (4 to 7).
It is convenient for generating the dusky shadow.

NOTE : When "1/2 Enable" of register <2130H> is enabled, the addition/subtraction result of each RGB becomes 1/2.

§ 7.2 COLOR CONSTANT ADDITION/SUBTRACTION

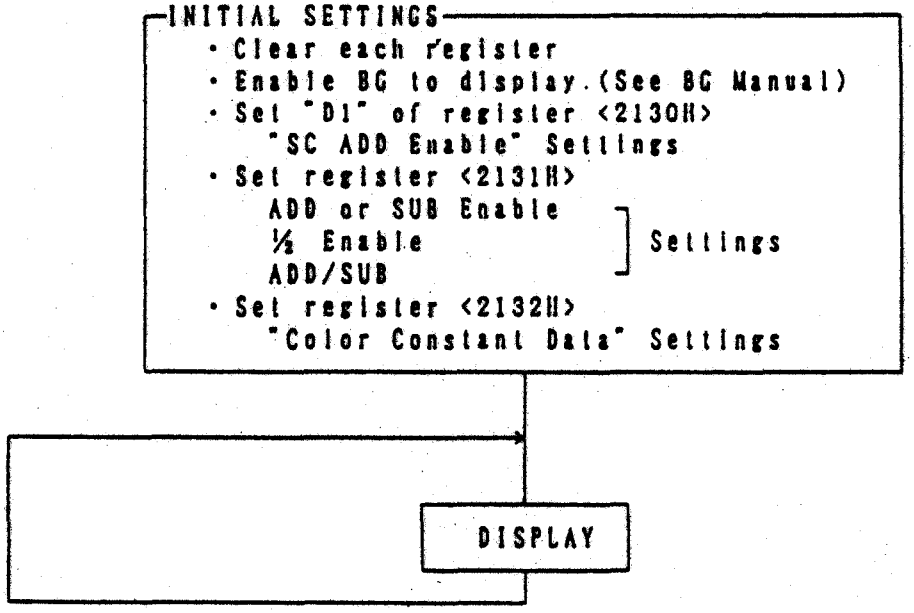
1. OUTLINE

This function can perform addition (overlapped light) or subtraction (lense filter) with the RGB value (color constant) set by the main screen and register <2132H>, and change the color on the display area.

2. FUNCTION

This function can perform addition/subtraction by using the RGB value (color constant) which is set by register <2132H> instead of the sub screen of the screen addition/subtraction described previously.

3. SETTING EXAMPLE



§ 7.3 COLOR WINDOW

(COMBINATION OF WINDOW & ADDITION/SUBTRACTION)

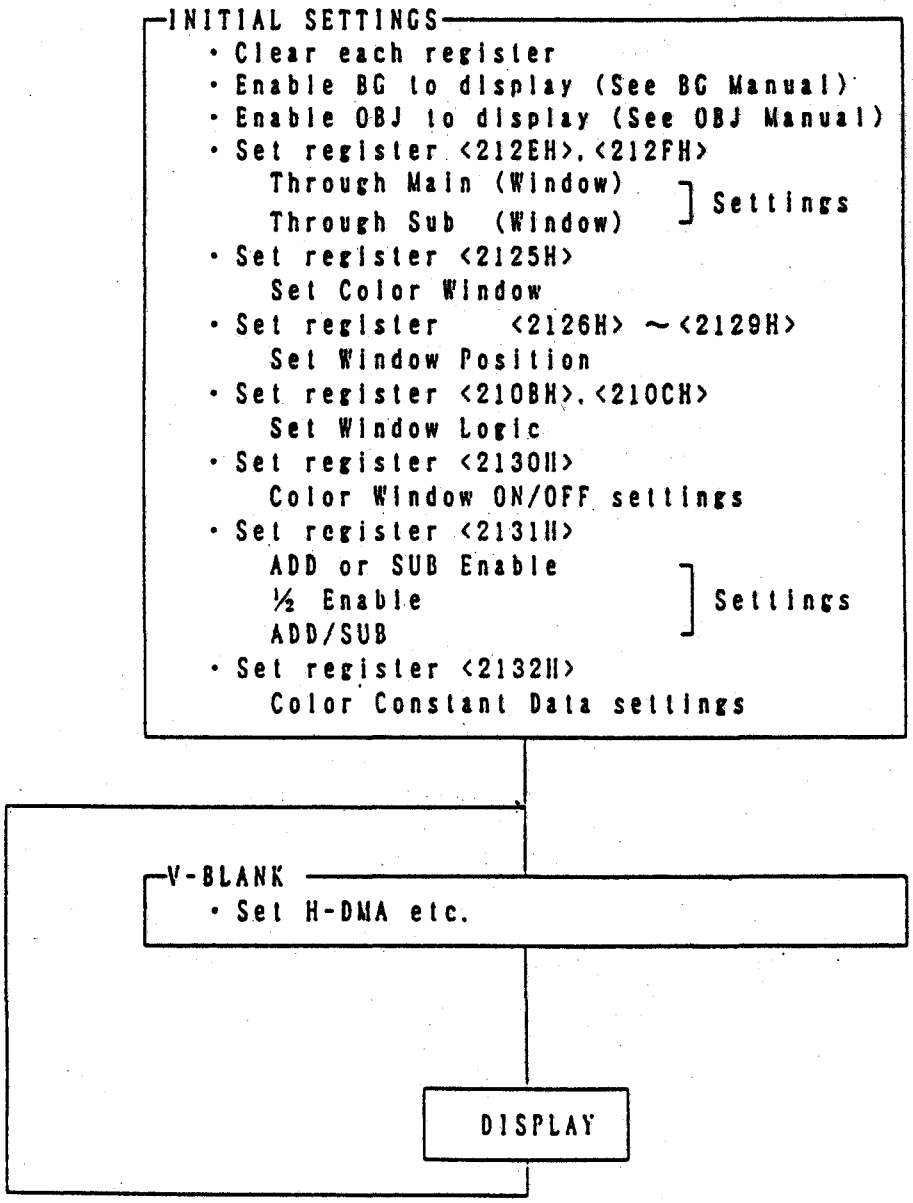
1. OUTLINE

The Screen Addition/Subtraction or the Color Constant Addition /Subtraction can be performed only inside (or outside) of the window.

2. FUNCTION

This is a function, which can select what portion of the window should be displayed and added or subtracted on each main screen and sub screen.
The following is the function as a window, the screen addition /subtraction and the color constant addition/subtraction.

3. SETTING EXAMPLE



§ 8 CG DIRECT SELECT

1. OUTLINE

On BG-1 in mode 3, 4 and 7, the character data can be used as the color data without using CG-RAM color data. BG-1 can be displayed using 2048 colors on mode 3 and 4, and 256 fixed colors on mode-7. BG-2 and OBJ can use the CG-RAM color data without holding in common with the color data on BG-1.

2. FUNCTION

When BG-1 on mode 3, 4, and 7 is displayed on the TV screen, this function is to display 8-bit color data per character dot without using the CG-RAM. the CG-RAM data is used for the other BG, OBJ and Background on main screen.

3. SETTING EXAMPLE

- Enable BG to display (See BG Instruction)
- Set "B0" of register <2130H>
  "Direct Select" Settings

NOTE : See PPU'Appendix-14 for the color data.

§ 9 H-PSEUDO 512

1. OUTLINE

In the mode other than 5 and 6, this function supplements between 2 dots next to each other horizontally, which changes the color smoothly, and has the effect of the gradation.

2. FUNCTION

This function utilizes screen addition/subtraction.
The color constant addition/subtraction can not be done at the same time that this function is performed.

3. SETTING EXAMPLE

- Enable BG to display (See BG Instruction)
- Set "D3" of register <2133H>
  "Pseudo 512" settings
- Set register <212CH>, <212DH>
  Through Main
  Through Sub
  ] Settings
- Set D1 of register <2130H>
  "CC ADD Enable" settings
- Set register <2131H>
  ADD or SUB Enable
  ½ Enable
  ADD/SUB
  ] Settings

§ 1 0 COMPLEMENTARY MULTIPLICATION (SIGNED MULTIPLICATION)

1. OUTLINE

The 2's complement multiplication will be performed with high speed. For example, to calculate the rotation parameter on mode 7, it will lighten the buden of the CPU processing.

2. FUNCTION

The high speed multiplication of 16-bit (2's complement) and 8-bit (2's complement) will be performed with "no-wait", and the result becomes 24-bit (2's complement).

3. SETTING EXAMPLE

- Set BG other than MODE-7 (or V-Blank/Forced Blank) (except during V-Blank or Forced Blank period)
- Write lower 8-Bit (Multiplicand) to register <211BH> :(Input)
- Write higher 8-Bit (Multiplicand) to register <211BH> :(Input)
- Write register 8-Bit (Multiplier) to register <211CH> :(Input)
- Read register <2134H> ～ <2136H> :(Result)

§ 1 1 H/V COUNTER LATCH

1. OUTLINE

This function is used for judging the process timing by knowing where the scanning is approximately on the screen line at certain timing.

2. FUNCTION

This function sets vertical and horizontal counter value at certain timing (when register <2137H> is read), and know where the raster is on the screen by reading the register value.
[The Scanning synchronizes with inner vertical and horizontal counter.]

3. SETTING EXAMPLE

- Read register <2137H> : (counter latch)
- Read register <213FH>
  (Initialize register <213CH>.<213DH> in the order of Low and High)
- Read register <213CH>.<213DH>

§ 1 2 OFFSET CHANGE

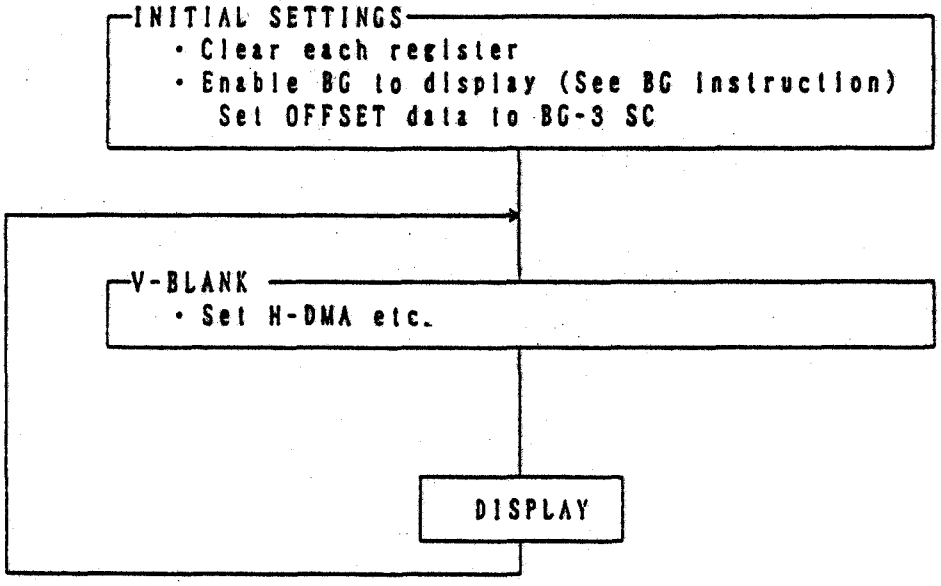
1. OUTLINE

The horizontal and vertical scroll (offset) value can be performed every horizontal 8-dot (character unit) in mode 2, 4 and 6.
The other part of the screen can be brought in the middle of the frame in order to have the effect like a window, and also, a vertical partial scroll can be made.

2. FUNCTION

This function can be selected whether both BG-1 and 2, or either BG-1 or 2 are applicable. The offset for both H and V can be changed at every character unit on mode-2 and 6, but the offset for either H or V can be changed on mode-4.
The same offset will be performed on each line, once the offset data for a horizontal line (32-characters) is set.
In case of setting the other offset value depending on the scanning line, the offset can be changed by changing "BG-3 SC Offset Address" or "BG-3 SC Base Address" during the H-DMA period.

3. SETTING EXAMPLE



§ 1 3 JOY CONTROLLER

1. OUTLINE

The switch status of the joy controller can be read automatically serially, and it will be converted to the parallel data.
It is not necessary to read the switch status one by one like the Family Computer and convert them to the parallel data every time.

2. FUNCTION

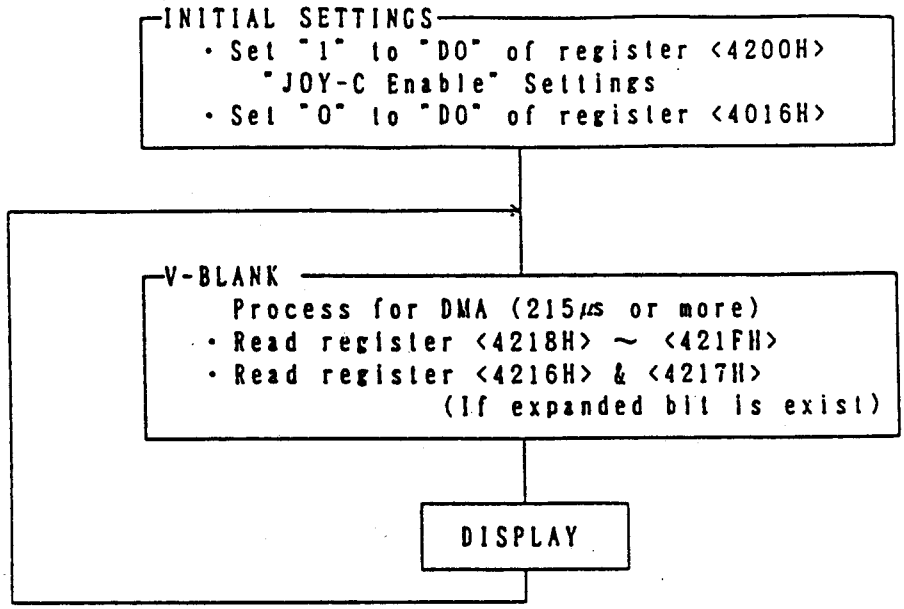
2 pcs of the Joy controller can be connected to the main unit.
(4 pcs of the Joy controller can be connected by using the expanded connector.)
1-bit data is assigned to each switch, and the number of bits to be read automatically for one Joy Controller is up to 16-bit.
For the expanded bit, the bit which is expanded can be read 1-bit by 1-bit by the software like the Family Computer.
The hardware operates for reading the data for about 215 μs right after the V-Blank flag is set or the NMI is applied, Therefore, please note that the register of the Joy Controller can not be read properly.

☆ 215 (214.55)μs is equivalent to 3.4 (3.38) scanning lines, which is a period of 580 (576) Byte to be transfered by the DMA. (In case the CPU clock is 2.68MHz, it is equivalent to 580 machine cycle.)
as soon as the V-Blank starts,
it is considered as the basic flow to perform the general purpose DMA.
Therefore, It is convenient if total number of byte to be transfered by the general purpose DMA is used as a read timing.
[Please refer to the System Flowchart]

☆ The Joy Controller data (register) should be read after confirming that "JOY-C Enable" of the register <4212H> is not set during the V-Blank period, so that the valid data can be read.

* After 18μs (32 machine cycle with 2.68MHz) from the beginning of the V-Blank, the hardware will start to read.
The "JOY-C Enable" of the register <4212H> can not be set during this period.

3. SETTING EXAMPLE



§ 1 4 PROGRAMABLE I/O PORT

1. OUTLINE

   8-BIT programable I/O port is provided to interface to peripheral devices. which are the keyboard, the 3D-glass and etc.

2. HOW TO USE

   "1" should be written to register <4200H> for the bit to be used as the in-port.
   The bit becomes the In-port and it can be read by register <4213H>.
   The data should be written to register <4201H> for the bit to be used as the Out-port.
   This written data can be output directly.

§ 1 5 ABSOLUTE MULTIPLICATION/DIVIDE

1. OUTLINE

The absolute multiplication (8-bit x 8-bit) and the absolute divide (16-bit x 8-bit) can be done using this function.
It is also convenient for the array table processing, and it can improve the processing speed for the multiplication and the divide.

2. FUNCTION

The multiplication calculation between the multiplicand of 8-bit absolute value (0～255) and the multiplication of 8-bit absolute value (0 ～255) can be performed, and can get the result of 16-bit product (0 ～65025).
Or, the divide calculation between the dividend of 16-bit absolute value (0 ～65535) and the divisor of 8-bit absolute value (0 ～255) can be performed, and can get the result of 16-bit quotient (0 ～65535) and 16-bit remainder.
If the divisor is "0" in the divide calculation, the quotient value becomes 65535 (0FFFFH) and the remainder becomes the dividend value, so that caution is required.
It takes about 8 machine cycle for the multiplication calculation and about 16 machine cycle for the divide calculation.
The register value for multiplicand and dividend will not be destroyed even after operation.

3. SETTING EXAMPLE

```
*  In case of Multiplication :
       · Set register <4202H>
           "Multiplicand-A" Settings
       · Set register <4203H>
           "Multiplier-B" Settings
       · Wait for 8 Machine Cycle
       · Read register <4216H>,<4217H>
           Read Product-C

*  In case of Divide :
       · Set register <4204H>,<4205H>
           "Dividend-C" Settings
       · Set register <4206H>
           "Divisor-B" Settings
       · Wait for 16 Machine Cycle
       · Read register <4214H>,<4215H>
           Read Quotient-C
       · Read register <4216H>,<4217H>
           Read Remainder
```

§ 1 6 H/V COUNT TIMER

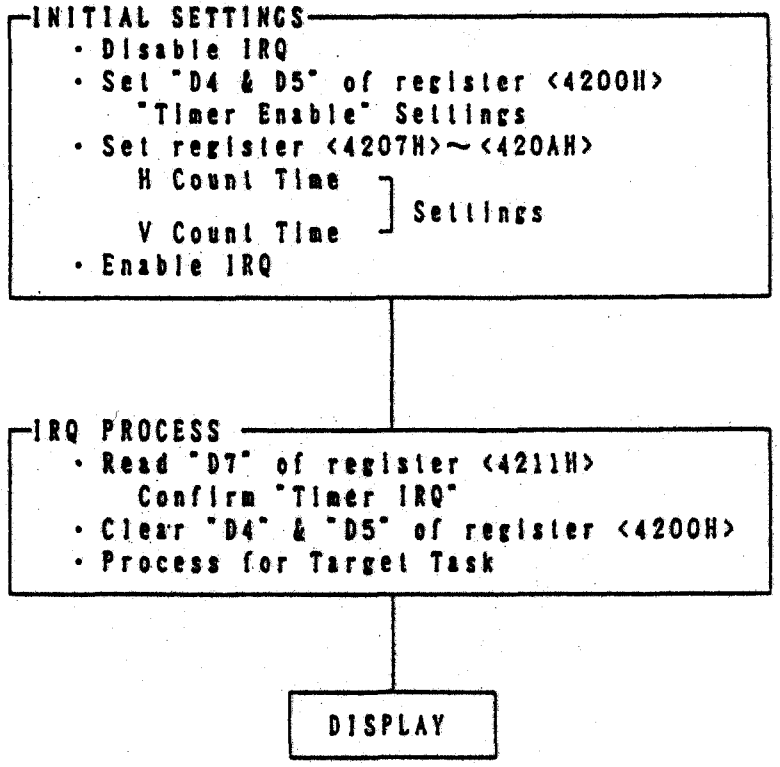
1. OUTLINE

The SFX has the timer synchronizing with the display on the TV screen. which is used for adjusting the timing of the scanning on the screen and the software process.

2. FUNCTION

This function can generate the interrupt either at any V-position or H-position of the scanning lines. It can also generate the interrupt at any position of the scanning line.

3. SETTING EXAMPLE



§ 1 7 DMA (DIRECT MEMORY ACCESS)

The DMA is the method to transfer the data as same as the data transfer which is done by the CPU. However, the DMA can transfer the data at high speed by using the hardware instead of the CPU.
Especially, the SFX has the exclusive DMA, since the picture data has to be transfered rapidly.
The DMA for the SFX is to transfer the data between "A-Bus address" in the CPU (0000000～0FFFFFF) and "B-Bus address" in the S-PPU (0002100 ～00021FF), which has 8-channels in total.
There are two kinds of the DMA, which are the general purpose DMA and the H-DMA, and either of the two can be set at each channel.
The data can be transfered between the same DMAs in the order from the lower channel number (0 ～7). And the H-DMA can interrupt even during the transfer by the general purpose DMA, which means that the H-DMA has higher priority than the general purpose DMA.
Furthermore, the CPU process stops automatically during the DMA period, and will start again after the DMA is completed. Therefore, it is not necessary to observe the DMA completion by the CPU.

§ 17.1 GENERAL PURPOSE DMA

1. OUTLINE

This function can transfer the data rapidly between 2 types of memory devices, which is memory which can be accessed directly by the CPU, such as a ROM on the game cartridge, and memory which has to be accessed through the S-PPU, such as the V-RAM.

2. FUNCTION

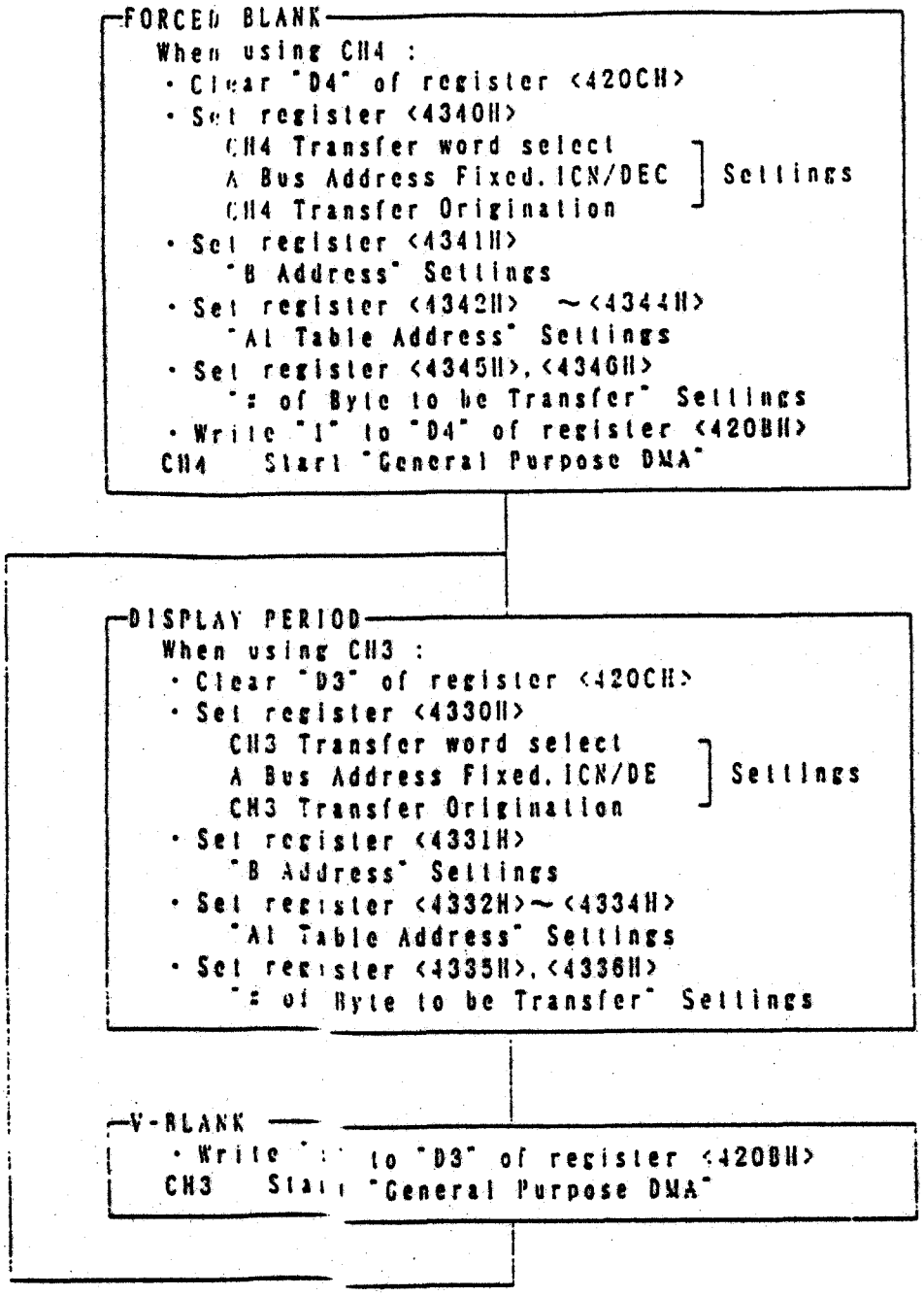
The maximum area of the A-Bus address which can be used in one channel is limited in one bank (65.536 Byte).
Therefore, in case of spreading over more than 2 banks, it is necessary to use more than 2 channels or transfer twice.
One A-Bus address basically is increased every time 1-byte data is transfered. However, it can be decreased or fixed depending on the settings ("D3" and "D4" of register <43X0H>).
The following table shows 4 ways of the B-Bus address changes.

# of Transfer (# of Byte) \ Transfer Word Select <43X0H>	0 or 2	1	3	4
0	B	B	B	B
1	B	B + 1	B	B + 1
2	B	B	B + 1	B + 2
3	B	B + 1	B + 1	B + 3
4	B	B	B	B
5 . . .	B . . .	B + 1 . . .	B . . .	B + 1 . . .

NOTE : B means the data of register <43X1H>.

☆ In case of 224-lines, the general purpose DMA can transfer 6K-Byte data maximum during V-BLANK period.

3. SETTING EXAMPLE



§ 17.2 H-DMA

1. OUTLINE

This is the special DMA, which can transfer the data automatically synchronizing with the H-Blank. Therefore, the S-PPU settings can be varied by each horizontal scanning line, and also, special effects can be added to the picture.

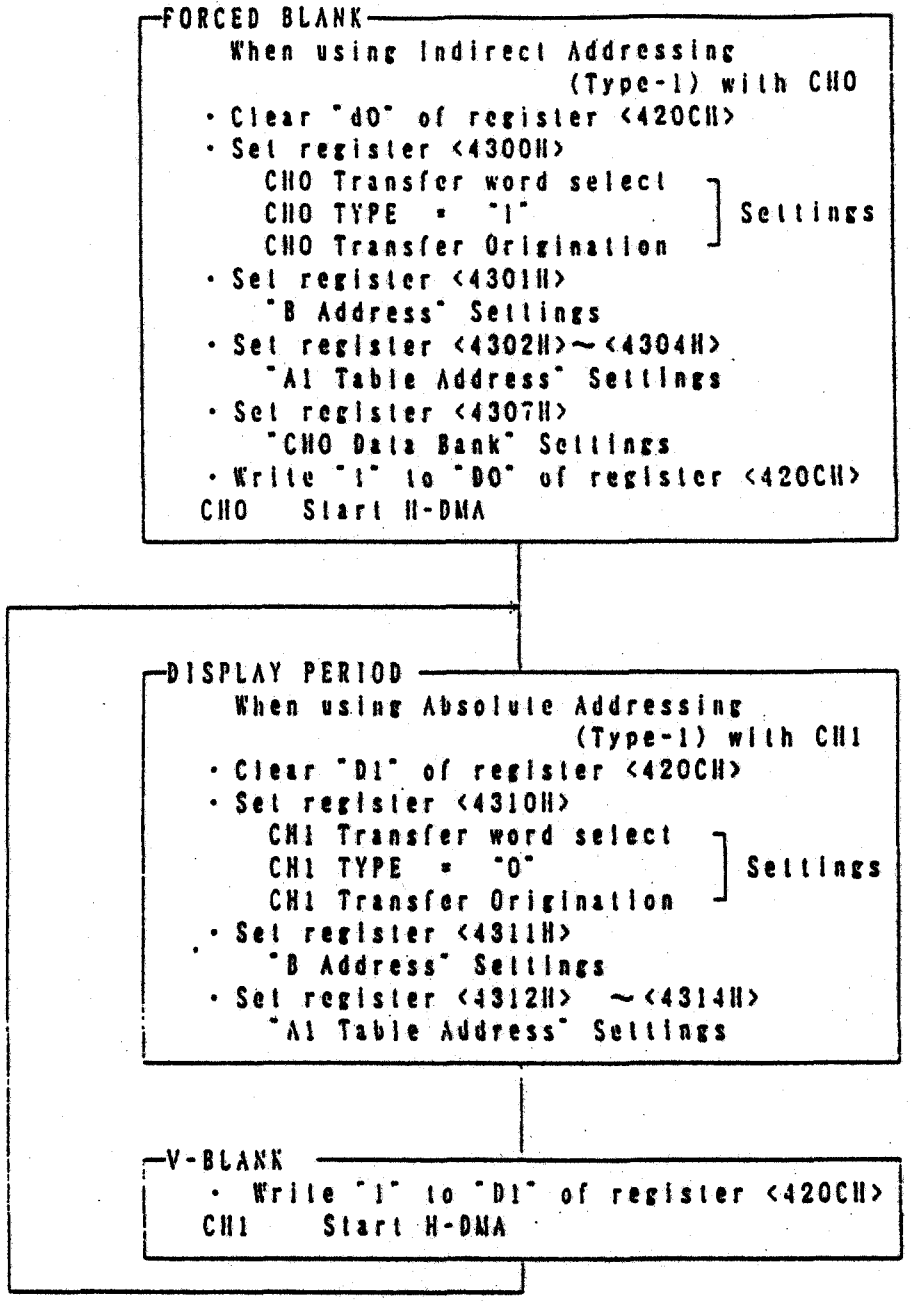
2. FUNCTION

This function basically transfers the data from the A-Bus memory (CPU memory) to the S-PPU register.
There are two kinds of the addressing modes on the A-Bus side, absolute addressing and indirect addressing, which can be set by each channel.
There are two kinds of the data transfer, one is to transfer a set of data each horizontal blank period, and the other is to transfer a set of data every certain number of the horizontal blanks.
These two methods can both be used in the data table for one screen (one field), therefore, necessary data can be transfered each necessary scanning line for one screen (one field).
The B-Bus address can be changed five ways according to the table shown below.

# of Line to be Transfered \ Transfer word select <43X0H>	0	1	2	3	4
1	B	B	B	B	B
				B	B + 1
		B + 1	B	B + 1	B + 2
				B + 1	B + 3
2	B	B	B	B	B
				B	B + 1
		B + 1	B	B + 1	B + 2
				B + 1	B + 3
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.

NOTE : B means the data of register <43X1H>.

3. SETTING EXAMPLE



§ 1 8 INTERLACE

1. BG MODE 0 ~ 4 & 7
   When "1" is written to "D0" of register <2133H>, the picture which is output from the SFX will be the interlace signal. Therefore, in case of BG mode 0 through 4 and 7, the same picture will be displayed unless the picture data is changed between the 1st field and the 2nd field. (See PPU Appendix-18)

2. BG MODE 5 & 6
   In case of the interlace on BG mode 5 and 6, the vertical resolution will be doubled in appearance, because a picture is displayed by using one frame of the combination of the 1st field and the 2nd field. (See Appendix-19)

3. OBJ
   When "1" is written to "D1" of register <2133H>, the vertical resolution will be doubled as same as the case above, because a picture is generated by one frame.
   However, the range of the V-position is 0 through 255, and it will not be doubled.

§ 1 9 H- 512 MODE (BG MODE 5 & 6)

1. MAIN SCREEN & SUB SCREEN SETTINGS

   The screen addition/subtraction should not be used, because a part of both main screen and sub screen function are used in this mode. Therefore, for the case except the color constant addition /subtraction, "1" should be written to "D4" and "D5" of register <2130H> and the sub switch should be "OFF".
   Also, in this mode, the same data should be written to registers <212DH> <212EH> and <212FH>, and "Through" should be the same for both the main and the sub screen.

2. FIXED COLOR ADITION/SUBTRACTION

   "D0 ~ D5" of the register <2131H> is the flag which can select the main screen for addition/subtraction.
   By the reason described above, this selection can not be done.
   It is necessary to write "1" to these 6 flags (D0 ~ D5) when the color constant addition/subtraction is performed.
   The remaining settings are the same as the other mode on page 15.
   However, in case of the color window function, there will be addition/subtraction every 2-dot unit horizontally, because the window has only 256 positions horizontally.

3. DISPLAY WITH OBJ

   As the name of H-512 mode implies , it indicates the 512 horizontal resolution for BG. But, the horizontal resolution for the OBJ is only 256-dot regardless of the BG mode.
   However, the priority order for BG is determined by every dot.

4. OTHERS

   See Appendix-19 for details

§ 2 0 OBJ 33'S LINES OVER & PRIORITY ORDER

1. 33's RANGE OVER

The number of OBJ which can be displayed in a horizontal line is limited. One of its limitation is called the "33's Range Over". This is the limitation that OBJs (33 or more) can not be displayed in a horizontal line regardless of the OBJ size.
If the "33's Range Over" is occured in one field (at least one line), "D6" of the register will be set.
For the line which this "33's Range Over" is occured, only 32 OBJs can be displayed out of more than 33 OBJs according to the priority order (selected from smaller OBJ number).

NOTE : "the number of displayed OBJ" counts the OBJ hidden by BG, window or other OBJs.

NOTE : If H-position is minus, and the OBJ is not displayed on the screen area to be displayed (located on the left of the left the screen to be displayed), "the number of the displayed OBJ" does not count them.

2. 35's TIME OVER

The other limitation on one horizontal line is the "35's time over". This is the limitation that OBJ character size is converted to character size (8-dot x 8-dot) and OBJs (35 or more) can not be displayed
If the "35's Time Over" has occured in one field (at least one line), "D7" of the register <213EH> will be set.
In the line which this "35's Time Over" has occured, only 32 OBJs out of "The OBJ which should be displayed" can be displayed according to the priority order (selected from larger OBJ number).
The other limitation on one horizontal line is the "35 time over". This limit is due to a conversion limit of less than 35 OBJs (8 x 8) displayed per horizontal line.
"The OBJ which should be displayed" means less than 33 OBJs which satisfy the display condition explained in "33's Range Over" above.

NOTE : There are characters (8-dot x 8-dot) which are not displayed on the display area depending on OBJ size and position. But they are not included in this limitation (34 or less).

3. PRIORITY ORDER SHIFTING

As mentioned above, limited numbers of the OBJs can be displayed in a line and are related to the priority order. It is desirable to develop a game within this limitation. However, more OBJs beyond this limitation sometimes need to be displayed. In this case, there is the way to display more OBJs imaginarily on one line. The priority order which is changed every frame is one of the methods. Also, there is another method, which changes the OBJ data order by programming. The SFX also has the function to rotate the priority order of 128 OBJs.
When using these methods, please consider that the OBJ will flash every frame unit, and the priority order among OBJs will change.
The setting method is as follows:

① display the OBJ.
② Write "1" to "D7" of the register <2103H>.
③ Write the highest priority OBJ number (0 ～ 127) to "D1～D7" of the register <2102H> during V-BLANK period every frame.
④ repeat ③

When OBJ number storing at ③ is "n"

OBJ NUMBER	PRIORITY ORDER
OBJ 0	129－n
・ ・ ・	・ ・ ・
OBJ n－1	128
OBJ n	1
OBJ n＋1	2
・ ・ ・	・ ・ ・
OBJ 127	128－n

§ 2 1　CPU CLOCK & ADDRESS MAP

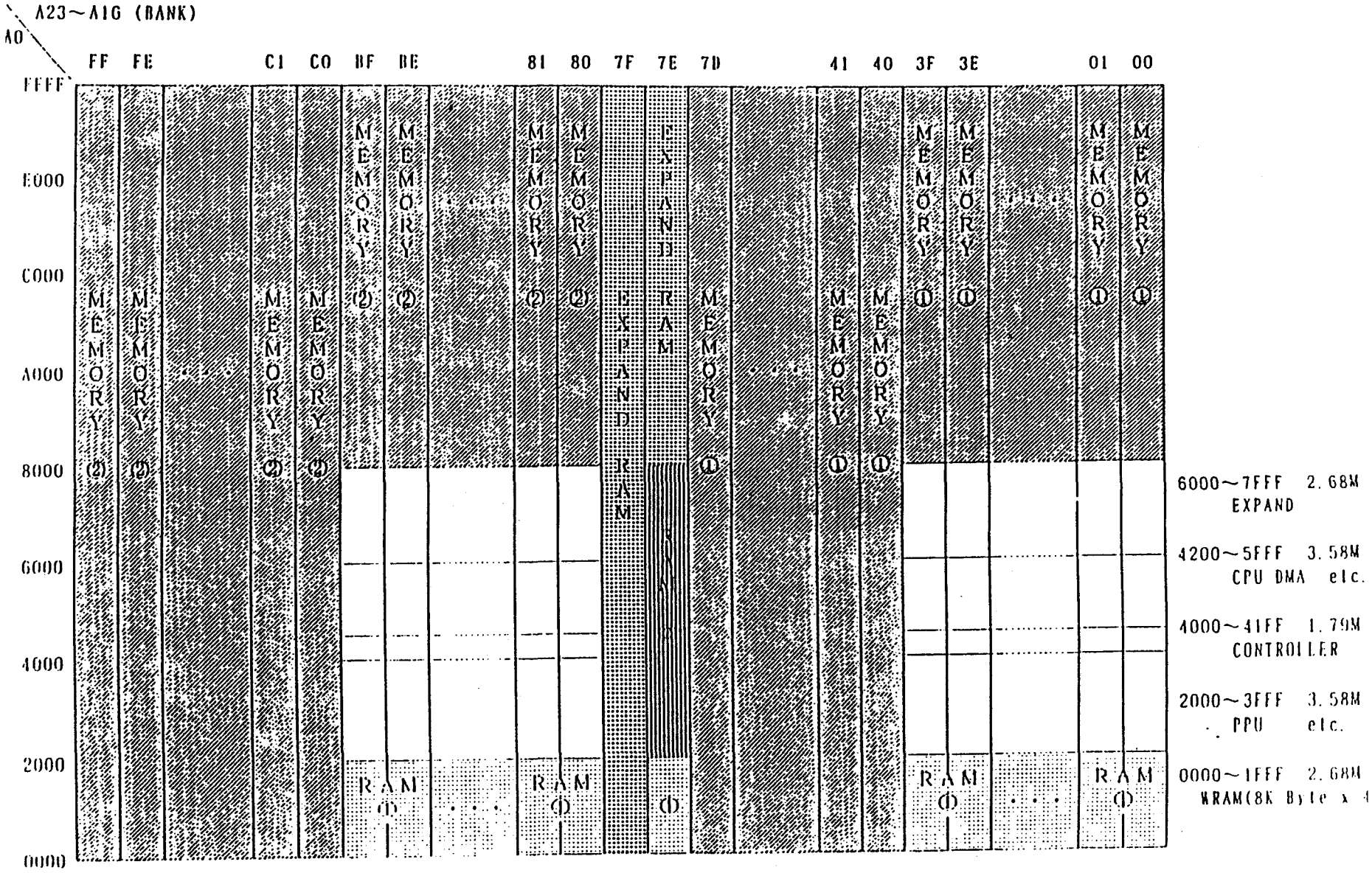
1. CPU CLOCK

The CPU clock can be switched automatically depending on the address to be accessed by the CPU.
There are 3 kinds of clock speed, which are 3.58MHz, 2.68MHz, 1.79MHz, and they can be used according to the device speed (ROM, RAM, LSI and etc.).
If the ROM and RAM of middle speed (access time less than 200ns) are used in the cartridge, it will be mapped to the address area (2.68MHz). If high speed (access time less than 120ns) are used, it will be mapped to the address area (3.58MHz).
[At present (as of January, 1989), because most of the ROM and the RAM used in the video games are designed for more than 150ns speed, 2.68MHz clock is used as the standard.]
Please refer to the "Frequency & Address Mapping" for the relation between the address and the clock.
Two clocks (2.68MHz & 3.58MHz) can be selected by setting "D0" of register <420DH> for the range of memory ㋐ shown on illustration. And 2.68MHz is set as default.
The CPU is operated internally with 3.58MHz clock speed.
[Regardless of the address, the DMA will be operated with 2.68MHz clock speed.]

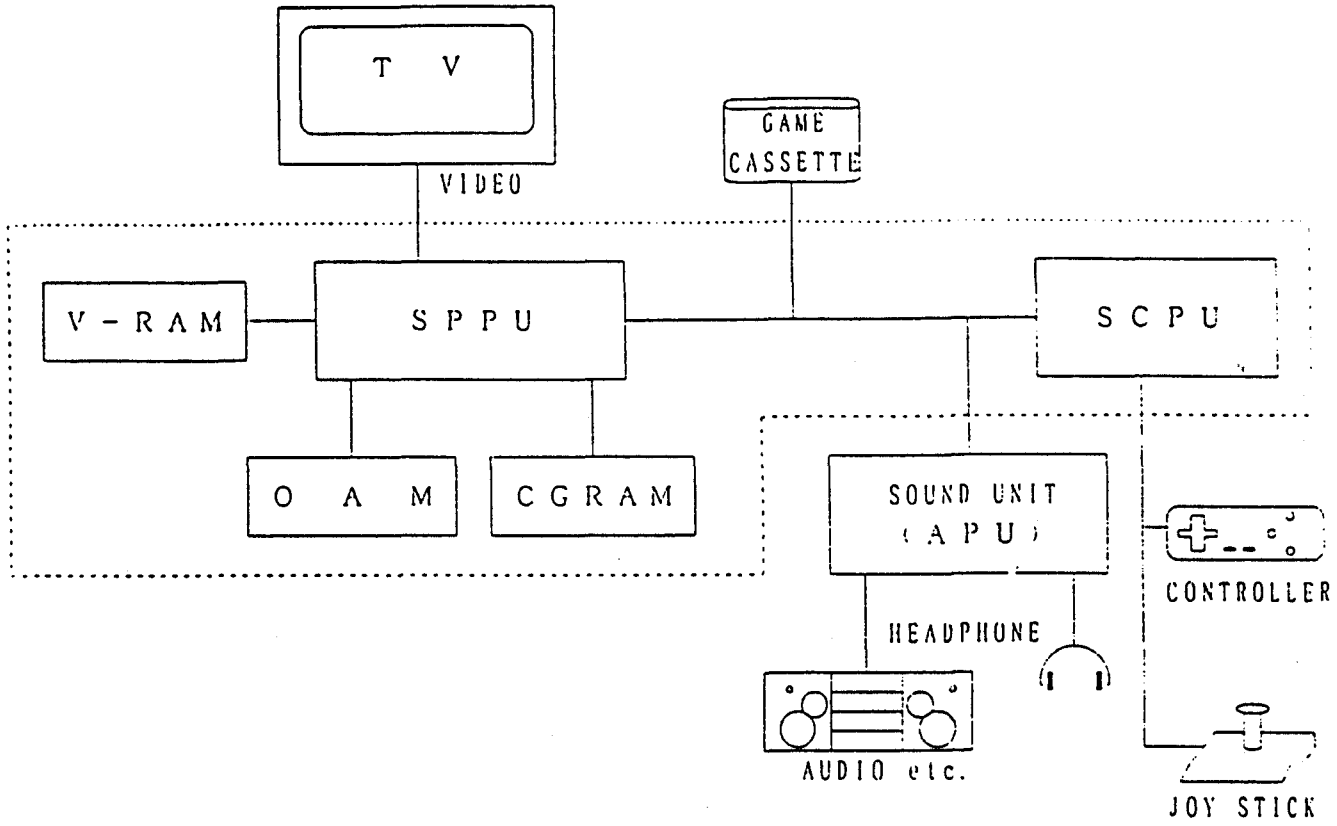
2. ADDRESS MAP

Please refer to the "Frequency & Address Mapping".
The WRAM (8K-Byte) is mapped to the address (0000～1FFF) of the bank (00 ～3F),(80 ～BF) and 7E.
Because this is the WRAM used as common bank, this 8K-Byte can be accessed from any bank described above.
Also, the WRAM (24K-Byte) is mapped to the address (2000 ～ 7FFF) of the bank 7E. Therefore, the WRAM (32K-Byte in total) is included in the SFX unit. The address (8000 ～ FFFF) of the bank 7E and the address (0000～ FFFF) of the bank 7F are provided as extra area for expanded WRAM.
Also, the address "2000～ 5FFF" of the bank "00～3F" and "80 ～ BF" are reserved as a register area of the S-PPU, DMA, etc.
Also, because this basically is reserved as a common bank area, the S-PPU and the DMA register can be accessed from any bank.

CPU SYSTEM CLOCK (FREQUENCY & ADDRESS MAP)



§ 2 2 HARDWARE CONFIGURATION



§ 22.1 NAME & FUNCTION

S C P U (C P U) . . . . . . This is a Central Processing Unit for the SFX.
This is equivalent to the SFX's brains. forwards the game according to the program data in cassette and has the useful function for the game.

S P P U (P P U) . . . . . . This is a Picture Processing Unit for SFX.
This is equivalent to the SFX's hands or legs. which generates various pictures according to the control from the CPU and has the function to vary image expression.

S O U N D U N I T (A P U) This is a Audio Processing Unit.
This is equivalent to the SFX's mouth. which generates produces necessary music or sound effect for the game and has the function to vary sound expression.

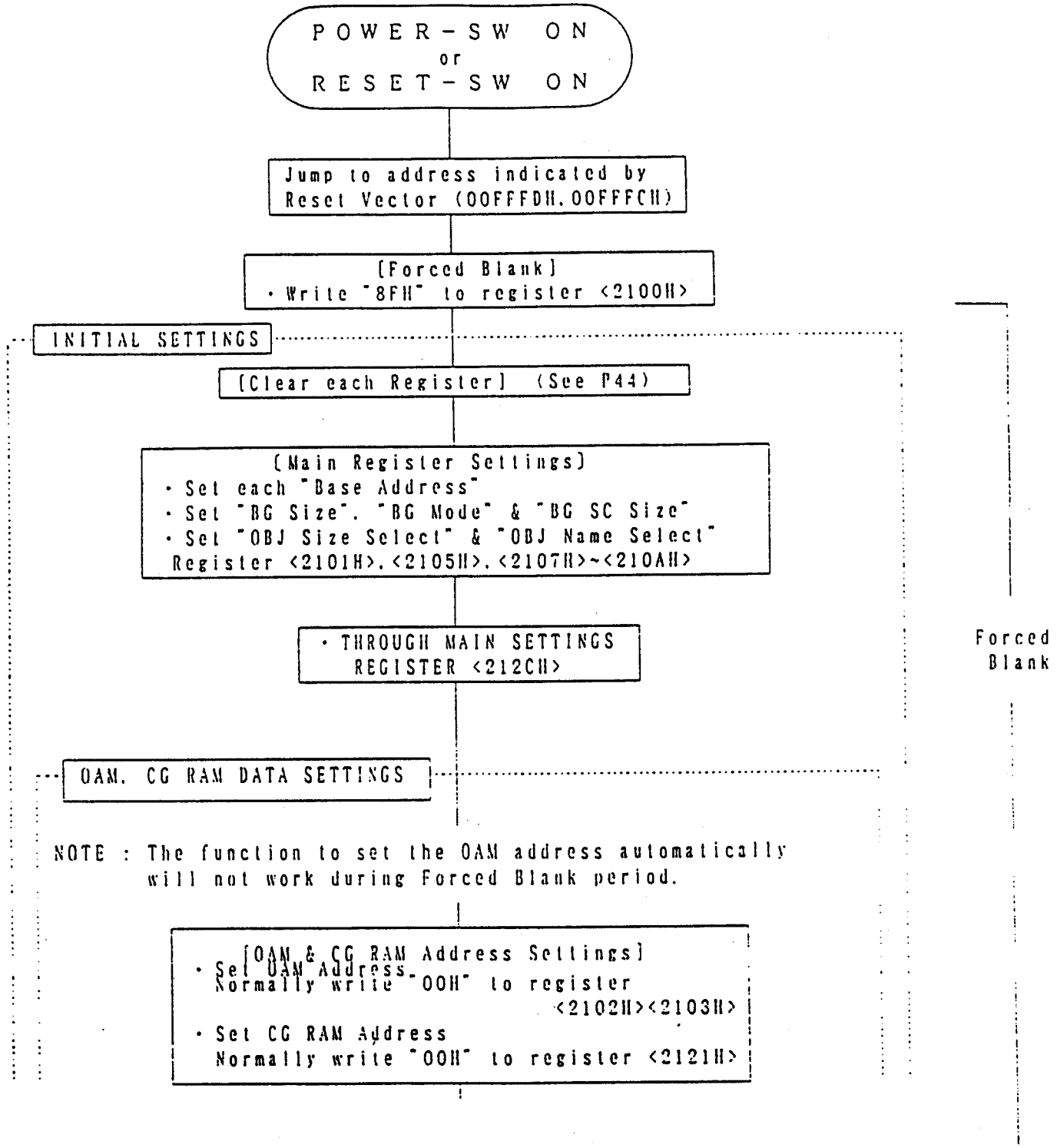
GAME CASSETTE・・ This is the memory to store necessary data. which is program data, character data or sound data.

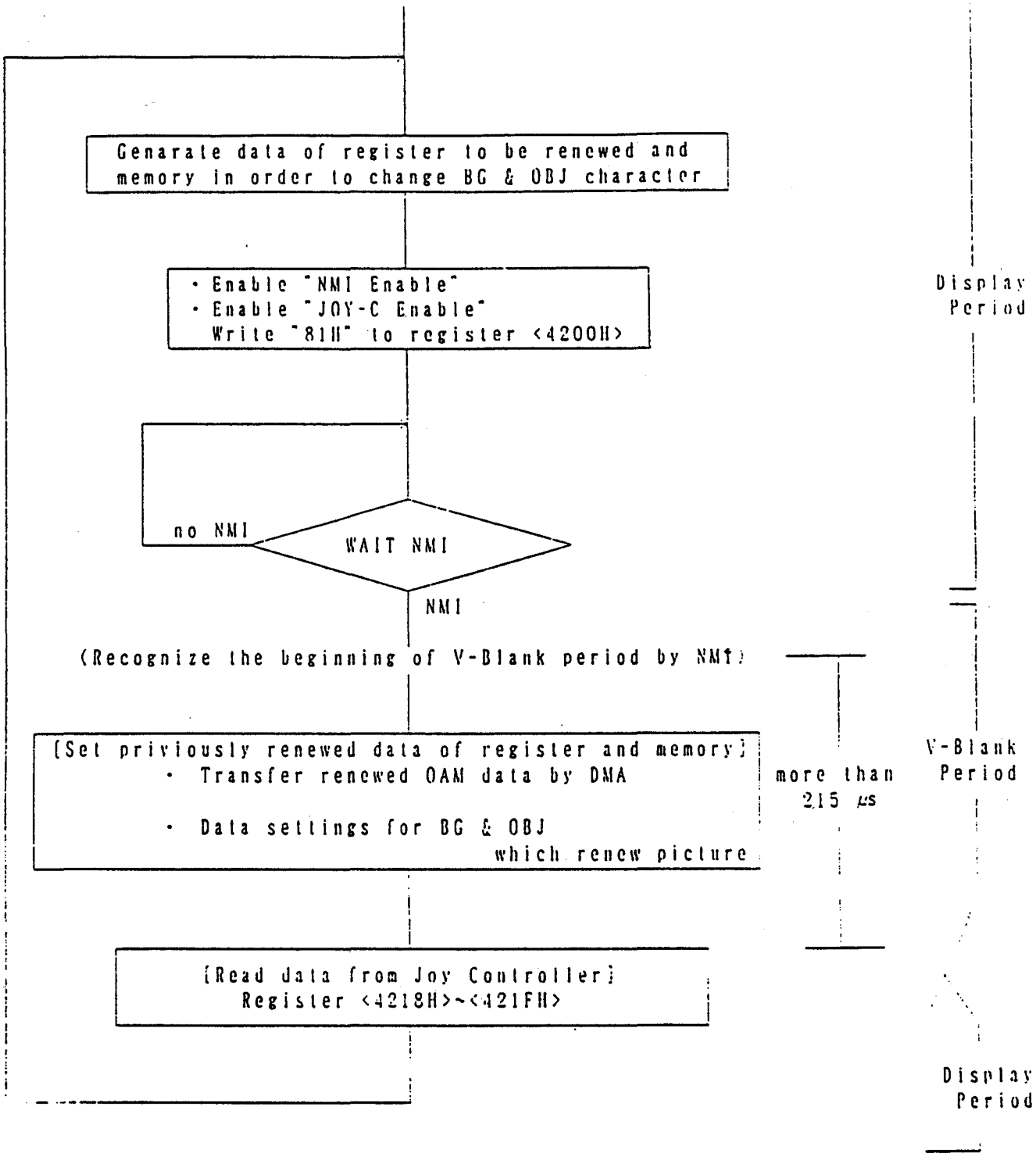
OAM・・・・・・・・・・・・ This is a Object Attribute Memory (OAM). This is used to store necessary data to move characters, such as the hero or enemy in the game.

CGRAM・・・・・・・・・・ This is a Color Generator RAM (CGRAM). This is used to store color data in order to color character data.

VRAM・・・・・・・・・・・ This is a video RAM (VRAM). This is used to store character data for the background characters.

§2.3 SYSTEM FLOWCHART




Genarate data of register to be renewed and memory in order to change BG & OBJ character
• Enable "NMI Enable"
• Enable "JOY-C Enable"
Write "81H" to register <4200H>
no NMI
WAIT NMI
NMI
(Recognize the beginning of V-Blank period by NMI)
[Set priviously renewed data of register and memory]
• Transfer renewed OAM data by DMA
• Data settings for BG & OBJ which renew picture
more than 215 μs
[Read data from Joy Controller]
Register <4218H>~<421FH>
Display Period
V-Blank Period
Display Period

§ 2 4 PROGRAMMING WARNINGS

- There are registers (<210DH>～<2114H>, <211BH>～<2120H>), which must be accessed in the order of Low and High twice.
  If the number of accessing the register (write twice or read twice) becomes unknown, please initialize as follows:

OAM, CGRAM, VRAM	Set the address again
Other Registers (Write)	The lower data should be written more than one time, and the higher data should be written.
H/V Counter Read	When reading the SC78 status register <213FH> it will be initialized. The data should be read in the order of Low and High.

- The period which can be accessed for the register is as follows:

V-RAM, OAM	Forced Blank or V-Blank period only
CG-RAM	Forced Blank, V-Blank or H-Blank period only
Other Register (Write)	All period (However, when writting the data, the picture may not be displayed properly.)
Other Register (Read)	All period (However, the data which may be changed during display period may not be read properly.)

- The address space for the V-RAM is 64K-word (1-word = 16-bit) maximum. 32K-word memory is installed in the SFX unit.
- When the V-RAM is accessed from the CPU, the address counter will be increased automatically.
  For the V-RAM increment mode, please use the register mode designated by the instruction.
- When the V-RAM is read continuously after the V-RAM address has been set, the address will not be increased for the first data only.
  Therefore, when reading the data continuously, the first data for the address increment should be read as a dummy data after the V-RAM address has been set.
- The top color data of each CG color data palette is transparency.
  Because the transparency is a color which is not displayed, so that any color can be set.
  However, the color data of the CG address (00H) is normally black (background).
- Even though 9-Bit is provided as the OAM H-position, the value <100H> must not be used.

§ 2 4 REGISTER CLEAR (INITIAL SETTINGS)

[Because this is a recommended settings for beginners. it is not necessary to perform according to this way.
However, the register status is not stable when power is turned on. initial settings must be done.]

ADDRESS(HEX)	DATA(HEX)
< 2 1 0 0 >	8 F (Forced Blank)
< 2 1 0 1 >	0 0
< 2 1 0 2 >	0 0
< 2 1 0 3 >	0 0
< 2 1 0 4 >	(OAM DATA)
< 2 1 0 5 >	0 0
< 2 1 0 6 >	0 0
< 2 1 0 7 >	0 0
< 2 1 0 8 >	0 0
< 2 1 0 9 >	0 0
< 2 1 0 A >	0 0
< 2 1 0 B >	0 0
< 2 1 0 C >	0 0
	(LOW) (HIGH)
< 2 1 0 D >	0 0 0 0
< 2 1 0 E >	0 0 0 0
< 2 1 0 F >	0 0 0 0
< 2 1 1 0 >	0 0 0 0
< 2 1 1 1 >	0 0 0 0
< 2 1 1 2 >	0 0 0 0
< 2 1 1 3 >	0 0 0 0
< 2 1 1 4 >	0 0 0 0
< 2 1 1 5 >	8 0
< 2 1 1 6 >	0 0
< 2 1 1 7 >	0 0
< 2 1 1 8 >	(VRAM DATA)
< 2 1 1 9 >	(VRAM DATA)
< 2 1 1 A >	0 0
< 2 1 1 B >	0 0 0 1
< 2 1 1 C >	0 0 0 0
< 2 1 1 D >	0 0 0 0
< 2 1 1 E >	0 0 0 1
< 2 1 1 F >	0 0 0 0

ADDRESS(HEX)	DATA(HEX)
< 2 1 2 0 >	0 0 0 0
< 2 1 2 1 >	0 0
< 2 1 2 2 >	(CG DATA)
< 2 1 2 3 >	0 0
< 2 1 2 4 >	0 0
< 2 1 2 5 >	0 0
< 2 1 2 6 >	0 0
< 2 1 2 7 >	0 0
< 2 1 2 8 >	0 0
< 2 1 2 9 >	0 0
< 2 1 2 A >	0 0
< 2 1 2 B >	0 0
< 2 1 2 C >	0 0
< 2 1 2 D >	0 0
< 2 1 2 E >	0 0
< 2 1 3 0 >	3 0
< 2 1 3 1 >	0 0
< 2 1 3 2 >	E 0
< 2 1 3 3 >	0 0
< 4 2 0 0 >	0 0
< 4 2 0 1 >	F F
< 4 2 0 2 >	0 0
< 4 2 0 3 >	0 0
< 4 2 0 4 >	0 0
< 4 2 0 5 >	0 0
< 4 2 0 6 >	0 0
< 4 2 0 7 >	0 0
< 4 2 0 8 >	0 0
< 4 2 0 9 >	0 0
< 4 2 0 A >	0 0
< 4 2 0 B >	0 0
< 4 2 0 C >	0 0
< 4 2 0 D >	0 0

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