# **SUMMARY OF REGISTERS**

### **REGISTERS (WRITE) S-PPU**

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0			
2100H	Blanking				FADE IN/OUT (0~15)						
2101H	OBJ	Size Sel	ect	OBJ Home	ne Select OBJ Home Base Address						
2103H				OAM A	ddress	•					
2103H	OAM Priority Rotation MSB										
2104H	OAM Data (Low, High)										
2105H	BG4	BG 16 x BG3	16 Size BG2	BG1	BG3 Priority	ВС	Mode (0~	7)			
2106H		Mosaic Si	ze (0~15)		BG4	Mosaic BG3	Enable BG2	BG1			
2107H			BG1 SC Ba	se Address	5		BG1 SC	Size			
2108H			BG2 SC Ba	se Address	5		BG2 SC	Size			
2109H			BG3 SC Ba	se Address	5		BG3 SC	Size			
210AH			BG4 SC Ba	se Address	BG4 SC Size						
210BH	ВС	G2 Home B	ase Addres	SS	BG1 Home Base Address						
210CH	ВС	G4 Home B	ase Addres	SS	BG3 Home Base Address						
210DH			BG1	L H-Offset	t (Low, High)						
210EH			BG1	L V-Offset	(Low, Hi	gh)					
210FH			BG2	? H-Offset	(Low, Hi	gh)					
2110H			BG2	V-Offset	(Low, Hi	gh)					
2111H			BG3	H-Offset	(Low, Hi	gh)					
2112H			BG3	V-Offset	t (Low, High)						
2113H			BG <sup>2</sup>	H-Offset	t (Low, High)						
2114H			BG <sup>2</sup>	V-Offset	(Low, Hi	gh)					
2115H	H-L Inc				l	M Address Traphic	Sequence SC Inc				
2116H				V-RAM Add	ress (Low)	)					
2117H			\	/-RAM Addr	ess (High	)					
2118H				V-RAM Da	ta (Low)						
2119H				V-RAM Da	ta (High)						
211AH	Screen Over						Screer V	Flip H			

### **REGISTERS (WRITE) S-PPU**

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0			
211BH	Matrix Parameter A (Low, High)										
211CH	Matrix Parameter B (Low, High)										
211DH	Matrix Parameter C (Low, High)										
211EH		Matrix Parameter D (Low, High)									
211FH			Center	Position	n X (Low,	High)					
2120H			Center	Position	n Y (Low,	High)					
2121H				CG-RAM	Address						
2122H			CG-	-RAM Data	(Low, Hig	gh)					
2123H	W2 EN	BG2 W IN/OUT	indow   W1 EN	IN/OUT	W2 EN	BG1 W IN/OUT	indow   W1 EN	IN/OUT			
2124H	W2 EN	BG4 W IN/OUT	indow   W1 EN	IN/OUT	W2 EN	BG3 W IN/OUT	indow   W1 EN	IN/OUT			
2125H	W2 EN	Color IN/OUT	Window   W1 EN	IN/OUT	W2 EN	OBJ W IN/OUT	indow   W1 EN	IN/OUT			
2126H	Window HO Position (0~255)										
2127H	Window H1 Position (0~255)										
2128H	Window H2 Position (0~255)										
2129H			Wind	ow H3 Pos	ition (0~	255)					
212AH	ВС	G4	l BC	Window 3	-	G2	ı B	G1			
212BH					Co <sup>-</sup>	Window lor	Logic 0	ВЈ			
212CH				OBJ	TI BG4	hrough Mai	in   BG2	BG1			
212DH				OBJ	T BG4	hrough Su   BG3	b BG2	BG1			
212EH				OBJ	Throug BG4	h Main (W   BG3	indow)	BG1			
212FH				OBJ	Through BG4	gh Sub (Wi	indow)   BG2	ı BG1			
2130H	Main SW	Window (M1/M0)	ON/OFF Sub SW	(S1/S0)			CG ADD Enable	Direct Select			
2131H	ADD/SUB	1/2 Enable	BACK	ОВЈ	ADD or SI BG4	UB Enable BG3	BG2	BG1			
2132H	Blue	Green	Red	Color Cons	stant Data Color	a Brillianc	e Data				
2133H	EXT Sync	EXT Input			Pseudo 512	224/239	OBJ-V Select	Interlace			
2134H				MPY	(Low)						
2135H	MPY (Mid)										
223311	MPY (High)										

### **REGISTERS (READ) S-PPU**

ADDRESS	D7 D6 D5 D4 D3 D2 D1 D0										
2137H	Soft Latch for H/V Counter										
2138H	OAM Data (Low, High)										
2139H		V-RAM Data (Low)									
213AH	V-RAM Data (High)										
213BH		CG Data (Low, High)									
213CH	Output Data of H-Counter (Low, High)										
213DH	Output Data of V-Counter (Low, High)										
213EH	Time Over	Range Over	Master /Slave		5C7	7 Version	Number				
213FH	Field	EXT Latch		NTSC/PAL	5C7	'8 Version	Number				
2140H	APU I/O Port										
2141H	APU I/O Port										
2142H				APU I/	0 Port						
2143H				APU I/	0 Port						

### REGISTERS (WRITE) S-CPU

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0			
4200H	NMI Enable		Timer V-EN	Enable H-EN				Joy-C Enable			
4201H	I/O Port										
4202H	Multiplicand-A										
4203H		Multiplier-B									
4204H		Dividend-C (Low)									
4205H		Dividend-C (High)									
4206H		Divisor-B									
4207H				H-Count	er Timer						
4208H								H-MSB			
4209H				V-Count	er Timer						
420AH		V-MSB									
420BH	CH7 EN	CH6 EN	General CH5 EN	Purpose I	OMA (Enabl	e Flag)   CH2 EN	CH1 EN	CHO EN			
420CH	CH7 EN	CH6 EN	CH5 EN		able Flag)   CH3 EN		CH1 EN	CHO EN			
420DH								2.68 /3.58			

### **REGISTERS (READ) S-CPU**

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0				
4210H	Blank NMI				5A22 Version Number							
4211H	Timer IRQ											
4212H	V-Blank H-Blank Joy-C Enable											
4213H	I/O Port											
4214H		Quotient-A (Low)										
4215H		Quotient-A (High)										
4216H		Product-C / Remainder (Low)										
4217H			Prod	uct-C / Re	mainder (	(High)						
4218H	X X	oy Control	ler I (Lo	ow)   TR								
4219H	A	В	Jo   Select	y Control <sup>°</sup>   Start	ler I (Hi   Up	gh)   Down	Left	Right				
421AH	Jo	y Control	ler II (L	ow)								
421BH		Joy Controller II (High)										
421CH	Joy	Joy Controller III (Low)										
421DH			Joy	Controll	er III (H	igh)						
421EH	Jo	y Control	ler IV (L	ow)								
421FH			Jo	y Controll	er IV (H	gh)						

## REGISTERS (WRITE) S-CPU

(X : Channel <0~7>)

	LICO (11	(A . Clialli	CI (0 1/)								
ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0			
43X0H	CHX CHX T-Org* Type A-Bus Address INC/DEC   Fixed CHX Transfer Word Select							l Select			
43X1H		CHX B-Address									
43X2H		CHX A1 Table Address (Low)									
43X3H		CHX A1 Table Address (High)									
43X4H		CHX A-Table Bank									
43X5H		CHX Data Address (H-DMA) (Low) Number of Byte to be transfered (General purpose DMA)									
43X6H	-	CHX Data Address (H-DMA) (High) Number of Byte to be transfered (General purpose DMA)									
43X7H		CHX Data Bank (H-DMA)									
43X8H		CHX A2 Table Address (Low)									
43X9H		CHX A2 Table Address (Low)									
43XAH	Continue Number of Line										

Note : T-Org means the "Transfer Origination"