Javed Sir Lecture 4&5 (Online); Course: Microprocessor; CSTE-3109; Session: 2017-18; Date: 11/06/2020

Microcontroller and Interfacing Devices:

A **microcontroller** also called MCU (Microcontroller Unit) is a small computer on a single metal-oxide-semiconductor (MOS) integrated circuit (IC) chip. A microcontroller contains one or more CPUs (processor cores) along with memory and programmable input/output peripherals. Program memory in the form of ferroelectric RAM, NOR flash ROM also often included on chip, as well as a small amount of RAM. Microcontrollers are designed for embedded applications, in contrast to the microprocessors used in personal computers or other general purpose applications consisting of various discrete chips.

The **Intel MCS-51** (commonly termed **8051**) is a single chip microcontroller (MCU) series developed by Intel in 1981 for use in embedded systems.
8051 microcontroller is designed by Intel in 1981. It is an 8-bit microcontroller. It is built with 40 pins DIP (dual inline package), 4kb of ROM storage and 128 bytes of RAM storage, 2 16-bit timers. It consists of are four parallel 8-bit ports, which are programmable as well as addressable as per the requirement and a serial port for transmitting and receiving data. An on-chip crystal oscillator (OSC) is integrated in the microcontroller having crystal frequency of 12 MHz.

In the following diagram, the system bus connects all the support devices to the CPU. The system bus consists of an 8-bit data bus, a 16-bit address bus and bus control signals. All other devices like program memory, ports, data memory, serial interface, interrupt control, timers, and the CPU are all interfaced together through the system bus.

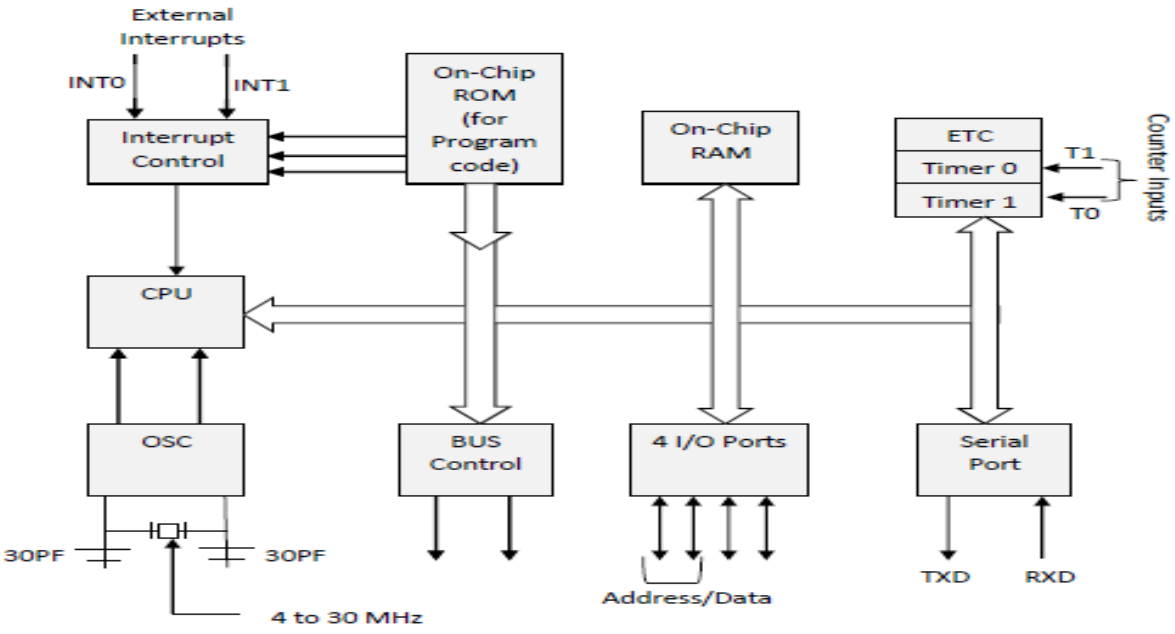
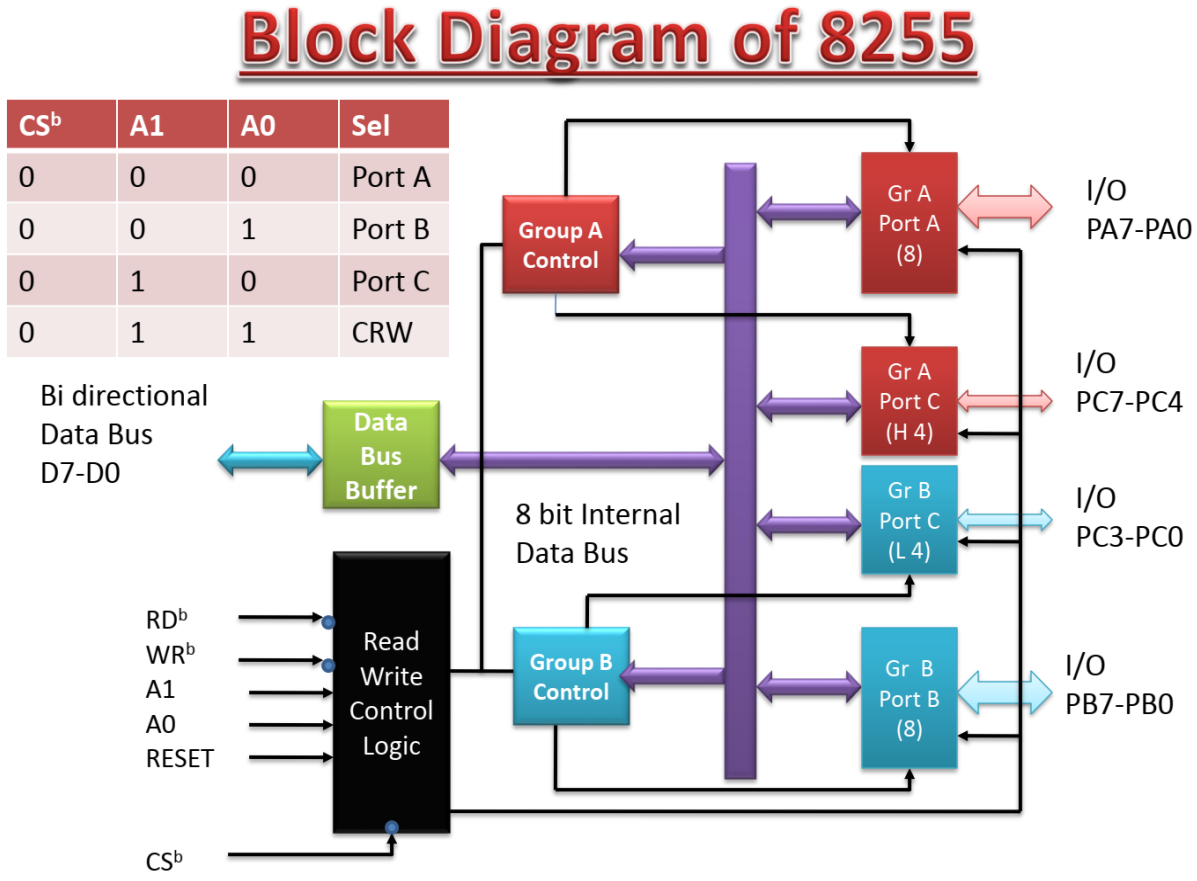


Figure 1: Architecture of **Intel MCS-51** (commonly termed **8051**).

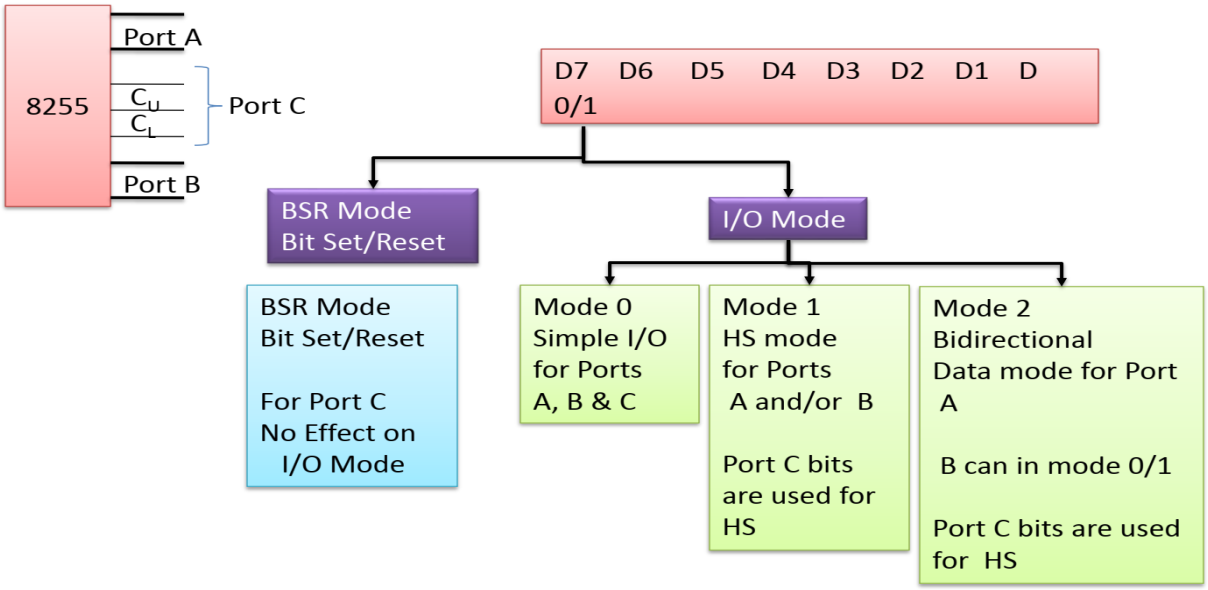
8255 (I/O Controller):



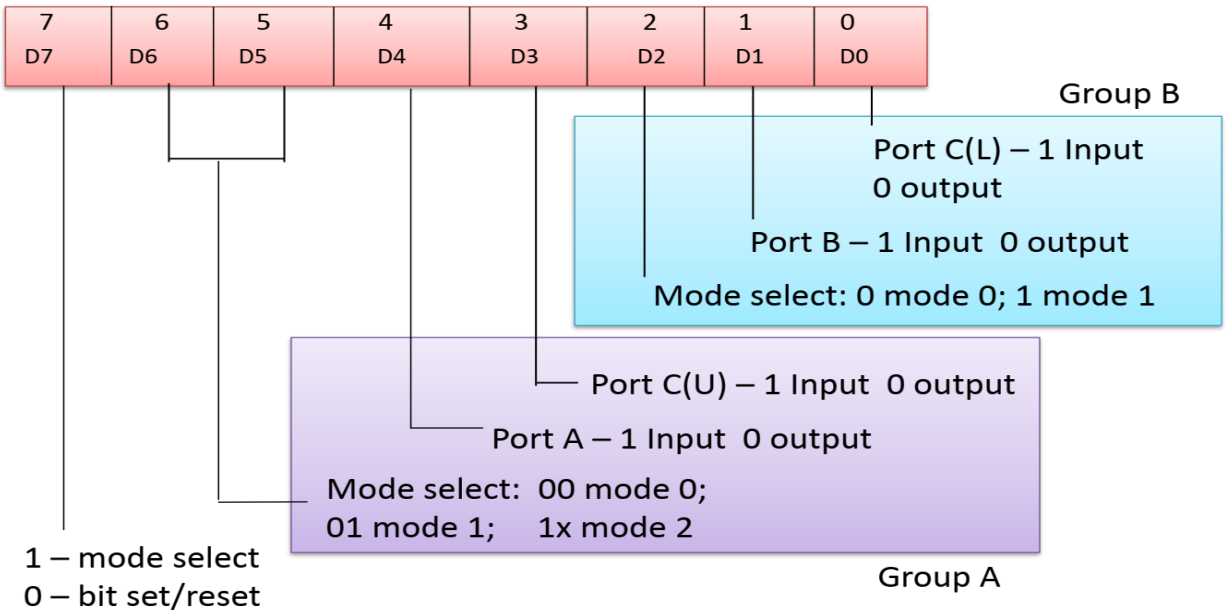
Port A= 8 I/O lines= PA7-PA0
Port B= 8 I/O lines= PB7-PB0
Port C= 4 I/O lines= PC7-PC4= Upper lines of Port C
Port C= 4 I/O lines= PC3-PC0= Lower lines of Port C
I/O= Input/Output
CRW= Control Register Word= Store 8-bit data= D7-D0
RD^b= Read Bubble line= Active with 0
WR^b= Write Bubble line= Active with 0
CS^b= Chip Select Bubble line= Active with 0
A0,A1= Address lines

For READ operation: RD^b=0, WR^b=1, CS^b=0
For WRITE operation: RD^b=1, WR^b=0, CS^b=0

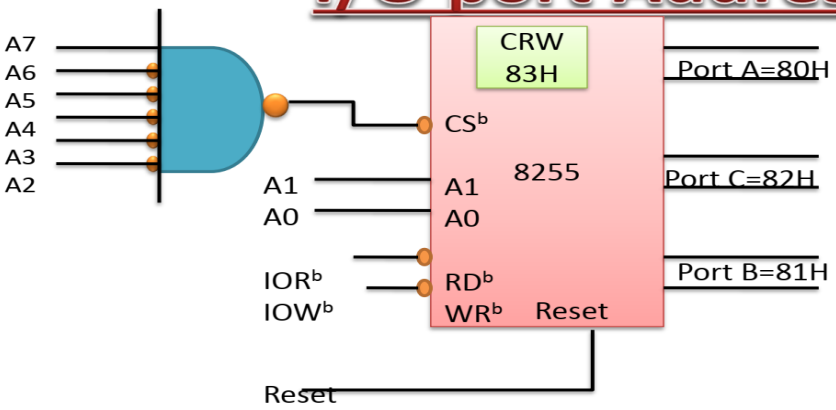
Ports & Modes in 8255



Ports & Modes in 8255 : Control register



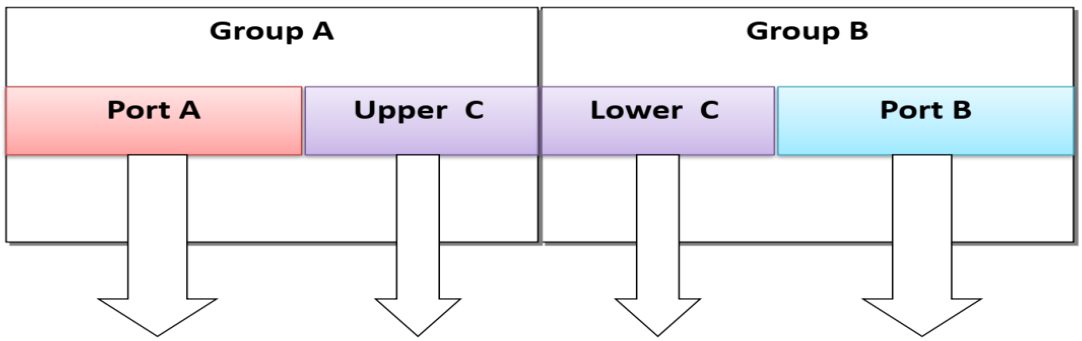
I/O port Addressing



CS^b	A1 A0	HEX Address	Port
A7 A6 A5 A4 A3 A2 1 0 0 0 0 0	A1 A0 0 0	= 80H	A
	0 1	=81H	B
	1 0	=82H	C
	1 1	=83H	Control Register

Ports

- Control register controls the overall operation of 8255
- All three ports A, B and C are grouped into two



Operation modes

- 8255 has three modes:
  - Mode 0: basic input-output
  - Mode 1: Strobbed input-output
  - Mode 2: Strobbed bi-directinal bus I/O
- In mode 0
  - Two 8-bit ports and two 4-bit ports
  - Any port can be input or output
  - Outputs are latched, inputs are not latched

Operation modes

- In mode 1:

  -Three ports are divided into two groups

  -Each group contains one 8-bit port and one 4-bit control/data port

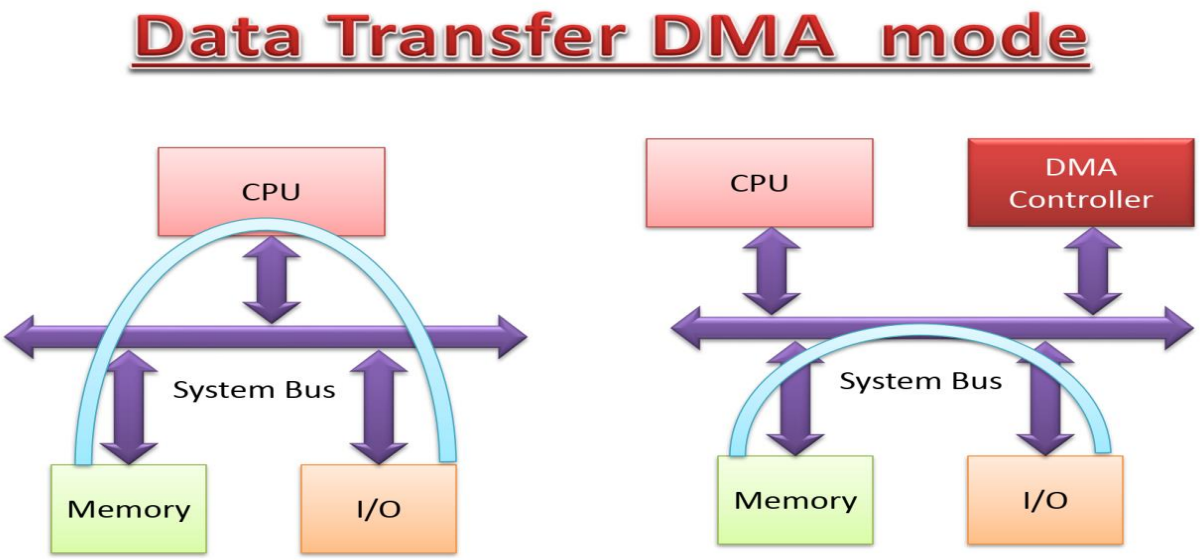
  - 8-bit port can be either input or output and both latched

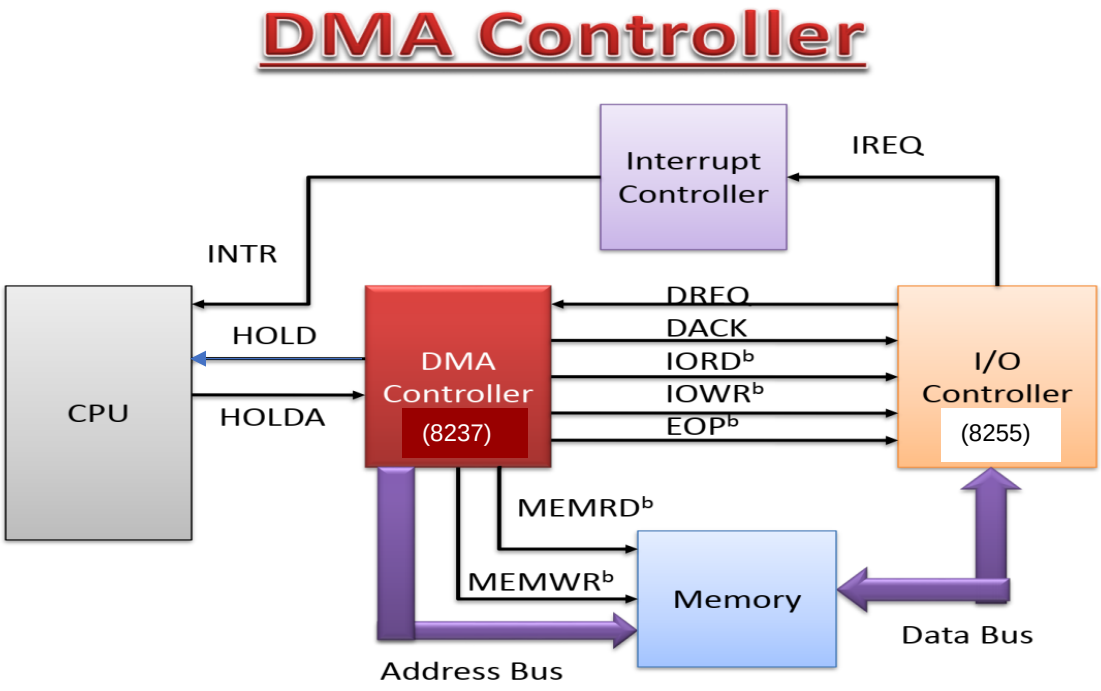
  - 4-bit port used for control and status of 8-bit data port
- In mode 2
  - Only port A is used
  - Port A becomes an 8-bit bidiectional bus
  - Port C acts as control port (only pins PC3-PC7 are used)

Latched= Closed, Strobed input-output= Handshake input-output

8237 (DMA Controller):

DMA: Direct memory access (**DMA**) is a feature of computer systems that allows certain hardware subsystems (such as I/O devices) to access main system memory independently without intervention from CPU.





DMA Controller interfaces with CPU, I/O Controller, Interrupt Controller and Memory.

HOLD and HOLDA= Hold signal and Hold Acknowledge signal= Handshaking signals between DMA controller and CPU.

DREQ, DACK, IORD^{b}, IOWR^{b} and EOP^{b}= DMA request signal, DMA acknowledge signal, Input-Output read signal, Input-Output write signal, End of operation signal= Handshaking signals between DMA controller and I/O controller.

MEMRD^{b}, MEMWR^{b}= Memory read signal, Memory write signal between DMA controller and Memory.

DMA Operation

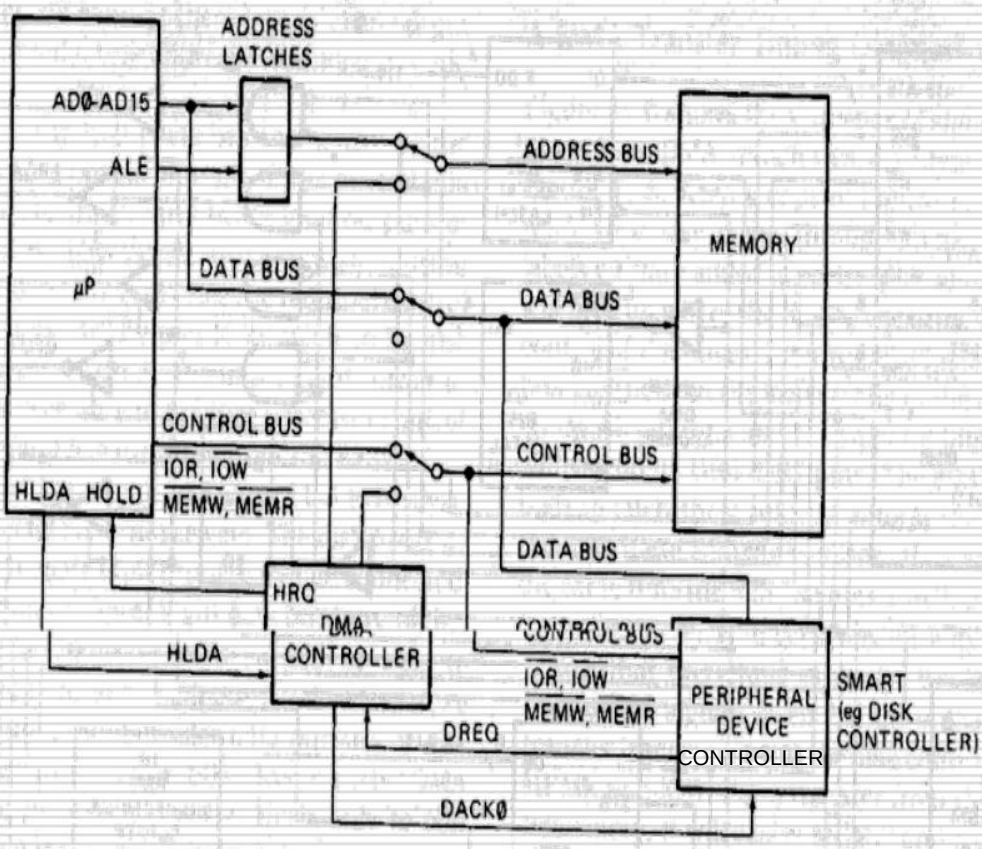


FIGURE 11-4 Block diagram showing how a DMA controller operates in a microcomputer system.

DMA operation:

1. At first, DMA Controller sends a request signal HOLD to microprocessor (CPU) then CPU sends an acknowledge to DMA controller. As a result, CPU will borrow address, date and control lines by address latch to memory or I/O devices and stop its operation for some times.
2. After that, DMA controller operates independently with memory or I/O with the help of address, data and control lines and also two handshaking signals. The handshaking signals, one from Peripheral Device controller (I/O Controller) to DMA controller (DREQ) and other from DMA controller to Peripheral Device controller (DACK).
3. DMA controller interfaces with memory for READ or WRITE operation by the help of two control signals $\overline{MEMR}$ and $\overline{MEMW}$.
4. DMA controller interfaces with I/O devices for READ or WRITE operation by the help of two control signals $\overline{IOR}$ and $\overline{IOW}$.

Notice:

1. **All students must be studied all of my class lectures and On-line lectures to take preparation for term final examination. After reopen Campus, I will take two review classes before term final examination.**
2. **All my assignments must be submitted on 25 June 2020 to my email.**
3. **All assignments must be in hand written form, then take snap shots and save in a PDF file.**
4. **Stay home, be safe.**

Lecture prepared by

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