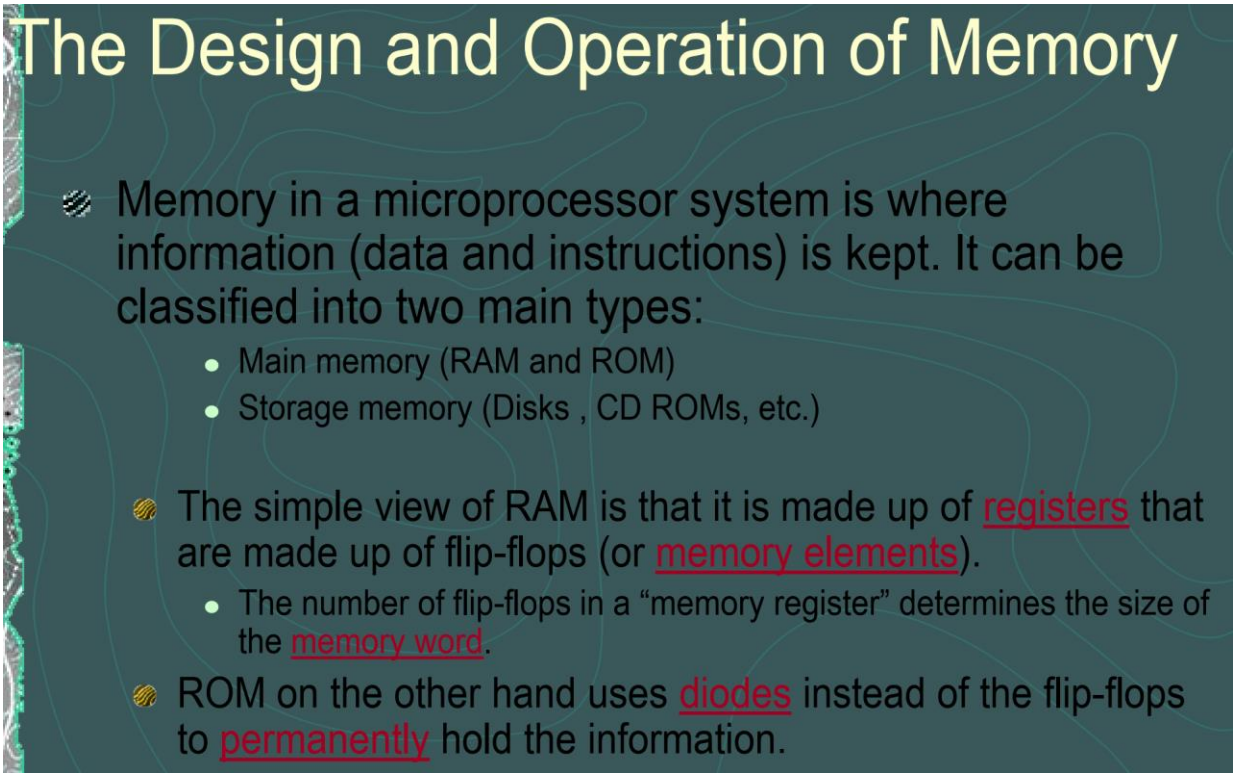
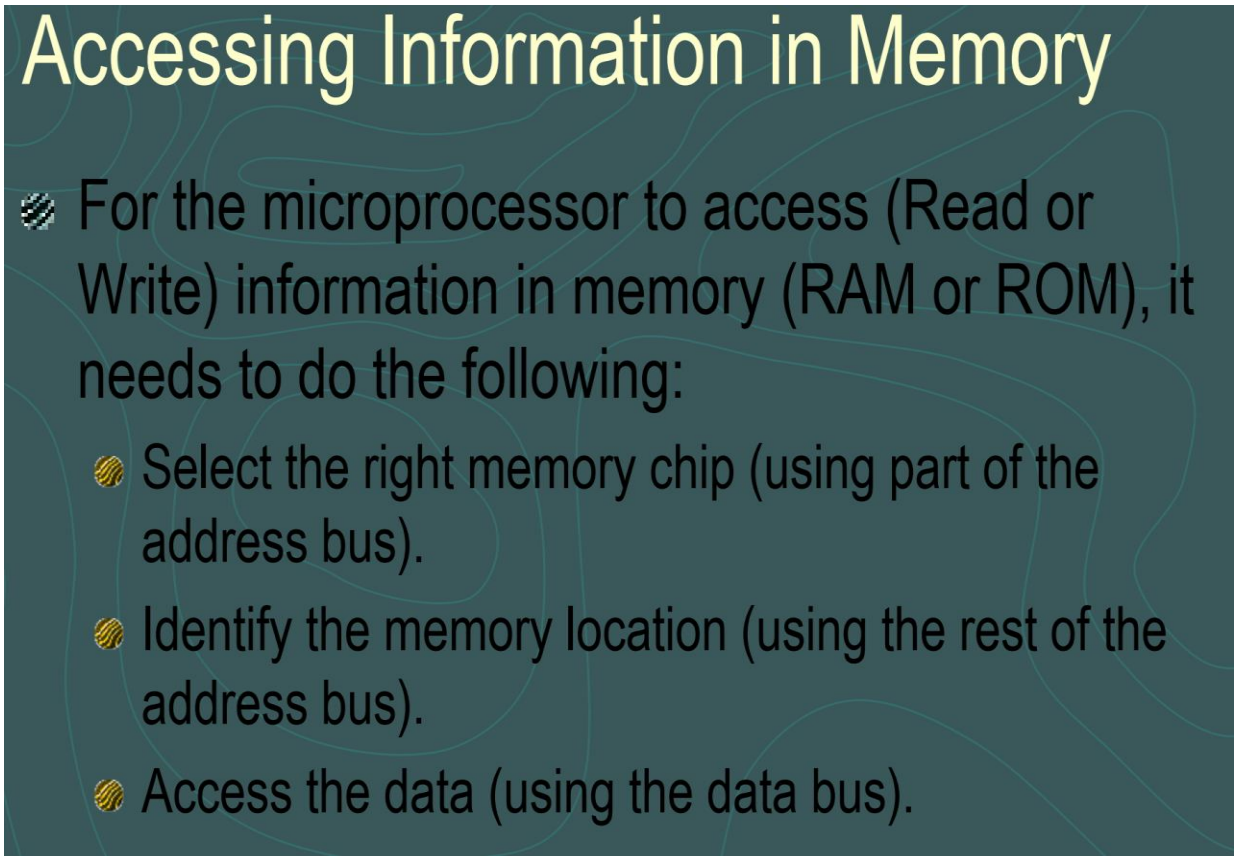
Memory Interfacing of 8085:





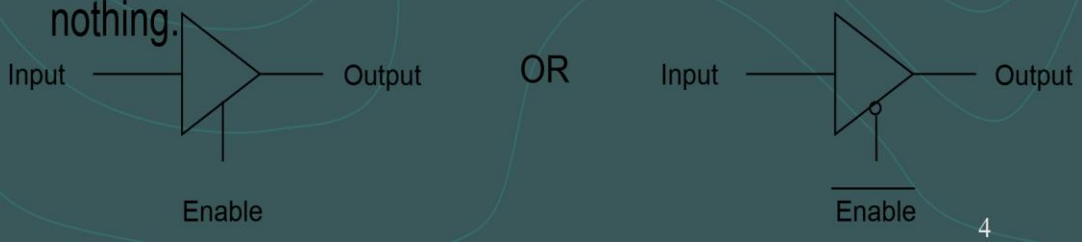
Tri-State Buffers

- An important circuit element that is used extensively in memory.
- This buffer is a logic circuit that has three states:
  - Logic 0, logic1, and high impedance.
  - When this circuit is in high impedance mode it looks as if it is disconnected from the output completely.

The Output is Low | The Output is High | High Impedance

The Tri-State Buffer

- This circuit has two inputs and one output.
  - The first input behaves like the normal input for the circuit.
  - The second input is an "**enable**".
    - If it is set high, the output follows the proper circuit behavior.
    - If it is set low, the output looks like a wire connected to nothing.



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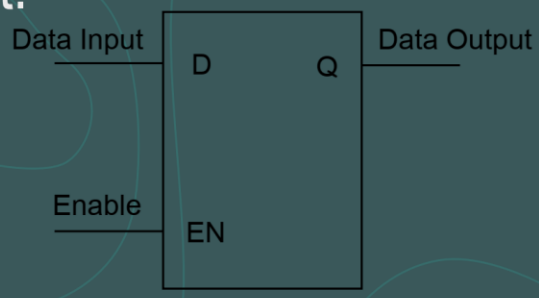
The Basic Memory Element

- The basic memory element is similar to a D latch/FF
- This latch has an input where the data comes in. It has an enable input and an output on which data comes out.



The Basic Memory Element

- The WR signal controls the input buffer.
  - The bar over WR means that this is an active low signal.
  - So, if WR is 0 the input data reaches the latch input.
  - If WR is 1 the input of the latch looks like a wire connected to nothing.
- The RD signal controls the output in a similar manner.

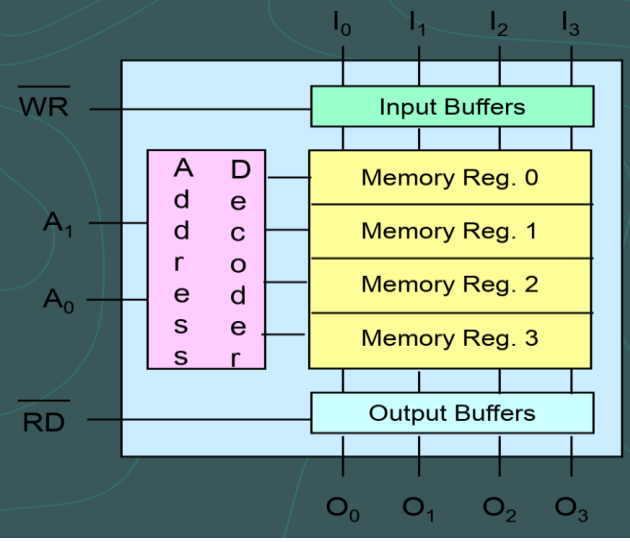
The Design of a Memory Chip

- Using the RD and WR controls we can determine the direction of flow either into or out of memory. Then using the appropriate Enable input we enable an individual memory register.

- What we have just designed is a memory with 4 locations and each location has 4 elements (bits). This memory would be called 4 X 4 [Number of location X number of bits per location].

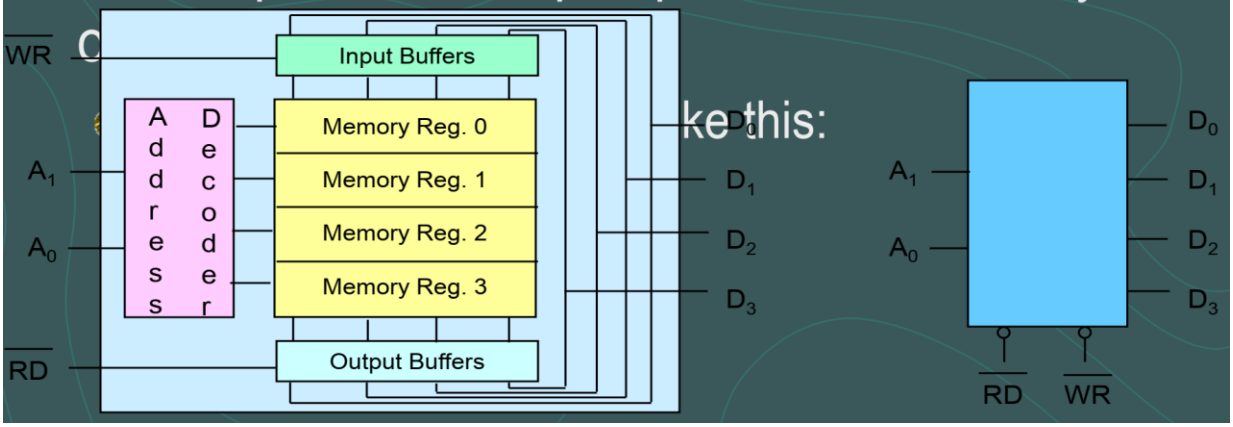
The Design of a Memory Chip

- So, the previous diagram would now look like the following:



The Design of a Memory Chip

- Since we have tri-state buffers on both the inputs and outputs of the flip flops, we can actually use c



Dimensions of Memory

- Memory is usually measured by two numbers: its length and its width (Length X Width).
  - The length is the total number of locations.
  - The width is the number of bits in each location.
- The length (total number of locations) is a function of the number of address lines.

  # of memory locations = $2^{(\#\text{ of address lines})}$
  - So, a memory chip with 10 address lines would have

    2^{10} = 1024 locations (1K)
  - Looking at it from the other side, a memory chip with 4K locations would need

    Log_2 4096=12 address lines

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The 8085 and Memory

- The 8085 has 16 address lines. That means it can address

  2^{16} = 64K memory locations.

  - Then it will need 1 memory chip with 64 k locations, or 2 chips with 32 K in each, or 4 with 16 K each or 16 of the 4 K chips, etc.

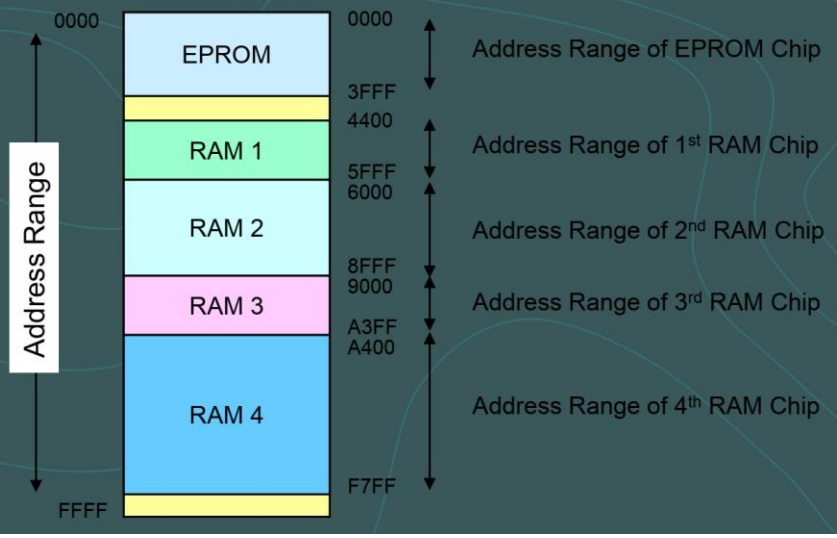
- how would we use these address lines to control the multiple chips?

The steps of writing into Memory

- What happens when the programmer issues the STA instruction?
  - The microprocessor would turn **on** the WR control (WR = 0) and turn **off** the RD control (RD = 1).
  - The address is applied to the address decoder which generates a **single** Enable signal to turn on **only one** of the memory registers.
  - The data is then applied on the data lines and it is stored into the enabled register.

Memory Map and Addresses

- The memory map is a picture representation of the address range and shows where the different memory chips are located within the address range.

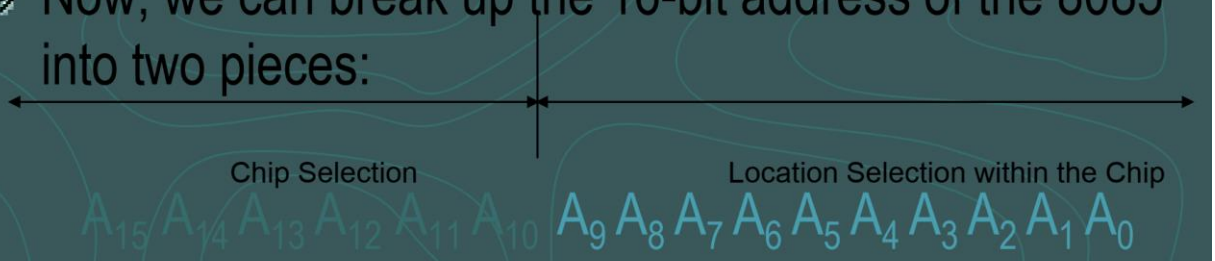


The 8085 and Address Ranges

- The 8085 has 16 address lines. So, it can address a total of 64K memory locations.
  - If we use memory chips with 1K locations each, then we will need 64 such chips.
  - The 1K memory chip needs 10 address lines to uniquely identify the 1K locations. ($\log_2 1024 = 10$)
  - That leaves 6 address lines which is the exact number needed for selecting between the 64 different chips ($\log_2 64 = 6$).

The 8085 and Address Ranges

- Now, we can break up the 16-bit address of the 8085 into two pieces:



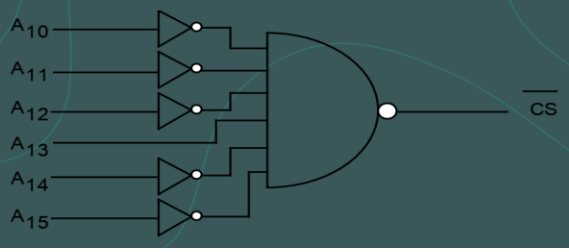
  - Depending on the combination on the address lines A_{15} - A_{10} , the address range of the specified chip is determined.

Chip Selection Example

- Assume that we need to build a memory system made up of 4 of the 4 X 4 memory chips we designed earlier.
- We will need to use 2 inputs and a decoder to identify which chip will be used at what time.
- The resulting design would now look like the one on the following slide.

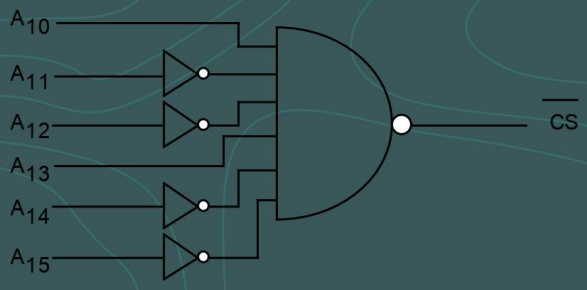
Chip Select Example

- A chip that uses the combination A_{15} - A_{10} = 001000 would have addresses that range from 2000H to 23FFH.
  - Keep in mind that the 10 address lines on the chip gives a range of 00 0000 0000 to 11 1111 1111 or 000H to 3FFH for each of the chips.
  - The memory chip in this example would require the following circuit on its chip select input:



Chip Select Example

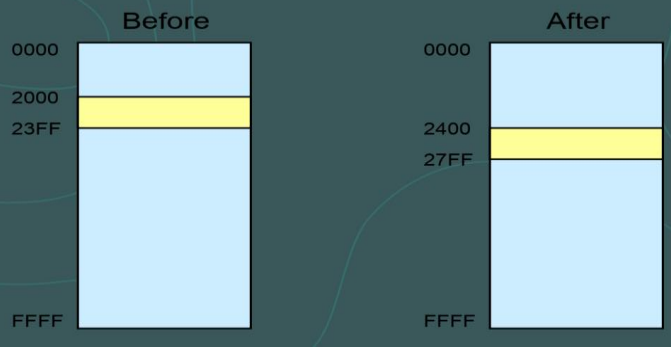
- If we change the above combination to the following:



  - Now the chip would have addresses ranging from: 2400 to 27FF.
  - Changing the combination of the address bits connected to the chip select changes the address range for the memory chip.

Chip Select Example

- To illustrate this with a picture:
  - in the first case, the memory chip occupies the piece of the memory map identified as before.
  - In the second case, it occupies the piece identified as after.



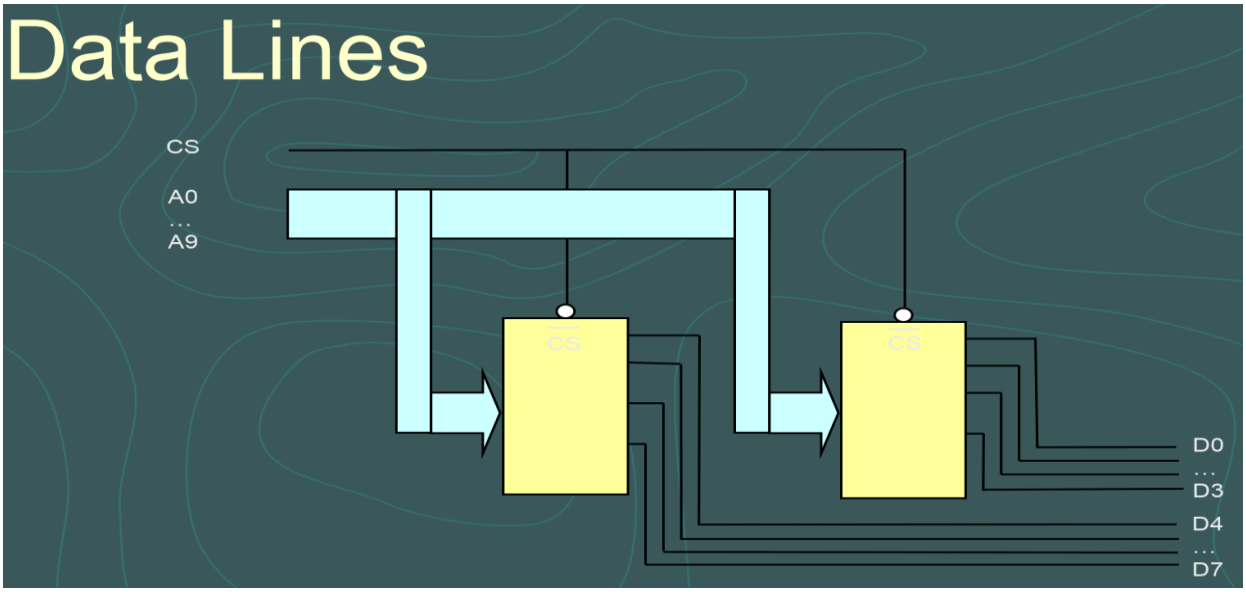
High-Order vs. Low-Order Address Lines

- The address lines from a microprocessor can be classified into two types:
  - High-Order
    - Used for memory chip selection
  - Low-Order
    - Used for location selection within a memory chip.
  - This classification is highly dependent on the memory system design.

Data Lines

- All of the above discussion has been regarding memory length. Lets look at memory width.
- We said that the width is the number of bits in each memory word.
  - We have been assuming so far that our memory chips have the right width.
  - What if they don't?
    - It is very common to find memory chips that have only 4 bits per location. How would you design a byte wide memory system using these chips?
    - We use two chips for the same address range. One chip will supply 4 of the data bits per address and the other chip supply the other 4 data bits for the same address.

Data Lines



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