

Digital Logic Design, CT:02

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XOR

(Count the odd numbers of 1)

$$A \oplus B = \bar{A}B + A\bar{B}$$

XNOR

(Count the even numbers of 1)

$$\overline{(A \oplus B)} = AB + \bar{A}\bar{B}$$

Even Parity Generator:

Even Parity Generator

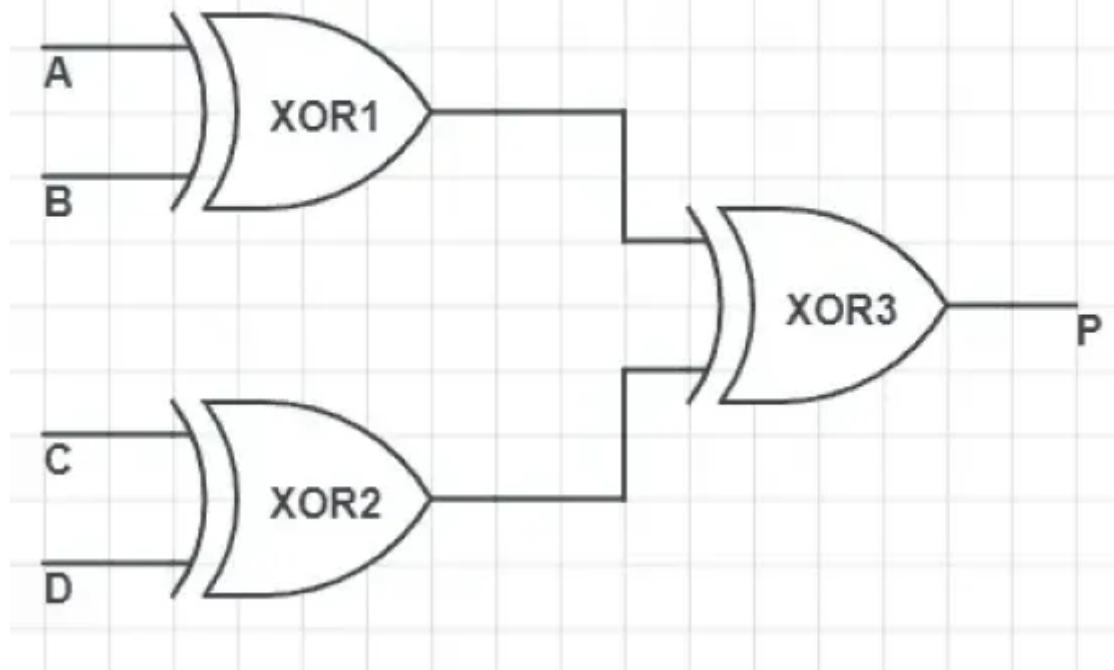
A	B	C	P
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$\begin{aligned} P &= \overline{\bar{A} \bar{B} C} + \overline{\bar{A} B \bar{C}} + \overline{A \bar{B} \bar{C}} + A B C \\ &= \overline{A} (\overline{\bar{B} C} + \overline{B \bar{C}}) + A (\overline{\bar{B} \bar{C}} + B C) \\ &= \overline{A} \underbrace{(B \oplus C)}_{X} + A \overline{(B \oplus C)} \end{aligned}$$
$$P = A \oplus B \oplus C$$

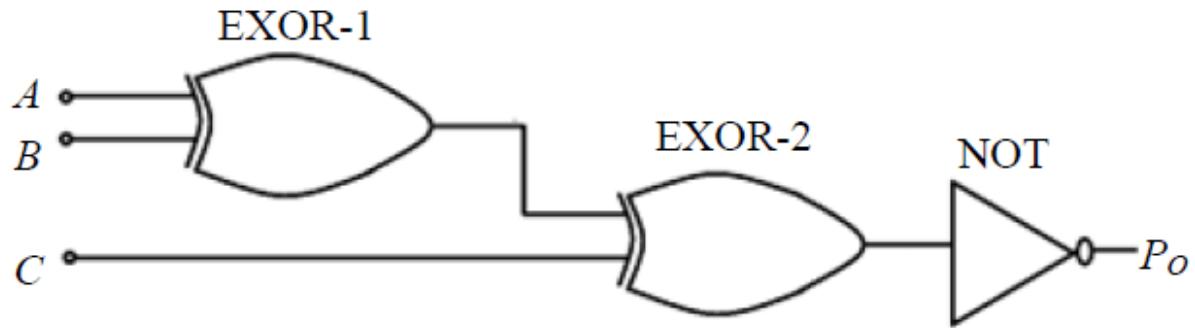
$n - th$ bit generator

$$P = A_0 \oplus \dots \oplus A_{n-1}$$

4-bit even parity generator



Odd Parity Generator



A	BC	00	01	11	10
0	00	1	0	1	0
1	01	0	1	0	1

$$P_o = \overline{A \oplus B \oplus C}$$

$n - th$ bit generator

$$P = A_0 \oplus \dots \oplus A_{n-1}$$

$$\text{Odd Generator, } Q = \bar{P}$$

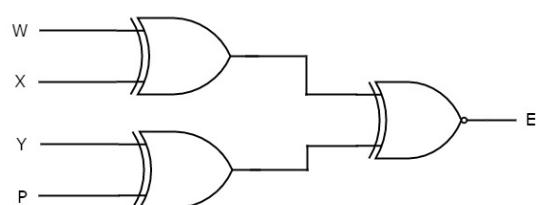
Parity Checker

Output : 1 - When there's an error

Even Parity Checker

$$P_C = A_0 \oplus A_1 \oplus \dots \oplus P$$

P = Parity bit



Odd Parity Checker

\bar{P}_C

Enable Circuit

- Output depends on signal

Disable Circuit

- Output is fixed

Flip-Flop

“ফিপ-ফপ বা ল্যাচ (ইংরেজি: **Flip-flop** অথবা **latch**) ইলেকট্রনিক্সে ব্যবহৃত এক ধরনের যন্ত্র যা উপাত্ত সঞ্চিত রাখার জন্য ব্যবহৃত হয়। ইলেক্ট্রনিক তথ্য প্রযুক্তির ধারাবাহিক যুক্তি তত্ত্বে এই যন্ত্রটি ব্যবহার করা হয়। একটি ল্যাচ এক বিট তথ্য ধারণ করতে পারে”

- memory unit
- made of logic circuit
- one or more output states
- input used to switch back and forth between it's possible output states
- input needs momentarily activated / pulse to change a output states
- output will remain in new state even input pulse is over

Two output : Q and \bar{Q}

When SET, FF is in HIGH state : $Q = 1$

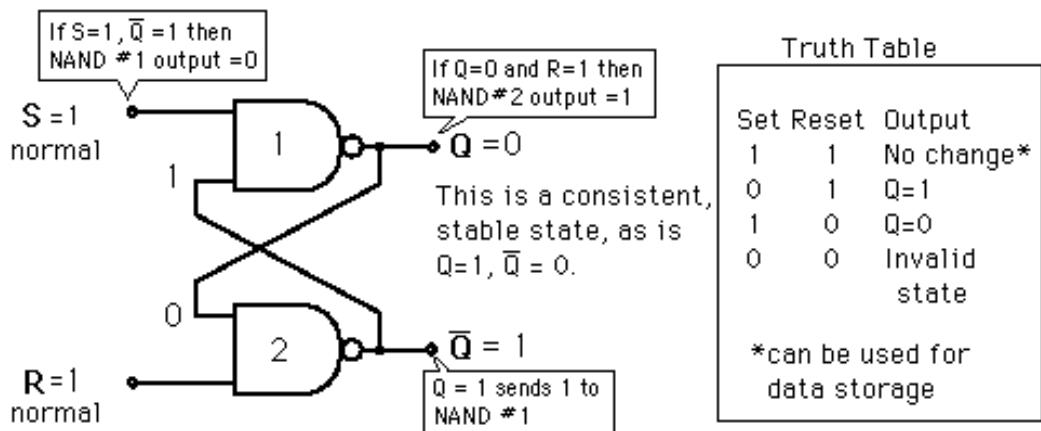
When Reset, FF is in LOW state : $\bar{Q} = 0$

Latch : bi-stable multivibrator

NAND Latch

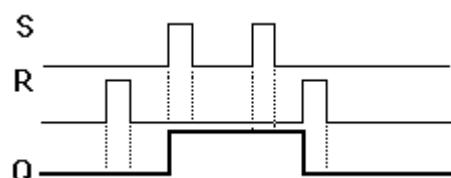
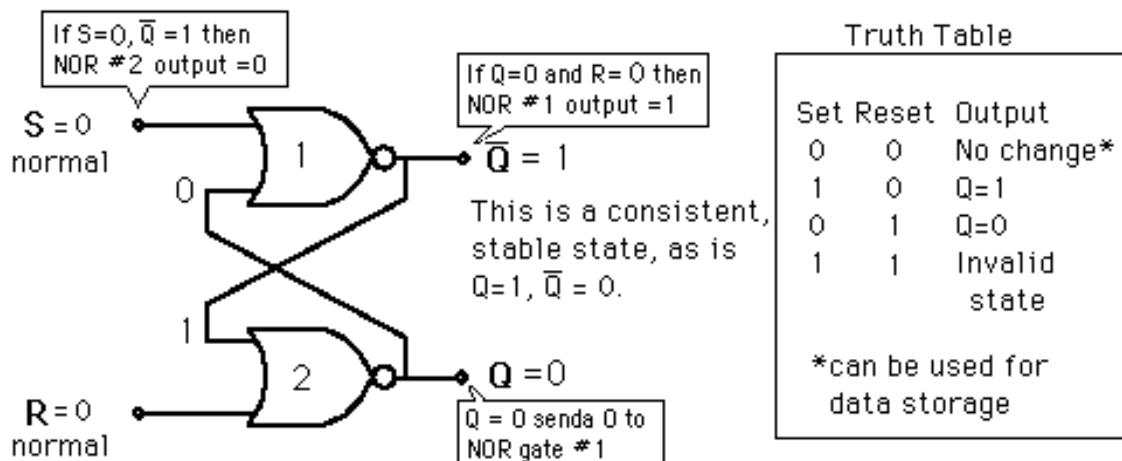
NAND : When a NAND gate input 0, then its output is ZERO. If S zero, Q 1.. R zero, Q-bar 1..

RESET has PRIORITY



NOR Latch

SET has Priority



Pulse :

- signal inactive to active state , causes something in the circuit

- returns to inactive the effect remains in the system, these signals are pulse

Positive Pulse: performs intended function when HIGH

Negative Pulse: Performs intended function when LOW

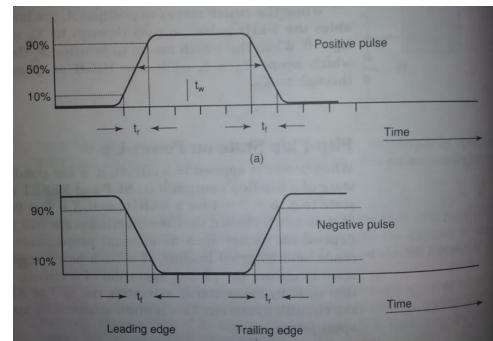
Rise time : LOW to HIGH, 10% high level voltage

Fall time: HIGH to LOW, 90% high level voltage

Leading Edge: the transition at the begin pulse

Tailing Edge: the transition at the ending pulse

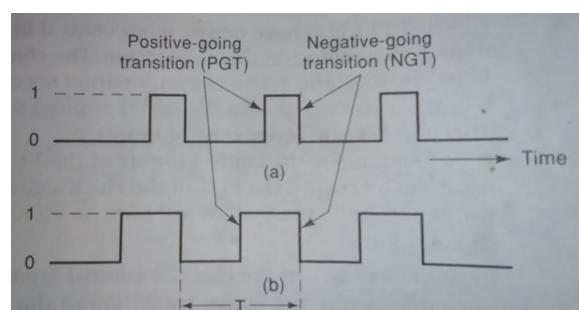
Duration of the Pulse : the time between the points when the leading and tailing edges are 50% of high level voltage



Clock Signal

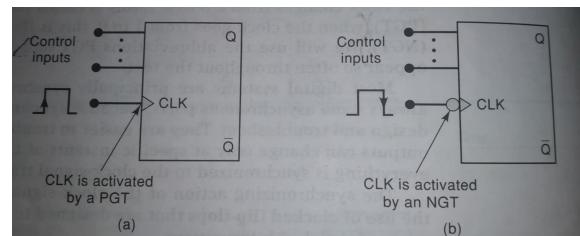
- **asynchronously :** output changes state any time one or more of the input changes
- **synchronously :** the exact times at which any output can change states are determined by a signal named clock
 - the clock change 0 to 1 : PGT (Positive Going Transition)
 - 1 to 0 : NGT

A clock signal : one PGT/NGT to next PGT/NGT



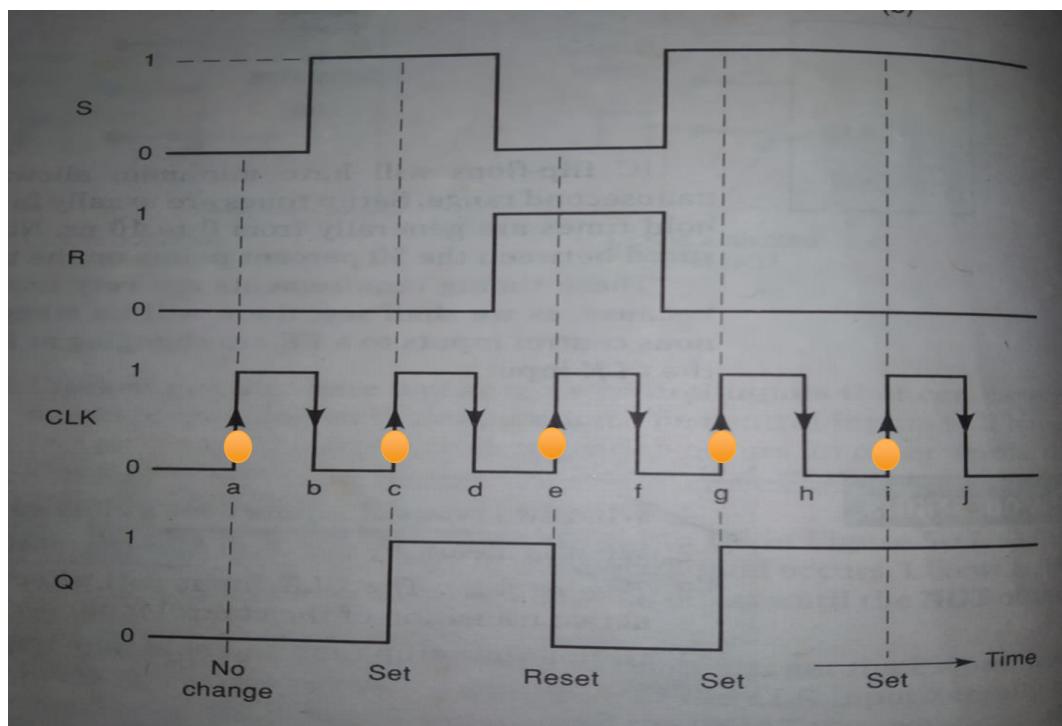
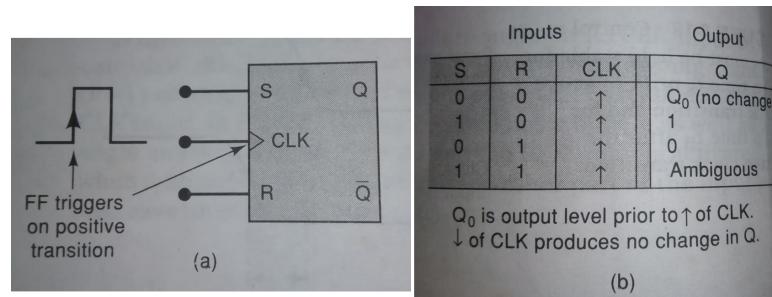
Clocked FFS

- **edge-triggered** : activated CLK when PGT/NGT
- may have one or more inputs but they wont occurs until active clock transition



CLK : WHEN, Control Input : WHAT happens

Clocked FF: (NOR latch)

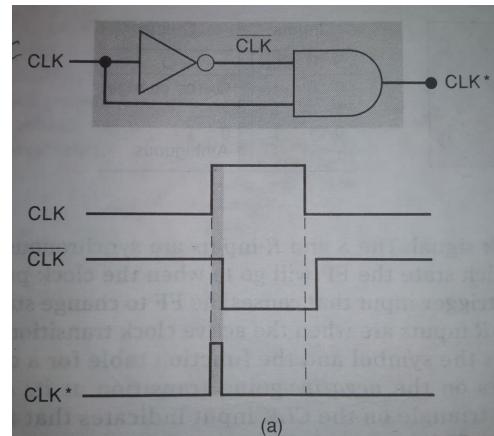
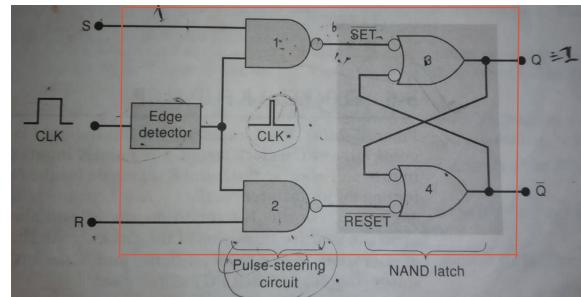


Edge Triggered SR

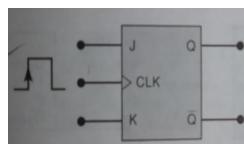
- NOR Latch (3, 4)
- Pulse Steering Circuit (1, 2)
 - it steers the spike through to the S or R input latch
 - to SET : * CLK to $NAND\ 1$
 - to RESET: * CLK to $NAND\ 2$

- Edge Detector

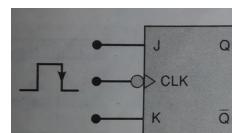
- Produces a narrow Spike
- delay due to inverted CLK
- Output Spike HIGH for nanoseconds
- Output HIGH when
 - $CLK \& C\bar{L}K = 1$ (PGT)



Clocked JK FF

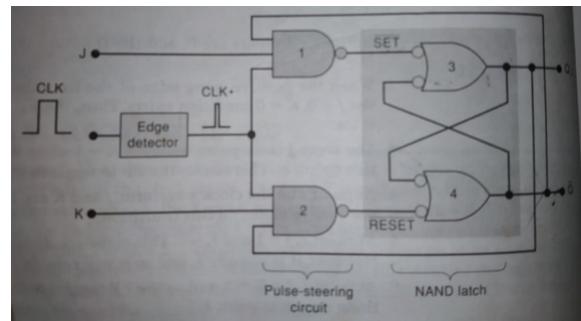
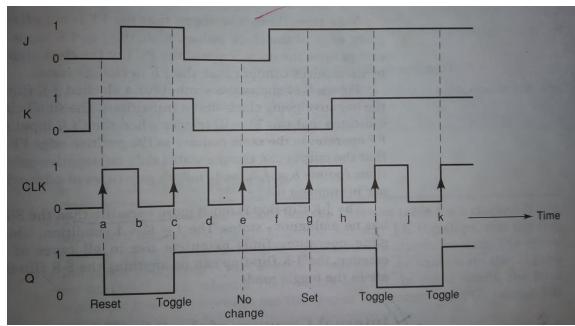


J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	Q_0 (toggles)



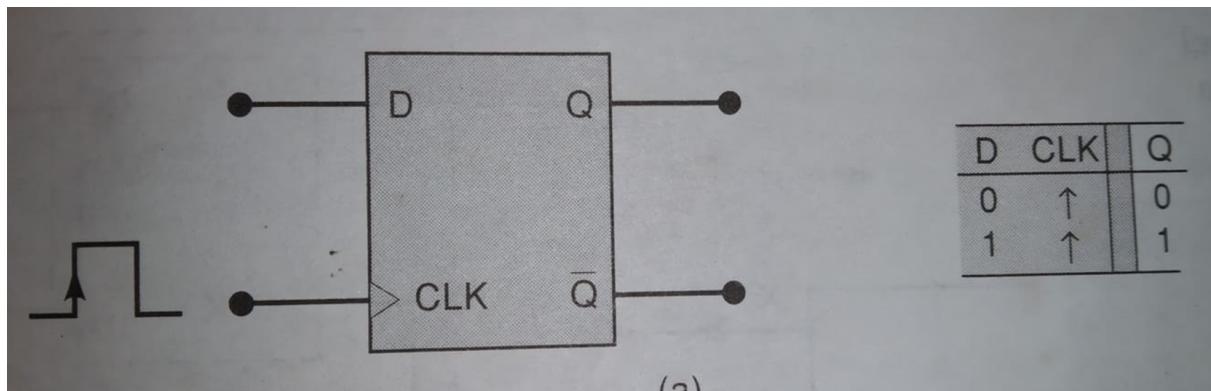
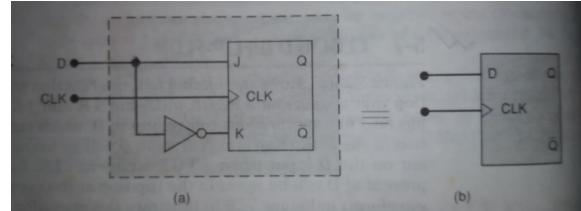
J	K	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	\bar{Q}_0 (toggles)

- J has more priorities
- $J = K = 1 \Rightarrow \text{Toggle}$

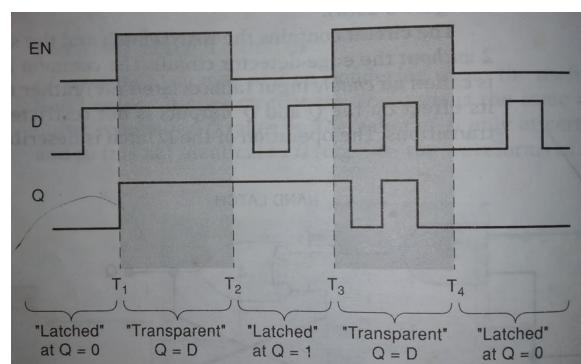
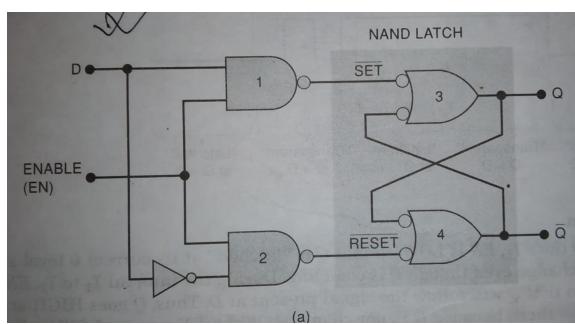


Clocked D FF

- one synchronous input D
- D stands for Data

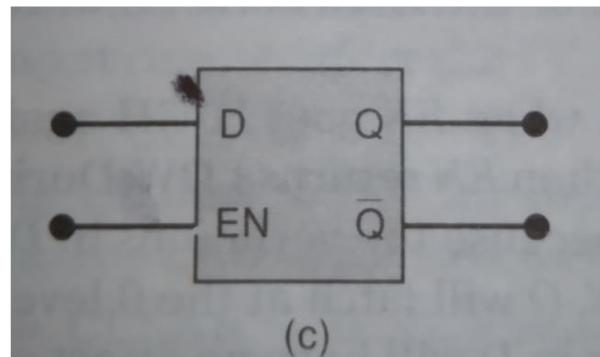


D Latch



Inputs		Output
EN	D	Q
0	X	Q_0 (no change)
1	0	0
1	1	1

"X" indicates "don't care."
 Q_0 is state Q just prior to EN going LOW.

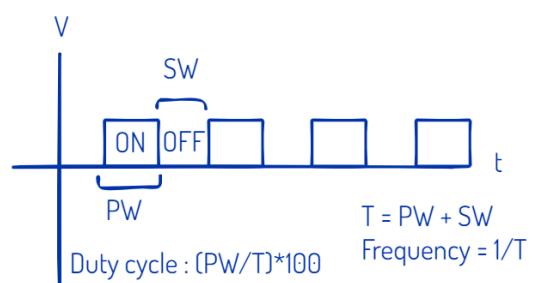
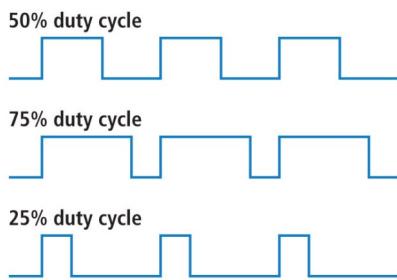


Duty cycle

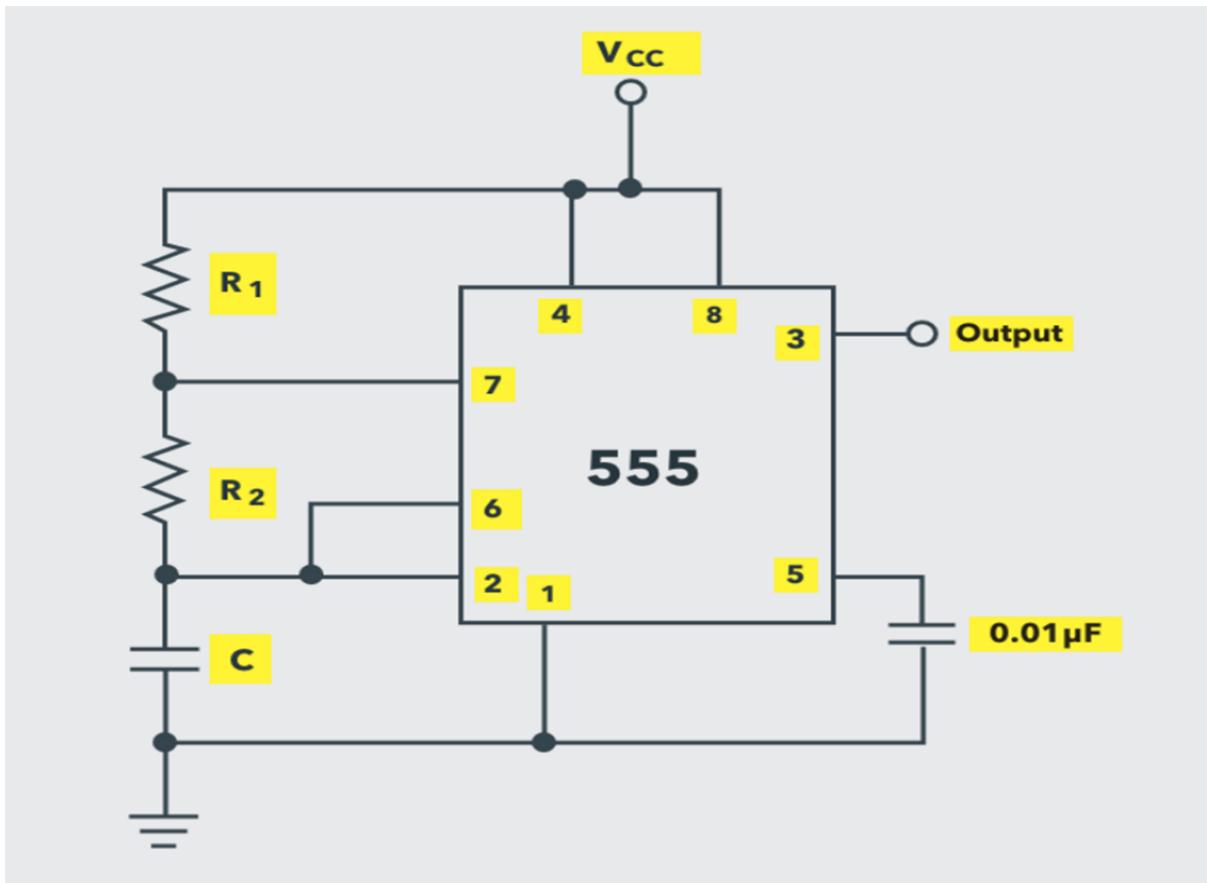
https://www.youtube.com/watch?v=pFl-swR8BRo&ab_channel=TheOrganicChemistryTutor

Duty cycle is the ratio of time a load or circuit is ON compared to the time the load or circuit is OFF.

Duty cycle, sometimes called "duty factor," is expressed as a percentage of ON time. A 60% duty cycle is a signal that is ON 60% of the time and OFF the other 40%.



Astable Multivibrator:



$$t_L = 0.693R_2C$$

$$t_H = 0.693R(R_1 + R_2)C$$

$$T = T_L + T_H$$

$$f = \frac{1}{T}$$

Duty Cycle : $\frac{T_H}{T} \times 100$

Example :

- Calculate the frequency and the duty cycle of the 555 astable multivibrator output for $C = 0.001 \mu F$, $R_A = 2.2 k\Omega$, $R_B = 100 k\Omega$.

$$t_L = 0.693(100k\Omega)(0.001 \mu F) = 69.3 \mu s$$

$$t_H = 0.693(102.2k\Omega)(0.001 \mu F) = 70.7 \mu s$$

$$T = 69.3 + 70.7 = 140 \mu s$$

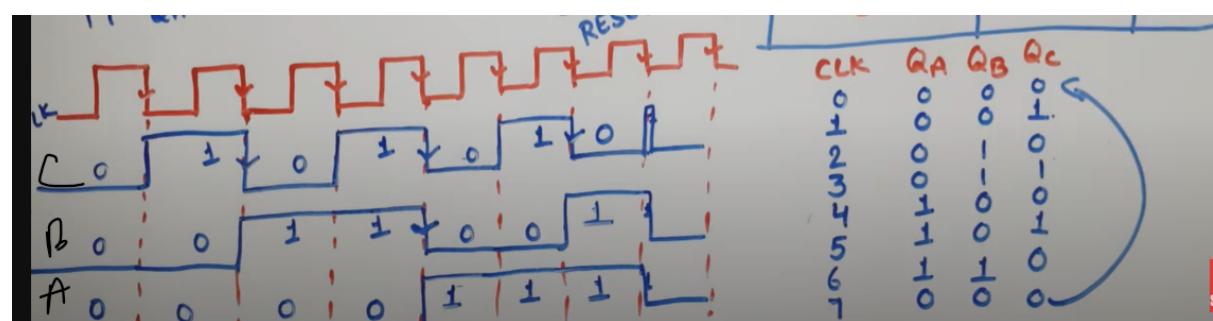
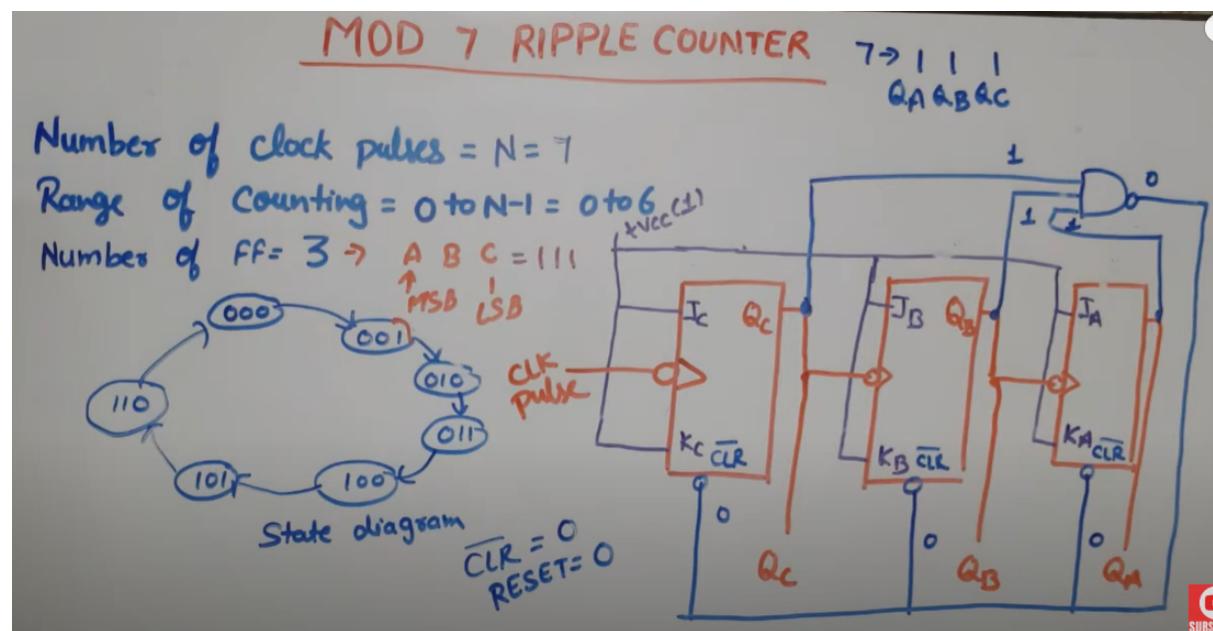
$$f = 1/140 \mu s = 7.29 \text{ kHz}$$

duty cycle = $70.7/140 = 50.5\%$

Ripple Counter

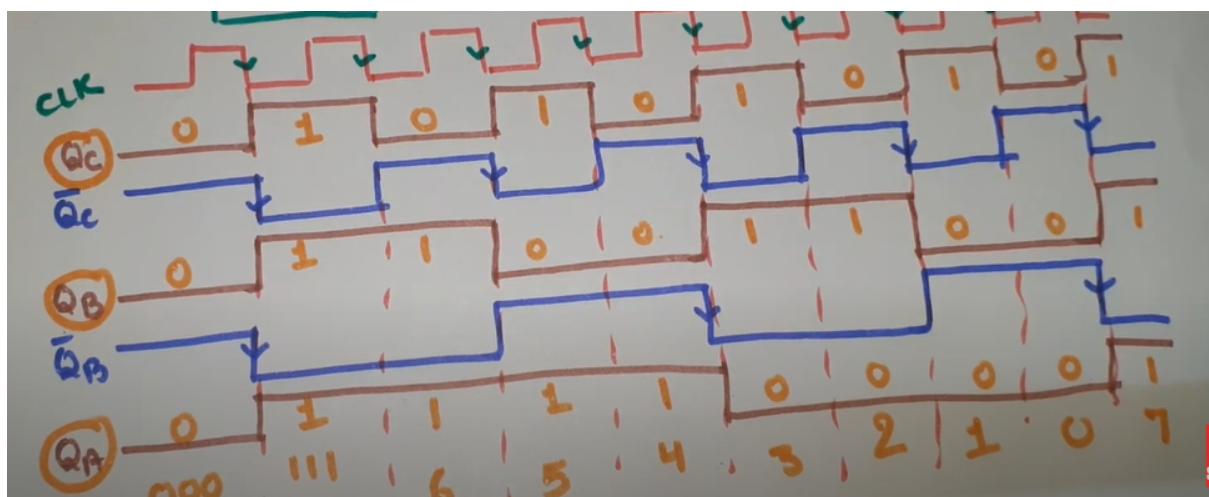
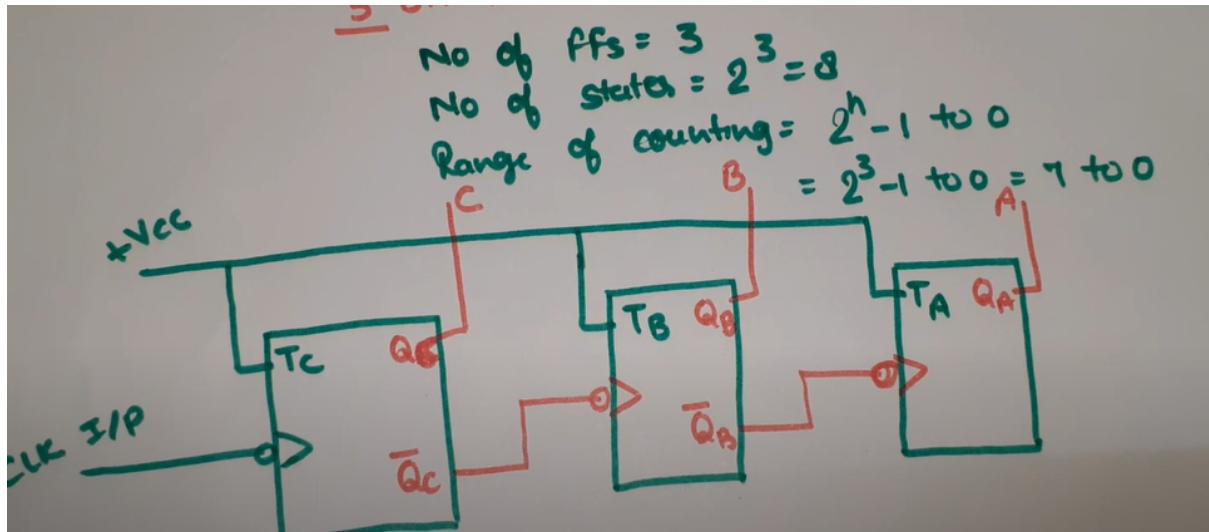
Ripple counter is a special type of Asynchronous counter in which the clock pulse ripples through the circuit

<https://www.youtube.com/watch?v=KA3Cw7yLRsM>



Ripple Down Counter

https://www.youtube.com/watch?v=yZkozx-g_Ho

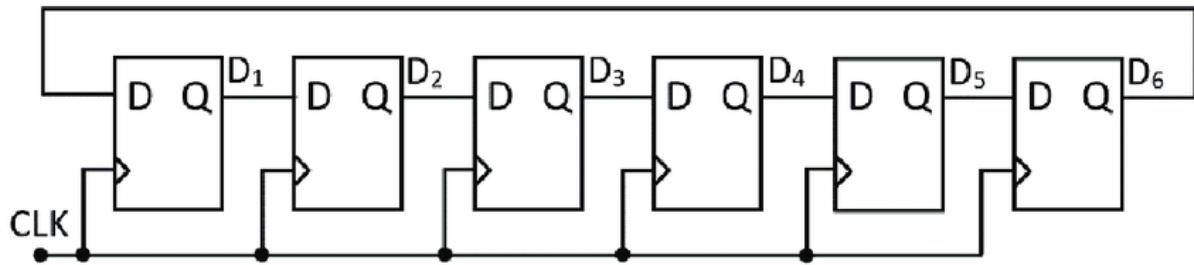


Math

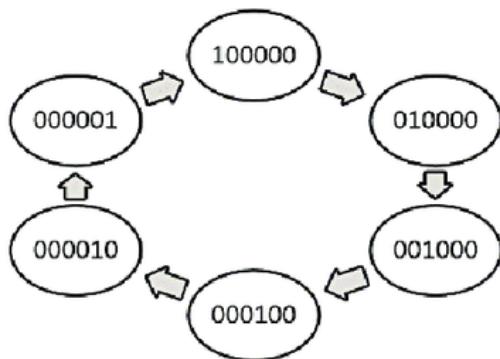
- Counter MOD of $n - th$ FFs = 2^n
- The output frequency of $n - th$ FF

$$= \frac{\text{Input Frequency}}{2^n}$$

Ring Counter



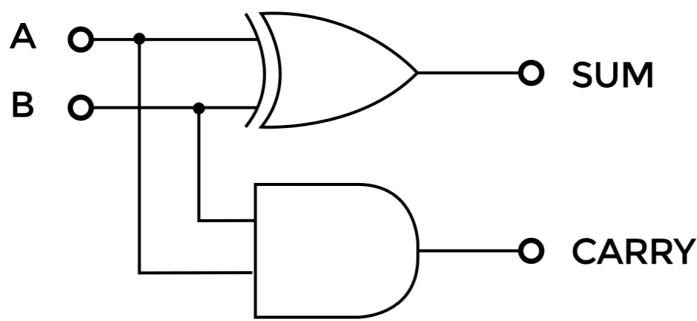
CLK	D ₁	D ₂	D ₃	D ₄	D ₅	D ₆
1	1	0	0	0	0	0
2	0	1	0	0	0	0
3	0	0	1	0	0	0
4	0	0	0	1	0	0
5	0	0	0	0	1	0
6	0	0	0	0	0	1



Half Adder

$$\text{Sum} = A \oplus B$$

$$\text{Carry} = AB$$



A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full Adder

$$\text{Sum} = A \oplus B \oplus C$$

$$\text{Carry} = AB + (A \oplus B)C$$

