

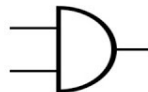
Digital Logic Design, CT:01

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⋮ Tags	

Drawing Circuit Figure:

WORKING & SIMULATION

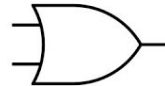
AND



NAND



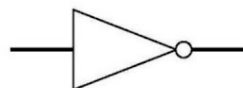
OR



NOR

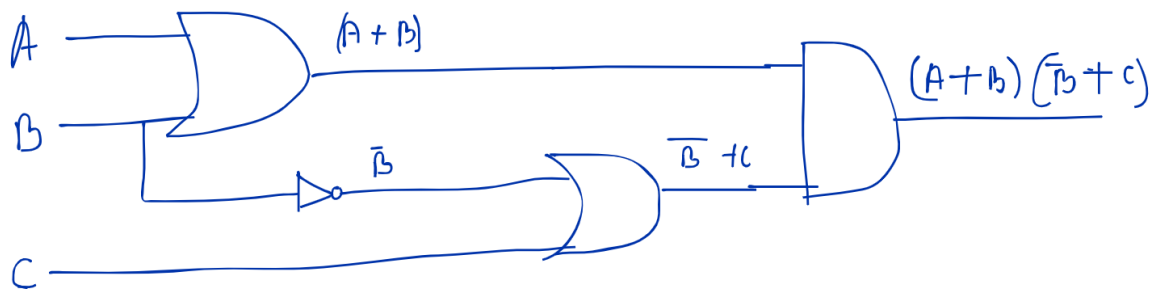


NOT



- $+$ \Rightarrow OR
- $*$ \Rightarrow AND

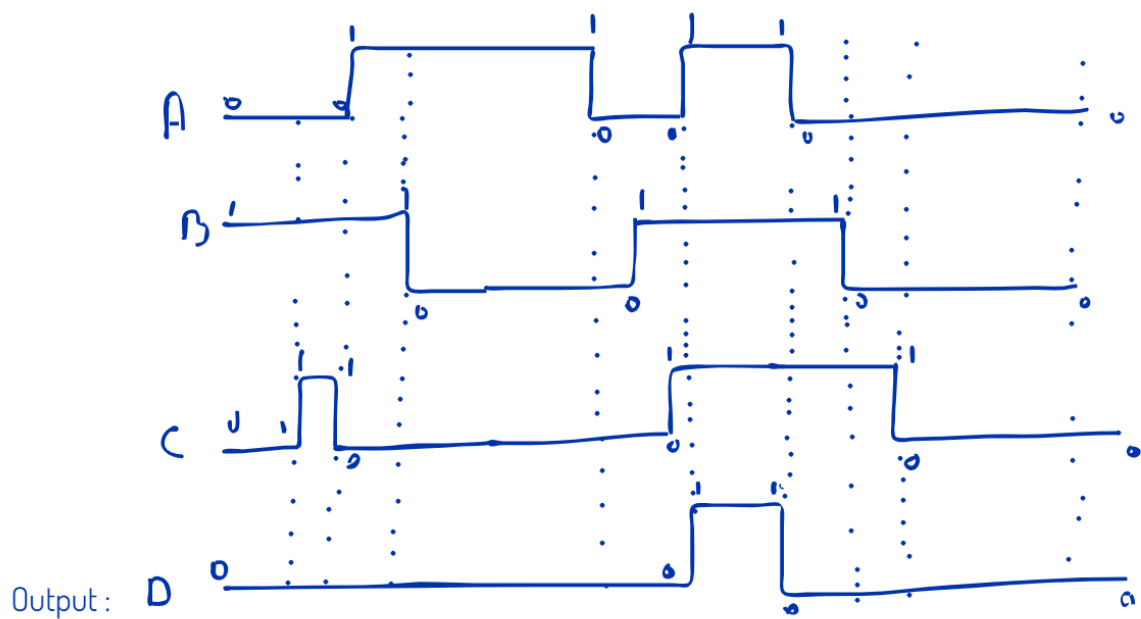
$$\rightarrow (A+B)(\bar{B}+C)$$



Writing output from input waveform :

https://www.youtube.com/watch?v=hkbFfEjZvv8&ab_channel=UndergradAcademy.

A,B, C AND gate output waveform:



De Morgan's Law:

A	B	\bar{A}	\bar{B}	$A \cdot B$	$\overline{A \cdot B}$	$\bar{A} + \bar{B}$
0	0	1	1	0	1	1
0	1	1	0	0	1	1
1	0	0	1	0	1	1
1	1	0	0	1	0	0

A	B	\bar{A}	\bar{B}	$A+B$	$\overline{A+B}$	$\bar{A} \cdot \bar{B}$
0	0	1	1	0	1	1
0	1	1	0	1	0	0
1	0	0	1	1	0	0
1	1	0	0	1	0	0

Parity:

1. Even Parity : Number of 1 is even, example : 101
2. Odd Parity : Number of 1 is odd, example : 100

Determine Even Parity code for
D P3 P2 P1 P0

1) 1001

D	P3	P2	P1	P0
0	1	0	0	1

2) 1000

D	P3	P2	P1	P0
1	1	0	0	0

Binary to Gray Code Conversion

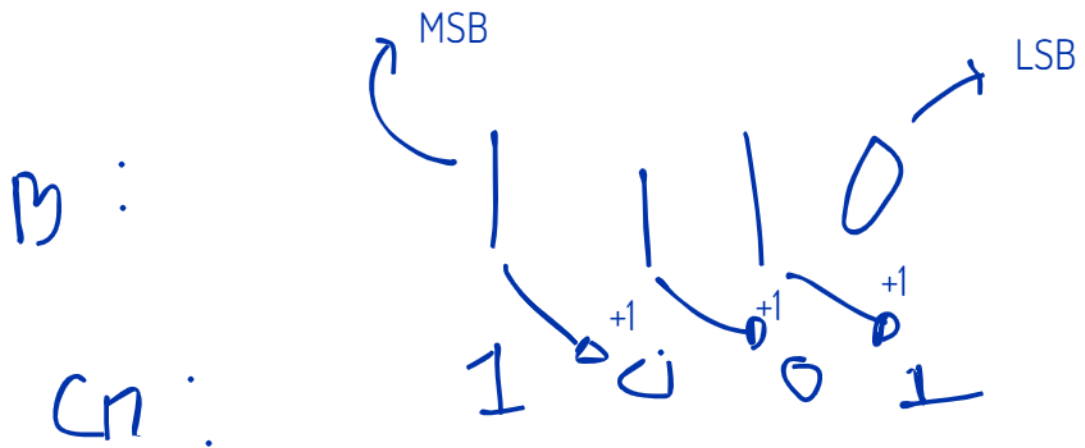
https://www.youtube.com/watch?v=cF-Q5j7RUEw&ab_channel=NesoAcademy.

https://www.youtube.com/watch?v=-gMm9hhvp9Y&t=243s&ab_channel=NesoAcademy.

- Print the MSB as it is
- i th bit = $(i - 1)$ bit + i th bit (Neglect the Carry)
- Repeat the process 2

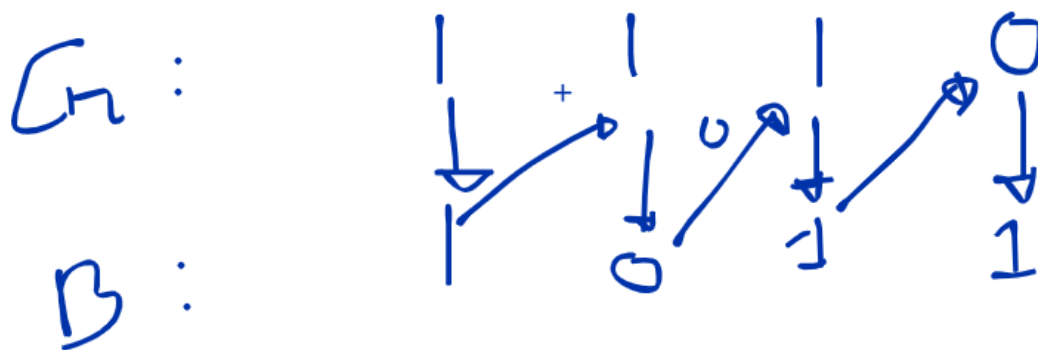
OR

- MSB = MSB
- i th bit = $(i) \text{ XOR } (i - 1)$



Binary to Gray Code:

- Print the MSB and Previous Sum = MSB
- i th bit = Previous Sum + i th bit (neglecting the carry)
- Update Previous Sum



Boolean Constants & Variables

- $0/False \Rightarrow 0 - 0.8V$
- $1/True \Rightarrow 2 - 5V$

$$\begin{aligned}
 (11) \quad & x + (y + z) = (x + y) + z = x + y + z \\
 (12) \quad & x(yz) = (xy)z = xyz \\
 (13a) \quad & x(y + z) = xy + xz \\
 (13b) \quad & (w + x)(y + z) = wy + xy + wz + xz \\
 (14) \quad & x + xy = x \\
 (15a) \quad & x + \bar{x}y = x + y \\
 (15b) \quad & \bar{x} + xy = \bar{x} + y
 \end{aligned}$$

M-Graph:

https://www.youtube.com/watch?v=lw1STgKUpW0&ab_channel=ALLABOUTELECTRONICS

https://www.youtube.com/watch?v=v08rGyVYall&t=169s&ab_channel=ALLABOUTELECTRONICS

https://www.youtube.com/watch?v=QNq6gfaWoNM&ab_channel=LearnElectronicsOnline

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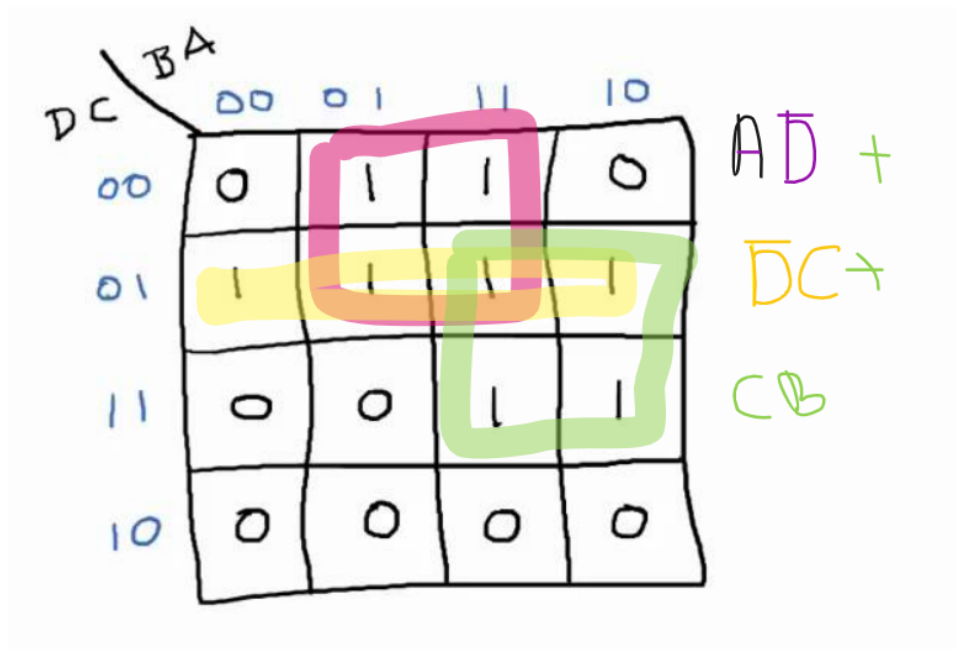
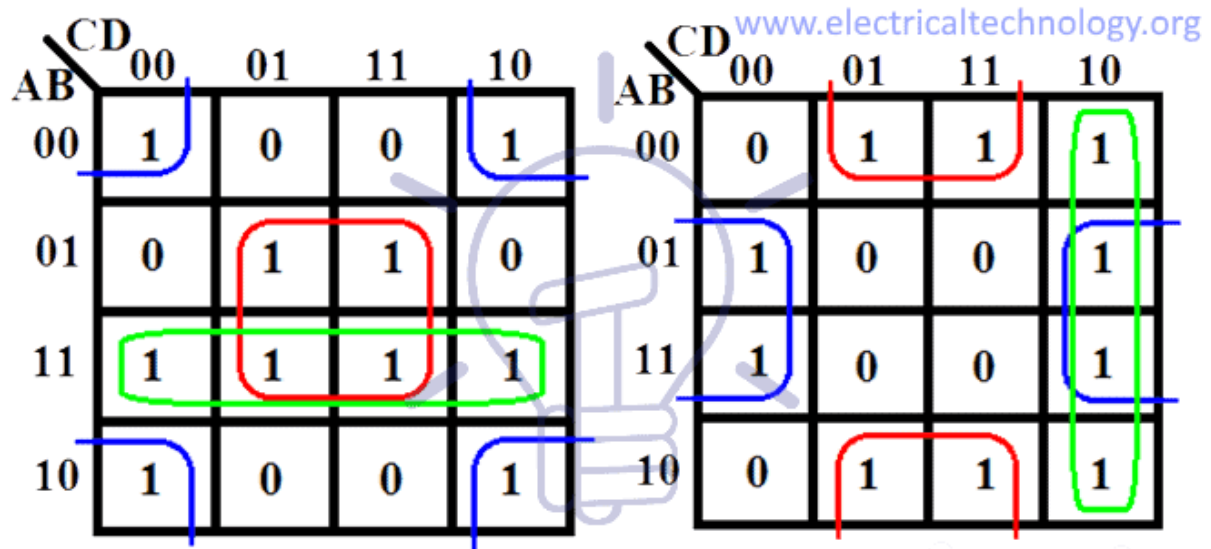
- We must make the group of size 2^n

		X		0	1
		Y		0	1
Y	0				
	1				

		X		0	1
		Y Z		00	01
Y Z	00				
	01				
	11				
	10				

		XY				00	01	11	10
		Z				0	1		
Z	0								
	1								

		WX				00	01	11	10
		YZ				00	01	11	10
YZ	00								
	01								
	11								
	10								



Design Logic Circuit corresponding to the truth table

- Truth table \rightarrow Expression \rightarrow Simplification the expression
- Design Logic Circuit according to the simplified expression