University of Asia Pacific (UAP)
Department of Electrical and Electronic Engineering (EEE)

Course Outline

Program:	B.Sc. in Electrical and Electronic Engineering (EEE)
Course Title:	VLSI Design I
Course Code:	EEE 423
Semester:	Spring-2022
Level:	4th Year 1st Semester
Credit Hour:	3.0
Name & Designation of Teacher:	Md. Moshiur Rahman, Assistant Professor, Department of EEE
Office/Room:	Department of EEE, 5th floor, 501.
Class Hours:	Monday: 03:30 pm -05:00 pm & Thursday: 09:30 am -11:00 am[A] Tuesday: 09:30 am -11:00 am & Thursday: 08:00 am -09:30 am[B]
Consultation Hours:	Monday : 02:00 pm - 03:30 pm, Wednesday: 11.00am-02.00pm
E-mail:	sourov.eee@uap-bd.edu
Mobile:	01670064572
Rationale:	This is an optional course that will help the students to understand the fabrication process and CMOS circuits design of digital IC's and logic devices.
Pre-requisite (if any)**:**	EEE 209
Course Synopsis:	Fabrication process and CMOS circuit design of different logic devices. Layout design rules and physical design of simple logic circuits. Review of MOS transistor theory, NMOS and CMOS inverter. CMOS circuit characteristics and performance estimation.
Course Objectives :	The objectives of this course are to: **1.** Introduce with fabrication process of MOSFET and Logic circuits. **2.** Design of CMOS circuits and Layout of different logic devices.

3. Discuss different memory and arithmetic devices and their design procedures.
4. Develop the skills regarding efficient, economic and precise design procedures of different logic devices.
5. Provide a clear idea about CMOS circuit characteristics and performance estimation.

Course Outcomes (CO) and their mapping with Program outcomes (PO) and Teaching-Learning Assessment methods:

CO No.	CO Statements: Upon successful completion of the course, students should be able to:	Corresponding POs (Appendix-1)	Bloom's taxonomy domain/level (Appendix-2)	Delivery methods and activities	Assessment Tools
CO1	Interpret the fabrication process and design the CMOS circuit of logic devices.	3 (WK5)	Apply	Class lecture and discussion	Assignment, Class Performance, Quiz, Mid Term, Final Exam
CO2	Layout design of different Memory, logical unit and Arithmetic devices	3 (WK5)	Apply	Class Lecture, discussion & Problem solving	Assignment, Class Performance, Quiz, Mid Term, Final Exam
CO3	Identify the controlling design parameters for efficient devices development of NMOS circuits.	2 (WK2)	Analyze	Class Lecture, discussion & Problem solving	Assignment, Class Performance, Quiz, Mid Term, Final Exam
CO4	Identify efficient and economic CMOS circuit development, also calculate power consumption and delay.	2 (WK2)	Analyze	Class Lecture, discussion & Problem solving	Assignment, Class Performance, Quiz, Mid Term, Final Exam

Weighting COs with Assessment methods:

AssessmentType	% Weight	CO1	CO2	CO3	CO4
Final Exam	**30%**	14.17		14.17	21.67
Mid Term	**20%**	6.67	13.33		
Class performance, Quizzes, Presentation, open book exam, Assignment, Viva	**30%**	10	10	10	
Total	**100%**	30.84	23.33	24.17	21.67

Grading Policy: As per the approved grading policy of UAP (Appendix-3)

Course Content Outline and mapping with Cos

Weeks	Topics / Content	Course Outcome	Delivery methods and activities	Reading Materials
1	Introductory discussion on VLSI design and MOS characteristics, fabrication technology of CMOS transistor.	CO1	Class lecture and discussion	D.A. Pucknell and Linda E.M. Brackenbury Chapter - 1
2-3	CMOS and NMOS circuit design process, stick diagram of different logic gates and devices.	CO1	Class lecture and discussion	D.A. Pucknell
4	NMOS & PMOS pass transistor, CMOS pass transistor, Implementation of logic circuits: multiplexer, adder, subtractor using NMOS, PMOS pass transistor & Transmission gate	CO1 CO2	Class lecture and discussion	D.A. Pucknell
Quiz-01				

5	Introduction on Verilog code, Design and implementation techniques of different logic circuits using Verilog code.	CO2	Class lecture and discussion	Class Lectures
6	Bus arbitration logic circuit, Parity generator circuit, and ALU.	CO2	Class lecture and discussion	D.A. Pucknell
Quiz-02				
7	PLA circuits	CO2	Class lecture and discussion	D.A. Pucknell
Midterm Exam				
8	Review of MOS transistor theory, threshold voltage, body effect, I-V equations and characteristics.	CO3	Class lecture and discussion	Linda E.M. Brackendury, Chapter – 2
9-10	NMOS Inverter: NMOS Inverter circuit with resistive, enhancement and depletion types load, power consumption, delay, aspect ratio calculation.	CO3 C04	Class lecture and discussion	Linda E.M. Brackendury, Chapter – 2
Quiz-03				
11-12	CMOS inverter: Power consumption, delay, aspect ratio calculation, voltage transfer characteristics	CO3 CO4	Class lecture and discussion	Linda E.M. Brackendury,
13	Buffer chain design for high capacitive load, RC delay calculation for CMOS circuits.	CO4	Class lecture and discussion	Linda E.M. Brackendury,
Quiz-04				
14	Review & problem-solving	All COs	Discussion	
Final Exam				

Required Reference(s):

1. D.A. Pucknell & K. Eshraghian, Basic VLSI Design
2. Design of VLSI Systems – A Practical Introduction, Linda E.M. Brackenbury.
3. CMOS VLSI Design, N.H.E. Weste, D. Harris & A. Banerjee.

Recommended Reference(s):

1. Microelectronic Circuits, Sedra & Smith
2. CMOS Circuit Design, Layout and Simulation, R.J. Baker.

Grading System: As per the approved grading scale of University of Asia Pacific (Appendix-2).

Special Instructions:

- Minimum 70% attendance is required to attend the semester final exam.
- There is no mark for class attendance. However, there is mark for class performance.
- There will be no make-up for quizzes and mid-term exam.
- No plagiarism would be allowed in assignments. Cases of copying one another in assignments or class tests would be dealt very strictly.
- Students must come to the class prepared for the course material covered in the previous class.
- Do not do anything which may disturb the class (such as passing irrelevant and negative comments etc.); you will be monitored, and disciplinary actions will be taken.

Prepared by	Checked by	Approved by
Md. Moshiur Rahman Assistant Professor Department of EE	Chairman, PSAC committee	Head of the Department

Appendix-1:

Washington Accord Program Outcomes (PO) for engineering programs:

No.	PO	Differentiating Characteristic
1	Engineering Knowledge	Breadth and depth of education and type of

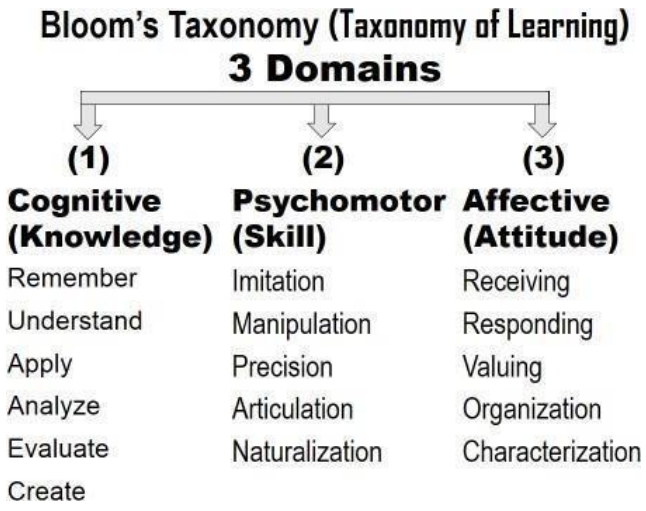
		knowledge, both theoretical and practical
2	Problem Analysis	Complexity of analysis
3	Design/ development of solutions	Breadth and uniqueness of engineering problems i.e. the extent to which problems are original and to which solutions have previously been identified or codified
4	Investigation	Breadth and depth of investigation and experimentation
5	Modern Tool Usage	Level of understanding of the appropriateness of the tool
6	The Engineer and Society	Level of knowledge and responsibility
7	Environment and Sustainability	Type of solutions.
8	Ethics	Understanding and level of practice
9	Individual and Team work	Role in and diversity of team
10	Communication	Level of communication according to type of activities performed
11	Project Management and Finance	Level of management required for differing types of activity
12	Lifelong learning	Preparation for and depth of Continuing learning.

Knowledge Profile:

WK	**Attribute**
WK1	A systematic, theory-based understanding of the natural **sciences** applicable to the discipline.
WK2	Conceptually based **mathematics**, numerical analysis, statistics and the formal aspects of computer and information science to support analysis and modeling applicable to the discipline.
WK3	A systematic, theory-based formulation of **engineering fundamentals** required in the engineering discipline
WK4	**Engineering specialization** knowledge that provides theoretical frameworks and bodies of knowledge for the accepted practice areas in the engineering discipline; much is at the forefront of the discipline.
WK5	Knowledge that supports engineering **design** in a practice area.
WK6	Knowledge of engineering practice (**technology**) in the practice areas in the engineering discipline.
WK7	Comprehension of the role of engineering in **society** and identified issues in engineering practice in the discipline: ethics and the engineer's professional responsibility to public safety; the impacts of engineering activity; economic, social, cultural, environmental and sustainability

WK8	Engagement with selected knowledge in the **research** literature of the discipline.

Appendix-2



Appendix-3

UAP Grading Policy:

Numeric Grade	Letter Grade	Grade Point
80% and above	A+	4.00
75% to less than 80%	A	3.75
70% to less than 75%	A-	3.50
65% to less than 70%	B+	3.25
60% to less than 65%	B	3.00
55% to less than 60%	B-	2.75
50% to less than 55%	C+	2.50
45% to less than 50%	C	2.25
40% to less than 45%	D	2.00
Less than 40%	F	0.00