TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

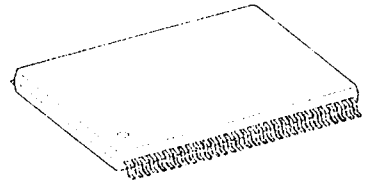
TD62C950RF, TD62C950LF

TD62C950RF : 40BIT SHIFT REGISTER / LATCHES DRIVER (RIGHT SHIFT)
TD62C950LF : 40BIT SHIFT REGISTER / LATCHES DRIVER (LEFT SHIFT)

FEATURES

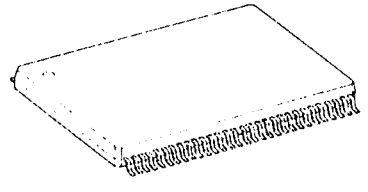
- Low Power Consumption
- High Speed Operation : f_{CK} = 4MHz
- High Voltage Output : 70V
- Push / Pull Output : −40mA / +2mA
- 40bit Shift Register / Latches / Outputs
- Both Right-direction Shift type (RF) and Left-direction type (LF) are available.
- CMOS Interface
- Compact 60 Leads Plastic Package

TD62C950LF



SSOP60-P-0.65

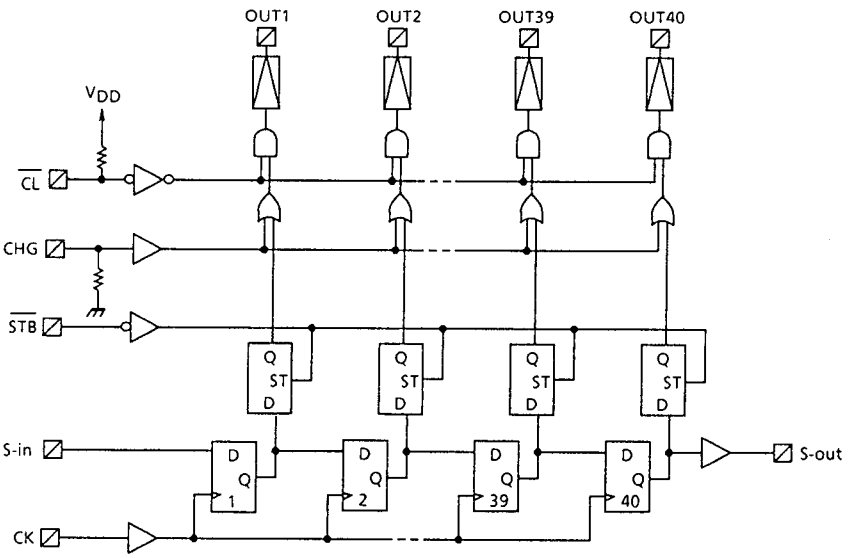
TD62C950RF



SSOP60-P-0.65A

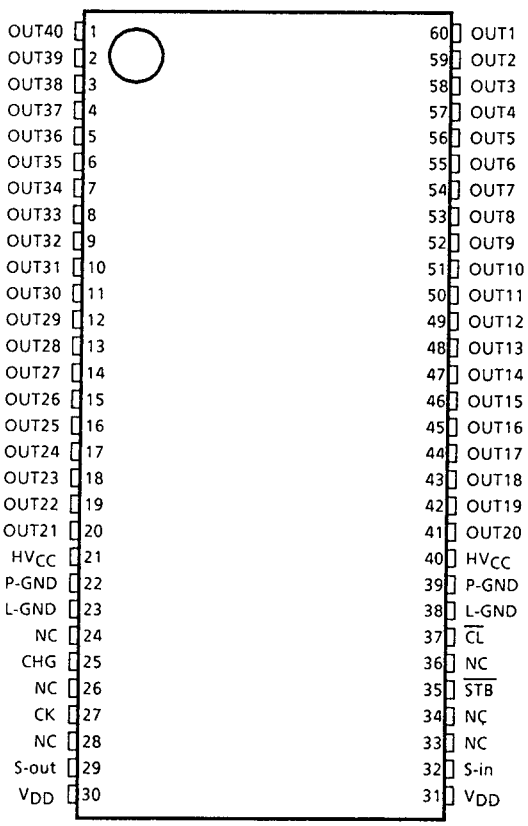
Weight SSOP60-P-0.65 : 1.47g (Typ.)
SSOP60-P-0.65A : 1.47g (Typ.)

BLOCK DIAGRAM

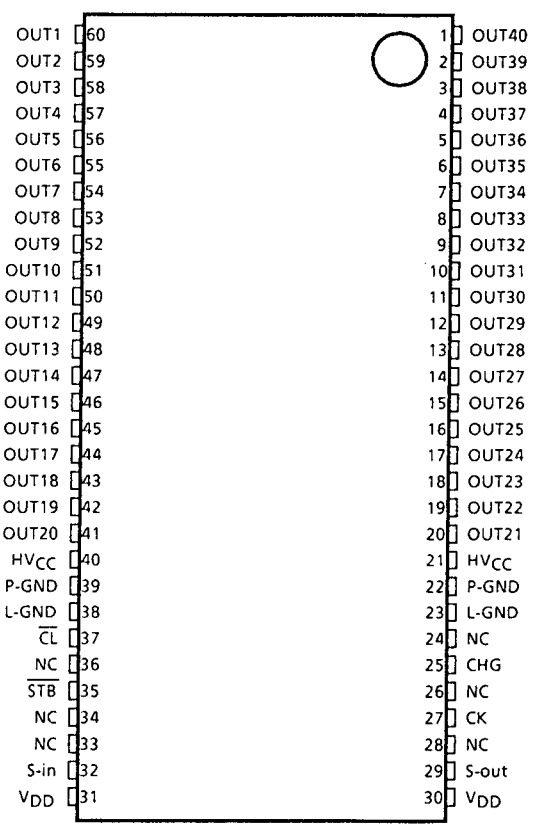


PIN CONNECTION (TOP VIEW)

TD62C950LF



TD62C950RF



PIN FUNCTION

PIN No.	PIN NAME	FUNCTION
1~20 41~60	OUTn	Output terminal
21, 40	HV_{CC}	Supply voltage terminal for driver
22, 39	P-GND	Power GND (GND terminal for driver)
23, 38	L-GND	Logic GND (GND terminal for control)
37	$\overline{CL}$	"L" : All outputs "L" Pull up register equipped
35	$\overline{STB}$	"L" : Data latch "H" : Data through
32	S-in	Serial data input terminal for shift register
30, 31	V_{DD}	Supply voltage terminal for control logic
29	S-out	Serial data output terminal for shift register
27	CK	"⌐¬" : Data shift
25	CHG	If $\overline{CL}$ = "H" at CHG = "L" input, it make all output "H". Pull down register equipped

TRUTH TABLE

INPUT					OUTPUT			
CK	CHG	$\overline{CL}$	$\overline{STB}$	S-in	OUT1	OUTm	OUT40	S-out
⌐¬	H	H	(*)	Dn	ALL H			Dn-39
	L	H	H	Dn	Dn	Dm-1	Dn-39	Dn-39
	L	H	L	Dn	Dn-1	Dn-m	Dn-40	Dn-39
	(*)	L	(*)	Dn	ALL L			Dn-39
¬⌐	H	H	(*)	Dn	ALL H			Dn-40
	L	H	(*)	Dn	Dn-1	Dn-m	Dn-40	Dn-40
	(*)	L	(*)	Dn	ALL L			Dn-40

(*) "H" or "L"

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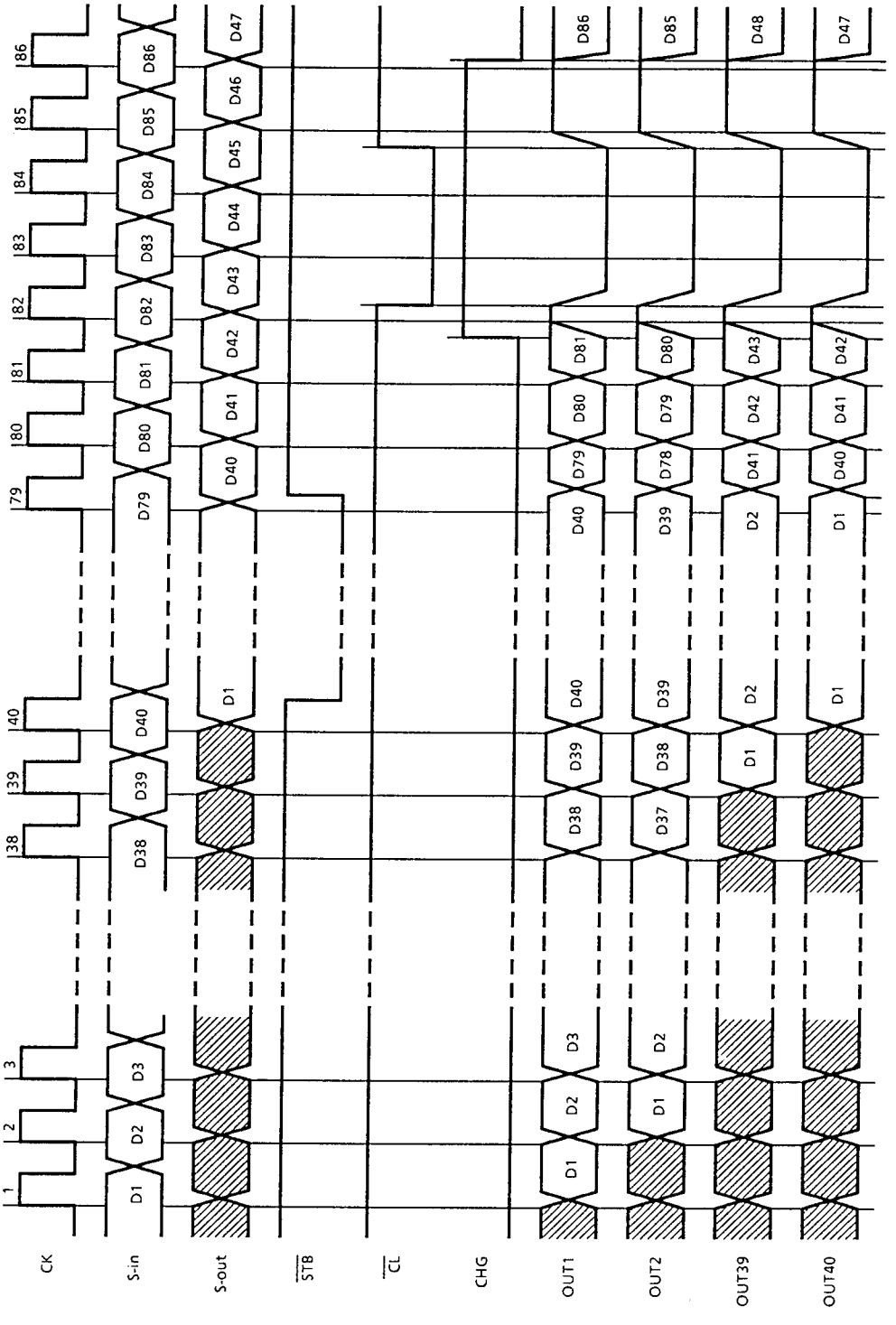
TIMING CHART



MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Output Driver Supply Voltage	HV_{CC}	70	V
Supply Voltage	V_{DD}	7	V
Output Voltage	V_{OUT}	GND − 2.0~HV_{CC} + 2.0	V
Input Voltage	V_{IN}	GND − 0.5~V_{DD} + 0.5	V
Power Dissipation	P_D	1.0	W
		1.3 (Note)	
Operating Temperature	T_{opr}	−40~85	°C
Storage Temperature	T_{stg}	−55~150	°C

(Note) Mounted on a 60 × 60 × 1.6mm Cu 24% glass epoxy PCB.

RECOMMENDED OPERATING CONDITION (Ta = −40~85°C)

CHARACTERISTIC			SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Driver Supply Voltage			HV_{CC}	—	—	—	70	V
			V_{DD}	—	4.5	5.0	5.5	
Output Current	"H" Level	S-out	I_{OH}	—	—	—	−0.5	mA
		OUTn		—	—	—	−40	
	"L" Level	S-out	I_{OL}	—	—	—	0.5	
		OUTn		—	—	—	2.0	
Input Voltage			V_{IN}	—	GND	—	V_{DD}	V
Operating Clock Frequency			f_{CK}	—	—	4	8	MHz
Clock Pulse Width			t_{WCK}	—	75	—	—	ns
Data Set Up Time			t_{setup}	—	50	—	—	ns
Data Hold Time			t_{hold}	—	50	—	—	ns
Power Dissipation			P_D	(*)	—	—	0.57	W

(*) On glass epoxy PCB (60 × 60 × 1.6mm Cu 24%)

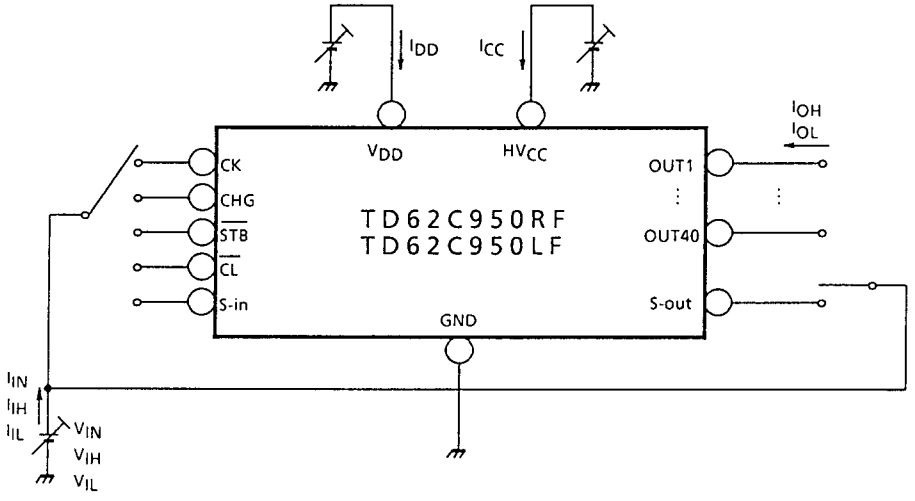
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC			SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Input Voltage	"H" Level		V_{IH}	—	—		70% V_{DD}	—	V_{DD}	V
	"L" Level		V_{IL}	—	—		GND	—	30% V_{DD}	
Input Current			I_{IN}	—	$\overline{CL}$ = H, CHG = L	V_{DD} = 5.0V	—	—	±1	μA
					$\overline{CL}$ = L, CHG = L	V_{IN} = GND or	—	—	−100	
					$\overline{CL}$ = H, CHG = H	V_{DD}	—	—	100	
Output Voltage	"H" Level	S-out	V_{OH}	—	V_{DD} = 5V, HV_{CC} = 70V	I_{OH} = −20μA	4.9	4.95	—	V
		OUTn				I_{OH} = −40mA	65.0	66.5	—	
						I_{OH} = −10μA	68.0	68.5	—	
	"L" Level	S-out	V_{OL}	—		I_{OL} = 20μA	—	0.01	0.1	
		OUTn				I_{OL} = 2mA	—	2.0	3.0	
						I_{OL} = 10μA	—	0.8	1.0	
Quiescent Current			I_{CCH}	—	HV_{CC} = 70V, V_{DD} = 5V	All output "H"	—	5.0	6.5	mA
			I_{CCL}			All output "L"	—	—	10	μA
			I_{DD}				—	—	10	μA
Operating Supply Current			$I_{CC\ opr.}$	—	HV_{CC} = 70V, V_{DD} = 5V	f_{CK} = 100MHz, Duty = 50%, CL = 0	—	6.0	7.0	mA
			$I_{DD\ opr.}$	—		f_{CK} = 1MHz, CL = 0	—	0.8	1.0	

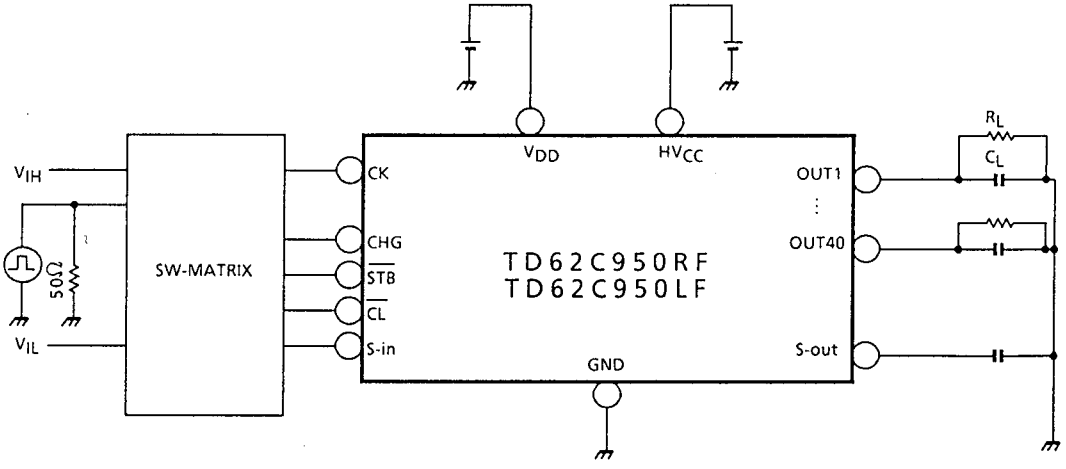
SWITCHING CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC			SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Maximum Operating Clock Frequency			f (max)	—	HV_{CC} = 70V V_{DD} = 5V V_{IH} = V_{DD} V_{IL} = GND C_L (OUTn) = 50pF R_L (OUTn) = 1.5kΩ C_L (S-out) = 15pF	9	17	—	MHz
Propagation Delay Time	"H" Level	CK-S-out	t_{pLH}	—		—	50	100	ns
		CK-OUTn				—	0.6	1.2	μs
		$\overline{CL}$-OUTn				—	0.6	1.2	
		$\overline{STB}$-OUTn				—	0.6	1.2	
	"L" Level	CK-S-out	t_{pHL}	—		—	50	100	ns
		CK-OUTn				—	0.1	0.5	μs
		$\overline{CL}$-OUTn				—	0.1	0.5	
		$\overline{STB}$-OUTn				—	0.1	0.5	
Minimum Pulse Width		CK	t_w min	—		70	—	—	ns
		$\overline{STB}$				70	—	—	
Data Set Up Time			t_{setup}	—		20	—	—	ns
CK-$\overline{STB}$ Set Up Time			$t_{setup\ (\overline{STB})}$	—		50	—	—	ns
Data Hold Time			t_{hold}	—		20	—	—	ns
Maximum Rise Time			t_r	—		—	—	1.0	μs
Maximum Fall Time			t_f	—		—	—	1.0	
Output Rise Time		S-out	t_{or}	—		—	20	45	ns
		OUTn				—	0.6	1.2	μs
Output Fall Time		S-out	t_{of}	—		—	20	45	ns
		OUTn				—	0.07	0.3	μs

DC CHARACTERISTIC TEST CIRCUIT

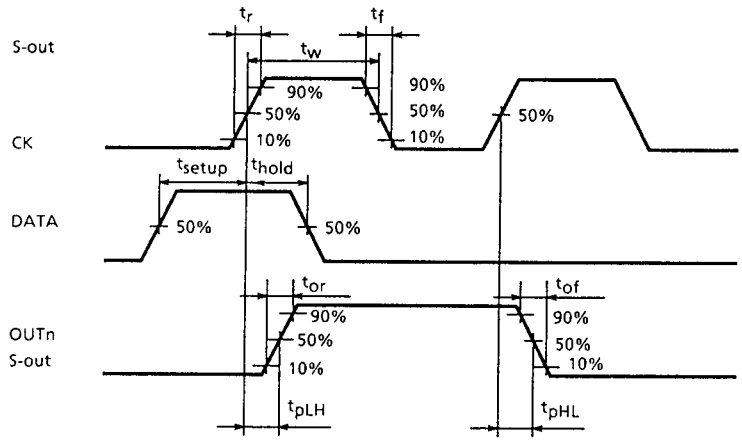


AC CHARACTERISTIC TEST CIRCUIT

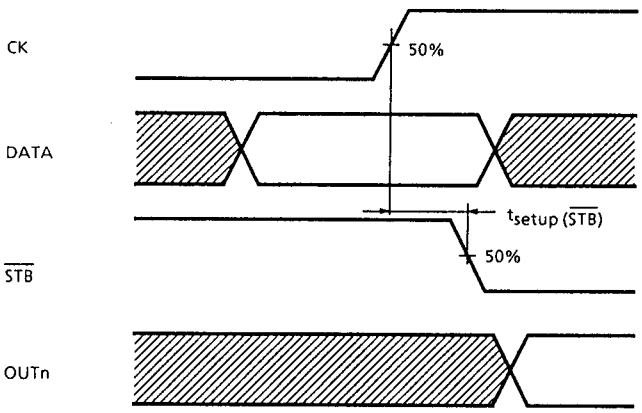


TIMING WAVEFORM

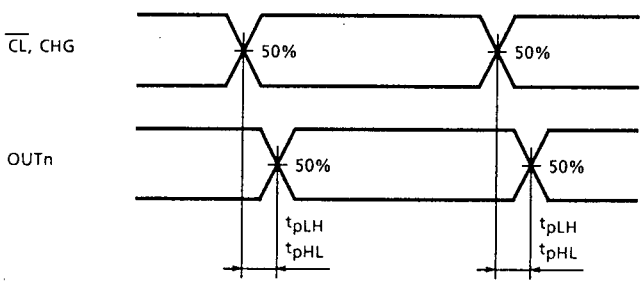
1. CK-OUTn



2. CK-$\overline{STB}$



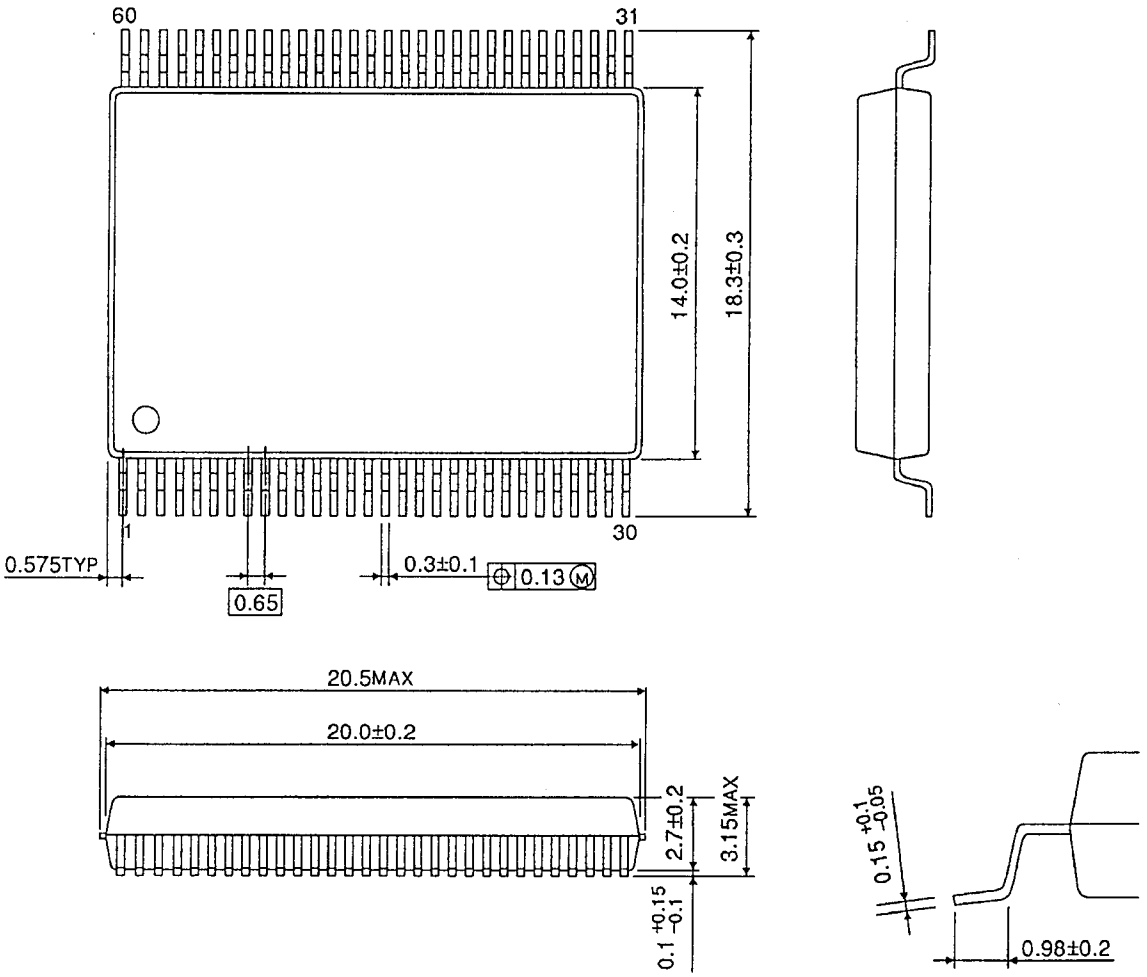
3. CHG, $\overline{CL}$-OUTn



OUTLINE DRAWING

SSOP60-P-0.65

Unit : mm

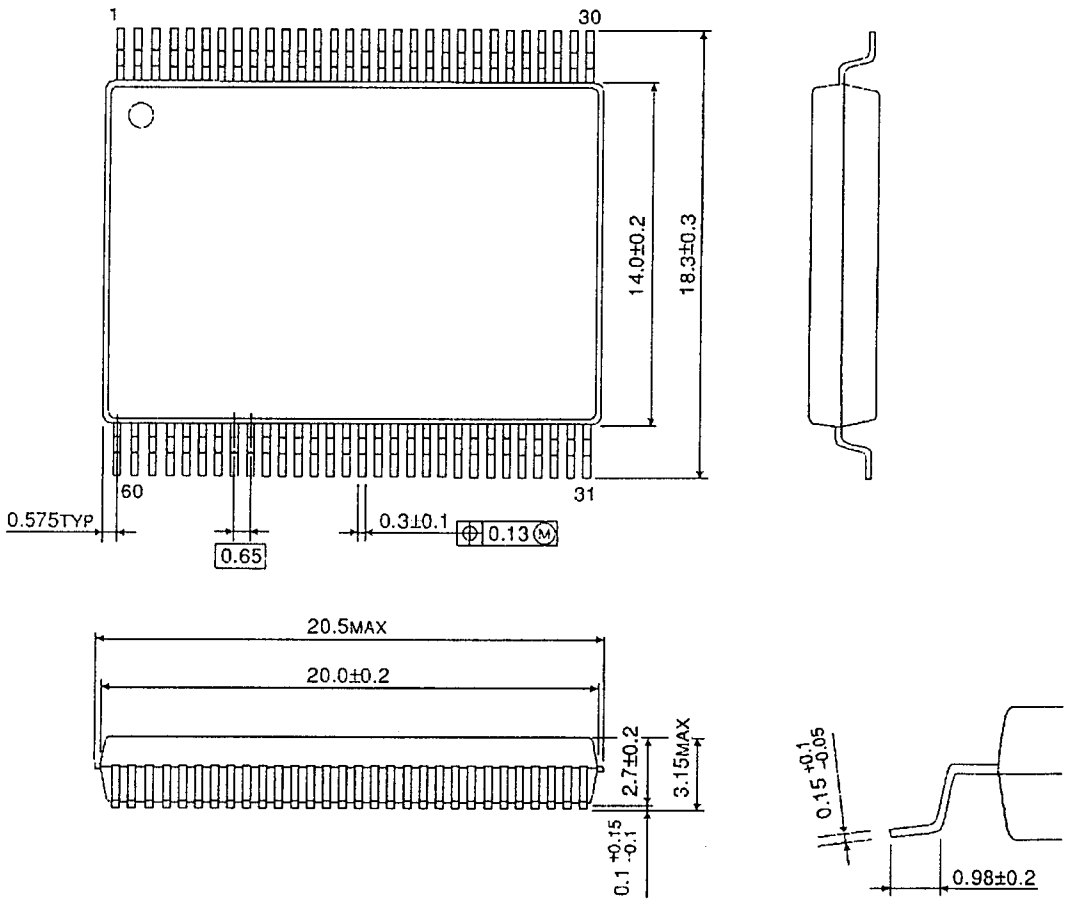


Weight : 1.47g (Typ.)

OUTLINE DRAWING

SSOP60-P-0.65A

Unit : mm



Weight : 1.47g (Typ.)