DS04-27401-4E

ASSP

Power Supply Monitor with Watch-Dog Timer

MB3773

■ DESCRIPTION

The Fujitsu MB3773 is designed to monitor the voltage level of a power supply (+5V or an arbitrary voltage) in a microprocessor circuit, memory board in a large-size computer, for example. The MB3773 also contains a watch-dog timer function to detect uncontrol. Table status of processor and reset system/processor.

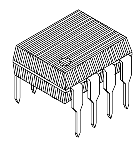
If the circuit's power supply deviates more than a specified amount, then the MB3773 generates a reset signal to the microprocessor. Thus, the computer data is protected from accidental erasure.

When the MB3773 does not receive the clock pulse from the processor in the specified period, the MB3773 generates a reset signal to the mciroprocessor.

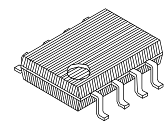
Using the MB3773 requires few external components. To monitor only a +5 volt supply, the MB3773 requires the connection of one external capacitor.

The MB3773 is available in an 8-pin Dual In-Line package space saving Flat Package, or a Single In-Line Package.

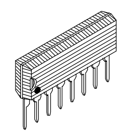
- Precision voltage detection (V_S = 4.2V ±2.5%)
- Threshold level with hysterisis
- Low voltage output for reset signal (V_{CC} = 0.8V typ.)
- Precision reference voltage output (V_{REF} = 1.245 V±1.5%)
- External clock monitor and reset signal generator
- Negative-edge input watch-dog timer
- Minimal number of external components (one capacitor min.)
- Available in a variety of packages
- 8-pin Dual In-Line Package
- 8-pin Flat Package
- 8-pin Single In-Line Package



PLASTIC PACKAGE
DIP-8P-M01



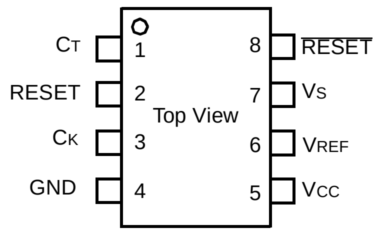
PLASTIC PACKAGE
FPT-8P-M01



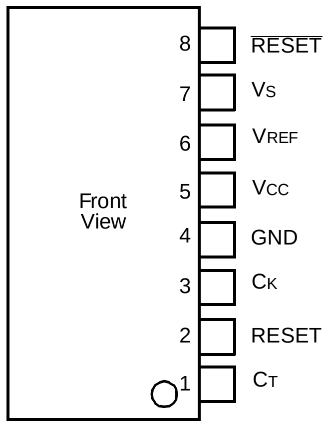
PLASTIC PACKAGE
SIP-8P-M03

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

■ PIN ASSIGNMENT



(DIP-8P-M01)
(FPT-8P-M01)



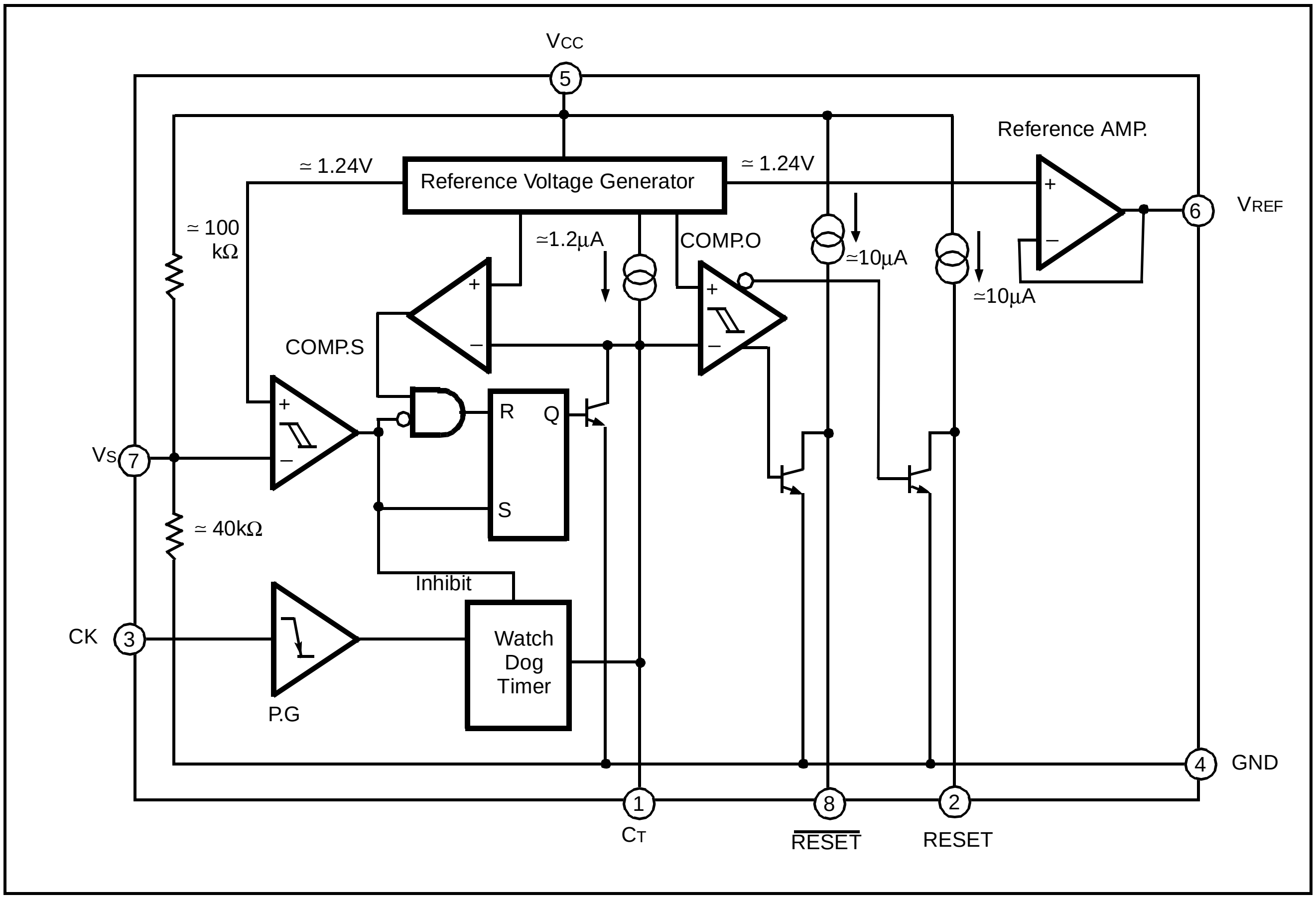
(SIP-8P-M03)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	-0.3 to +18	V
Input voltage	VS	-0.3 to V_{CC} +0.3 (≤+18)	V
	V_S	-0.3 to +18	V
$\overline{\text{RESET}}$, RESET Supply voltage	V_{OH}	-0.3 to V_{CC} +0.3 (≤+18)	V
Power dissipation($T_a \le 85$°C)	P_D	200	mW
Storage temperature	T_{STG}	-55 to +125	°C

NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ BLOCK DIAGRAM



■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply voltage	V_{CC}	+3.5 to +16	V
Reset, reset sink current	I_{OL}	0 to 20	mA
V_{REF} output current	I_{OUT}	-200 to +5	µA
Watch clock setting time	t_{WD}	0.1 to 1000	ms
Rising/falling time	t_{FC}, t_{RC}	<100	µs
Terminal capacitance	C_T	0.001 to 10	µF
Operating ambient temperature	T_a	-40 to +85	°C

■ ELECTORICAL CHARACTERISTICS

(1) DC Characteristics

(V_{CC}=5V, T_a=25°C)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
Supply current	Watch dog timer operating	I_{CC}	-	600	900	µA
Detection voltage	V_{CC}	V_{SL}	4.10	4.20	4.30	V
	T_a = -40°C to +85°C		4.05	4.20	4.35	
	V_{CC}	V_{SH}	4.20	4.30	4.40	
	T_a = -40°C to +85°C		4.15	4.30	4.45	
Hysterisis width	V_{CC}	V_{HYS}	50	100	150	mV
Reference voltage	-	V_{REF}	1.227	1.245	1.263	V
	T_a = -40°C to +85°C		1.215	1.245	1.275	
Reference voltage change rate	V_{CC} = 3.5 to 16V	ΔV_{REF1}	-	3	10	mV
Reference voltage output loading change rate	I_{OUT} = -200µA to+5µA	ΔV_{REF2}	-5	-	+5	mV
CK threshold voltage	T_a = -40°C to +85°C	V_{TH}	0.8	1.25	2.0	V
CK input current	V_{CK} = 5.0V	I_{IH}	-	0	1.0	µA
	V_{CK} = 0.0V	I_{IL}	-1.0	-0.1	-	
CK input current	Watch dog timer operating V_{CT} = 1.0V	I_{CTD}	7	10	14	µA
High level output voltage	V_S open, $I_{\overline{RESET}}$ = -5µA	V_{OH1}	4.5	4.9	-	V
	V_S = 0V, I_{RESET} = -5µA	V_{OH2}	4.5	4.9	-	
Output saturation voltage	V_S = 0V, $I_{\overline{RESET}}$ = 3mA	V_{OL1}	-	0.2	0.4	V
	V_S = 0V, $I_{\overline{RESET}}$ = 10mA	V_{OL2}	-	0.3	0.5	
	V_S open, I_{RESET} = 3mA	V_{OL3}	-	0.2	0.4	
	V_S open, I_{RESET} = 10mA	V_{OL4}	-	0.3	0.5	
Output sink current	V_S = 0V, $V_{\overline{RESET}}$ = 1.0V	I_{OL1}	20	60	-	mA
	V_S open, V_{RESET} = 1.0V	I_{OL2}	20	60	-	

(1) DC Characteristics (Continued)

(V_{CC}=5V, T_a=25°C)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
C_T charge current	Power on reset operating V_{CT} = 1.0V	I_{CTU}	0.5	1.2	2.5	µA
Min. supply voltage for $\overline{RESET}$	$V_{\overline{RESET}}$ = 0.4V $I_{\overline{RESET}}$ = 0.2mA	V_{CCL1}	-	0.8	1.2	V
Min. supply voltage for RESET	V_{RESET} =VCC -0.1V R_L (2 pin - GND) = 1MΩ	V_{CCL2}	-	0.8	1.2	V

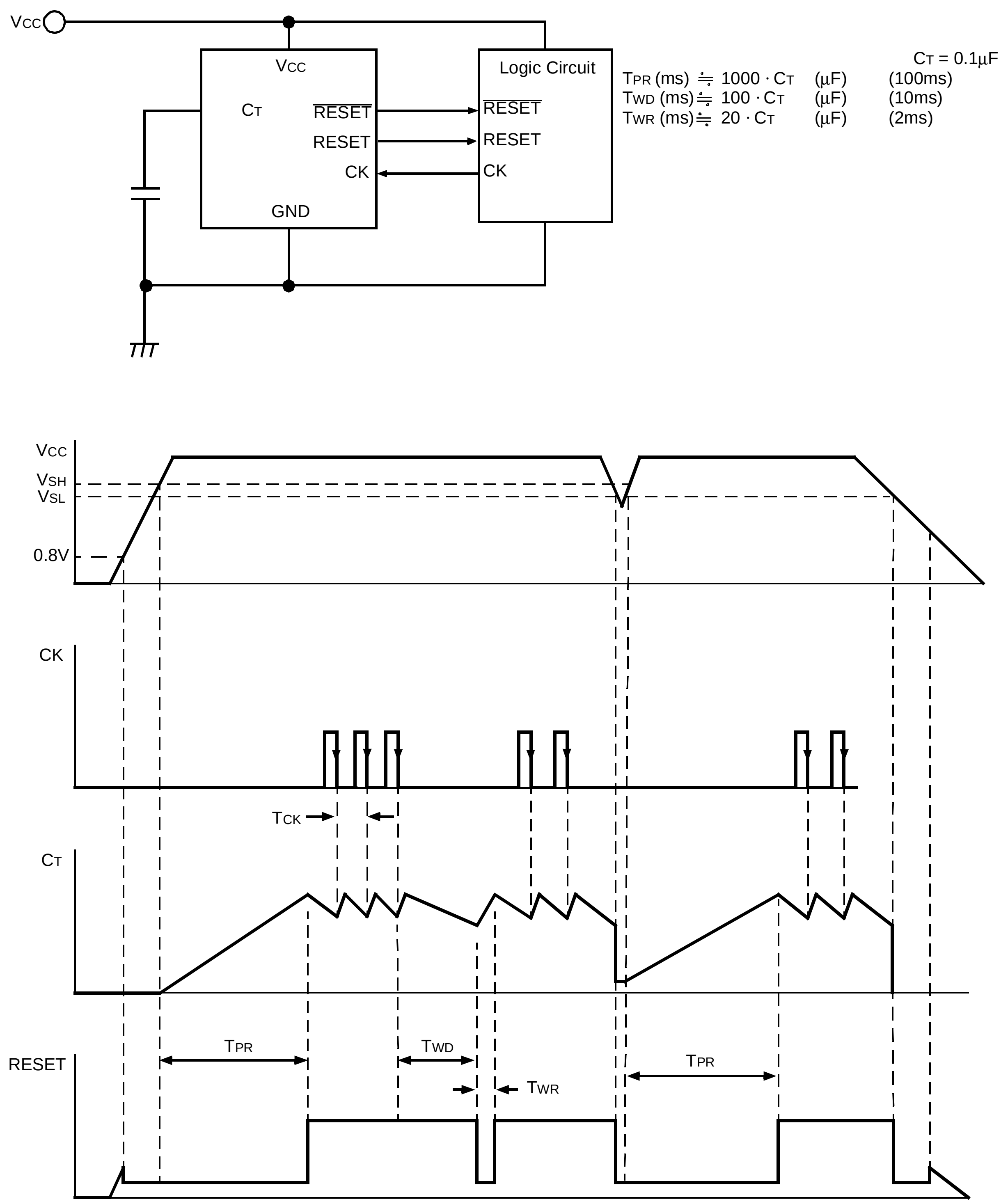
(2)AC Characteristics

(V_{CC}=5V, T_a=25°C)

Parameter	Condition	Symbol	Value			Unit
			Min	Typ	Max	
V_{CC} input pulse width	V_{CC} 5V 4V	T_{PI}	8.0	-	-	µs
CK input pulse width	CK or	T_{CKW}	3.0	-	-	µs
CK input frequency		T_{CK}	20	-	-	µs
Watch dog timer watching time	C_T = 0.1µF	T_{WD}	5	10	15	ms
Watch dog timer reset time	C_T = 0.1µF	T_{WR}	1	2	3	ms
Rising reset hold time	C_T = 0.1µF, V_{CC}	T_{PR}	50	100	150	ms
Output propagation Delay time from V_{CC}	$\overline{RESET}$, R_L = 2.2kΩ C_L = 100pF	T_{PD1}	-	2	10	µs
	RESET, R_L = 2.2kΩ C_L = 100pF	T_{PD2}	-	3	10	
Output rising time *	R_L = 2.2kΩ C_L = 100pF	t_R	-	1.0	1.5	µs
Output falling time *	R_L = 2.2kΩ C_L = 100pF	t_F	-	0.1	0.5	

* Output rising/falling time are measured at 10% to 90% of voltage.

Fig. 1 - MB3773 Basic Operation



■ TYPICAL CHARACTERISTIC CURVES

Fig. 2 - Supply current vs. supply voltage

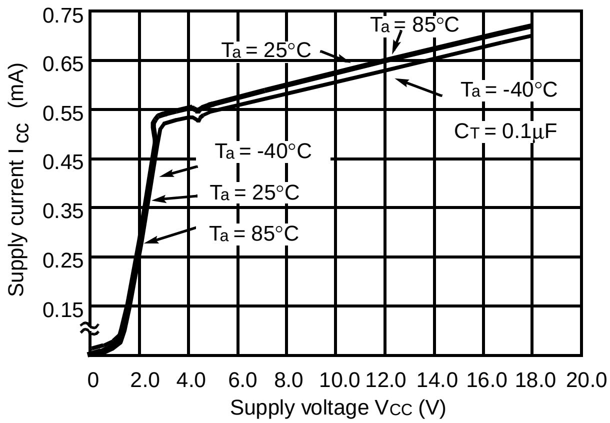


Fig. 3 - Output voltag vs. supply voltage

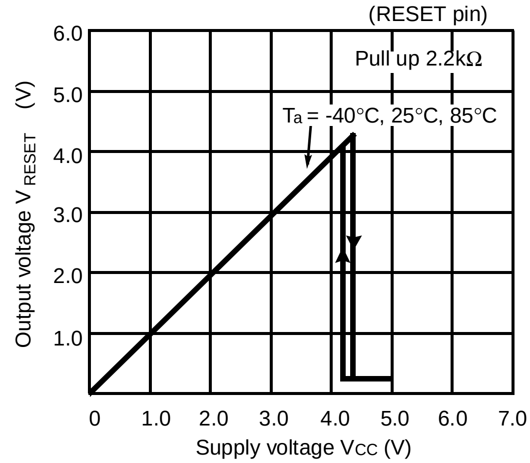


Fig. 4 - Output voltag vs. supply voltage

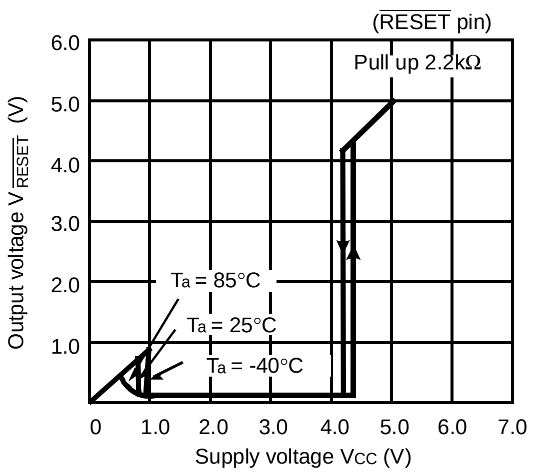


Fig. 5 - Detection voltage (VSH, VSL) vs. temperature

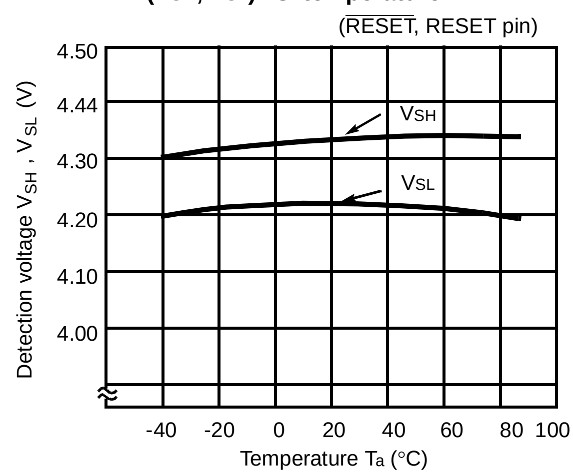


Fig. 6 - Output saturation voltage vs. output sink current

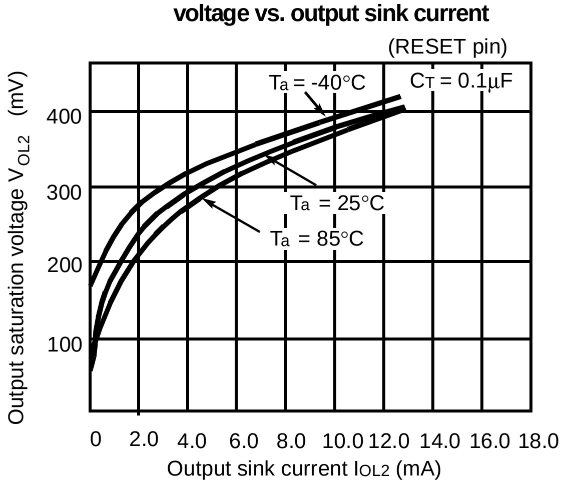
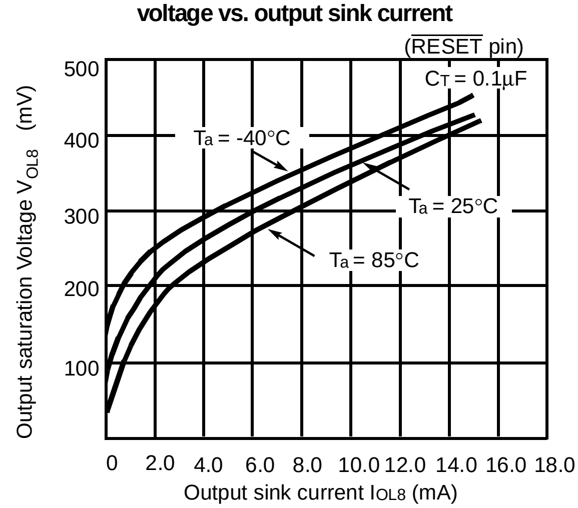


Fig. 7 - Output saturation voltage vs. output sink current



■ TYPICAL CHARACTERISTIC CURVES (Continued)

Fig. 8 - High level output voltage vs. high level output current

(RESET pin)

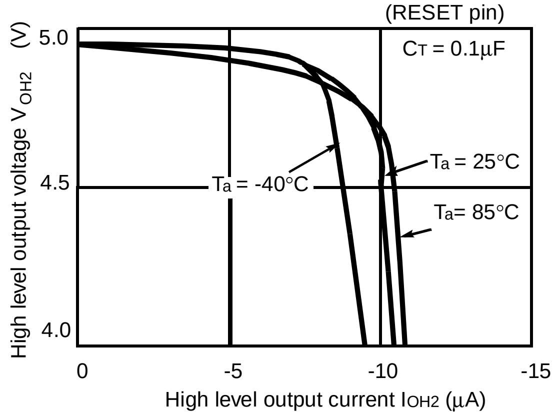


Fig. 9 - High level output voltage vs. high level output current

($\overline{RESET}$ pin)

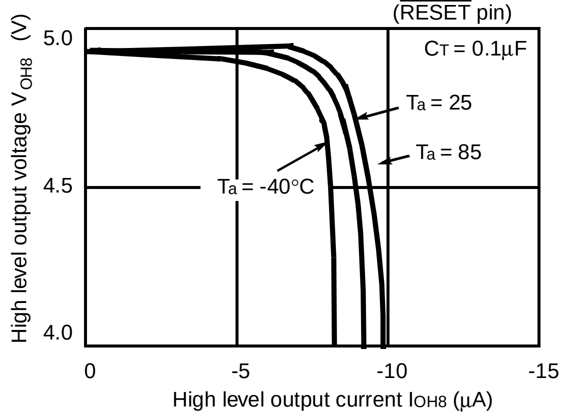


Fig. 10 - Reference voltage vs. supply voltage

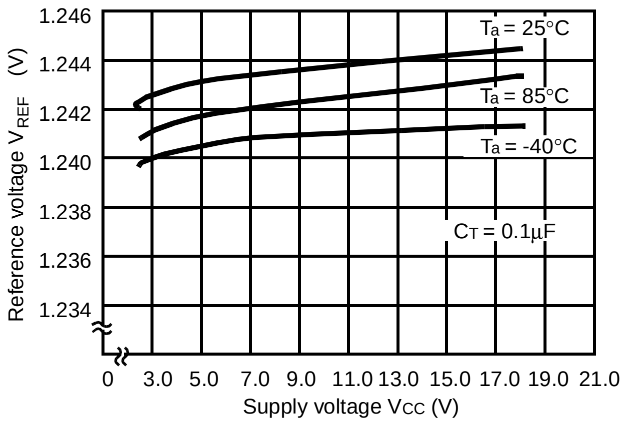


Fig. 11 - Reference voltage vs. reference current

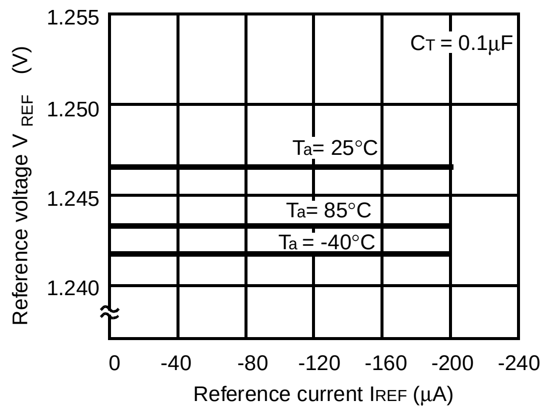


Fig. 12 - Reference voltage vs. temperature

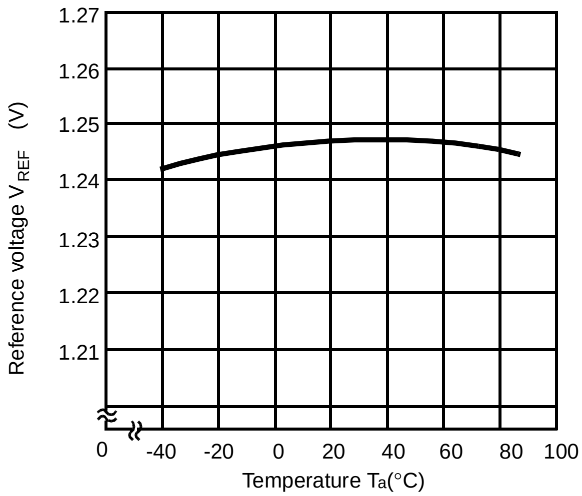
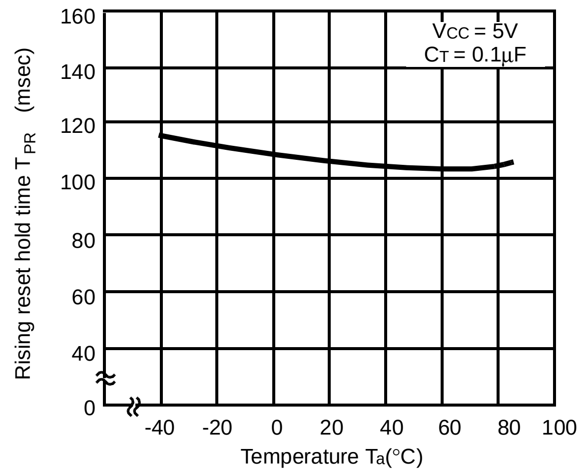


Fig. 13 - Rising reset hold time vs. temperature



■ TYPICAL CHARACTERISTIC CURVES (Continued)

Fig. 14 - Reset time vs. temperature

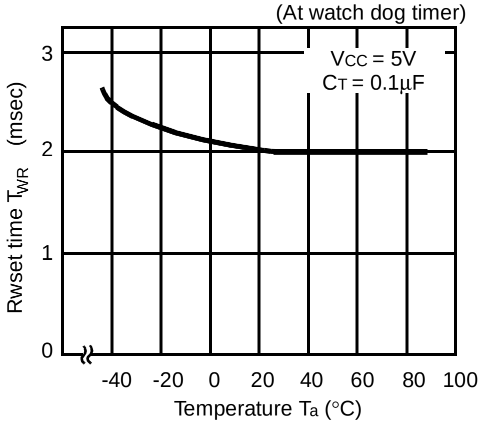


Fig. 15 - Watch dog timer watching time vs. temperature

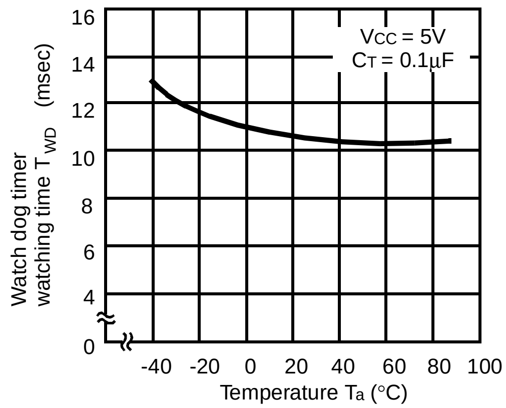


Fig. 16 - Terminal capacitance vs. rising reset hold time

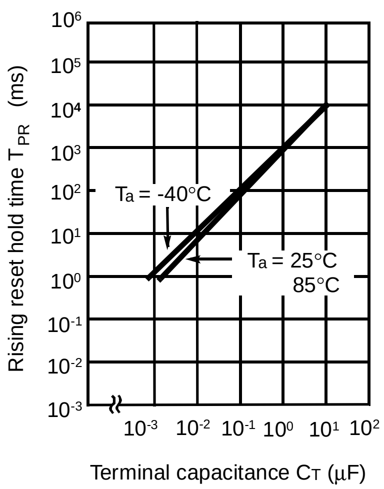


Fig. 17 - Terminal capacitance vs. reset time

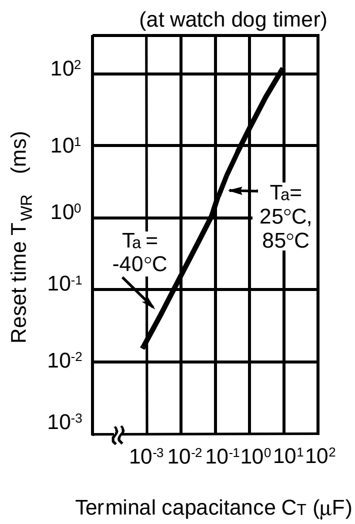
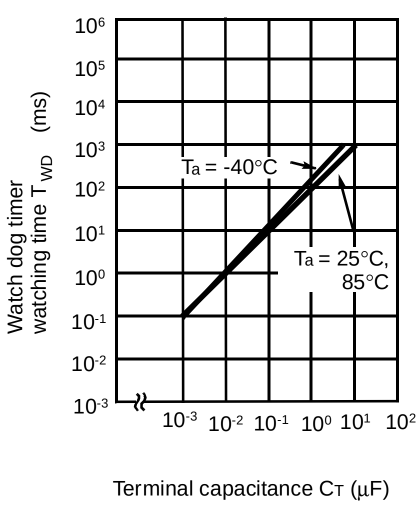
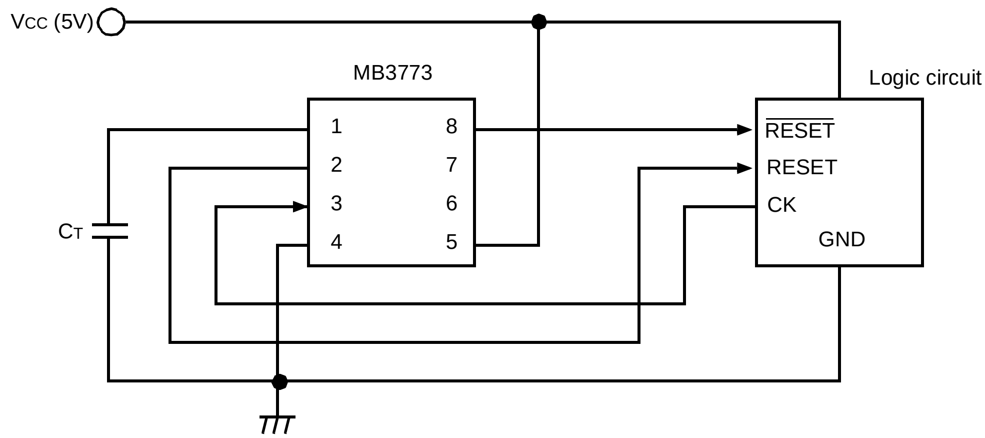


Fig. 18 - Terminal capacitance vs. watch dog timer watching time



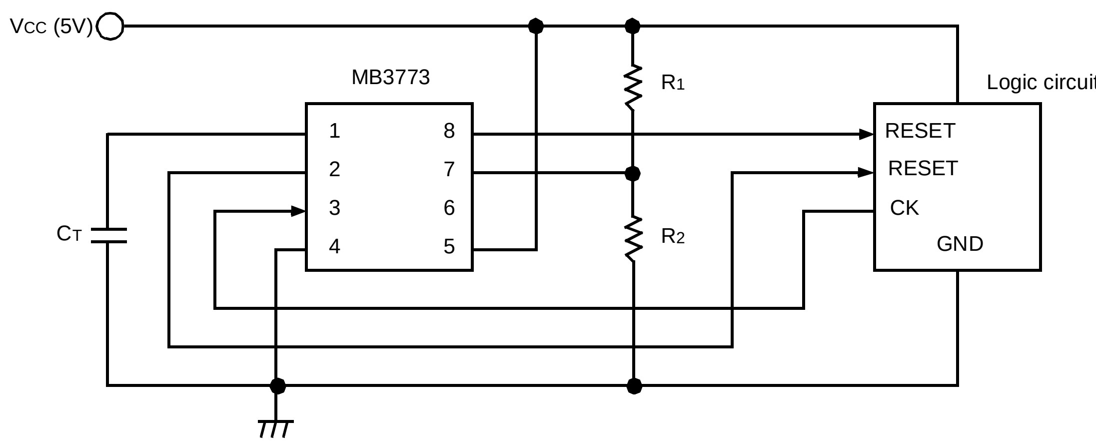
■ APPLICATION CIRCUIT

EXAMPLE 1 : Monitoring 5V Supply Voltage and Watch-dog Timer



- Supply voltage is monitored using Vs.
  Detection voltage are VSH and VSL.

EXAMPLE 2 : 5V Supply Voltage Monitoring (external fine-tuning type)

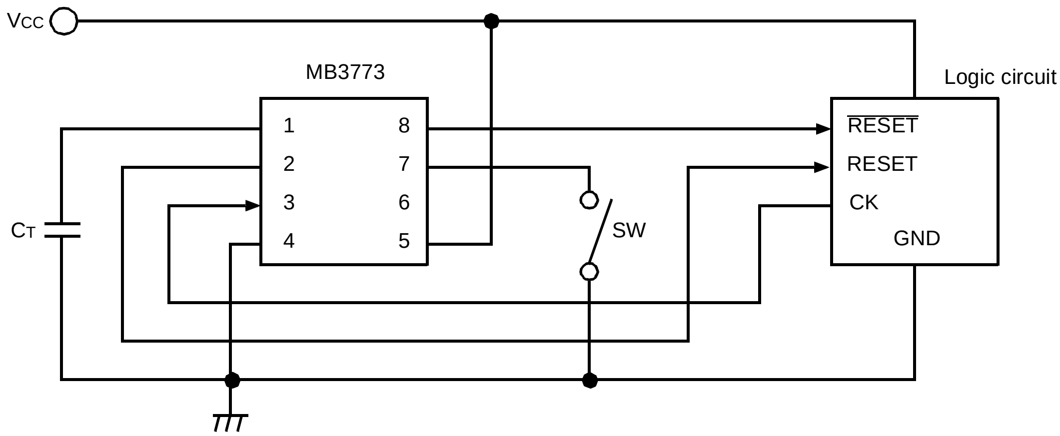


- Vs detection voltage can be adjusted externally.
- Selecting R_1 and R_2 values that are sufficiently lower than the resistance of the IC's internal voltage divider allows the detection voltage to be set according to the resistance ratio between R_1 and R_2. (See the table below.)

R_1 (kΩ)	R_2 (kΩ)	Detection voltage:V_{SL} (V)	Detection voltage:V_{SH} (V)
10	3.9	4.4	4.5
9.1	3.9	4.1	4.2

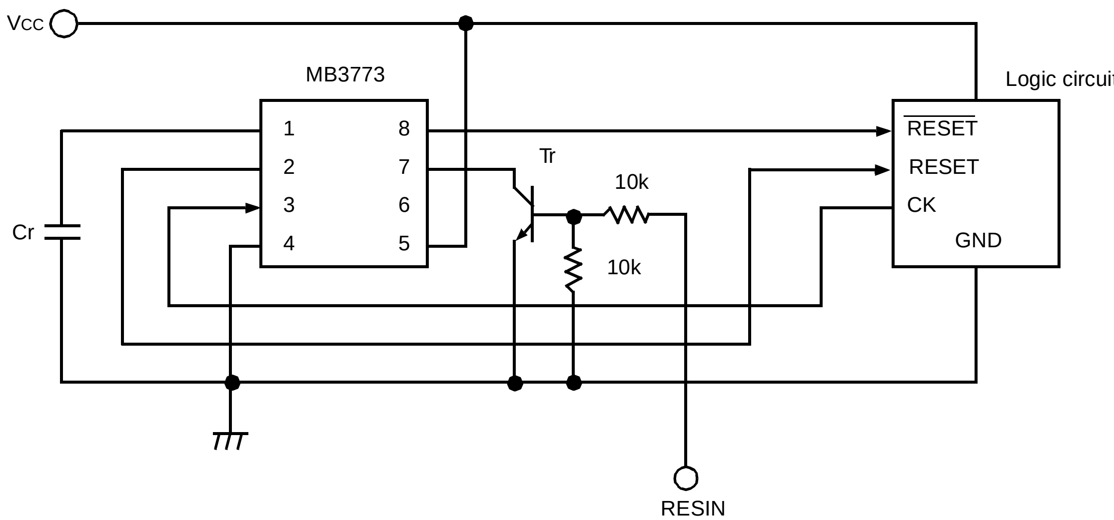
EXAMPLE 3 : With Forced Reset (with reset hold)

a



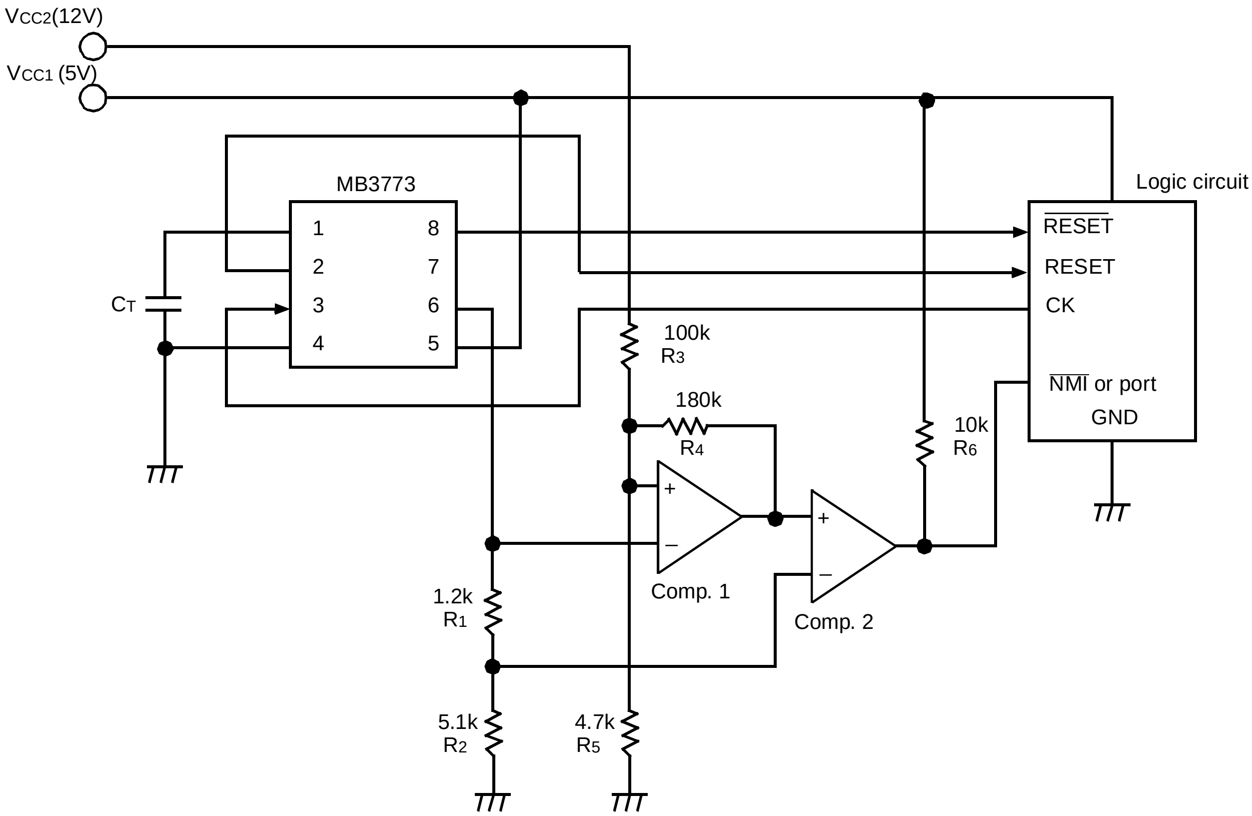
- Grouding pin 7 at the time of SW ON sets $\overline{\text{RESET}}$ (pin 8) to Low and RESET (pin 2) to High.

b



- Feeding the signal to pin RESIN and turning on Tr sets the $\overline{\text{RESET}}$ pin to Low and the RESET pin to High.

EXAMPLE 4 : Montitoring Two Supply Voltages (with hysterisis, reset output and NMI)



Example : Comp. 1, Comp. 2
: MB4204, MB47393

NOTE: The 5V supply voltage is monitored by the MB3773.
The 12V supply viltage is monitored by the external circuit. Its output is connected to the $\overline{\text{NMI}}$ pin and, when voltage drops, Comp. 2 interrrupts the logic circuit.

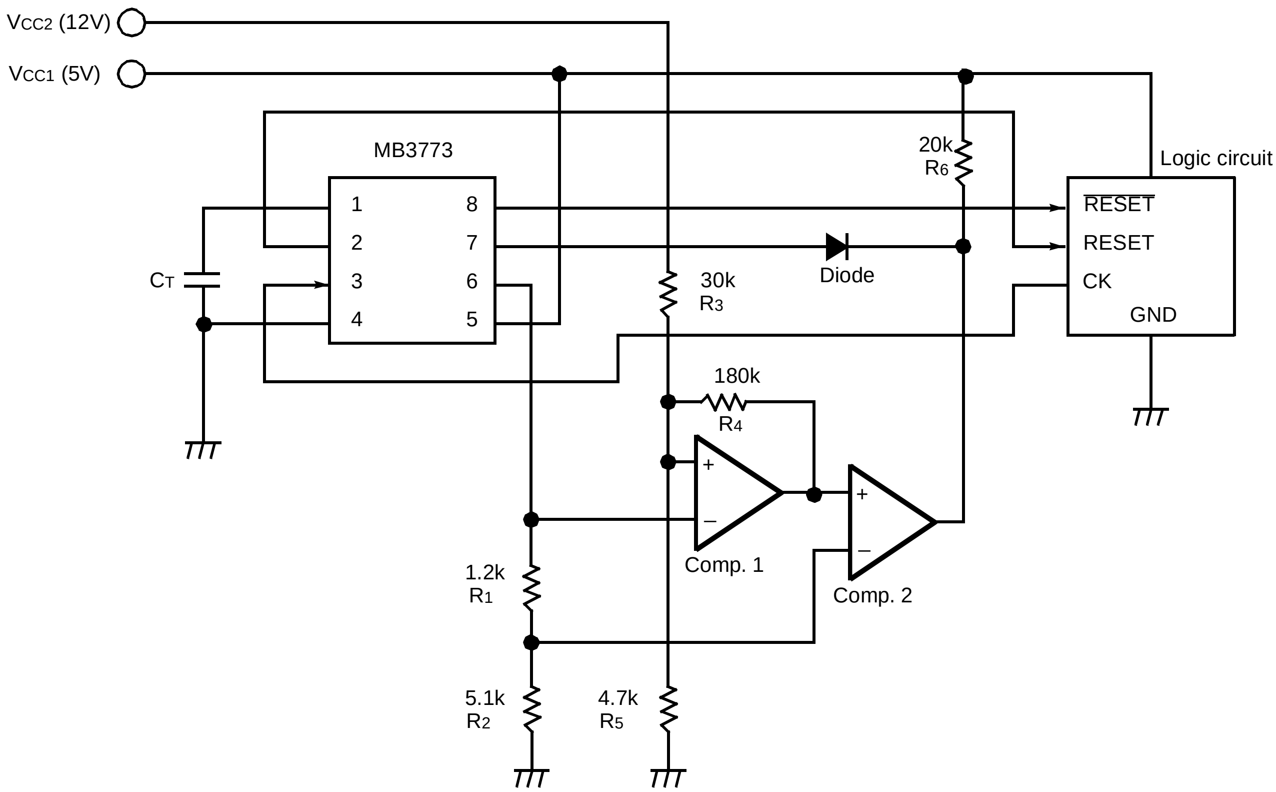
- Use $V_{CC}1$ (=5V) to power the comparators (Comp. 1 and Comp. 2) in the external circuit shown above.
- The detection voltage of the $V_{CC}2$ (=12V) supply voltage is approximately 0.2V.
  $V_{CC}2$ detection voltage and hysterisis width can be found using the following formulas:

→Detection voltage $V_{2H} = \dfrac{R_3 + (R_4 // R_5)}{R_4 // R_5} \times V_{REF}$ (Approx. 9.4V in the above illustration)

$V_{2L} = \dfrac{R_3 + R_5}{R_5} \times V_{REF}$ (Approx. 9.2V in the above illustration)

→Hysterisis width $V_{HYS} = V_{2H} - V_{2L}$

EXAMPLE 5 : Montitoring Two (M) Supply Voltages (with hysterisis and reset output)

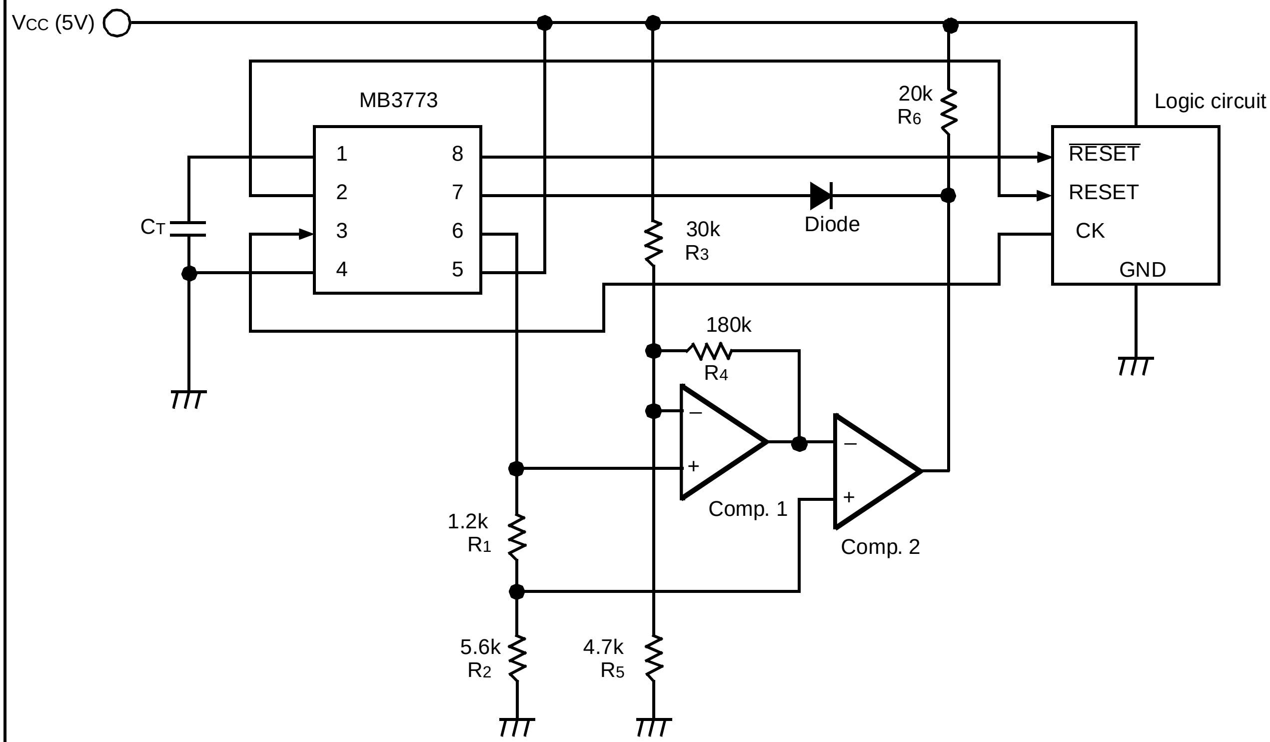


Example : Comp. 1, Comp. 2
: MB4204, MB47393

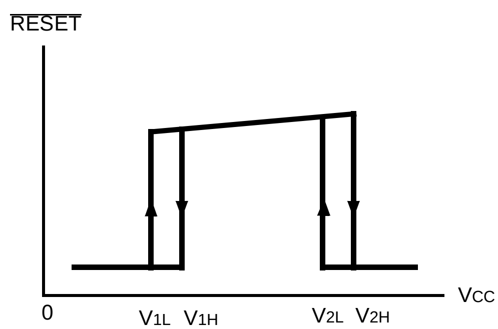
NOTE: When either 5V or 12V supply voltage decreases below its detection voltage (V_{SL}), the MB3773 RESET pin is set to High and the MB3773 $\overline{\text{RESET}}$ pin is set to Low.

- Use $V_{CC}1$ (=5V) to power the comparators (Comp. 1 and Comp. 2) in the external circuit shown above.
- The detection voltage of the $V_{CC}2$ (=12V) supply voltage is approximately 9.2V/9.4V and has a hysterisis width of approximately 0.2V.
  For the formulas for finding hysterisis width and detection voltage, see section 4.

EXAMPLE 6 : Montitoring Low voltage and Overvoltage Monitoring (with hysterisis)

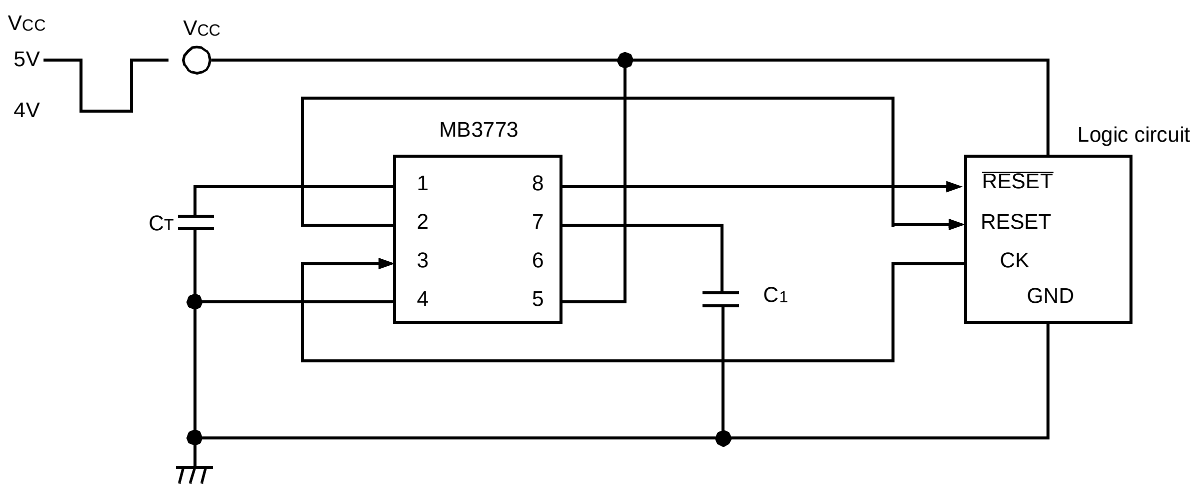


Example : Comp. 1, Comp. 2
: MB4204, MB47393



- Comp. 1 and Comp. 2 are used to monitor for overvoltage while the MB3773 is used to monitor for low voltage.
  Detection voltages V_1/V_{1H} at the time of low voltage areappoximately 4.2V/4.3V. Detection voltages V_{2L}/V_{2H} at the time of overvoltage are approximately 6.0V/6.1V.
  For the formulas for finding hysterisis width and detection voltage, see section 4.
- Use V_{CC} (=5V) to power the comparators (Comp. 1 and Comp. 2) in the external circuit shown above.

EXAMPLE 7 : Monitoring Supply Voltage Using Delayed Trigger



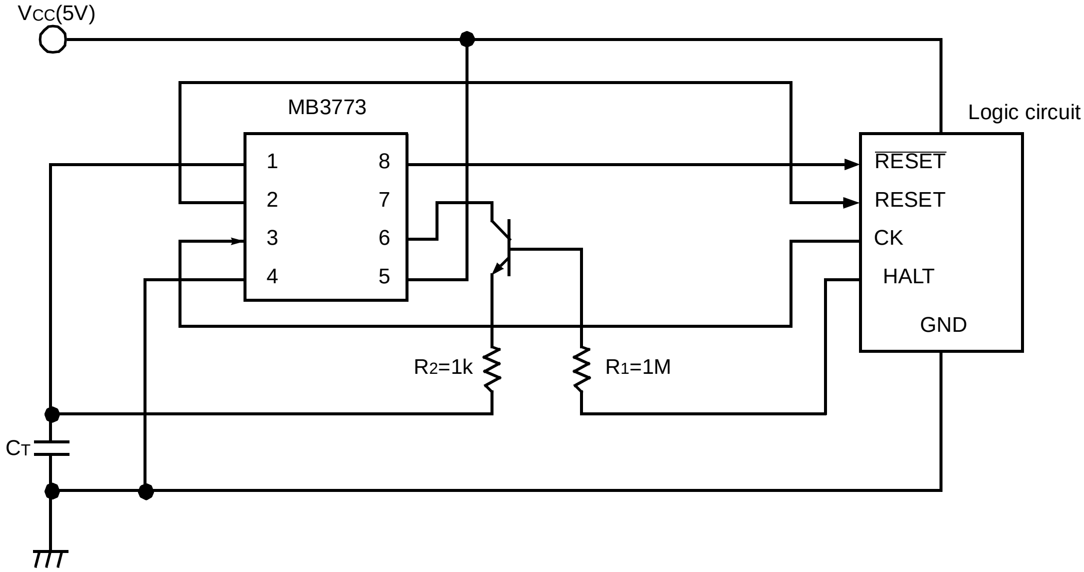
- Adding voltage such as shown in the figure to VCC increases the minimum input pulse width by 50 microseconds (C_1 = 1000pF).

EXAMPLE 8 : Stopping Watch-dog Timer (Monitering only supply voltage)

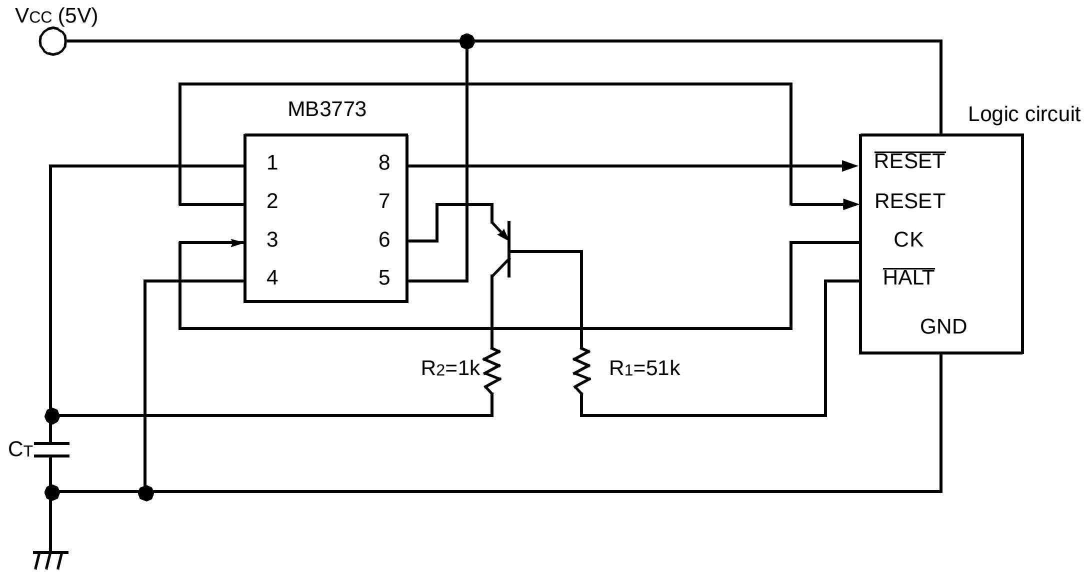
These are example application circuts in which the MB3773 monitors supply voltage alone without resetting the microcomputer even if the latter, used in standby mode, stops sending the clock pulse to the MB3773.

- The watch-dog timer is inhibited by clamping the Cr pin voltage to VREF .
  The supply voltage is constantly monitored even while the watch-dog timer is inhibited.
  For this reason, a reset signal is output at the occurrence of either instataneous disruption or a sudden drop to low voltage.
  Note that in application examples a and b, the hold signal is inactive when the watch-dog timer is inhibited at the time of resetting.
  If the hold signal is active when tie microcomputer is reset, the solution is to add a gate, as in examples c and d.

a Using NPN transistor



b Using PNP transistor



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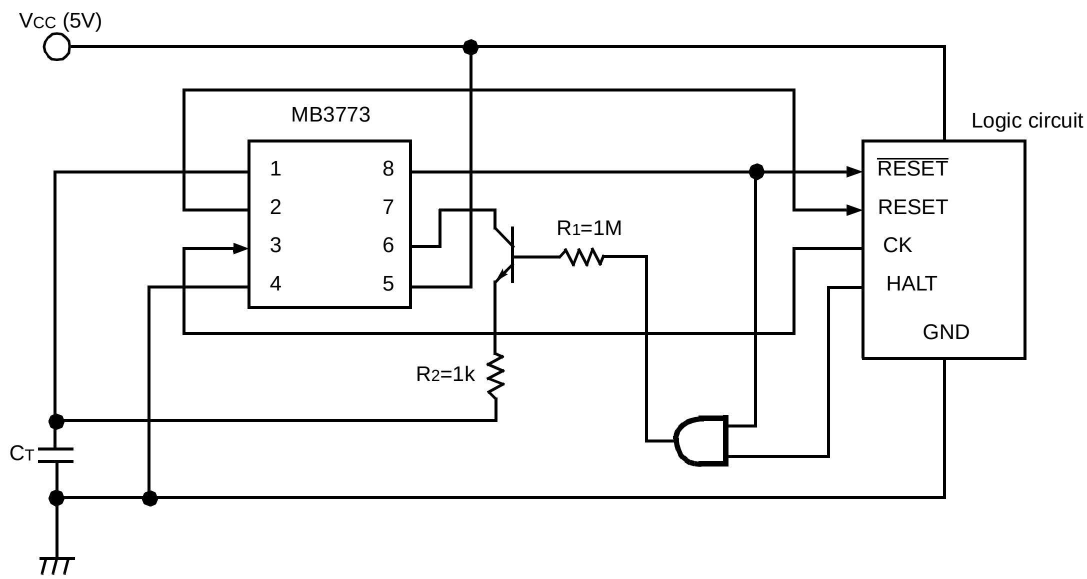
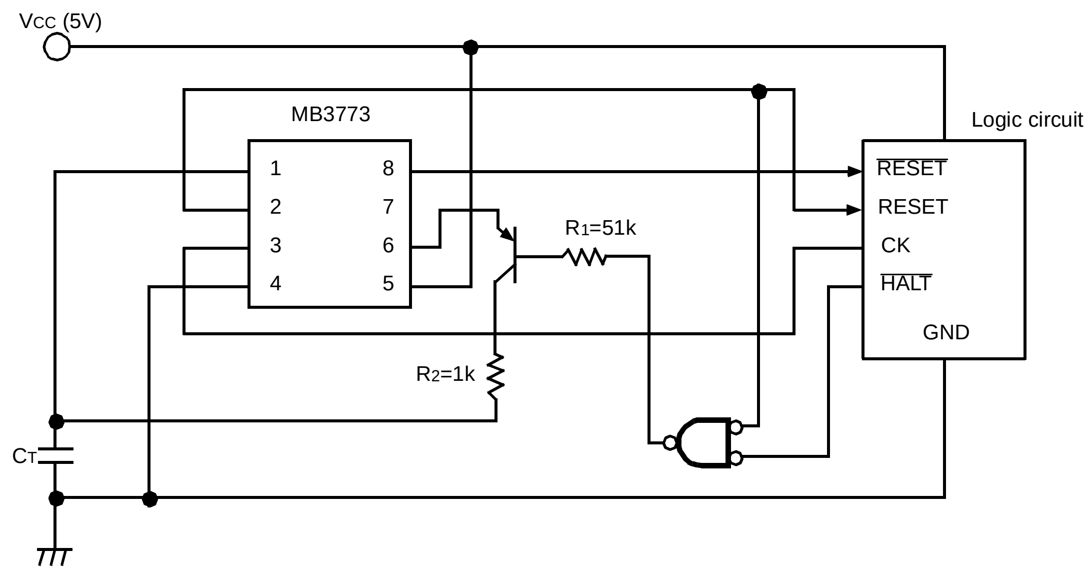
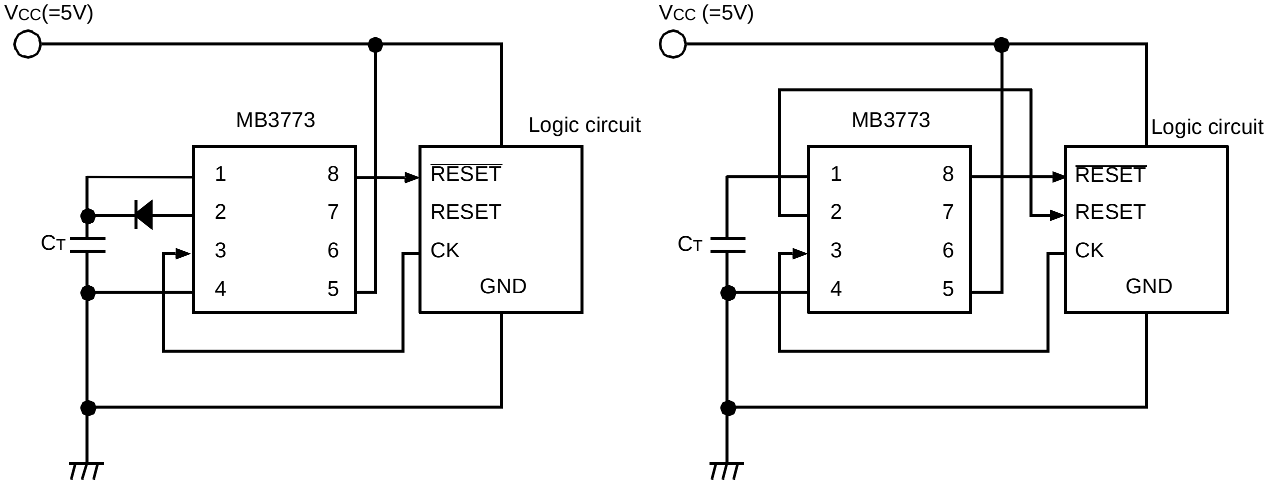
c Using NPN transistor



d Using PNP transistor



EXAMPLE 9 : Reducing Reset Hold Time



(a) T_{PR} reduction method (b) Standard usage

- $\overline{\text{RESET}}$ is the only output that can be used.
- Standard T_{PR}, T_{WD} and T_{WR} value can be found using the following formulas.

Formulas :

T_{PR} (ms) $\simeq$ 100 × C_T (µF)
T_{WD} (ms) $\simeq$ 100 × C_T (µF)
T_{WR} (ms) $\simeq$ 16 × C_T (µF)

- The above formulas allow fo standard values in determining T_{PR}, T_{WD} and T_{WR}.
  Reset hold time is compared below between the reduction circuit and the standard circuit.

C_T = 0.1µF

	T_{PR} reduction circuit	Standard circuit
T_{PR} $\simeq$	10ms	100ms
T_{WD} $\simeq$	10ms	10ms
T_{WR} $\simeq$	1.6ms	2.0ms

EXAMPLE 10 : Circuit for Monitoring Multiple Microcomputers

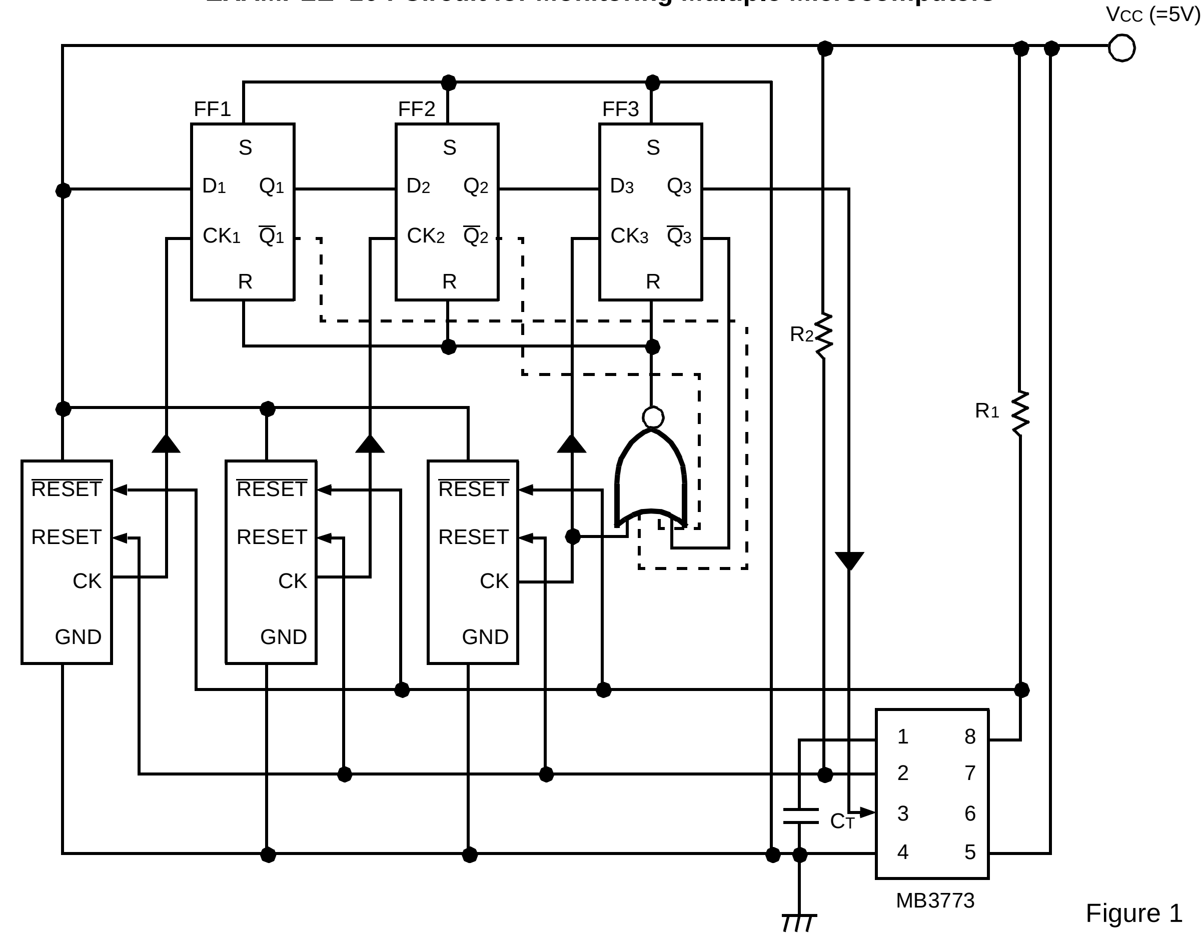


Figure 1

- - - - - - connects from FF1 and FF2 outputs Q_1 and Q_2 to the NOR input.
  Depending on timing, these connections may not be necessary.
  Example: $R_1 = R_2 = 2.2k\Omega$
  $C_T = 0.1\mu F$

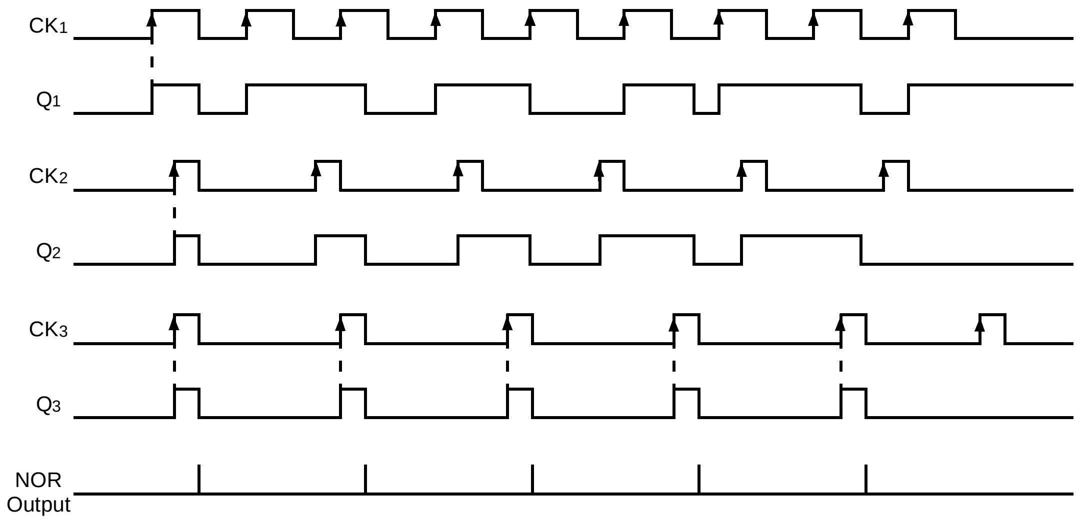


Figure 2

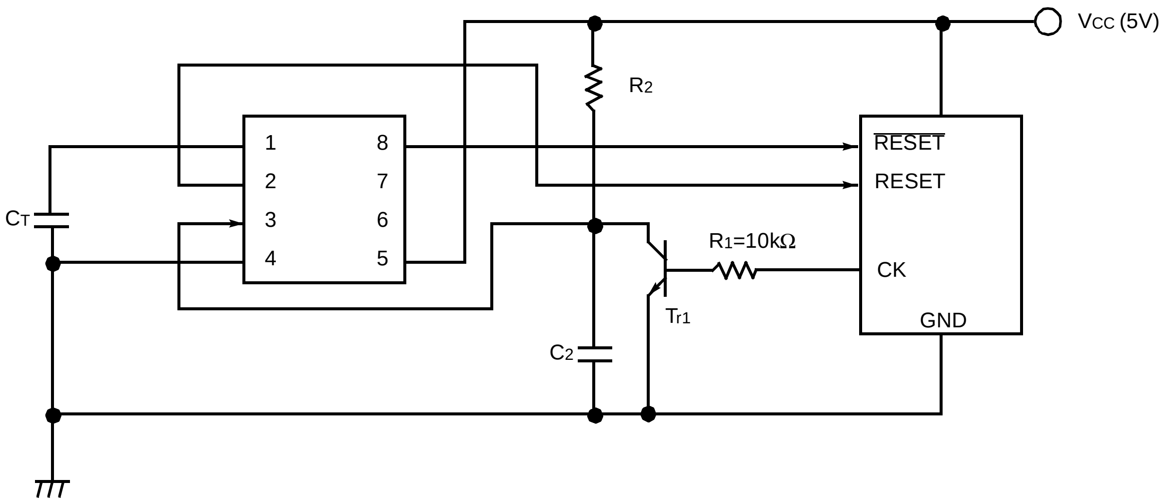
Description of Application Circuits

Using one MB3773, this application circuit monitors multiple microcomputers in one system. Signals from each microcomputer are sent to FF1, FF2 and FF3 clock inputs. Figure 2 shows these timings. Each flip-flop operates using signals sent from microcomputers as its clock pulse. When even one signal stops, the relevant receiving flip-flop stops operating. As a result, cyclical pulses are not generated at output Q_3. Since the clock pulse stops arriving at the CK pin of the MB3773, the MB3773 generates a reset signal.
Note that output Q_3 frequncy f will be in the following range, where the clock frequencies of CK1, CK2 and CK3 are f_1, f_2 and f_3 respectively.

$$\Rightarrow \quad \frac{1}{f_0} \leq \frac{1}{f} \leq \frac{1}{f_1} + \frac{1}{f_2} + \frac{1}{f_3}$$

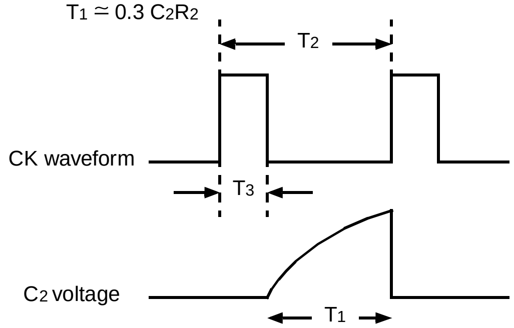
where f_0 is the lowest frequency among f_1, f_2 and f_3.

EXAMPLE 11 : Circuit for Limiting Upper Clock Input Frequency



- This is an example application to limit upper frequency f_H of clock pulses sent from the microcomputer.
  If the CK cycle sent from the microcomputer exceeds f_H, the circuit generates a reset signal.
  (The lower freqency has already been set using Cr.)
- When a clock pulse such as shown below is sent to pin CK, a short T_2 prevents C_2 voltage from reaching the CK input threshold level (≃1.25V), and will cause a reset signal to be output.
  The T_1 value can be found using the following formula :

$T_1 \simeq 0.3\ C_2 R_2$



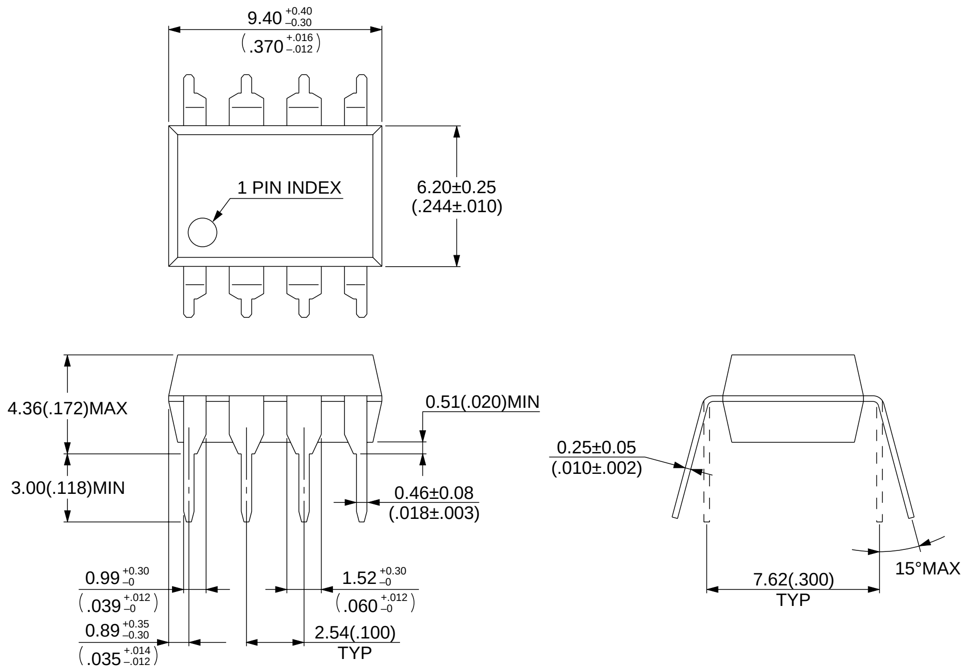
where V_{CC} = 5V, $T_3 \geq 3.0\mu sec$, $T_2 \geq 20\mu sec$

Example : Setting C and R allow the upper T_1 value to be set (See the table below.)

C	R	T_1
0.01µF	10kΩ	30µs
0.1µF	10kΩ	300µs

■ PACKAGE DIMENSIONS

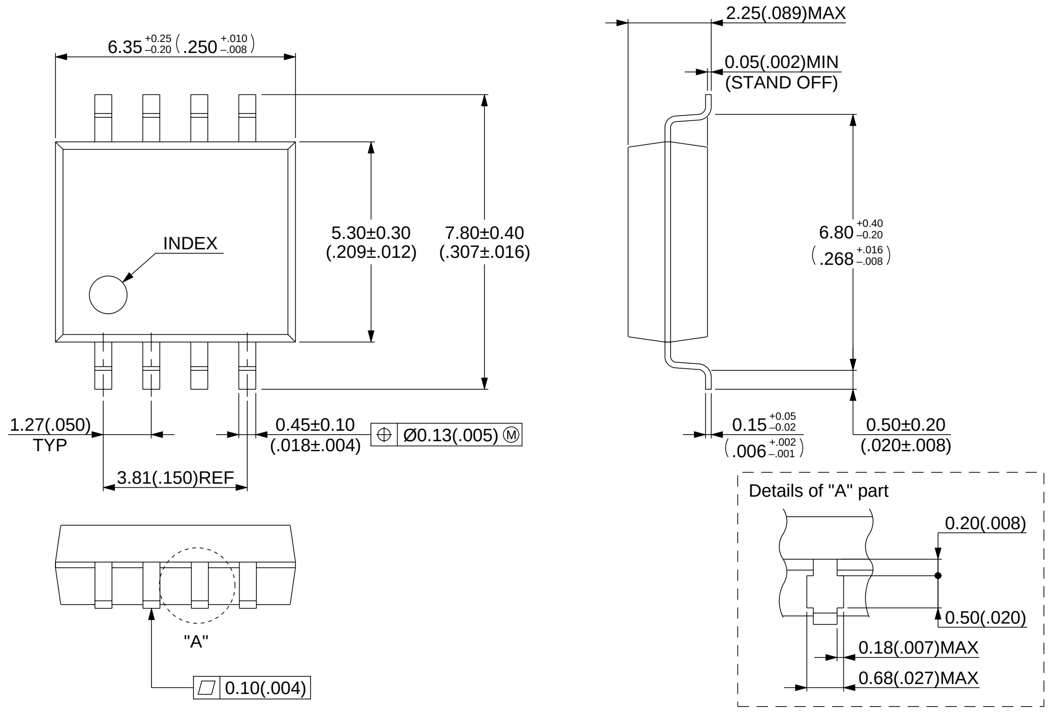
8 pin, Plastic DIP
(DIP-8P-M01)



Dimensions in mm (inches).

■ PACKAGE DIMENSIONS (Continued)

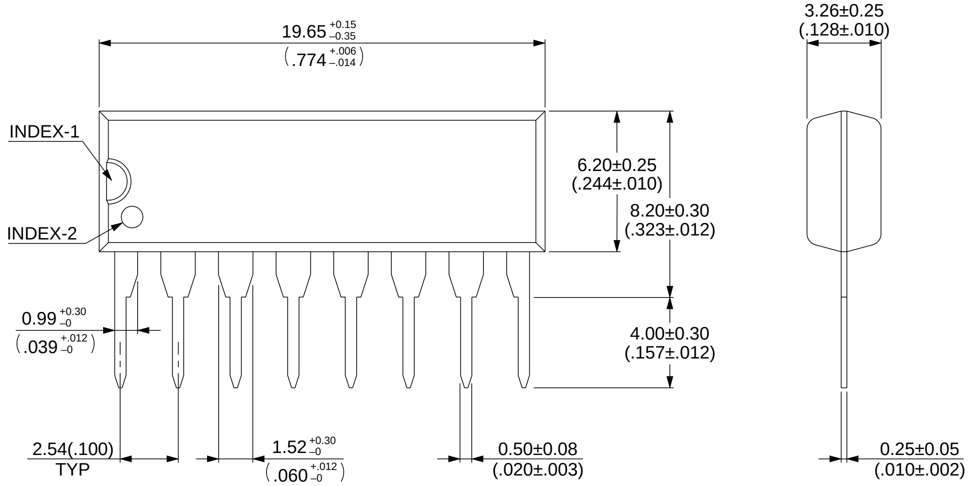
8 pin, Plastic SOP
(FPT-8P-M01)



Dimensions in mm (inches).

■ PACKAGE DIMENSIONS (Continued)

8 pin, Plastic SIP
(SIP-8P-M03)



Dimensions in mm (inches).

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