Enrico Caruso 14
Muxless/UMA Schematics Document
Sandy Bridge
Intel PCH
2011-04-07
REV : A00

```
DY :      None Installed
UMA:      UMA ONLY installed
PSL:      KBC795 PSL circuit for 10mW solution installed.
10mW:     External circuit for 10mW solution installed.
DIS:      MUXLESS solution installed.
Surge:    For GO Rural config stuff.
GIGA:     For GIGA LAN config stuff.
HDMI:     For HDMI config stuff.
DIS_CRT:  Pure DIS install
```

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Cover Page		
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Block Diagram (Discrete/UMA co-lay)

##OnMainBoard

Project code: 91.4IU01.001
PCB P/N : 48.4IU16.0SC
Revision : 10315-SC

VRAM gDDR3 900NHz
1GB (128Mx16x4)
512MB (64Mx16x4)
88,89,90,91

gDDR3 900MHz

Seymou-XT S3
83.84,85,86,87

PCIe x 8
(Discrete only)

Intel CPU
Sandy Bridge
4,5,6,7,8,9,10

DDRIII 1066/1333 Channel A
DDRIII 1066/1333 Channel B

DDRIII Slot 0 1066/1333 15
DDRIII Slot 1 1066/1333 14

FDIx4x2
DMIx4 1GB/s

Intel PCH
Cougar Point
14 USB 2.0/1.1 ports
ETHERNET (10/100/1000Mb)
High Definition Audio
SATA ports (6)
PCIE ports (8)
LPC I/F
ACPI 1.1
17,18,19,20,21,22,23,24,25

PCIE x 1
10/100 /1000 LOM
Realtek RTL8111E (Giga LAN)
Realtek RTL8105E (10M/100M) 31
RJ45 CONN 59

PCIE x 1
802.11a/b/g
Mini-Card WLAN+BT3.0 64

PCIE 100MHz 2.5Gbps

CRT 50
LCD 49
HDMI 51

CRT
LVDS
HDMI

USB 2.0 x 1
CAMERA 49

USB 2.0 480Mbps
USB 2.0 x 1
M/B USB x1 (Left) 61

USB 2.0 x 2
I/O board USB x2 (Right) 82

SD/MMC/MS/ MS Pro 74
CardReader
Realtek RTS5138 32
USB2.0

LPC Bus 33MHz

KBC
NUVOTON
NPCE795BA0DX 27

PS/2
PS/2
Touch PAD 69
Int. KB 69

Thermal
ENE P2800 28
ENE P2793 Fan 28

Audio board
Internal Analog MIC 58
HP1 82
MIC IN
2CH SPEAKER 58

Azalia CODEC
IDT 92HD87 29
AZALIA 24MHz

SATA
SATA 3Gbps
SPI

HDD 56
ODD 56
Flash ROM 4MB 60

SYSTEM DC/DC APL5916 48	
INPUTS	OUTPUTS
DCBATOUT	0D85V_S0

CPU DC/DC VT1316+1314 42~44	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51218 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC TPS51125 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5 15V_S5

SYSTEM DC/DC TPS51216R 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

GFX DC/DC VT1316+1317 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE

VGA RT8208B 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24707 40	
INPUTS	OUTPUTS
+DC_IN_S5 +PBATT	DCBATOUT

SYSTEM DC/DC APW7153B 47	
INPUTS	OUTPUTS
3D3V_S5	1D8V_S0

SYSTEM DC/DC G9731 93	
INPUTS	OUTPUTS
1D5V_S3 3D3V_S0	1V_VGA_S0 1D8V_VGA_S0
Switches	
INPUTS	OUTPUTS
1D5V_S3 5V_S5 3D3V_S5	1D5V_S0 5V_S0 3D3V_S0

PCB LAYER

L1:Top L4:Signal
L2:GND L5:VCC
L3:Signal L6:Bottom

<Core Design>

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PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-k - 10-k weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	**Enable Danbury:** Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. **Disable Danbury:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] **Disable Danbury:** Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	**PCI-Express Port Bifurcation Straps**	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	**PEG DEFER TRAINING**	**1:** PEG Train immediately following xxRESETB de assertion **0:** PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

SATA Table

SATA	
Pair	Device
0	HDD1
1	N/A
2	N/A
3	N/A
4	ODD
5	N/A

USB Table

Pair	Device
0	X
1	USB Ext. port 2 (MB)
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 3
9	USB Ext. port 1
10	X
11	Mini Card1 (WLAN+BT)
12	CAMERA
13	X

SMBus ADDRESSES

I² C / SMBus Addresses Device	Ref Des	HURON RIVER ORB Address	Hex	Bus
EC SMBus 1 Battery CHARGER				BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP				SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI				PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

PCIE Routing

LANE1	X
LANE2	LAN
LANE3	X
LANE4	Wireless
LANE5	X
LANE6	X
LANE7	X
LANE8	X

DN15ATI Whistler

Wistron Corporation
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Title: Table of Content

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SSID = CPU

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics function for power saving.

NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

NOTE:
Select a Fast FET similar to 2N7002E whose rise/ fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-k pull-Up resistor on the motherboard.

CPU1A — SANDY — 1 OF 9 — CPU1 — SANDY SKT-BGA989C470395-1H180

62.10055.421

2nd = 62.10040.771

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Title: CPU (PCIE/DMI/FDI)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

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SSID = CPU

Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through 1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP through 1K +/- 5% resistorpower (~15 mW) may be wasted.

CPU1B — 2 OF 9 — SANDY

MISC: SNB_IVB#, SKTOCC#
THERMAL: CATERR#, PECI, PROCHOT#, THERMTRIP#
PWR MANAGEMENT: PM_SYNC, UNCOREPWRGOOD, SM_DRAMPWROK, RESET#
CLOCKS: BCLK, BCLK#, DPLL_REF_SSCLK, DPLL_REF_SSCLK#
DDR3 MISC: SM_DRAMRST#, SM_RCOMP0, SM_RCOMP1, SM_RCOMP2
JTAG & BPM: PRDY#, PREQ#, TCK, TMS, TRST#, TDI, TDO, DBR#, BPM#0–BPM#7

CPU1

SANDY SKT-BGA989C470395-1H180
62.10055.421
2nd = 62.10040.771

1D05V_VTT
R501 62R2J-GP
H_PROCHOT#
C502 SC47P50V2JN-3GP
CRB : 47pf
CEKLT:43pf

18 H_SNB_IVB# — C26 SNB_IVB#
TPAD14-GP TP501 — SKTOCC# R — AN34 SKTOCC#
TPAD14-GP TP502 — H_CATERR# — AL33 CATERR#
22,27 H_PECI — AN33 PECI
27,40,42 H_PROCHOT# — R513 56R2J-4-GP — H_PROCHOT# R — AL32 PROCHOT#
Connect EC to PROCHOT# through inverting OD buffer.
22,36,85 H_THERMTRIP# — AN32 THERMTRIP#

19 H_PM_SYNC — AM34 PM_SYNC
22,36 H_CPUPWRGD — R504 0R0402-PAD — CPUPWRGD_R — AP33 UNCOREPWRGOOD
X01-0127 Add C504 for noise couple.
R503 10KR2J-3-GP
C504 SCD1U10V2KX-5GP
19,37 PM_DRAM_PWRGD — R505 0R2J-2-GP DY — VDDPWRGOOD — V8 SM_DRAMPWROK
37 VDDPWRGOOD
18,27,31,65,71,83 PLT_RST# — R510 1K5R2F-2-GP — BUF_CPU_RST# — AR33 RESET#
R509 750R2F-GP
C501 SC220P50V2KX-3GP DY

BCLK A28 — CLK_EXP_P 20
BCLK# A27 — CLK_EXP_N 20
DPLL_REF_SSCLK A16 — CLK_DP_P_R — RN502 4 3 1 2 — 1D05V_VTT
DPLL_REF_SSCLK# A15 — CLK_DP_N_R
SRN1KJ-7-GP
X01-0210 MergeR512 R514

SM_DRAMRST# R8 — R502 4K99R2F-L-GP — SM_DRAMRST# 37

SM_RCOMP0 AK1 — SM_RCOMP_0 — R506 140R2F-GP
SM_RCOMP1 A5 — SM_RCOMP_1 — R507 25D5R2F-GP
SM_RCOMP2 A4 — SM_RCOMP_2 — R508 200R2F-L-GP
Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

PRDY# AP29 — XDP_PRDY# — TP511 TPAD14-GP
PREQ# AP27 — XDP_PREQ# — TP512 TPAD14-GP
11/16 remove TP for layout space
TCK AR26 — XDP_TCLK
TMS AR27 — XDP_TMS
TRST# AP30 — XDP_TRST#
TDI AR28 — XDP_TDI
TDO AP26 — XDP_TDO
DBR# AL35 — XDP_DBRESET#

BPM#0 AT28 — XDP_BPM0 — TP503 TPAD14-GP
BPM#1 AR29 — XDP_BPM1 — TP504 TPAD14-GP
BPM#2 AR30 — XDP_BPM2 — TP505 TPAD14-GP
BPM#3 AT30 — XDP_BPM3 — TP506 TPAD14-GP
BPM#4 AP32 — XDP_BPM4 — TP507 TPAD14-GP
BPM#5 AR31 — XDP_BPM5 — TP508 TPAD14-GP
BPM#6 AT31 — XDP_BPM6 — TP509 TPAD14-GP
BPM#7 AR32 — XDP_BPM7 — TP510 TPAD14-GP

12/6 swap net for layout
1D05V_VTT
RN501 SRN51J-1-GP
XDP_TDI
XDP_TMS
XDP_TDO
XDP_TCLK
XDP_TRST# R511 51R2J-2-GP

3D3V_S0
19 XDP_DBRESET# — XDP_DBRESET# — R516 10KR2J-3-GP

Buffered reset to CPU
1D05V_VTT
R518 75R2J-1-GP DY
3D3V_S0
C503 SCD1U10V2KX-5GP DY
U501 74VHC1G09DFT2G-GP
IN B VCC
IN A DY
GND OUT Y
18,27,31,65,71,83 PLT_RST#
BUFO_CPU_RST#
R517 43R2J-GP DY
BUF_CPU_RST#
R515 0R2J-2-GP DY
73.01G09.AAH

<Core Design>
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Title: CPU (THERMAL/CLOCK/PM)
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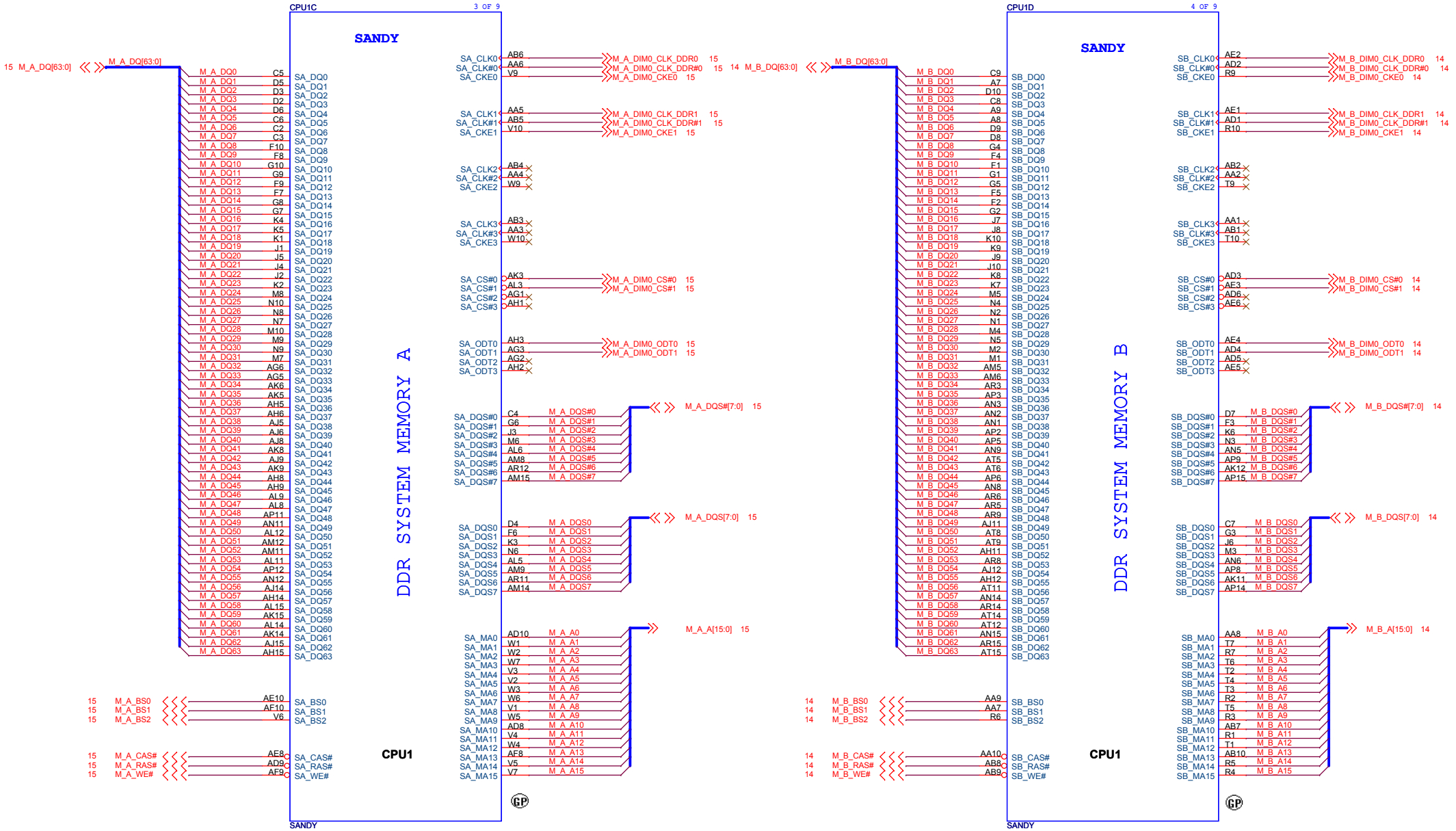
SSID = CPU



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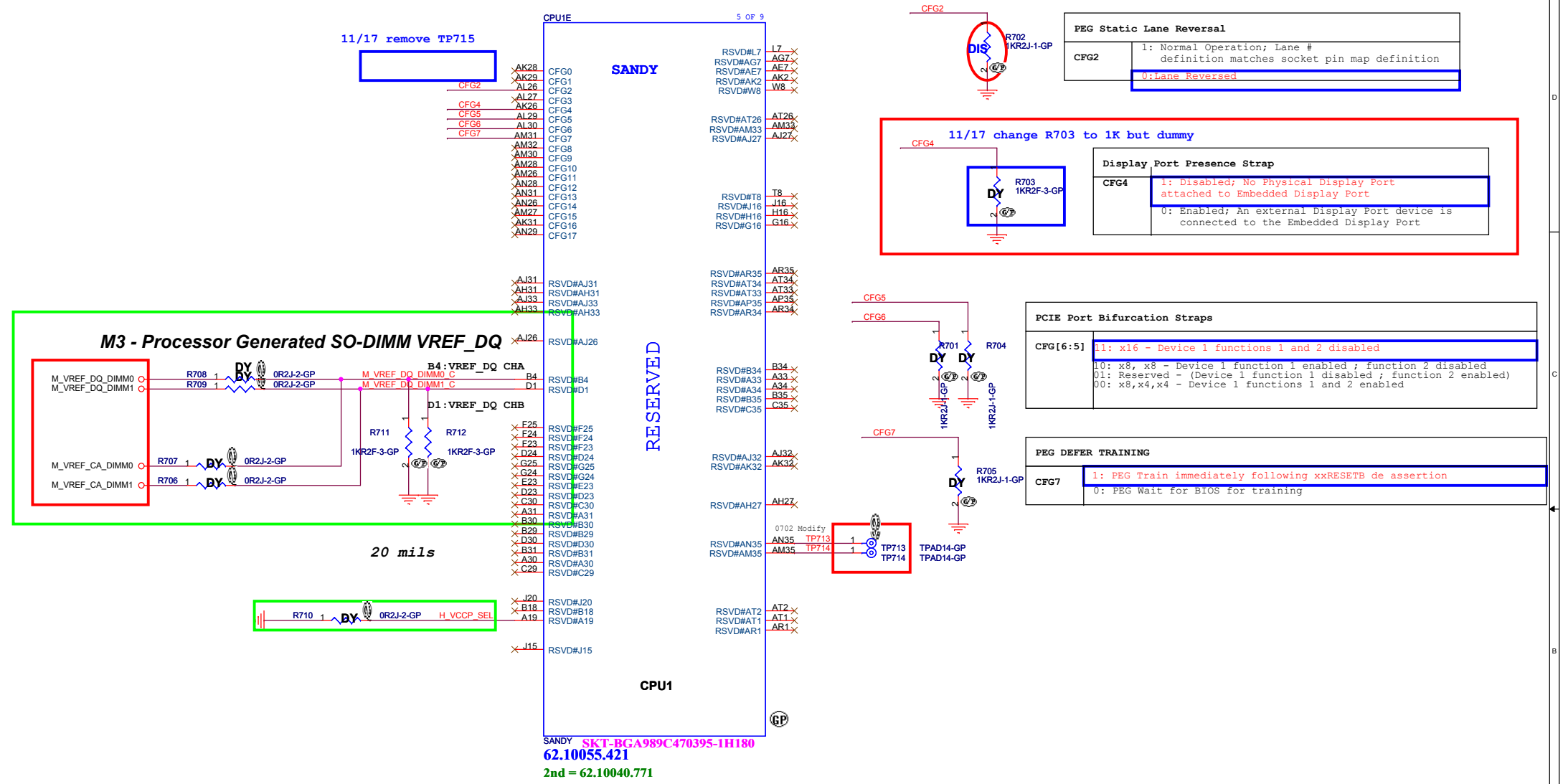
Title: CPU (DDR)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 6 of 105

SSID = CPU



DN15ATI Whistler

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Title: CPU (RESERVED)

Size	Document Number	Rev
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SSID = CPU

POWER

Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

PROCESSOR CORE POWER

53A

11/15 change Caps to 78.22610.51L

12/23 stuff the capacities

12/28 Yellow mark for OPI change

VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

11/4 add Caps to 28 location as vendor recommand.

X01-0127 Stuff C812, C822, C831, C834
for VCC core noise issue.

X01-0217 Stuff C801=22uF
change C817 to 22uF

CPU1F

SANDY

6 OF 9

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

CPU1

VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top

12/28 Yellow mark for OPI change

PROCESSOR VCCIO: 8.5A

12/23 stuff the capacities

No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.

11/16 follow DN13 to meet schematic check list

These resistors need to close to power IC

11/17 change part refernce R807 to R805

VR_SVID_ALERT# R805 75R2J-1-GP

H_CPU_SVIDCLK R806 54D9R2F-L1-GP

H_CPU_SVIDDAT R804 130R2F-1-GP

VIDALERT# AJ29 H_CPU_SVIDALRT# R803 43R2J-GP

VIDSCLK AJ30 H_CPU_SVIDCLK

VIDSOUT AJ28 H_CPU_SVIDDAT

VCC_SENSE AJ35

VSS_SENSE AJ34

VCCIO_SENSE B10

VSSIO_SENSE A10

R801 100R2F-L1-GP-U

R802 100R2F-L1-GP-U

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_CORE)

Size: Custom | Document Number: Enrico Caruso 14 | Rev: A00

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SSID = CPU

VAXG Output Decoupling Recommendation:
2 x 470 uF at Bottom Socket Edge
2 x 22 uF at Top Socket Cavity
4 x 22 uF at Top Socket Edge
2 x 22 uF at Bottom Socket Cavity
4 x 22 uF at Bottom Socket Edge

Voltage Rail	Voltage	Iccmax
VCC_CORE(QC)	0.8~1.35	94A
VCC_CORE(DC)	0.8~1.35	53A
VCCIO	1.05	8.5A
VDDQ	1.5	10A
VCCSA	0.75~0.9	6A
VCCPLL	1.8	1.2A
VAXG	0~1.52	33A

POWER

VCC_GFXCORE

CPU1G — SANDY — 7 OF 9

PROCESSOR VAXG: 33A

C901 SC4D7U6D3V5KX-3GP; C902 SC10U6D3V5KX-1GP; C904 SC10U6D3V5KX-1GP; C905 SC10U6D3V5KX-1GP; DY C906 SC10U6D3V5KX-1GP

12/28 Yellow mark for OPI

C908 SC4D7U6D3V3KX-GP; C920 SC4D7U6D3V3KX-GP; C921 SC4D7U6D3V3KX-GP

AT24 AT23 AT21 AT20 AT18 AT17 AR24 AR23 AR21 AR20 AR18 AR17 AP24 AP23 AP21 AP20 AP18 AP17 AN24 AN23 AN21 AN20 AN18 AN17 AM24 AM23 AM21 AM20 AM18 AM17 AL24 AL23 AL21 AL20 AL18 AL17 AK24 AK23 AK21 AK20 AK18 AK17 AJ24 AJ23 AJ21 AJ20 AJ18 AJ17 AH24 AH23 AH21 AH20 AH18 AH17 — VAXG

GRAPHICS

SENSE LINES

VAXG_SENSE AK35 — VCC_AXG_SENSE 42
VSSAXG_SENSE AK34 — VSS_AXG_SENSE 42

Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on S3 power reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

VREF

SM_VREF AL1 — +V_SM_VREF_CNT — +V_SM_VREF_CNT 37

Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT should have 10 mils trace width.

VCC_GFXCORE
R906 100R2F-L1-GP-U
VCC_AXG_SENSE
VSS_AXG_SENSE
R907 100R2F-L1-GP-U

DDR3 -1.5V RAILS

PROCESSOR VDDQ: 10A

1D5V_S0

VDDQ AE7 AF4 AE1 AC7 AC4 AC1 Y7 Y4 Y1 U7 U4 U1 P7 P4 P1

C909 DY SC10U6D3V3MX-GP; C910 DY SC10U6D3V3MX-GP; C911 DY SC10U6D3V3MX-GP; C912 SC4D7U6D3V5KX-3GP; C913 SC10U6D3V5KX-1GP; C914 SC10U6D3V5KX-1GP; TC901 ST330U2VDM-4-GP; C907 DY SCD1U10V2KX-5GP; C918 DY SCD1U10V2KX-5GP; C919 DY SCD1U10V2KX-5GP; C925 DY SCD1U10V2KX-5GP

1D5V_S3

12/28 Yellow mark for OPI

79.33719.20L
2nd = 77.C3371.13L

VDDQ Output Decoupling Recommendation:
1 x 330 uF
6 x 10 uF

SA RAIL

0D85V_S0

PROCESSOR VCCSA: 6A

VCCSA M27 M26 L26 J26 J25 J24 H26 H25

C916 SC10U6D3V5KX-1GP; C915 SC10U6D3V5KX-1GP; C917 SC10U6D3V5KX-1GP; DY EC902 SCD1U50V3KX-GP

VCCSA Output Decoupling Recommendation:
1 x 330 uF
2 x 10 uF at Bottom Socket Cavity
1 x 10 uF at Bottom Socket Edge

11/16 Follow Annie team's schematic by power solution

VCCSA_SENSE H23 — VCCSA_SENSE — R910 10R2J-2-GP — 0D85V_S0

R910 close to pin H23.

FC_C22 C22 — H_FC_C22
VCCSA_VID1 C24 — VCCSA_SEL — VCCSA_SEL 48

DY RN901 SRN1KJ-7-GP

11/ 17 dummy RN901

1.8V RAIL

1D8V_S0

PROCESSOR VCCPLL: 1.2A

C923 SC10U6D3V5KX-1GP; C922 SC1U10V2KX-1GP; C924 SC1U10V2KX-1GP

VCCPLL B6 A6 A2

VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

MISC

CPU1

SANDY
62.10055.421
2nd = 62.10040.771

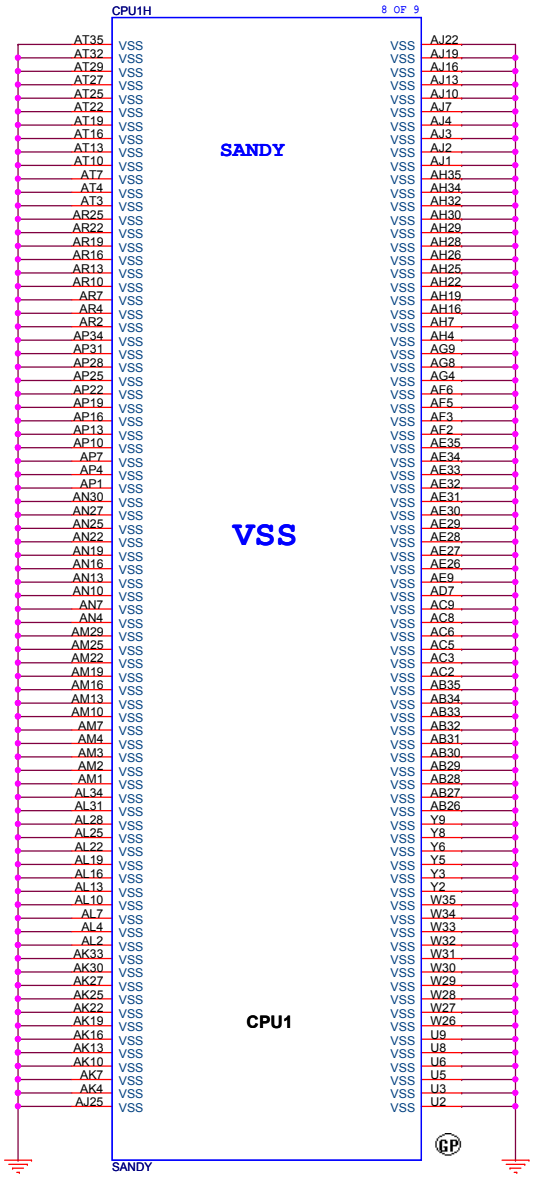
Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

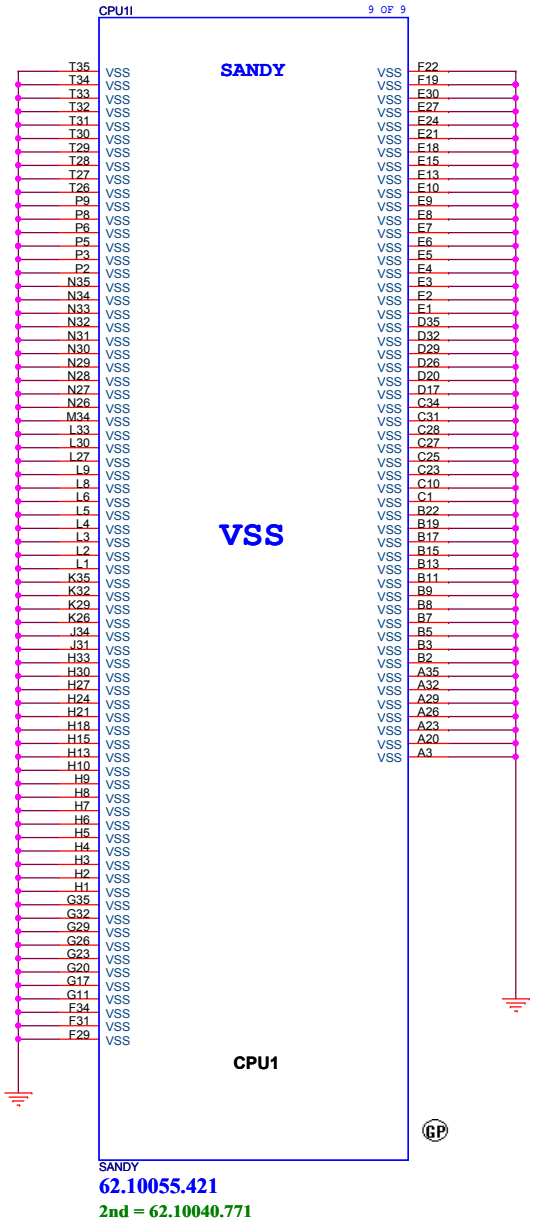
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VCC_GFXCORE)
Size: A3
Document Number: Enrico Caruso 14
Rev: A00
Date: Wednesday, April 13, 2011
Sheet 9 of 105

SSID = CPU





DN15ATI Whistler

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 10 of 105

(Blanking)

DN15ATI Whistler

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: XDP

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 11 of 105

(Blanking)

DN15ATI Whistler

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 12 of 105

(Blanking)

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Enrico Caruso 14* | Rev: *A00*

Date: Wednesday, April 13, 2011 | Sheet 13 of 105

SSID = MEMORY

DM2

DDR_VREF_S3
R1405 0R0402-PAD
M_VREF_CA_DIMM1
C1423 SCD1U10V2KX-5GP
C1425 DY SC2D2U10V3KX-1GP
C1424 SCD1U10V2KX-5GP

DDR_VREF_S3
R1404 0R0402-PAD
M_VREF_DQ_DIMM1
C1411 SCD1U10V2KX-5GP
C1412 DY SC2D2U10V3KX-1GP
C1413 SCD1U10V2KX-5GP

X02-0303 change 0R to short pad

0D75V_S0
Place these caps close to VTT1 and VTT2.
C1419 SC1U6D3V2KX-GP
C1420 SC1U6D3V2KX-GP
C1421 SC1U6D3V2KX-GP
C1422 SC1U6D3V2KX-GP
C1418 DY SC10U6D3V5KX-1GP

M_B_A[15:0] 6
M_B_BS2 6
M_B_BS0 6
M_B_BS1 6
M_B_DQ[63:0] 6

M_B_A0 98 A0
M_B_A1 97 A1
M_B_A2 96 A2
M_B_A3 95 A3
M_B_A4 92 A4
M_B_A5 91 A5
M_B_A6 90 A6
M_B_A7 86 A7
M_B_A8 89 A8
M_B_A9 85 A9
M_B_A10 107 A10/AP
M_B_A11 84 A11
M_B_A12 83 A12
M_B_A13 119 A13
M_B_A14 80 A14
M_B_A15 78 A15
79 A16/BA2
109 BA0
108 BA1

M_B_DQ0 5 DQ0
M_B_DQ1 7 DQ1
M_B_DQ2 15 DQ2
M_B_DQ3 17 DQ3
M_B_DQ4 4 DQ4
M_B_DQ5 6 DQ5
M_B_DQ6 16 DQ6
M_B_DQ7 18 DQ7
M_B_DQ8 21 DQ8
M_B_DQ9 23 DQ9
M_B_DQ10 33 DQ10
M_B_DQ11 35 DQ11
M_B_DQ12 22 DQ12
M_B_DQ13 24 DQ13
M_B_DQ14 34 DQ14
M_B_DQ15 36 DQ15
M_B_DQ16 39 DQ16
M_B_DQ17 41 DQ17
M_B_DQ18 51 DQ18
M_B_DQ19 53 DQ19
M_B_DQ20 40 DQ20
M_B_DQ21 42 DQ21
M_B_DQ22 50 DQ22
M_B_DQ23 52 DQ23
M_B_DQ24 57 DQ24
M_B_DQ25 59 DQ25
M_B_DQ26 67 DQ26
M_B_DQ27 69 DQ27
M_B_DQ28 56 DQ28
M_B_DQ29 58 DQ29
M_B_DQ30 68 DQ30
M_B_DQ31 70 DQ31
M_B_DQ32 129 DQ32
M_B_DQ33 131 DQ33
M_B_DQ34 141 DQ34
M_B_DQ35 143 DQ35
M_B_DQ36 130 DQ36
M_B_DQ37 132 DQ37
M_B_DQ38 140 DQ38
M_B_DQ39 142 DQ39
M_B_DQ40 147 DQ40
M_B_DQ41 149 DQ41
M_B_DQ42 157 DQ42
M_B_DQ43 159 DQ43
M_B_DQ44 146 DQ44
M_B_DQ45 148 DQ45
M_B_DQ46 158 DQ46
M_B_DQ47 160 DQ47
M_B_DQ48 163 DQ48
M_B_DQ49 165 DQ49
M_B_DQ50 175 DQ50
M_B_DQ51 177 DQ51
M_B_DQ52 164 DQ52
M_B_DQ53 166 DQ53
M_B_DQ54 174 DQ54
M_B_DQ55 176 DQ55
M_B_DQ56 181 DQ56
M_B_DQ57 183 DQ57
M_B_DQ58 191 DQ58
M_B_DQ59 193 DQ59
M_B_DQ60 180 DQ60
M_B_DQ61 182 DQ61
M_B_DQ62 192 DQ62
M_B_DQ63 194 DQ63

M_B_DQS#0 10 DQS0#
M_B_DQS#1 27 DQS1#
M_B_DQS#2 45 DQS2#
M_B_DQS#3 62 DQS3#
M_B_DQS#4 135 DQS4#
M_B_DQS#5 152 DQS5#
M_B_DQS#6 169 DQS6#
M_B_DQS#7 186 DQS7#

M_B_DQS0 12 DQS0
M_B_DQS1 29 DQS1
M_B_DQS2 47 DQS2
M_B_DQS3 64 DQS3
M_B_DQS4 137 DQS4
M_B_DQS5 154 DQS5
M_B_DQS6 171 DQS6
M_B_DQS7 188 DQS7

M_B_DQS#[7:0] 6
M_B_DQS[7:0] 6

6 M_B_DIM0_ODT0 116 ODT0
6 M_B_DIM0_ODT1 120 ODT1
M_VREF_CA_DIMM1 126 VREF_CA
M_VREF_DQ_DIMM1 1 VREF_DQ
15,37 DDR3_DRAMRST# 30 RESET#
0D75V_S0 203 VTT1
204 VTT2

NP1 NP2

RAS# 110 M_B_RAS# 6
WE# 113 M_B_WE# 6
CAS# 115 M_B_CAS# 6

CS0# 114 M_B_DIM0_CS#0 6
CS1# 121 M_B_DIM0_CS#1 6

CKE0 73 M_B_DIM0_CKE0 6
CKE1 74 M_B_DIM0_CKE1 6

CK0 101 M_B_DIM0_CLK_DDR0 6
CK0# 103 M_B_DIM0_CLK_DDR#0 6

CK1 102 M_B_DIM0_CLK_DDR1 6
CK1# 104 M_B_DIM0_CLK_DDR#1 6

DM0 11
DM1 28
DM2 46
DM3 63
DM4 136
DM5 153
DM6 170
DM7 187

SDA 200 PCH_SMBDATA 15,20,65
SCL 202 PCH_SMBCLK 15,20,65

EVENT# 198 TS#_DIMM0_1 15

VDDSPD 199

SA0 197 SA0_DIM1
SA1 201 SA1_DIM1

NC#1 77
NC#2 122
NC#/TEST 125

VDD1 75
VDD2 76
VDD3 81
VDD4 82
VDD5 87
VDD6 88
VDD7 93
VDD8 94
VDD9 99
VDD10 100
VDD11 105
VDD12 106
VDD13 111
VDD14 112
VDD15 117
VDD16 118
VDD17 123
VDD18 124

VSS 2 3 8 9 13 14 19 20 25 26 31 32 37 38 43 44 48 49 54 55 60 61 65 66 71 72 127 128 133 134 138 139 144 145 150 151 155 156 161 162 167 168 172 173 178 179 184 185 189 190 195 196 205 206

1D5V_S3

3D3V_S0
R1402 10KR2J-3-GP
SA1_DIM1
SA0_DIM1
R1401 10KR2J-3-GP

SWAP SA0_DM1 and SA1_DIM1 each other for DM2 can't boot up issue(only DN15/DQ15)

11/ 17 Change SMbus adress note

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4
SO-DIMMA TS Address is 0x34

C1401 SCD1U10V2KX-5GP
C1402 DY SC2D2U10V3KX-1GP

Thermal EVENT
TS#_DIMM0_1 R1403 10KR2J-3-GP 3D3V_S0

SODIMM A DECOUPLING
1D5V_S3
TC1401 DY ST330U2VDM4-GP
C1403 DY SC10U6D3V5KX-1GP
C1404 SC10U6D3V5KX-1GP
C1405 DY SC10U10V5ZY-1GP
C1406 SC10U6D3V5KX-1GP
C1407 DY SC10U6D3V5KX-1GP
C1408 DY SC10U10V5ZY-1GP
C1409 DY SC10U6D3V5KX-1GP
C1410 DY SC10U6D3V5KX-1GP

Layout Note:
Place these Caps near SO-DIMMA.
C1414 SC1U6D3V2KX-GP
C1415 SC1U10V2KX-5GP
C1416 SC1U10V2KX-5GP
C1417 SC1U6D3V2KX-GP

12/28 Yellow mark for OPI change

H =5.2mm

DDR3-204P-135-GP
62.10024.E21

12/3 Change DM2 to 62.10024.E21
12/9 Change DM2 to 62.10017.K01
12/21 Change DM2 to 62.10017.P61
12/22 Change DM2 to 62.10024.E21

DN15ATI Whistler

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR3-SODIMM2
Size: Custom
Document Number: Enrico Caruso 14
Rev: A00
Date: Wednesday, April 13, 2011
Sheet 14 of 105

SSID = MEMORY

11/ 17 Change SMbus adress note

Note:
SO-DIMMB SPD Address is 0xA0
SO-DIMMB TS Address is 0x30

SO-DIMMB is placed farther from the Processor than SO-DIMMA

DM1

M_A_A[15:0] 6

M_A_A0 98
M_A_A1 97
M_A_A2 96
M_A_A3 95
M_A_A4 92
M_A_A5 91
M_A_A6 90
M_A_A7 86
M_A_A8 89
M_A_A9 85
M_A_A10 107
M_A_A11 84
M_A_A12 83
M_A_A13 119
M_A_A14 80
M_A_A15 78

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2

6 M_A_BS2
6 M_A_BS0 109
6 M_A_BS1 108
6 M_A_DQ[63:0]

BA0 BA1

M_A_DQ0 5
M_A_DQ1 7
M_A_DQ2 15
M_A_DQ3 17
M_A_DQ4 4
M_A_DQ5 6
M_A_DQ6 16
M_A_DQ7 18
M_A_DQ8 21
M_A_DQ9 23
M_A_DQ10 33
M_A_DQ11 35
M_A_DQ12 22
M_A_DQ13 24
M_A_DQ14 34
M_A_DQ15 36
M_A_DQ16 39
M_A_DQ17 41
M_A_DQ18 51
M_A_DQ19 53
M_A_DQ20 40
M_A_DQ21 42
M_A_DQ22 50
M_A_DQ23 52
M_A_DQ24 57
M_A_DQ25 59
M_A_DQ26 67
M_A_DQ27 69
M_A_DQ28 56
M_A_DQ29 58
M_A_DQ30 68
M_A_DQ31 70
M_A_DQ32 129
M_A_DQ33 131
M_A_DQ34 141
M_A_DQ35 143
M_A_DQ36 130
M_A_DQ37 132
M_A_DQ38 140
M_A_DQ39 142
M_A_DQ40 147
M_A_DQ41 149
M_A_DQ42 157
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M_A_DQ51 177
M_A_DQ52 164
M_A_DQ53 166
M_A_DQ54 174
M_A_DQ55 176
M_A_DQ56 181
M_A_DQ57 183
M_A_DQ58 191
M_A_DQ59 193
M_A_DQ60 180
M_A_DQ61 182
M_A_DQ62 192
M_A_DQ63 194

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

M_A_DQS#0 10
M_A_DQS#1 27
M_A_DQS#2 45
M_A_DQS#3 62
M_A_DQS#4 135
M_A_DQS#5 152
M_A_DQS#6 169
M_A_DQS#7 186

DQS0# DQS1# DQS2# DQS3# DQS4# DQS5# DQS6# DQS7#

M_A_DQS0 12
M_A_DQS1 29
M_A_DQS2 47
M_A_DQS3 64
M_A_DQS4 137
M_A_DQS5 154
M_A_DQS6 171
M_A_DQS7 188

DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7

6 M_A_DIM0_ODT0 116
6 M_A_DIM0_ODT1 120

ODT0 ODT1

M_VREF_CA_DIMM0 126
M_VREF_DQ_DIMM0 1

VREF_CA VREF_DQ

14,37 DDR3_DRAMRST# 30

RESET#

0D75V_S0 203 204

VTT1 VTT2

NP1 NP2

RAS# 110 M_A_RAS# 6
WE# 113 M_A_WE# 6
CAS# 115 M_A_CAS# 6

CS0# 114 M_A_DIM0_CS#0 6
CS1# 121 M_A_DIM0_CS#1 6

CKE0 73 M_A_DIM0_CKE0 6
CKE1 74 M_A_DIM0_CKE1 6

CK0 101 M_A_DIM0_CLK_DDR0 6
CK0# 103 M_A_DIM0_CLK_DDR#0 6

CK1 102 M_A_DIM0_CLK_DDR1 6
CK1# 104 M_A_DIM0_CLK_DDR#1 6

M_A_DQS#[7:0] 6
M_A_DQS[7:0] 6

DM0 11
DM1 28
DM2 46
DM3 63
DM4 136
DM5 153
DM6 170
DM7 187

SDA 200 PCH_SMBDATA 14,20,65
SCL 202 PCH_SMBCLK 14,20,65

EVENT# 198 TS#_DIMM0_1 14

VDDSPD 199

SA0 197 SA0_DIM0
SA1 201 SA1_DIM0

NC#1 77
NC#2 122
NC#/TEST 125

VDD1 75 VDD2 76 VDD3 81 VDD4 82 VDD5 87 VDD6 88 VDD7 93 VDD8 94 VDD9 99 VDD10 100 VDD11 105 VDD12 106 VDD13 111 VDD14 112 VDD15 117 VDD16 118 VDD17 123 VDD18 124

VSS 2 3 8 9 13 14 19 20 25 26 31 32 37 38 43 44 48 49 54 55 60 61 65 66 71 72 127 128 133 134 138 139 144 145 150 151 155 156 161 162 167 168 172 173 178 179 184 185 189 190 195 196 205 206

DDR3-204P-128-GP
62.10024.D51

H =9.2mm

SA1_DIM0
SA0_DIM0

R1502 10KR2J-3-GP
R1501 10KR2J-3-GP

3D3V_S0

C1501 SCD1U10V2KX-5GP
C1502 SC2D2U10V3KX-1GP DY

1D5V_S3

DDR_VREF_S3

R1504 0R0402-PAD
M_VREF_CA_DIMM0
C1523 SCD1U10V2KX-5GP
C1524 DY SC2D2U10V3KX-1GP
C1522 SCD1U10V2KX-5GP

DDR_VREF_S3

R1503 0R0402-PAD
M_VREF_DQ_DIMM0
C1515 SCD1U10V2KX-5GP
C1516 DY SC2D2U10V3KX-1GP
C1517 SCD1U10V2KX-5GP

X02-0303 change 0R to short pad

SODIMM B DECOUPLING

12/28 Yellow mark for OPI change

1D5V_S3

C1503 DY SC10U10V5ZY-1GP
C1504 DY SC10U10V5ZY-1GP
C1505 SC10U6D3V5KX-1GP
C1506 SC10U6D3V5KX-1GP
C1507 SC10U6D3V5KX-1GP
C1508 DY SC10U10V5ZY-1GP
C1509 SC10U6D3V5KX-1GP
C1510 DY SC10U6D3V5KX-1GP

C1511 SC1U6D3V2KX-GP
C1512 SCD1U10V2KX-5GP
C1513
C1514 SCD1U10V2KX-5GP

Layout Note:
Place these Caps near SO-DIMMB.

Place these caps close to VTT1 and VTT2.

0D75V_S0

C1518 DY SC1U6D3V2KX-GP
C1519 SC1U6D3V2KX-GP
C1520 DY SC1U6D3V2KX-GP
C1521 SC1U6D3V2KX-GP

12/7 Change DM1 to 62.10024.D51
12/9 Change DM1 to 62.10017.K11
12/17 Change DM1 to 62.10017.N11
12/21 Change DM1 to 62.10017.Q41
12/22 Change DM1 to 62.10024.D91
12/22 Change DM1 to 62.10024.D51

Note:
The symbol DM1 is change value and PN only.

DN15ATI Whistler

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR3-SODIMM1**
Size: Custom
Document Number: Enrico Caruso 14
Rev: A00
Date: Wednesday, April 13, 2011
Sheet 15 of 105

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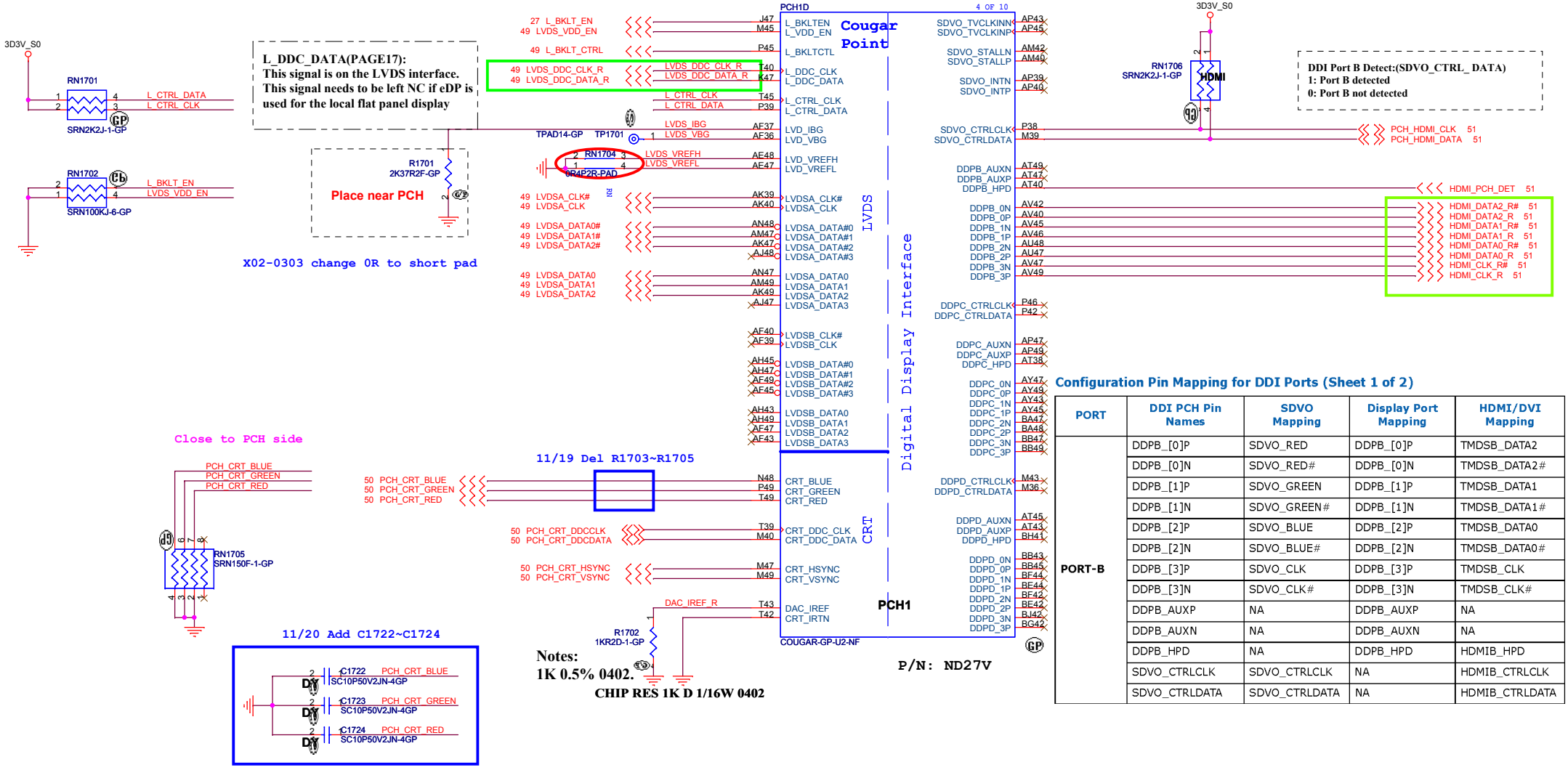
DN15ATI Whistler

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
A3	*Enrico Caruso 14*	*A00*

Date: Wednesday, April 13, 2011 Sheet 16 of 105



Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)

PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
	DDPB_HPD	NA	DDPB_HPD	HDMIB_HPD
	SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMIB_CTRLCLK
	SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMIB_CTRLDATA

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (LVDS/CRT/DDI)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 17 of 105

SSID = PCH

12/2 Net swap for layout

RN1801 SRN8K2J-2-GP-U
INT_PIRQB# 1
INT_PIRQD# 2
INT_PIRQC# 3
INT_PIRQF# 4
5
10 INT_PIRQE#
9 INT_PIRQA#
8 INT_PIRQH#
7 INT_PIRQG#
6
3D3V_S0

R1801 DY 1 4K7R2J-2-GP PCI_GNT3#

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

R1802 DY 1KR2J-1-GP BBS_BIT1
R1803 DY 1KR2J-1-GP BBS_BIT0 BBS_BIT0 21

BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI (Default)

RN1803 SRN10KJ-5-GP
DGPU_HOLD_RST# 1
DGPU_PWR_EN# 2
4
3

PCH1E Cougar Point 5 OF 10

RSVD: BG26 BJ26 BH25 BJ16 BG16 AH38 AH37 AK43 AK45 C18 N30 H3 AH12 AM4 AM5 Y13 K24 L24 AB46 AB45
NVRAM: B21 M20 AY16 BG46 BE28 BC30 BE32 BJ32 BC28 BE30 BF32 BG32 AV26 BB26 AU28 AY30 AU26 AY26 AV28 AW30
TP1 TP2 TP3 TP4 TP5 TP6 TP7 TP8 TP9 TP10 TP11 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24 TP25 TP26 TP27 TP28 TP29 TP30 TP31 TP32 TP33 TP34 TP35 TP36 TP37 TP38 TP39 TP40

RSVD: AY7 AV7 AU3 BG4 AT10 BC8 AU2 AT4 AT3 AT1 AY3 AT5 AV3 AV1 BB1 BA3 BB5 BB3 BB7 BE8 BD4 BF6 AV5 AY1 AV10 AT8 AY5 BA2 AT12 BF3
AV5 NV_ALE
AY1 NV_CLE
DF_TVS
AV10 NV_RCOMP 1 TP1803 TPAD14-GP

USB Ext. port 1 (HS)
External debug port use on Huron river platform

USB: C24 A24 C25 B25 C26 A26 K28 H28 E28 D28 C28 A28 C29 B29 N28 M28 L30 K30 G30 E30 C30 A30 L32 K32 G32 E32 C32 A32 C33 B33 A14 K20 B17 C16 L16 A16 D14 C14
USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P USBP12N USBP12P USBP13N USBP13P
USB_PN1 61
USB_PP1 61
USB_PN5 32
USB_PP5 32
USB_PN8 82
USB_PP8 82
USB_PN9 82
USB_PP9 82
USB_PN11 65
USB_PP11 65
USB_PN12 49
USB_PP12 49
USBRBIAS# USB_RBIAS
USBRBIAS
R1811 22D6R2F-L1-GP
OC0#/GPIO59 OC1#/GPIO40 OC2#/GPIO41 OC3#/GPIO42 OC4#/GPIO43 OC5#/GPIO9 OC6#/GPIO10 OC7#/GPIO14
USB_OC#0_1
USB_OC#2_3
USB_OC#4_5
USB_OC#6_7
USB_OC#8_9
USB_OC#10_11
USB_OC#12_13
PCH_GPIO14
USB_OC#0_1 61
USB_OC#8_9 61

PCI: A42 G40 C42 D44 K10 C6 K40 K38 H38 G38 C46 C44 E40 D47 E42 F46
PIRQE#/GPIO2 PIRQF#/GPIO3 PIRQG#/GPIO4 PIRQH#/GPIO5 PME# PLTRST# PIRQA# PIRQB# PIRQC# PIRQD# REQ1#/GPIO50 REQ2#/GPIO52 REQ3#/GPIO54 GNT1#/GPIO51 GNT2#/GPIO53 GNT3#/GPIO55

3D3V_S0
R1814 8K2R2J-3-GP
INT_PIRQA#
INT_PIRQB#
INT_PIRQC#
INT_PIRQD#
83 DGPU_HOLD_RST# TPAD14-GP TP1807
93 DGPU_PWR_EN#
DGPU_SELECT#
DGPU_PWR_EN#
TPAD14-GP TP1806 PCH_GPIO53
TPAD14-GP TP1801 PCI_GNT3#
BBS_BIT1
56 SATA_ODD_DA# R1813 0R0402-PAD
INT_PIRQE#
INT_PIRQF#
INT_PIRQG#
INT_PIRQH#
TPAD14-GP TP1802 PCI_PME#
PCI_PLTRST#

X02-0311 dummy R1804

71 CLK_PCI_LPC
20 CLK_PCI_FB
27 CLK_PCI_KBC
R1804 DY 22R2J-2-GP CLK_PCI_LPC_R H49
R1805 22R2J-2-GP CLK_PCI_FB_R H43
R1806 22R2J-2-GP CLK_PCI_KBC_R J48
CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4 K42 H40

EC1802 DY SC4D7P50V2CN-1GP
EC1801 DY SC33P50V2JN-3GP
EC1803 DY SC33P50V2JN-3GP

KBC CLK EMI

PCH1
COUGAR-GP-U2-NF
P/N: ND27V

OC[3:0]# for Device 29 (Ports 0-7)
OC[7:4]# for Device 26 (Ports 8-13)

X02-0303 change 0R to short pad

5,27,31,65,71,83 PLT_RST#
R1807 0R0402-PAD
PCI_PLTRST#
R1816 DY 100KR2J-GP
C1801 DY SC220P50V2KX-3GP

12/1 Swap net for layout
11/11 change to RN1802 to meet schematic check result.

RN1802 SRN8K2J-2-GP-U
PCH_GPIO14 1
USB_OC#6_7 2
USB_OC#10_11 3
USB_OC#4_5 4
5
3D3V_S5
10
9 USB_OC#0_1
8 USB_OC#12_13
7 USB_OC#8_9
6 USB_OC#2_3
3D3V_S5

1D8V_S0
R1808 2K2R2J-2-GP
R1809 1KR2J-1-GP
NV_CLE 1
H_SNB_IVB# 5

DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

1D8V_S0
R1810 1KR2J-1-GP DY
NV_ALE

Danbury Technology: Disabled when Low. Enable when High.

USB Table

Pair	Device
0	X
1	USB Ext. port 2 (MB)
2	X
3	X
4	X
5	CARD READER
6	X
7	X
8	USB Ext. port 3
9	USB Ext. port 1
10	X
11	Mini Card1 (WLAN+BT)
12	CAMERA
13	X

USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

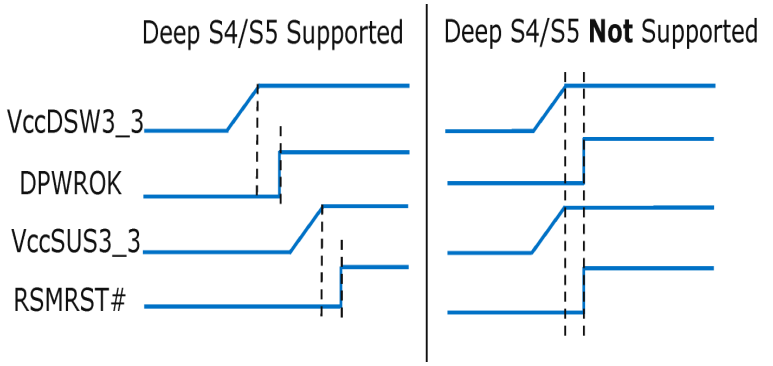
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI/USB/NVRAM)
Size: A3
Document Number: Enrico Caruso 14
Rev: A00
Date: Wednesday, April 13, 2011
Sheet 18 of 105

SSID = PCH

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and routing length less than 500 mils.
DMI_IRCOMP keep W=4 mils and routing length less than 500 mils.



For platforms not supporting Deep S4/S5
1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
2.DPWROK and RSMRST# will rise at the same time (connected on board)
3.SLP_SUS# and SUSACK# are left as "no connect"
4.SUSWARN# used as SUSPWRDNACK/GPIO30

PCH1C — 3 OF 10 — Cougar Point — DMI — FDI — System Power Management

X02-0303 change 0R to short pad

S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

12/2 Swap net for layout

PCIE_WAKE#
CRB : 1K
CEKLT: 10K

P/N: ND27V

<Core Design>

Wistron Corporation
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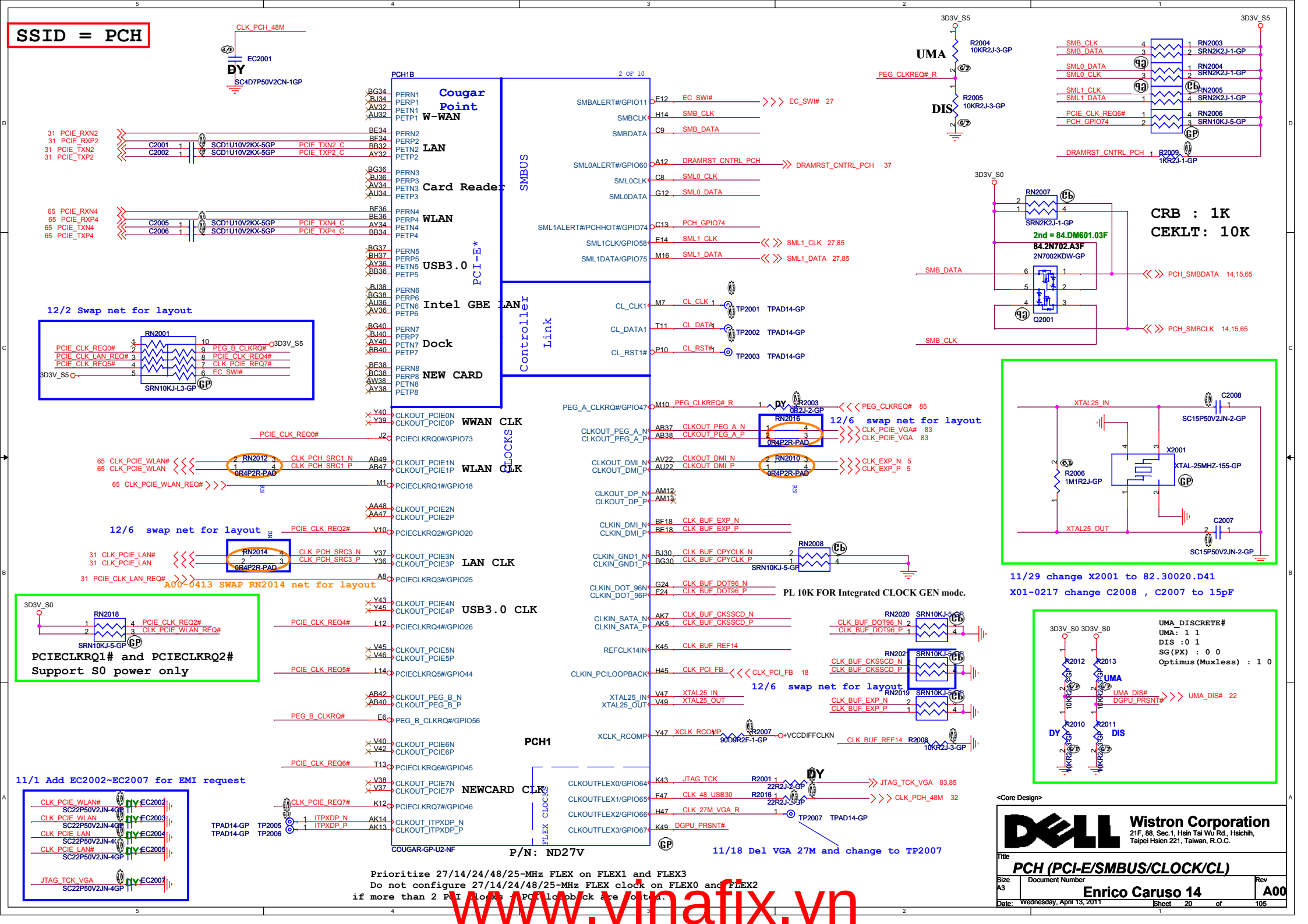
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (DM I/FDI/PM)
Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00
Date: Wednesday, April 13, 2011 | Sheet 19 of 105

SSID = PCH



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (PCI-E/SMBUS/CLOCK/CL)

Size	Document Number	Rev
A3	Enrico Caruso 14	A00

Date: Wednesday, April 13, 2011 Sheet 20 of 105

SSID = PCH

X01-0210 Merge R2115 R2116

X01-0208 Add RN2101, R2127 for LPC EA result
X01-0210 change RN2101 to RN2104 RN2105

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

82.30001.A81
2nd = 82.30001.691
3rd = 82.30001.861

Notes:
ME_UNLOCK (HDA_SDO) connect to EC.
Make sure EC drive this pin "low" all the time.

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

NO REBOOT STRAP

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

This signal has a weak internal pull down.
On Die PLL VR is supplied by 1.5V when
sampled high, 1.8 V when sampled low.
Needs to be pulled High for Huron River platform.
co-operate with R2310

PLL ODVR VOLTAGE	
HDA_SYNC	Low = 1.8V (Default) High = 1.5V

HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

11/1 Add R2111 for EMI request

11/ 17 change R2111 from 33ohm to 0ohm and change to ER2111

11/2 Merge R2122 into Q2101

12/6 Separate RN2103 to R2125 and R2126

11/11Remove RN2104 and FP_DET#

HDD1

ODD

P/N: ND27V

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (SPI/RTC/LPC/SATA/IHDA)
Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00
Date: Wednesday, April 13, 2011 | Sheet 21 of 105

SSID = PCH

Note:
For PCH debug with XDP, need to DUMMY R2218

PCH1F — 6 OF 10 — Cougar Point

GPIO / CPU/MISC / NCTF

BMBUSY#/GPIO0	T7	TACH4/GPIO68	C40
TACH1/GPIO1	A42	TACH5/GPIO69	B41
TACH2/GPIO6	H36	TACH6/GPIO70	C41
TACH3/GPIO7	E38	TACH7/GPIO71	A40
GPIO8	C10		
LAN_PHY_PWR_CTRL/GPIO12	C4		
GPIO15	G2	A20GATE	P4
SATA4GP/GPIO16	U2	PECI	AU16
TACH0/GPIO17	D40	RCIN#	P5
SCLOCK/GPIO22	T5	PROCPWRGD	AY11
GPIO24/MEM_LED	E8	THRMTRIP#	AY10
GPIO27	E16	INIT3_3V#	T14
GPIO28	P8		
STP_PCI#/GPIO34	K1	TS_VSS1	AH8
GPIO35	K4	TS_VSS2	AK11
SATA2GP/GPIO36	V8	TS_VSS3	AH10
SATA3GP/GPIO37	M5	TS_VSS4	AK10
SLOAD/GPIO38	N2	NC_1	P37
SDATAOUT0/GPIO39	M3		
SDATAOUT1/GPIO48	V13	NCTF_VSS#BG2	BG2
SATA5GP/GPIO49	V3	NCTF_VSS#BG48	BG48
GPIO57	D6	NCTF_VSS#BH3	BH3
		NCTF_VSS#BH47	BH47
NCTF_VSS#A4	A4	NCTF_VSS#BJ4	BJ4
NCTF_VSS#A44	A44	NCTF_VSS#BJ44	BJ44
NCTF_VSS#A45	A45	NCTF_VSS#BJ45	BJ45
NCTF_VSS#A46	A46	NCTF_VSS#BJ46	BJ46
NCTF_VSS#A5	A5	NCTF_VSS#BJ5	BJ5
NCTF_VSS#A6	A6	NCTF_VSS#BJ6	BJ6
NCTF_VSS#B3	B3	NCTF_VSS#C2	C2
NCTF_VSS#B47	B47	NCTF_VSS#C48	C48
NCTF_VSS#BD1	BD1	NCTF_VSS#D1	D1
NCTF_VSS#BD49	BD49	NCTF_VSS#D49	D49
NCTF_VSS#BE1	BE1	NCTF_VSS#E1	E1
NCTF_VSS#BE49	BE49	NCTF_VSS#E49	E49
NCTF_VSS#BF1	BF1	NCTF_VSS#F1	F1
NCTF_VSS#BF49	BF49	NCTF_VSS#F49	F49

NCTF TEST PIN: A4,A44,A45,A46,A5,A6,B3,B47,BD1,BD49,BE1,BE49,BF1,BF49 / BG2,BG48,BH3,BH47,BJ4,BJ44,BJ45,BJ46,BJ5,BJ6,C2,C48 / D1,D49,E1,E49,F1,F49

COUGAR-GP-U2-NF

PCH1

P/N: ND27V

3D3V_S0 — R2202 100KR2J-1-GP — SATA_ODD_PRSNT#

3D3V_S0 — RN2203 SRN10KJ-5-GP — H_A20GATE, H_RCIN#

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator, should not place external pull down.

11/11 Remove R2220 for GPIO48 set to GPO

X02-0303 change 0R to short pad

21 S_GPIO — R2218 100R2J-2-GP — PCH_GPIO0

27 EC_SMI#

DGPU_HPD_INTR#

EC_SCI#

TPAD14-GP TP2219

ICC_EN#

60 RTC_SENSE#

PCH_GPIO15

56 SATA_ODD_PRSNT# — R2213 0R0402-PAD — PCH_GPIO16

86,92,93 DGPU_PWROK

TPAD14-GP TP2210 — PCH_GPIO22

TPAD14-GP TP2212 — PCH_GPIO24

TPAD14-GP TP2203 — PCH_GPIO27

PLL_ODVR_EN

21 PSW_CLR# — TPAD14-GP TP2213 — PCH_GPIO35

GAP-OPEN G2201

DMI_OVRVLTG

FDI_OVRVLTG

MFG_MODE

TPAD14-GP TP22 — GFX_CRB_DET

TPAD14-GP TP2214 — PCH_GPIO48

PCH_TEMP_ALERT#

TPAD14-GP TP2206 — PCH_NCTF_1

TPAD14-GP TP2207 — PCH_NCTF_2

TPAD14-GP TP2208 — PCH_NCTF_3

TPAD14-GP TP2209 — PCH_NCTF_4

3D3V_S0 — PCH_TEMP_ALERT# R2222 10KR2J-3-GP; MFG_MODE R2223 10KR2J-3-GP; RN2201 SRN10KJ-6-GP: DGPU_HPD_INTR#, EC_SCI#, EC_SMI#

11/11Remove DBC_EN
X01-0211 swap DGPU_HPD_INTR#, EC_SMI# for layout.

12/1 Add R2224 pull high — 3D3V_S5 — RTC_SENSE# R2224 10KR2J-3-GP; PCH_GPIO15 R2201 1KR2J-1-GP DY

11/15 Remove Rn2204

11/ 17 Dummy R2201 because GPIO15 internal PH

C40 SATA_ODD_PWRGT 56

B41 UMA_DIS# — UMA_DIS# 20

C41 PCH_GPIO70 — TP2204 TPAD14-GP

A40 PCH_GPIO71 — TP2205 TPAD14-GP

P4 H_A20GATE 27

AU16 H_PECI_R — R2203 0R2J-2-GP DY — H_PECI 5,27

P5 H_RCIN# 27

AY11 H_CPUPWRGD 5,36

AY10 PCH_THERMTRIP_R — R2204 390R2J-1-GP — H_THERMTRIP# 5,36,85

T14 INIT3_3V# — TP2201 TPAD14-GP

AK10 TS_VSS — R2219 0R0402-PAD

TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4 should not float on the motherboard. They should be tied to GND directly.

3D3V_S0 — R2207 10KR2J-3-GP DY — FDI_OVRVLTG — R2208 10KR2J-3-GP

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

3D3V_S0 — R2209 10KR2J-3-GP DY — DMI_OVRVLTG — R2210 10KR2J-3-GP

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY)- DISABLED [DEFAULT]
	LOW (R2211)- ENABLED

ICC_EN#1 — R2211 1KR2J-1-GP

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

PLL ON DIE VR ENABLE
NOTE:This signal has a weak internal pull-up 20K ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT DISABLED -- LOW (R2212 STUFFED)

PLL_ODVR_EN DY 1 R2212 1KR2J-1-GP

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

Size	Document Number	Rev
A3	Enrico Caruso 14	A00

Date: Wednesday, April 13, 2011 Sheet 22 of 105

SSID = PCH 6A

11/ 17 Add R2301 but dummy it
and change L2301 source to 3D3V_DAC_S0

POWER

PCH1G

7 OF 10

Cougar Point

1.3A(Total current of VCCCORE)

11/18 change capacity to 0603 package

2.925A(Total current of VCCIO)

12/28 Yellow mark for OPI change

0.266A (Totally VCC3_3 current)

0.159A(Totally current of VCCVRM)

0.042A (Totally current of VCCDMI)

VCCVRM(Internal PLL and VRMs):
A.1.5V for Mobile
B.1.8 V for Desktop

11/2 change
R2304, R2305 to 0ohm

X02-0303
change 0R to short pad

11/18 change capacity to 0603 package

X02-0303
change 0R to short pad

COUGAR-GP-U2-NF

P/N: ND27V

Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

Refer to NPCE795 shared SPI flash architecture

(**) - When the control signal is low, the switch is "on".

11/3 Add LDO for CRT DAC power

11/ 17change U2301 Vout power rail and stuff the circuit

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (POWER1)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 23 of 105

SSID = PCH

POWER

Cougar Point

PCH1J

10 OF 10

USB

Clock and Miscellaneous

PCI/GPIO/LPC

SATA

MISC

CPU

PCH1

RTC

HDA

COUGAR-GP-U2-NF

P/N: ND27V

11/18 change capacity to 0603 package

12/28 Yellow mark for OPI change

11/ 17 Change R2406 from close gap to 0ohm

11/ 17 Change R2409 from close gap to 0ohm

X02-0303 change 0R to short pad

0.002A

0.097A (Totally current of VCCSUS3_3)

1.01A (Total current of VCCASW)

0.16A (Totally current of VCCVRM)

0.08A

0.08A

0.055A

0.095A

0.001A

0.001A

0.001A

0.001A

6uA

0.01A

2nd = 83.R2004.B8F

Voltage Rail	Voltage	Iccmax
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC3	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.1	0.042
VccIO3	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW3_3	3.3	0.002
VccDFTERM	1.8	0.19
VccRTC	3.3	6u
VccSus3_3	3.3	0.097
VccSusHDA	3.3	0.01
VccVRM	1.5	0.16
VccClkDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS3	1.8	0.06

<Core Design>

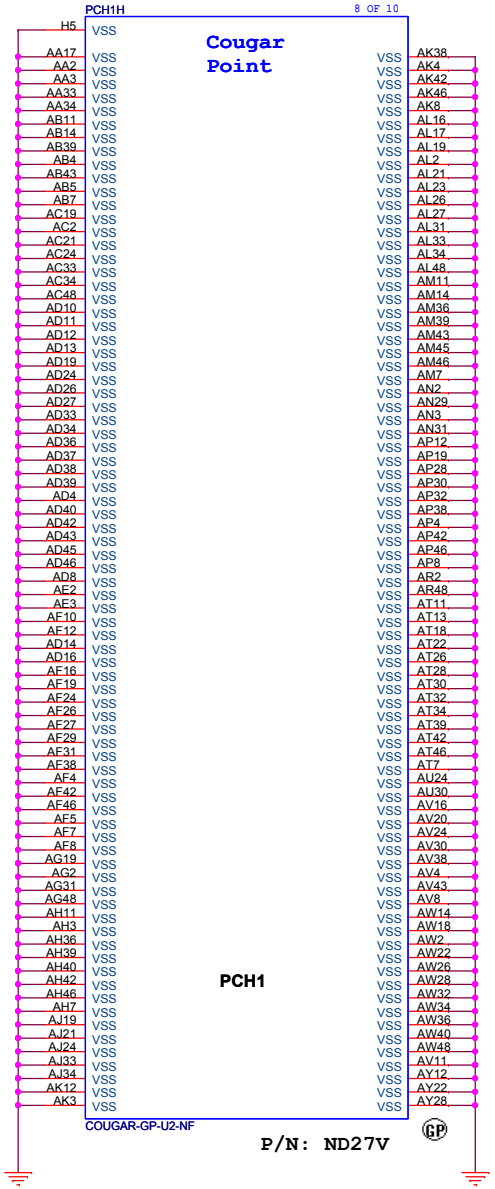
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

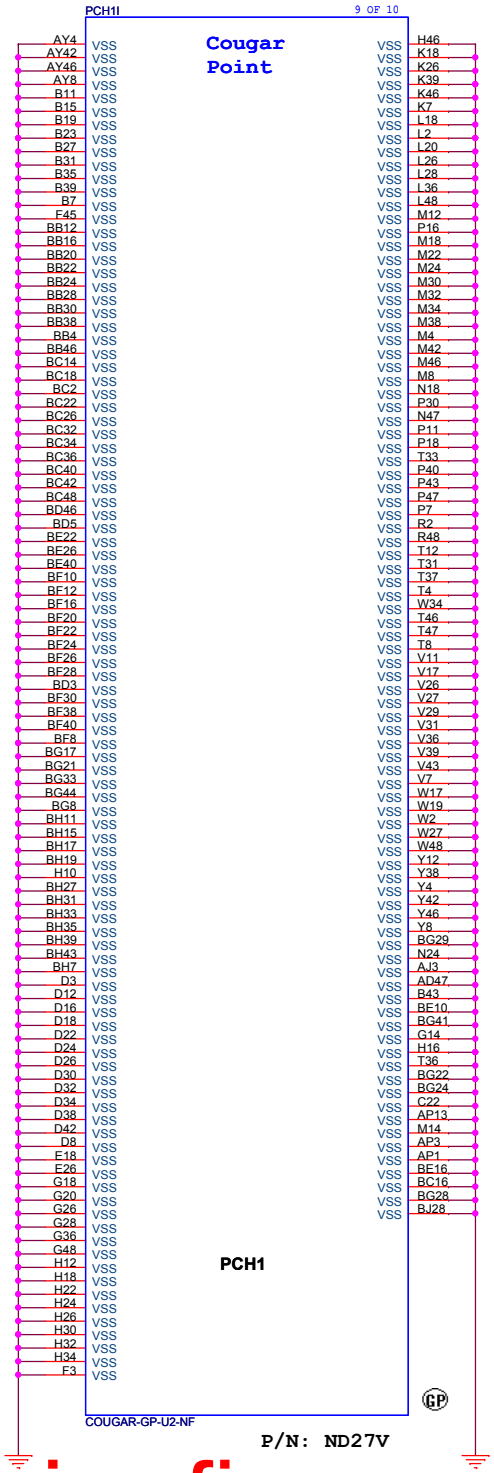
Title: PCH (POWER2)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 24 of 105

SSID = PCH





DN15ATI Whistler

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *PCH (VSS)*

Size	Document Number	Rev
A3	Enrico Caruso 14	A00

Date: Wednesday, April 13, 2011 Sheet 25 of 105

(Blanking)

DN15ATI Whistler

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 26 of 105

SSID = KBC

11/ 17 change R2702 from close gap to 0ohm
X02-0303 change 0R to short pad

11/17 change R2724 to meet X00 PCB ver
X01-0210 change R2724 to meet X01 PCB ver
X02-0314 change R2724 to meet X02 PCB ver

Reserved 0.1uF on all of ADC input pins
base on NUVOTON feedback list.(C2717~C2721)

A00-0413 change R2724 to 47K for PCB ver

A00-0328
change R2735 to 10R
and C2711 to 220p

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
A00	100.0K	47.0K	2.24V
Reserved	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

11/2 Add MODEL_ID_DET pin
for Vostro & Inspron select

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
Reserved	100.0K	10.0K(64.10025.6DL)	3.0V
Reserved	100.0K	20.0K(64.20025.6DL)	2.75V
DV15_UMA with HDMI	100.0K	33.0K	2.48V
DV15_UMA without HDMI	100.0K	47.0K(64.47025.6DL)	2.24V
DV14_UMA with HDMI	100.0K	64.9K(64.64925.6DL)	2.0V
DV14_UMA without HDMI	100.0K	76.8K(64.76825.6DL)	1.87V
DV14_DIS(512M) with HDMI	100.0K	100.0K(64.10035.6DL)	1.65V
DV14_DIS(512M) without HDMI	100.0K	143.0K(64.14335.L0L)	1.358V
DV14_DIS(1G) with HDMI	100.0K	174.0K(74.17435.6DL)	1.204V
DV14_DIS(1G) without HDMI	100.0K	215.0K(64.21535.6DL)	1.048V

11/16 Add R2728 R2729
for SERIES_ID

NOTES:
The NPCE795P GPIO/PWM outputs that are connected to LEDs have high drive buffers (20mA) and can be connected directly to the LEDs.

11/19 add TP2701 for KBC_GPIO10

Follow DQ15 change PCIE_RST#
to AD_IA_HW2

<------ TP

<------ BATTERY / CHARGER

<------PCH / eDP

11/22 change WLAN LED control to KBC

X02-0309 change 0R to short pad

11/22 add RTC_AUX_S5 to KBC_GPIO72

X01-0127 Del R2757 to follow
standard 10mw circuit

Very close to EC

11/1 Add R2777, C2777 for EMI

11/ 17 add R2774 pull high for LID_CLOSE#

NOTE:
Locate resistors R2736,R2719 and R2722 close to the NPCE795P.

NOTE:
Connect GND and AGND planes via either 0R resistor or one point layout connection.

Notes:
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

11/16 Add R2776 for aviod kbc code error

11/ 17 DY D2705 to meet DN13 result

12/10 Add R2762 and dummy R2732, Q2702

EC_GPIO47 High Active

PSL SOLUTION

10mW SOLUTION

11/ 17 DY R2734 and stuff R2756 to keep KBC data

VBACKUP

PSL_IN1

X01-0208 dummy R2769

PSL_OUT

12/22 swap net for layout

12/6 swap net for layout

EC GPIO standard PH/PL

NOTES:
Please make sure there's no pull-down resistor on USB_PWR_EN#,AC_PRESENT,E51_TXD.

ROSA Multi GPIO setting

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KBC Nuvoton NPCE795

Size: A2 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 27 of 105

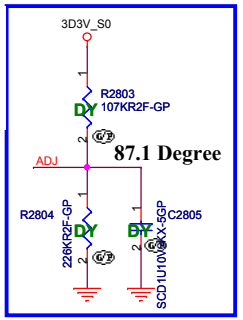
SSID = Thermal

Thermal sensor P2800

Option 1: OTZ=95°C → ADJ=3.3V

Option 2: OTZ=85°C → ADJ=Floating

Option 3: OTZ=90°C → ADJ=GND



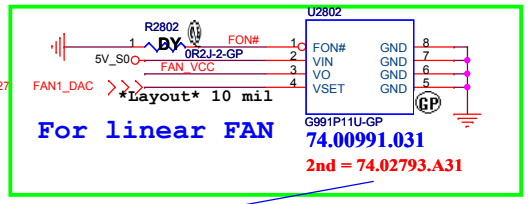
12/14 dummy R2803, R2804 and C2805

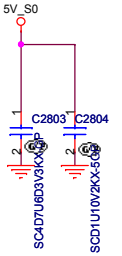
Very close to CPU1

2.System Sensor, Put on palm rest

	Pin-1	Definition
P2793A	/FON	Low(<0.4V): VOUT =Vin and the fan is fully-on High(>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm
P2793B	EN	Low (<0.4): IC is shutdown. High(>1.6V): VOUT=1.6*VSET This pin is internal Pull-High with ~500K ohm

Fan controller P2793



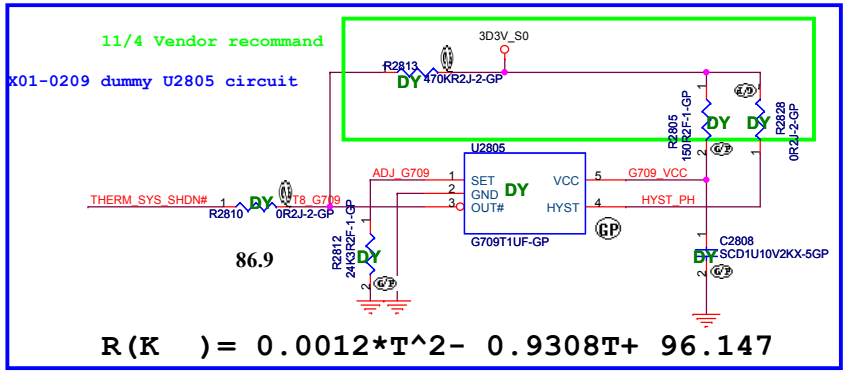


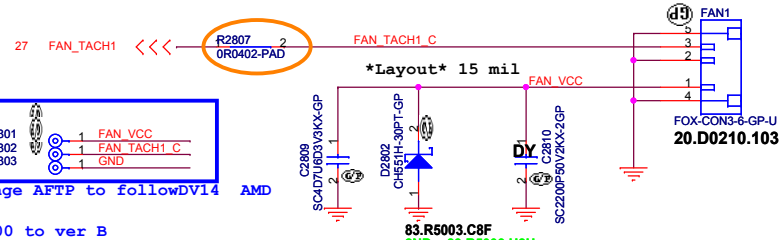
Very close to CPU1

12/15 Remove 3rd source

11/4 Vendor recommand

X01-0209 dummy U2805 circuit

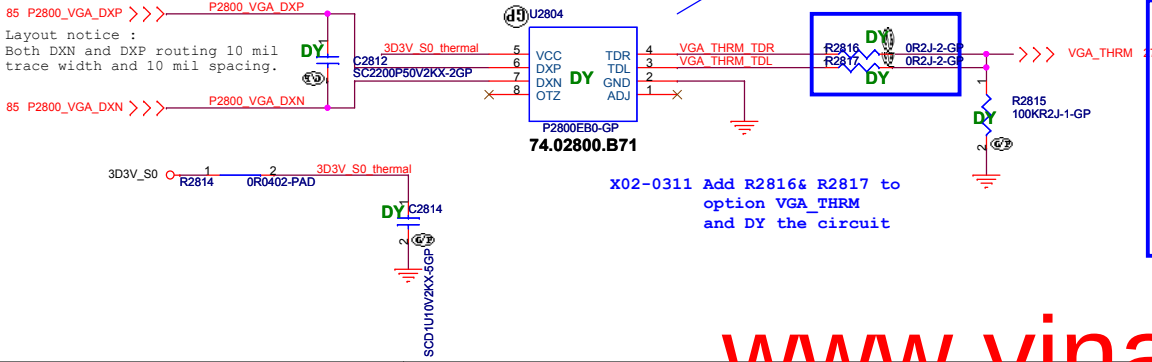




X02-0309 change AFTP to followDV14 AMD

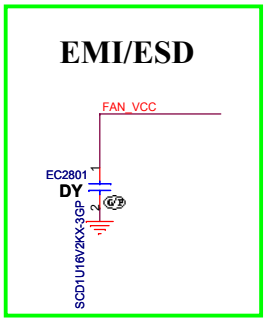
12/13 change P2800 to ver B

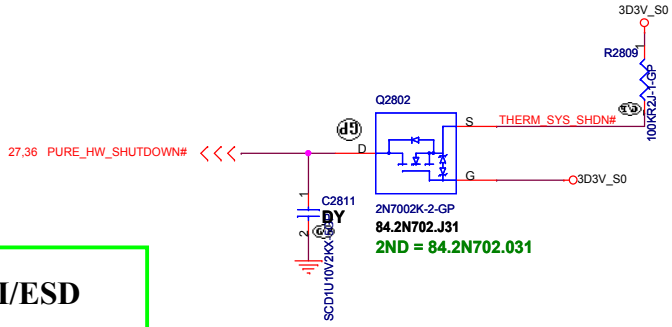
VGA Thermal sensor P2800



11/18 remove R2817, R2818, C2816
and NC U2804 OTZ pin

X02-0311 Add R2816& R2817 to
option VGA_THRM
and DY the circuit





<Core Design>

Wistron Corporation
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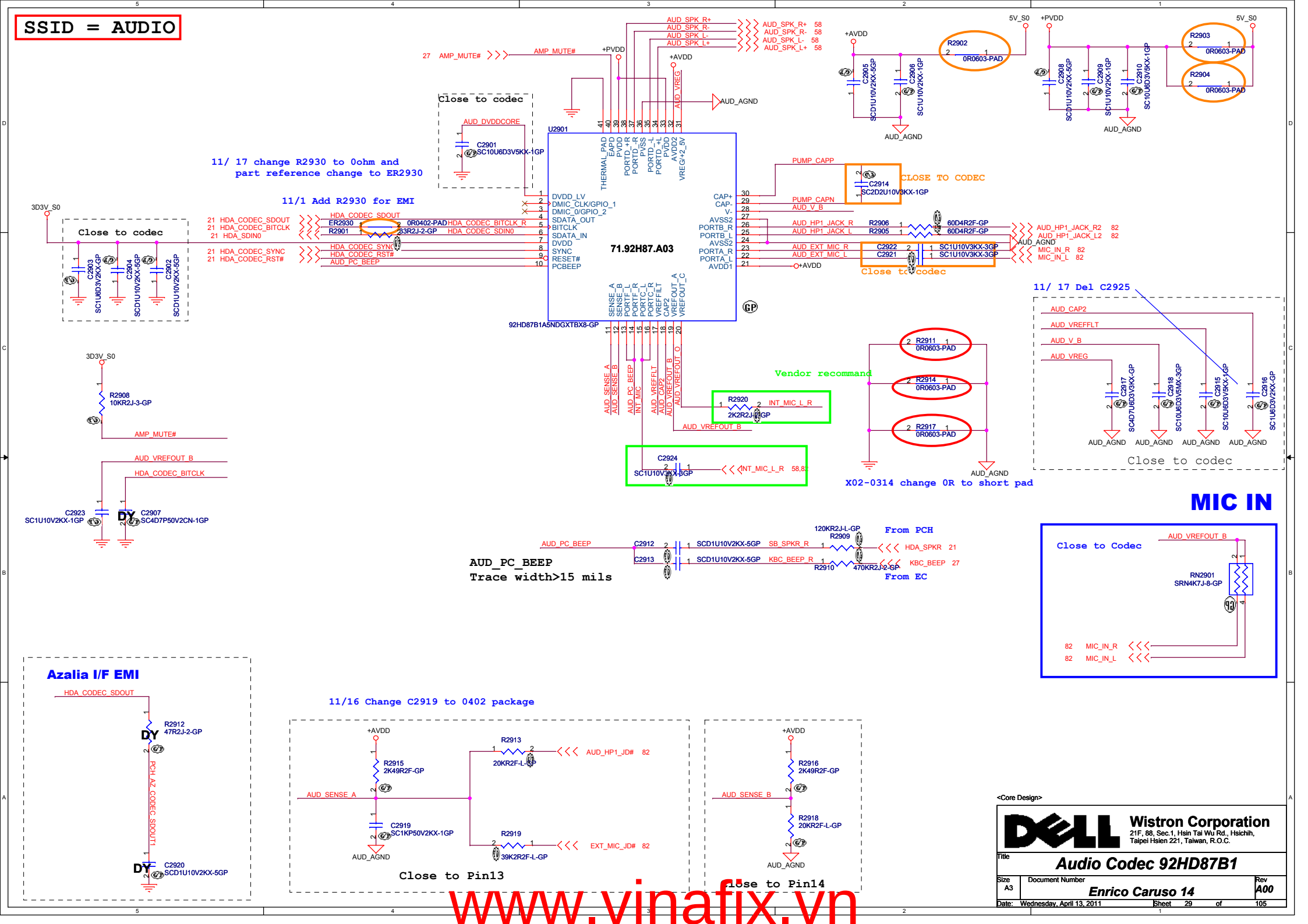
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal P2800/Fan Controllor P2793

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 28 of 105

SSID = AUDIO



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DN15ATI Whistler

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 30 of 105

LAN CHIP

11/18 change L3101 to slime type

60 mils

L3101 IND-4D7UH-192-GP

LANOUP_1.05S

CTRL10A_R

R3117 0R0603-PAD

R3115 0R0603-PAD

EVDD10

C3106 SC1U10V3ZY-6GP

C3120 SCD1U16V2ZY-2GP

C3115 SC4D7U6D3V3KX-GP

X5R

C3113 C3109 C3114 C3117 C3112 C3123 C3116 SCD1U16V2ZY-2GP

GIGA

DVDD10

3D3V_LAN_S5

40 mils

C3118 C3121 C3119 SCD1U16V2ZY-2GP

AVDD33_REG

R3104 0R0603-PAD

C3101 SC4D7U6D3V3KX-GP

C3111 SCD1U16V2ZY-2GP

X5R

X02-0303 change 0R to short pad

3D3V_LAN_S5

RN3103 SRN10KJ-5-GP

Q3104_B

Q3104 PMBS3904-1-GP

LAN_RST#

R3130 DY 0R2J-2-GP

PLT_RST# 5,16,27,65,71,83

X02-0311 add circuit to provent leakage.

X02-0314 SWAP net

3D3V_S0

3D3V_LAN_S5

R3119 DY 0R3J-0-U-GP

R3120 DY 0R3J-0-U-GP

3D3V_S5

PA102FMG-GP-U Q3103

main: 84.00102.031

2nd: 84.03403.031

C3130 SCD1U10V2KX-4GP

R3121 10KR2J-3-GP

C3122 SC1U6D3V2KX-GP

R3118 20KR2F-L-GP

PM_LAN_ENABLE_R

DY C3125 SC1U10V2KX-1GP

C3129 SCD1U10V2KX-5GP

C3126 SCD1U10V2KX-4GP

GIGA

C3128 SCD1U10V2KX-5GP

11/19 add R3131 for KBC code test

R3131 0R2J-2-GP DY

Q3102

27 PM_LAN_ENABLE

LAN_ENABLE_R_C

2N7002K-2-GP

A00-0320

Change R3118 for LOM power sequence

X01-0211 add C3122 for soft-sart

3D3V_LAN_S5

X01-0127 change Q3101 base power rail for leakage issue.

R3102 10KR2J-3-GP DY

R3101 10KR2J-3-GP DY

Q3101_B

CLK_LAN_REQ#_R

Q3101 PMBS3904-1-GP

PCIE_CLK_LAN_REQ# 20

R3108 DY 0R2J-2-GP

R3123 DY 10KR2J-3-GP

11/2 change LAN_REQ# circuit to prevent leakage.

X02-0302 Dummy PCIE_CLK_LAN_REQ# circuit

For Switch Regulator enable

R3105 0R0402-PAD

R3106 0R2J-2-GP DY

R3113 2K49R2F-GP

LAN_RSET

U3101

LAN

RTL8111E-VB-GR-GP

LANOUP_1.05S

ENSWREG

EEDI/SDA

LAN_EECS

PCIE_WAKE# 27

ISOLATE#

LAN_RST#

R3107 10KR2J-3-GP

R3110 1KR2J-1-GP

R3109 15KR2F-GP

3D3V_S0

TPAD14-GP TP3101

SMBDATA_LAN

CLK_LAN_REQ#_R

PCIE_TXP2

PCIE_TXN2

CLK_PCIE_LAN

CLK_PCIE_LAN#

PCIE_RXP2_C

PCIE_RXN2_C

C3131 SCD1U10V2KX-5GP

PCIE_WAKE# 10KR2J-3-GP DY R3122

LANXOUT

C3102 SC15P50V2JN-2-GP

X3101 XTAL-25MHZ-155-GP

82.30020.D41

LANXIN

C3103 SC15P50V2JN-2-GP

11/29 change X3101 to 82.30020.D41

X01-0217 change C3102, C3103 to 15pF

C3105 SCD1U10V2KX-5GP

C3104 SCD1U10V2KX-5GP

PCIE_RXP2 20

PCIE_RXN2 20

PCIE_TXP2 20

PCIE_TXN2 20

CLK_PCIE_LAN 20

CLK_PCIE_LAN# 20

R3116 GIGA 10KR2J-3-GP SMBDATA_LAN

R3103 GIGA 1KR2J-1-GP GPO

R3114 10KR2J-3-GP EEDI/SDA

DN15ATI Whistler

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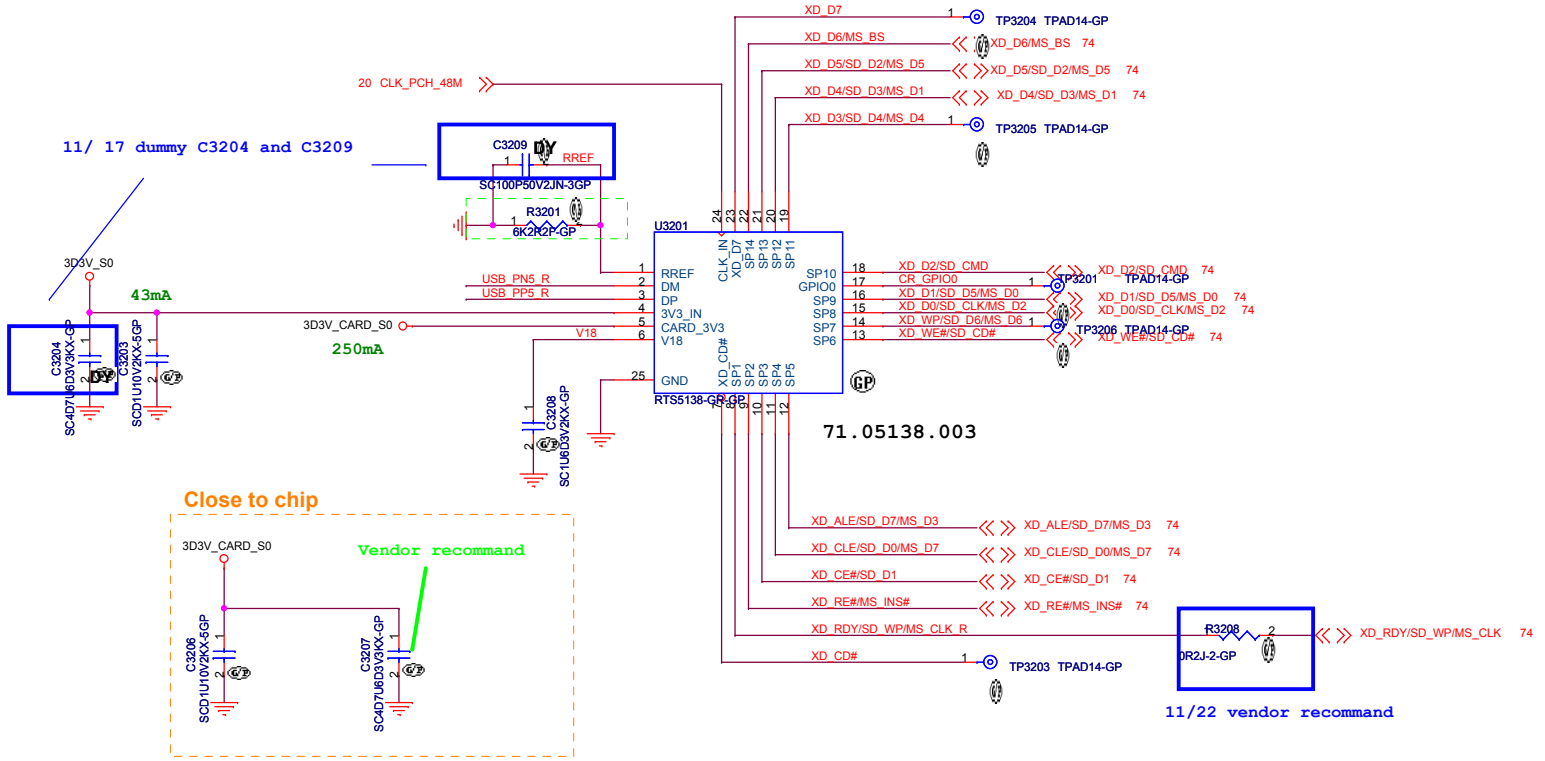
Title: Reserved

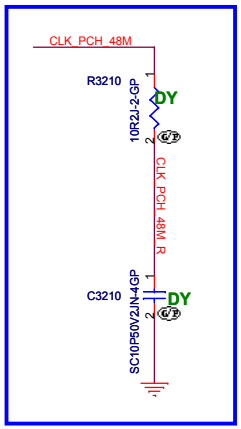
Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

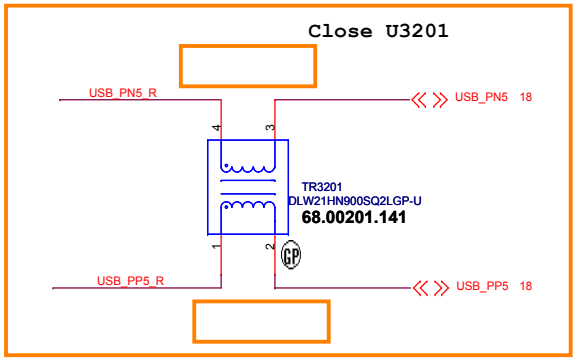
Date: Wednesday, April 13, 2011 | Sheet 31 of 105

SSID = SDIO



11/1 Add R3210, C3210 for EMI





X02-0311 stuff TR3201 and change symbol to 68.00201.141

A00-0324 change TR6102 to TR3201

A00-0406 remove R3206, R3207 PAD

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Card Reader-RTS5138

Size	Document Number	Rev
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Title: Reserved

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 33 of 105

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Title: Reserved

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Date: Wednesday, April 13, 2011 | Sheet 34 of 105

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DN15ATI Whistler

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Title: Reserved

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 35 of 105

SSID = Reset.Suspend

20101206 X02:
Add Q3603 for RTC power sequence.

27,42 IMVP_PWRGD >>> R3614 0R0402-PAD SYS_PWROK

PS_S3CNTRL Q3603 2N7002K-2-GP

C3612 SCD01U50V2KX-1GP DY

X02-0303 change 0R to short pad

12/16 Add Q3603 to meet RTC sequence as DN13

Power Sequence

19,27 S0_PWR_GOOD >>> D3602 BAS16-6-GP DY SYS_PWROK 19

83.00016.K11
2ND = 83.00016.F11

1D05V_VTT R3622 56R2J-4-GP H_THERMTRIP# 5,22,85

5,22 H_CPUPWRGD >>> R3601 1KR2J-1-GP DY H_PWRGD_R

Q3601 CHT2222APT-GP

C3602 SCD01U50V2KX-1GP DY

2ND = 83.00016.F11
83.00016.K11
BAS16-6-GP

PURE_HW_SHUTDOWN# 27,28

41 3V_5V_EN <<< D3601 R3603 1KR2J-1GP S5_ENABLE 27

R3602 200KR2J-L1-GP DY

ROSA Run Power

15V_S5 R3604 100KR2J-1-GP

AO4468 MAX 9A
Rds(on) = 18.5mOhm
2nd = 84.08882.037

5V_S5 84.04468.037 AO4468-GP U3601 5V_S0

C3603 SC10U10V5ZY-1GP

C3608 SCD01U50V2KX-1GP

R3605 10KR2J-3-GP 5V_RUN_ENABLE

5V_S0

+5V_RUN Comsumption
Peak current 7.73A

3D3V_AUX_S5

R3606 100KR2J-1-GP PS_S3CNTRL

PS_S3CNTRL 37

Q3602 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F

19,27,37,47 PM_SLP_S3#

RUN_ENABLE

Rds(on) = 18.5mOhm
AO4468 MAX 11.6A
2nd = 84.08882.037

3D3V_S5 84.04468.037 AO4468-GP U3602 3D3V_S0

C3604 SC10U6D3V5KX-1GP

C3605 SCD01U50V2KX-1GP

R3607 10KR2J-3-GP 3.3V_RUN_ENABLE

3D3V_S0

+3.3V_RUN Comsumption
Peak current 8.14A

1.5V_RUN for VGA Comsumption
Peak current 7.39A

+1.5V_RUN_CPU Comsumption
Peak current 3A

+1.5V_RUN for Mini-Card Comsumption
Peak current 1A

1D5V_S3 1D5V_S0

TPCA8062-H-GP MAX 28A
Rds(on) = 4.1~5.4m OHM

U3606 POWERPAK-8P-GP

C3609 SC10U6D3V5KX-1GP

C3610 SCD01U50V2KX-1GP

R3630 10KR2J-3-GP 1.5V_RUN_ENABLE

X02-0314 Change U3606 footprint.

1D5V_S0

MAX Current ? mA
Design Current ? mA
Total= 11.39A

<Core Design>

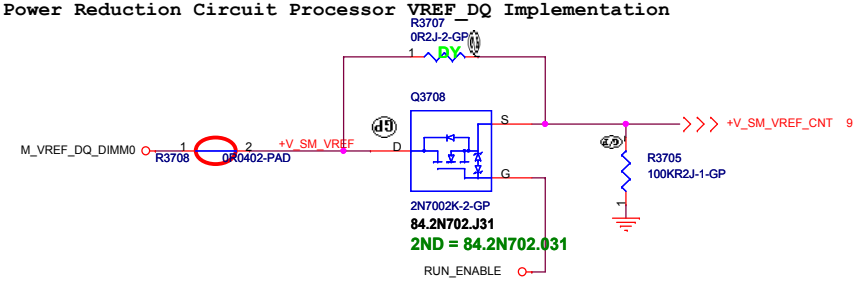
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

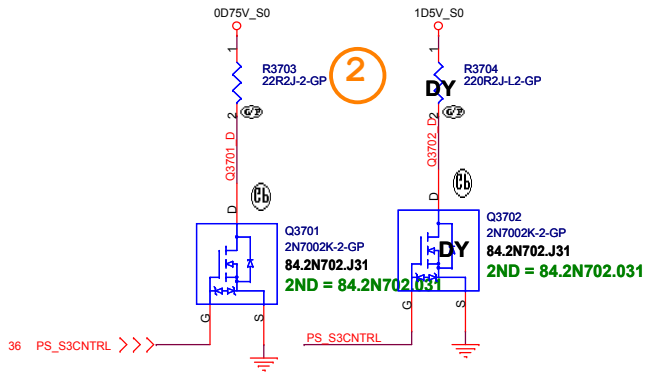
Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

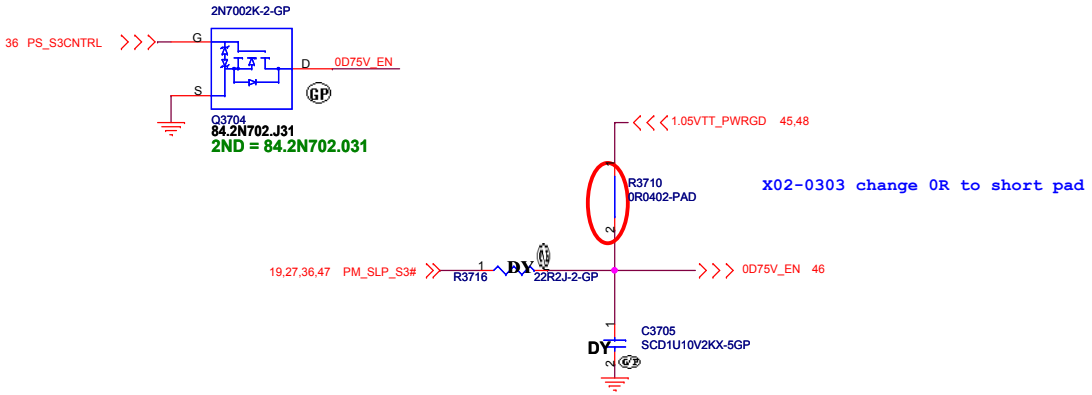
Date: Wednesday, April 13, 2011 | Sheet 36 of 105

Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

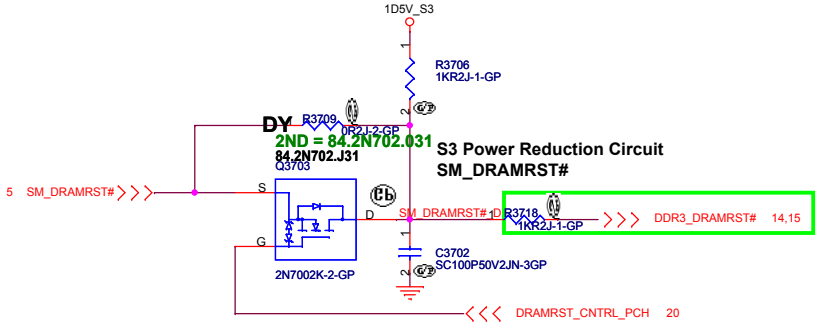


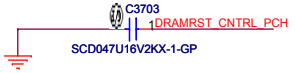
Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK



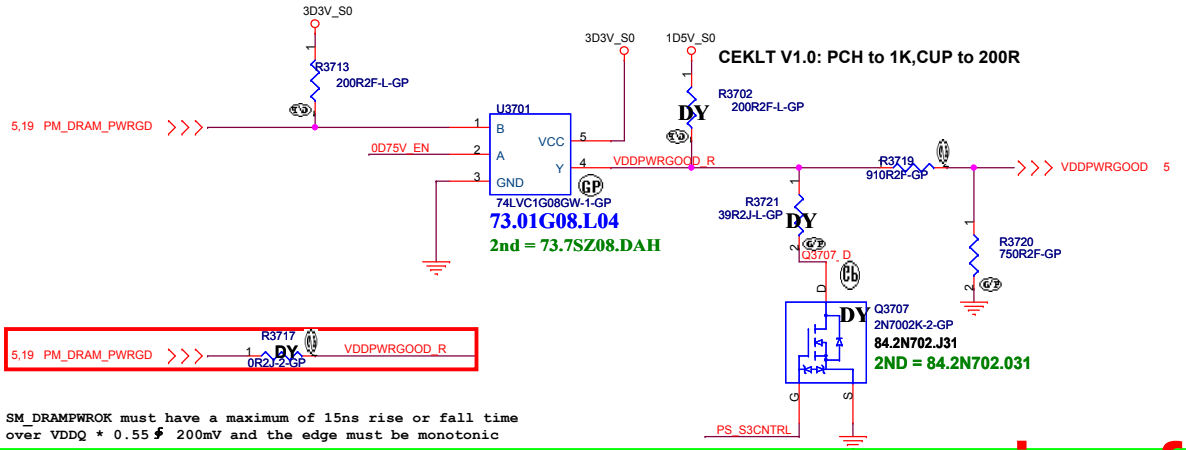


Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK





Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

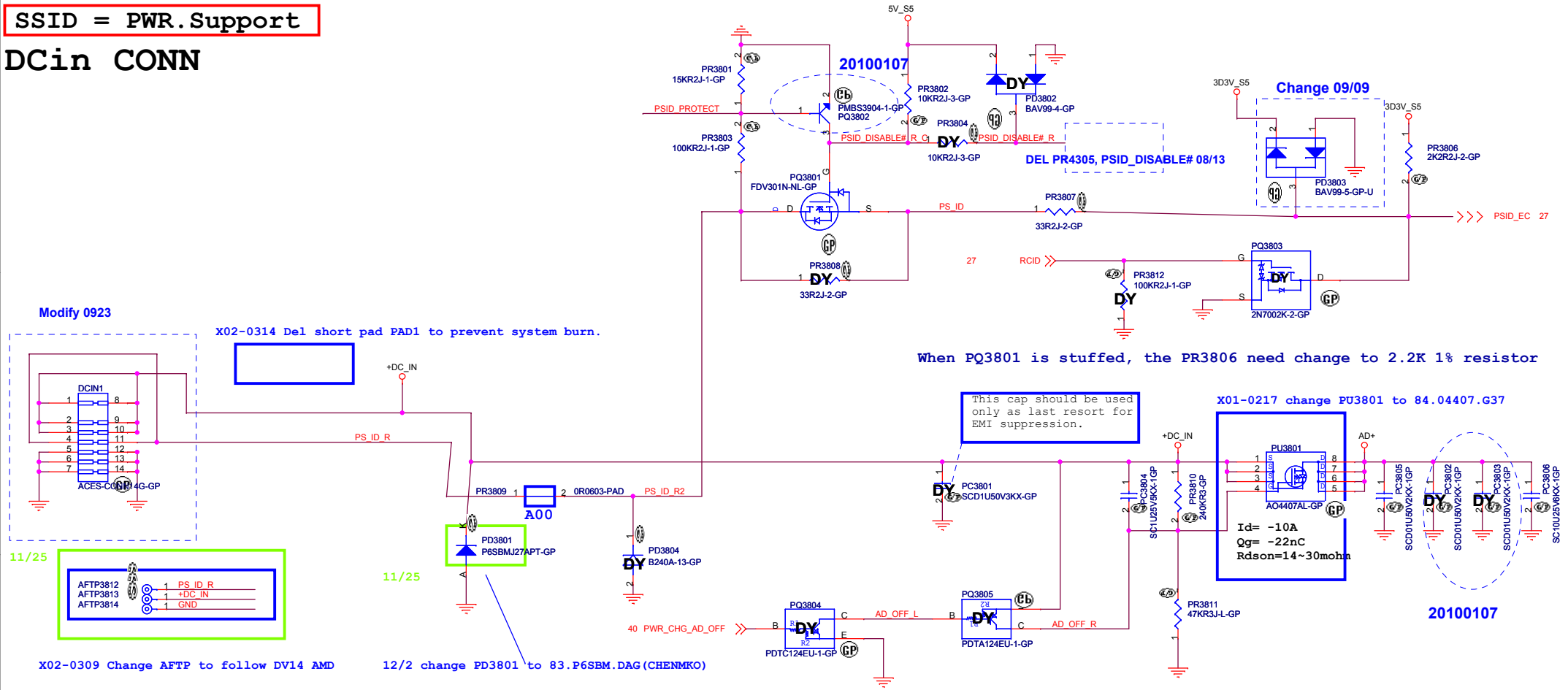
Title: S3 Reduction Circuit

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 37 of 105

SSID = PWR.Support

DCin CONN



<Core Design>

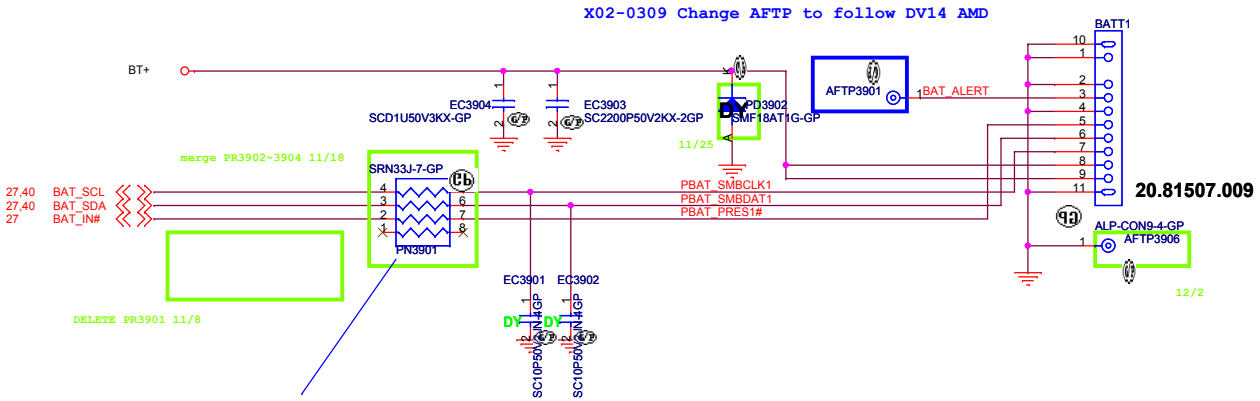
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN Jack		
Size: A3	Document Number: Enrico Caruso 14	Rev: A00
Date: Wednesday, April 13, 2011	Sheet 38 of 105	

SSID = PWR.Support

Batt Connecter

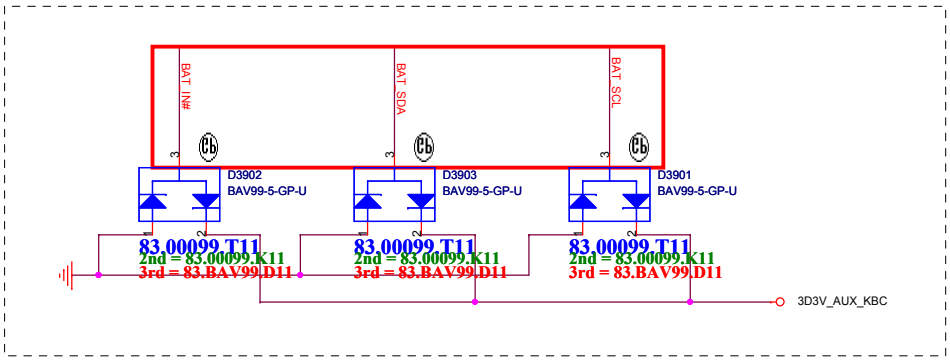
X02-0309 Change AFTP to follow DV14 AMD



X02-0309 change AFTP to follow DV14 AMD

For actual location, need to be swap all pin

Placement: Close to Batt Connector



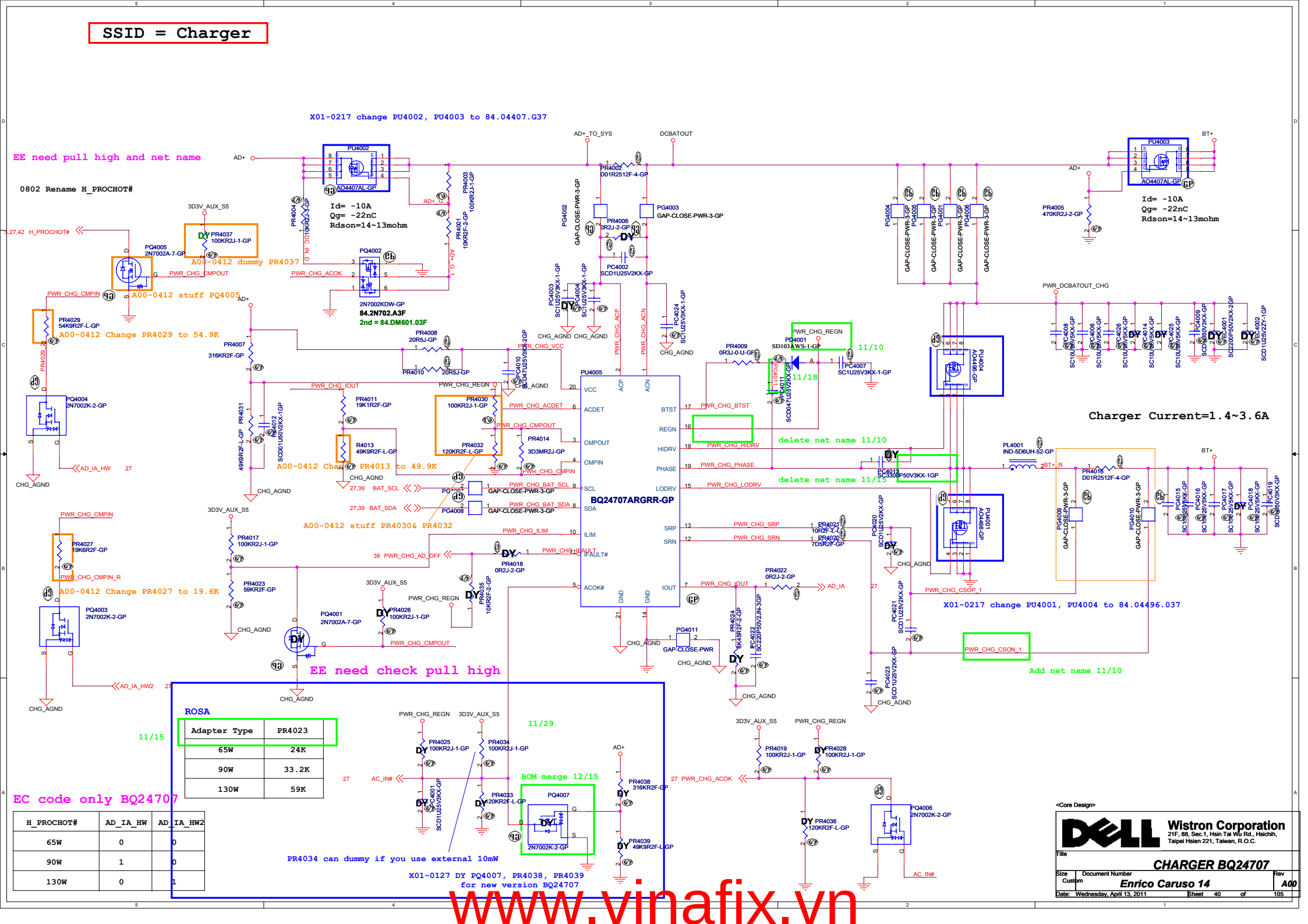
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size	Document Number	Rev
A3	Enrico Caruso 14	A00

Date: Wednesday, April 13, 2011 Sheet 39 of 105

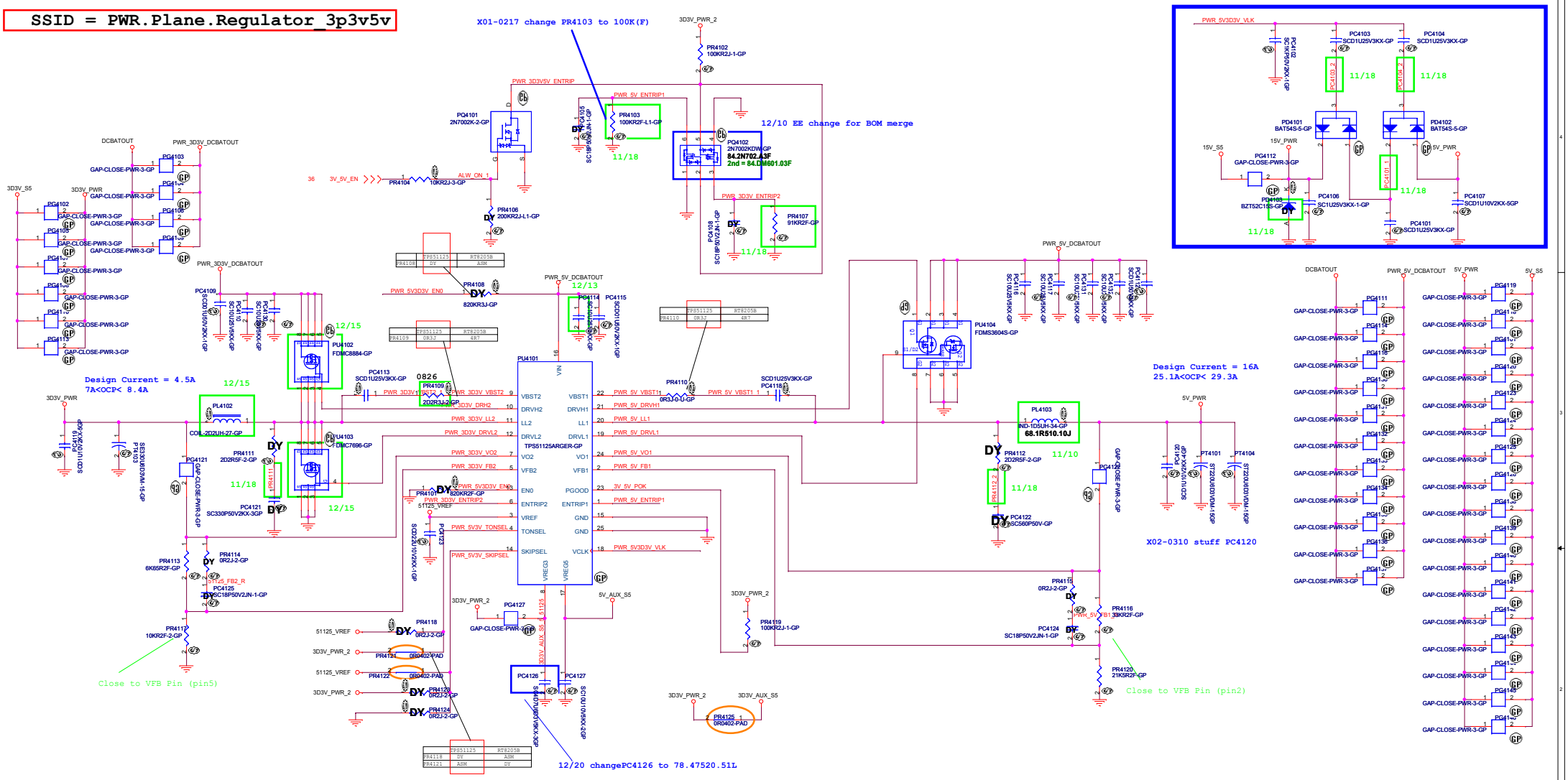


Adapter Type	PR4023
65W	24K
90W	33.2K
130W	59K

H_PROCHOT#	AD_IA_HW	AD_IA_HW2
65W	0	0
90W	1	0
130W	0	1

<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title: CHARGER BQ24707
Size: Custom | Document Number: Enrico Caruso 14 | Rev: A00
Date: Wednesday, April 13, 2011 | Sheet 40 of 105

SSID = PWR.Plane.Regulator_3p3v5v



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 2.2U PCMC063T-2R2MN Cyntec 18mohm/20mohm Isat =10Arms 68.2R210.20B
O/P cap: 330U6.3V M6.3*5.7 15mOhm 3.16Arms Matsuki/77.53371.04L
H/S: SIS412DN / 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: SI7716ADN / 13.5mohm/16.5mOhm@4.5Vgs/ 84.07716.037

I/P cap:10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.50UH PCMC104T-1R5 Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 220U 6.3V PSLV0J227M 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
H/S,L/S: FDMS3604S / 7.5mohm/9.8mOhm@4.5Vgs, 2.6mohm/3.2mOhm@4.5Vgs/ 84.03604.037

SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820k to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

TPS51125:

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

RT8205B:

TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

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Title: TPS51125_5V/3D3V
Size: A2 | Document Number: Enrico Caruso 14 | Rev: A00
Date: Wednesday, April 13, 2011 | Sheet 41 of 105

SSID = CPU.Regulator

Delete PR4212 Pull-up 200 R of ALL_SYS_PWRGD

12/17 change PR4246 to 475K(1%) as DN13

DELETE 11/8

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1316+1314_CPU_CORE(1/3)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 42 of 105

X01-0217 change PR4202, PR4213, PR4230
PR4247 to 7.5K(F)

400mils or Copper Shape

2120mils or Copper Shape

400mils or Copper Shape

53A=2120mils or Copper Shape

12/29 change PL4201 to HF part

<Core Design>

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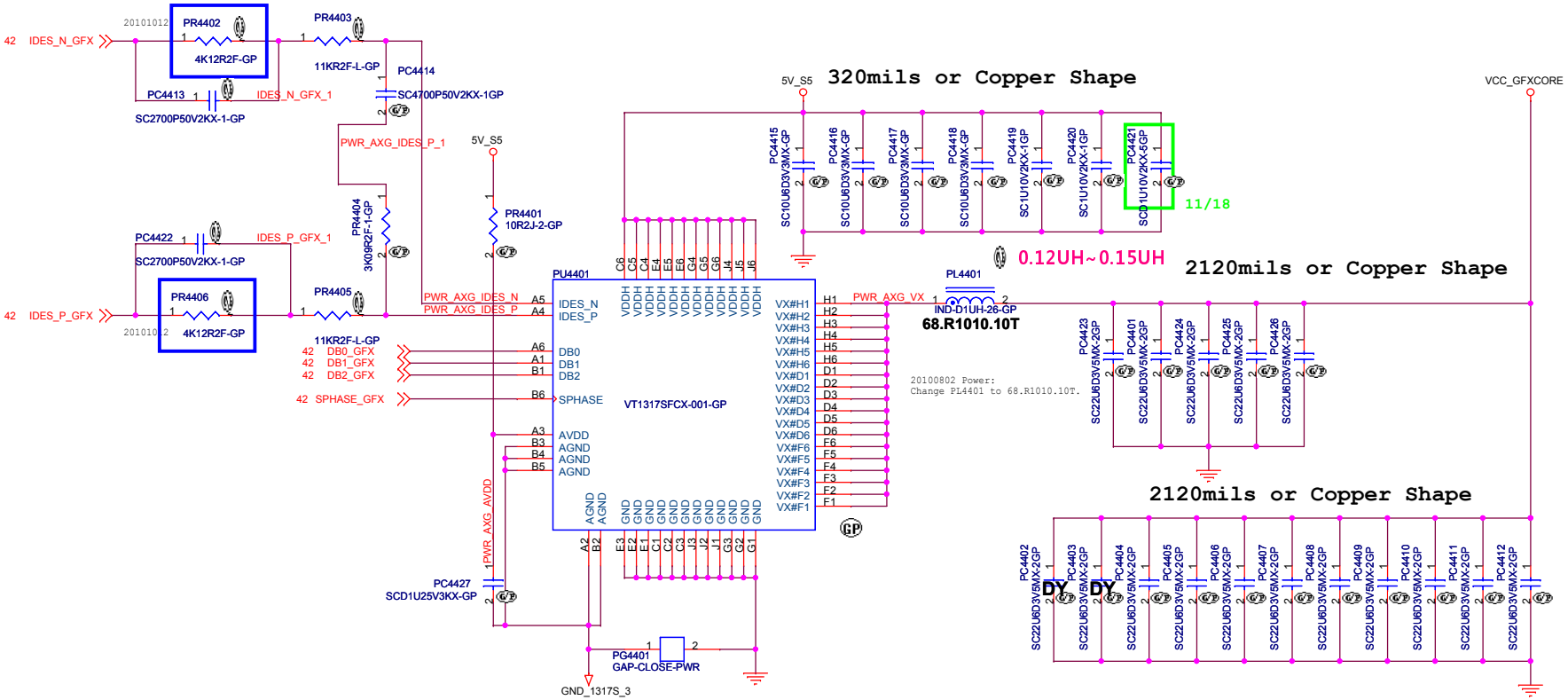
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1316+1314_CPU_CORE(2/3)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 43 of 105

X01-0217 change PR4402& PR4406 to 4.12K(F)



<Core Design>

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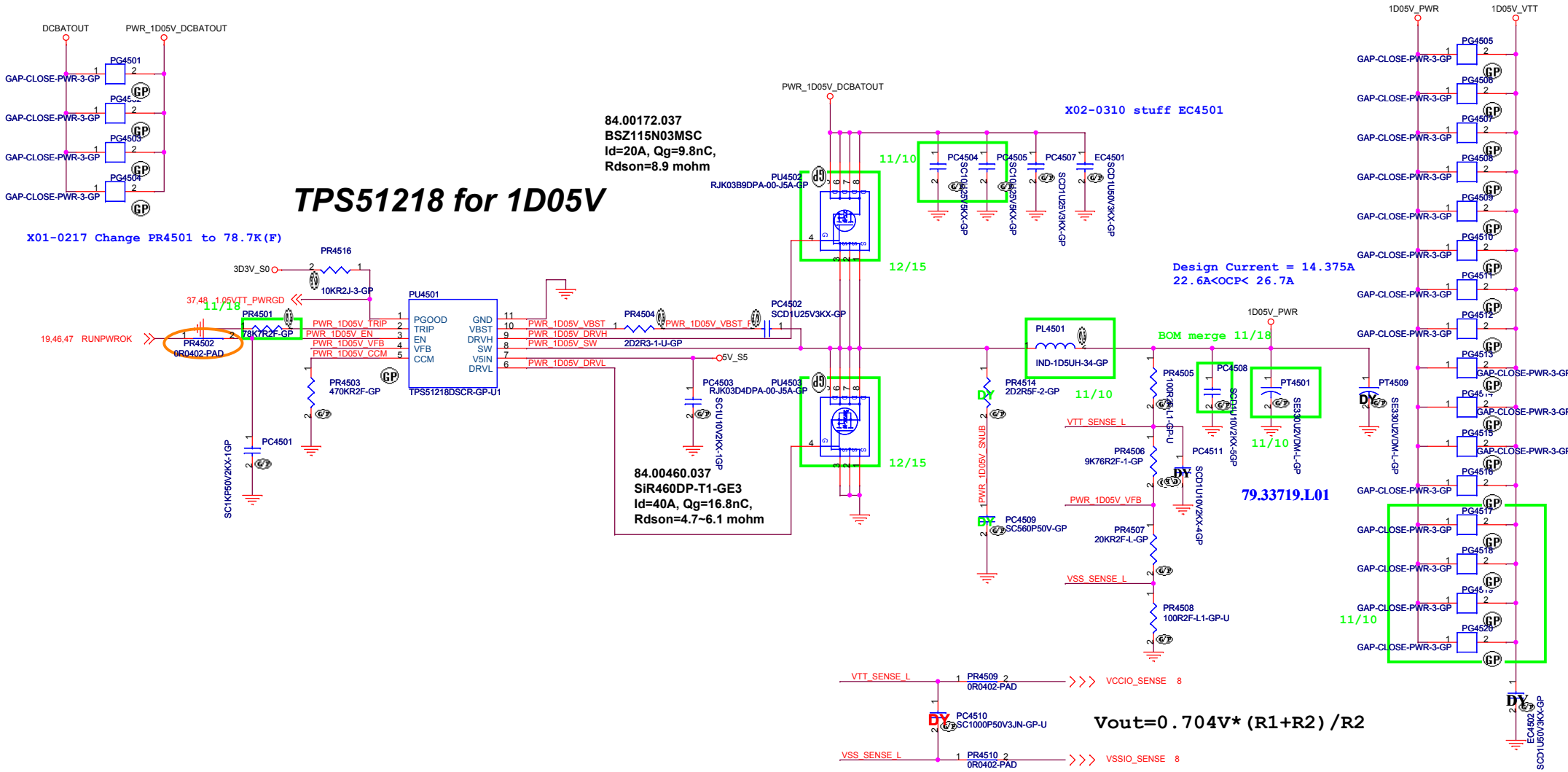
Taipei Hsien 221, Taiwan, R.O.C.

Title: VT1316+1317_AXG_CORE(3/3)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 44 of 105



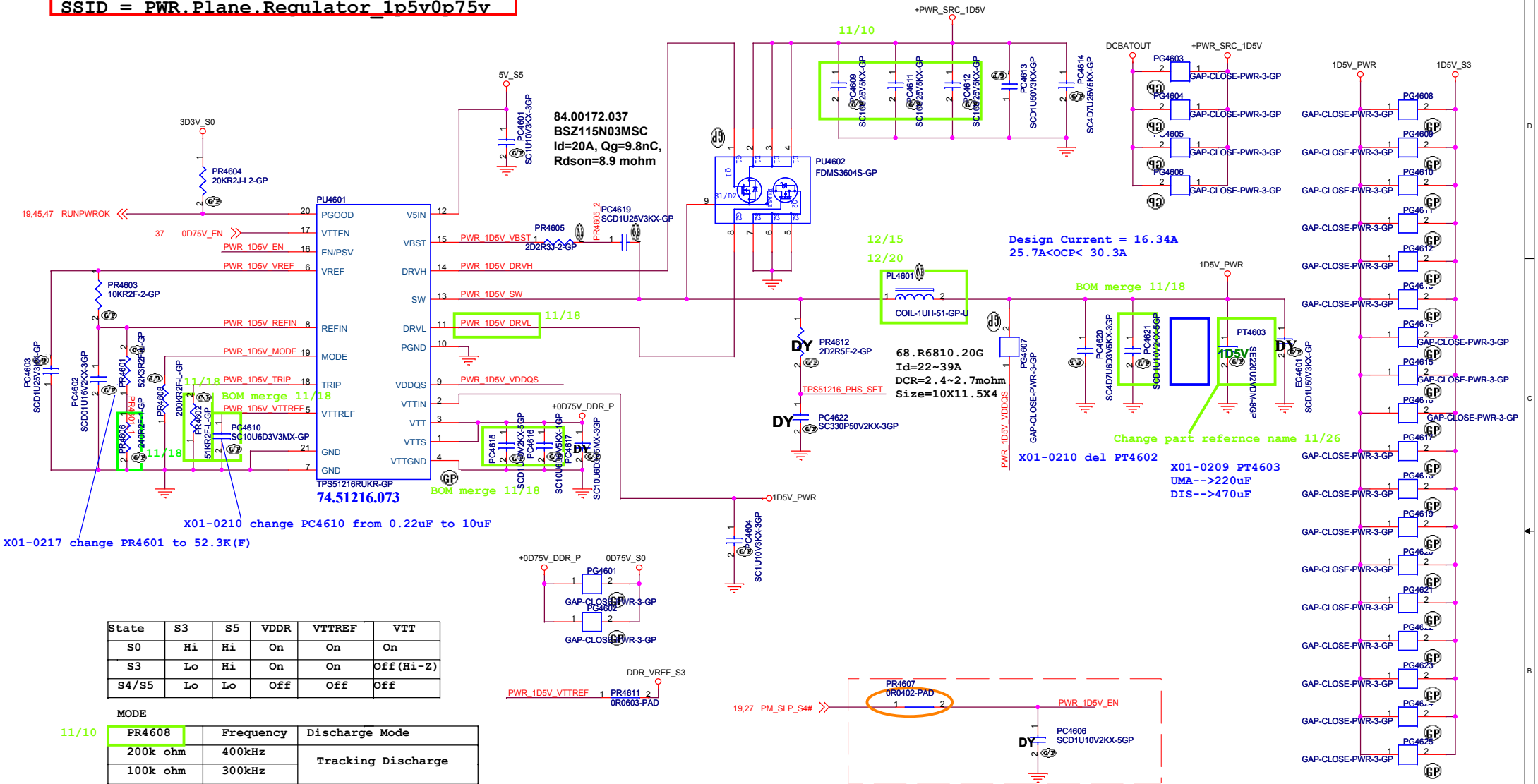
I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: 1.50UH PCMC104T Cyntec 3.8mohm/4.2mohm Isat =33Arms 68.1R510.10J
O/P cap: 330U2V EEFSX0D331ER 9mOhm 3Arms Panasonic/79.33719.L01
H/S: SIR172DP / 10.3mohm/12.4mOhm@4.5Vgs/ 84.00172.037
L/S: SiR460DP / 0.49mohm/0.61mOhm@4.5Vgs/ 84.00460.037

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51218_+1.05V_VTT
Size: A3
Document Number: Enrico Caruso 14
Rev: A00
Date: Wednesday, April 13, 2011
Sheet 45 of 105

SSID = PWR.Plane.Regulator_1p5v0p75v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

11/10

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap:10U 25V K0805 X5R/ 78.10622.51L
Inductor: 0.68UH PCMC104T-R68MN Cyntec 2.4mohm/2.7mohm Isat =39Arms 68.R6810.20G
O/P cap: 220U2V EEFCX0D221R 15mOhm 2.7Arm/Panasonic/79.22719.20L
H/S,L/S: FDMS3604S / 7.5mohm/9.8mOhm@4.5Vgs, 2.6mohm/3.2mOhm@4.5Vgs/ 84.03604.037

<Core Design>

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Title: TPS51216_+1.5V_SUS

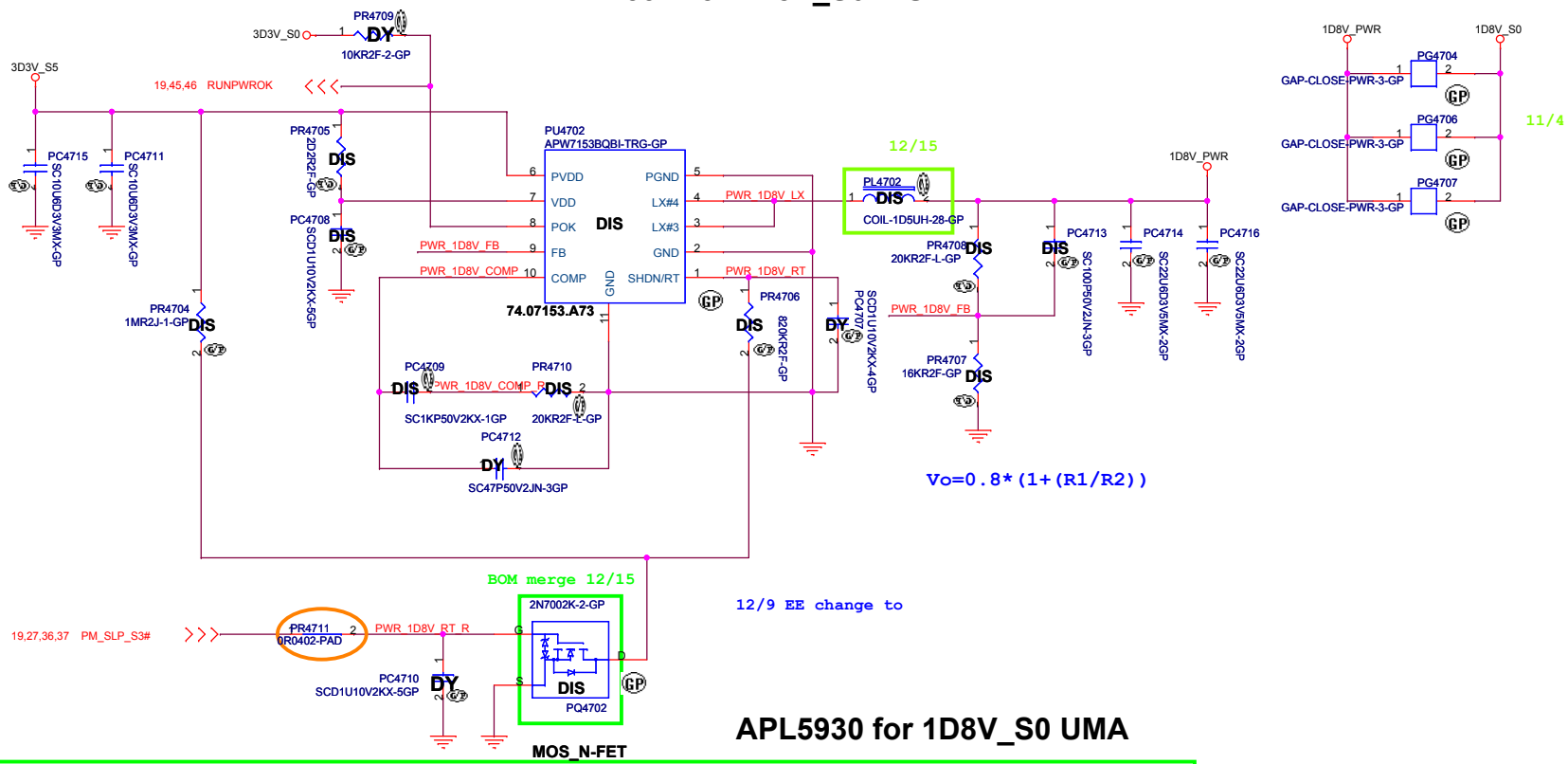
Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 46 of 105

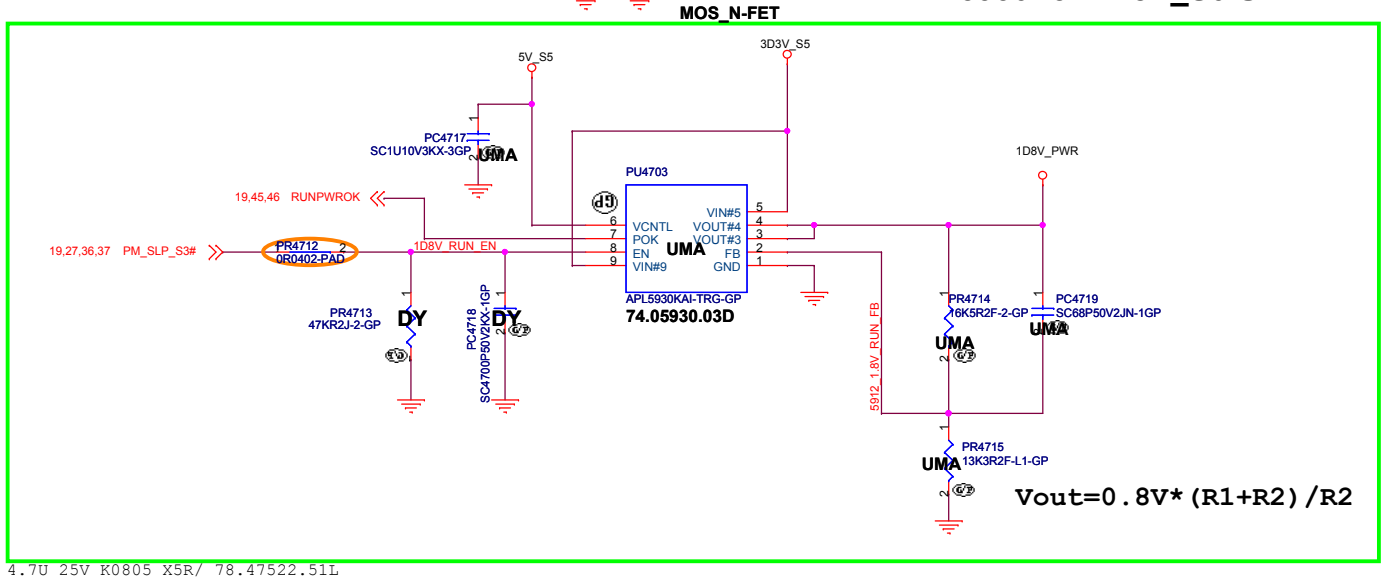
SSID = PWR.Plane.Regulator_1p8v

+1.8V_RUN
Design current = 1.015A

APW7153B for 1D8V_S0 DIS



APL5930 for 1D8V_S0 UMA



I/P cap: 4.7U 25V K0805 X5R/ 78.47522.51L
O/P cap: 22U 25V M0805 X5R/ 78.22610.51L
Inductor: 1.5U PCMC063T Cyntec 14mohm/15mohm Isat =18Arms 68.1R510.10K

<Core Design>

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Title: APW7153B_ +1.8V_RUN
Size: A3
Document Number: Enrico Caruso 14
Rev: A00
Date: Wednesday, April 13, 2011
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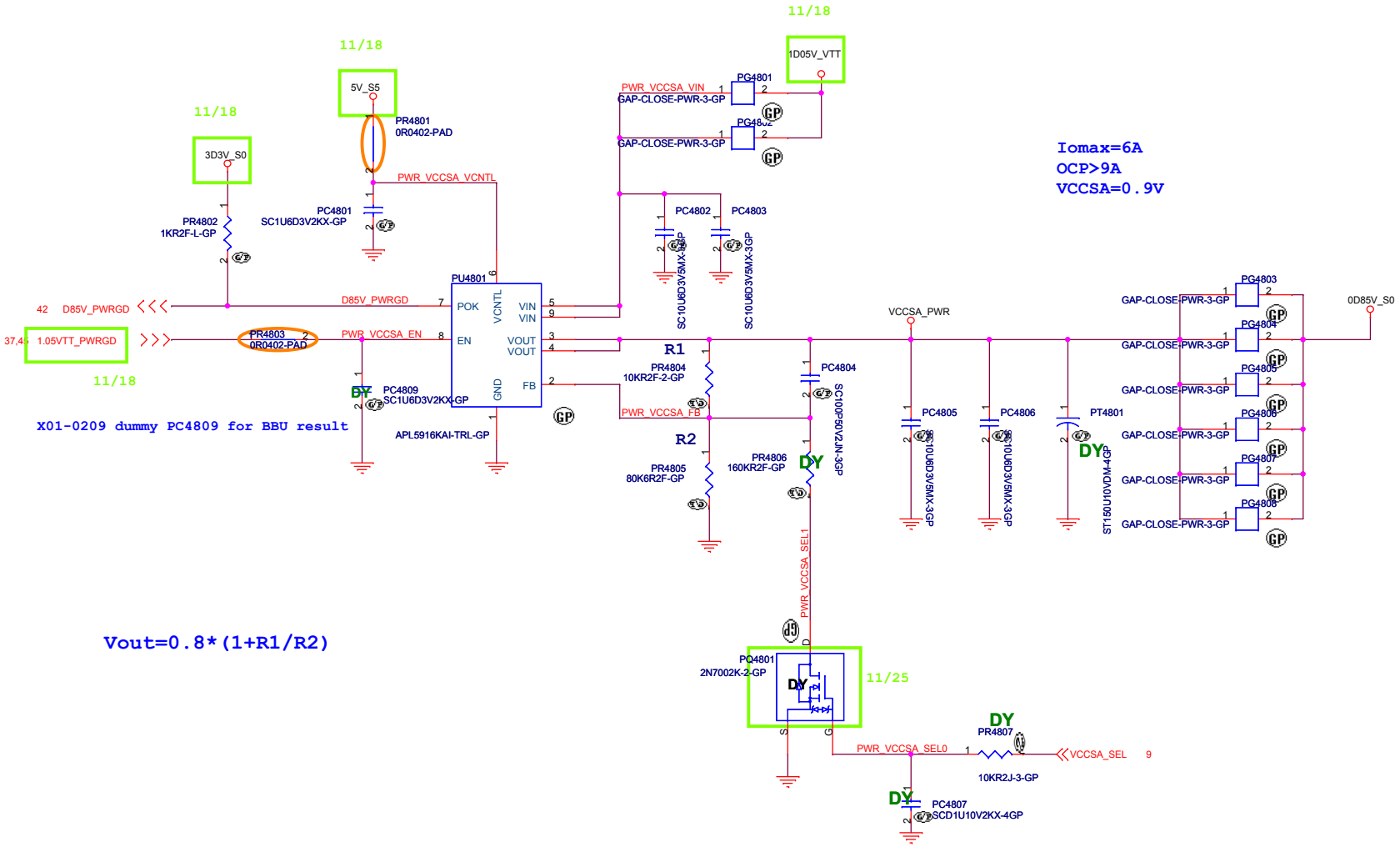
APL5916 for VCCSA



JV10-CS

緯創資通 **Wistron Corporation**
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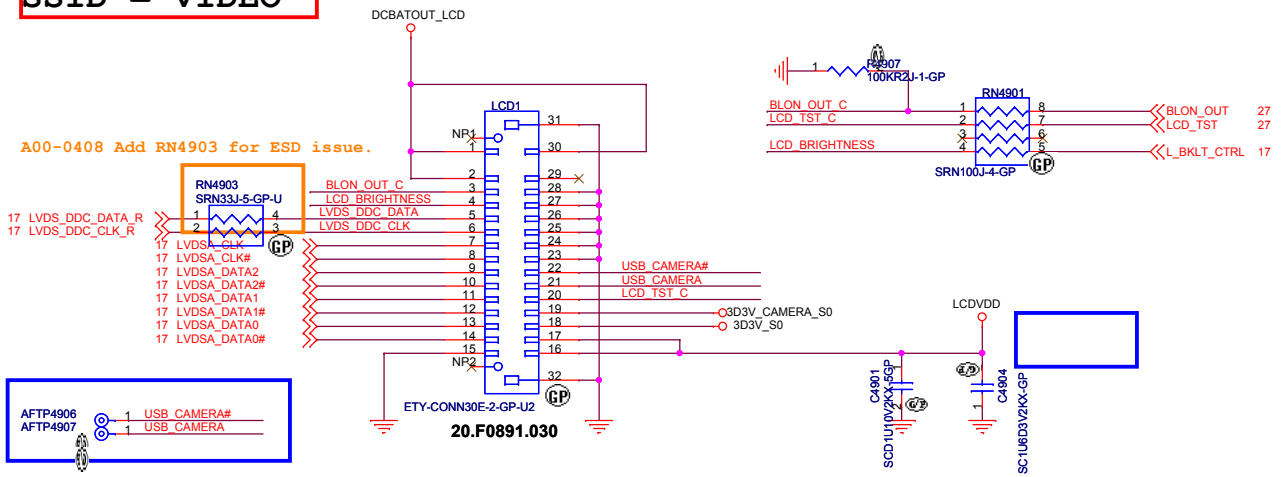
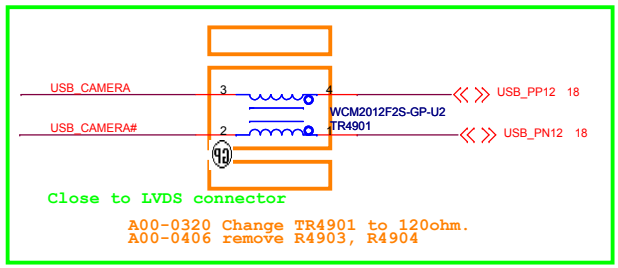
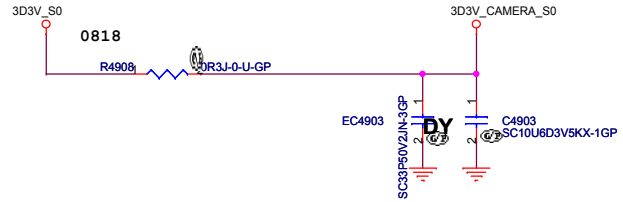
Taipei Hsien 221, Taiwan, R.O.C.

Title	APL5916_VCCSA		
Size	Document Number	Enrico Caruso 14	Rev A00
Date: Wednesday, April 13, 2011	Sheet 48 of 105		

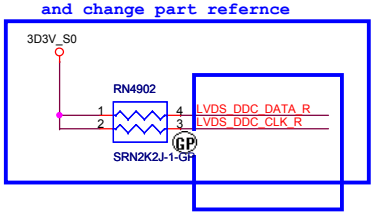
SSID = VIDEO





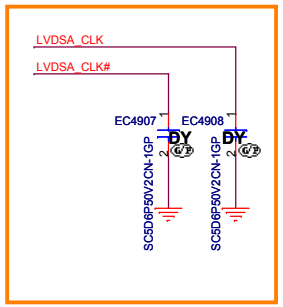


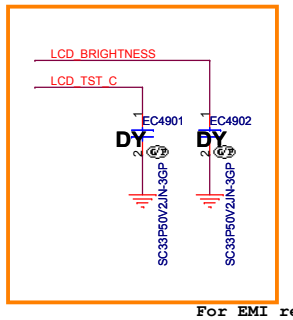
11/17 move RN1703 from P17 to P49
and change part refernce



12/22 swap net for layout

Close to LVDS connector

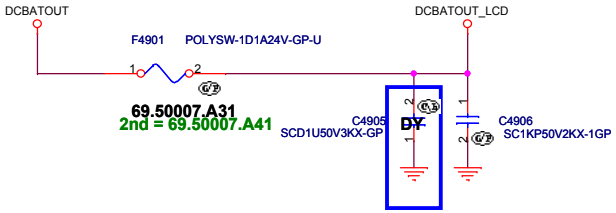




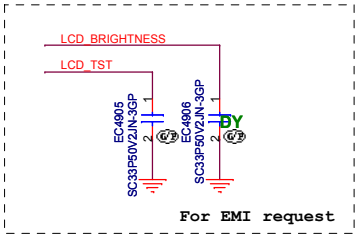
For EMI request

SSID = Inverter

INVERTER POWER



11/ 17 dummy C4905

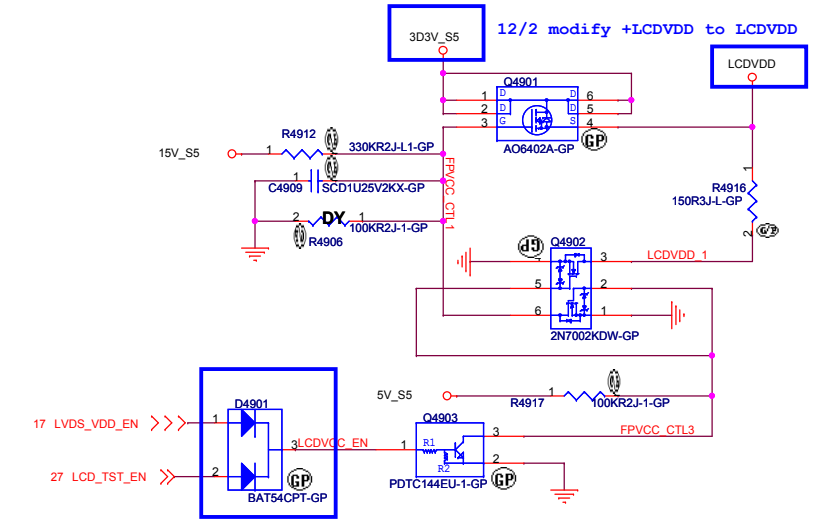


SSID = VIDEO

LCD POWER

11/15 change LCDVDD source from S0 to S5

12/2 modify +LCDVDD to LCDVDD



12/9 BOM merge

<Core Design>

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Title: LCD Connector

Size	Document Number	Rev
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Date: Wednesday, April 13, 2011 Sheet 49 of 105

SSID = VIDEO

11/ 17 Add RN5012 for SMbus pull high

X01: change RN5012 from 0R to 2.2KR

11/3 Add RN5010 for CRT SMBus

X02-0303 change 0R to short pad

11/29 change CRT1 to 20.20927.015

X02-0309 change AFTP to follow DV14 AMD

11/15 remove F5501 base on brazos result.

11/ 17 Remove R5001

11/18 change Fuse for CRT and HDMI share

5V Tolerance

Layout Note:

*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.

* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.

Hsync & Vsync level shift

X00 9/23

X01-0208 change R5002, R5003 to 33R

CLOSE TO TRANSFORMER

DN15ATI Whistler

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Title: CRT Connector

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 50 of 105

SSID = VIDEO

HDMI Level Shifter & CONNECTOR

HDMI CONN

HDMI_CLK_R_C — R5101 0R0402-PAD — HDMI_CLK_R_C_CON
HDMI_CLK_R_C# — R5102 0R0402-PAD — HDMI_CLK_R_C#_CON
HDMI_DATA1_R_C — RR5106 0R0402-PAD — HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C# — RR5105 0R0402-PAD — HDMI_DATA1_R_C#_CON

A00-0407 remove TR5101, TR5102, TR5103, TR5104 PAD and remove 0R PAD.

HDMI_DATA0_R_C — RR5104 0R0402-PAD — HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C# — RR5103 0R0402-PAD — HDMI_DATA0_R_C#_CON
HDMI_DATA2_R_C — RR5108 0R0402-PAD — HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C# — RR5107 0R0402-PAD — HDMI_DATA2_R_C#_CON

HDMI_PLL_GND — R5123 0R2J-2-GP — Q5103 2N7002K-2-GP 84.2N702.J31
2ND = 84.2N702.031
5V_S0 — R5113 100KR2J-1-GP DY
11/19 change net Q5103_G to 5V_S0

HDMI1 SKT-HDMI19P-63-GP-U 22.10296.171
HDMI_DATA2_R_C_CON
HDMI_DATA2_R_C#_CON
HDMI_DATA1_R_C_CON
HDMI_DATA1_R_C#_CON
HDMI_DATA0_R_C_CON
HDMI_DATA0_R_C#_CON
HDMI_CLK_R_C_CON
HDMI_CLK_R_C#_CON
DDC_CLK_HDMI
DDC_DATA_HDMI
HPD_HDMI_CON
11/18 change Fuse for CRT and HDMI share
5V_CRT_S0_R
C5102 SCD1U10V2KX-5GP
X02-0309
Del AFTP test point to follow DV14 AMD
3D3V_S0
12/9 BOM merge
12/23 BOM merge
Q5102 PMBS3904-1-GP 84.03904.L06
2ND = 84.03904.M11
HDMI_HPD_B — R5111 150KR2J-L1-GP
HDMI_HPD_E — R5125 0R0402-PAD — HDMI_PCH_DET 17
R5110 200KR2J-L1-GP DY
R5112 10KR2J-3-GP

HDMI DISCRETE/ UMA Co-lay

17 HDMI_CLK_R# — C5103 SCD1U10V2KX-5GP — HDMI_CLK_R_C#
17 HDMI_CLK_R — C5104 SCD1U10V2KX-5GP — HDMI_CLK_R_C
17 HDMI_DATA0_R# — C5105 SCD1U10V2KX-5GP — HDMI_DATA0_R_C#
17 HDMI_DATA0_R — C5106 SCD1U10V2KX-5GP — HDMI_DATA0_R_C
66.68136.08L=>680ohm for UMA
66.47136.A8L=>470ohm for GPU
17 HDMI_DATA1_R# — C5110 SCD1U10V2KX-5GP — HDMI_DATA1_R_C#
17 HDMI_DATA1_R — C5107 SCD1U10V2KX-5GP — HDMI_DATA1_R_C
17 HDMI_DATA2_R# — C5108 SCD1U10V2KX-5GP — HDMI_DATA2_R_C#
17 HDMI_DATA2_R — C5109 SCD1U10V2KX-5GP — HDMI_DATA2_R_C
RN5106 SRN680J-GP
RN5107 SRN680J-GP
HDMI_PLL_GND

5V_CRT_S0_R
12/1 Modify 5V_HDMI to 5V_CRT_S0_R
RN5101 SRN2K2J-1-GP
3D3V_S0
11/18 change RN5117 BOM control property to HDMI
17 PCH_HDMI_CLK
17 PCH_HDMI_DATA
RN5117 0R4P2R-PAD
X02-0303 change 0R to short pad
DDC_CLK_Q
DDC_DATA_Q
Q5104 2N7002KDW-GP 84.2N702.A3F
2nd = 84.DM601.03F
DDC_CLK_HDMI
DDC_DATA_HDMI

11/16 Del RN5112~5115 for no need to reserve for VGA

Routing Guidelines:
CTRLDATA must be routed longer than CTRLCLK within 1000 mils (25.4 mm).
The total delay on CTRLDATA should be longer than CTRLCLK.

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Level Shifter/Connector
Size: A3
Document Number: Enrico Caruso 14
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Date: Wednesday, April 13, 2011
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DN15ATI Whistler

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Title: Reserved

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 52 of 105

(Blanking)

DN15ATI Whistler

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Title: LVDS_Switch

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 53 of 105

(Blanking)

DN15ATI Whistler

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Title: Reserved

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 54 of 105

SSID = User.Interface

(Blanking)

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ITP/Fan Connector

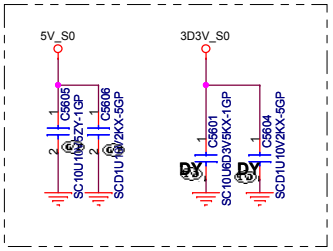
Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 55 of 105

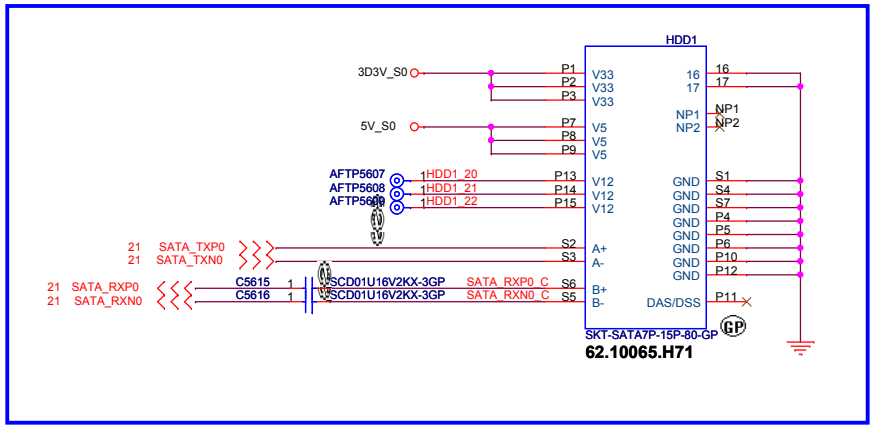
SSID = SATA

SATA HDD Connector

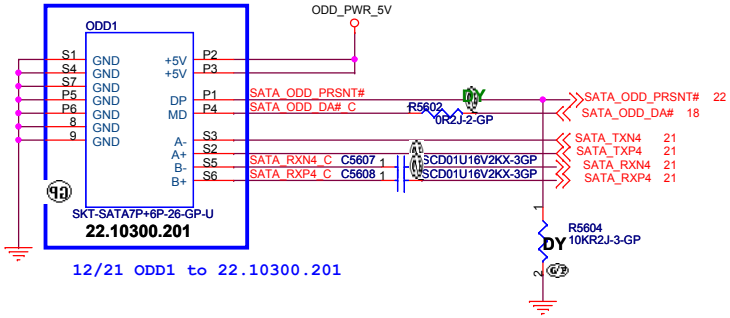
11/10 Change HDD1 CONN to 62.10065.031
12/22 Change HDD1 CONN to62.10065.H71



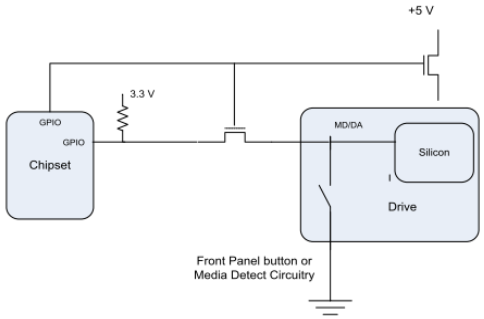
Close to HDD1



ODD Connector

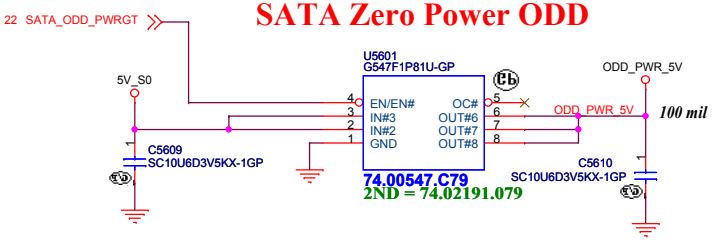


12/21 ODD1 to 22.10300.201

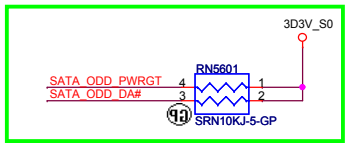


When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

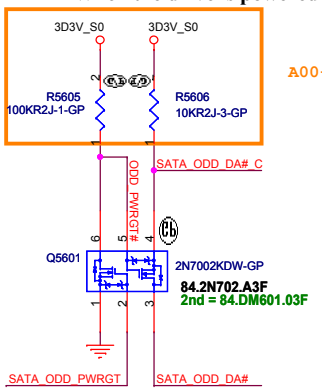
SATA Zero Power ODD



Current limit
Active High
typ =>2A



SUPPORT ZERO SATA ODD



A00-0408 Add R5606 to pull high 3.3V_S0
Change pull high to 3.3V_S0

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD/ODD

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 56 of 105

SSID = ESATA

(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title	ESATA	
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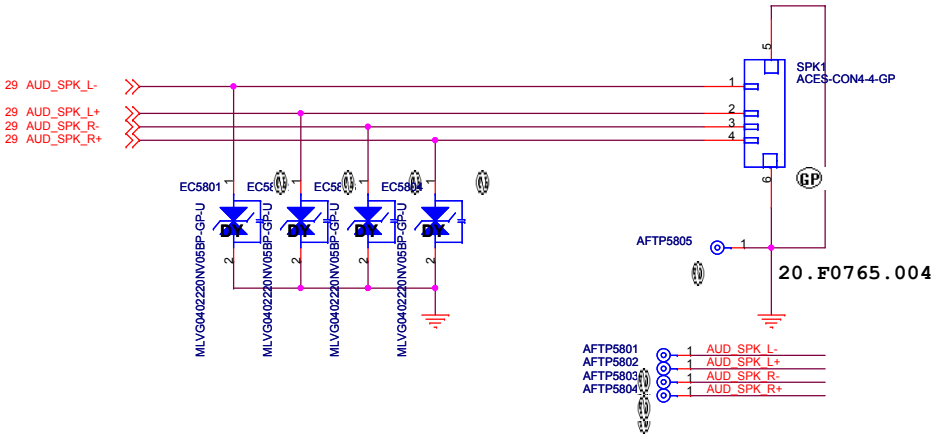
SSID = AUDIO

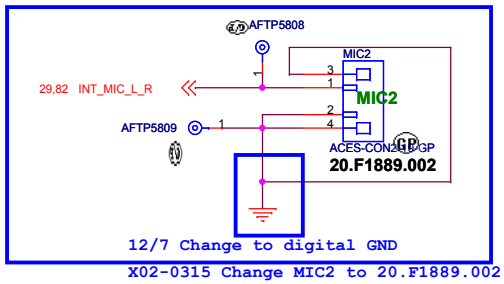
Speaker Connector



11/10 remove MIC1

11/26 reserve MIC2

12/7 change MIC2 to 20.F1050.002



X02-0315 Change MIC2 to 20.F1889.002

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Title: SPEAKER CONN

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SSID = LOM

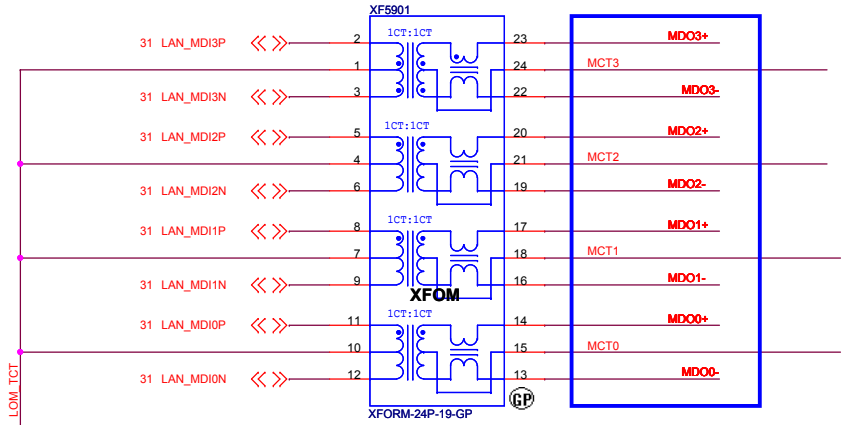
LAN TransFormer

X01-0211 Add EMI solution for Surge

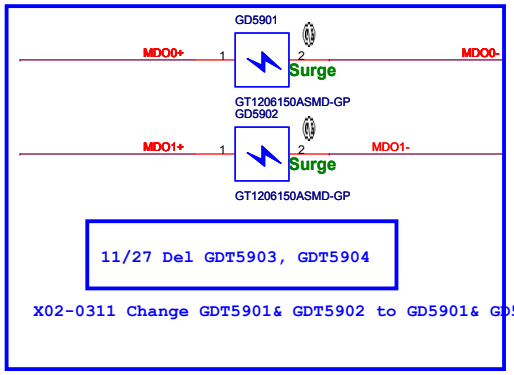
11/30 swap net

Giga Main: 68.IH601.301
Giga 2nd: 68.05009.30A

10/100 Main: 68.HH035.301
10/100 Main: 68.01284.30A



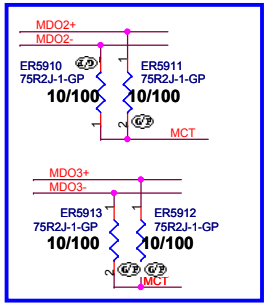
2nd = 68.89240.30B

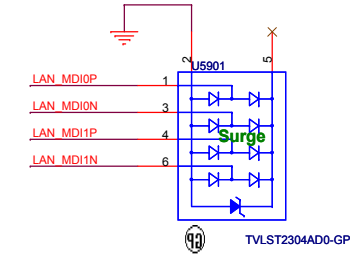


11/27 Del GDT5903, GDT5904

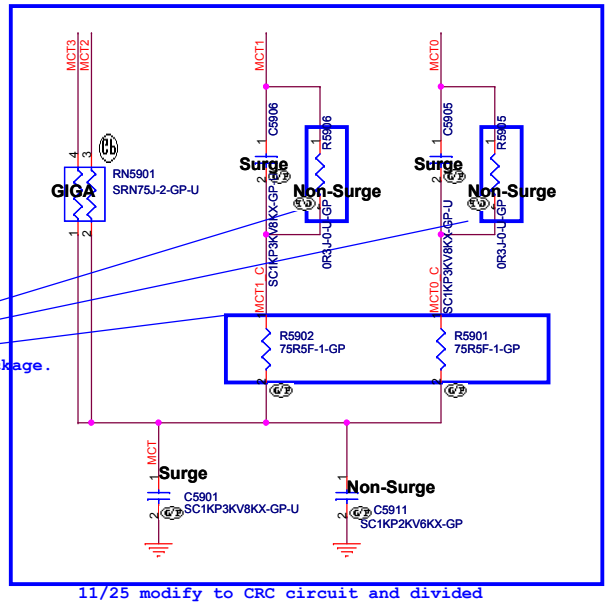
X02-0311 Change GDT5901& GDT5902 to GD5901& GD5902

0722 : change to gas tube





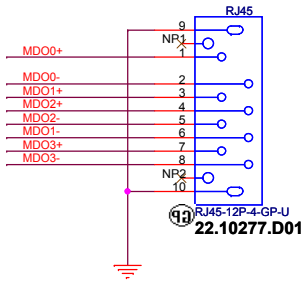
11/27 Del U5902



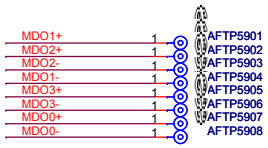
12/6 change resistor package.

11/25 modify to CRC circuit and divided resistor as EMI suggest
11/29 Change C5911 to 78.1022S.22L

RJ45



11/29 change RJ45 to 22.10277.D01



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Title: XFOM&RJ45

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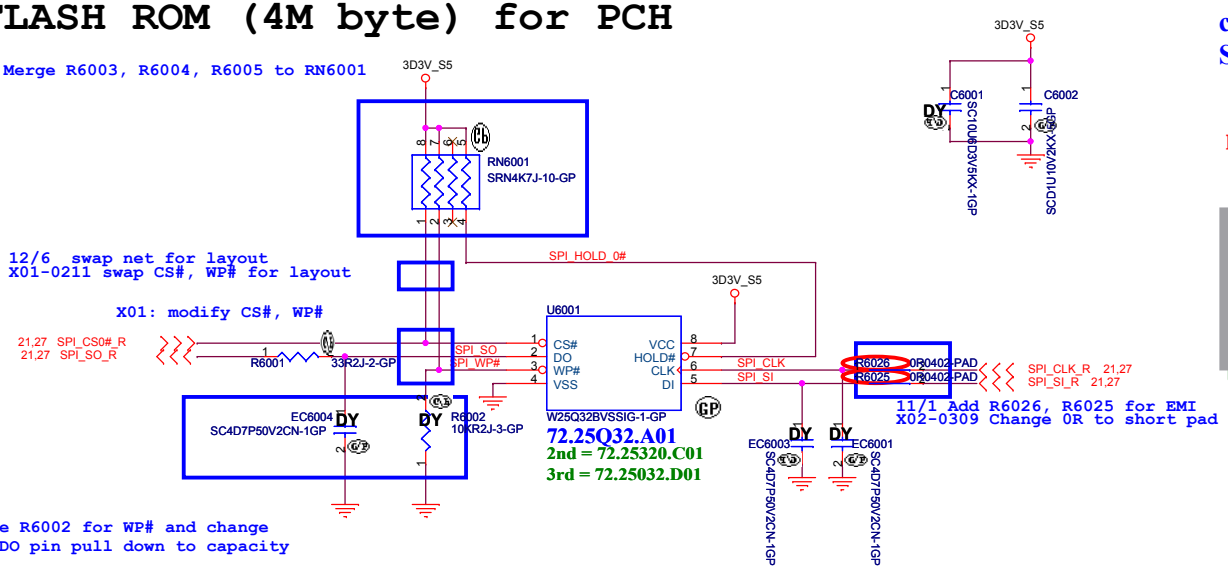
SSID = Flash.ROM

SPI FLASH ROM (4M byte) for PCH

11/18 Merge R6003, R6004, R6005 to RN6001

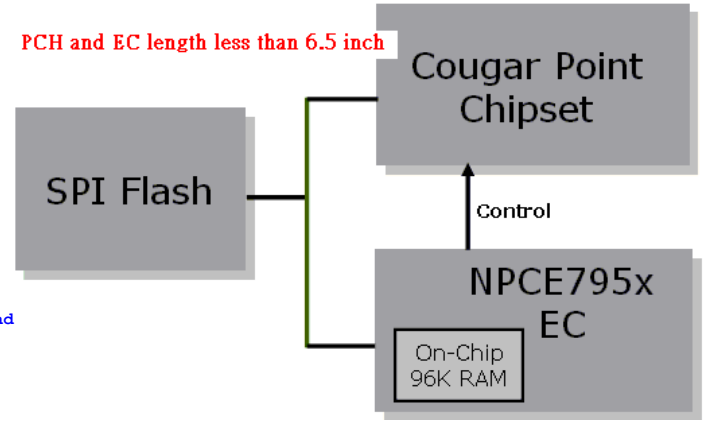


11/18 reserve R6002 for WP# and change
change DO pin pull down to capacity

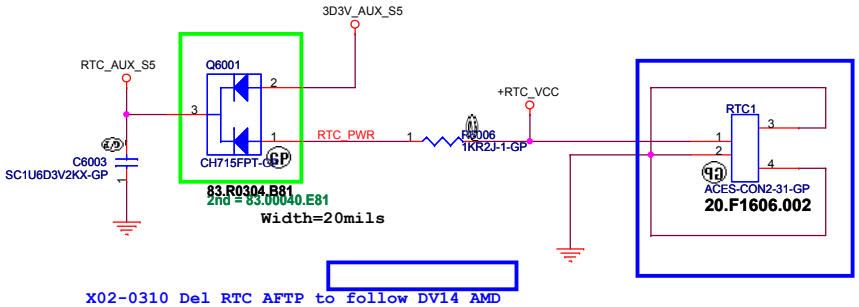
Pirority	Wistron P/N	Manufacturer	Vendor P/N
1	72.25Q32.A01	WINBOND	W25Q32BVSSIG
2	72.25320.C01	MXIC	MX25L3206EM2I-12G
3	72.25032.D01	SST	SST25VF032B-80-4I-S2AF
4	72.25P32.C01	Numonyx	M25PX32-VMW6F

Notes:
The total SPI interface signal between EC and PCH can't not exceed 6500mil. The mismatch between SPI signal must be within 500mil

PCH and EC length less than 6.5 inch

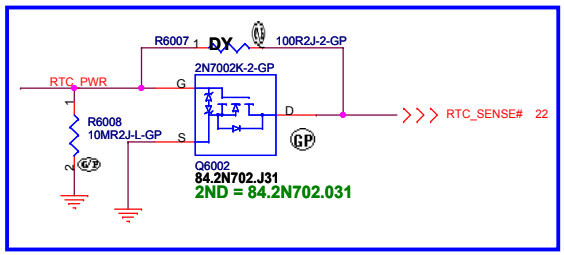


SSID = RBATT

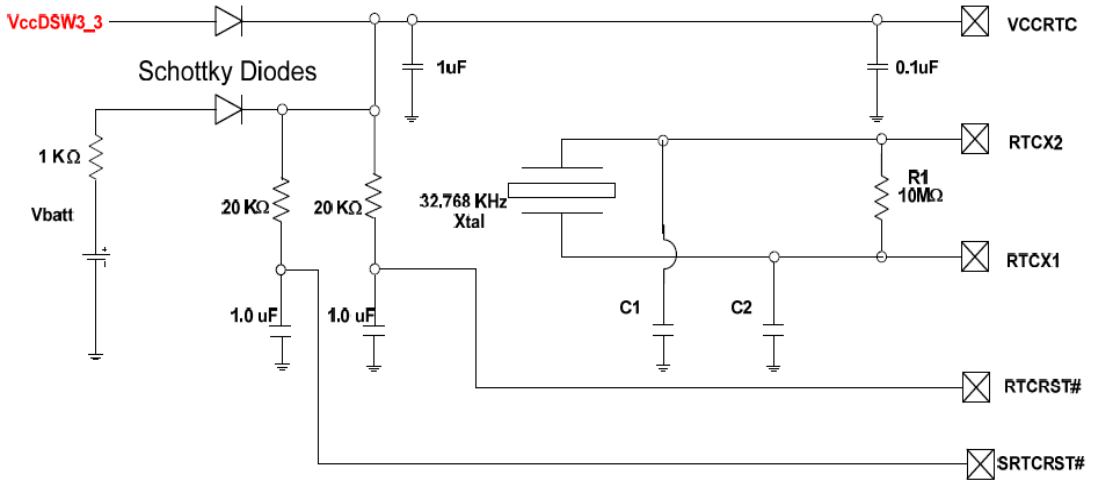


X02-0310 Del RTC AFTP to follow DV14 AMD

11/29 change RTC1 to 20.F1606.002



11/23 add RTC DET circuit



VccRTC is now connected to VccDSW3_3 through the Schottky diode instead of the 3.3V Sus well.

<Core Design>

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Title: Flash/RTC

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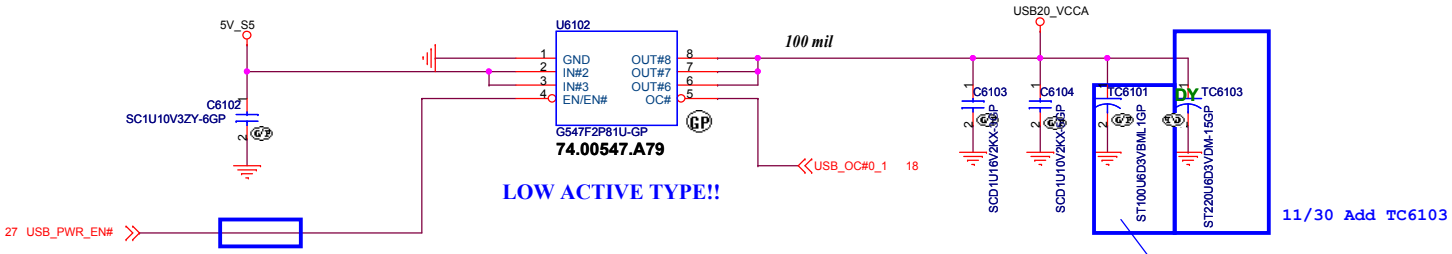
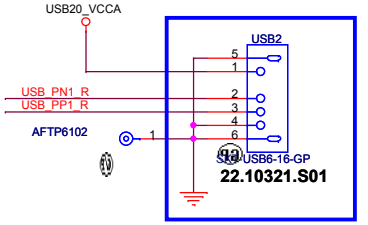
SSID = USB



LOW ACTIVE TYPE!!

11/30 Add TC6103

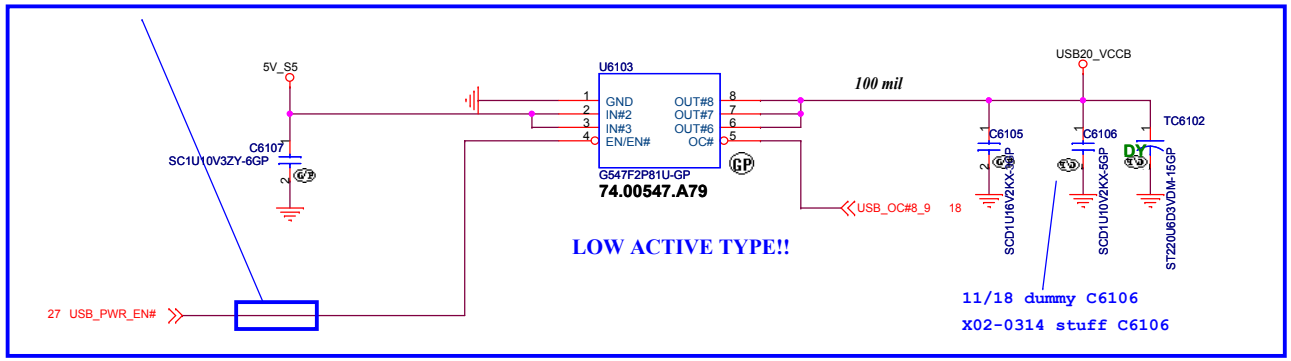
12/22 change TC6101 to 100uF



11/29 change USB2 to 22.10321.S01

11/18 remove R6101, R6104

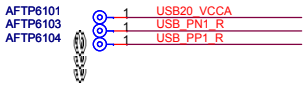
11/10 Move USB power SW to Mainboard



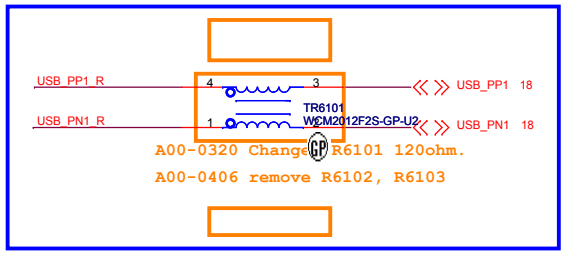
LOW ACTIVE TYPE!!

11/18 dummy C6106

X02-0314 stuff C6106



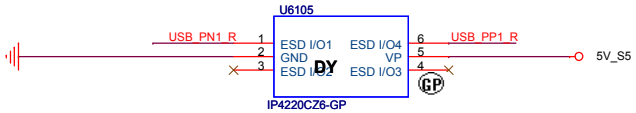
11/1 Stuff TR6101 for EMI



A00-0320 Change R6101 120ohm.

A00-0406 remove R6102, R6103

A00-0408 Swap TR6101 net for layout



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Title: USB Power SW

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SSID = User.Interface

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Title: Bluetooth

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: RESERVED

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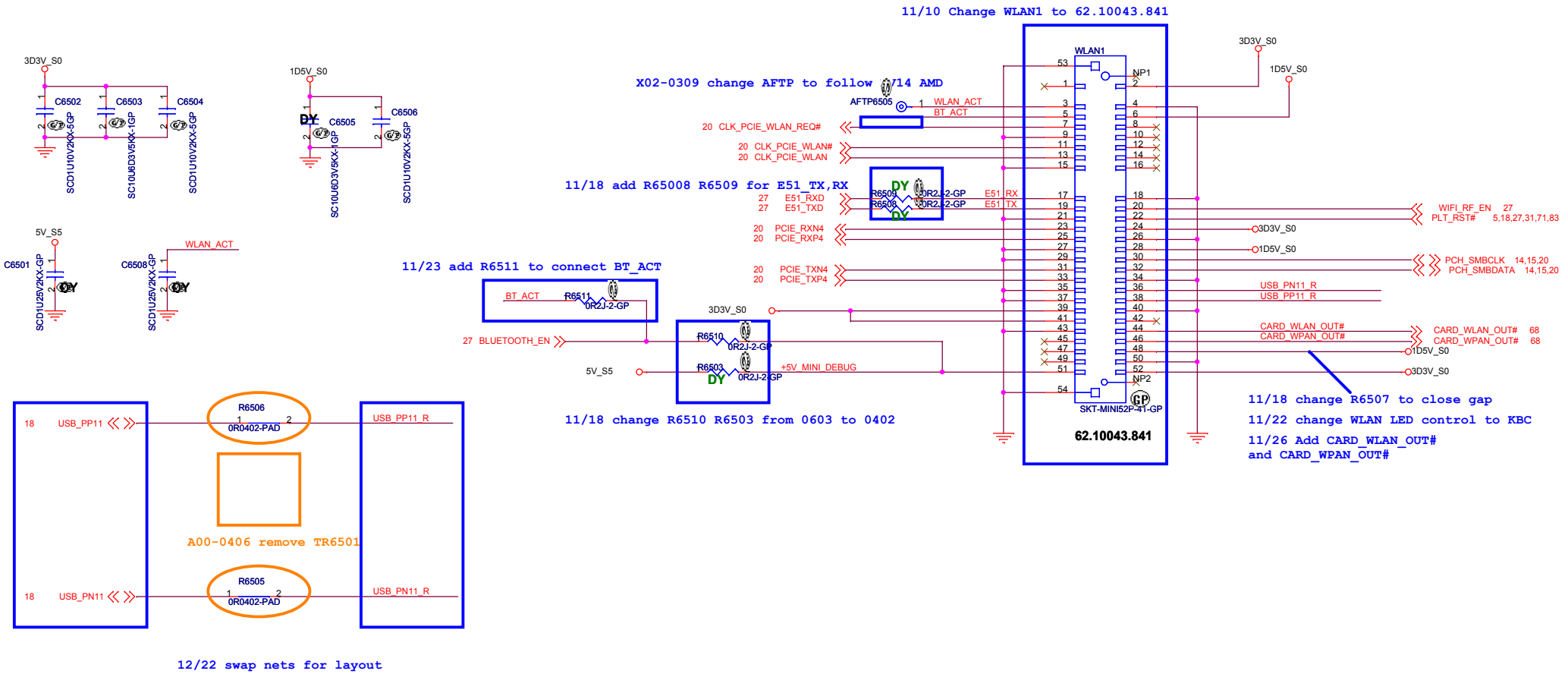
SSID = Wireless

Mini Card Connector(802.11a/b/g)



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Title: MINICARD(WLAN)/ITP CONN

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Title: Reserved

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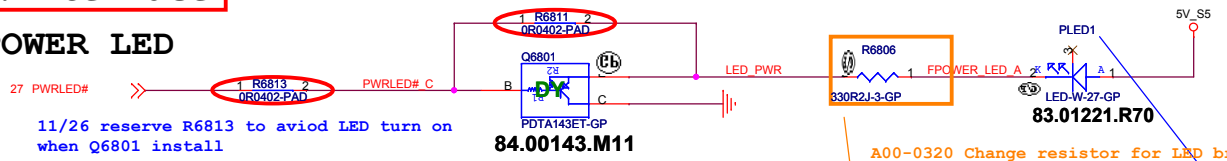
SSID = User.Interface

FRONT POWER LED



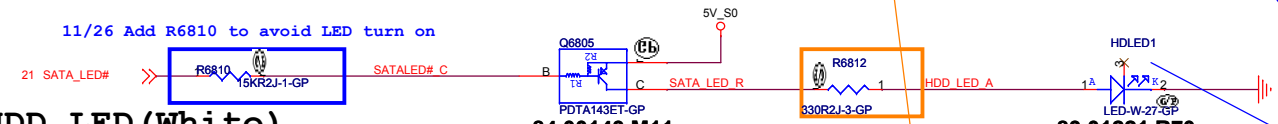
11/26 reserve R6813 to aviod LED turn on when Q6801 install

84.00143.M11

83.01221.R70

A00-0320 Change resistor for LED brightness

11/26 Add R6810 to avoid LED turn on

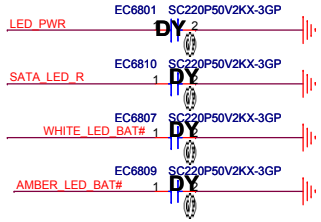


SATA HDD LED(White)

84.00143.M11

83.01221.R70

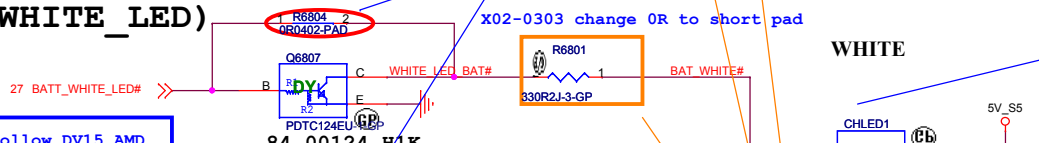
Need change to LOW actived from KBC GPIO



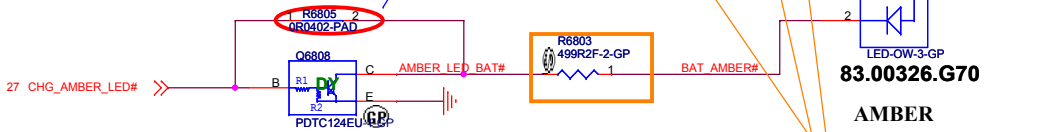
12/3 Change LED part reference to follow standard

11/18 add R6804 R6805 0ohm and dummy Q6807, Q6808

Battery LED2(WHITE_LED)



11/16 Del RN6801 to follow DV15 AMD



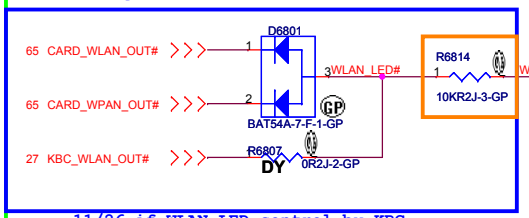
Battery LED1(AMBER_LED)

A00-0413 change R6806, R6812, R6801, R6808 to 330ohm

Wireless LED

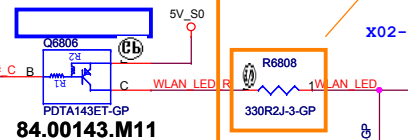
A00-0328 change R6814 to 10KR

11/26 change WLANLED control circuit



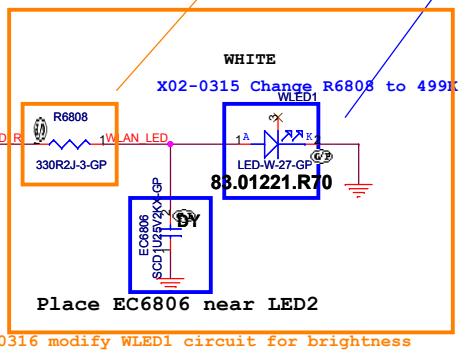
11/26 if WLAN LED control by KBC. remove D6801 and short R6814, R6807

11/26 remove R6835



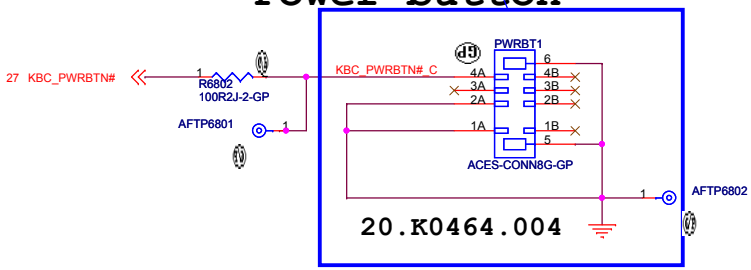
84.00143.M11

X01-0217 Change R6814 to 0R



A00-0316 modify WLED1 circuit for brightness

Power button



12/10 change PWRBT1 pin define

12/21 change PWRBT1 to 20.K0464.004

<Core Design>

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Title: LED Bard/Power Button

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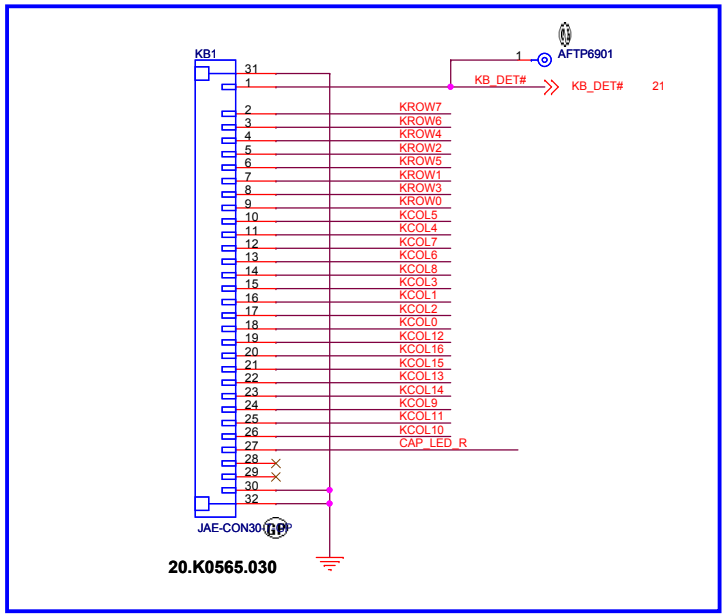
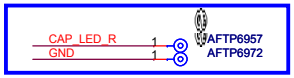
SSID = KBC



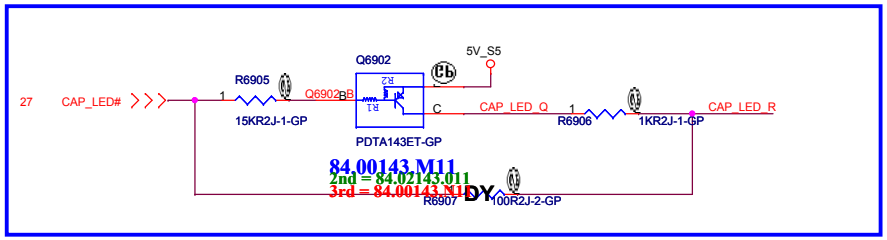
11/26 change KB1 to 20.K0597.030
12/8 Change KB1 to 20.K0565.030

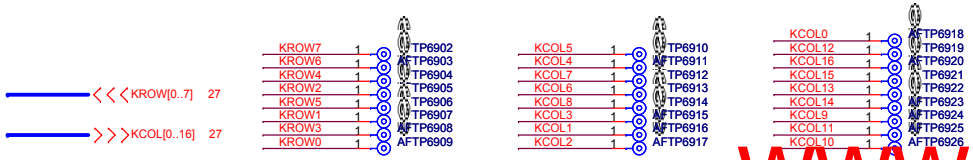
X02-0309 change AFTP to follow DV14 AMD



12/8 Add Cap LED control circuit

CAP LED CONTROL



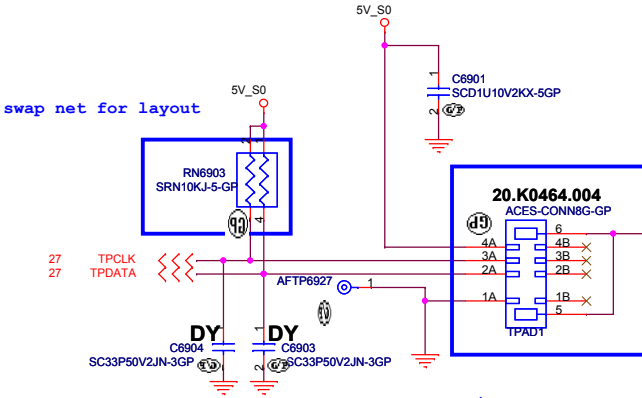


SSID = Touch.Pad

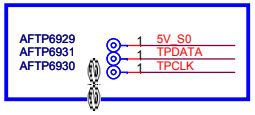
X01-0216 Modify pin define error

TouchPad Connector

12/6 swap net for layout



X01-0216 Modify pin define error



X01-0216 exchange C6903& C6904

11/23 change TPAD1 to 20.K0320.004
X01-0208 change TPAD1 to 20.K0464.004
X01-0216 Modify pin define error

<Core Design>

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Title: Key Board/Touch Pad
Size: A3
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Hall Sensor*

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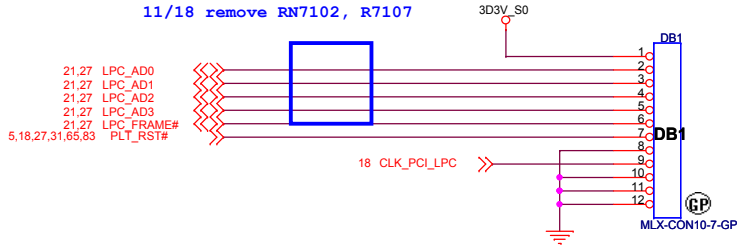
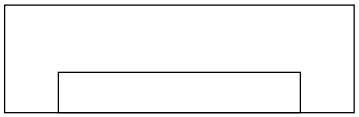
11/18 remove RN7102, R7107



20.D0183.110



DN15ATI Whistler

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
Debug connector		
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DN15ATI Whistler

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Enrico Caruso 14* | Rev: *A00*

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DN15ATI Whistler

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Reserved

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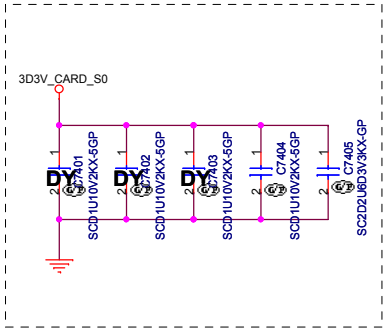
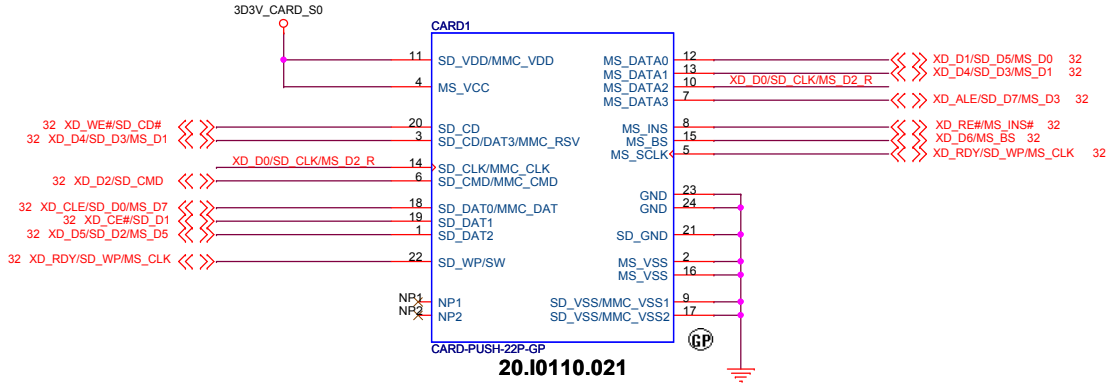
Date: Wednesday, April 13, 2011 | Sheet 73 of 105

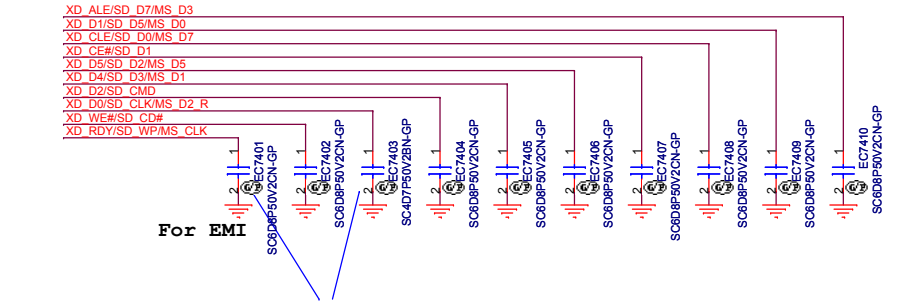
SSID = SDIO





20.I0110.021

0810 Vendor Recommand

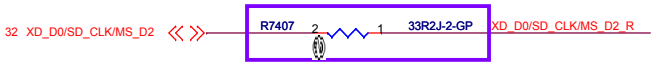


For EMI

11/18 Dummy EC7401, EC7403

11/20 vendor recommand to reserve 5P

X01-0216 stuff EC7401~EC7410 for EMI



For EMI

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **SD/XD/MS/MMC Card CONN**

Size: A3 | Document Number: **Enrico Caruso 14** | Rev: **A00**

Date: Wednesday, April 13, 2011 | Sheet 74 of 105

SSID = ExpressCard

<Core Design>

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Title: Express Card

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A3	Enrico Caruso 14	A00

Date: Wednesday, April 13, 2011 Sheet 75 of 105

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Title: Reserved

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

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Title: Reserved

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Date: Wednesday, April 13, 2011 | Sheet 77 of 105

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Title: Reserved

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Date: Wednesday, April 13, 2011 | Sheet 78 of 105

SSID = User.Interface

(Blanking)

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Title: Free Fall Sensor

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 79 of 105

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Title: Reserved

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 80 of 105

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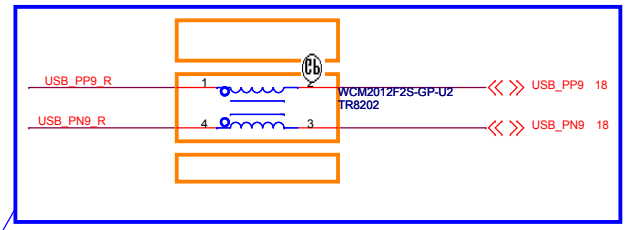
Title: *Reserved*

Size: A3 | Document Number: *Enrico Caruso 14* | Rev: *A00*

Date: Wednesday, April 13, 2011 | Sheet 81 of 105

11/1 Stuff TR8201, TR8202 for EMI

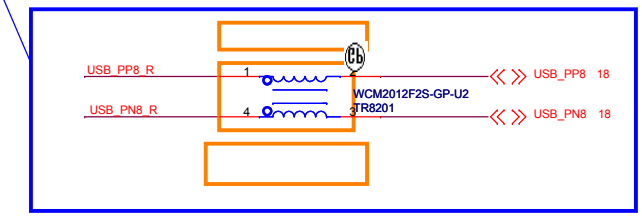


A00-0406 remove R8201, R8202, R8203, R8204 pad

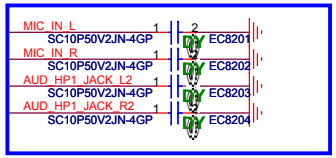
A00-0320 Change TR8201, TR8202 to 120ohm.

A00-0408 Swap net for layout

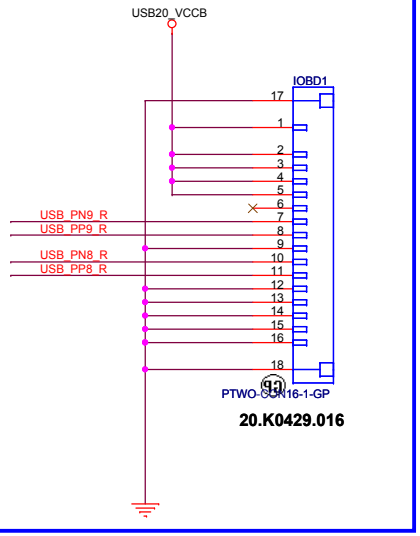
12/6 swap net for layout



11/1 Add EC2901~EC2904 for EMI request



IOBD1 is for USB board

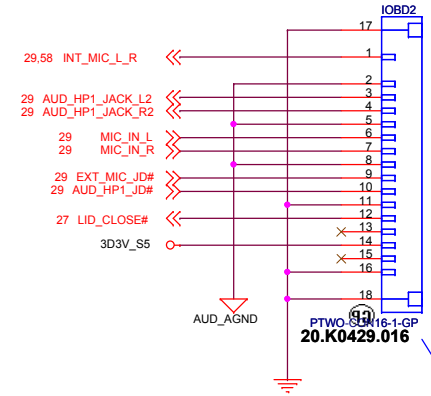


11/10 modify B2B CONN and pin define

X01-0214 add AFTP8201~8210

X02-0309 Del AFTP8201~8210

IOBD2 is for Audio board



X02-0309 Del AFTP8201~8210

12/10 Change pin defien for audio board routing smooth.

12/14 Change IOBD2 to 20.K0429.016 and change pin define.

<Core Design>

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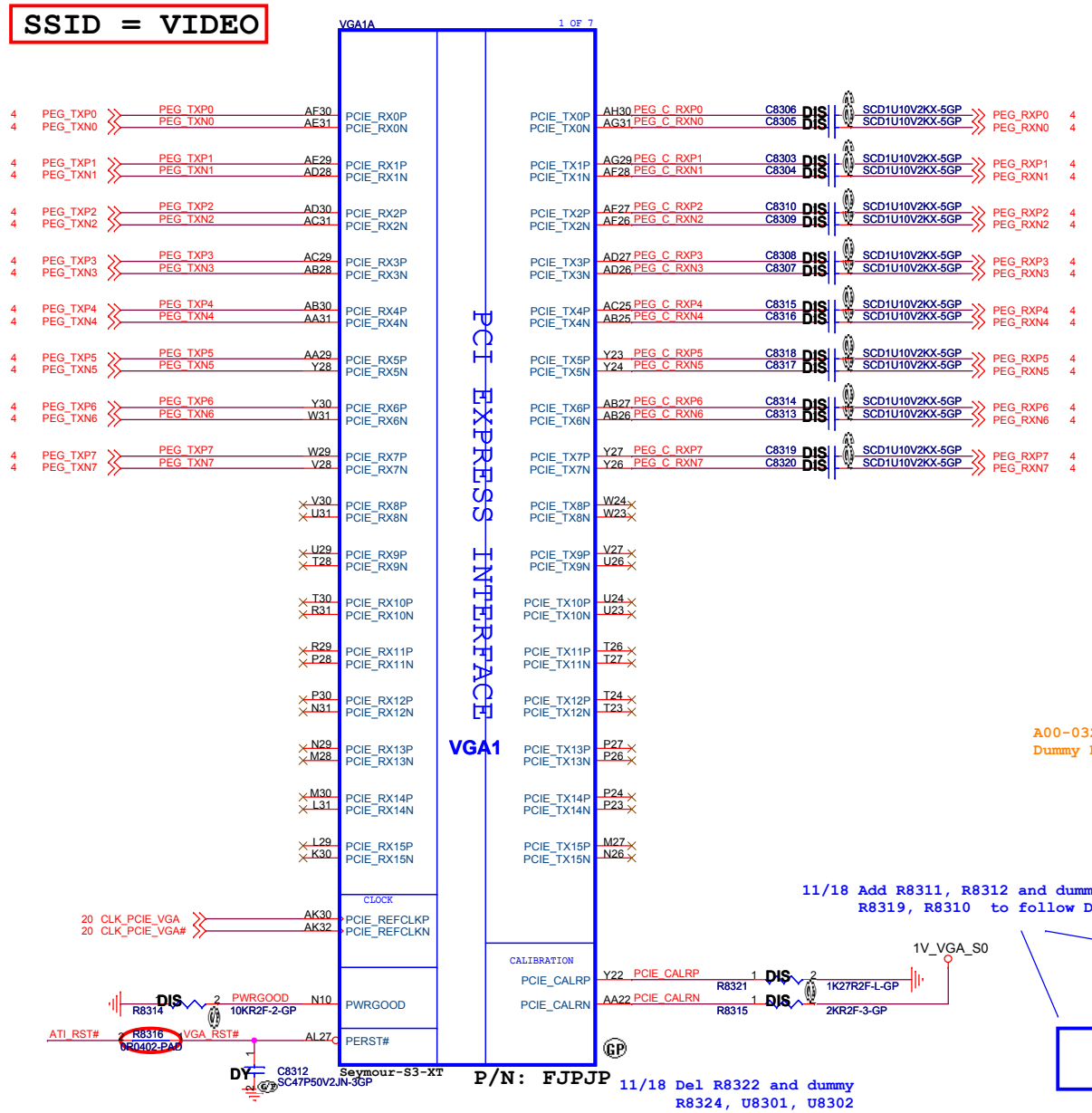
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 82 of 105

SSID = VIDEO



P/N: FJPJP

11/18 Del R8322 and dummy R8324, U8301, U8302

11/18 Add R8311, R8312 and dummy R8319, R8310 to follow DN13

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMEND	PLATFORM SETTING
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: Full Tx output swing	X	1
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0:Tx de-emphasis disabled 1:Tx de-emphasis enabled	X	1
BIF_GEN2_EN_A	GPIO2	0:Advertises the PCIe device as 2.5GT/s capable at power on. 1:Advertises the PCIe device as 5.0GT/s capable at power on.	0	0
GPIO5_AC_BATT	GPIO5	optional input allow the system to request a fast power reduction by setting GPIO5 to low.	?	0
GPIO8_ROMSO	GPIO8	RESERVED	0	0
VGA_DIS	GPIO9	0:VGA Controller capacity enabled 1:The device won't be recognized as the system's VGA controller	0	0
ROMIDCFG[2:0]	GPIO[13:11]	BIOS_ROM_EN=1, Config[2:0] defines the ROM type BIOS_ROM_EN=0, Config[2:0] defines the primary memory aperture size	X X X	0 0 1 (256MB)
GPIO21_BB_EN	GPIO21	RESERVED	0	0
BIOS_ROM_EN	GPIO_22_ROMCSB	0:Disable external BIOS ROM device 1:Enable external BIOS ROM device	X	0
VIP_DEVICE_STRAP_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver that it sense whether or not a VIP device is connected on the VIP Host interface.	X	0
RSVD	H2SYNC	RESERVED	0	0
RSVD	GENERICC	RESERVED	0	0
AUD[1]	HSYNC	AUD[1:0]:11-Audio for both DisplayPort and HDMI	X	1
AUD[0]	VSYNC		X	1

2010/06/11

PIN STRAPS

3D3V_VGA_S0

A00-0322
Dummy R8302 for disable de-emphasis

2010/06/11
Need to check

85 TX_PWRS_ENB R8301 DIS 3KR2J-2-GP
85 TX_DEEMPH_EN R8302 DY 3KR2J-2-GP (2010/07/13 Stuff for 5.0GT/S)
85 BIF_GEN2_EN_A R8303 DIS 10KR2J-3-GP
85 GPIO8_ROMSO R8304 DY 10KR2J-3-GP
85 VGA_DIS R8305 DY 10KR2J-3-GP
85 CONFIG0 R8306 DIS 10KR2J-3-GP
85 CONFIG1 R8307 DY 10KR2J-3-GP
85 CONFIG2 R8308 DY 10KR2J-3-GP
50,85 VGA_CRT_VSYNC R8309 DY 10KR2J-3-GP
50,85 VGA_CRT_HSYNC R8310 DY 10KR2J-3-GP
85 VSYNC_DAC2 R8311 DY 10KR2J-3-GP
85 HSYNC_DAC2 R8312 DY 10KR2J-3-GP
85 BIOS_ROM_EN R8313 DY 10KR2J-3-GP
85 GPIO5_AC_BATT R8318 DY 10KR2J-3-GP
85 GPIO21_BB_EN R8317 DY 10KR2J-3-GP

3D3V_VGA_S0

85 JTAG_TMS_VGA R8325 DY 10KR2J-3-GP
R8328 DY 10KR2J-3-GP
84 TESTEN R8327 DIS 5K11R2F-L1-GP
85 JTAG_TRST#_VGA R8326 DY 10KR2J-3-GP
20,85 JTAG_TCK_VGA R8329 DY 10KR2J-3-GP

JTAG SIGNAL OPTION

Signal	Normal mode	Debug mode	pilot run mode
TESTEN	"1"(PU)	"1"(PU)	"0"(PD)
JTAG_TRST#	"0"(PD)	"1"(PU)	NC
JTAG_TCK	CLK	"1"(PU)	NC
JTAG_TMS	"1"(PU)	"1"(PU)	NC

11/2 change to 1D5V_VGA_PWOK

85 1D5V_VGA_PWOK R8330 DY 0R2J-2-GP
93 1D8V_S0_VGA_PG R8324 DY 0R2J-2-GP
PLT_RST# R8323 DY 0R2J-2-GP ATI_RST#
1D8V_S0_VGA_PG_R
C8311 DY SCD1U10V2KX-4GP
U8301 74LVC1G08GW-1-GP 73.01G08.L04 2ND =
3D3V_VGA_S0
U8301_Y
5,18,27,31,65,71 PLT_RST#

X02-0311 Change R8316, R8331 to short pad

18 DGPU_HOLD_RST# R8331 0R0402-PAD
U8302 74LVC1G08GW-1-GP 73.01G08.L04 2ND =
3D3V_VGA_S0
ATI_RST# ATI_RST# 85

PE_GPIO0	
dGPU mode	H
IGPU	L
IGPU with BACO	H

<Core Design>

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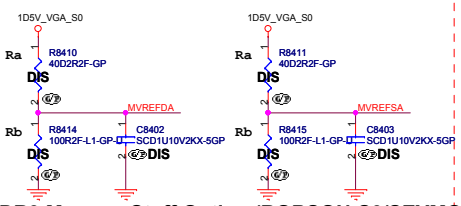
Title: GPU_PCIE/STRAPPING(1/5)
Size: A3 Document Number: Enrico Caruso 14 Rev: A00
Date: Wednesday, April 13, 2011 Sheet 83 of 105

SSID = VIDEO

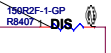
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

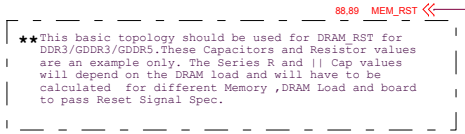


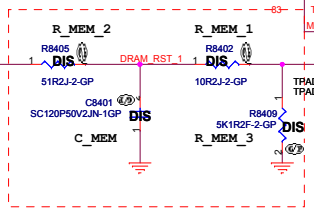
DDR3/GDDR3 Memory Stuff Option (ROBSON-S3/SEYMOUR-XT-S3)

	DDR5	DDR3
MVDDQ	1.5V	1.5V/1.8V
Ra	40.2R	40.2R
Rb	100R	100R

DPC_CALR (Park/Robson-S3):
Analog calibration.
Connect DPxx_CALR to GND through a 150- (1%)
resistor.

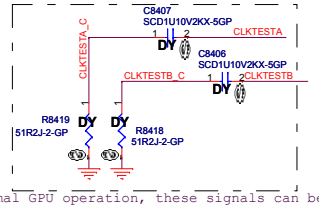






Designator	For SEYMOUR	For Robson
R_MEM_1	10R	10R
R_MEM_2	50R	50R
R_MEM_3	5K	5K
C_MEM	120pF	120pF

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except R_MEM_2



For normal GPU operation, these signals can be left floating (do not populate the capacitors and resistors).

11/16 change part reference to R8441 and stuff

11/18 move R8441 before R8440

2010/07/06
Schematics check list:
A pull-down resistor is required.

P/N: FJPJP

DN15ATI Whistler

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Title: GPU Memory(2/5)

Size: Custom | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 84 of 105

MEMORY ID Table

DVPDATA[3:0]	Description
0000	DDR3 SAMSUNG-K4W1G1646G-BC11(900MHz)64M*16
0001	DDR3 Hynix-H5TQ1G63DFR-11C (900MHz) 64M*16
0010	DDR3 SAMSUNG K4W2G1646C-HC11 (900MHz) 128M*16
0011	DDR3 Hynix-H5TQ2G63BFR-11C (900MHz) 128M*16

DVPDATA[0:3] Default:Pull down

SSID = VIDEO

For Seymour,
DPC_PVDD is DPC_VDD18 2010/06/11
DPC_PVSS and all DPC_VSSR are DP_VSSR

0923 Modify for DV14 Config

MEM_ID Control

2010/06/11

2010/07/07 Remove TP8517,TP8518,TP8506,TP8519,TP8512

Vendor suggest to reserve test point 09/06

X01: dummy VGA thermal circuit based on DN15

11/18 Del C8529 to follow DN13

12/17 dummy R8523 for panel interface unused.

2010/07/07 Change to RSVD based on DS v3.05

PLACE VREFG DIVIDER AND CAP CLOSE TO ASIC

11/18 Del 27M CLK circuit from PCH

2010/07/06
Schematics check list:
A 1~M ohm resistor must be connected between XTALIN and XTALOUT when a crystal is used.

Change to DY 9/20

Clock Input Configuraiton -GDDR3/DDR3
a) 27MHz crystal connected to XTALIN or XTALOUT or
b) 27MHz (1.8V) oscillator connected to XTALIN or
c) 27MHz (3.3V) oscillator connected to XO_IN (Park, Madison, and Broadway only)

11/2 Stuff X8501, R8502
C8524, C8525

11/29 change X8501 to 82.30034.641

12/20 NC R-,G-,B- on SSI and try to co-layout with Rosbson in PT stage

12/20 Add R8504 for Robson.

12/9 chnage R8501 to ROB

0820

0723 Add SMBUS

AUXP PD 100K
AUXN PD 100K
Draw on EDP circuit page

12/16 change R8507, R8505 and R8513 to ROB

Modified 9/1

P/N: FJPJP

LVDS Interface

P/N: FJPJP

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Title: GPU_DP/LVDS/CRT/GPIO(3/5)
Size: A2 | Document Number: Enrico Caruso 14 | Rev: A00
Date: Wednesday, April 13, 2011 | Sheet 85 of 105

SSID = VIDEO

12/28 Yellow mark for OPI change

POWER

VGA1

P/N: FJPJP

12/6 remove tp8604, 8605

12/2 change property to EMI for BOM control

12/28 Yellow mark for OPI change

Close to VGA pin R21, U21

X01: add capacity for BIF_VDDC

2010/06/17_1

Rds(on) = 1ow
VGS=0.7~1.5V

AO4468 MAX 3.1A
Rds(on) = 101~155mOhm
VGS=+/-12V

2010/07/08

1D5V_VGA_PWOK

11/18 dummy 1D5V_VGA_PWOK circuit

11/2 change net name to 1D5V_VGA_PWOK

Change polarity , switch pin D and pin S. 9/6

X02-0302 Add R8605, R8609 PU 5V for lower Rdson

X01: modify to DGPU_PWROK

Non-BACO= HIGH
BACO = LOW

	PX_EN	8209A_EN/DEM_VGA	1D5V_VGA_PWOK_R	PX_EN#	PX_EN##
Non-BACO	0	1	1	0	1
BACO	1	0	0	1	0

PX_EN# = High, BIF_VDDC = 1V_VGA_S0
PX_EN## = High, BIF_VDDC = VGA_CORE

12/16 dummy U8605 and stuff R8601 to follow standard schematic.

<Core Design>

Wistron Corporation
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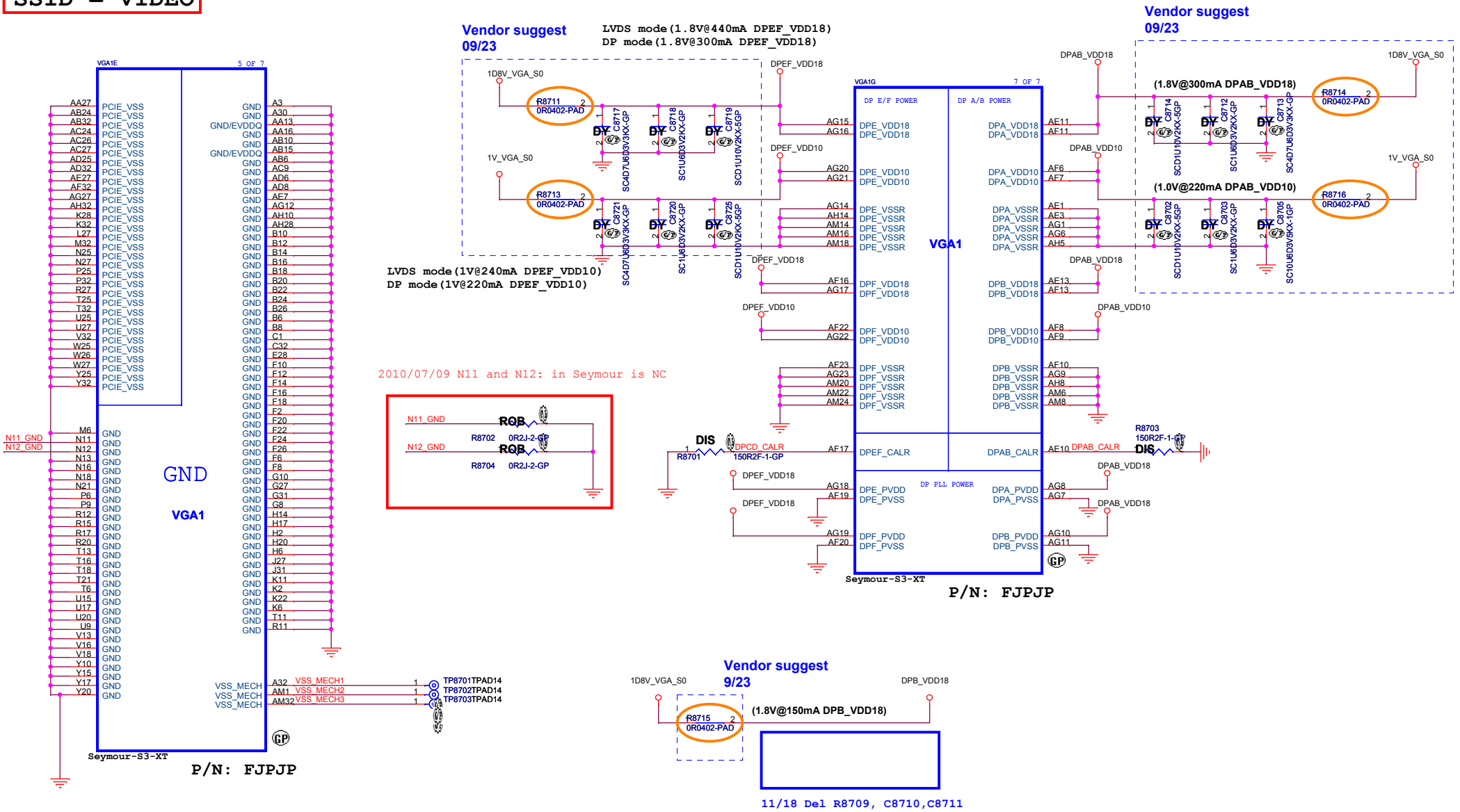
Title: GPU_POWER(4/5)

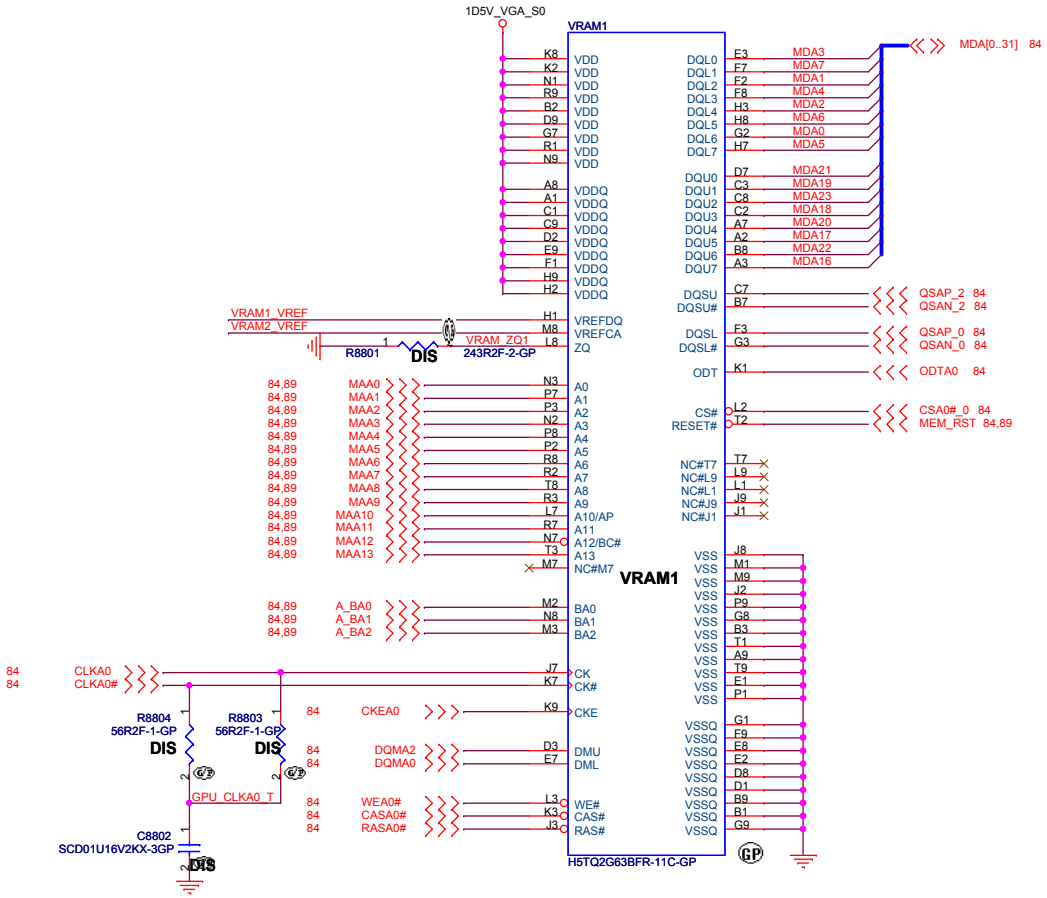
Size: A2 | Document Number: Enrico Caruso 14 | Rev: A00

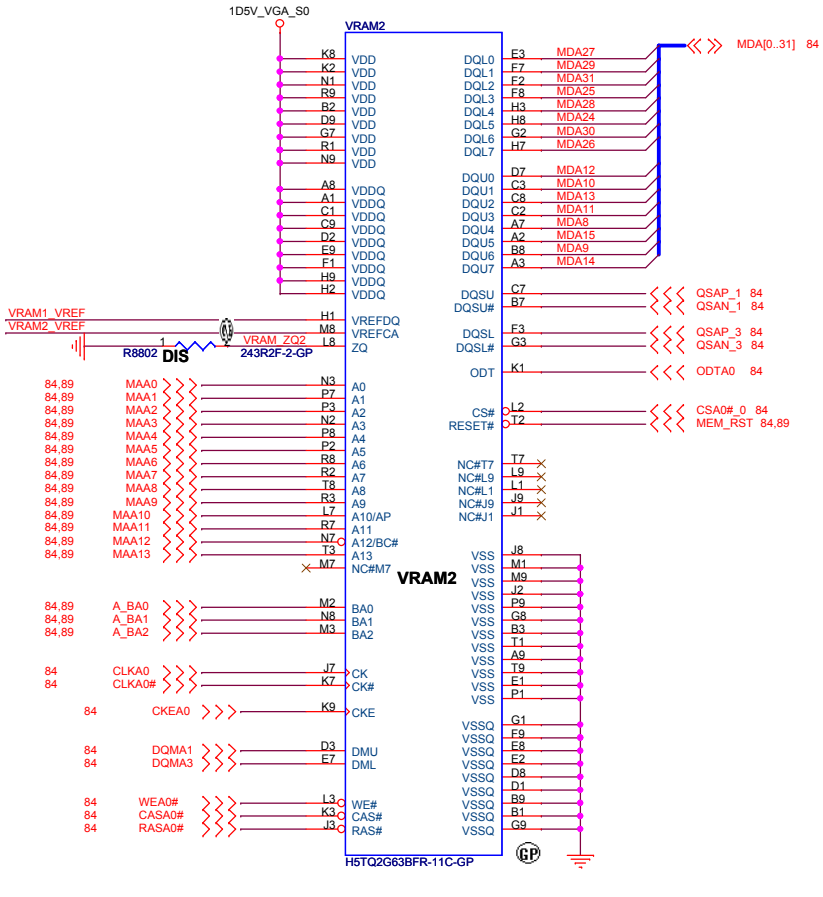
Date: Wednesday, April 13, 2011 | Sheet 86 of 105

SSID = VIDEO

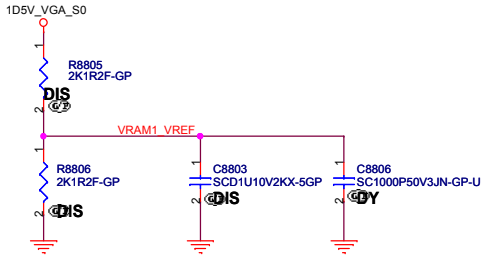


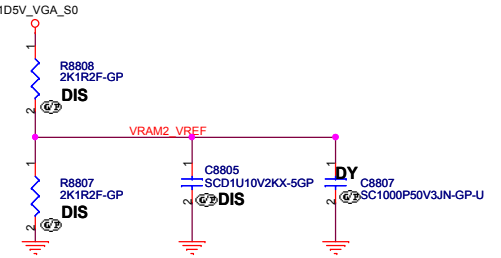
SSID = VIDEO





X01-0211 change VRAM symbol for layout (larger package)





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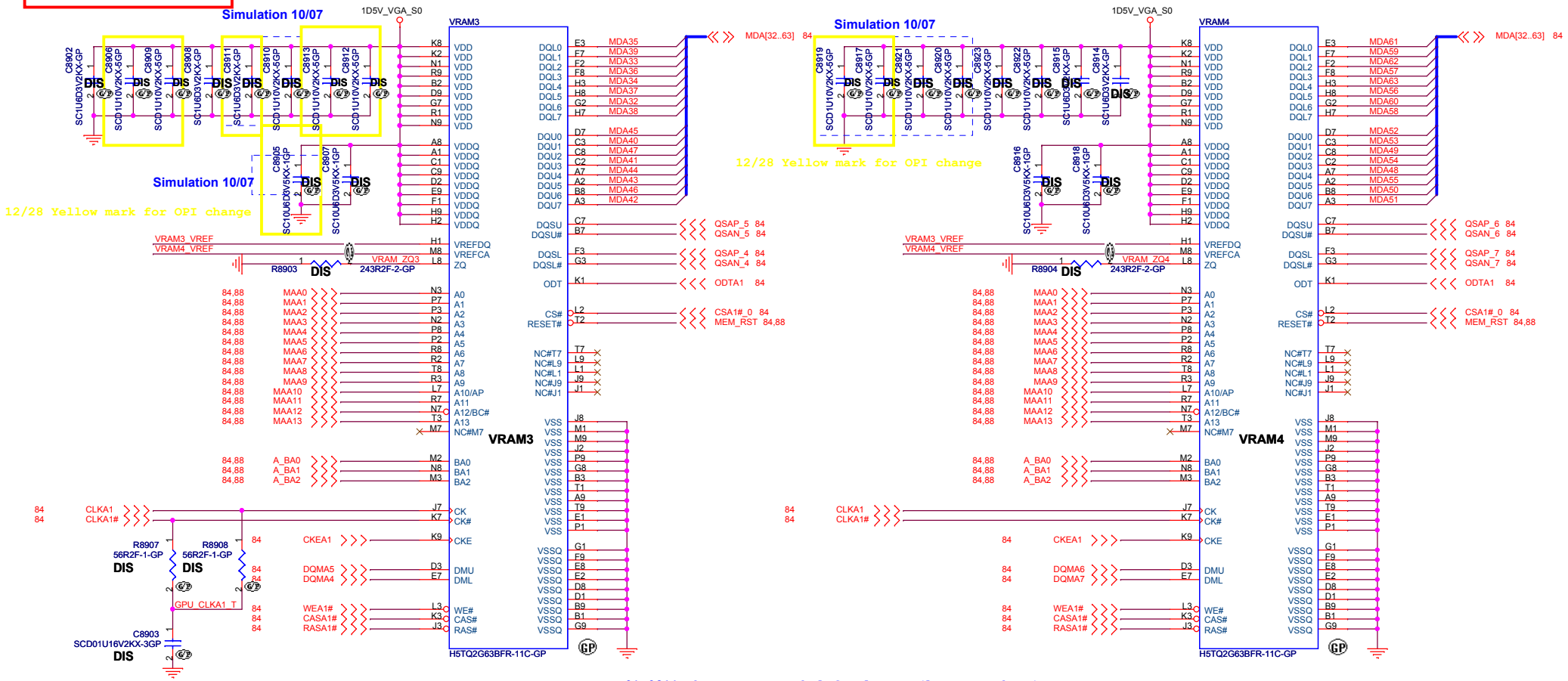
Title: GPU-VRAM1,2 (1/4)

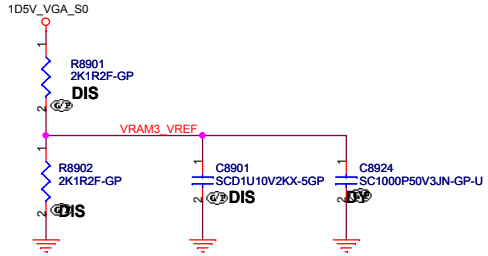
Size: Custom | Document Number: Enrico Caruso 14 | Rev: A00

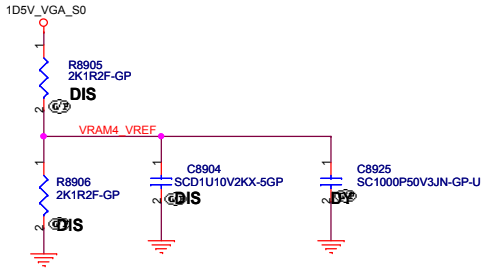
Date: Wednesday, April 13, 2011 | Sheet 88 of 105

SSID = VIDEO



X01-0211 change VRAM symbol for layout (larger package)





DN15ATI Whistler

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size: Custom | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 89 of 105

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DN15ATI Whistler

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Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM5,6 (3/4)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 90 of 105

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DN15ATI Whistler

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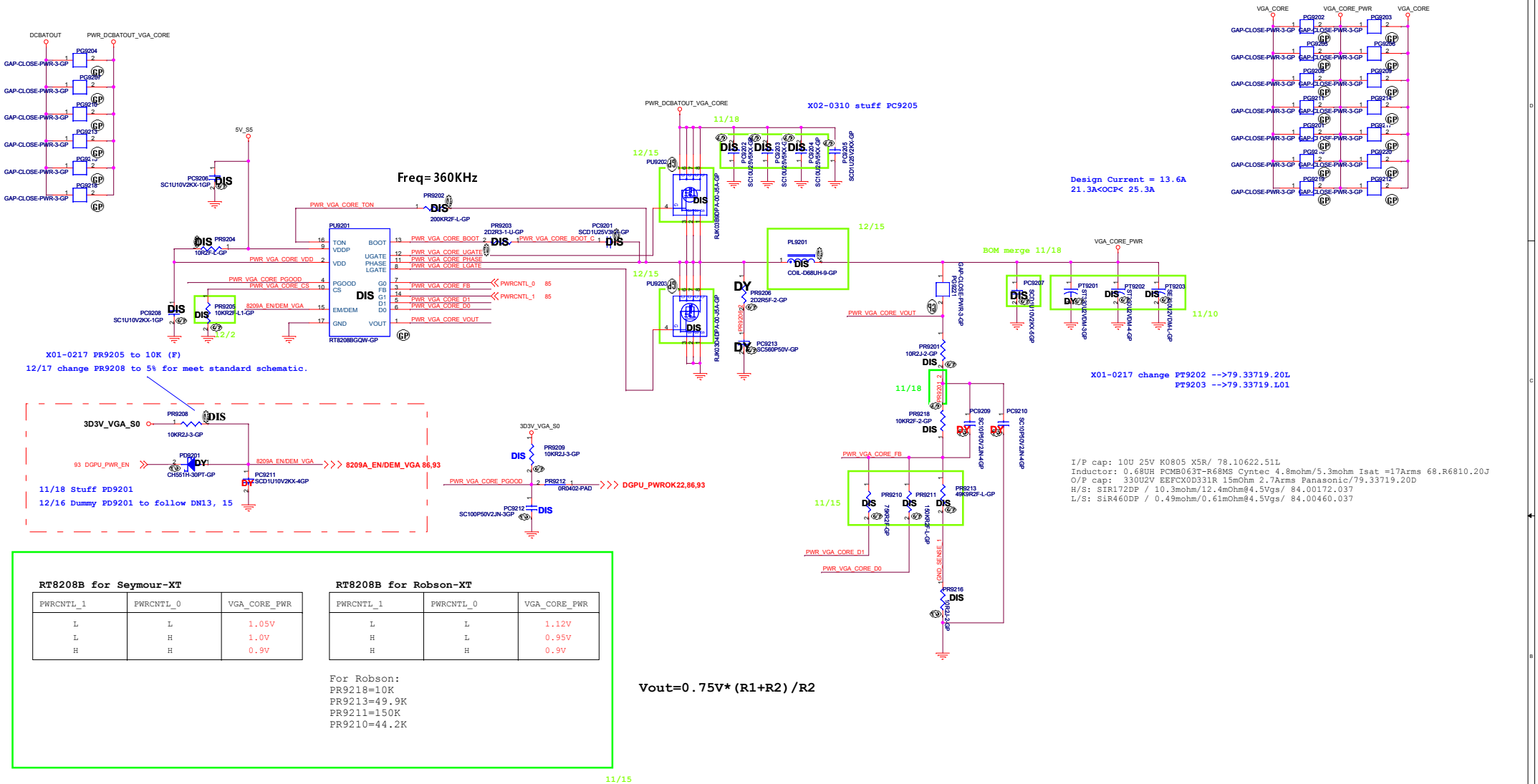
Title: GPU-VRAM7,8 (4/4)

Size: A3 | Document Number: Enrico Caruso 14 | Rev: A00

Date: Wednesday, April 13, 2011 | Sheet 91 of 105

SSID = PWR.Plane.Regulator_VGACORE



RT8208B for Seymour-XT

PWRCNTL_1	PWRCNTL_0	VGA_CORE_PWR
L	L	1.05V
L	H	1.0V
H	H	0.9V

RT8208B for Robson-XT

PWRCNTL_1	PWRCNTL_0	VGA_CORE_PWR
L	L	1.12V
H	L	0.95V
H	H	0.9V

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208B +VGA_CORE

Size: A2 | Document Number: Enrico Caruso 14 | Rev: A00

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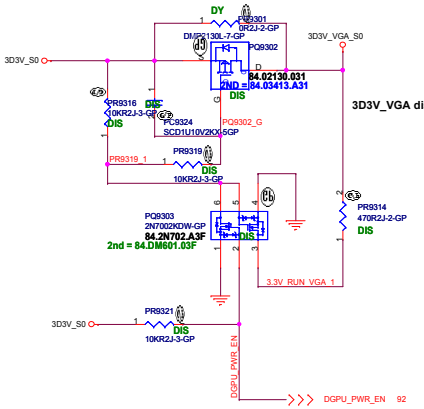
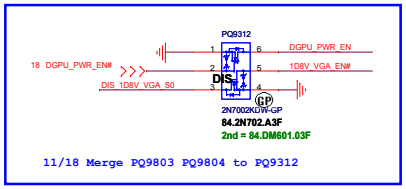
3D3V_S0 to 3D3V_VGA_S0 Transfer

Change DUMMY Reference Name to PX_BACO



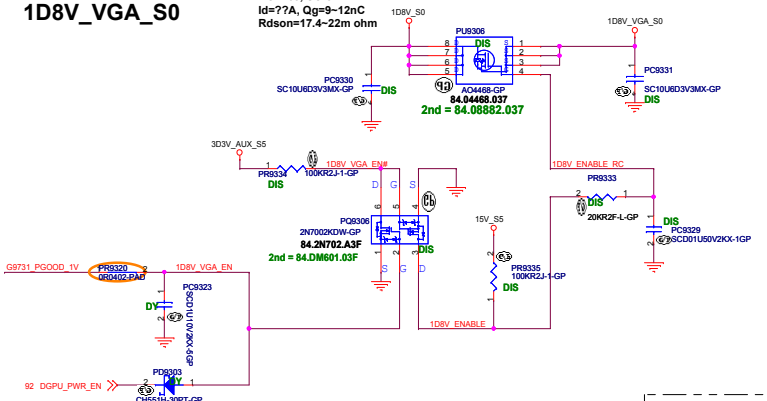
	DGPU_PWR_EN#
dGPU mode	L
IGPU	H
IGPU with BACO	L



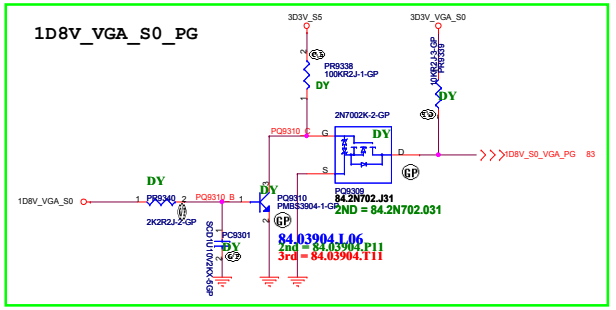
11/18 Merge PQ9803 PQ9804 to PQ9312

1D8V_VGA_S0

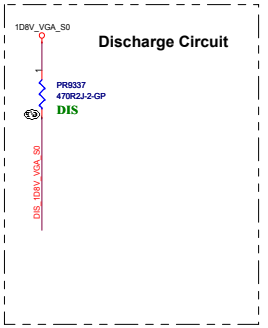
AO4468, SO-8
Id=??A, Qg=9~12nC
Rdson=17.4~22m ohm



1D8V_VGA_S0_PG



Discharge Circuit



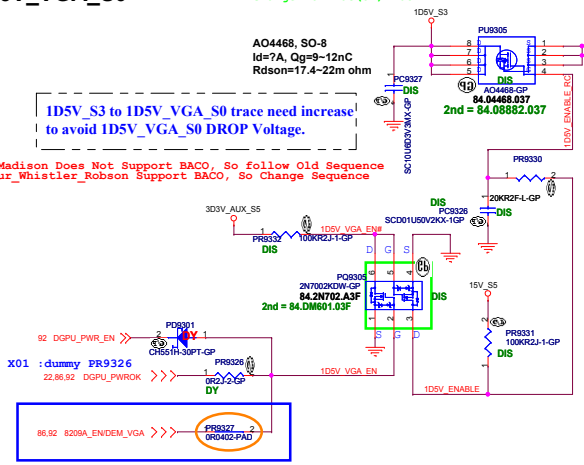
1D5V_VGA_S0

change low Rds(on) MOSFET

AO4468, SO-8
Id=?A, Qg=9~12nC
Rdson=17.4~22m ohm

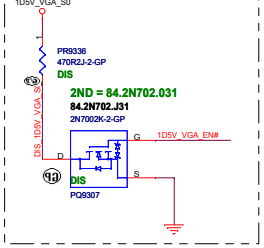
1D5V_S3 to 1D5V_VGA_S0 trace need increase to avoid 1D5V_VGA_S0 DROP Voltage.

Park_Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence



11/18 Add PR9327 for 8209A_EN/DEM_VGA turn on 1D5V_VGA_S0 power.

Discharge Circuit



G9731 for 1V_VGA_S0

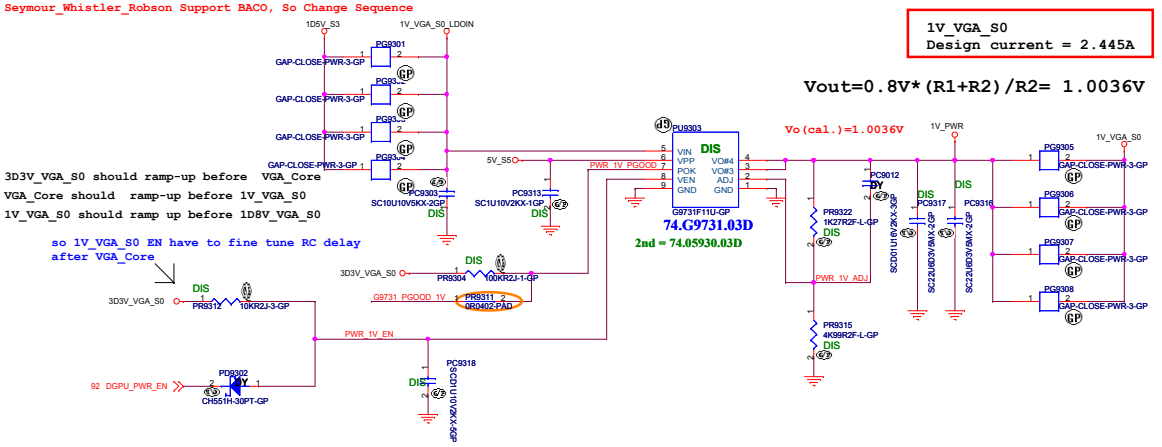
Park_Madison Does Not Support BACO, So follow Old Sequence
Seymour_Whistler_Robson Support BACO, So Change Sequence

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1V_VGA_S0
1V_VGA_S0 should ramp up before 1D8V_VGA_S0

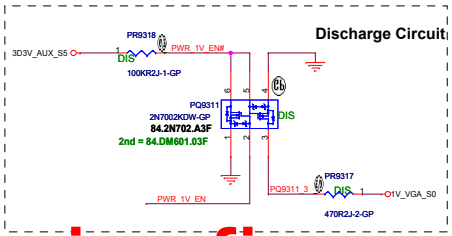
so 1V_VGA_S0 EN have to fine tune RC delay after VGA_Core

1V_VGA_S0
Design current = 2.445A

Vout=0.8V*(R1+R2)/R2= 1.0036V



Discharge Circuit



<Core Design>

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Title: DISCRETE VGA POWER

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Title: *LVDS_Switch*		
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(Blanking)

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Title	CRT_Switch
Size: A3	Document Number: Enrico Caruso 14
Rev	A00
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SSID = SDIO

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Title: TOUCH PANEL

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SSID = Mechanical

H1 HT85BE85R29-U-5-GP
H2 HOLE256R115-GP
H3 HT85BE85R29-U-5-GP
H4 HT85BE85R29-U-5-GP
H5 HT85BE85R29-U-5-GP
H6 HT85BE85R29-U-5-GP
H7 HT85B95X975R29-S-GP

X01-0208 stuff SPR1 and add SPR2

SPR1 SPRING-62-GP 34.39S07.003

A00-0406 dummy SPR2
SPR2 SPRING-58-GP 34.4B312.002
X02-0314 stuff SPR2

12/17 add SPR1 for EMI
12/21 change SPR1 to 34.4B312.002
12/22 change SPR1 to 34.39S07.003

X01-0211 change SPR2, SPR3 to 34.4B312.002
X01-0210 add SPR3

SPR3 SPRING-58-GP 34.4B312.002

SPR4 SPRING-13-GP-U 34.43E24.001
SPR5 SPRING-13-GP-U 34.43E24.001
X01-0211 add SPR4, SPR5

For CPU BRACKET
H8 HOLE197R166-1-GP
H9 HOLE197R166-1-GP
H10 HOLE197R166-1-GP

VGA Stand-Off
H11 STF237R117H83-1-GP DIS

PCH Stand-Off
H12 STF217R113H162-GP
H13 STF237R117H83-1-GP DY

A00-0412 dummy H12, H13 for remove PCH Heatsink
A00-0413 change H12 to 34.4HL17.001

12/2 Delete SPR1, SPR2

DCBATOUT
EC9701 EC9702 EC9703 EC9704 EC9705 EC9706 EC9707 EC9708 EC9709 DY EC9710 DY EC9711 DY EC9712 DY EC9713 EC9714 EC9715 EC9716 EC9717 EC9718 DY EC9719
SCD1U25V2KX-GP

5V_S5
X02-0314 stuff EC9722
EC9720 DY EC9721 DY EC9722 DY EC9723 EC9724 EC9725 DY EC9726
SCD1U25V2KX-GP

PWR_3D3V_DCBATOUT
EC9727
SCD1U25V2KX-GP
12/15 Stuff EC9727

3D3V_S5
EC9728
SCD1U25V2KX-GP

1D5V_S3
EC9729 DY EC9730 DY EC9731
SCD1U25V2KX-GP

VCC_GFXCORE
EC9732
SCD1U25V2KX-GP

VCC_CORE
EC9733 EC9734 EC9735 EC9736 EC9737
SCD1U25V2KX-GP

1D05V_VTT
EC9738 EC9739
SCD1U25V2KX-GP

5V_S5
EC9740
SCD1U25V2KX-GP
3D3V_S5

BT+
EC9741
SCD1U25V2KX-GP
12/17 Add EC9741

12/6 Add EMI capacities
12/20 change EMI caps to 0402 package

EC9742 DY EC9743 DY EC9744 DY EC9745 DY EC9746
SCD1U10V2KX-5GP
AUD_AGND
X01-0208 add EC9742~EC9746

<Core Design>

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Title: UNUSED PARTS/EMI Capacitors
Size: A3
Document Number: Enrico Caruso 14
Rev: A00
Date: Wednesday, April 13, 2011
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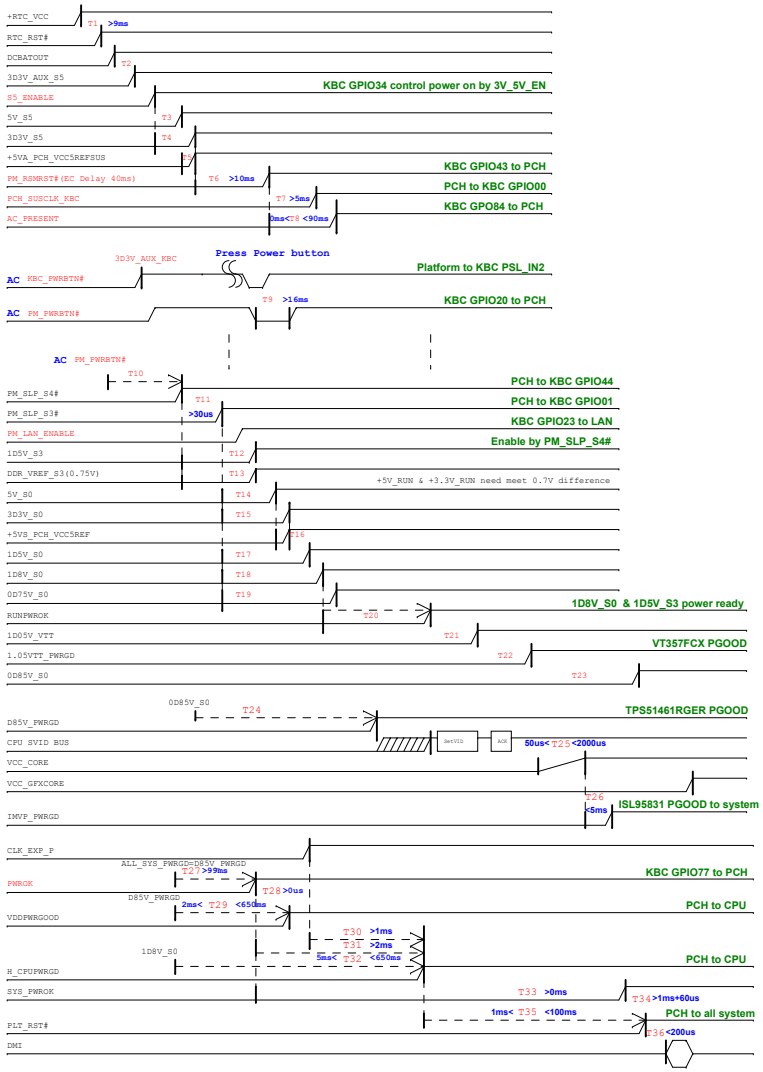
Huron River Platform Power Sequence

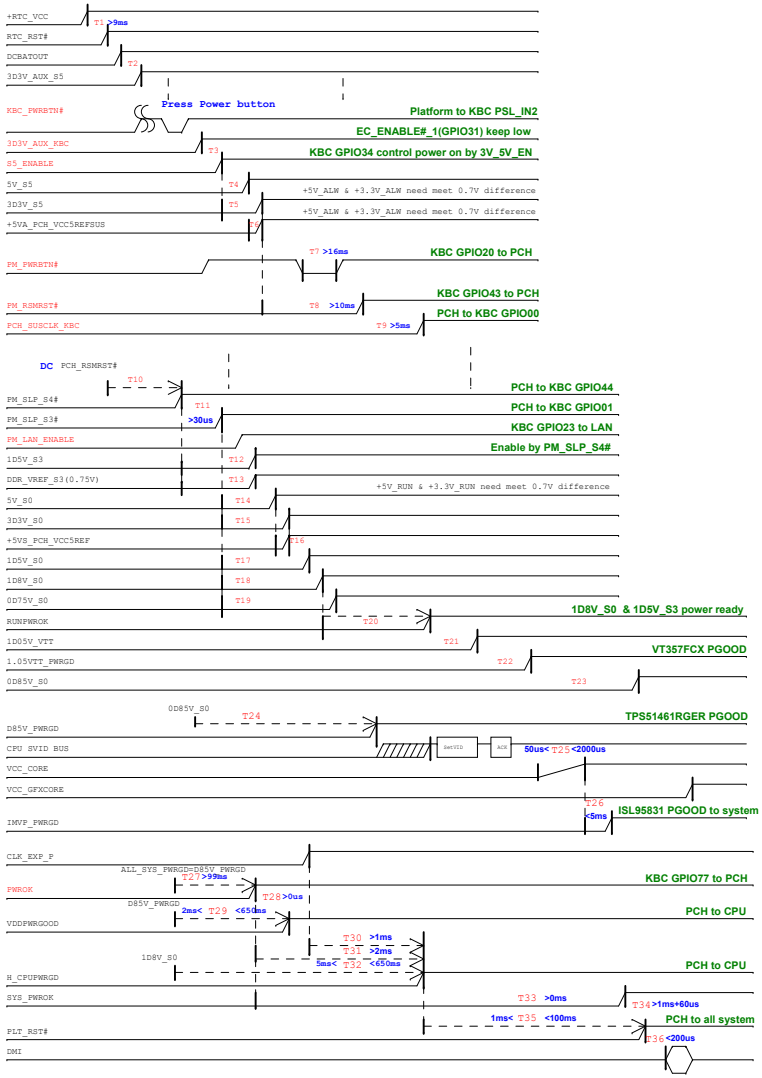
(AC mode)

red word: KBC GPIO

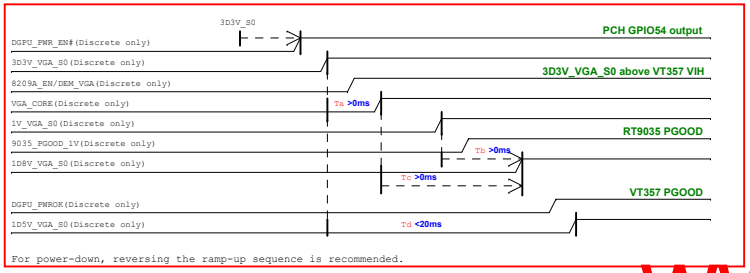


(DC mode)

red word: KBC GPIO



Robson XT Power-Up/Down Sequence



For power-down, reversing the ramp-up sequence is recommended.

<Core Design>
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Title: Power Sequence
Size: A1 | Document Number: Enrico Caruso 14 | Rev: A00
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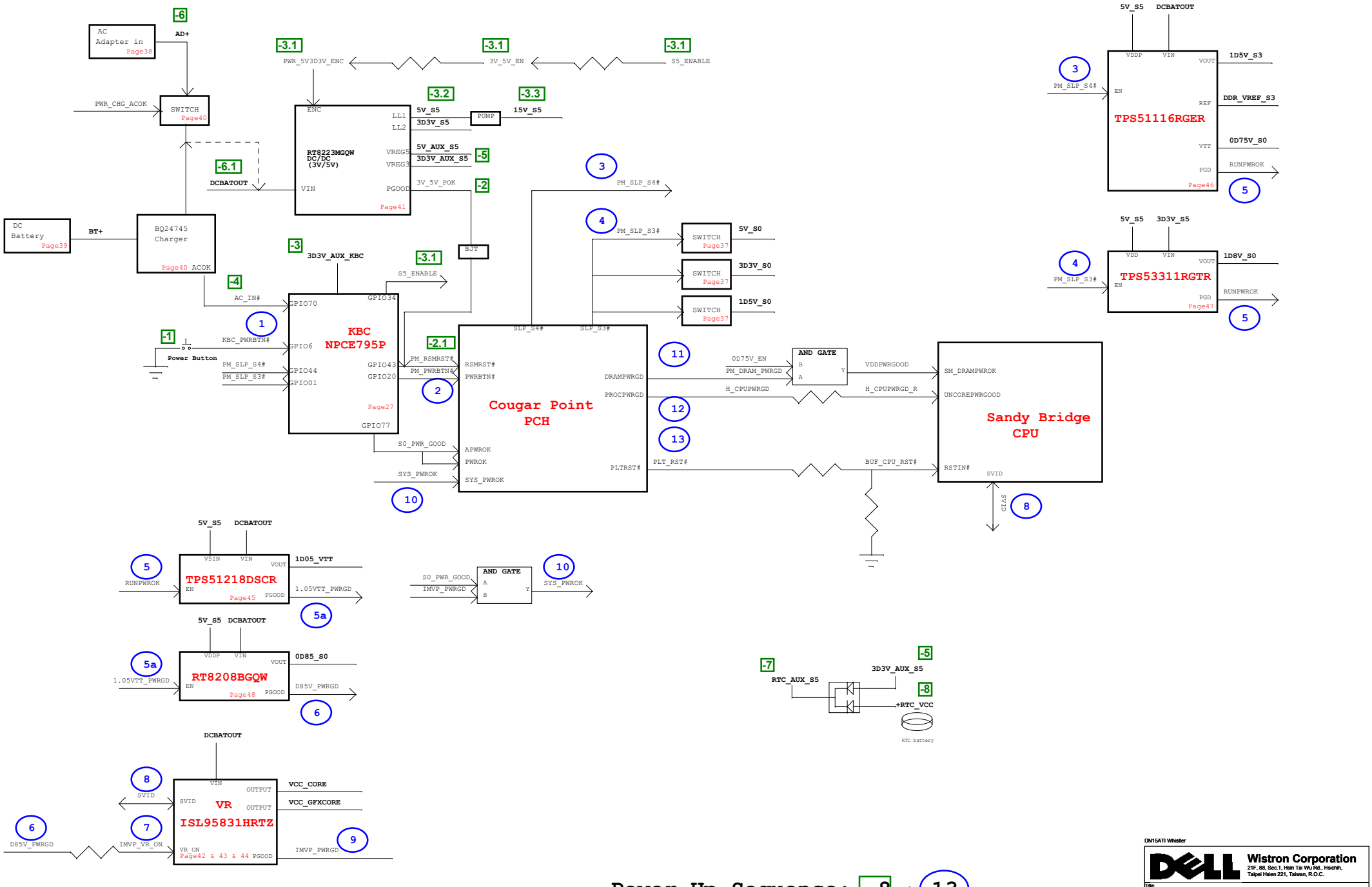
Wistron HURON RIVER POWER UP SEQUENCE DIAGRAM



Power Up Sequence: -8 ~ 13

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Title: Power Sequence Diagram

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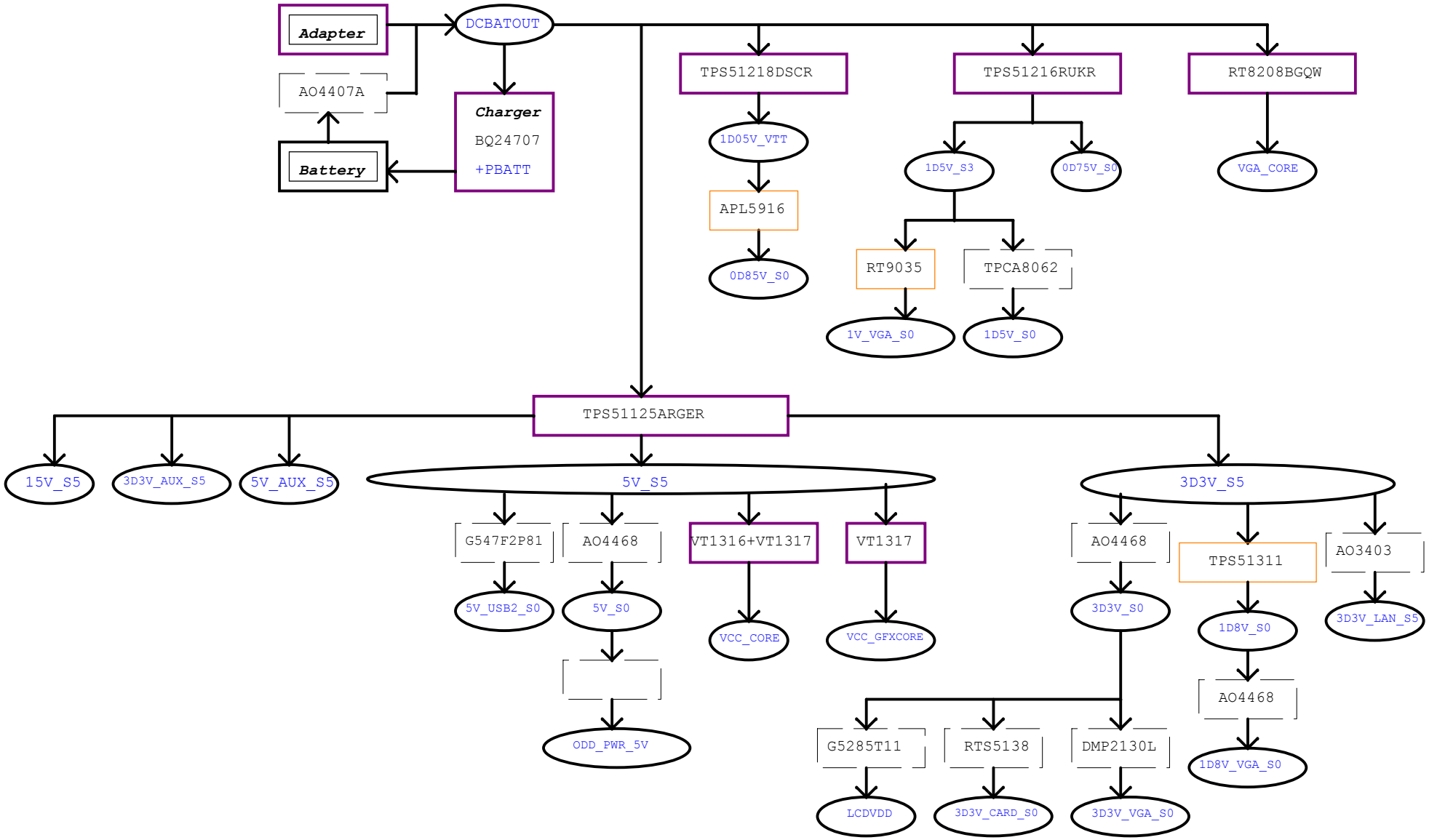

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Title: Power Block Diagram

Size	Document Number	Rev
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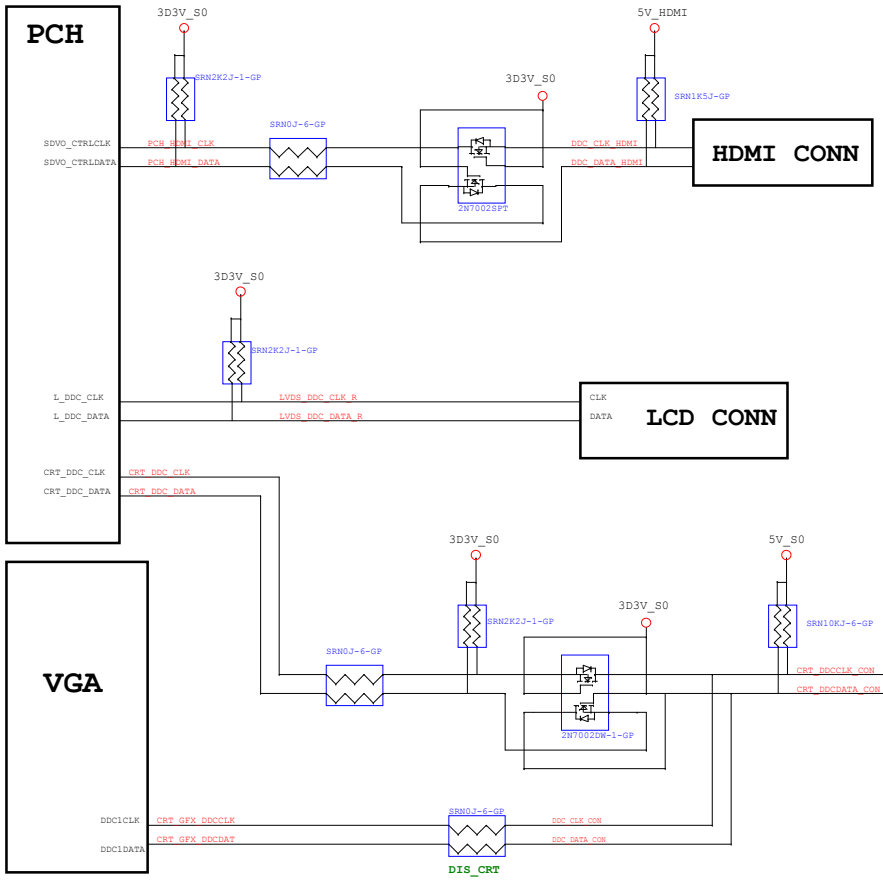
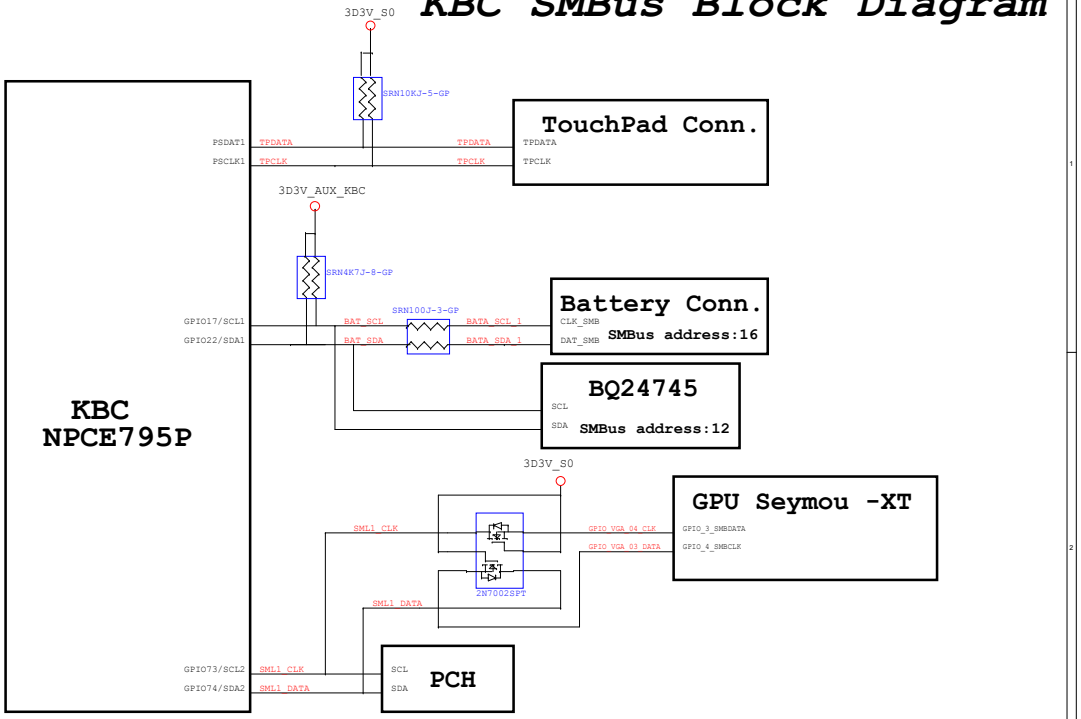
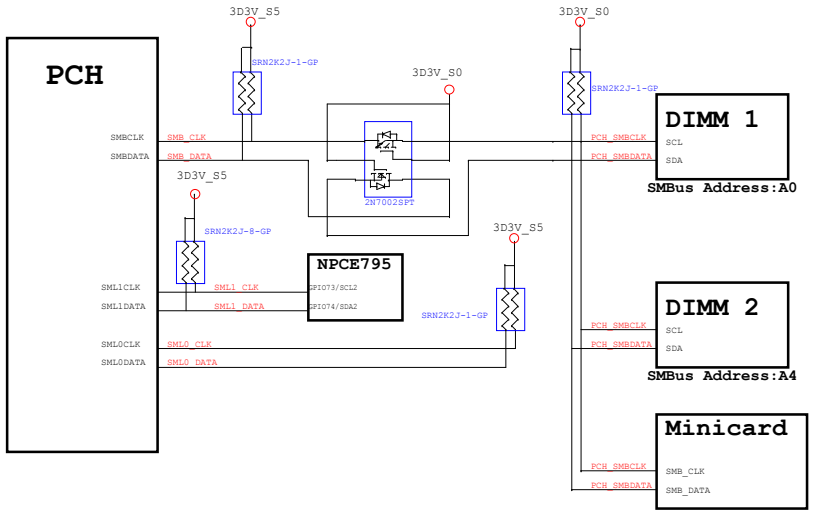
PCH SMBus Block Diagram



KBC SMBus Block Diagram





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Title: SMBUS Block Diagram

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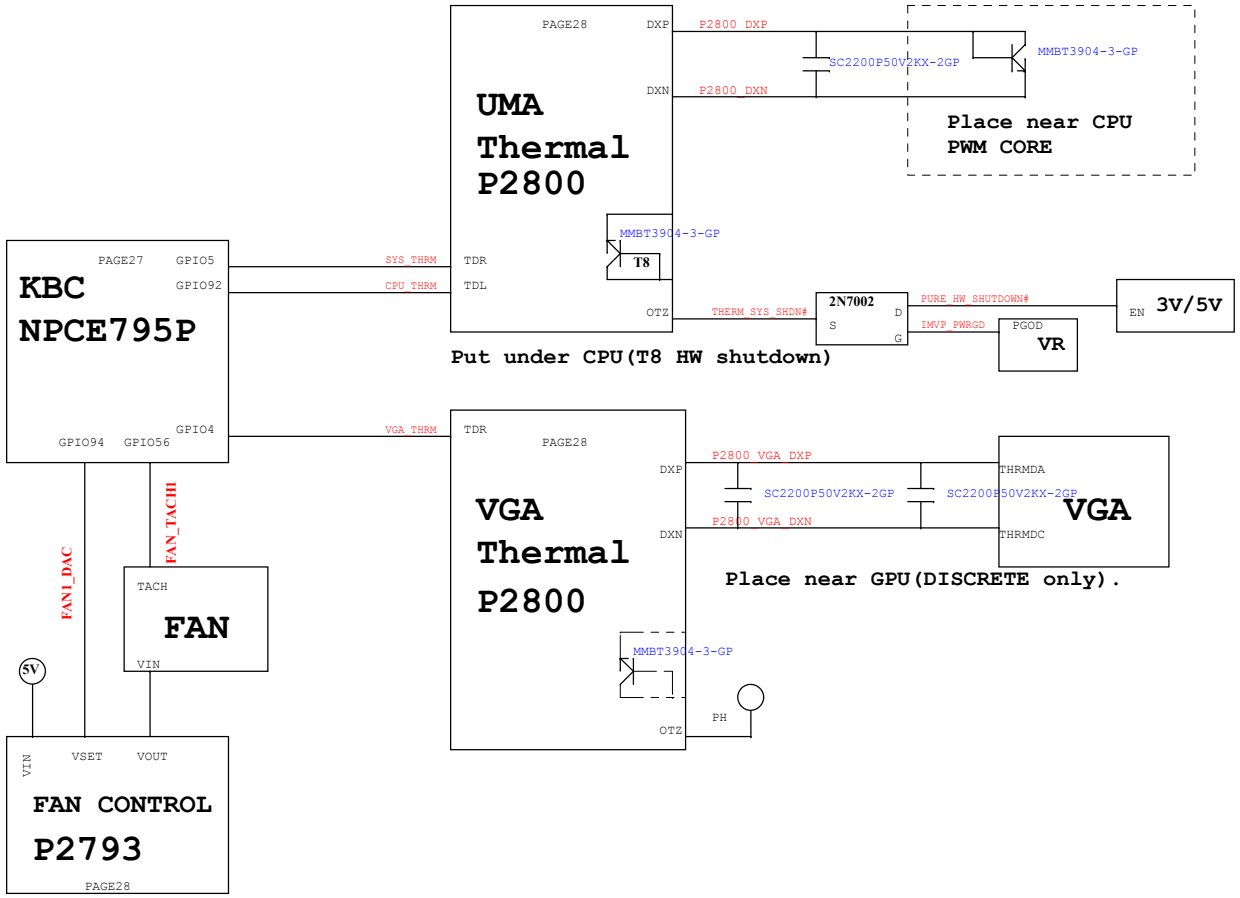
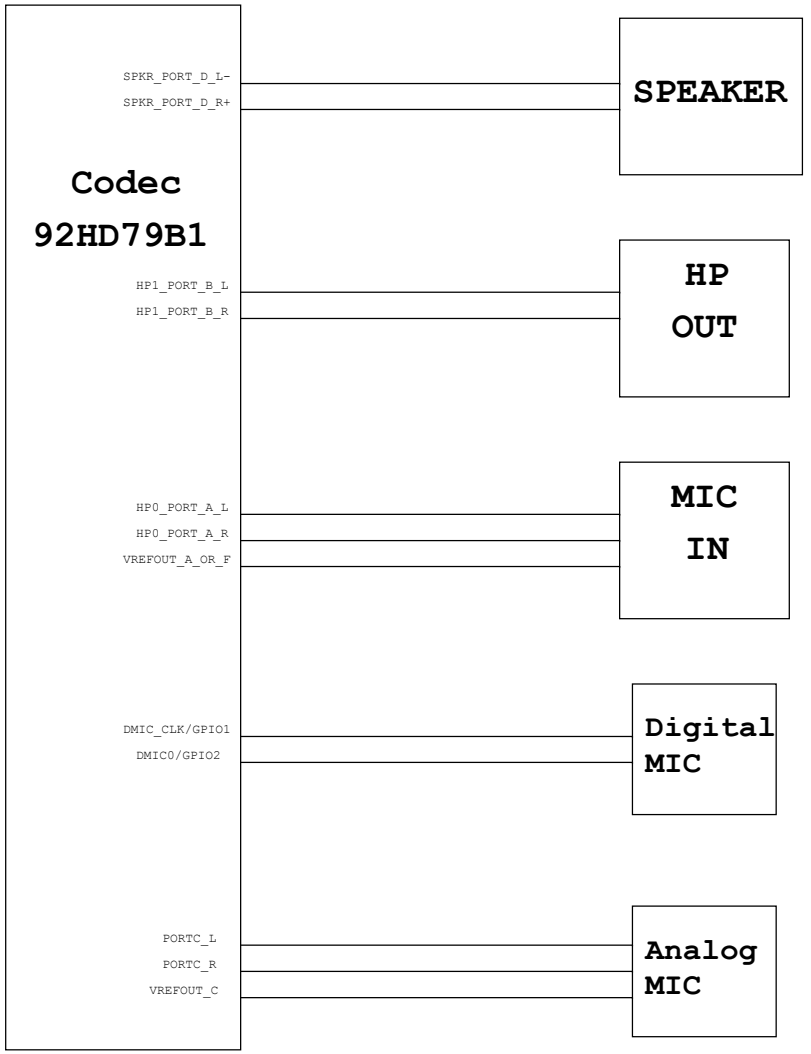
Thermal Block Diagram



Audio Block Diagram



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Title: Thermal/Audio Block Diagram

Size: Custom | Document Number: Enrico Caruso 14 | Rev: A00

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DATA	PAGE	Change Description	Version
12/28	85	dummy VGA thermal circuit	X01
12/28	86	modify to DGPU_PWROK	X01
12/28	86	add capacity for BIF_VDDC	X01
12/28	93	dummy PR9326	X01
1/14	93	modify CS#, WP#	X01
1/27	5	Add C504 for noise couple.	X01
1/27	8	Stuff C812, C822, C831, C834 for VCC core noise issue.	X01
1/27	27	Del R2757 to follow standard 10mW circuit	X01
1/27	31	change Q3101 base power rail for leakage issue.	X01
1/27	40	X01-0127 DY PQ4007, PR4038, PR4039 for new version BQ24707	X01
2/8	21	Add RN2101, R2127 for LPC EA result	X01
2/8	27	Dummy R2769	X01
2/8	50	change R5002, R5003 to 33R	X01
2/8	69	TPAD1 to 20.K0464.004	X01
2/8	27	change R5002, R5003 to 33R	X01
2/8	97	add EC9742~EC9746	X01
2/8	97	stuff SPR1 and add SPR2	X01
2/9	28	dummy U2805 circuit	X01
2/9	46	PT4603 UMA-->220uF DIS-->470uF	X01
2/9	48	dummy PC4809 for BBU result.	X01
2/10	5	Merge R512 R514	X01
2/10	21	change RN2101 to RN2104 RN2105	X01
2/10	27	change R2724 to meet X01 PCB ver	X01
2/10	46	del PT4602	X01
2/10	46	change PC4610 from 0.22uF to 10uF	X01
2/10	97	add SPR3	X01
2/10	21	Merge R5115 R2116	X01
2/11	31	add C3122 for soft-sart	X01
2/11	59	Add EMI solution for Surge	X01
2/11	19,27	Change R1925, R1924, R1906, R1913, R2720, R2758, R2759, R2760 to short-pad	X01
2/14	82	add AFTP8201~8210	X01

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Title: Change History

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DATA	PAGE	Change Description	Version
0212	40	Change charger IC to new version	X01
0302	31	Dummy PCIE_CLK_LAN_REQ# circuit	X02
0302	86	Add R8605, R8609 PU 5V for lower Rdson	X02
0303	14,15,17,18 19,22,23,24 27,29,31,36 37,50,51,68	Change R1404, R1405,R1504, R1503,RN1704, R1807, R1903, R1910, R1912, R2214, R2304, R2305, R2306, R2307, R2404, R2405, R2406, R2409, R2702, R2735,R2762, R2756, R2911,R2914, R2917, R3104, R3115, R3117, R3614, R3710, RN5010, RN5117, R6811, R6813, R6804, R6805 0R to short pad	X02
0309	86	Change AFTP test point to follow DV14 AMD	X02
0310	41,45,92,97	Stuff PC4120, EC4501, PC9205, EC9708, EC9709, EC9714, EC9715, EC9716, EC9717, EC9718, EC9720, EC9724, EC9725, EC9740	X02
0311	28	Add R2816& R2817 to option VGA_THRM and DY the circuit	X02
0311	83	Change R8316, R8331 to short pad	X02
0311	59	Change GDT5901& GDT5902 to GD5901& GD5902	X02
0311	18	dummy R1804	X02
0311	31	add rest circuit to provent leakage.	X02
0311	32	Stuff TR3201 and change symbol to 68.00201.141	X02
0314	38	Del short pad PAD1 to prevent system burn.	X02
0314	97	Stuff SPR2	X02
0314	61,97	Stuff EC9722,C6106	X02
0314	36	Change U3606 footprint.	X02
0315	58	Change MIC2 to 20.F1889.002	X02
0315	88,89	Modify VRAM property PN and footprint	X02
0315	32,59	Modify part reference problem of ER5912& TR3201.	X02
0316	68	Modify WLED1 cirucit for brightness.	A00
0320	31	Change R3118 for LOM power sequence	A00
0320	49	Change TR4901 to 120ohm.	A00
0320	61	Change TR601 120ohm.	A00
0320	68	Change resistor for LED brightness	A00
0320	82	Change TR8201, TR8202 to 120ohm.	A00
0320	83	Dummy R8302 for disable de-emphasis	A00
0329	27	change R2735 to 10R and C2711 to 220p	A00
0329	68	Change R6814 to 10KR	A00
0406	97	Dummy SPR2	A00
0406	32, 49, 61, 65,82	Remove R3206, R3207, R4903, R4904, R6102, R6103, TR6501, R8201, R8202, R8203, R8204 PAD	A00

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Title: Change History

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DATA	PAGE	Change Description	Version
0407	51	remove HDMI common mode choke PAD	A00
0408	49,61,82	Swap TR4901, TR6101, TR8201, TR8202 net for layout	A00
0408	49	Add RN4903 for ESD issue.	A00
0408	56	Add R5606 to pull high 3.3V_S0 and change R5605 pull high to 3.3V_S0	A00
0412	40	Change PR4027 to 19.6K Change PR4029 to 54.9K Change PR4013 to 49.9K	A00
0412	40	Dummy PR4037 and stuff PR4030, PR4032, PQ4005	A00
0412	97	dummy H12, H13 for remove PCH Heatsink	A00
0412	5,28,29,31 50,65,85 84,86,87	Change R504,R2807,R3105, R6505, R6506, R8601,R2902,R2903,R2904,R8440,R8517,R8711,R8713,R8714,R8715,R8716,RN2010,RN2012,RN2014,RN2016,,RN5007,RN5008 to short-PAD	A00
0412	21,29	Change ER2111,ER2930 to short-PAD	A00
0412	41,42,45 46,47,48 93	Change PR4121,PR4122,PR4125,PR4217,PR4218,PR4219,PR4220,PR4254,PR4502,PR4607,PR4801,PR4803,PR4711,PR9311,PR9320,PR9327,PR4712 to short-PAD	A00
0413	97	change H12 to 34.4HL17.001	A00
0413	27	change R2724 to 47K for PCB ver	
0413	68	change R6806, R6812, R6801, R6808 to 330ohm	
0413	41,,45,47 89,93	Change close-GAP to green cover-GAP	
0413	28	update P2800 thermal option.	
0413	20	SWAP RN2014 net for layout	

Title <Title>

Size A3 | Document Number <Doc> | Rev A00

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