

# ACLU1&ACLU2

(G40-70 & G50-70)

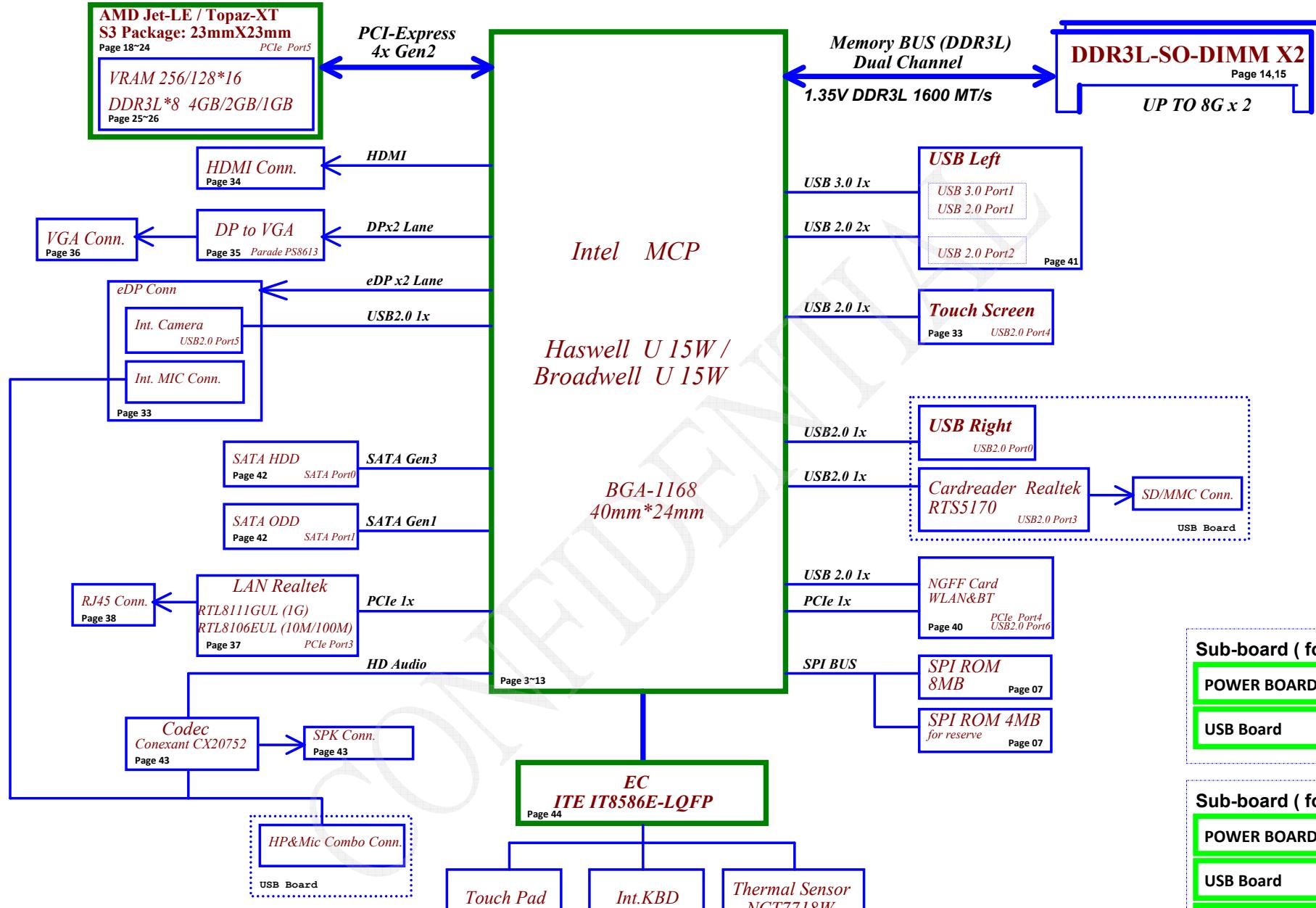
NM-A271 Rev 1.0 Schematic

Intel Haswell/Broadwell U-Processor with DDRIIIIL + AMD Jet-LE/Topaz-XT GPU

2013-12-17

REV:1.0

Security Classification	LC Future Center Secret Data			Title	Cover Page	LCFC	Rev. 1.0
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**Voltage Rails (O --> Means ON , X --> Means OFF)**

Power Plane State	B+	+3VALW		+3VALW_PCH		+1.35V
		+3VS	+1.5VS	+1.35VS	+1.05VS	
S0	O	O	O	O	O	
S3	O	O	O	O	X	
S3 Battery only	O	O	O	O	X	
S5 S4/AC Only	O	O	O	X	X	
S5 S4 Battery only	O	X	X	X	X	
S5 S4 AC & Battery don't exist	X	X	X	X	X	

**SMBUS Control Table**

	SOURCE	VGA	BATT	IT8586E	SODIMM	WLan	Thermal Sensor	PCH	TP Module	charger
EC_SMB_CK1	IT8586E			V						
EC_SMB_DA1	+3VALW	X	V	+3VALW	X	X	X	X	X	V
EC_SMB_CK2	IT8586E	V		V						
EC_SMB_DA2	+3VS	X		+3VS	X	X	V	V	X	X
PCH_SMB_CLK	PCH			V		V		V		
PCH_SMB_DATA	+3VALW_PCH	X	X	+3VS	+3VS	X	+3VALW_PCH	X	X	

**EC SM Bus1 address**

Device Smart Battery 0X16  
Charger 0001 0010 b

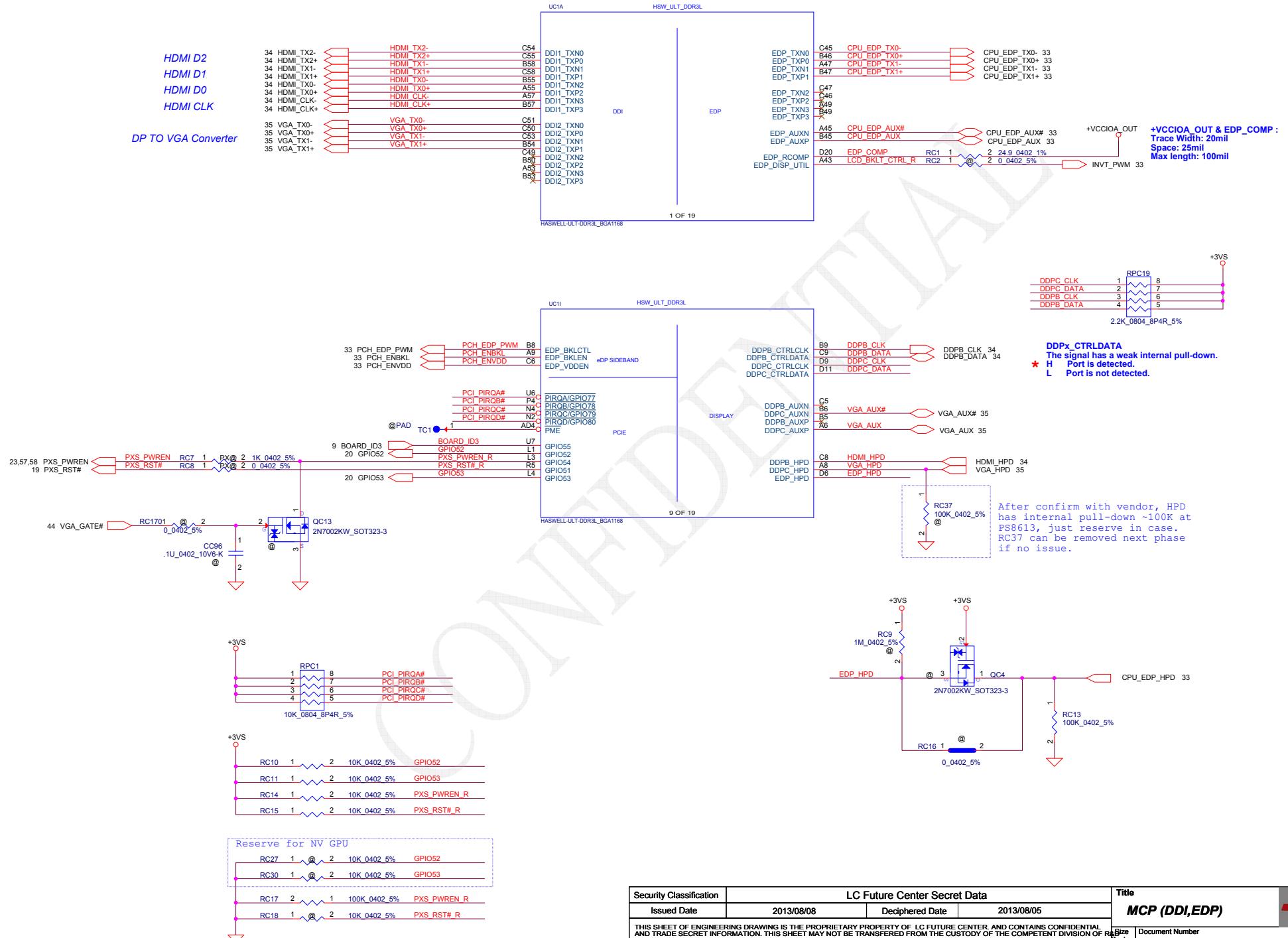
**EC SM Bus2 address**

Device Thermal Sensor NCT7718W  
VGA  
PCH

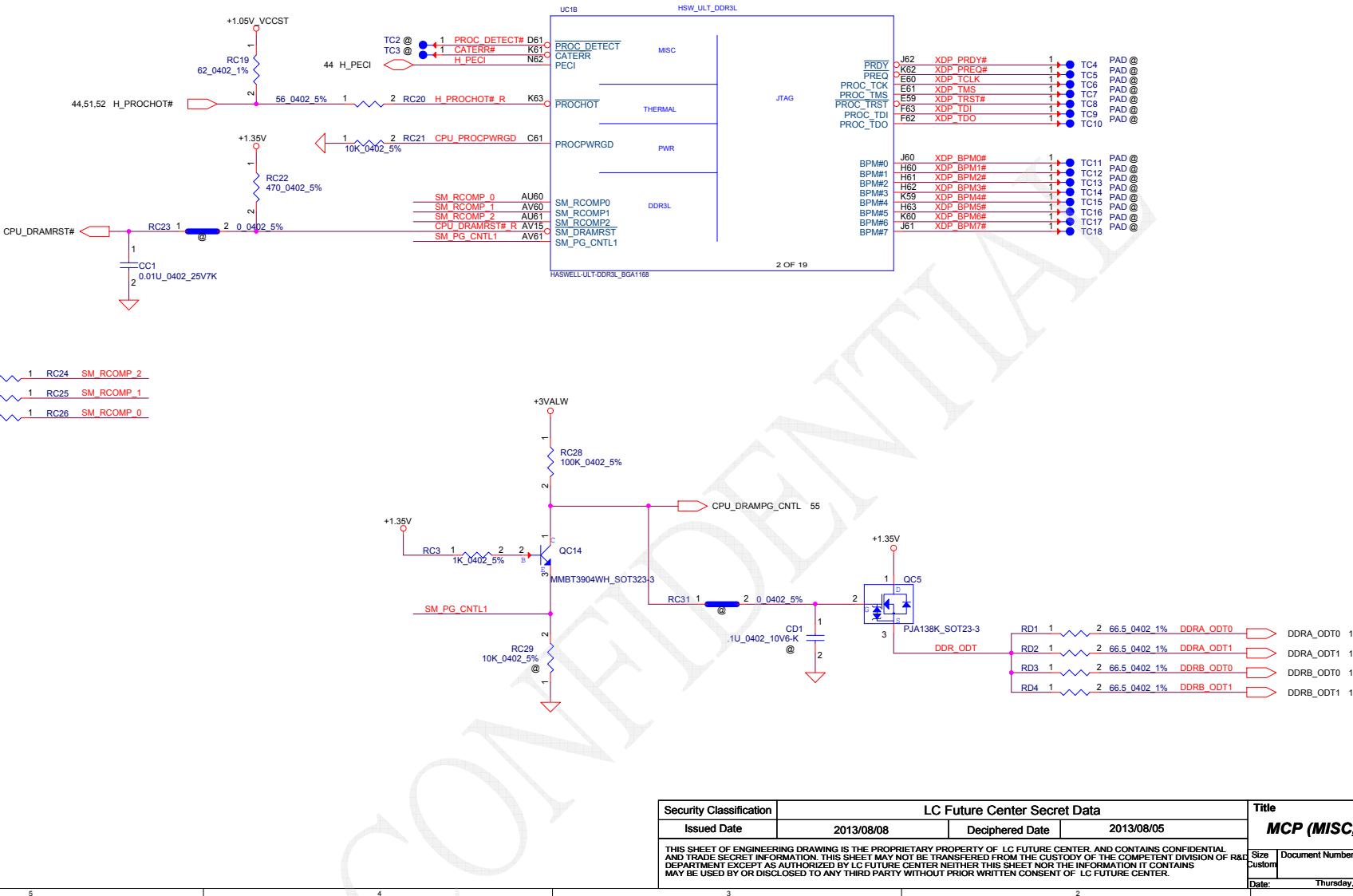
**PCH SM Bus address**

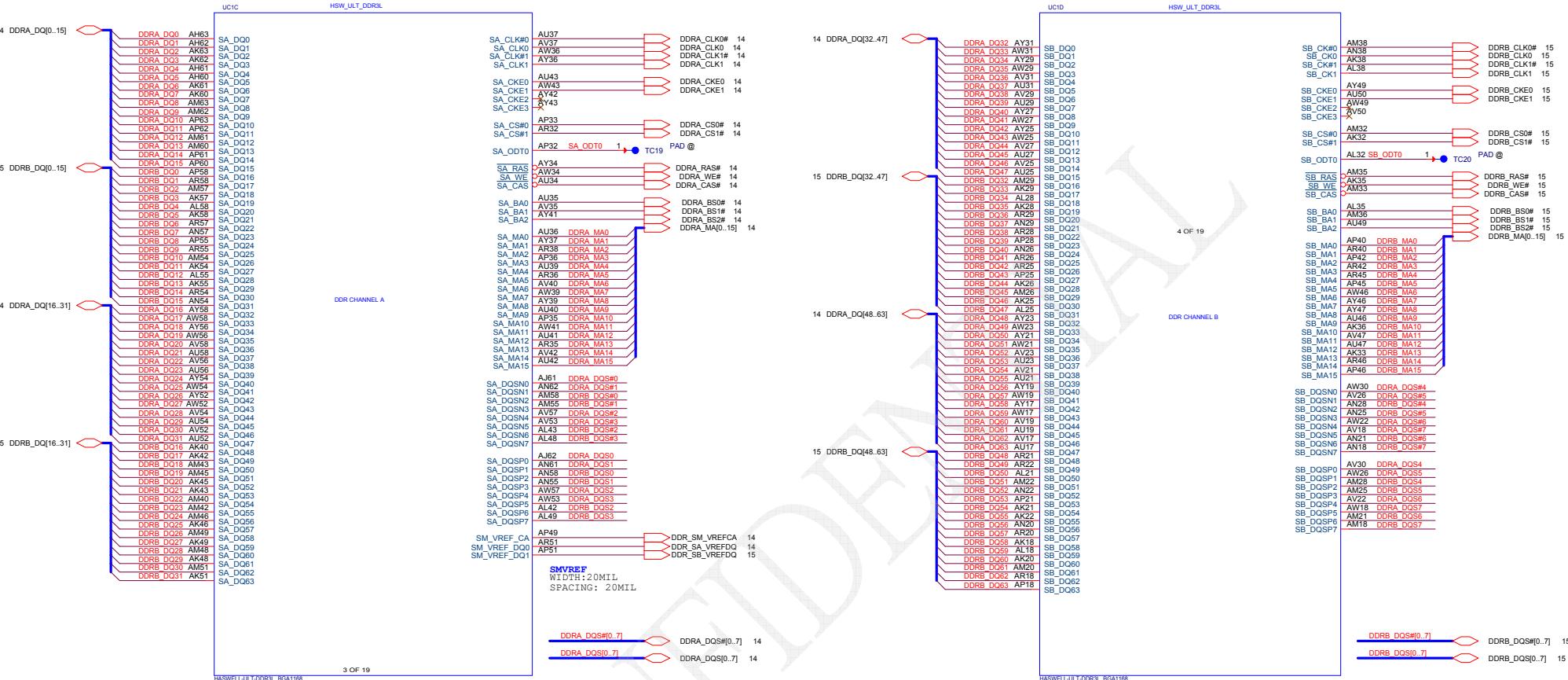
Device	Address
DDR DIMMA	1010 000Xb
DDR DIMMB	1010 010Xb
Wlan	Rsvd

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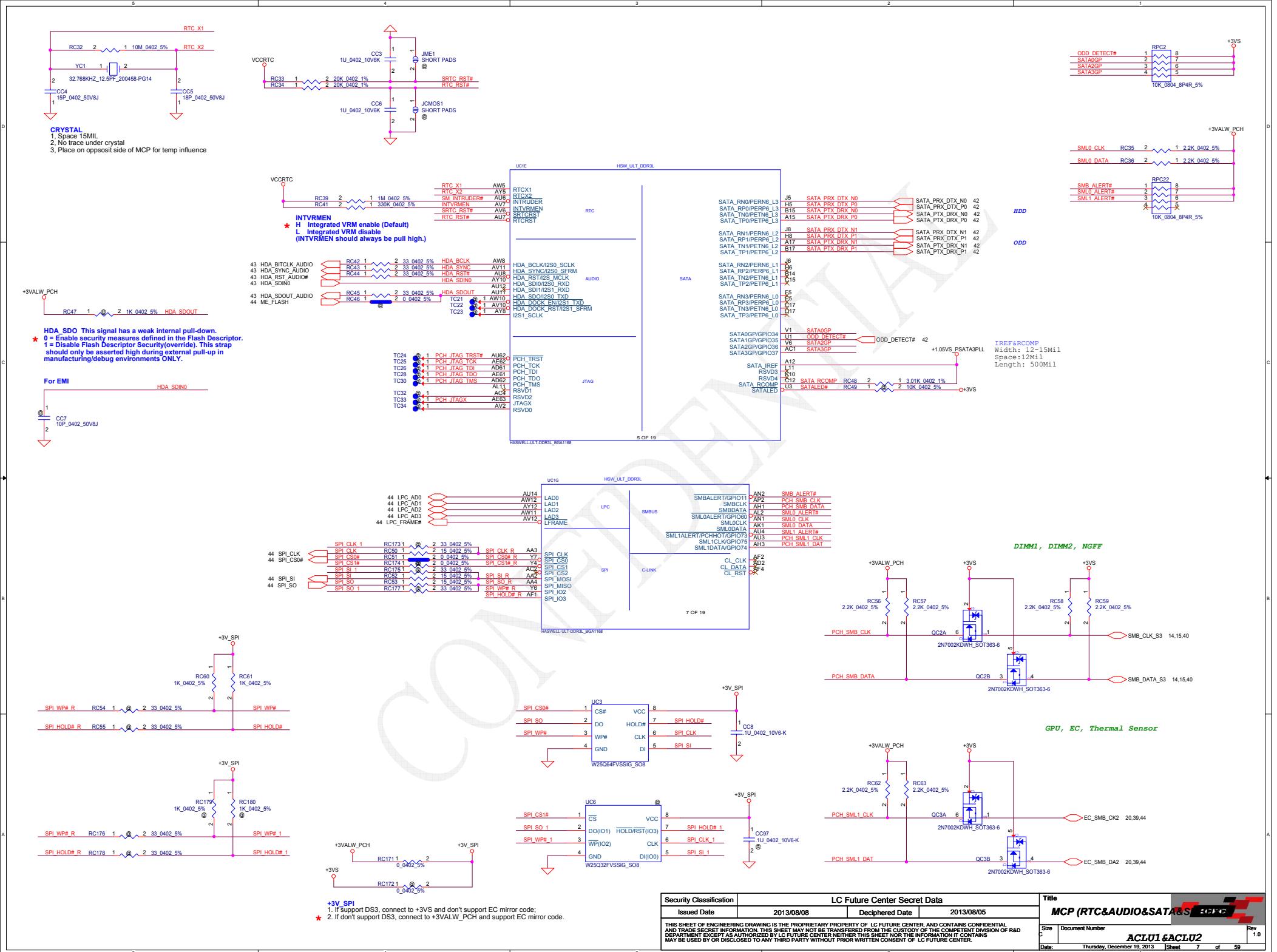


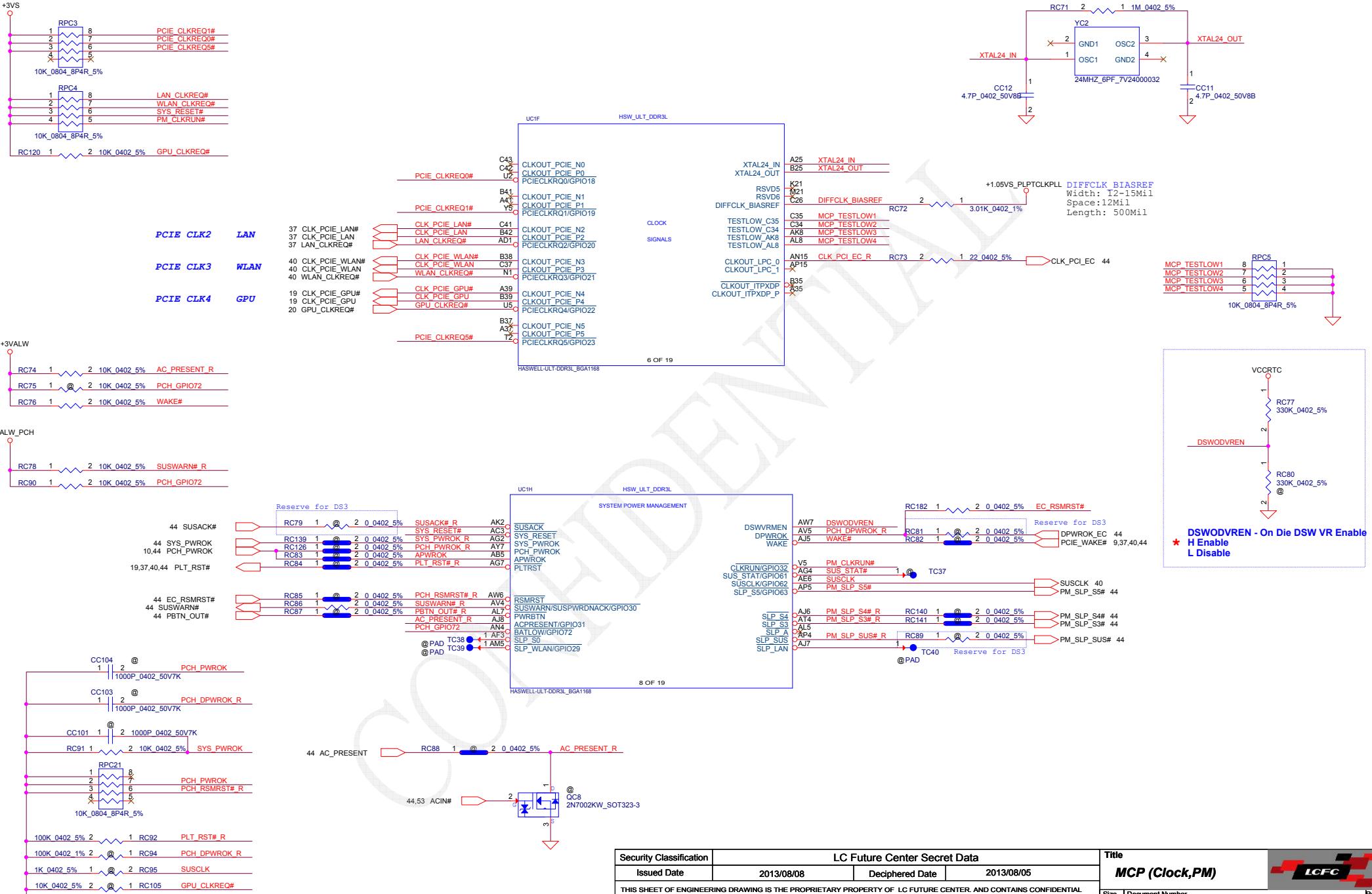
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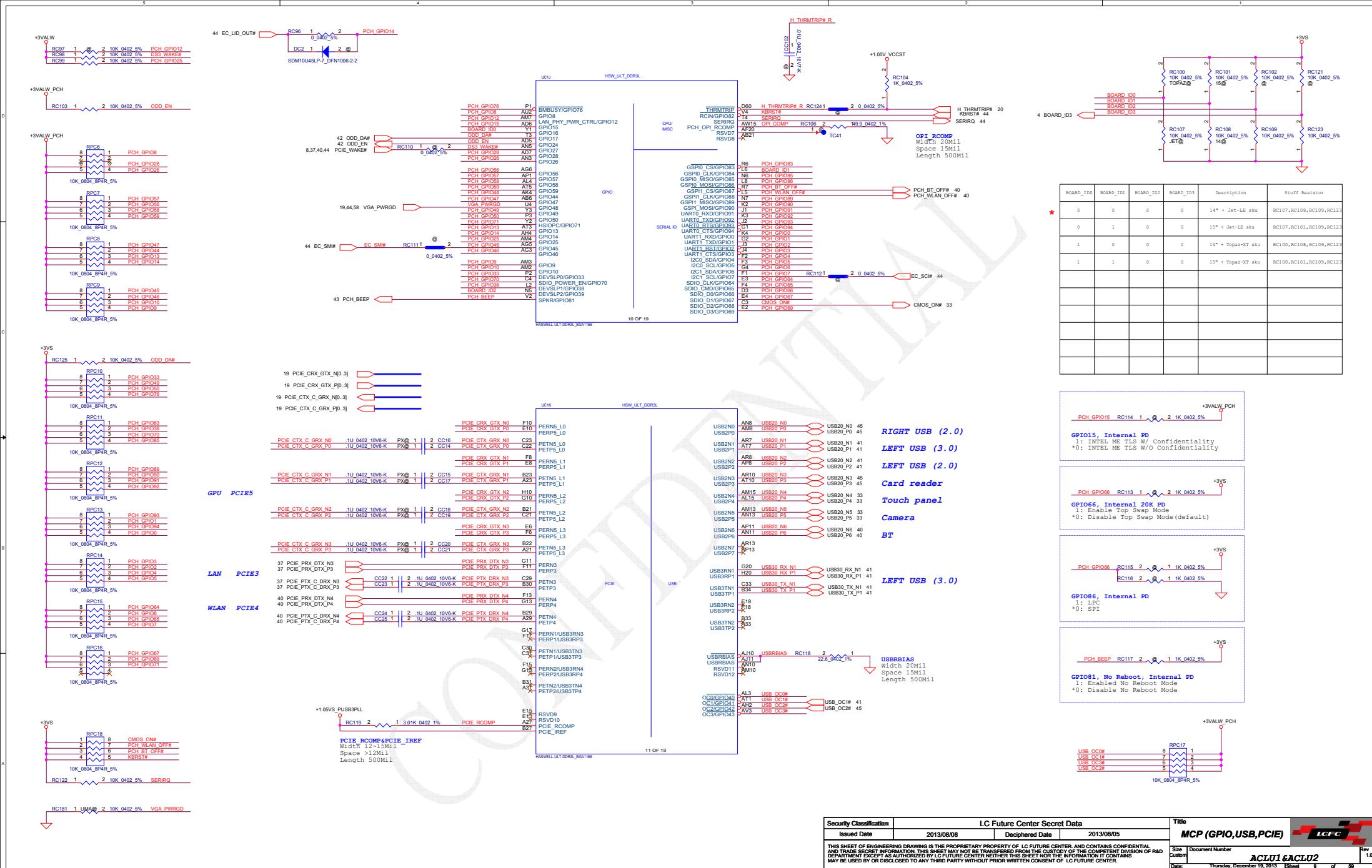


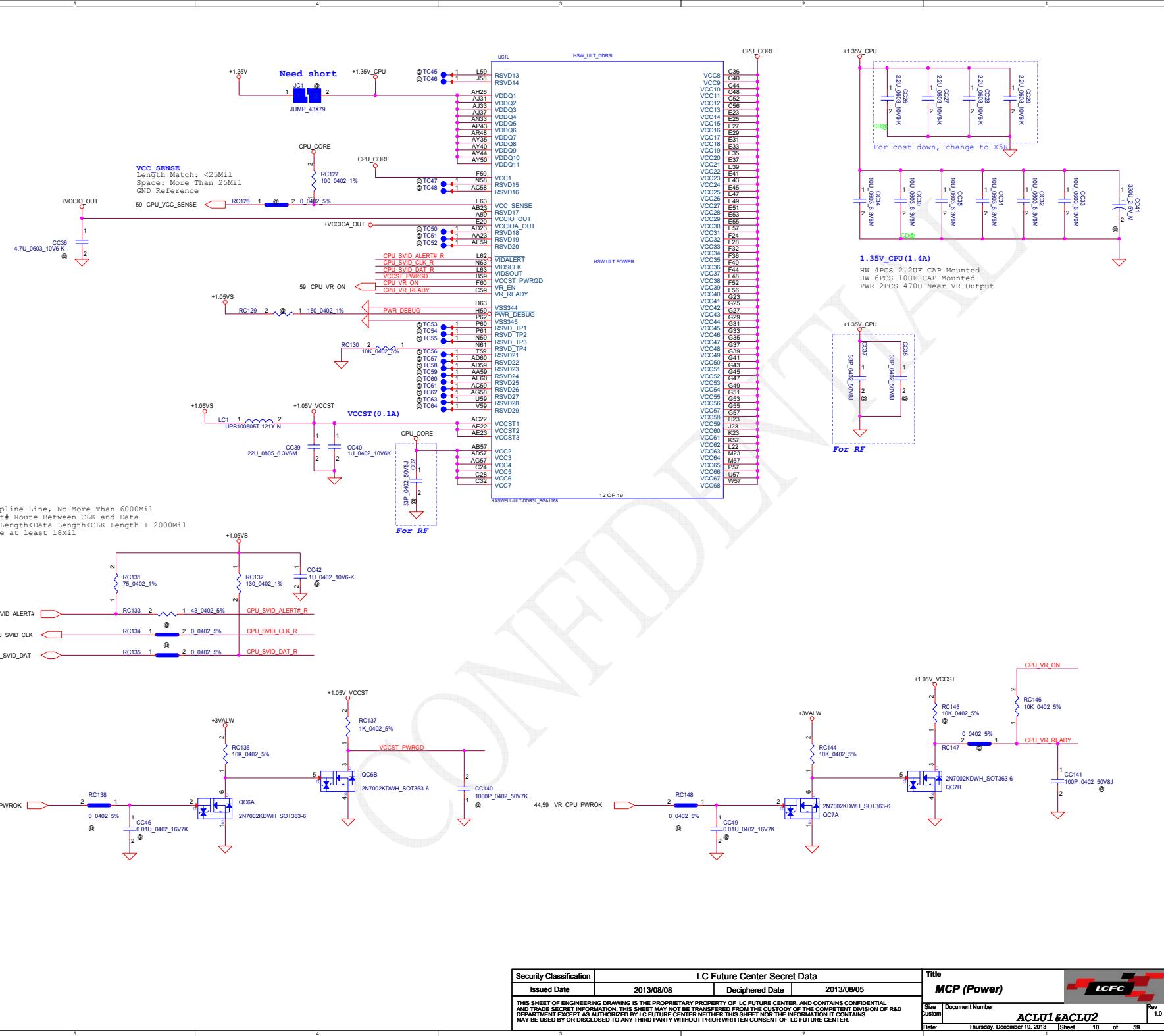
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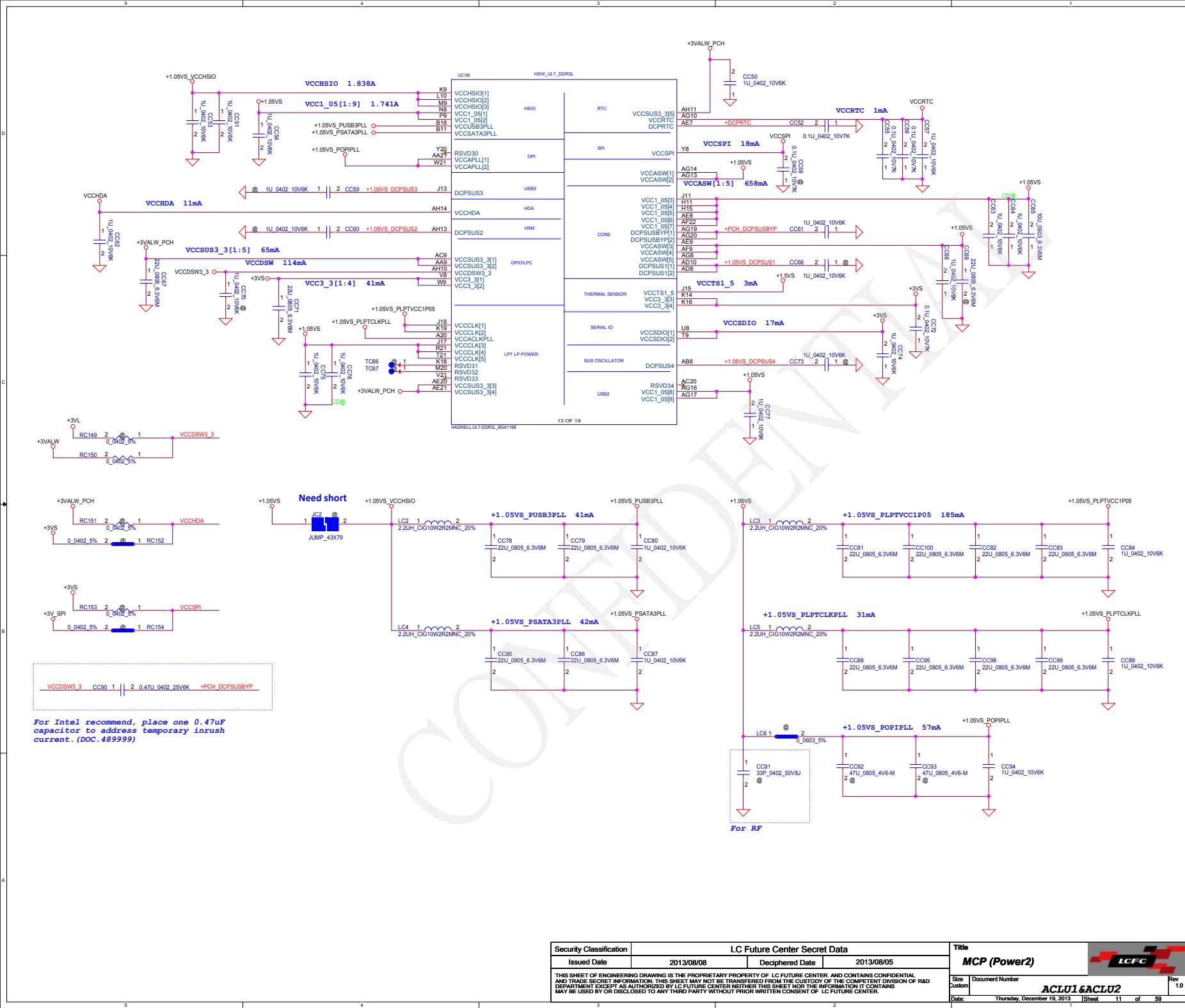


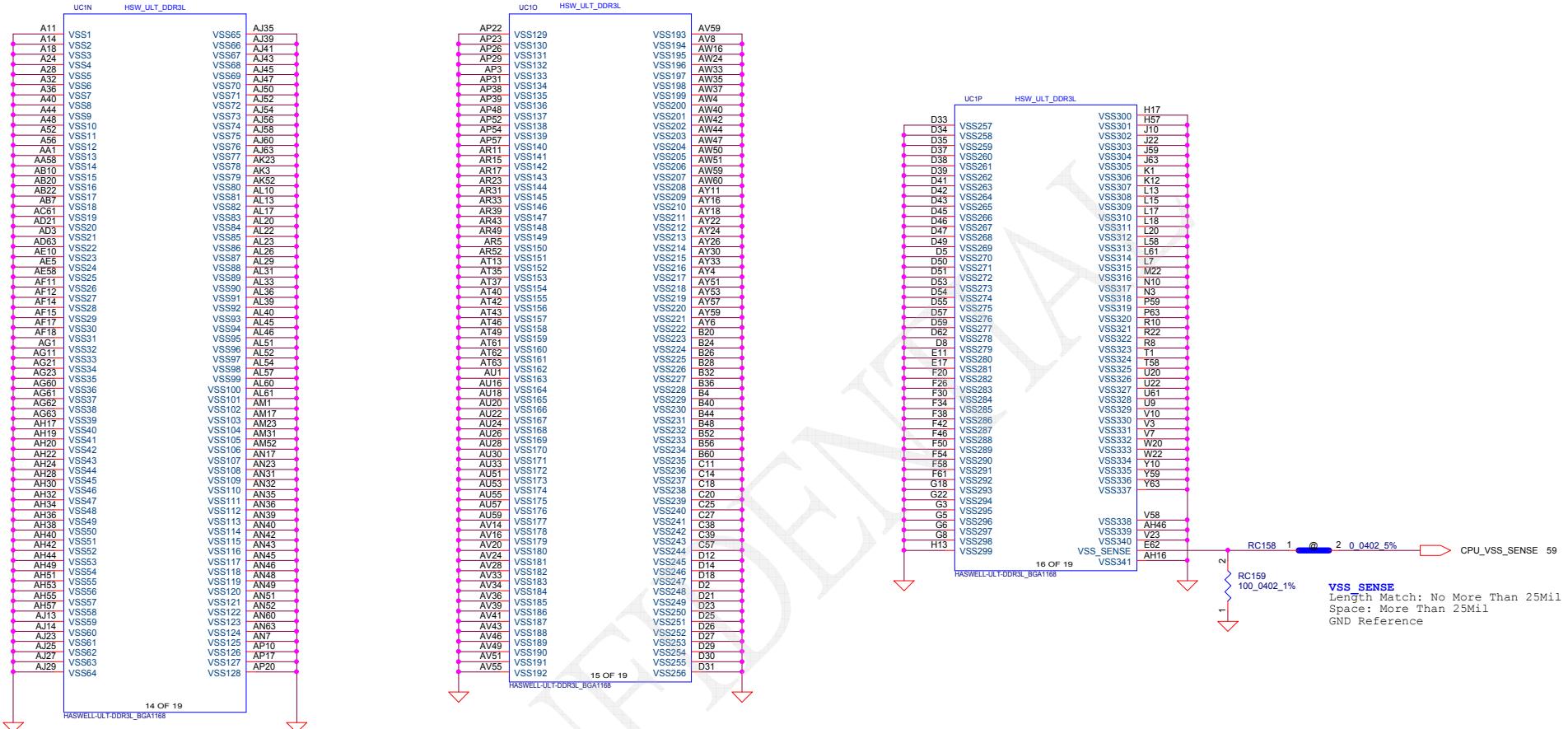


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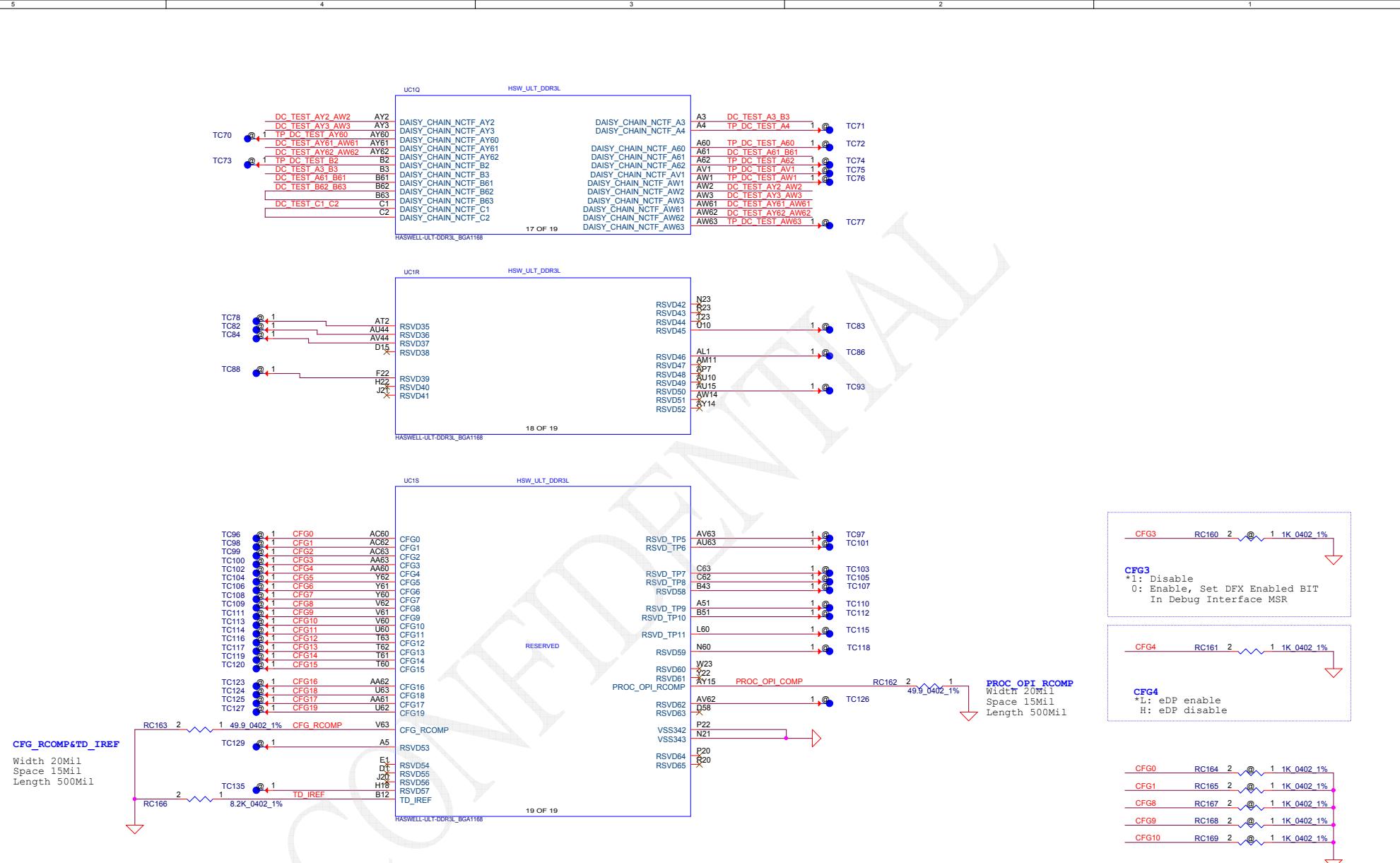
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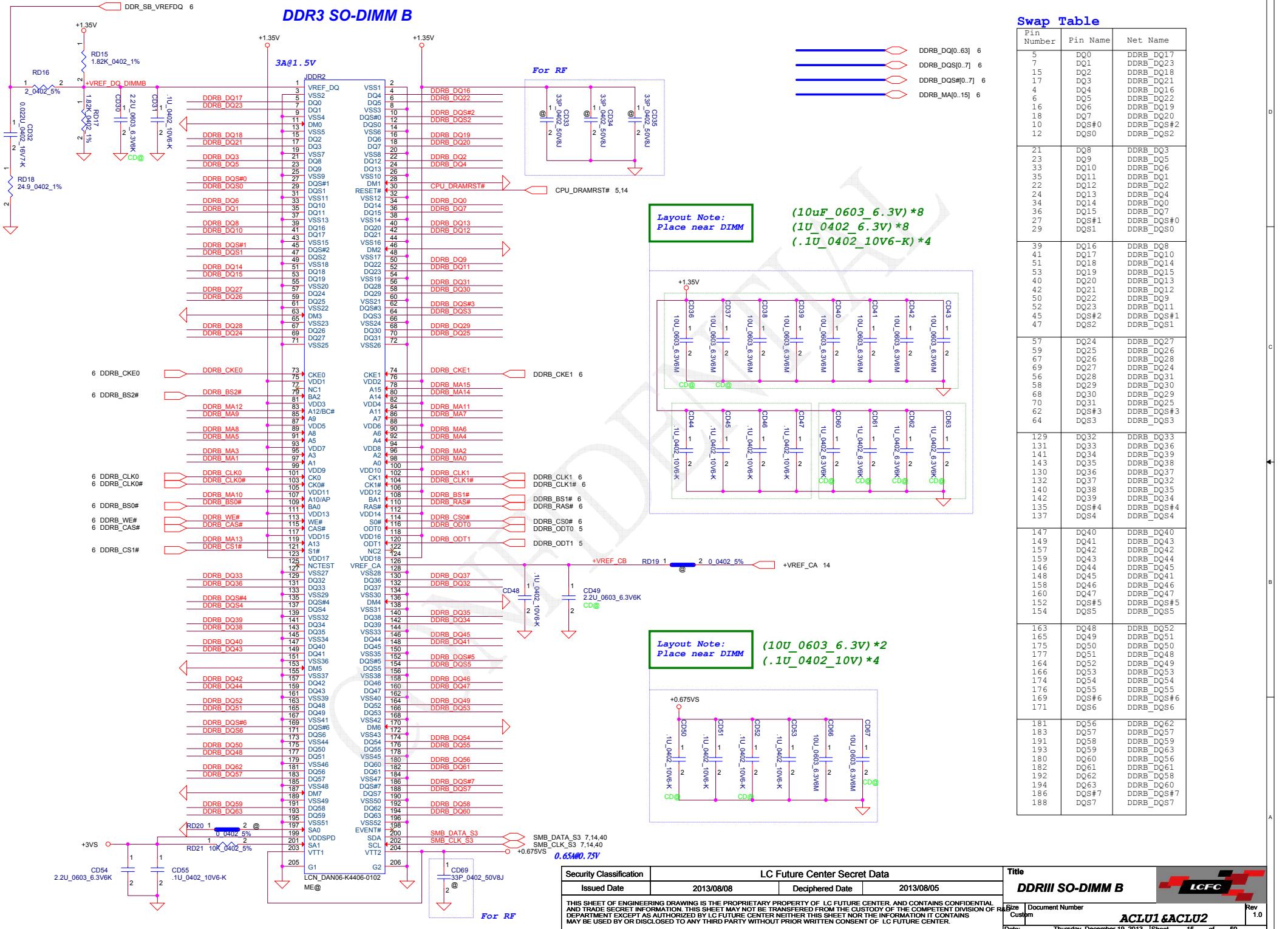
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## Power-Up/Down Sequence

"Topaz" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

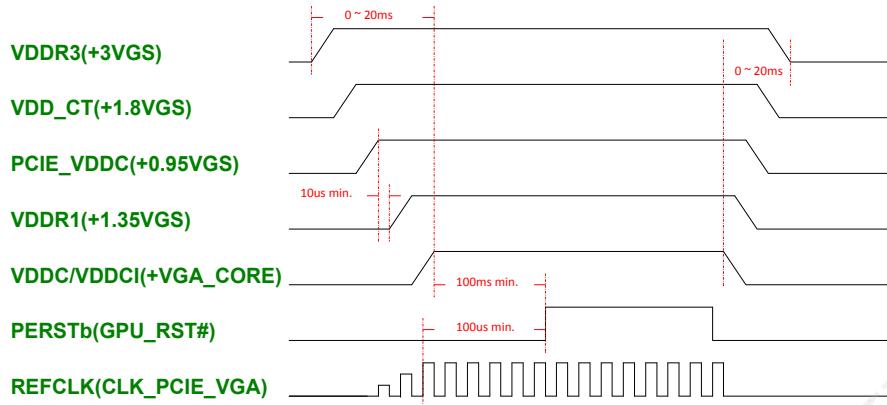
All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/μs.

It is recommended that the 3.3-V rail ramp up first.

The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready state at least 10 μs before VDDC, VDDCI, and VMEMIO start to ramp up.

The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as ≤ 50 mV/μs).

For power down, reversing the ramp-up sequence is recommended.



**CONFIGURATION STRAPS**  
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
0=DO NOT INSTALL RESISTOR  
1=INSTALL 10K RESISTOR  
X=DESIGNER DISENTANT  
NA=NOT APPLICABLE

MLPS Bit	Strap Name	Description	RECOMMENDED SETTINGS
PS_0[1] PS_0[2] PS_0[3]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	Define the ROM type when STRAP_BIOS_ROM_EN = 1. Define the primary memory-aperture size when STRAP_BIOS_ROM_EN = 0.  100 = 256MB	X
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	AUD_PORT_CONN_PINSTRAP[0]	The LSB (least significant bit) of the strap option that indicates the number of audio-capable display outputs.	1
PS_1[1]	STRAP_BIF_GEN3_EN_A	1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	0 = Not support X
PS_1[2]	STRAP_BIF_CLK_PM_EN	0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	0 = The transmitter half-swing is enabled 1 = Tx de-emphasis is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	0 = Tx de-emphasis disabled. 1 = Tx de-emphasis enabled.	1 = Enable X
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	0 = Disable X
PS_2[4]	STRAP_BIF_VGA_DIS	0 = VGA controller capacity enabled. 1 = The device will not be recognized as the system's VGA controller.	1
PS_2[5]	N/A	Reserved	1
PS_3[1] PS_3[2] PS_3[3]	BOARD_CONFIG[0] BOARD_CONFIG[1] BOARD_CONFIG[2]	Board configuration related strapping, such as for memory ID 000 = Hynix 256M*16 100 = Samsung 256M*16 010 = Micron 256M*16 111 = Micron 128M*16	X
PS_3[4] PS_3[5]	AUD_PORT_CONN_PINSTRAP[1] AUD_PORT_CONN_PINSTRAP[2]	Determines the maximum number of digital display audio endpoints that will be presented to the OS and user.(Combine with PS_0[5]) 111 = No usable endpoints. 110 = One usable endpoint. 101 = Two usable endpoints. 100 = Three usable endpoints. 011 = Four usable endpoints. 010 = Five usable endpoints. 001 = Six usable endpoints. 000 = All endpoints are usable.	111 = No usable endpoints. 11 X

## VRAM ID config

Memory Type		VRAM ID PS_3[3:1]	PU resistor RV33	PD resistor RV36
128Mx16	Hynix H5TC2G63FFR-11C	100	4.53K	4.99K
	Micron MT41J128M16JT-093G	111	4.75K	NC
	Samsung K4W2G1646Q-BC1A	110	3.4K	10K
256Mx16	Hynix H5TC4G63AFR-11C	000	NC	4.75K
	Micron MT41J256M16HA-093G	010	4.53K	2K
	Samsung K4W4G1646D-BC1A	001	8.45K	2K
	Micron MT41K256M16HA-107G	011	6.98K	4.99K

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## VGA Notes List

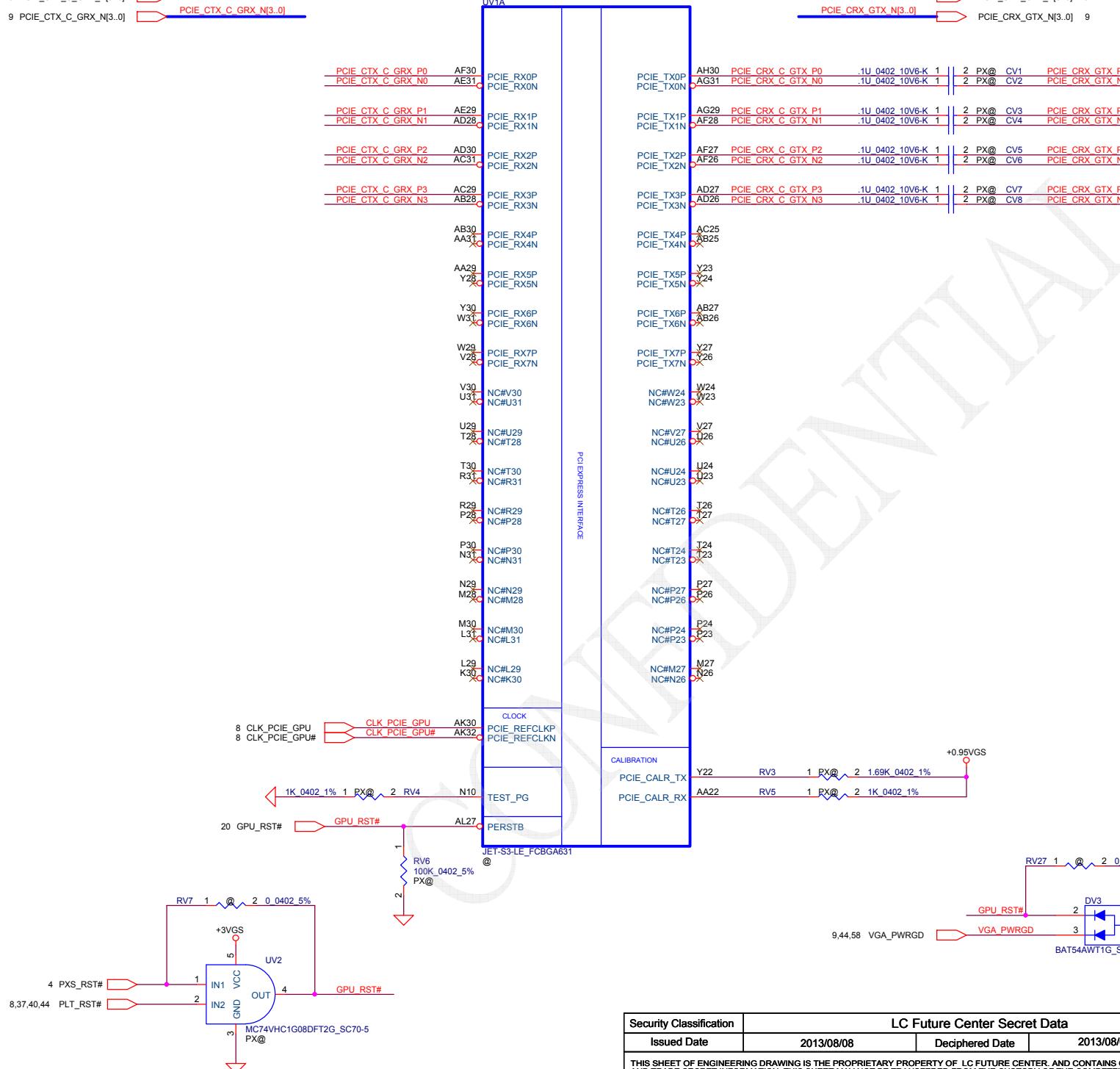
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5 4 3 2 1  
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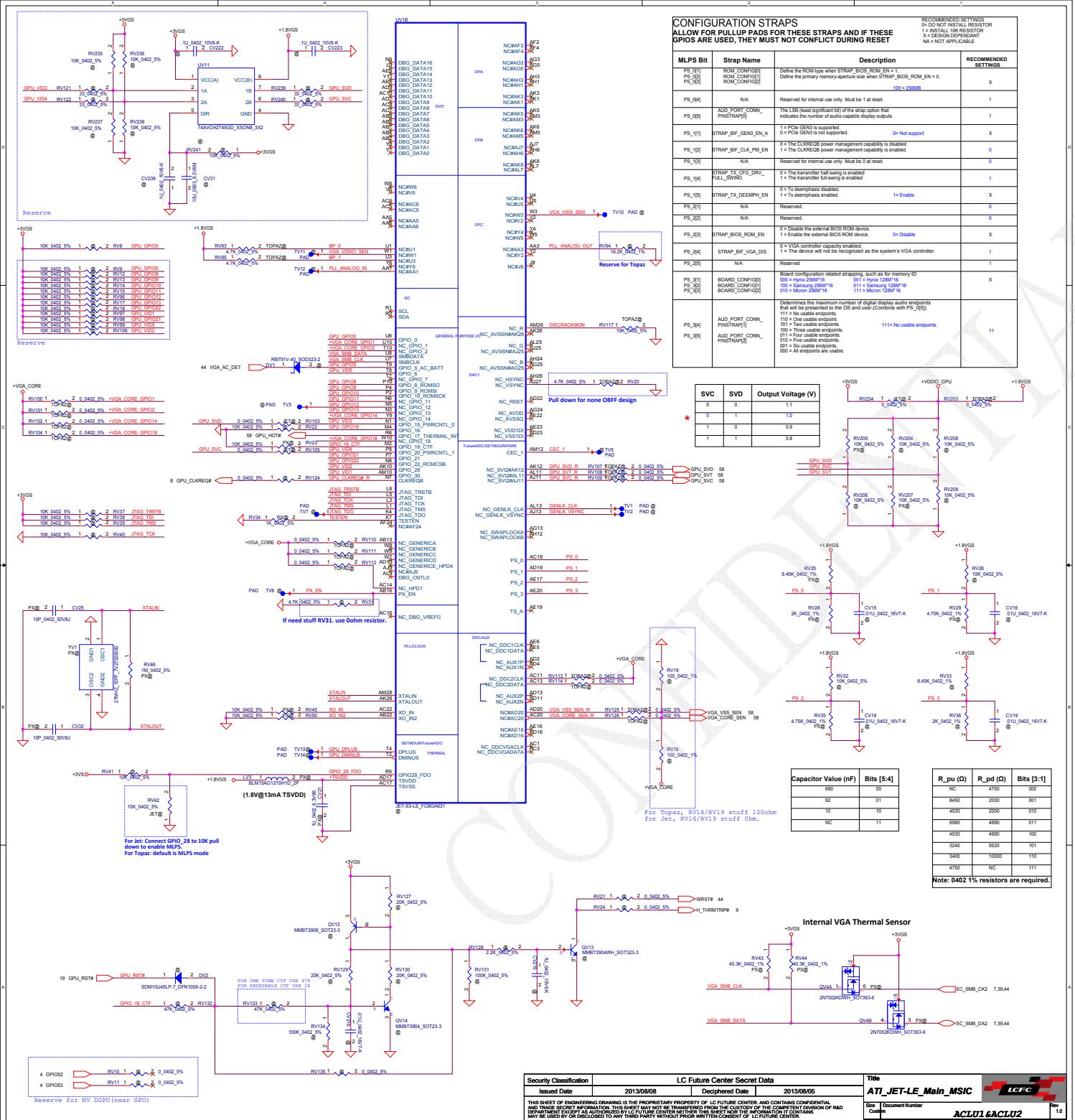
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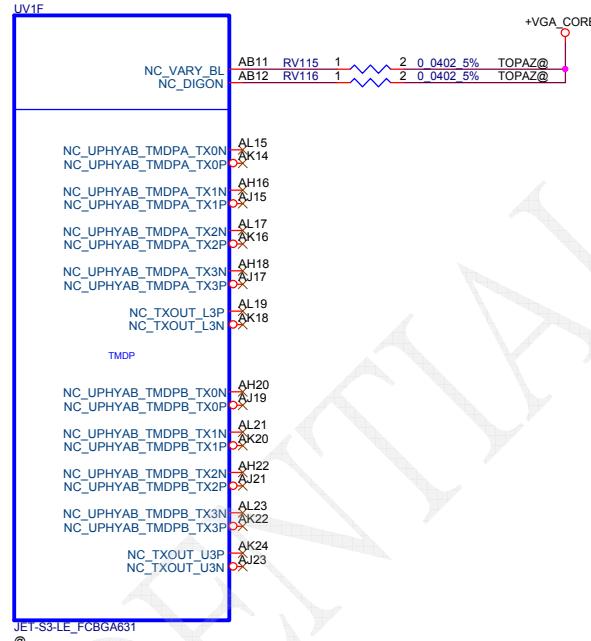
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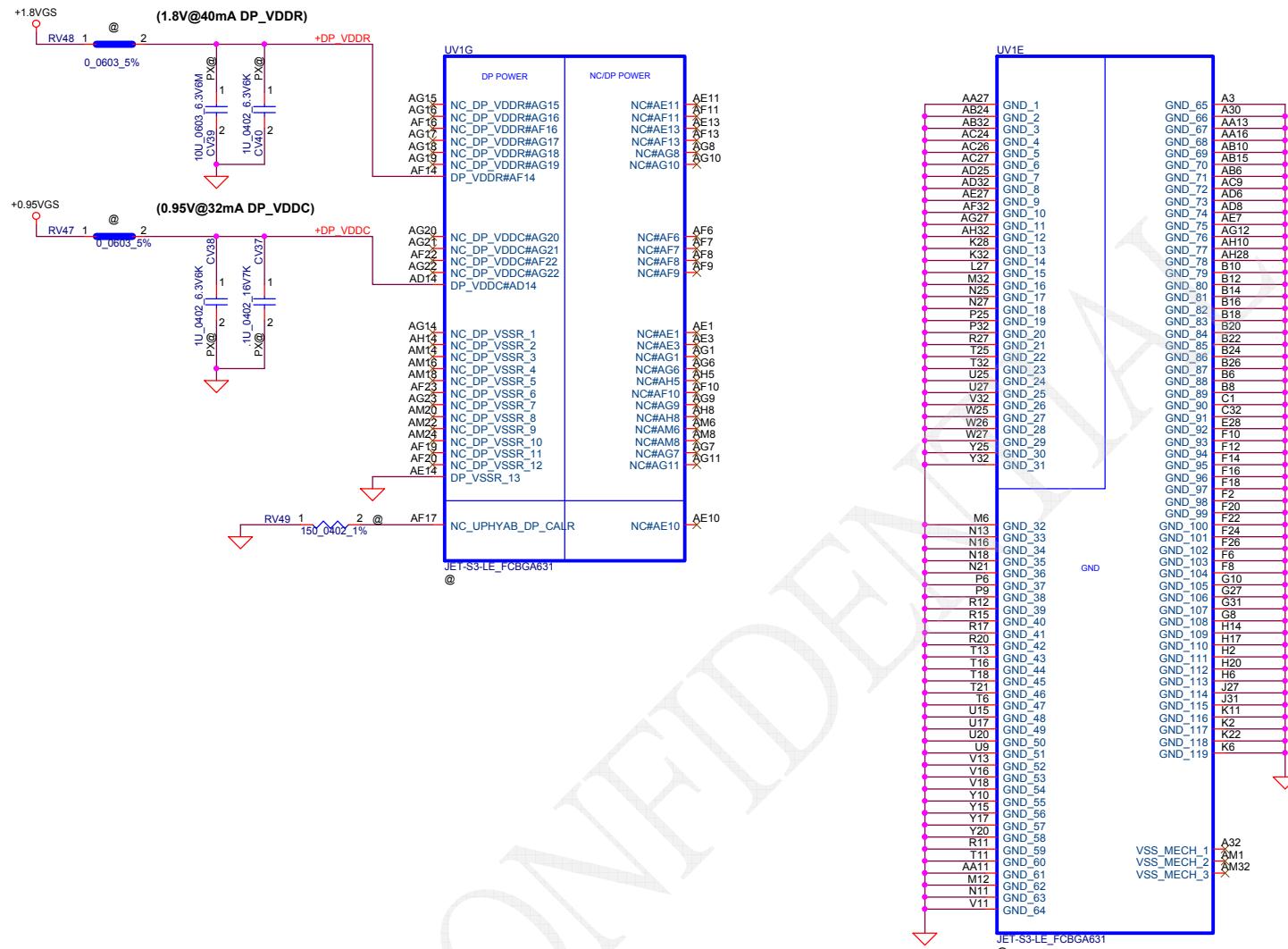


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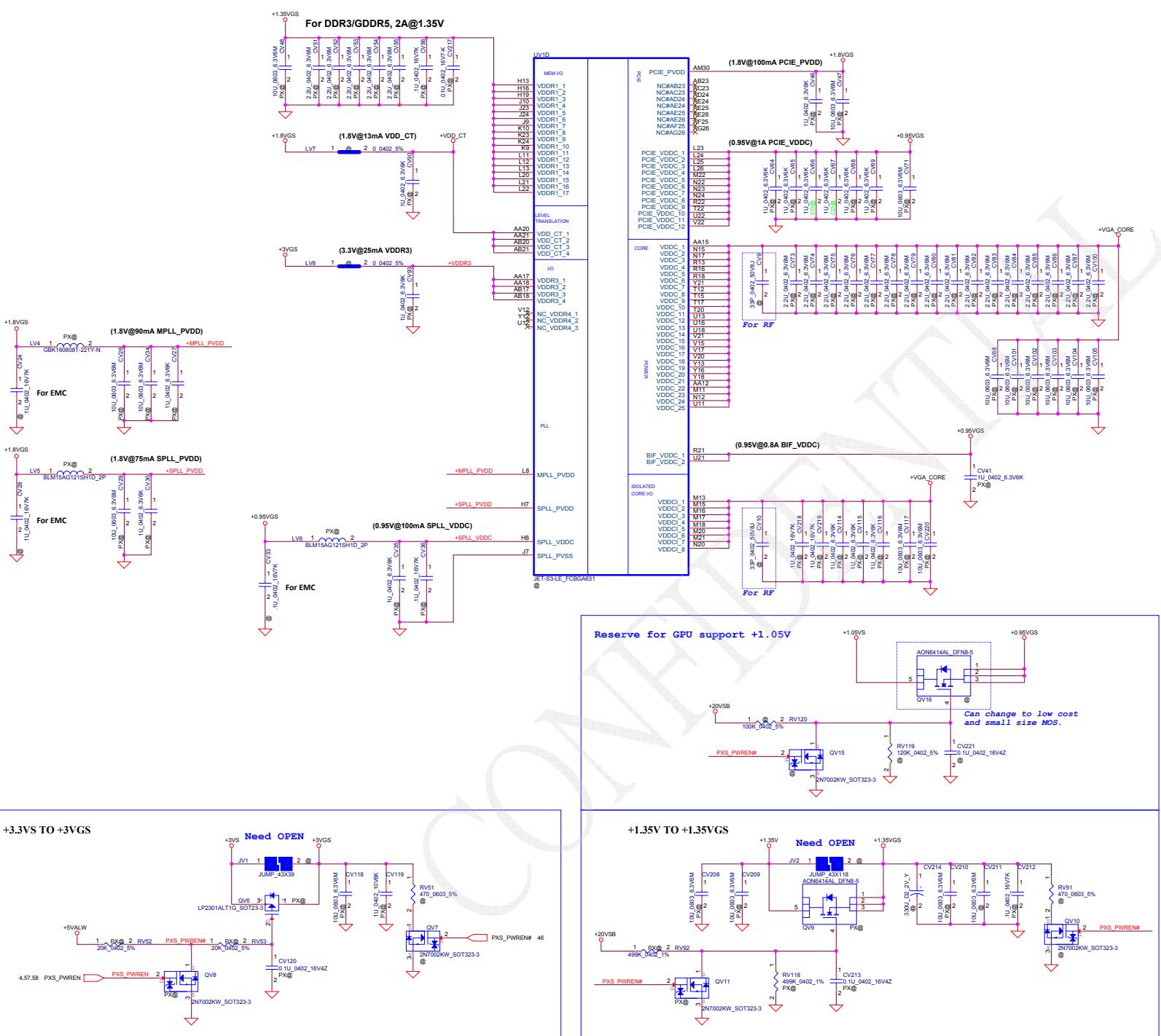
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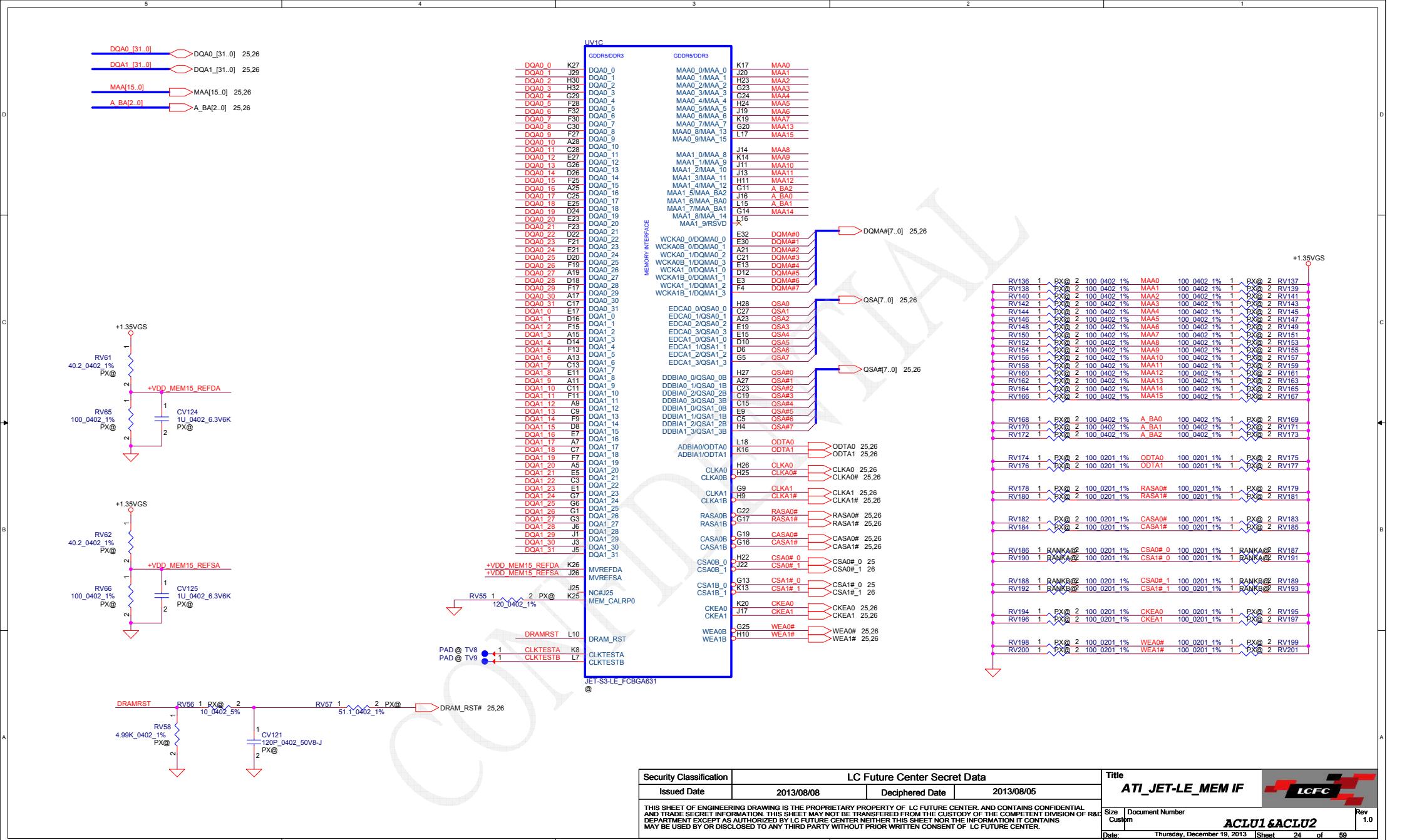
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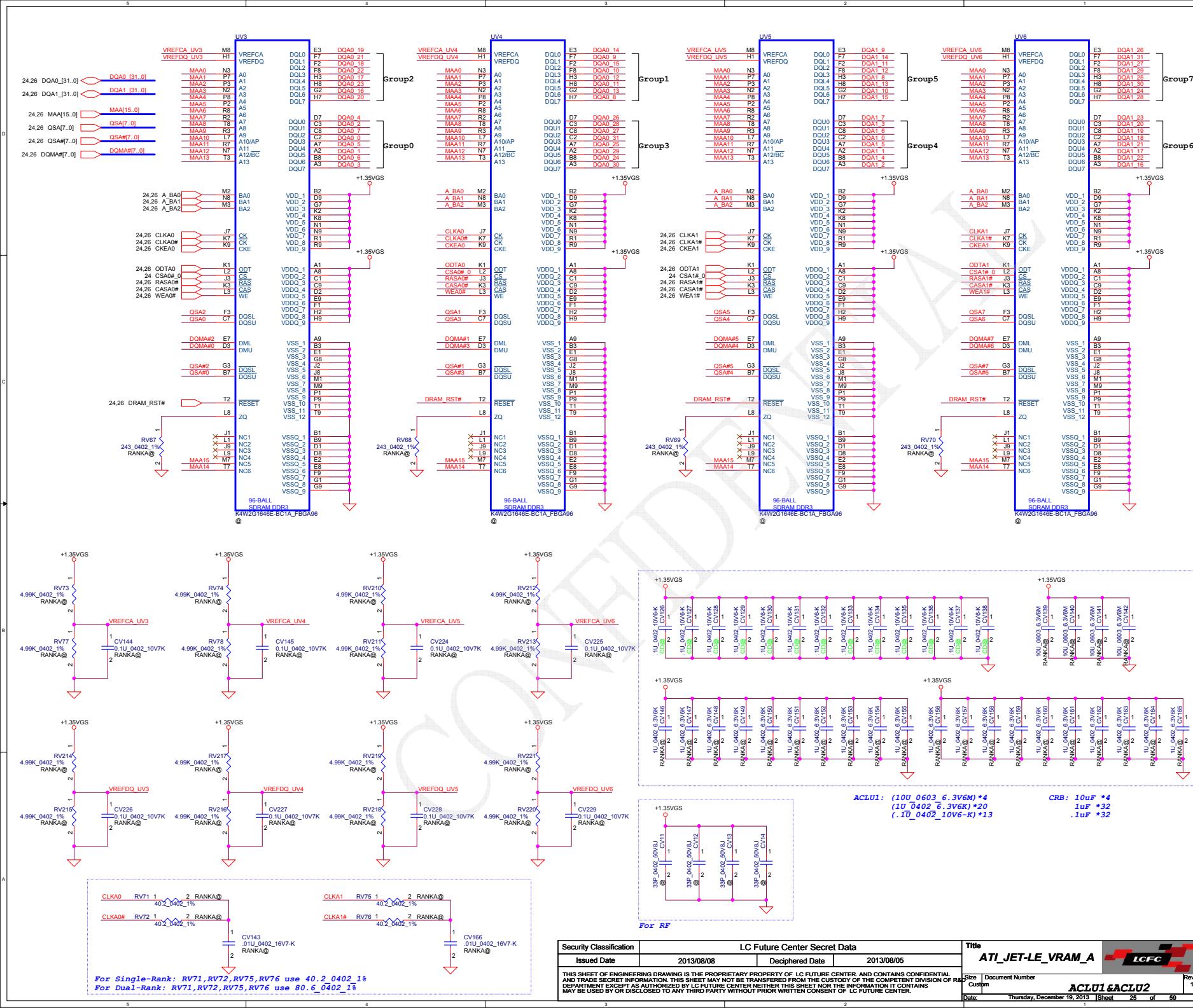
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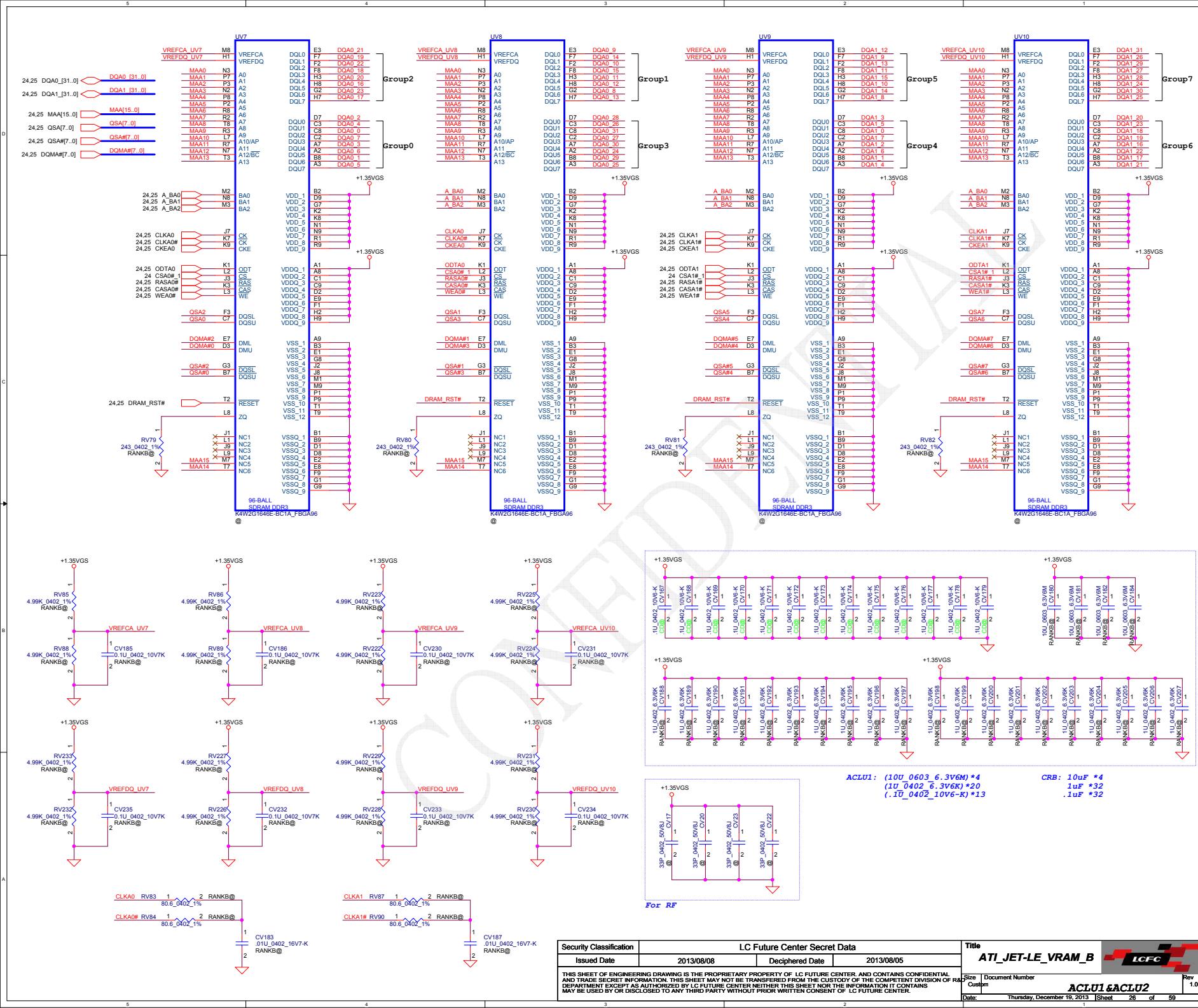
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## Title

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Size

Document Number

Rev

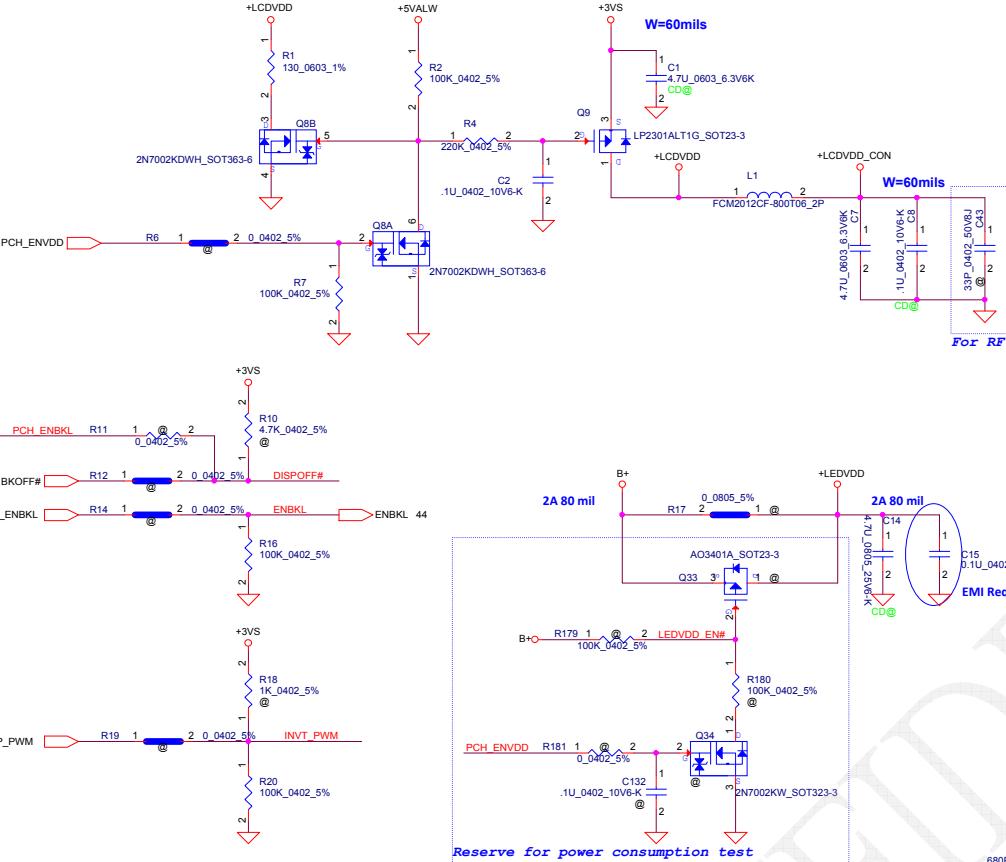
Custom

ACLU1 &amp; ACLU2

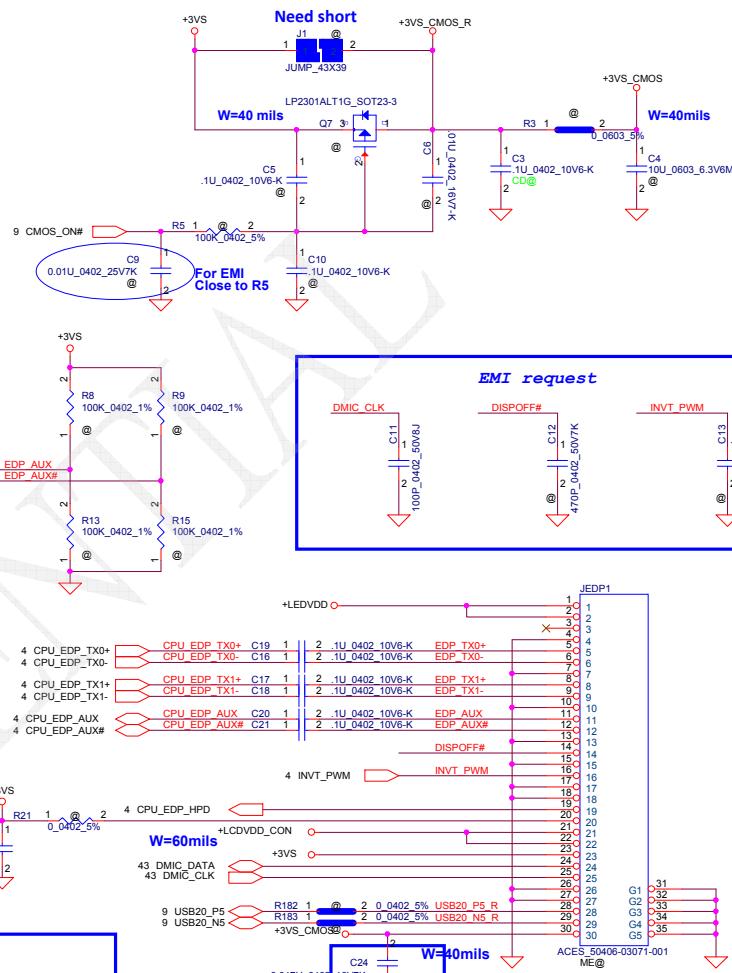
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Date: Thursday, December 19, 2013 Sheet 32 of 59

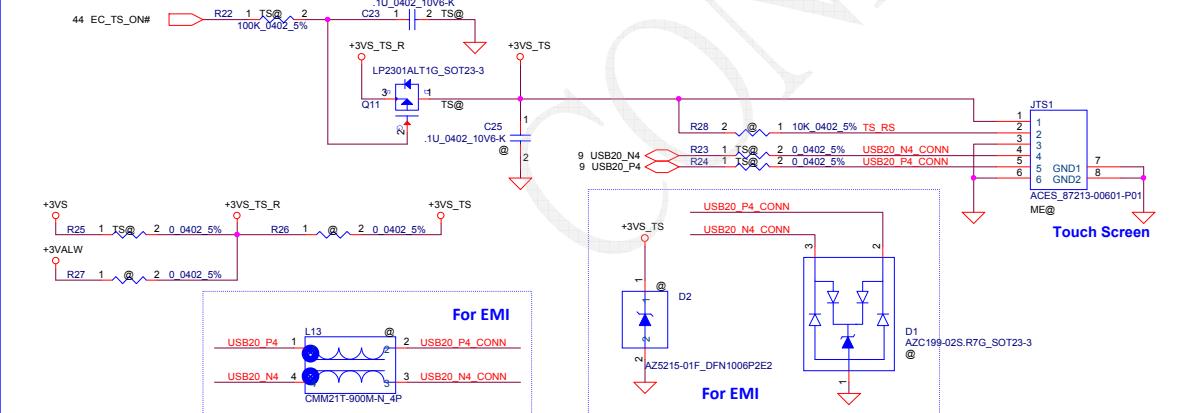
## LCD POWER CIRCUIT

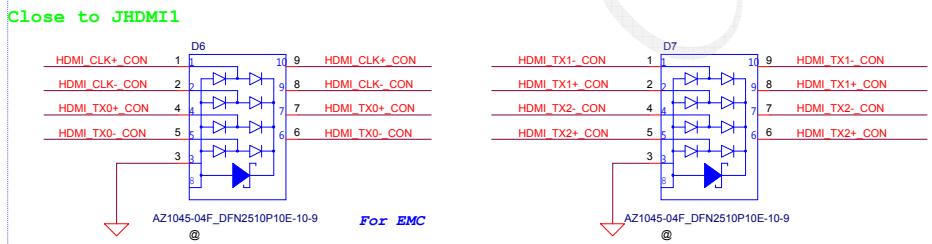
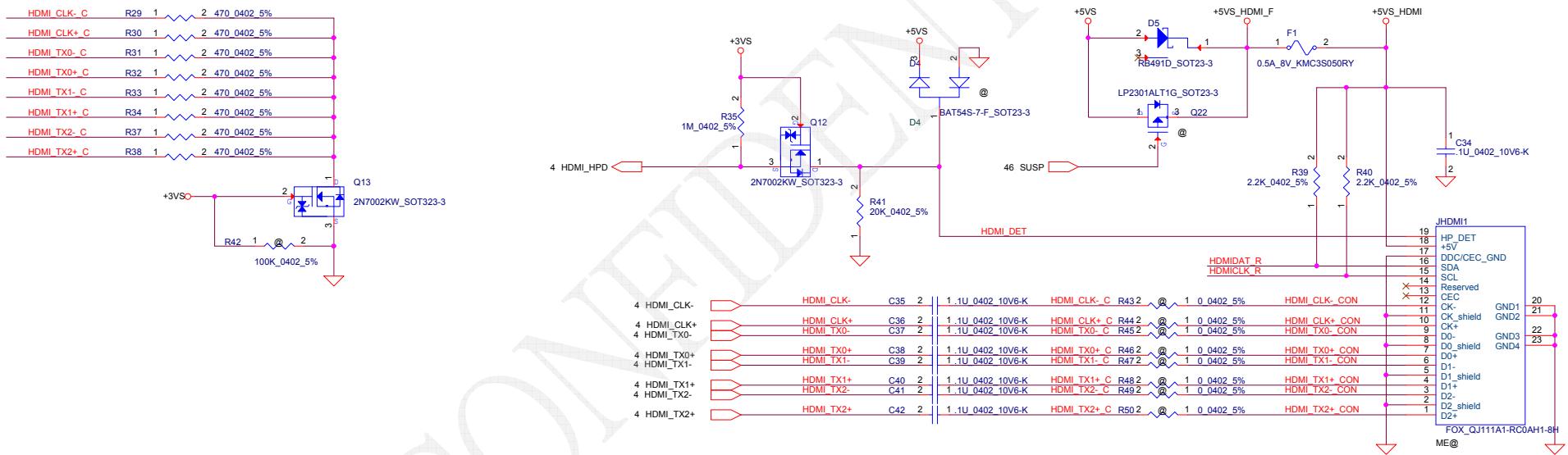
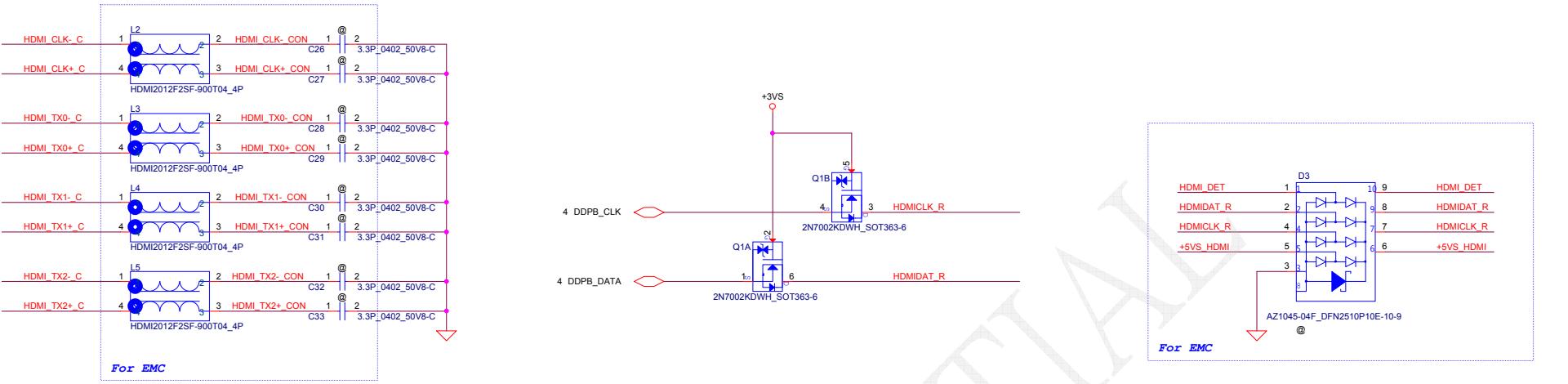


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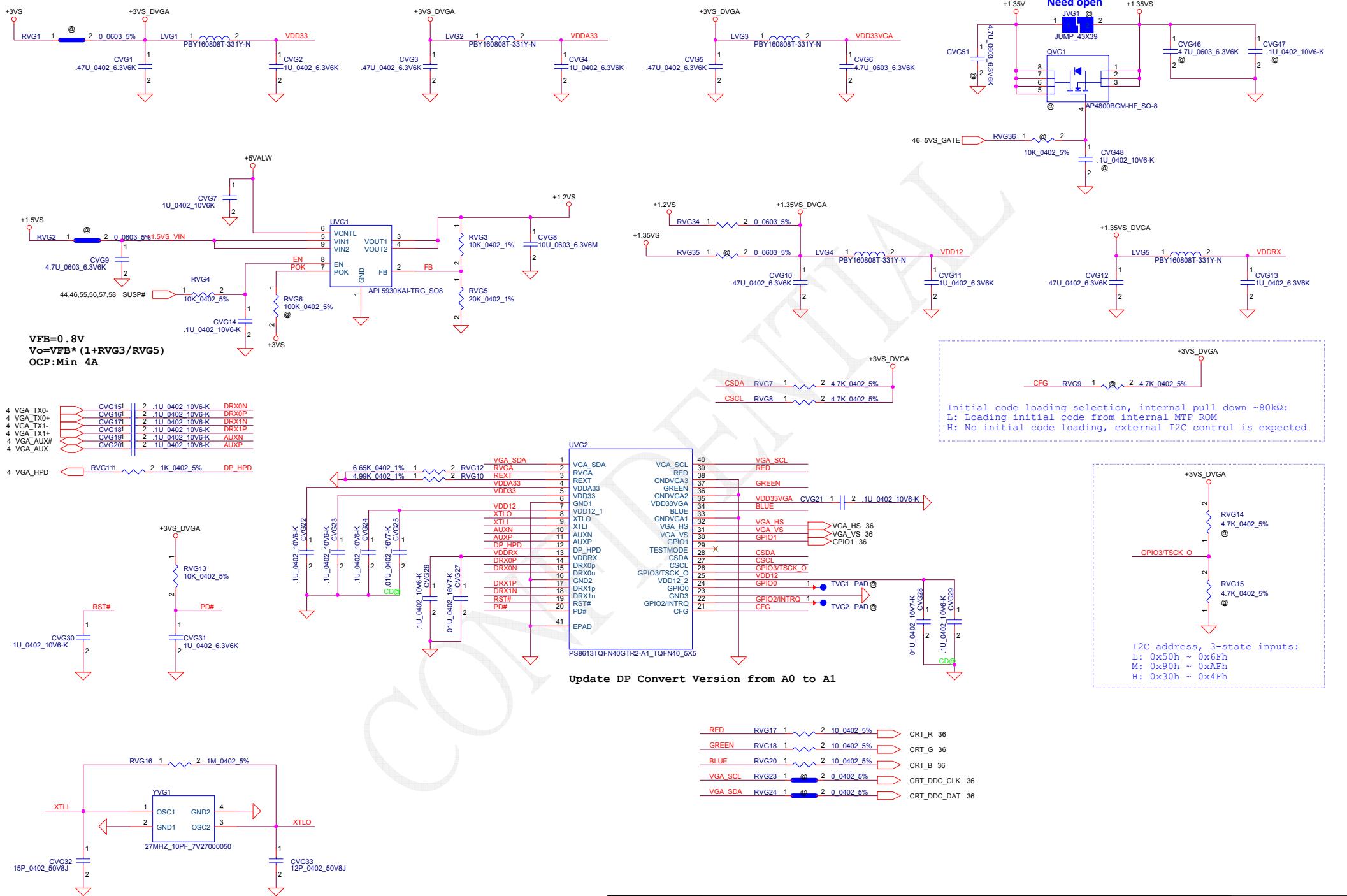


## Touch Screen



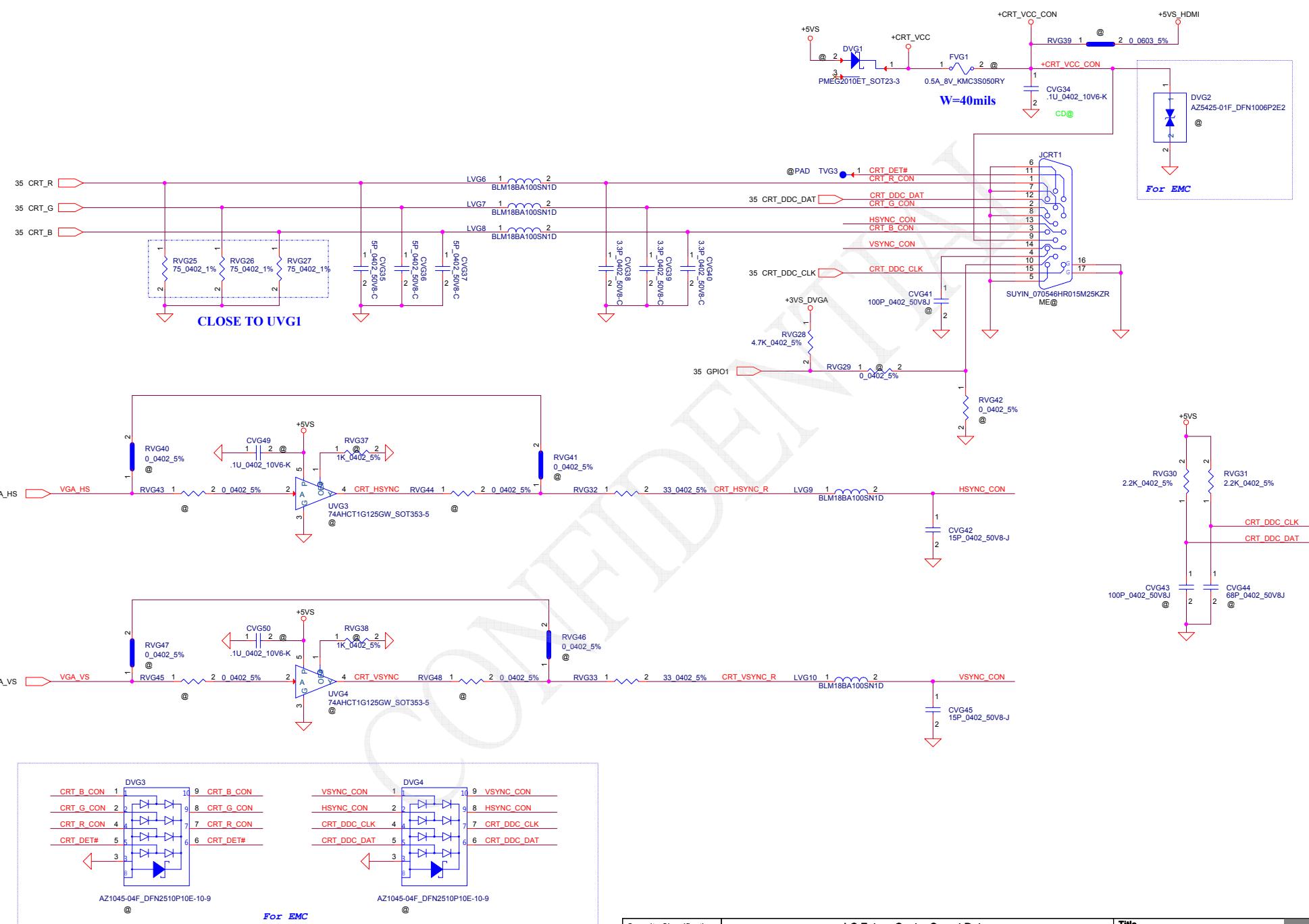


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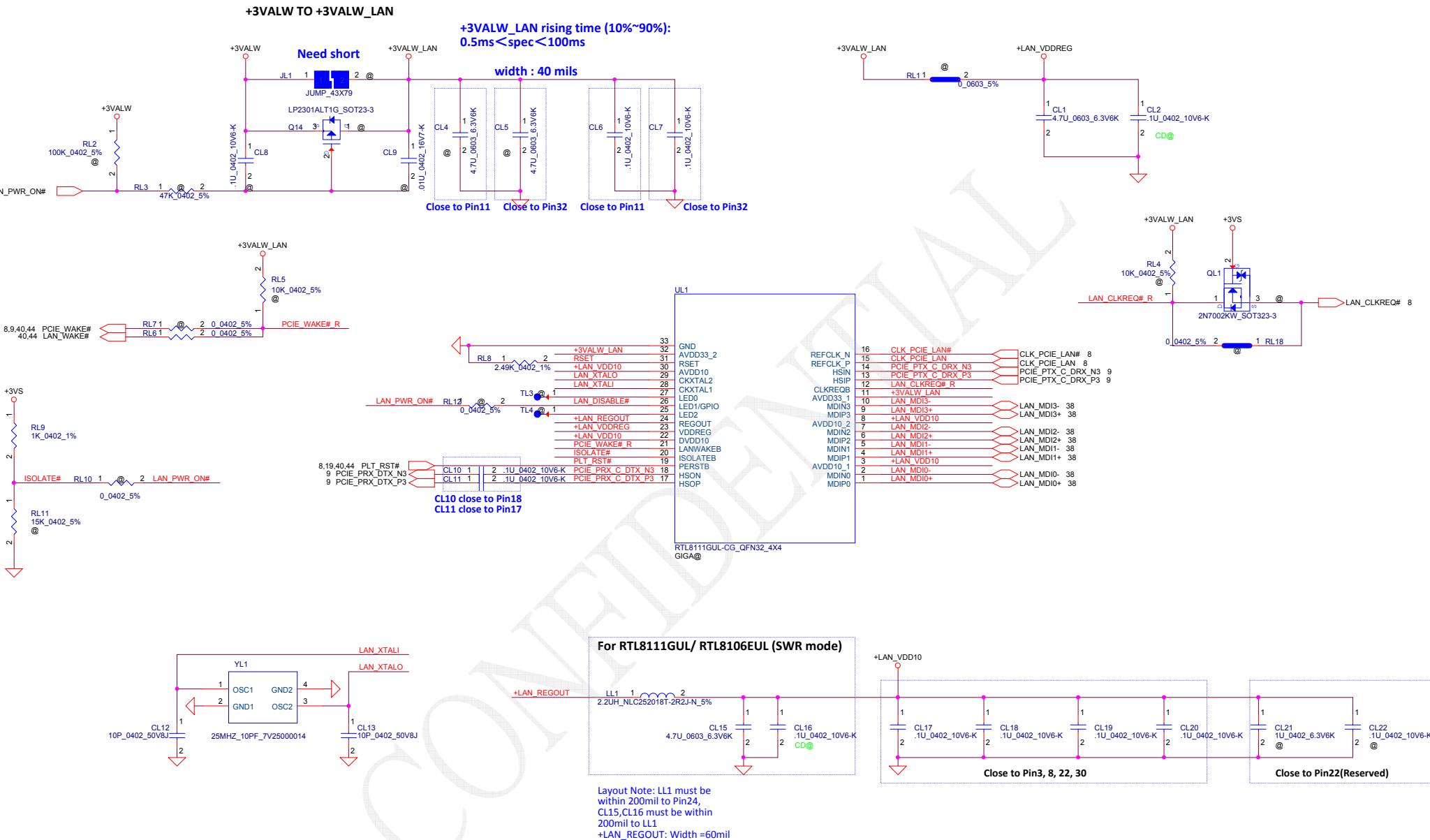


Security Classification	LC Future Center Secret Data			Title		
Issued Date	2013/08/08			DP to CRT Converter(PS8613)		
Deciphered Date	2013/08/05			Size	Document Number	Rev
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Custom	<b>ACLU1 &amp; ACLU2</b>			Date:	Thursday, December 19, 2013	Sheet 35 of 59

# CRT Connector

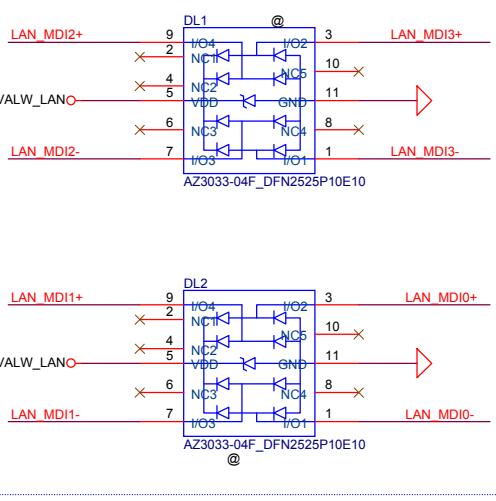


Security Classification	LC Future Center Secret Data			Title
Issued Date	2013/08/08	Deciphered Date	2013/08/05	CRT
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Size	Document Number	Rev		
Custom		1.0		
Date:	Thursday, December 19, 2013	Sheet	36	of 59
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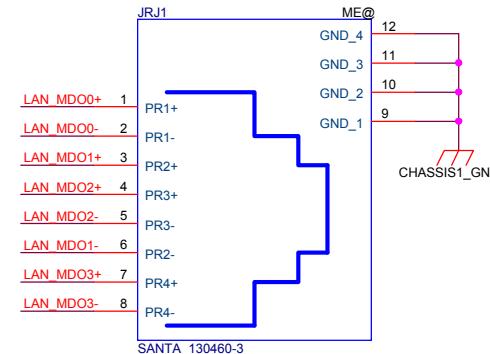
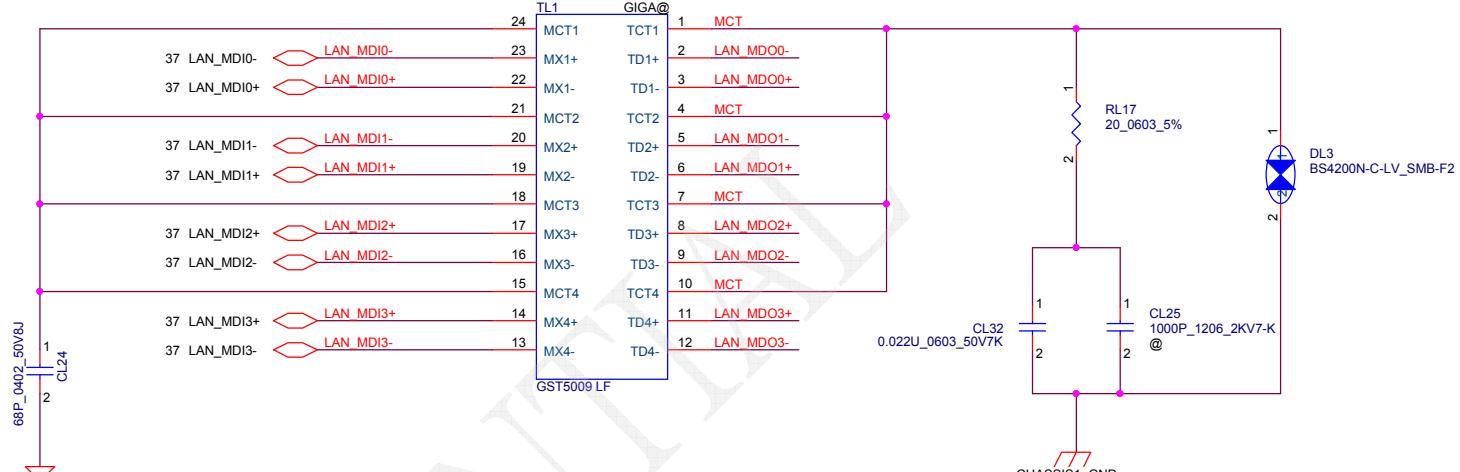
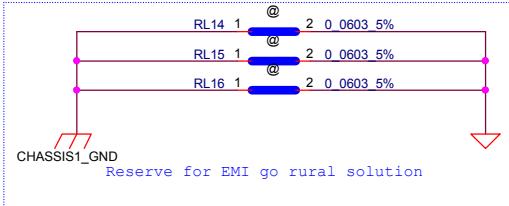


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Issued Date	Deciphered Date	Document Number	Rev	
2013/08/08	2013/08/05	ACL1 & ACL2	1.0	
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Date:	Thursday, December 19, 2013	Sheet	37	of 59

**DL1/DL2  
1'S PN:SC300003M00**

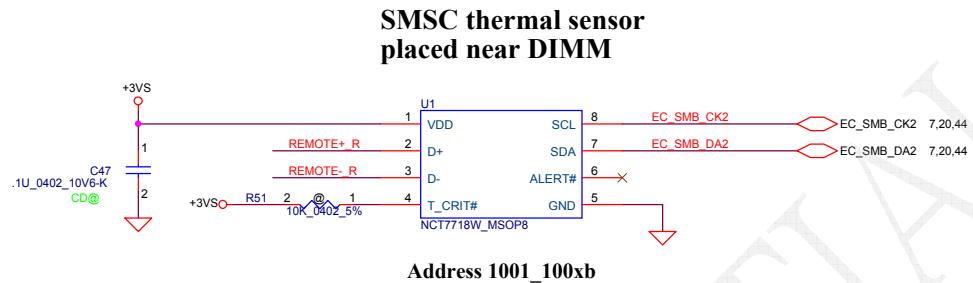
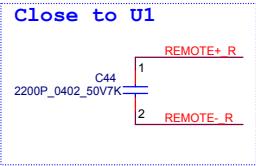


Place Close to TL1



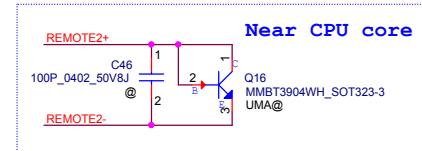
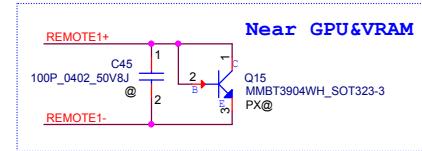
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Issued Date	Deciphered Date	2013/08/08	2013/08/05				
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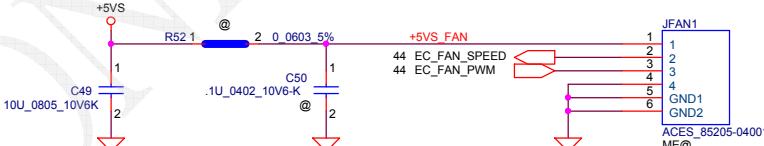


REMOTE1+ R175 1 @ 2 0 0402 5%  
 REMOTE2+ R176 1 UMA@ 2 0 0402 5% REMOTE+ R  
 REMOTE2- R177 1 UMA@ 2 0 0402 5% REMOTE- R  
 REMOTE1- R178 1 @ 2 0 0402 5%

REMOTE+/- R, REMOTE1+/-, REMOTE2+/-:  
 Trace width/space:10/10 mil  
 Trace length:<8"

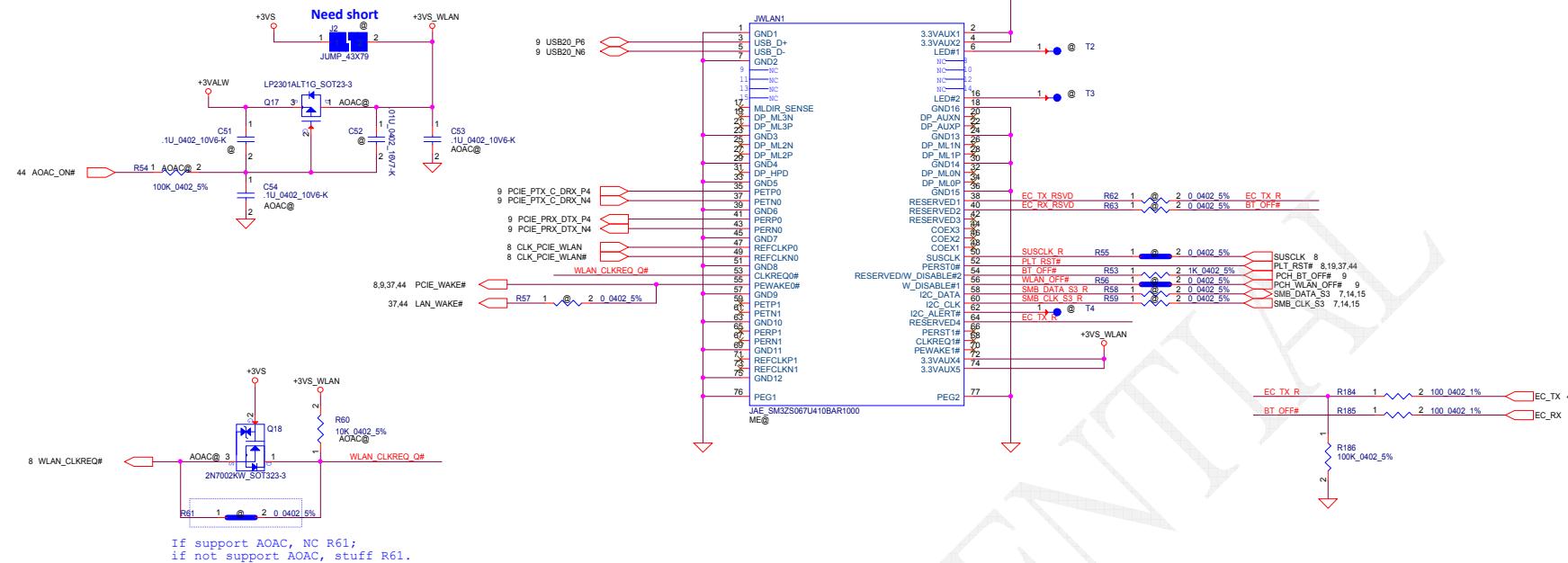


### FAN Conn



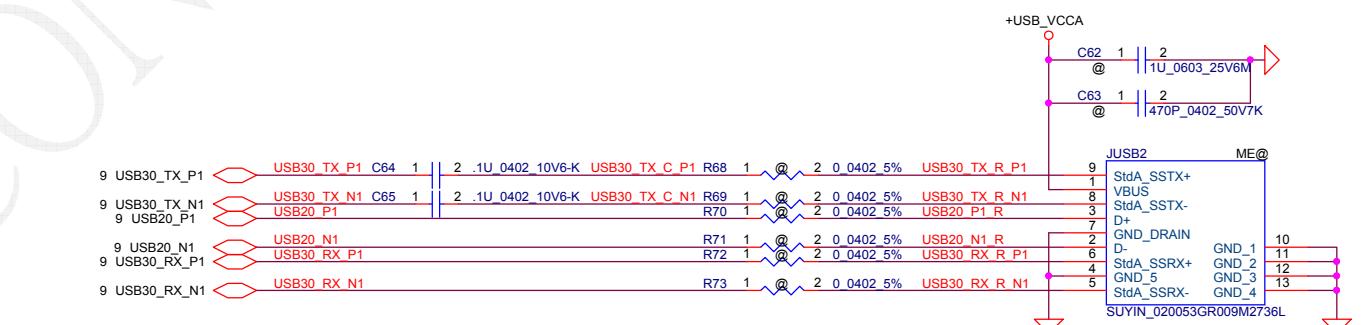
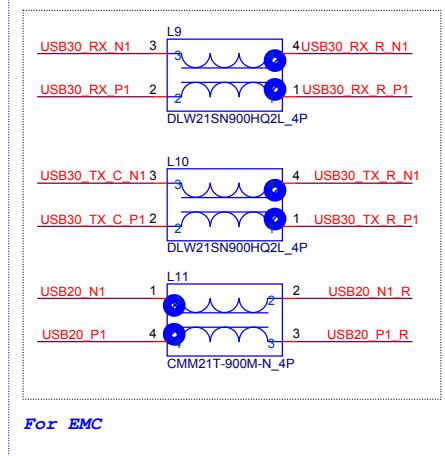
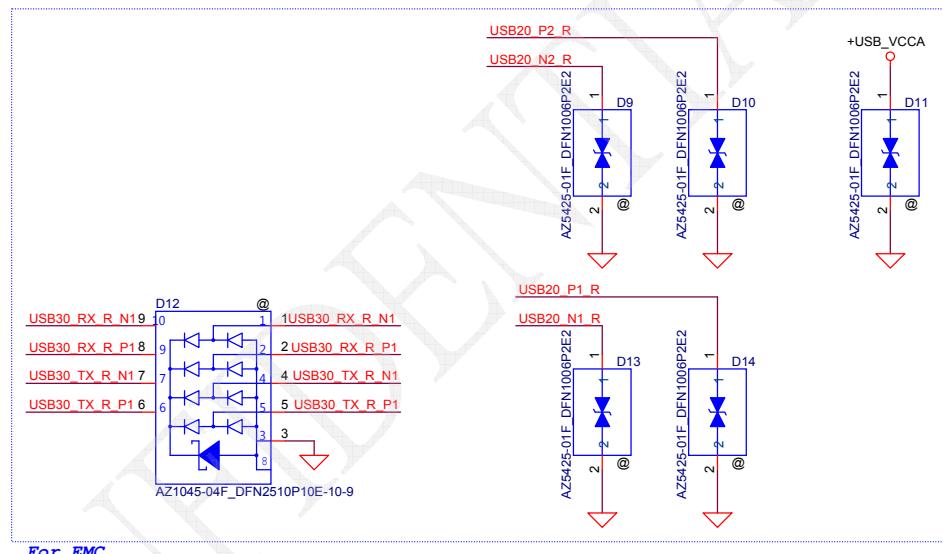
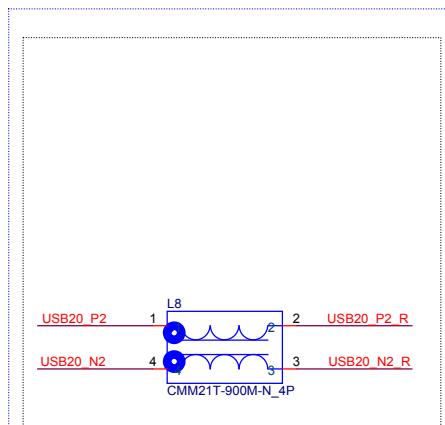
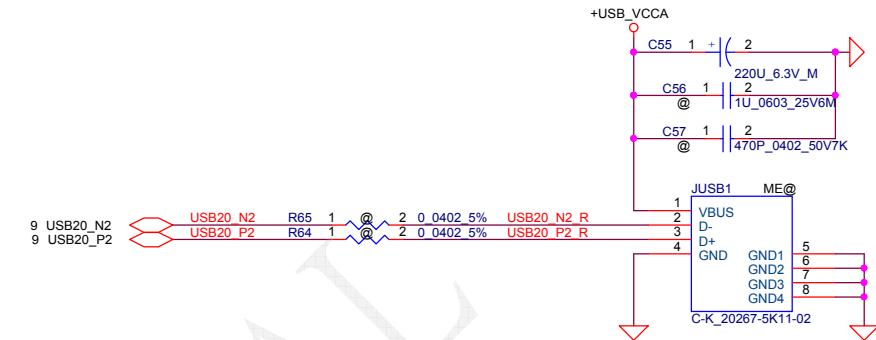
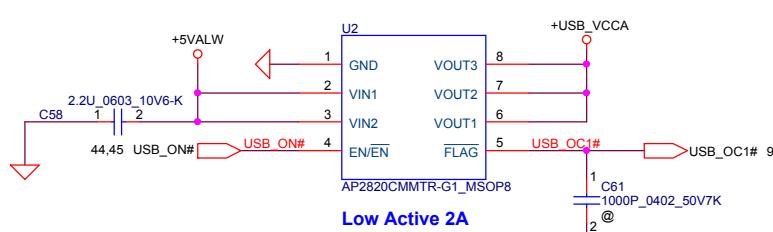
Security Classification	LC Future Center Secret Data			Title	Thermal sensor/FAN CONN		LCFC
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### **Mini-Express Card(WLAN/WiMAX)**



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## LEFT SIDE USB3.0 PORT X2



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2013/08/05

Title

USB2.0/USB3.0 PORT (LEFT)



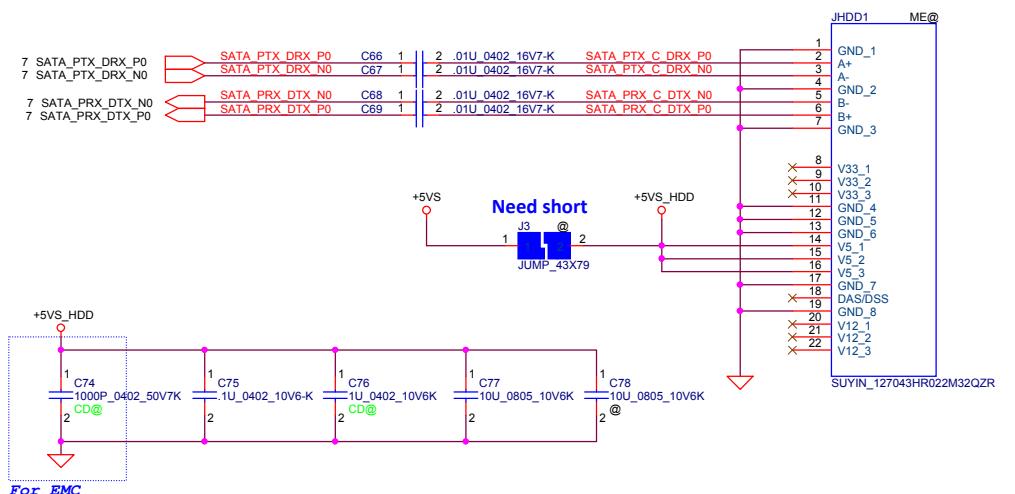
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Rev 1.0  
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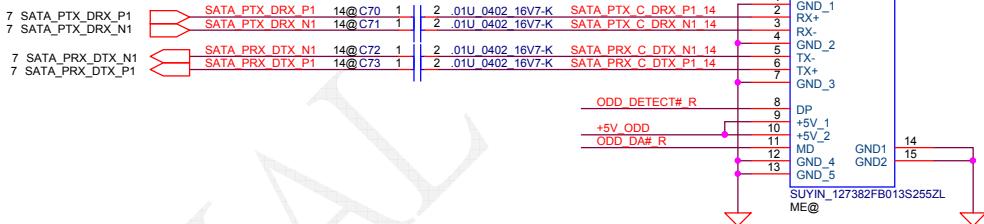
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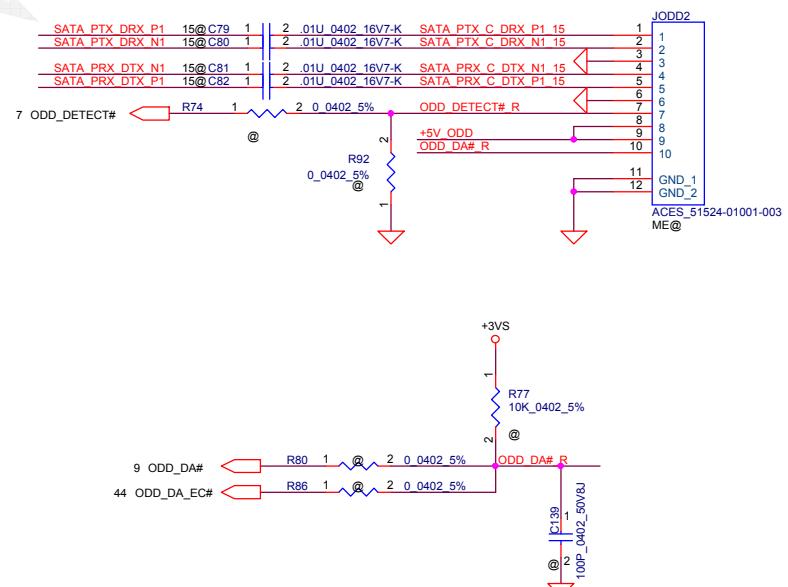
# SATA HDD Conn.



FOR 14"  
SATA ODD Conn.



FOR 15"  
SATA ODD FFC Conn



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HDD/ODD CONN



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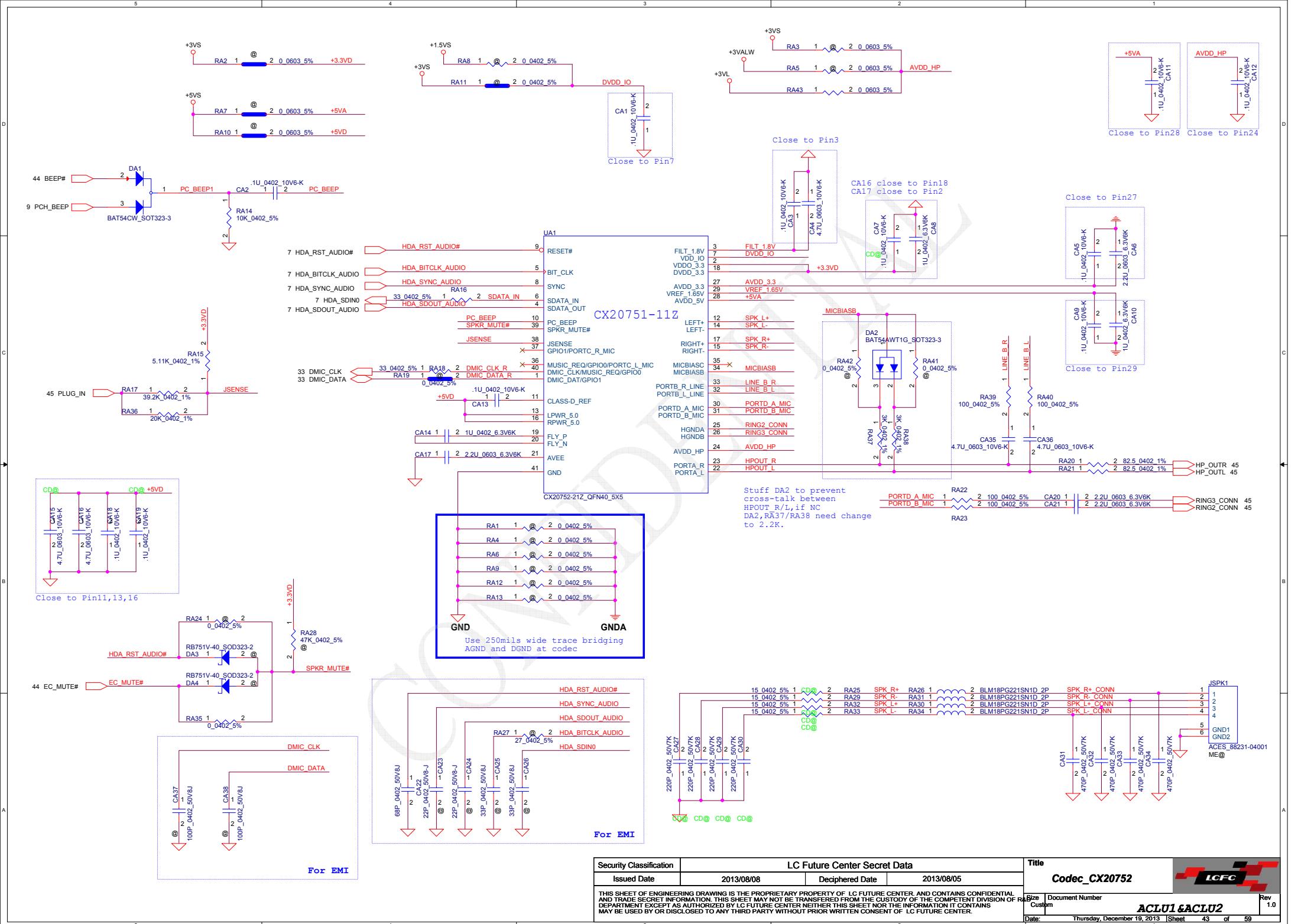
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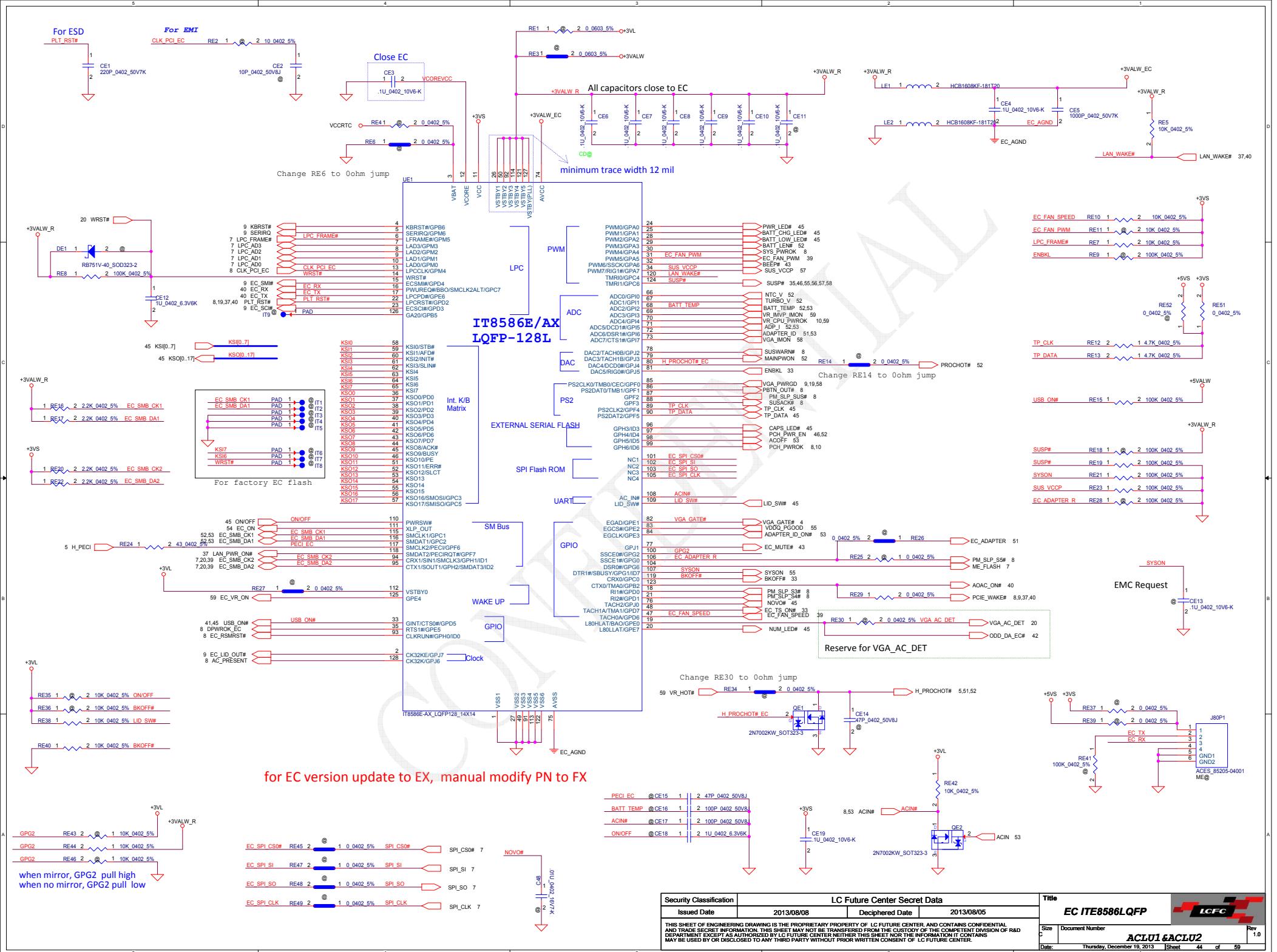
Sheet

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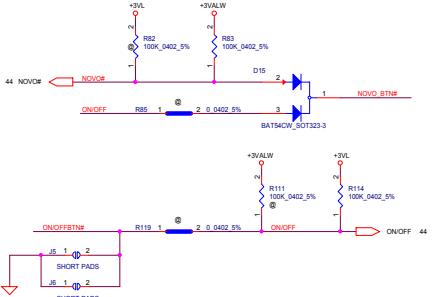
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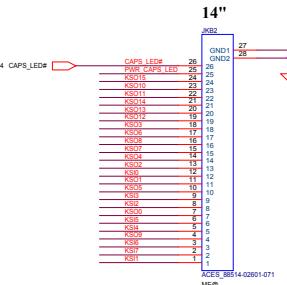




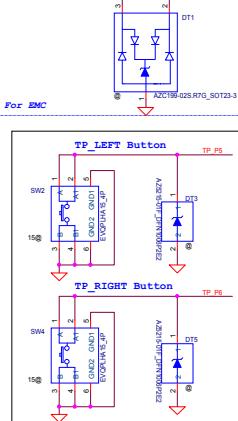
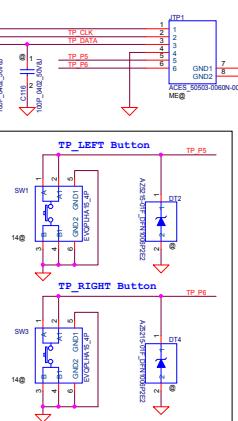
## ON/OFF switch



<b>KSD9_7)</b>	<b>KSD10_7)</b>	44	
<b>KSD9_11)</b>	<b>KSD10_11)</b>	44	
C117 1	2	100P 0402 50VJ	PWR_CAPS_LED C133 1
C118 1	2	100P 0402 50VJ	PWR_NUM_LED C134 1
C98 1	2	100P 0402 50VJ	KS016 C91 1
C92 1	2	100P 0402 50VJ	KS017 C98 1
C94 1	2	100P 0402 50VJ	KS01 C90 1
C96 1	2	100P 0402 50VJ	KS027 C93 1
C98 1	2	100P 0402 50VJ	KS02 C95 1
C100 1	2	100P 0402 50VJ	KS03 C97 1
C102 1	2	100P 0402 50VJ	KS04 C99 1
C104 1	2	100P 0402 50VJ	KS05 C101 1
C106 1	2	100P 0402 50VJ	KS07 C105 1
C108 1	2	100P 0402 50VJ	KS08 C107 1
C110 1	2	100P 0402 50VJ	KS14 C109 1
C112 1	2	100P 0402 50VJ	KS15 C111 1
			KS11 C113 1

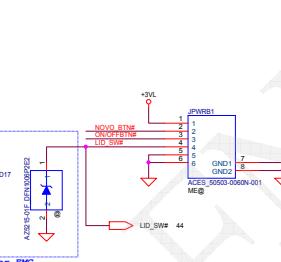


## **TP/B Connector**

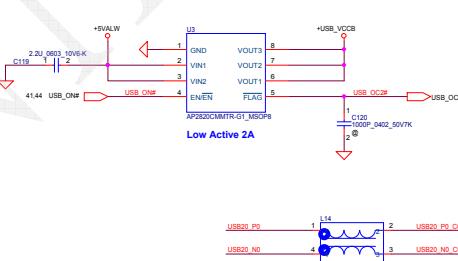


For 14"		For 15"	
1	VDD	1	VDD
2	CLK	2	CLK
3	DAT	3	DAT
4	GND	4	GND
5	TP-L	5	TP-L
6	TP-R	6	TP-R

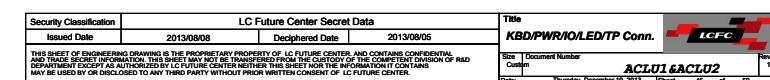
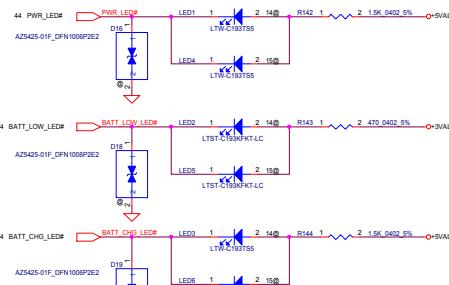
#### PWR/B Connector



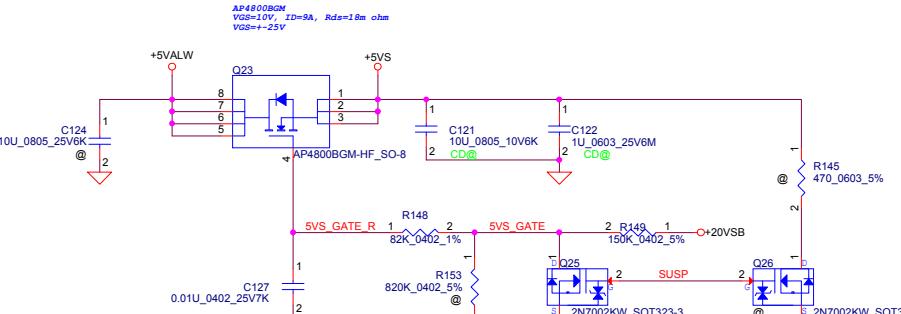
### **USB I/O Connector**



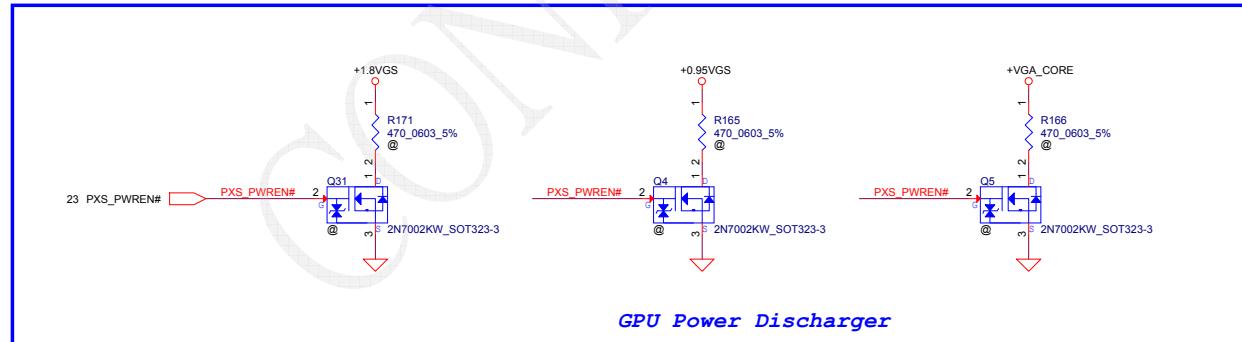
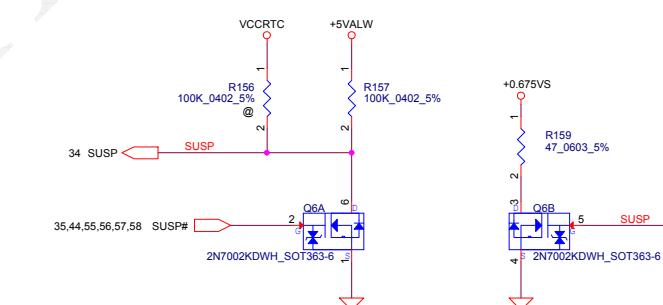
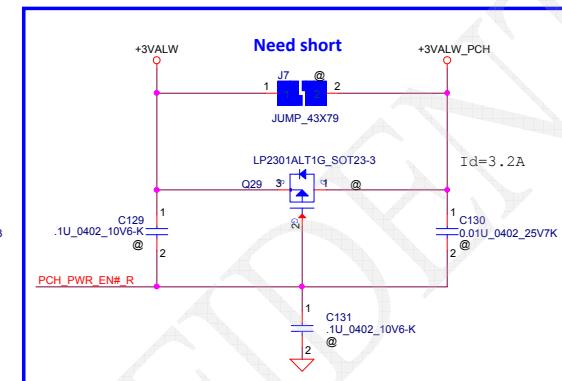
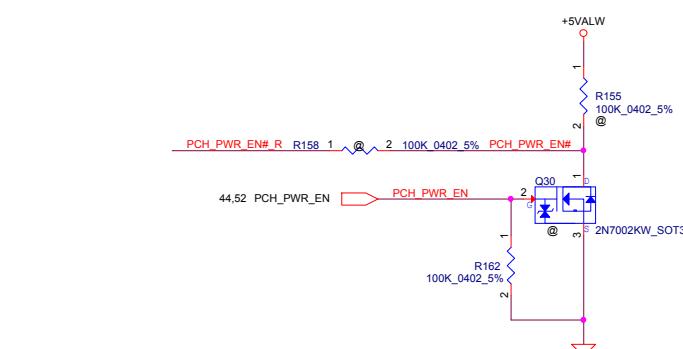
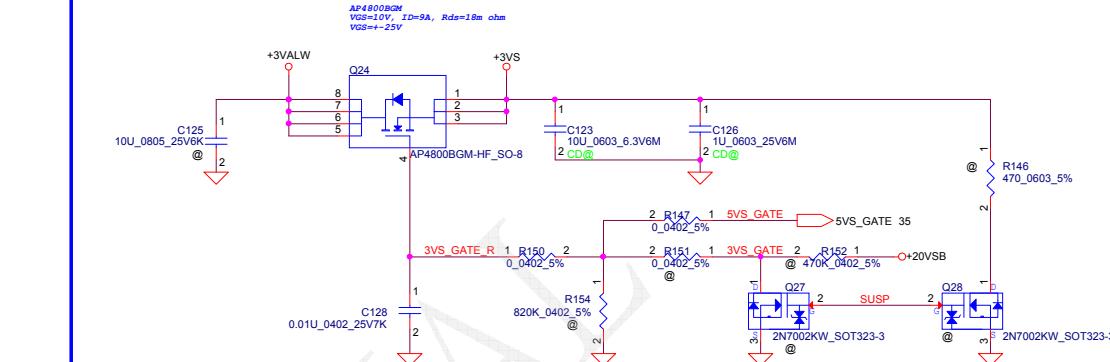
LED



+5VALW to +5VS



+3VALW to +3VS



Security Classification

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Title

DC V to VS INTERFACE



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2013/08/08

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Size

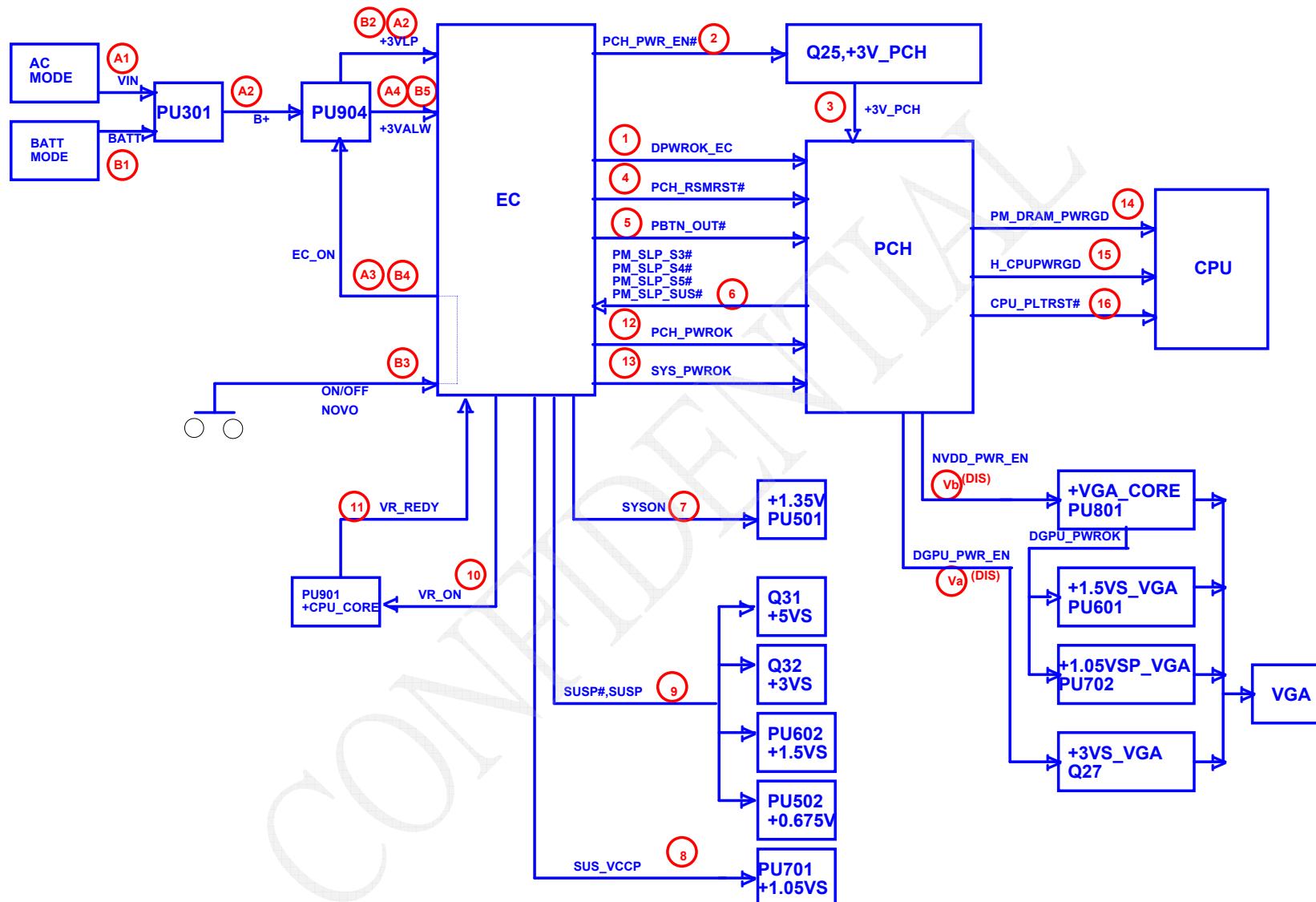
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Document Number

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Title

Power sequence Block



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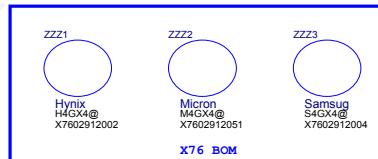
Rev 1.0

ACLU1 &amp; ACLU2

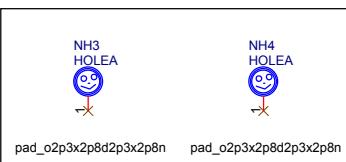
Date: Thursday, December 19, 2013 Sheet 47 of 59

UL1 RTL8106EUL-CG SA00006Q000 LAN chip	TL1 TST1284A LF SP050008C00 Transformer	UV1 JET@ AMD Jet-LE GPU SA000054J00	RV16 JET@ 0_0402_5% SD02800008J	RV19 JET@ 0_0402_5% SD02800008J	UV1 TOPAZ@ AMD Topaz-XT GPU SA000062R09	RV16 TOPAZ@ 100_0402_1% SD03410008J	RV19 TOPAZ@ 100_0402_1% SD03410008J	ZZZ4 14@ PCB PN DA20TG00200	ZZZ5 15@ PCB PN DA20TH00200
VRAM_Hynix_256M*16									
UV3 H4@ Hynix_H5TC4G63AFR-11C SA00005YLO0	UV4 H4@ Hynix_H5TC4G63AFR-11C SA00005YLO0	UV5 H4@ Hynix_H5TC4G63AFR-11C SA00005YLO0	UV6 H4@ Hynix_H5TC4G63AFR-11C SA00005YLO0						RV36 H4@ 4.75K_0402_1% SD03447518J
VRAM_Micron_256M*16									
UV3 M4@ Micron_MT41J256M16HA-093G SA00006010	UV4 M4@ Micron_MT41J256M16HA-093G SA00006010	UV5 M4@ Micron_MT41J256M16HA-093G SA00006010	UV6 M4@ Micron_MT41J256M16HA-093G SA00006010	RV33 M4@ 4.53K_0402_1% SD03445318J					
VRAM_Samsung_256M*16									
UV3 S4@ Samsung_K4W4G1646D-BC1A SA000063F10	UV4 S4@ Samsung_K4W4G1646D-BC1A SA000063F10	UV5 S4@ Samsung_K4W4G1646D-BC1A SA000063F10	UV6 S4@ Samsung_K4W4G1646D-BC1A SA000063F10	RV33 S4@ 8.45K_0402_1% SD000011R00					
VRAM_Samsung_256M*16									
UV3 S4@ Samsung_K4W4G1646D-BC1A SA000063F10	UV4 S4@ Samsung_K4W4G1646D-BC1A SA000063F10	UV5 S4@ Samsung_K4W4G1646D-BC1A SA000063F10	UV6 S4@ Samsung_K4W4G1646D-BC1A SA000063F10	RV33 S4@ 2K_0402_1% SD034200T8J					

Board ID					
BOARD_ID0	BOARD_ID1	BOARD_ID2	BOARD_ID3	Description	Stuff Resistor
0	0	0	0	14" + Jet-LE sku	RC107,RC108,RC109,RC12
0	1	0	0	15" + Jet-LE sku	RC107,RC101,RC109,RC12
1	0	0	0	14" + Topaz-XT sku	RC100,RC108,RC109,RC12
1	1	0	0	15" + Topaz-XT sku	RC100,RC101,RC109,RC12



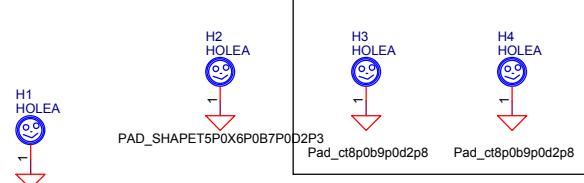
NH1  
HOLEA  
pad\_c2p3d2p3n



NH5  
HOLEA  
pad\_c2p3d2p3n

### PCB Fiducial Mark PAD

FD1  
FD2  
FD3  
FD4  
FD5  
FD6



H5  
HOLEA  
pad\_shapet8p8x8p0cb9p0d2p8

H6  
HOLEA  
pad\_shapet8p8x8p0cb9p0d2p8

H7  
HOLEA  
PAD\_CT6P5B5P0D4P0

H8  
HOLEA  
PAD\_CT6P5B5P0D4P0

H9  
HOLEA  
PAD\_CT6P5B5P0D4P0

H10  
HOLEA  
PAD\_CT6P5B5P0D4P0

H11  
HOLEA  
pad\_ct6p0d4p3

H12  
HOLEA  
Pad\_ct6p0b8p0d4p6

pad\_SHT7P0X7P05BR10P65X10P3D2P8

H13  
HOLEA  
pad\_cb8p0d7p0

H14  
HOLEA  
pad\_ct6p0shapeb8p0x6p75d2p3

H15  
HOLEA  
PAD\_CT6P0shapeb10p04x10p0d2p8

H16  
HOLEA  
pad\_ct6p0b7p0d2p3

H17  
HOLEA  
pad\_shapef6p8x8p0cb8p0d2p5

H18  
HOLEA  
PAD\_ShapeT5P0X6P0-D

H19  
HOLEA  
PAD\_shapeT5P0X6P0-U

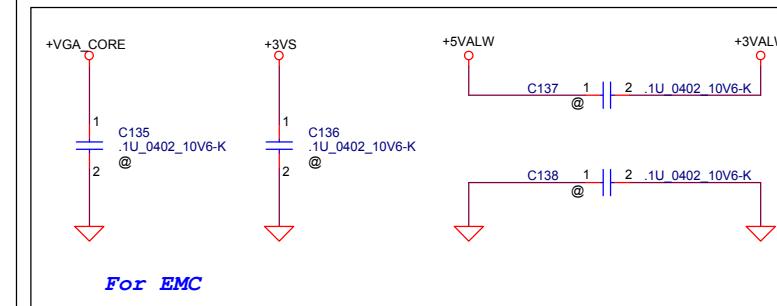
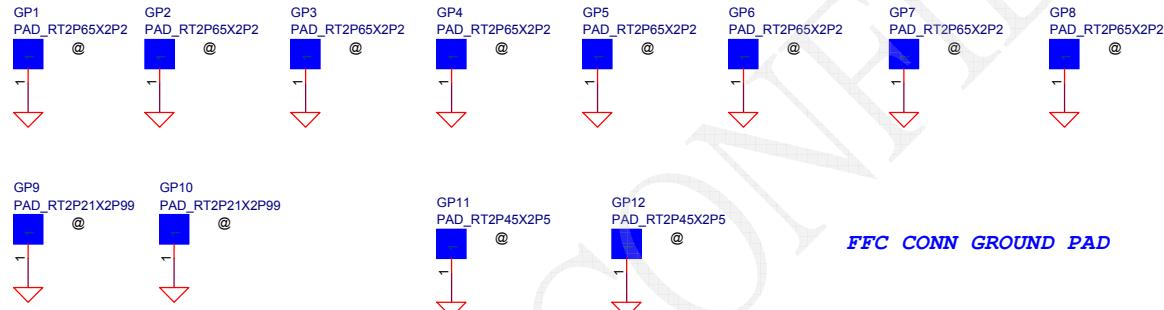
H20  
HOLEA  
pad\_ct5p5b6p0d3p3

H22  
HOLEA  
pad\_ct5p5b6p0d3p3

H23  
HOLEA  
pad\_ct5p5b6p0d3p3

H24  
HOLEA  
pad\_ct5p5b6p0d3p3

H21  
HOLEA  
CHASSIS1\_GND  
pad\_ct5p5b8p0d2p5



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Issued Date

2013/08/08

### LC Future Center Secret Data

Deciphered Date

2013/08/05

### Title

Hole



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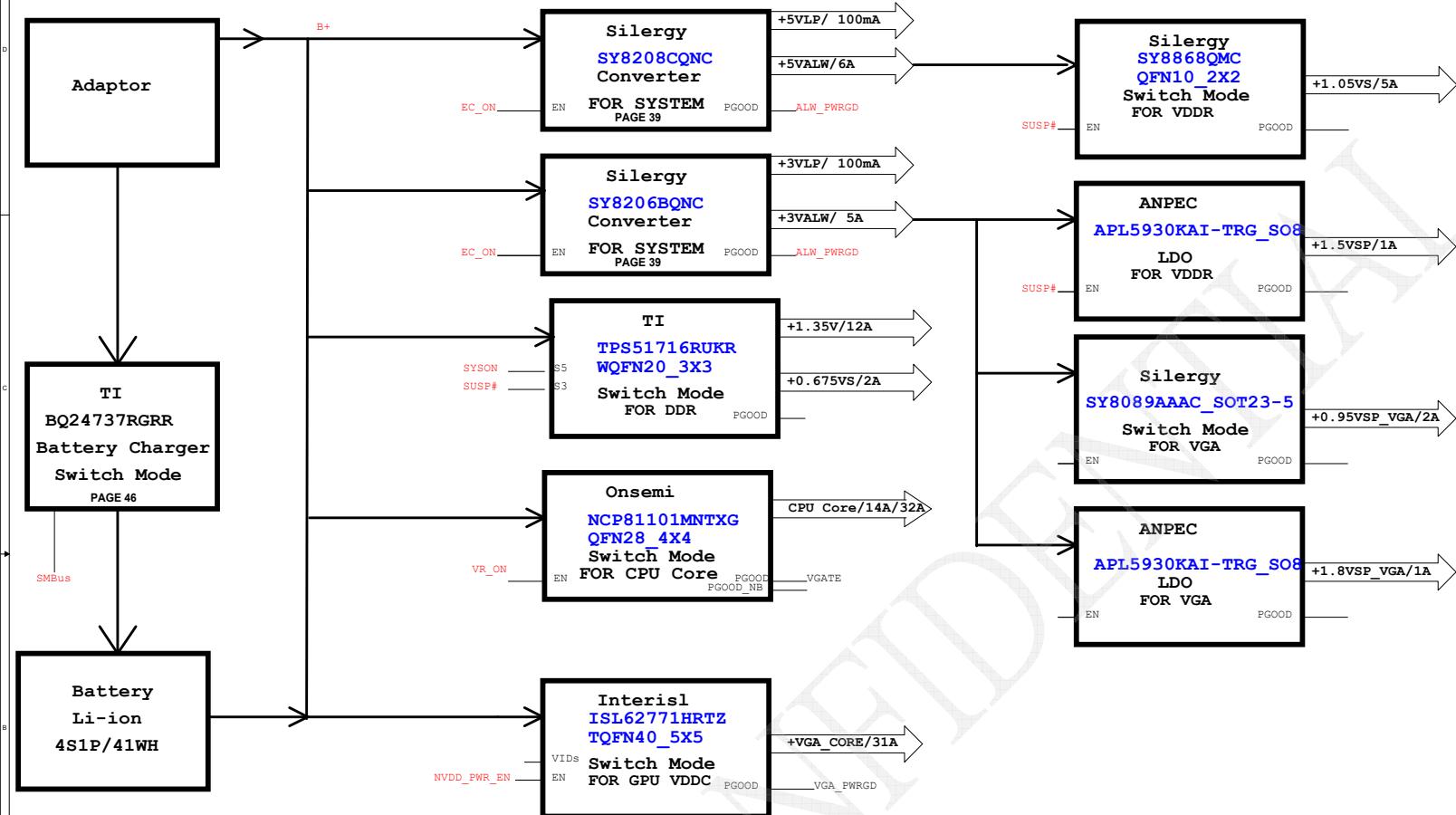
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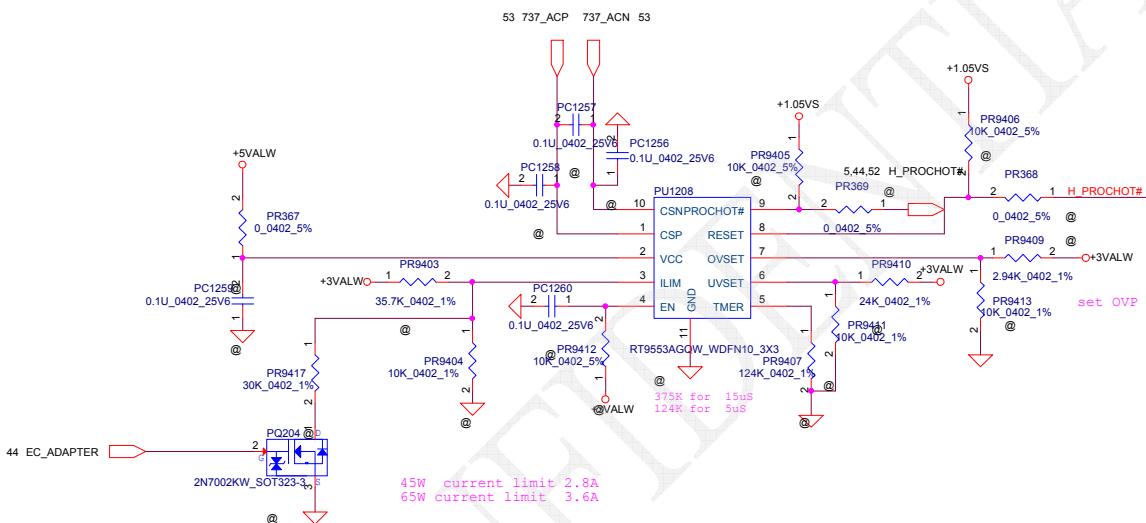
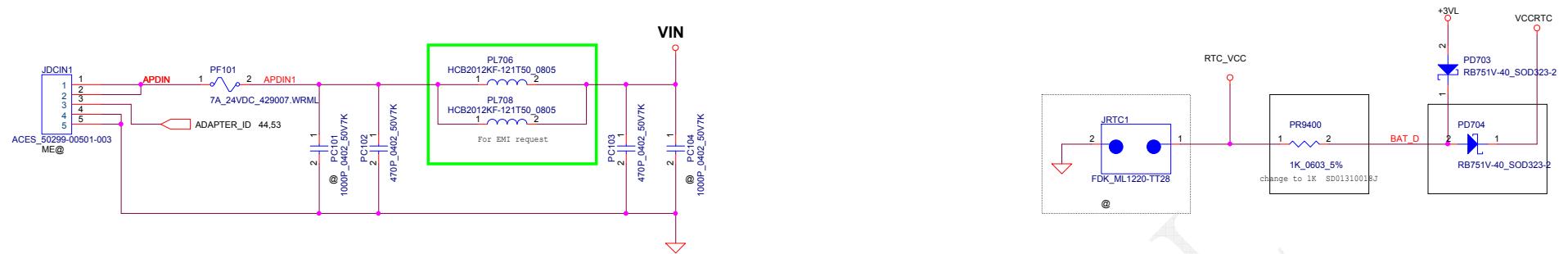
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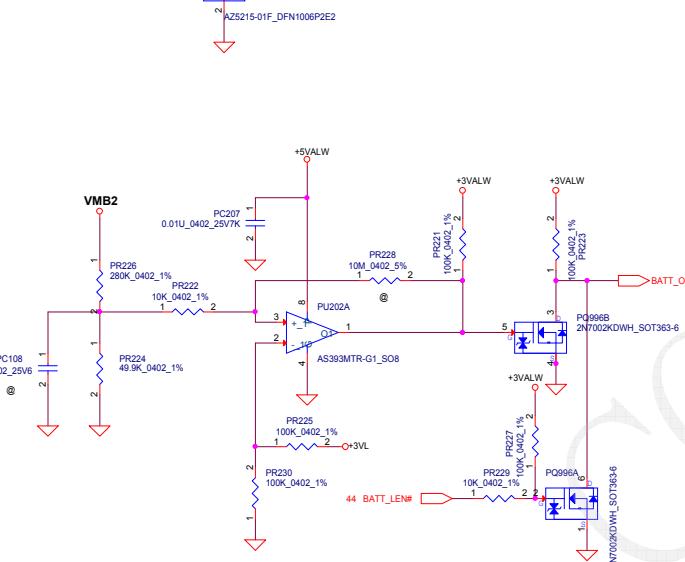
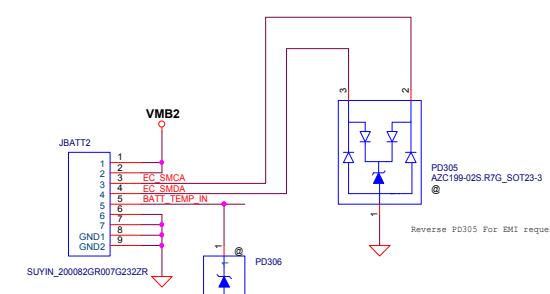
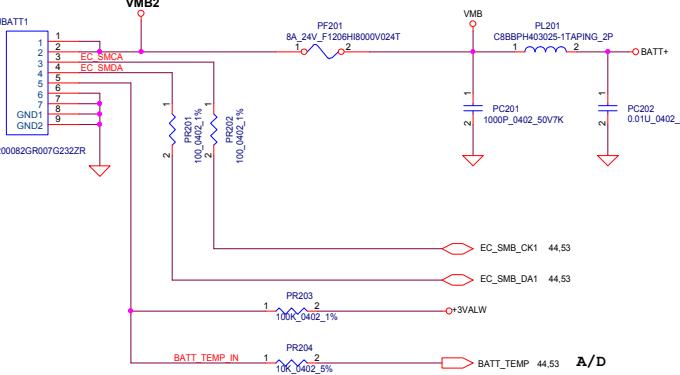
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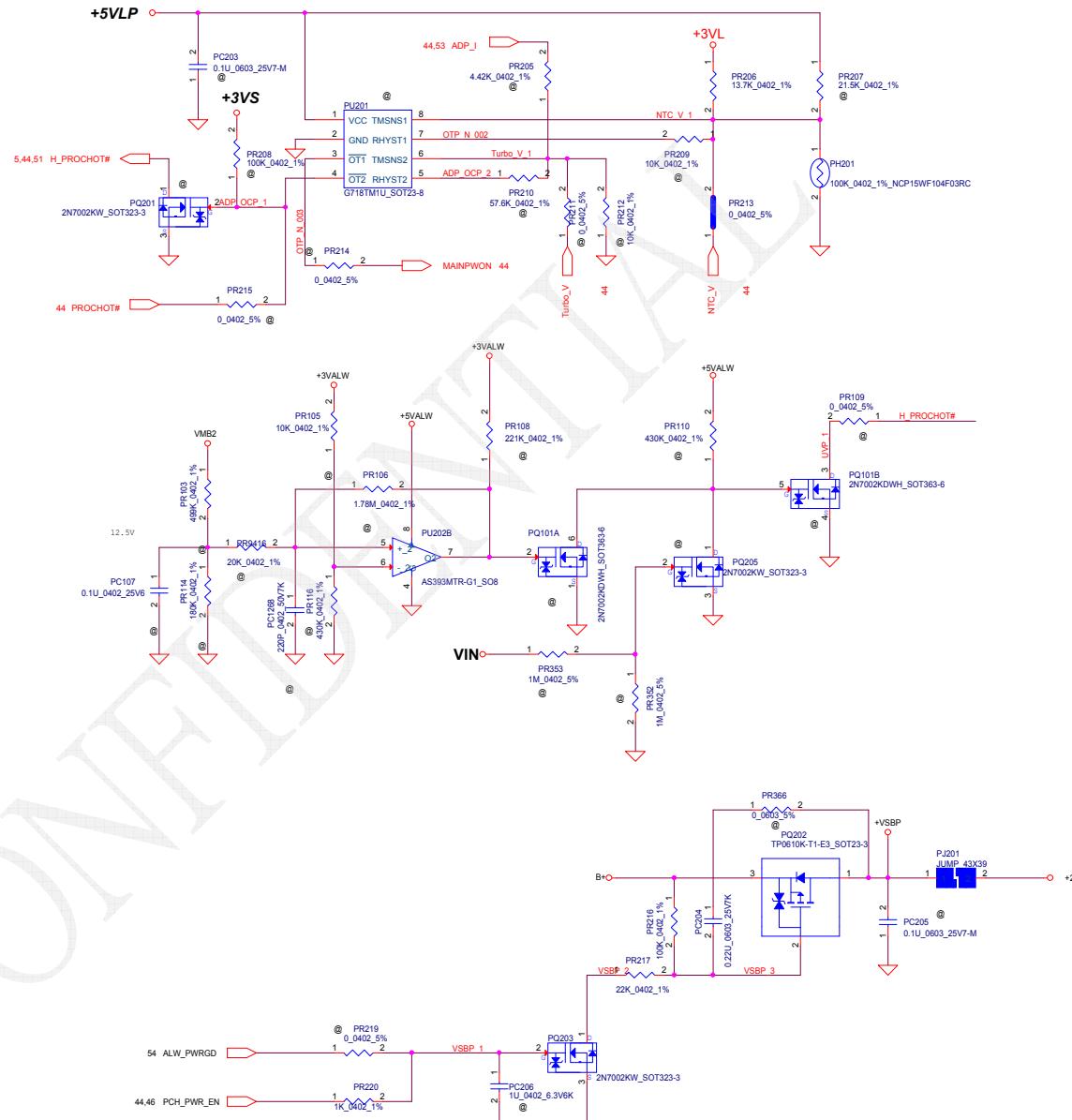




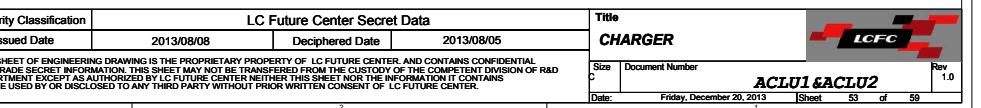
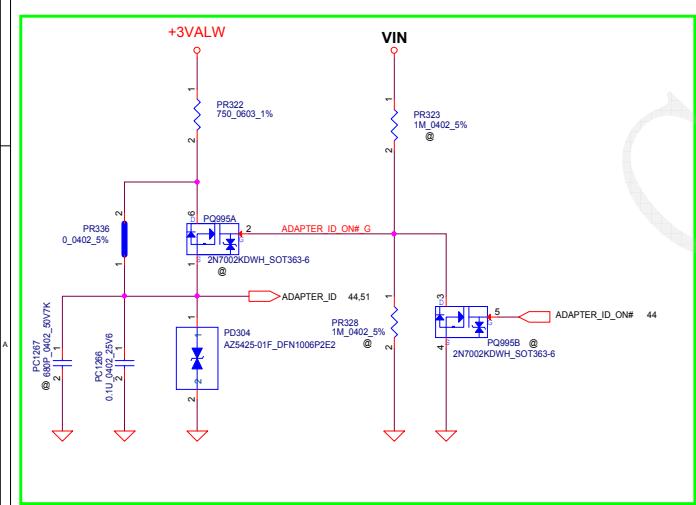
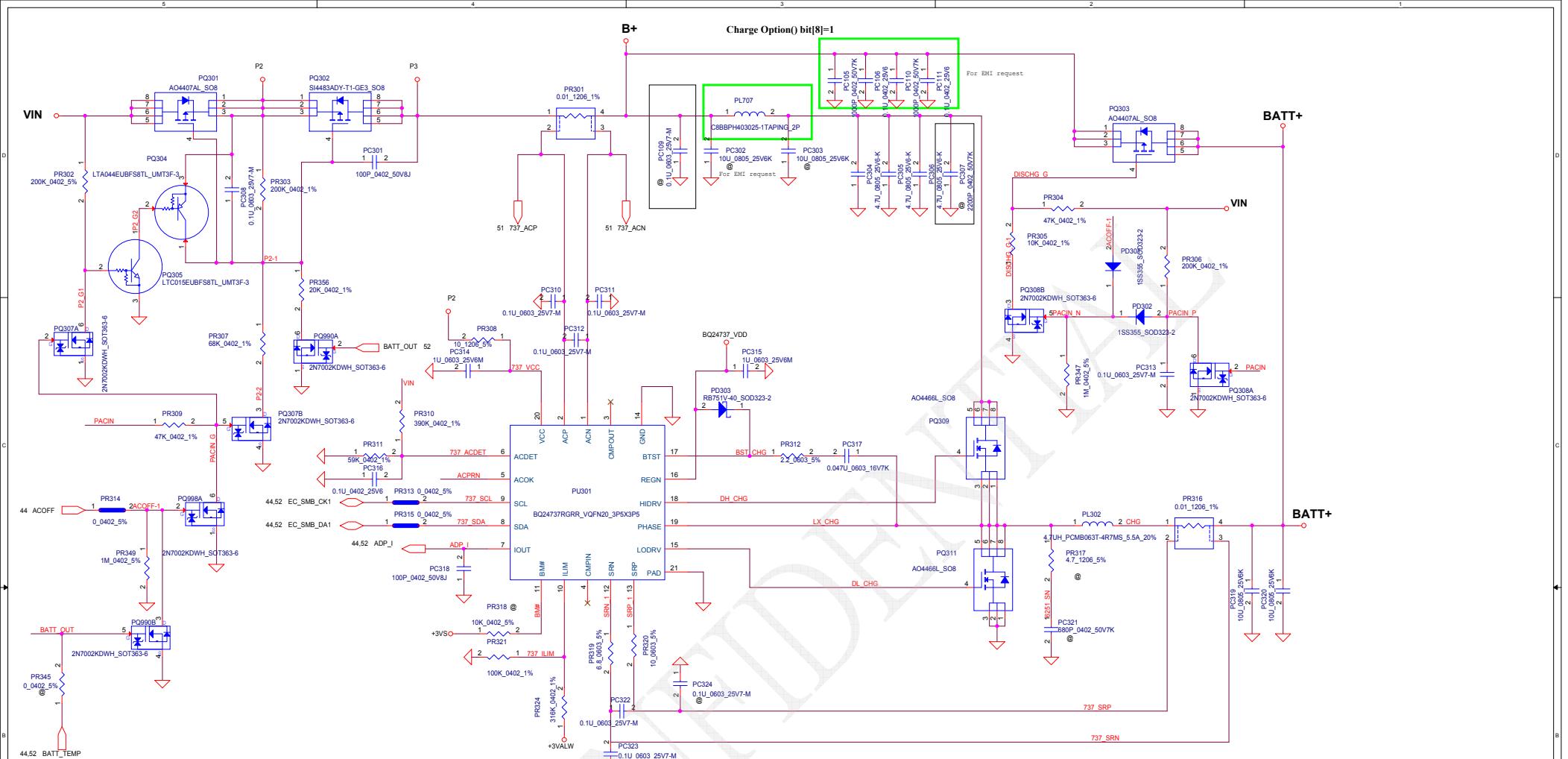
*PH201 under CPU botton side :  
CPU thermal protection at 92+-3 degree  
Recovery at 56 +-3 degree C*

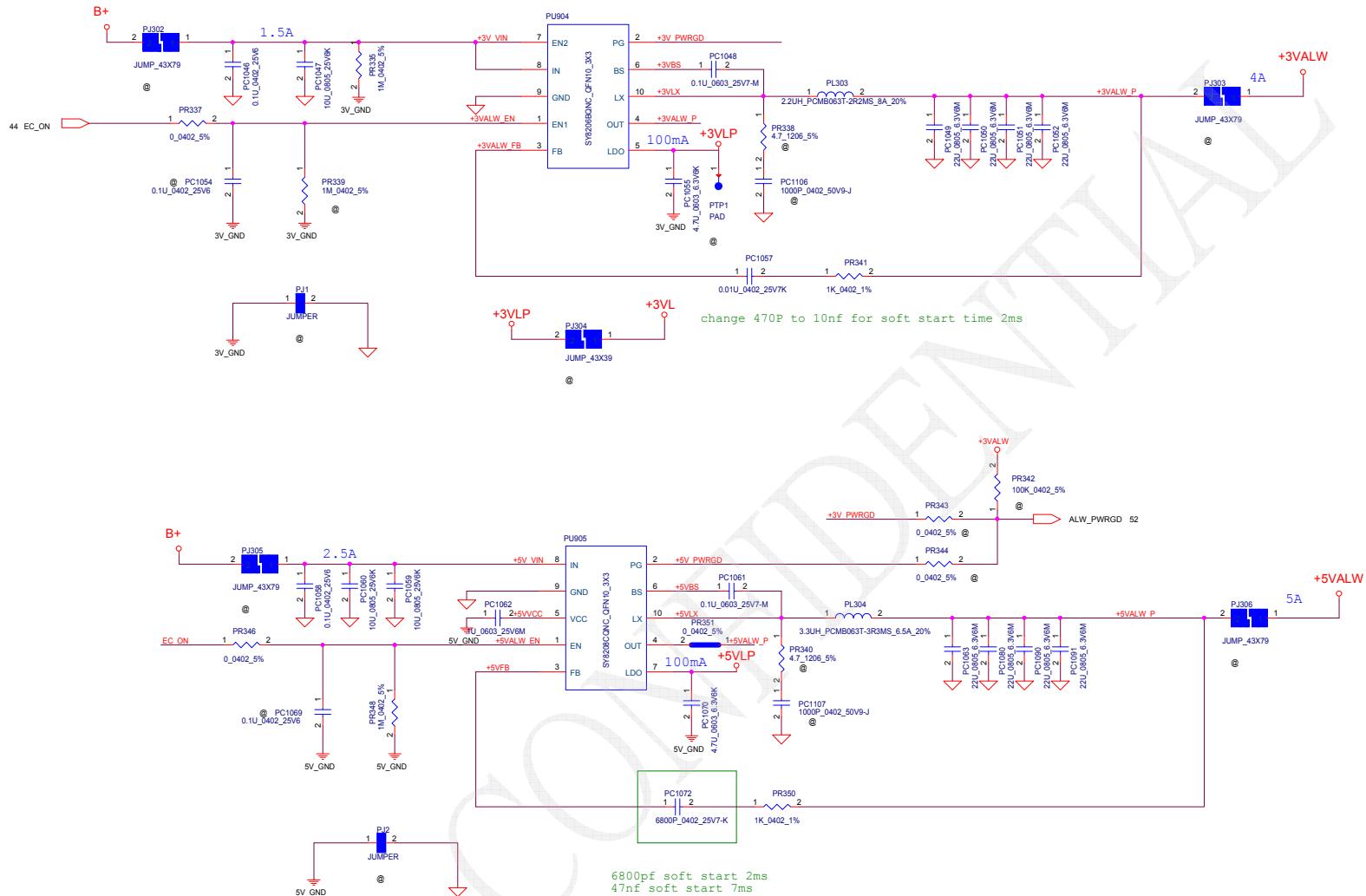
*For KB930 --> Keep PU1 circuit  
(Vth = 0.825V)*

**For KB9012 (Red square) --> Remove PU201 circuit, but keep PR201, PR205, PR211, PQ201, PR208, PR212**

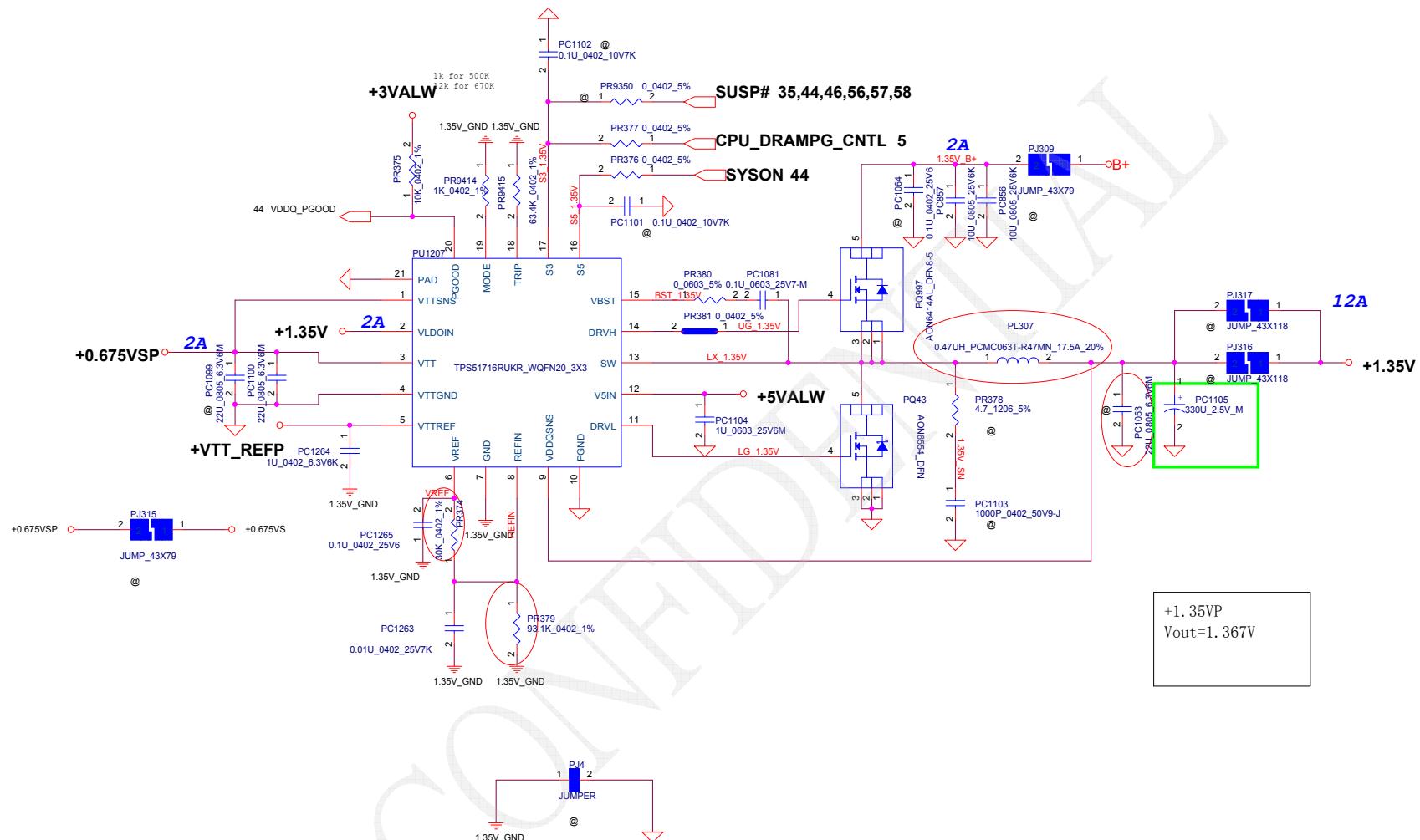


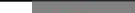
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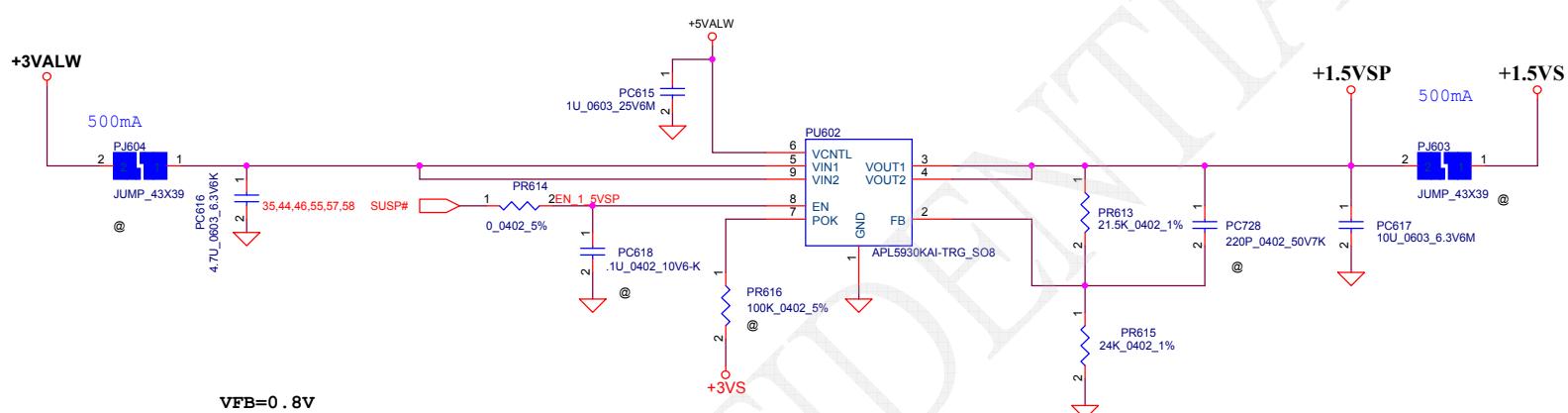




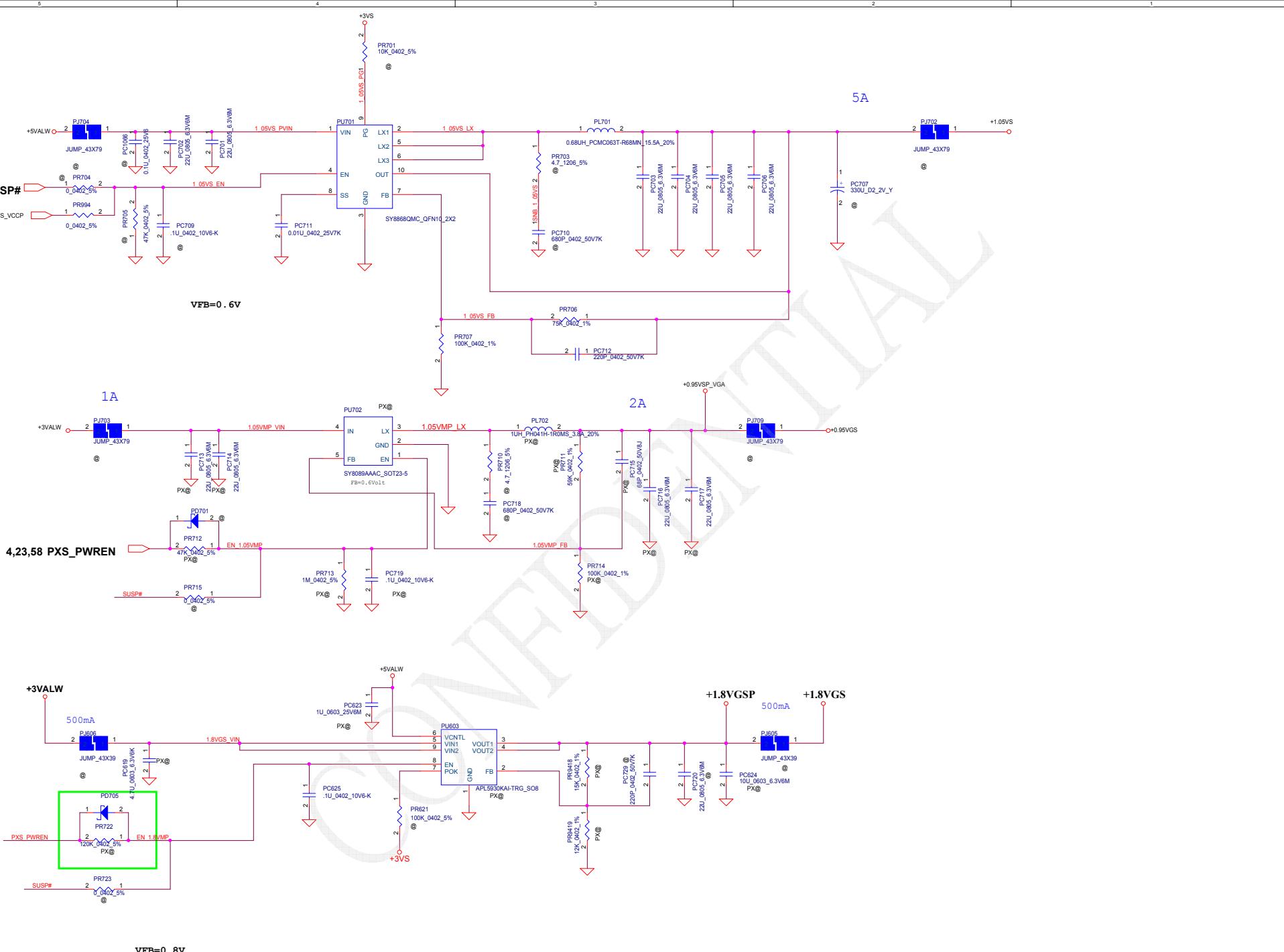
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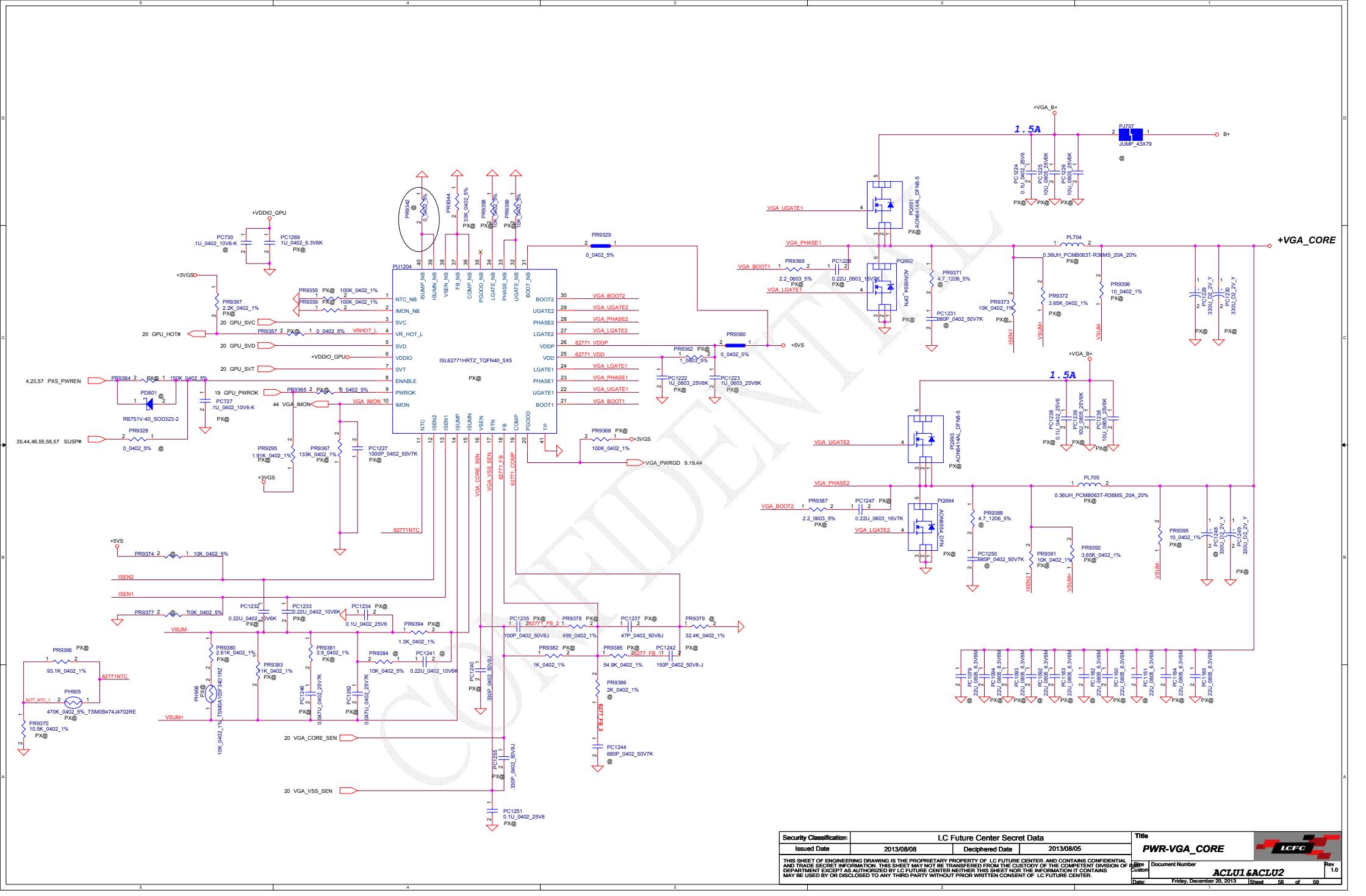
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custom				ACLU1&ACLU2		1.0
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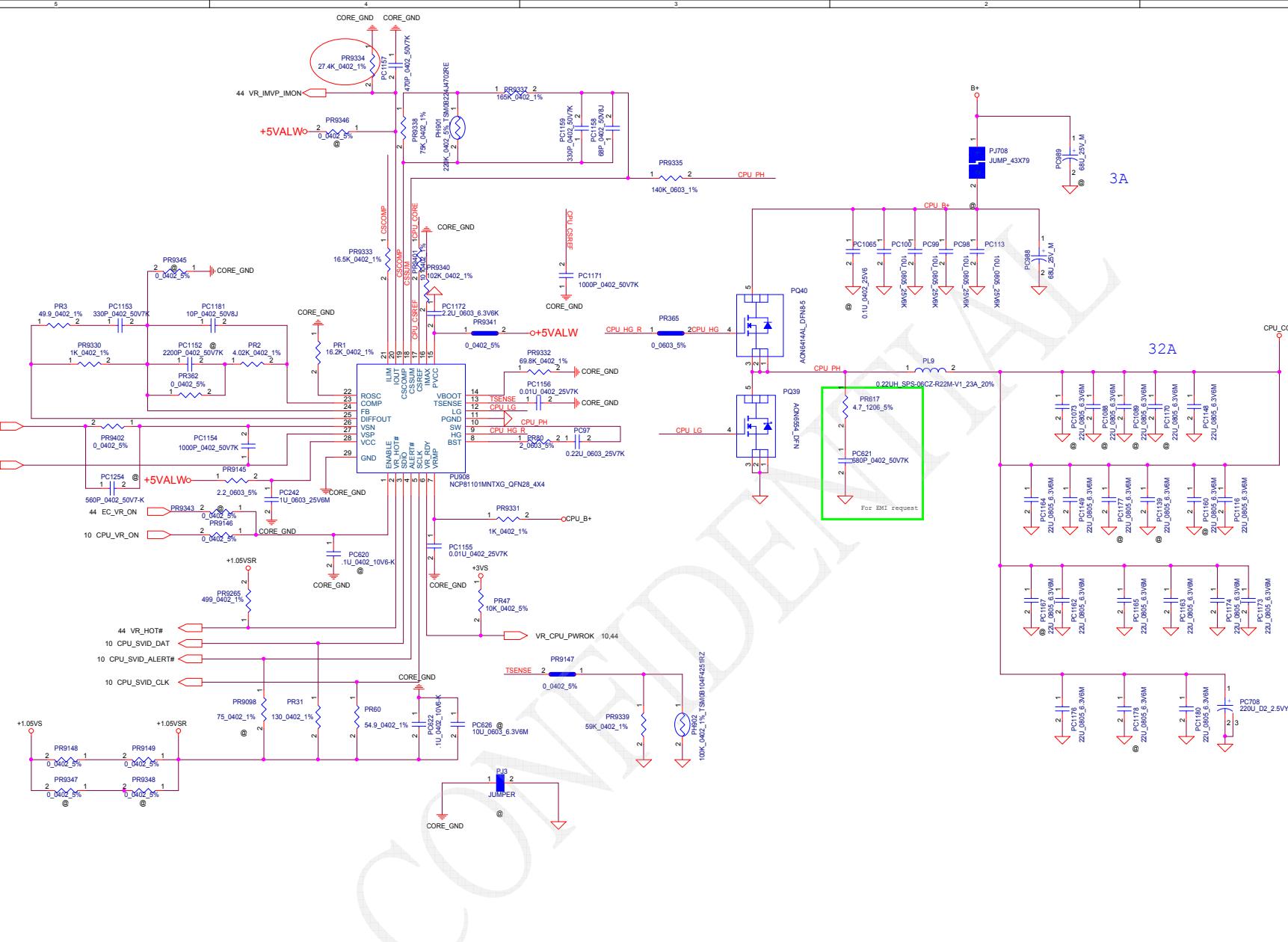


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