

EA40_HU_ULT

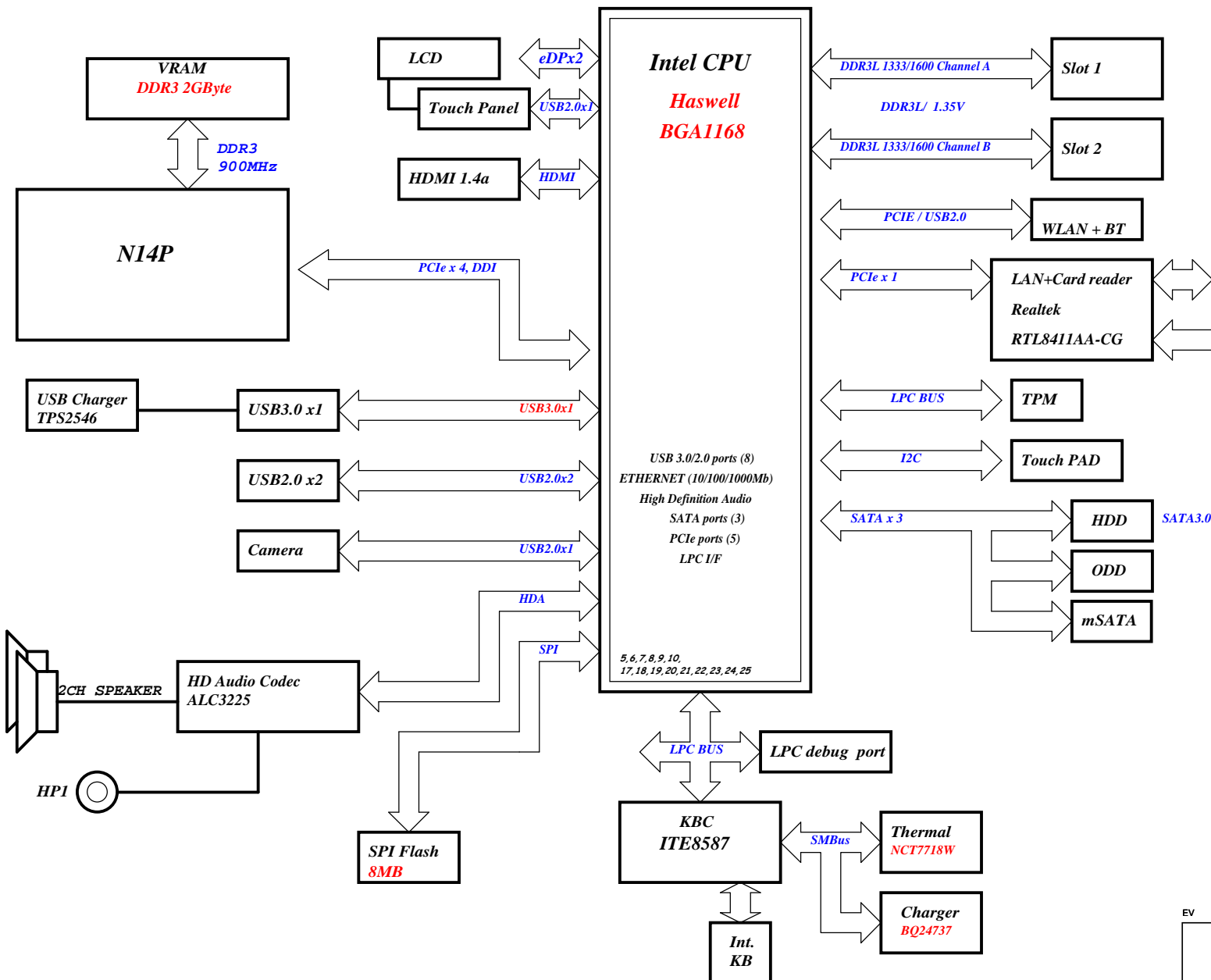
Schematics Document

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Title					
Cover Page					
Size A3	Document Number				Rev
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EA40-HW ULV Board Block Diagram

Project code : 91.4YN01.001
PCB P/N : 12243
Revision : 1



CHARGER	
BQ24737	44
INPUTS	OUTPUTS
DCBATOUT	BT+
SYSTEM DC/DC	
TPS51225	45
INPUTS	OUTPUTS
DCBATOUT	5V_Charger
	3D3V_S5
CPU DC/DC	
TPS51622	46-47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE
SYSTEM DC/DC	
SY8208A	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT
SYSTEM DC/DC	
RT8207	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3
SYSTEM DC/DC	
SYW232	50
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0
SYSTEM DC/DC	
SYW232	51
INPUTS	OUTPUTS
DCBATOUT	1D5V_S0
TPS51728RHAR	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE
Switches	
INPUTS	OUTPUTS
3D3V_S0	3D3V_VGA_S0
1D8V_S0	1D8V_VGA_S0
1V_S0	1V_VGA_S0
TPS51728RHAR	
INPUTS	OUTPUTS
DCBATOUT	1D5V_VGA_S0
PCB LAYER	
L1:Top	L4:Signal
L2:VCC	L5:GND
L3:Signal	L6:Bottom

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Block Diagram	
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SSTN = CPU

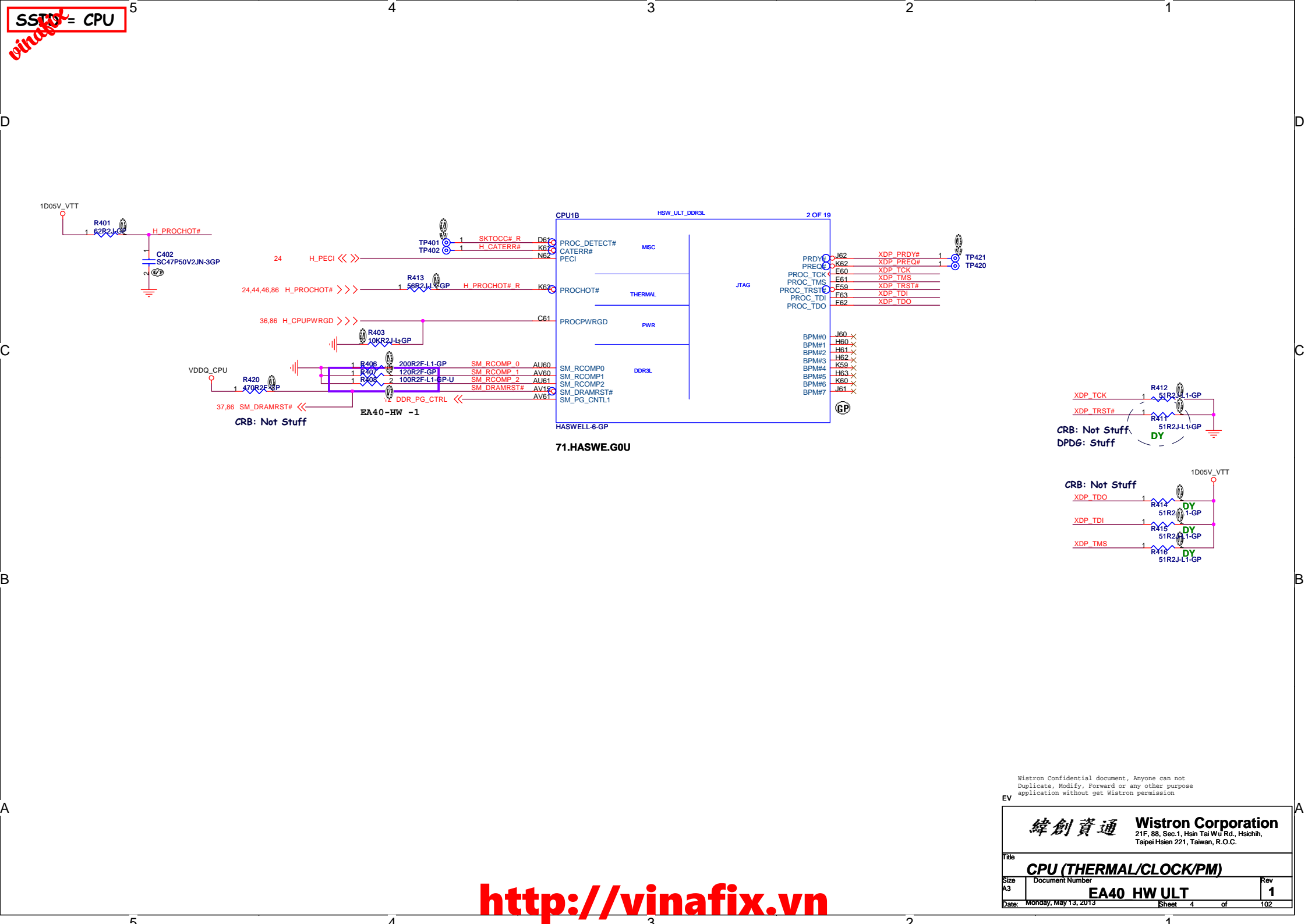
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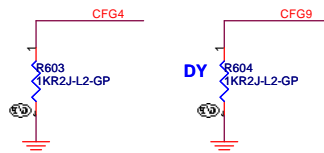
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CPU (Reserved)			
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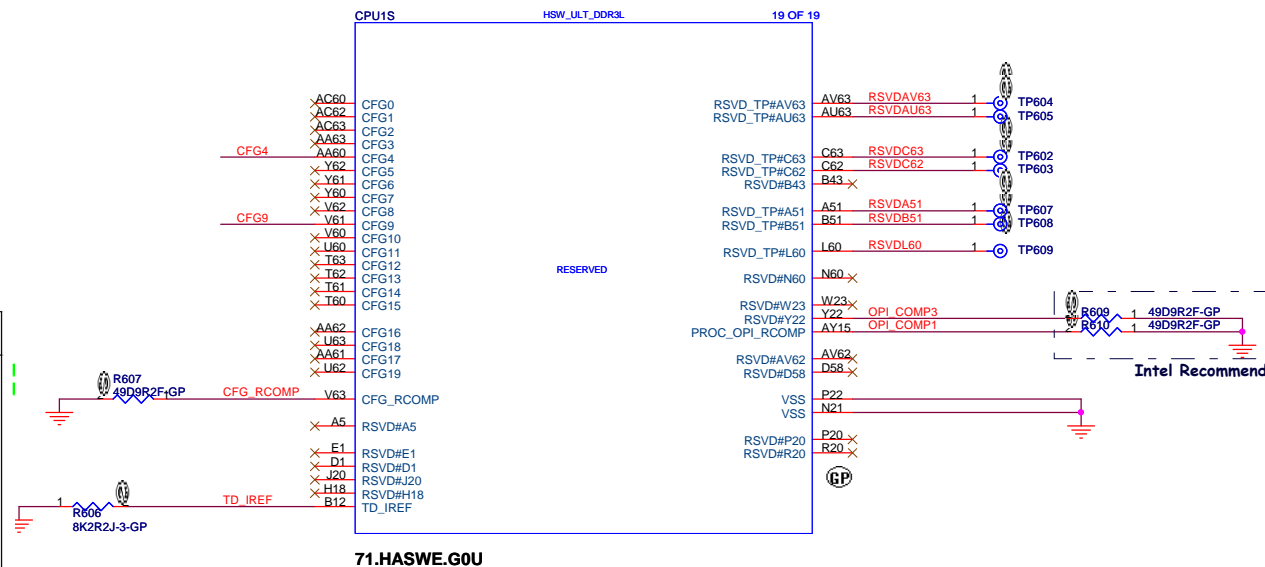


RSVD = CPU

eDP Enable	1:Disable
CFG4	0:Enable



Signal Name	Description	Direction/Buffer Type
CFG[19:0]	Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired. <ul style="list-style-type: none">CFG[3:0]: Reserved configuration lane. A test point may be placed on the board for these lanes.PCI Express* Static x16 Lane Numbering Reversal.——• CFG[4]: eDP enable<ul style="list-style-type: none">1 = Disabled0 = Enabled[19:5]: Reserved configuration lanes. A test point may be placed on the board for these lands.	I/O GTL
CFG_RCOMP	Configuration resistance compensation.	—
FC_x	FC signals are signals that are available for compatibility with other processors. A test point may be placed on the board for these lands. Refer to the appropriate platform design guide for implementation details.	
continued...		



7.4 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD – these signals should not be connected
- RSVD_TP – these signals should be routed to a test point
- RSVD_NCTF – these signals are non-critical to function and may be left unconnected

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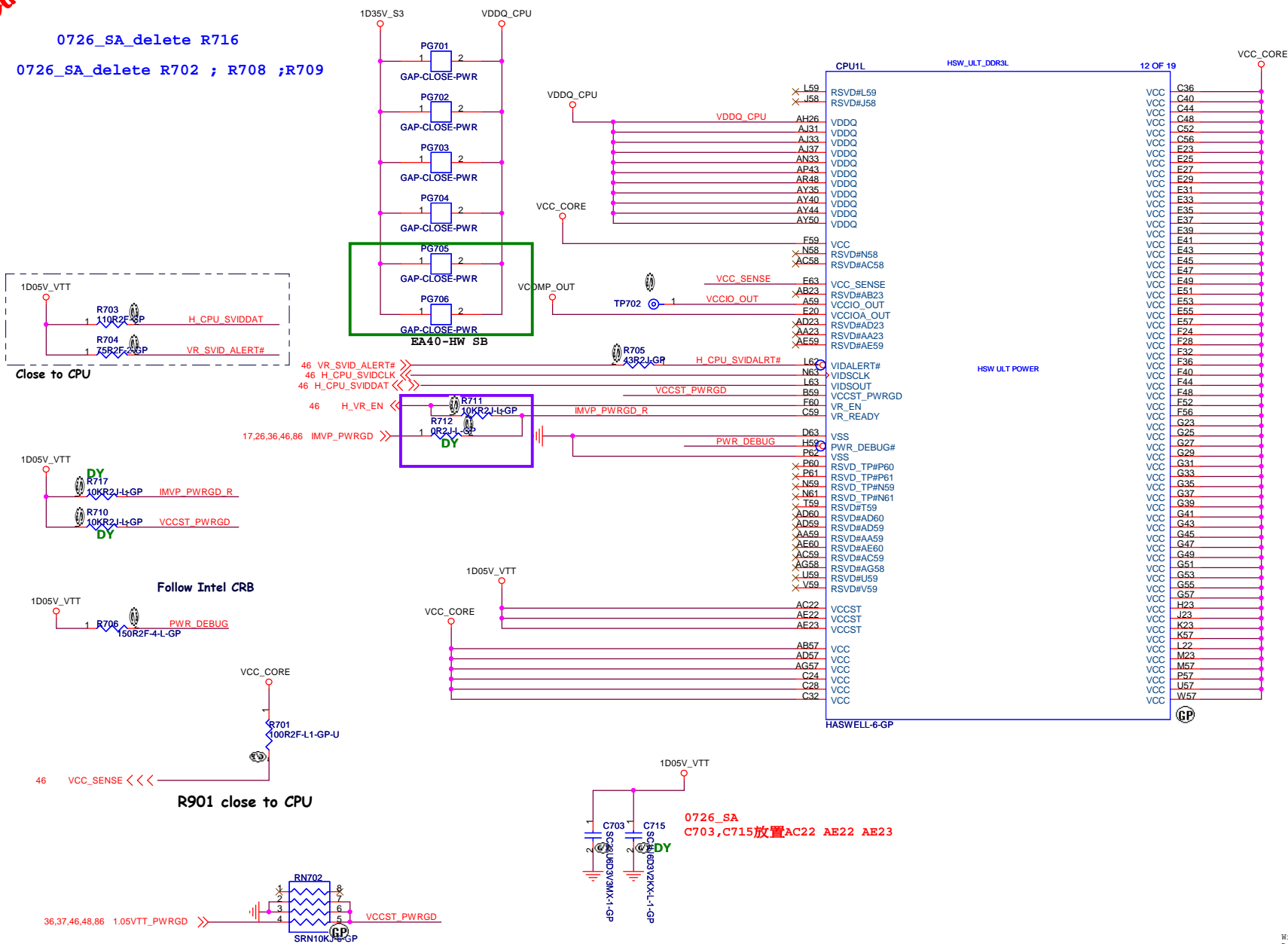
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CPU (CFG)			
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SSD = CPU

0726_SA_delete R716

```
0726_SA_delete R702 ; R708 ;R709
```



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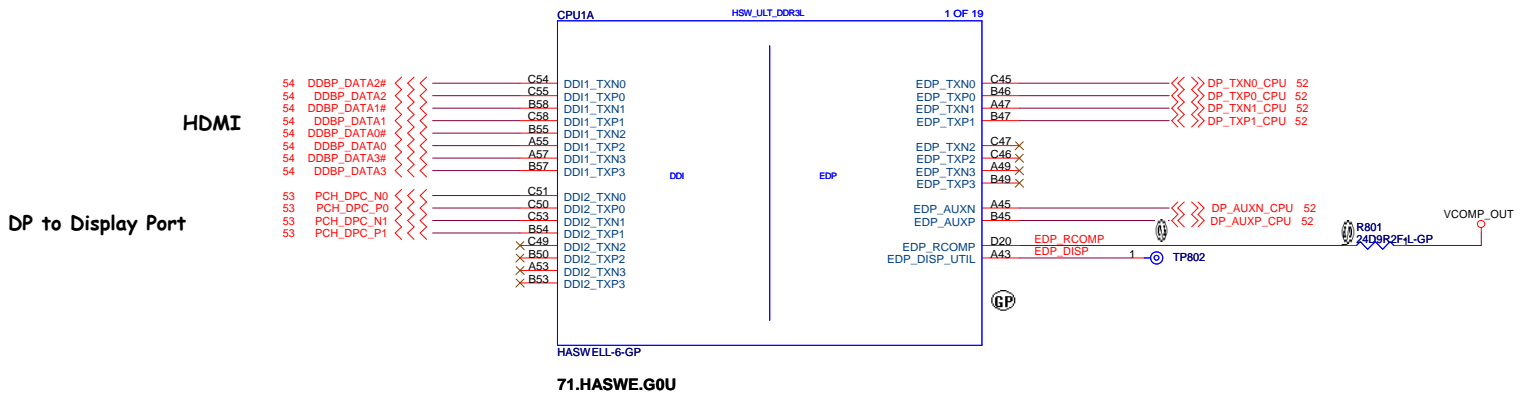
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CPU (VCC CORE)			
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SS not = CPU

win10

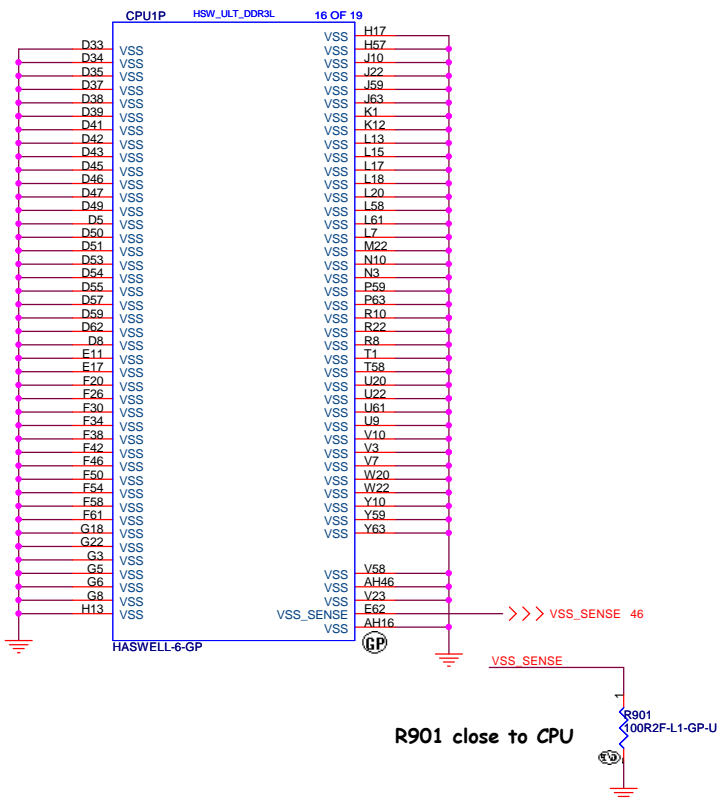


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Title CPU (DDI/EDP)		
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SSD = CPU

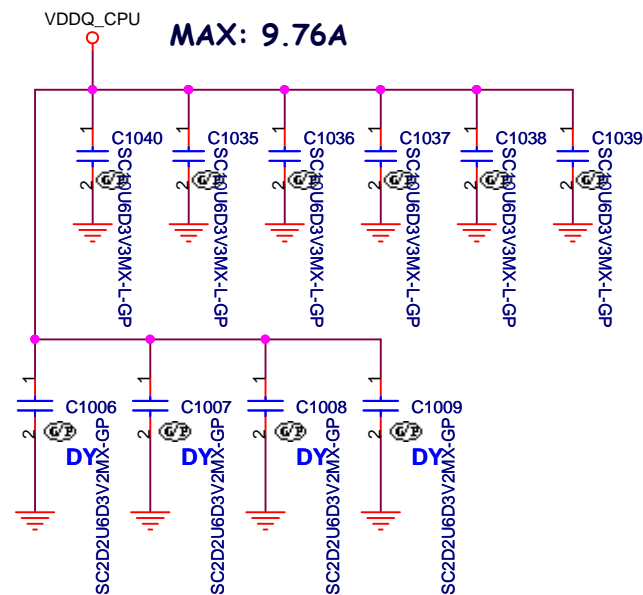


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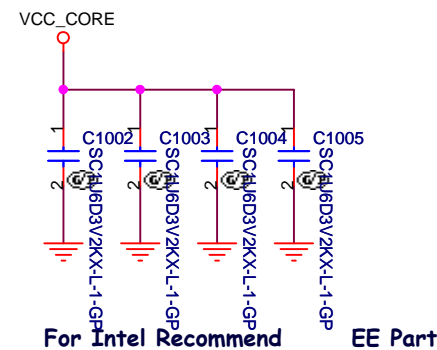
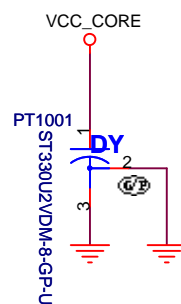
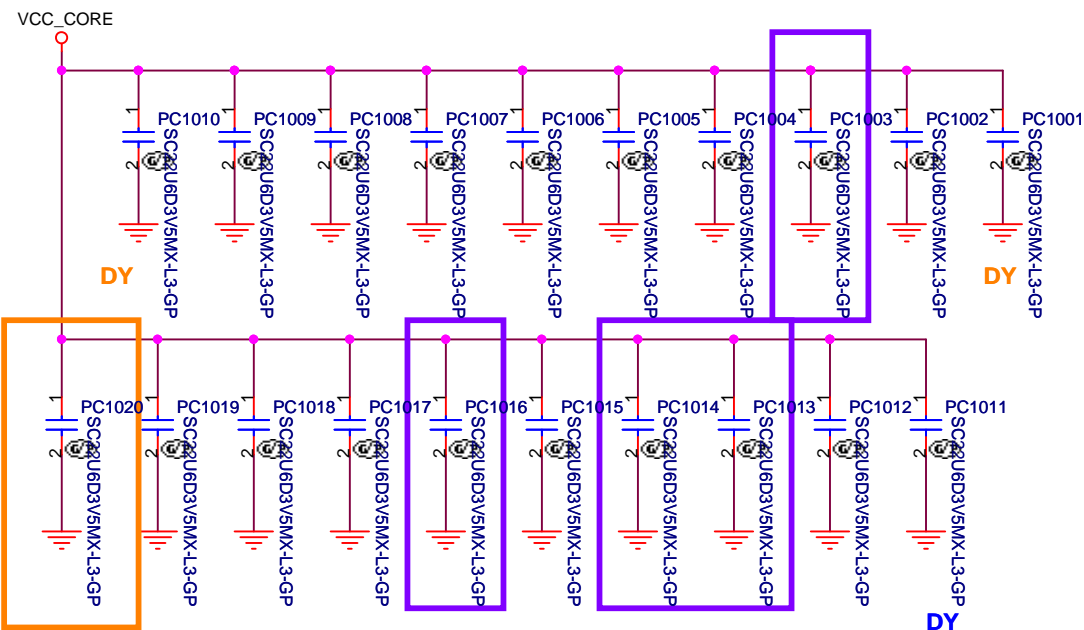
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For Intel Recommend EE Part



For Intel Recommend EE Part

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Title		
CPU (Power CAP1)		
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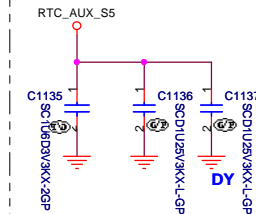
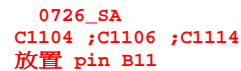
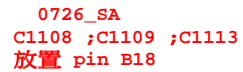
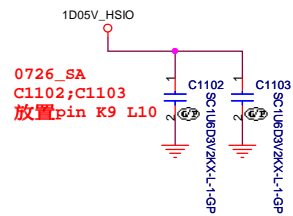
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0726_SA 擺放電容的位置請參考Page 21
每個位置如下

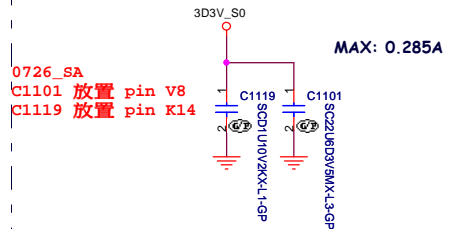
MAX: 1.92A

0726_SA DY C1137

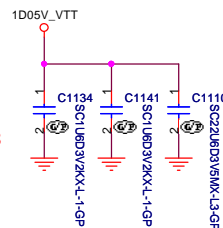
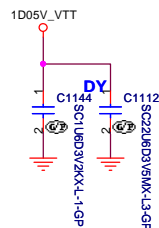
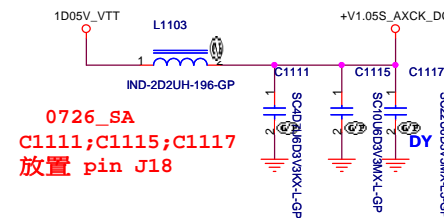
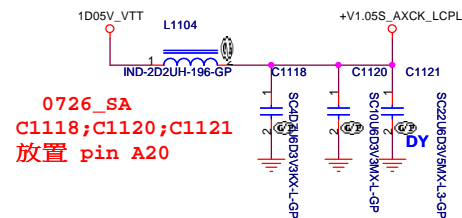


```
0726_SA
C1135;C1136;C1137
放置 pin AG10
```

MAX: 3.51A



MAX: 0.285A



```
0726_SA
C1122;C1123;C1124
放置 pin AA21
```

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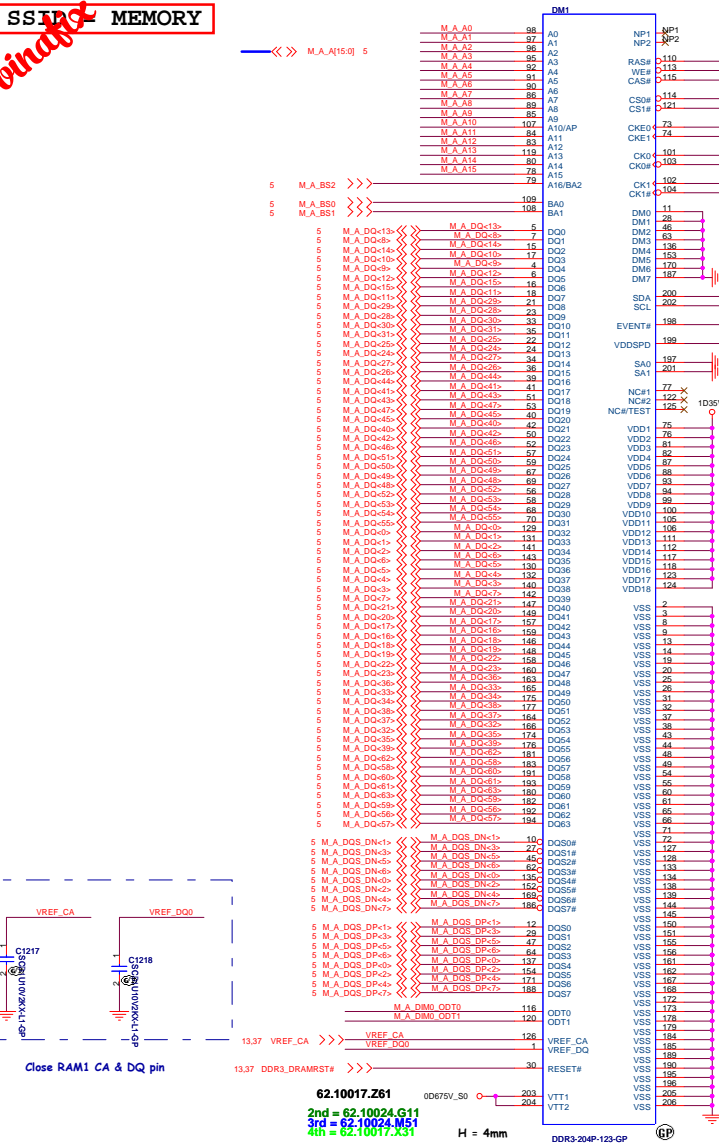
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CPU (Power CAP2)			
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SSIP MEMORY

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D

C

B

A

D

C

B

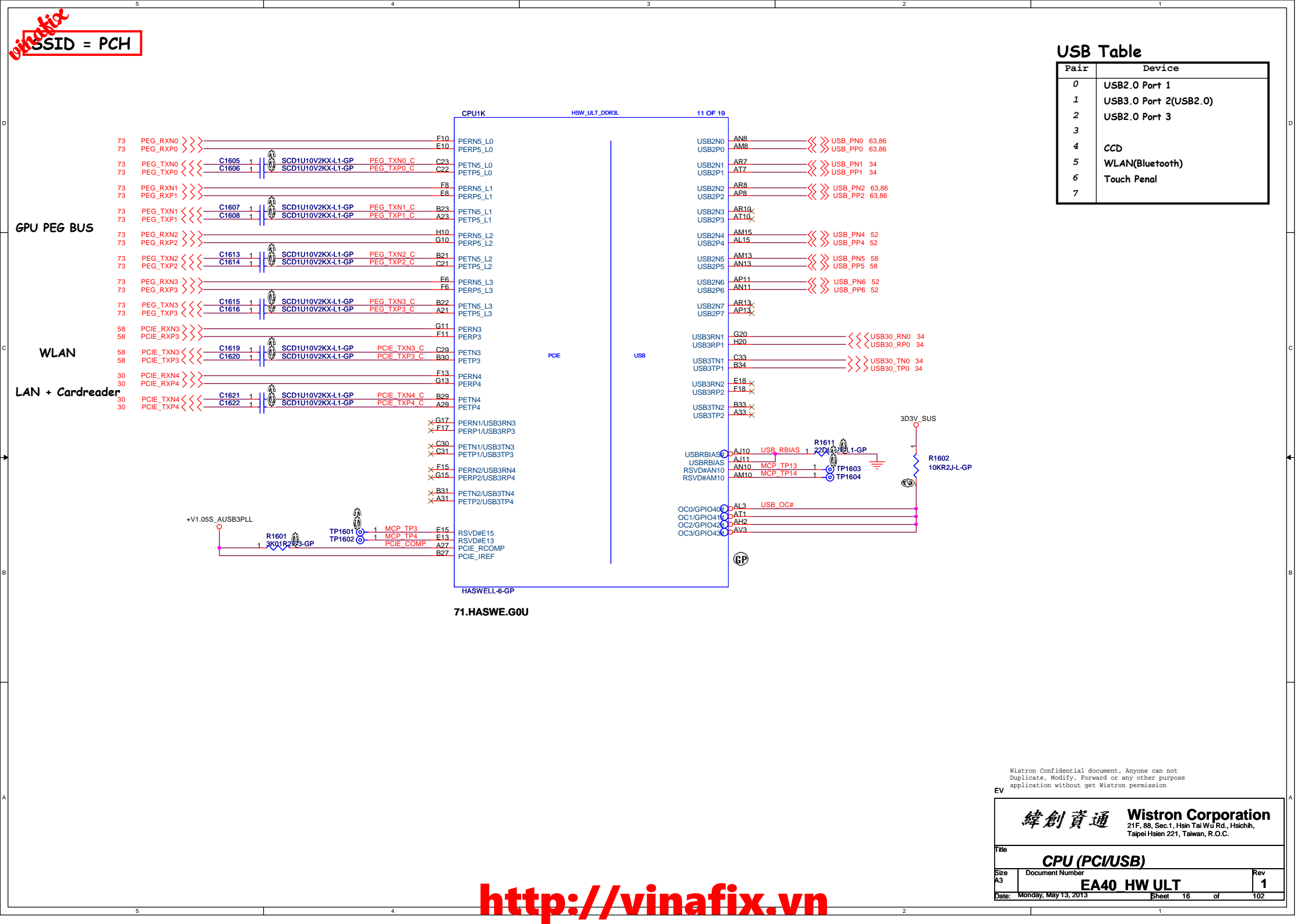
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Title			
(Reserved) SODIMM SODIMM4			
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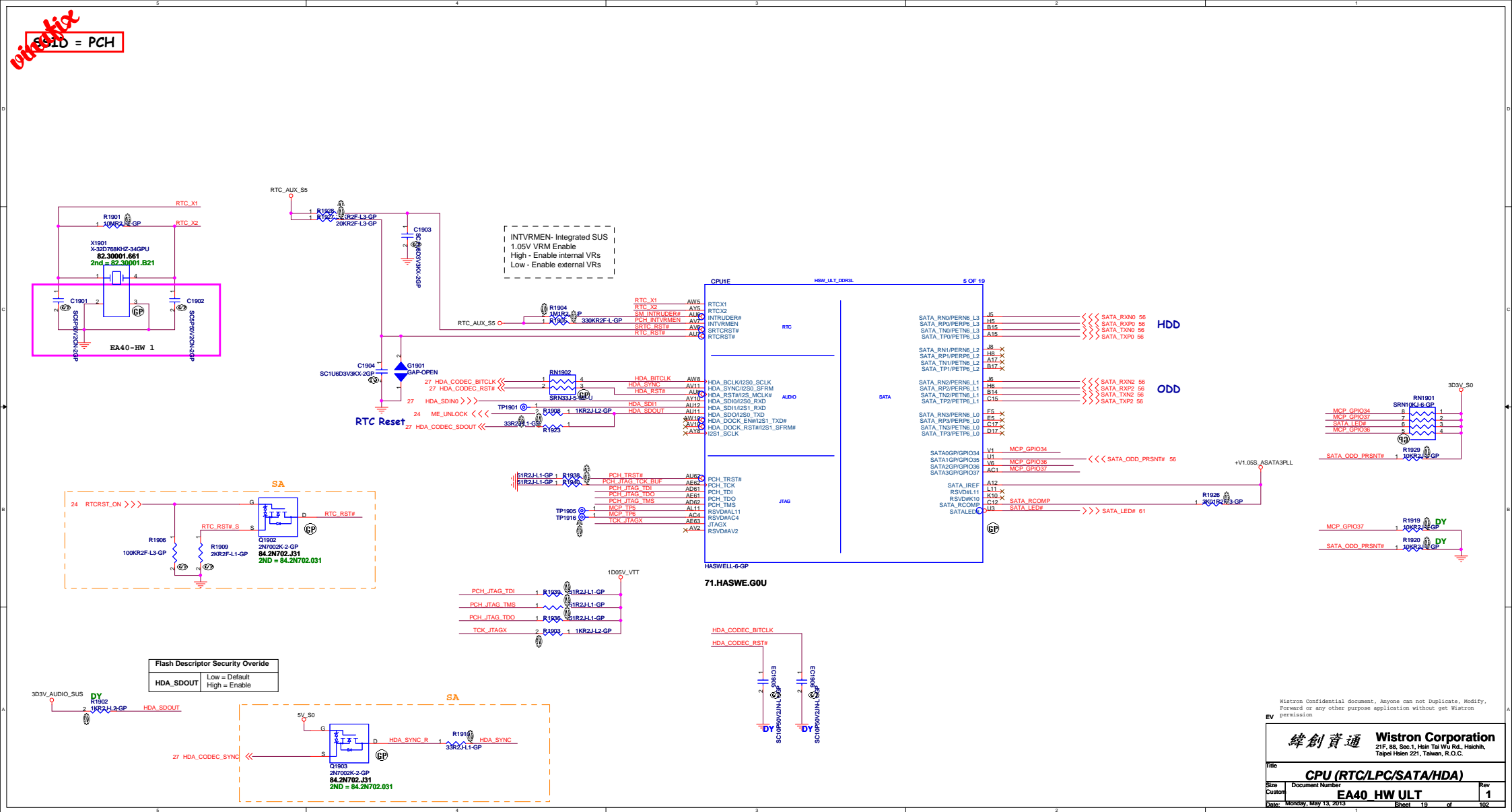
SSS

B

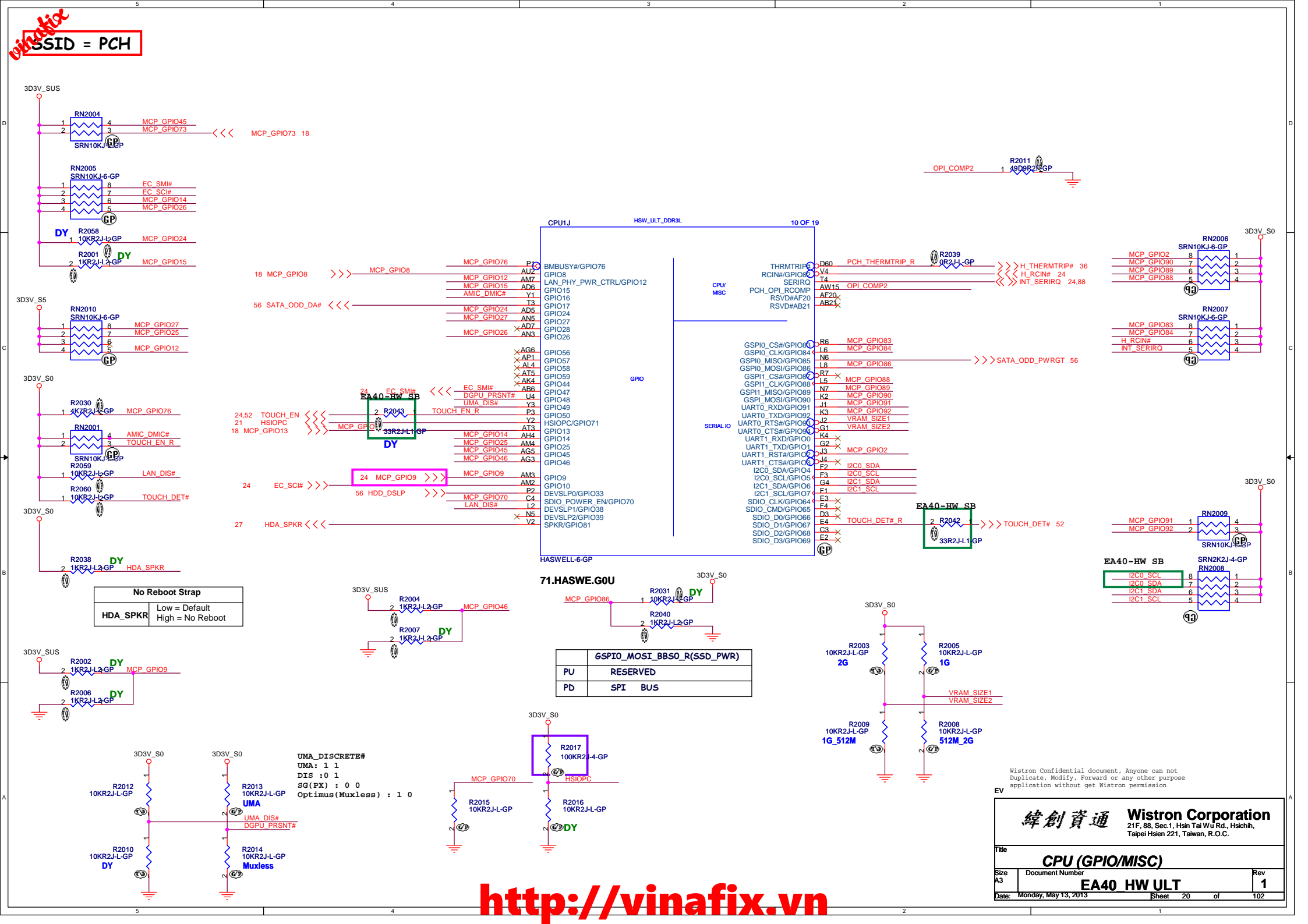
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Title			
CPU (DMI/FDI/PM)			
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SSIR



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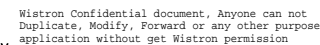
CPU (GPIO/MISC)

EA40 HW ULT

Sheet

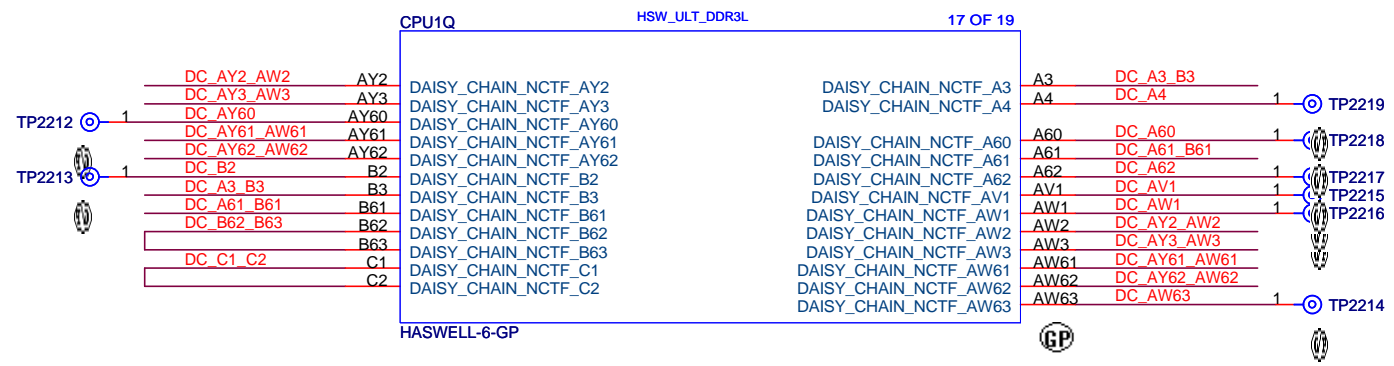
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1. Required only on external SUS.
2. Placeholder only. Does not need to be stuffed.
3. The following pins are not to be connected and be left floating. Test point is optional on these pins: AC20, Y20, K18, M20, V21.
4. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near balls" instructions above to ensure this sharing is optimized.
5. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
6. For description of (R)unway, and (E)dge decoupling capacitor placement, please refer to [Section 41.3, "Loop Inductance Reduction Decoupling"](#) on page 532.

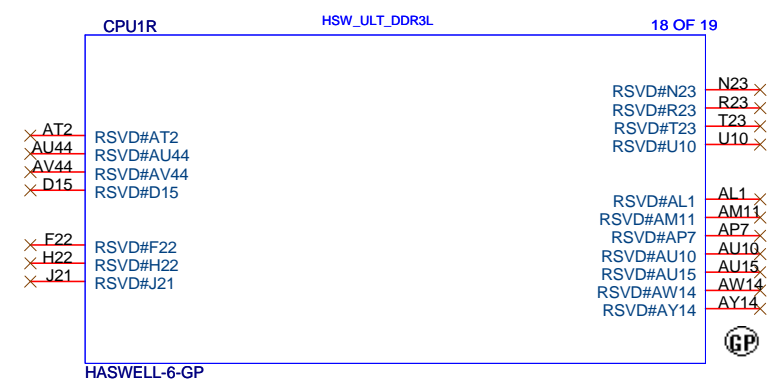


Title			
CPU (POWER1)			
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71.HASWE.G0U



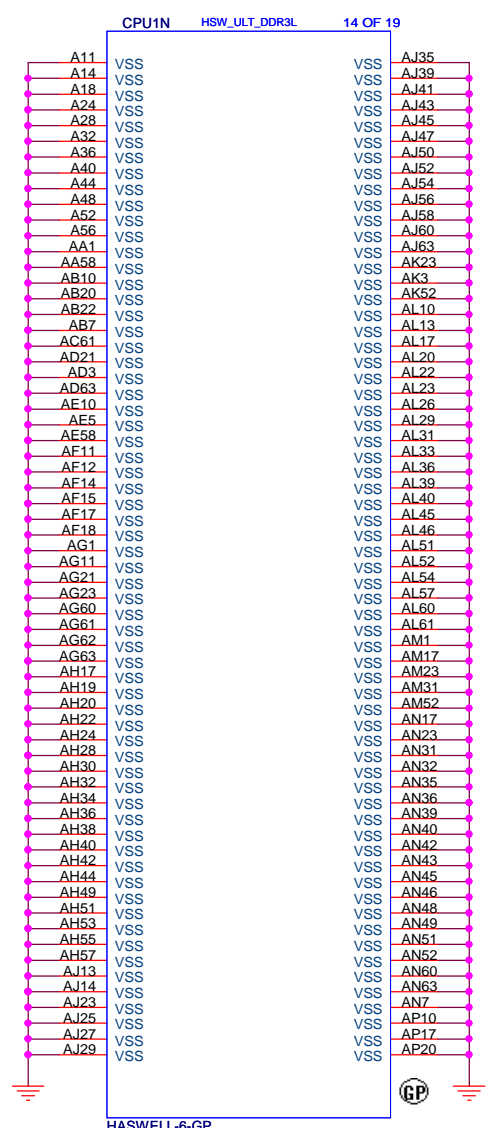
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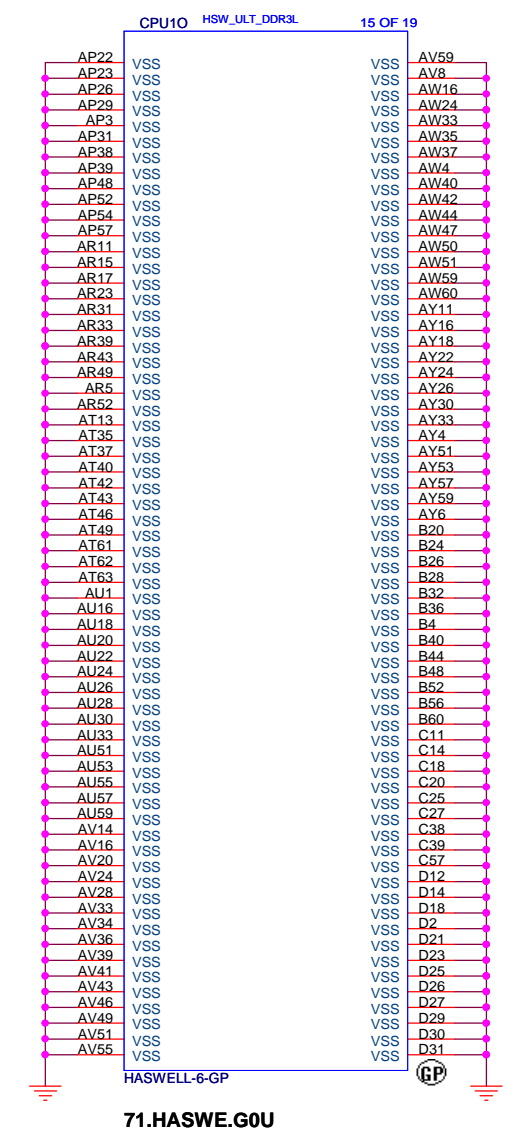
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SOLID = PCH



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Title		CPU (VSS)	
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SPI FLASH ROM (8M byte) for PCH

[illegible][illegible]

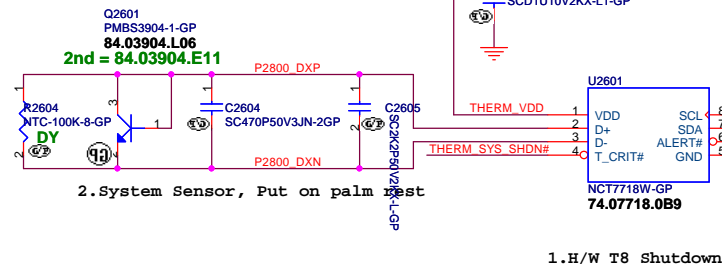
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Flash/(KBC+PCH)/RTC			
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SID = Thermal

Thermal sensor NCT 7718W

Layout notice :
Both DXN and DXP routing 10 mil
trace width and 10 mil spacing.

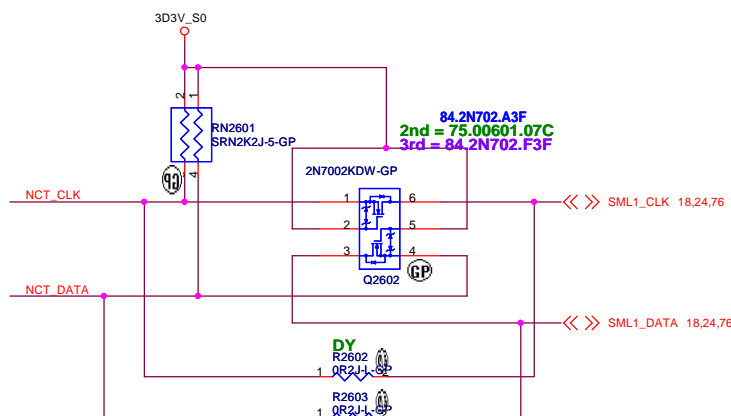


ALERT# /T CRIT#
Pull-up Resistor

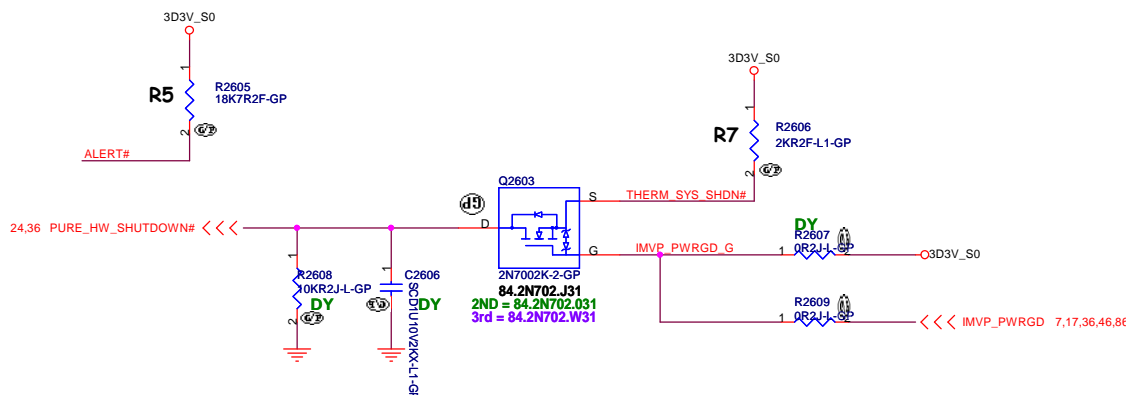
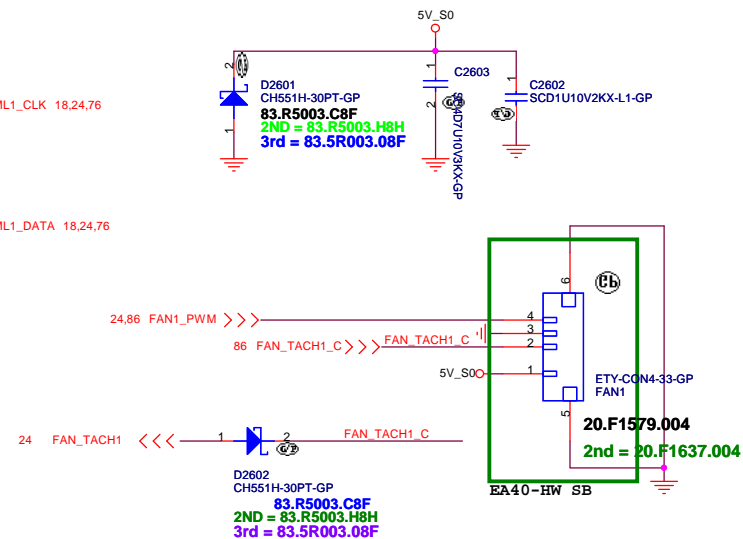
	R5	2Kohm	7.5Kohm	10.5Kohm	14Kohm	18.7Kohm
77°C	77°C	77°C	77°C	77°C	77°C	77°C
79°C	79°C	79°C	79°C	79°C	79°C	79°C
81°C	81°C	81°C	81°C	81°C	81°C	81°C
83°C	83°C	83°C	83°C	83°C	83°C	83°C
85°C	85°C	85°C	85°C	85°C	85°C	85°C

T_CRIT temperature strapping point

T8=85 degree



Layout 15 mil

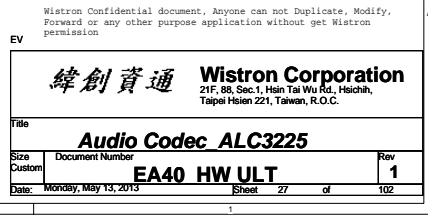


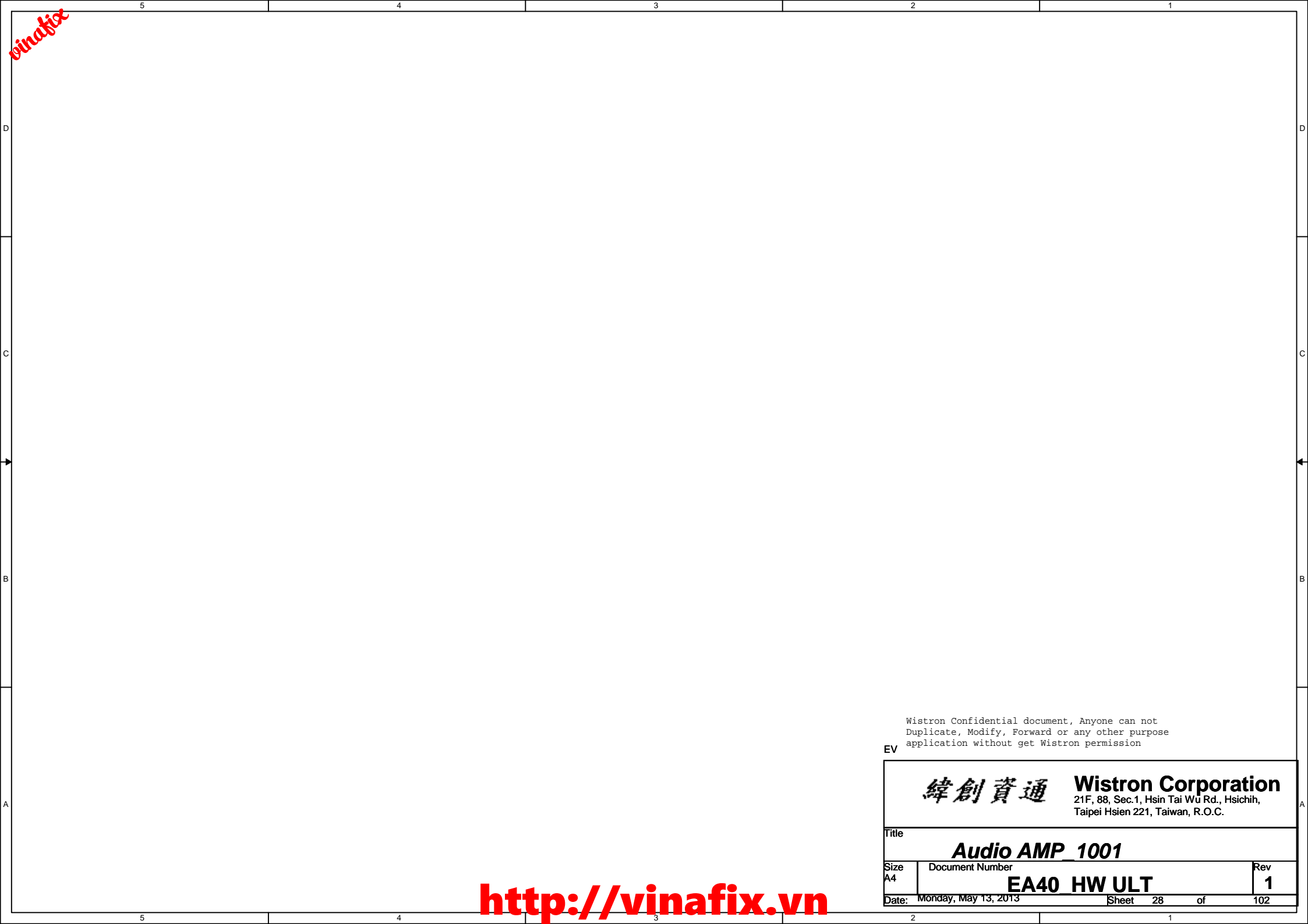
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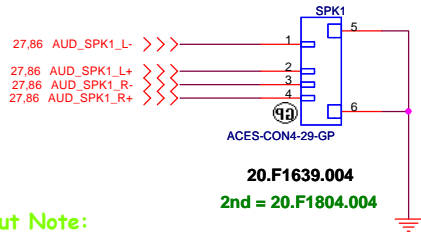
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Audio AMP_1001			
Size A4	Document Number EA40 HW ULT		Rev 1
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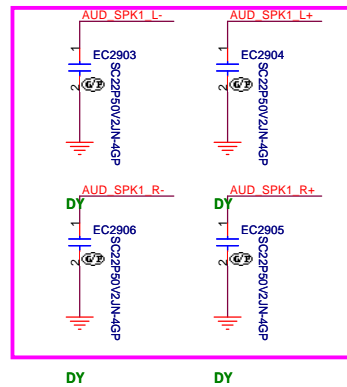
SEND = AUDIO

Speaker

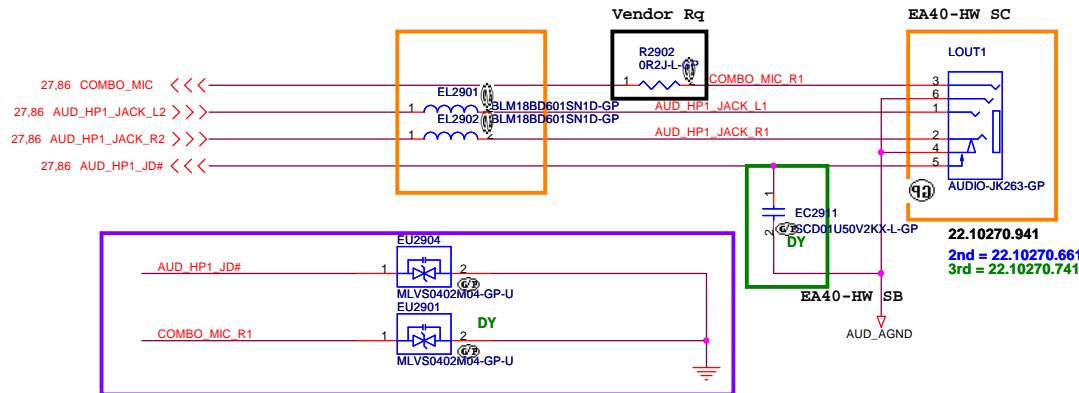


Layout Note:

Trace width=40mil



Combo Jack



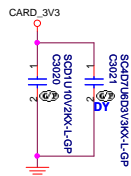
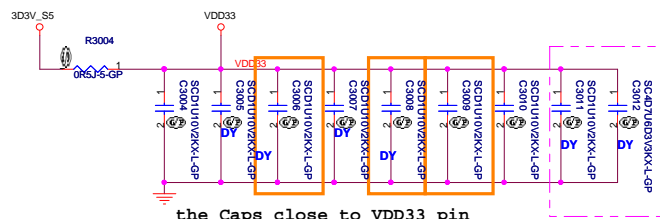
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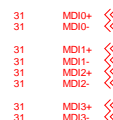
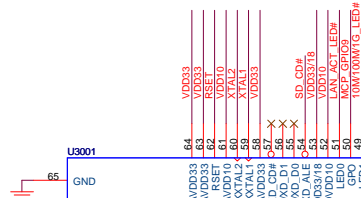
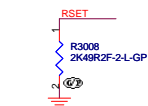
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Audio Jack		
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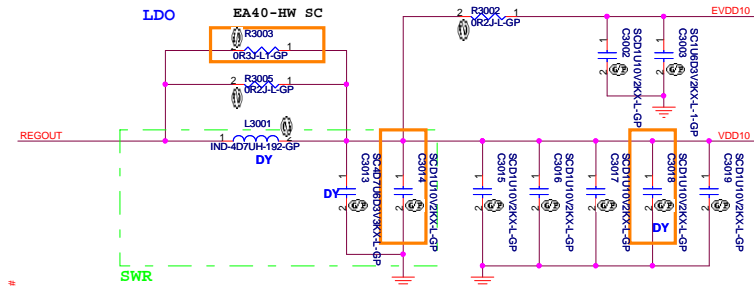
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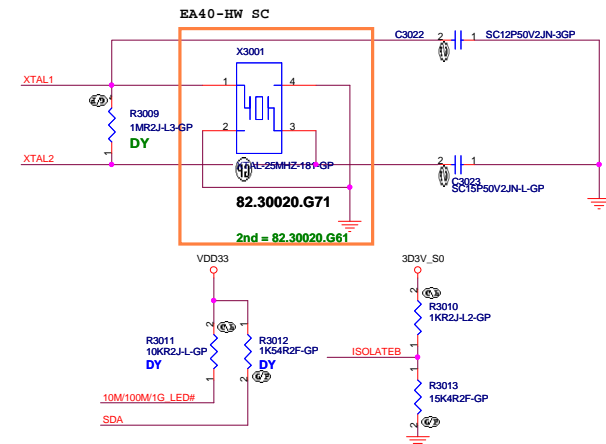
Close to VDDREG pin



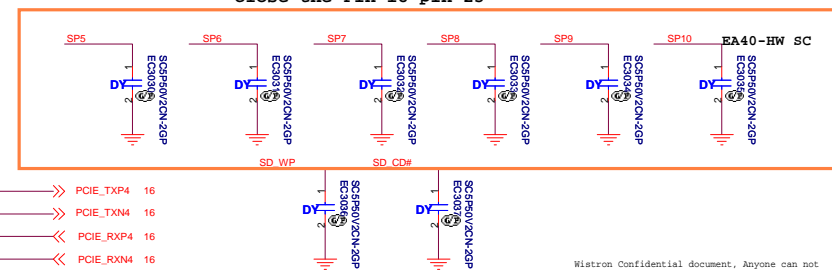
71.08411.B03



24 MCP_GPIO9 >>>



close to pin33 and pin53



close the Pin 18-pin 23

SP1	SD_D7	xD_RDY
SP2	SD_D6	xD_RE#
SP3	SD_D5	xD_CE#
SP4	SD_D4	xD_WE#
SP5	SD_D3	xD_D0
SP6	SD_D2	xD_D1
SP7	SD_D1	xD_D2
SP8	SD_D0	xD_D3
SP9	SD_CLK	xD_D4
SP10	SD_CMD	xD_D5
SP11	SD_D3	xD_D6
SP12	SD_D2	xD_D7
SP13	SD_D1	xD_D8
SP14	SD_D0	xD_D9
SP15	SD_CLK	xD_D10
SP16	SD_CMD	xD_D11

SP5	2	ER3014	<<<	SD_DATA1	33,86
SP6	2	ER3022	<<<	SD_DATA0	33,86
SP7	2	ER3021	<<<	SD_CLK	33,86
SP8	2	ER3024	<<<	SD_CMD	33,86
SP9	2	ER3023	<<<	SD_DATA3	33,86
SP10	2	ER3025	<<<	SD_DATA2	33,86
SD_WP	<<<			SD_WP	33
SD_CD#	<<<			SD_CD#	33

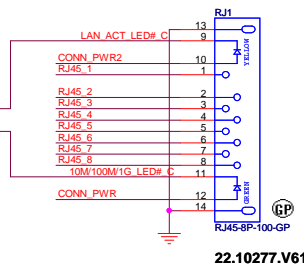
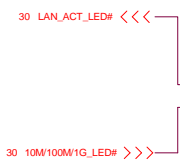
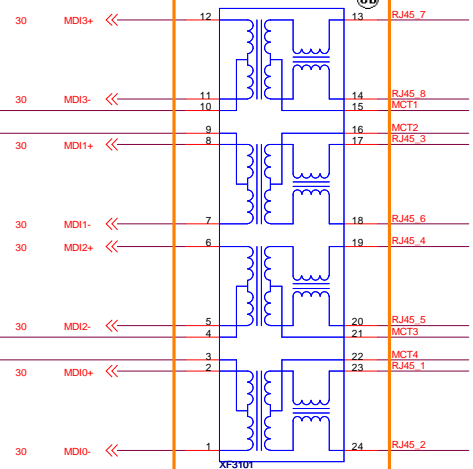
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.	
Title	LAN(RTL8411)
Size	Document Number
Custom	EA40 HW ULT
Date	Monday, May 13, 2013
Sheet	30 of 102

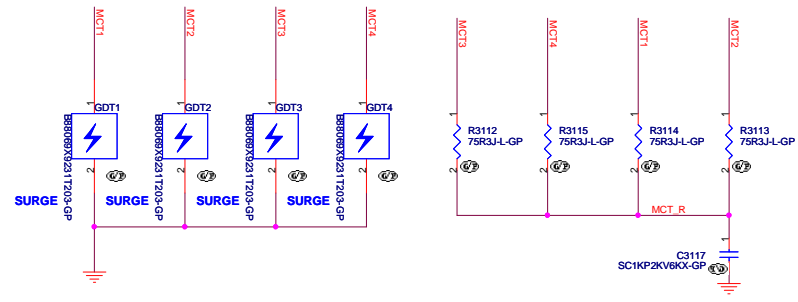
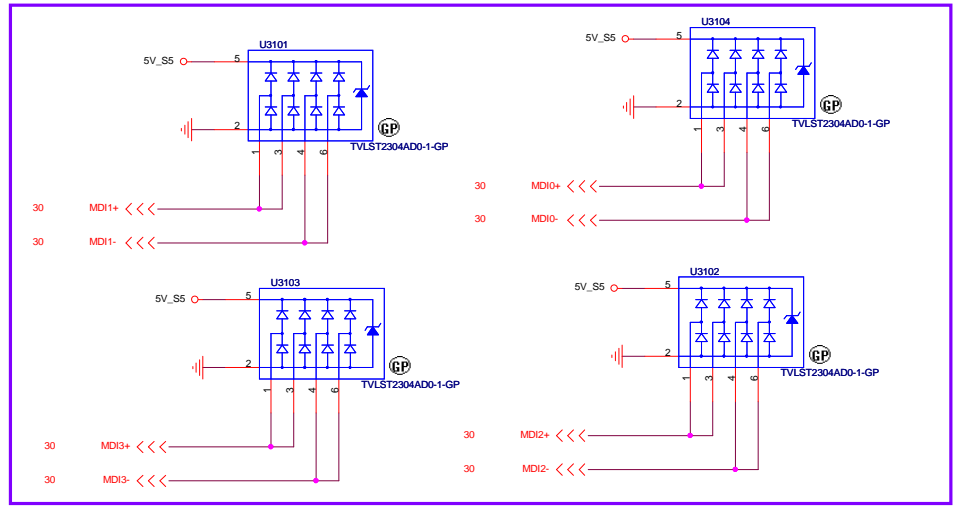
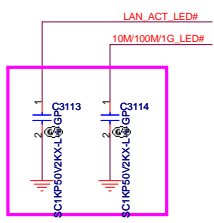
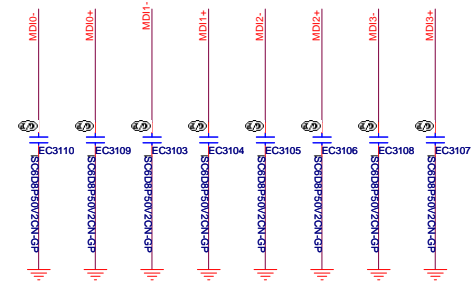
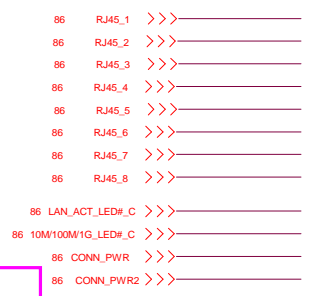
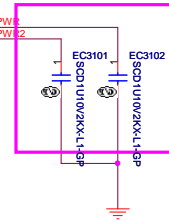
WINDUP
SMD = LAN

EA40-HW SC

3rd = 68.00069.30A
2nd = 68.1H115.30A
68.69241.301
XFORM-270-GP-U



3D3V_S5



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EV		
緯創資通 Wistron Corporation		
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Title (LAN+VGA) CONNECTOR		
Size Custom	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013	Sheet 31	of 102

D

C

B

A

D

C

B

A

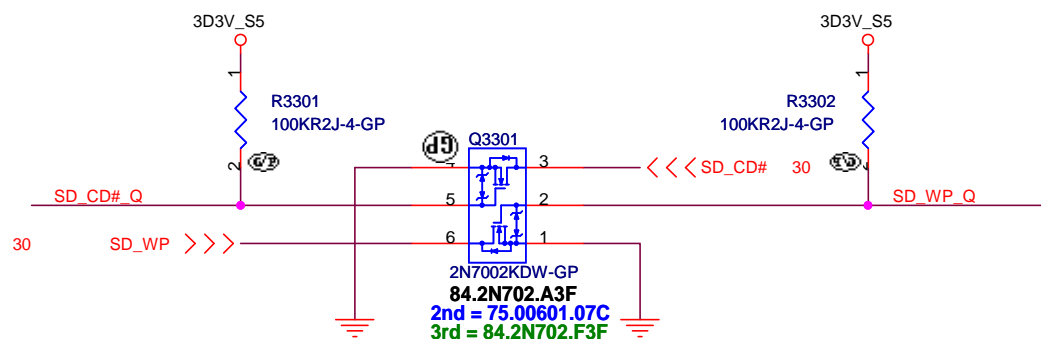
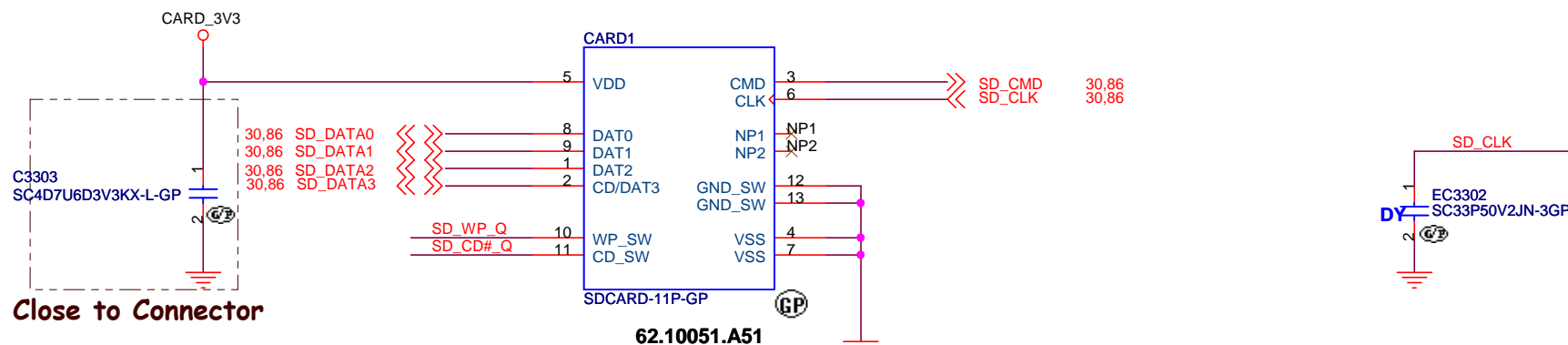
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EV

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title RTS5229(CARD READER)			
Size A4	Document Number EA40 HW ULT		Rev 1
Date: Monday, May 13, 2013		Sheet 32	of 102

SSID = SDIO

SD//MS Card Reader



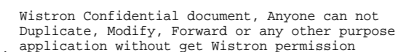
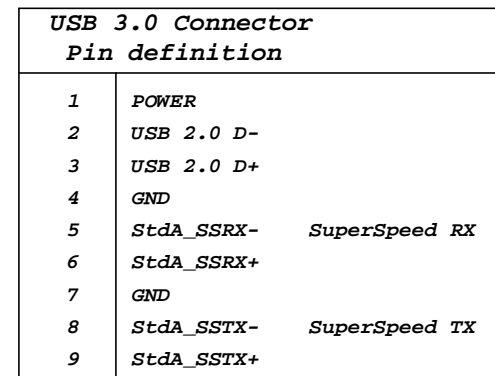
86 SD_WP_Q >>> _____
86 SD_CD#_Q >>> _____

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EV

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
CARD Reader CONN			
Size	Document Number	Rev	
Custom	EA40 HW ULT	1	
Date:	Monday, May 13, 2013	Sheet	33 of 102

<http://vinafix.vn>



緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

USB 2.0 / 3.0 Port

Document Number

EA40 HW ULT

Date: Monday, May 13, 2013

Sheet 34 of 34

Rev

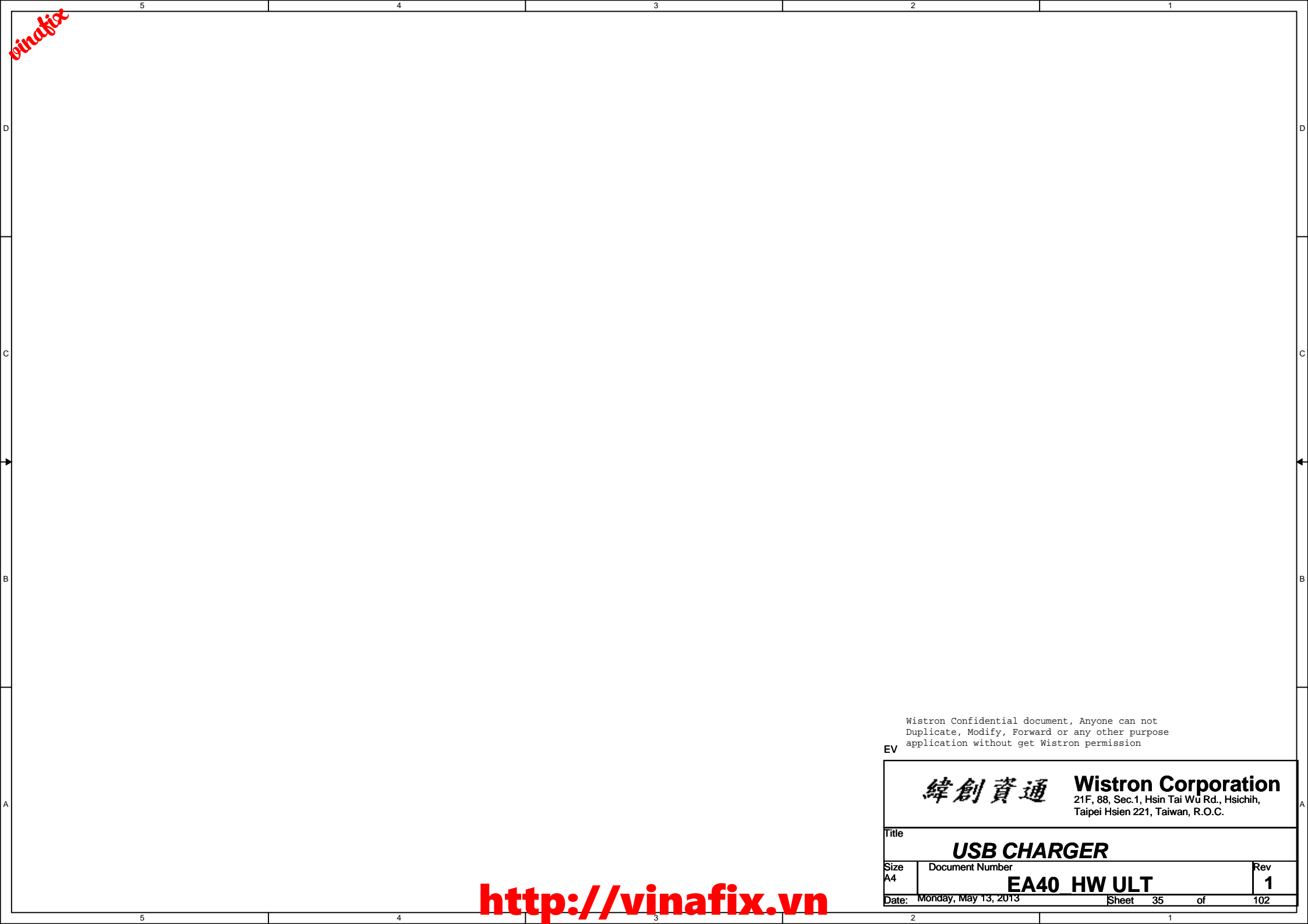
1

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Date: Monday, May 13, 2013

Sheet 34 of 34

102



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Taipei Hsien 221, Taiwan, R.O.C.

Title

USB CHARGER

Size
A4

Document Number

EA40 HW ULT

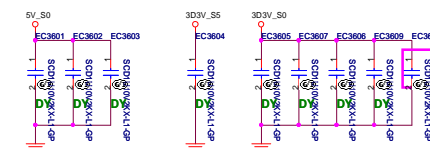
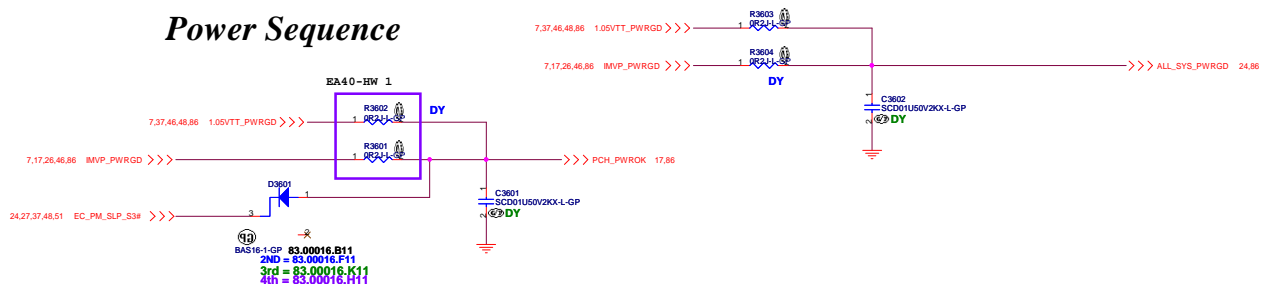
Rev
1

Date: Monday, May 13, 2013

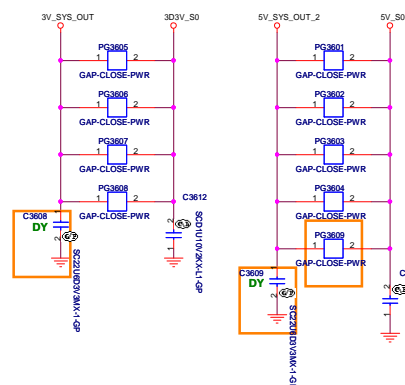
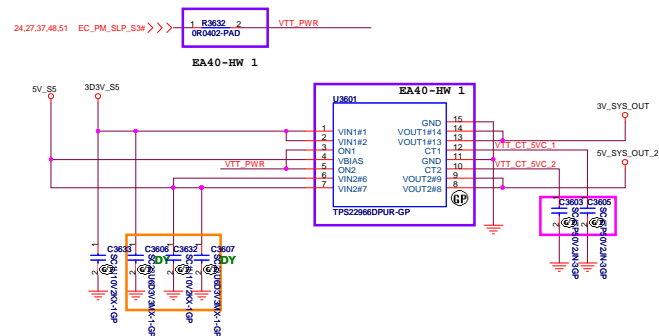
Sheet 35 of 102

<http://vinafix.vn>

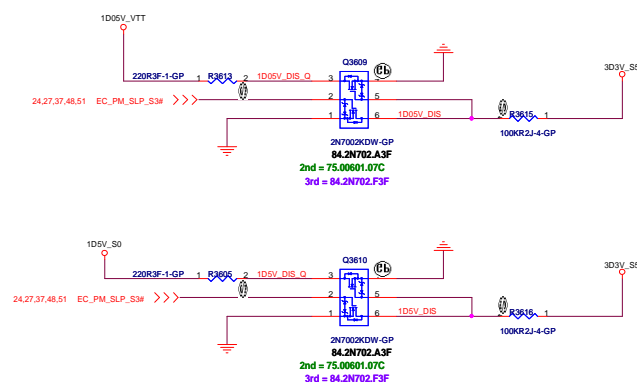
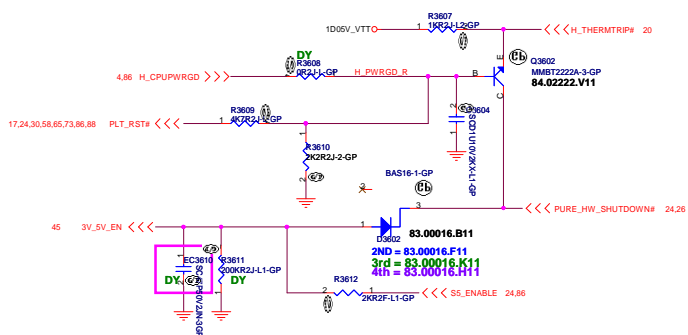
Power Sequence



ANNIE Run Power

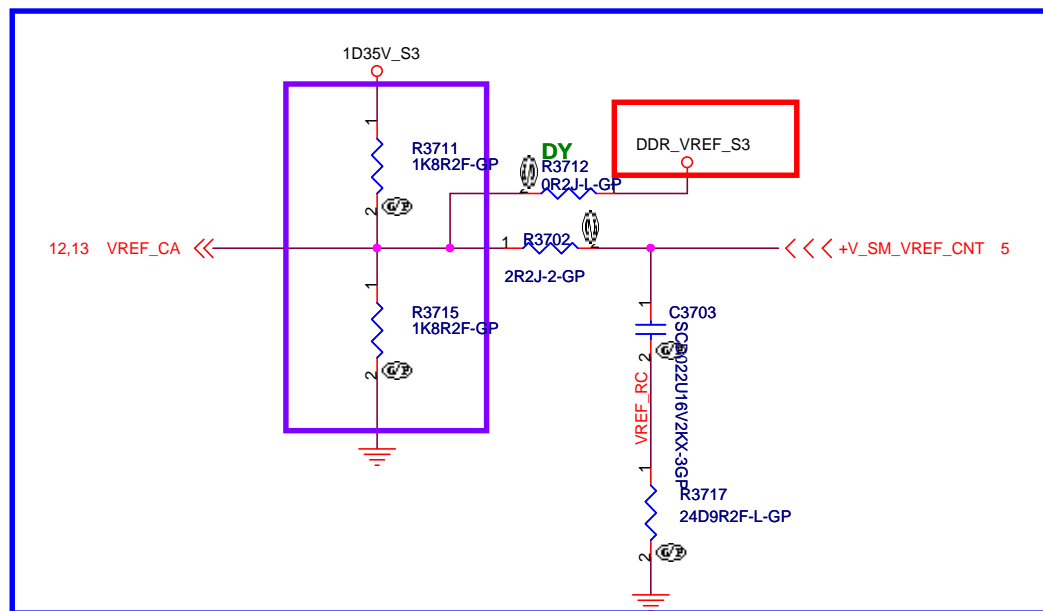
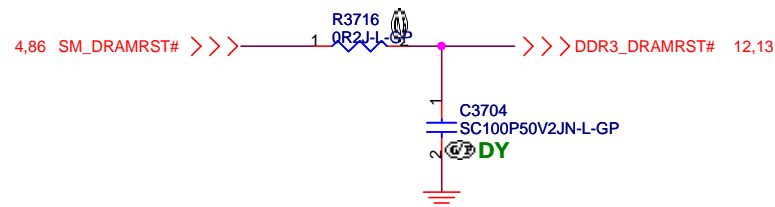


Discharge circuit



DY 3D3V_S0 discharge circuit

vinafix



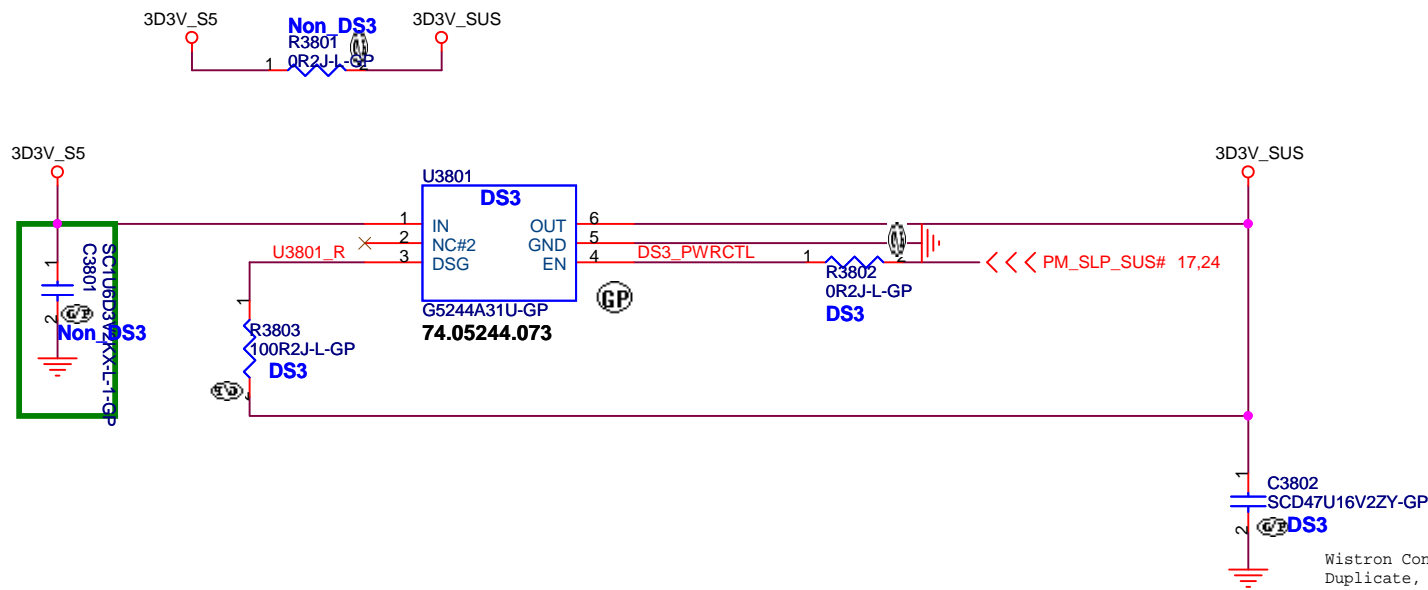
For Intel Recommend Close to DIMM

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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title ADAPTER OCP / S3 reduction					
Size Custom	Document Number EA40 HW ULT				Rev 1
Sheet 37 of 102					

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Title

DS3

Size
A4

Document Number

EA40 HW ULT

Rev
1

Date: Monday, May 13, 2013

Sheet 38 of 102

Power Sequence

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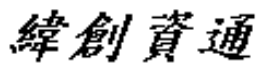
EV	
<div><div>緯創資通</div><div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div></div>	
Title	
1D05 M	
Size	Document Number
Custom	EA40 HW ULT
Date: Monday, May 13, 2013	Sheet 39 of 102
Rev	
1	

	5	4	3	2	1	
D						D
C						C
B						B
A						A
	5	4	3	2	1	

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EV

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Title	
Connected Standby1	
Size A	Document Number EA40 HW ULT
Rev 1	
Date: May 13, 2013	Sheet 40 of 102

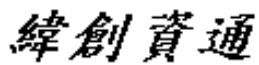
<http://vinafix.vn>

	5	4	3	2	1
D					D
C					C
B					B
A					A
	5	4	3	2	1

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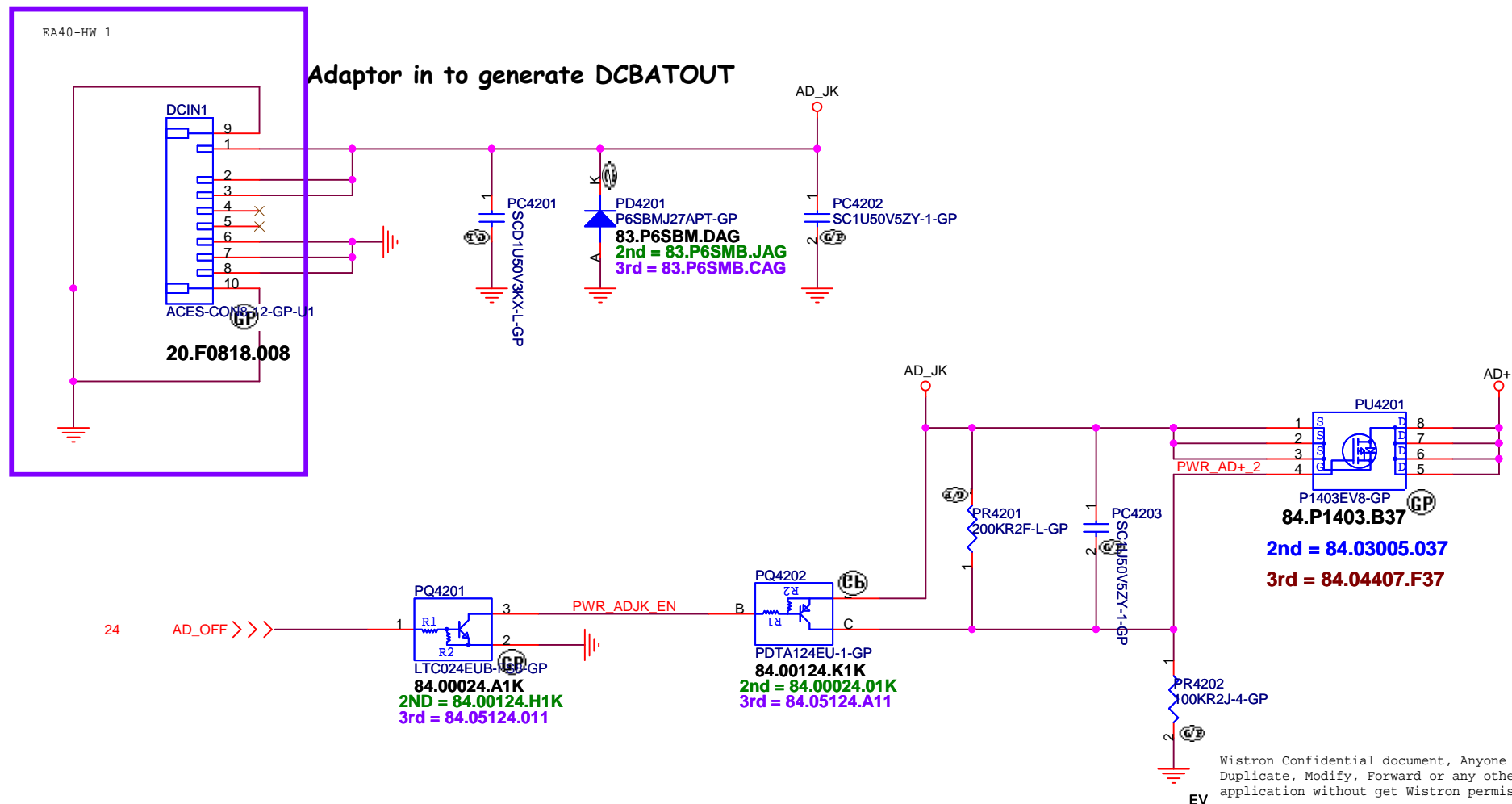
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 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
Connected Standby2	
Size A	Document Number EA40 HW ULT
Rev 1	
Date: May 13, 2013	
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ANNIE solution



緯創資通

Wistron Corporation

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Title

DCIN JACK

Size
A4

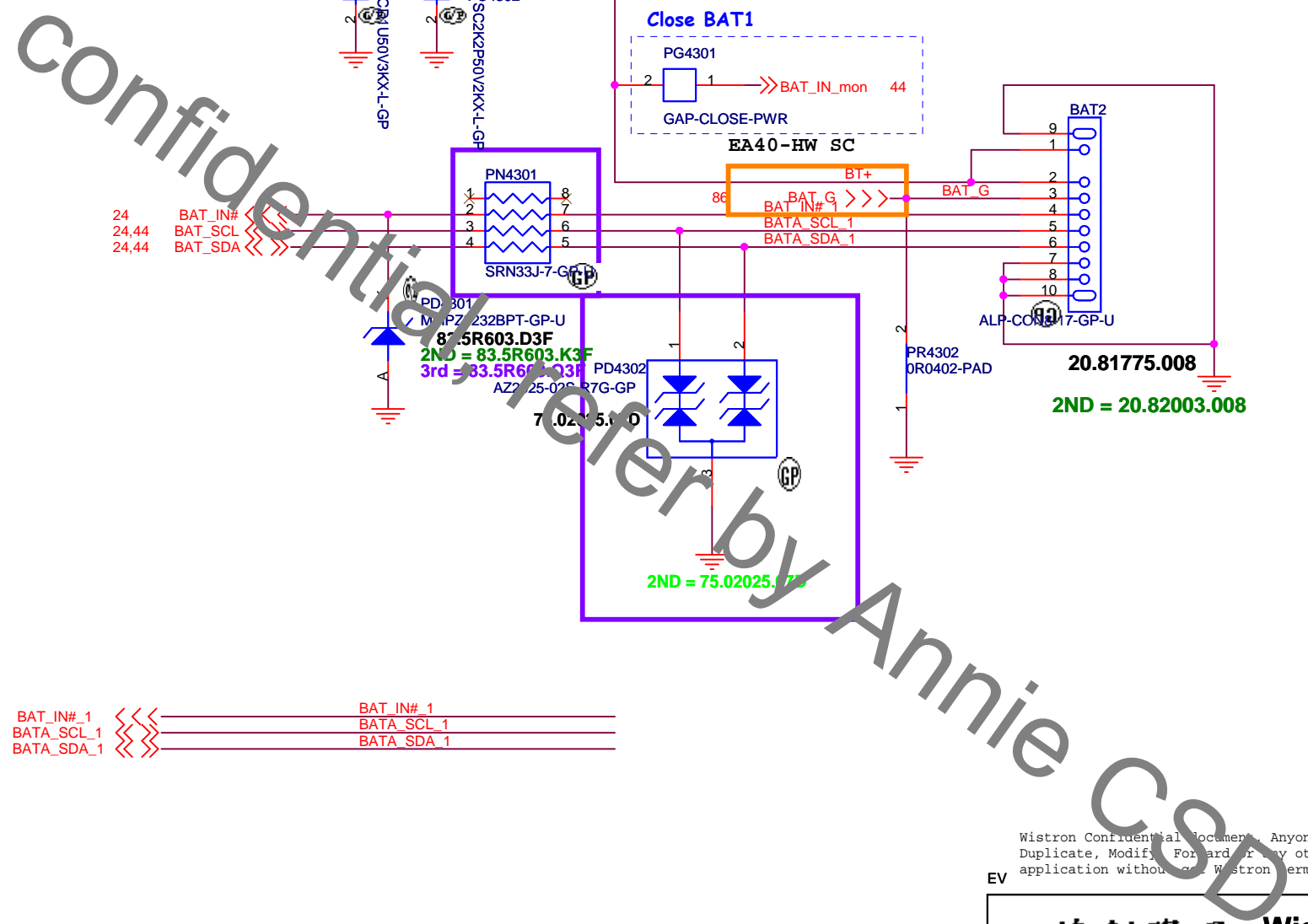
Document Number

EA40 HW ULT

Rev
1

Date: Monday, May 13, 2013

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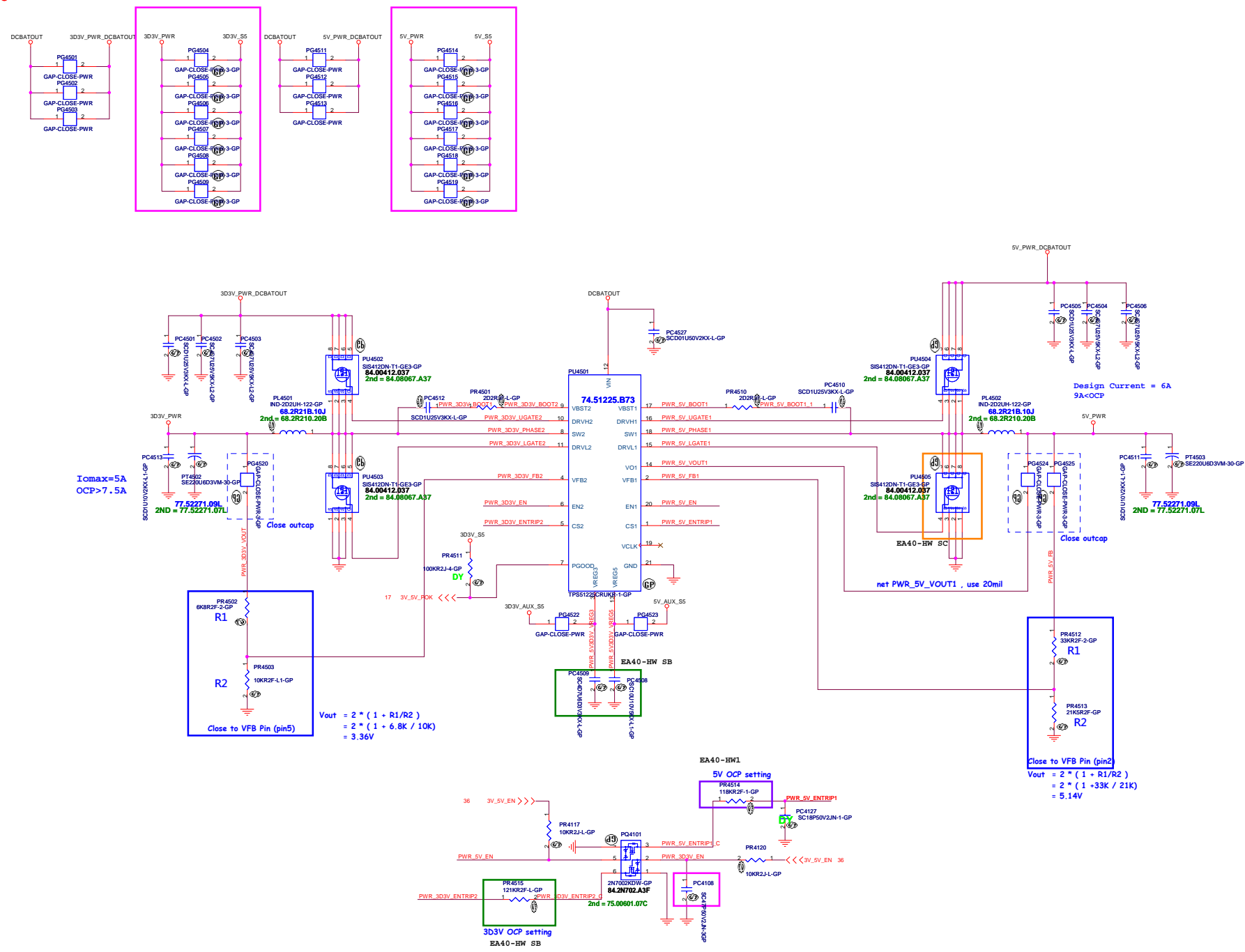
86 BAT_IN#_1 <<< BAT_IN#_1
 86 BATA_SCL_1 <<< BATA_SCL_1
 86 BATA_SDA_1 <<< BATA_SDA_1

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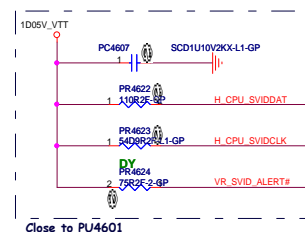
EV

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title BATT CONN			
Size A4	Document Number EA40 HW ULT		Rev 1
Date: Monday, May 13, 2013		Sheet 43 of	102

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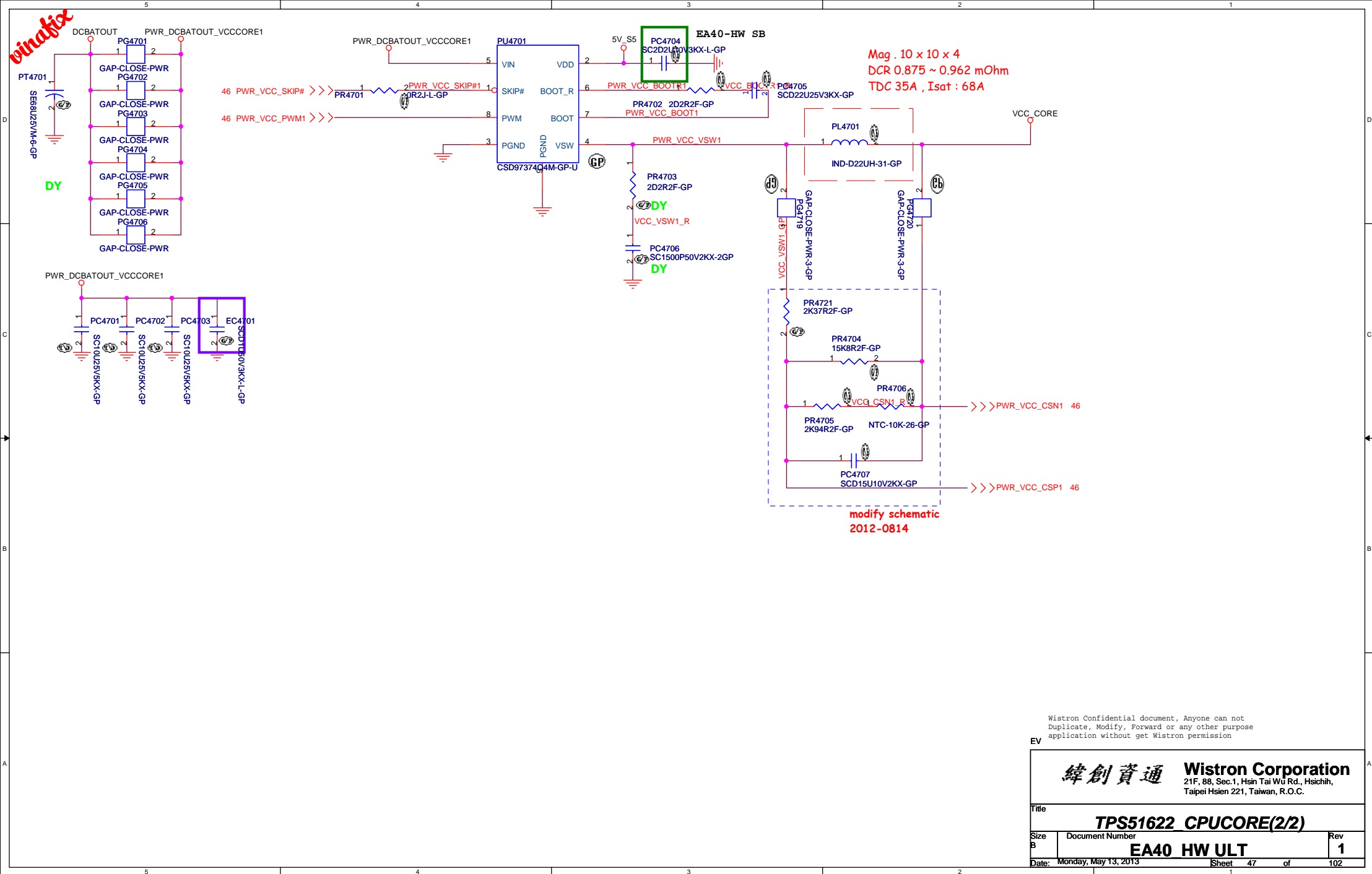


<http://vinafix.vn>

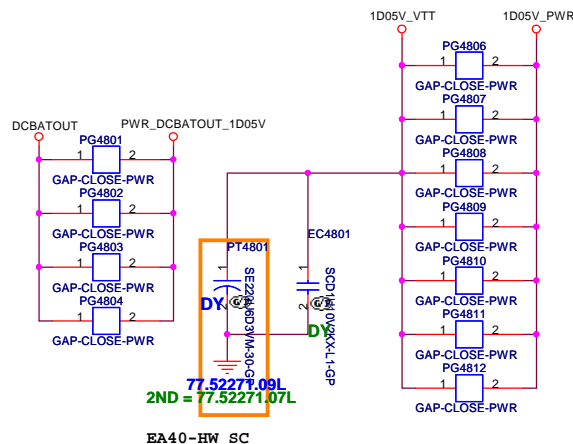


EV

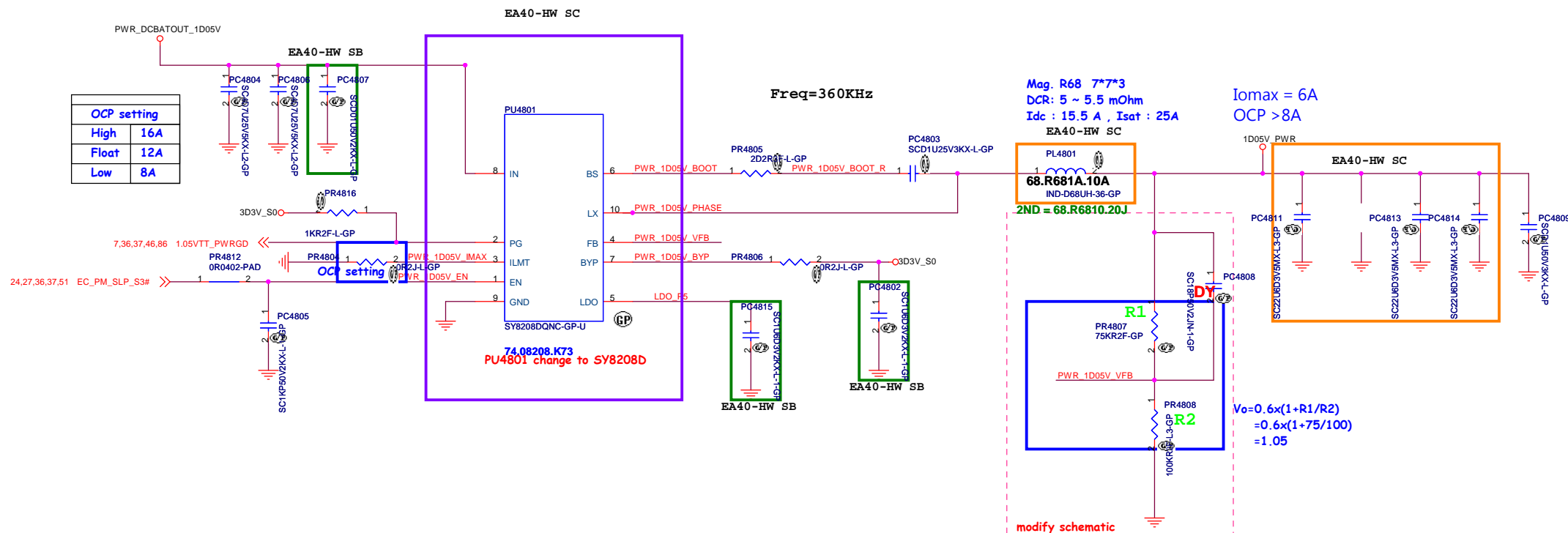
Title			
TPS51622 CPUCORE(1/2)			
Size C	Document Number		Rev 1
	EA40 HW ULT		
Date:	Monday, May 13, 2013	Sheet 46 of	102



SY8208D for 1D05V



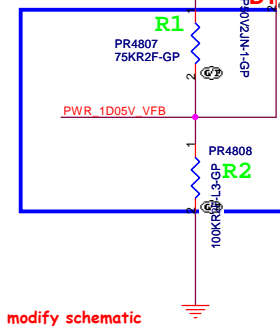
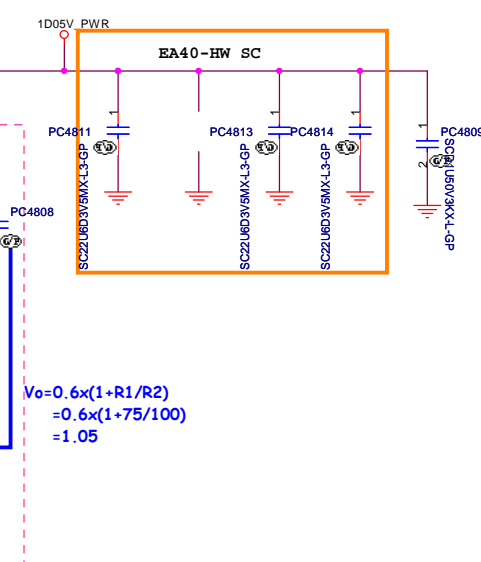
OCP setting	
High	16A
Float	12A
Low	8A



Mag. R68 7*7*3
DCR: 5 ~ 5.5 mOhm
Idc : 15.5 A , Isat : 25A

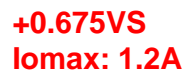
Iomax = 6A
OCP > 8A

EA40-HW SC
PL4801
68.R681A.10A
IND-D68UH-36-GP
2ND = 68.R6810.20J



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Title	
DC to DC 1D05V(SY8208D)	
Size	Document Number
A3	EA40 HW ULT
Date	Friday, May 24, 2013
Sheet	48 of 102
Rev	1



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Title			
RT8207(VDDQ VTT)			
Size	Document Number	Rev	
Custom	EA40 HW ULT	1	
Date:	Monday, May 13, 2013	Sheet	49 of 102

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SYW232 for 1D8V_S0

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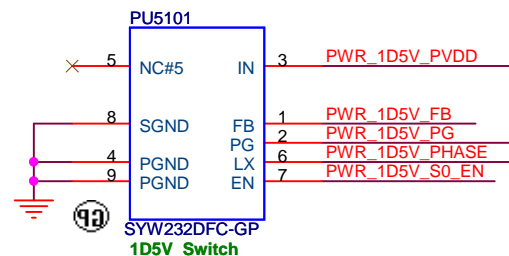
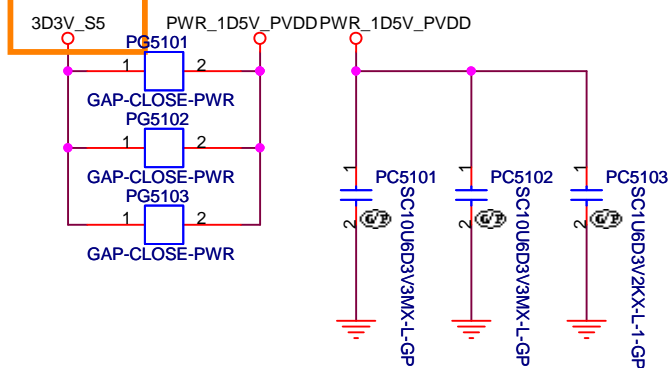
EV

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title 1D8V_S0 SYW232		
Size A4	Document Number EA40 HW ULT	Rev 1
Date: Monday, May 13, 2013		Sheet 50 of 102

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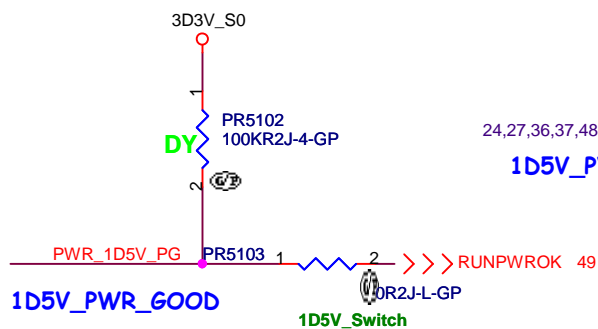
Check!!

SYW232 for 1D5V_S0



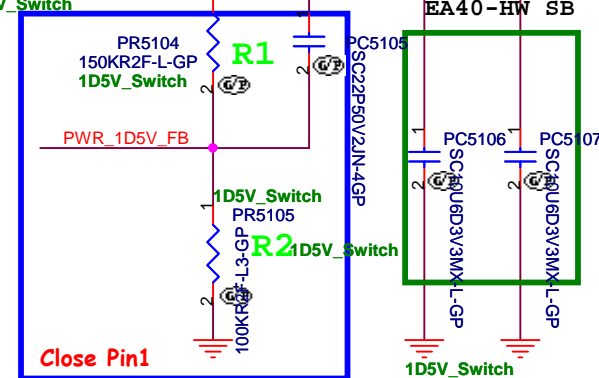
Mag. 2D2uH 5.3 x 4.7 x 3
DCR=29 ~ 35mohm
Isat : 5.5 ~ 9 A

$I_{omax}=3.2A$
 $OCP>5A$



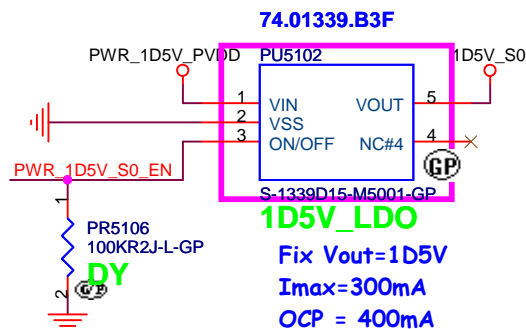
24,27,36,37,48 EC_PM_SLP_S3#
1D5V_PWR_EN

PL5101
IND-1UH-145-GP
CHIP IND 1UH VLS3015ET-1R0N
1D5V_Switch



$$V_o = 0.6 \times (1 + R1/R2) \\ = 0.6 \times (1 + 150/100) \\ = 1.5$$

EA40-HW SC



74.01339.B3F

1D5V_LDO

Fix Vout=1D5V
 $I_{max}=300mA$
 $OCP = 400mA$

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緯創資通

Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

1D5V_S0 SYW232

Size

A4

Document Number

EA40 HW ULT

Rev

1

Date:

Monday, May 13, 2013

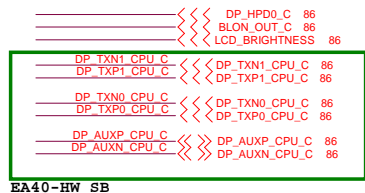
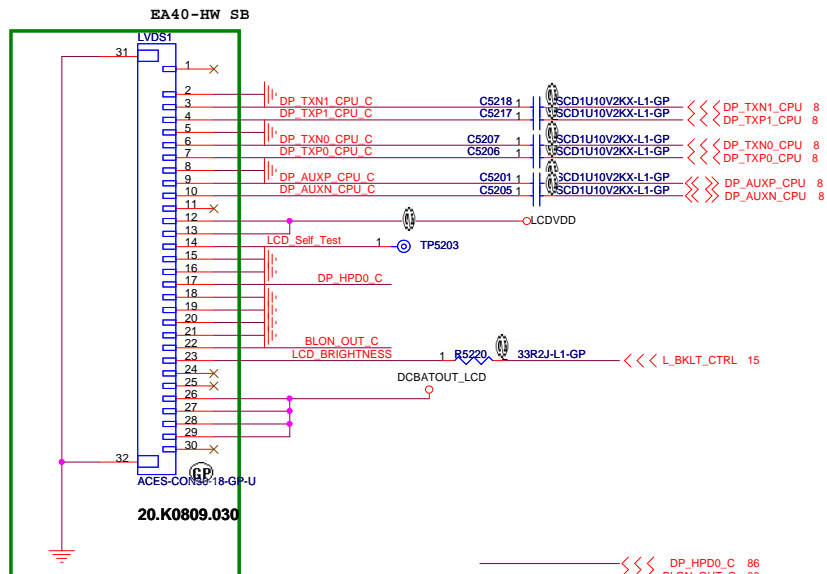
Sheet

51

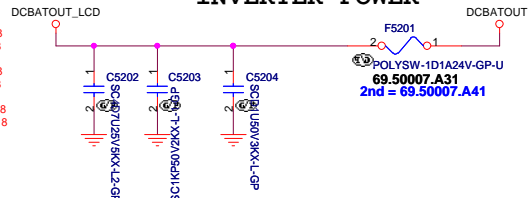
of

102

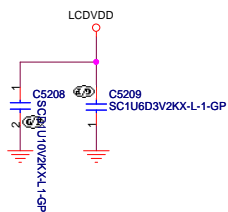
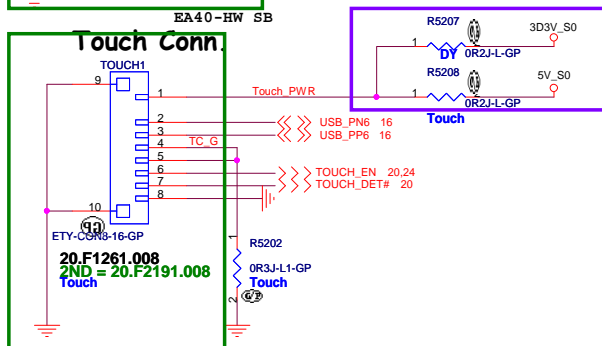
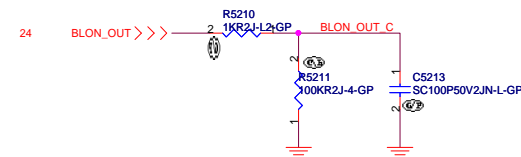
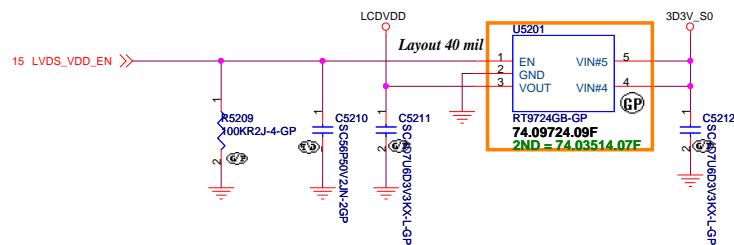
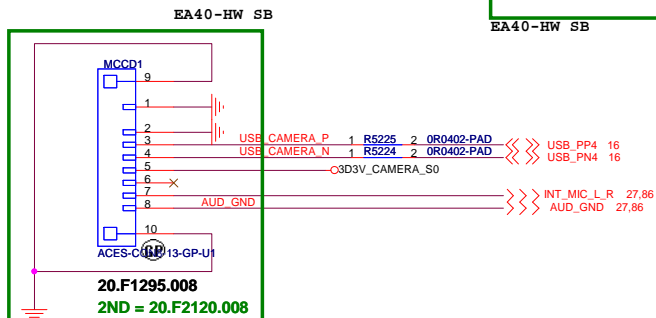
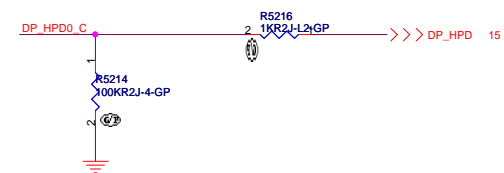
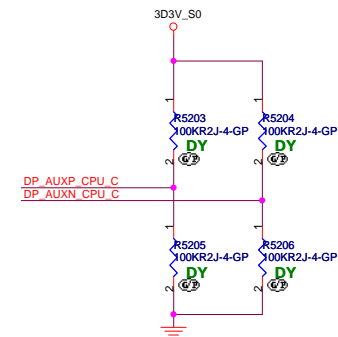
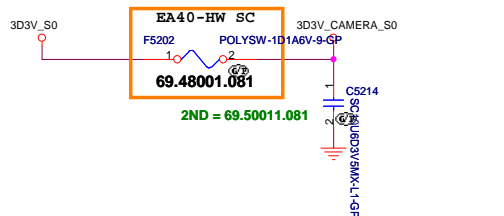
SCD = VIDEO



INVERTER POWER



Camera Power



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EV

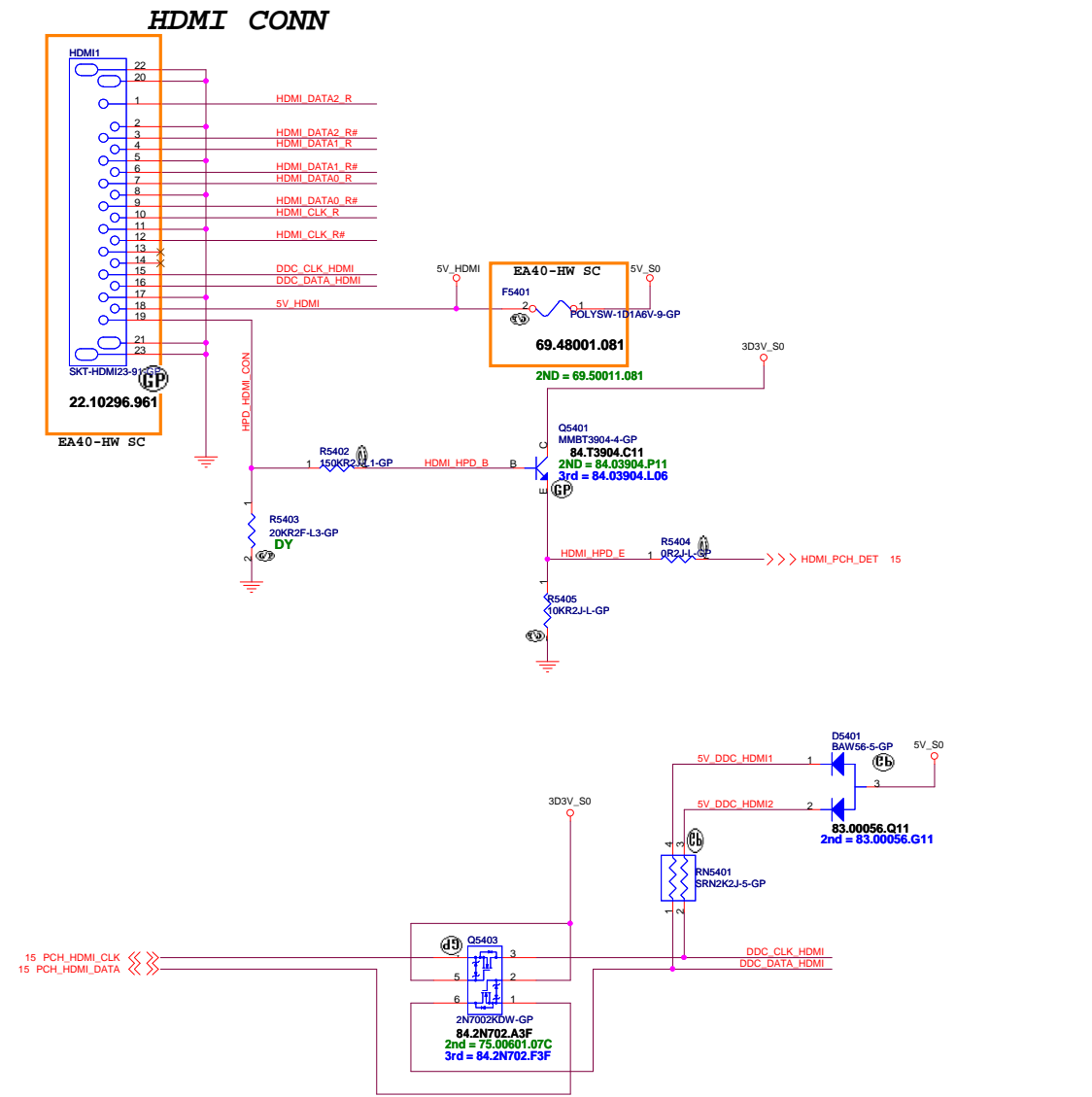
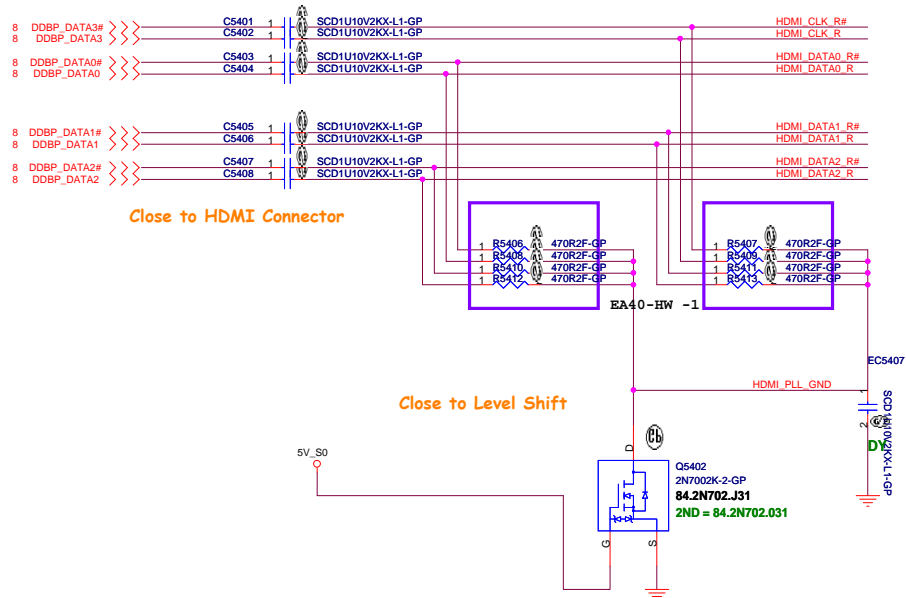
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	LCD Connector	
Size	Document Number	Rev
Custom	EA40 HW ULT	1
Date:	Thursday, May 30, 2013	Sheet 52 of 102

<http://vinafix.vn>

SOLID = VIDEO

HDMI Level Shifter & CONNECTOR

UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103~C5110 to 0 ohm resistor



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File		HDMI Level Shifter/Connector	
Size	Custom	Document Number	EA40 HW ULT
Date	Monday, May 13, 2013	Sheet	54 of 102
Rev		1	

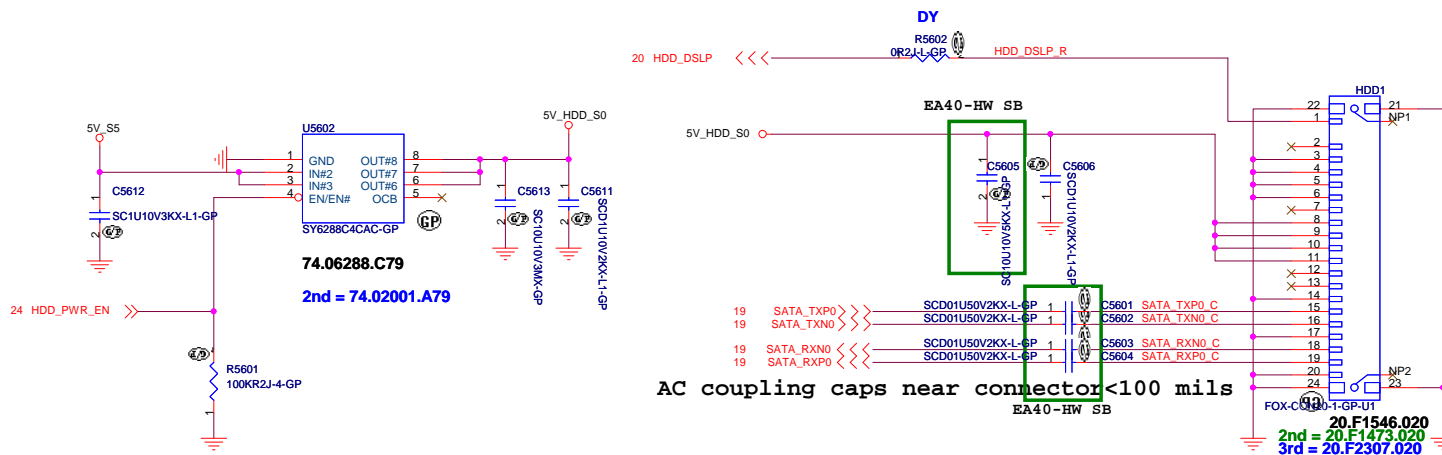


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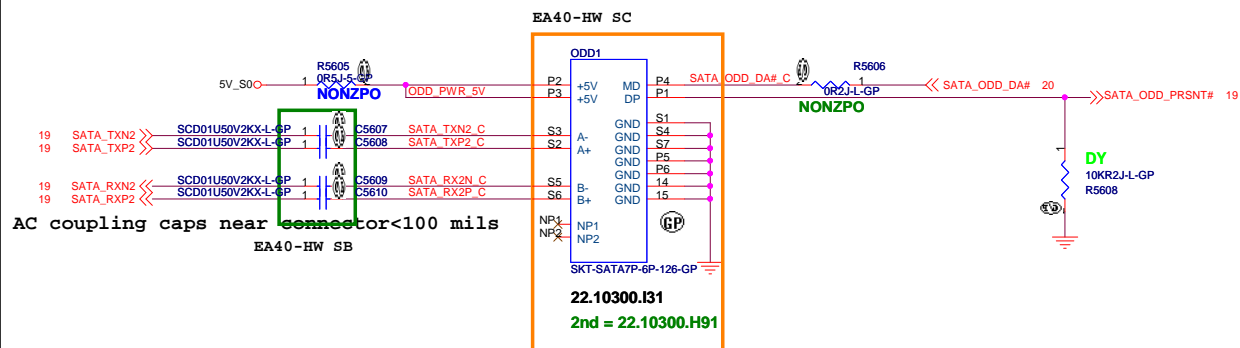
EV

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Display Port			
Size	Document Number		Rev
Custom	EA40 HW ULT		1
Date:	Monday, May 13, 2013		Sheet 55 of 102

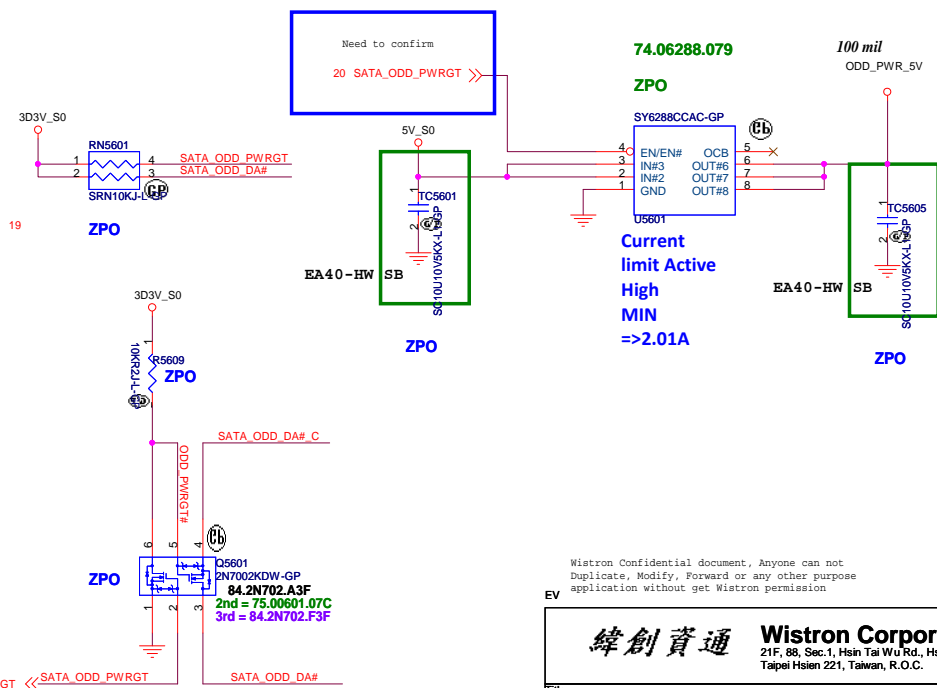
SATA HDD Connector



ODD Connector

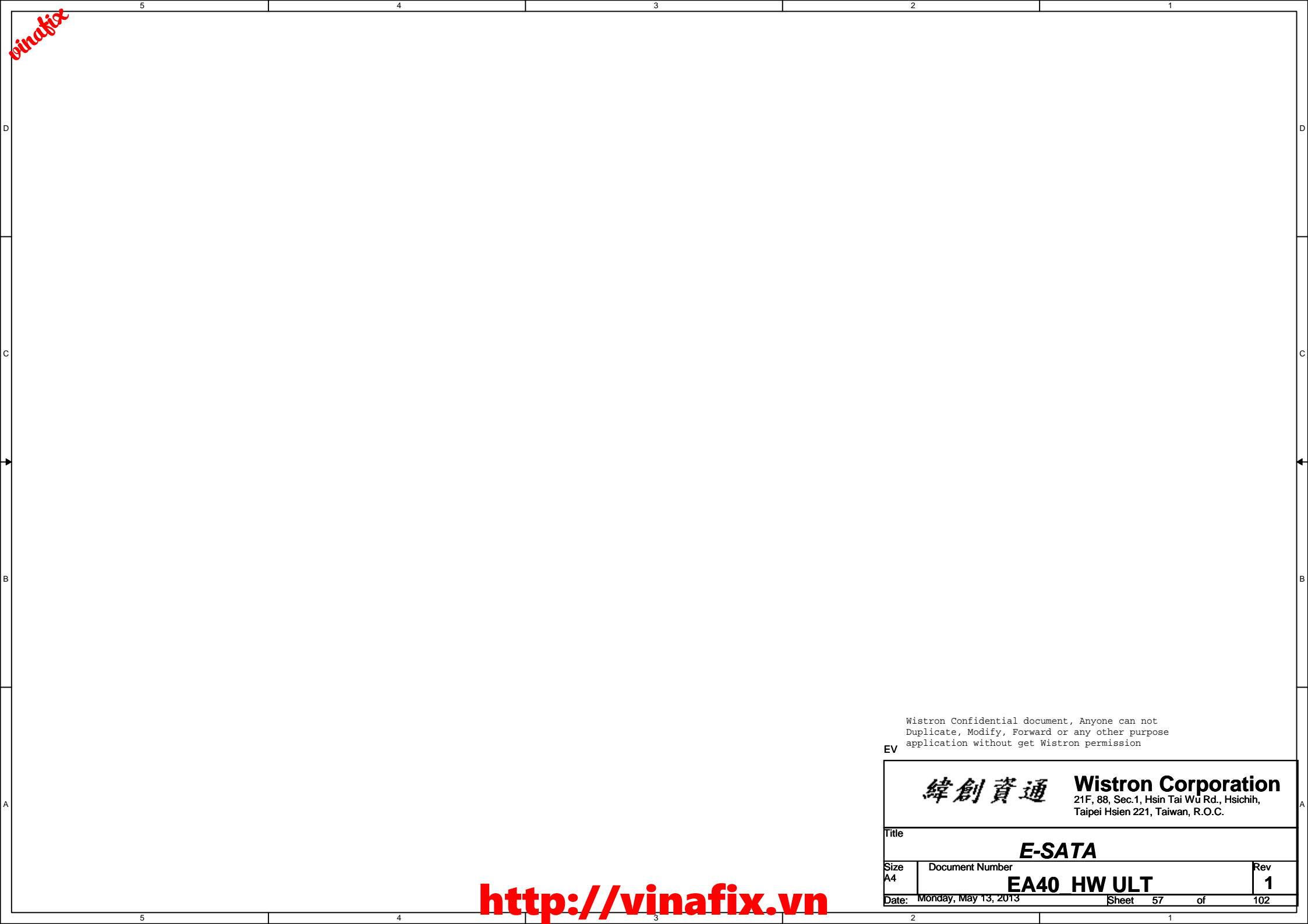


SATA Zero Power ODD



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HDD / ODD / NGFF SSD	
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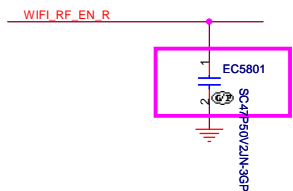
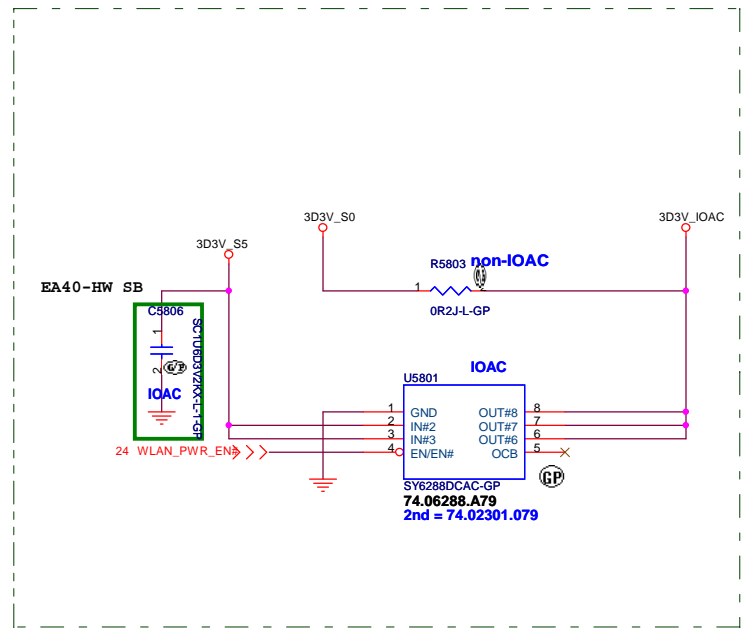
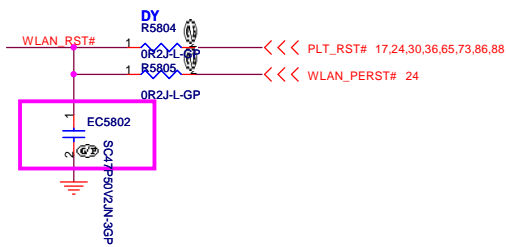
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E-SATA		
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SSID = Wireless *Mini Card Connector(802.11a/b/g/n)*



62.10043.I31
2nd = 62.10043.I51
3rd = 62.10043.K81

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MINICARD(WLAN)			
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SSID = Wireless

Mini Card Connector(mSATA)

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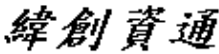
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SSID = mSATA

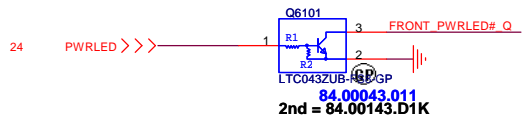
Mini Card Connector(mSATA)

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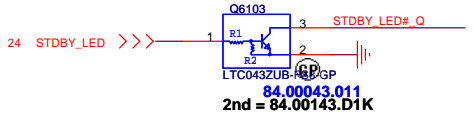
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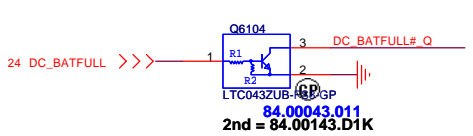
Power button LED



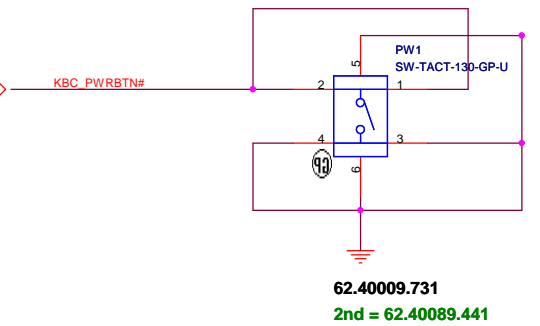
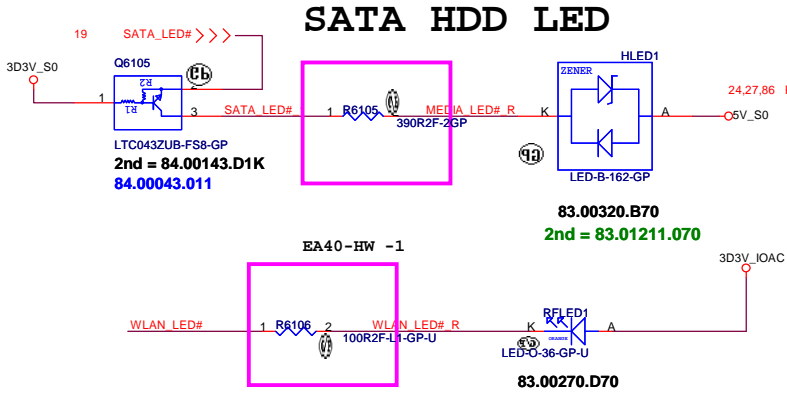
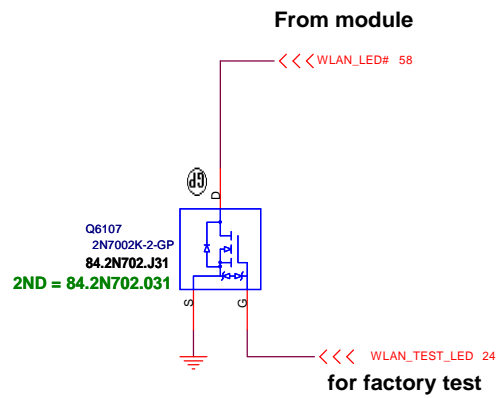
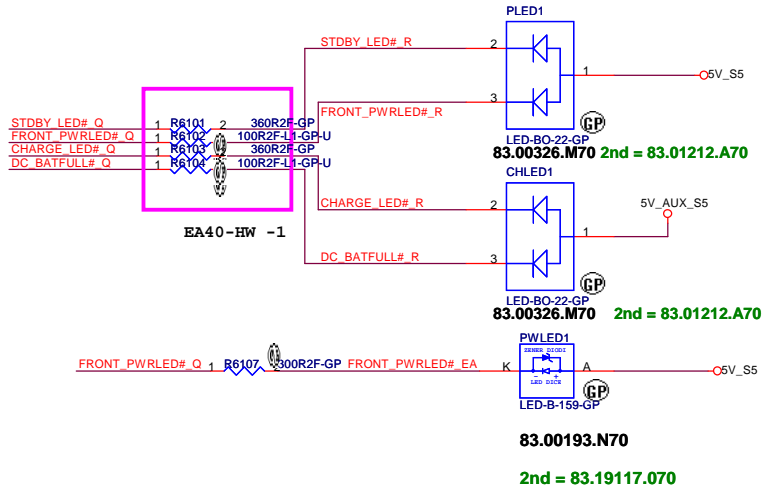
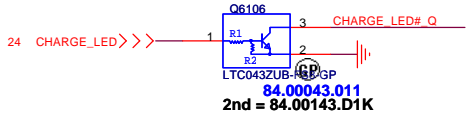
Power STDBY_LED



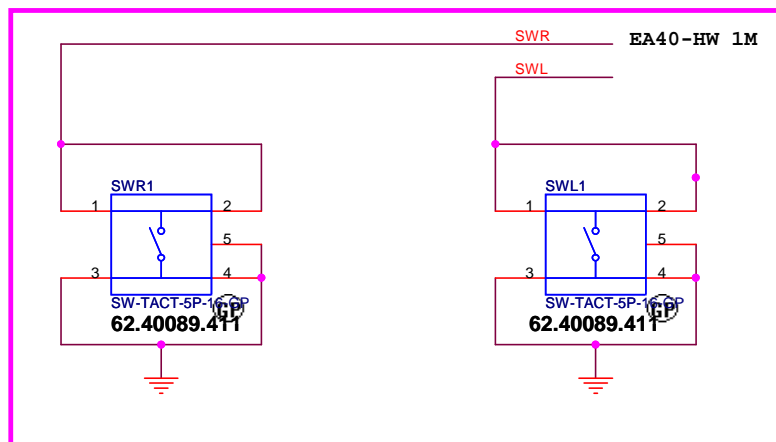
Battery LED2(DC_BATFULL)



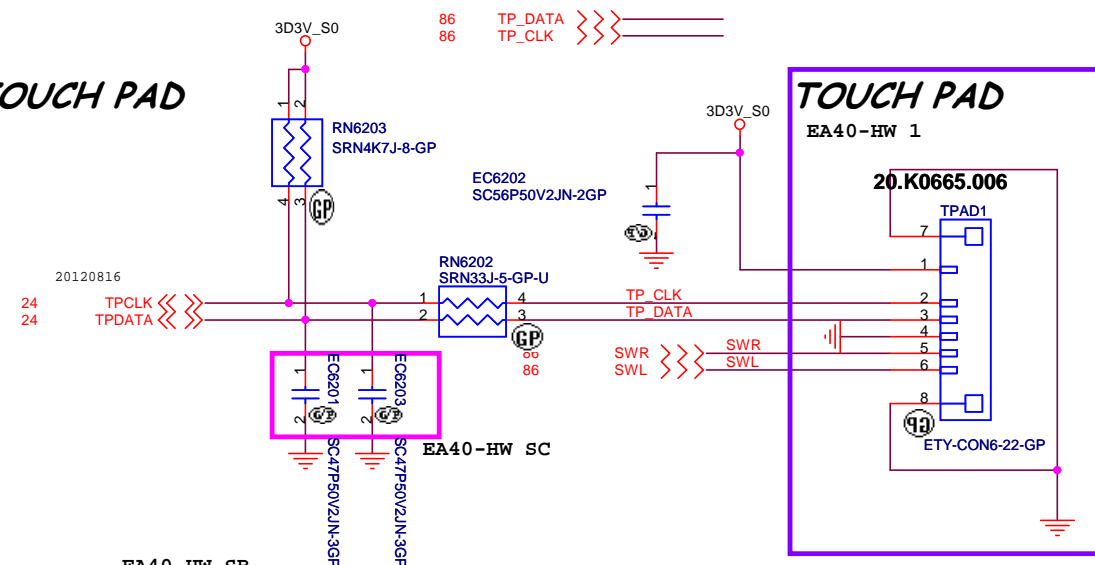
Battery LED1(CHARGE)



minatix

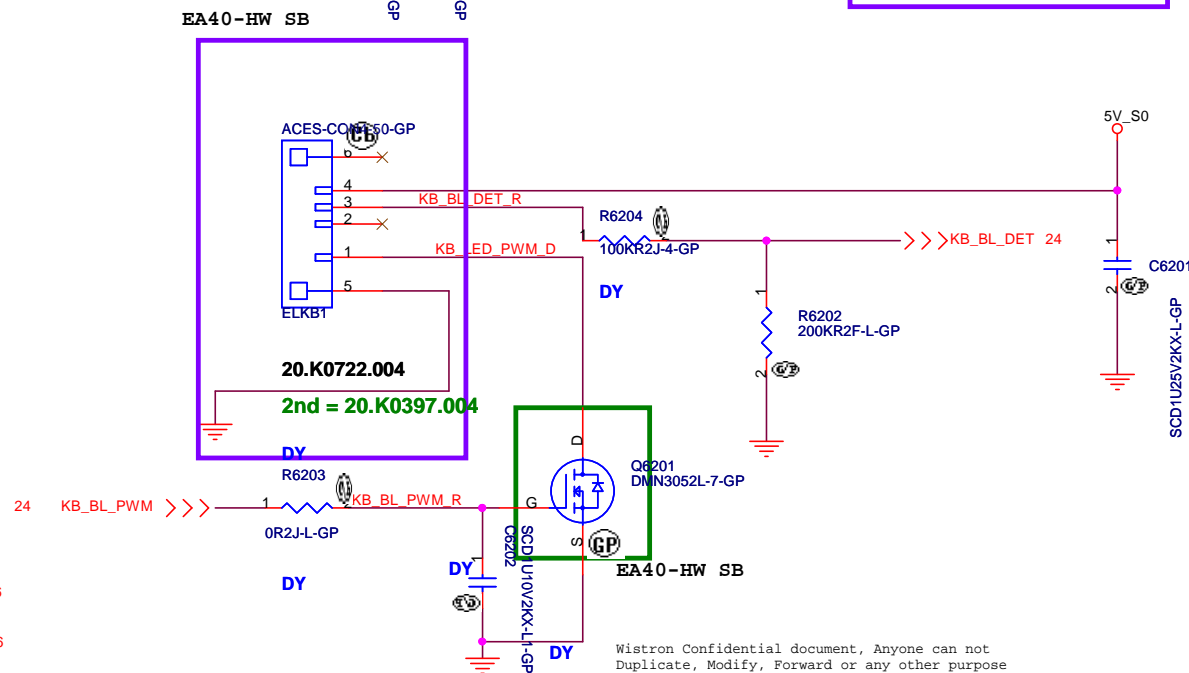
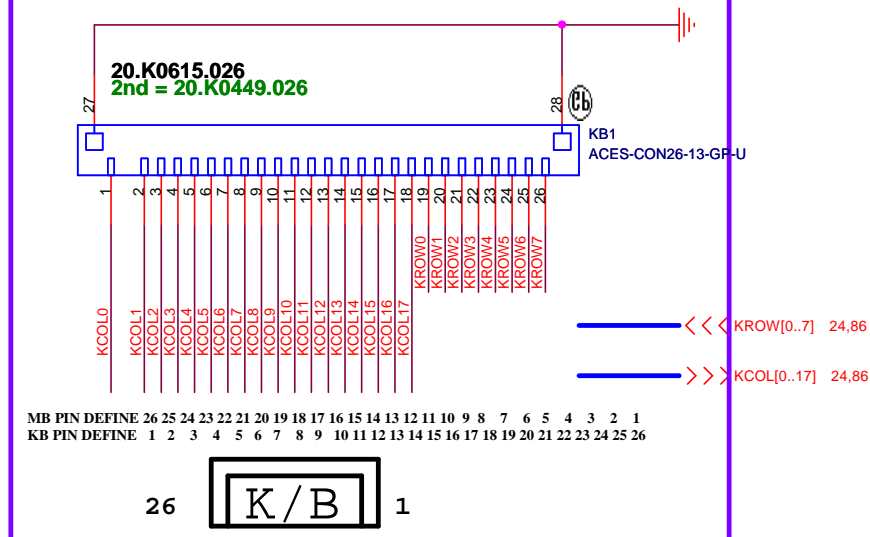


TOUCH PAD



EA40-HW SB

Internal KeyBoard Connector



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Title	Author	Year	Journal	Volume	Page
1. The Effect of Temperature on the Rate of Reaction of Hydrogen Peroxide with Potassium Iodide	John Doe	2018	Journal of Chemical Education	95	1234
2. Kinetic Study of the Reaction Between Sulfuric Acid and Sodium Hydroxide	Jane Smith	2019	Journal of Chemical Education	96	1235
3. The Effect of Concentration on the Rate of Reaction of Hydrogen Peroxide with Potassium Iodide	John Doe	2018	Journal of Chemical Education	95	1236
4. Kinetic Study of the Reaction Between Sulfuric Acid and Sodium Hydroxide	Jane Smith	2019	Journal of Chemical Education	96	1237
5. The Effect of Temperature on the Rate of Reaction of Hydrogen Peroxide with Potassium Iodide	John Doe	2018	Journal of Chemical Education	95	1238
6. Kinetic Study of the Reaction Between Sulfuric Acid and Sodium Hydroxide	Jane Smith	2019	Journal of Chemical Education	96	1239
7. The Effect of Concentration on the Rate of Reaction of Hydrogen Peroxide with Potassium Iodide	John Doe	2018	Journal of Chemical Education	95	1240
8. Kinetic Study of the Reaction Between Sulfuric Acid and Sodium Hydroxide	Jane Smith	2019	Journal of Chemical Education	96	1241
9. The Effect of Temperature on the Rate of Reaction of Hydrogen Peroxide with Potassium Iodide	John Doe	2018	Journal of Chemical Education	95	1242
10. Kinetic Study of the Reaction Between Sulfuric Acid and Sodium Hydroxide	Jane Smith	2019	Journal of Chemical Education	96	1243

Key Board/Touch Pad

Size

Document Number

Customer	Equipment Number
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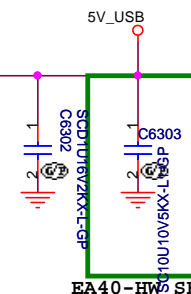
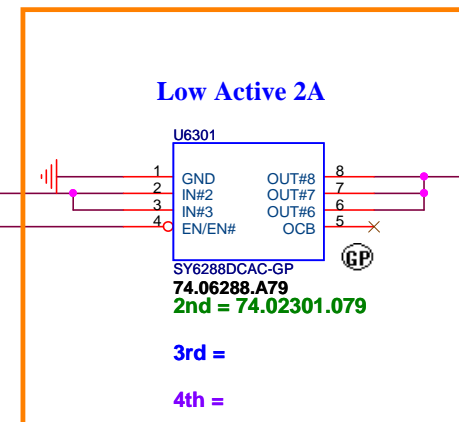
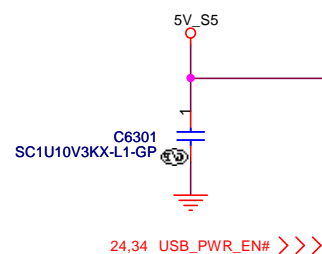
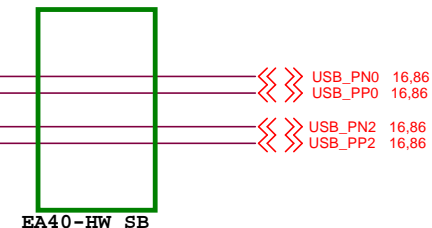
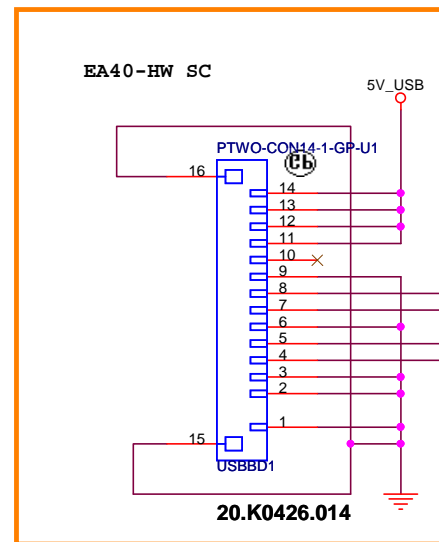
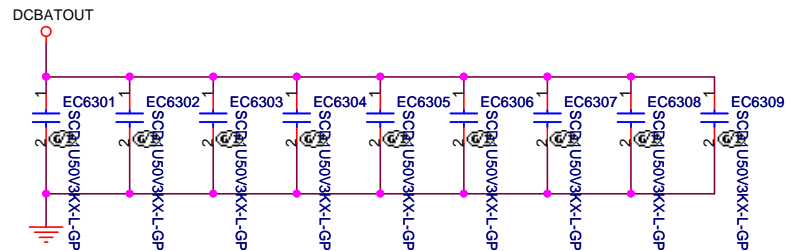
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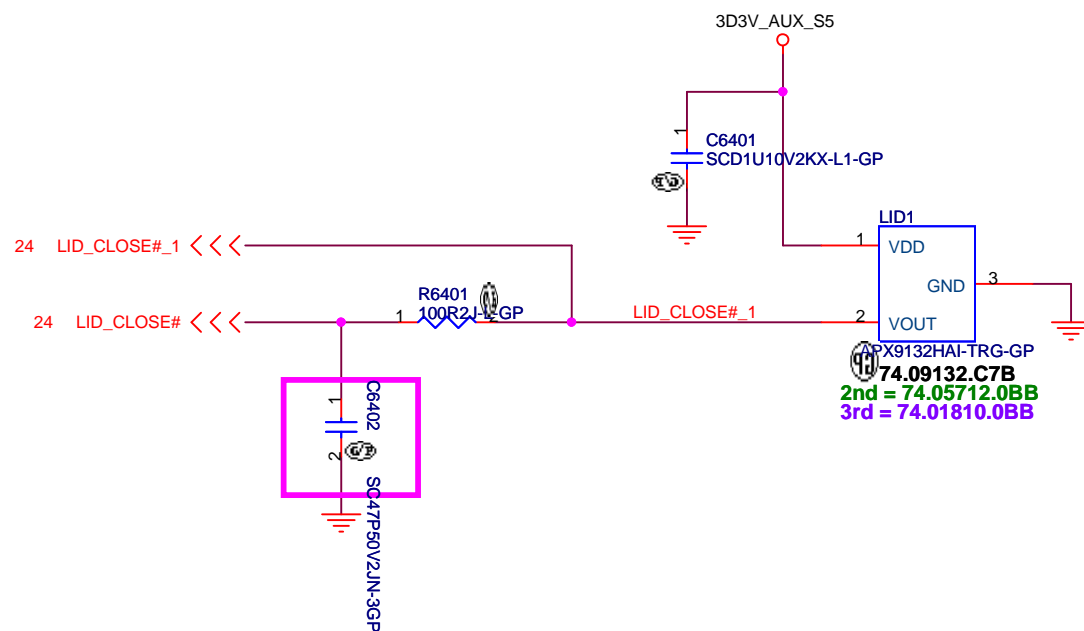


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IO Board Connector			
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Hall Sensor

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A4

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(Blanking)

Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

SDO="H"; address="3Ah"
*SDO="L"; address="38h"

*CS="H"; mode="I2C"
CS="L"; mode="SPI"

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Title

G Sensor

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Title **Thunderbolt (2/5)**

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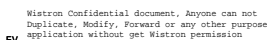
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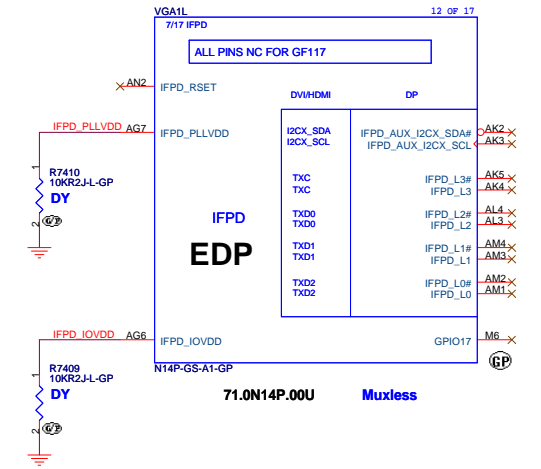
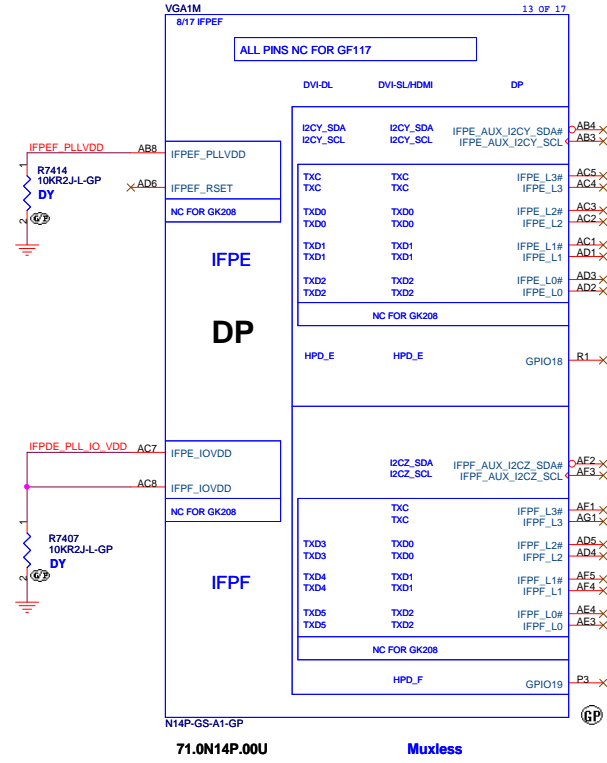
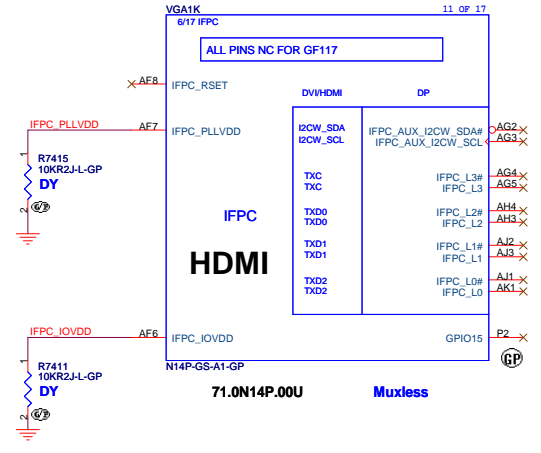
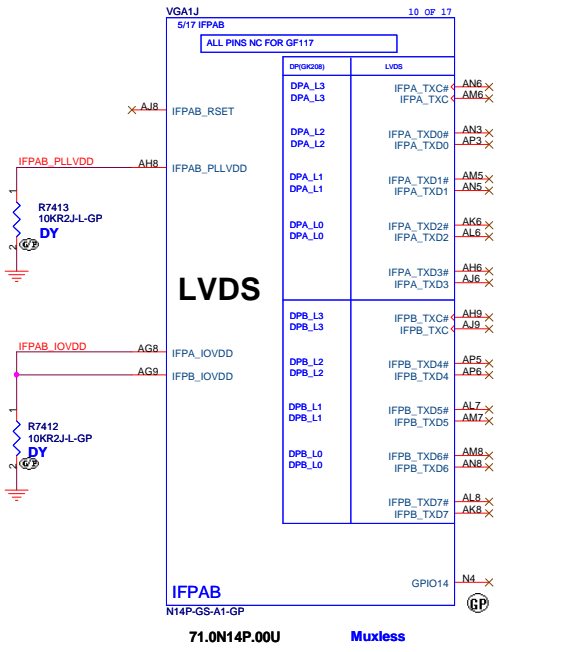
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Title			
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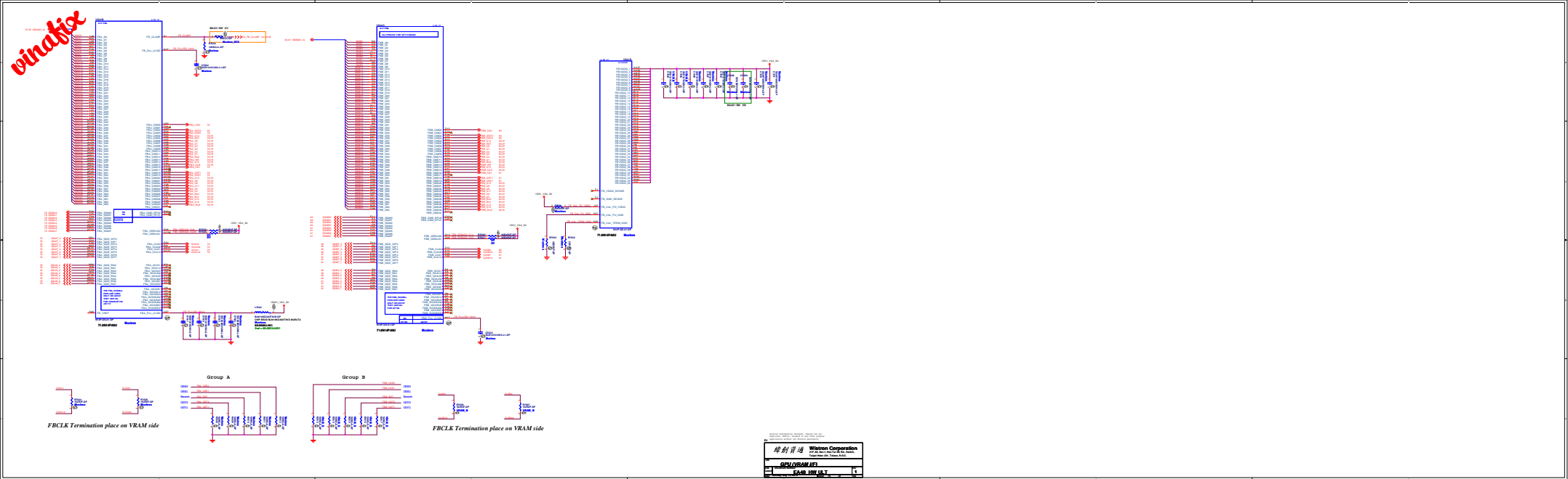
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Title GPU (DIGITALOUT)	
Size	Document Number EA40 HW ULT
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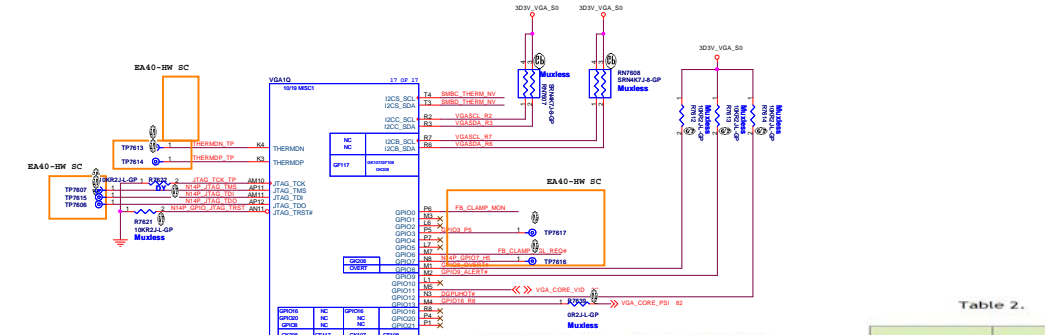
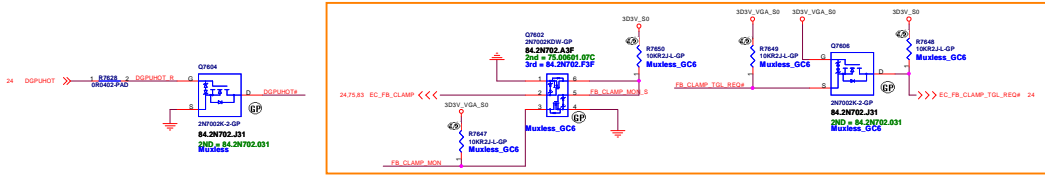
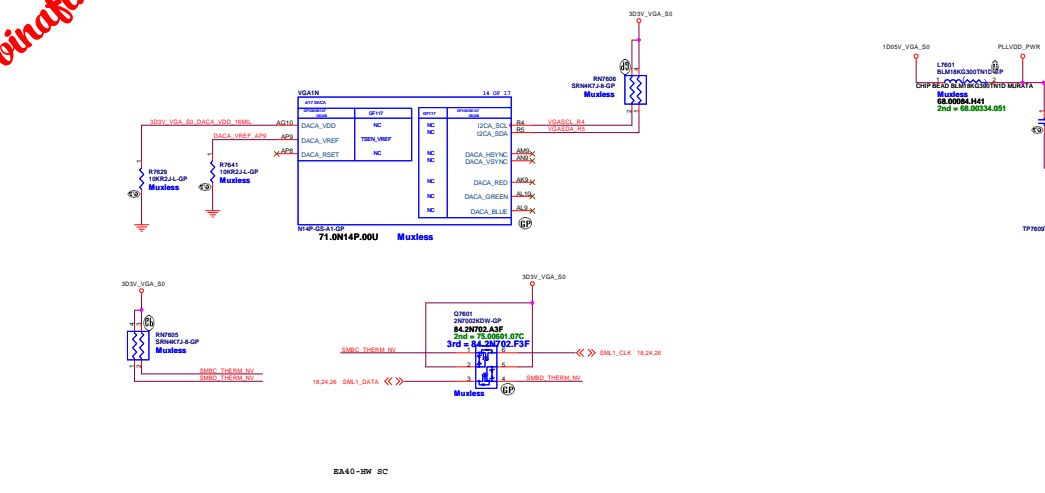
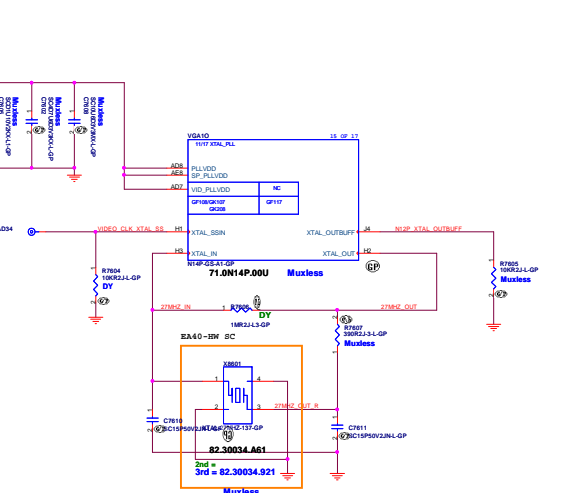
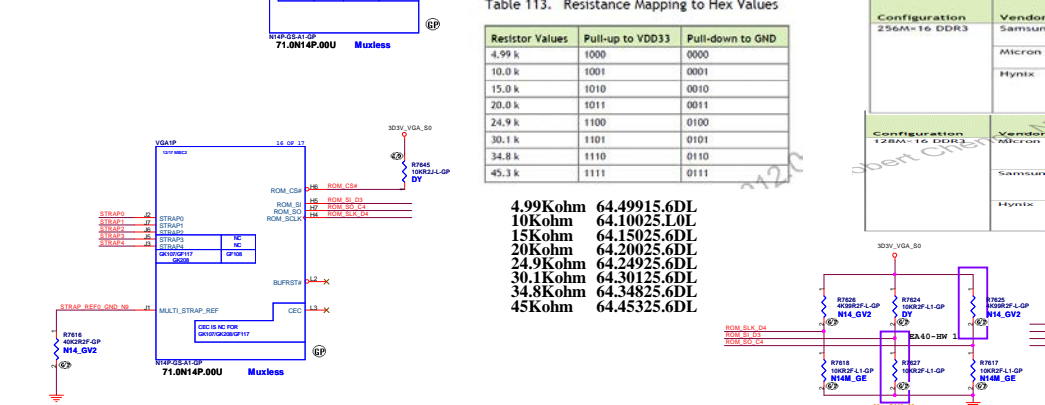


Table 113. Resistance Mapping to Hex Values

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

4.99Kohm	64.49915.6DL
10Kohm	64.10025.L0L
15Kohm	64.15025.6DL
20Kohm	64.20025.6DL
24.9Kohm	64.24925.6DL
30.1Kohm	64.30125.6DL
34.8Kohm	64.34825.6DL
45Kohm	64.45325.6DL



N14M-GE use Binary Strap. Please see the below information.

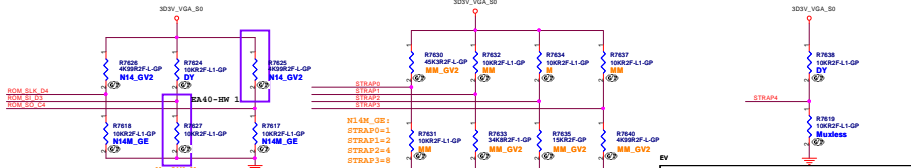
Table 122 Binary Strap Mode Mapping

Strap Pin Name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10k Ω	Pull-down to GND
ROM_SI	SMB_VIDH0R	10k Ω	Pull-down to 3V3 if VBIOS ROM exposed Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10k Ω	Pull-down to GND (no display)
STRAP0	RAH_CFG[0]	10k Ω	See Hoto below
STRAP1	RAH_CFG[1]	10k Ω	See Hoto below
STRAP2	RAH_CFG[2]	10k Ω	See Hoto below
STRAP3	RAH_CFG[3]	10k Ω	See Hoto below
STRAP4	PCI_MAX_SPEED	10k Ω	Pull-down to GND

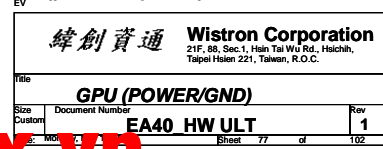
Strap Pin Name	Logical Shipping B03	Logical Shipping B02	Logical Shipping B01	Logical Shipping B00
ROM_CLK	PCI_DEVID[4]	SUB_VENDOR	PCI_DEVID[5]	FLEX_FLN_EN_TERM
	0	0	0	0
ROM_S1	RAM_CFG[1]	RAM_CFG[2]	RAM_CFG[0]	RAM_CFG[3]
	0	0	0	0
ROM_SD	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
	0	0	0	0
STRAP 0	USBR[1]	USBR[2]	USBR[1]	USBR[0]
	1	1	1	1
STRAP 1	NOIO_PADCFG[3]	NOIO_PADCFG[2]	NOIO_PADCFG[1]	NOIO_PADCFG[0]
	0	0	0	0
STRAP 2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
	0	0	0	0
STRAP 3	S0R1_EXPOSED	S0R2_EXPOSED	S0R1_EXPOSED	S0R0_EXPOSED
	0	0	0	0
STRAP 4	RESERVED	PCI_EPRD_CHANGE_GEN1	PCI_MAX_SPEED	DP_FLN_VDD33V

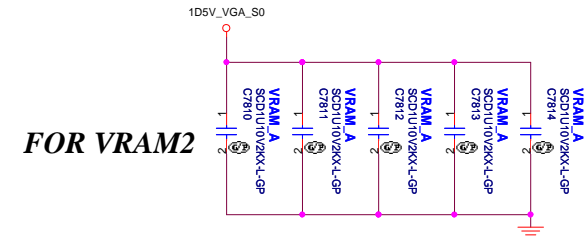
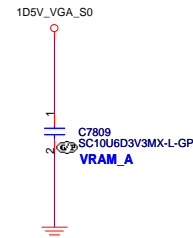
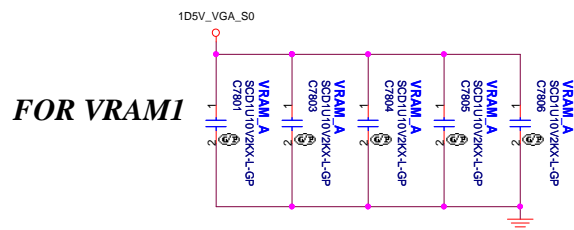
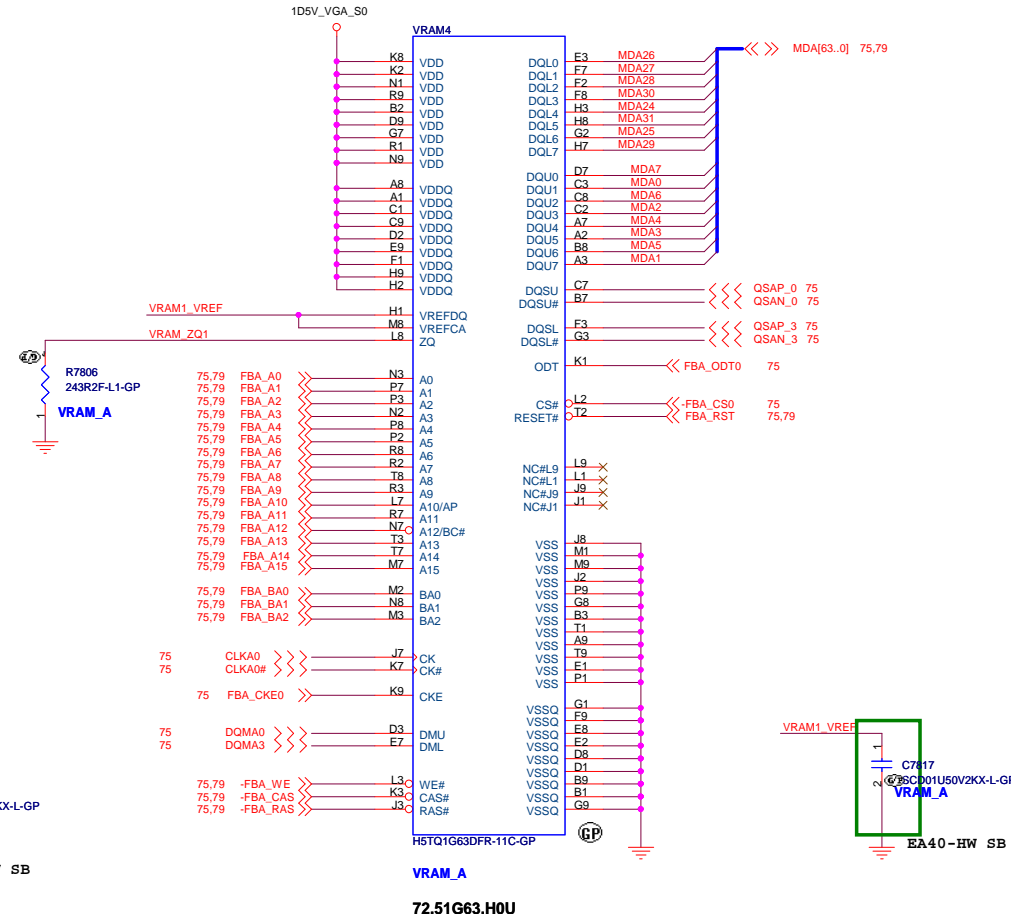
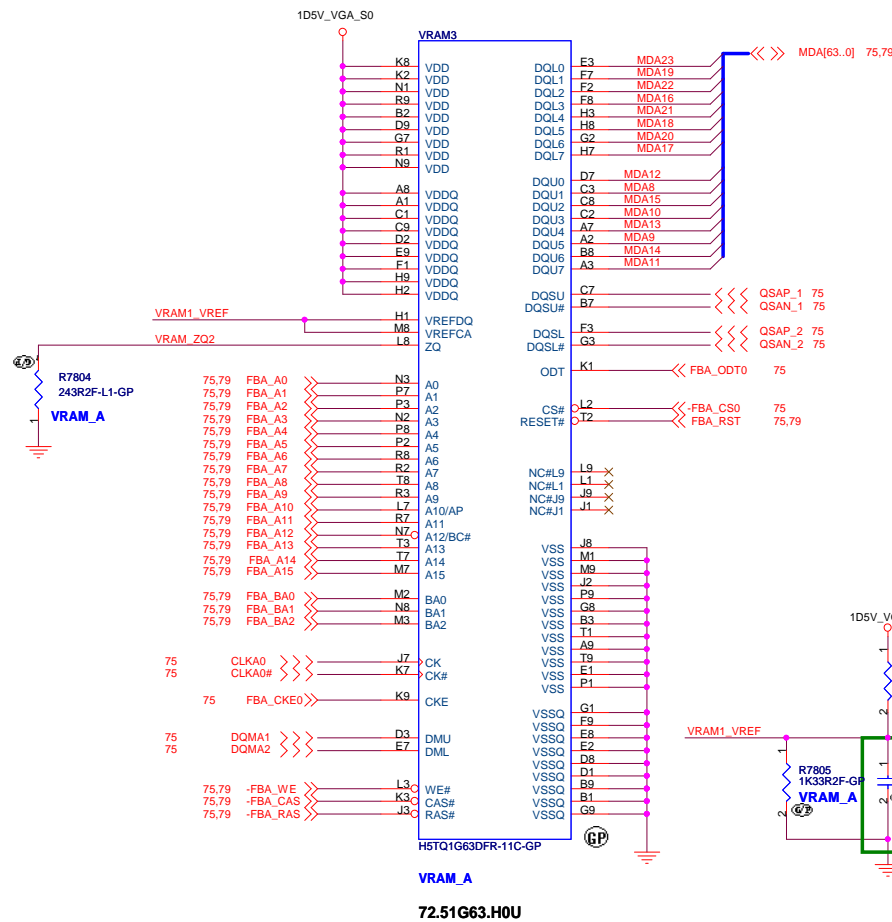
Table 2. N14M-GE/GL DDR3 Recommended Memories 256Mx16 Configuration

Configuration	Vendor	Strap	FBVDD/ FBVDQ	Manufacturer Part Number	Max Speed Data Rate (MHz)	Memory Data Code Minimum	Status
256M-16 DDR3	Samsung	0x8	1.5 V/ 1.5 V	K4W401646B-HC11	900	N/A	Production ready
	Micron	0xD	1.5 V/ 1.5 V	MT41K256M16HA-107G1E	900	N/A	Production ready
	Hynix	0x3	1.5 V/ 1.5 V	H5TQ4G63MFR-11C	900	N/A	Production ready
		0x4		H5TQ4G63AFR-11C		N/A	Post-Production Candidate
128M-16 DDR3	Micron	0x1	1.5 V/ 1.5 V	AT41128RA16JT-09AC1	1000	1234	Production ready
				AT41128RA16JT-10AC1	900	1150	Production ready
	Samsung	0x5	1.5 V/ 1.5 V	K4V2G1646E-BC1A	1000	1204	Production ready
				K4V2G1646E-BC11	900	1204	Production ready
	Hynix	0x6	1.5 V/ 1.5 V	H5TQ2G63DFR-11C	1000	N/A	Production ready
			H5TQ2G63DFR-11C	900	N/A	Production ready	



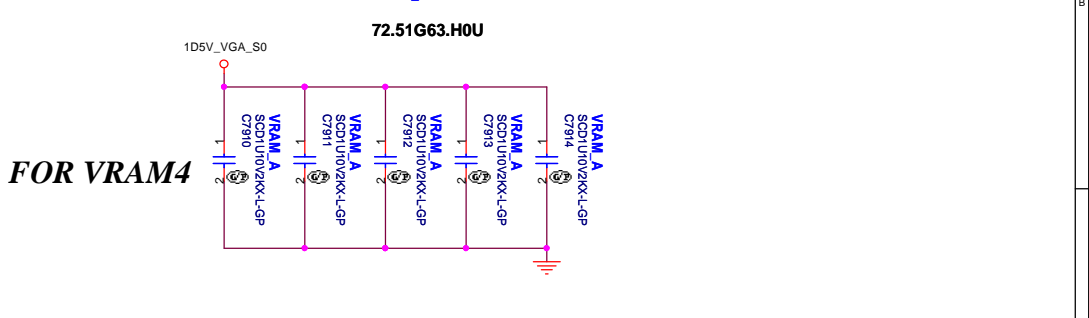
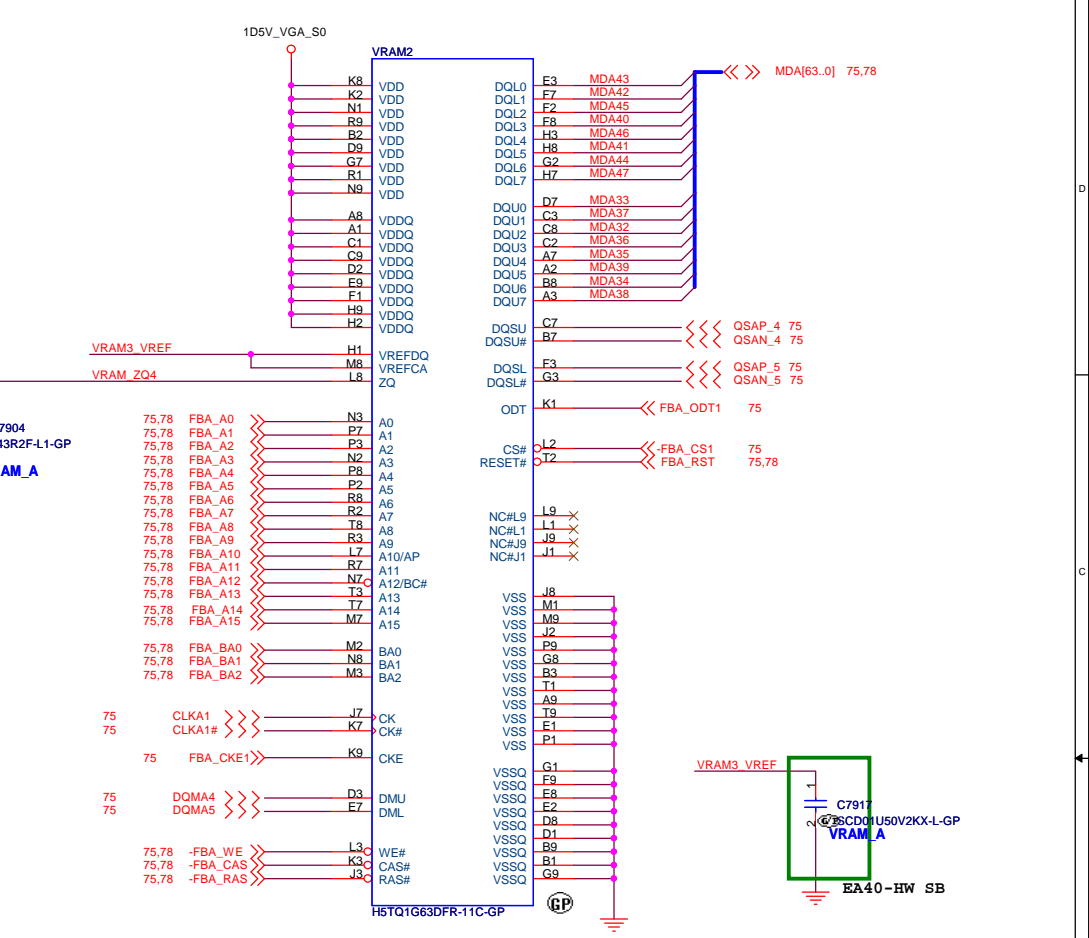
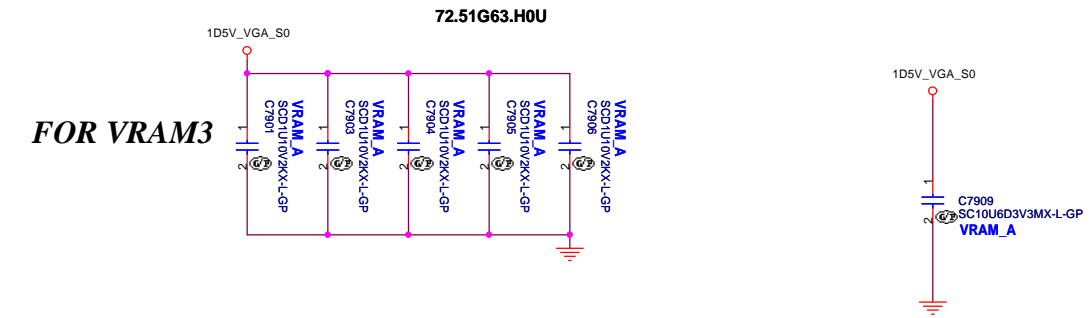
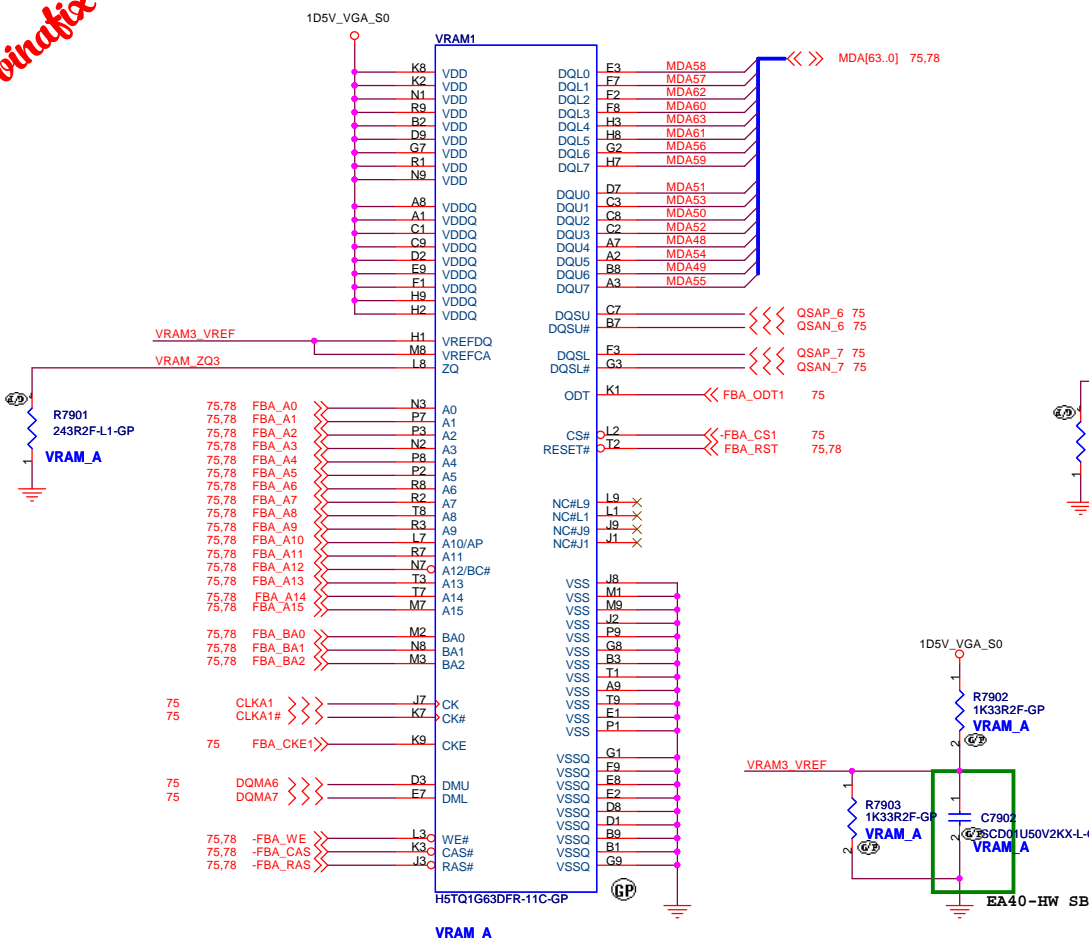
ROM_SCLK		Strap2	
N14P-GT1-A2	0x0FE4 0010	15K ohm pull down	0100 25K ohm pull down
N14P-GV2-B-A1	0x1292 1000	5K ohm pull up	0010 15K ohm pull down



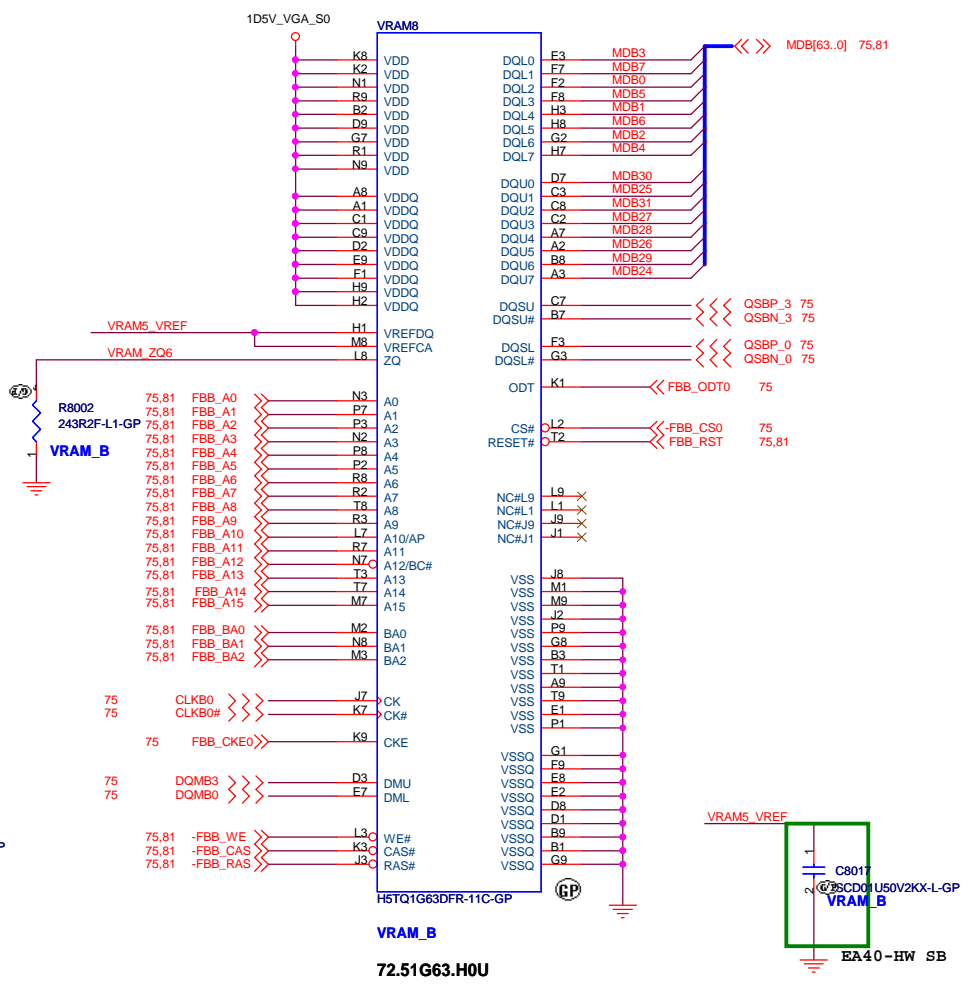
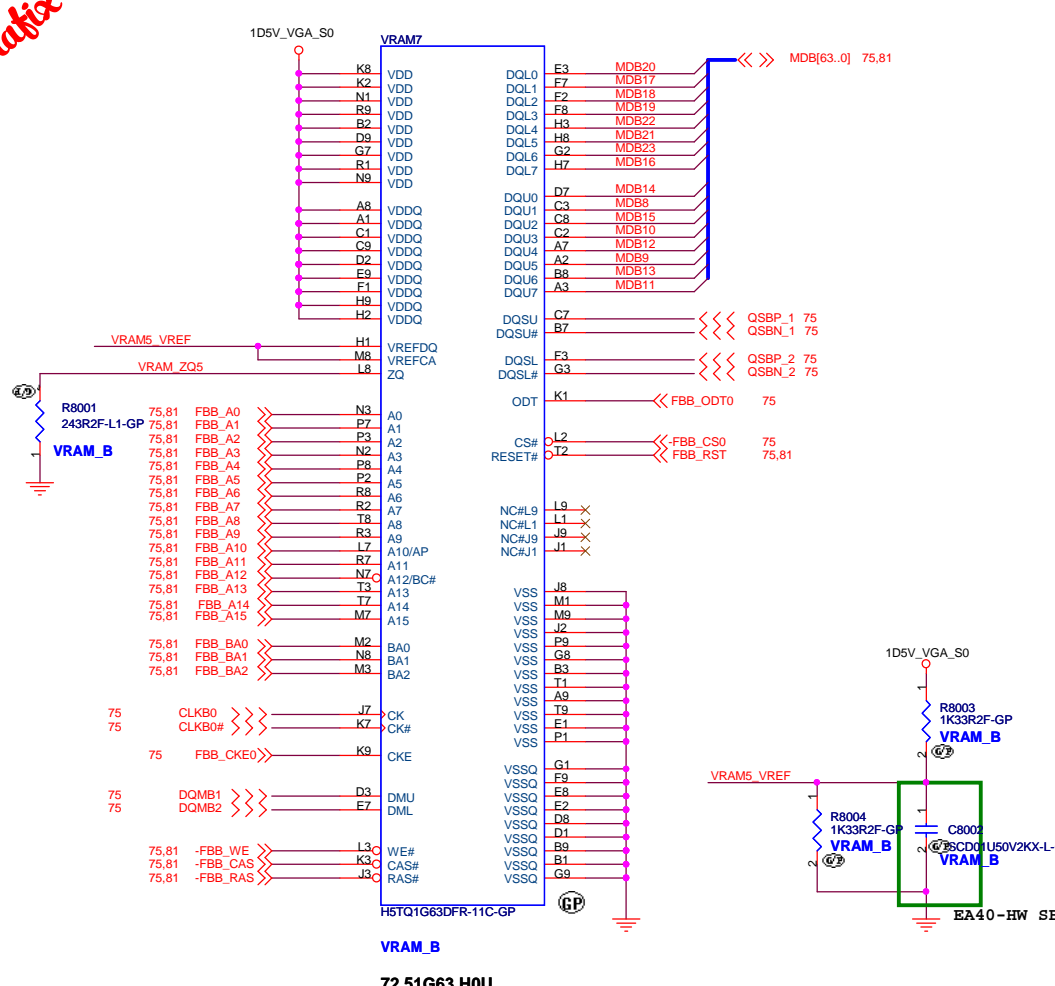


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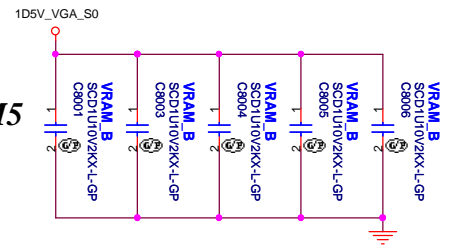
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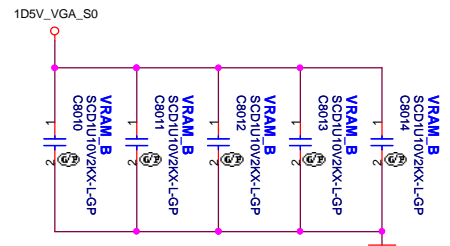
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FOR VRAM5



FOR VRAM6



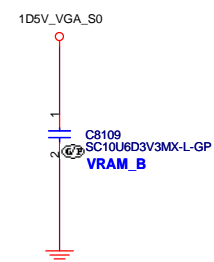
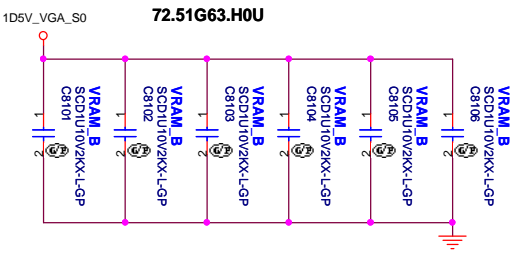
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Title GPU-VRAM5,6 (3/4)	
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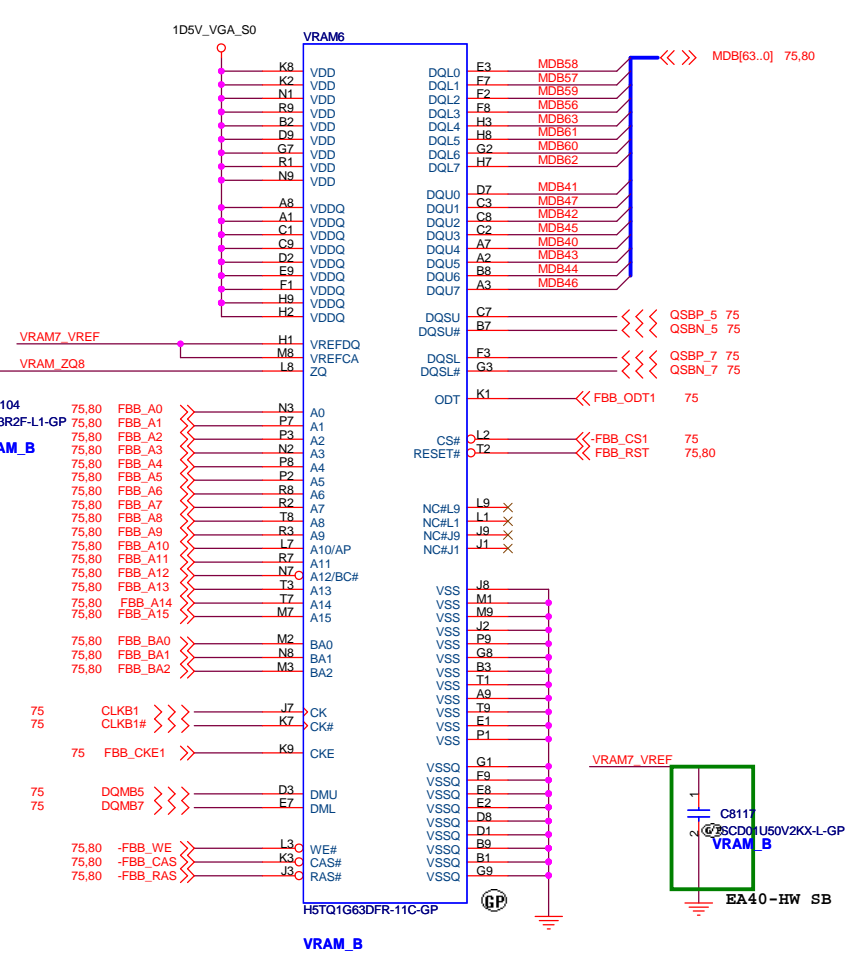
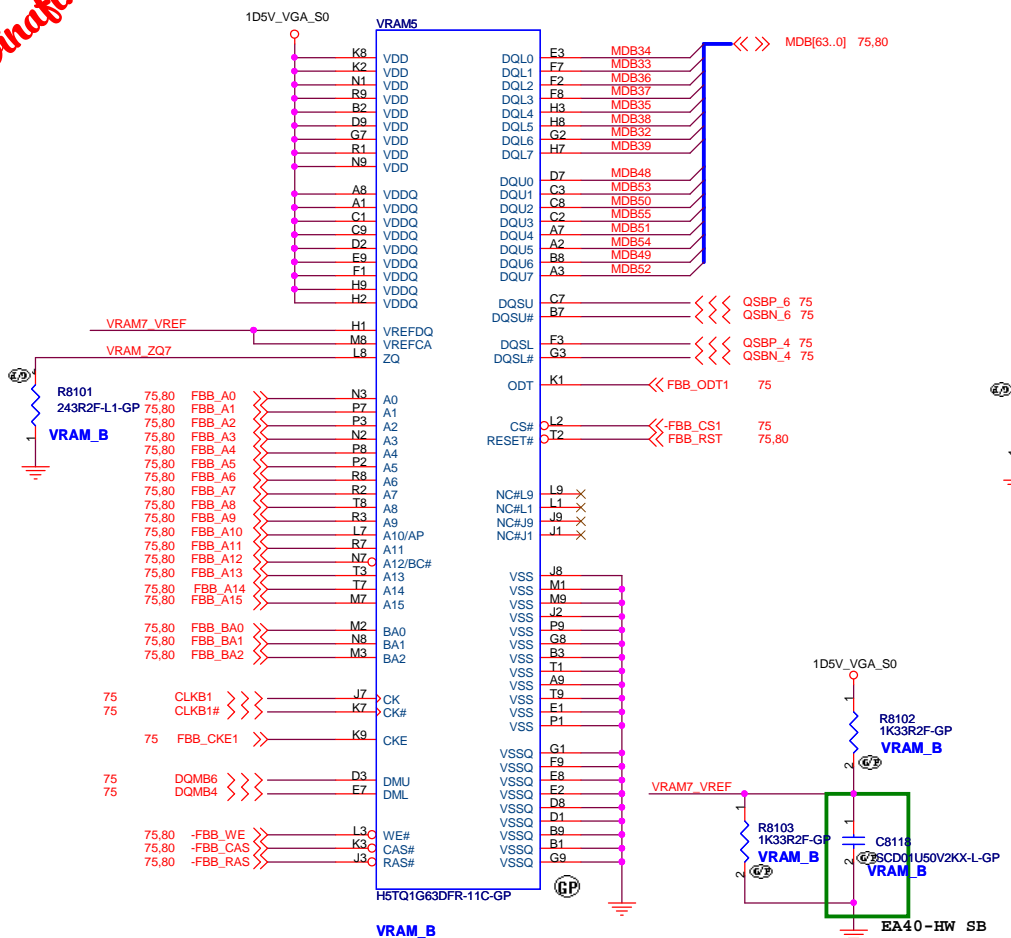
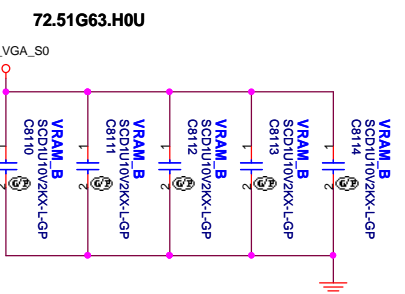
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FOR VRAM7

72.51G63.H0U




FOR VRAM8

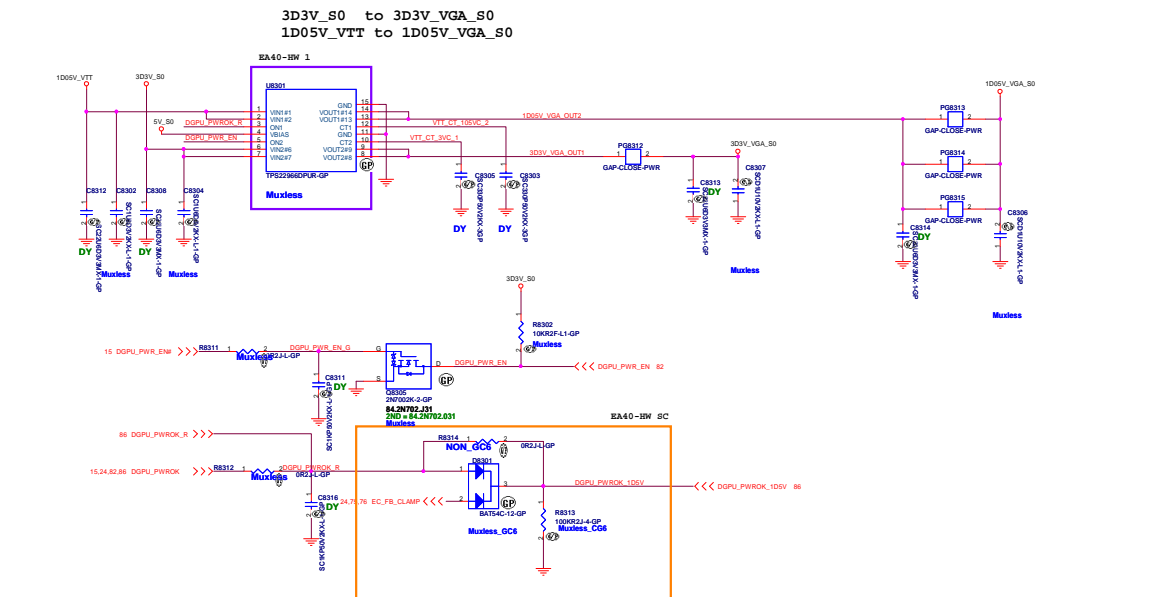


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PU8205	84.03664.037 FDMS3664S	

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RT8812A VGA CORE	
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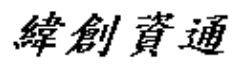
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Title Switchable GFX LCD(1/2)			
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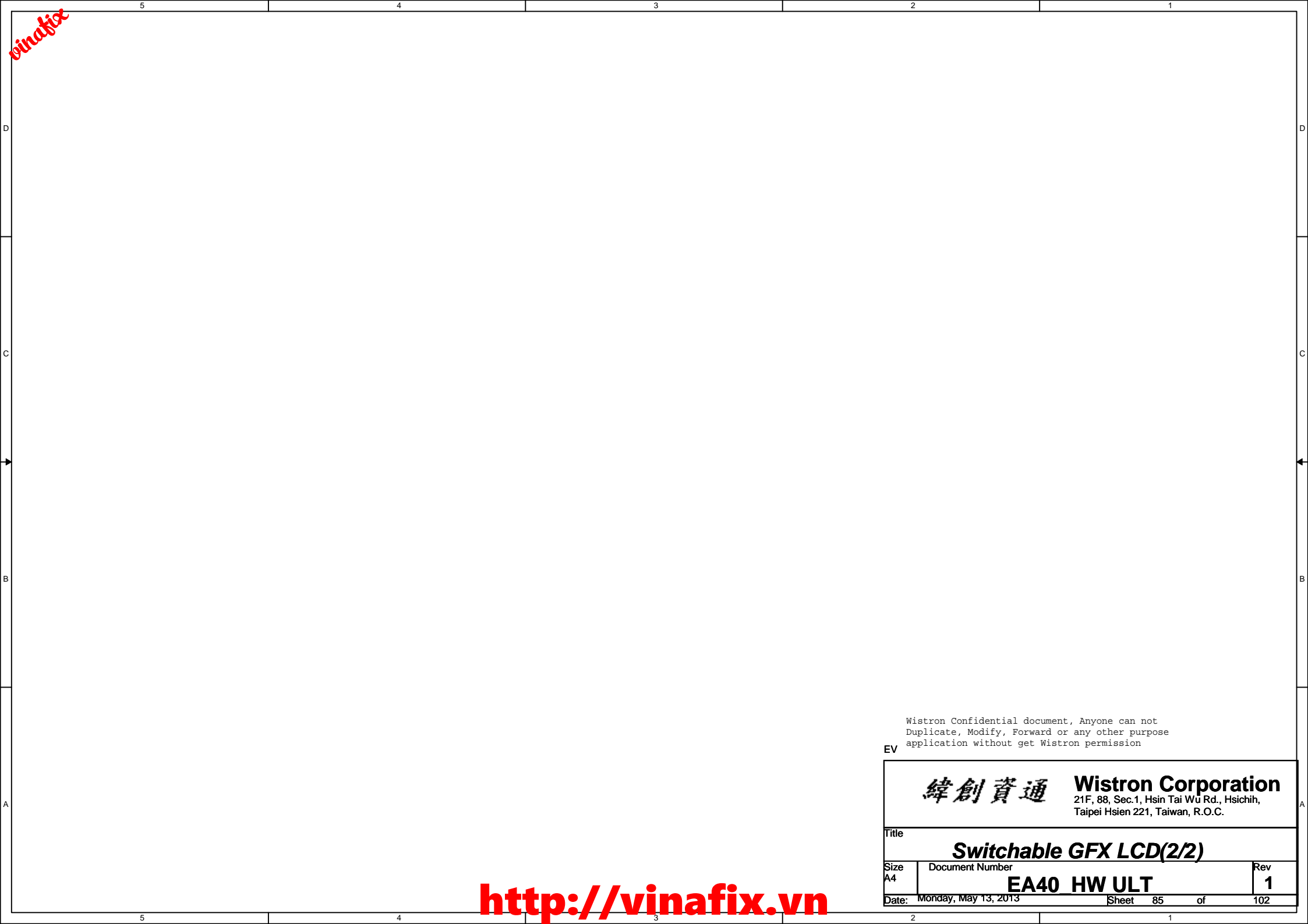
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Title

Switchable GFX LCD(2/2)

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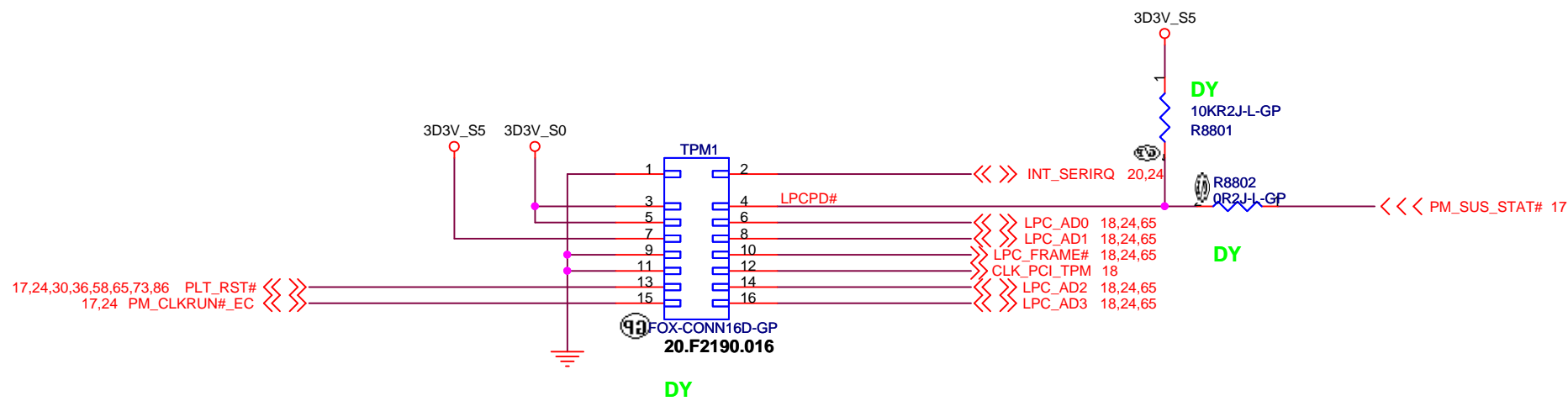
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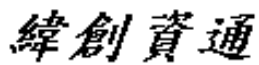
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Express Card	
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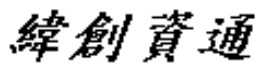
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Title Smart Card socket	
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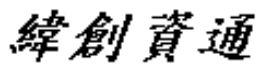
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Switchable GFX eDP	
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Title			
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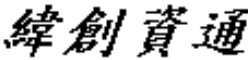
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Title LAN Switch	
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Pin	XDP Signal Name	Target Signal	I/O	Device	Pin	XDP Signal Name	Target Signal	I/O	Device
1	OBSFN_A0	Open	I/O		2	OBSFN_A1	Open	I/O	
3	GND	GND	NA		4	OBSDATA_A[0]	Open	I/O	
5	OBSDATA_A[1]	Open	I/O		6	GND	GND	NA	
7	OBSDATA_A[2]	Open	I/O		8	OBSDATA_A[3]	Open	I/O	
9	GND	GND	NA		10	HOOK0 ¹	RSMRST#	I	System
11	HOOK1	BP_PWRGD_RST# ¹	O	System	12	HOOK2	Open	NA	
13	HOOK3	Open	NA		14	HOOK4 ¹	1.05V core	NA	
15	HOOK5	Open	NA		16	VCCOBS_AB	3.3V SUS	I	System
17	HOOK6	RSMRST# ¹	O	System	18	HOOK7	DBR# ¹	O	System
19	GND	GND	NA		20	TDO	JTAG_TDO	I	PCH
21	TRSTn	Open	NA		22	TDI	JTAG_TDI	O	PCH
23	TMS	JTAG_TMS	O	PCH	24	TCK1	Open	NA	
25	GND	GND	NA		26	TCK0	JTAG_TCK	O	PCH

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PCH_XDP			
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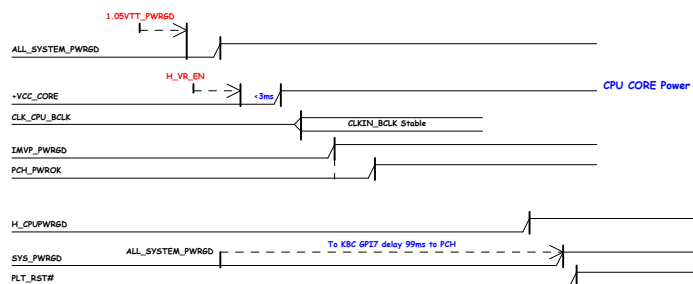
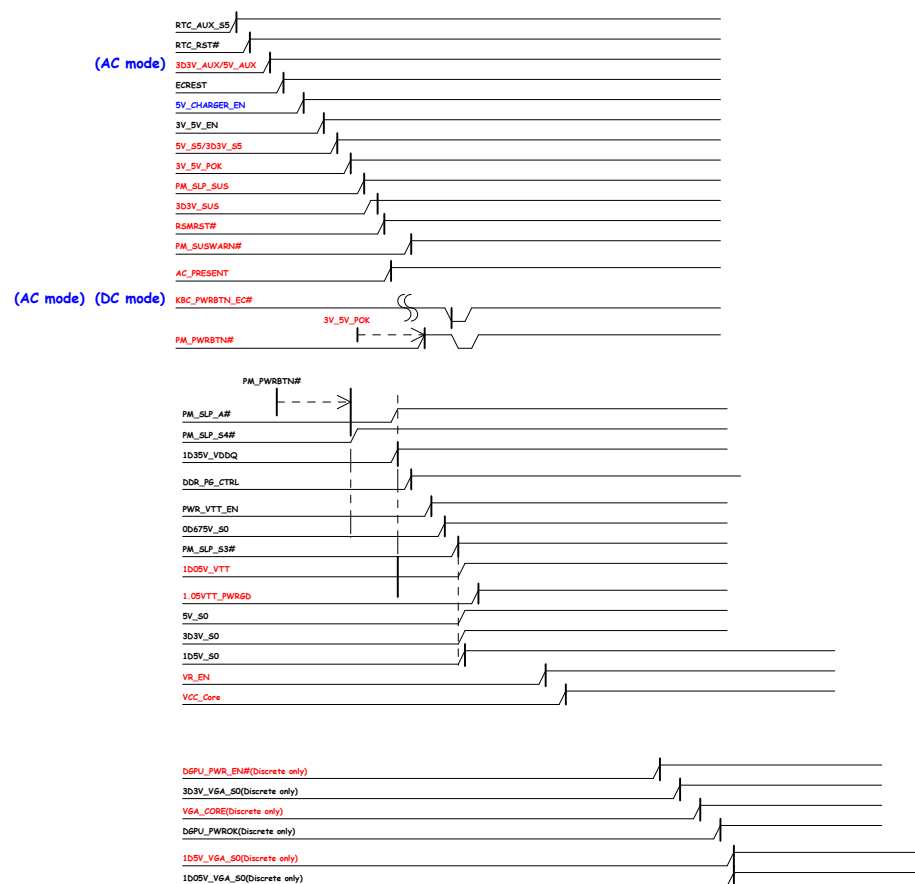
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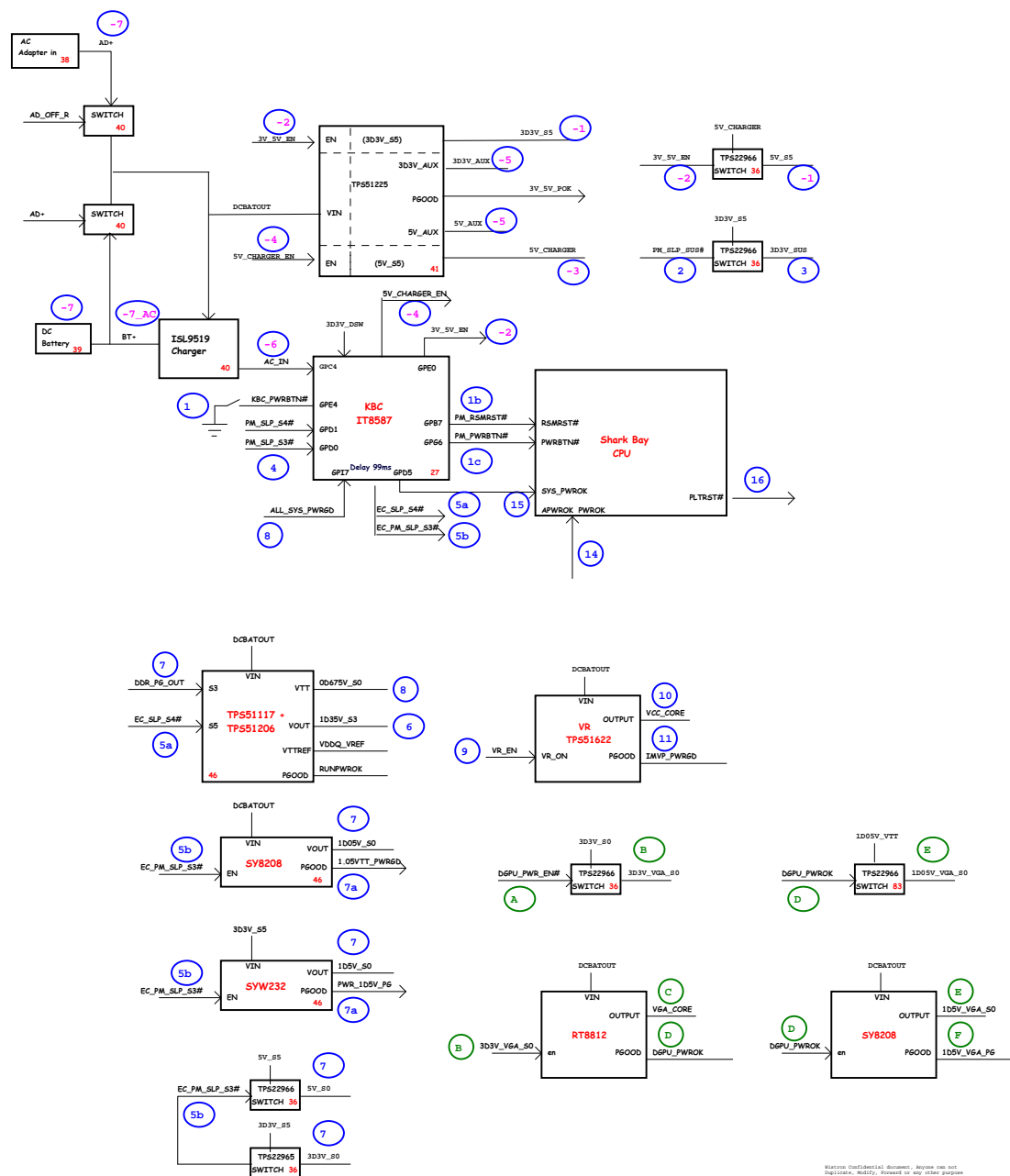
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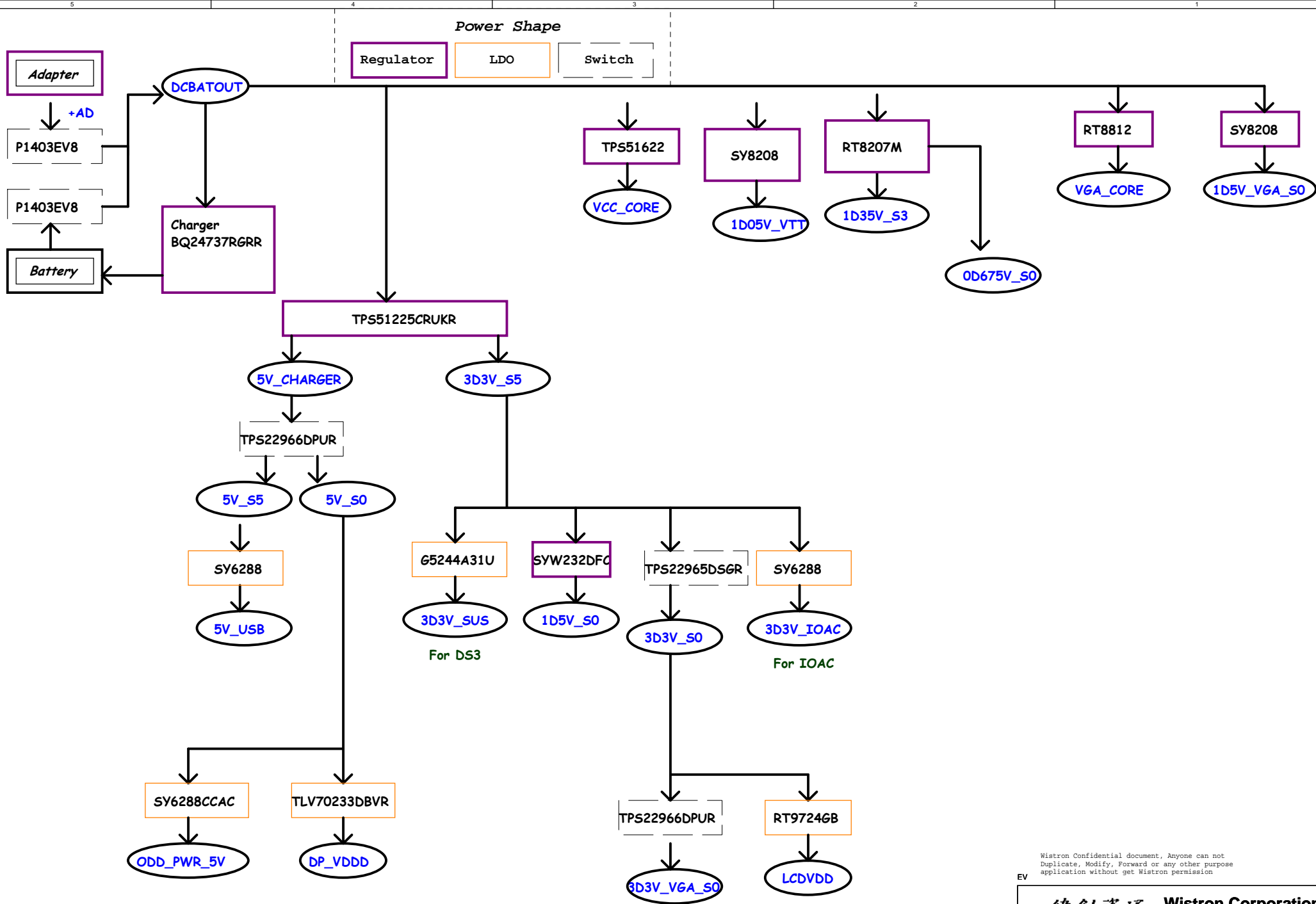
Intel-Power Up Sequence



SHARK BAY POWER UP SEQUENCE DIAGRAM



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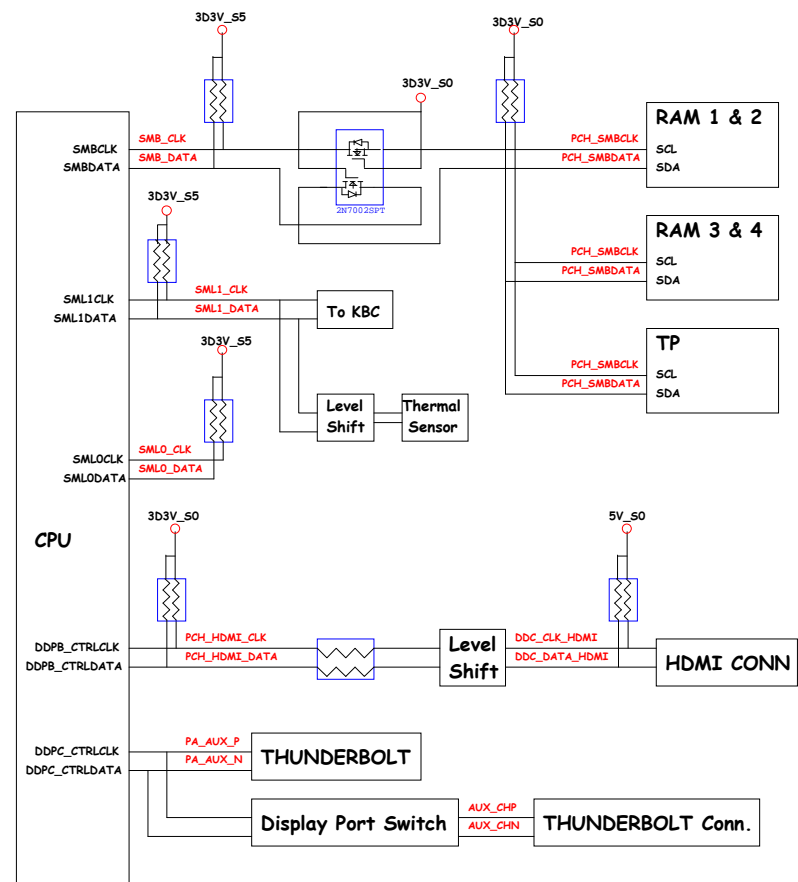
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Power Block Diagram			
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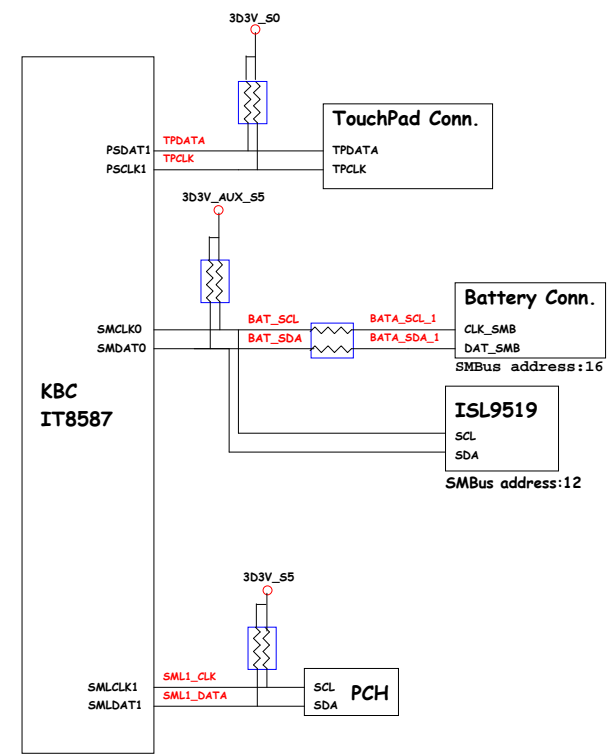
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CH SMBus Block Diagram



KBC SMBus Block Diagram

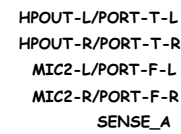


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