Cars - Berlinetta X4
Cars - Maranello X4
Cars - Barchetta X3

uATX(244 mm X 244 mm)

CPU:

Intel Skylake Processor

System Chipset:

Intel Skylake PCH-H

OnBoard Chipset:

AZALIA Codec: Realtek ALC 221 VB3
LAN: Realtek RTL8111HSH-CG 10/100/1000 NIC
SIO: Nuvoton NPCD315H
DP to VGA: ITE IT6515
Flash ROM: 128 Mb

Main Memory:

DDRIII (1600MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 2
PCI Express (X16) Slot /w X4 Signal * 1
DDI Port Slot *1

PWM:

Controller: ISL95855
Controller:TPS51216RUKR

Other:

SATA *3
USB3.0 *7 (Rear*4 Front*2 Internal*1)
USB2.0 *2 (Rear*2)
DP PORT*1
VGA PORT *1
COM PORT *1
COM Header *1

Marking	Description
I	Install
NI	Not Install
MP	Production Part ONLY
PROTO	Not For Production Part
CRITICAL	Critical Components

BOM DISTRIBUTION RULE
Berlinetta,Maranello,Barchetta
(BOM,BOM,BOM)

BOARD REV	Development Phase	
0	DB-1	
1	DB-2	
2	DB-3	
3	SI-1	
4	SI-2	
5	SI-3	
6	PV-1	●
7	PV-2	

PCA P/N, BERLINETTA/MARANELLO/BARCHETTA	793305-001/793305-002/793302-001
SCH P/N, BERLINETTA/MARANELLO/BARCHETTA	793306-000/793306-000/793303-000
PCB P/N, BERLINETTA/MARANELLO/BARCHETTA	793307-001/793307-001/793304-001
SSID, BERLINETTA/MARANELLO/BARCHETTA	805F/8061/8060
Board ID, BERLINETTA/MARANELLO/BARCHETTA	7/8/9

	Berlinetta	Maranello	Barchetta
PCH	H170	H110	H110

Project	
Berlinetta	
Maranello	V
Barchetta	

Latest modified date:
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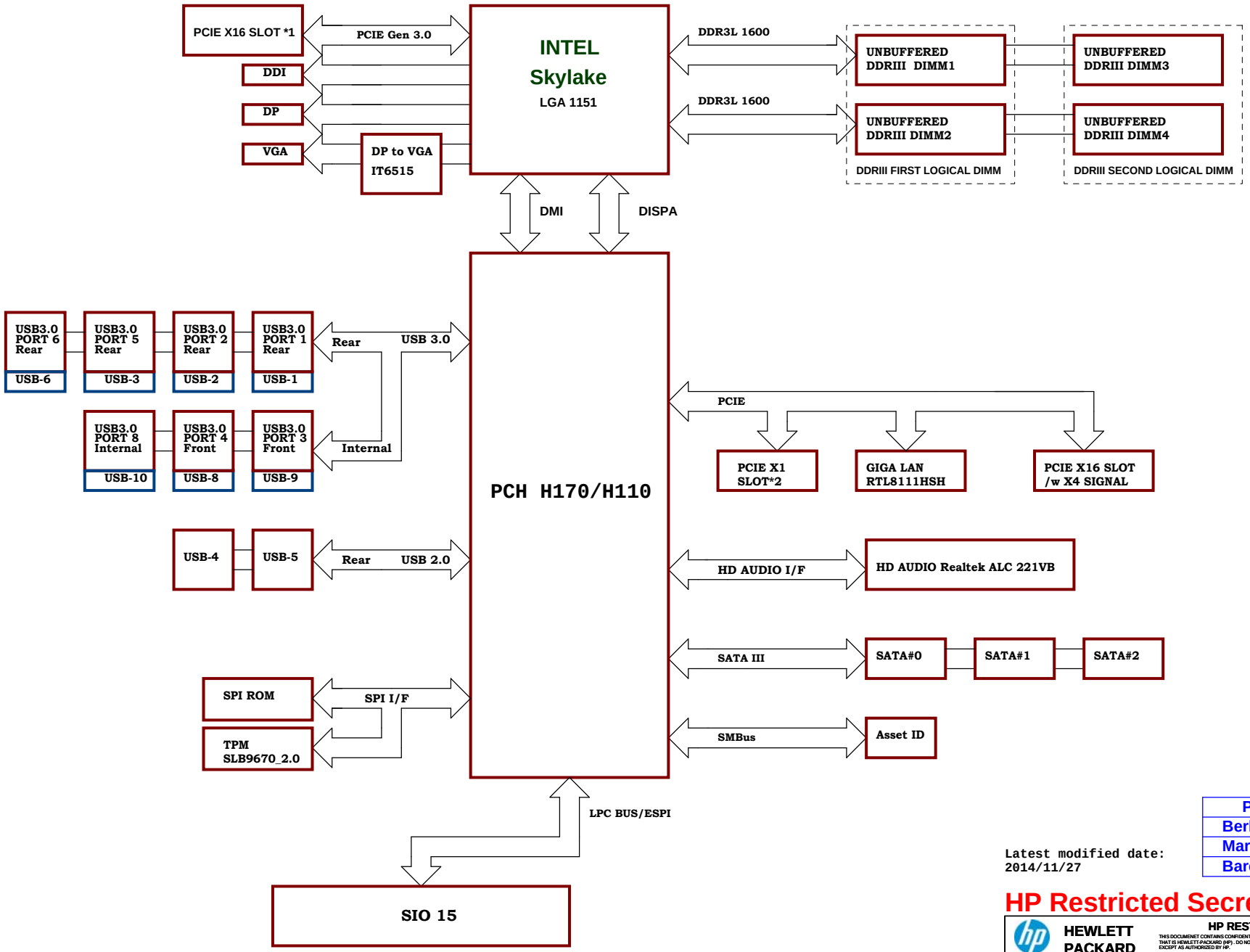
Title: Cover Sheet

Size: Custom | Document Number: HP SCH P/N: 793306-000(MSI MS-7957) | Rev: X4

Date: Friday, June 05, 2015 | Sheet 1 of 65



Project	
Berlinetta	V
Maranello	V
Barchetta	

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Title: Block Diagram

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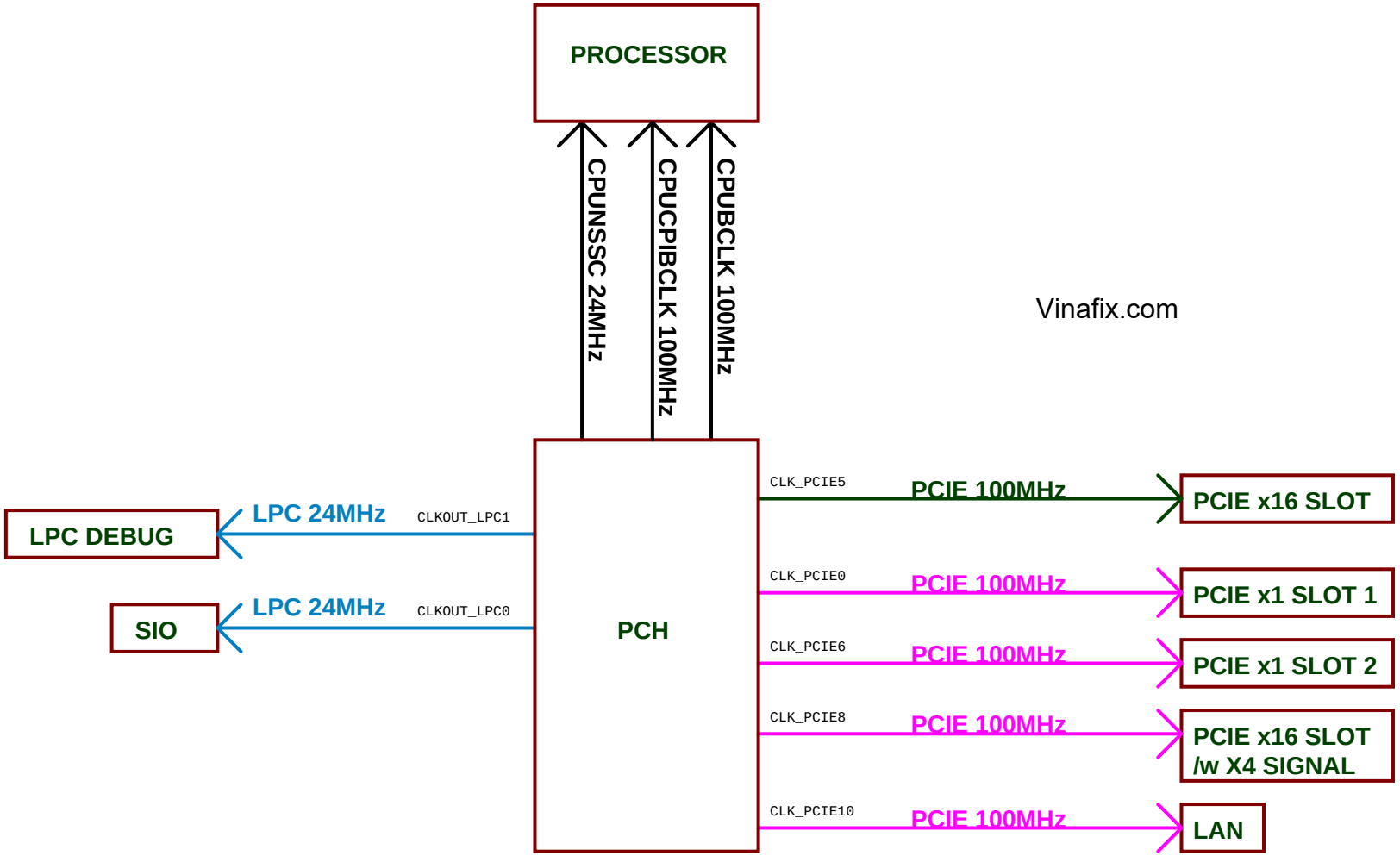

Project	
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Maranello	V
Barchetta	

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Title: **Clock Distribution**

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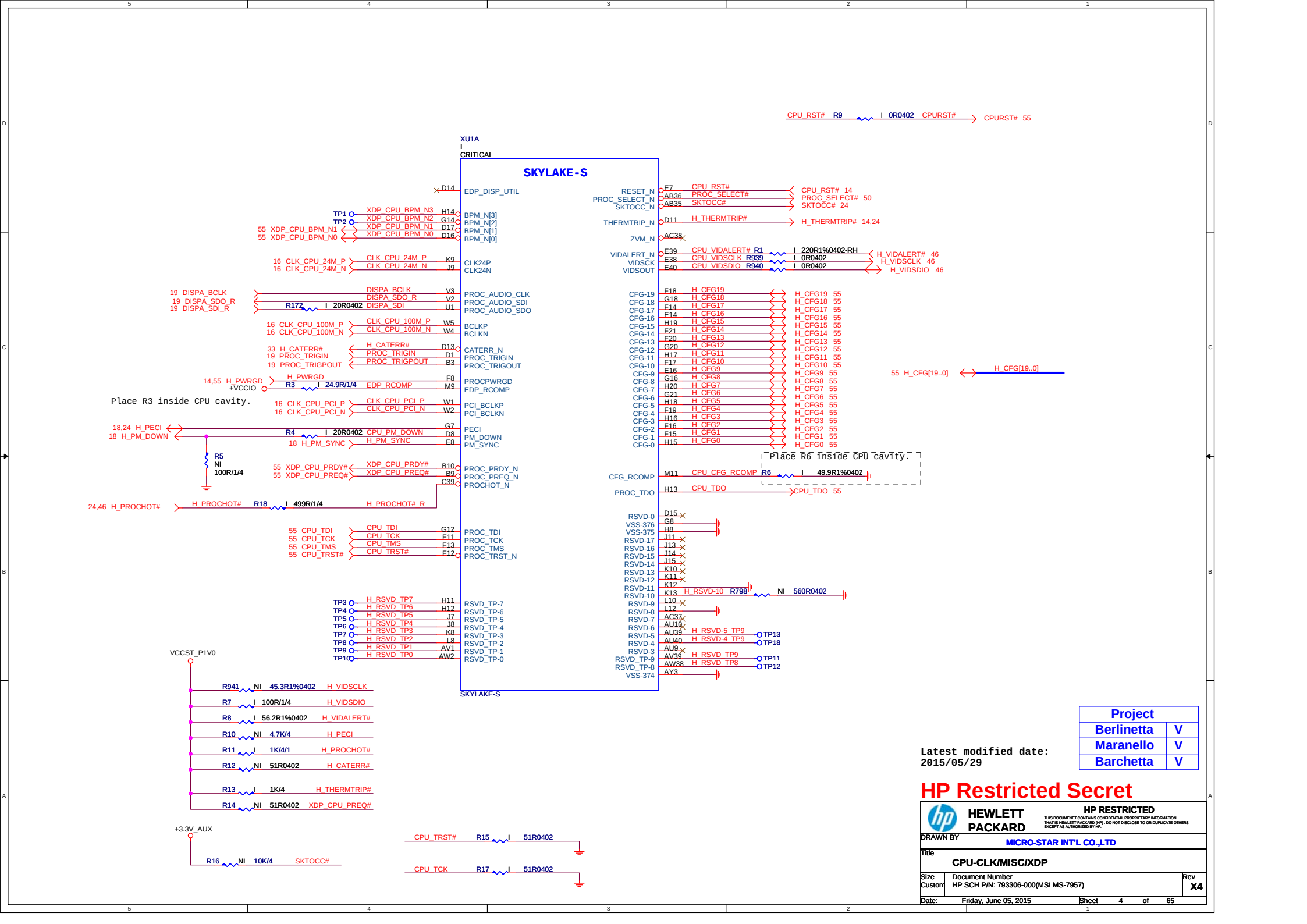
XU1A
CRITICAL
SKYLAKE-S
SKYLAKE-S
CPU_RST# R9 0R0402 CPURST# CPURST# 55
D14 EDP_DISP_UTIL
TP1 XDP_CPU_BPM_N3 H14 BPM_N[3]
TP2 XDP_CPU_BPM_N2 G14 BPM_N[2]
55 XDP_CPU_BPM_N1 XDP_CPU_BPM_N1 D17 BPM_N[1]
55 XDP_CPU_BPM_N0 XDP_CPU_BPM_N0 D16 BPM_N[0]
16 CLK_CPU_24M_P CLK_CPU_24M_P K9 CLK24P
16 CLK_CPU_24M_N CLK_CPU_24M_N J9 CLK24N
19 DISPA_BCLK DISPA_BCLK V3 PROC_AUDIO_CLK
19 DISPA_SDO_R DISPA_SDO_R V2 PROC_AUDIO_SDI
19 DISPA_SDI_R R172 20R0402 DISPA_SDI U1 PROC_AUDIO_SDO
16 CLK_CPU_100M_P CLK_CPU_100M_P W5 BCLKP
16 CLK_CPU_100M_N CLK_CPU_100M_N W4 BCLKN
33 H_CATERR# H_CATERR# D13 CATERR_N
19 PROC_TRIGIN PROC_TRIGIN D1 PROC_TRIGIN
19 PROC_TRIGPOUT PROC_TRIGPOUT B3 PROC_TRIGOUT
14,55 H_PWRGD H_PWRGD F8 PROCPWRGD
+VCCIO R3 24.9R/1/4 EDP_RCOMP M9 EDP_RCOMP
Place R3 inside CPU cavity.
16 CLK_CPU_PCI_P CLK_CPU_PCI_P W1 PCI_BCLKP
16 CLK_CPU_PCI_N CLK_CPU_PCI_N W2 PCI_BCLKN
18,24 H_PECI G7 PECI
18 H_PM_DOWN R4 20R0402 CPU_PM_DOWN D8 PM_DOWN
18 H_PM_SYNC H_PM_SYNC E8 PM_SYNC
R5 NI 100R/1/4
55 XDP_CPU_PRDY# XDP_CPU_PRDY# B10 PROC_PRDY_N
55 XDP_CPU_PREQ# XDP_CPU_PREQ# B9 PROC_PREQ_N
C39 PROCHOT_N
24,46 H_PROCHOT# H_PROCHOT# R18 499R/1/4 H_PROCHOT#_R
55 CPU_TDI CPU_TDI G12 PROC_TDI
55 CPU_TCK CPU_TCK F11 PROC_TCK
55 CPU_TMS CPU_TMS F13 PROC_TMS
55 CPU_TRST# CPU_TRST# F12 PROC_TRST_N
TP3 H_RSVD_TP7 H11 RSVD_TP-7
TP4 H_RSVD_TP6 H12 RSVD_TP-6
TP5 H_RSVD_TP5 J7 RSVD_TP-5
TP6 H_RSVD_TP4 J8 RSVD_TP-4
TP7 H_RSVD_TP3 K8 RSVD_TP-3
TP8 H_RSVD_TP2 L8 RSVD_TP-2
TP9 H_RSVD_TP1 AV1 RSVD_TP-1
TP10 H_RSVD_TP0 AW2 RSVD_TP-0
VCCST_P1V0
R941 NI 45.3R1%0402 H_VIDSCLK
R7 100R/1/4 H_VIDSDIO
R8 56.2R1%0402 H_VIDALERT#
R10 NI 4.7K/4 H_PECI
R11 1K/4/1 H_PROCHOT#
R12 NI 51R0402 H_CATERR#
R13 1K/4 H_THERMTRIP#
R14 NI 51R0402 XDP_CPU_PREQ#
+3.3V_AUX
R16 NI 10K/4 SKTOCC#
CPU_TRST# R15 51R0402
CPU_TCK R17 51R0402
RESET_N E7 CPU_RST# CPU_RST# 14
PROC_SELECT_N AB36 PROC_SELECT# PROC_SELECT# 50
SKTOCC_N AB35 SKTOCC# SKTOCC# 24
THERMTRIP_N D11 H_THERMTRIP# H_THERMTRIP# 14,24
ZVM_N AC38
VIDALERT_N E39 CPU_VIDALERT# R1 220R1%0402-RH H_VIDALERT# 46
VIDSCK E38 CPU_VIDSCLK R939 0R0402 H_VIDSCLK 46
VIDSOUT E40 CPU_VIDSDIO R940 0R0402 H_VIDSDIO 46
CFG-19 F18 H_CFG19 H_CFG19 55
CFG-18 G18 H_CFG18 H_CFG18 55
CFG-17 F14 H_CFG17 H_CFG17 55
CFG-16 E14 H_CFG16 H_CFG16 55
CFG-15 H19 H_CFG15 H_CFG15 55
CFG-14 F21 H_CFG14 H_CFG14 55
CFG-13 F20 H_CFG13 H_CFG13 55
CFG-12 G20 H_CFG12 H_CFG12 55
CFG-11 H17 H_CFG11 H_CFG11 55
CFG-10 F17 H_CFG10 H_CFG10 55
CFG-9 E16 H_CFG9 H_CFG9 55
CFG-8 G16 H_CFG8 H_CFG8 55
CFG-7 H20 H_CFG7 H_CFG7 55
CFG-6 G21 H_CFG6 H_CFG6 55
CFG-5 H18 H_CFG5 H_CFG5 55
CFG-4 F19 H_CFG4 H_CFG4 55
CFG-3 H16 H_CFG3 H_CFG3 55
CFG-2 F16 H_CFG2 H_CFG2 55
CFG-1 F15 H_CFG1 H_CFG1 55
CFG-0 H15 H_CFG0 H_CFG0 55
55 H_CFG[19..0] H_CFG[19..0]
Place R6 inside CPU cavity.
CFG_RCOMP M11 CPU_CFG_RCOMP R6 49.9R1%0402
PROC_TDO H13 CPU_TDO CPU_TDO 55
RSVD-0 D15
VSS-376 G8
VSS-375 H8
RSVD-17 J11
RSVD-16 J13
RSVD-15 J14
RSVD-14 J15
RSVD-13 K10
RSVD-12 K11
RSVD-11 K12
RSVD-10 K13 H_RSVD-10 R798 NI 560R0402
RSVD-9 L10
RSVD-8 L12
RSVD-7 AC37
RSVD-6 AU10
RSVD-5 AU39 H_RSVD-5_TP9 TP13
RSVD-4 AU40 H_RSVD-4_TP9 TP18
RSVD-3 AU9
RSVD_TP-9 AV39 H_RSVD_TP9 TP11
RSVD_TP-8 AW38 H_RSVD_TP8 TP12
VSS-374 AY3
Project
Berlinetta V
Maranello V
Barchetta V
Latest modified date:
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CPU-CLK/MISC/XDP
Size Custom
Document Number HP SCH P/N: 793306-000(MSI MS-7957)
Rev X4
Date: Friday, June 05, 2015
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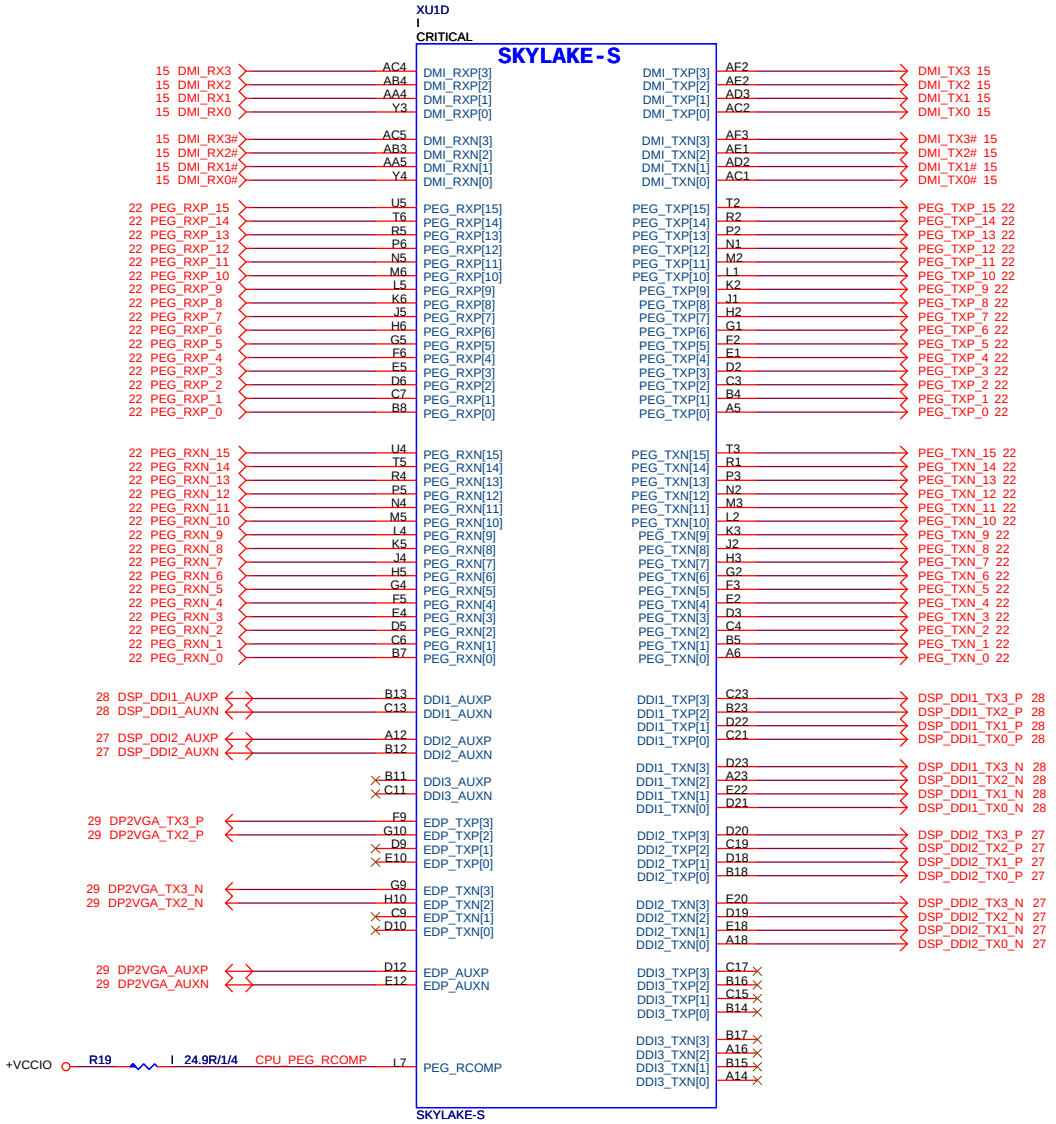

Project	
Berlinetta	V
Maranello	V
Barchetta	

Latest modified date:
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Size	Document Number	Rev
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XU1B
I
CRITICAL

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10,11 MEM_MA_DATA[63..0]

MEM_MA_DATA63	AK1	DDR0_DQ[63] / DDR1_DQ[47]
MEM_MA_DATA62	AH3	DDR0_DQ[62] / DDR1_DQ[46]
MEM_MA_DATA61	AK2	DDR0_DQ[61] / DDR1_DQ[45]
MEM_MA_DATA60	AH4	DDR0_DQ[60] / DDR1_DQ[44]
MEM_MA_DATA59	AH2	DDR0_DQ[59] / DDR1_DQ[43]
MEM_MA_DATA58	AK4	DDR0_DQ[58] / DDR1_DQ[42]
MEM_MA_DATA57	AH1	DDR0_DQ[57] / DDR1_DQ[41]
MEM_MA_DATA56	AK3	DDR0_DQ[56] / DDR1_DQ[40]
MEM_MA_DATA55	AM1	DDR0_DQ[55] / DDR1_DQ[39]
MEM_MA_DATA54	AP1	DDR0_DQ[54] / DDR1_DQ[38]
MEM_MA_DATA53	AM2	DDR0_DQ[53] / DDR1_DQ[37]
MEM_MA_DATA52	AP4	DDR0_DQ[52] / DDR1_DQ[36]
MEM_MA_DATA51	AM3	DDR0_DQ[51] / DDR1_DQ[35]
MEM_MA_DATA50	AP3	DDR0_DQ[50] / DDR1_DQ[34]
MEM_MA_DATA49	AM4	DDR0_DQ[49] / DDR1_DQ[33]
MEM_MA_DATA48	AP2	DDR0_DQ[48] / DDR1_DQ[32]
MEM_MA_DATA47	AT3	DDR0_DQ[47] / DDR1_DQ[15]
MEM_MA_DATA46	AT4	DDR0_DQ[46] / DDR1_DQ[14]
MEM_MA_DATA45	AW4	DDR0_DQ[45] / DDR1_DQ[13]
MEM_MA_DATA44	AV3	DDR0_DQ[44] / DDR1_DQ[12]
MEM_MA_DATA43	AT2	DDR0_DQ[43] / DDR1_DQ[11]
MEM_MA_DATA42	AT1	DDR0_DQ[42] / DDR1_DQ[10]
MEM_MA_DATA41	AV4	DDR0_DQ[41] / DDR1_DQ[9]
MEM_MA_DATA40	AY4	DDR0_DQ[40] / DDR1_DQ[8]
MEM_MA_DATA39	AY6	DDR0_DQ[39] / DDR1_DQ[7]
MEM_MA_DATA38	AW6	DDR0_DQ[38] / DDR1_DQ[6]
MEM_MA_DATA37	AV8	DDR0_DQ[37] / DDR1_DQ[5]
MEM_MA_DATA36	AU8	DDR0_DQ[36] / DDR1_DQ[4]
MEM_MA_DATA35	AU6	DDR0_DQ[35] / DDR1_DQ[3]
MEM_MA_DATA34	AV6	DDR0_DQ[34] / DDR1_DQ[2]
MEM_MA_DATA33	AW8	DDR0_DQ[33] / DDR1_DQ[1]
MEM_MA_DATA32	AY8	DDR0_DQ[32] / DDR1_DQ[0]
MEM_MA_DATA31	AU35	DDR0_DQ[31] / DDR0_DQ[47]
MEM_MA_DATA30	AT35	DDR0_DQ[30] / DDR0_DQ[46]
MEM_MA_DATA29	AV37	DDR0_DQ[29] / DDR0_DQ[45]
MEM_MA_DATA28	AU37	DDR0_DQ[28] / DDR0_DQ[44]
MEM_MA_DATA27	AW35	DDR0_DQ[27] / DDR0_DQ[43]
MEM_MA_DATA26	AV35	DDR0_DQ[26] / DDR0_DQ[42]
MEM_MA_DATA25	AU38	DDR0_DQ[25] / DDR0_DQ[41]
MEM_MA_DATA24	AW37	DDR0_DQ[24] / DDR0_DQ[40]
MEM_MA_DATA23	AR40	DDR0_DQ[23] / DDR0_DQ[39]
MEM_MA_DATA22	AR39	DDR0_DQ[22] / DDR0_DQ[38]
MEM_MA_DATA21	AN37	DDR0_DQ[21] / DDR0_DQ[37]
MEM_MA_DATA20	AN39	DDR0_DQ[20] / DDR0_DQ[36]
MEM_MA_DATA19	AR37	DDR0_DQ[19] / DDR0_DQ[35]
MEM_MA_DATA18	AR38	DDR0_DQ[18] / DDR0_DQ[34]
MEM_MA_DATA17	AN40	DDR0_DQ[17] / DDR0_DQ[33]
MEM_MA_DATA16	AN38	DDR0_DQ[16] / DDR0_DQ[32]
MEM_MA_DATA15	AL40	DDR0_DQ[15]
MEM_MA_DATA14	AL39	DDR0_DQ[14]
MEM_MA_DATA13	AJ39	DDR0_DQ[13]
MEM_MA_DATA12	AJ40	DDR0_DQ[12]
MEM_MA_DATA11	AL37	DDR0_DQ[11]
MEM_MA_DATA10	AL38	DDR0_DQ[10]
MEM_MA_DATA9	AJ37	DDR0_DQ[9]
MEM_MA_DATA8	AJ38	DDR0_DQ[8]
MEM_MA_DATA7	AG40	DDR0_DQ[7]
MEM_MA_DATA6	AG39	DDR0_DQ[6]
MEM_MA_DATA5	AE40	DDR0_DQ[5]
MEM_MA_DATA4	AE39	DDR0_DQ[4]
MEM_MA_DATA3	AG37	DDR0_DQ[3]
MEM_MA_DATA2	AG38	DDR0_DQ[2]
MEM_MA_DATA1	AE37	DDR0_DQ[1]
MEM_MA_DATA0	AE38	DDR0_DQ[0]

	AY31	DDR0_ECC[7]
	AW31	DDR0_ECC[6]
	AV33	DDR0_ECC[5]
	AU31	DDR0_ECC[4]
	AV31	DDR0_ECC[3]
	AW33	DDR0_ECC[2]
	AT33	DDR0_ECC[1]
	AU33	DDR0_ECC[0]

11 MEM_MA_CLK_H3	MEM_MA_CLK_H3	AT16
11 MEM_MA_CLK_H2	MEM_MA_CLK_H2	AW16
10 MEM_MA_CLK_H1	MEM_MA_CLK_H1	AW17
10 MEM_MA_CLK_H0	MEM_MA_CLK_H0	AW18
11 MEM_MA_CLK_L3	MEM_MA_CLK_L3	AU16
11 MEM_MA_CLK_L2	MEM_MA_CLK_L2	AV16
10 MEM_MA_CLK_L1	MEM_MA_CLK_L1	AY17
10 MEM_MA_CLK_L0	MEM_MA_CLK_L0	AV18

DDR0_CKP[3]
DDR0_CKP[2]
DDR0_CKP[1]
DDR0_CKP[0]
DDR0_CKN[3]
DDR0_CKN[2]
DDR0_CKN[1]
DDR0_CKN[0]

10,11 MEM_MA_BANK2	MEM_MA_BANK2	AW23
10,11 MEM_MA_BANK1	MEM_MA_BANK1	AV15
10,11 MEM_MA_BANK0	MEM_MA_BANK0	AY13

DDR0_BA[2] / DDR0_CAA[5]/ DDR0_BG[0]
DDR0_BA[1] /DDR0_CAB[6]/DDR0_BA[1]
DDR0_BA[0] /DDR0_CAB[4]/DDR0_BA[0]

SKYLAKE-S

Note: Pin function corresponing to
different DDR technologies
Left to right: DDR3L/LPDDR3/DDR4

DDR0_DQSP[8]	AV32	
DDR0_DQSP[7] / DDR1_DQSP[5]	AJ2	MEM_MA_DQS_H7
DDR0_DQSP[6] / DDR1_DQSP[4]	AN2	MEM_MA_DQS_H6
DDR0_DQSP[5] / DDR1_DQSP[1]	AU2	MEM_MA_DQS_H5
DDR0_DQSP[4] / DDR1_DQSP[0]	AV7	MEM_MA_DQS_H4
DDR0_DQSP[3] / DDR0_DQSP[5]	AV36	MEM_MA_DQS_H3
DDR0_DQSP[2] / DDR0_DQSP[4]	AP38	MEM_MA_DQS_H2
DDR0_DQSP[1]	AK38	MEM_MA_DQS_H1
DDR0_DQSP[0]	AF38	MEM_MA_DQS_H0

MEM_MA_DQS_H7 10,11
MEM_MA_DQS_H6 10,11
MEM_MA_DQS_H5 10,11
MEM_MA_DQS_H4 10,11
MEM_MA_DQS_H3 10,11
MEM_MA_DQS_H2 10,11
MEM_MA_DQS_H1 10,11
MEM_MA_DQS_H0 10,11

DDR0_DQSN[8]	AU32	
DDR0_DQSN[7] / DDR1_DQSN[5]	AJ3	MEM_MA_DQS_L7
DDR0_DQSN[6] / DDR1_DQSN[4]	AN3	MEM_MA_DQS_L6
DDR0_DQSN[5] / DDR1_DQSN[1]	AU3	MEM_MA_DQS_L5
DDR0_DQSN[4] / DDR1_DQSN[0]	AW7	MEM_MA_DQS_L4
DDR0_DQSN[3] / DDR0_DQSN[5]	AU36	MEM_MA_DQS_L3
DDR0_DQSN[2] / DDR0_DQSN[4]	AP39	MEM_MA_DQS_L2
DDR0_DQSN[1]	AK39	MEM_MA_DQS_L1
DDR0_DQSN[0]	AF39	MEM_MA_DQS_L0

MEM_MA_DQS_L7 10,11
MEM_MA_DQS_L6 10,11
MEM_MA_DQS_L5 10,11
MEM_MA_DQS_L4 10,11
MEM_MA_DQS_L3 10,11
MEM_MA_DQS_L2 10,11
MEM_MA_DQS_L1 10,11
MEM_MA_DQS_L0 10,11

Note: Pin function corresponing to
different DDR technologies
Left to right: DDR3L/LPDDR3/DDR4

DDR0_MA[15] /DDR0_CAA[8]/DDR0_ACT#	AU24	MEM_MA_ADD15
DDR0_MA[14] /DDR0_CAA[9]/ DDR0_BG[1]	AV23	MEM_MA_ADD14
DDR0_MA[13] /DDR0_CAB[0] /DDR0_MA[13]	AV12	MEM_MA_ADD13
DDR0_MA[12] /DDR0_CAA[6] /DDR0_MA[12]	AV22	MEM_MA_ADD12
DDR0_MA[11] /DDR0_CAA[7] /DDR0_MA[11]	AU22	MEM_MA_ADD11
DDR0_MA[10] /DDR0_CAB[7]/DDR0_MA[10]	AY14	MEM_MA_ADD10
DDR0_MA[9] /DDR0_CAA[1] /DDR0_MA[9]	AT22	MEM_MA_ADD9
DDR0_MA[8] / DDR0_CAA[3] /DDR0_MA[8]	AT20	MEM_MA_ADD8
DDR0_MA[7] /DDR0_CAA[4] /DDR0_MA[7]	AU21	MEM_MA_ADD7
DDR0_MA[6] /DDR0_CAA[2] /DDR0_MA[6]	AV20	MEM_MA_ADD6
DDR0_MA[5] /DDR0_CAA[0] /DDR0_MA[5]	AU20	MEM_MA_ADD5
DDR0_MA[4]	AT19	MEM_MA_ADD4
DDR0_MA[3]	AV19	MEM_MA_ADD3
DDR0_MA[2] /DDR0_CAB[5]/DDR0_MA[2]	AU17	MEM_MA_ADD2
DDR0_MA[1] /DDR0_CAB[8]/DDR0_MA[1]	AU18	MEM_MA_ADD1
DDR0_MA[0] /DDR0_CAB[9]/DDR0_MA[0]	AW15	MEM_MA_ADD0

MEM_MA_ADD[15..0] 10,11

DDR0_CKE[3]	AV25	MEM_MA_CKE3
DDR0_CKE[2]	AV24	MEM_MA_CKE2
DDR0_CKE[1]	AW24	MEM_MA_CKE1
DDR0_CKE[0]	AY24	MEM_MA_CKE0

MEM_MA_CKE3 11
MEM_MA_CKE2 11
MEM_MA_CKE1 10
MEM_MA_CKE0 10

DDR0_ODT[3]	AY10	MEM_MA_ODT3
DDR0_ODT[2]	AU12	MEM_MA_ODT2
DDR0_ODT[1]	AU14	MEM_MA_ODT1
DDR0_ODT[0]	AW11	MEM_MA_ODT0

MEM_MA_ODT3 11
MEM_MA_ODT2 11
MEM_MA_ODT1 10
MEM_MA_ODT0 10

DDR0_CS_N[3]	AV10	MEM_MA_CS_L3
DDR0_CS_N[2]	AV13	MEM_MA_CS_L2
DDR0_CS_N[1]	AU11	MEM_MA_CS_L1
DDR0_CS_N[0]	AW12	MEM_MA_CS_L0

MEM_MA_CS_L3 11
MEM_MA_CS_L2 11
MEM_MA_CS_L1 10
MEM_MA_CS_L0 10

Note: Pin function corresponing to
different DDR technologies
Left to right: DDR3L/LPDDR3/DDR4

DDR0_ALERT_N	AT23	
DDR0_CAS#/DDR0_CAB[1]/DDR0_MA[15]	AY11	MEM_MA_CAS_L
DDR0_RAS# /DDR0_CAB[3]/DDR0_MA[16]	AW13	MEM_MA_RAS_L
DDR0_WE#/DDR0_CAB[2]/DDR0_MA[14]	AV14	MEM_MA_WE_L
DDR0_PAR	AY15	

MEM_MA_CAS_L 10,11
MEM_MA_RAS_L 10,11
MEM_MA_WE_L 10,11

DDR1_VREF_DQ	AC39	MEM_CPU_VREF_DQ1 12
DDR0_VREF_DQ	AC40	MEM_CPU_VREF_DQ0 10
DDR_VREF_CA	AB40	MEM_CPU_VREF_CA 10
DDR_VTT_CNTL	AC36	DDR_VTT_CNTL 45

Project	
Berlinetta	V
Maranello	V
Barchetta	V

Latest modified date:
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Title: CPU-Memory-Channel A

Size: Custom | Document Number: HP SCH P/N: 793306-000(MSI MS-7957) | Rev: X4

Date: Friday, June 05, 2015 | Sheet 6 of 65

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12,13 MEM_MB_DATA[63..0]

MEM_MB_DATA63	AF6	DDR1_DQ[63]
MEM_MB_DATA62	AE7	DDR1_DQ[62]
MEM_MB_DATA61	AH6	DDR1_DQ[61]
MEM_MB_DATA60	AH7	DDR1_DQ[60]
MEM_MB_DATA59	AE7	DDR1_DQ[59]
MEM_MB_DATA58	AE6	DDR1_DQ[58]
MEM_MB_DATA57	AJ7	DDR1_DQ[57]
MEM_MB_DATA56	AJ6	DDR1_DQ[56]
MEM_MB_DATA55	AL6	DDR1_DQ[55]
MEM_MB_DATA54	AM6	DDR1_DQ[54]
MEM_MB_DATA53	AL9	DDR1_DQ[53]
MEM_MB_DATA52	AM9	DDR1_DQ[52]
MEM_MB_DATA51	AL7	DDR1_DQ[51]
MEM_MB_DATA50	AM7	DDR1_DQ[50]
MEM_MB_DATA49	AL10	DDR1_DQ[49]
MEM_MB_DATA48	AM10	DDR1_DQ[48]
MEM_MB_DATA47	AP6	DDR1_DQ[47] / DDR1_DQ[31]
MEM_MB_DATA46	AR6	DDR1_DQ[46] / DDR1_DQ[30]
MEM_MB_DATA45	AP9	DDR1_DQ[45] / DDR1_DQ[29]
MEM_MB_DATA44	AR9	DDR1_DQ[44] / DDR1_DQ[28]
MEM_MB_DATA43	AP7	DDR1_DQ[43] / DDR1_DQ[27]
MEM_MB_DATA42	AR7	DDR1_DQ[42] / DDR1_DQ[26]
MEM_MB_DATA41	AR10	DDR1_DQ[41] / DDR1_DQ[25]
MEM_MB_DATA40	AP10	DDR1_DQ[40] / DDR1_DQ[24]
MEM_MB_DATA39	AL12	DDR1_DQ[39] / DDR1_DQ[23]
MEM_MB_DATA38	AM12	DDR1_DQ[38] / DDR1_DQ[22]
MEM_MB_DATA37	AP13	DDR1_DQ[37] / DDR1_DQ[21]
MEM_MB_DATA36	AR13	DDR1_DQ[36] / DDR1_DQ[20]
MEM_MB_DATA35	AL13	DDR1_DQ[35] / DDR1_DQ[19]
MEM_MB_DATA34	AM13	DDR1_DQ[34] / DDR1_DQ[18]
MEM_MB_DATA33	AP12	DDR1_DQ[33] / DDR1_DQ[17]
MEM_MB_DATA32	AR12	DDR1_DQ[32] / DDR1_DQ[16]
MEM_MB_DATA31	AP28	DDR1_DQ[31] / DDR0_DQ[63]
MEM_MB_DATA30	AR28	DDR1_DQ[30] / DDR0_DQ[62]
MEM_MB_DATA29	AL28	DDR1_DQ[29] / DDR0_DQ[61]
MEM_MB_DATA28	AM28	DDR1_DQ[28] / DDR0_DQ[60]
MEM_MB_DATA27	AR29	DDR1_DQ[27] / DDR0_DQ[59]
MEM_MB_DATA26	AP29	DDR1_DQ[26] / DDR0_DQ[58]
MEM_MB_DATA25	AM29	DDR1_DQ[25] / DDR0_DQ[57]
MEM_MB_DATA24	AL29	DDR1_DQ[24] / DDR0_DQ[56]
MEM_MB_DATA23	AP31	DDR1_DQ[23] / DDR0_DQ[55]
MEM_MB_DATA22	AN31	DDR1_DQ[22] / DDR0_DQ[54]
MEM_MB_DATA21	AP34	DDR1_DQ[21] / DDR0_DQ[53]
MEM_MB_DATA20	AN34	DDR1_DQ[20] / DDR0_DQ[52]
MEM_MB_DATA19	AP32	DDR1_DQ[19] / DDR0_DQ[51]
MEM_MB_DATA18	AN32	DDR1_DQ[18] / DDR0_DQ[50]
MEM_MB_DATA17	AN35	DDR1_DQ[17] / DDR0_DQ[49]
MEM_MB_DATA16	AP35	DDR1_DQ[16] / DDR0_DQ[48]
MEM_MB_DATA15	AL31	DDR1_DQ[15] / DDR0_DQ[31]
MEM_MB_DATA14	AK31	DDR1_DQ[14] / DDR0_DQ[30]
MEM_MB_DATA13	AL34	DDR1_DQ[13] / DDR0_DQ[29]
MEM_MB_DATA12	AK34	DDR1_DQ[12] / DDR0_DQ[28]
MEM_MB_DATA11	AL32	DDR1_DQ[11] / DDR0_DQ[27]
MEM_MB_DATA10	AK32	DDR1_DQ[10] / DDR0_DQ[26]
MEM_MB_DATA9	AL35	DDR1_DQ[9] / DDR0_DQ[25]
MEM_MB_DATA8	AK35	DDR1_DQ[8] / DDR0_DQ[24]
MEM_MB_DATA7	AH34	DDR1_DQ[7] / DDR0_DQ[23]
MEM_MB_DATA6	AG34	DDR1_DQ[6] / DDR0_DQ[22]
MEM_MB_DATA5	AE34	DDR1_DQ[5] / DDR0_DQ[21]
MEM_MB_DATA4	AE35	DDR1_DQ[4] / DDR0_DQ[20]
MEM_MB_DATA3	AH35	DDR1_DQ[3] / DDR0_DQ[19]
MEM_MB_DATA2	AG35	DDR1_DQ[2] / DDR0_DQ[18]
MEM_MB_DATA1	AD35	DDR1_DQ[1] / DDR0_DQ[17]
MEM_MB_DATA0	AD34	DDR1_DQ[0] / DDR0_DQ[16]

	AL26	DDR1_ECC[7]
	AL25	DDR1_ECC[6]
	AP25	DDR1_ECC[5]
	AP26	DDR1_ECC[4]
	AM25	DDR1_ECC[3]
	AM26	DDR1_ECC[2]
	AR26	DDR1_ECC[1]
	AR25	DDR1_ECC[0]

13 MEM_MB_CLK_H3	AP19	DDR1_CKP[3]
13 MEM_MB_CLK_H2	AN20	DDR1_CKP[2]
12 MEM_MB_CLK_H1	AP22	DDR1_CKP[1]
12 MEM_MB_CLK_H0	AM20	DDR1_CKP[0]
13 MEM_MB_CLK_L3	AP20	DDR1_CKN[3]
13 MEM_MB_CLK_L2	AN21	DDR1_CKN[2]
12 MEM_MB_CLK_L1	AP21	DDR1_CKN[1]
12 MEM_MB_CLK_L0	AM21	DDR1_CKN[0]

12,13 MEM_MB_BANK2	AW28	DDR1_BA[2] / DDR1_CAA[5]/ DDR1_BG[0]
12,13 MEM_MB_BANK1	AM18	DDR1_BA[1] /DDR1_CAB[6]/DDR1_BA[1]
12,13 MEM_MB_BANK0	AL18	DDR1_BA[0] /DDR1_CAB[4]/DDR1_BA[0]

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DDR1_DQSP[8]	AN25	
DDR1_DQSP[7]	AG7	MEM_MB_DQS_H7
DDR1_DQSP[6]	AL8	MEM_MB_DQS_H6
DDR1_DQSP[5] / DDR1_DQSP[3]	AP8	MEM_MB_DQS_H5
DDR1_DQSP[4] / DDR1_DQSP[2]	AN12	MEM_MB_DQS_H4
DDR1_DQSP[3] / DDR0_DQSP[7]	AN28	MEM_MB_DQS_H3
DDR1_DQSP[2] / DDR0_DQSP[6]	AP33	MEM_MB_DQS_H2
DDR1_DQSP[1] / DDR0_DQSP[3]	AL33	MEM_MB_DQS_H1
DDR1_DQSP[0] / DDR0_DQSP[2]	AF35	MEM_MB_DQS_H0

	AN26	
DDR1_DQSN[8]	AG6	MEM_MB_DQS_L7
DDR1_DQSN[7]	AM8	MEM_MB_DQS_L6
DDR1_DQSN[6]	AR8	MEM_MB_DQS_L5
DDR1_DQSN[5] / DDR1_DQSN[3]	AN13	MEM_MB_DQS_L4
DDR1_DQSN[4] / DDR1_DQSN[2]	AN29	MEM_MB_DQS_L3
DDR1_DQSN[3] / DDR0_DQSN[7]	AN33	MEM_MB_DQS_L2
DDR1_DQSN[2] / DDR0_DQSN[6]	AK33	MEM_MB_DQS_L1
DDR1_DQSN[1] / DDR0_DQSN[3]	AF34	MEM_MB_DQS_L0

MEM_MB_DQS_H7 12,13
MEM_MB_DQS_H6 12,13
MEM_MB_DQS_H5 12,13
MEM_MB_DQS_H4 12,13
MEM_MB_DQS_H3 12,13
MEM_MB_DQS_H2 12,13
MEM_MB_DQS_H1 12,13
MEM_MB_DQS_H0 12,13

MEM_MB_DQS_L7 12,13
MEM_MB_DQS_L6 12,13
MEM_MB_DQS_L5 12,13
MEM_MB_DQS_L4 12,13
MEM_MB_DQS_L3 12,13
MEM_MB_DQS_L2 12,13
MEM_MB_DQS_L1 12,13
MEM_MB_DQS_L0 12,13

Note: Pin function corresponing to different DDR technologies
Left to right: DDR3L/LPDDR3/DDR4

DDR1_MA[15] /DDR1_CAA[8]/DDR1_ACT#	AU28	MEM_MB_ADD15
DDR1_MA[14] /DDR1_CAA[9]/ DDR1_BG[1]	AY28	MEM_MB_ADD14
DDR1_MA[13] /DDR1_CAB[0] /DDR1_MA[13]	AR15	MEM_MB_ADD13
DDR1_MA[12] /DDR1_CAA[6] /DDR1_MA[12]	AV27	MEM_MB_ADD12
DDR1_MA[11] /DDR1_CAA[7] /DDR1_MA[11]	AU27	MEM_MB_ADD11
DDR1_MA[10] /DDR1_CAB[7]/DDR1_MA[10]	AP18	MEM_MB_ADD10
DDR1_MA[9] /DDR1_CAA[1] /DDR1_MA[9]	AW27	MEM_MB_ADD9
DDR1_MA[8] / DDR1_CAA[3] /DDR1_MA[8]	AU26	MEM_MB_ADD8
DDR1_MA[7] /DDR1_CAA[4] /DDR1_MA[7]	AY26	MEM_MB_ADD7
DDR1_MA[6] /DDR1_CAA[2] /DDR1_MA[6]	AW26	MEM_MB_ADD6
DDR1_MA[5] /DDR1_CAA[0] /DDR1_MA[5]	AL23	MEM_MB_ADD5
DDR1_MA[4]	AP23	MEM_MB_ADD4
DDR1_MA[3]	AM23	MEM_MB_ADD3
DDR1_MA[2] /DDR1_CAB[5]/DDR1_MA[2]	AM22	MEM_MB_ADD2
DDR1_MA[1] /DDR1_CAB[8]/DDR1_MA[1]	AL22	MEM_MB_ADD1
DDR1_MA[0] /DDR1_CAB[9]/DDR1_MA[0]	AL19	MEM_MB_ADD0

MEM_MB_ADD[15..0] 12,13

DDR1_CKE[3]	AU29	MEM_MB_CKE3
DDR1_CKE[2]	AW29	MEM_MB_CKE2
DDR1_CKE[1]	AV29	MEM_MB_CKE1
DDR1_CKE[0]	AY29	MEM_MB_CKE0

MEM_MB_CKE3 13
MEM_MB_CKE2 13
MEM_MB_CKE1 12
MEM_MB_CKE0 12

DDR1_ODT[3]	AL15	MEM_MB_ODT3
DDR1_ODT[2]	AP15	MEM_MB_ODT2
DDR1_ODT[1]	AL16	MEM_MB_ODT1
DDR1_ODT[0]	AM16	MEM_MB_ODT0

MEM_MB_ODT3 13
MEM_MB_ODT2 13
MEM_MB_ODT1 12
MEM_MB_ODT0 12

DDR1_CS_N[3]	AM15	MEM_MB_CS_L3
DDR1_CS_N[2]	AN17	MEM_MB_CS_L2
DDR1_CS_N[1]	AN15	MEM_MB_CS_L1
DDR1_CS_N[0]	AP17	MEM_MB_CS_L0

MEM_MB_CS_L3 13
MEM_MB_CS_L2 13
MEM_MB_CS_L1 12
MEM_MB_CS_L0 12

DDR1_ALERT_N	AY25	
DDR1_CAS#/DDR1_CAB[1]/DDR1_MA[15]	AP16	MEM_MB_CAS_L 12,13
DDR1_RAS# /DDR1_CAB[3]/DDR1_MA[16]	AN18	MEM_MB_RAS_L 12,13
DDR1_WE#/DDR1_CAB[2]/DDR1_MA[14]	AL17	MEM_MB_WE_L 12,13
DDR1_PAR	AL20	

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Note: Pin function corresponing to different DDR technologies
Left to right: DDR3L/LPDDR3/DDR4

Note: Pin function corresponing to different DDR technologies
Left to right: DDR3L/LPDDR3/DDR4

Project	
Berlinetta	V
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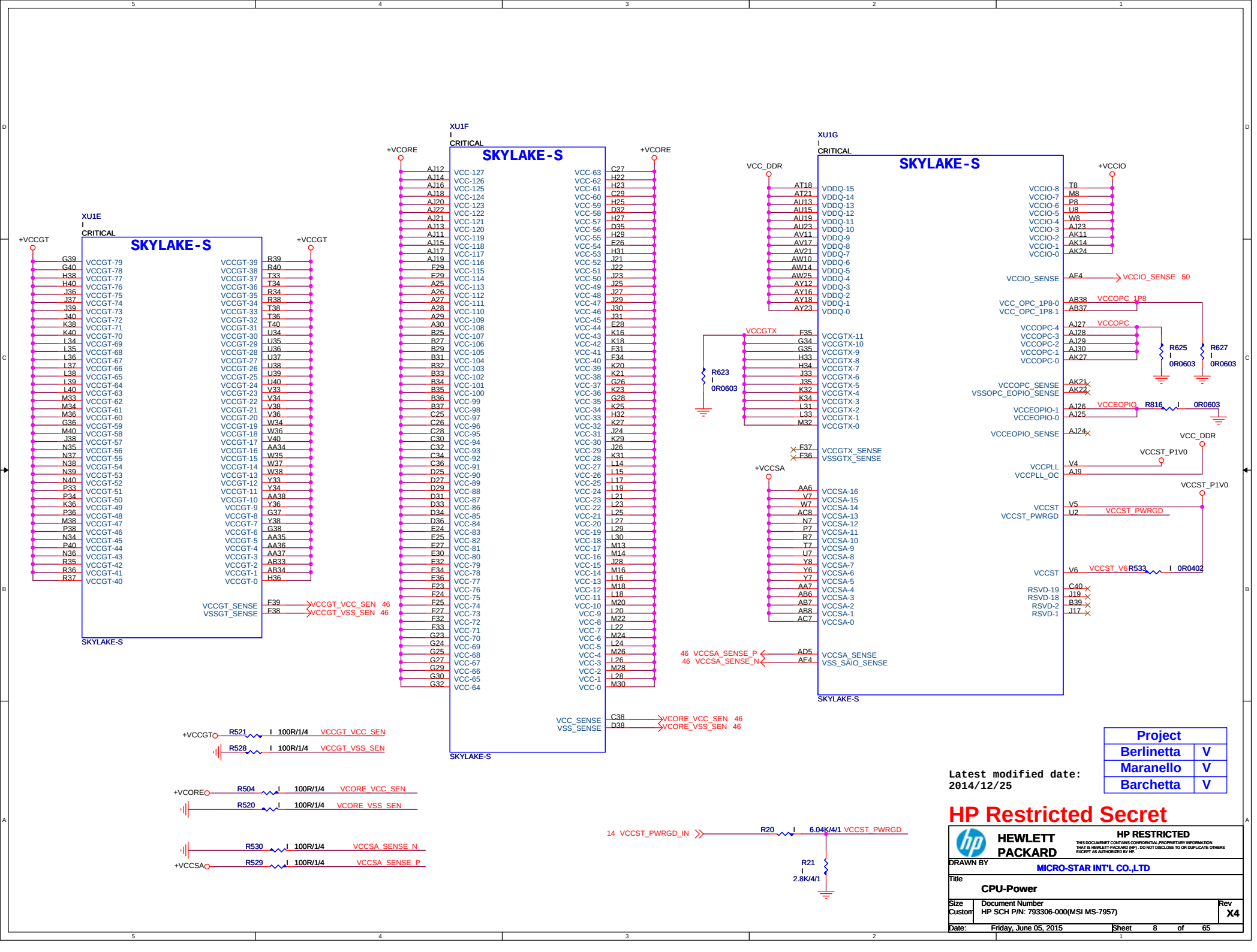
Size: Custom | Document Number: HP SCH P/N: 793306-000(MSI MS-7957) | Rev: X4

Date: Friday, June 05, 2015 | Sheet 7 of 65


XU1E
CRITICAL
SKYLAKE-S
SKYLAKE-S
+VCCGT
+VCCGT
VCCGT-79
VCCGT-78
VCCGT-77
VCCGT-76
VCCGT-75
VCCGT-74
VCCGT-73
VCCGT-72
VCCGT-71
VCCGT-70
VCCGT-69
VCCGT-68
VCCGT-67
VCCGT-66
VCCGT-65
VCCGT-64
VCCGT-63
VCCGT-62
VCCGT-61
VCCGT-60
VCCGT-59
VCCGT-58
VCCGT-57
VCCGT-56
VCCGT-55
VCCGT-54
VCCGT-53
VCCGT-52
VCCGT-51
VCCGT-50
VCCGT-49
VCCGT-48
VCCGT-47
VCCGT-46
VCCGT-45
VCCGT-44
VCCGT-43
VCCGT-42
VCCGT-41
VCCGT-40
VCCGT-39
VCCGT-38
VCCGT-37
VCCGT-36
VCCGT-35
VCCGT-34
VCCGT-33
VCCGT-32
VCCGT-31
VCCGT-30
VCCGT-29
VCCGT-28
VCCGT-27
VCCGT-26
VCCGT-25
VCCGT-24
VCCGT-23
VCCGT-22
VCCGT-21
VCCGT-20
VCCGT-19
VCCGT-18
VCCGT-17
VCCGT-16
VCCGT-15
VCCGT-14
VCCGT-13
VCCGT-12
VCCGT-11
VCCGT-10
VCCGT-9
VCCGT-8
VCCGT-7
VCCGT-6
VCCGT-5
VCCGT-4
VCCGT-3
VCCGT-2
VCCGT-1
VCCGT-0
VCCGT_SENSE
VSSGT_SENSE
VCCGT_VCC_SEN 46
VCCGT_VSS_SEN 46
XU1F
CRITICAL
SKYLAKE-S
SKYLAKE-S
+VCORE
+VCORE
VCC-127
VCC-126
VCC-125
VCC-124
VCC-123
VCC-122
VCC-121
VCC-120
VCC-119
VCC-118
VCC-117
VCC-116
VCC-115
VCC-114
VCC-113
VCC-112
VCC-111
VCC-110
VCC-109
VCC-108
VCC-107
VCC-106
VCC-105
VCC-104
VCC-103
VCC-102
VCC-101
VCC-100
VCC-99
VCC-98
VCC-97
VCC-96
VCC-95
VCC-94
VCC-93
VCC-92
VCC-91
VCC-90
VCC-89
VCC-88
VCC-87
VCC-86
VCC-85
VCC-84
VCC-83
VCC-82
VCC-81
VCC-80
VCC-79
VCC-78
VCC-77
VCC-76
VCC-75
VCC-74
VCC-73
VCC-72
VCC-71
VCC-70
VCC-69
VCC-68
VCC-67
VCC-66
VCC-65
VCC-64
VCC-63
VCC-62
VCC-61
VCC-60
VCC-59
VCC-58
VCC-57
VCC-56
VCC-55
VCC-54
VCC-53
VCC-52
VCC-51
VCC-50
VCC-49
VCC-48
VCC-47
VCC-46
VCC-45
VCC-44
VCC-43
VCC-42
VCC-41
VCC-40
VCC-39
VCC-38
VCC-37
VCC-36
VCC-35
VCC-34
VCC-33
VCC-32
VCC-31
VCC-30
VCC-29
VCC-28
VCC-27
VCC-26
VCC-25
VCC-24
VCC-23
VCC-22
VCC-21
VCC-20
VCC-19
VCC-18
VCC-17
VCC-16
VCC-15
VCC-14
VCC-13
VCC-12
VCC-11
VCC-10
VCC-9
VCC-8
VCC-7
VCC-6
VCC-5
VCC-4
VCC-3
VCC-2
VCC-1
VCC-0
VCC_SENSE
VSS_SENSE
VCORE_VCC_SEN 46
VCORE_VSS_SEN 46
XU1G
CRITICAL
SKYLAKE-S
SKYLAKE-S
VCC_DDR
VDDQ-15
VDDQ-14
VDDQ-13
VDDQ-12
VDDQ-11
VDDQ-10
VDDQ-9
VDDQ-8
VDDQ-7
VDDQ-6
VDDQ-5
VDDQ-4
VDDQ-3
VDDQ-2
VDDQ-1
VDDQ-0
VCCGTX
VCCGTX-11
VCCGTX-10
VCCGTX-9
VCCGTX-8
VCCGTX-7
VCCGTX-6
VCCGTX-5
VCCGTX-4
VCCGTX-3
VCCGTX-2
VCCGTX-1
VCCGTX-0
R623
0R0603
VCCGTX_SENSE
VSSGTX_SENSE
+VCCSA
VCCSA-16
VCCSA-15
VCCSA-14
VCCSA-13
VCCSA-12
VCCSA-11
VCCSA-10
VCCSA-9
VCCSA-8
VCCSA-7
VCCSA-6
VCCSA-5
VCCSA-4
VCCSA-3
VCCSA-2
VCCSA-1
VCCSA-0
46 VCCSA_SENSE_P
46 VCCSA_SENSE_N
VCCSA_SENSE
VSS_SAIO_SENSE
+VCCIO
VCCIO-8
VCCIO-7
VCCIO-6
VCCIO-5
VCCIO-4
VCCIO-3
VCCIO-2
VCCIO-1
VCCIO-0
VCCIO_SENSE
VCCIO_SENSE 50
VCC_OPC_1P8-0
VCC_OPC_1P8-1
VCCOPC_1P8
VCCOPC-4
VCCOPC-3
VCCOPC-2
VCCOPC-1
VCCOPC-0
VCCOPC
R625
0R0603
R627
0R0603
VCCOPC_SENSE
VSSOPC_EOPIO_SENSE
VCCEOPIO-1
VCCEOPIO-0
VCCEOPIO
R816
0R0603
VCCEOPIO_SENSE
VCC_DDR
VCCST_P1V0
VCCPLL
VCCPLL_OC
VCCST_P1V0
VCCST
VCCST_PWRGD
VCCST_PWRGD
VCCST
VCCST_V6
R533
0R0402
RSVD-19
RSVD-18
RSVD-2
RSVD-1
+VCCGT
R521
100R/1/4
VCCGT_VCC_SEN
R528
100R/1/4
VCCGT_VSS_SEN
+VCORE
R504
100R/1/4
VCORE_VCC_SEN
R520
100R/1/4
VCORE_VSS_SEN
R530
100R/1/4
VCCSA_SENSE_N
+VCCSA
R529
100R/1/4
VCCSA_SENSE_P
14 VCCST_PWRGD_IN
R20
6.04K/4/1
VCCST_PWRGD
R21
2.8K/4/1
Latest modified date:
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Project
Berlinetta V
Maranello V
Barchetta V
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CPU-Power
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Custom
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8
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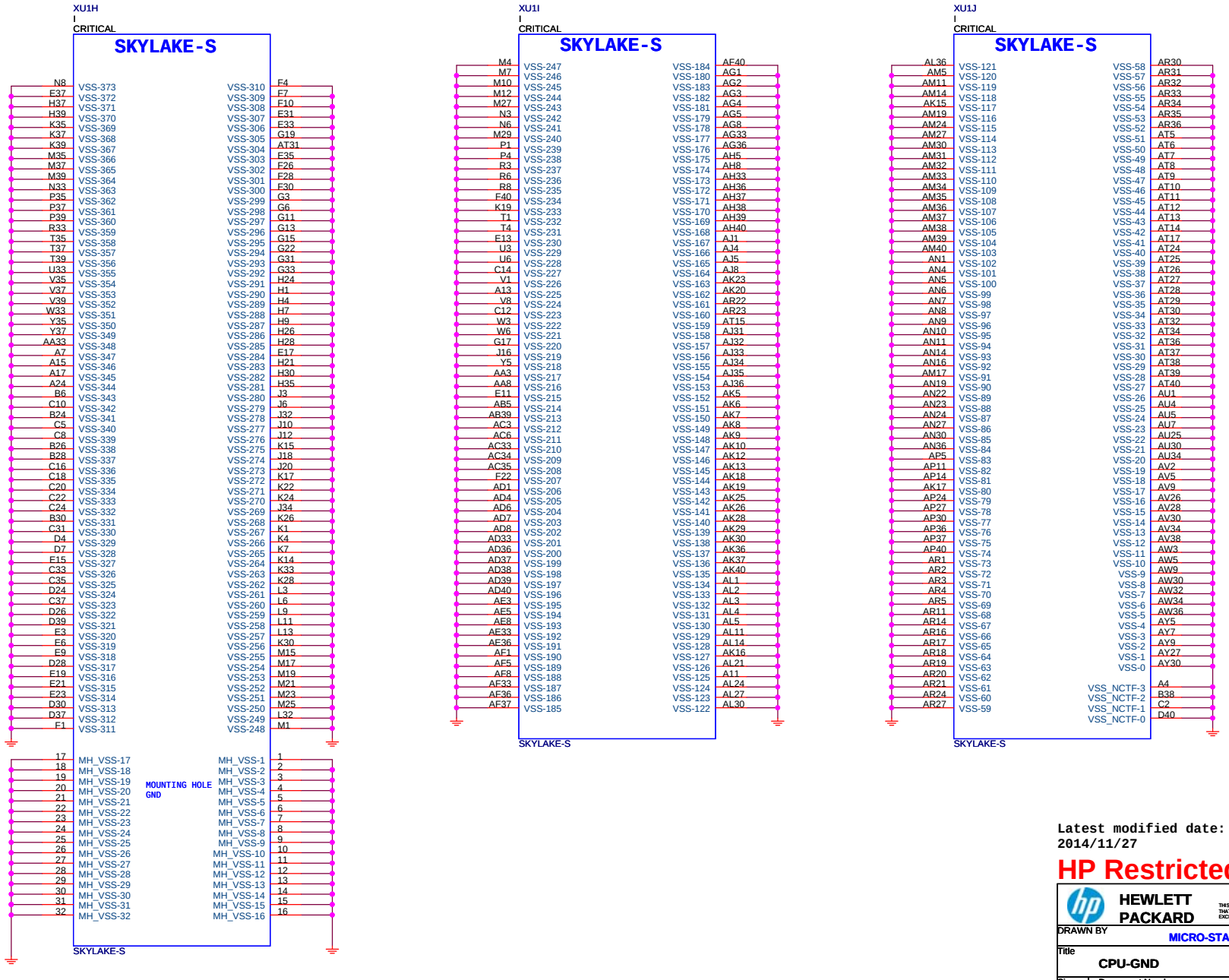
65



Project	
Berlinetta	V
Maranello	V
Barchetta	V

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Size: Custom	Document Number: HP SCH P/N: 793306-000(MSI MS-7957)
Rev	X4
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DDRIII DIMM_A1

WHITE COLOR
N13-2401611-F02

Palce Caps Between CHA And CHB

XMM4
I,NI,NI
CRITICAL

DDR3

DDRIII-240P_WHITE-RH-2
XMM4(CHANNEL-A)
ADDRESS = 1:1 [SA1:SA0]

Project	
Berlinetta	
Maranello	V
Barchetta	V

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Size: Custom
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Rev: X4
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Sheet 10 of 65

DDRIII DIMM_A2

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BLACK COLOR
N13-2401591-F02

XMM3
CRITICAL

DDR3

DDRIII-240P_BLACK-RH-6

XMM3(CHANNEL-A)
ADDRESS = 1:0 [SA1:SA0]

Project	
Berlinetta	
Maranello	V
Barchetta	V

Latest modified date:
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Date:	Friday, June 05, 2015
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DDRIII DIMM_B1

WHITE COLOR
N13-2401611-F02

DDR3

XMM2
I,NI,NI
CRITICAL

7,13 MEM_MB_DATA[63..0]

MEM_MB_ADD[15..0] 7,13

SMBCLK_DDR → SMBCLK_DDR 10,11,13
SMBDATA_DDR → SMBDATA_DDR 10,11,13

6 MEM_CPU_VREF_DQ1
VREF_DQ1_RC
R38 I 1K/4/1
R39 I 2R1%0402
R40 I 1K/4/1
R41 I 24.9R/1/4
C15 I 0.022u25X/4
C16 I 0.1u25X50402

C17 I 0.1u25X50402
C18 I 0.1u25X50402

DIMMB0_SA1 R926 NI 0R0402 +3.3V
R925 I 0R0402
DIMMB0_SA0 R924 I 0R0402 +3.3V
R923 NI 0R0402

DDRIII-240P_WHITE-RH-2

XMM2(CHANNEL-B)
ADDRESS = 0:1 [SA1:SA0]

Project	
Berlinetta	
Maranello	V
Barchetta	V

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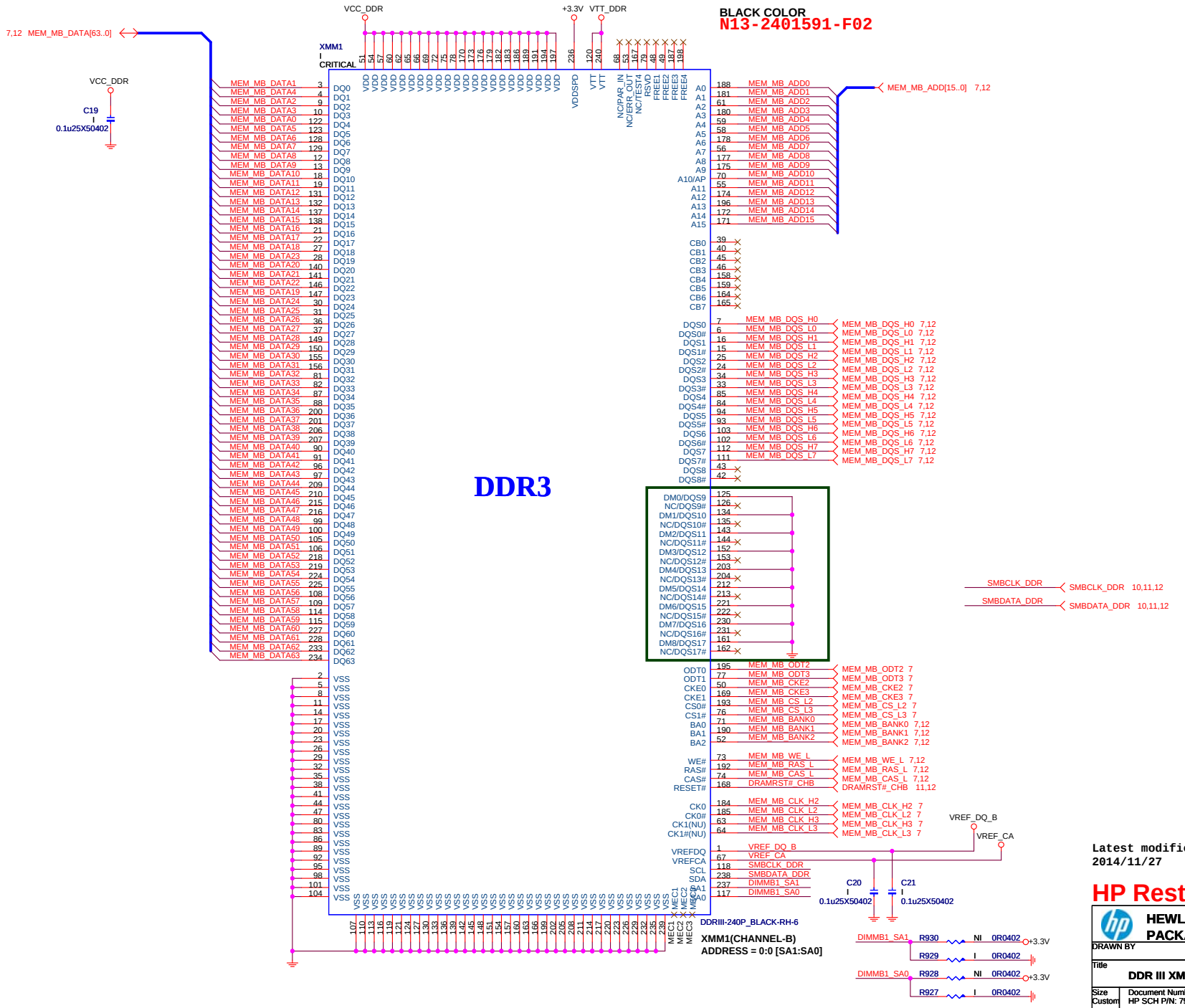
DDRIII DIMM_B2



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Maranello	V
Barchetta	V

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U4A
I,NI,NI
CRITICAL

SKYLAKE PCH-H

DPWROK Generation Schematic

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Maranello	V
Barchetta	V

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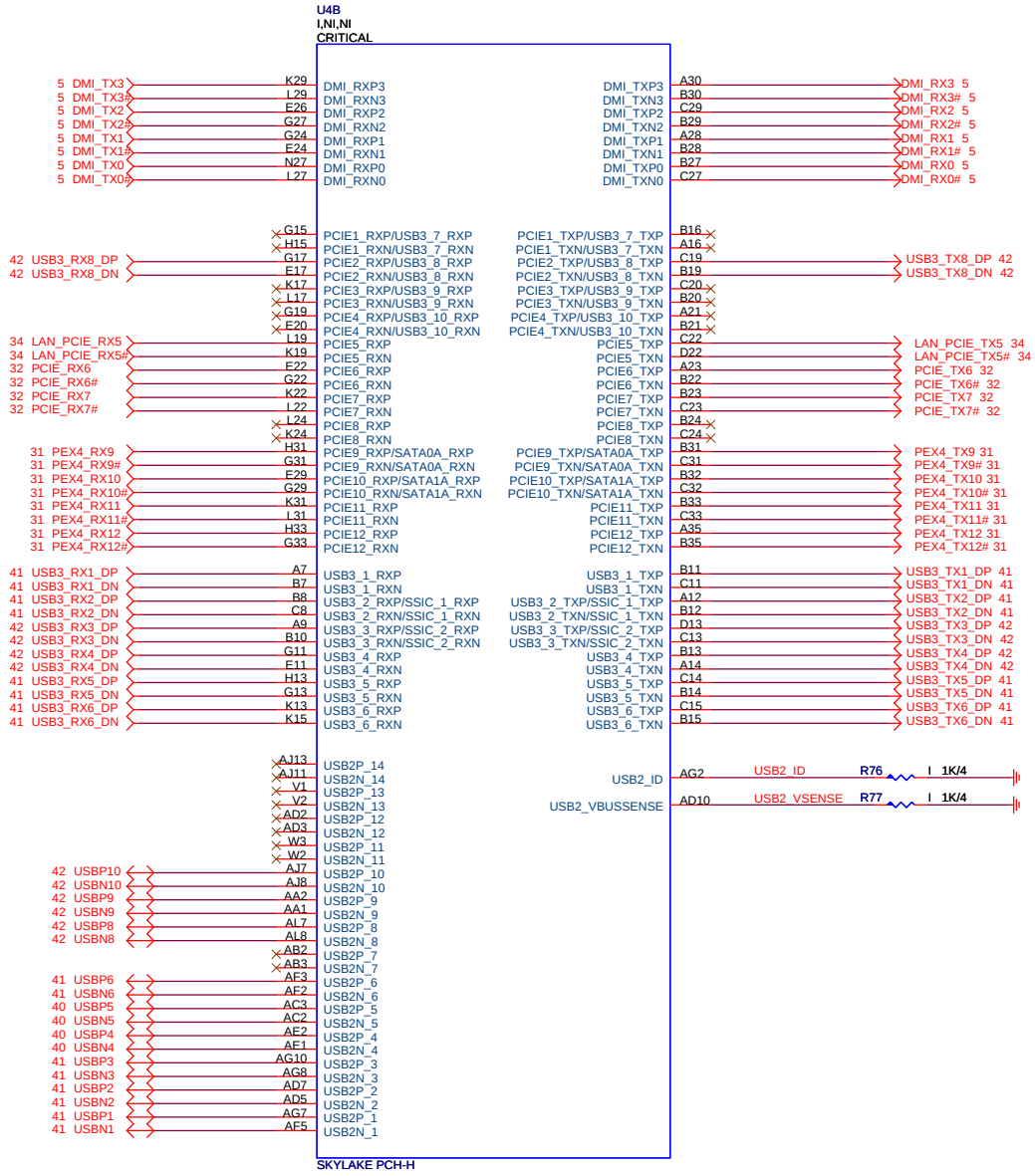

Project	
Berlinetta	V
Maranello	V
Barchetta	

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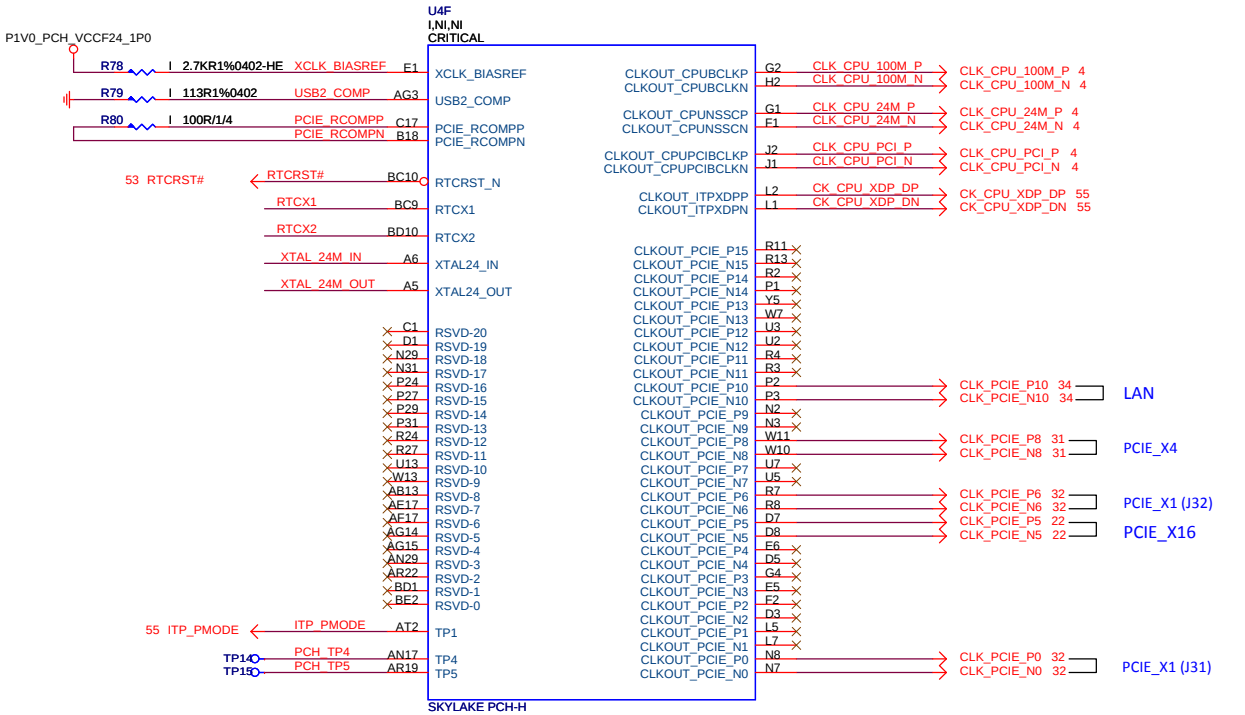
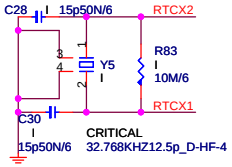
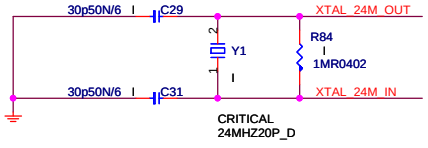
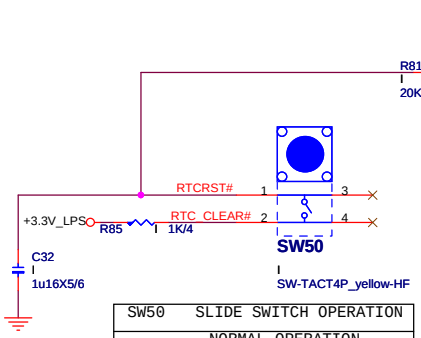


RTC Block

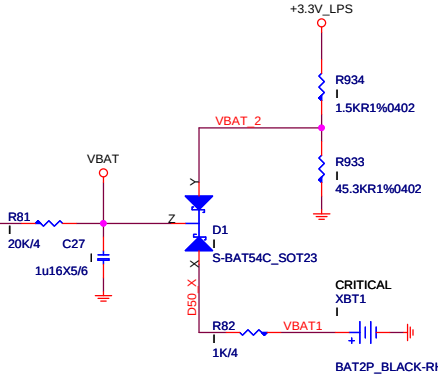
Close to PCH







SW50	SLIDE SWITCH OPERATION
	NORMAL OPERATION
	CLEAR CMOS



N91-01F0201-L06

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Maranello	V
Barchetta	

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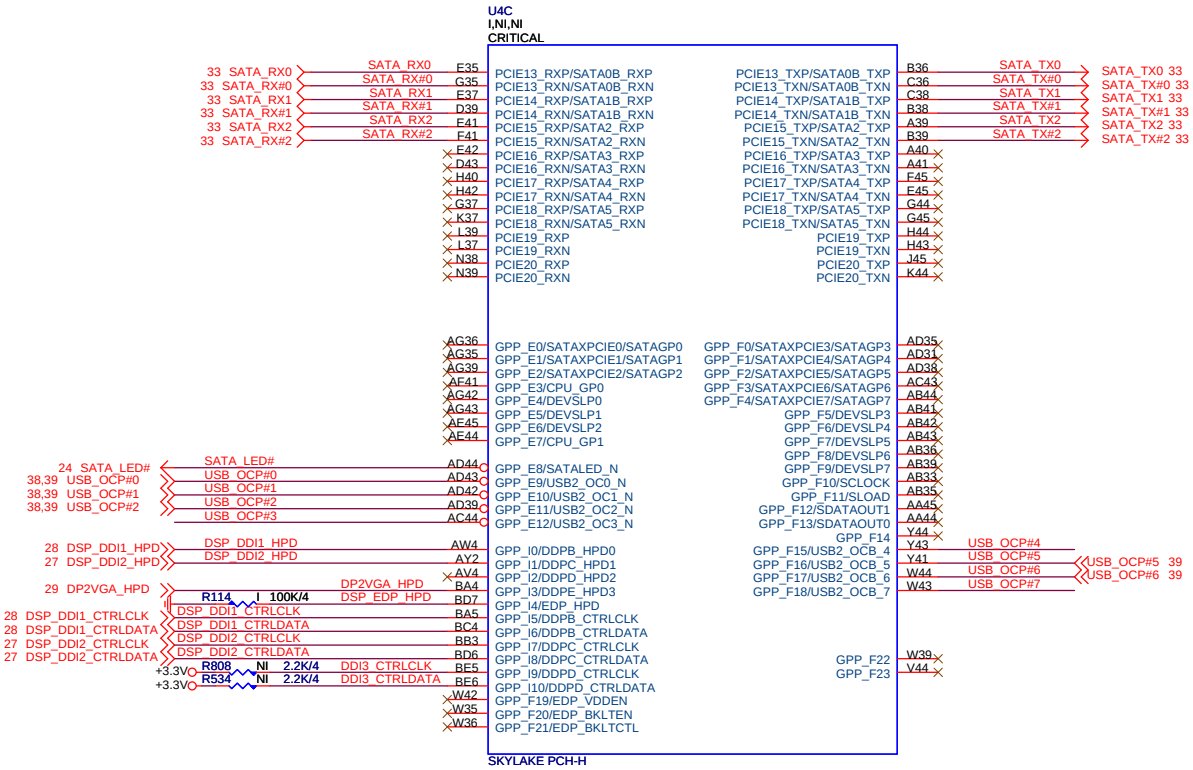

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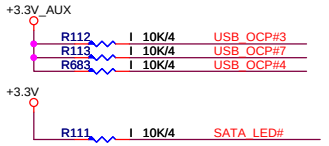

Project	
Berlinetta	V
Maranello	V
Barchetta	

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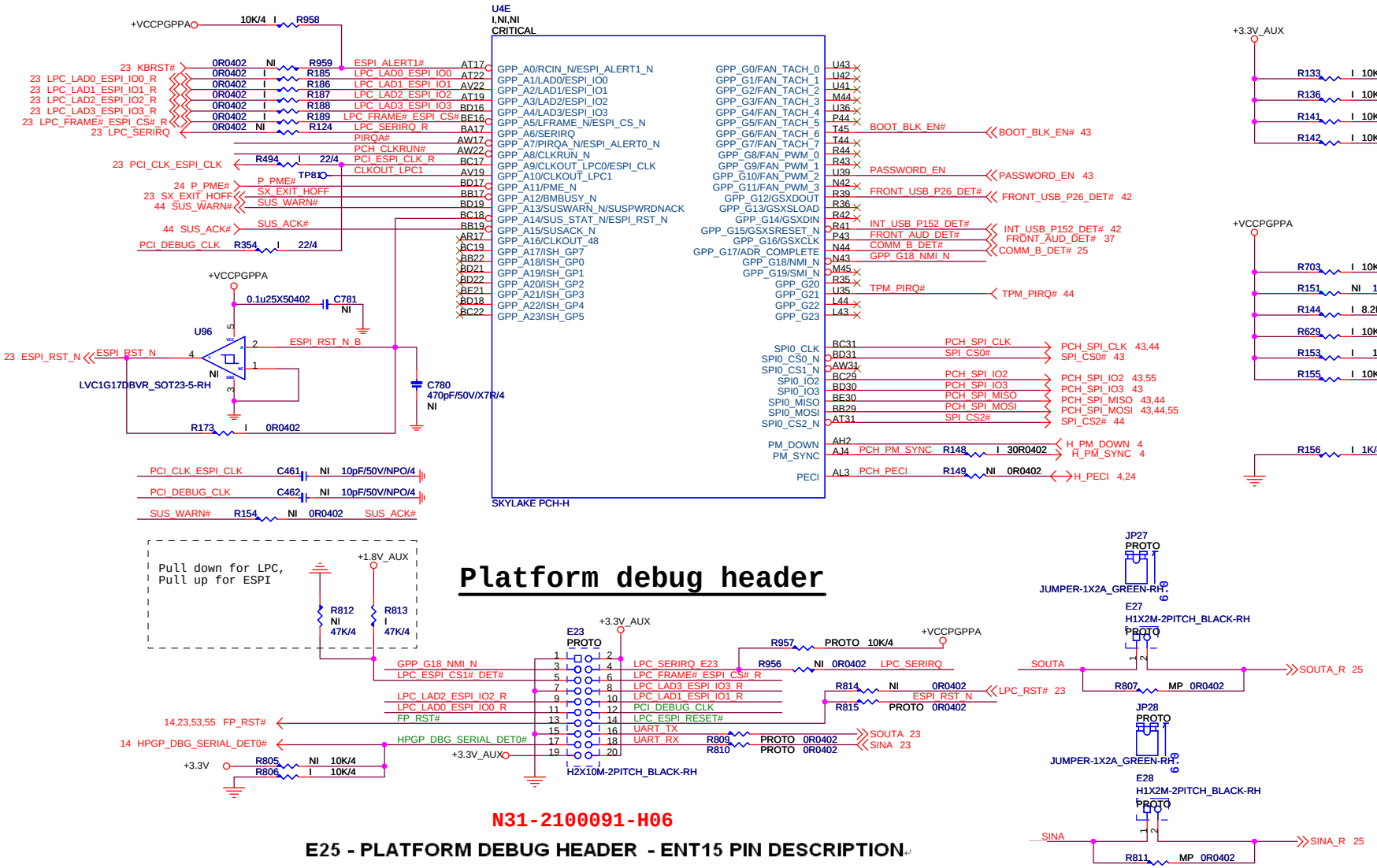

N31-2100091-H06

E25 - PLATFORM DEBUG HEADER - ENT15 PIN DESCRIPTION

PIN #	Voltage Level	Direction	SIGNAL NAME	SIGNAL NAME	Direction	Voltage	PIN #
1	GND	GND	GND	+3.3V_AUX	Power	Power	2
3	O/D	IN	NMI#	eSPI_ALERT#_LPCIRQ	BiDi	1.8V/3.3V	4
5	1.8V/3.3V	OUT	eSPI_CS1#/LPC_detect#	eSPI_CS0#/LPC_LFRAME#	OUT	1.8V/3.3V	6
7	GND	GND	GND	eSPI_DATA3/LPC_AD3	BiDi	1.8V/3.3V	8
9	1.8V/3.3V	BiDi	eSPI_DATA2/LPC_AD2	eSPI_DATA1/LPC_AD1	BiDi	1.8V/3.3V	10
11	1.8V/3.3V	BiDi	eSPI_DATA0/LPC_AD0	eSPI_CLK/LPC_LPC	OUT	1.8V/3.3V	12
13	O/D	IN	System RESET IN#	eSPI_RESET#/LPC_RESET#	OUT	1.8V/3.3V	14
15	GND	GND	GND	UART_TX	OUT	3.3V	16
17	3.3V	IN	HPGP_DBG_SERIAL_DET0#	UART_RX	IN	3.3V	18
19	Power	Power	+3.3V_AUX	+3.3V_AUX	Power	Power	20

Project	
Berlinetta	V
Maranello	V
Barchetta	V

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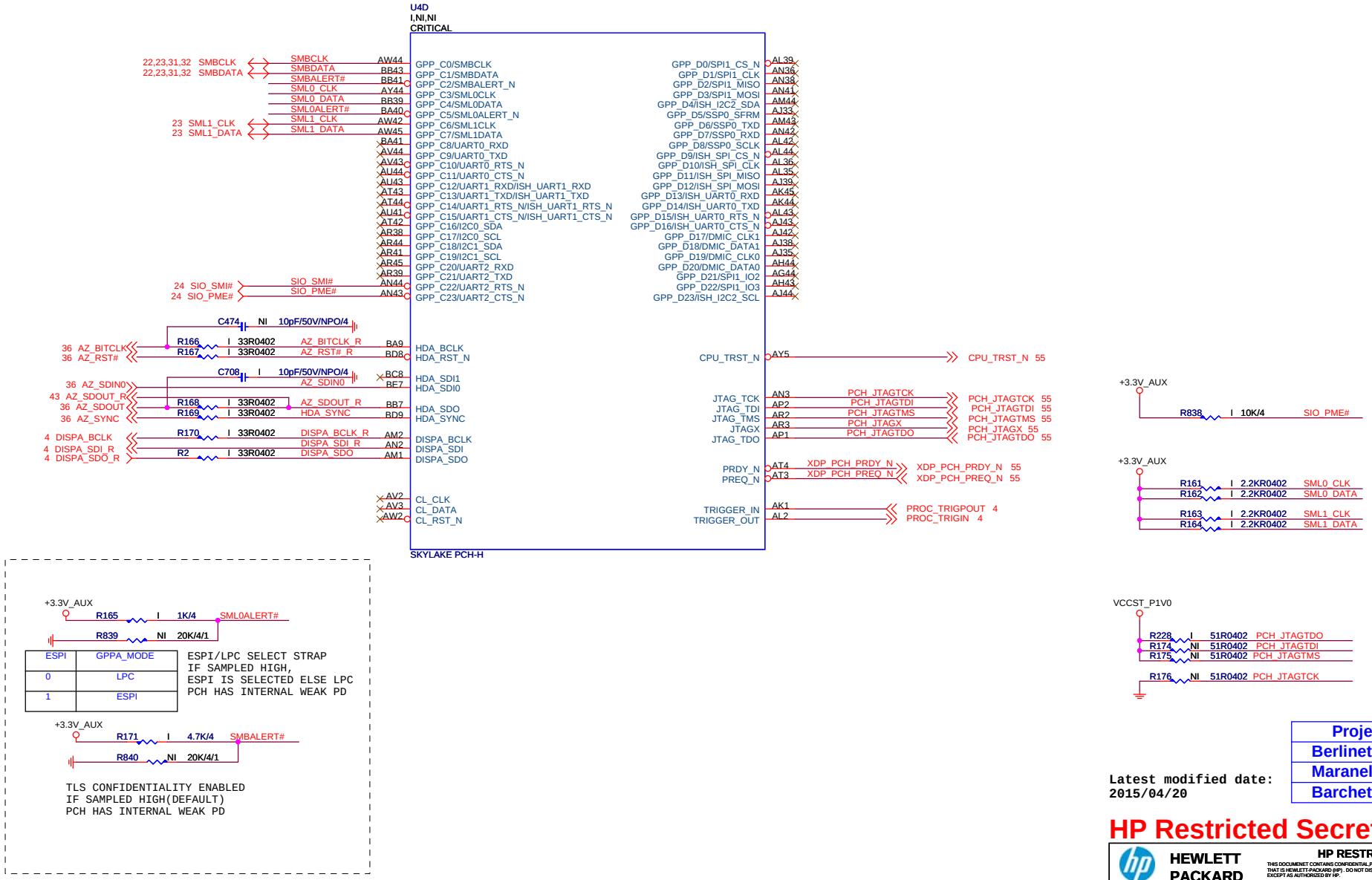

Project	
Berlinetta	V
Maranello	V
Barchetta	V

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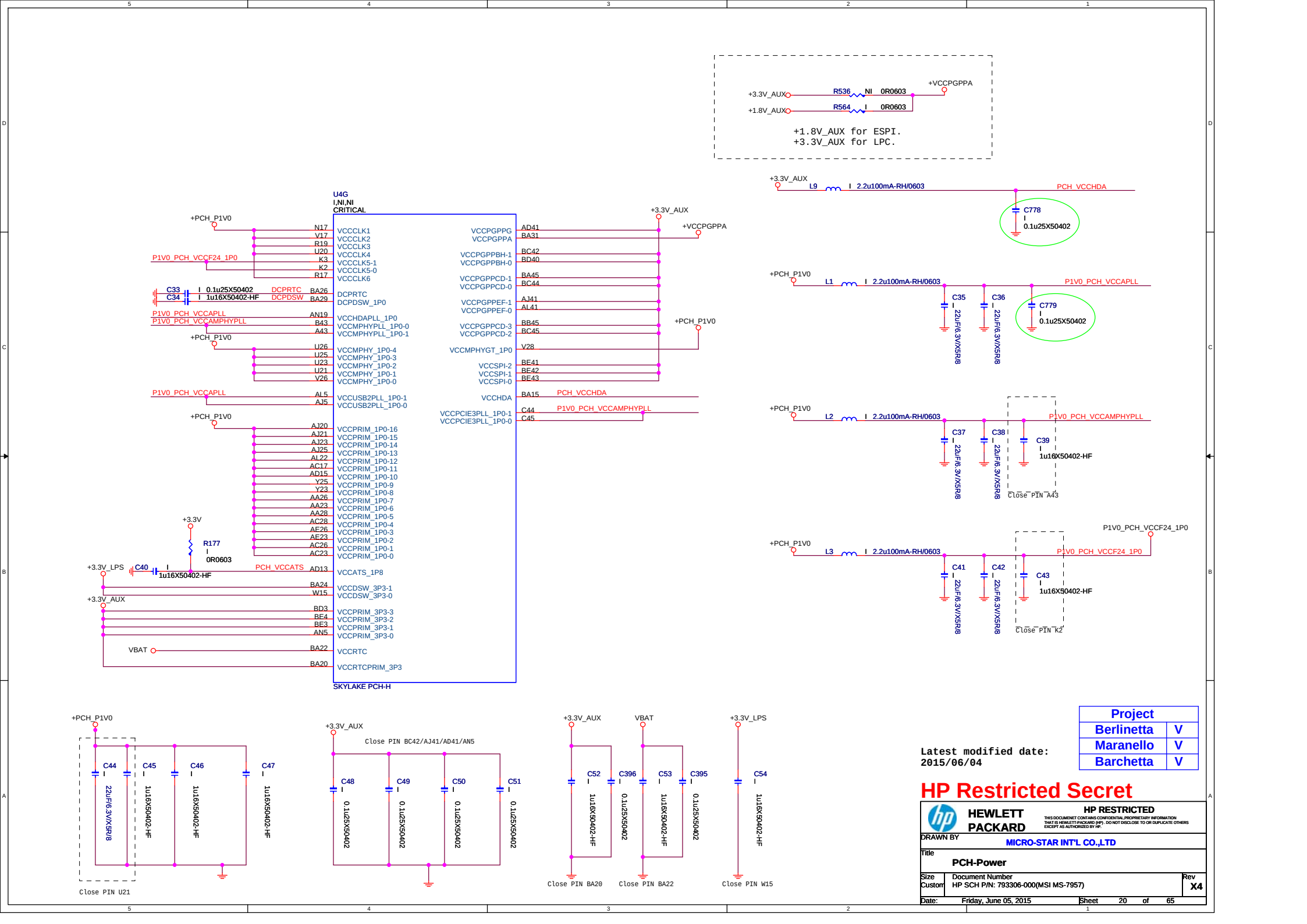

Project	
Berlinetta	V
Maranello	V
Barchetta	V

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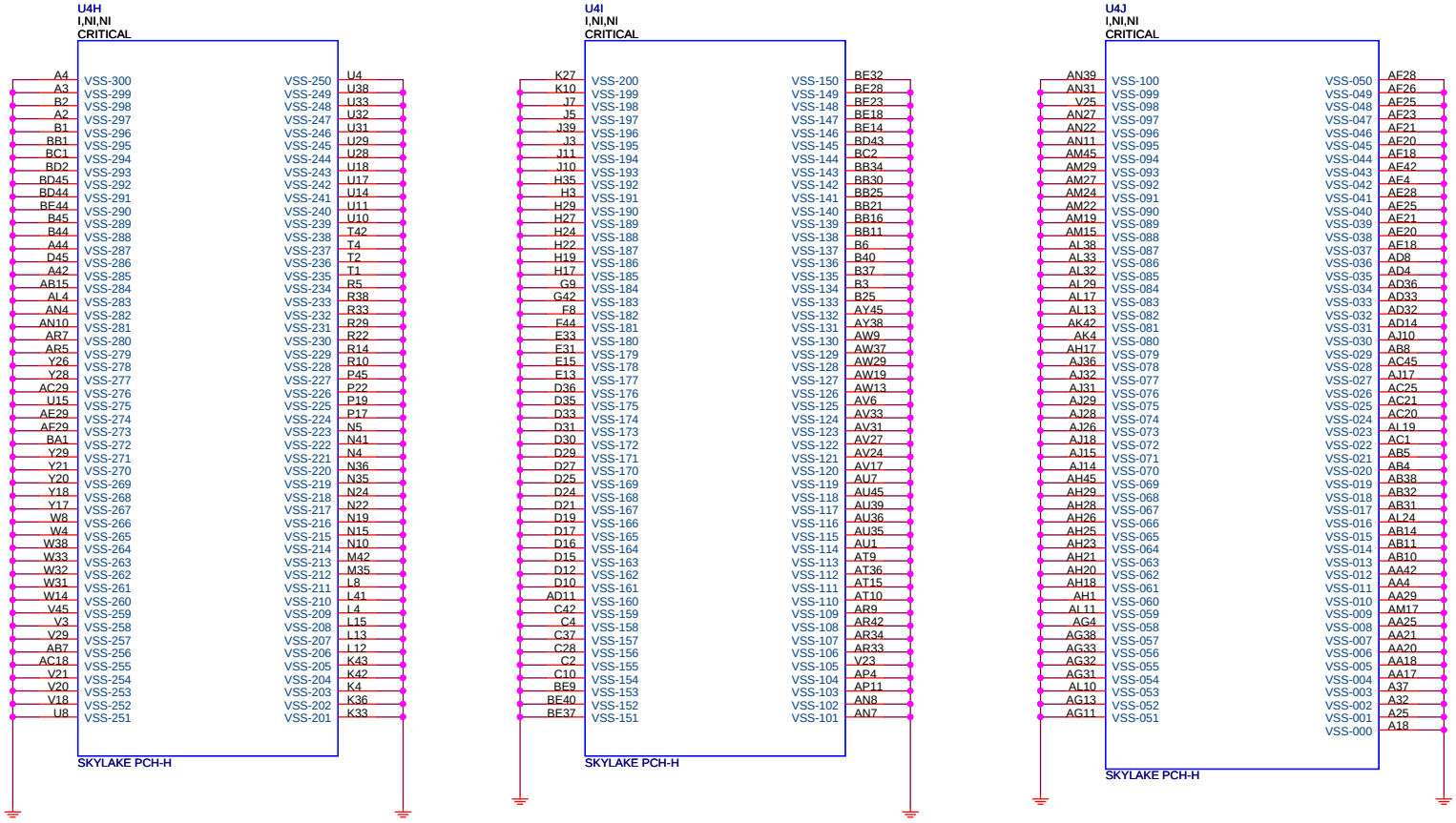

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Project	
Berlinetta	V
Maranello	V
Barchetta	V

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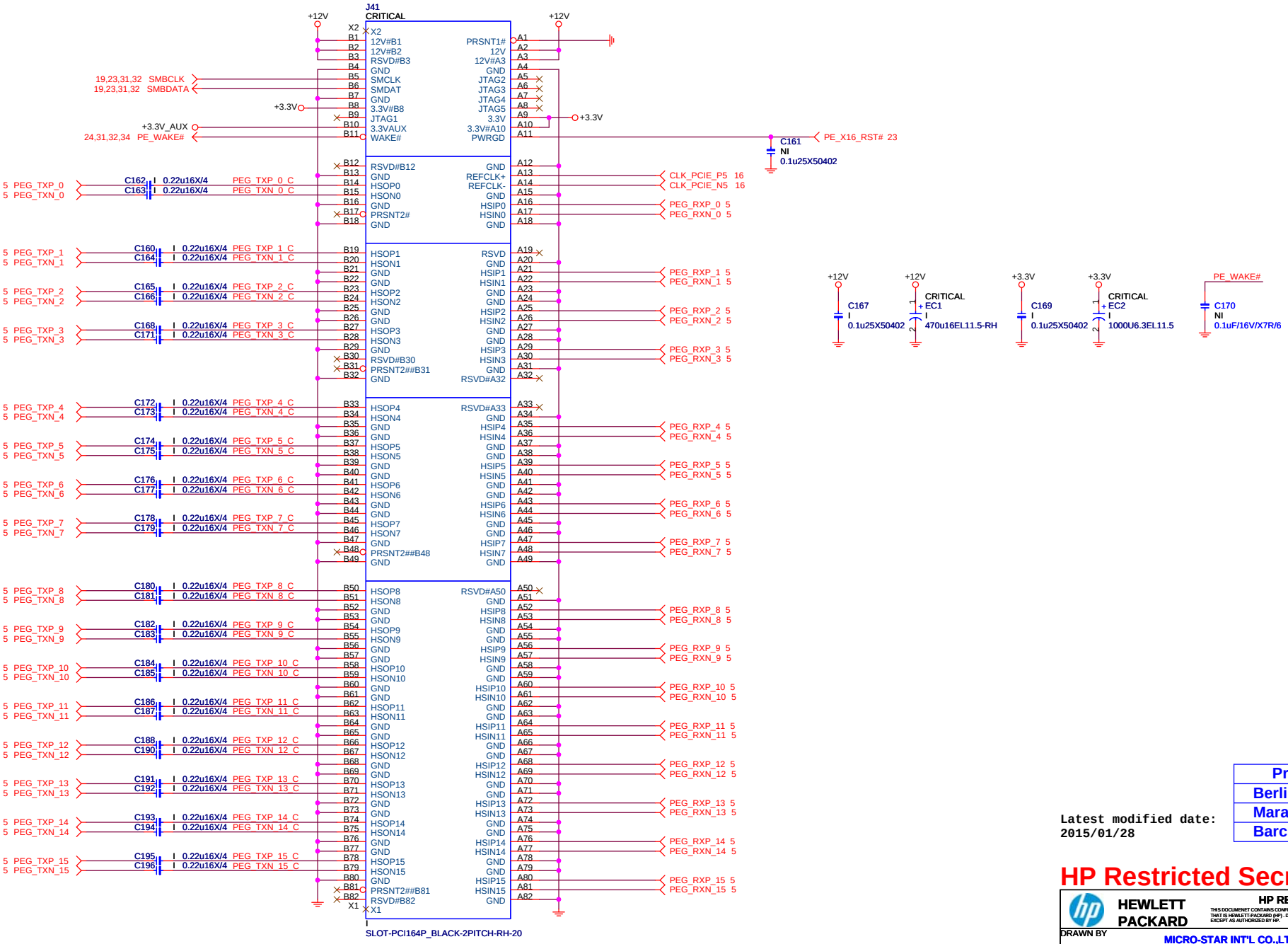
PCI_EXPRESS X16 SLOT



N11-1641151-L06

Project	
Berlinetta	V
Maranello	V
Barchetta	V

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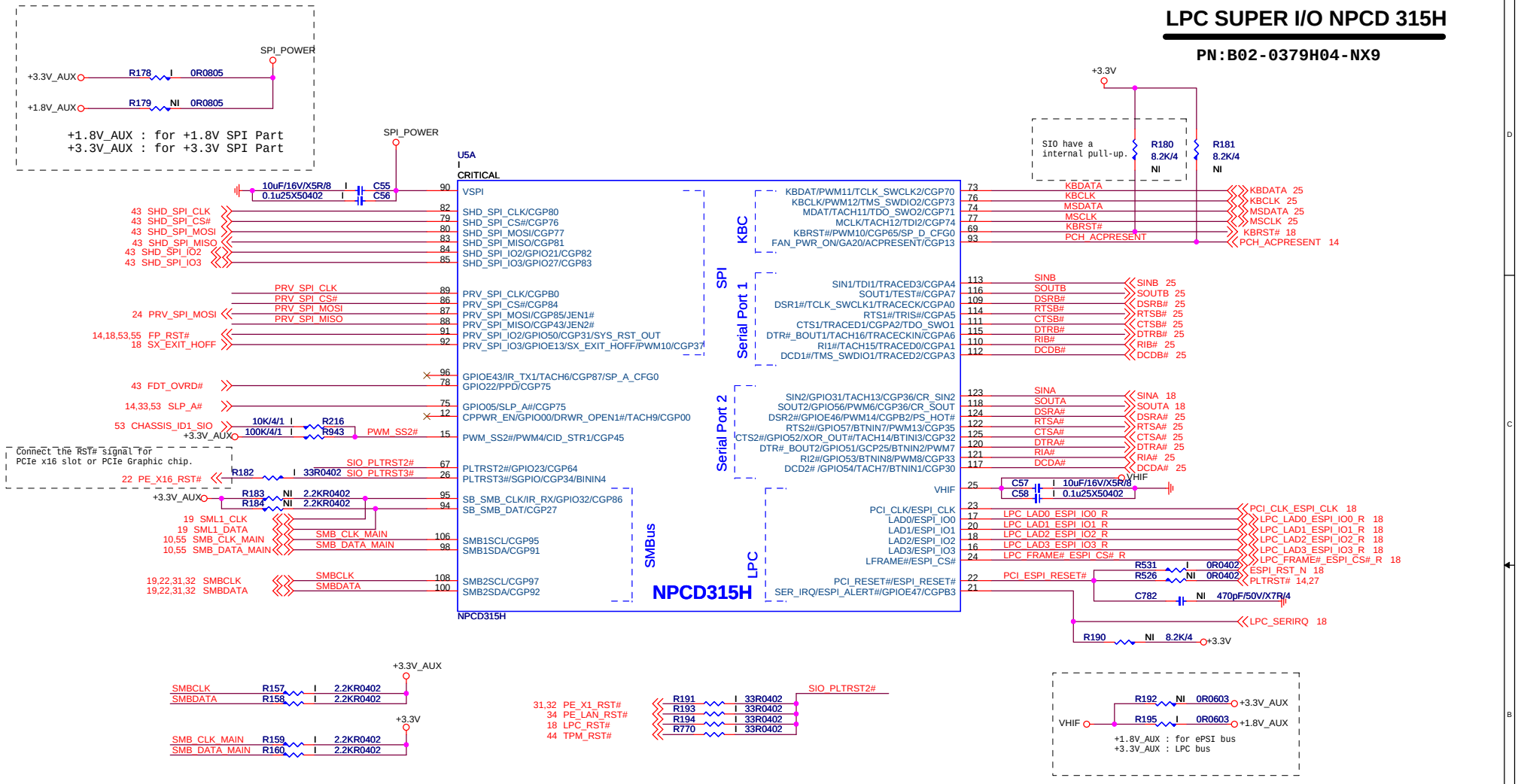
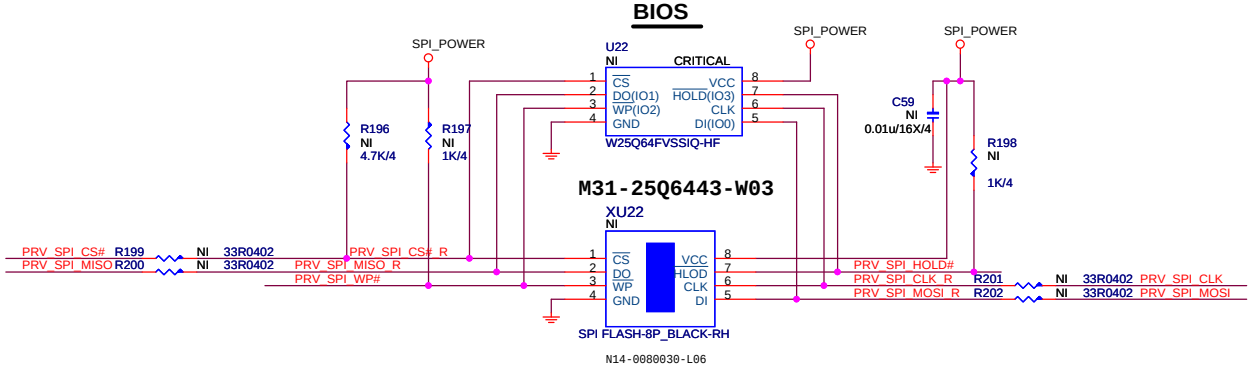
LPC SUPER I/O NPCD 315H

PN:B02-0379H04-NX9



SPI FLASH ROM



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Project	
Berlinetta	V
Maranello	V
Barchetta	V

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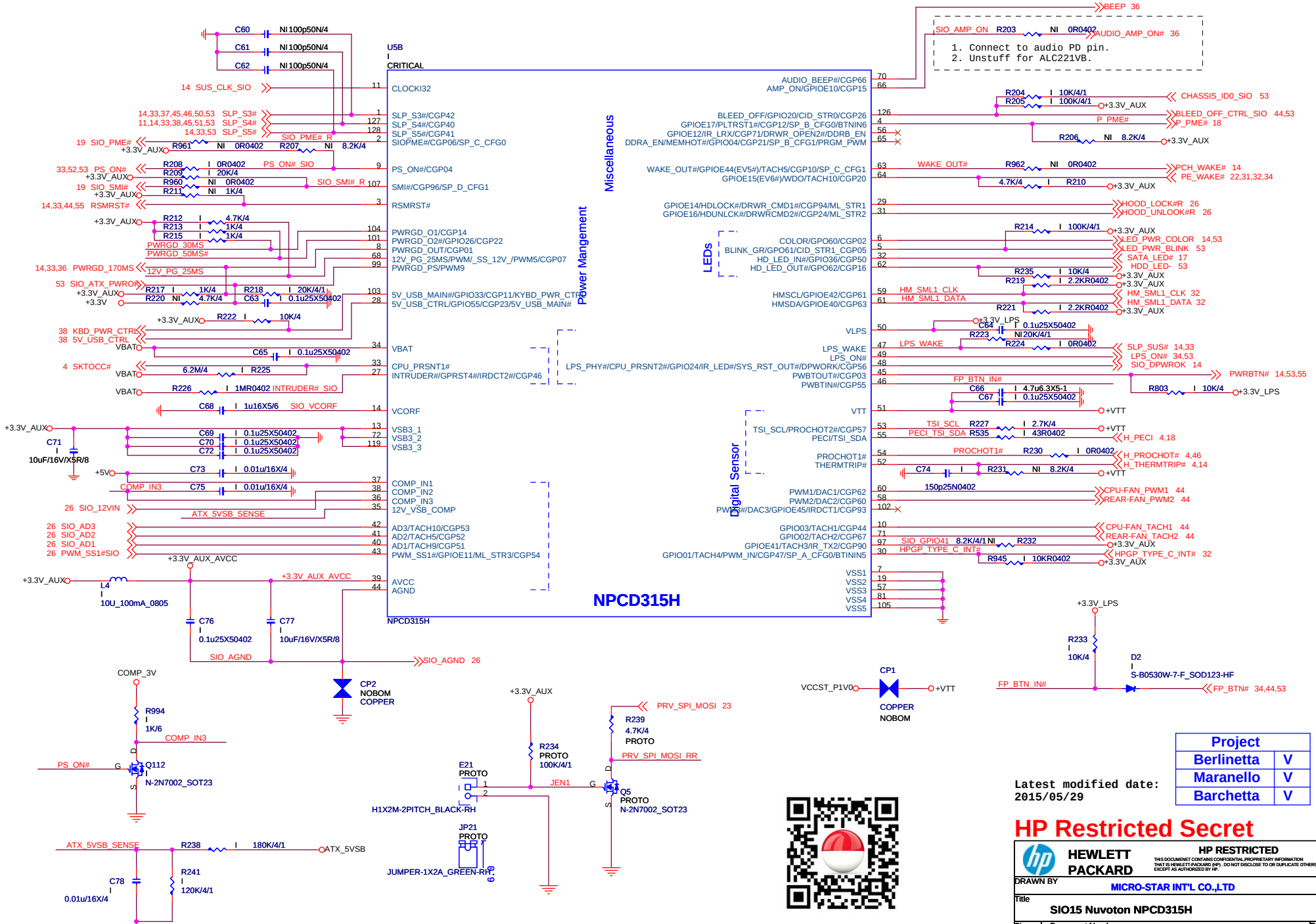

Project	
Berlinetta	V
Maranello	V
Barchetta	V

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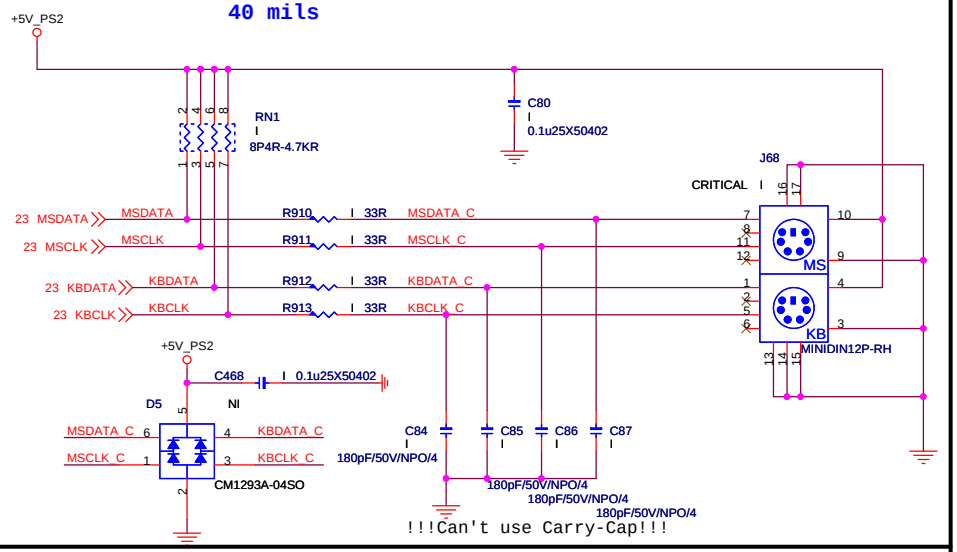
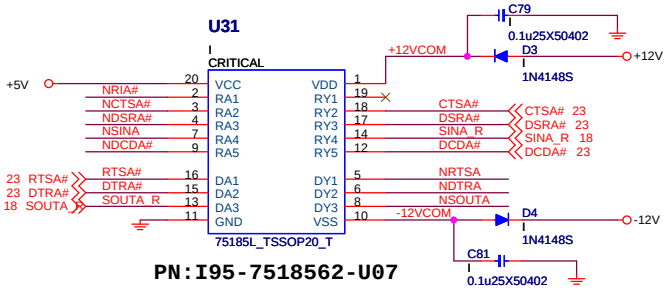
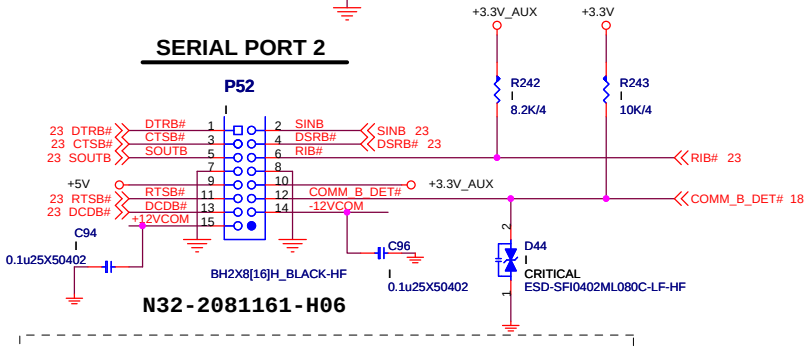
PS2 KEYBOARD & MOUSE CONNECTOR



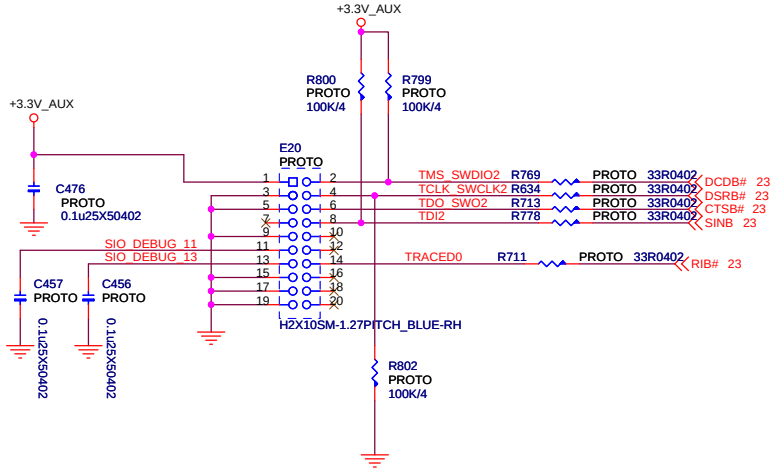
SERIAL PORT 1



SERIAL PORT 2



SIO15 ULINKPro DEBUG PORT



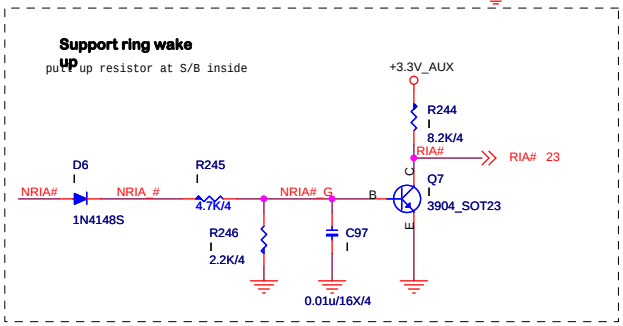


TABLE 12
FLOATING SERIAL PORT PIN DEFINITION (TOP VIEW)

P52

Pin #	Signal Name	Signal Name	Pin #
1	DTR#	RXD	2
3	CTS#	DSR#	4
5	TXD	RI#	6
7	GND	GND	8
9	+5 V	+3.3 VAUX	10
11	RTS#	COMM B DETECT#	12
13	DCD#	-12 V (THRU DIODE)	14
15	+12 V (THRU DIODE)	KEY	16

Project	
Berlinetta	V
Maranello	V
Barchetta	V

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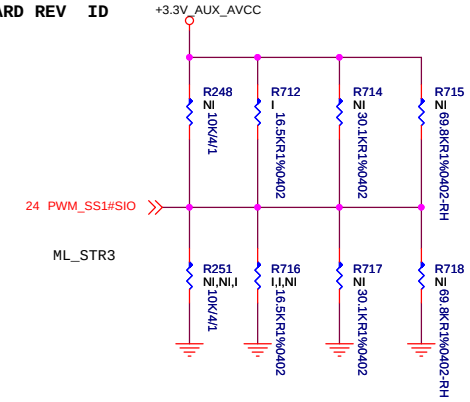
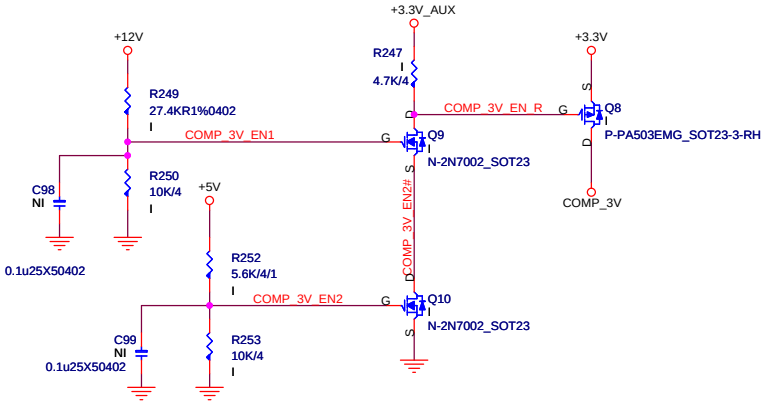
BOARD REV ID

Board REV	Pull-Down	Pull-UP	Development Phase
0	10K	NI	BD-1
1	10k	69.8k	BD-2
2	10k	30.1k	BD-3
3	10k	16.5k	SI-1
4	16.5k	16.5k	SI-2
5	16.5k	10k	SI-3
6	30.1k	10k	PV-1
7	69.8k	10k	PV-2

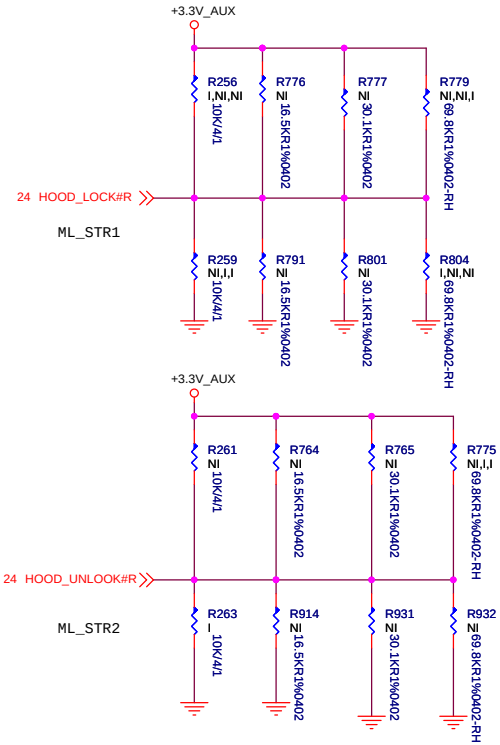


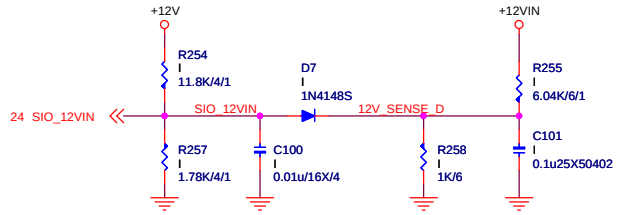


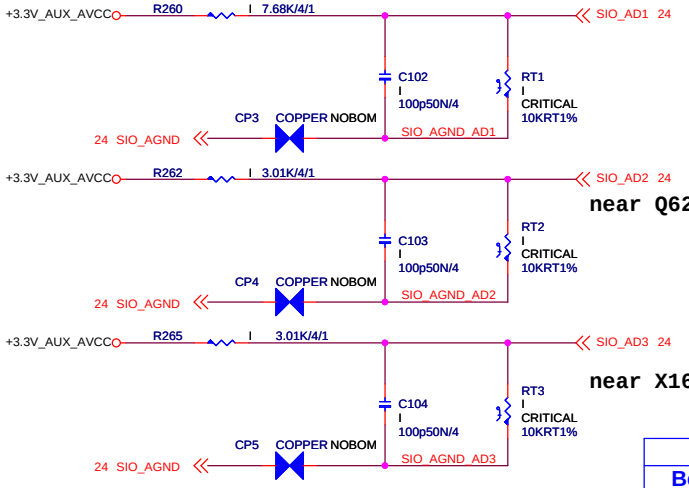
PCA

PCA	ML_STR2[2:0] (hex)	ML STR1[2:0] (hex)
Berlinetta	0	7
Maranello	1	0
Barchetta	1	1
Enzo	1	2

BRD_ID







Project	
Berlinetta	V
Maranello	V
Barchetta	V

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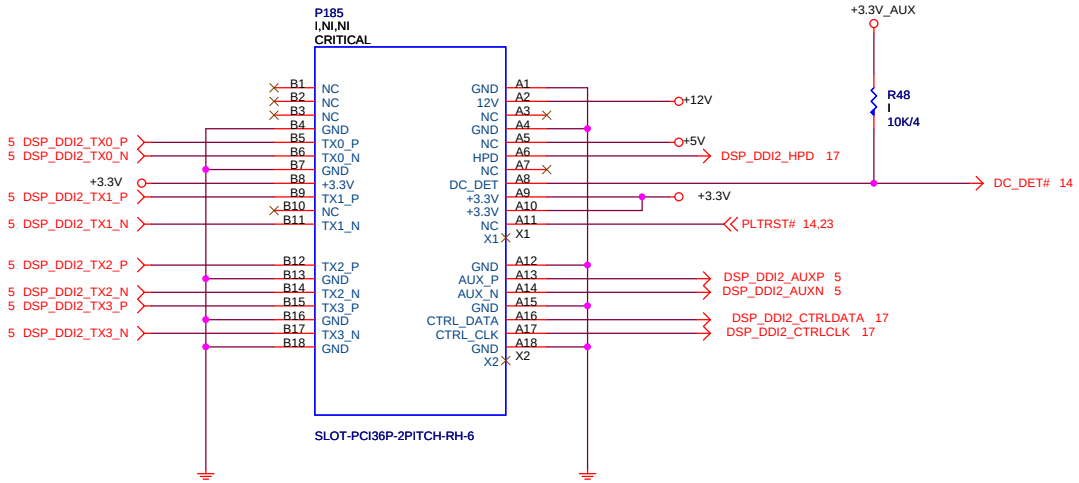
DDI Port Slot



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Berlinetta	V
Maranello	V
Barchetta	

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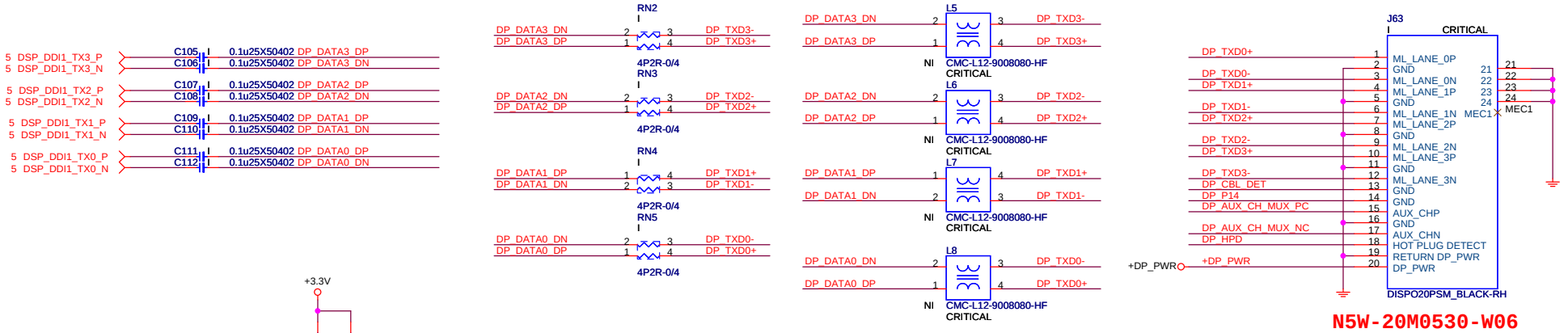
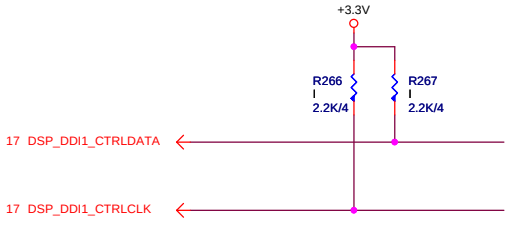
Title: DDI Port Slot

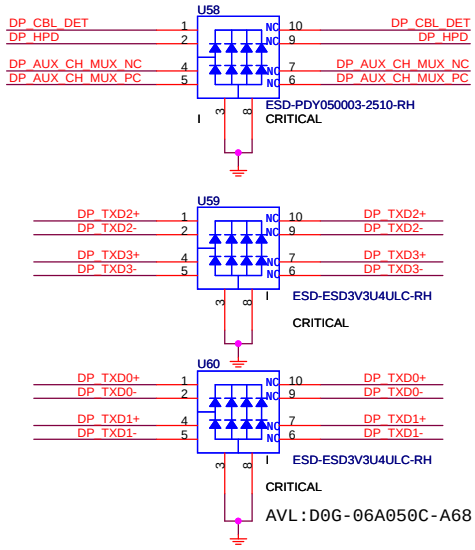
Size: Custom | Document Number: HP SCH P/N: 793306-000(MSI MS-7957) | Rev: X4

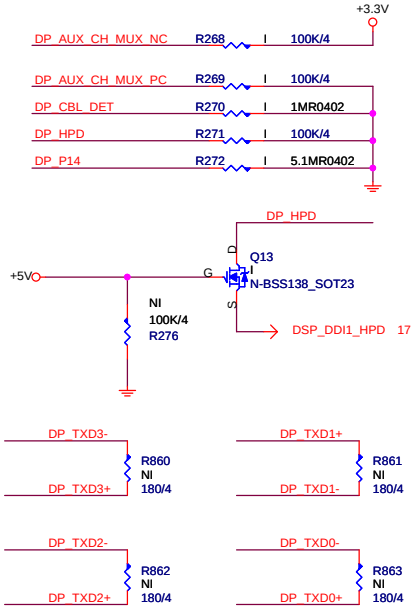
Date: Friday, June 05, 2015 | Sheet 27 of 65

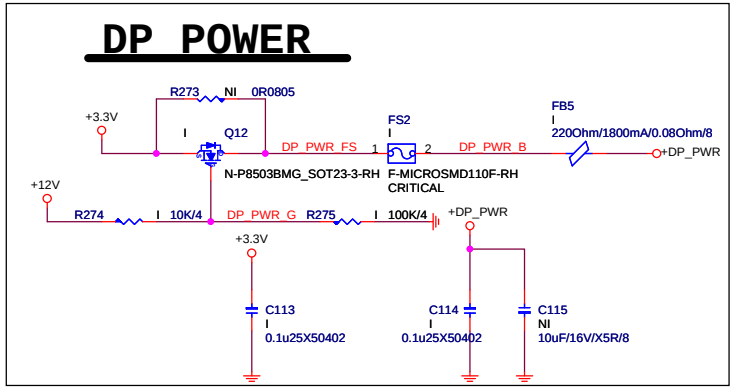


N5W-20M0530-W06

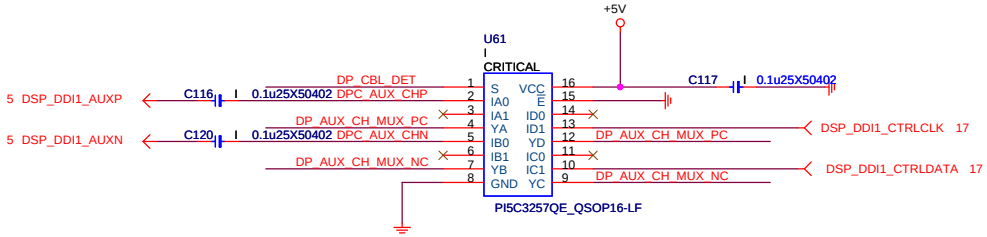


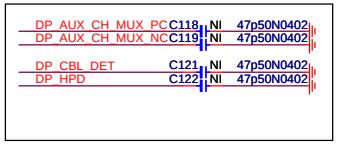






Vinafix.com





Project	
Berlinetta	V
Maranello	V
Barchetta	

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Title	DISPLAY CONN
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Rev	X4
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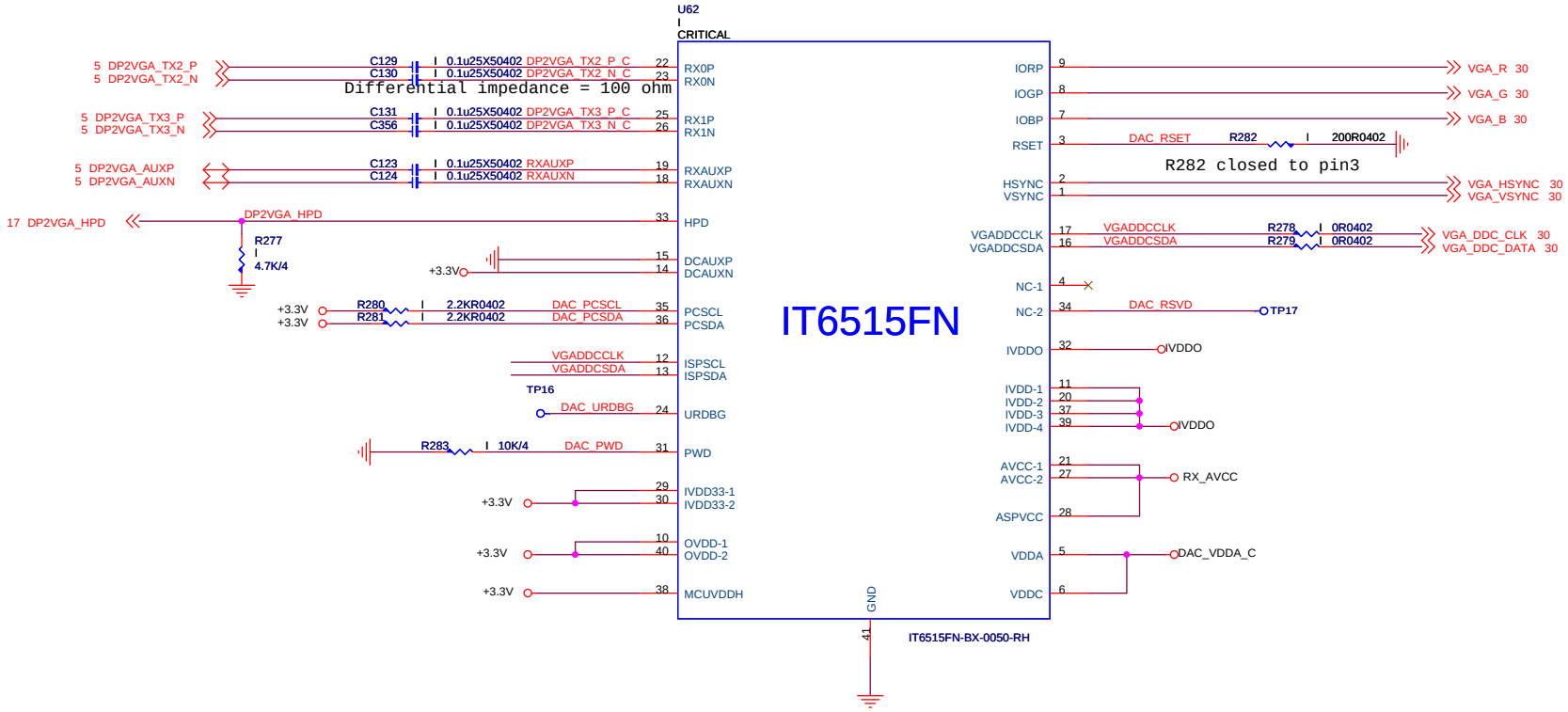

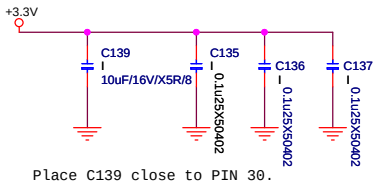

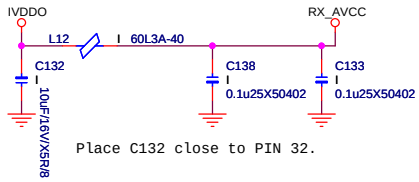

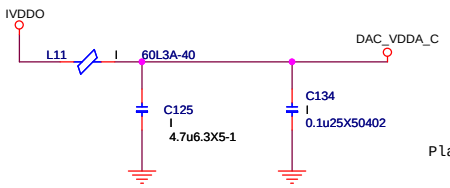

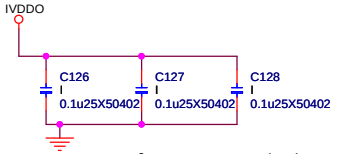

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Barchetta	V

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Title	DP to VGA- ITE IT6515
Size: Custom	Document Number: HP SCH P/N: 793306-000(MSI MS-7957)
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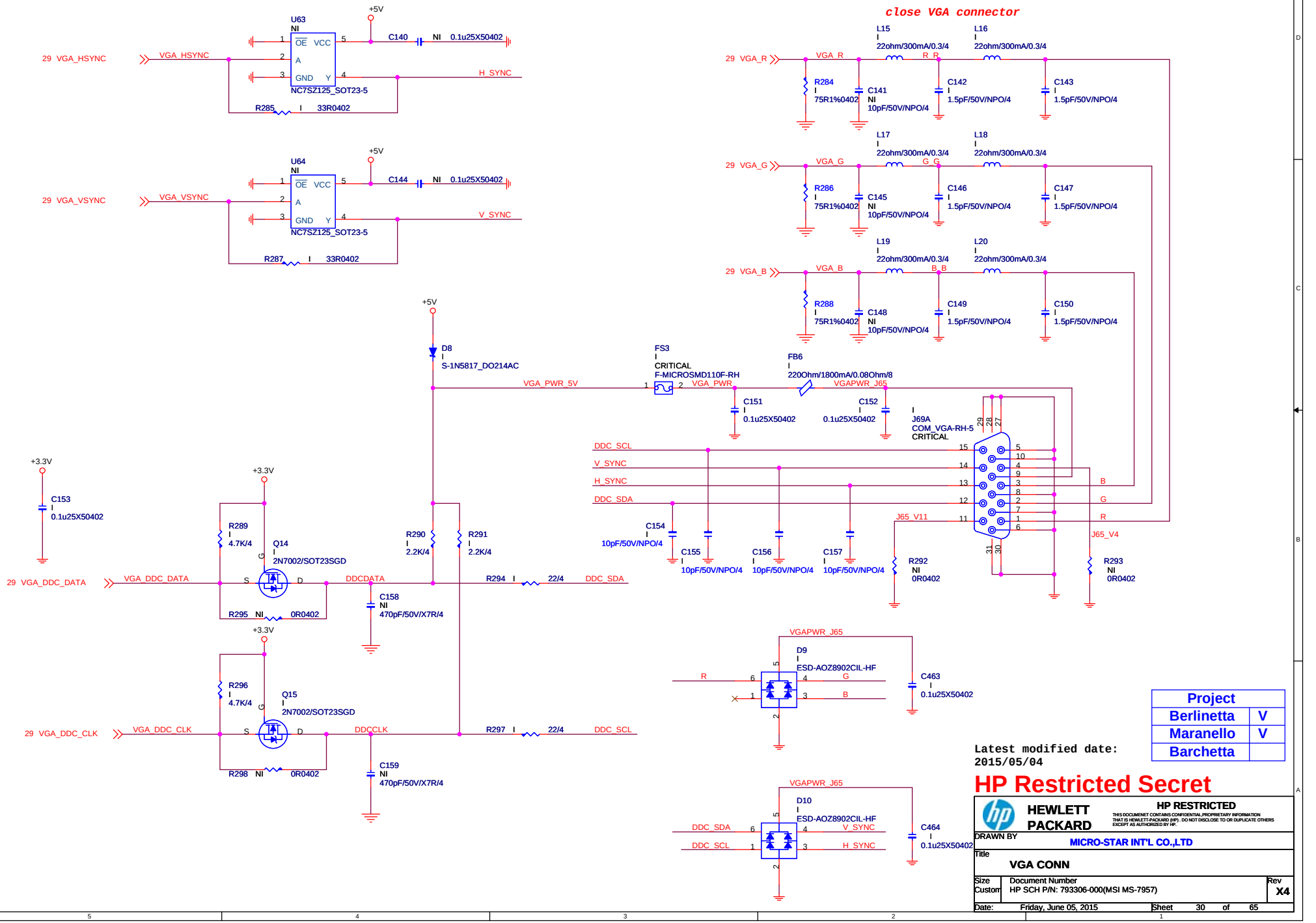
VGA CONN BLOCK



Project	
Berlinetta	V
Maranello	V
Barchetta	

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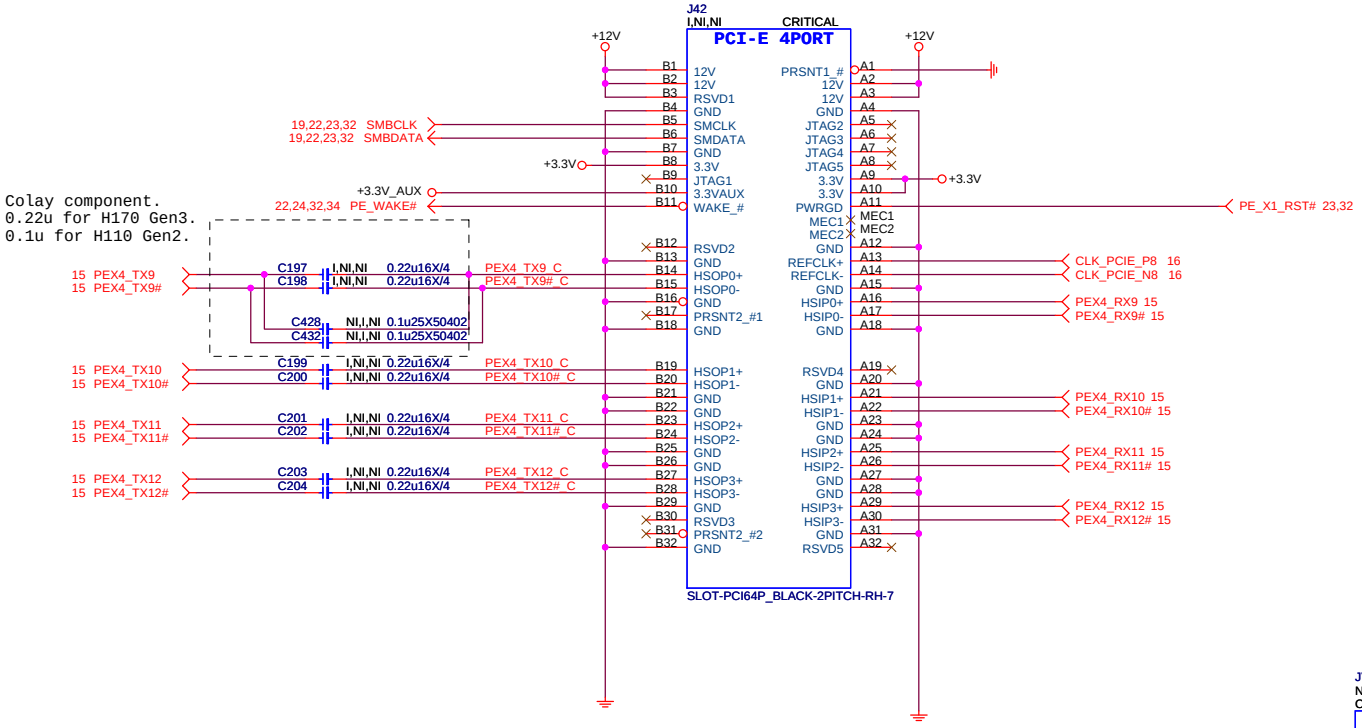
PCI EXPRESS X16 SLOT



JV42
NI,I,NI
CRITICAL
PCIE X1 SLOT
SLOT-PCI36P_BLACK-2PITCH-RH-22

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Berlinetta	V
Maranello	V
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Title: PCIE x16 Slot /w X4 Signal

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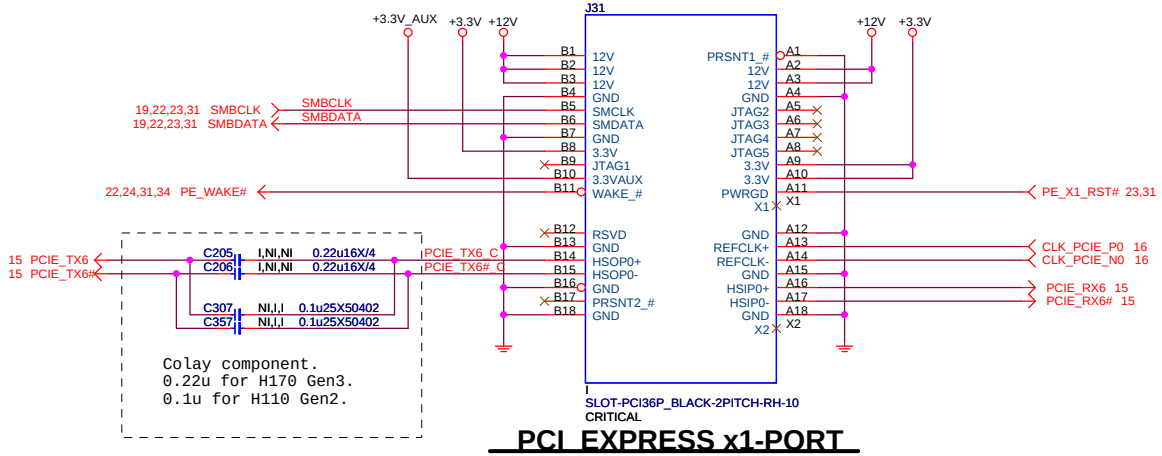
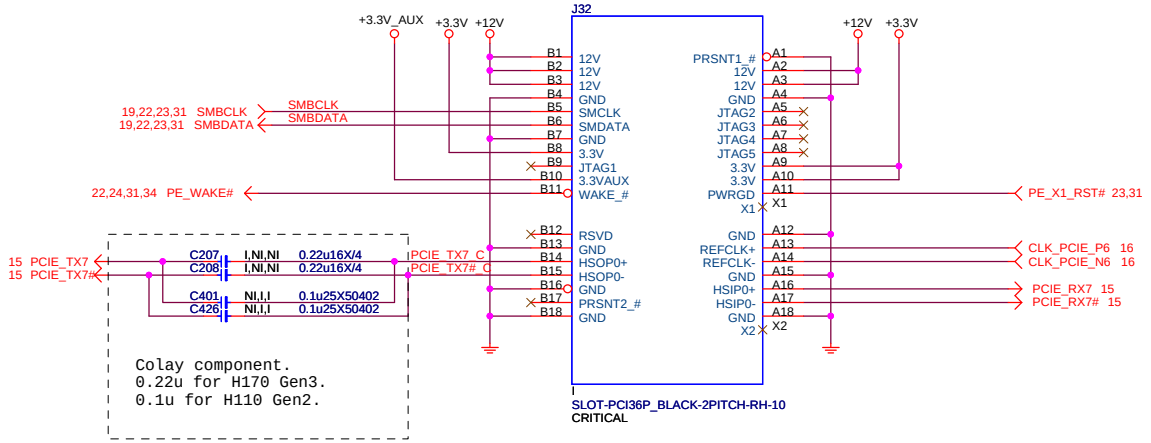
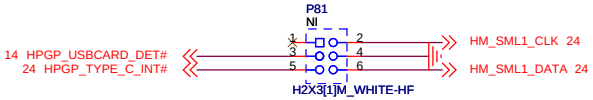
PCI_EXPRESS x1-PORT



PCI_EXPRESS x1-PORT





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Berlinetta	V
Maranello	V
Barchetta	V

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Title: PCIE x1 Slots

Size	Document Number	Rev
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SATA Connector

P60

17 SATA_TX0 — C209 0.01u/16X/4 — ST_TX0
17 SATA_TX#0 — C210 0.01u/16X/4 — ST_TX#0
17 SATA_RX#0 — C213 0.01u/16X/4 — ST_RX#0
17 SATA_RX0 — C214 0.01u/16X/4 — ST_RX0

Dark Blue
N5N-07M2281-L06

SATA7P_DARKBLUE
CRITICAL

P62

17 SATA_TX2 — C211 0.01u/16X/4 — ST_TX2
17 SATA_TX#2 — C212 0.01u/16X/4 — ST_TX#2
17 SATA_RX#2 — C215 0.01u/16X/4 — ST_RX#2
17 SATA_RX2 — C216 0.01u/16X/4 — ST_RX2

Light Blue
N5N-07M2291-L06

SATA7P_BLUE
CRITICAL

P61

17 SATA_TX1 — C217 0.01u/16X/4 — ST_TX1
17 SATA_TX#1 — C218 0.01u/16X/4 — ST_TX#1
17 SATA_RX#1 — C219 0.01u/16X/4 — ST_RX#1
17 SATA_RX1 — C220 0.01u/16X/4 — ST_RX1

Light Blue
N5N-07M2291-L06

SATA7P_BLUE
CRITICAL

SLP_LAN#

Q17
PROTO
P-PA503EMG_SOT23-3-RH

+3.3V_AUX — S — D — SLP_LAN#_LED_R
G — 14 SLP_LAN#
R300 PROTO 330R/6
SLP_LAN#_LED
CR5 PROTO LED04-G-30mA2.1/8

D0C-0400500-E07

RSMRST#

Q108
PROTO
P-PA503EMG_SOT23-3-RH

+3.3V_AUX — S — D — RSMRST#_LED_R
RSMRST#_L — G
R984 PROTO 100K/4/1
14,24,44,55 RSMRST#
R985 PROTO 330R/6
RSMRST#_LED
CR12 PROTO LED04-G-30mA2V_1608-RH

D0C-0400620-L05

SLP_A#

Q19
PROTO
P-PA503EMG_SOT23-3-RH

+3.3V_AUX — S — D — SLP_A#LED_R
14,23,53 SLP_A# — SLP_A# — G
R302 PROTO 330R/6
SLP_A#LED
CR4 PROTO LED04-G-30mA2.1/8

SLP_S4#

Q18
PROTO
P-PA503EMG_SOT23-3-RH

+3.3V_AUX — S — D — SLP4LED_R
11,14,24,38,45,51,53 SLP_S4# — G
R301 PROTO 330R/6
SLP4LED
CR2 PROTO LED04-G-30mA2.1/8

D0C-0400500-E07

3VSB

+3.3V_AUX
R303 330R/6
3VDLED
CR1 LED04-G-30mA2.1/8

D0C-0400500-E07

VRMPWRGD

+3.3V_AUX

D0C-0400500-E07

R304 PROTO 330R/6
VR_GDLED — CR3 PROTO LED04-G-30mA2.1/8 — VR_GDLED_R
14,46 VRM_PGD — G — Q20 PROTO N-2N7002P_SOT23

POWERGOOD_140MS

+3.3V_AUX

D0C-0400500-E07

R305 PROTO 330R/6
PD_170MS_LED — CR6 PROTO LED04-G-30mA2.1/8 — PD_170MS_LED_R
14,24,36 PWRGD_170MS — G — Q23 PROTO N-2N7002P_SOT23

PS_ON#

Q21
PROTO
P-PA503EMG_SOT23-3-RH

+3.3V_AUX — S — D — PS_ON#LED_R
24,52,53 PS_ON# — G
R306 PROTO 330R/6
PS_ON#LED
CR7 PROTO LED04-G-30mA2.1/8

D0C-0400500-E07

SLP_S5#

Q22
P-PA503EMG_SOT23-3-RH

+3.3V_AUX — S — D — SLP5LED_R
14,24,53 SLP_S5# — G
PROTO
R307 PROTO 330R/6
SLP5LED
CR8 PROTO LED04-G-30mA2.1/8

D0C-0400500-E07

IERR

Q24
P-PA102FMG_SOT23-HF

+3.3V — S — D — CATERRLED_R
R308 PROTO 4.7K/4
+3.3V_AUX — CATERRLED_G — G
PROTO
R310 PROTO 10K/4
+VCCIO — CATERRLED_B — B — Q25 2N3904 — C — E
4 H_CATERR# — PROTO
R309 PROTO 330R/6
CATERRLED
CR9 PROTO LED04-R-30mA2V_1608-RH

D0C-0402010-L05

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Berlinetta	V
Maranello	V
Barchetta	V

SLP_S3#

Q26
PROTO
P-PA503EMG_SOT23-3-RH

+3.3V_AUX — S — D — SLP3LED_R
14,24,37,45,46,50,53 SLP_S3# — G
R311 PROTO 330R/6
SLP3LED
CR10 PROTO LED04-G-30mA2.1/8

D0C-0400500-E07

SLP_SUS#

Q27
PROTO
P-PA503EMG_SOT23-3-RH

+3.3V_AUX — S — D — SLP_SUS#LED_R
14,24 SLP_SUS# — G
R312 PROTO 330R/6
SLP_SUS#LED
CR11 PROTO LED04-G-30mA2.1/8

D0C-0400500-E07

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Title	SATA/LED
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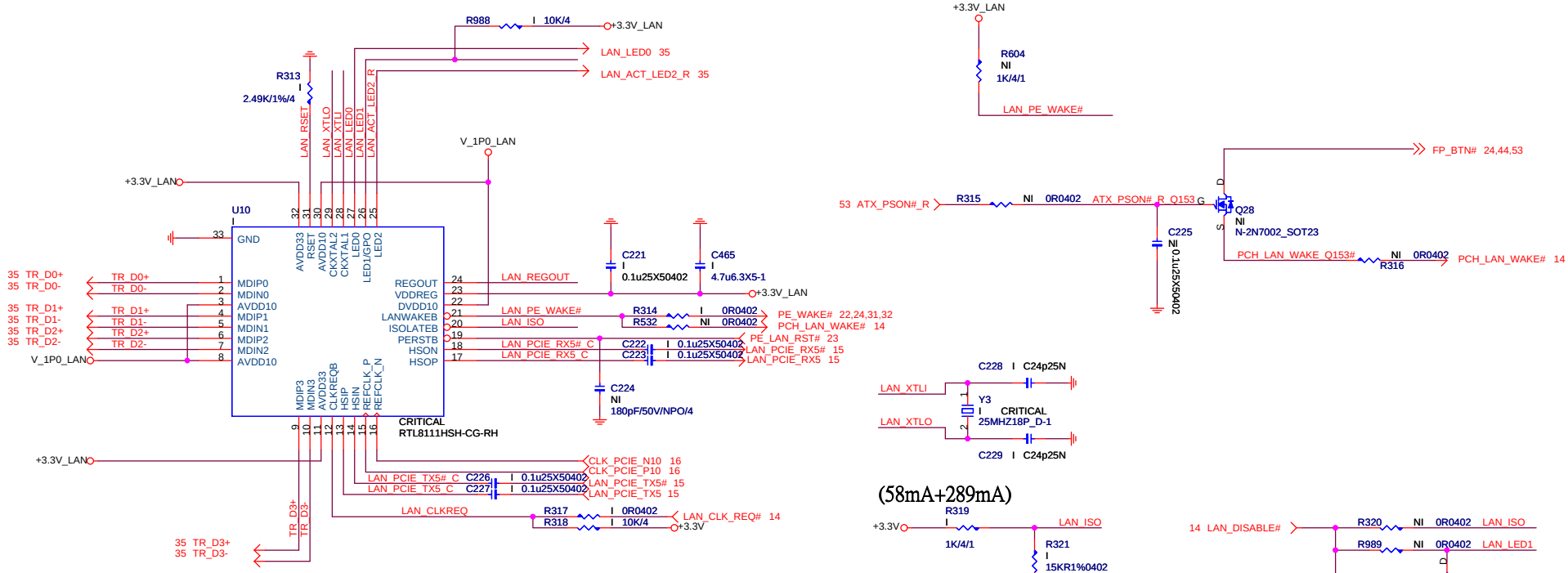
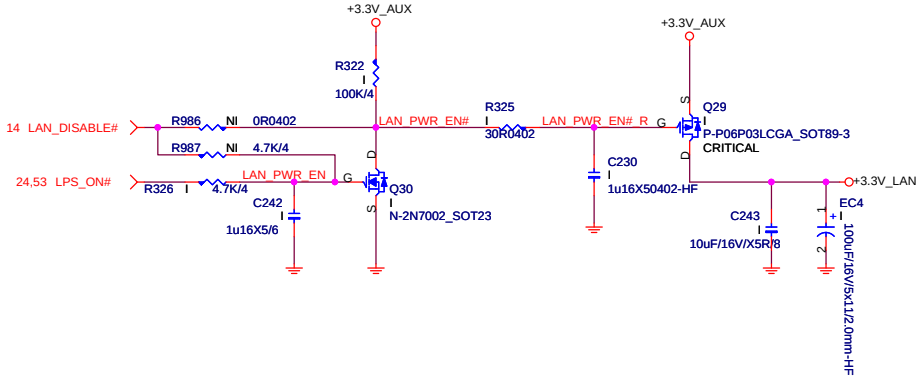
Gigabit LAN RTL8111HSH-CG

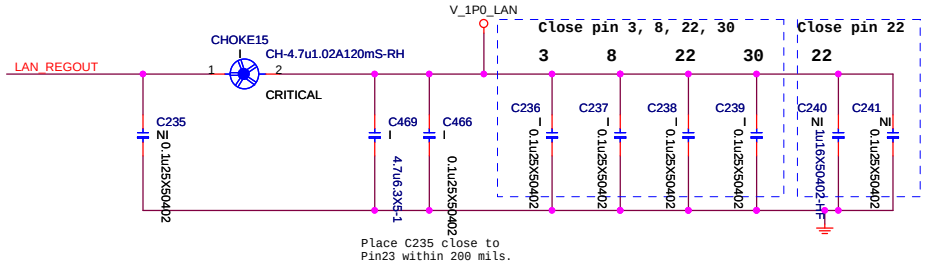


B06-08111FC-R09

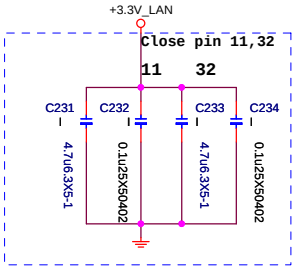
Place Near Pin

LAN Power





Place Near Pin



Project	
Berlinetta	V
Maranello	V
Barchetta	V

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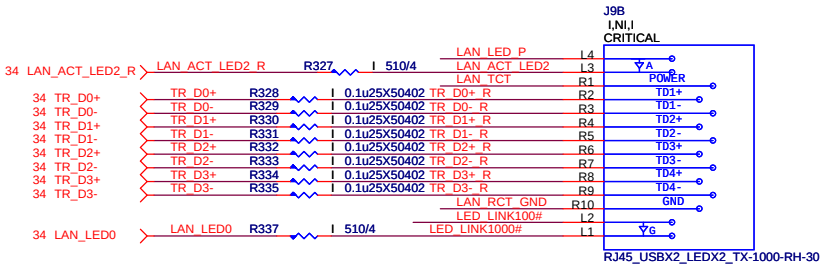
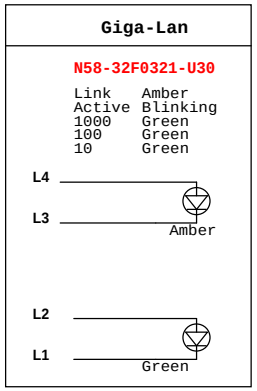
Size: Custom	Document Number: HP SCH P/N: 793306-000(MSI MS-7957)
Rev	X4
Date: Friday, June 05, 2015	Sheet 34 of 65

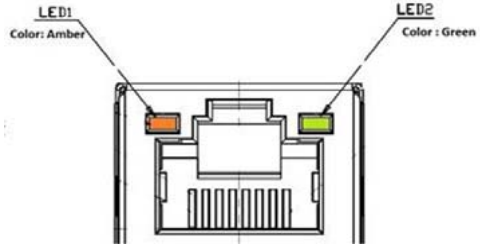
LAN Connector



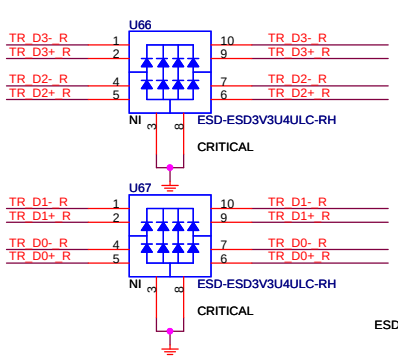
N58-32F0321-U30

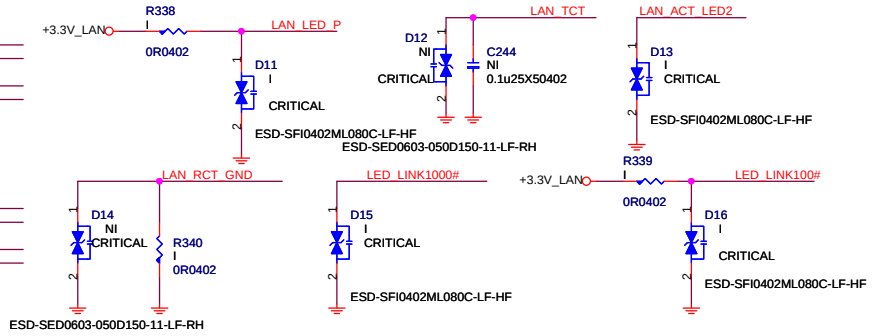


WOL ON	Speed	Active/Idle Mode		
		S0	S3/S4	S5
Active LED	1G Bit	Blink Amber	Blink Amber	Blink Amber
	100M Bit	Blink Amber	Blink Amber	Blink Amber
	10M Bit	Blink Amber	Blink Amber	Blink Amber
Link Speed LED	1G Bit	Green	Green	Green
	100M Bit	Green	Green	Green
	10M Bit	Green	Green	Green
WOL OFF		S0	S3/S4	S5
Active LED	1G Bit	Blink Amber	OFF	OFF
	100M Bit	Blink Amber	OFF	OFF
	10M Bit	Blink Amber	OFF	OFF
Link Speed LED	1G Bit	Green	OFF	OFF
	100M Bit	Green	OFF	OFF
	10M Bit	Green	OFF	OFF
Link OFF		S0	S3/S4	S5
Active LED	1G Bit	OFF	OFF	OFF
	100M Bit	OFF	OFF	OFF
	10M Bit	OFF	OFF	OFF
Link Speed LED	1G Bit	OFF	OFF	OFF
	100M Bit	OFF	OFF	OFF
	10M Bit	OFF	OFF	OFF



ESD

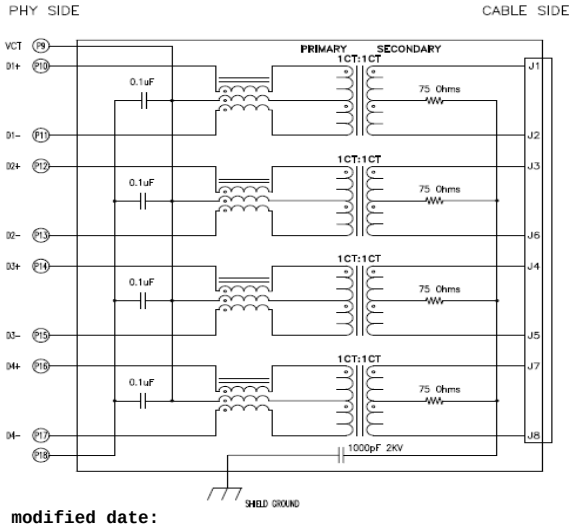




D12,D14,
D0G-1500500-SI0
AVL:D0G-3500510-N47

D11,D13,D15,D16
D0G-2950500-SI0
AVL:D0G-3010510-I05

SCHEMATIC



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Project	
Berlinetta	V
Maranello	V
Barchetta	V

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Title: LAN CONNECTOR

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Date: Friday, June 05, 2015 | Sheet 35 of 65

ALC 221 CODEC

B05-LC2212C-R09

Install R341 for ALC221-VA

ALC221: Install R342, Un-Install C245
ALC221-VB:Un-install R342,Install C245

Install R344 for ALC221-VB

ALC221: Install R346
ALC221-VB:Install R345

ALC221: Install R343, Un-Install R347
ALC221-VB:Un-install R343,Install R347

Install FB9, C254 for ALC221-VB

ALC221: Install FB10, Un-Install FB8
ALC221-VB:Un-install FB10,Install FB8

ALC221: Install R350, Un-Install C257
ALC221-VB:Un-install R350,Install C257

ALC221-VB: Install R353

place 0.1uf close to pin1 and pin9 each

ALC221: Install C270
ALC221-VB:Un-install C270

Digital

Analog

(PORT-C)

ALC221-VB-CG-HF

ALC221 JACK DETECT

All of JD resistors should be placed as close as possible to the sense pin of codec.

AUDIO AMPLIFIER ENABLE

EMI Solution

FRONT I/O AUDIO

REAR I/O AUDIO

AUDIO CODEC

1000pf stitch cap for EMI, and place close to jack

Vinafix.com

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2015/04/14

Project	
Berlinetta	V
Maranello	V
Barchetta	V

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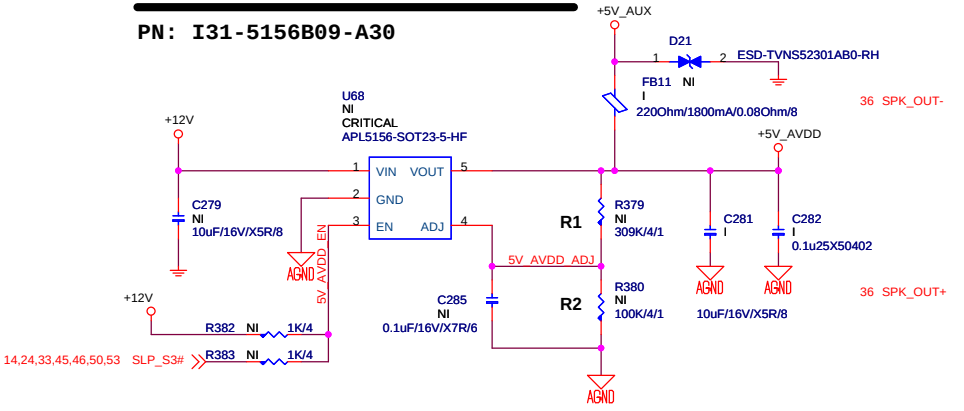
Title	Azalia Codec-ALC 221
Size: Custom	Document Number: HP SCH P/N: 793306-000(MSI MS-7957)
Rev	X4
Date: Friday, June 05, 2015	Sheet 36 of 65

AUDIO CODEC REGULATORS

PN: I31-5156B09-A30



SPEAKER HEADER

P/N:N32-1020521-F02

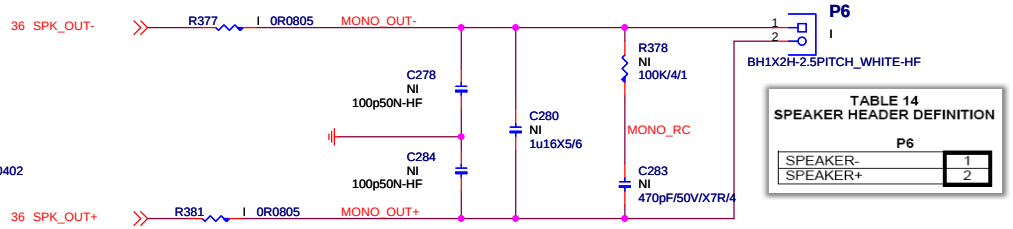


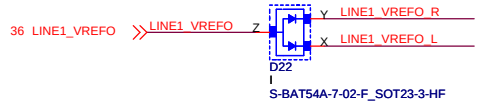
TABLE 14
SPEAKER HEADER DEFINITION

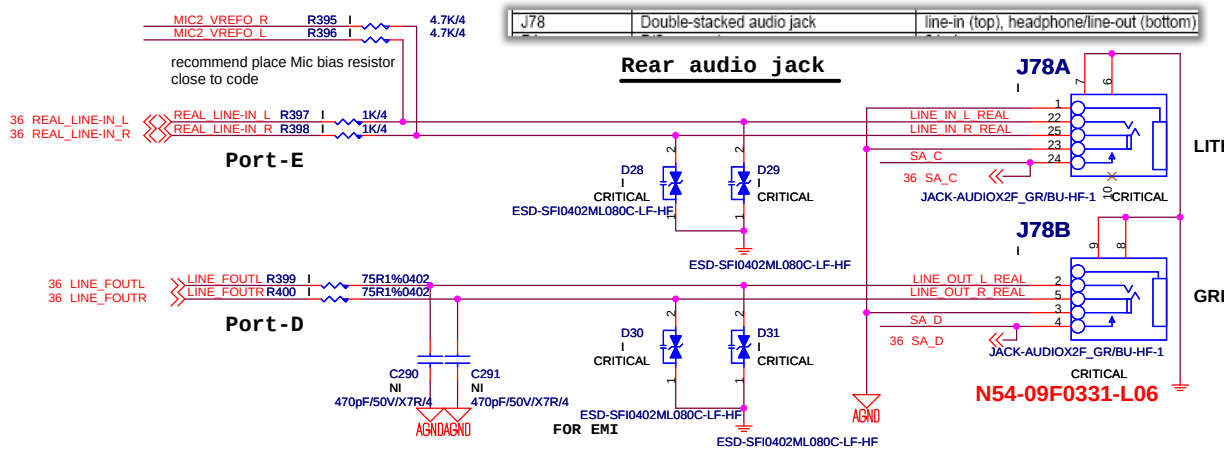
P6	
SPEAKER-	1
SPEAKER+	2

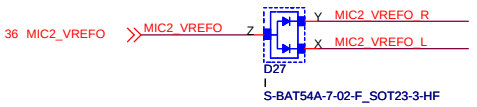
SPK+- TRACE WIDTH
Speaker 4 ohm ==> 40mils
Speaker 8 ohm ==> 20mils

Azalia Front Audio Connector

N31-2051491-H06







D23,D24,D25,D26,D28,D29,D30,D31
D0G-2950500-SI0
AVL:D0G-3010510-I05

Latest modified date:
2014/11/27

Project	
Berlinetta	V
Maranello	V
Barchetta	V

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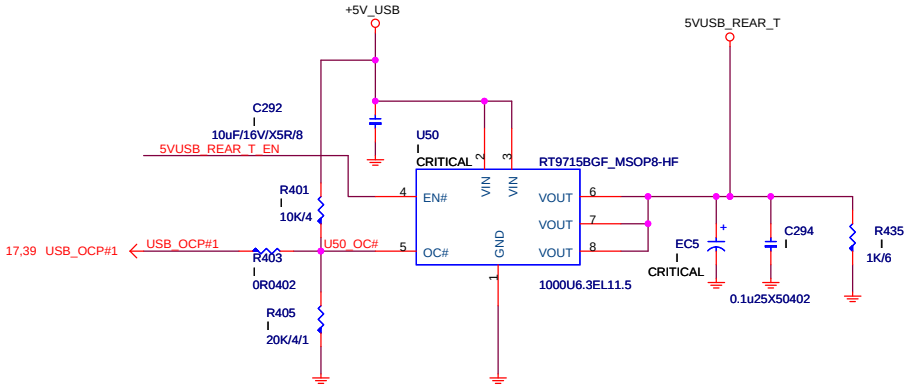
Title AUDIO CONNECTOR

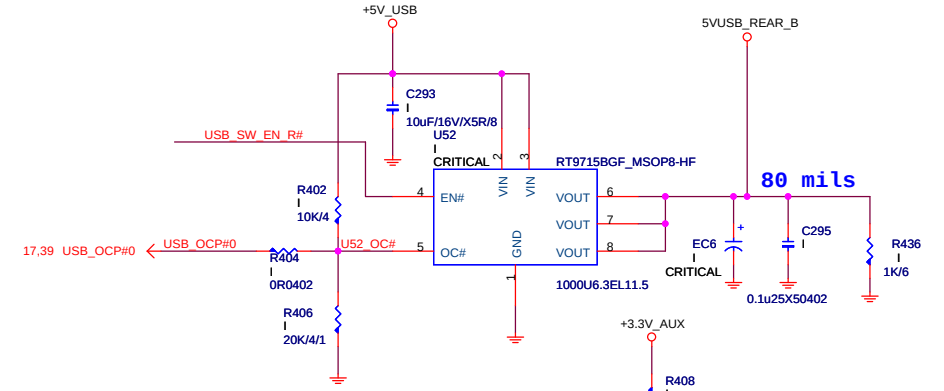
Size Custom | Document Number HP SCH P/N: 793306-000(MSI MS-7957) | Rev X4

Date: Friday, June 05, 2015 | Sheet 37 of 65

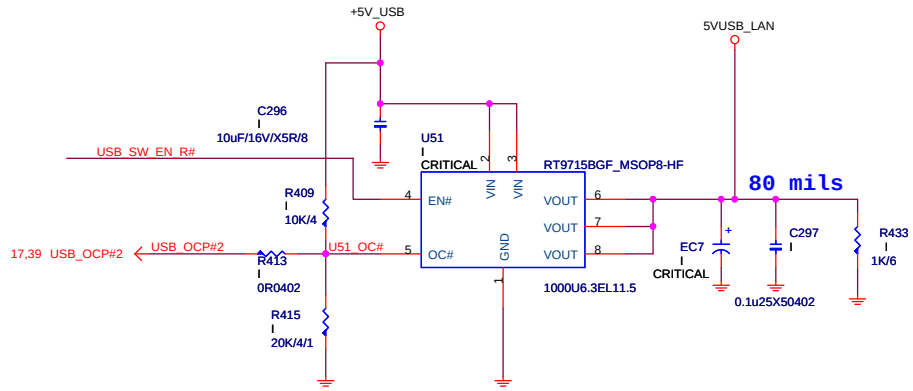
P/N:I36-9715B02-R11

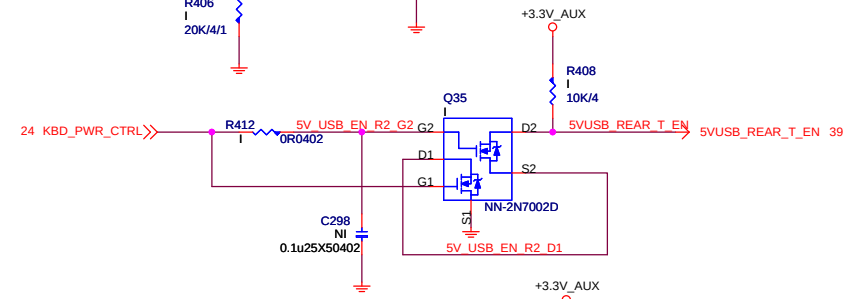


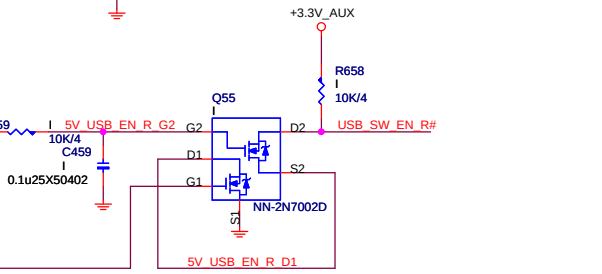
P/N:I36-9715B02-R11

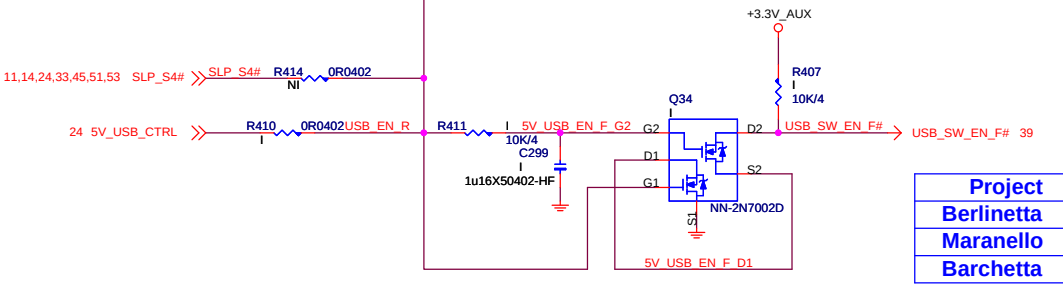


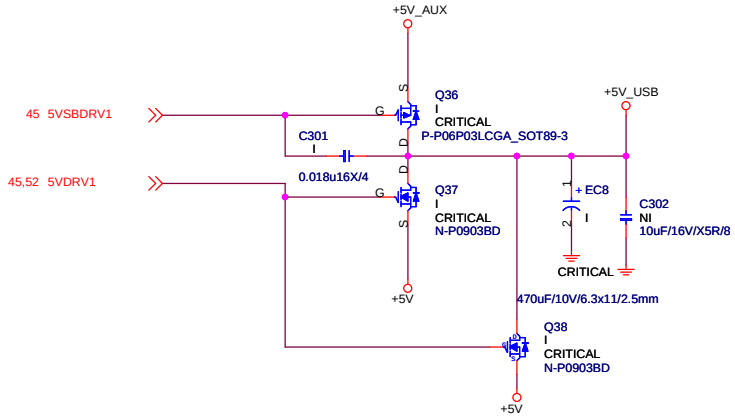
P/N:I36-9715B02-R11











Project	
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Maranello	V
Barchetta	V

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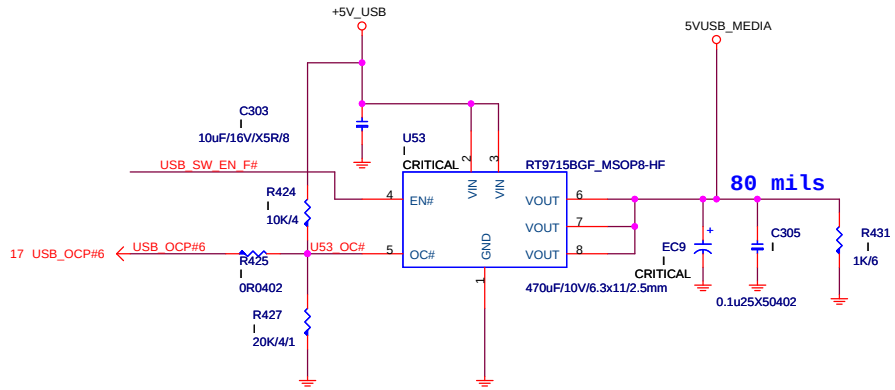
Title: Rear USB POWER

Size: Custom | Document Number: HP SCH P/N: 793306-000(MSI MS-7957) | Rev: X4

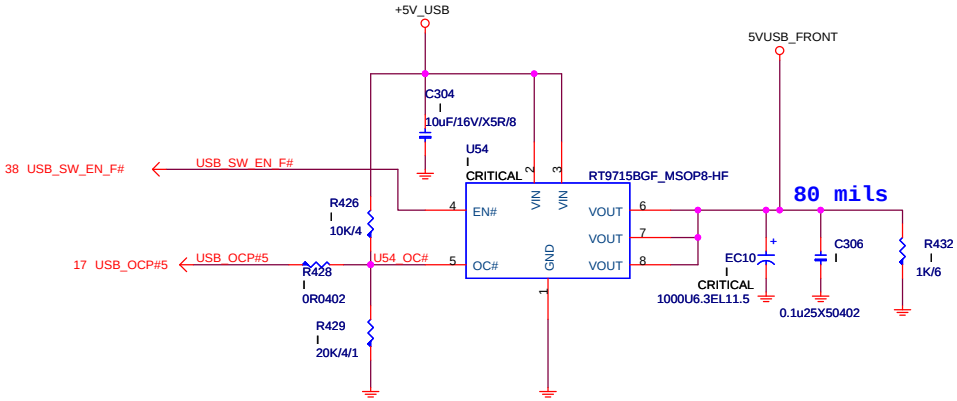
Date: Friday, June 05, 2015 | Sheet 38 of 65

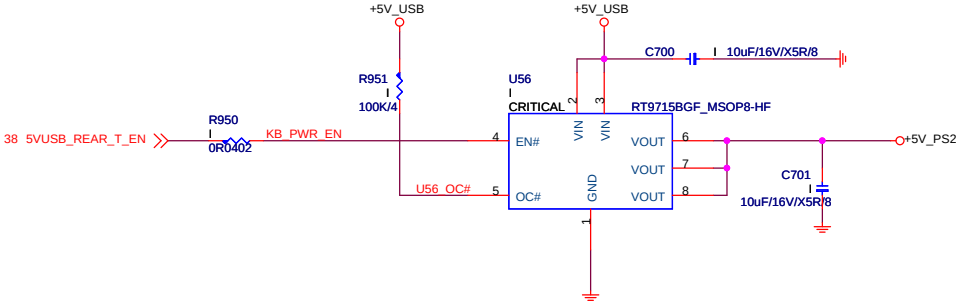
Latest modified date:
2015/02/13

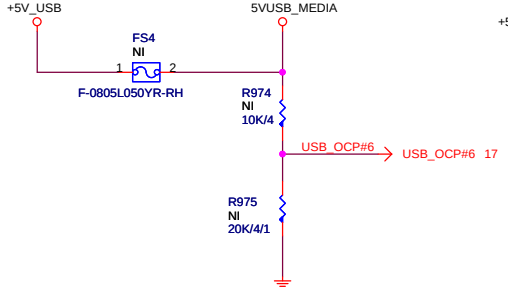
P/N:I36-9715B02-R11

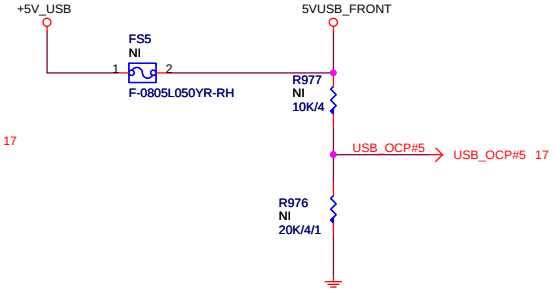


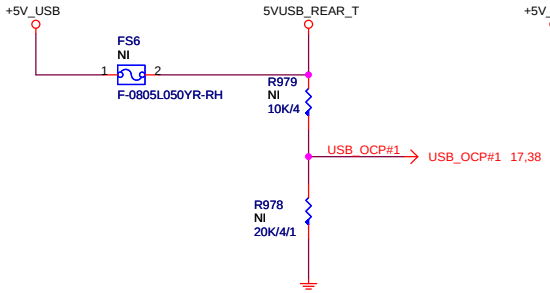
P/N:I36-7534Q02-U33

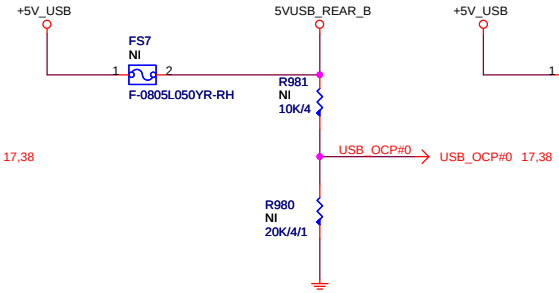


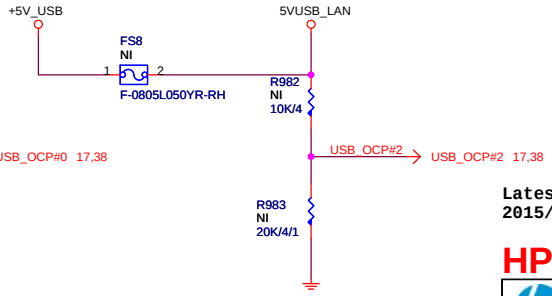












Project	
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Maranello	V
Barchetta	V

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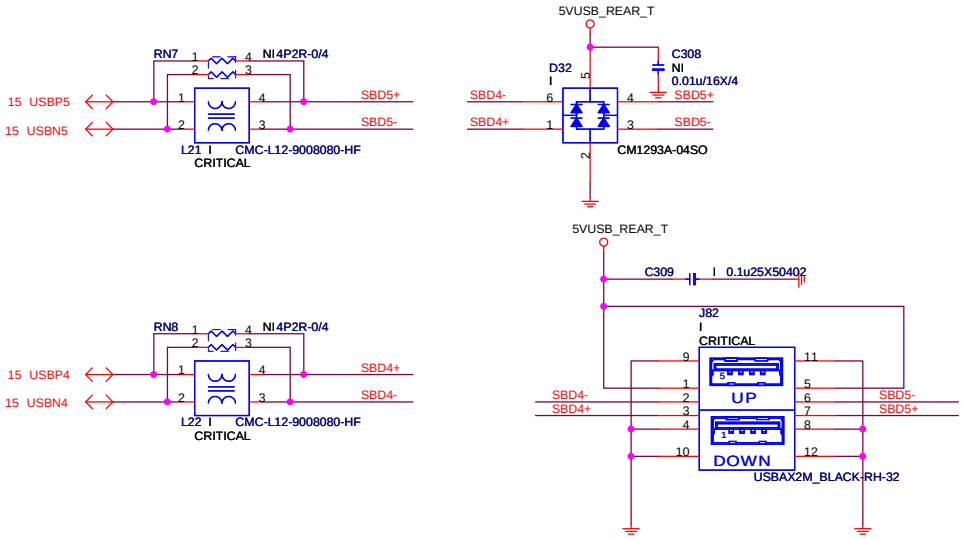
Rear USB Connnector For USB Port 4 / 5



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Project	
Berlinetta	V
Maranello	V
Barchetta	

Latest modified date:
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Title: USB2.0

Size: Custom | Document Number: HP SCH P/N: 793306-000(MSI MS-7957) | Rev: X4

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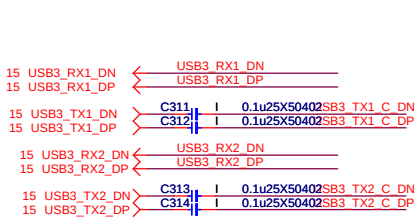
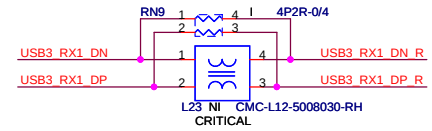
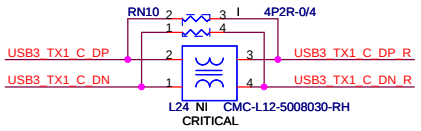
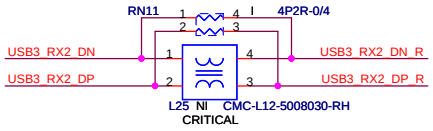
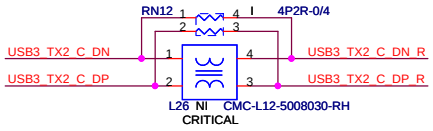
REAR USB3.0 Connnector

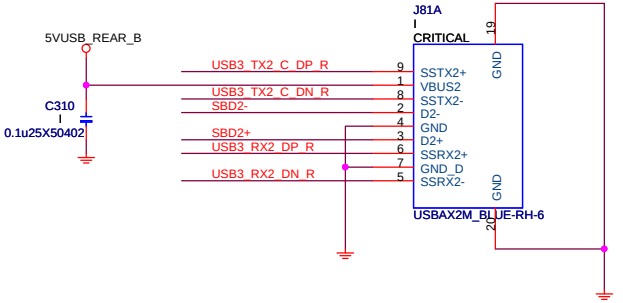


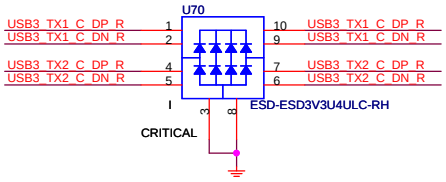


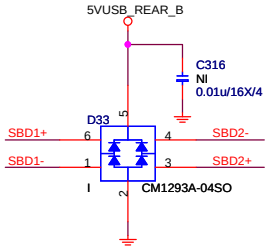


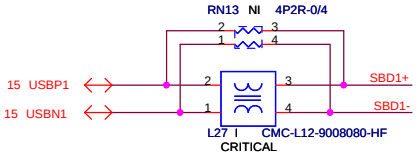


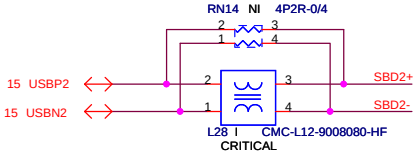


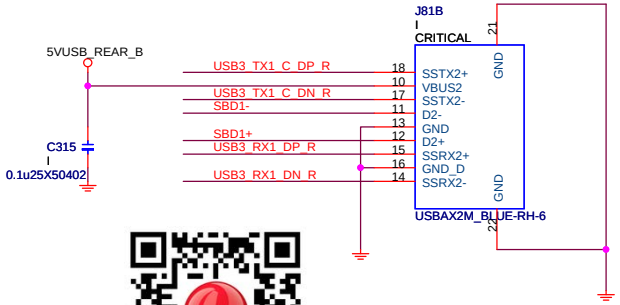


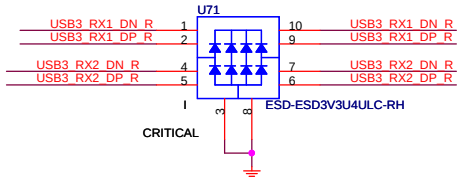




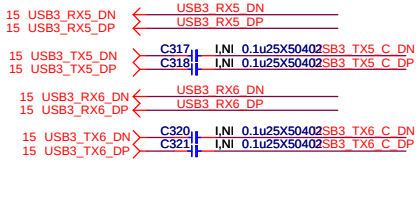


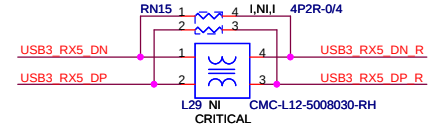


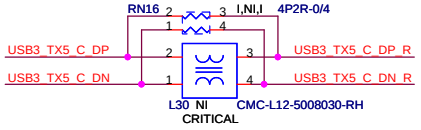


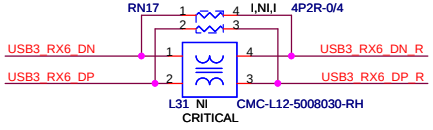


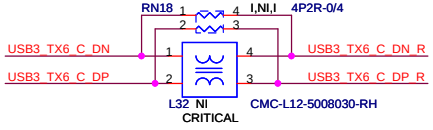
REAR USB3.0 Connnector

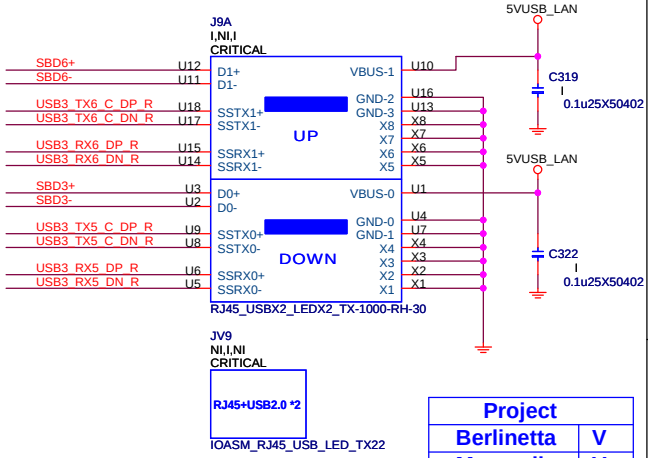


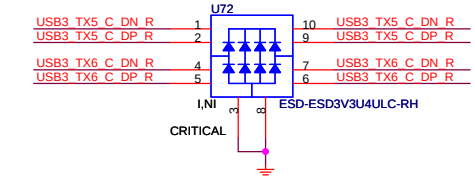


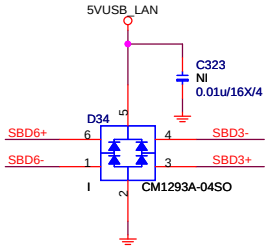


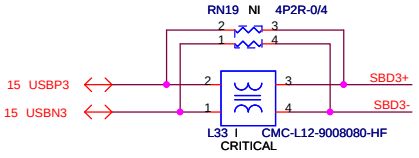


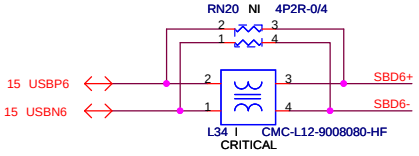


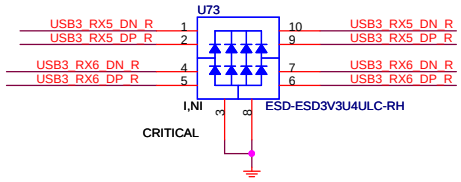












Latest modified date:
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Project	
Berlinetta	V
Maranello	V
Barchetta	

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Title	Rear USB 3.0
Size: Custom	Document Number: HP SCH P/N: 793306-000(MSI MS-7957)
Rev	X4
Date: Friday, June 05, 2015	Sheet 41 of 65

FRONT USB3.0 Connnector

15 USB3_RX3_DN → USB3_RX3_DN
15 USB3_RX3_DP → USB3_RX3_DP
15 USB3_TX3_DN — C325 0.1u25X50402 — USB3_TX3_C_DN
15 USB3_TX3_DP — C326 0.1u25X50402 — USB3_TX3_C_DP
15 USB3_RX4_DN → USB3_RX4_DN
15 USB3_RX4_DP → USB3_RX4_DP
15 USB3_TX4_DN — C327 0.1u25X50402 — USB3_TX4_C_DN
15 USB3_TX4_DP — C328 0.1u25X50402 — USB3_TX4_C_DP

5VUSB_FRONT
C329 NI 0.01u/16X/4
D35 CM1293A-04SO
SBD8+ SBD8- SBD9- SBD9+

15 USBN8 / 15 USBP8 — RN25 NI 4P2R-0/4 — SBD8- / SBD8+
L39 CMC-L12-9008080-HF CRITICAL

U74 ESD-ESD3V3U4ULC-RH CRITICAL
USB3_RX3_DP_R / USB3_RX3_DN_R
USB3_RX4_DP_R / USB3_RX4_DN_R

U75 ESD-ESD3V3U4ULC-RH CRITICAL
USB3_TX4_C_DN_R / USB3_TX4_C_DP_R
USB3_TX3_C_DN_R / USB3_TX3_C_DP_R

RN21 4P2R-0/4 — USB3_TX4_C_DN → USB3_TX4_C_DN_R; USB3_TX4_C_DP → USB3_TX4_C_DP_R
CRITICAL L35 NI CMC-L12-5008030-RH

RN22 4P2R-0/4 — USB3_TX3_C_DN → USB3_TX3_C_DN_R; USB3_TX3_C_DP → USB3_TX3_C_DP_R
CRITICAL L36 NI CMC-L12-5008030-RH

RN23 4P2R-0/4 — USB3_RX4_DN → USB3_RX4_DN_R; USB3_RX4_DP → USB3_RX4_DP_R
CRITICAL L37 NI CMC-L12-5008030-RH

RN24 4P2R-0/4 — USB3_RX3_DN → USB3_RX3_DN_R; USB3_RX3_DP → USB3_RX3_DP_R
L38 NI CMC-L12-5008030-RH CRITICAL

RN26 NI 4P2R-0/4 — 15 USBN9 / 15 USBP9 — SBD9- / SBD9+
L40 CMC-L12-9008080-HF CRITICAL

5VUSB_FRONT
C324 0.1u25X50402
C330 0.1u25X50402

P26 BH2X10[20]-2PITCH_BLUE-RH-2 2X10_CONNECTOR

19	VBUS2		
18	RX2-	X1	USB3_RX3_DN_R
17	RX2+		USB3_RX3_DP_R
16	GND		
15	TX2-		USB3_TX3_C_DN_R
14	TX2+		USB3_TX3_C_DP_R
13	GND		
12	D2-		SBD9-
11	D2+		SBD9+
1	VBUS1		5VUSB_FRONT
2	RX1-		USB3_RX4_DN_R
3	RX1+		USB3_RX4_DP_R
4	GND		
5	TX1-		USB3_TX4_C_DN_R
6	TX1+		USB3_TX4_C_DP_R
7	GND		
8	D1-		SBD8-
9	D1+		SBD8+
10	DETECT#	X2	18 FRONT_USB_P26_DET#

N32-2101181-H06

MEDIA USB3.0 Connnector

15 USB3_RX8_DN → USB3_RX8_DN
15 USB3_RX8_DP → USB3_RX8_DP
15 USB3_TX8_DN — C331 I,NI 0.1u25X50402 — USB3_TX8_C_DN
15 USB3_TX8_DP — C332 I,NI 0.1u25X50402 — USB3_TX8_C_DP

5VUSB_MEDIA
C333 0.1u25X50402

P152 I,NI,NI H2X6M_BLACK-RH

1	SBD10-	2	USB3_RX8_DN_R
3	SBD10+	4	USB3_RX8_DP_R
5		6	
7		8	
9		10	
11	USB3_TX8_C_DP_R	12	USB3_TX8_C_DN_R

INT_USB_P152_DET# 18

PV152 NI,I,I H2X5_NP9-4

U76 I,NI ESD-ESD3V3U4ULC-RH CRITICAL
USB3_TX8_C_DP_R / USB3_TX8_C_DN_R
USB3_RX8_DP_R / USB3_RX8_DN_R

5VUSB_MEDIA
C334 NI 0.01u/16X/4
D36 CM1293A-04SO
SBD10+ SBD10-

RN27 I,NI,NI 4P2R-0/4 — USB3_RX8_DN → USB3_RX8_DN_R; USB3_RX8_DP → USB3_RX8_DP_R
L41 NI CMC-L12-5008030-RH CRITICAL

RN28 I,NI,NI 4P2R-0/4 — USB3_TX8_C_DN → USB3_TX8_C_DN_R; USB3_TX8_C_DP → USB3_TX8_C_DP_R
L42 NI CMC-L12-5008030-RH CRITICAL

RN30 NI 4P2R-0/4 — 15 USBP10 / 15 USBN10 — SBD10+ / SBD10-
L44 CMC-L12-9008080-HF CRITICAL

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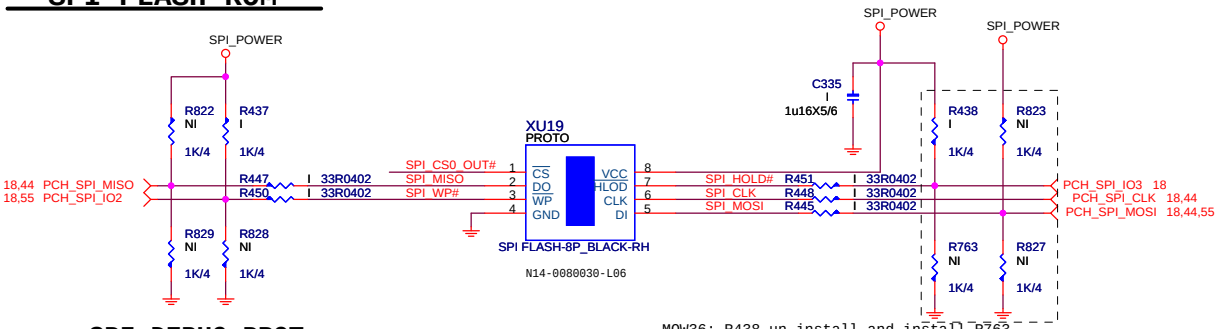
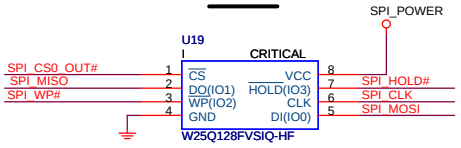
Sheet 42 of 65

SPI FLASH ROM



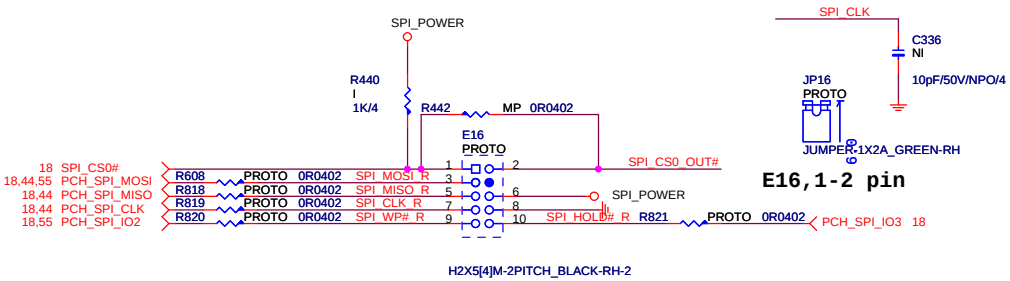
MOW36: R438 un-install and install R763
for Skylake PCH-H Pre ES1/ES1 and Pre ES2/ES2 sample.

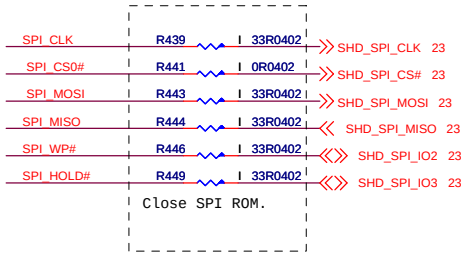
BIOS



M31-2512853-W03

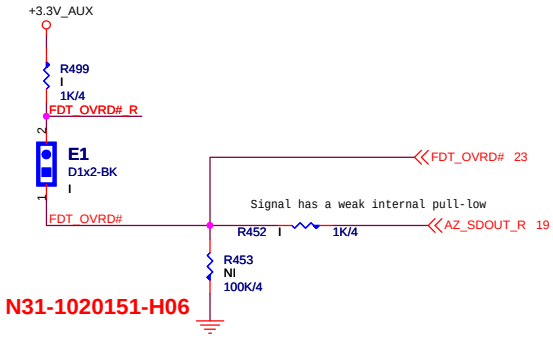
SPI DEBUG PROT





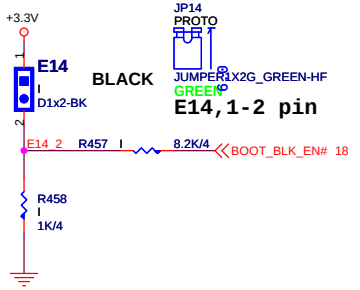
Flash Descriptor Override Header (ME_DIS)

FLASH DESCRIPTOR OVERRIDE



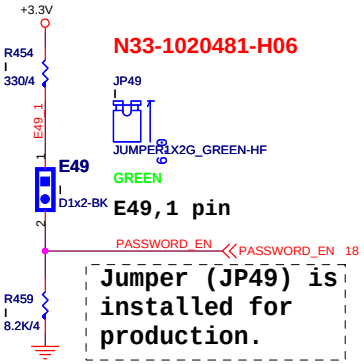
N31-1020151-H06

BOOT BLOCK WRITE JUMPER



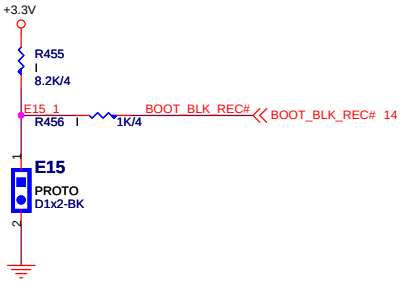
N33-1020271-H06

PASSWORD JUMPER



N33-1020481-H06

BOOT BLOCK RECOVERY HEADER



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Barchetta	V

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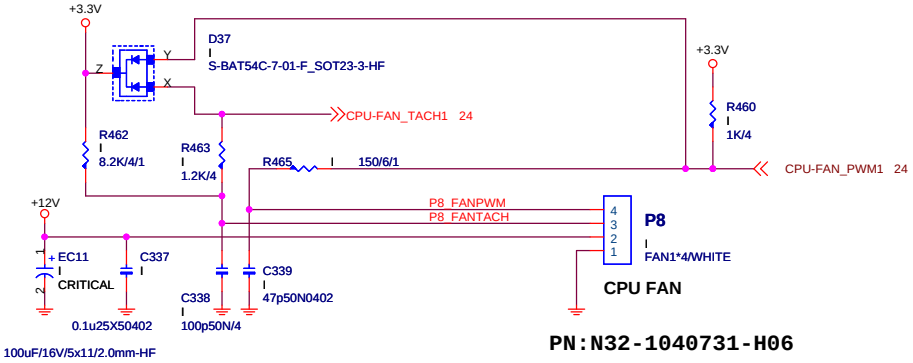
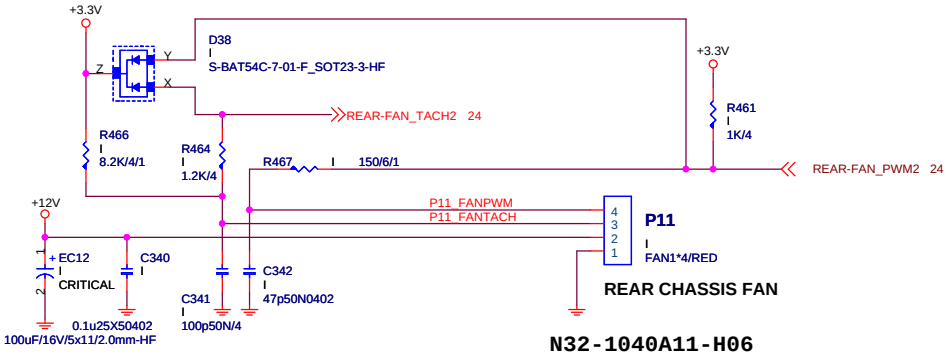
FAN BLOCK

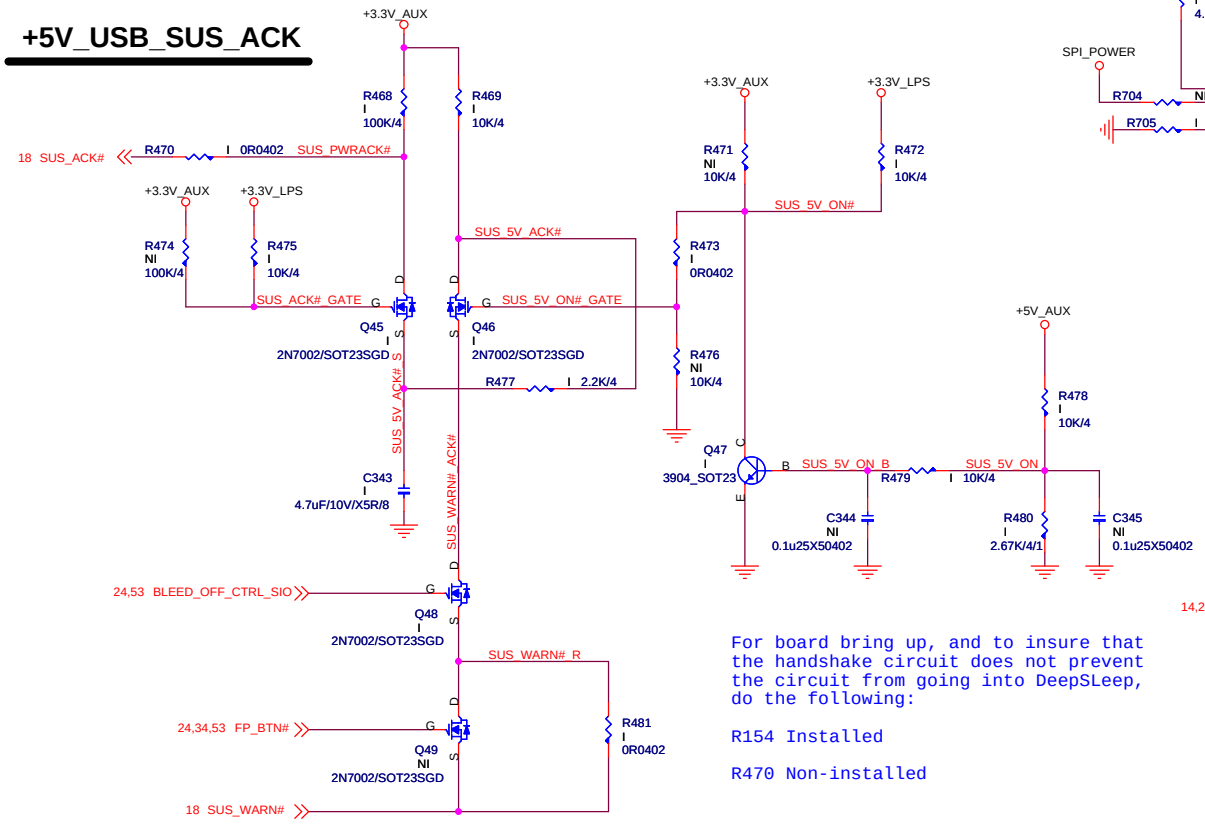


PN:N32-1040731-H06



N32-1040A11-H06

+5V_USB_SUS_ACK

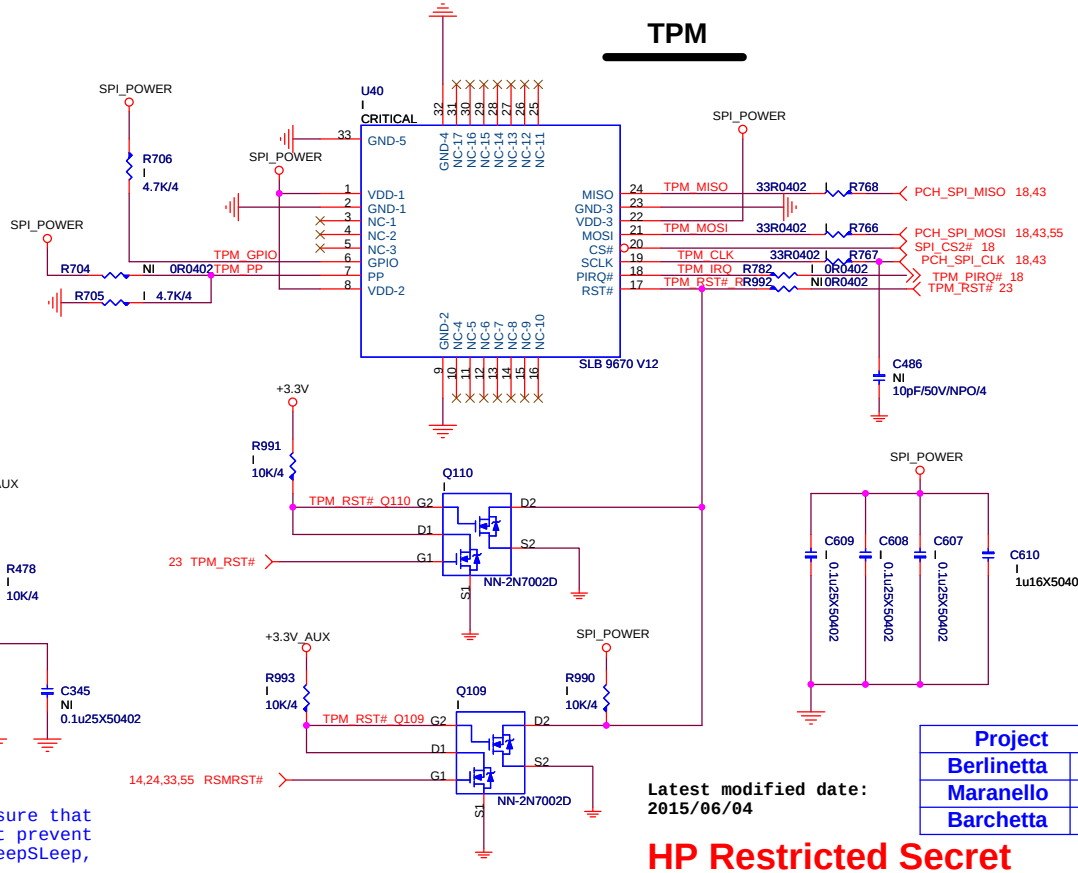


For board bring up, and to insure that the handshake circuit does not prevent the circuit from going into DeepSLeep, do the following:

R154 Installed

R470 Non-installed

TPM



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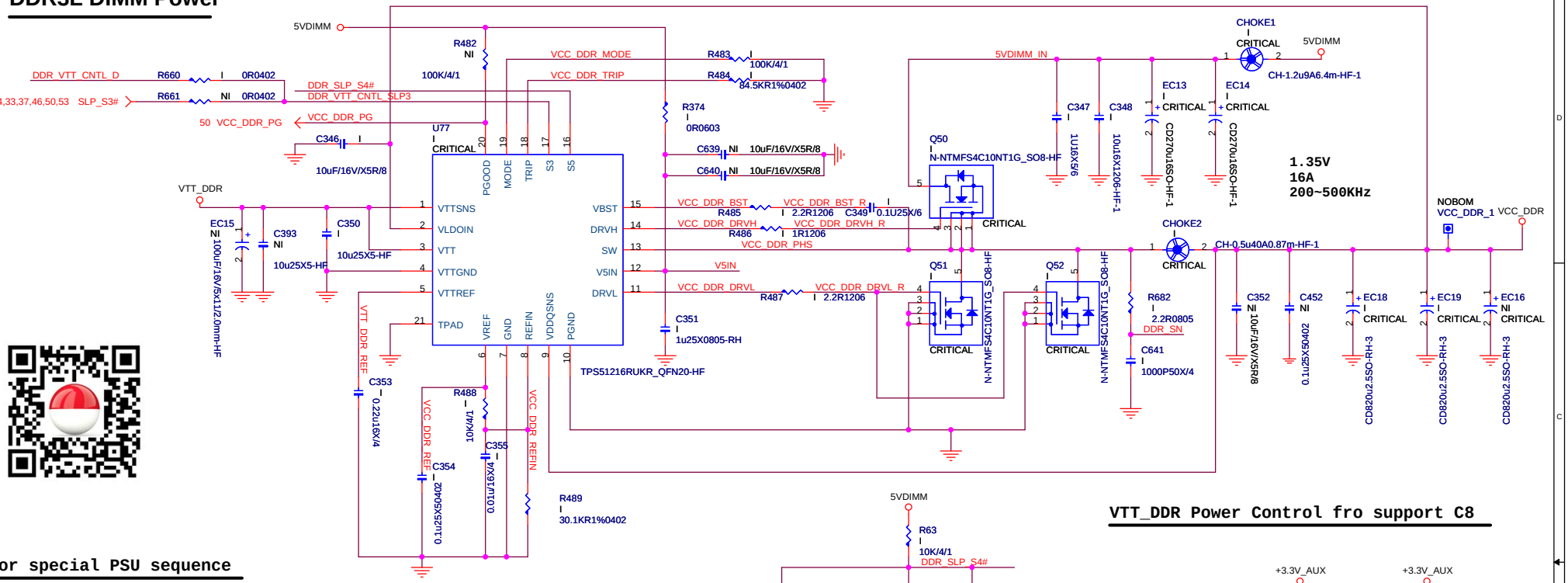
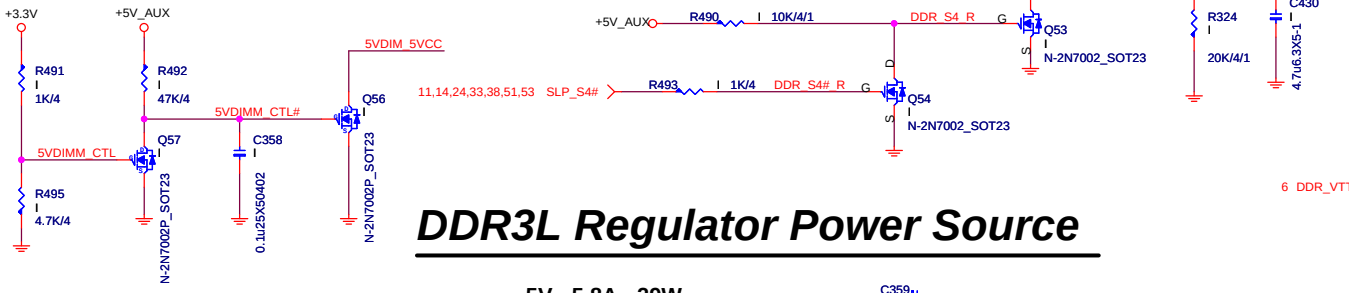
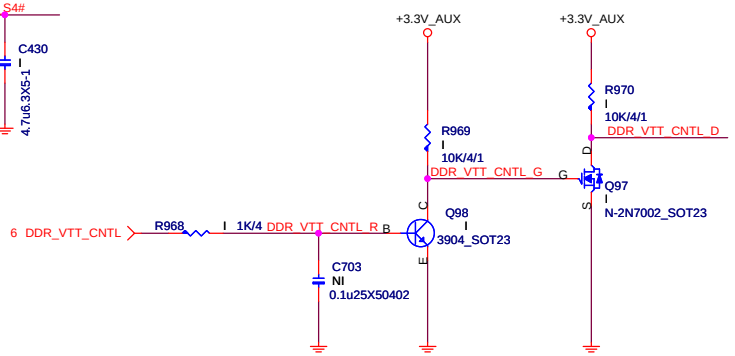
DDR3L DIMM Power



For special PSU sequence

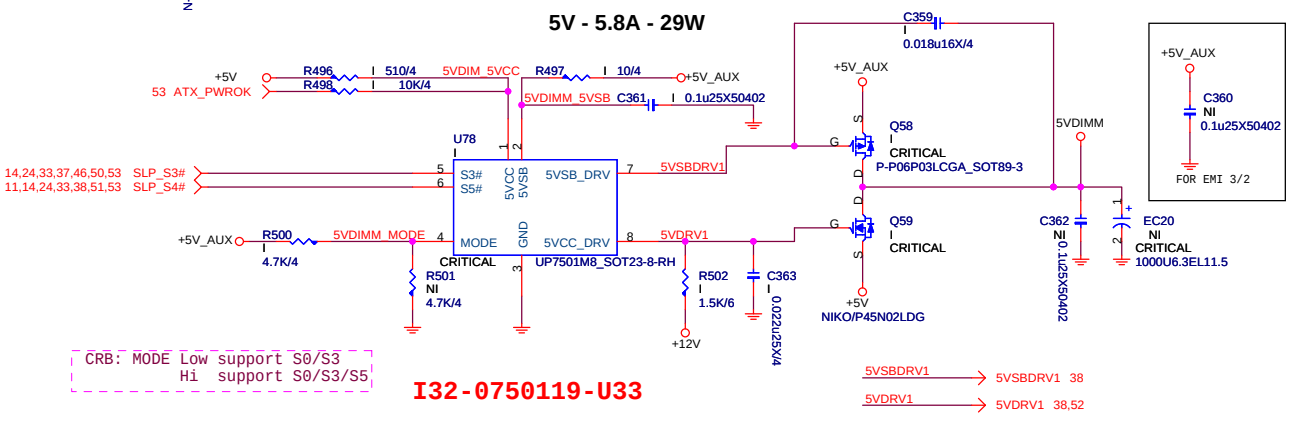


VTT_DDR Power Control fro support C8



DDR3L Regulator Power Source

5V - 5.8A - 29W



CRB: MODE Low support S0/S3
Hi support S0/S3/S5

I32-0750119-U33

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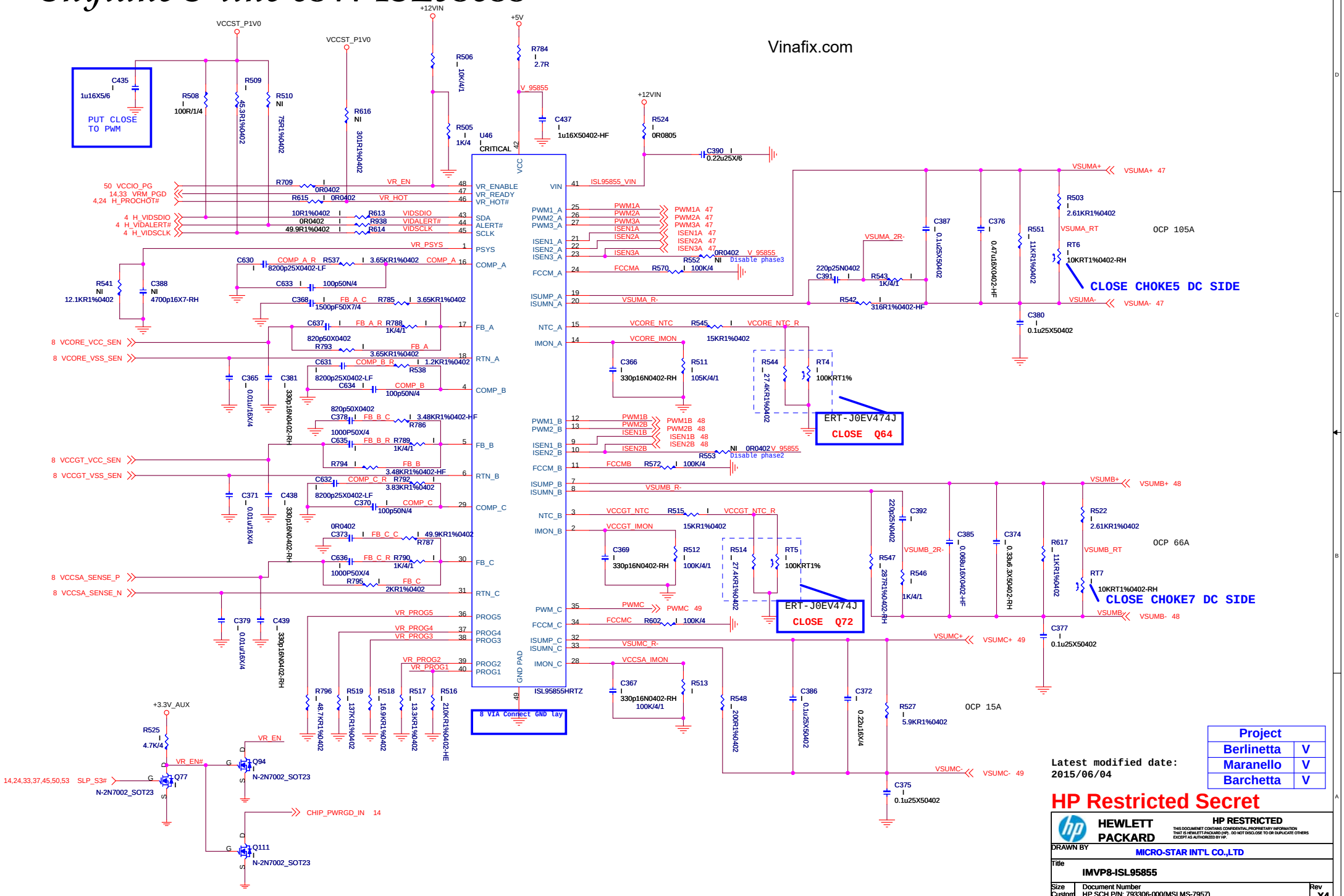
Skylake S-line 65W ISL95855



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Maranello	V
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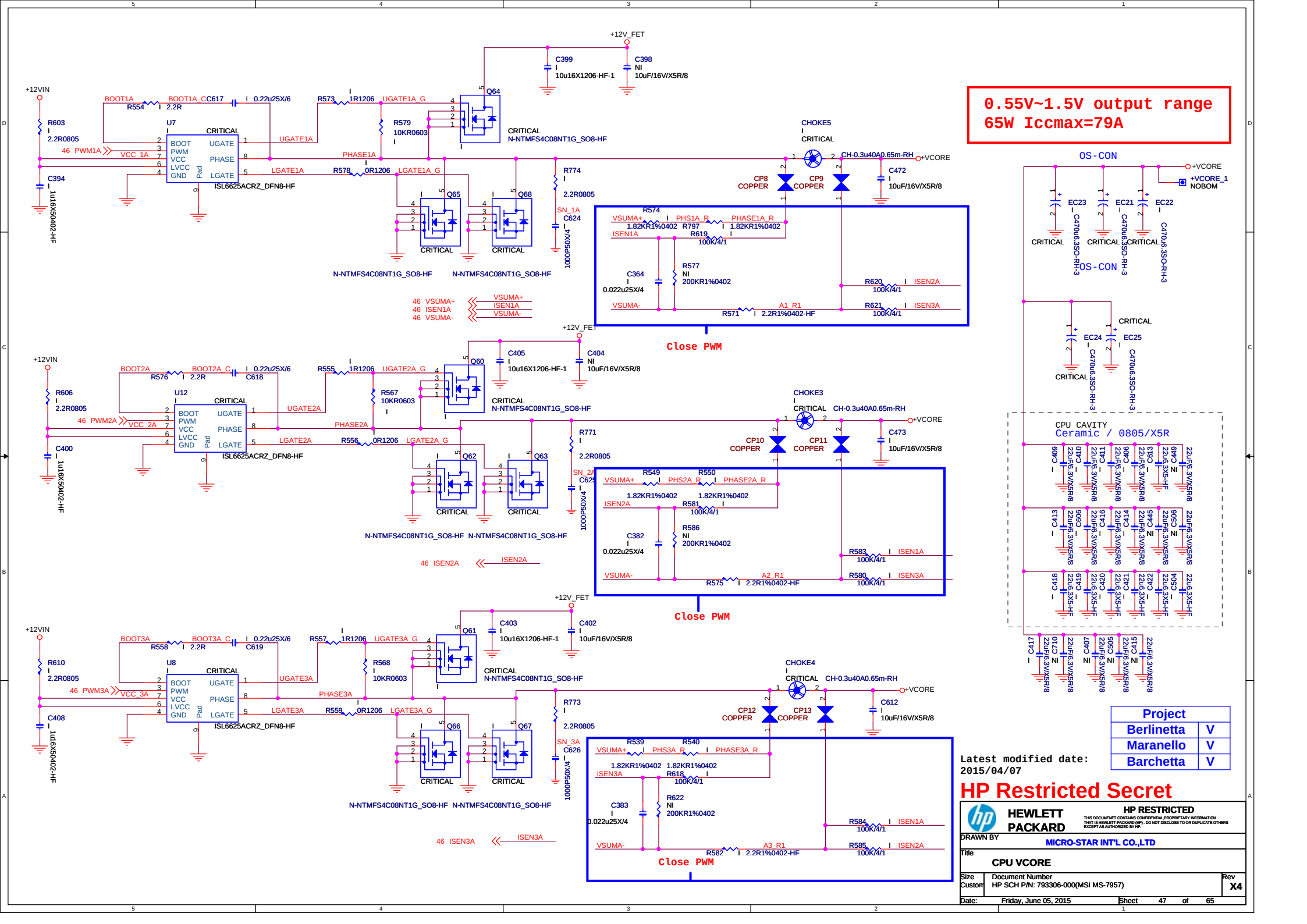
0.55V~1.5V output range
65W Iccmax=79A
+12V_FET
+12VIN
+VCORE
+VCORE_1
NOBOM
OS-CON
CPU CAVITY
Ceramic / 0805/X5R
Close PWM
Close PWM
Close PWM
U7
U12
U8
ISL6625ACRZ_DFN8-HF
N-NTMFS4C08NT1G_SO8-HF
CH-0.3u40A0.65m-RH
CHOKE5
CHOKE3
CHOKE4
CP8 COPPER
CP9 COPPER
CP10 COPPER
CP11 COPPER
CP12 COPPER
CP13 COPPER
46 PWM1A
46 PWM2A
46 PWM3A
46 VSUMA+
46 ISEN1A
46 VSUMA-
46 ISEN2A
46 ISEN3A
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CPU VCORE
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Custom
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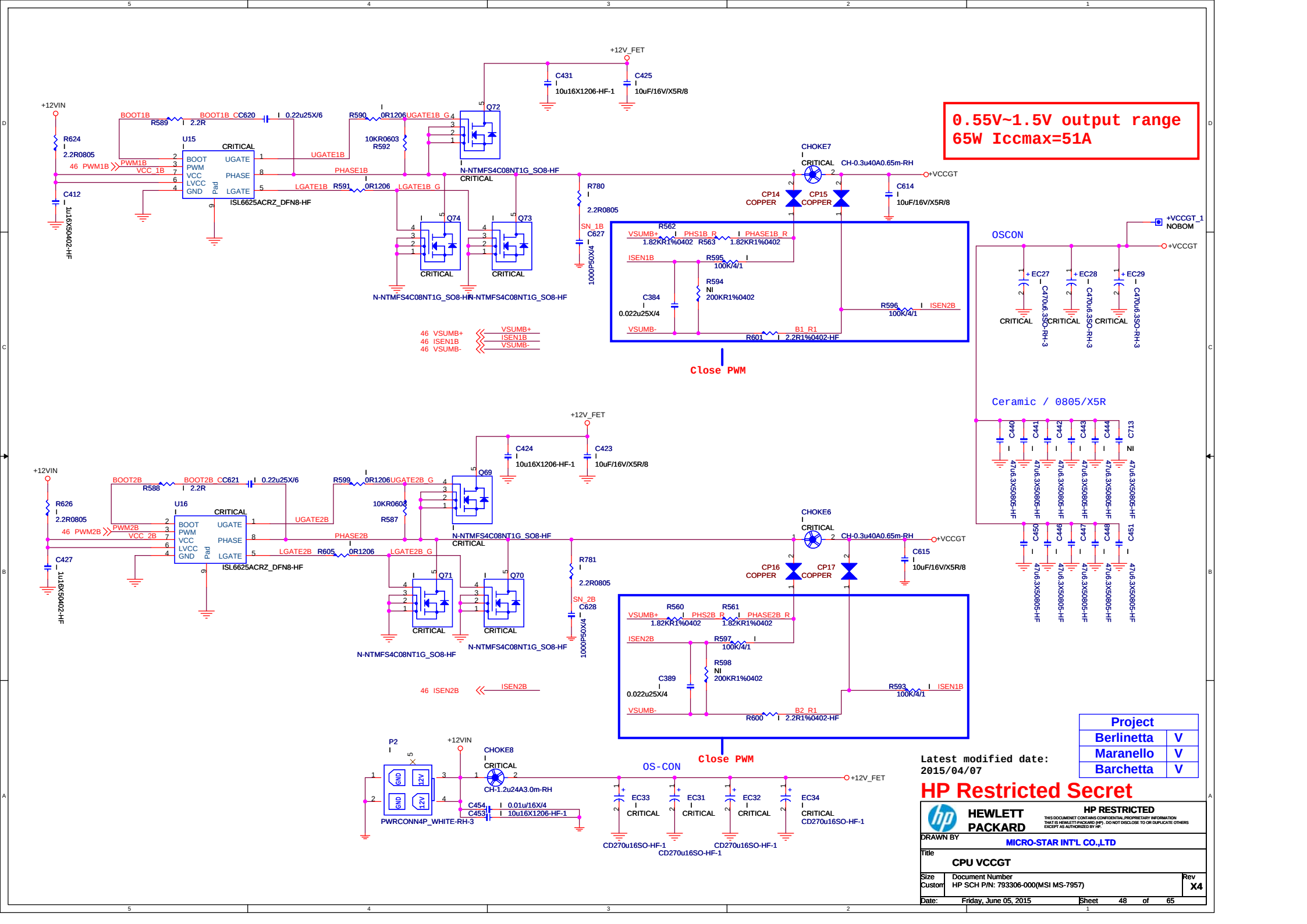
0.55V~1.5V output range
65W Iccmax=51A
+12V_FET
C431
10u16X1206-HF-1
C425
10uF/16V/X5R/8
+12VIN
R624
2.2R0805
C412
1u16X50402-HF
BOOT1B
R589
2.2R
BOOT1B_CC620
0.22u25X/6
R590
0R1206
UGATE1B_G
Q72
U15
CRITICAL
BOOT
PWM
VCC
LVCC
GND
UGATE
PHASE
LGATE
Pad
ISL6625ACRZ_DFN8-HF
46 PWM1B
PWM1B
VCC_1B
UGATE1B
PHASE1B
LGATE1B
R591
0R1206
LGATE1B_G
10KR0603
R592
Q74
Q73
CRITICAL
N-NTMFS4C08NT1G_SO8-HF
R780
2.2R0805
SN_1B
C627
1000P50X/4
CHOKE7
CH-0.3u40A0.65m-RH
+VCCGT
CP14
COPPER
CP15
COPPER
C614
10uF/16V/X5R/8
R562
VSUMB+
PHS1B_R
PHASE1B_R
1.82KR1%0402
R563
1.82KR1%0402
ISEN1B
R595
100K/4/1
R594
NI
200KR1%0402
C384
0.022u25X/4
VSUMB-
R596
100K/4/1
ISEN2B
B1_R1
R601
2.2R1%0402-HF
46 VSUMB+
46 ISEN1B
46 VSUMB-
Close PWM
OSCON
+VCCGT_1
NOBOM
+VCCGT
+ EC27
+ EC28
+ EC29
C470u6.3SO-RH-3
CRITICAL
Ceramic / 0805/X5R
C440
C441
C442
C443
C444
C713
NI
47u6.3X50805-HF
+12V_FET
C424
10u16X1206-HF-1
C423
10uF/16V/X5R/8
+12VIN
R626
2.2R0805
C427
1u16X50402-HF
BOOT2B
R588
2.2R
BOOT2B_CC621
0.22u25X/6
R599
0R1206
UGATE2B_G
Q69
U16
CRITICAL
ISL6625ACRZ_DFN8-HF
46 PWM2B
PWM2B
VCC_2B
UGATE2B
PHASE2B
LGATE2B
R605
0R1206
LGATE2B_G
10KR0603
R587
Q71
Q70
CRITICAL
N-NTMFS4C08NT1G_SO8-HF
R781
2.2R0805
SN_2B
C628
1000P50X/4
CHOKE6
CH-0.3u40A0.65m-RH
+VCCGT
CP16
COPPER
CP17
COPPER
C615
10uF/16V/X5R/8
R560
R561
VSUMB+
PHS2B_R
PHASE2B_R
1.82KR1%0402
1.82KR1%0402
ISEN2B
R597
100K/4/1
R598
NI
200KR1%0402
C389
0.022u25X/4
VSUMB-
R593
100K/4/1
ISEN1B
B2_R1
R600
2.2R1%0402-HF
46 ISEN2B
Close PWM
P2
PWRCONN4P_WHITE-RH-3
GND
12V
+12VIN
CHOKE8
CH-1.2u24A3.0m-RH
C454
0.01u/16X/4
C453
10u16X1206-HF-1
OS-CON
EC33
EC31
EC32
EC34
CRITICAL
CD270u16SO-HF-1
+12V_FET
Project
Berlinetta V
Maranello V
Barchetta V
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CPU VCCGT
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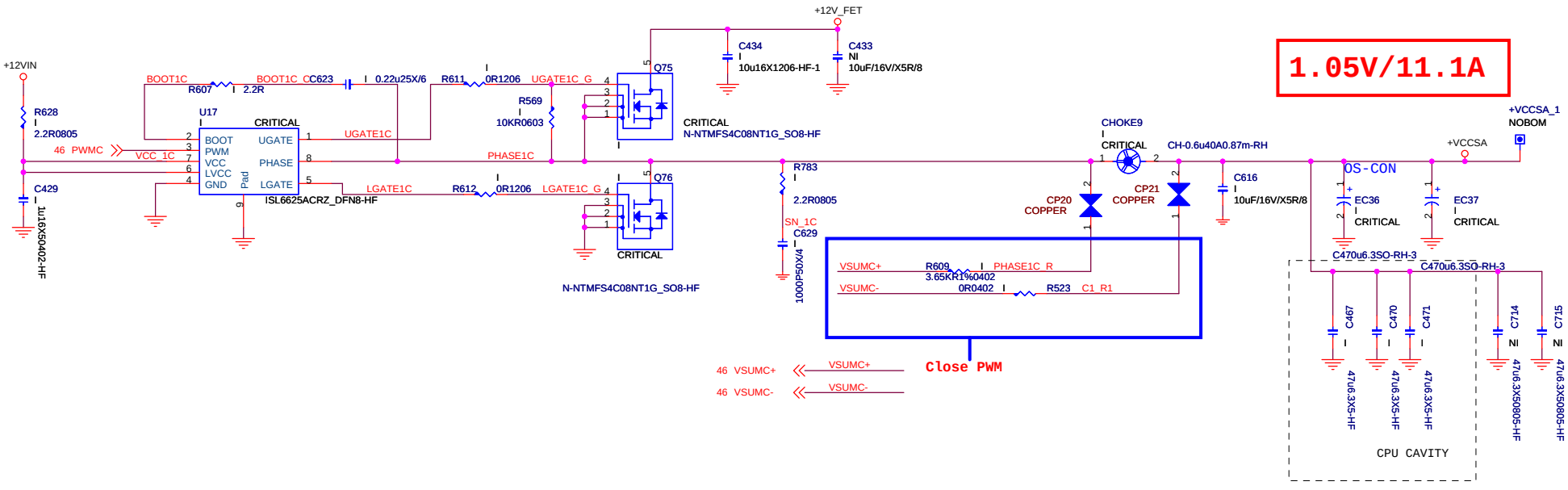

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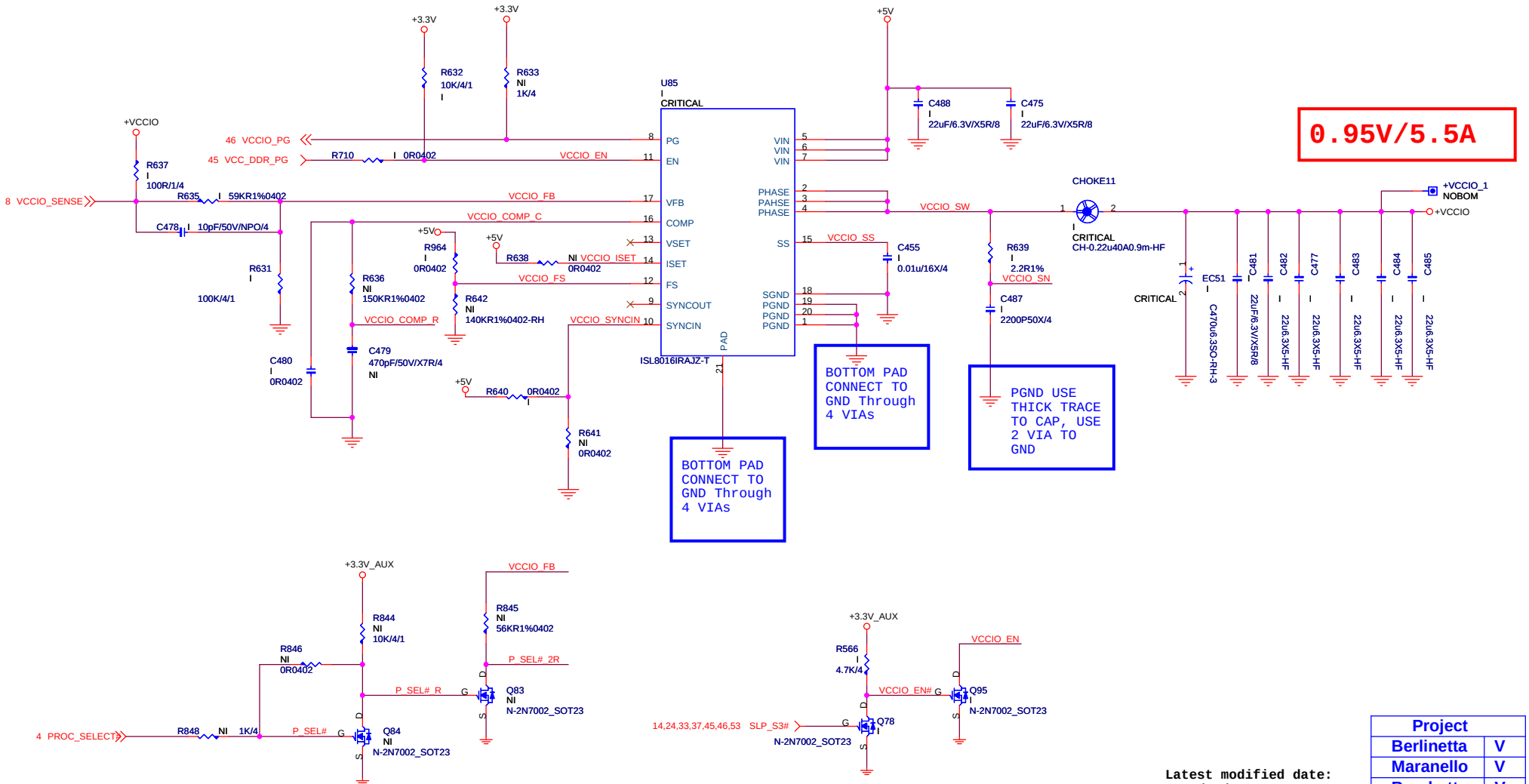
SKYLAKE VCCIO POWER CKT



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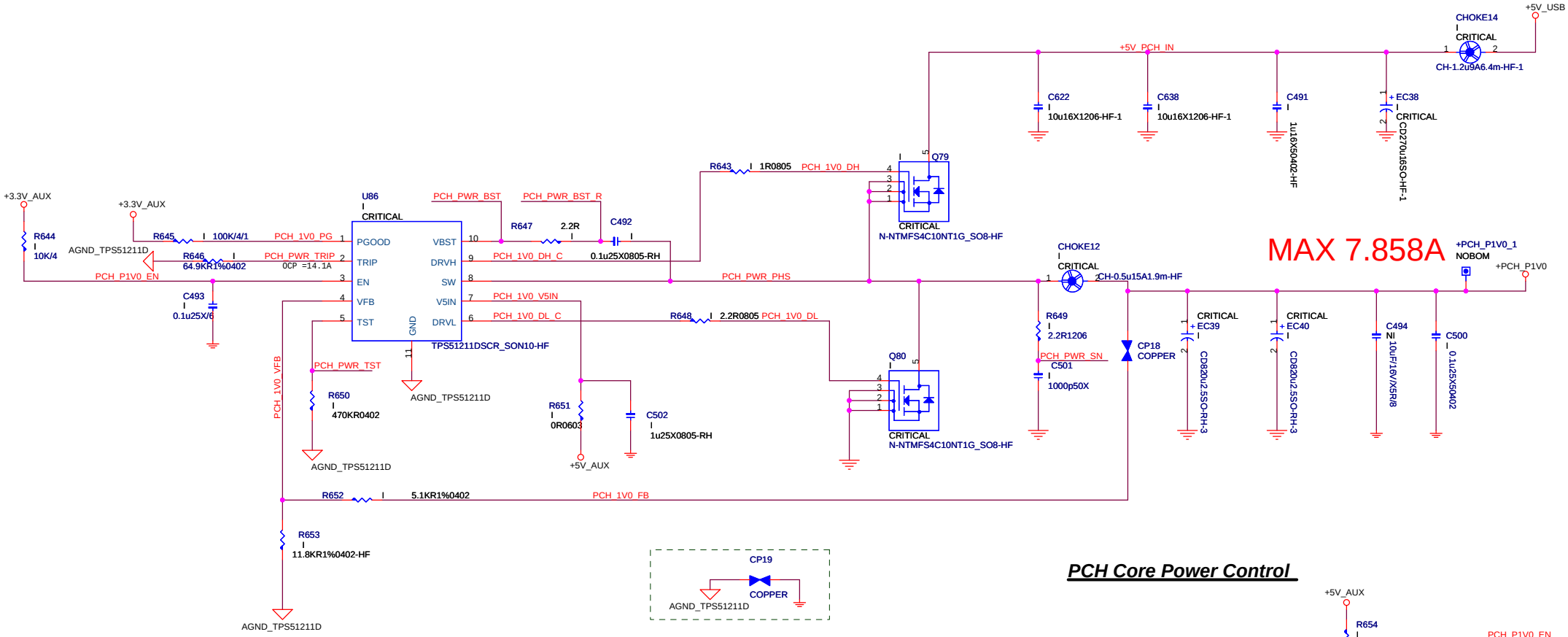

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Barchetta	V

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Rev	X4
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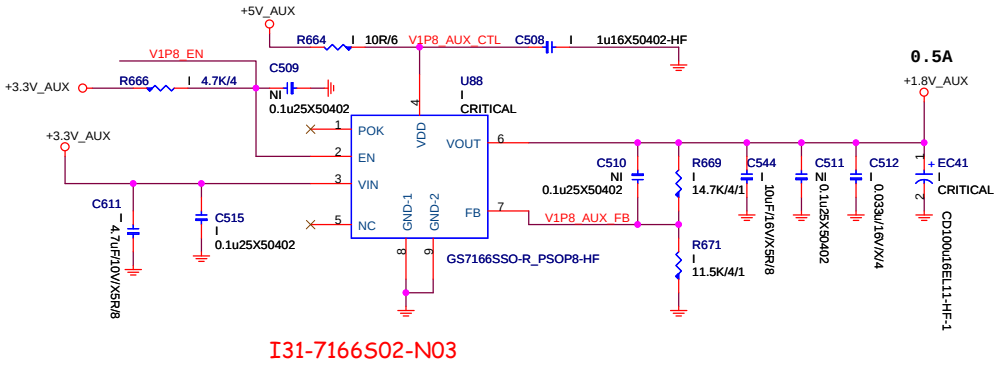
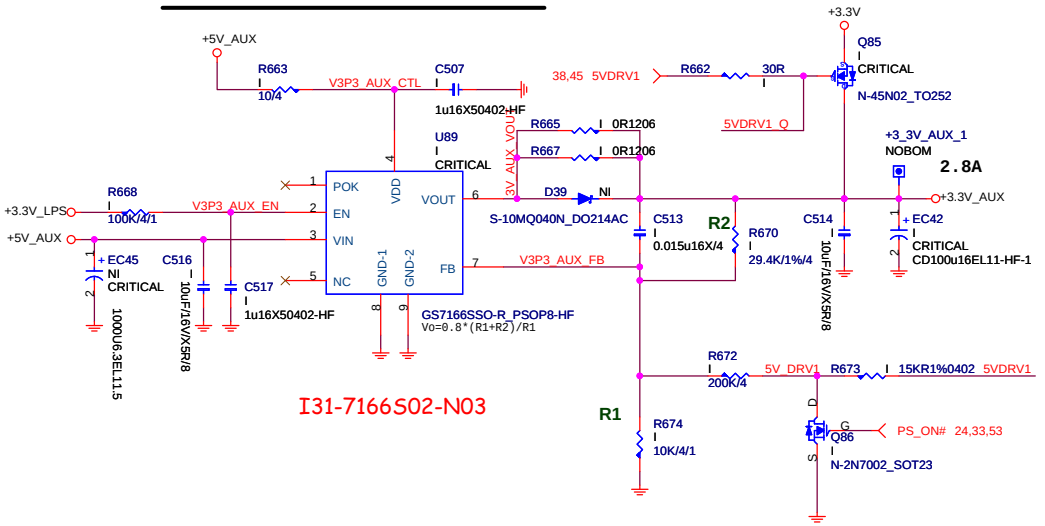
1.8V_AUX Power

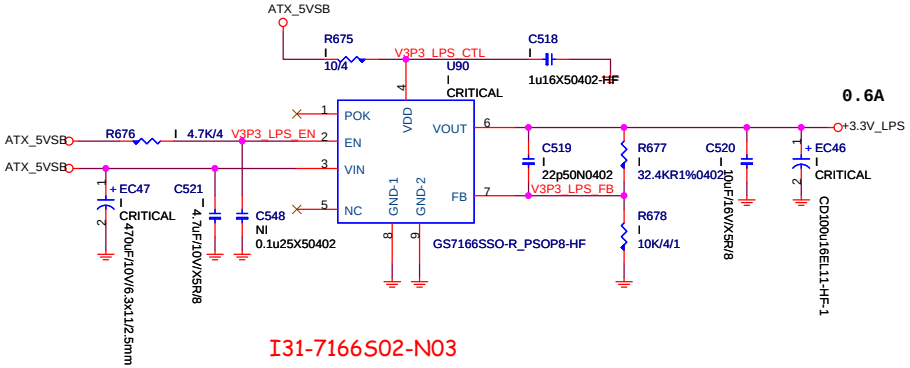


I31-7166S02-N03

3V Standby Power



I31-7166S02-N03



I31-7166S02-N03

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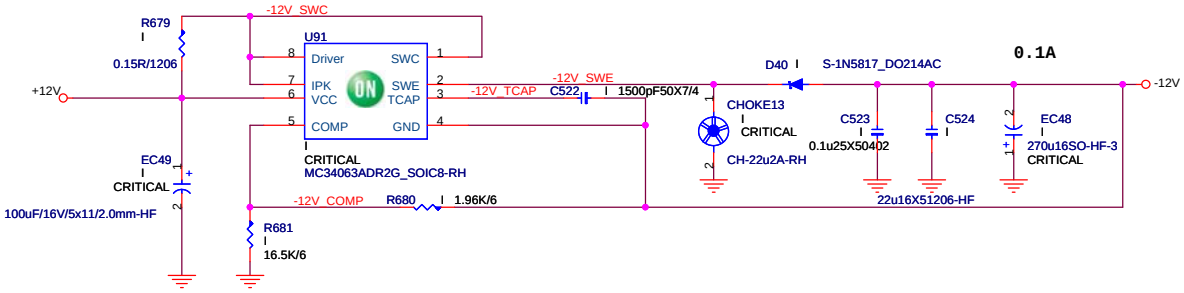
-12V POWER



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Project	
Berlinetta	V
Maranello	V
Barchetta	V

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Title	-12V/+3.3V_AUX/+1.8V_AUX
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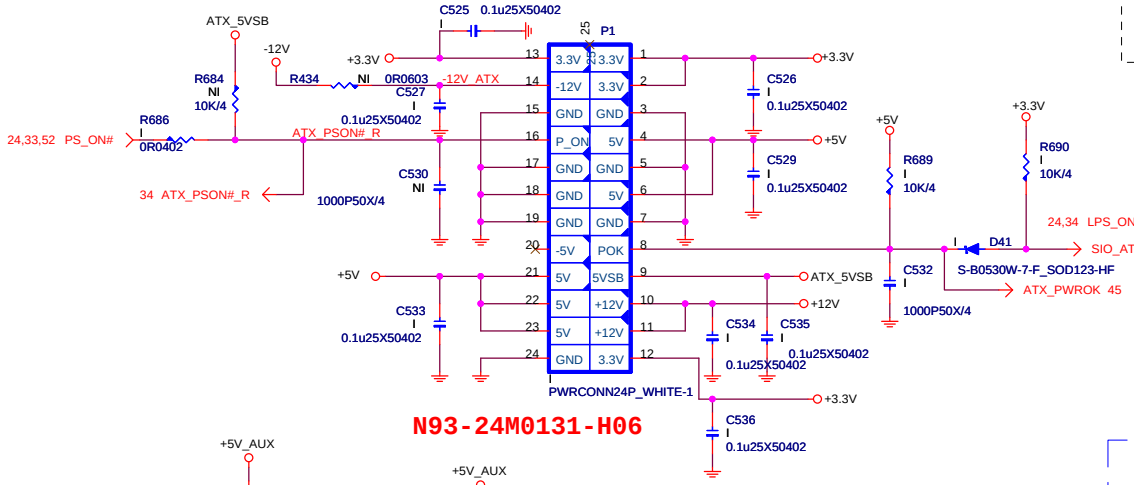
Date: Friday, June 05, 2015	Sheet 52 of 65

ATX Power Connector / Front Panel / LED/DSW

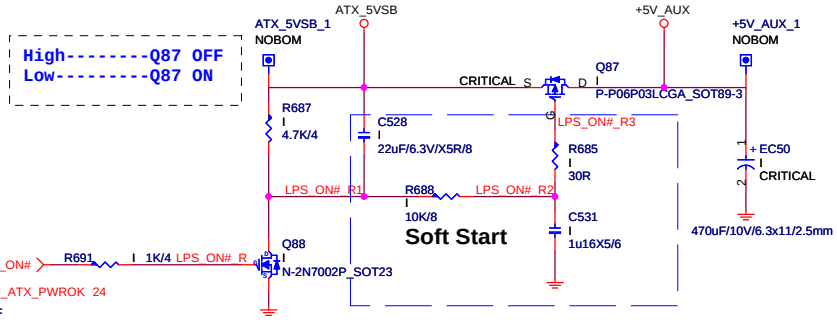
ATX CONNECTOR

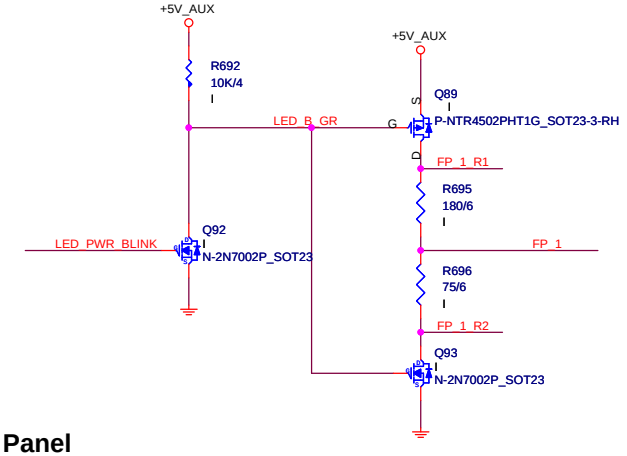


N93-24M0131-H06

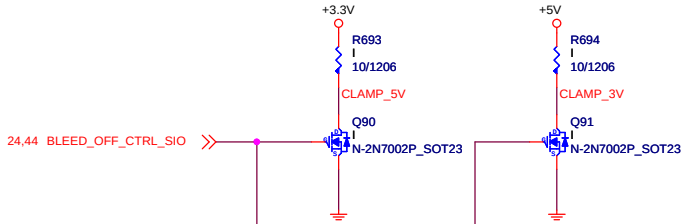
+5V_AUX Power Switch

Trace Width 80mils.



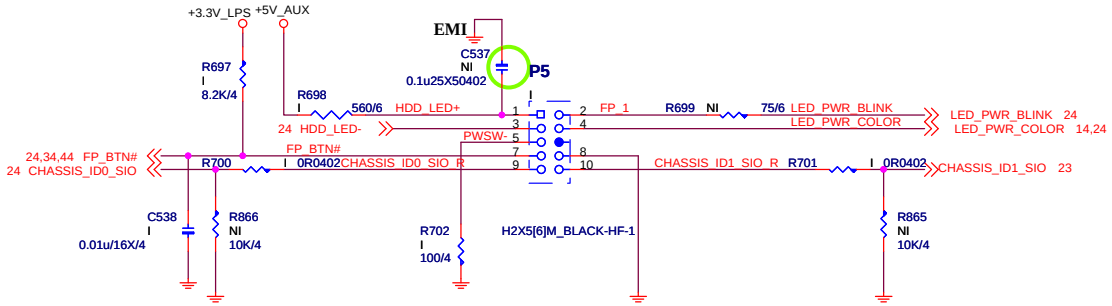


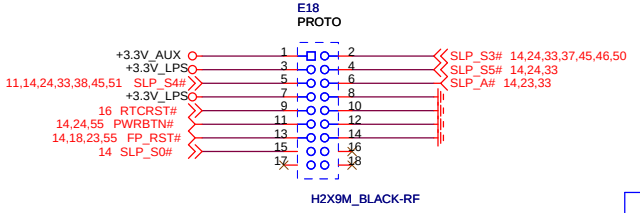
BLEED-OFF CIRCUIT



Front Panel

PN:N31-2051641-H06





Project	
Berlinetta	V
Maranello	V
Barchetta	V

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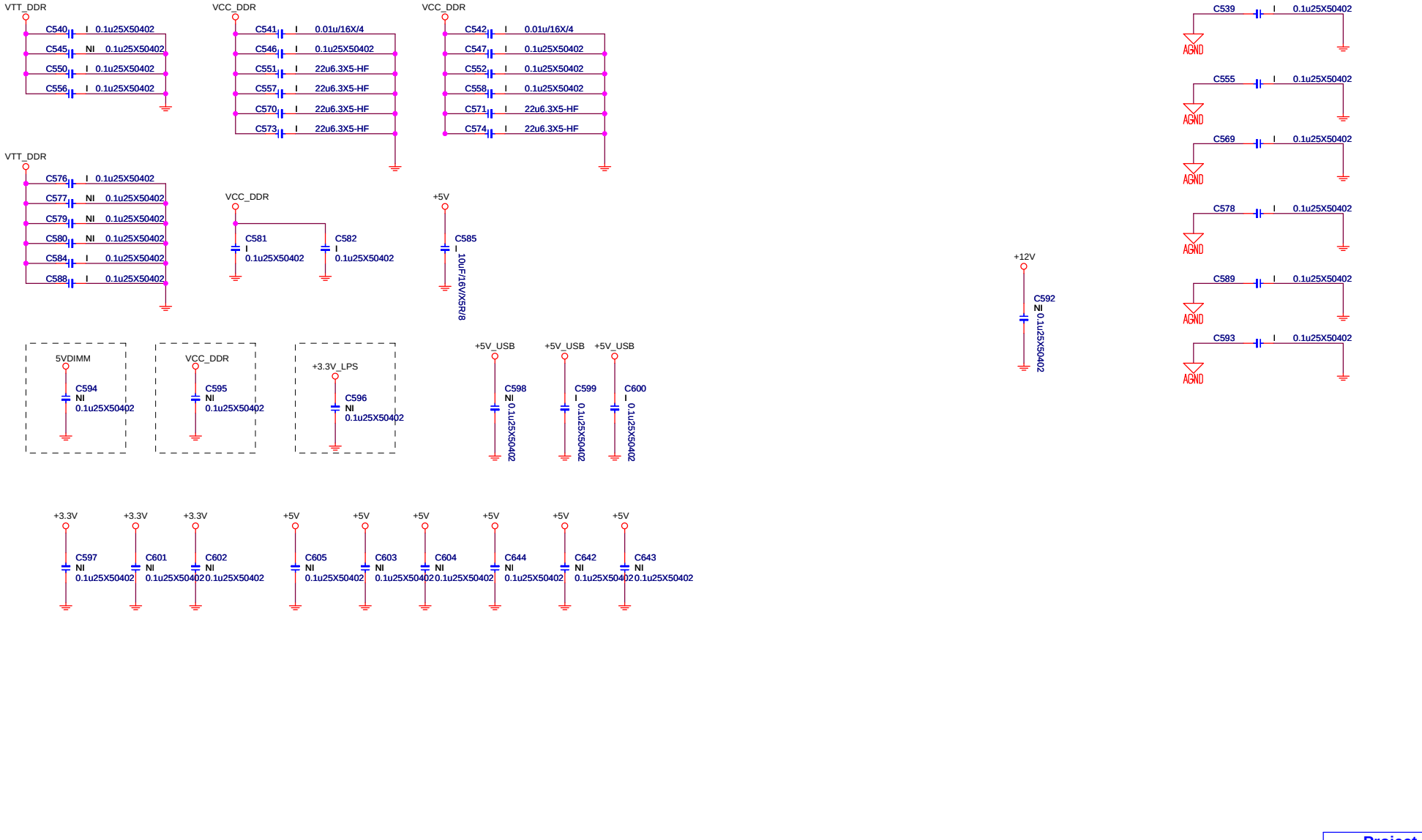
EMI CAPs



Project	
Berlinetta	V
Maranello	V
Barchetta	

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Title: EMI cap

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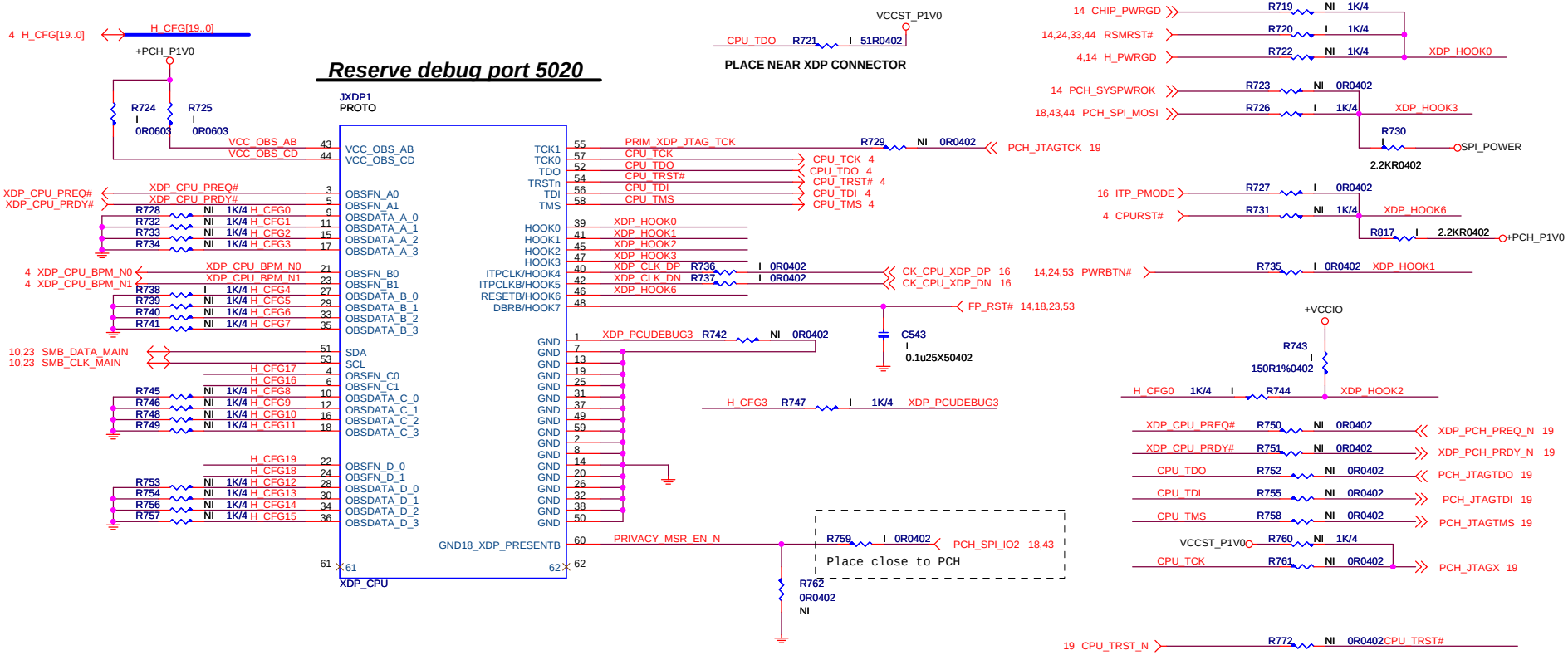
Date: Friday, June 05, 2015 Sheet 54 of 65



Project	
Berlinetta	V
Maranello	V
Barchetta	V

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2015/01/06

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Title	CPU/PCH/DMI XDP
Size: Custom	Document Number: HP SCH P/N: 793306-000(MSI MS-7957)
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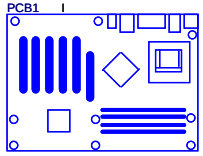
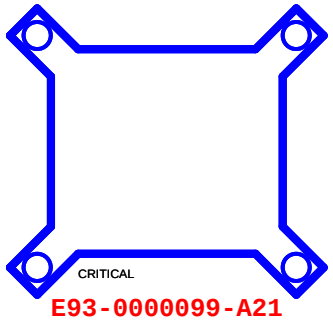
Manual Parts

PCB1 I



CRITICAL PCB1

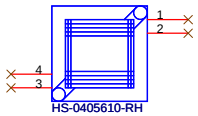
XU1_X1
I
E93-0000099-A21



CRITICAL

E93-0000099-A21
AVL:E22-B009010-C22

U4_X1
NI



HS-0405610-RH
CRITICAL

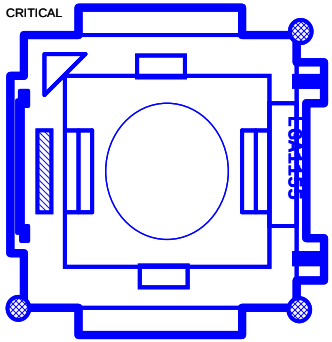
U4_X1_1
I

U4_X1_2
I

UV4
NI,I,I
CRITICAL

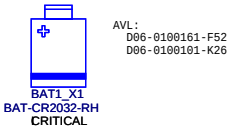
INTEL H110

XU1_X2
CPU SOCKET I
CRITICAL



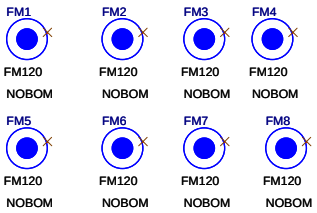
E21-AC71010-L06
AVL:E21-7826010-F02

Simulation

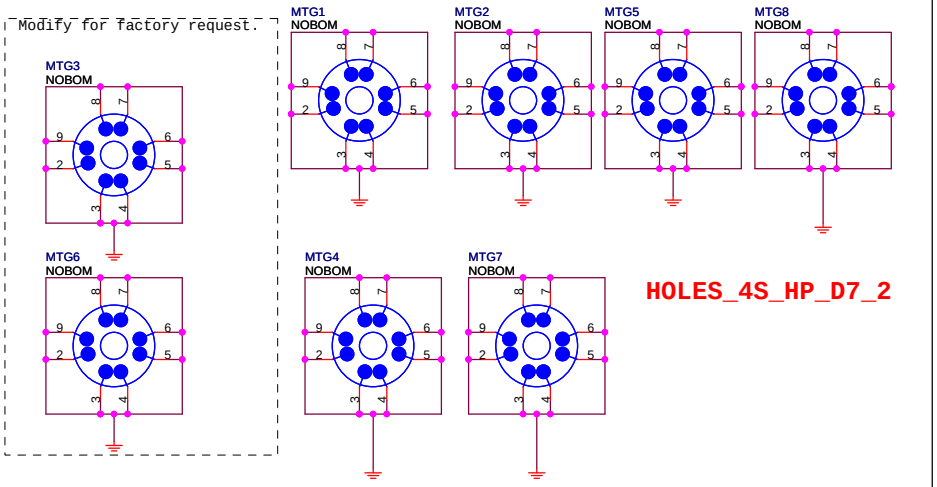


D06-0100101-P01

Optics Orientation Holes



Mounting Holes



HOLES_4S_HP_D7_2

Latest modified date:
2015/04/22

Project	
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Maranello	V
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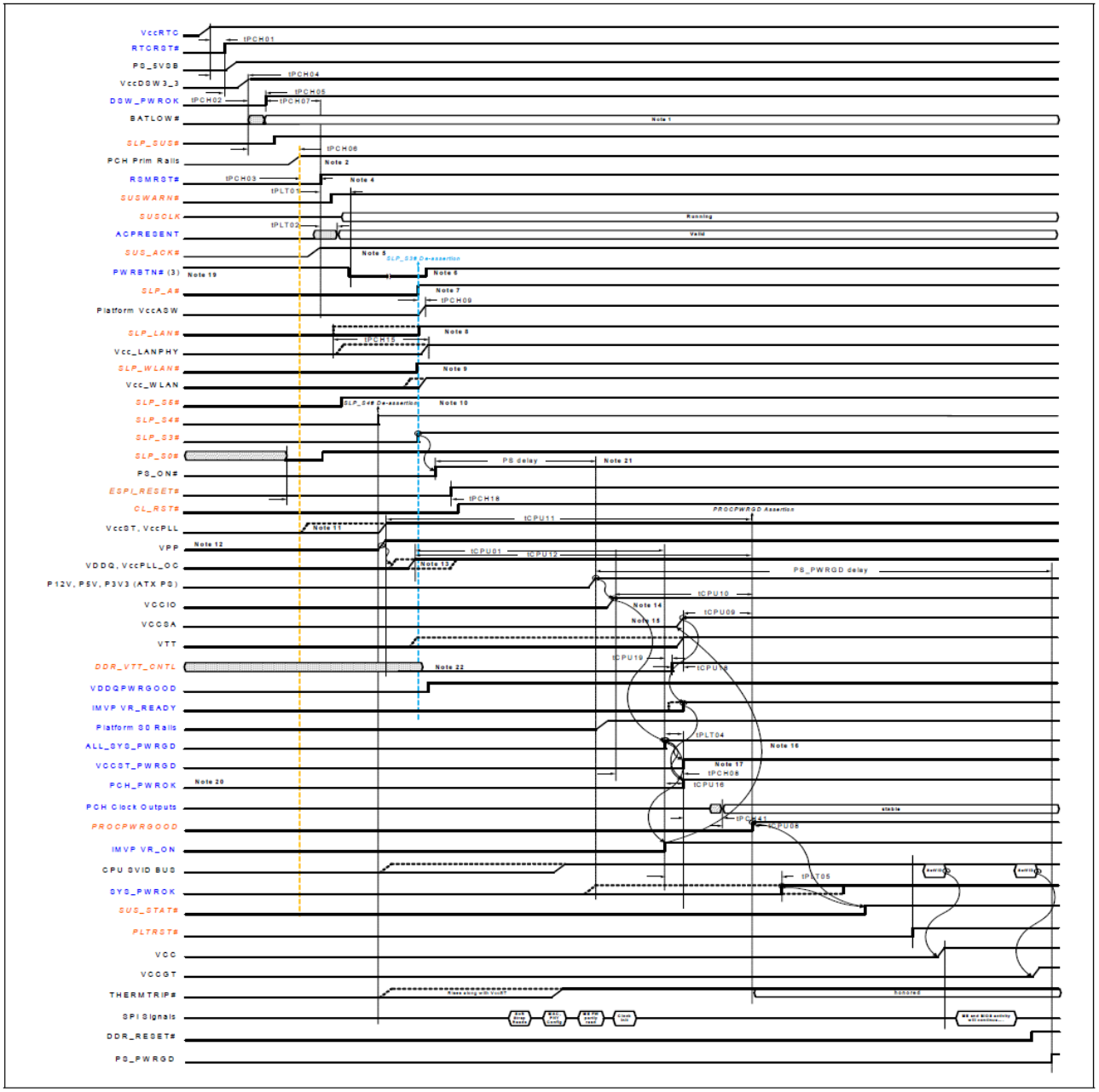

G3-S5

ATX_5VSB
+3.3V_LPS
SLP_SUS#
LPS_ON#
+5V_AUX
+3.3V_AUX/+1.8V_AUX
+PCH_P1V0
RSMRST#

S5-S0

PWBTIN#
PWBTOUT#
SLP_S5/S4/S3
PSON#
+12V/+5V/+3.3V
VCC_DDR
+VCCIO
+VCCP
SYS_PWROK
CHIP_PWRGD
H_PWRGD
PLTRST#

Project	
Berlinetta	V
Maranello	V
Barchetta	V

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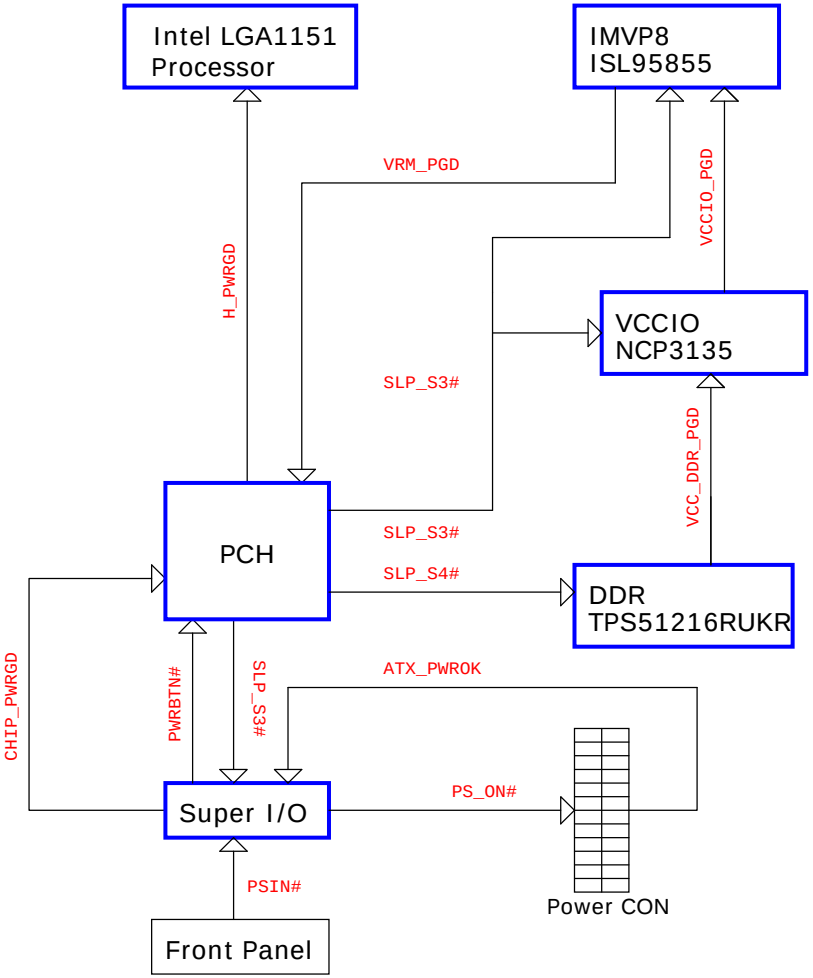
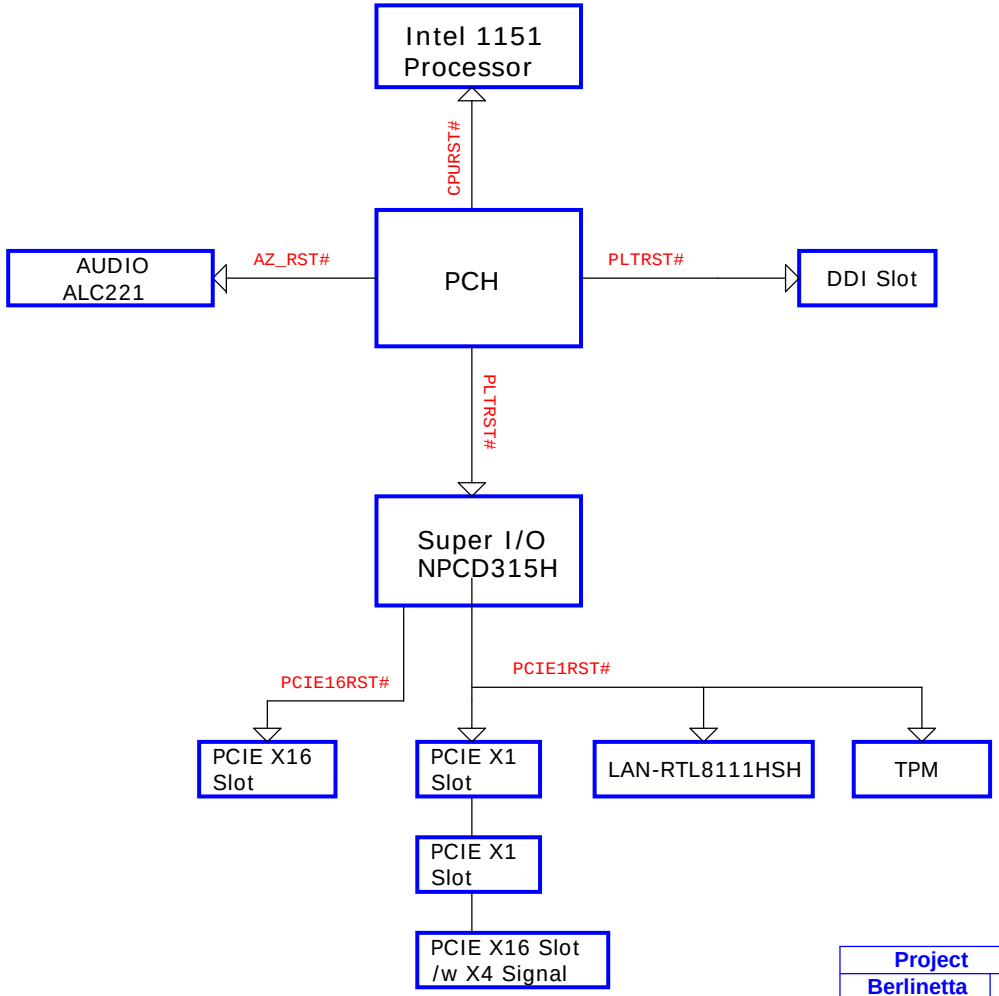
PWROK MAP



RESET MAP



Project	
Berlinetta	V
Maranello	V
Barchetta	

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Title: **Pwrok/Reset**

Size	Document Number	Rev
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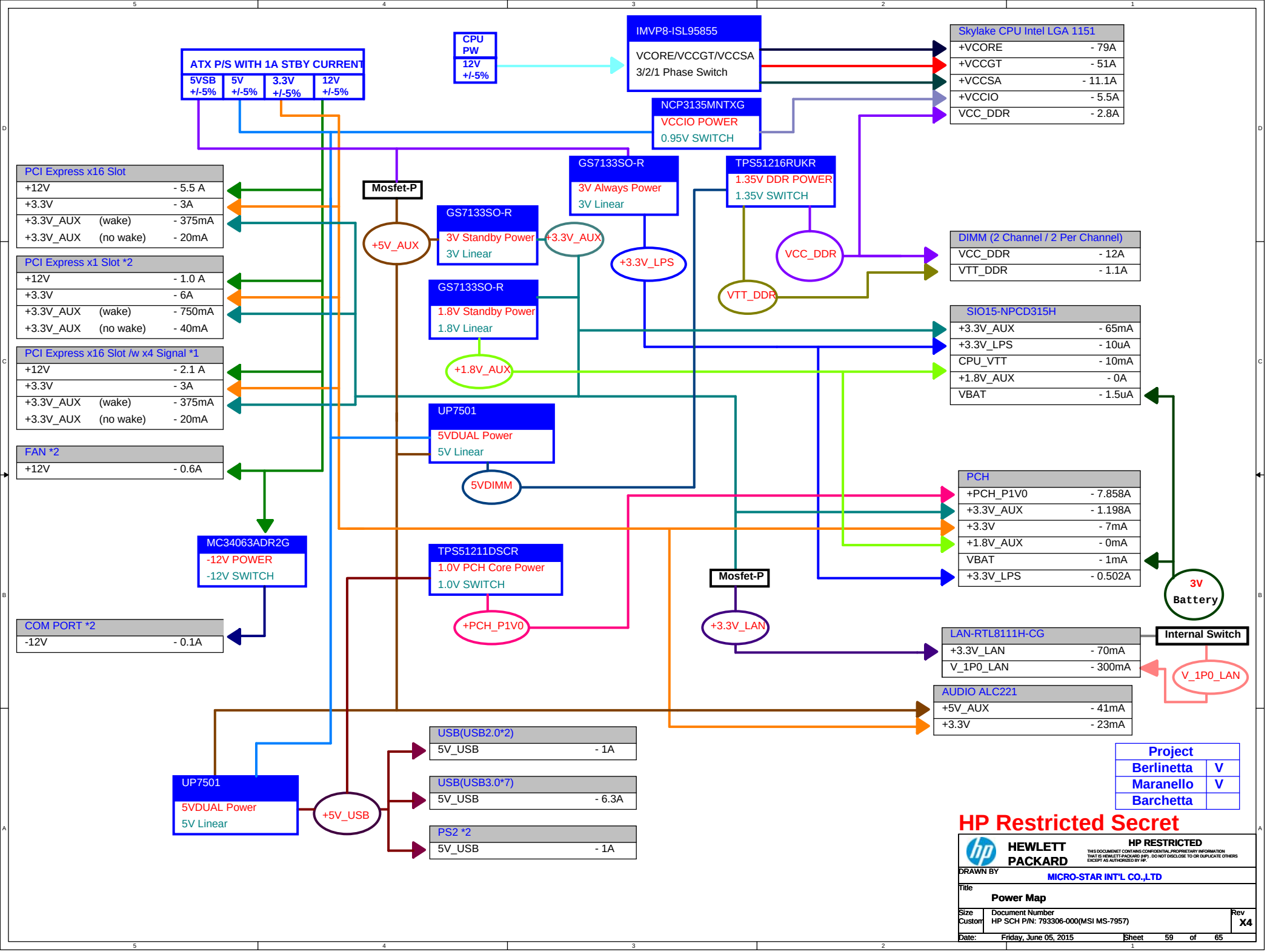
ATX P/S WITH 1A STBY CURRENT
5VSB +/-5%
5V +/-5%
3.3V +/-5%
12V +/-5%
CPU PW
12V +/-5%
IMVP8-ISL95855
VCORE/VCCGT/VCCSA
3/2/1 Phase Switch
Skylake CPU Intel LGA 1151
+VCORE - 79A
+VCCGT - 51A
+VCCSA - 11.1A
+VCCIO - 5.5A
VCC_DDR - 2.8A
NCP3135MNTXG
VCCIO POWER
0.95V SWITCH
PCI Express x16 Slot
+12V - 5.5 A
+3.3V - 3A
+3.3V_AUX (wake) - 375mA
+3.3V_AUX (no wake) - 20mA
PCI Express x1 Slot *2
+12V - 1.0 A
+3.3V - 6A
+3.3V_AUX (wake) - 750mA
+3.3V_AUX (no wake) - 40mA
PCI Express x16 Slot /w x4 Signal *1
+12V - 2.1 A
+3.3V - 3A
+3.3V_AUX (wake) - 375mA
+3.3V_AUX (no wake) - 20mA
FAN *2
+12V - 0.6A
COM PORT *2
-12V - 0.1A
Mosfet-P
+5V_AUX
GS7133SO-R
3V Standby Power
3V Linear
+3.3V_AUX
GS7133SO-R
3V Always Power
3V Linear
+3.3V_LPS
TPS51216RUKR
1.35V DDR POWER
1.35V SWITCH
VCC_DDR
VTT_DDR
DIMM (2 Channel / 2 Per Channel)
VCC_DDR - 12A
VTT_DDR - 1.1A
GS7133SO-R
1.8V Standby Power
1.8V Linear
+1.8V_AUX
SIO15-NPCD315H
+3.3V_AUX - 65mA
+3.3V_LPS - 10uA
CPU_VTT - 10mA
+1.8V_AUX - 0A
VBAT - 1.5uA
UP7501
5VDUAL Power
5V Linear
5VDIMM
PCH
+PCH_P1V0 - 7.858A
+3.3V_AUX - 1.198A
+3.3V - 7mA
+1.8V_AUX - 0mA
VBAT - 1mA
+3.3V_LPS - 0.502A
MC34063ADR2G
-12V POWER
-12V SWITCH
TPS51211DSCR
1.0V PCH Core Power
1.0V SWITCH
+PCH_P1V0
Mosfet-P
+3.3V_LAN
3V Battery
Internal Switch
LAN-RTL8111H-CG
+3.3V_LAN - 70mA
V_1P0_LAN - 300mA
V_1P0_LAN
AUDIO ALC221
+5V_AUX - 41mA
+3.3V - 23mA
USB(USB2.0*2)
5V_USB - 1A
USB(USB3.0*7)
5V_USB - 6.3A
PS2 *2
5V_USB - 1A
UP7501
5VDUAL Power
5V Linear
+5V_USB
Project
Berlinetta V
Maranello V
Barchetta
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Power Map
Size Custom
Document Number
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Sheet 59 of 65

Project	
Berlinetta	V
Maranello	V
Barchetta	V

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Title: GPIO Table1

Size	Document Number	Rev
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Project	
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Maranello	V
Barchetta	V

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Title: GPIO Table2

Size	Document Number	Rev
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Project	
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Maranello	V
Barchetta	V

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Title: **GPIO Table3**

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Berlinetta/Maranello X1

2014/08/11

EMI team suggest :

PAGE 24/29: Add 0.1uF cap by EMI suggest.
Add C463, C464, C468.

PAGE 27: Reserve bridge resistor by EMI suggest.
Add R860, R861, R862, R863.

PAGE 19: Reserve 10pF cap by EMI suggest.
Add C474. (SI:1082697)

SIO vendor review :

PAGE 24: Modify R180 from I to NI by SIO vendor review.
Modify R180 from I to NI. (SI:1082699)

2014/08/12

PAGE 36: Update audio codec LIB and MSI PN to ALC221VB.
Modify U13 PN to B05-LC2212C-R09. (SI:1082700)

PAGE 44: Connect TPM_PIRQ# to GPP_G21 following CRB. (SI:1082701)

Follow PCA spec to rename part reference :

PAGE 25: Modify LPC DEBUG PORT from E52 to E17.
Modify LPC DEBUG PORT from E52 to E17

PAGE 25: Modify U57 to U31.

PAGE 27: Modify J64 to J63.

PAGE 24/29: Modify J65 to J69.

PAGE 47: Modify U17 to U7 and Modify U14 to U8.

PAGE 33: Rename CR5 to CR1, rename CR1 to CR5. (SI: 1082698)

Power team suggest:

PAGE 46: Modify R796 from 29.9K to 48.7K. Modify R516 from 113K to 210K.
Modify R542 from 200 ohm to 316 ohm.Modify R541 and C388 from I to NI.
Modify R793 from 2.21K to 3.65K. Modify R547 from 200 ohm to 287 ohm.
Modify C385 from 0.082uF to 0.068uF. Modify C374 from 0.47uF to 0.33uF.
Modify R794 from 3.83K to 3.48K. Modify R548 from 200 ohm to 100 ohm.
Modify C386 from I to NI. Modify C372 from 0.47uF to 0.22uF.
Modify RT4, RT5 from 470k to 100k. Modify R515, R545 from 3.83k to 10k.
Modify R514, R544 from 27.4k to 10k. Modify R519 from 73.2K to 71.5K.

PAGE 49:Modify CHOKE9 PN to L04-06A7111-L65. Add C616

PAGE 47: Add C472, C473, C504. Reserve C612, C505, C506, C606, C613.

PAGE 48: Add C614, C615.

PAGE 51: Delete L45, C488, C489, C490, C495, C496, C497, C498, C499,
Add CHOKE14, C622, C638. Modify EC39 to 820uF, modify C494 to 10uF and NI, modify R646 to 60.4K ohm.

PAGE 45: Delete EC17, C456, C457, C452, C455
Add C639, C640, C641, R682. Modify EC13, EC14 to 270uF, modify EC18, EC19 to 820uF,
modify C352 to 10uF and NI, modify C346 to 10uF, modify EC15 to NI, modify R484 to 41.2k ohm.

PAGE 50: Modify C475 from NI to I. (SI:1082696)

2014/08/19

PAGE 50: Modify +VCCIO circuit by power team suggest.
Connecot R632 to +5V and add R864. (SI:1082696)

PAGE 43/44: Modify power well of TPM and SPI recovery header to SPI_POWER.
Connect Pin 6 of E16 to SPI_POWER and connect TPM power to SPI_POWER. (SI:1082702)

PAGE 53: Reserve pull-down resistor on CHASSIS_ID0 and CHASSIS_ID1.
Add R865, R866. (SI:1072381)

2014/08/21

PAGE 8/14/25: Modify SYS_PWRGD, PCH_PWRGD sequence.
Add R869, R868 and modify R70, R264 from I to NI. (SI:1082703)

2014/08/22

PAGE 14/18/19: Following HP specific to modify GPIO and port map table.
Connect BOOT_BLK_REC# to GPP_B15, connect LAN_CLK_REQ# to GPP_H4, connect BOOT_BLK_EN# to GPP_G6,
connect PASSWORD_EN to GPP_G9, connect FRONT_USB_P26_DET# to GPP_G12, connect INT_USB_P152_DET# to GPP_G15,
connect FRONT_AUD_DET# to GPP_G16, connect COMM_B_DET# to GPP_G17, connect TPM_PIRQ# to GPP_G21,
connect SIO_SMI# to GPP_C22, connect SIO_PME# to GPP_C23, connect HPGP_DBG_SERIAL_DET#1 to GPP_H9.
 (SI:1073982)

2014/08/25

PAGE 50: Modify +VCCIO circuit by power team suggest.
Change VR IC from NCP3135 to ISL8016IRAJZ and modify the relative circuit. (SI:1082696)

2014/09/02

PAGE 10/11/12/13: reserve SPD address HIGH&LOW resistors for DIMM.
Add R915,R916,R917,R918,R919,R920,R921,R922,R923,R924,R925,R926,R927,R928,R929,R930.(SI:1075817)

PAGE 1: PCA/PCB PN and SSID need to be updated into schematic .
Add PCA/PCB PN and SSID into schematic.(SI:1075810)

2014/09/04

PAGE 43: SKL Platforms - SPI0_IO3 Signal Implementation Requirement for ES or pre-ES1/ES1 Samples
Modify R438 from I to NI and add R763.(SI:1076956)

SIO schematic check feedback.

Page 22: Modify R190 pull-up power well to +3.3V

Page 23: Add a pull-up resistor R803 at PWRBTN# signal. (SI:1082699)

2014/09/18

Intel schematic check feedback.

Page 16: Modify Pin E1 of PCH pull-up power rail to P1V0_PCH_VCCF24_1P0.

Page 16: Modify VCCRTC circuit make sure VCCRTC does not exceed 3.2V.
Add R933, R934.

Page 8: Unused VGTX/VccOPC/VccEOPIO pins suggested to reserved resistor to GND.
Reserve R623, R625,, R627, R816.

Page 4: Modify serial resistor for PROC_AUDIO_SDO.
Modify R172 from 33 ohm to 20 ohm.

Page 4: Modify serial resistor for SPI chip select.
Modify R608, R439 from 33 ohm to 0 ohm. (SI:1080996)

Page 18/27: Modify Platform debug header from 2x6 to 2x10 following HP request.
Delete E17. Add R812,R813,R806,R814,R815,R809,R810,R807,R811,E25,E27,E28,JP27,JP28. (SI:1082704)

2014/09/24

Connect the CPU VTT rail and the SIO15 VTT rail are the same

Page 24: Connect +PCH_P1V0 to SIO15 VTT power rail.

Page 46: Modify H_PROCHOT# pull-up resistor pull up to +PCH_1PV0.
Modify R616 pull-up power rail to +PCH_1PV0. (SI:1082705)

2014/09/25

Page 43: SPI_MISO/ SPI_MOSI/ SPI_CLK/ SPI_WP#/ SPI_HOLD#
FOR BETTER SI, Need add 0 ohm connect to E16.
Add R608, R818, R819, R820, R821. (SI:1082706)

2014/09/26

Page 4/14: Add a serial resistor at PROCHOT_N/H_PWRGD/PLTRST# signal according CRB 1.0.
Add R18, R936, R937. (SI:1082707)

Page 14: Add a serial resistor at PCH_THERMTRIP# signal according Intel Design guide.
Add R935. (SI:1082708)

PAGE 22/31/32: Following HP specific to modify GPIO and port map table.
Connect PCIE6 to J31 and connect PCIE7 to J32.
Connect PCIE_CLK0 to J31, connect PCIE_CLK5 to J41, connect PCIE_CLK6 to J32, connect PCIE_CLK8 to J42.
(SI:1073982)

2014/09/29

Power team suggest:

PAGE 51/54: Modify component package to 0603 size.
Modify R647, C501, C551, C557,C407, C415, C505, C417.(SI:1082696)

PAGE 43: Add pull-up resistor at PCH_SPI_MISO/PCH_SPI_MOS1 for ES or pre-ES1/ES1 Samples
Add R823 and R822.(SI:1076956)

Project	
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Maranello	V
Barchetta	

HEWLETT PACKARD

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Title: History

Size	Document Number	Rev
Custom	HP SCH P/N: 793306-000(MSI MS-7957)	X4

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Berlinetta/Maranello X1

2014/10/7

PAGE 26: Modify Berlinetta board ID to 7 and Maranell board ID to 8.
Modify R256 from I to I,NI, modify R259 from NI to NI,I, modiyf R801 from NI,I to NI, modify R261 from I to NI,
modify R775 from NI to NI,I, modify R263 from NI to I, modify R932 from I to NI.(SI:1084026)

PAGE 14/19/43: Add PCH strapping pin pull-up/pull-down resistor.
Add R86, R824, R88, R839, R827, R87, R825, R826, R840.(SI:1084027)

PAGE 4/19/55: Modify XDP debug port circuit according Intel CRB 1.0.
Modify R228,R174,R175,R751,R750,R752,R755,R758,R726,R730,R720,R727,R817 from NI to I,
modify R176,R723,R731,R719,R15 from I to NI.(SI:1084028)

2014/10/16

PAGE 43: Modify PCH_SPI_MOSI/PCH_SPI_MISO pull-up resistor to NI.
Modify R822, R823 from I to NI.(SI:1084027)

PAGE 43: Modify PCH_SPI_MOSI pull-up resistor to I.
Modify R823 from NI to I.(SI:1084027)

Berlinetta/Maranello X2

2014/10/24

PAGE 44: Connect TPM power pin to correct power rail.
Connect pin 22 of U40 from +3.3V to SPI_POWER, connect R704 from +3.3V to SPI_POWER (SIO1088438)

PAGE 46: Modify SVIDCLK pull-up resistor value from 45.3K ohm to 45.3 ohm.
Modify R509 from 45.3K ohm to 45.3 ohm (SIO1088410)

PAGE 4/46: Modify SVID topology according Intel design guide.
Add R938, R939, R940, R941 (SIO1105529)

2014/10/29

PAGE 36: Modify audio amplifier control circuit.
Reserve R942 and modify R370, Q31 from I to NI. (SIO1092577)

2014/10/29

PAGE 34/52/53: Marking EC45, EC47, EC50 and CHOKE15 as CCL parts. (SIO1105535)

2014/11/18

Modify SIO15 circuit according SIO15 demo circuit.

PAGE 18/24: Pin 4 of U5 connect to pin BD17 and rename PCH_PME# to P_PME#. Modify R206 from I to NI.(SIO1105544)

PAGE 23/24: Connect chassis ID1 to pin15 of SIO.
move R216 to page 23 and add R943 pull up to +3.3V_AUX.(SIO1091273)

PAGE 23: Connect SIO15 pin 94 to SML1_DATA and pull-up resistor R184 change from I to NI(chipset side have a pull-up resistor.
(SIO1105563)

PAGE 23: Connect SIO15 pin 95 to SML1_CLK and pull-up resistor R183 change from I to NI(chipset side have a pull-up resistor.
(SIO1105563)

PAGE 24: Connect SIO15 pin 59/61 only pull up to +3.3V.(SIO1105563)

PAGE 38: Keyboard power control change to pin 103 of SIO15.
Change R410 connecting from 5V_USB_CTRL to KBD_PWR_CTRL.(SIO1105570)

Modify power circuit for improve power quality.

PAGE 46: Modify R511 from 100k ohm to 105k ohm. Modify C387 from 0.082uF to 0.22uF. Modify R537 from 1.2k ohm to 3.65k ohm.
Modify C637 from 1500pF to 820pF. Modify C635 from 1800pF to 1000pF. Modify C378 from 680pF to 1000pF.
Modiyf R548 from 137 ohm to 200 ohm.(SIO1102639)

PAGE 51: Modify R648 from 0 ohm to 1 ohm. modify EC39 from NI to I.(SIO1102639)

PAGE 45: Modify R486 from 0 ohm to 1 ohm. modify R487 from 0 ohm to 1 ohm.(SIO1102639)

PAGE 50: Modify R640 from NI to I. modify R641 from I to NI.(SIO1102639)

2014/11/24

PAGE 25: Modify COM port header part reference from P54 to P52.(SI:1091757)

PAGE 18: Modify Platfrom debug port header part reference from E25 to E23.(SIO1091698)

PAGE 43: Change JP14 to longer jumper, modify jumper PN from N33-1020271-H06 to N33-1020481-H06.(SIO1091713)

PAGE 34/45: Modify EC4/EC15 PN from C93-10116A1-N07 to C93-10116D1-N07.(SIO1105579)

PAGE 39: Add another power well +5V_PS2 for PS/2.
Add R950, R951, C700, C701, U56.(SIO1105582)

PAGE 51: Modify C487 from 1000pF to 2200pF for improve power quality.(SIO1102639)

Page 23: Modify R192,R190,R526 from I to NI for ESPI support.(SIO1100905)

Page 23: Modify R195,R531 from NI to I for ESPI support.(SIO1100905)

Page 20: Modify R564 from NI to I and modify R536 from I to NI for ESPI support.(SIO1100905)

Page 18: Debug header clock connect to U4.BC17.
U4.AV19 connect to a test point TP81. Reserve R956. Add R957. Modify R812 from I to NI.
Modify R813 from NI to I for ESPI support.(SIO1100905)

Page 18: Modify R814 from PROTO to NI and modify R815 from NI to PROTO for ESPI support.(SIO1100905)

Page 18: ESPI_ALERT1# add a pull-up R958 for ESPI support.(SIO1100905)

Page 18: Reserve R959 for ESPI support.(SIO1100905)

Page 18: Modify R124 from I to NI for ESPI support.(SIO1100905)

Page 14: Reserve R953,R954,R955 for ESPI support.(SIO1100905)

Page 19: Modify R165 from 4.7k to 1k and modify from NI to I, modify R839 from I to NI for ESPI support.(SIO1100905)

Page 24: Reserve R960,R961,R962 for ESPI support.(SIO1100905)

2014/11/27

Page 18: Modify R153 from NI to I for ESPI support.(SIO1100905)

Page 36: Modify R349 from I to NI, modify R565 from NI to I, modify R356/R357 from 51k ohm to 10k ohm,
modify R360/R361 from 10k ohm to 20k ohm for no beep sound issue.(SIO1094868)

Page 26: Modify RT3, C104 from NI to I following SIO demo circuit.(SIO1105574)

Page 24: Move R239 to Q5.D pin, modify R234 from 47k ohm to 100k ohm,
delete R236 to follow SIO demo circuit.(SIO1105578)

Page 9: Modify CPU mounting hole to meet PCA spec.
CPU footrpint change to ZIF_SOCK1151_TEST_7957
and add mounting hole ground pin MH_VSS-1 to MH_VSS-32.(SIO1098277)

Page 14: Modify R53 from I to NI for ESPI support.(SIO1100905)

2014/12/04

Page 51: Modify +1P0V_EN circuit for System can not power on from S5 Max Power Saving mode
Add Q96, R963, C702. (SIO1096836)

PAGE 45: Modify R484 from 80.6k ohm to 84.5k ohm for improve power quality.(SIO1102639)

PAGE 16: Modify 24MHz cristal circuit.
Modify C29, C31 from 27pF to 30pF.(SIO1092380)

2014/12/08

PAGE 50: Modify C480 from 10pF to 0 ohm for improve +VCCIO power quality.(SIO1102639)
PAGE 50: Modify R636, C479, R642 from I to NI for improve +VCCIO power quality.(SIO1102639)
PAGE 50: Add R964 and connect U85.P12 to +5V for improve +VCCIO power quality.(SIO1102639)

PAGE 17: Connect DP to VGA HPD_pin to DDPE_HPD3 for no VGA output isssue.(SIO1099784)
PAGE 17: Connect EPD_HPD to GND through R114 for no VGA output isssue.(SIO1099784)

2014/12/15

PAGE 50: Add EC51 for improve +VCCIO power quality.(SI:SIO1102639)
PAGE 50: Modify CHOKE11 from 0.5uH to 0.22uH +VCCIO power quality.(SIO1102639)
PAGE 51: Modify R646 from 113k ohm to 64.9k for improve +1P0V_PCH power quality.(SIO1102639)
PAGE 34: Modify LAN power control circuit.
R326 connect to LPS_ON#.(SIO1105584)

PAGE 14/34: Modify LAN clock request circuit.
Modify R317 from NI to I, Modify R630 from I to NI, Reserve R965.(SIO1105585)

PAGE 28: Modify Q12 from NI to I and modify R273 from I to NI and modify C115 from I to NI.(SIO1092498)
PAGE 14: Use GPP_H2 for PCI_EXT_DET.
Add R966, R967(SIO1097287)

2014/12/22

Page 18: Connect R813 to +1.8V_AUX for ESPI support.(SIO1100905)
Page 23/43: Connect FDT_OVRD# to SIO15 Pin 78 GPIO22 .(SIO1102607)
Page 18: Modify VTT_DDR Power Control for support C8.
Modify R660 from NI to I. Modify R661 from I to NI.
Add R968, R969, R970, C703, Q97, Q98.(SIO1105589)

2014/12/23

Page 43: Modify R823 from I to NI.9SIO1105596)

Page 38/39: Modify USB discharge control circuit.
Delete Q39,Q40,Q41,Q43,Q44.
Modify R431,R432,R433,R435,R436 from 680 ohm/0402 to 1k ohm/0603.(SIO1105598)

2014/12/25

Page 44: Connect R478 from 5VDIMM to +5V_AUX.(SIO1105600)
Add one power rail VCCST_P1V0 for VCC_DDR leakage.
Page 51:Add Q99,Q100,R971,R972,R973,C705,C706.(SIO1105602)

Page 4: Connect RR941,R7,R8,R10,R11,R12,R13,R14 from +PCH_P1V0 to VCCST_P1V0.(SIO1105602)
Page 8: Connect XU1 PIN V4/V5/V6 from +PCH_P1V0 to VCCST_P1V0.(SIO1105602)
Page 19: Connect R228,R174,R175 from +PCH_P1V0 to VCCST_P1V0.(SIO1105602)
Page 24: Connect SIO +VTT from +PCH_P1V0 to VCCST_P1V0.(SIO1105602)
Page 46: Connect R508,R509,R510,C435 from +PCH_P1V0 to VCCST_P1V0.(SIO1105602)
Page 55: Connect R721,R760 from +PCH_P1V0 to VCCST_P1V0.(SIO1105602)

Page 14: Add U92, C704 and modify R868 from 0 ohm to 10k ohm for POS.(SIO1107787)

Add power test point on power plane.
Page 45: Add VCC_DDR_1(SIO1107791)
Page 47: Add +VCORE_1(SIO1107791)
Page 48: Add +VCCGT_1(SIO1107791)
Page 49: Add +VCCSA_1(SIO1107791)
Page 50: Add +VCCIO_1(SIO1107791)
Page 51: Add +PCH_P1V0_1(SIO1107791)
Page 52: Add +3_3V_AUX_1(SIO1107791)
Page 53: Add +5V_AUX_1 and ATX_5VSB_1(SIO1107791)

2015/01/05

Page 19/36: Delete D18 and add C707, C708.(SIO1107794)

2015/01/06

Page 47/48: Modify C402,C425,C423 from NI to I for power quality.(SIO1102639)

Modify XDP circuit.
Page 55: Modify R729,R752,R755,R758,R761,R772,R750, R751 from I to NI.(SIO1107823)
Page 19: Modify R174, R175 from I to NI.(SIO1107823)
Page 4: Modify R15 from NI to I.(SIO1107823)
Page 14: Modify R86 from 4.7K to 150K and I.(SIO1107823)

USB power switch and poly fuse co-layout.
Page 39: Reserve FS4,FS5,FS6,FS7,FS8,R974,R975,R976
,R977,R978,R979,R980,R981,R982,R983.(SIO1107825)

5VDIMM and +5VUSB use the same control IC.
Page 45: Modify R500 from NI to I, R501 from I to NI.(SIO1107829)
Page 38: Delete R656,C458,R657,C460,R417,C380,R416,R418,
R420,R423,R419,R421,R422,U69.(SIO1107829)

Page 26: Modify R715 from NI to I for DB2 revision ID.(SIO1107832)

2015/01/13

Page 19/36: Add C707, C708 for audio signal quality.(SIO1109650)

Page 25/30/40/41/42: Modify D5,D9,D10,D32,D33,D34,D35,D36 PN to D0G-03A0509-SI0
for EMC issue.(SIO1099109/SIO1099132)

Page 40/41/42: Modify L29,L30,L31,L32,L23,L24,L25,L26,L35,L36,L37,L38,L42,L41
from NI to I for EMC issue.(SIO1099109/SIO1099132)

Page 40/41/42: Modify RN27,RN28,RN21,RN22,RN23,RN24,RN26,RN9,RN10,RN11,RN12,RN15,RN16,RN17,RN18
from I to NI for EMC issue.(SIO1099109/SIO1099132)

Page 40/41/42: Modify RN7,RN8,RN13,RN14,RN19,RN20,RN25,RN26,RN30
from I to NI for EMC issue.(SIO1099078/SIO1099133)

Page 40/41/42: Modify L21,L22,L27,L28,L33,L34,L39,L40,L44
from NI to I for EMC issue.(SIO1099078/SIO1099133)

Page 43: Modify R438 from NI to I and modify R763 from I to NI for PCH ES2 sample.(SIO1076956)

2015/01/15

Page 47: Modify R573,R555,R557 from 0 ohm to 1 ohm for power quality.(SIO1102639)
Page 34: Modify C228,C229 from 27 pF to 24 pF for Crystal matching.(SIO1115033)
Page 41/42: Modify L29,L30,L31,L32,L23,L24,L25,L26,L35,L36,L37,L38,L41,L42
PN to L12-5008030-I05 for EMC isssue.(SIO1099078/SIO1099133)

Page 44: Modify U40 PN to OBC-7957001-IX4.(SIO1101434)

2015/01/21

Page 33: Add R984,R985,CR12,Q108 for RSMRST# debug LED.(SIO1111709)

2015/01/28

Page 52: Modify R678 from 102k to 10k ohm, modify R677 from 324k to 32.4k ohm,
modify C519 from 0.015uf to 22pf for +3.3V_LPS leakage in G3 state.(SIO1105602)

Page 22: Delete RN6,U65,C189,EC3,R299,Q16.(SIO1113861)

Page 34: Modify LAN power control circuit
Reserve R986, R987 NI.(SIO1105584)

2015/01/29

Page 34: Modify onboard LAN wake to PE_WAKE.
Modify R314 from NI to I, modify R532 from I to NI.(SIO1115093)

2015/01/30

Page 34/35: Add R988, R989, modify R339 from 510 ohm to 0 ohm and modify from NI to I,
delete R336, modify R337 from 249 ohm to 510 ohm.(SIO1105584)

2015/02/13

Page 38: Modify C299 from 0.22uf to 1uf to seperate USB power turn on timing.
(SIO1121957)

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Berlinetta/Maranello X3

2015/04/01

PAGE 46: Modify C368 from 680pF to 820pF, modify C387 friom 0.22uF to 0.1uF,
modify C378 from 1000pF to 820pF for power quality.(SIO1139867)

PAGE 51: Modify R647 from 0 ohm to 2.2 ohm, modify R648 friom 1 ohm to 2.2 ohm,
modiyf R649, C501 from NI to I for +PCH_P1V0 power quality.(SIO1139867)

PAGE 45: Modify R485 from 0 ohm to 2.2 ohm, modify R487 friom 1 ohm to 2.2 ohm,
modiyf R682, C641 from NI to I for VCC_DDR power quality.(SIO1139867)

Add USB type C to PCA.
PAGE 32: Add P81, R945, R946.(SIO1117893)

TPM leakage current and power down fixed circuit
PAGE 44: Add Q109,Q110,R990,R991,R992,R993.(SIO1134627)

2015/04/07

PAGE 47/48: Add C710, C713 and move C445,C449 to Vcore accordding MOW10.(SIO1137561)

PAGE 14/46: Add R91,R92,Q111 and modify R868 from 10k ohm to 0 ohm for tCPU22 and tCPU28 sequence.(SIO1139888)

2015/04/10

PAGE 52: Modify R669 from 147k ohm to 14.7k ohm and modify R671 from 115k ohm to 11.5k ohm for power quality.(SIO1139867)

PAGE 26: Modify R251 from I to NI and modify R761 from NI to I for SI2 Revision ID.(SIO1139871)

PAGE 34: Add Q39 for LED on at S5 state while WOL is disable.(SIO1138523)

2015/04/14

PAGE 36: Modify R369 size from 0402 to 0603 and modify C259,C263 from 0.01uF to 0.1uF by vender suggestion.(SIO1141465)

2015/04/17

Modify JP14 and JP49 to shorted type jumper.
PAGE 43: Modify JP14 and JP49 MSI PN from N33-1020481-H06 to N33-1020271-H06(SIO1143522)

PAGE 43: Modify R438 from NI to I and modify R763 from I to NI for PCH QS sample.(SIO1076956)

2015/04/20

Modify THERMTRIP# control circuit.
PAGE 14: Modify R59 from I to NI and move Q11 to Page 14 and modify to NI.(SIO1143755)

PAGE 32: Modify P81 from PROTO to NI.(SIO1143756)

Modify PCH PN to QS sample PN.
PAGE 14 ~21/56: Modify PCH PN to QS sample. OB1-7957002-IX6 for H170, OB1-7957003-IX6 for H110.(SIO1144254)

2015/04/22

Remove PCH heatsink from BOM.
Page 56:Modify U4_X1 from I to NI.(SIO1121944)

2015/04/24

Modify TPM IC PN to FW6.10.
PAGE 44: Modify U40 from OBC-7957001-IX4 to OBC-G006001-IX4.(SIO1150968)

Modify PCB PN for SI2.
PAGE 56: Modify PCB PN to PF0-079570C-G37.(SIO1150974)

2015/04/30

Modify SIO15 to A3 version.
PAGE 23/24: Modify U5 from OB02-0315H04-N62 to B02-0315H14-N62.(SIO1150981)

Modify VRM IC to 2.0 version.
PAGE 46: Modify U46 from I32-958550C-I11 to I32-958551C-I11.(SIO1150985)

Modify J42 X4 slot to the other one with latch.
PAGE 31: Modify U46 from N11-0640341-L06 to IN11-0640371-L06.(SIO1142659)

2015/05/04

Modify VRM circuit to improve VCCSA power.
PAGE 46: Modify R795 from 1k ohm to 2k ohm, modify R787 to 49.9k ohm and I, modify C373 to 0 ohm and I,
modify R519 from 71.5k ohm to 137k ohm, modify C467/C470/C471 from 22uF to 47uF.(SIO1150996)

Fix EMI issue.
PAGE 30: Modify C154/C155/C156/C157 to 10pF and I, modify C142/C146/C149 from 2.2pF to 1.5pF,
modify C143/C147/C150 from 4.7pF to 1.5pF, modify L15/L16/L17/L18/L19/L20 to 22ohm Bead,
modify J69 PN from N58-24F0171-F02 to N58-24F0241-W06.(SIO1140515/SIO1143873)

Remove unnecessary ESD protestion Diode.
PAGE 25/35: Modify D5/U66/U67/D12/D14 from I to NI.(SIO1151002)

Modify connector and slot PN to follow PCA plating define.
PAGE 10/11/12/13/27/31: Modify J41 to N11-1641481-L06, modify J42 to N11-0640371-L06, modify P185 to N11-0360231-L06,
modify XMM1/XMM3 to N13-2401581-F02, modify XMM2/XMM4 to N13-2401571-F02., modify JV42 to N11-0360501-L06.(SIO1151036)

Modify 470uF cap to MSI common material.
Page 38/39/52/53: Modify EC8/EC9/EC47/EC50 from C93-4711031-N07 to C93-4711041-N07.(SIO1151096)

Modify front USB3.0 header PN.
Page 42: Modify P26 from N32-2101181-H06 to N32-2101211-H06.(SIO1151118)

2015/05/07

Fix EMI issue.
PAGE 30: Modify J69 PN from N58-24F0171-F02 to N58-24F0241-W06.(SIO1140515/SIO1143873)

Berlinetta/Maranello X4

2015/05/29

Modify PROCHOT# topology.
PAGE 4: Modify R11 from 75 ohm to 1k ohm, modify R18 from 100 ohm to 499 ohm.(SIO1141156)

Modify LAN_DISABLE# pull-up resistor to NI.
PAGE 14: Modify R507 from I to NI.(SIO1167214)

SIO15 COMP_IN3 control update
PAGE 24: Add R994,Q112.(SIO1163512)

Reserve 2 cap at VCCSA power plane.
PAGE 49: Add C714,C715.(SIO1170291)

2015/06/04

Modify circuit according Intel SR_Rev16.
PAGE 20: Add L9,C778,C779.(SIO1170296)

Modify EC11 to 5000 hr cap.
PAGE 44: Modify EC11 PN from C93-10116D1-N07 to C94-1011621-N07.(SIO1170297)

Modify PWM IC to version 2.1.
PAGE 46: Modify U46 PN from I32-958551C-I11 to I32-958552C-I11.(SIO1159108)

Add buffer at ESPI RESET signal..
PAGE 18/23: Add C780,C781,U96R173,R782.(SIO1170298)

PAGE 46: Modify C368 from 820 pf to 1500 pf for Vcore power quality.(SIO1170300)

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