

Wistron Confidential

MV

2008/05/15

REV : -1

<Variant Name>

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Karia			
Size A3	Document Number	KARIA - DISCRETE	Rev SH
Date: Friday, May 16, 2008		Sheet 1 of	58

KARIA DISCRETE BLOCK DIAGRAM

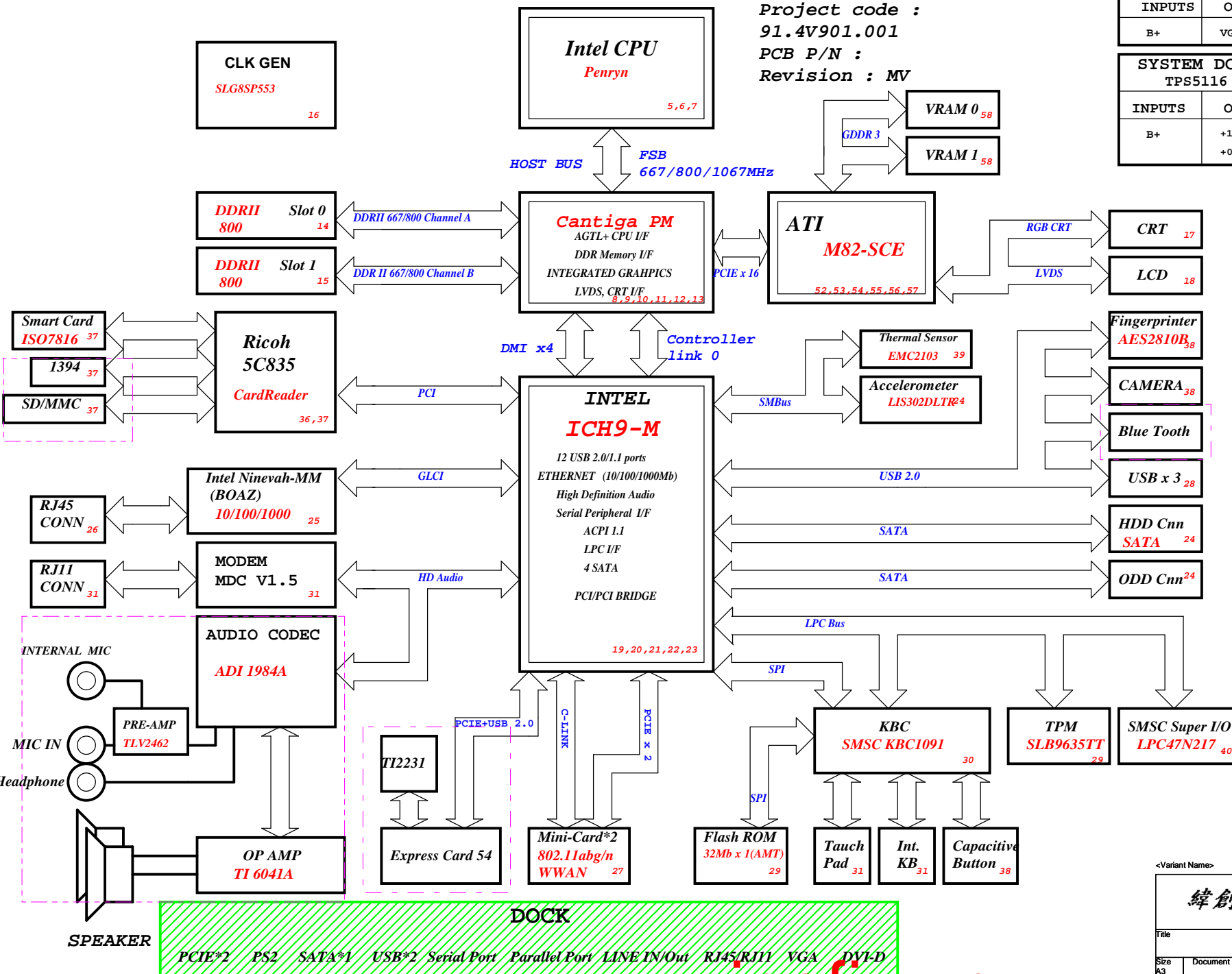
Project code :
91.4V901.001
PCB P/N :
Revision : MV

SYSTEM DC/DC SC471AML		SYSTEM DC/DC TPS51120	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
B+	VGA_CORE 45	B+	+5VALW 7A +3VALW 6A 46
SYSTEM DC/DC TPS5116		SYSTEM DC/DC SC412A	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
B+	+1.8V 7A 47 +0.9V 1A	B+	+1.5VS 3A 50 +1.05VM 13A 48

CHARGER BQ27470	
INPUTS	OUTPUTS
BATT_A BATT_B	BATT 18V 3.0A 5V 100mA 51

CPU DC/DC ISL6260A	
INPUTS	OUTPUTS
B+	+VCC_CORE 0.844~1.3V 44A 43

PCB LAYER	
L1:	Signal 1
L2:	GND
L3:	Signal 2
L4:	Signal 3
L5:	GND
L6:	VCC
L7:	Signal 4
L8:	Signal 5
L9:	GND
L10:	Signal 6



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Title: **Block Diagram**

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- Discrete PV
- 03/11/08:
- Page 51 - Change R118 to 287K ohm from Vox information.
 - Page 43 - Change R582.2 to +3VALW from +3VS to power U89.39 (3V3)
 - Page 45 - Change R232 to NO INSTALL
 - Page 30 - Remove D48, connect signal directly to ADP_PRES, and uninstall R558
 - Page 27 - Reserve a 1u 0603 cap (NO INSTALL) on MC2_DISALBE (same as MC1_DISABLE)
 - Page 19 - Add a 0 ohm series on PLT_RST# at U113.4
 - Page 33 - Add a 0 ohm series on PM_PWROK_R at R175.2
 - Page 13 - Uninstall BGA_CRACK circuit: U115, U116, R740, R744, R801, & R802
 - Page 23 - Uninstall BGA_CRACK circuit: U117, U118, R803, R804, R805, & R806
 - Page 39 - Change R710 (SHDN_SEL) to 15K 1% to use Internal Diode for H/W critical shutdown
 - Page 57 - Add a discharging FET (gate connect to Q15.D) on 3.3V_DELAY at Q42.D
 - Page 25 - May require a discharging FET for +3VM_LAN at Q39.D
 - Page 32 - May need to change RGB q-switches power to +5VALW or +5VS (depending on wavy impact)
 - Page 51 - Change R97 to 33K from 1.27K
 - Page 41 - Change DAUGTH1 pin 52 and pin 54 to +5VS from +5VALW
 - Page 41 - Remove ICH_SMB_CLK/DATA from DAUGTH1 pin 32 and 34

Voltage Rails

o MEANS ON x MEANS OFF

power plane State	+BB LDO3 LDO5	+3VALW +5VALW	+1.8V +5V +0.9V	+5VS +3VS +1.8VS +1.5VS +VGA_CORE +CPU_CORE +VCCP	+3VM +1.05VM	CLOCK
S0	O	O	O	O	O	O
S3/M1	O	O	O	X	O	O
S3	O	O	O	X	O	O
S5 S4/AC	O	O	X	X	O	O
S5 S4/Battery only	O	X	X	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X	X	X

PCI Devices

EXTERNAL	IDSEL#	REQ/GNT#	PIRQ
Cardreader&1394	AD25	2	G,E

PCIE Devices

DEVICE	NUMBER	CHANNEL
UWB(no support)	1	1
WLAN	1	2
EXPRESS CARD	1	3
WWLAN	1	4
DOCKING	1	5
GIGA LAN	1	6

USB PORT	Device
0	USB1
1	Free
2	EX-P
3	WLAN
4	USB2
5	USB3
6	BLUETOOTH
7	WWAN
8	FignerPrint
9	Dock1
10	WEBCAM
11	DOCK2

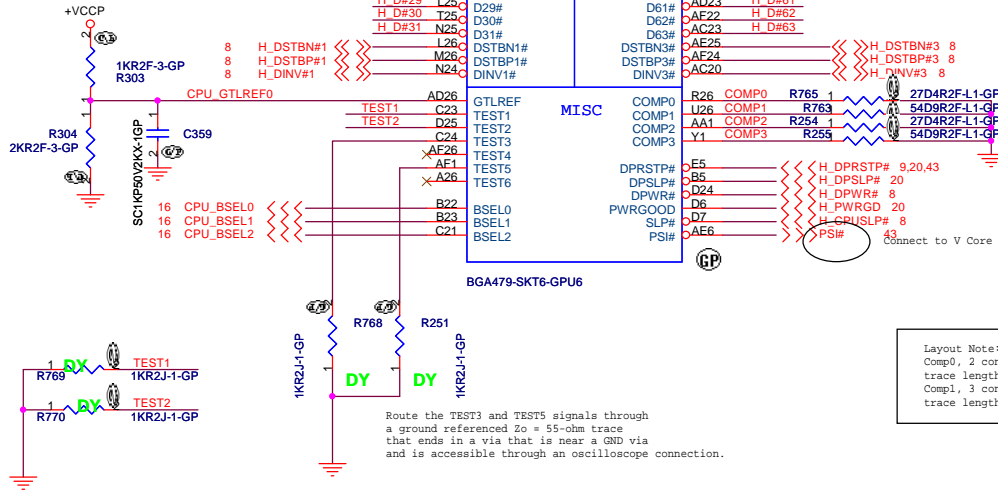
Symbols	Description
DY/DUMMY	No install
1KR2J	Resistor 1K ohm ,Size 0402 ,5%
1KR3F	Resistor 1K ohm ,Size 0603 ,1%
GP	ROHS parts
NC	Pin no connect to anything
1U16V2ZY-2GP	Caps 1U ,Size 0402 Y5V
2D2U6D3V3MX	Caps 2.2U ,Size 0603 X5R

IRQ	Device
0	System Timer
1	Keyboard
2	N/A
3	Serial port (COM2) ,LAN/Modem
4	Serial port (COM1)
5	Audio/VGA
6	Floppy
7	Parallel port
8	System CMOS/Real-time clock
9	Microsoft ACPI
10	N/A,Modem,LAN
11	Mass storage control/PCI simple communication control
12	synactic PS2 port GlidePAD
13	Numeric Data Process
14	Primary IDE interface ,HDD
15	Secondary IDE interface ,CD-ROM
16	Mobile Intel Crestline Express Chipset Family Microsoft UAA Bus Drive for High Definition Audio Intel 82801H (ICH9 Family) PCI Express Root Port -27D0 Broadcom NetXtreme Gigabit Ethernet
17	Intel 82801H (ICH9 Family) PCI Express Root Port -27D2 Broadcom 802.11b/g WLAN Intel 82801H (ICH9 Family) USB Universal Host Control
18	Intel 82801H (ICH9 Family) USB Universal Host Control Richo R5C835 Integrates FlashMedia Control Richo R5C835 Gemcore based SmartCard Control
19	Intel 82801H (ICH9 Family) PCI Express Root Port -27D6 Intel 82801H (ICH9 Family) USB Universal Host Control
20	Intel 82801H (ICH9 Family) USB Universal Host Control Intel 82801H (ICH9 Family) USB2 Enhanced Host Control
21	Intel 82801H (ICH9 Family) USB Universal Host Control
22	SDA Standard Compliant SD Host Control
23	HP Mobile Data Protection Sensor

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Title	
Karia List	
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KARIA - DISCRETE	
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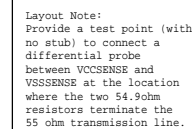
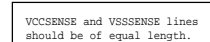
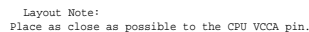
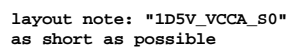
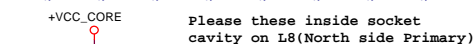
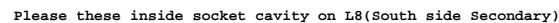
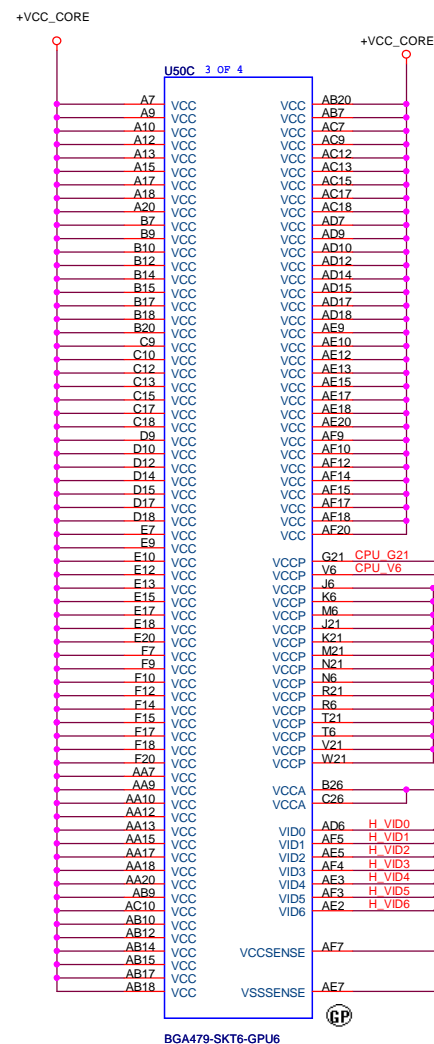
Layout notes
Z= 55 Ohm 0.5" MAX for GTLREF



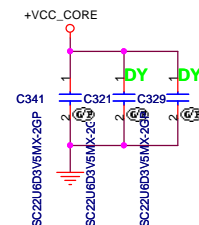
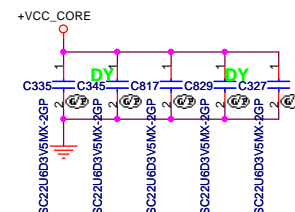
Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

Layout Note:
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" .
Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .

H_DINV#[3..0] << >> H_DINV#[3..0] 8
H_DSTBN#[3..0] << >> H_DSTBN#[3..0] 8
H_DSTBP#[3..0] << >> H_DSTBP#[3..0] 8
H_D#[63..0] << >> H_D#[63..0] 8

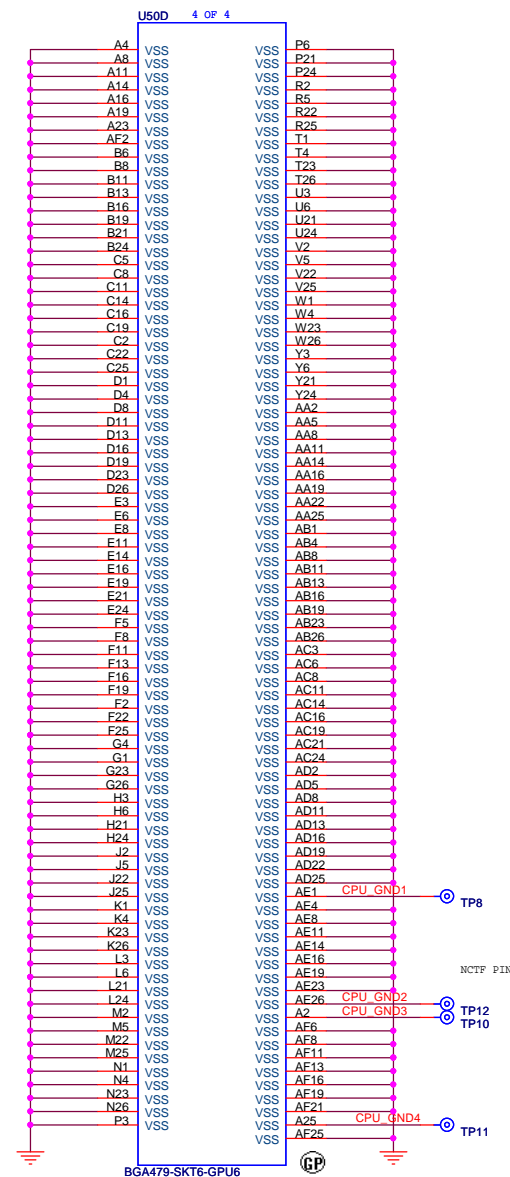
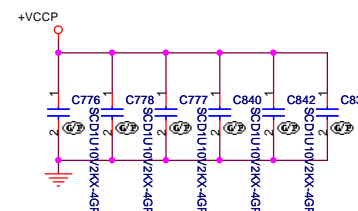
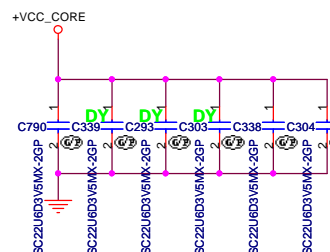


Please these outside socket
cavity on L8(North side Secondary)



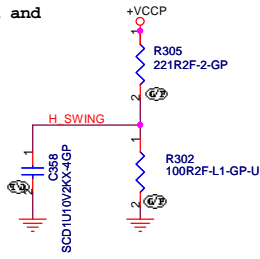
Please these outside socket
cavity on L8(South side Secondary)

Please these inside socket
cavity on L8(South side Primary)

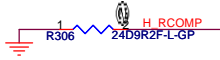


H_SWING routing Trace width and Spacing use 10 / 20 mil

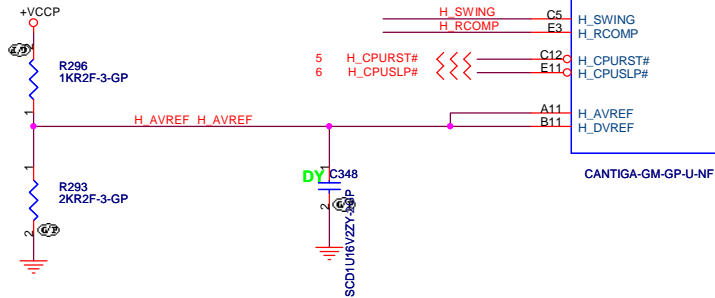
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")

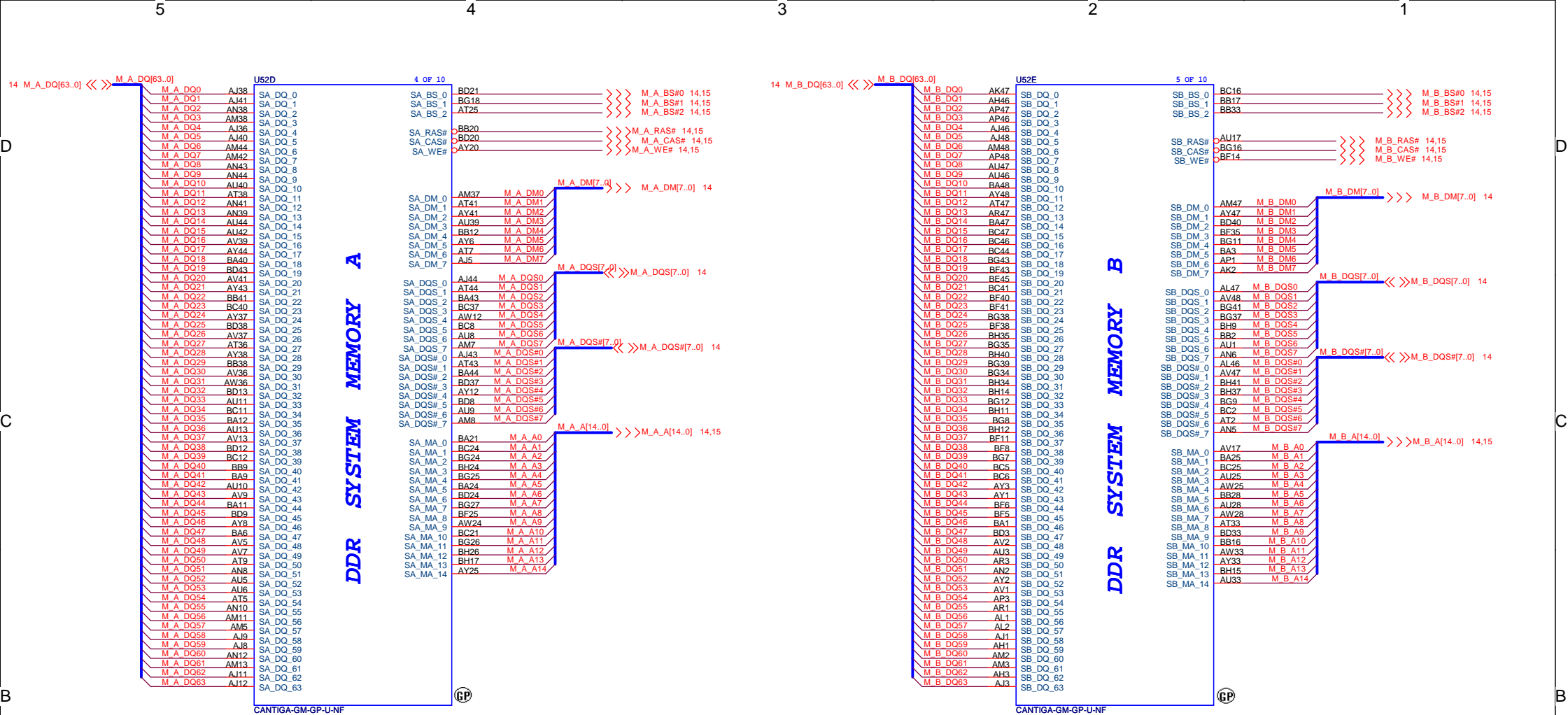


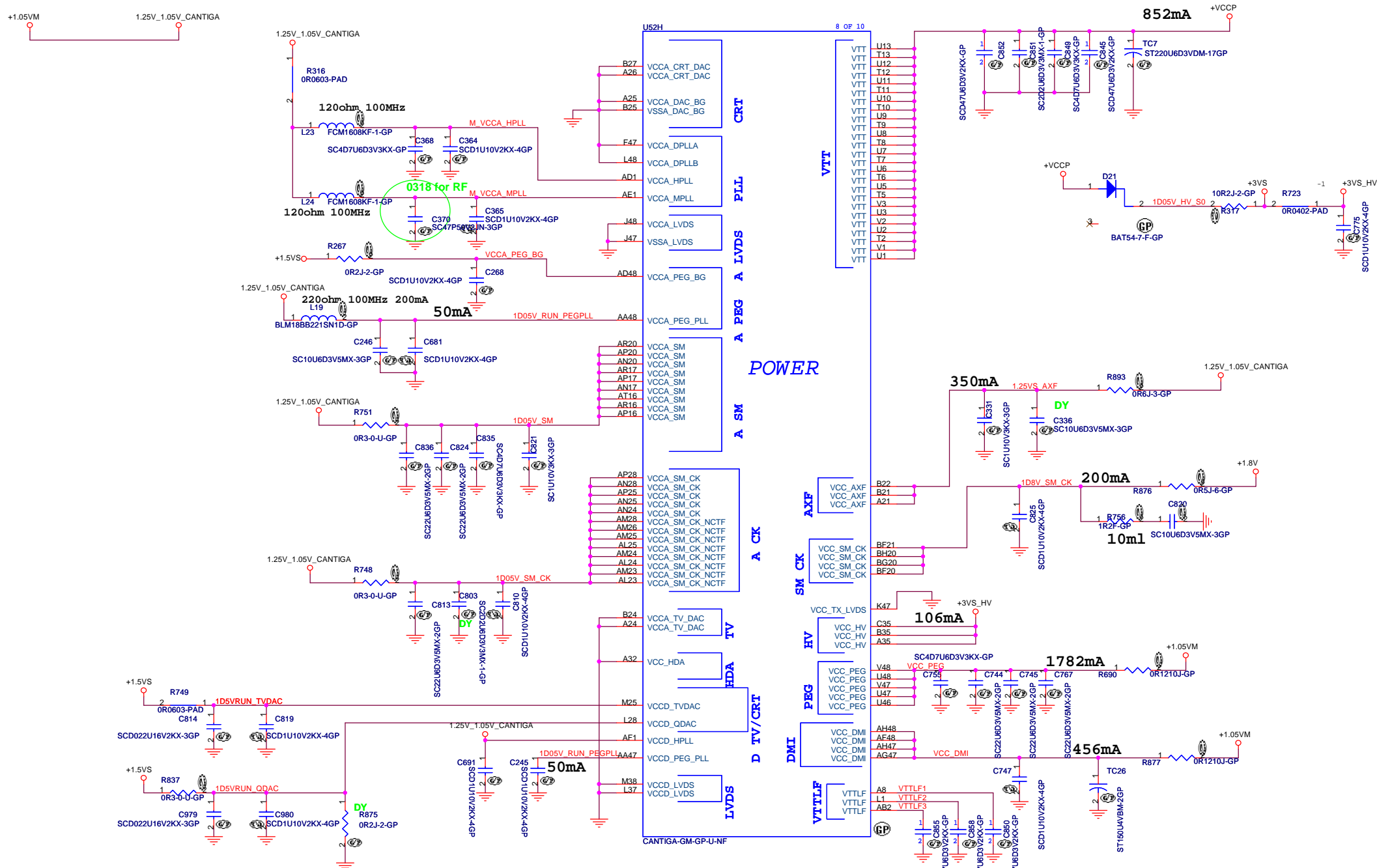
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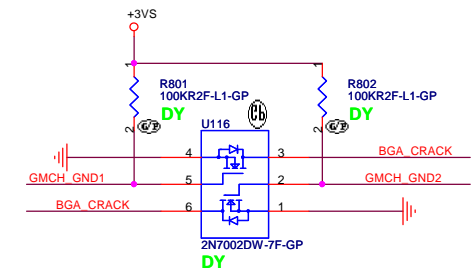
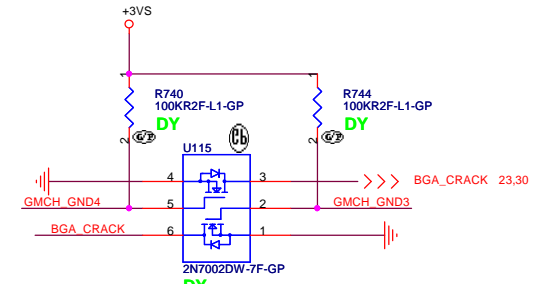
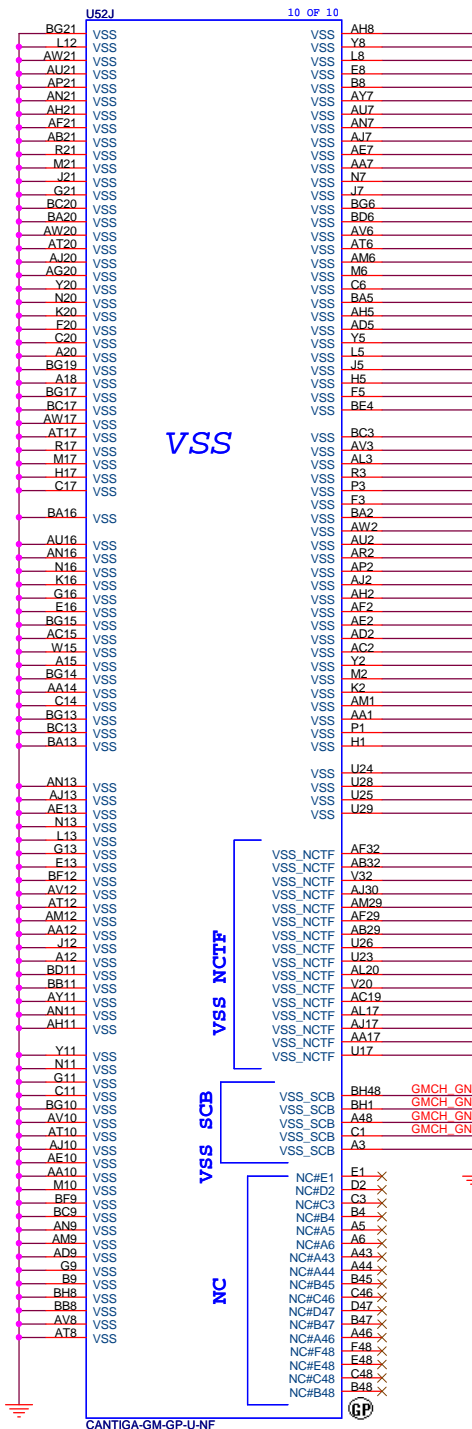
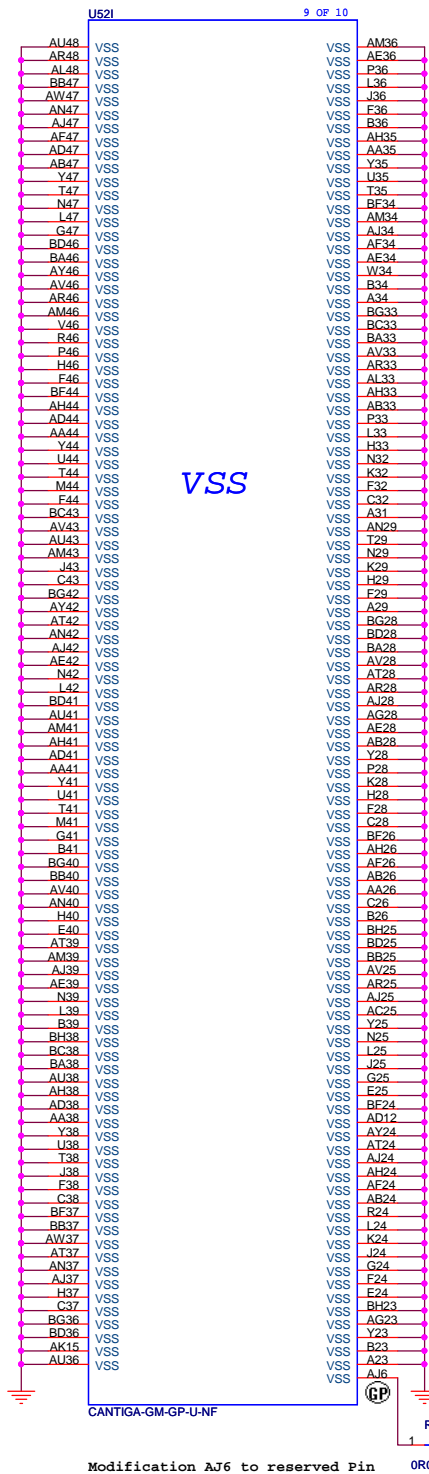
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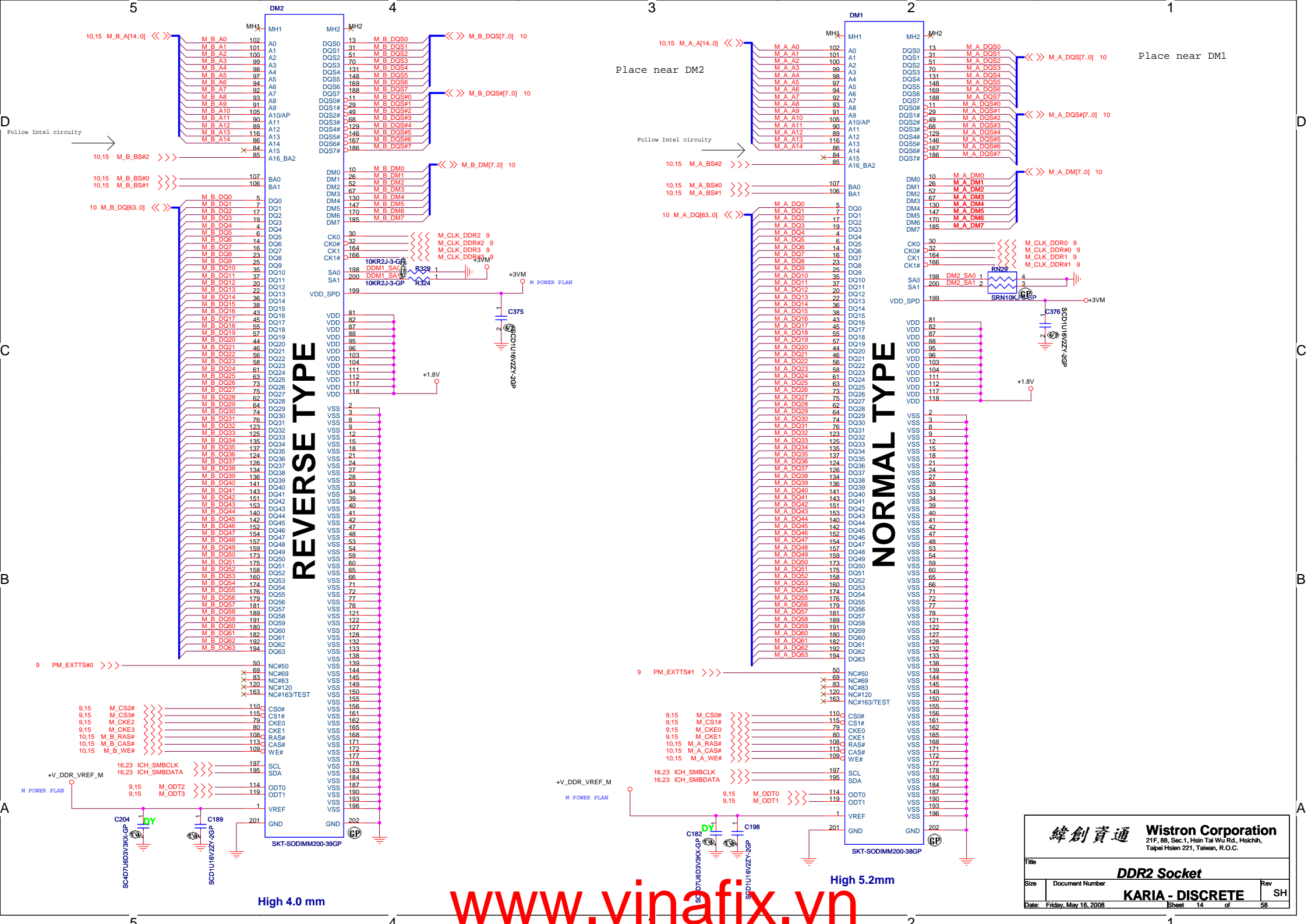
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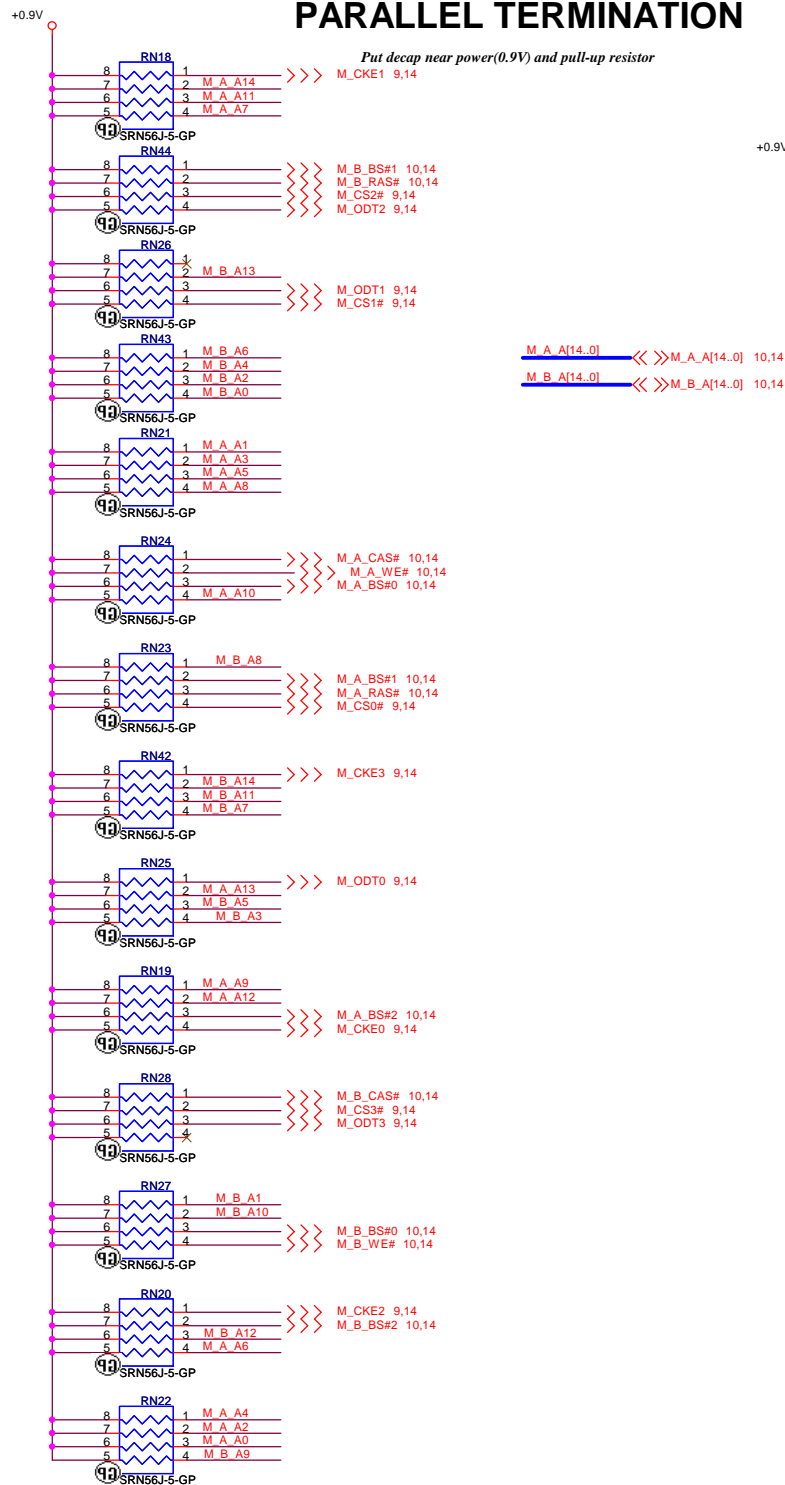




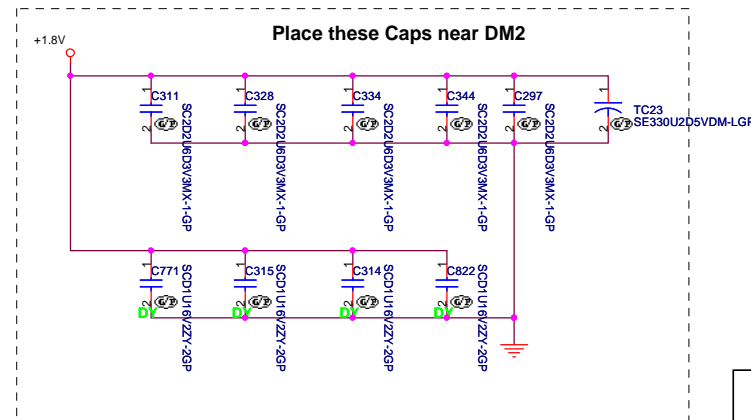
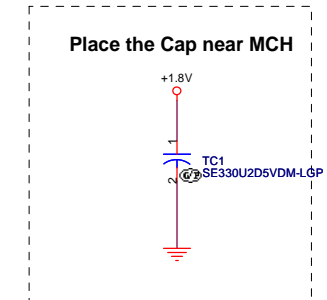
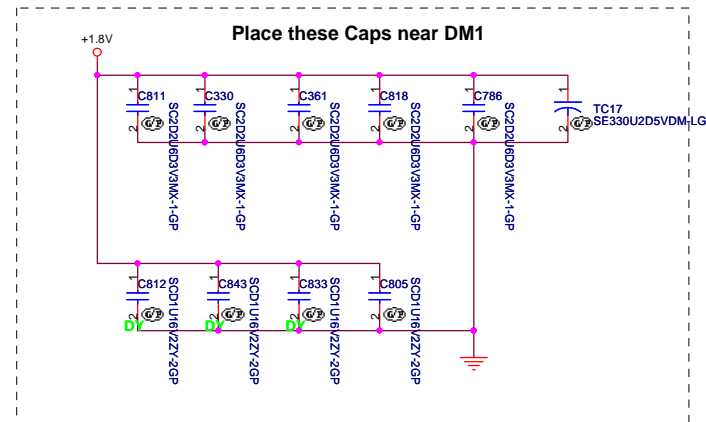
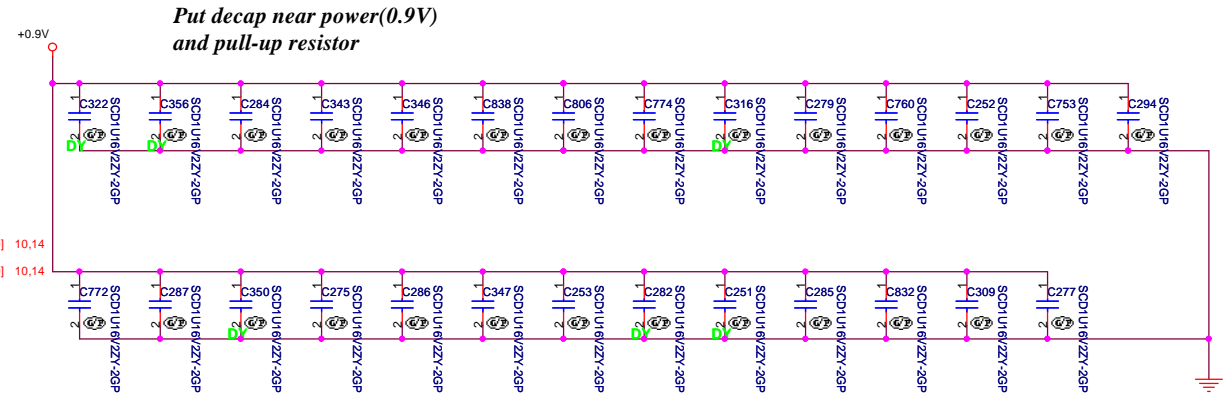
NCTF PIN



PARALLEL TERMINATION



Decoupling Capacitor




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Title			
DDR2 Termination Resistor			
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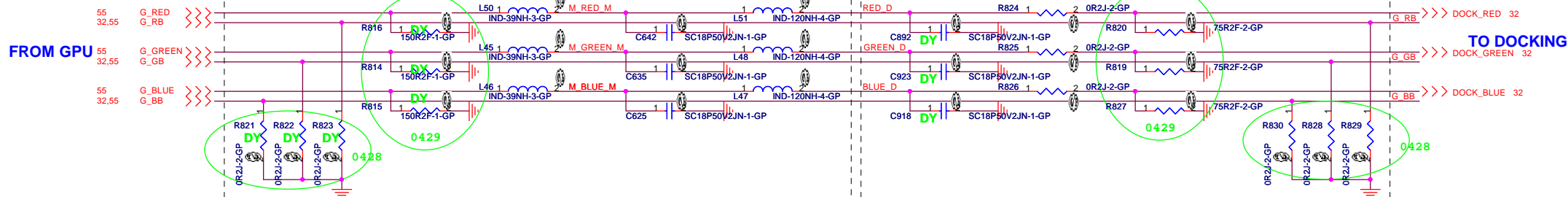
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Clock Generator		
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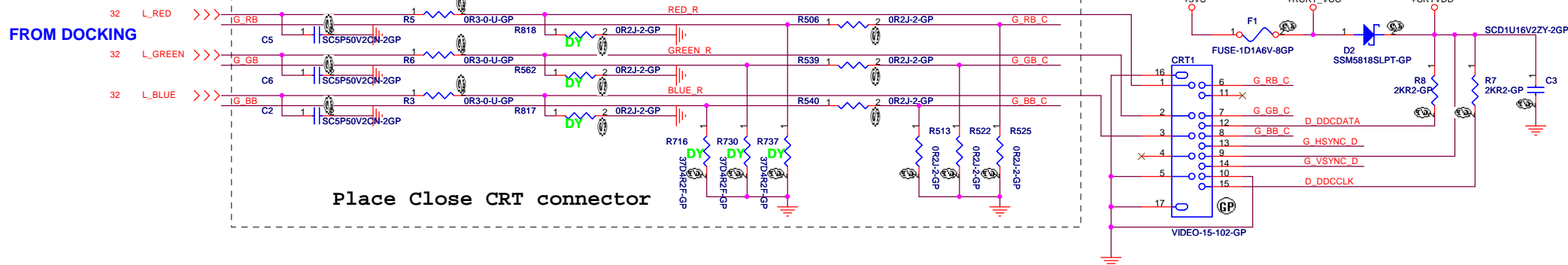
CRT

CRT Termination/EMI Filter

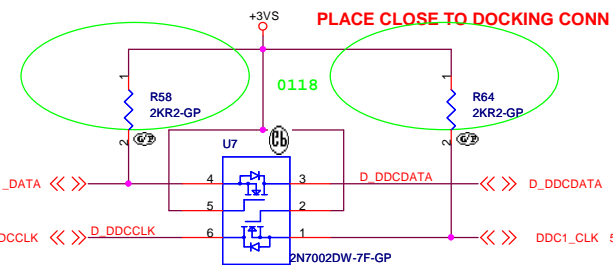
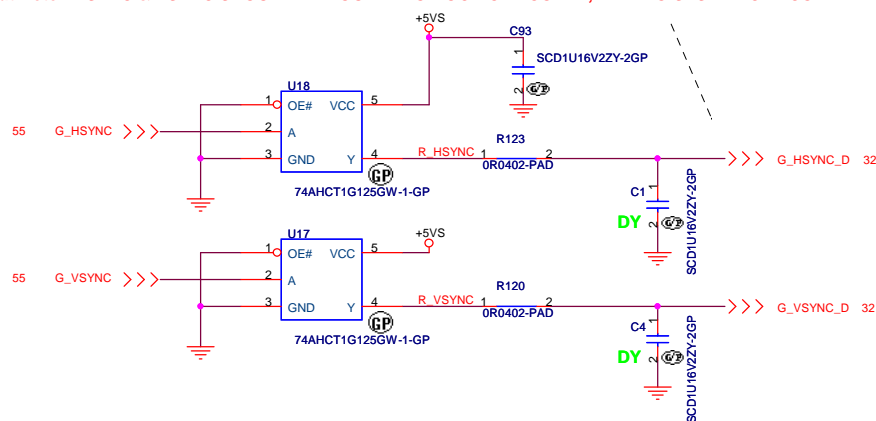
Place Close VGA Chip



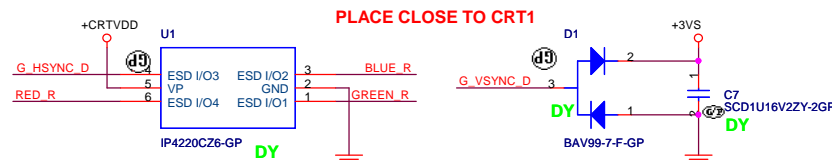
FROM DOCKING



Layout Note : HSYNC & VSYNC SHOULD BE ROUTED TO DOCK CRT CONN., THEN TO SYSTEM CRT CONN.

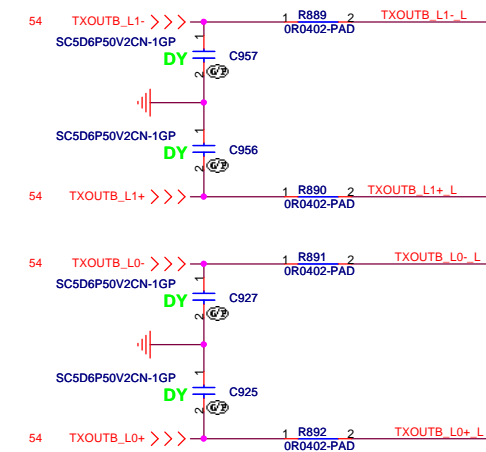
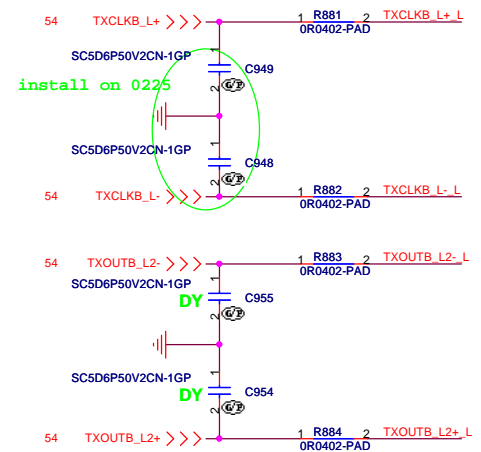
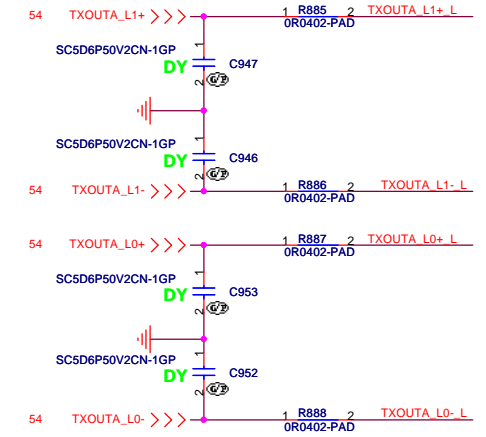
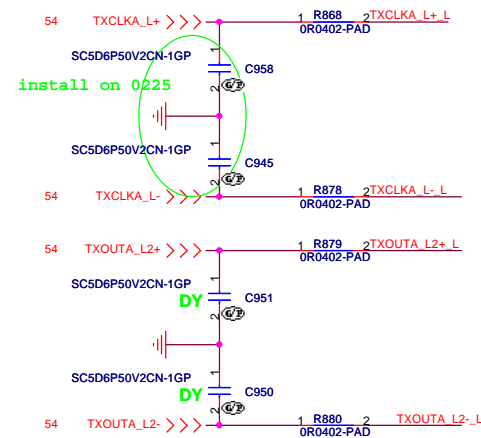
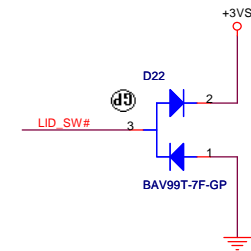
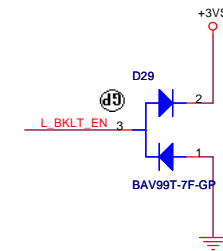
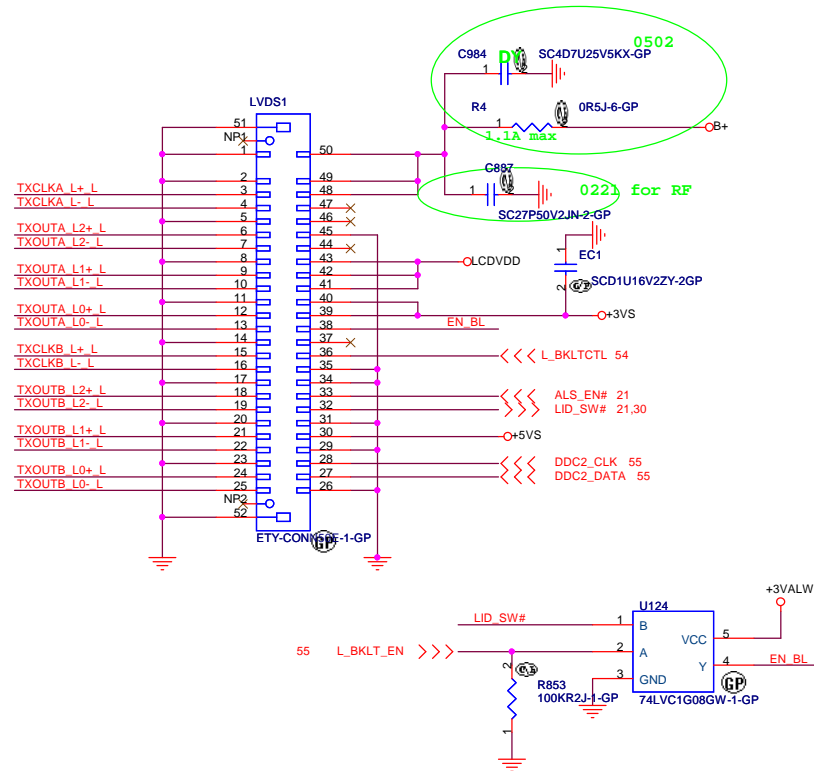


PLACE CLOSE TO CRT1

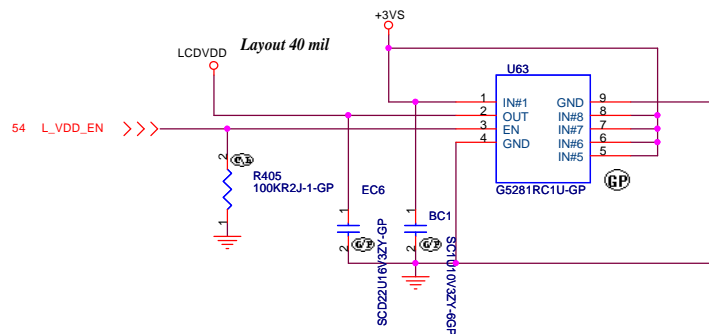


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Title			
CRT CONNECTOR			
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LVDS CONN



LCD POWER CIRCUIT

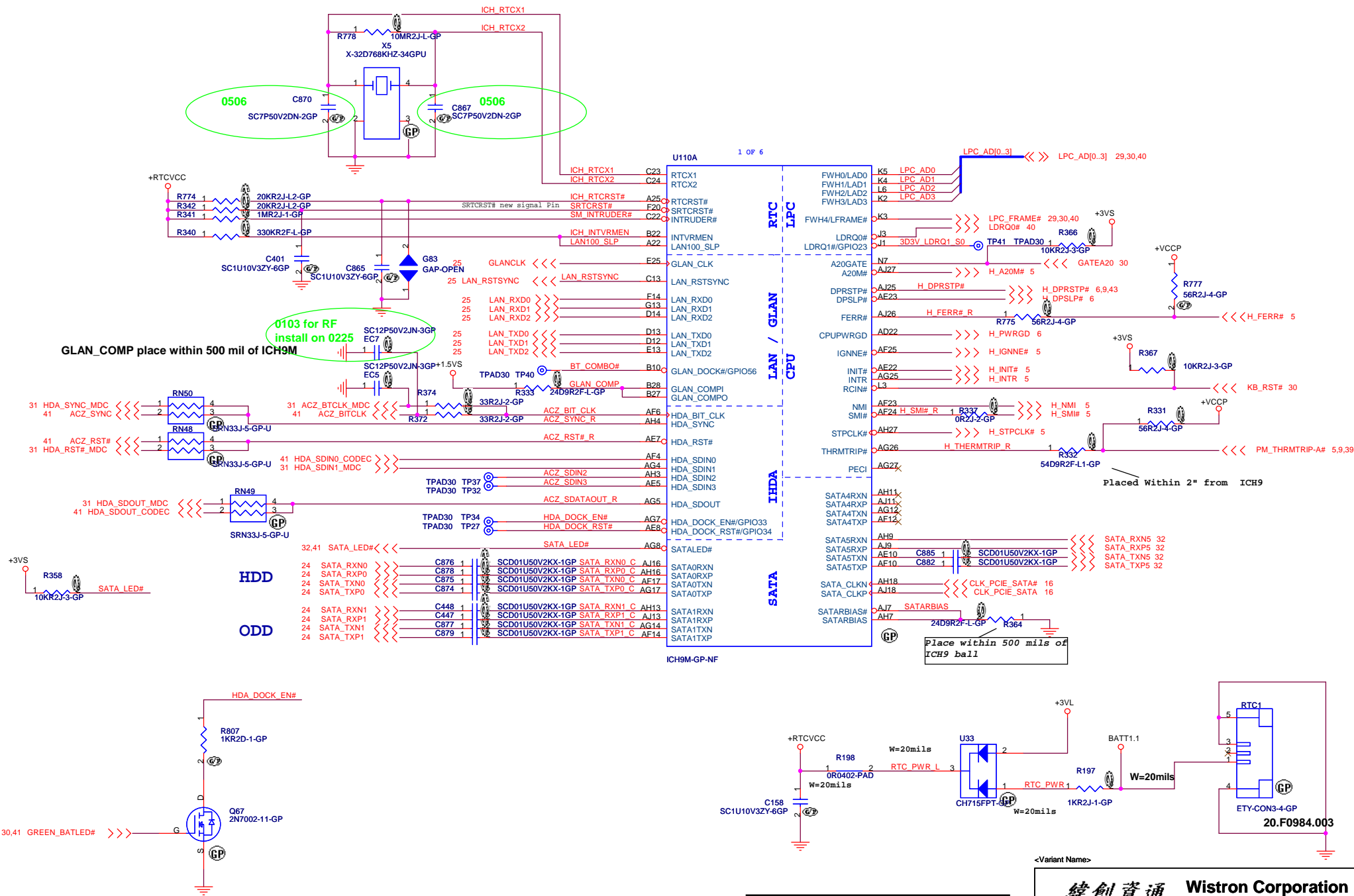


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Diagram illustrating the PLT_RST# signal path. The signal originates from the PCI PLTRST# input, passes through a 74VLC1G08GW-1-GP inverter (U113), and is then connected to the PLT_RST# output (9.27,29,40,41,54) via a 0R2J-2-GP resistor (R82) and a 100k resistor (R797) to ground.



integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

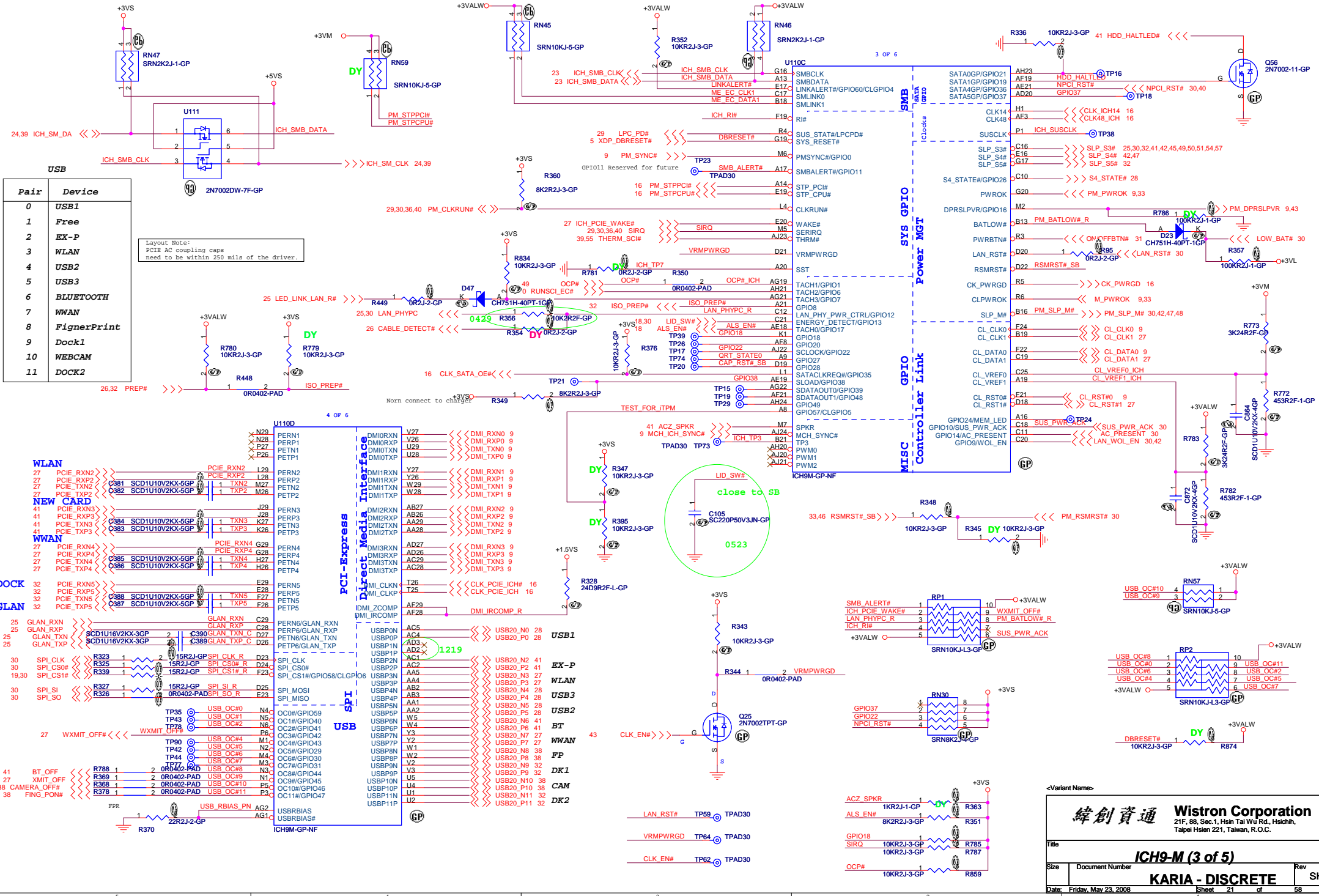
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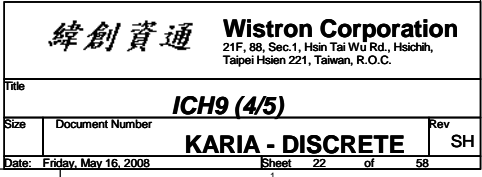
緯創資通 Wistron Corporation
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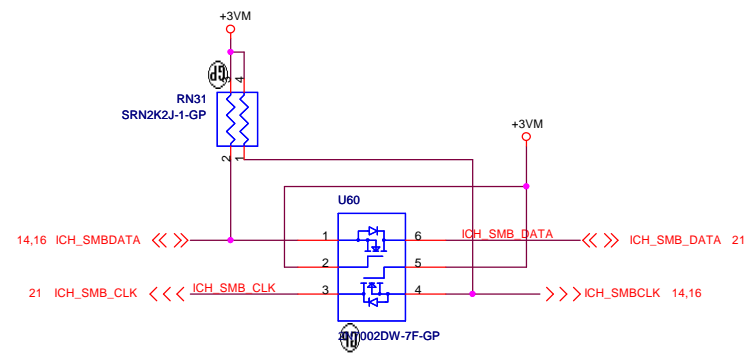
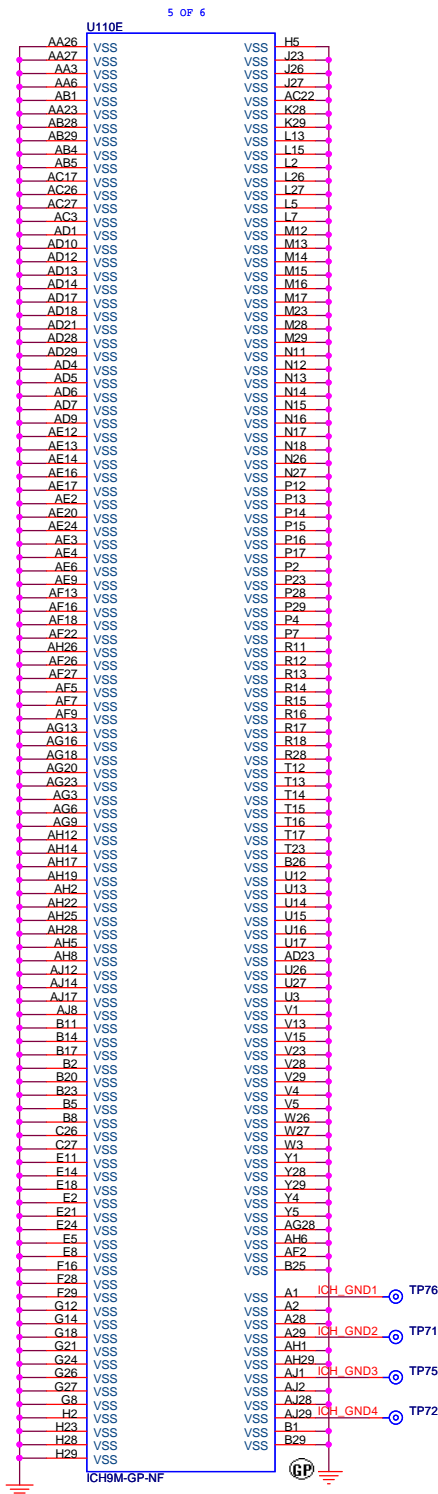
ICH9-M (2 of 5)

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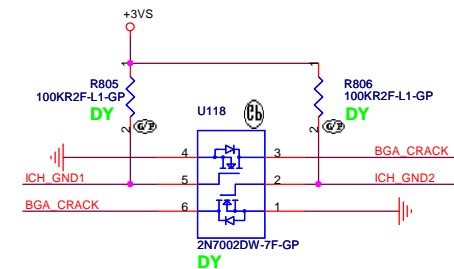
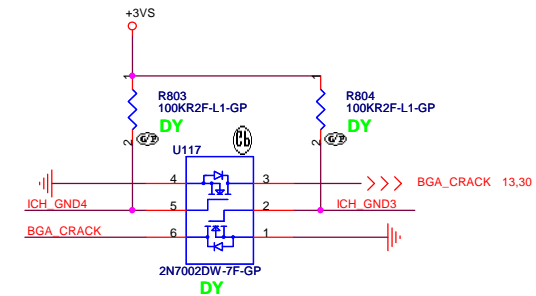






Q13 & Q14 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance

SMBUS



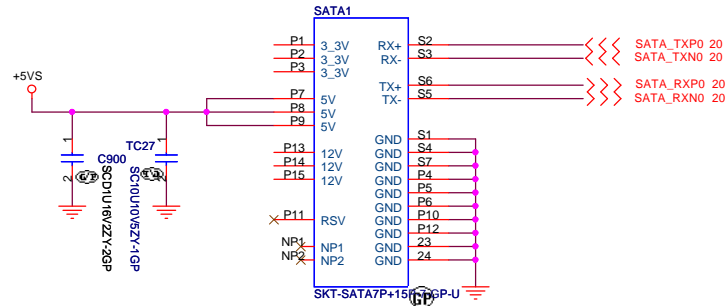
緯創資通

Wistron Corporation

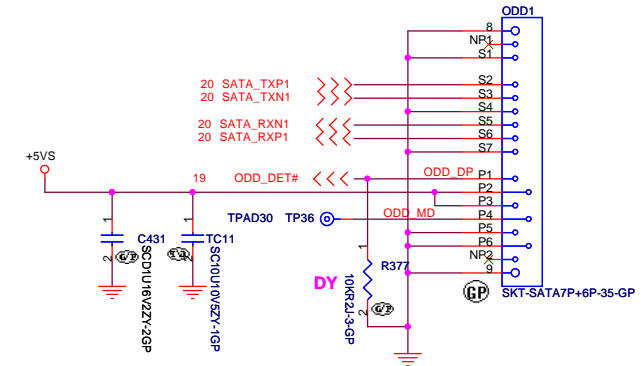
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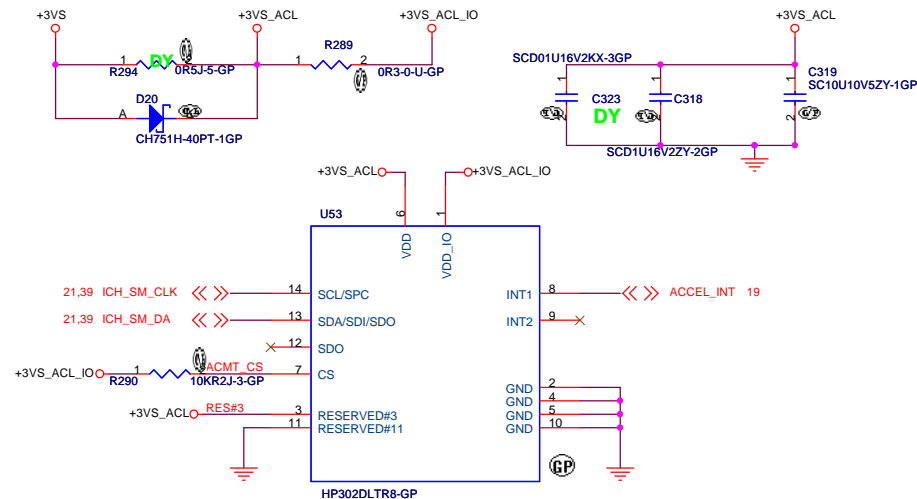
SATA HD Connector



ODD Connector



ACCELEROMETER

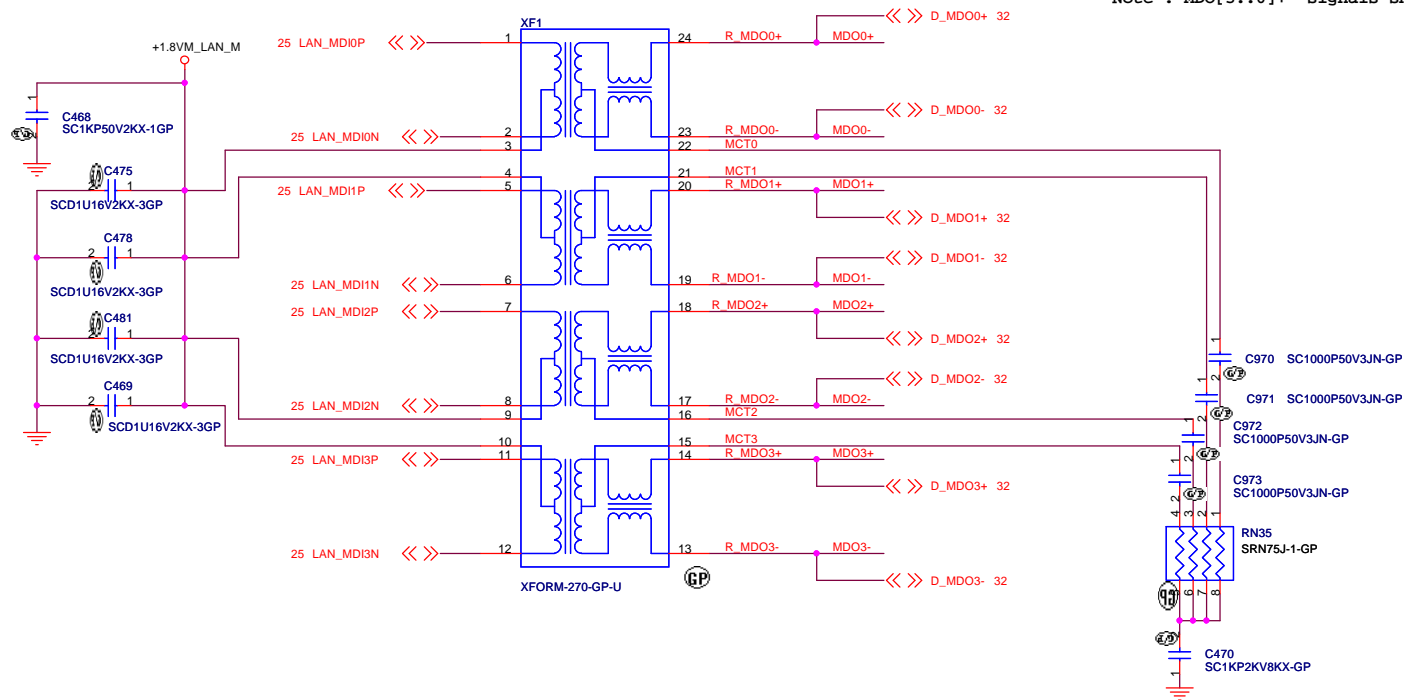


Must be placed in the center of the system

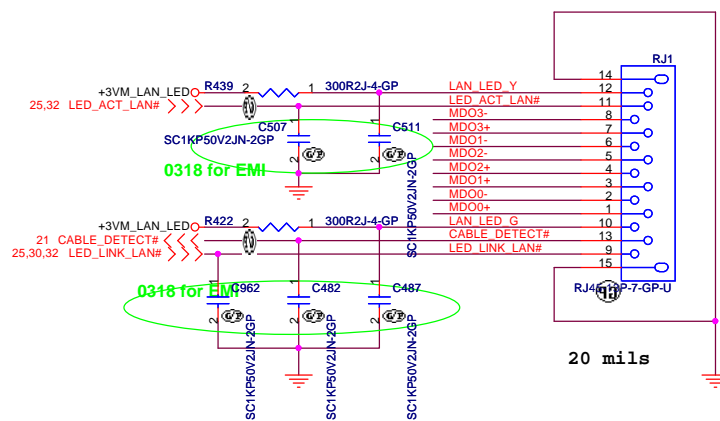
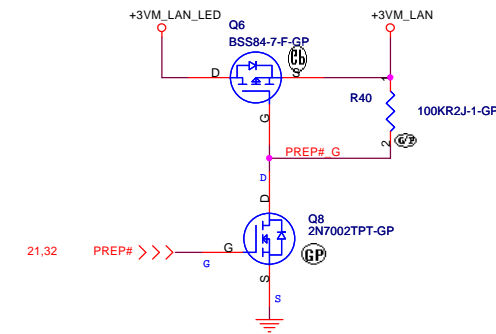
www.vinafix.vn

<Variant Name>

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HDD/ODD/ACCELEROMETER	
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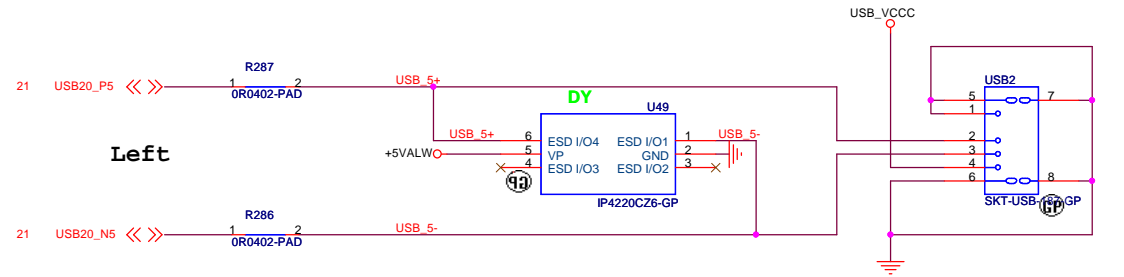
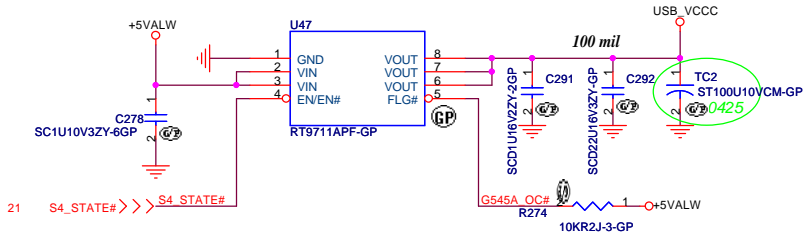
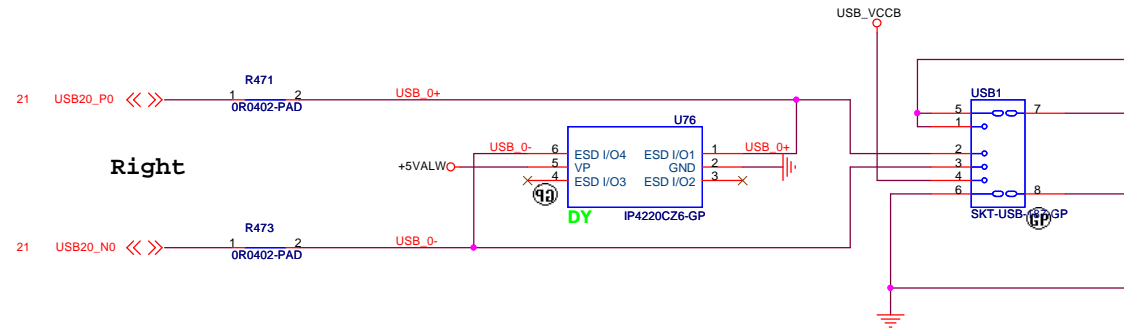
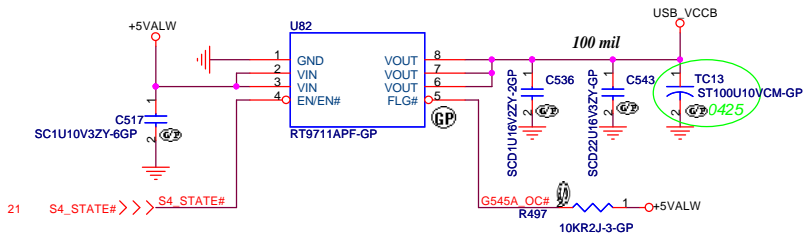
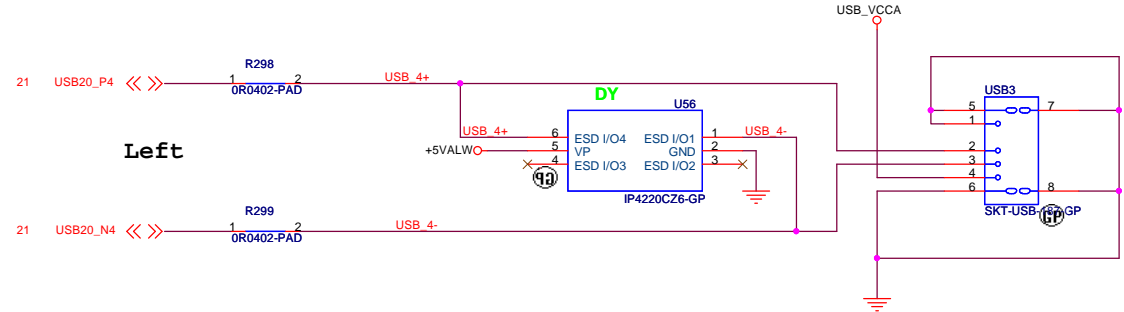
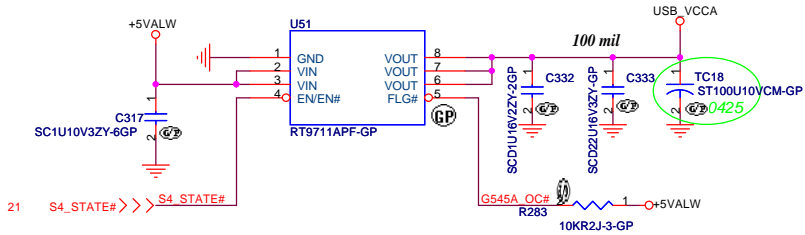


LAN ENERGY DET

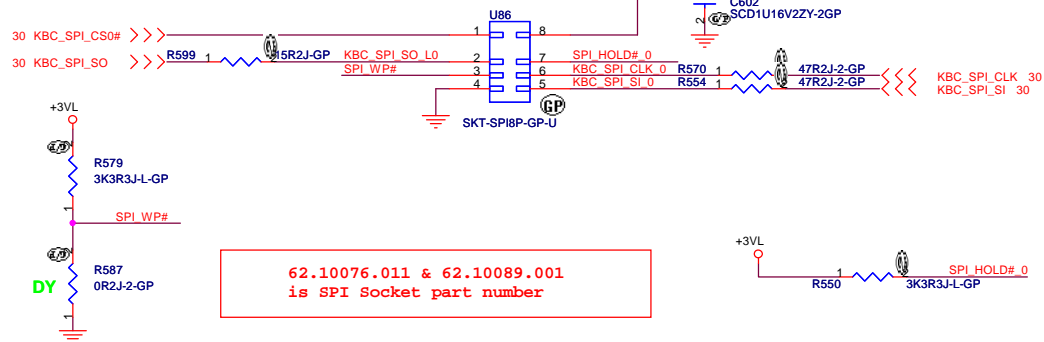


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<Variant Name>		緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		Magnetic & RJ45	
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32Mb x 1

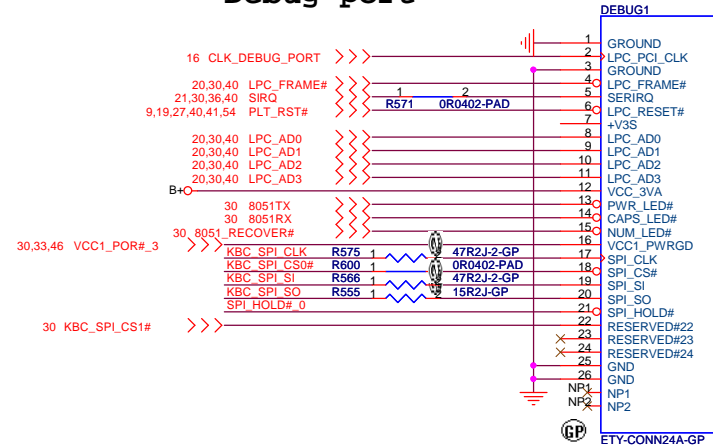


62.10076.011 & 62.10089.001
is SPI Socket part number

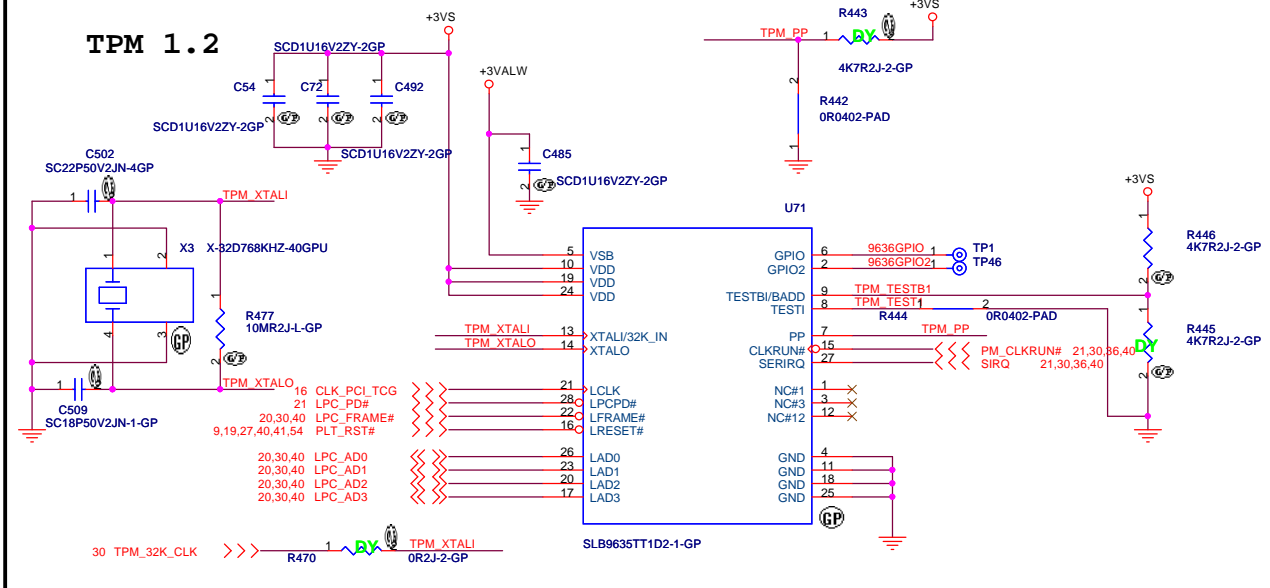
32M SPI
> 72.25325.A01 MXIC MX25L3205D
32M SPI
> 72.26321.A01 IC FEROM AT26DF321-SU, by Atmel

Keep traces of SPI as short as possible and keep trace spacing close to 7mils to any other signal (basically follow specs).

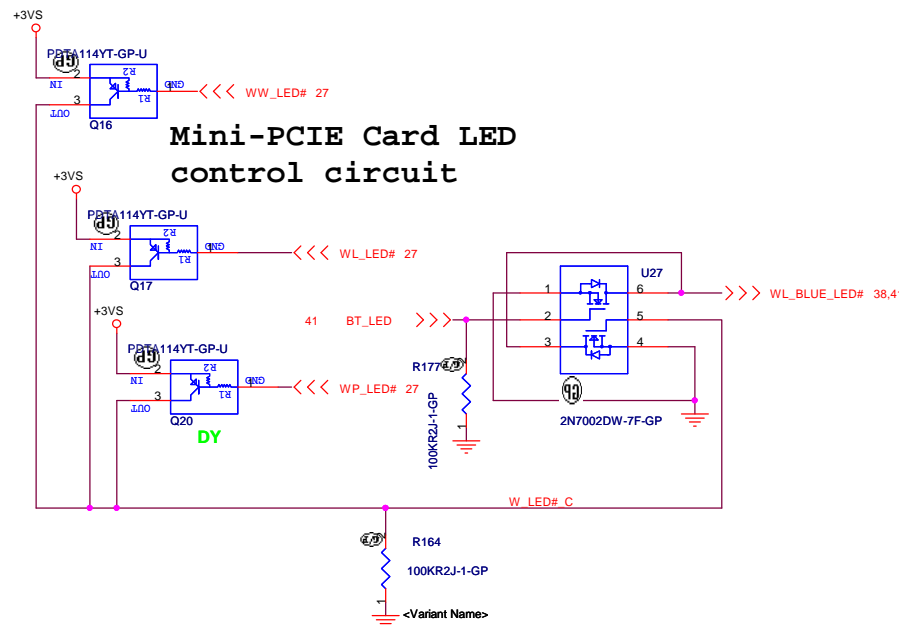
Debug port



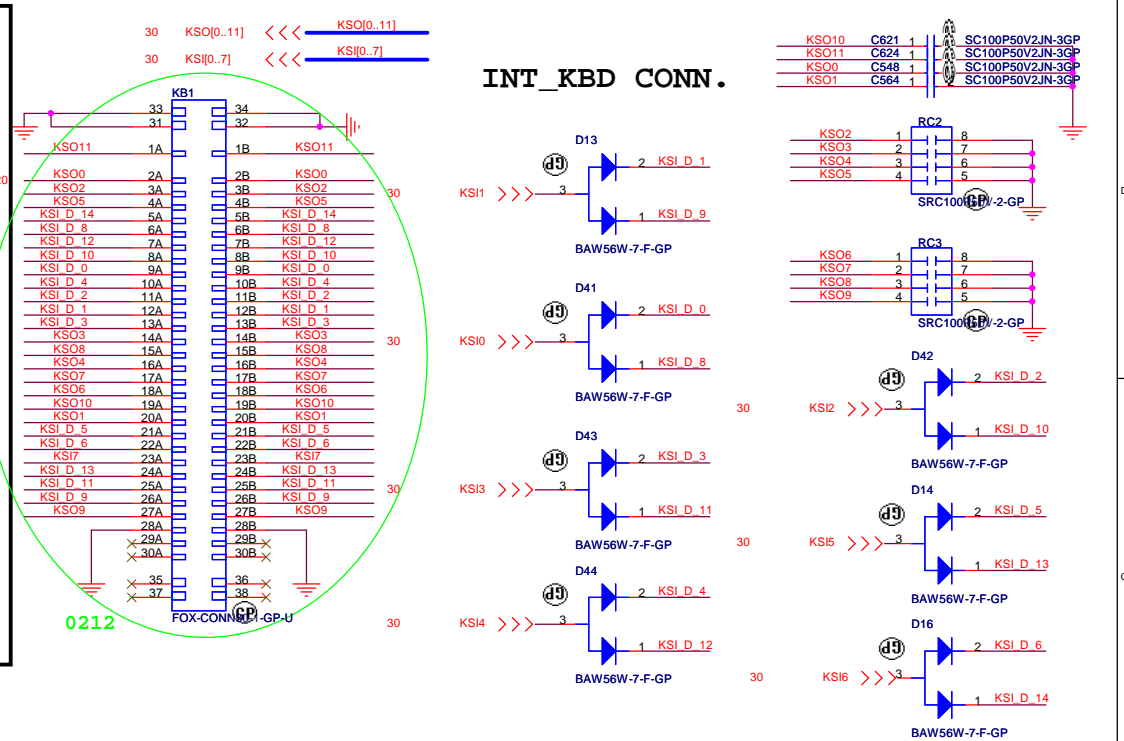
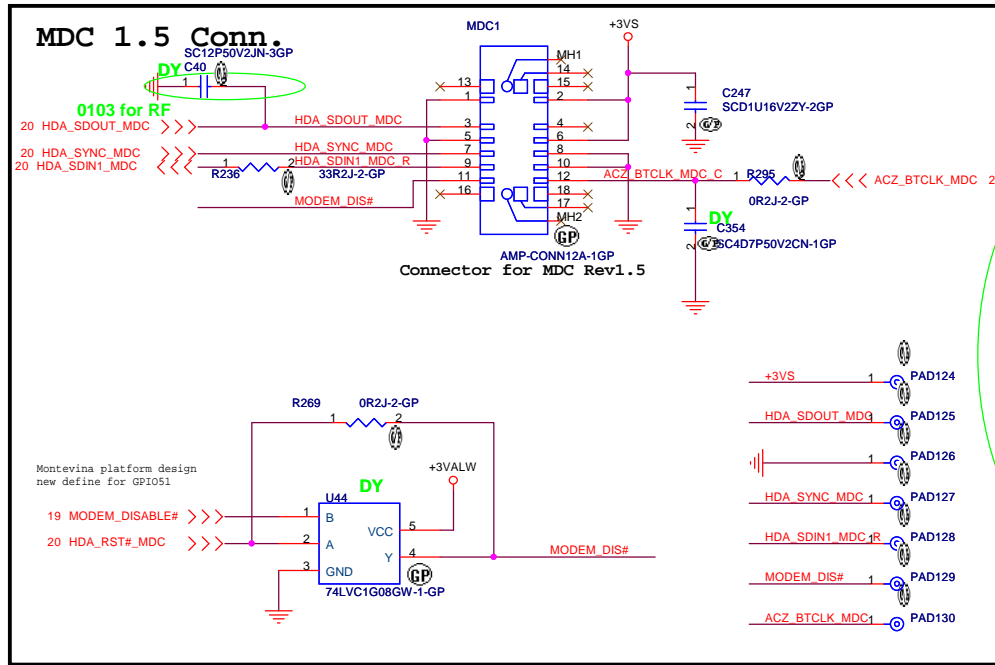
TPM 1.2



Mini-PCIE Card LED control circuit

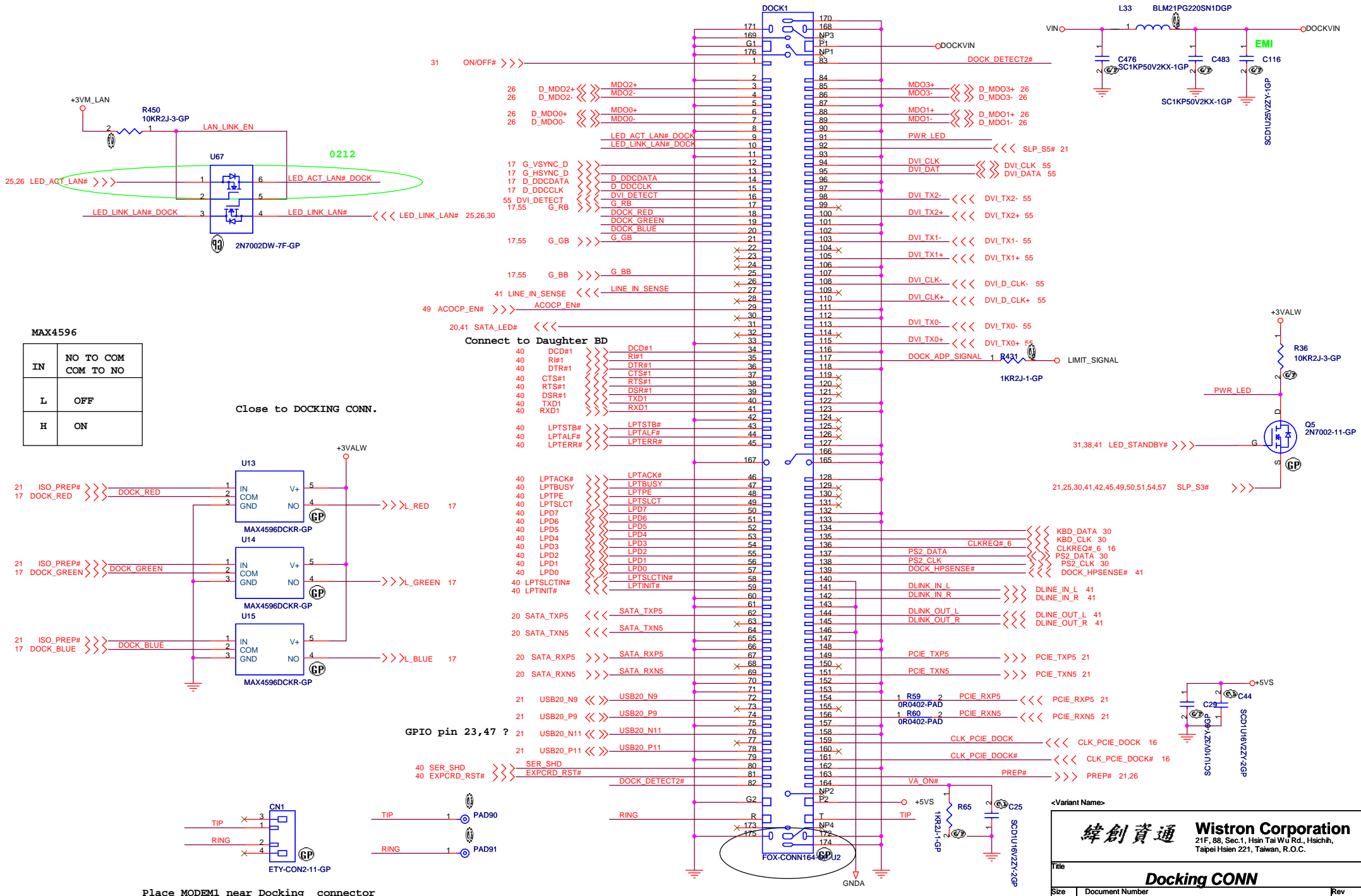


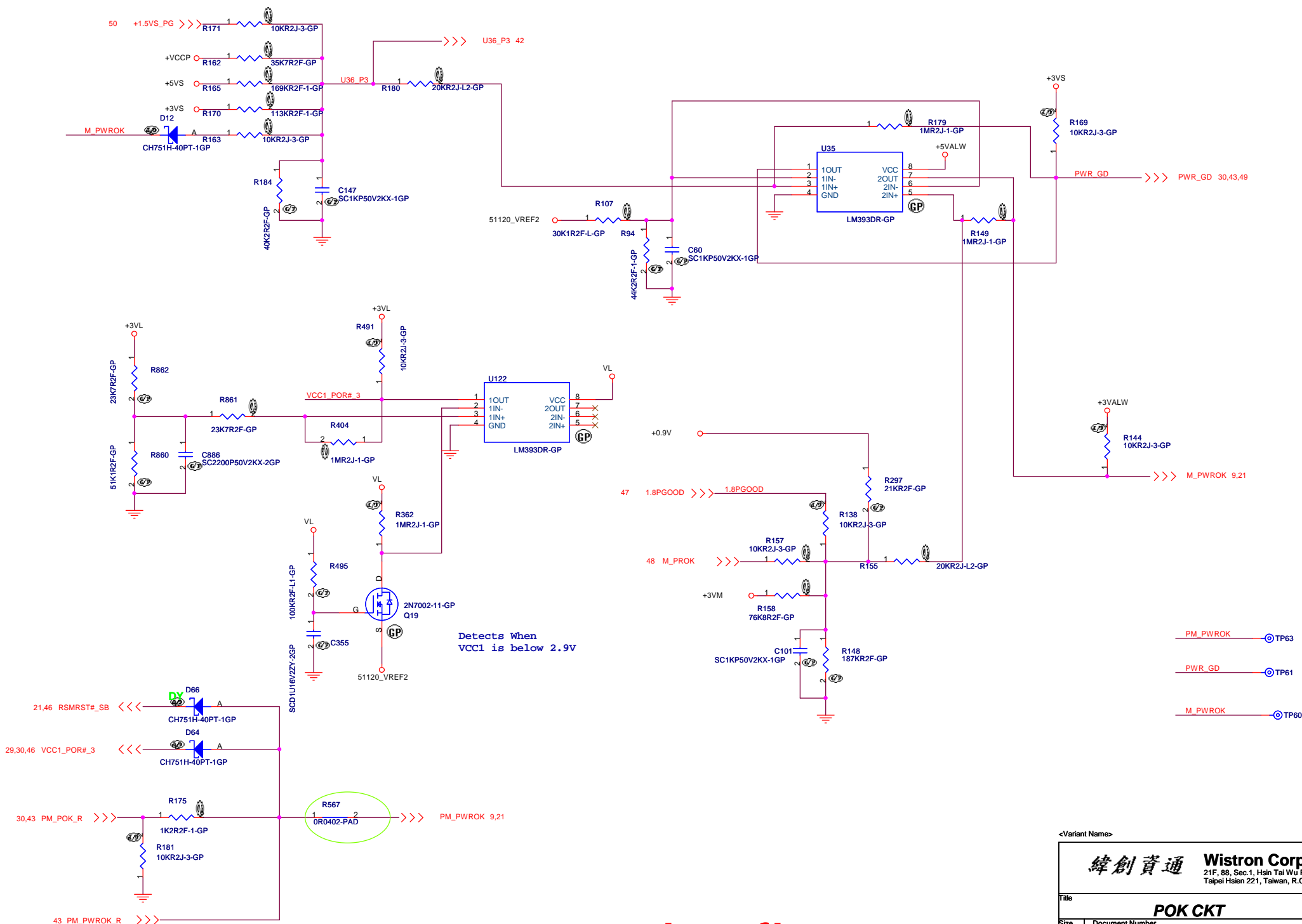




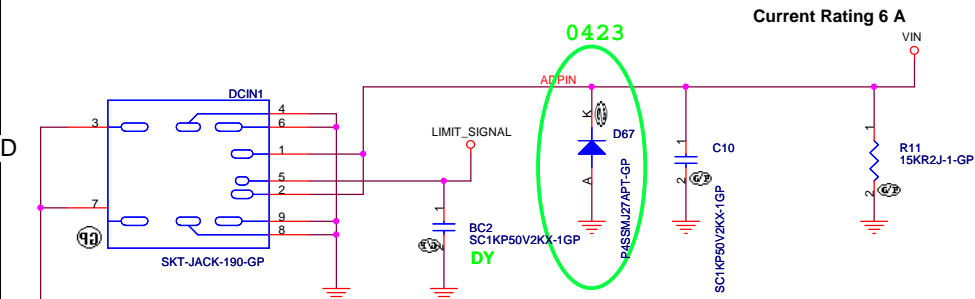
Docking CONN. 164 PIN

current rating 6A



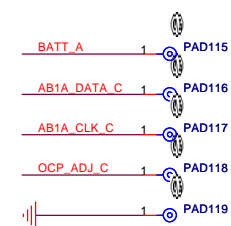
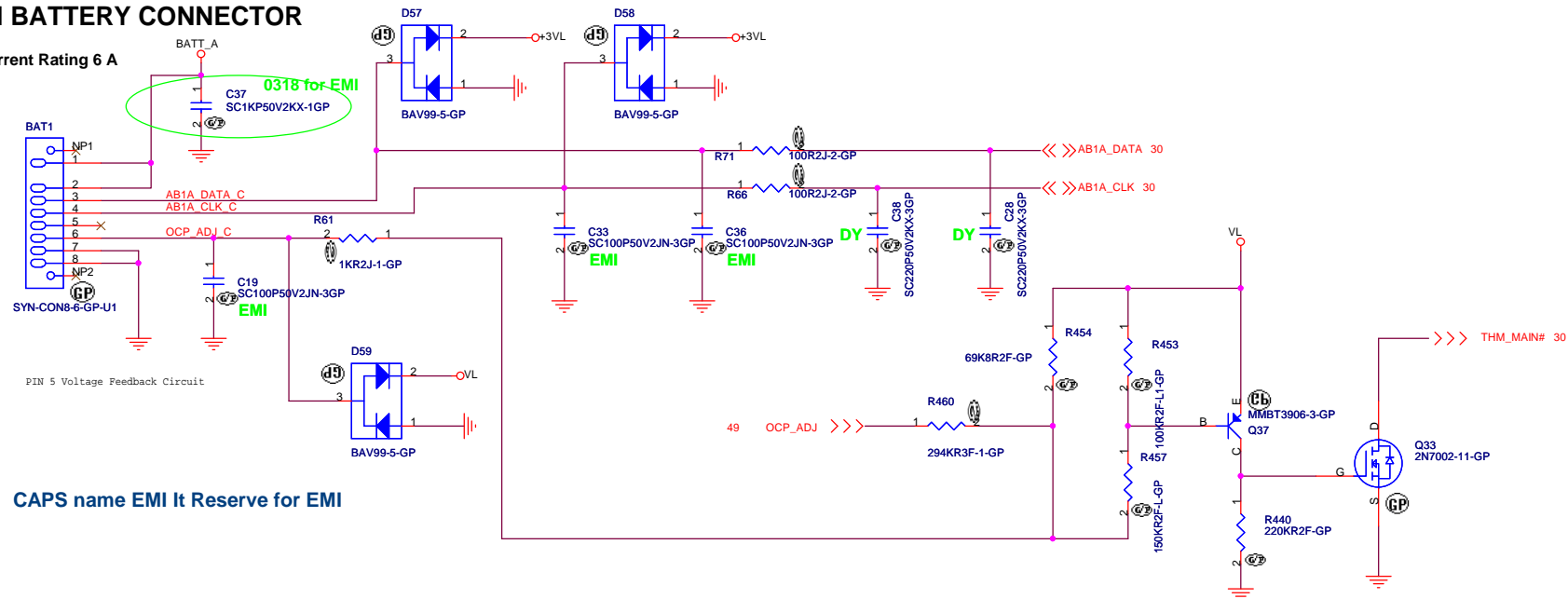


Adaptor in to generate DCBATOUT



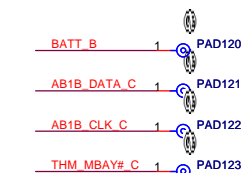
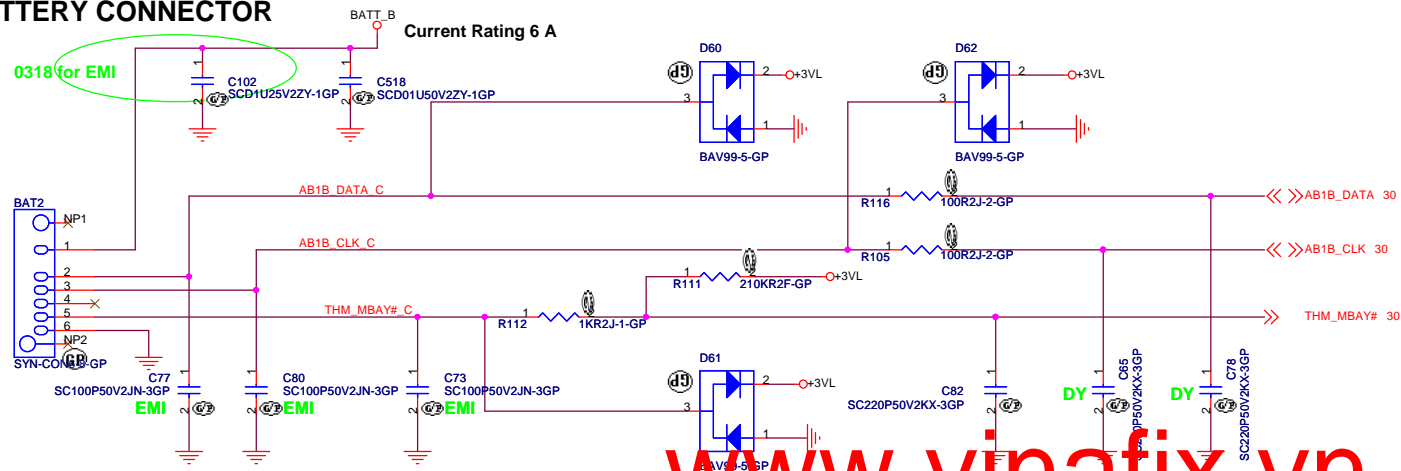
MAIN BATTERY CONNECTOR

Current Rating 6 A



BAY BATTERY CONNECTOR

Current Rating 6 A

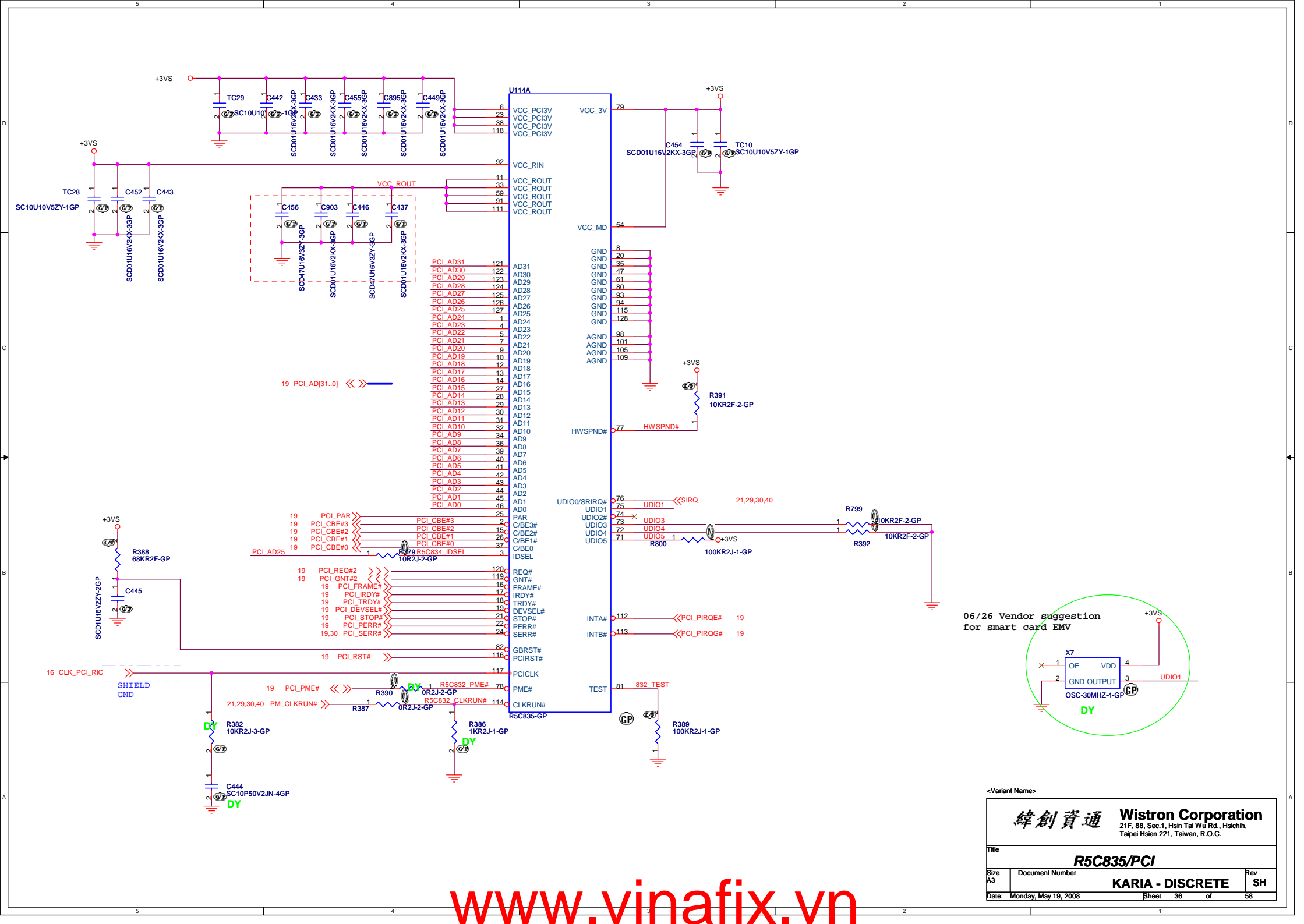


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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
DC & BATTERY CONN.	
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Taipei Hsien 221, Taiwan, R.O.C.

Title

R5C835/PCI

Size
A3

Document Number

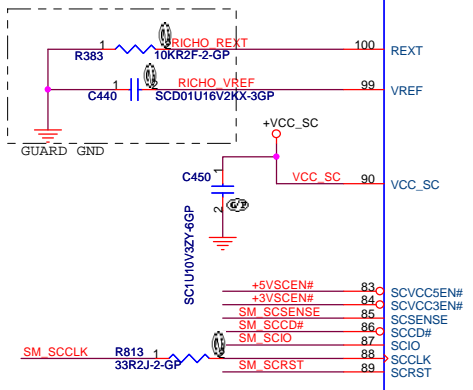
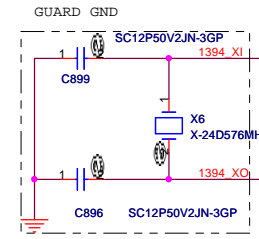
KARIA - DISCRETE

Rev
SH

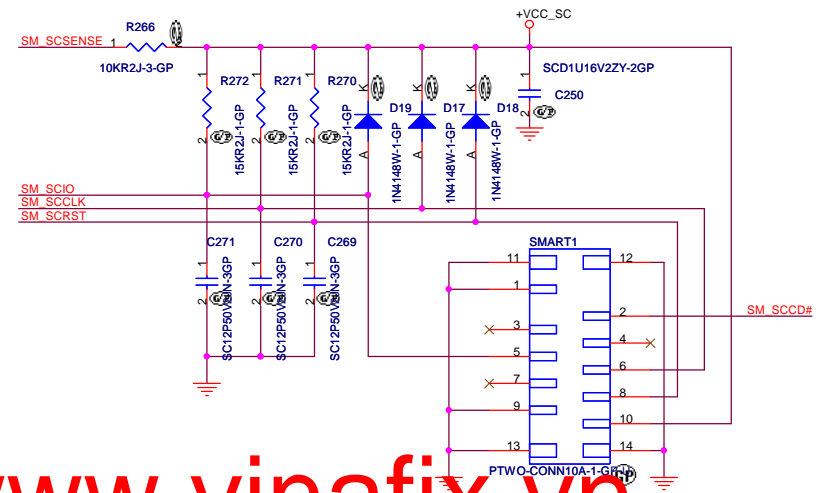
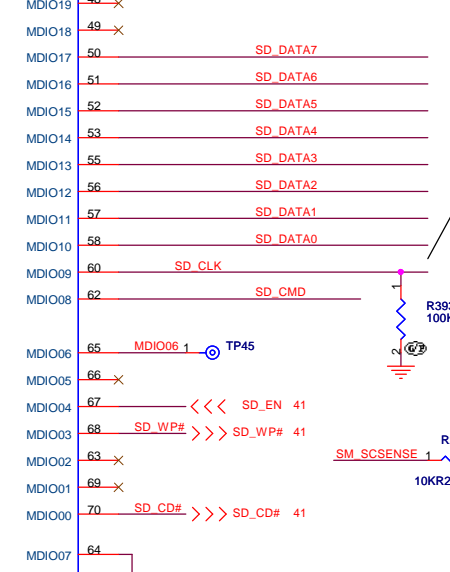
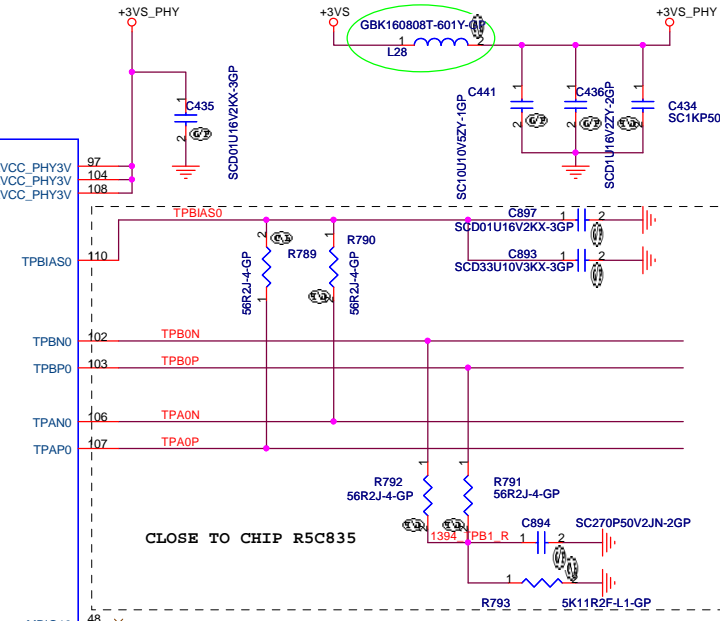
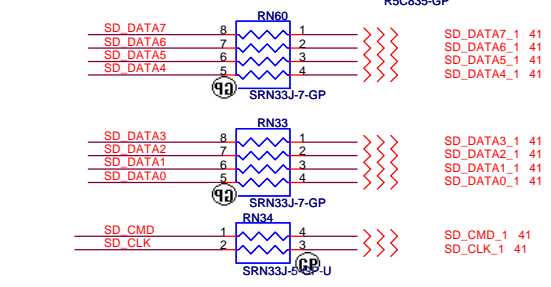
Date: Monday, May 19, 2008

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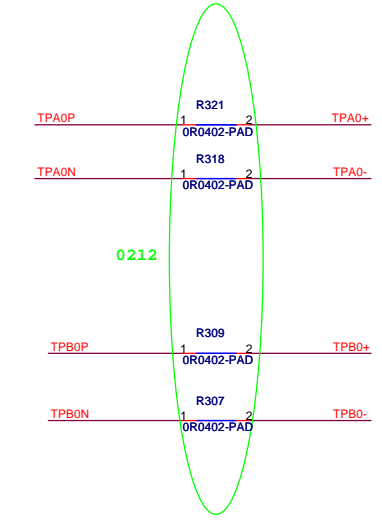
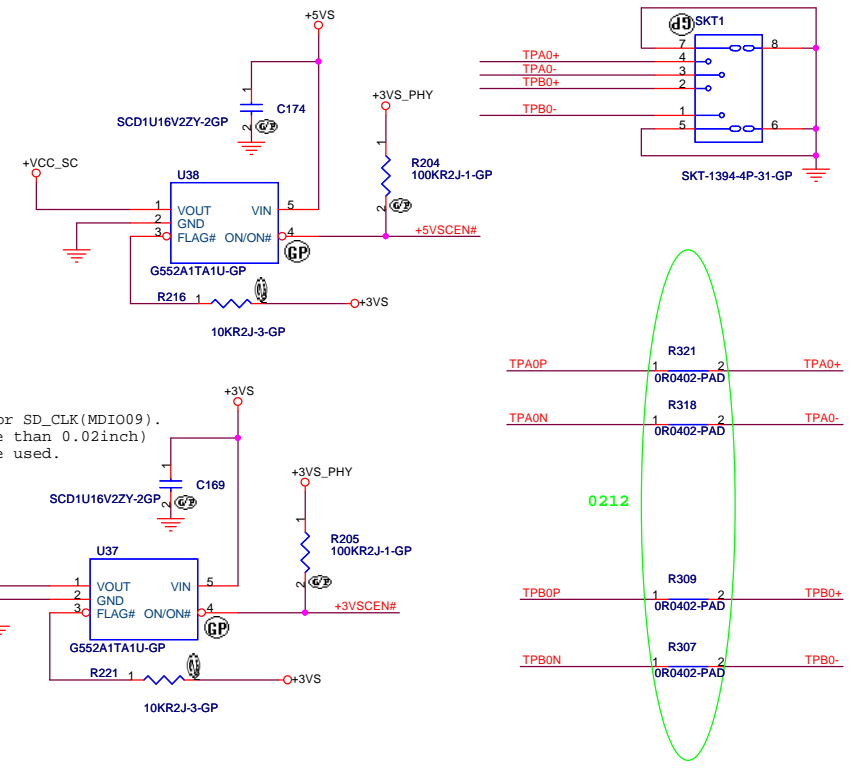


Layout notes :
external parts for
VREF, REXT and FIL0 as
close as possible to R5C833.

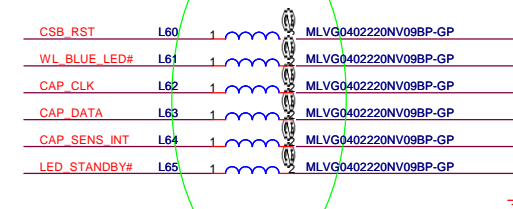
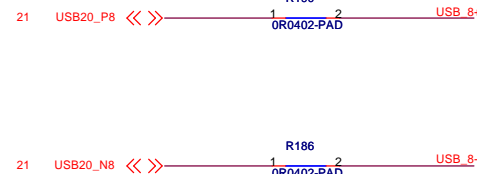
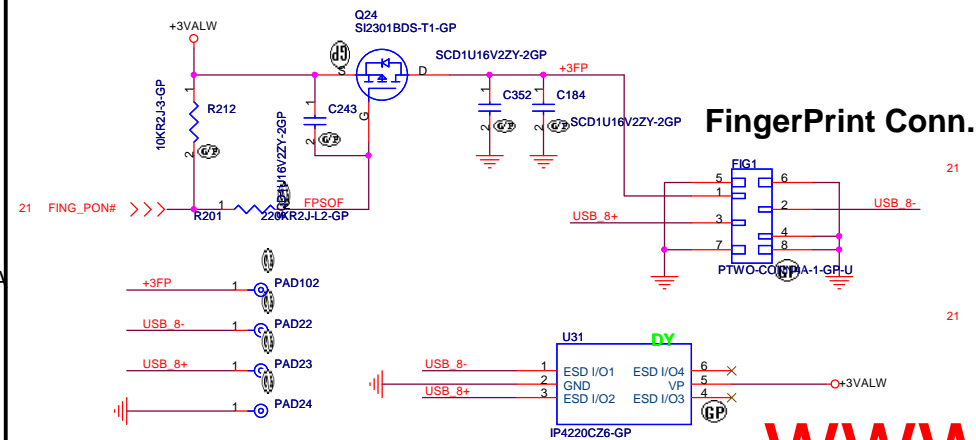
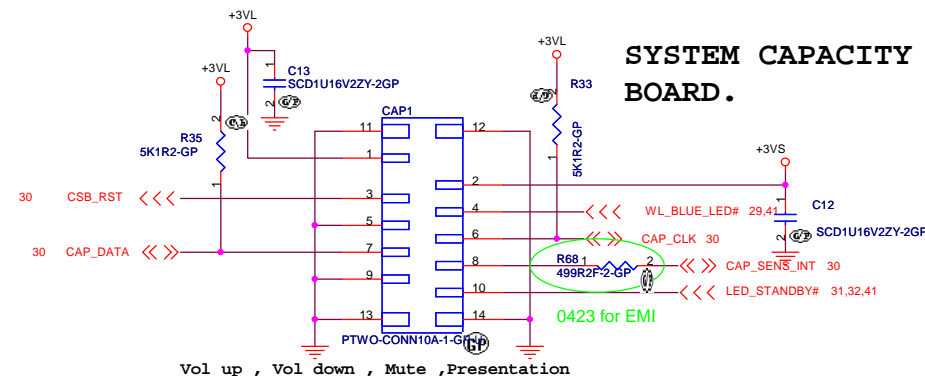
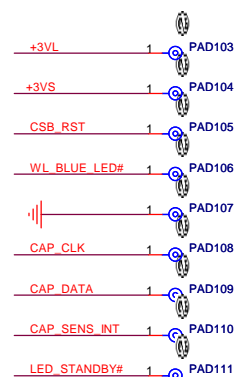
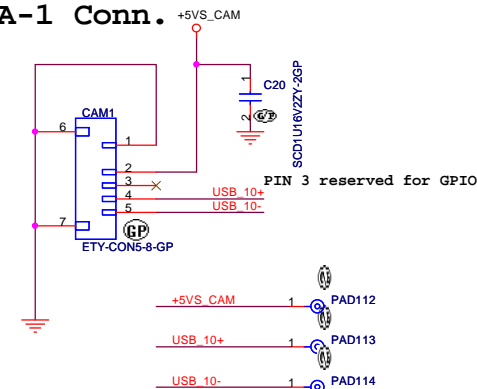
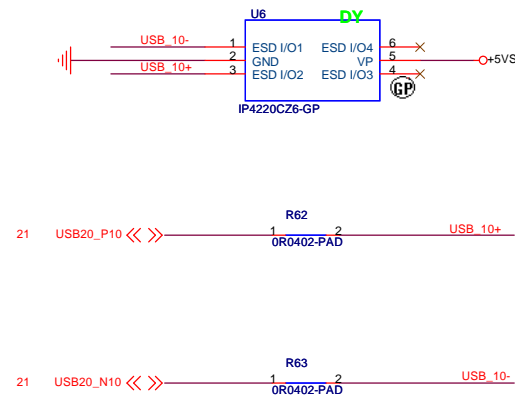
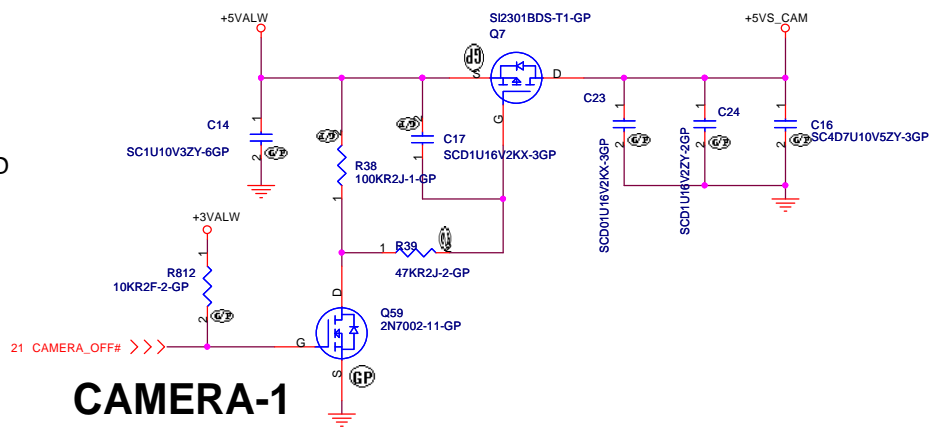


The shield GND is needed for SD_CLK(MDIO09).
Also, the wide-width (more than 0.02inch)
trace for MDIO09 should be used.

Layout notes :
1394
=====GND-
-----TPB0-
-----TPB0+
=====GND-
-----TPA0-
-----TPA0+
=====GND



<div> <div>緯創資通</div> <div>Wistron Corporation</div> <div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div> </div>			
Title			
R5C835/1394/SD/Smart			
Size	Document Number	Rev	
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4

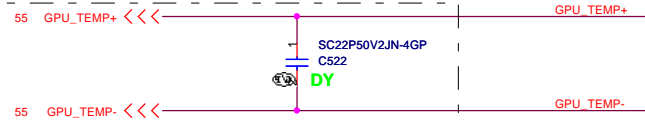
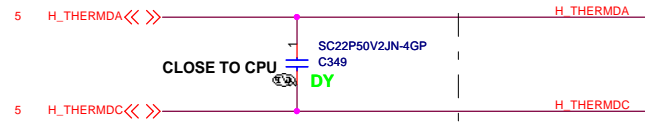
3

2

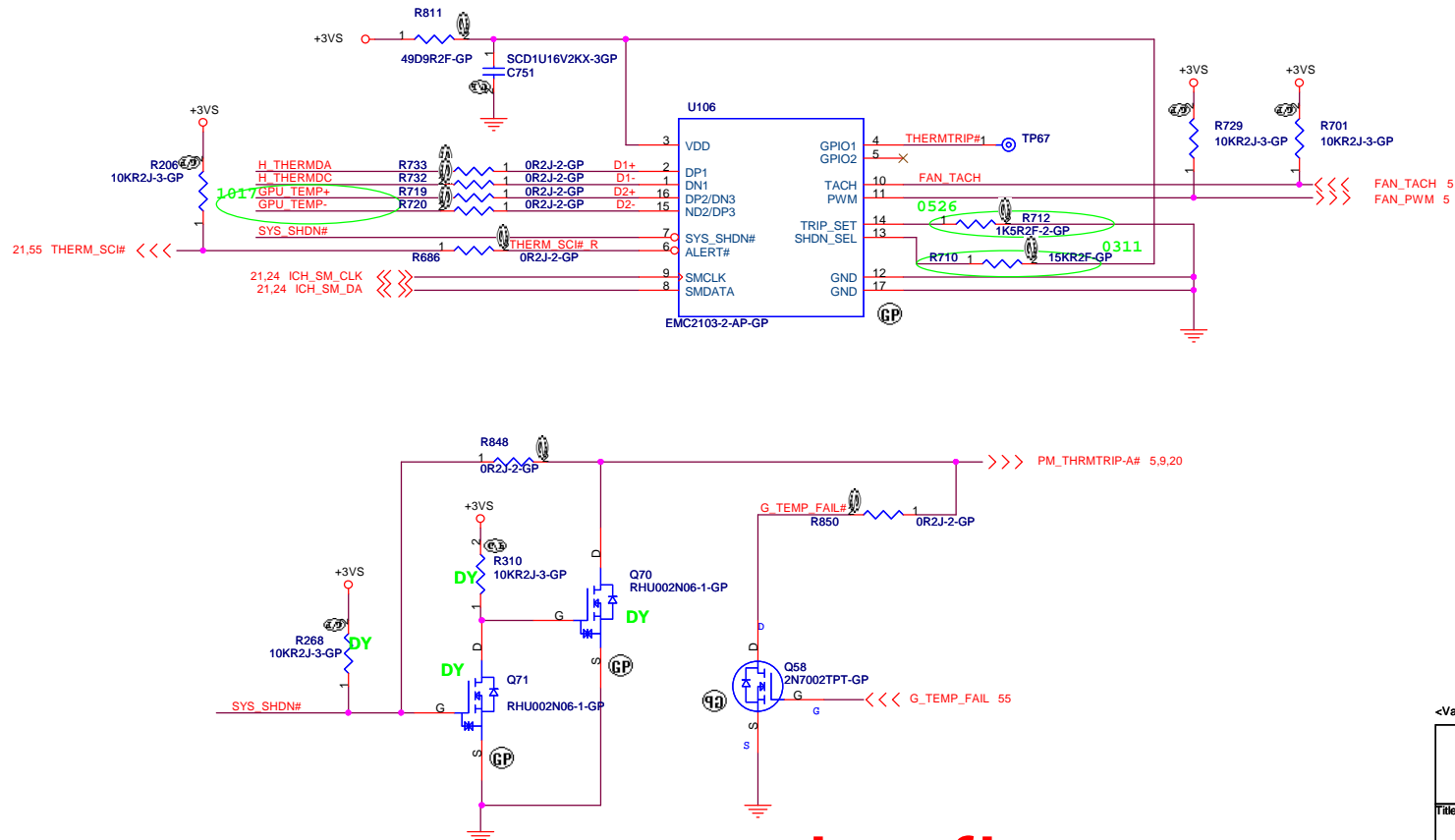
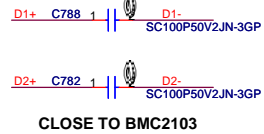
1

CPU TEMP:

H_THERMDA and H_THERMDC routing 10mil trace width and spacing. Locate Capacity near thermal diode



GPU DIE TEMP:
REMOTE2+ and REMOTE2- routing 10mil trace width and 10 mil spacing.



<Variant Name>

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Title

ADT7473 Thermal Sensor

Size

A3

Document Number

KARIA - DISCRETE

Rev

SH

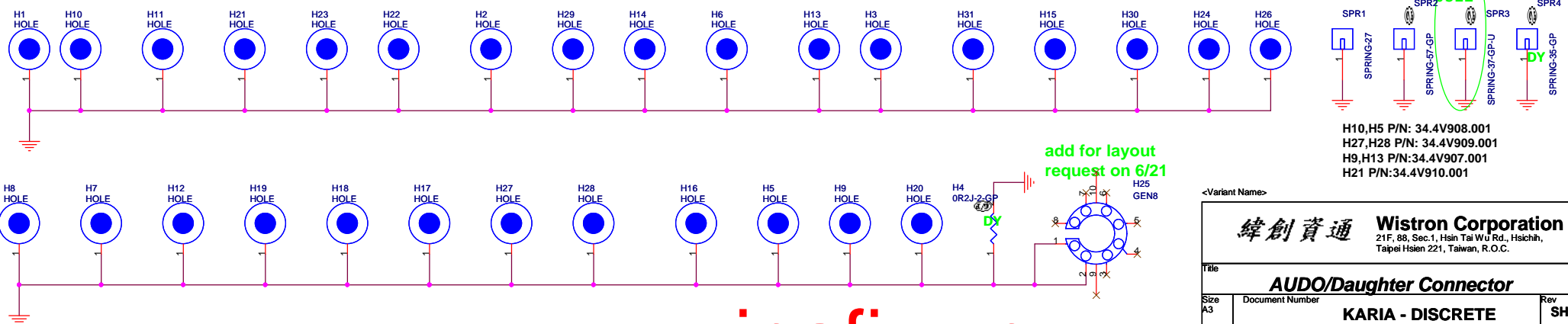
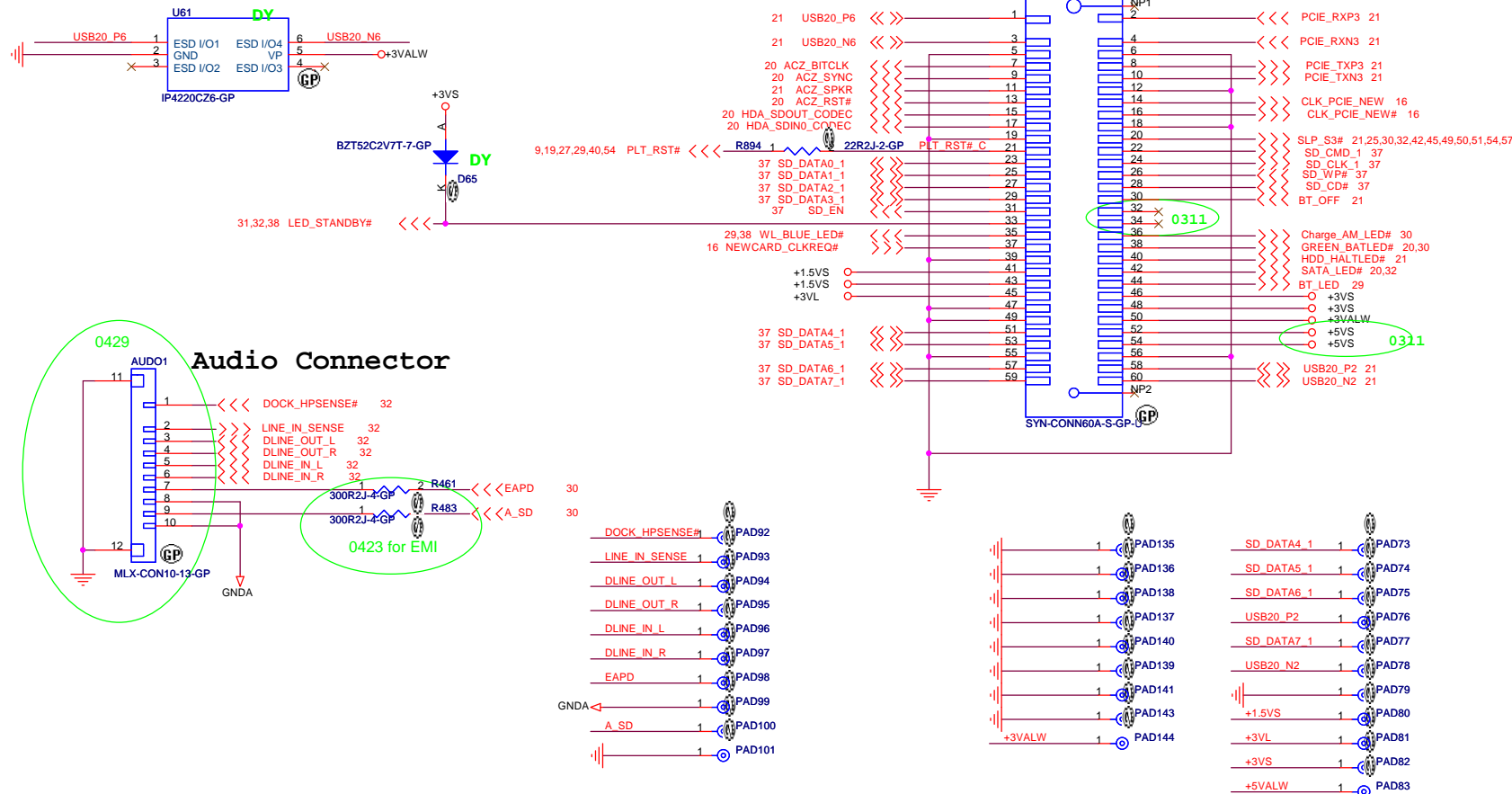
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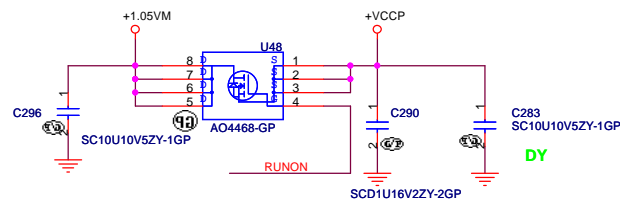
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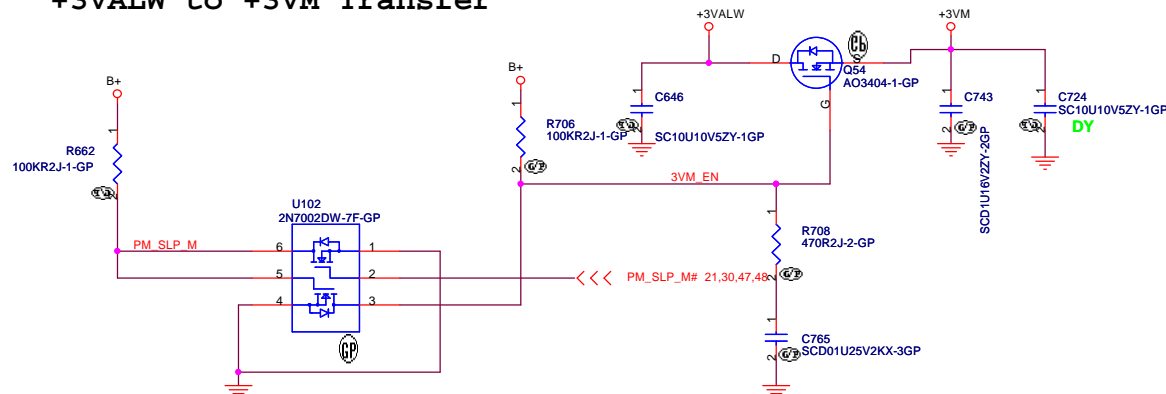
Daughter Board Connector



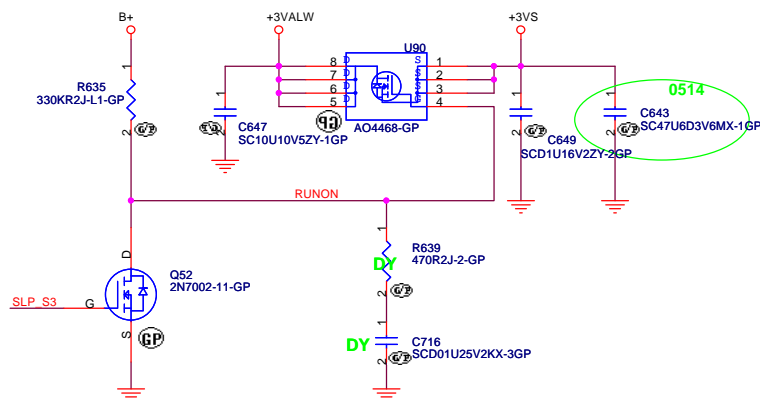
+1.05VM to +VCCP Transfer



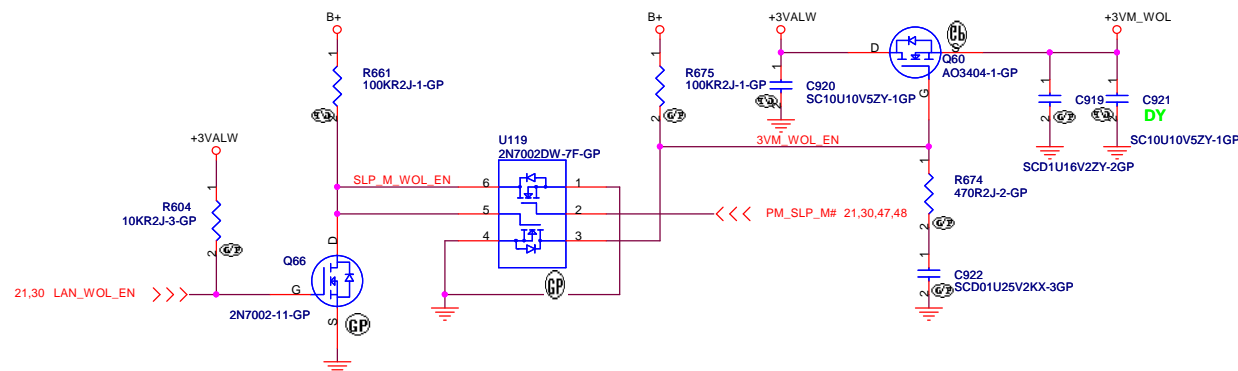
+3VALW to +3VM Transfer



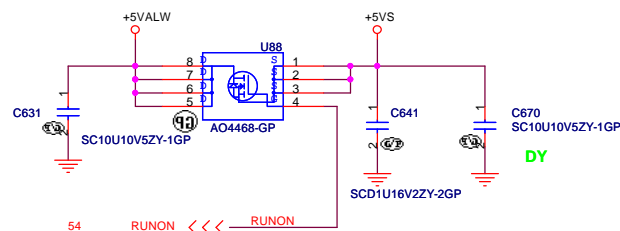
+3VALW to +3VS Transfer



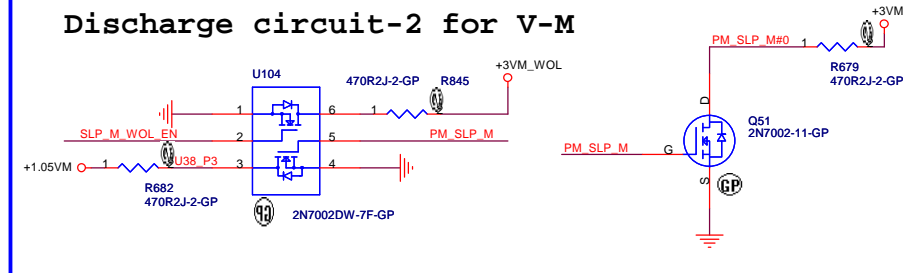
+3VALW to +3VM_WOL



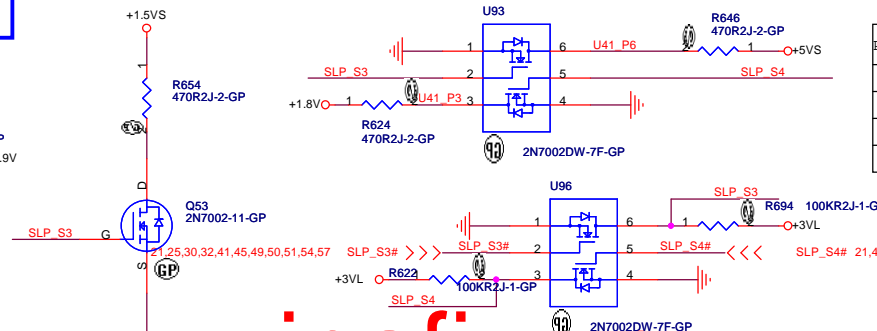
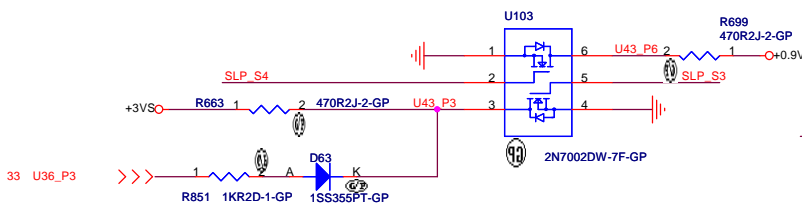
+5VALW to +5VS Transfer



Discharge circuit-2 for V-M



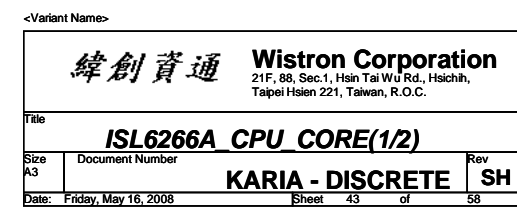
Discharge circuit-1

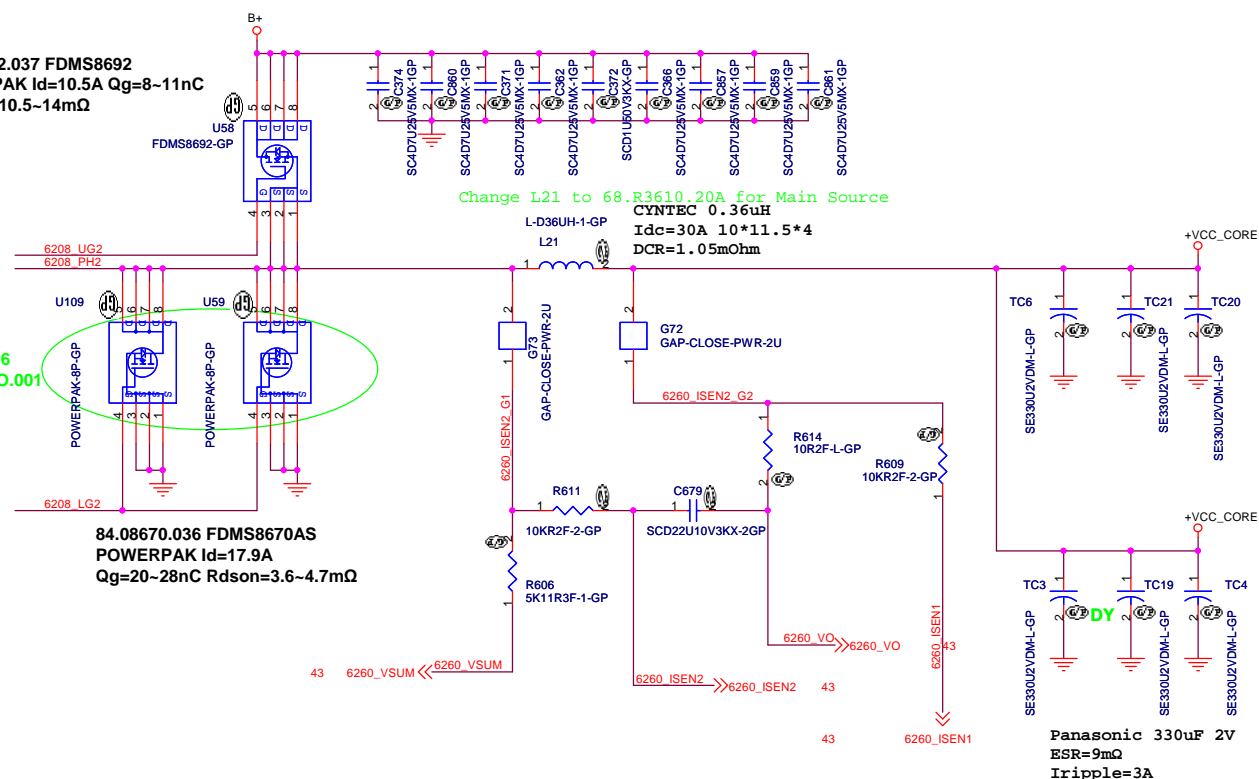


PM_SLP_M#	LAN_WOL_EN	+3VM_WOL	+3VM	SYSTEM STATE
0	0	0V	0V	Moff / No WOL
0	1	3.3V	0V	Legacy WOL/ Mof
1	0	3.3V	3.3V	M1
1	1	3.3V	3.3V	M1

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DC/DC Circuit		
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<Variant Name>

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Wistron Corporation
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Title

ISL6266A_CPU_CORE(2/2)

Size

	Document Number
--	-----------------

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84.08692.037 FDMS8692
Power PAK Id=10.5A
Qg=8~11nC Rdson=10.5~14mΩ

CYNTEC 0.82uH
Idc=13A 6.5*6.9*3
DCR=6.7m Ohm

VGA_CORE
Iomax=16A
OCP<19.5A

84.08670.036 FDMS8670AS
POWERPAK Id=17.9A
Qg=20~28nC
Rdson=3.6~4.7mΩ

Panasonic 470uF 2.5V
ESR=9mOhm
Tripple=3.725A

VGA_CORE TABLE

G1, G0	Vout Equation	R1 (R586)	R2 (R601)	R3 (R258+R262)	R4 (R595+R602)	Vout
(0,0)	$0.75 \cdot (1 + R1/R2 + R1/R3 + R1/R4)$	1K	100K	4.98K	3.82K	1.104V
(0,1)	$0.75 \cdot (1 + R1/R2 + R1/R4)$	1K	100K		3.08K	1.001V
(1,0)	$0.75 \cdot (1 + R1/R2 + R1/R3)$	1K	100K	4.98K		0.908V
(1,1)	$0.75 \cdot (1 + R1/R2)$	1K	100K			0.758V

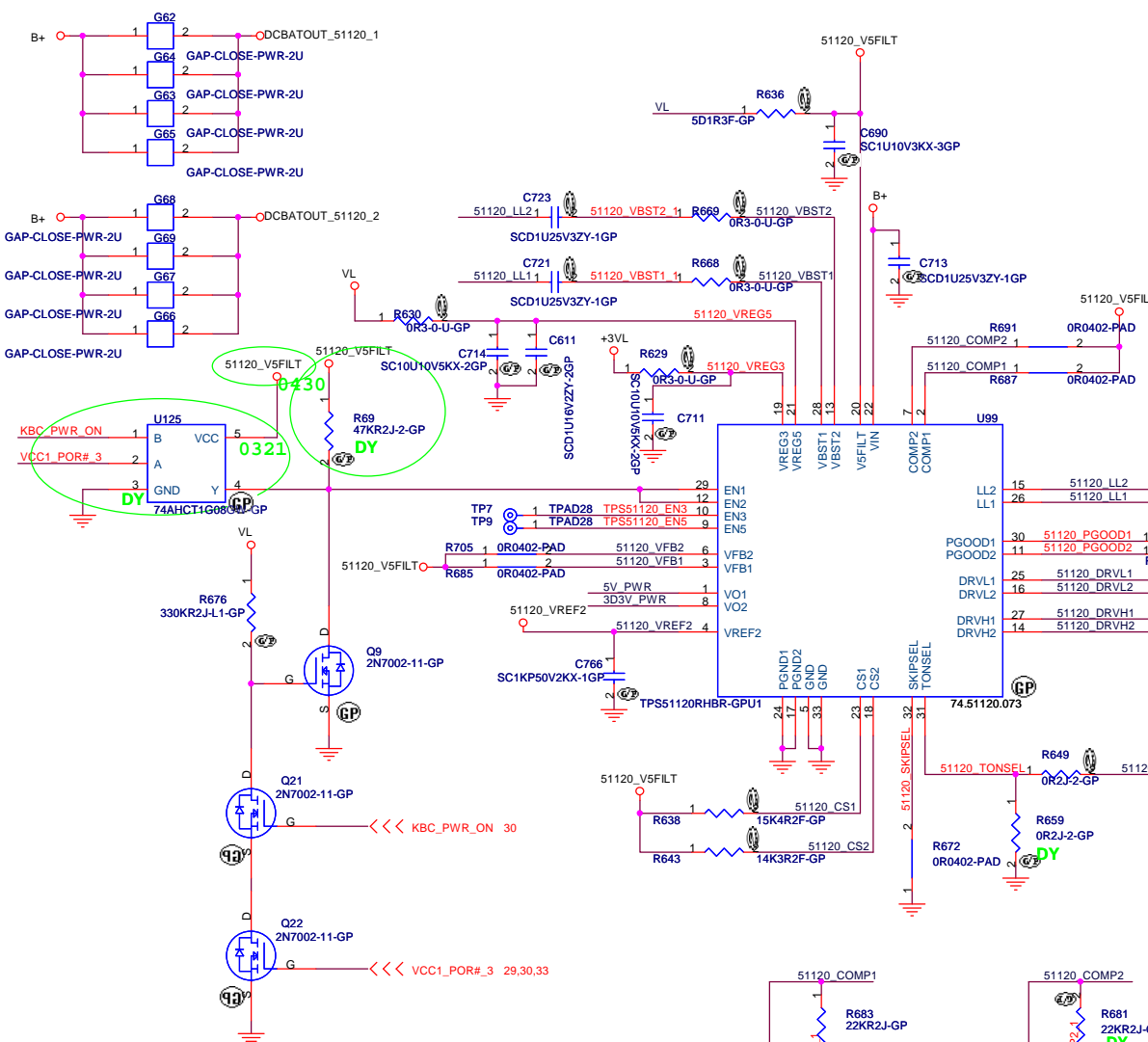
Removed these GAP
by Power's Request

Removed these GAP
by Power's Request

<Variant Name>

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Title SC471A VGA CORE		
Size B	Document Number KARIA - DISCRETE	Rev SH
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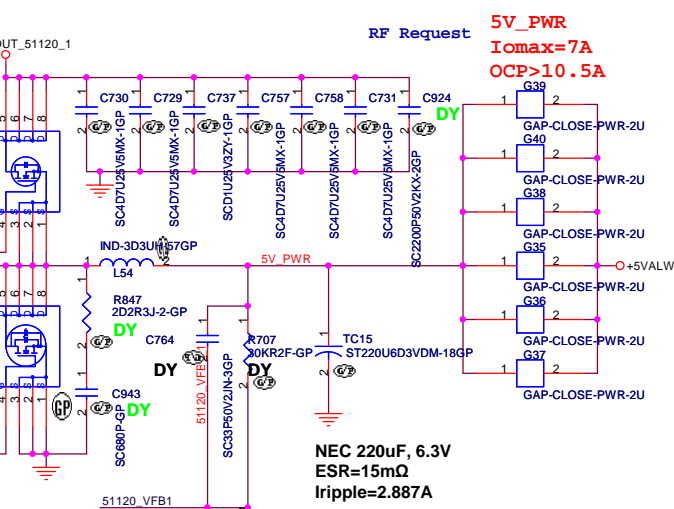


84.04800.D37
SI4800BDY SO8 Id=7A
Qg=8.7~13nC Rds(on)=23~30mΩ

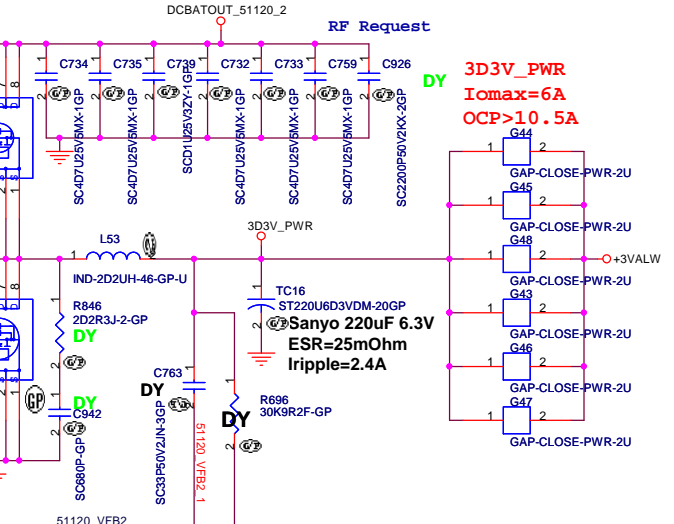
84.04812.A37 SI4812BDY
SO8 Id=7.7A Qg=8.5~13nC
Rds(on)=16.5~21mΩ

84.04800.D37
SI4800BDY SO8 Id=7A
Qg=8.7~13nC Rds(on)=23~30mΩ

84.04812.A37 SI4812BDY
SO8 Id=7.7A Qg=8.5~13nC
Rds(on)=16.5~21mΩ



CYNTec 3.3uH
Idc=6A 6.5*6.9*3
DCR=28mOhm



CYNTec 2.2uH
Idc=8A 6.5*6.9*3
DCR=18mOhm

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	Adjustable output (connect to the resistor divider)			5V Fixed Output
VFB2				3.3V Fixed Output
EN1, EN2	Switcher OFF	Switchchr ON		Switcher ON
EN3, EN5	LDO OFF	not use	LDO ON	VREG3 on (EN3 only)

For TPS51120,
Vout=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

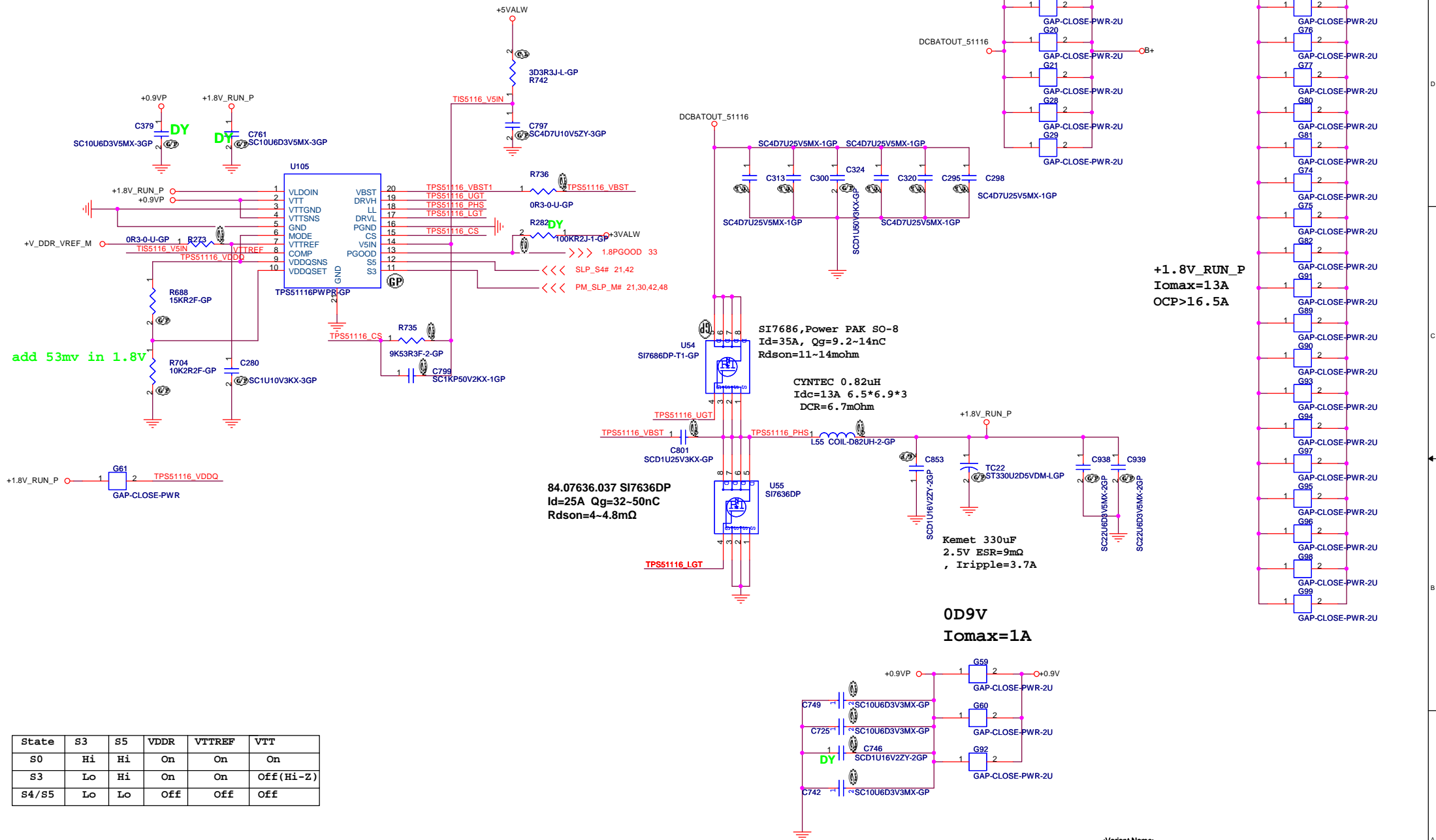
緯創資通 Wistron Corporation
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File: TPA51120 +5VALW +3VALW

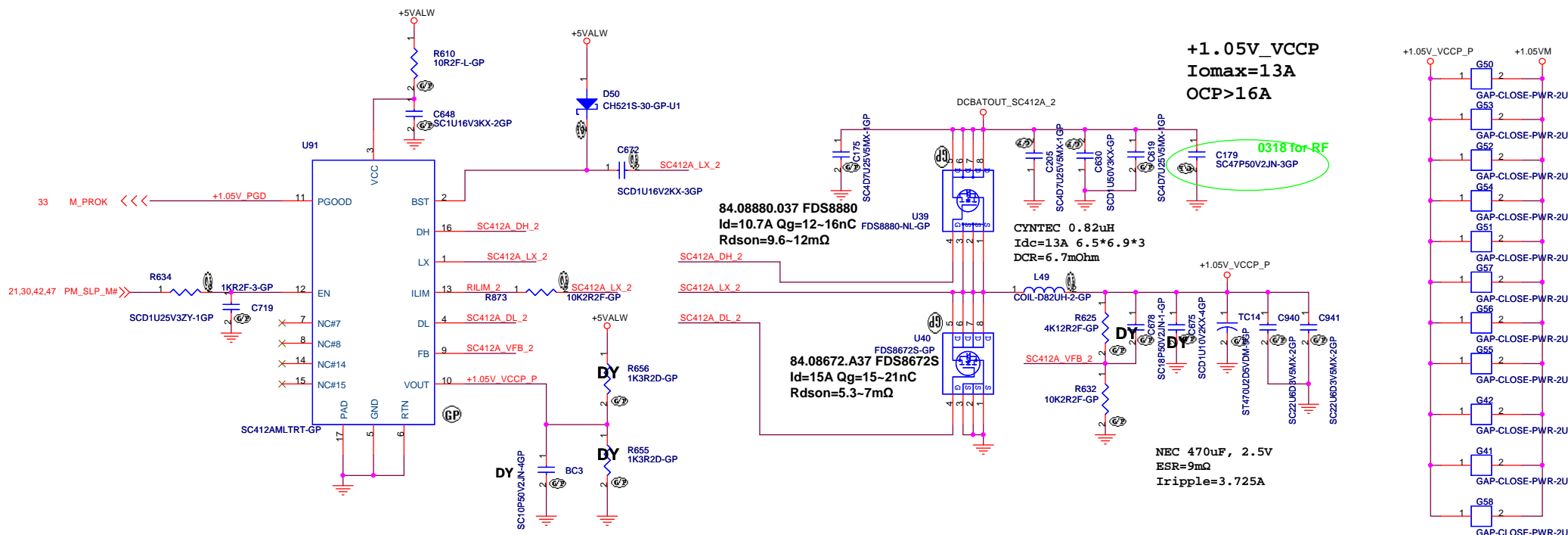
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TI TPS51116 for 1D8V and 0D9V



B+ DCBATOUT_SC412A_2

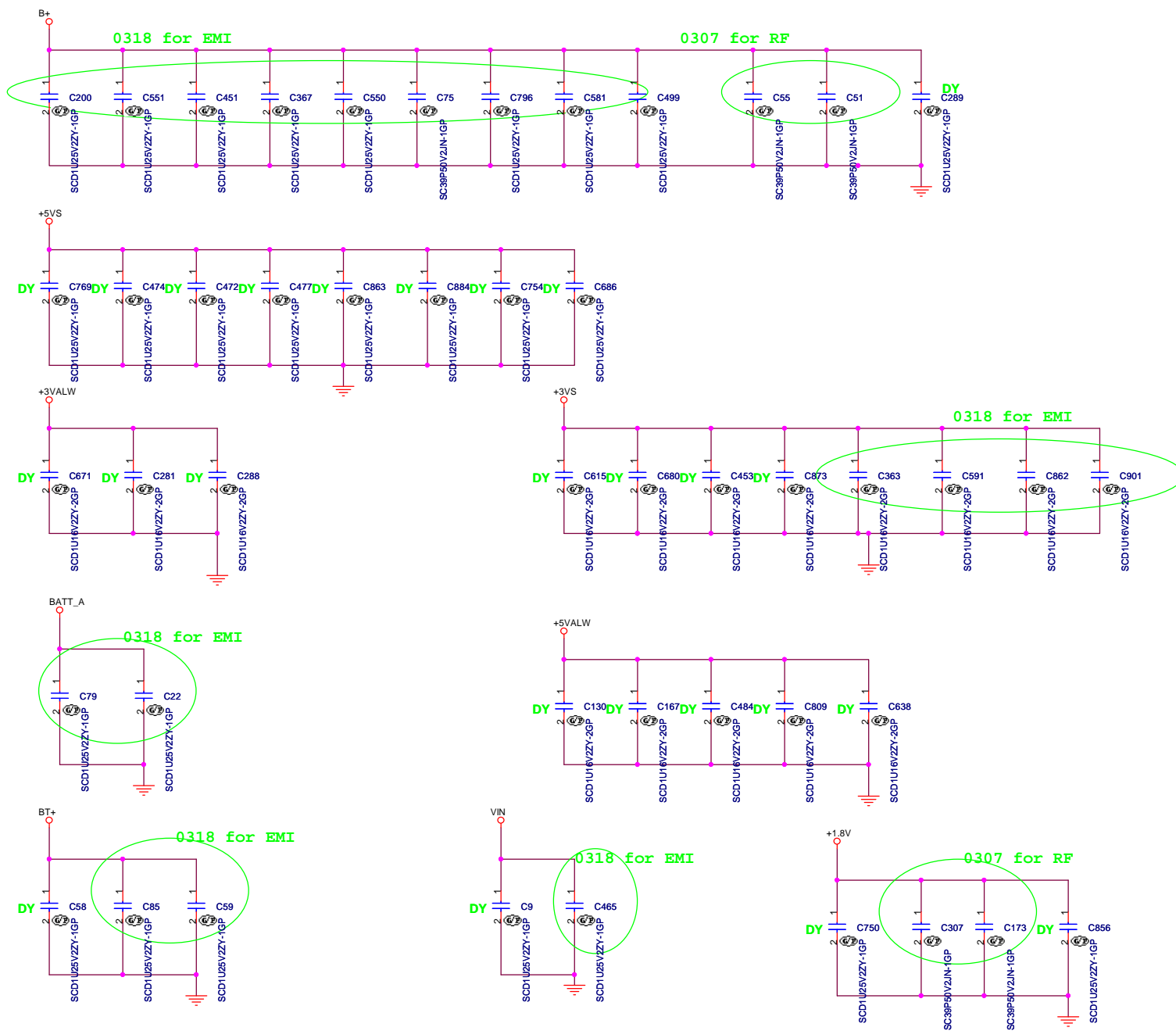


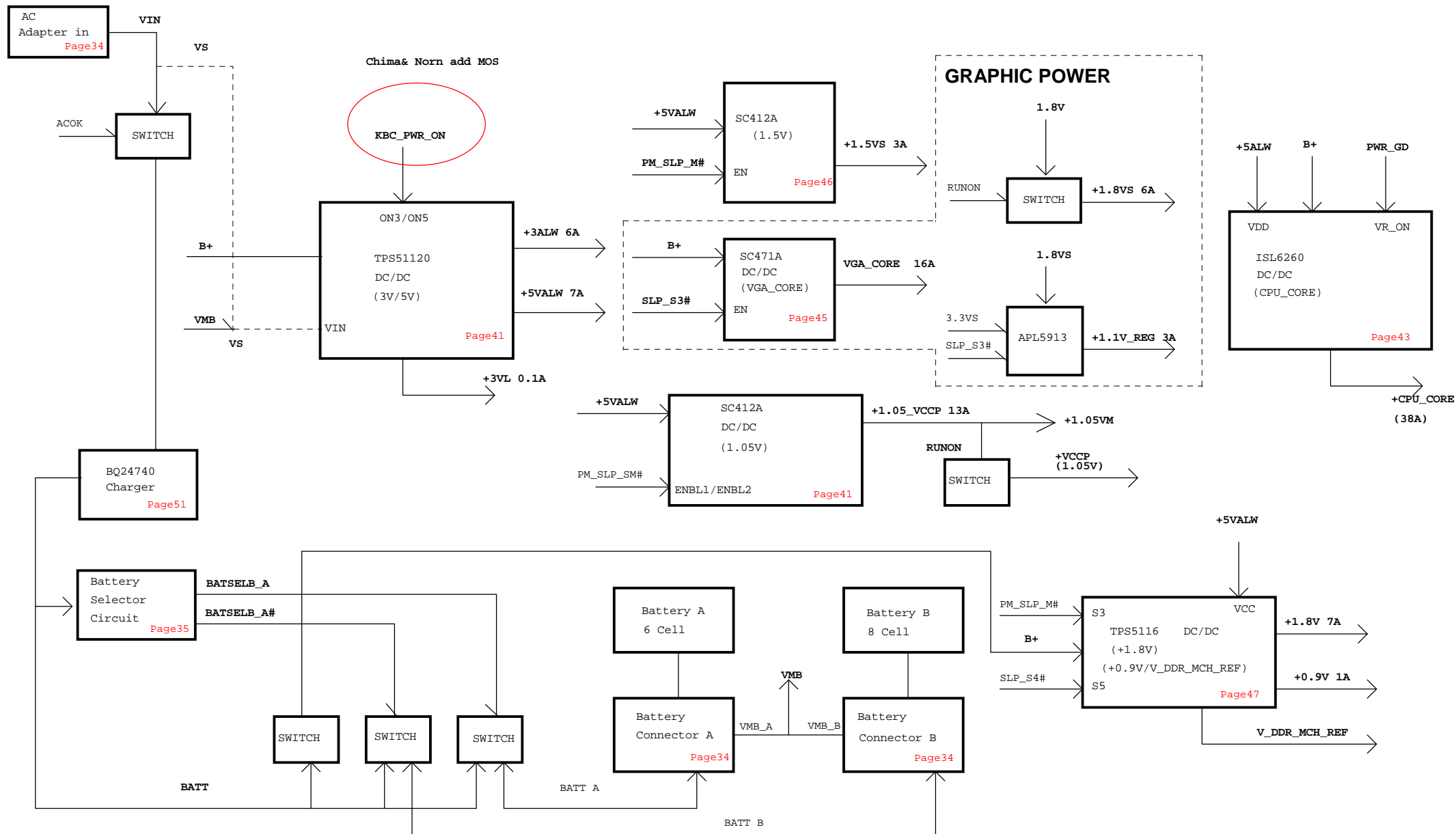
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 Taipei Hsien 221, Taiwan, R.O.C.

Title		
SC412A +1.05VM		
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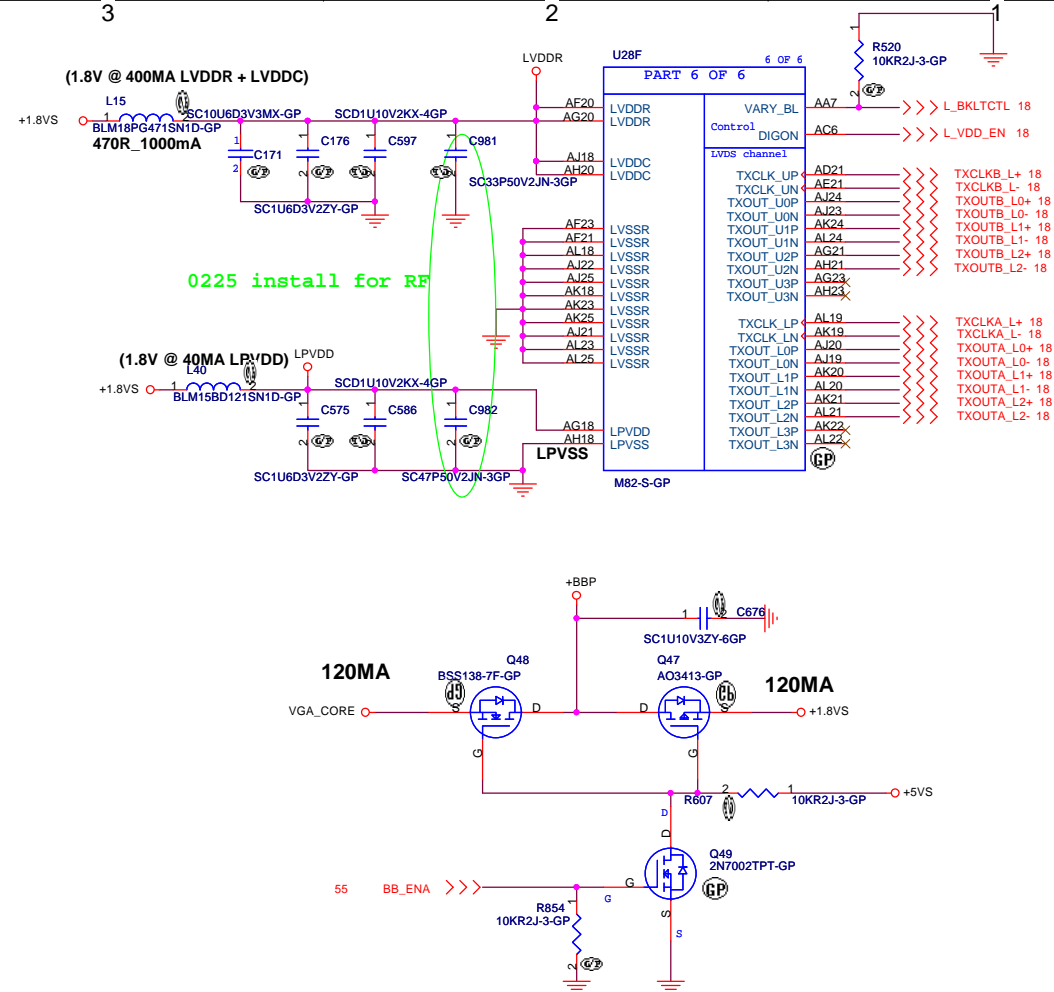
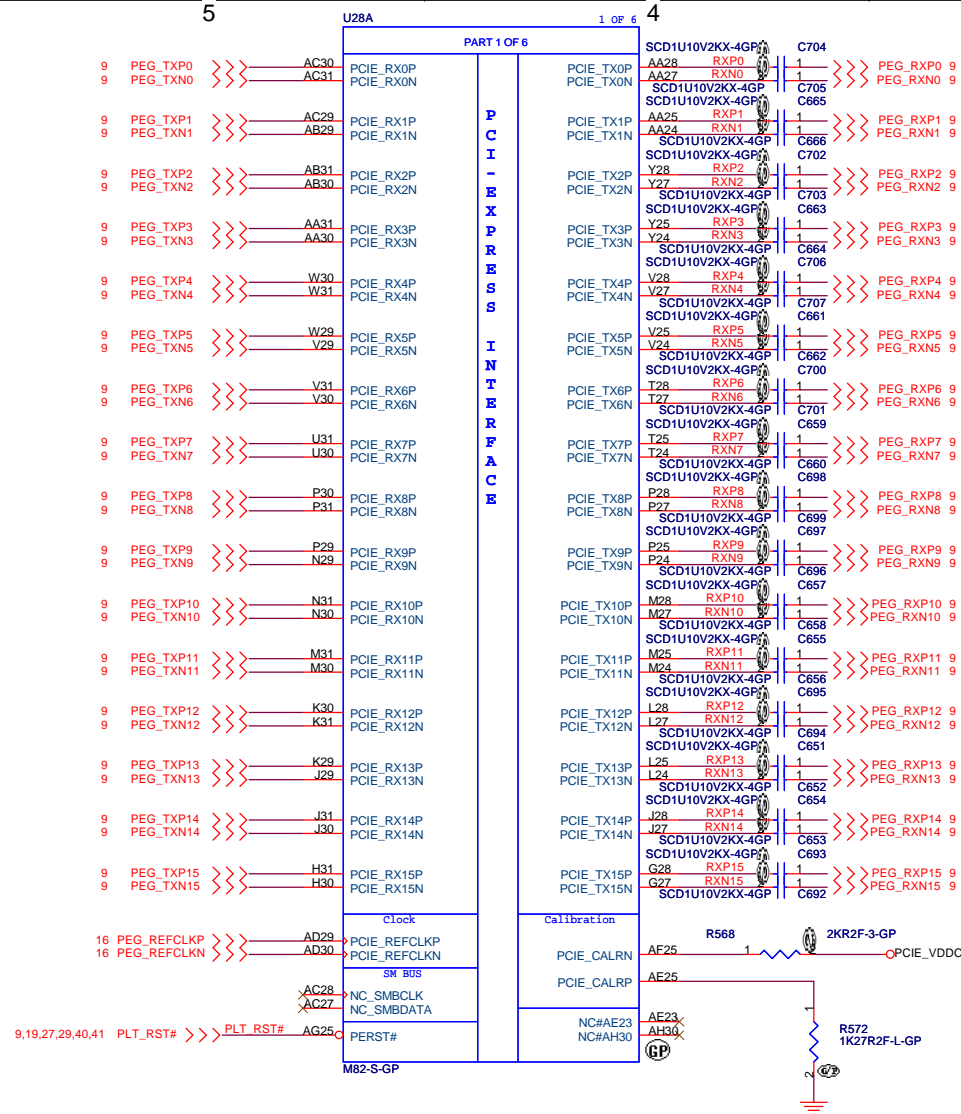




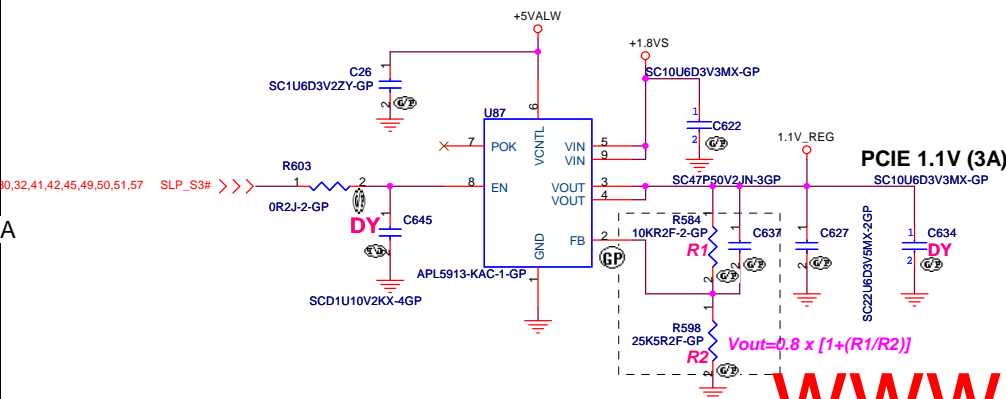


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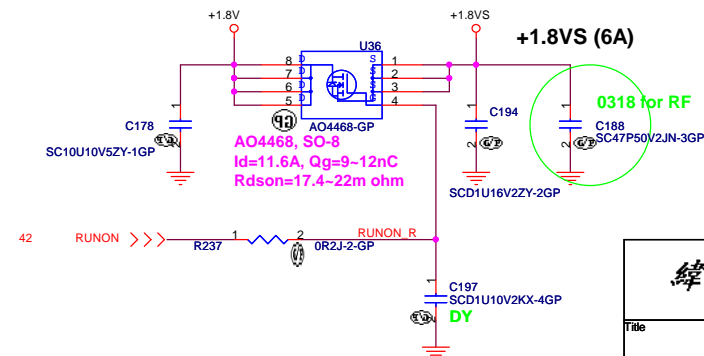
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Power Block Diagram	
Title Size A3 Date: Friday, May 16, 2008	Document Number KARIA - DISCRETE Sheet 53 of 58
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+1.8V to PCIe 1.1V Transfer



+1.8V to +1.8VS Transfer



0 = DON'T INSTALL RES
1 = INSTALL 10K RES
NA = NOT APPLICABLE

0 = DON'T INSTALL RES
1 = INSTALL 10K RES
NA = NOT APPLICABLE

GDDR3 64bit

00	-->8M*32	00	-->Qimonda
01	-->16M*32	01	-->Samsung
10	-->32M*32		

<-- Default



Un-install to disable HD-Audio function



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

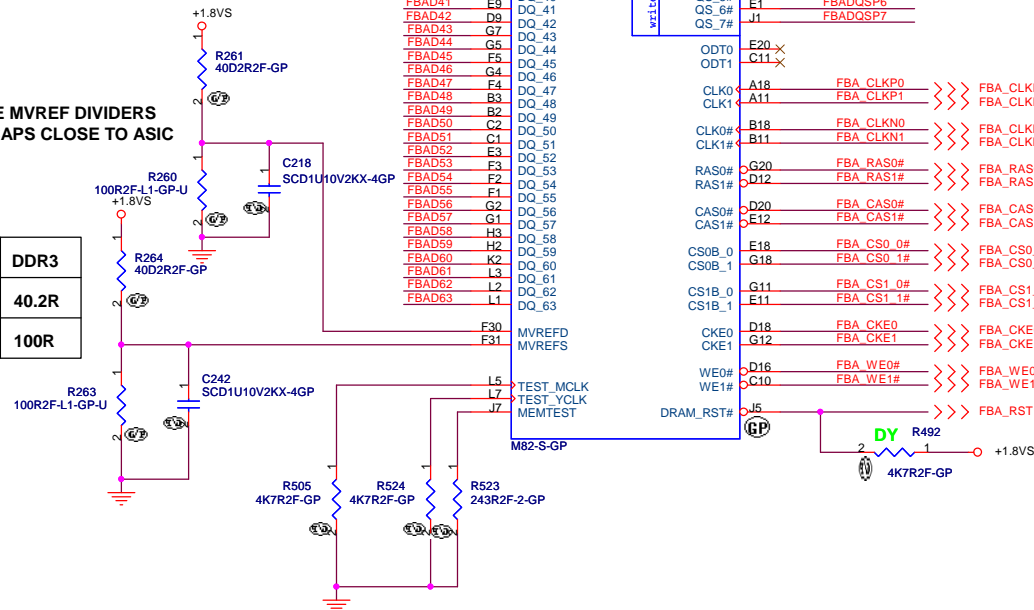
M82-S (2/4) I/C

KARIA - DISCRE

19. 2008 15m

PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



MEMORY
INTERFACE



FOR DUAL RANK CONNECTIONS
USE THE CSxB_1 CHIP SELECT PINS

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title M82-S (3/4) VRAM Interface	
Size A3	Document Number KARIA - DISCRETE
Date: Friday, May 16, 2008	Rev SH
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