ZZZ1

PCB

SE000008600

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Everest Schematics Document

Intel Merom Processor with Crestline + DDRII + ICH8M

2007-03-05

REV: 0.2

Security Classification	Compal Secret Data		
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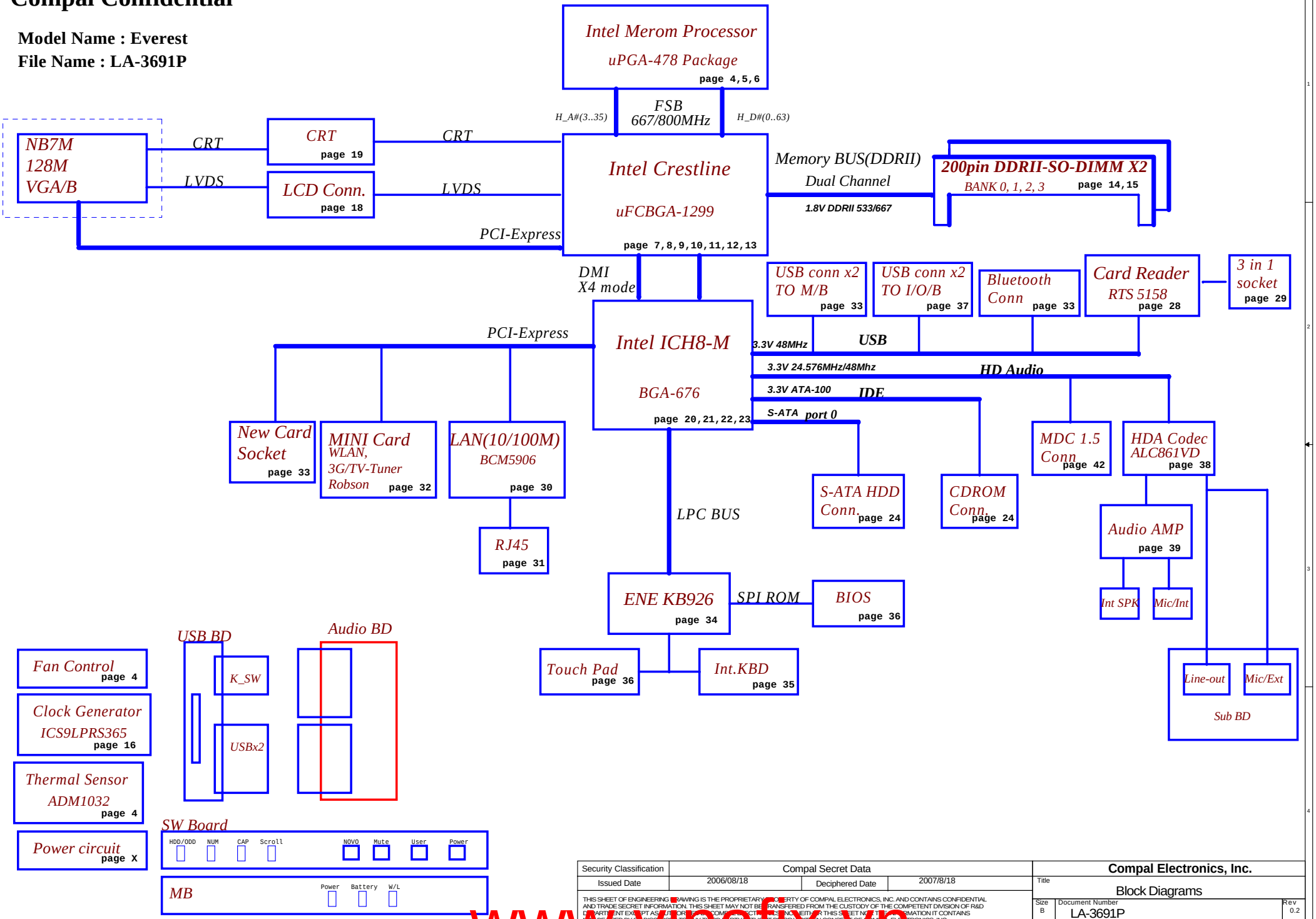
Model Name : Everest
File Name : LA-3691P



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Title: Block Diagrams

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

ID1	ID0	TEST
0(R744)	0(R745)	A-TEST
0(R744)	1(R742)	B-TEST
1(R741)	0(R745)	C-TEST

PANEL ID Table

R	Size
Ra (R743)	15W
Rb (R740)	14W

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ

No PCI Device

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b

EC SM Bus2 address

Device	Address
GMT-781	1001 100X b
NVIDIA NB8X	

ICH8M SM Bus address

Device	Address
Clock Generator (ICS9LPRS325AKLFT_MLF72)	1101 001Xb
DDR DIMM0	1010 000Xb
DDR DIMM1	1010 010Xb

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Title: Notes List

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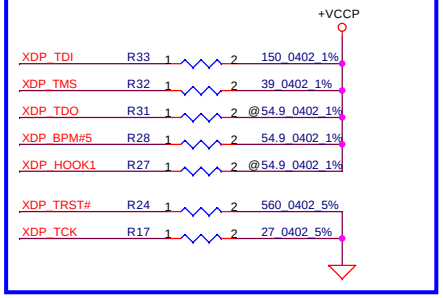
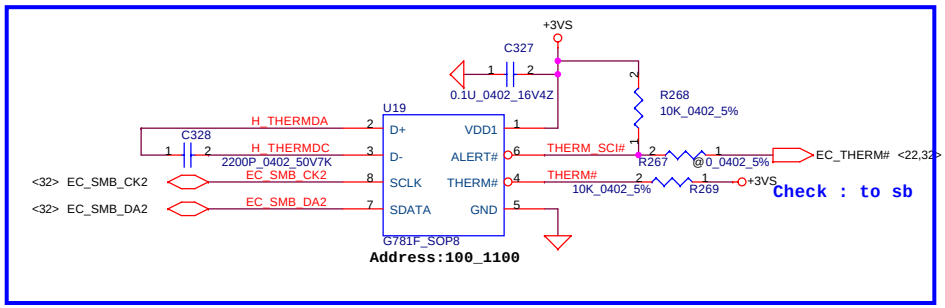
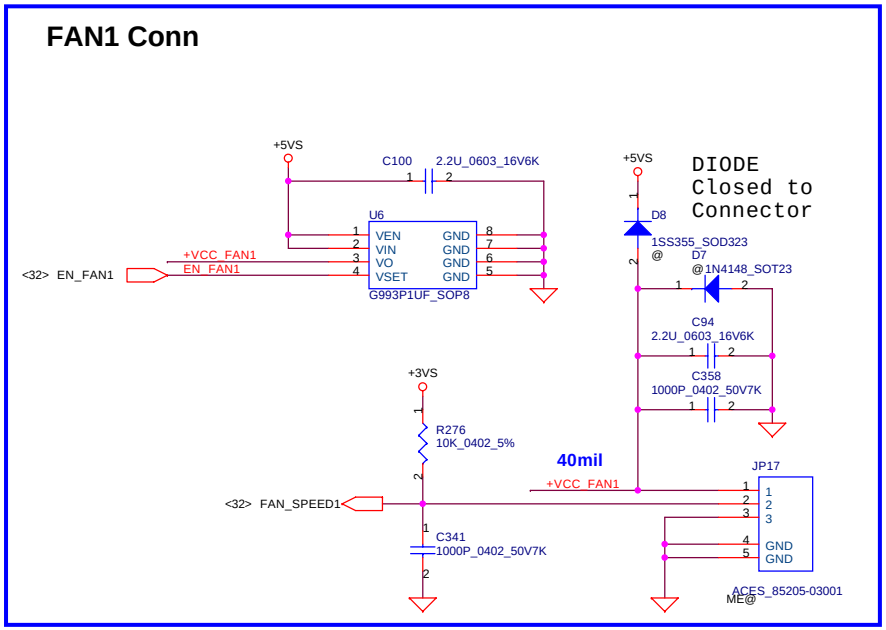
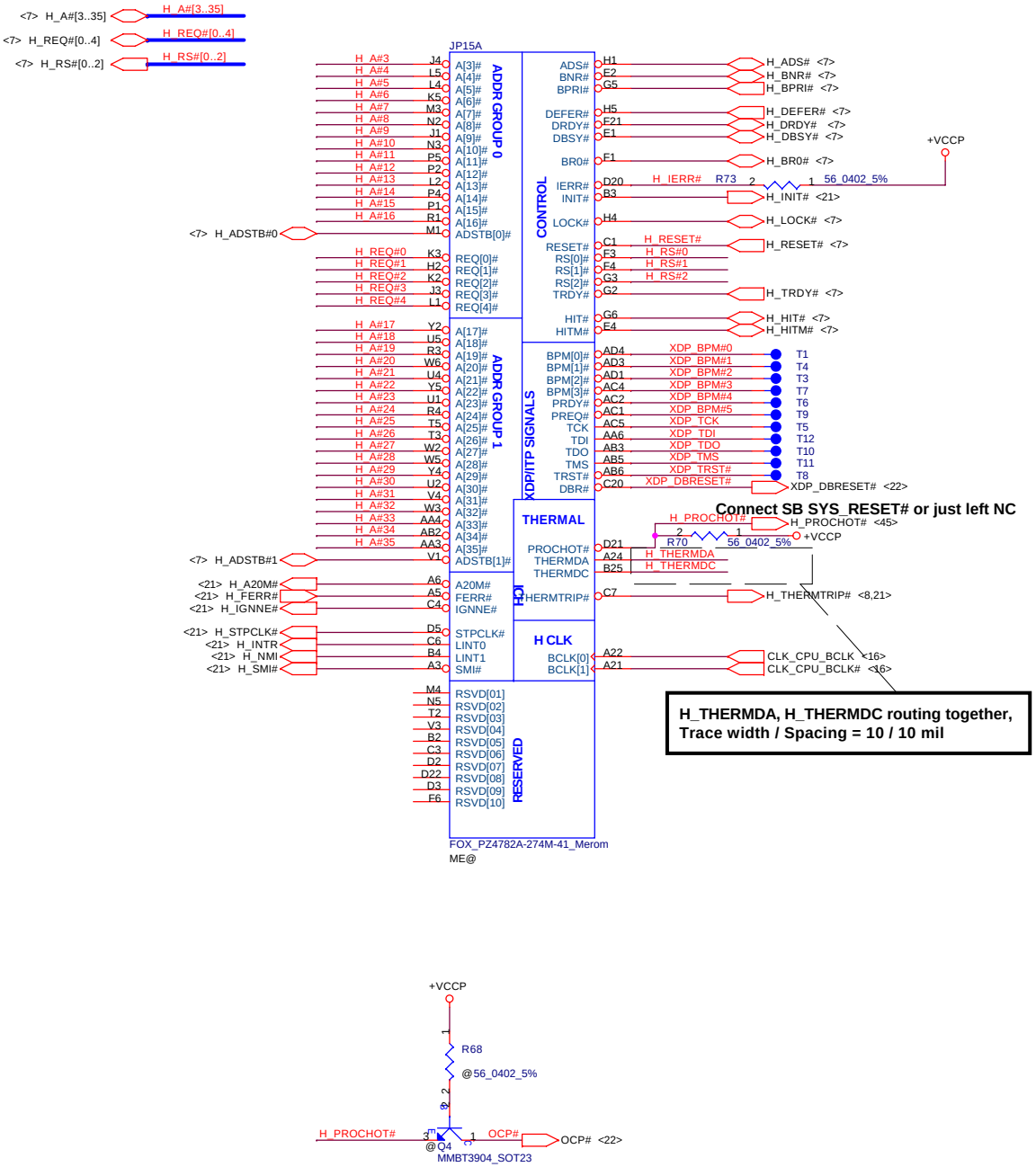
Place close to CPU within 500mil

XDP Reserve









H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

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Title: Merom (1/3)

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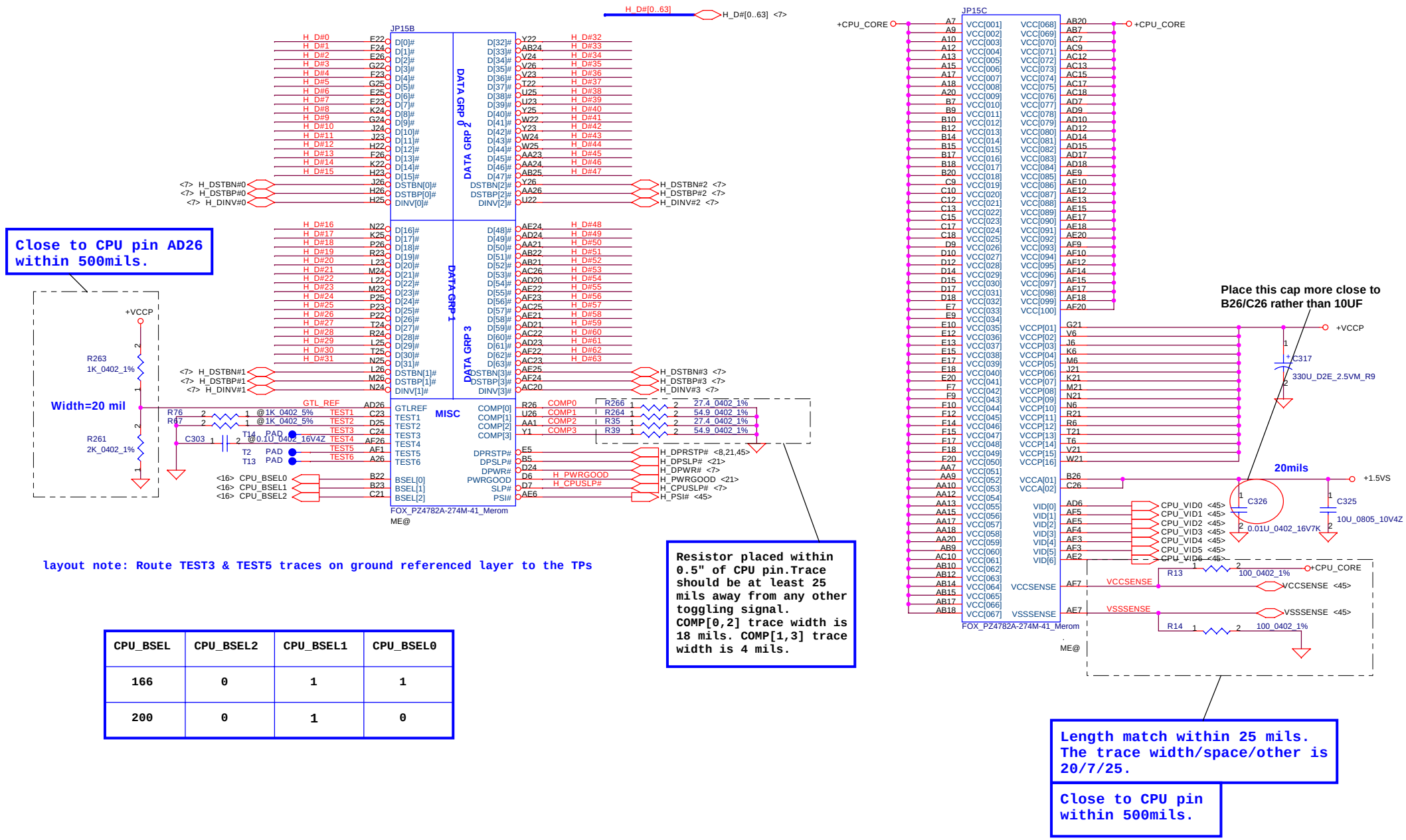

CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

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Title	Merom (2/3)
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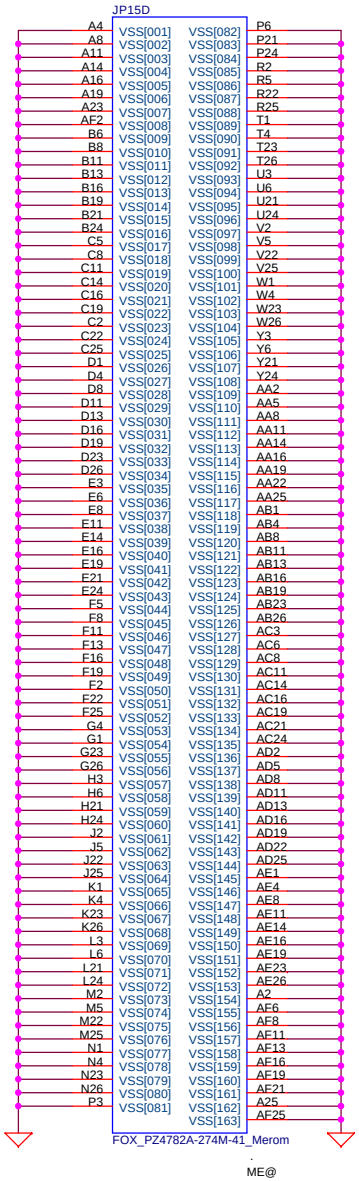
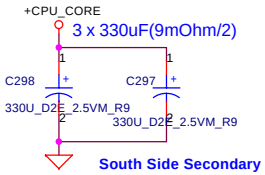
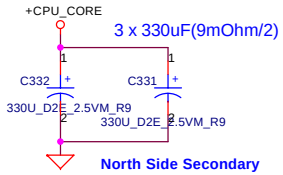
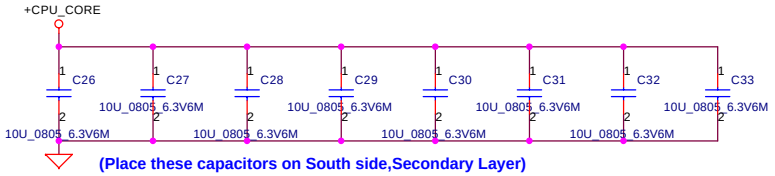




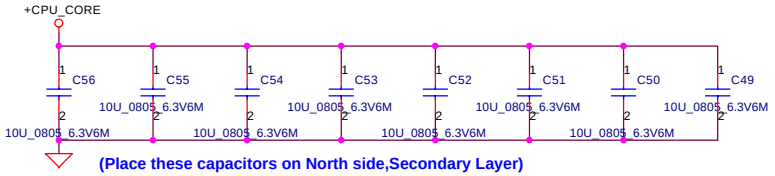
South Side Secondary



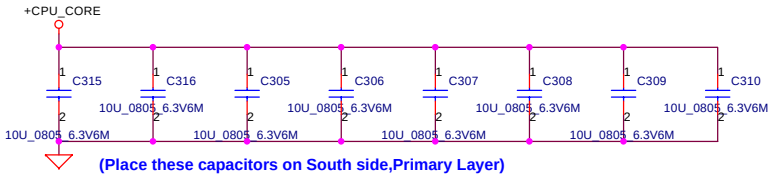
North Side Secondary



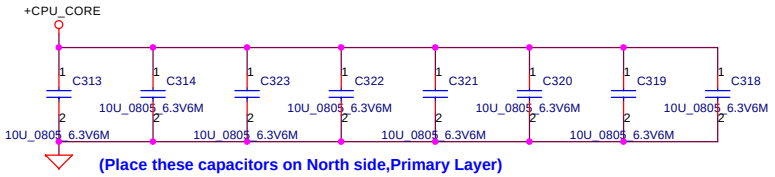
(Place these capacitors on South side,Secondary Layer)



(Place these capacitors on North side,Secondary Layer)



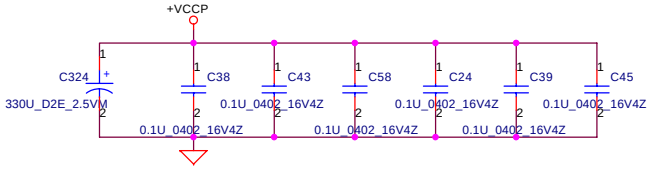
(Place these capacitors on South side,Primary Layer)



(Place these capacitors on North side,Primary Layer)

9/25 10U checked. OK for use!

+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



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Compal Electronics, Inc.

Title: Merom (3/3)

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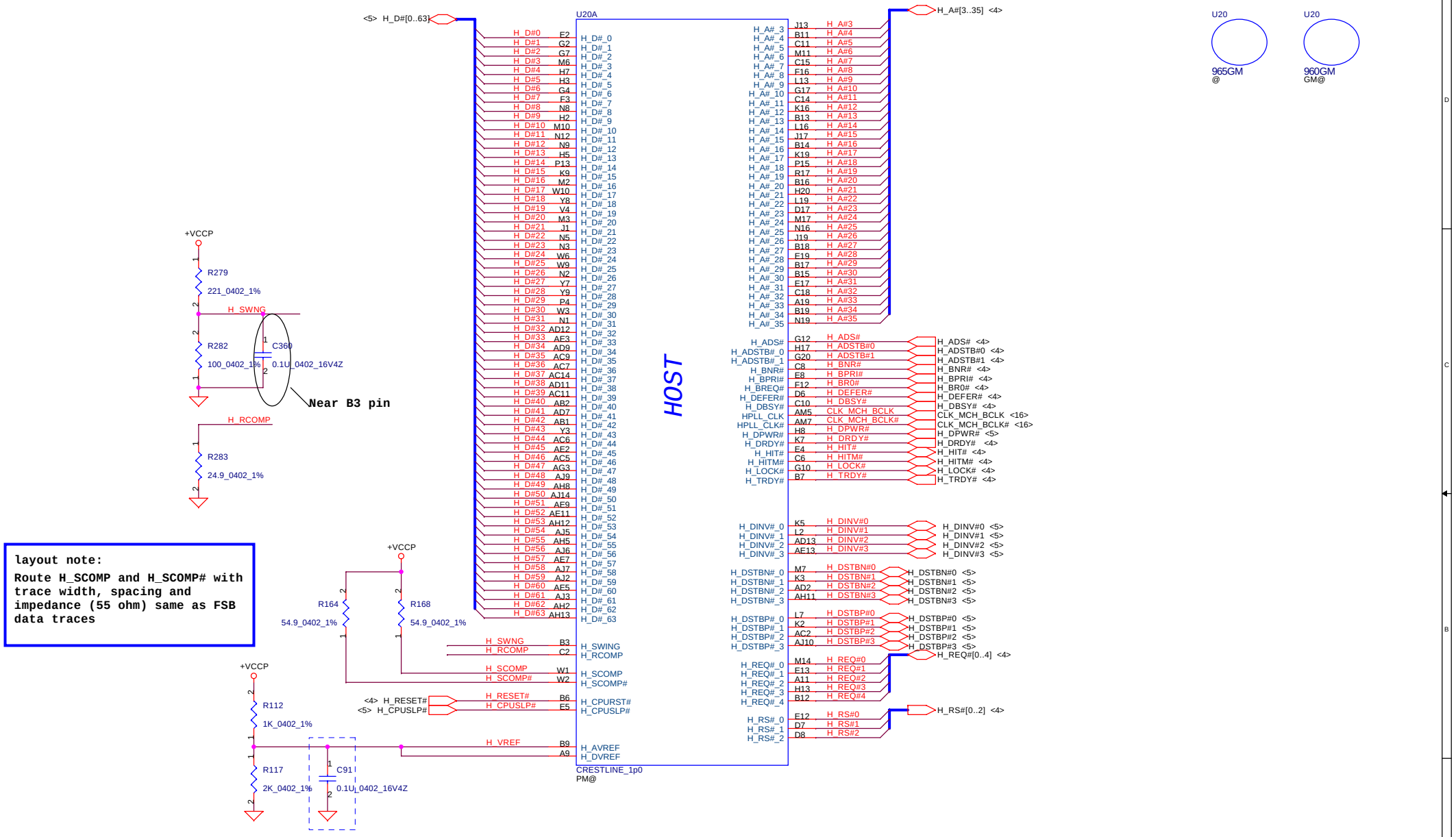

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U20B

DDR SYSTEM CLOCK
DDR MUXING
CLK
DMI
GRAPHICS VID
MISC
CRESTLINE_1p0
PM@

RSVD1 RSVD2 RSVD3 RSVD4 RSVD5 RSVD6 RSVD7 RSVD8 RSVD9 RSVD10 RSVD11 RSVD12 RSVD13 RSVD14
RSVD20 RSVD21 RSVD22 RSVD23 RSVD24 RSVD25 RSVD26 RSVD27 RSVD28 RSVD29 RSVD30 RSVD31
SA_MA_14 SB_MA_14 RSVD34 RSVD35 RSVD36 LVDSA_DATA#_3 LVDSA_DATA_3 RSVD39 RSVD40 RSVD41 RSVD42 RSVD43 RSVD44 RSVD45

<14> DDRA_SMA14
<15> DDRB_SMA14
DDRA_SMA14
DDRB_SMA14

9/20 Modify NB symbol for Pin BJ29/BE24/C48/D47

SM_CK_0 SM_CK_1 SM_CK_3 SM_CK_4 → AV29 BB23 BA25 AV23 → DDRA_CLK0 <14> DDRA_CLK1 <14> DDRB_CLK0 <15> DDRB_CLK1 <15>
SM_CK#_0 SM_CK#_1 SM_CK#_3 SM_CK#_4 → AW30 BA23 AW25 AW23 → DDRA_CLK0# <14> DDRA_CLK1# <14> DDRB_CLK0# <15> DDRB_CLK1# <15>
SM_CKE_0 SM_CKE_1 SM_CKE_3 SM_CKE_4 → BE29 AY32 BD39 BG37 → DDRA_CKE0 <14> DDRA_CKE1 <14> DDRB_CKE0 <15> DDRB_CKE1 <15>
SM_CS#_0 SM_CS#_1 SM_CS#_2 SM_CS#_3 → BG20 BK16 BG16 BE13 → DDRA_SCS0# <14> DDRA_SCS1# <14> DDRB_SCS0# <15> DDRB_SCS1# <15>
SM_ODT_0 SM_ODT_1 SM_ODT_2 SM_ODT_3 → BH18 BJ15 BJ14 BE16 → DDRA_ODT0 <14> DDRA_ODT1 <14> DDRB_ODT0 <15> DDRB_ODT1 <15>

SM_RCOMP → BL15 SMRCOMP → R382 1 2 20_0402_1%
SM_RCOMP# → BK14 SMRCOMP# → R381 1 2 20_0402_1%
SM_RCOMP_VOH → BK31 SM_RCOMP_VOH
SM_RCOMP_VOL → BL31 SM_RCOMP_VOL
SM_VREF_0 SM_VREF_1 → AR49 AW4 → SM_VREF 20mil

+1.8V → R182 1K_0402_1% → SM_VREF → R180 1K_0402_1% → C161 0.1U_0402_16V4Z

DPLL_REF_CLK → B42 CLK_DREF_96M → CLK_DREF_96M <16>
DPLL_REF_CLK# → C42 CLK_DREF_96M# → CLK_DREF_96M# <16>
DPLL_REF_SSCLK → H48 CLK_DREF_SSC → CLK_DREF_SSC <16>
DPLL_REF_SSCLK# → H47 CLK_DREF_SSC# → CLK_DREF_SSC# <16>
PEG_CLK → K44 CLK_MCH_3GPLL → CLK_MCH_3GPLL <16>
PEG_CLK# → K45 CLK_MCH_3GPLL# → CLK_MCH_3GPLL# <16>

DMI_RXN_0 DMI_RXN_1 DMI_RXN_2 DMI_RXN_3 → AN47 AJ38 AN42 AN46 → DMI_ITX_MRX_N0 DMI_ITX_MRX_N1 DMI_ITX_MRX_N2 DMI_ITX_MRX_N3 → DMI_ITX_MRX_N0 <22> DMI_ITX_MRX_N1 <22> DMI_ITX_MRX_N2 <22> DMI_ITX_MRX_N3 <22>
DMI_RXP_0 DMI_RXP_1 DMI_RXP_2 DMI_RXP_3 → AM47 AJ39 AN41 AN45 → DMI_ITX_MRX_P0 DMI_ITX_MRX_P1 DMI_ITX_MRX_P2 DMI_ITX_MRX_P3 → DMI_ITX_MRX_P0 <22> DMI_ITX_MRX_P1 <22> DMI_ITX_MRX_P2 <22> DMI_ITX_MRX_P3 <22>
DMI_TXN_0 DMI_TXN_1 DMI_TXN_2 DMI_TXN_3 → AJ46 AJ41 AM40 AM44 → DMI_MTX_IRX_N0 DMI_MTX_IRX_N1 DMI_MTX_IRX_N2 DMI_MTX_IRX_N3 → DMI_MTX_IRX_N0 <22> DMI_MTX_IRX_N1 <22> DMI_MTX_IRX_N2 <22> DMI_MTX_IRX_N3 <22>
DMI_TXP_0 DMI_TXP_1 DMI_TXP_2 DMI_TXP_3 → AJ47 AJ42 AM39 AM43 → DMI_MTX_IRX_P0 DMI_MTX_IRX_P1 DMI_MTX_IRX_P2 DMI_MTX_IRX_P3 → DMI_MTX_IRX_P0 <22> DMI_MTX_IRX_P1 <22> DMI_MTX_IRX_P2 <22> DMI_MTX_IRX_P3 <22>

<16> MCH_CLKSEL0 → MCH_CLKSEL0 P27 → CFG_0
<16> MCH_CLKSEL1 → MCH_CLKSEL1 N27 → CFG_1
<16> MCH_CLKSEL2 → MCH_CLKSEL2 N24 → CFG_2
C21 → CFG_3
C23 → CFG_4
MCH_CFG_5 → F23 → CFG_5
N23 → CFG_6
MCH_CFG_7 → G23 → CFG_7
MCH_CFG_8 → J20 → CFG_8
MCH_CFG_9 → C20 → CFG_9
R24 → CFG_10
MCH_CFG_12 → L23 → CFG_11
MCH_CFG_13 → J23 → CFG_12
E23 → CFG_13
E20 → CFG_14
K23 → CFG_15
MCH_CFG_16 → M20 → CFG_16
M24 → CFG_17
L32 → CFG_18
MCH_CFG_19 → N33 → CFG_19
MCH_CFG_20 → L35 → CFG_20

GFX_VID_0 GFX_VID_1 GFX_VID_2 GFX_VID_3 GFX_VR_EN → E35 A39 C38 B39 E36

<22> PM_BMBUSY# → G41 → PM_BM_BUSY#
<5,21,45> H_DPRSTP# → L39 → PM_DPRSTP#
<14> PM_EXTTS#0 → PM_EXTTS#0 L36 → PM_EXT_TS#_0
<15> PM_EXTTS#1 → PM_EXTTS#1 J36 → PM_EXT_TS#_1
GMCH_PWROK → AW49 → PWROK
<17,20,22,24,25,30> PLT_RST_BUF# → MCH_RSTIN# AV20 → RSTIN#
<4,21> H_THERMTRIP# → R176 100_0402_5% → R104 0_0402_5% → N20 → THERMTRIP#
<22,45> PM_DPRSLPVR → G36 → DPRSLPVR

If THERMTRIP no used, left NC

CL_CLK → AM49 → CL_CLK0 <22>
CL_DATA → AK50 → CL_DATA0 <22>
CL_PWROK → AT43 → CL_PWROK <22>
CL_RST# → AN49 → CL_RST# <22>
CL_VREF → AM50 → C142 0.1U_0402_16V4Z
+1.25VS → R173 1K_0402_1% → CL_VREF → R172 392_0402_1%

SDVO_CTRL_CLK → H35 SDVO_CTRL_CLK
SDVO_CTRL_DATA → K36 SDVO_CTRL_DATA
CLK_REQ# → G39 MCH_CLKREQ# → MCH_CLKREQ# <16>
ICH_SYNC# → G40 → MCH_ICH_SYNC# <22>

TEST_1 → A37 MCH_TEST_1 → R124 0_0402_5%
TEST_2 → R32 MCH_TEST_2 → R158 20K_0402_5%

BJ51 BK51 BK50 BL50 BL49 BL3 BL2 BK1 BJ1 E1 A5 C51 B50 A50 A49 BK2 → NC_1 NC_2 NC_3 NC_4 NC_5 NC_6 NC_7 NC_8 NC_9 NC_10 NC_11 NC_12 NC_13 NC_14 NC_15 NC_16

Use VGATE for GMCH_PWROK

<22,45> VGATE → VGATE R184 @0_0402_5% → GMCH_PWROK
<22,32> ICH_POK → ICH_POK R186 0_0402_5%

+1.8V → R410 1K_0402_1% → SM_RCOMP_VOH → R397 3.01K_0402_1% → SM_RCOMP_VOL → R384 1K_0402_1%
C469 2.2U_0805_10V6K
C465 0.01U_0402_16V7K
C467 2.2U_0805_10V6K
C464 0.01U_0402_16V7K

Layout Note:
SM_VREF trace width and spacing is 20/20.

Maybe not used
+VCCP
CLK_DREF_96M# R122 PM@ 0_0402_5%
CLK_DREF_SSC# R146 PM@ 0_0402_5%
CLK_DREF_96M R123 PM@ 0_0402_5%
CLK_DREF_SSC R142 PM@ 0_0402_5%

CFG[17:3] have internal pull up
CFG[19:18] have internal pull down

Strap Pin Table

CFG[2:0]	011 = 667MT/s FSB 010 = 800MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. * (Default) 1 = PCIE/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present

MCH_CFG_5 R132 @4.02K_0402_1%
MCH_CFG_9 R141 @4.02K_0402_1%
MCH_CFG_12 R145 @4.02K_0402_1%
MCH_CFG_13 R133 @4.02K_0402_1%
MCH_CFG_16 R155 @4.02K_0402_1%
MCH_CFG_7 R135 @4.02K_0402_1%
MCH_CFG_8 R151 @4.02K_0402_1%
MCH_CFG_19 R113 @4.02K_0402_1% +3VS
MCH_CFG_20 R126 @4.02K_0402_1%
PM_EXTTS#0 R114 10K_0402_5% +3VS
PM_EXTTS#1 R138 10K_0402_5%
MCH_CLKREQ# R125 10K_0402_5%
SDVO_CTRL_CLK R149 @ 0_0402_5%
SDVO_CTRL_DATA R160 @ 0_0402_5%

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Title: Crestline (2/7)-DMI/DDR

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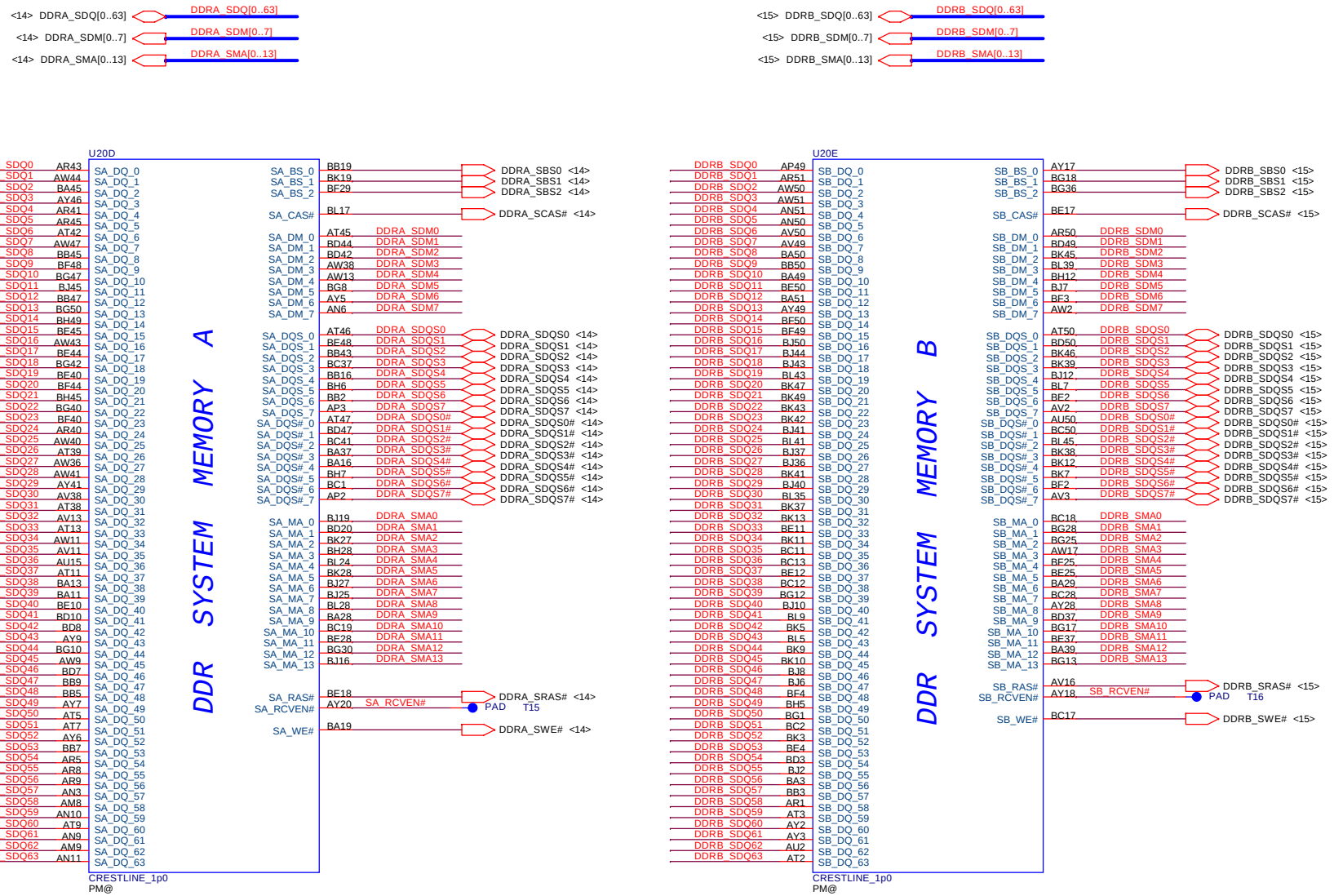

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Compal Electronics, Inc.

Title: Crestline (3/7)-DDRII

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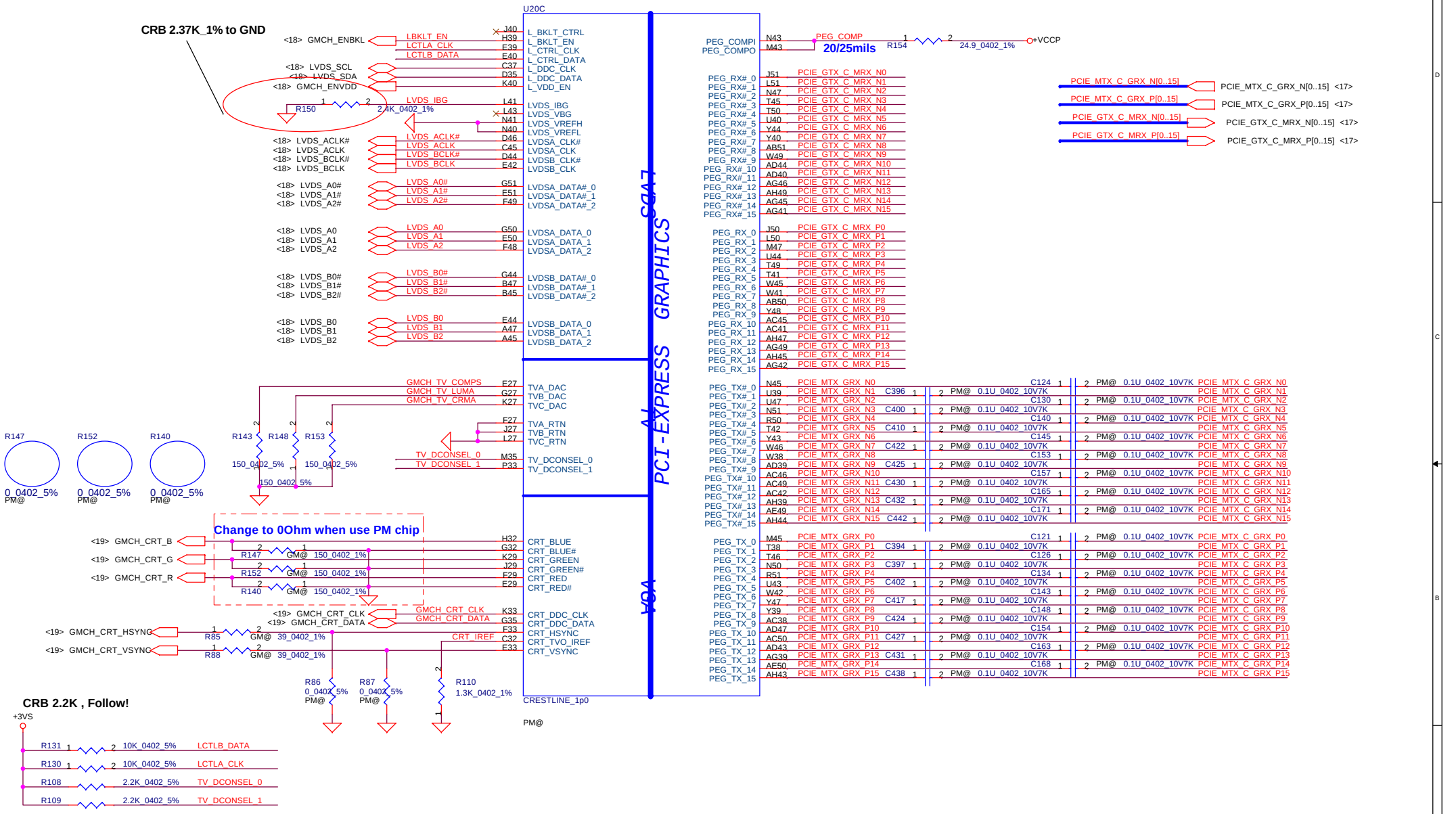

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Title	Crestline (4/7)-VGA/LVDS/TV	
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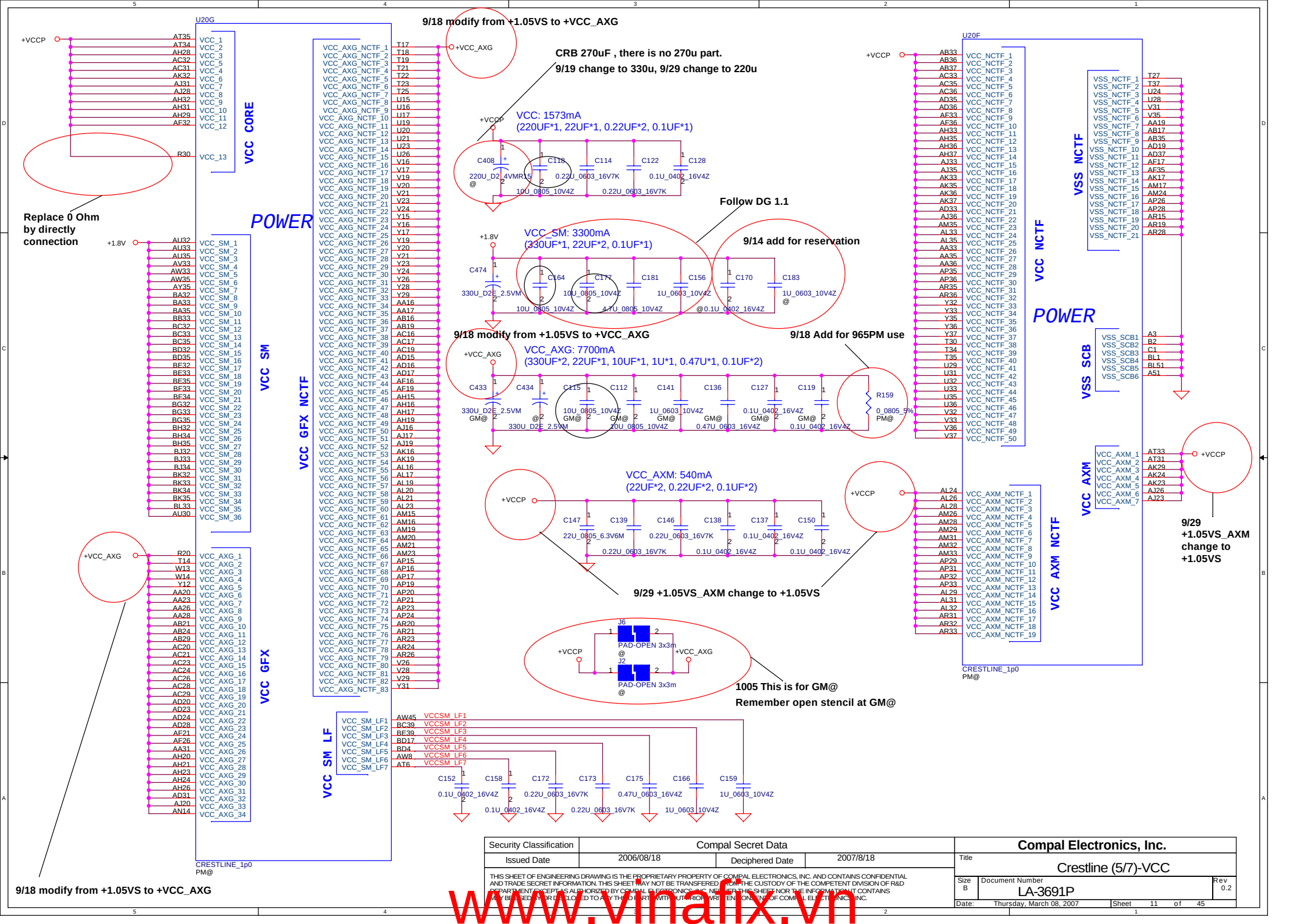

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Title: Crestline (5/7)-VCC

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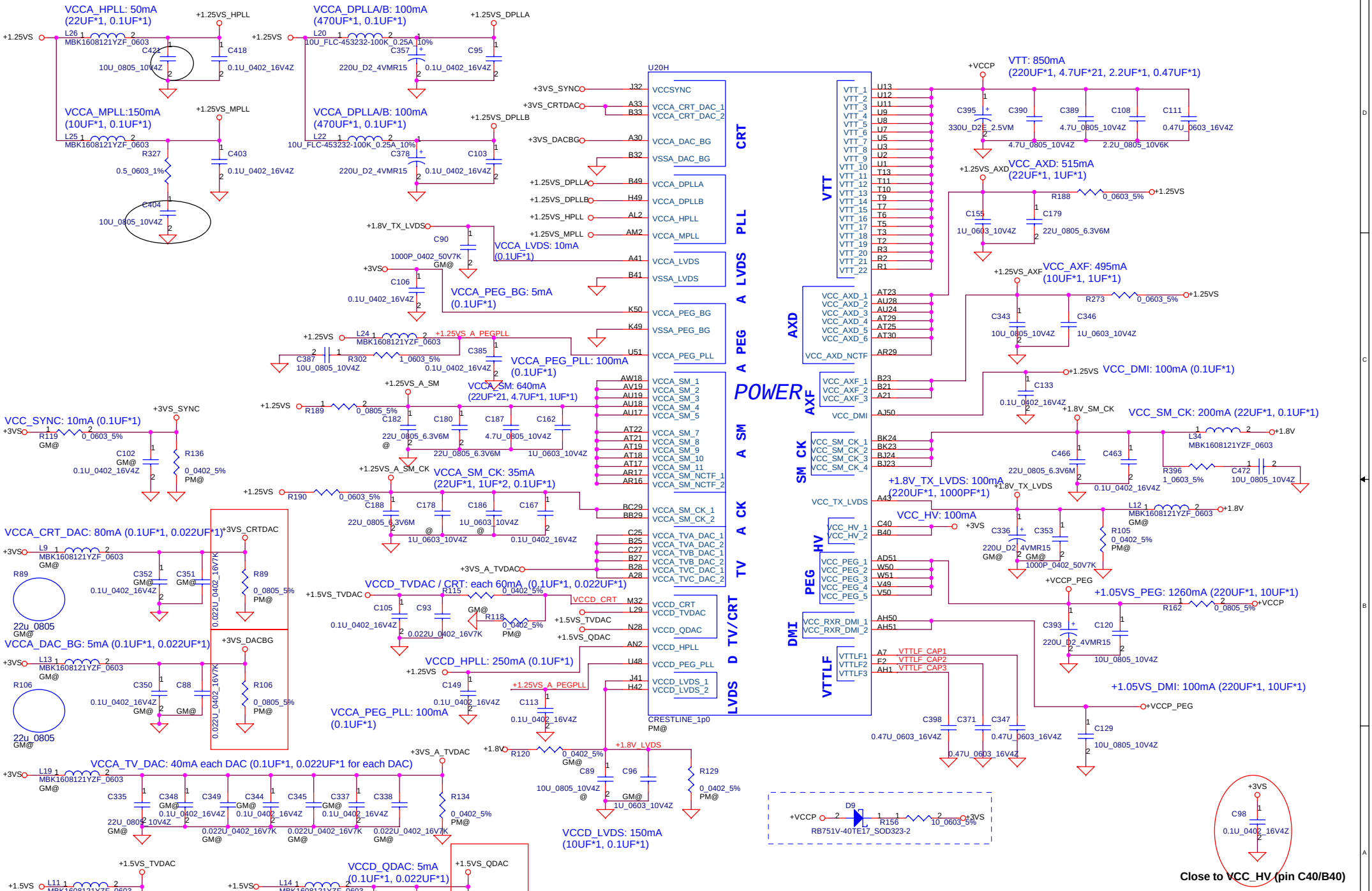

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Title	Crestline (6/7)-VCC		
Size B	Document Number LA-3691P		Rev 0.2
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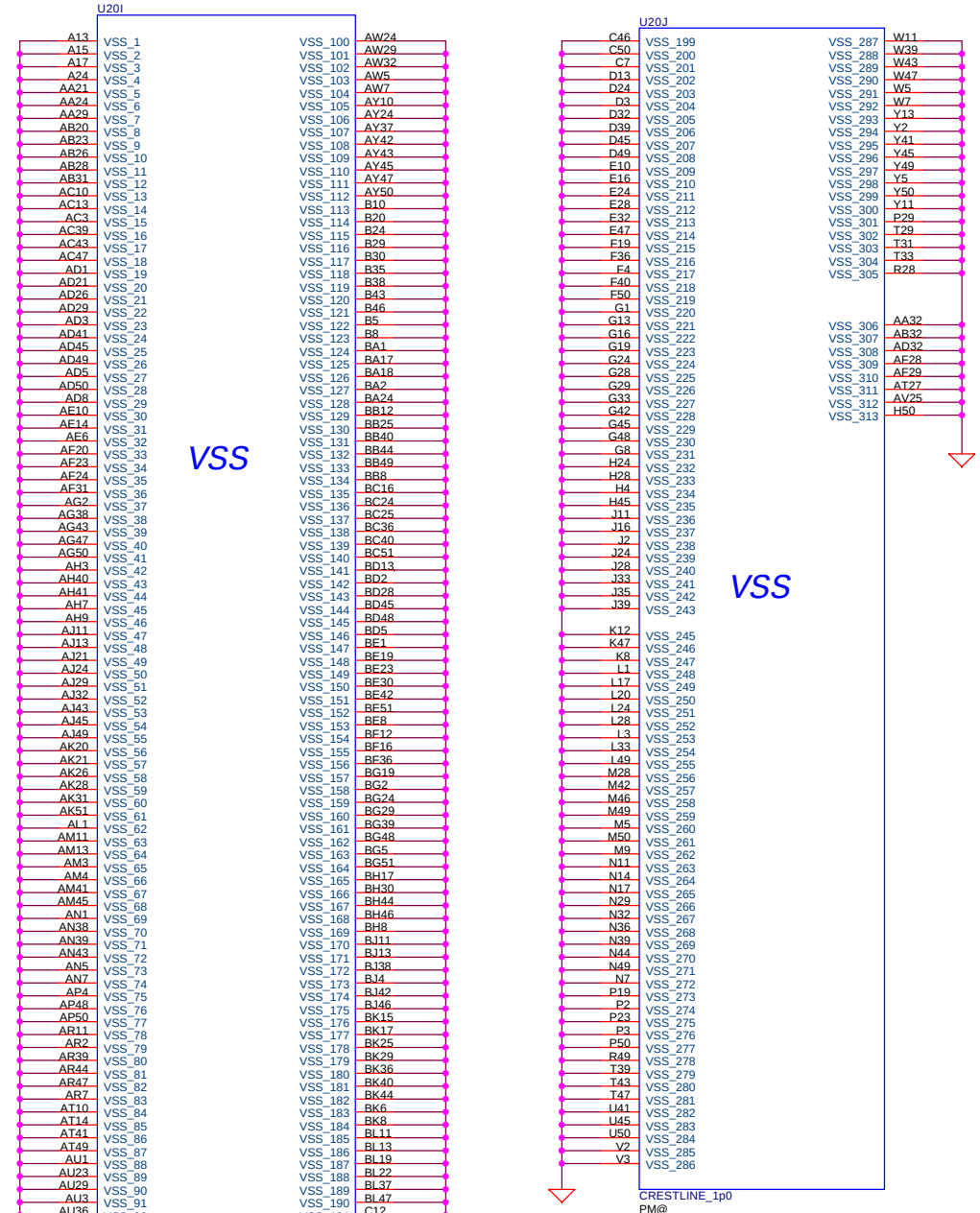
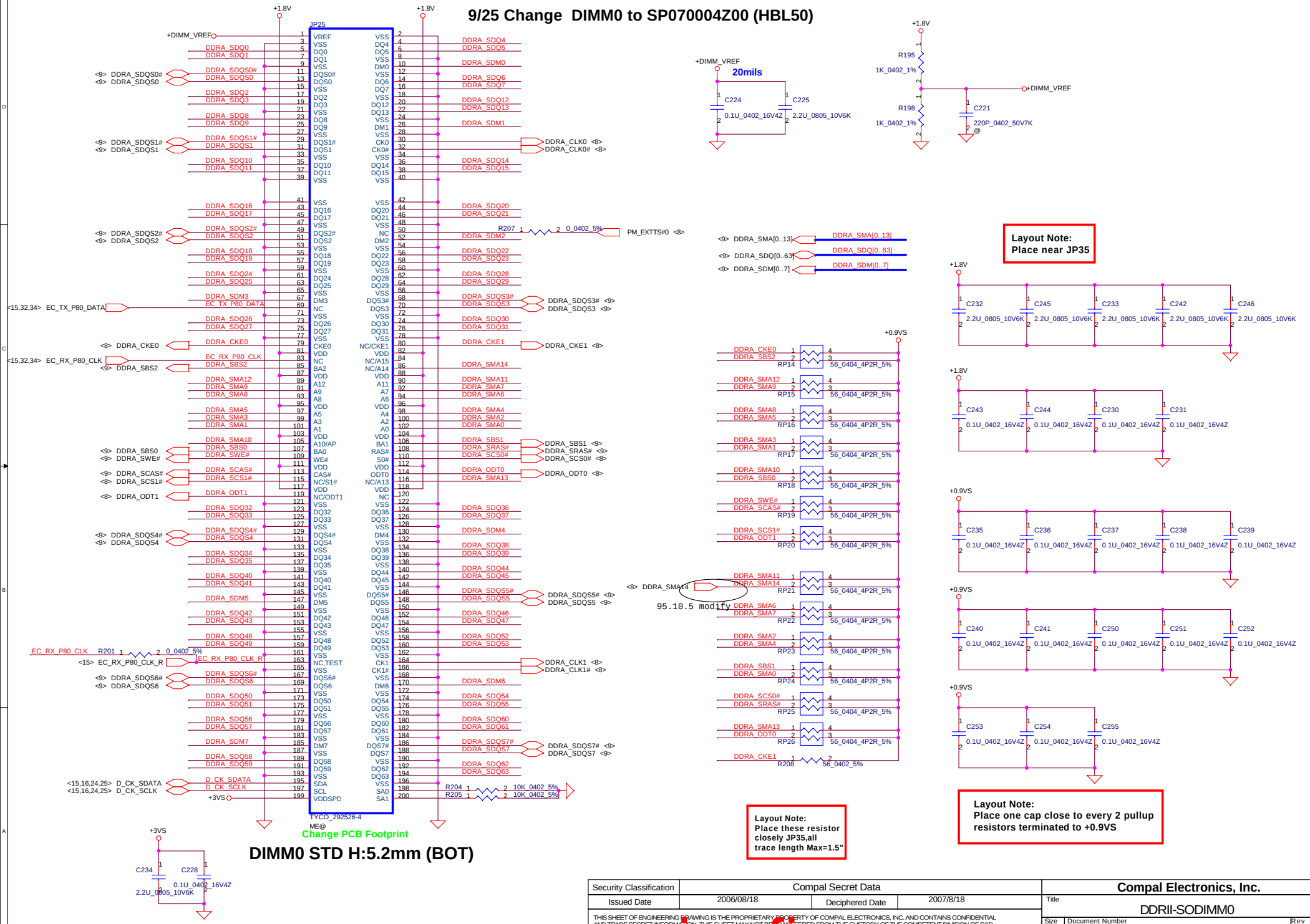


Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title	Crestline (7/7)-GND	
Size B	Document Number LA-3691P	Rev 0.2
Date: Thursday, March 08, 2007	Sheet 13 of 45	

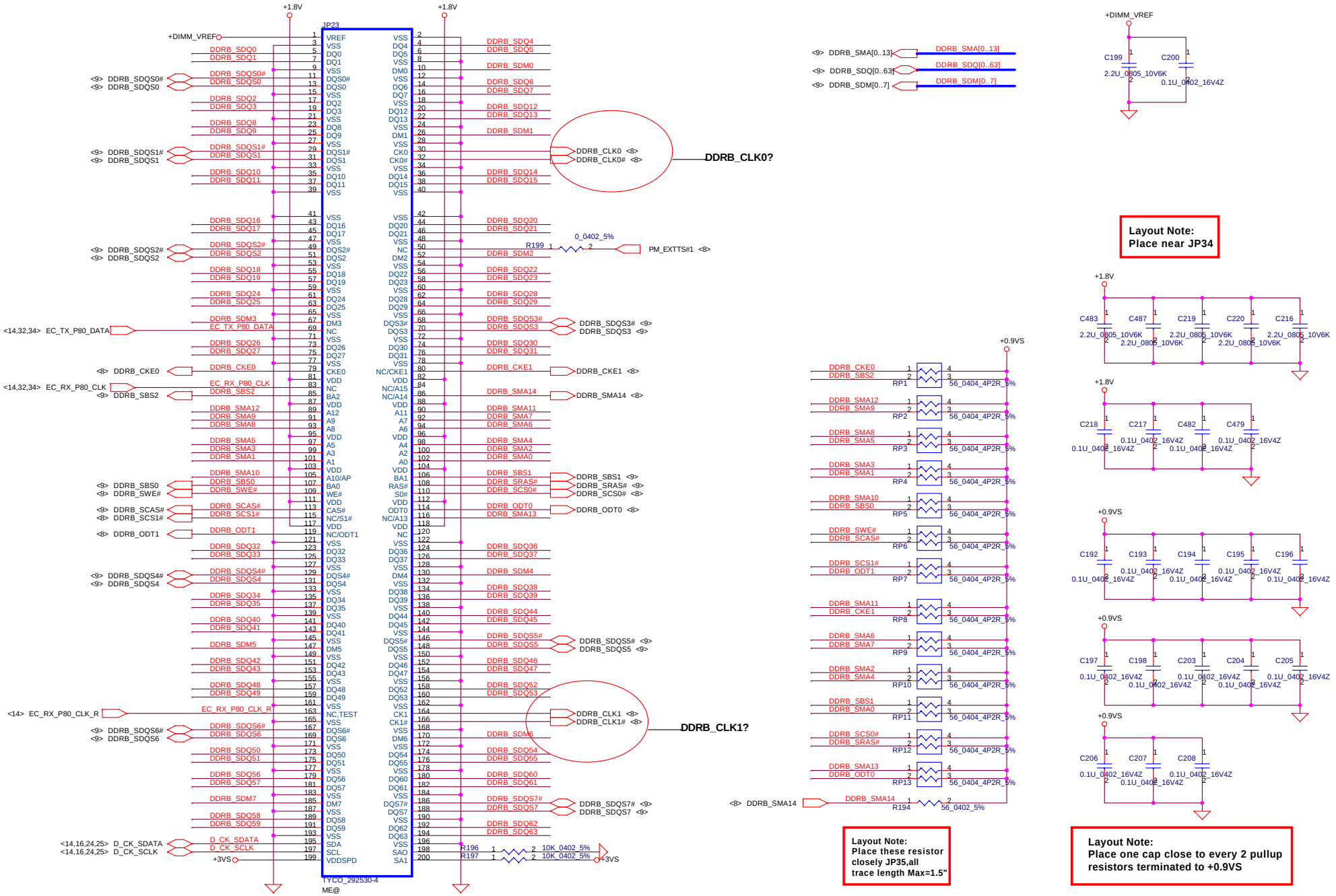
9/25 Change DIMM0 to SP070004Z00 (HBL50)



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.			
Title	DDRII-SODIMM0		
Size B	Document Number LA-3691P		Rev 0.2
Date: Thursday, March 08, 2007	Sheet 14 of 45		

9/25 Change DIMM1 to SP070006F00



Layout Note:
Place these resistor closely JP35,all trace length Max=1.5"

Layout Note:
Place near JP34

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS

DIMM1 STD H:9.2mm (BOT)

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: DDRII-SODIMM1

Size	Document Number	Rev
B	LA-3691P	0.2

Date: Thursday, March 08, 2007 Sheet 15 of 45

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	1	0	200	100	33.3
0	1	1	166	100	33.3

FSB Frequency Selet:

CPU Driven	Stuff						
*(Default)	No Stuff	R401	R408	R417	R430	R438	R447
667MHz	Stuff	R401	R417	R447			
	No Stuff	R408	R430	R438			
800MHz	Stuff	R408	R417	R447			
	No Stuff	R401	R430	R438			

10/17 : Change P/N from SA0001GT00 to SA00001GT10

Need to update Symbol

For ITP_EN, 0 =SRC8/SRC8#; 1 = ITP/ITP#
For 27_SEL, 0 = Enable DOT96 & SRC1,
1= Enable SRC0 & 27MHz
For PCI2_EN, 0 = Overclocking of CPU and SRC Allowed
1 = Overclocking of CPU and SRC NOT allowed

Routing the trace at least 10mil

Place close to U35

ICS9LPRS365/SA00001GT00

<BOM Structure>

* Internal Pull-Up Resistor
* Internal Pull-Down Resistor

Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

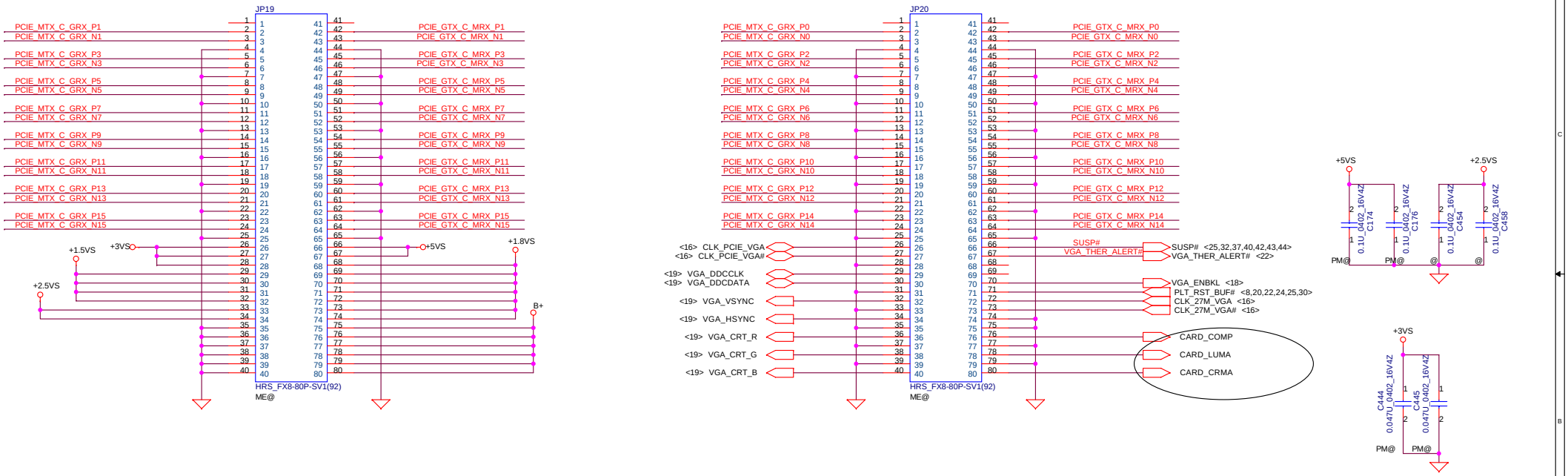
Compal Electronics, Inc.

Title: Clock generator

Size: | Document Number: LA-3691P | Rev: 0.2

Date: Thursday, March 08, 2007 | Sheet 16 of 45

MAX. 4.06A @ 1.8V
MAX. 130mA @ 2.5V
MAX. 655mA @ 3.3V



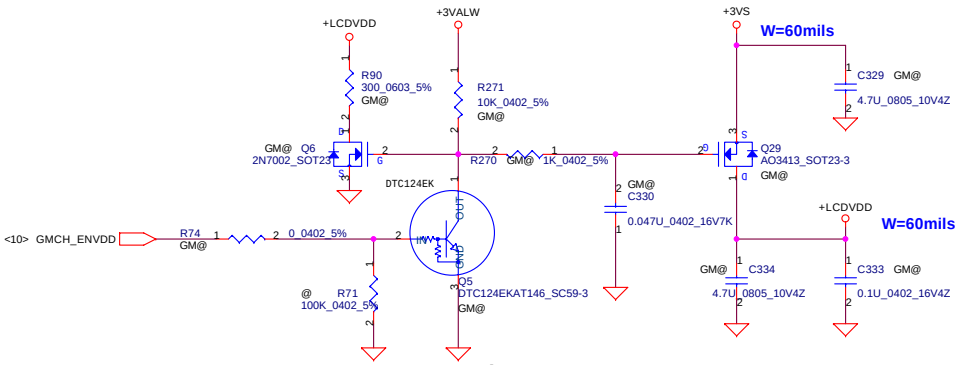
Compal Electronics, Inc.

Title: VGA/B connector

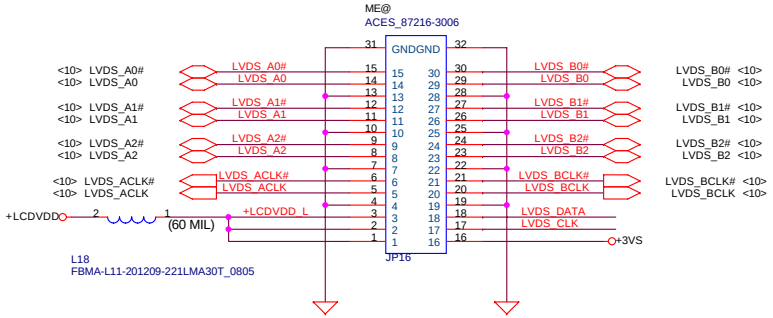
Size	Document Number	Rev
Custom	IEL10 LA-3451P	0.2

Date: Thursday, March 08, 2007 Sheet 17 of 45

LCD POWER CIRCUIT

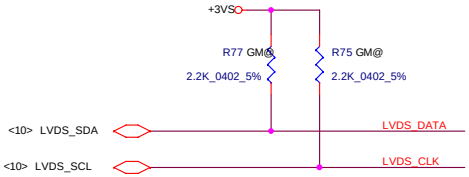


LCD/PANEL BD. Conn.

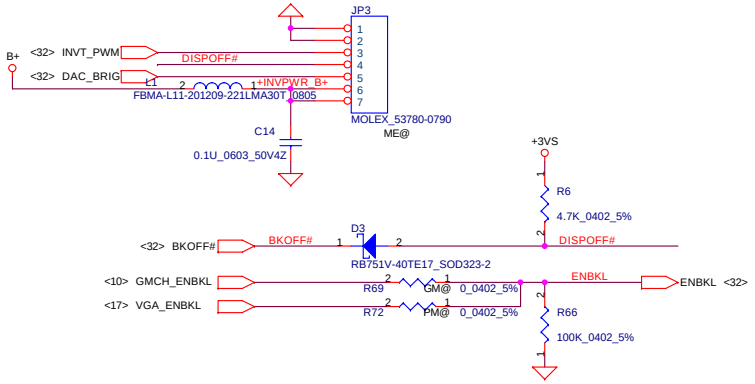


Follow HEL80's pin definition

Except pin 29



INVERTER Conn.



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

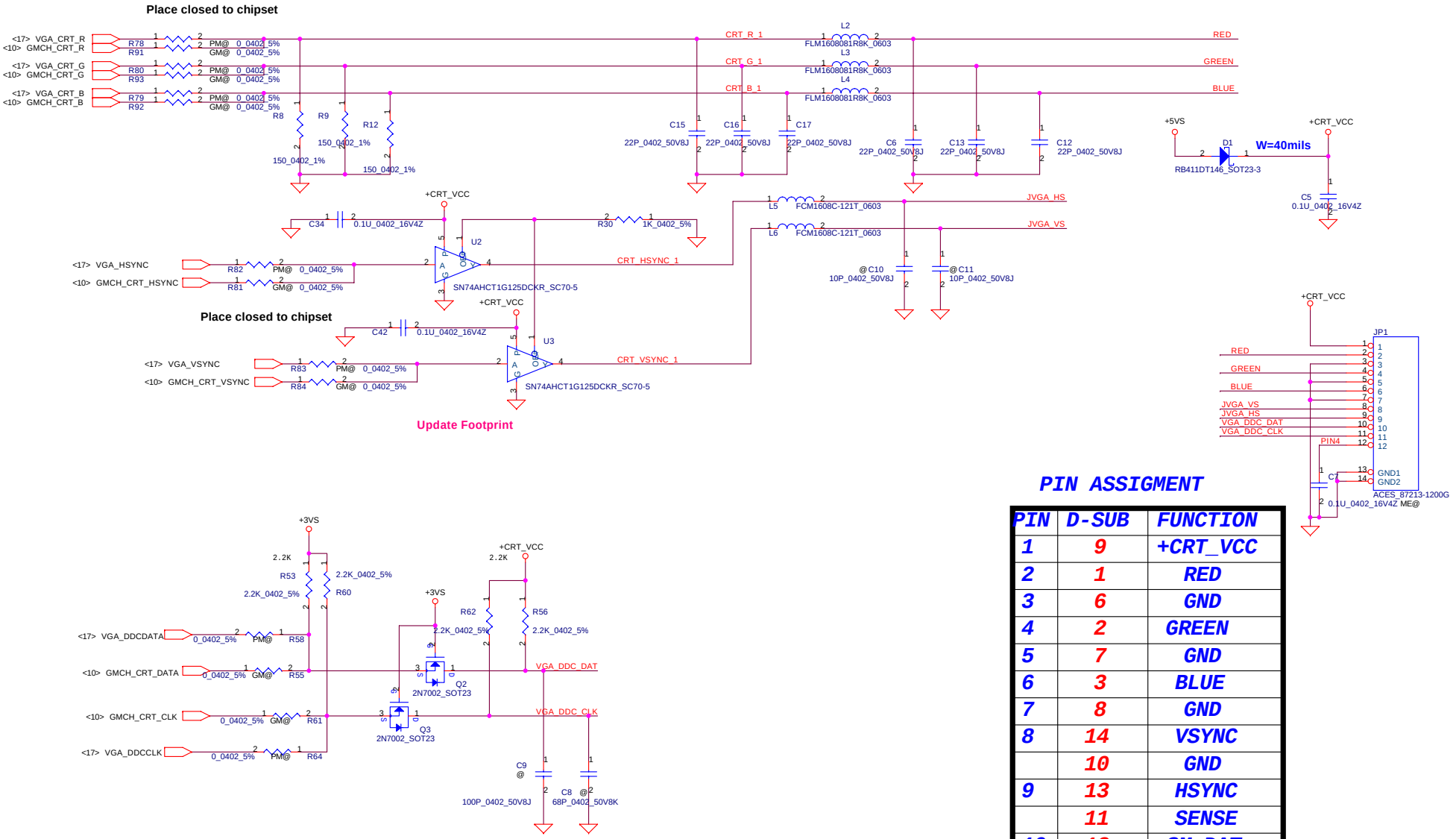
Compal Electronics, Inc.

Title: LVDS & DVI Connector

Size	Document Number	Rev
B	LA-3691P	0.2

Date: Thursday, March 08, 2007 Sheet 18 of 45

CRT Connector



PIN ASSIGMENT

PIN	D-SUB	FUNCTION
1	9	+CRT_VCC
2	1	RED
3	6	GND
4	2	GREEN
5	7	GND
6	3	BLUE
7	8	GND
8	14	VSYNC
	10	GND
9	13	HSYNC
	11	SENSE
10	12	SM_DAT
11	15	SM_CLK
12	4	PIN4

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: CRT & TV-OUT Connector

Size	Document Number	Rev
B	LA-3691P	0.2

Date: Thursday, March 08, 2007 Sheet 19 of 45

10/17 : Change P/N from SA000010G00 to SA00001JU10

10/17 : FootPrint : SA000010G00
BOM : SA00001JU10

+3VS

R97 1 2 8.2K_0402_5% PCI_DEVSEL#
R96 1 2 8.2K_0402_5% PCI_STOP#
R281 1 2 8.2K_0402_5% PCI_TRDY#
R101 1 2 8.2K_0402_5% PCI_FRAME#
R111 1 2 8.2K_0402_5% PCI_PLOCK#
R278 1 2 8.2K_0402_5% PCI_IRDY#
R297 1 2 8.2K_0402_5% PCI_SERR#
R107 1 2 8.2K_0402_5% PCI_PERR#

+3VS

R301 1 2 8.2K_0402_5% PCI_PIRQA#
R128 1 2 8.2K_0402_5% PCI_PIRQB#
R139 1 2 8.2K_0402_5% PCI_PIRQC#
R99 1 2 8.2K_0402_5% PCI_PIRQD#
R298 1 2 8.2K_0402_5% PCI_PIRQE#
R300 1 2 8.2K_0402_5% PCI_PIRQF#
R296 1 2 8.2K_0402_5% PCI_PIRQG#
R121 1 2 8.2K_0402_5% PCI_PIRQH#
R116 1 2 8.2K_0402_5% PCI_REQ#0
R102 1 2 8.2K_0402_5% PCI_REQ#1
R103 1 2 8.2K_0402_5% PCI_REQ#2
R100 1 2 8.2K_0402_5% PCI_REQ#3

U5B

PCI

D20	AD0	REQ0#	A4 PCI_REQ#0
E19	AD1	GNT0#	D7 PCI_GNT#0
D19	AD2	REQ1#/GPIO50	E18 PCI_REQ#1
A20	AD3	GNT1#/GPIO51	C18
D17	AD4	REQ2#/GPIO52	B19 PCI_REQ#2
A21	AD5	GNT2#/GPIO53	F18
A19	AD6	REQ3#/GPIO54	A11 PCI_REQ#3
C19	AD7	GNT3#/GPIO55	C10 PCI_GNT#3
A18	AD8		
B16	AD9	C/BE0#	C17
A12	AD10	C/BE1#	E15
E16	AD11	C/BE2#	F16
A14	AD12	C/BE3#	E17
G16	AD13		
A15	AD14	IRDY#	C8 PCI_IRDY#
B6	AD15	PAR	D9
C11	AD16	PCIRST#	G6 PCIRST#
A9	AD17	DEVSEL#	D16 PCI_DEVSEL#
D11	AD18	PERR#	A7 PCI_PERR#
B12	AD19	PLOCK#	B7 PCI_PLOCK#
C12	AD20	SERR#	F10 PCI_SERR#
D10	AD21	STOP#	C16 PCI_STOP#
C7	AD22	TRDY#	C9 PCI_TRDY#
E13	AD23	FRAME#	A17 PCI_FRAME#
E11	AD24		
E13	AD25	PLTRST#	AG24 PLT_RST#
E12	AD26	PCICLK	B10 CLK_PCI_ICH <16>
D8	AD27	PME#	G7 PCI_PME# <32>
A6	AD28		
E8	AD29		
D6	AD30		
A3	AD31		

Interrupt I/F

PCI_PIRQA# F9	PIRQA#	PIRQE#/GPIO2	F8 PCI_PIRQE#
PCI_PIRQB# B5	PIRQB#	PIRQF#/GPIO3	G11 PCI_PIRQF#
PCI_PIRQC# C5	PIRQC#	PIRQG#/GPIO4	F12 PCI_PIRQG#
PCI_PIRQD# A10	PIRQD#	PIRQH#/GPIO5	B3 PCI_PIRQH#

ICH8M REV 1.0

Place closely pin B10

CLK_PCI_ICH
R280 10_0402_5% @
C356 10P_0402_50V8J @

R284 1 2 1K_0402_5% @ PCI_GNT#3
R286 1 2 1K_0402_5% @ PCI_GNT#0
R285 1 2 1K_0402_5% @ SPI_CS#1 <22>

A16 Swap Override Strap	
PCI_GNT#3	Low= A16 swap override Enable High= Default*

Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*

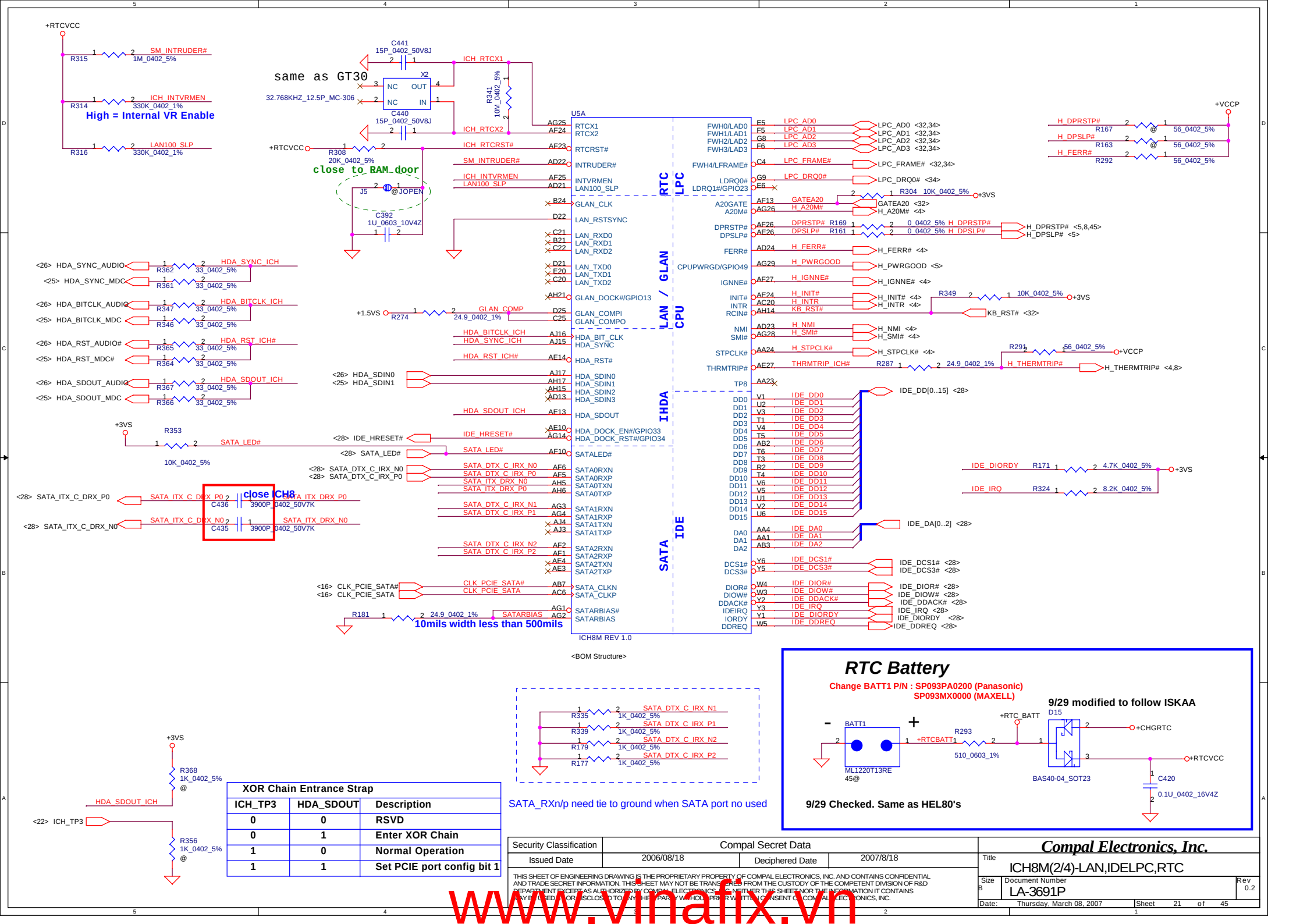
+3VS
U21 NC7SZ08P5X_NL_SC70-5 @
PLT_RST# → PLT_RST_BUF# <8,17,22,24,25,30>
R370 100K_0402_5%
R340 0_0402_5%

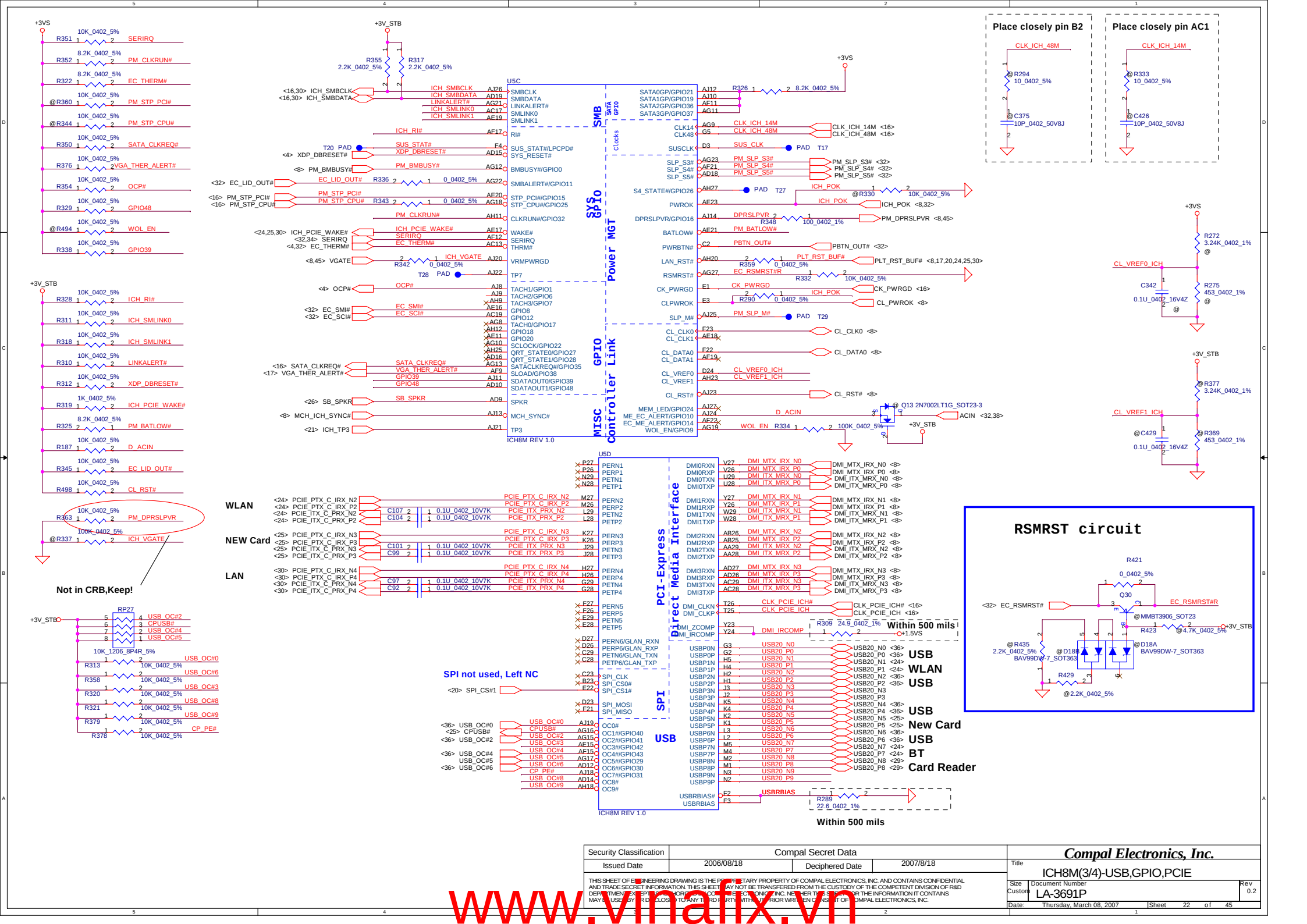
+3VS
U8 NC7SZ08P5X_NL_SC70-5 @
PCIRST# → PCI_RST# <32,34>
R157 100K_0402_5%
R144 0_0402_5%

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title	ICH8M(1/4)-PCI		
Size	Document Number		Rev
	LA-3691P		0.2
Date:	Thursday, March 08, 2007	Sheet	20 of 45





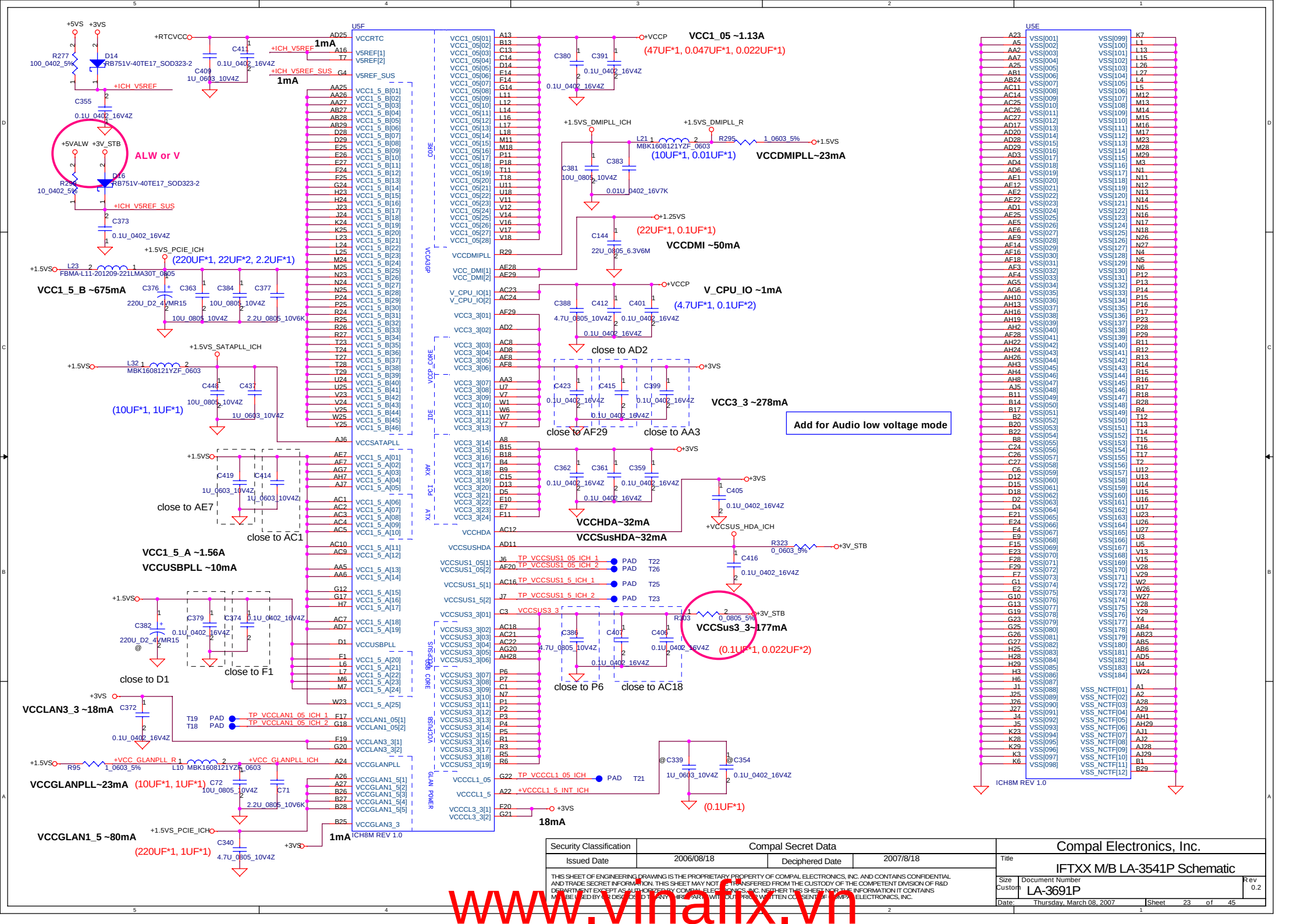
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: ICH8M(3/4)-USB,GPIO,PCIE

Size	Document Number	Rev
Custom	LA-3691P	0.2

Date: Thursday, March 08, 2007 Sheet 22 of 45



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

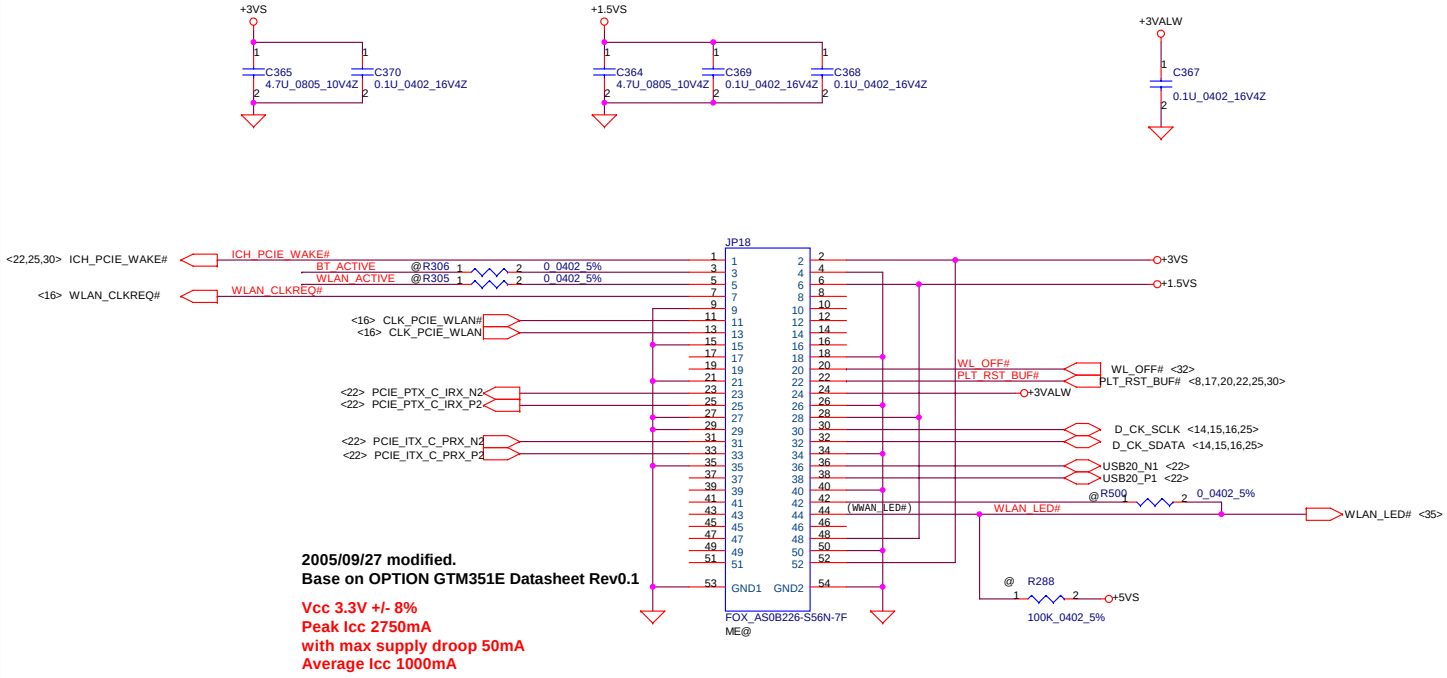
Compal Electronics, Inc.

Title: IFTXX M/B LA-3541P Schematic

Size	Document Number	Rev
Custom	LA-3691P	0.2

Date: Thursday, March 08, 2007 Sheet 23 of 45

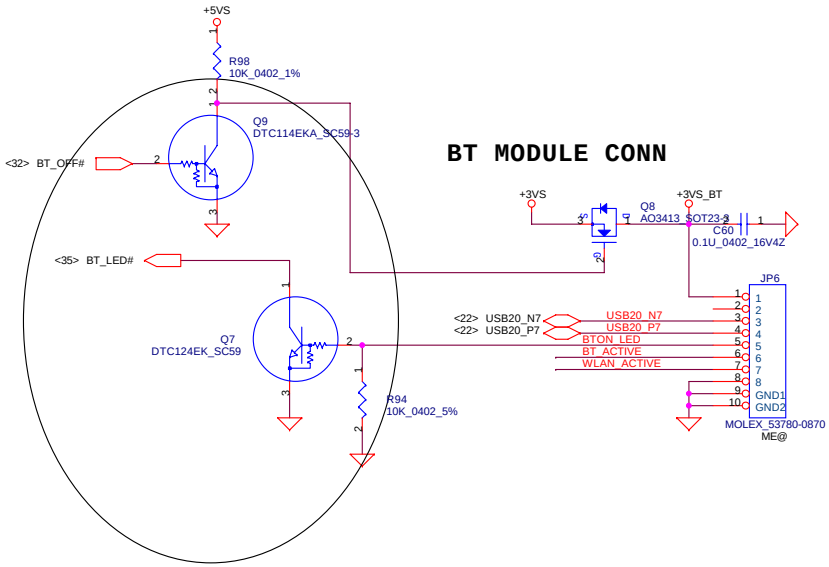
Mini-Express Card for 3G Or TV Tuner
Mini-Express Card for WLAN



2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1

Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

BT MODULE CONN



Security Classification	Compal Secret Data		
Issued Date	2006/08/05	Deciphered Date	2007/08/05

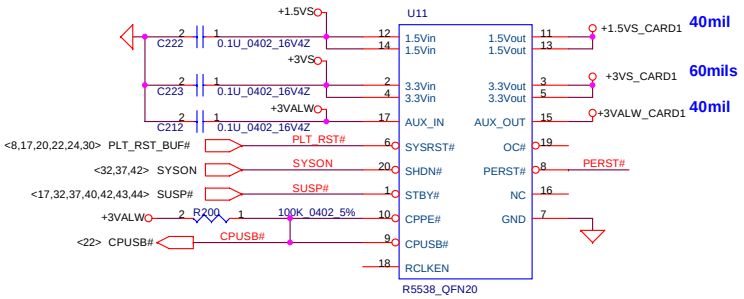
Compal Electronics, Inc.

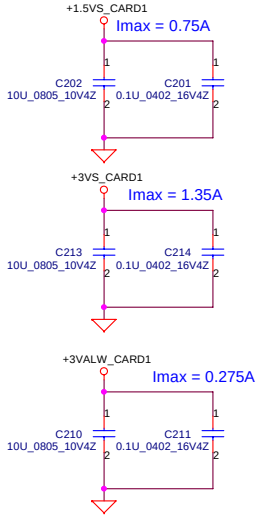
Title: **Mini-Card/3G/FeliCa/FP**

Size	Document Number	Rev
	LA-3691P	0.2

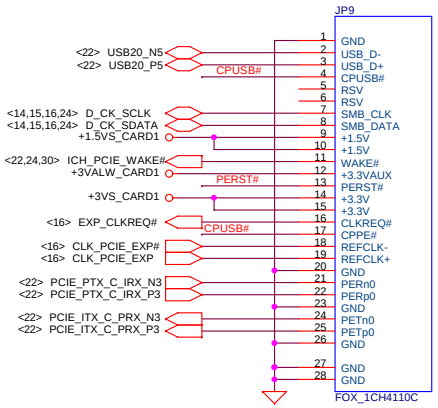
Date: Thursday, March 08, 2007 Sheet 24 of 45

Express Card Power Switch



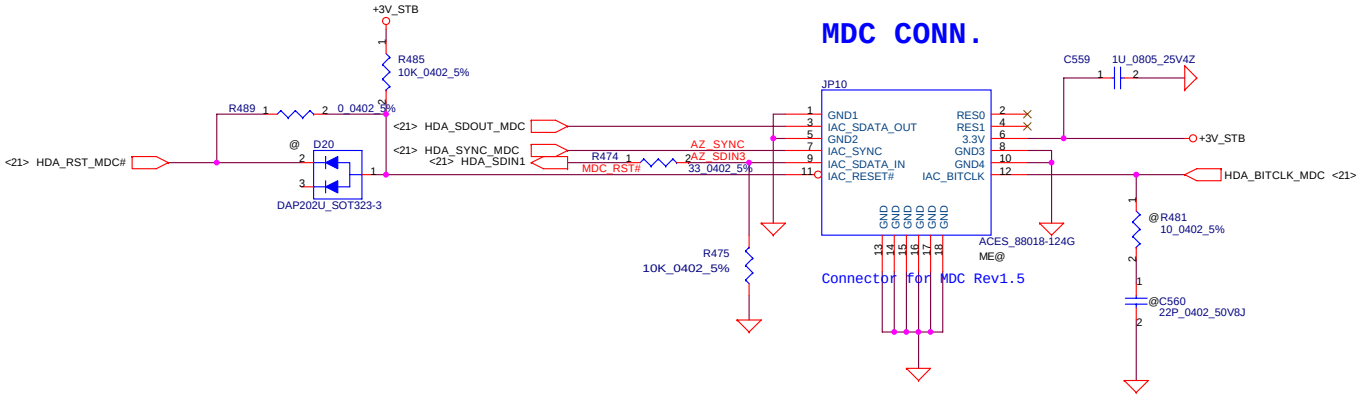


New Card Socket (Left/TOP)



(NEW)

MDC CONN.



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: NEW CARD & USB Connector

Size	Document Number	Rev
B	LA-3691P	0.2

Date: Thursday, March 08, 2007 | Sheet 25 of 45

AC97 Codec

28.7K for Module Design (VDDA = 4.702)

(output = 250 mA)

	SUB WOOFER SUPPORT
ALC262	
ALC861D	

Window mode

DOS mode Driver initial

ACPI

RST

EC_MUTE

12sec

DOS mode

DOS mode

RST

EC_MUTE

12sec

GND GNDA

Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

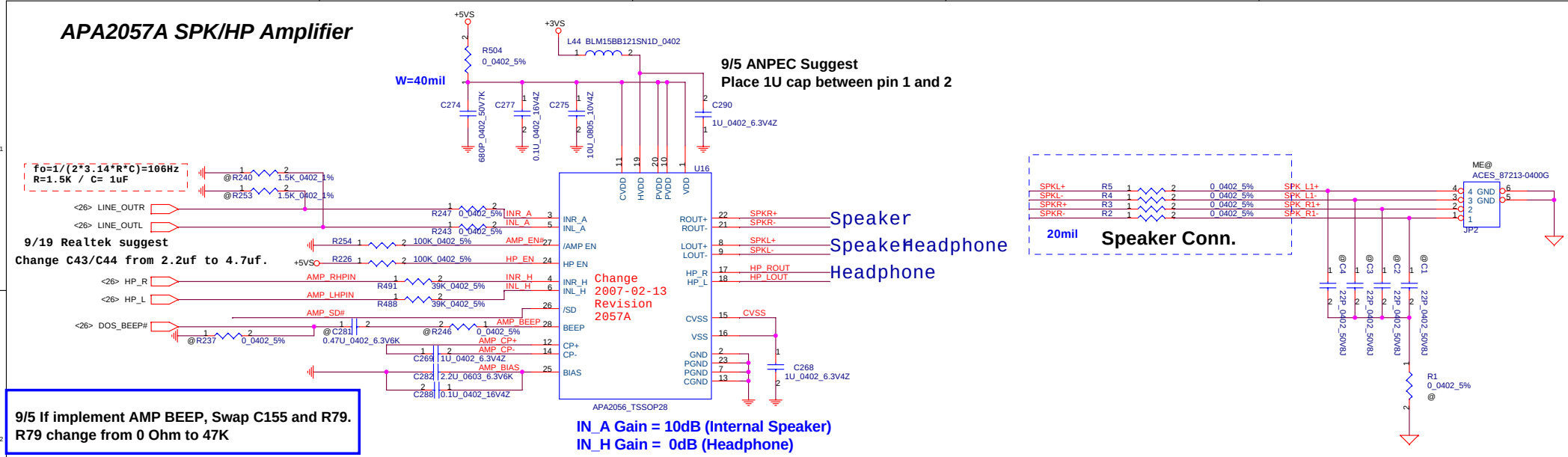
Compal Electronics, Inc.

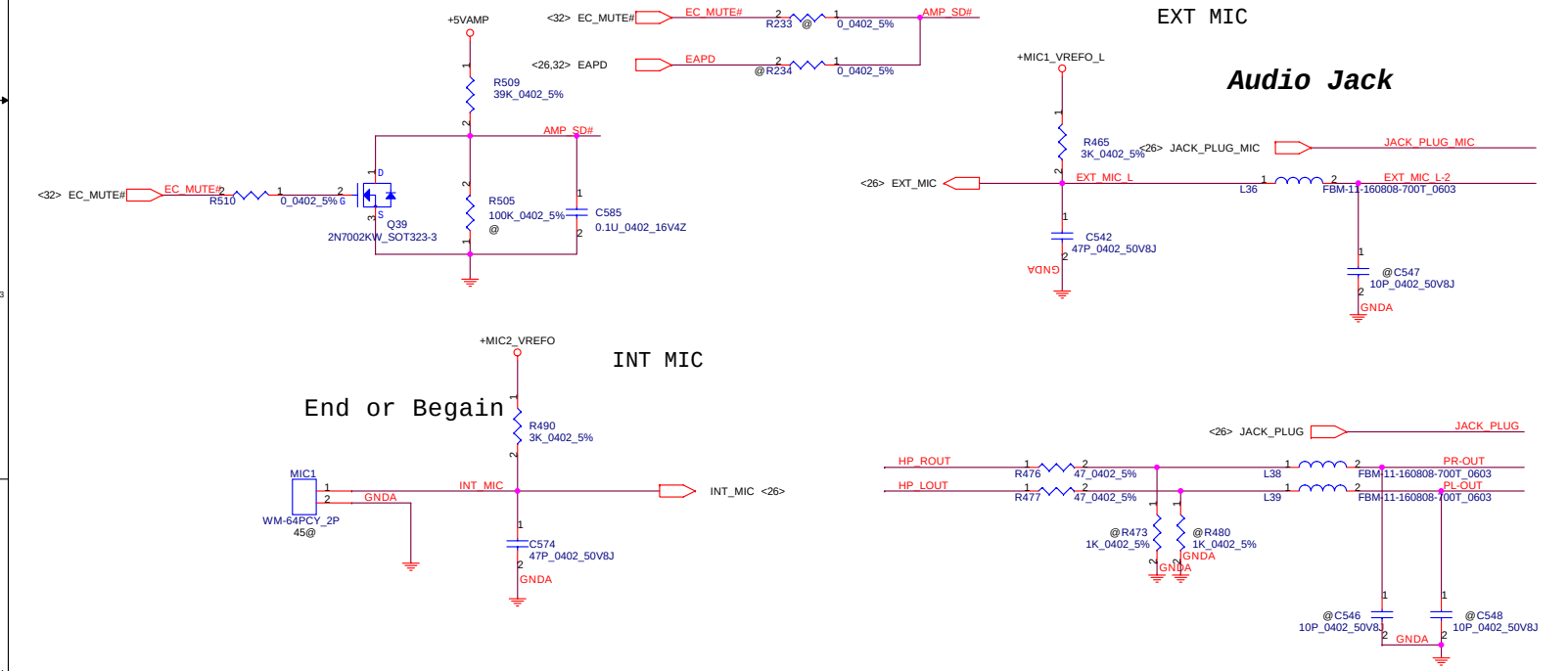
Title: ALC861 VD Codec

Size: Custom | Document Number: IEL10 LA-3451P | Rev: 0.2

Date: Thursday, March 08, 2007 | Sheet 26 of 45

APA2057A SPK/HP Amplifier





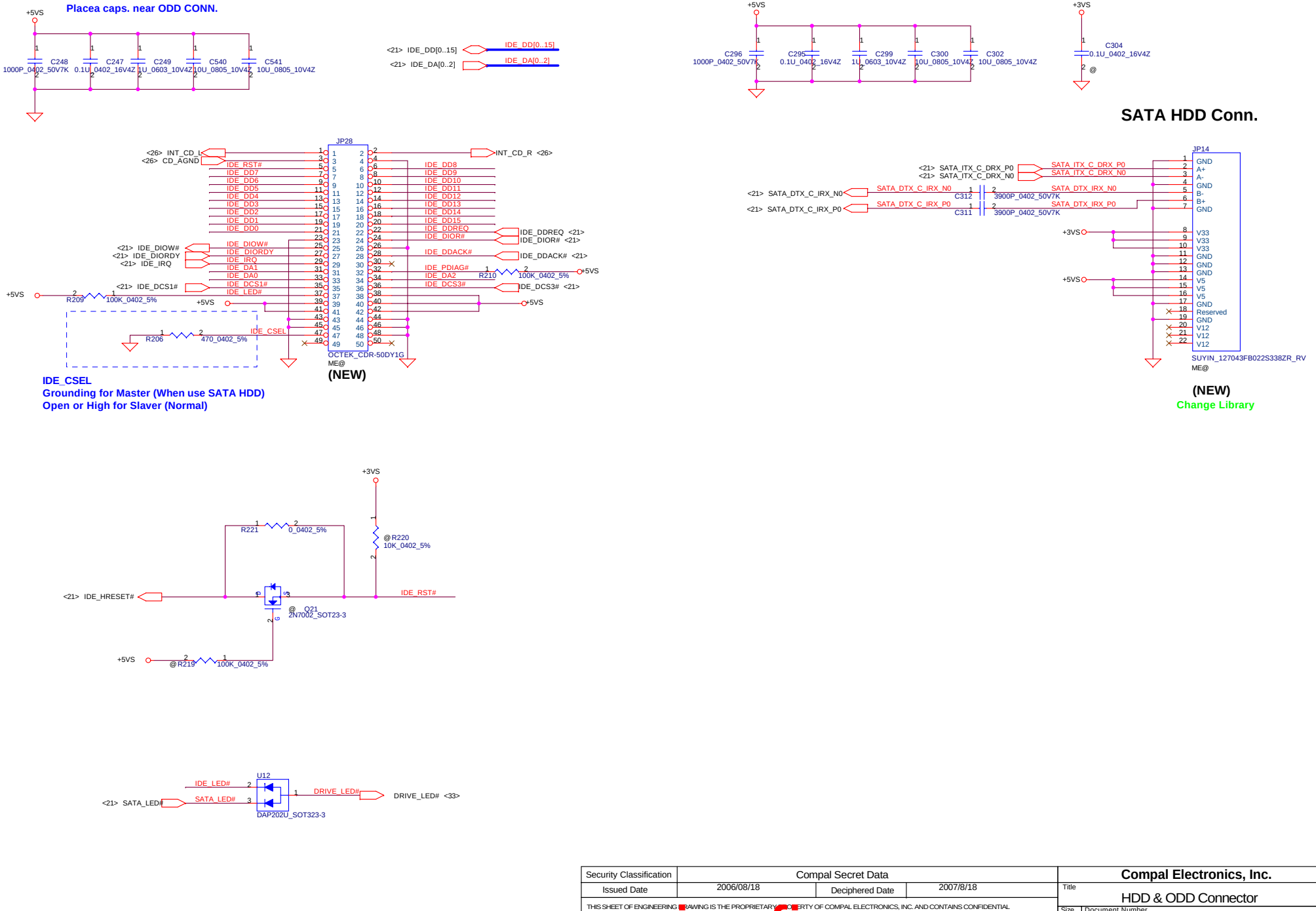
Security Classification	Compal Secret Data		
Issued Date	2006/08/05	Deciphered Date	2007/08/05

Compal Electronics, Inc.

Title: AMP/VR/Audio Jack/MIC

Size	Document Number	Rev
Custom	LA-3691P	0.2

Date: Thursday, March 08, 2007 Sheet 27 of 45



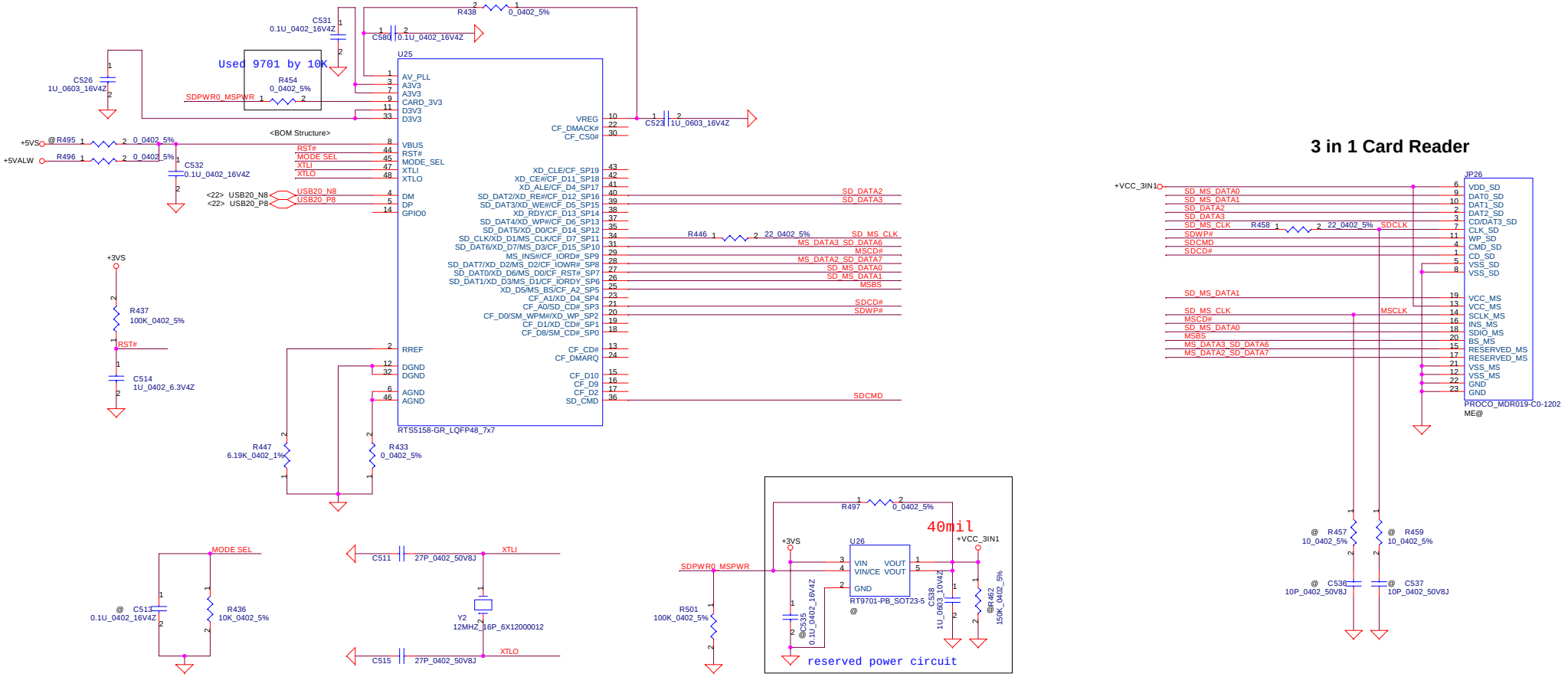
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: HDD & ODD Connector

Size	Document Number	Rev
B	LA-3691P	0.2

Date: Thursday, March 08, 2007 Sheet 28 of 45



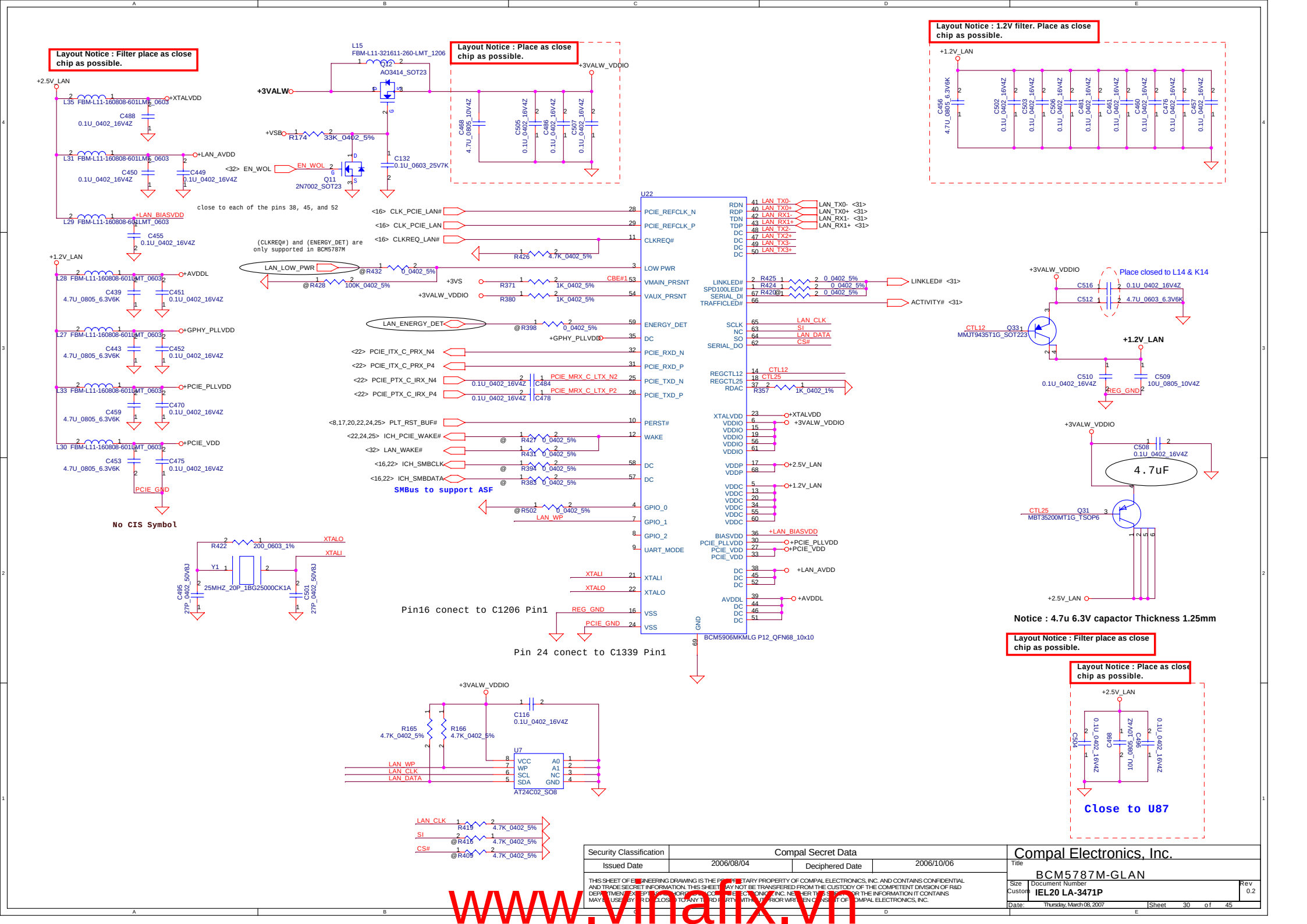
Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

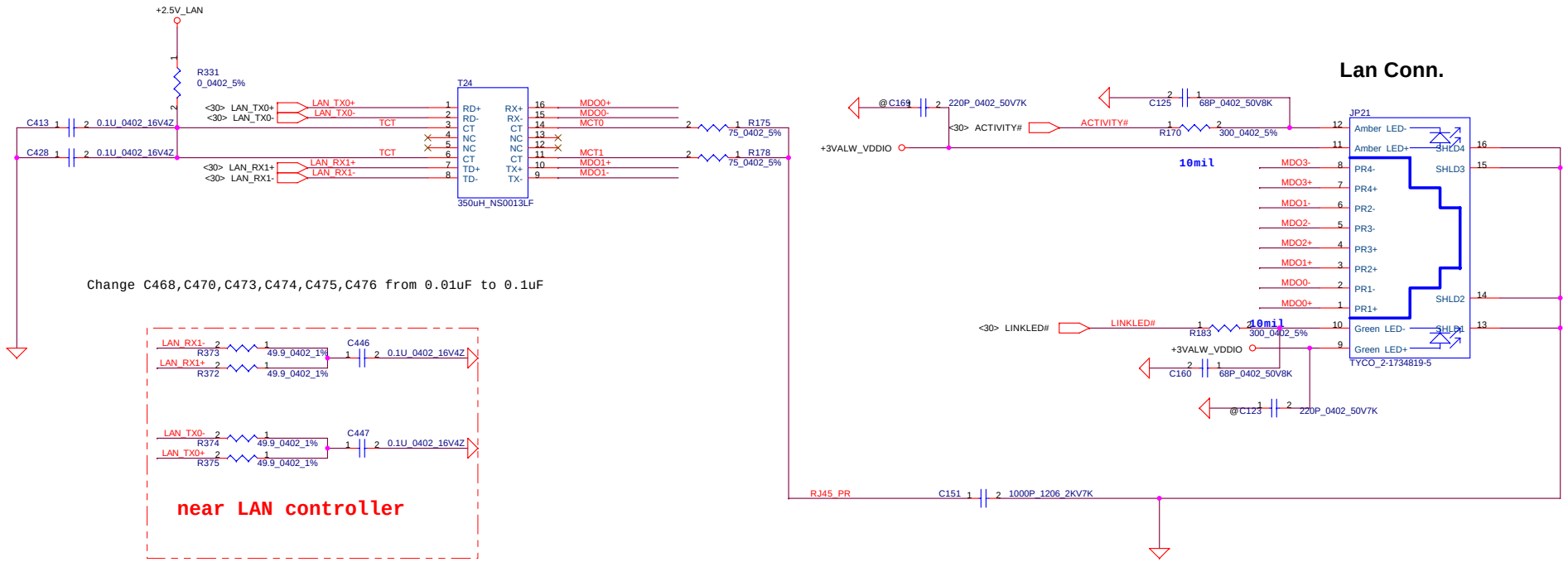
Compal Electronics, Inc.

Title: *1394+3 in 1 Card*

Size	Document Number	Rev
Custom	*LA-3691P*	0.2

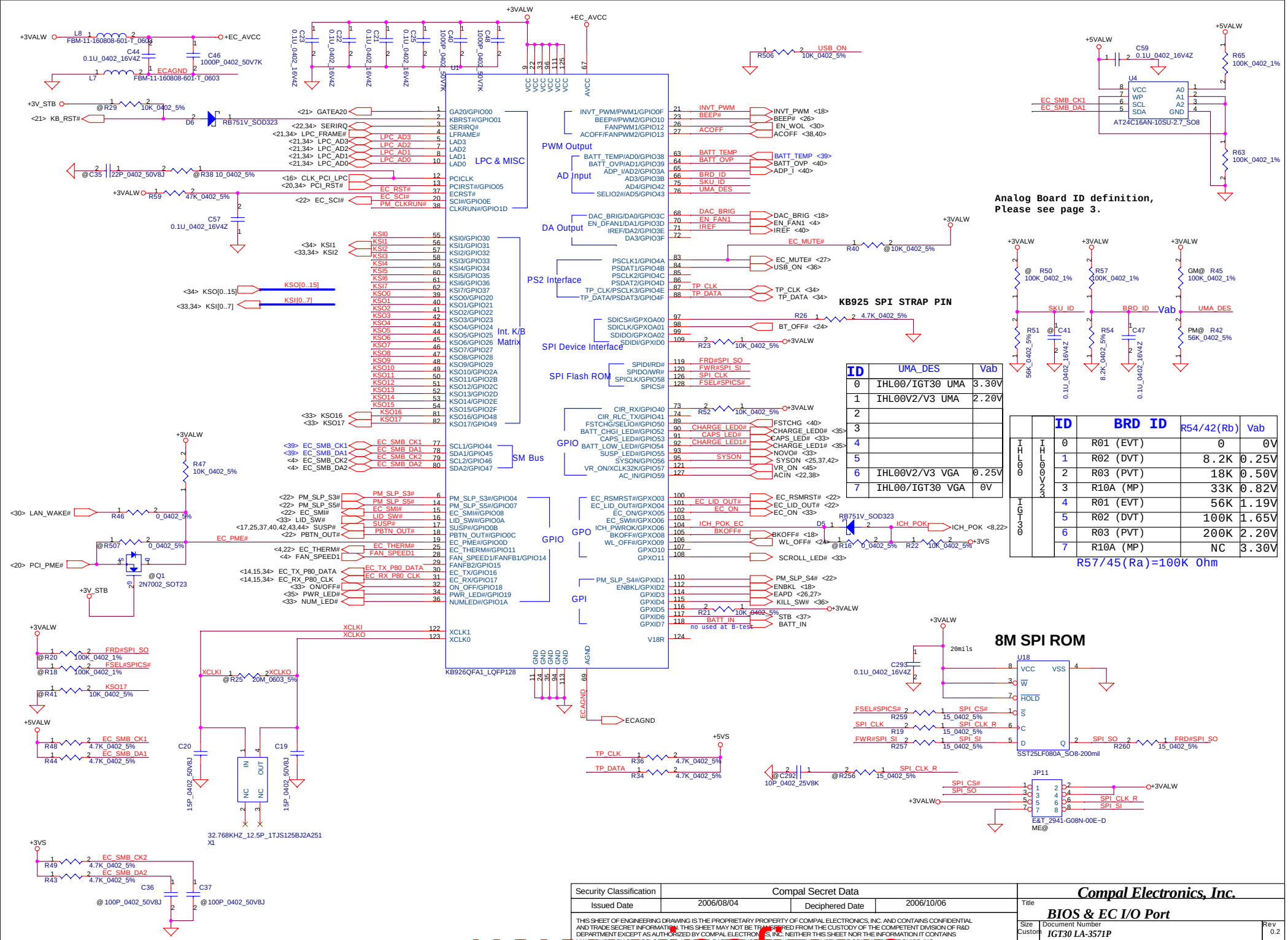
Date: Thursday, March 08, 2007 | Sheet 29 of 45


Layout Notice : Filter place as close chip as possible.
Layout Notice : Place as close chip as possible.
Layout Notice : 1.2V filter. Place as close chip as possible.
+2.5V_LAN
+XTALVDD
+LAN_AVDD
+LAN_BIASVDD
+1.2V_LAN
+AVDDL
+GPHY_PLLVDD
+PCIE_PLLVDD
+PCIE_VDD
PCIE_GND
No CIS Symbol
+3VALW
+3VALW_VDDIO
close to each of the pins 38, 45, and 52
(CLKREQ#) and (ENERGY_DET) are only supported in BCM5787M
SMBus to support ASF
Pin16 conect to C1206 Pin1
Pin 24 conect to C1339 Pin1
BCM5906MKMLG P12_QFN68_10x10
Place closed to L14 & K14
Notice : 4.7u 6.3V capactor Thickness 1.25mm
Close to U87
Security Classification
Compal Secret Data
Issued Date
2006/08/04
Deciphered Date
2006/10/06
Compal Electronics, Inc.
BCM5787M-GLAN
IEL20 LA-3471P
Thursday, March 08, 2007
www.vinafix.vn



Security Classification	Compal Secret Data		
Issued Date	2006/08/04	Deciphered Date	2006/10/06

Compal Electronics, Inc.	
Title	LAN CONTROLLER
Size: Custom	Document Number: LA-3691P
Rev	0.2
Date: Thursday, March 08, 2007	Sheet 31 of 45



ID	UMA_DES	Vab
0	IHL00/IGT30 UMA	3.30V
1	IHL00V2/V3 UMA	2.20V
2		
3		
4		
5		
6	IHL00V2/V3 VGA	0.25V
7	IHL00/IGT30 VGA	0V

		ID	BRD ID	R54/42(Rb)	Vab
IHL00	IHL00V23	0	R01 (EVT)	0	0V
		1	R02 (DVT)	8.2K	0.25V
		2	R03 (PVT)	18K	0.50V
		3	R10A (MP)	33K	0.82V
IGT30		4	R01 (EVT)	56K	1.19V
		5	R02 (DVT)	100K	1.65V
		6	R03 (PVT)	200K	2.20V
		7	R10A (MP)	NC	3.30V

R57/45(Ra)=100K Ohm

Security Classification	Compal Secret Data
Issued Date	2006/08/04
Deciphered Date	2006/10/06

Compal Electronics, Inc.

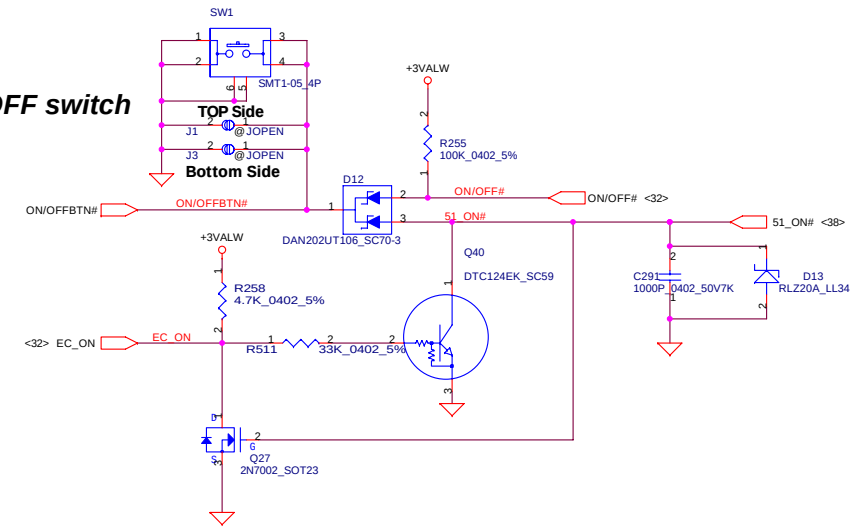
Title: BIOS & EC I/O Port

Size: Custom | Document Number: IGT30 LA-3571P | Rev: 0.2

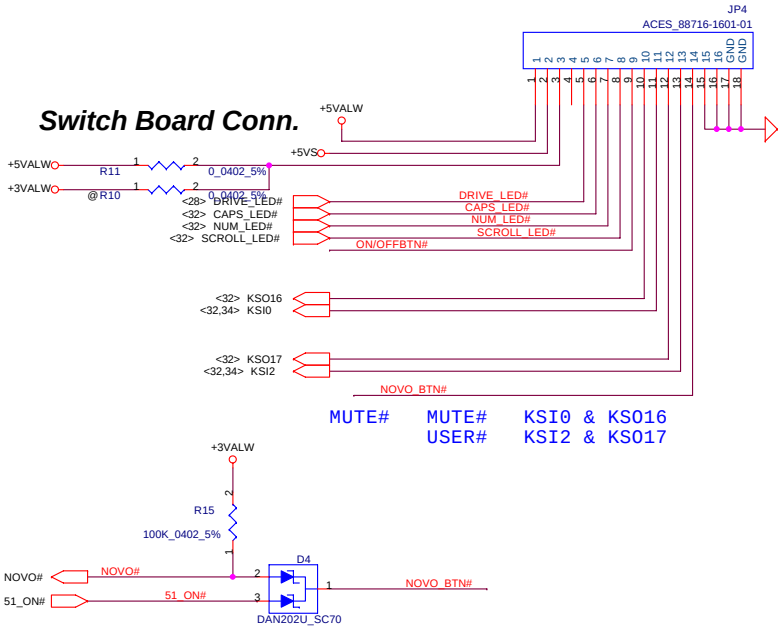
Date: Thursday, March 08, 2007 | Sheet 32 of 45

Power Button

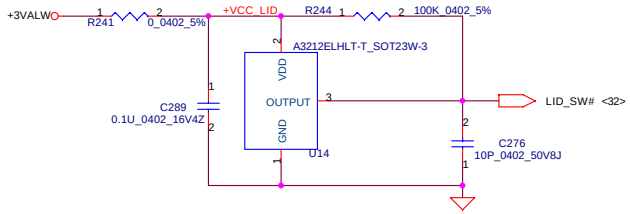
ON/OFF switch



Switch Board Conn.



Lid Switch



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

Size	Document Number	Rev
B	LA-3691P	0.2

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INT_KBD Conn.

KSI[0..7] → KSI[0..7] <32,33>

KSO[0..15] → KSO[0..15] <32>

KSI0	C65	KSO4	C66
KSI1	C73	KSO5	C64
KSI2	C63	KSO6	C82
KSI3	C78	KSO7	C81
KSI4	C76	KSO8	C67
KSI5	C62	KSO9	C61
KSI6	C75	KSO10	C85
KSI7	C74	KSO11	C70
KSO0	C77	KSO12	C83
KSO1	C79	KSO13	C69
KSO2	C80	KSO14	C84
KSO3	C68	KSO15	C86

All: 1 — 2 @100P_0402_50V8J

For IHL00

ME@
ACES_85202-24051

KSI1	1	1	
KSI7	2	2	
KSI6	3	3	
KSO9	4	4	
KSI4	5	5	
KSI5	6	6	
KSO0	7	7	
KSI2	8	8	
KSI3	9	9	
KSO5	10	10	
KSO1	11	11	
KSI0	12	12	
KSO2	13	13	
KSO4	14	14	
KSO7	15	15	
KSO8	16	16	
KSO6	17	17	
KSO3	18	18	
KSO12	19	19	
KSO13	20	20	
KSO14	21	21	
KSO11	22	22	
KSO10	23	23	
KSO15	24	24	
	25	G1	
	26	G2	

JP7

To TP/B Conn.

+5VS
<32> TP_DATA
<32> TP_CLK
TP_DATA
TP_CLK

JP8
ACES_87151-0807G
ME@

+5VS
C117
0.1U_0402_16V4Z

TP_DATA
TP_CLK
@D10
PSOT24C_SOT23

Update Footprint

FOR LPC SIO DEBUG PORT

JP13

1	+5VS		
2			
3	+3VS		
4			
5			
6		CLK_14M_SIO	<16>
7	LPC_AD0	LPC_AD0	<21,32>
8	LPC_AD1	LPC_AD1	<21,32>
9	LPC_AD2	LPC_AD2	<21,32>
10	LPC_AD3	LPC_AD3	<21,32>
11	LPC_FRAME#	LPC_FRAME#	<21,32>
12	LPC_DRQ0#	LPC_DRQ0#	<21>
13	PCI_RST#	PCI_RST#	<20,32>
14			
15	CLK_PCI_DB	CLK_PCI_DB	<16>
16	SERIRQ	SERIRQ	<22,32>
17			
18			
19			
20			

R265 2 — 1 10K_0402_5%

ACES_85201-2005
ME@

EC DEBUG PORT

+3VALW
<14,15,32> EC_TX_P80_DATA
<14,15,32> EC_RX_P80_CLK
EC_TX_P80_DATA
EC_RX_P80_CLK

JP12
ACES_85205-0400
ME@

Security Classification	Compal Secret Data	
Issued Date	2006/08/18	Deciphered Date 2007/8/18

Compal Electronics, Inc.

Title: EC ENE KB910L(Reserved)

Size: B | Document Number: LA-3691P | Rev: 0.2

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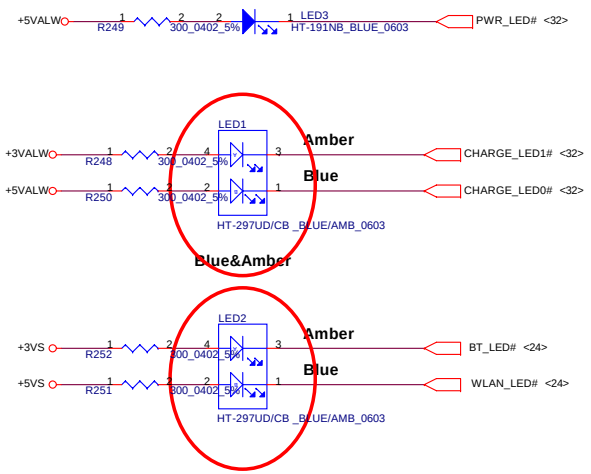
LED



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: MDC/CIR & LED

Size	Document Number	Rev
B	LA-3691P	0.2

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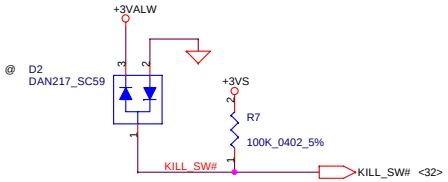
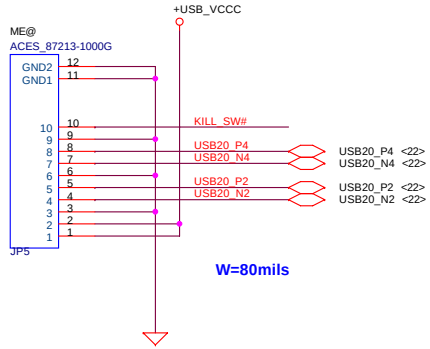
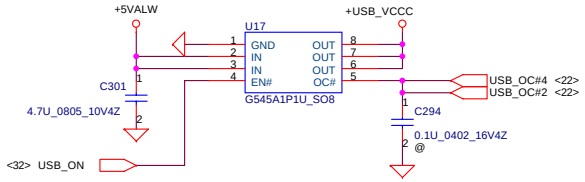
USB Conn.

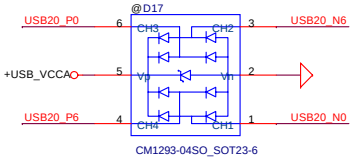
W=80mils

Kill SWITCH

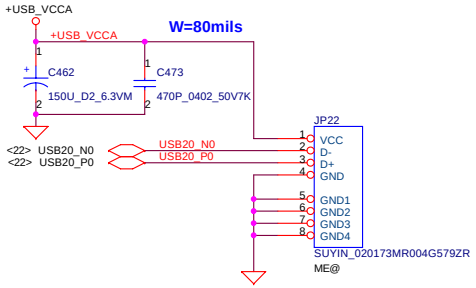


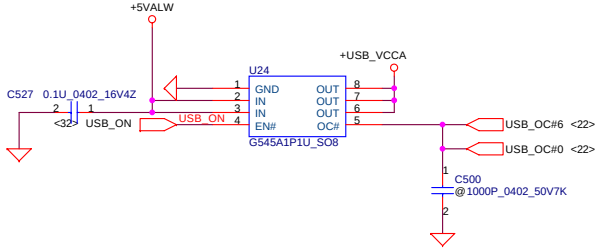




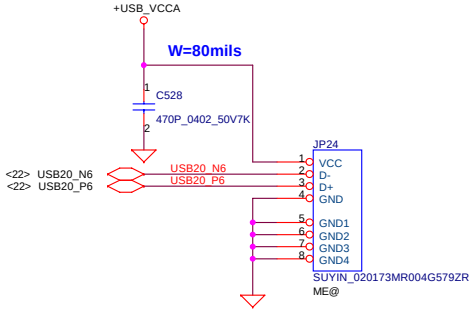


USB CONN. 1





USB CONN. 2



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: Power OK, Reset and RTC Circuit, TP

Size	Document Number	Rev
B	LA-3691P	0.2

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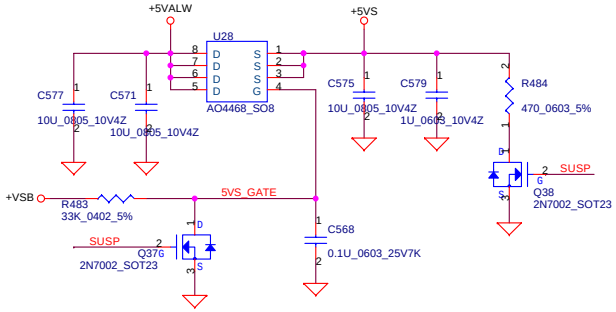
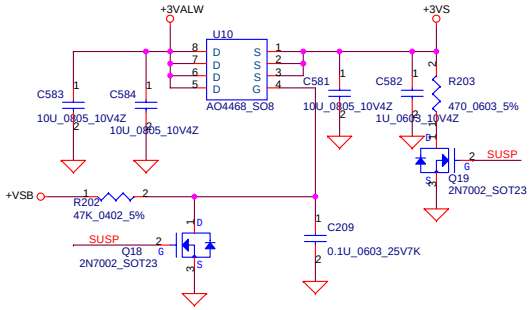
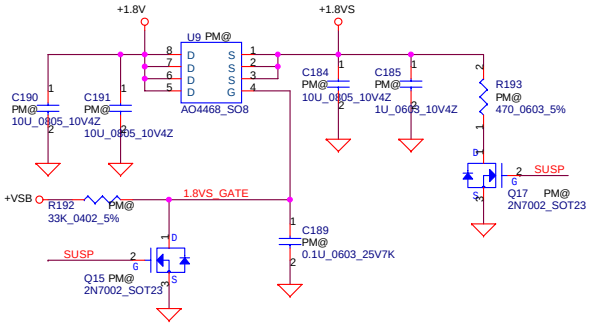
+5VALW TO +5VS



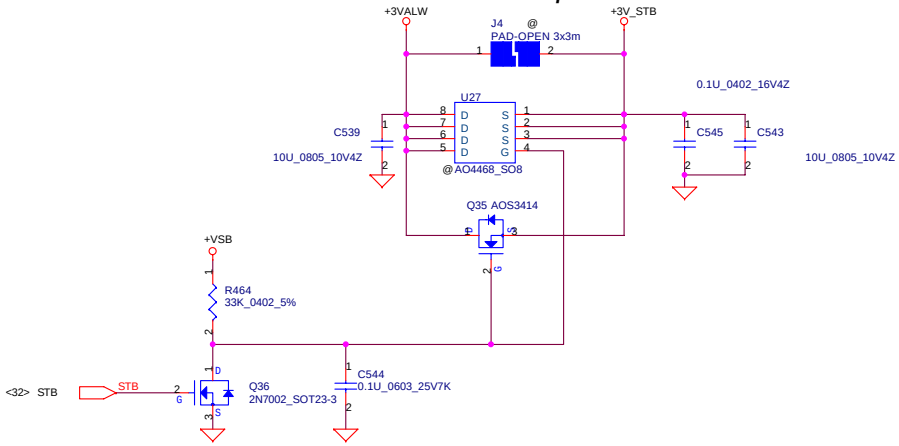
+3VALW TO +3VS

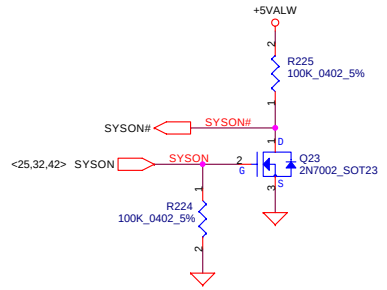


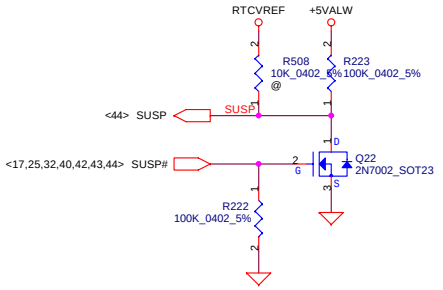
+1.8V to +1.8VS

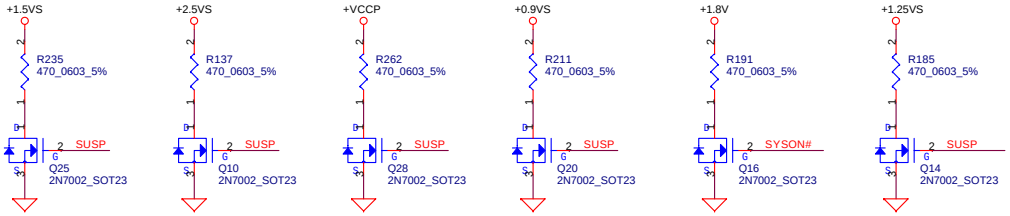


+3VALW to +3V Transfer









Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
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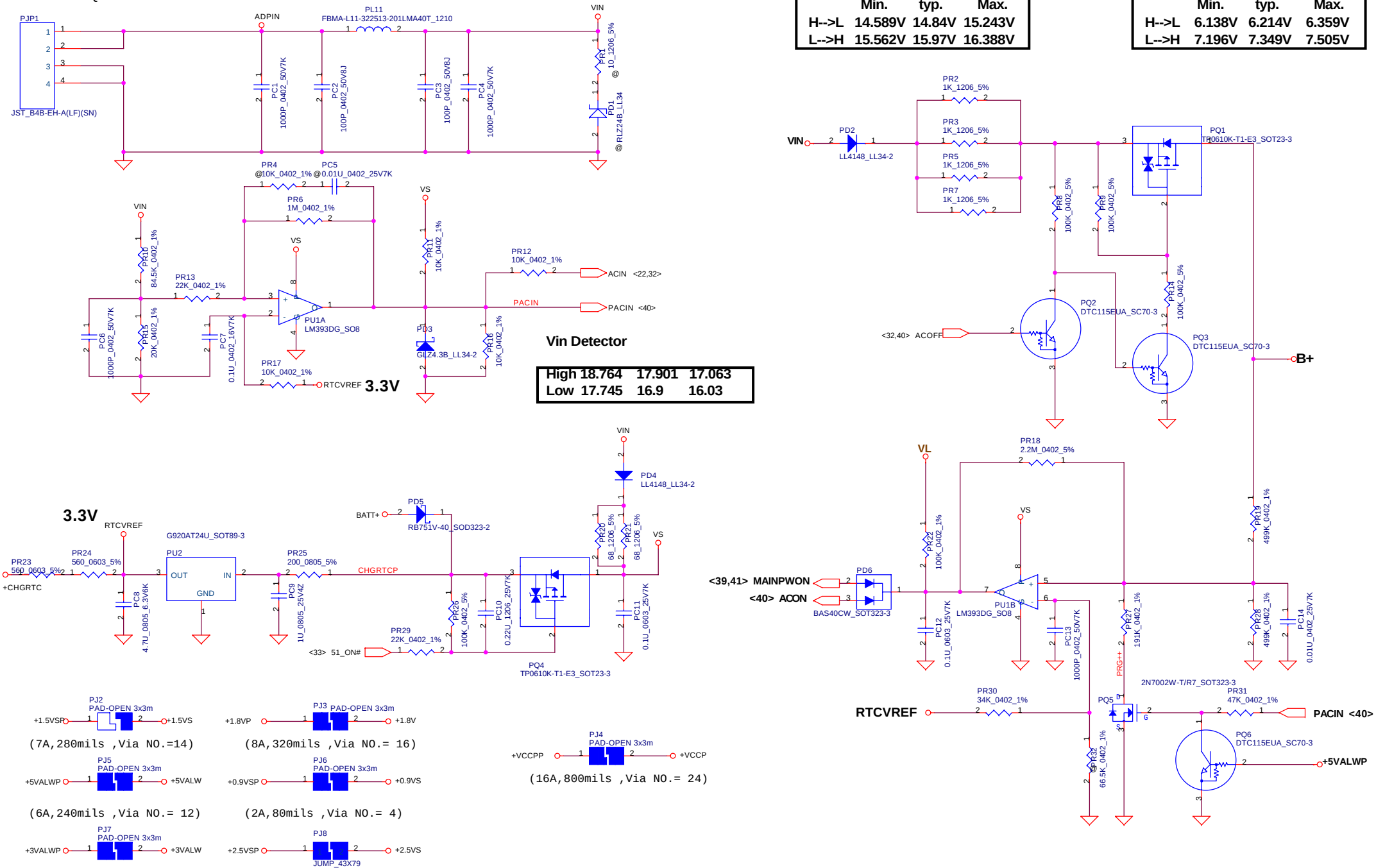
DC030005Q00



Security Classification	Compal Secret Data		
Issued Date	2005/10/17	Deciphered Date	2006/10/17

Compal Electronics, Inc.

Title: DCIN/DECTOR

Size: B | Document Number: IHL00 LA-3691P | Rev: 0.2

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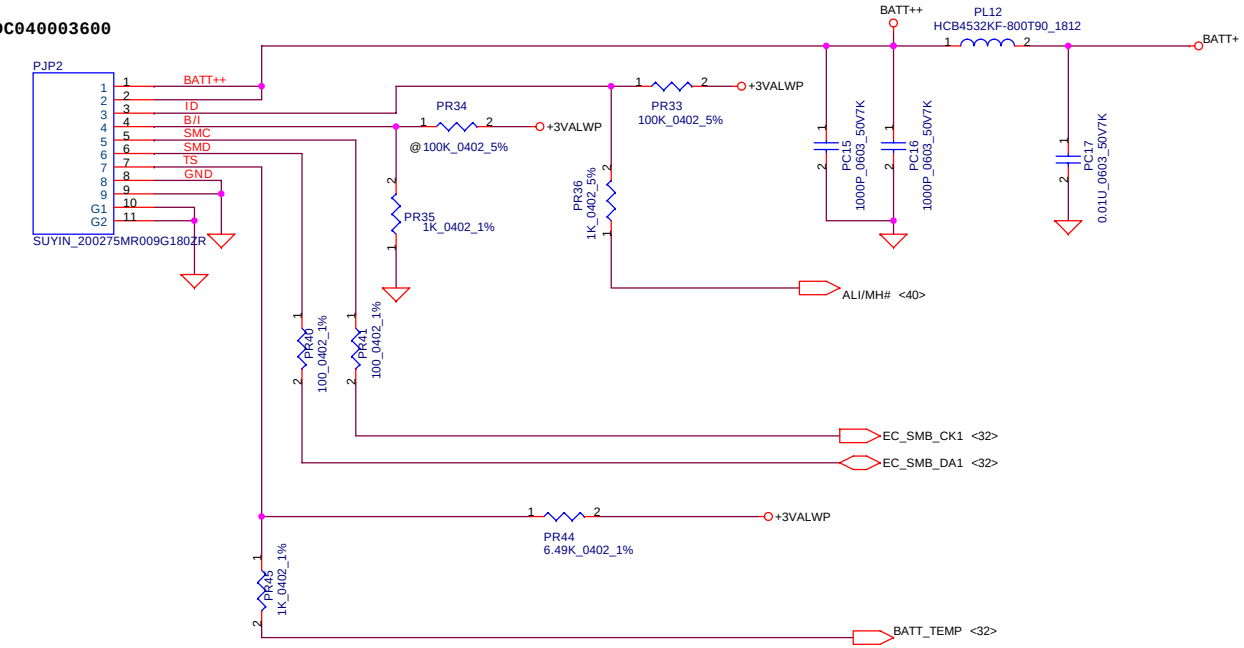
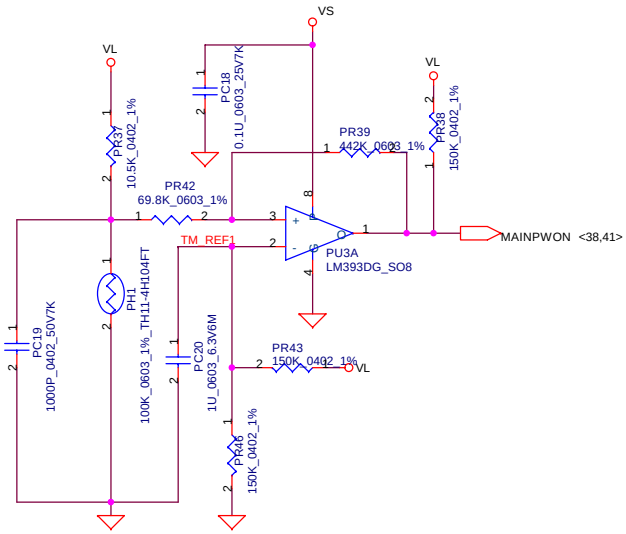
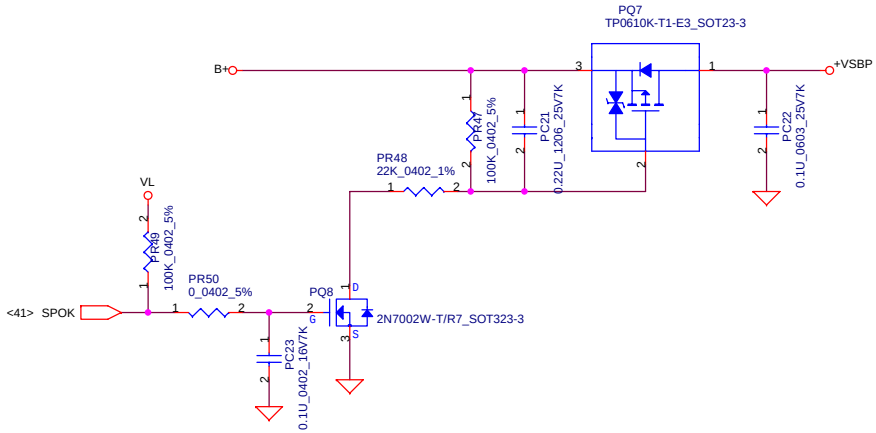
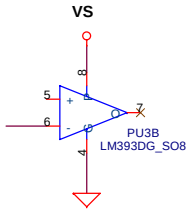
DC040003600



PH1 under CPU botten side :
CPU thermal protection at 87 degree C
Recovery at 70 degree C







Security Classification	Compal Secret Data		
Issued Date	2005/10/17	Deciphered Date	2006/10/17

Compal Electronics, Inc.			
Title	BATTERY CONN. / OTP		
Size B	Document Number IHL00 LA-3691P		Rev 0.2
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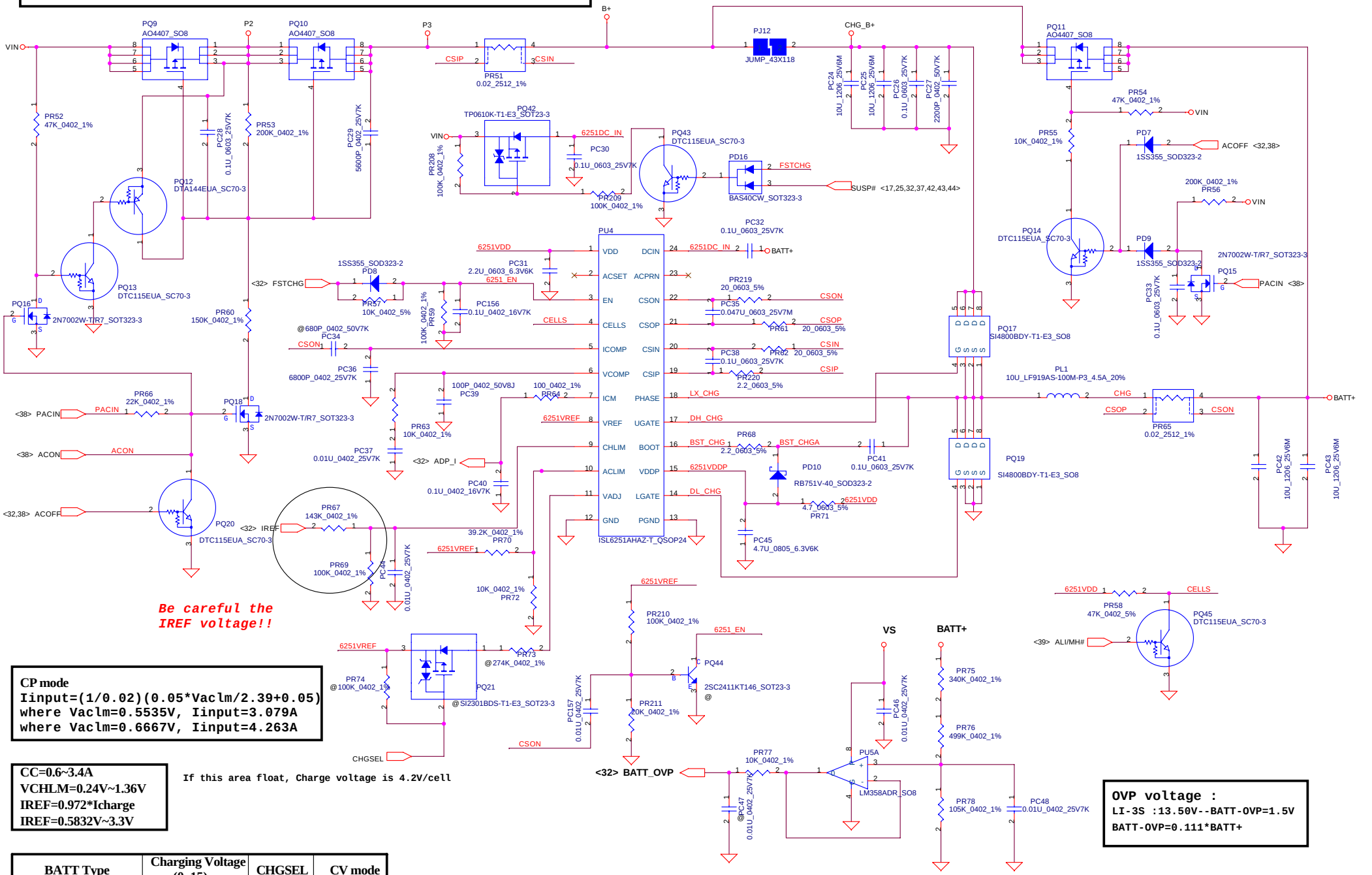
65W, Iadapter=0~3.42A, Current sense=0.02ohm, PR70=39.2K, CP=3.079A
90W, Iadapter=0~4.74A, Current Sense=0.015ohm, PR70=28.7K, CP=4.263A

ADP_I = 19.9*Iadapter*Rsense



Be careful the IREF voltage!!

CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=0.5535V, Iinput=3.079A
where Vaclm=0.6667V, Iinput=4.263A

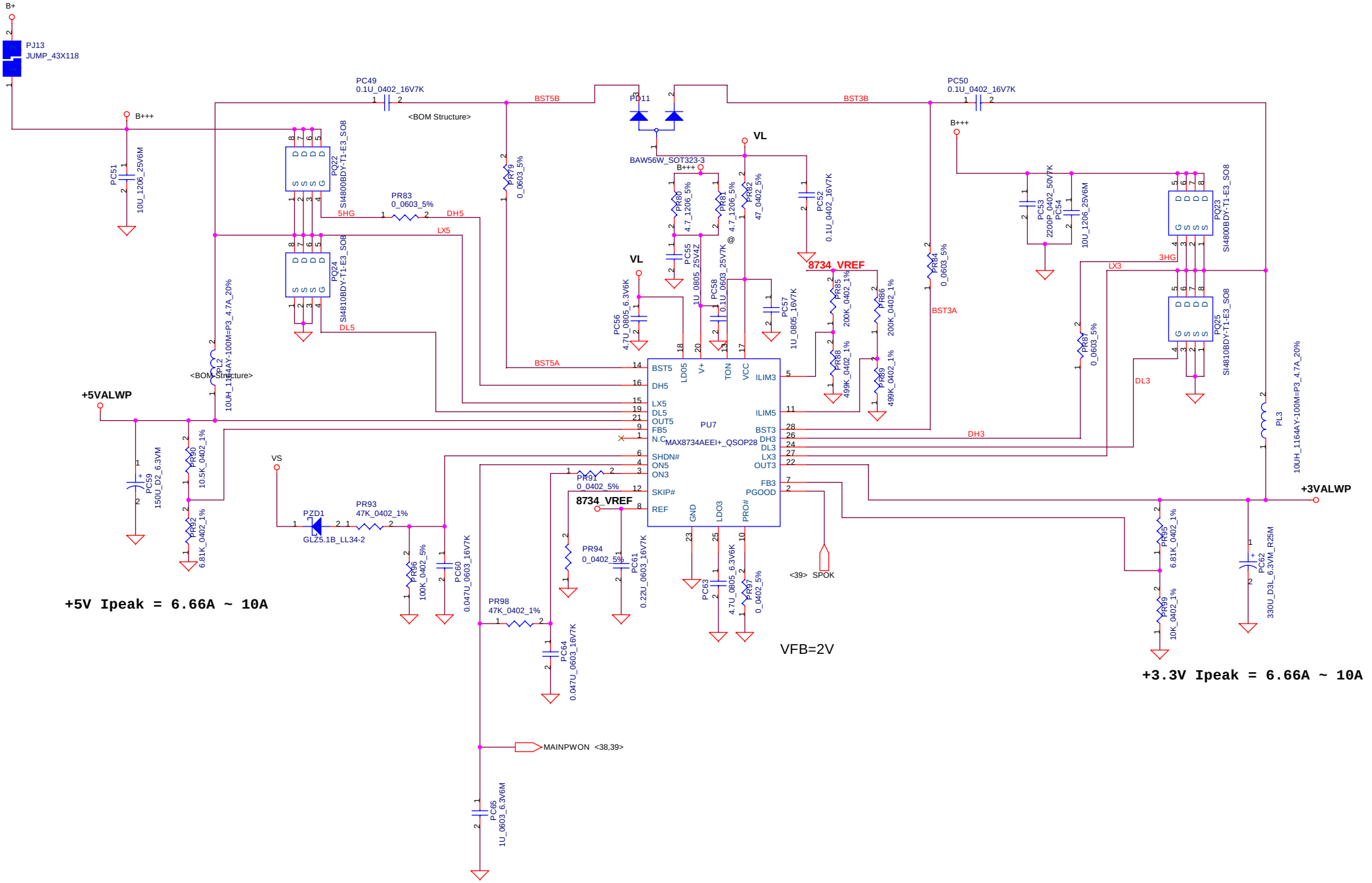
CC=0.6~3.4A
VCHLM=0.24V~1.36V
IREF=0.972*Icharge
IREF=0.5832V~3.3V

If this area float, Charge voltage is 4.2V/cell

OVP voltage :
LI-3S :13.50V--BATT-OVP=1.5V
BATT-OVP=0.111*BATT+

BATT Type	Charging Voltage (0x15)	CHGSEL	CV mode
2800mAH 3S pack	13050mV	LOW	12.90V
Normal 3S LI-ON Cells	12600mV	HIGH	12.60V

Compal Electronics, Inc.
Title: CHARGER
Size: Document Number: IHL00 LA-3691P Rev: 0.2
Date: Thursday, March 08, 2007 Sheet 40 of 45



Security Classification	Compal Secret Data		
Issued Date	2005/10/17	Deciphered Date	2006/10/17

Compal Electronics, Inc.			
Title	+5VALWP/+3VALWP		
Size: Custom	Document Number: IHL00 LA-3691P		Rev: 0.2
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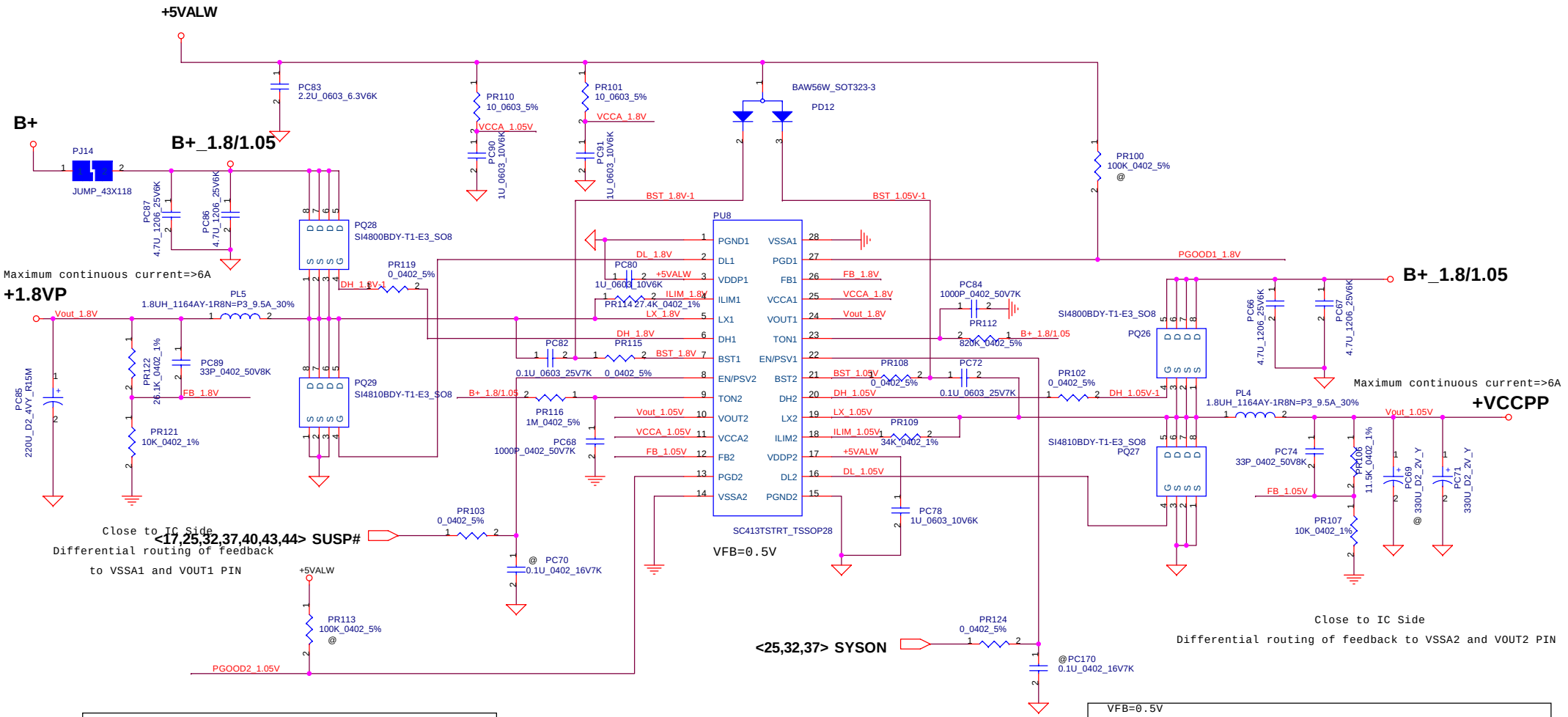

VFB=0.5V
Vo=VFB*(1+PR122/PR127)=1.805V
Ipeak=12.17A, Imax=8.519A
Ton=(3.3E-12*(PR121+37K)*(Vout/VBat))+50ns
=3.3*10e-12*(820K+37K)*(1.8/19)+50ns=0.3179us
FDS6670AS:Rds(on)=>Typ:9 mOhm
Max:11.5 mOhm
Iocp=Ivalley+ Iripple /2
Iripple=(vin-vout)*(Ton/L)=5.467A, 1/2 Iripple=2.734A.
Ivalleymin=10E-6*(PR120/Rds(ON)max*1.5)
=9*10e-6*(27.4K/0.0115*1.5)=14.295A>11.73*1.2=14.076A
Ivalleymax=10E-6*(PR120/Rds(ON)typ*1.2)
=11*10e-6*(27.4K/0.009*1.2)=27.907A.
OCP==>17.029A~30.641A

VFB=0.5V
Vo=VFB*(1+PR129/PR130)=1.5V
Ipeak=5.16A, Imax=3.612A
Ton=(3.3E-12*(PR125+37K)*(Vout/VBat))+50ns
=0.3201us
AO4916 Rds(on)=>Typ:21 mOhm
Max:27 mOhm
Ivalleymin=9*10u*(29.4K/0.027*1.4)=7A
Ivalleymax=11*E-6*(29.4K/0.021*1.1)=12.833A
Iripple=(vin-vout)*(Ton/L)=2.546A, 1/2Iriiple=1.273A
Iocp=Ivalley+ Iripple /2
OCP==>8.273A~14.106A

Security Classification	Compal Secret Data		
Issued Date	2005/10/17	Deciphered Date	2006/10/17

Compal Electronics, Inc.

Title: VCCPP/1.8VP

Size: Custom | Document Number: IHL00 LA-3691P | Rev: 0.2

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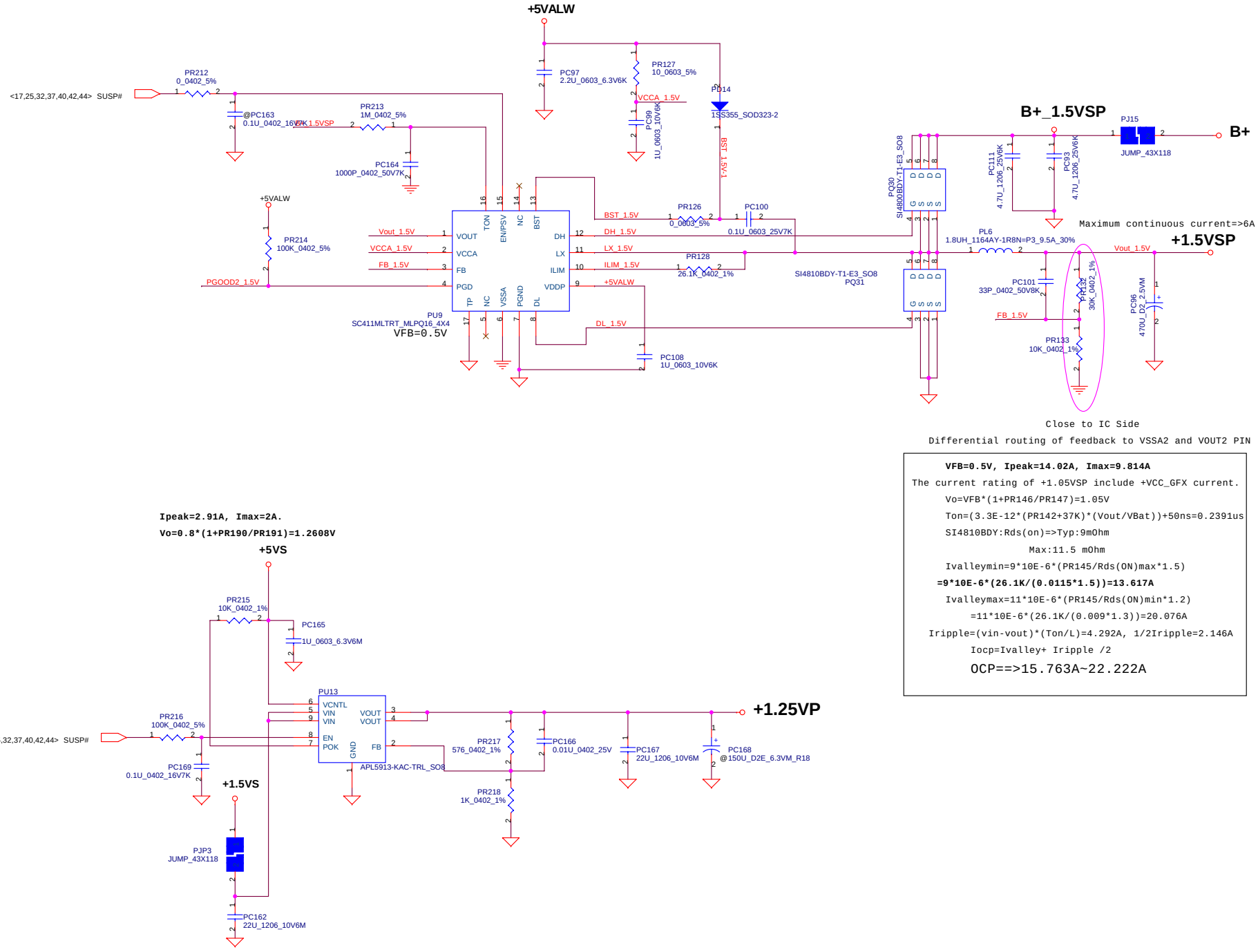


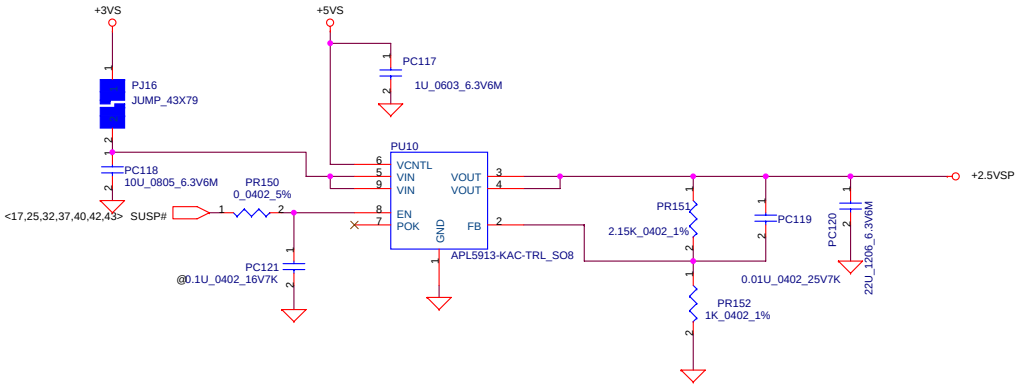
Security Classification	Compal Secret Data		
Issued Date	2005/10/17	Deciphered Date	2006/10/17

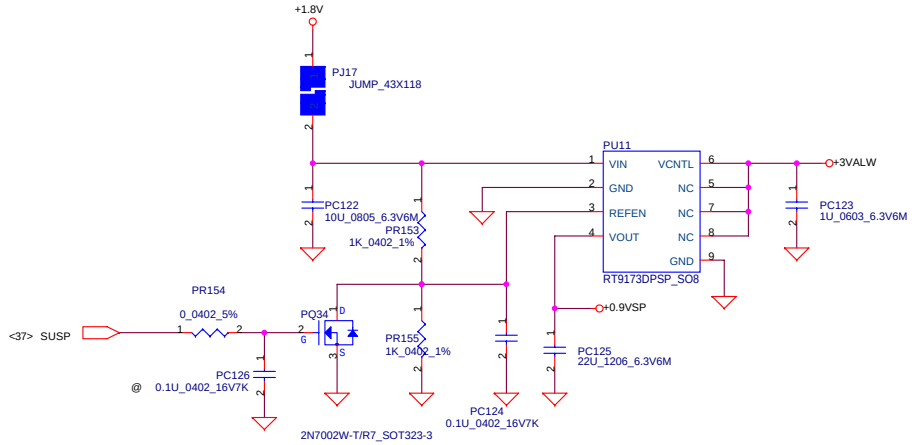
Compal Electronics, Inc.

Title: 1.5VSP/1.25VP

Size: Custom | Document Number: IHL00 LA-3691P | Rev: 0.2

Date: Thursday, March 08, 2007 | Sheet 43 of 45





Security Classification	Compal Secret Data		
Issued Date	2005/10/17	Deciphered Date	2006/10/17

Compal Electronics, Inc.

Title: +2.5VSP/0.9VSP

Size	Document Number	Rev
Custom	IHL00 LA-3691P	0.2

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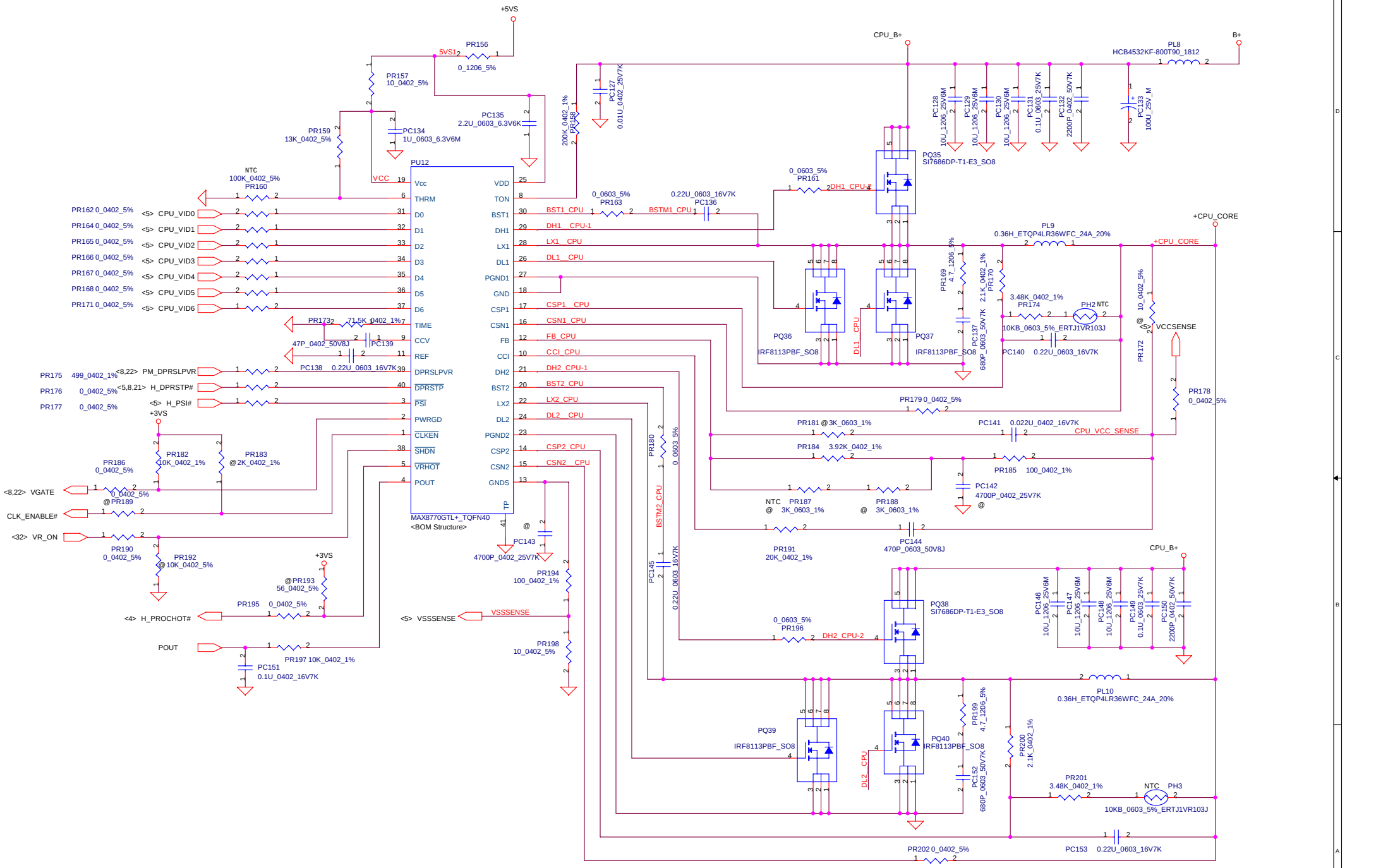

Security Classification	Compal Secret Data		
Issued Date	2005/10/17	Deciphered Date	2006/10/17

Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
Custom	IHL00 LA-3691P	0.2

Date: Thursday, March 08, 2007 | Sheet 45 of 45

Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG#	Modify List	B.Ver#	Phase
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						
15						
16						
17						

Compal Electronics, Inc.

Title: POWER PIR

Size | Document Number | Rev

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Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG#	Modify List	B.Ver#	Phase
1	XDP_BPM#0~4 test point short as EMI request	B	4	Modify Layout		
2	ADD J6 for +VCC_AXG UMA VGA power shape	B	11	Modify Layout		
3	Fixed Speaker no function	A2	37	Change Q91 form SI2301BDS to MMBT3906, Del R895		
4	Fixed SWDJ function can't work	A2	36	Add R904		
5	Fixed Audio Codec can't work	A2	29	Add R905,Q96		
6	Fixed USB Port4 can't work	A2	27	Swap USB_N4 & USB_P4		
7	Fixed EMI issue	A2	32 37	Add R908,C878,C879		
8	Fixed SWDJ mode EC_MUTE# ISSUE	B	30	Add D39,Q99,R914		
9	Fixed CMOS noise	B	36	Add R912,C880		
10	Fixed EMI	B	25	Add C881,C882		
11	Add chipset id	B	33	Add R915,R916		
12	Fix SWDJ Subwoofer issue	B	31	Add R917		
13	Fix DFX issue	C	22,33	Change Y3,X1,Y2 footprint		
14	FOR E-STAR V4 wake on lan	C	22,33	Add R918,R919		
15	For ESD issue	C	36	Add C883~C887 D40,D41		
16	For AUDIO team design	C	30	Add R920 R921		
17	Change LAN led function	C	25	Swap JP73 PIN12 & PIN14		

Compal Electronics, Inc.

Title: POWER PIR

Size | Document Number | Rev

Date: Thursday, March 08, 2007 | Sheet 48 of 48