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Intel Skylake-U Platform

Skylake-U CPU (TDP 15W) SoC

Project Information

Phase: EVT

PCB AND SILKSCREEN COLOR		
Program Phase	**Color of PCB**	**Silkscreen**
EVT	**RED**	**YELLOW**
DVT	**LIGHT BLUE**	**YELLOW**
PVT/MVB / PRODUCTION	**GREEN**	**WHITE**

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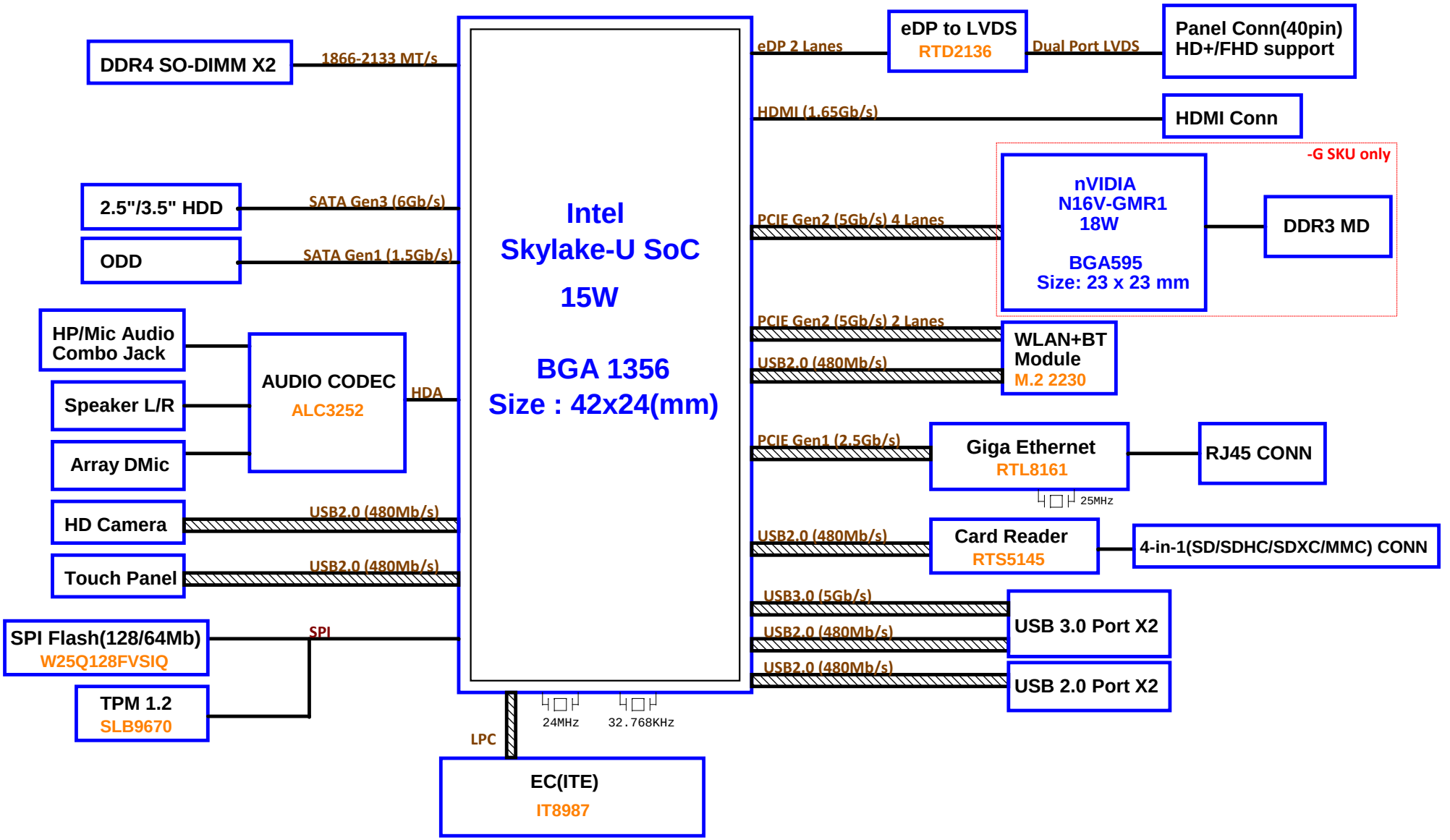
Intel Skylake-U Platform Block Diagram (Hawaii-G/-U)



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[5,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[5,7,17,46,48] +VCCIO
[5,6,7,10,43,46] +VCCSTPLL

HDMI

U21A SKL_ULT ?

[22] IN_D2# E55
[22] IN_D2 F55
[22] IN_D1# E58
[22] IN_D1 F58
[22] IN_D0# F53
[22] IN_D0 G53
[22] IN_CLK# F56
[22] IN_CLK G56

DDI1_TXN[0] DDI1_TXP[0] DDI1_TXN[1] DDI1_TXP[1] DDI1_TXN[2] DDI1_TXP[2] DDI1_TXN[3] DDI1_TXP[3]

C50 DDI2_TXN[0]
D50 DDI2_TXP[0]
C52 DDI2_TXN[1]
D52 DDI2_TXP[1]
A50 DDI2_TXN[2]
B50 DDI2_TXP[2]
D51 DDI2_TXN[3]
C51 DDI2_TXP[3]

DDI

EDP

EDP_TXN[0] C47 INT_EDP_TXN0 → INT_EDP_TXN0 [20]
EDP_TXP[0] C46 INT_EDP_TXP0 → INT_EDP_TXP0 [20]
EDP_TXN[1] D46 INT_EDP_TXN1 → INT_EDP_TXN1 [20]
EDP_TXP[1] C45 INT_EDP_TXP1 → INT_EDP_TXP1 [20]
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

EDP_AUXN E45 INT_EDP_AUXN → INT_EDP_AUXN [20]
EDP_AUXP F45 INT_EDP_AUXP → INT_EDP_AUXP [20]

EDP_DISP_UTIL B52

DISPLAY SIDEBANDS

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN G48
DDI2_AUXP F48
DDI3_AUXN G46
DDI3_AUXP F46

[22] SDVO_CLK L13
[22] SDVO_DATA L12

GPP_E18/DDPB_CTRLCLK
GPP_E19/DDPB_CTRLDATA

NZ
+3V R208 2.2K_4 N8

GPP_E20/DDPC_CTRLCLK
GPP_E21/DDPC_CTRLDATA

N11
TP22 N12

GPP_E22/DDPD_CTRLCLK
GPP_E23/DDPD_CTRLDATA

+VCCIO R116 24.9/F_4 EDP_RCOMP E52

EDP_RCOMP

GPP_E13/DDPB_HPD0 L9 PCH_HDMI_HPD → PCH_HDMI_HPD [22]
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 N9
GPP_E16/DDPE_HPD3 C10 EDP_HPD → EDP_HPD [20]
GPP_E17/EDP_HPD

EDP_BKLTEN R12 PCH_LVDS_BLON → PCH_EDP_BLON [21]
EDP_BKLTCTL R11 PCH_DPST_PWM → PCH_DPST_PWM [20]
EDP_VDDEN U13 PCH_LCDVCC_EN → PCH_LCDVCC_EN [21]

SKL_ULT
REV = 1

1 OF 20

?

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!

+3V
R505 *10K_4
EDP_HPD
R504 100K_4

U21D SKL_ULT ?

TP45 CATERR# D63
[29] EC_PECI A54
[29,43,47] H_PROCHOT# R408 499/F_4 PROCHOT# C65
PM_THRMTRIP# C63
A65

CATERR#
PECI
PROCHOT#
THERMTRIP#
SKTOCC#

CPU MISC

[17] XDP_BPM0 C55
[17] XDP_BPM1 D55
B54
C56

BPM#[0]
BPM#[1]
BPM#[2]
BPM#[3]

A6
A7
BA5
AY5

GPP_E3/CPU_GP0
GPP_E7/CPU_GP1
GPP_B3/CPU_GP2
GPP_B4/CPU_GP3

[26] RF_OFF

R170 49.9/F_4 PROC_POPIRCOMP AT16
R164 49.9/F_4 PCH_OPI_RCOMP AU16
R79 49.9/F_4 EDRAM_OPIO_RCOMP H66
R80 49.9/F_4 EOPIO_RCOMP H65

PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

JTAG

PROC_TCK B61 XDP_TCK0 → XDP_TCK0 [17]
PROC_TDI D60 XDP_TDI_CPU → XDP_TDI_CPU [17]
PROC_TDO A61 XDP_TDO_CPU → XDP_TDO_CPU [17]
PROC_TMS C60 XDP_TMS_CPU → XDP_TMS_CPU [17]
PROC_TRST# B59 XDP_TRST#_CPU → XDP_TRST#_CPU [17]

PCH_JTAG_TCK B56 JTAG_TCK_PCH → JTAG_TCK_PCH [17]
PCH_JTAG_TDI D59 JTAG_TDI_PCH → JTAG_TDI_PCH [17]
PCH_JTAG_TDO A56 JTAG_TDO_PCH → JTAG_TDO_PCH [17]
PCH_JTAG_TMS C59 JTAG_TMS_PCH → JTAG_TMS_PCH [17]
PCH_TRST# C61 XDP_TRST#_CPU
JTAGX A59 JTAGX_PCH → JTAGX_PCH [17]

SKL_ULT
REV = 1

4 OF 20

+VCCSTPLL
PM_THRMTRIP# R422 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL . 470 OHM IS FOR I/P

PLACE NEAR CPU

+VCCIO
XDP_TMS_CPU R435 *51_4
XDP_TDI_CPU R436 *51_4
XDP_TDO_CPU R427 *51_4

+VCCSTPLL
H_PROCHOT# R406 1K_4
XDP_TCK0 R430 51_4
XDP_TRST#_CPU R439 51_4

EC-PV-01

+VCCIO R428 *0/S_4

R431 *51_4 JTAGX_PCH
R440 51_4 JTAG_TMS_PCH
R444 51_4 JTAG_TDI_PCH
R448 51_4 JTAG_TDO_PCH
R443 51_4 JTAG_TCK_PCH

Close to Chipset

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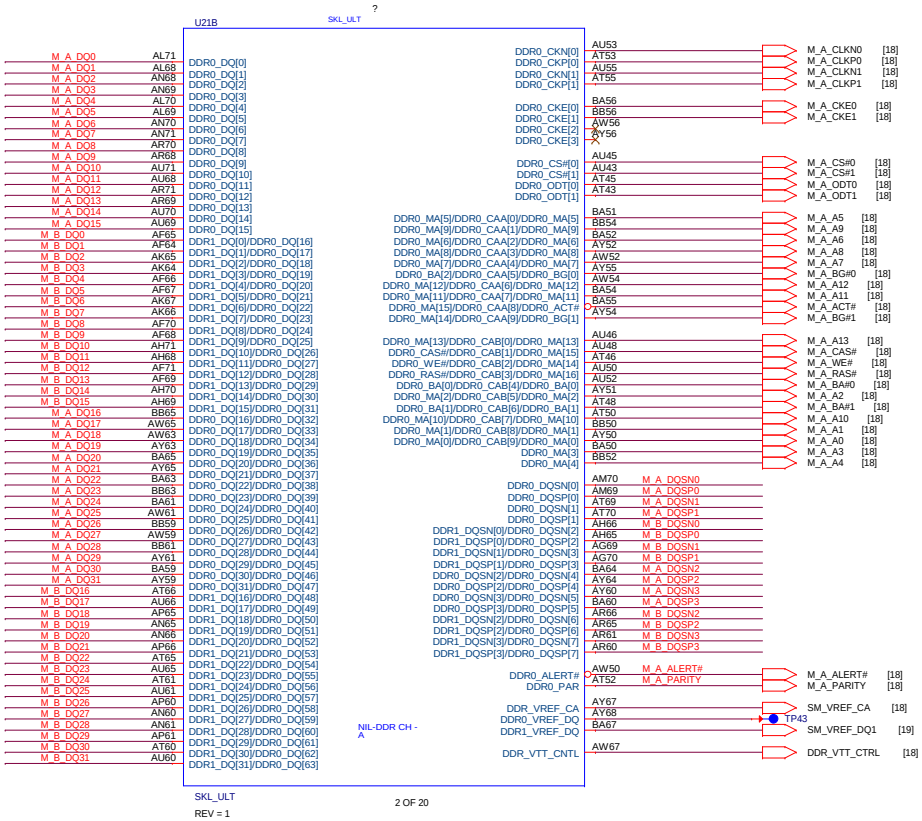
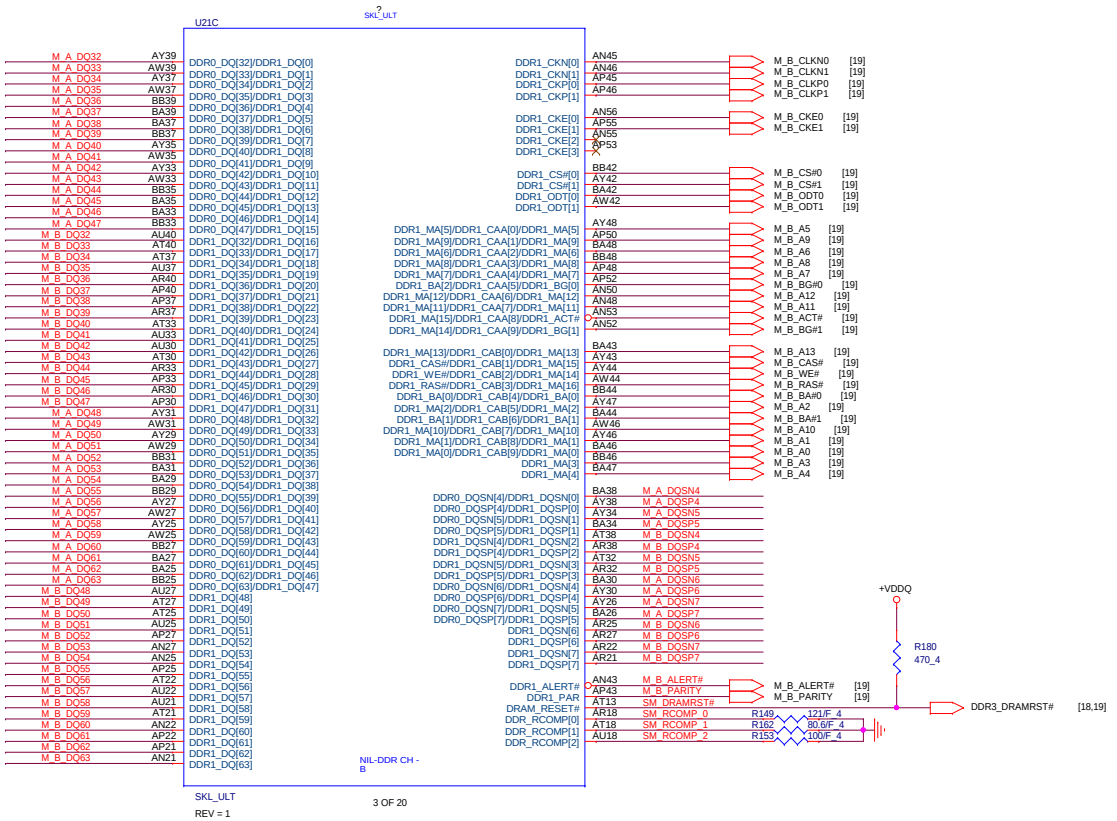
SkyLake ULT Processor (DDR4 IL)





[18] M_A_DQSN[7:0]
[18] M_A_DQSP[7:0]
[18] M_A_DQ[63:0]

[19] M_B_DQSN[7:0]
[19] M_B_DQSP[7:0]
[19] M_B_DQ[63:0]

[7,18,19,32,40] +VDDQ

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[11,12,13,15,16,17,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52] +3V_S5
[3,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[21,23,27,28,32,39,40,41,43,45,46,47,48,52] +5V_S5
[3,7,17,46,48] +VCCIO
[3,6,7,10,43,46] +VCCSTPLL
[14,16] +3V_RTC_2

U21K SKL_ULT ?
SYSTEM POWER MANAGEMENT

[24,26,29,31,33] PLTRST#
[17] SYS_RESET#
[17,29] RSMRST#
RSMRST# R485 *0/S_4 RSMRST#_R
R403 *10K_4 PROCPWRGD
H_VCCST_PWRGD
EC-PV-01
[17,29] HWPG R484 *0/S_4 DPWROK
[29] EC_SUSPWRACK R580 *0_4 SUSWARN#
[29] EC_SUSACK# R192 *0_4 SUSACK#
[24,26] PCIE_WAKE#
TP23 PCIE_LAN_WAKE#
TP58 LAN_DIS#
TP18

GPP_B13/PLTRST# AN10
SYS_RESET# B5
RSMRST# AY17
PROCPWRGD A68
VCCST_PWRGD B65
SYS_PWROK B6
PCH_PWROK BA20
DSW_PWROK BB20
GPP_A13/SUSWARN#/SUSPWRDNACK AR13
GPP_A15/SUSACK# AP11
WAKE# BB15
GPD2/LAN_WAKE# AM15
GPD11/LANPHYPC AW17
GPD7/RSVD AT15

GPP_B12/SLP_S0# AT11 PM_SLP_S0#
GPD4/SLP_S3# AP15
GPD5/SLP_S4# BA16
GPD10/SLP_S5# AY16
SLP_SUS# AN15
SLP_LAN# AW15 SLP_LAN#
GPD9/SLP_WLAN# BB17 SLP_WLAN#
GPD6/SLP_A# AN16
GPD3/PWRBTN# BA15 DNBSWON#
GPD1/ACPRESENT AY15 AC_PRESENT_EC
GPD0/BATLOW# AU13 PM_BATLOW_N_EC
GPP_A11/PME# AU11
INTRUDER# AP16 INTRUDER#_R R177 1M_4 +3V_RTC_2
GPP_B11/EXT_PWR_GATE# AM10 EXT_PWR_GATE#
GPP_B2/VRALERT# AM11

PM_SLP_S0# [17,29]
SUSB# [17,29]
SUSC# [17,29]
SLP_S5# [17,29]
PM_SLP_SUS# [29]
TP62
TP60
SLP_A# [17]
TP31
DNBSWON# [17,29]
AC_PRESENT_EC [29]
TP27

SKL_ULT
REV = 1
11 OF 20
?

PCH Pull-high/low(CLG)

+3V_S5
SUSWARN# R189 *10K_4
SUSACK# R191 *10K_4
PM_BATLOW_N_EC R181 10K_4

+3V_S5
PCIE_WAKE# R493 1K_4
AC_PRESENT_EC R490 10K_4
PCIE_LAN_WAKE# R187 10K_4
EXT_PWR_GATE# R186 *20K/F_4

+3V
SYS_RESET# R500 10K_4
PLTRST# R222 *10K/F_4
R223 100K/F_4
RSMRST# R487 10K_4
DPWROK R481 *100K/F_4

RSMRST#
SYS_RESET#
PLTRST#
EC5 *220P/50V_4
C554 *220P/50V_4
C549 *220P/50V_4

[29] EC_DPWROK
RSMRST# EC_DPWROK R483 *0_4 R538 *0/S_4 DPWROK
EC-PV-01

Close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"

+VCCIO +VCCSTPLL
R401 1K_4
R405 *1K_4
HWPG D141 2 RB500V-40 H_VCCST_PWRGD_R R404 60.4_4 H_VCCST_PWRGD
C512 *10P/50V_4

+VCCIO +5V_S5 +3V_S5
R478 15K_4
R479 100K_4
R476 10K_4
HWPG
+1.0V_PWRGD_G2 2 Q31 2N7002K
R475 100K_4
+1.0V_PWRGD_G1 2 Q32 METR3904-G
C530 0.1U/16V_4
R480 100K_4

System PWR_OK(CLG)

SYS_PWROK
EC-PV-01
R496 *0/S_4
EC_PWROK
EC_PWROK [29]
C552 *0.1U/16V_4
R497 100K/F_4

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[32,43,44] +VCC_CORE
[7] +VCCSTG
[3,5,7,10,43,46] +VCCSTPLL

U21L SKL_ULT ?
CPU POWER 1 OF 4
33A
SKL_ULT
REV = 1
12 OF 20

+VCC_CORE

A30 VCC_A30
A34 VCC_A34
A39 VCC_A39
A44 VCC_A44
AK33 VCC_AK33
AK35 VCC_AK35
AK37 VCC_AK37
AK38 VCC_AK38
AK40 VCC_AK40
AL33 VCC_AL33
AL37 VCC_AL37
AL40 VCC_AL40
AM32 VCC_AM32
AM33 VCC_AM33
AM35 VCC_AM35
AM37 VCC_AM37
AM38 VCC_AM38
G30 VCC_G30

K32 RSVD_K32
AK32 RSVD_AK32

AB62 VCCOPC_AB62
P62 VCCOPC_P62
V62 VCCOPC_V62

H63 VCC_OPC_1P8_H63
G61 VCC_OPC_1P8_G61

AC63 VCCOPC_SENSE
AE63 VSSOPC_SENSE

AE62 VCCEOPIO
AG62 VCCEOPIO

AL63 VCCEOPIO_SENSE
AJ62 VSSEOPIO_SENSE

+VCC_CORE

VCC_G32 G32
VCC_G33 G33
VCC_G35 G35
VCC_G37 G37
VCC_G38 G38
VCC_G40 G40
VCC_G42 G42
VCC_J30 J30
VCC_J33 J33
VCC_J37 J37
VCC_J40 J40
VCC_K33 K33
VCC_K35 K35
VCC_K37 K37
VCC_K38 K38
VCC_K40 K40
VCC_K42 K42
VCC_K43 K43

VCC_SENSE E32
VSS_SENSE E33

VIDALERT# B63
VIDSCK A63
VIDSOUT D64

VCCSTG_G20 G20

C270 10U/6.3V_4 C265 22U/6.3V_6 C229 22U/6.3V_6 C267 22U/6.3V_6 C225 22U/6.3V_6 C226 22U/6.3V_6 C266 22U/6.3V_6 C269 22U/6.3V_6
C233 10U/6.3V_4 C246 10U/6.3V_4 C268 10U/6.3V_4 C236 10U/6.3V_4 C256 10U/6.3V_4 C241 10U/6.3V_4 C258 10U/6.3V_4
C227 22U/6.3V_6 C264 22U/6.3V_6 C245 22U/6.3V_6 C228 22U/6.3V_6 C223 22U/6.3V_6 C230 22U/6.3V_6
Under CPU

C276 1U/6.3V_4 C249 1U/6.3V_4 C232 1U/6.3V_4 C247 1U/6.3V_4 C274 1U/6.3V_4 C261 1U/6.3V_4 C248 1U/6.3V_4
C240 1U/6.3V_4 C252 1U/6.3V_4 C251 1U/6.3V_4 C250 1U/6.3V_4 C271 1U/6.3V_4 C272 1U/6.3V_4 C259 1U/6.3V_4 C221 1U/6.3V_4
Under CPU

R129 100/F_4 +VCC_CORE
R132 100/F_4 VCC_SENSE [43]
VSS_SENSE [43]

100- ±1% pull-up to VCC near processor.

H_CPU_SVIDALRT#
VR_SVID_CLK_R
H_CPU_SVIDDAT
+VCCSTG

Close CPU
+VCC_CORE
C501 47U/6.3V_8 C237 47U/6.3V_8 C211 47U/6.3V_8 C75 47U/6.3V_8 C502 47U/6.3V_8 C239 47U/6.3V_8 C506 47U/6.3V_8 C217 47U/6.3V_8
+VCC_CORE
C243 10U/6.3V_4 C523 10U/6.3V_4 C521 10U/6.3V_4 C244 10U/6.3V_4 C519 10U/6.3V_4 C522 10U/6.3V_4 C524 10U/6.3V_4 C520 10U/6.3V_4

+VCC_CORE
C510 *1U/6.3V_4
C505 *22U/6.3V_6
C508 *1U/6.3V_4
C503 *22U/6.3V_6
RF RESERVE

Layout note: need routing together and ALERT need between CLK and DATA.

CLOSE TO CPU
PLACE THE PU RESISTORS
+VCCSTPLL
R418 56.2/F_4
SVID ALERT
H_CPU_SVIDALRT# R417 220/F_4 VR_SVID_ALERT# [43]
C513 *0.1U/16V_4

PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE
+VCCSTPLL
R424 *54.9/F_4
SVID CLK
VR_SVID_CLK_R EC-PV-01 R423 *0/S_4 VR_SVID_CLK [43]

CLOSE TO CPU
PLACE THE PU RESISTORS
+VCCSTPLL
R412 100/F_4
SVID DATA
H_CPU_SVIDDAT EC-PV-01 R413 *0/S_4 VR_SVID_DATA [43]

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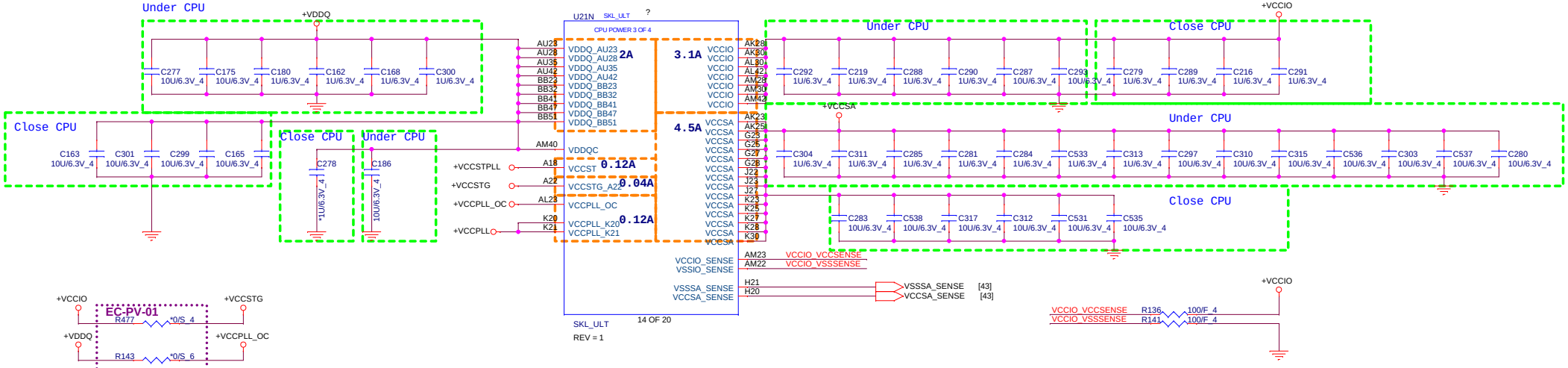
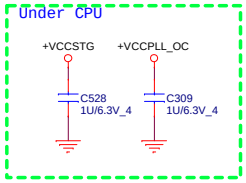
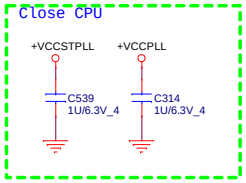
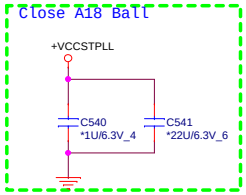
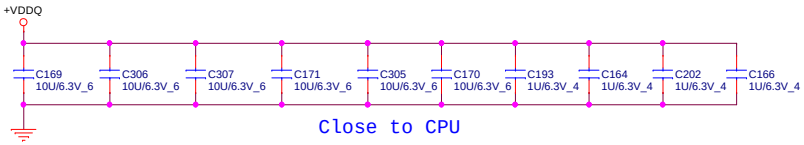
[3,5,17,46,48] +VCCIO
[43,45] +VCCSA
[4,18,19,32,40] +VDDQ
[3,5,6,10,43,46] +VCCSTPLL
[6] +VCCSTG











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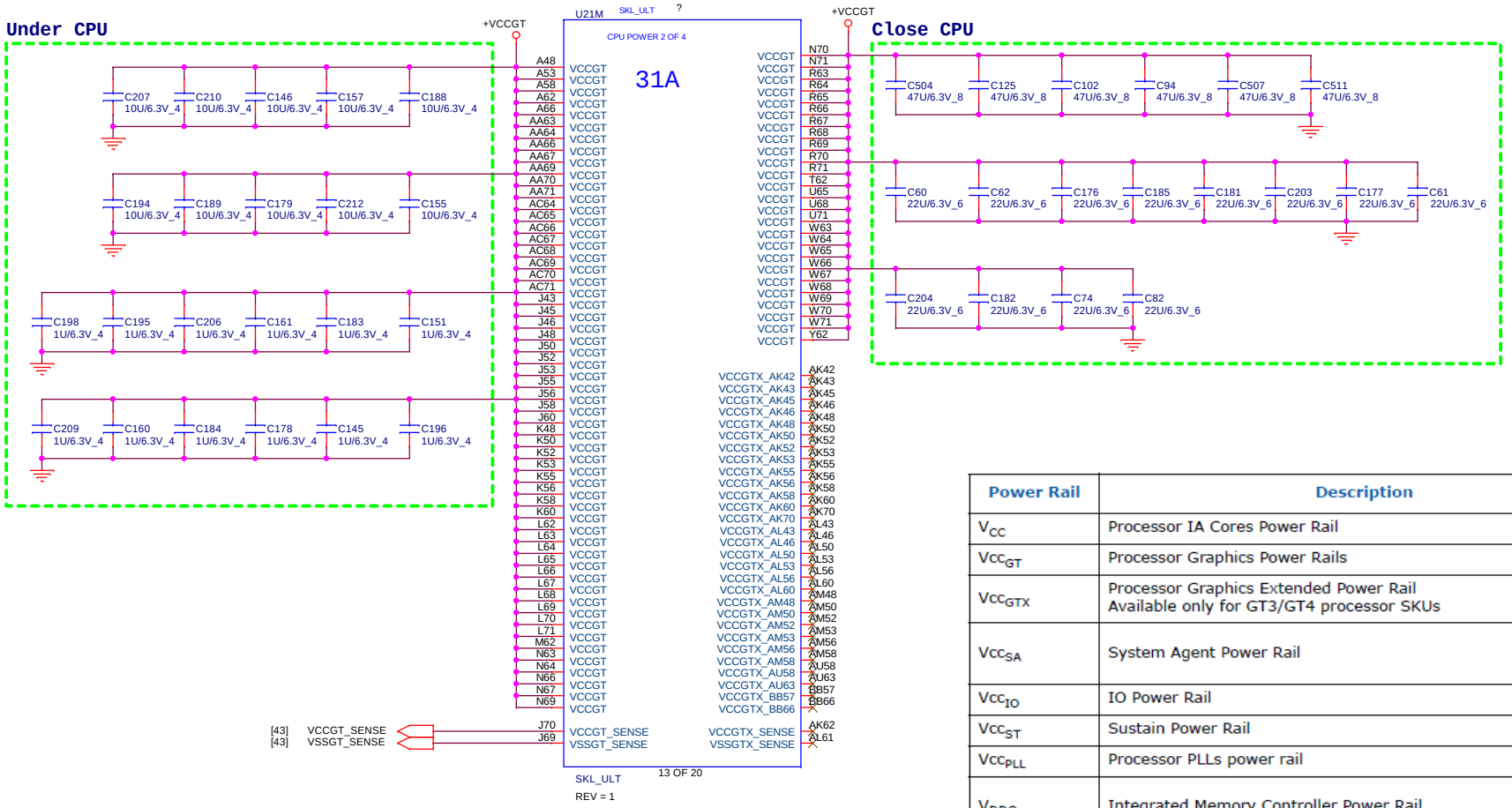
+VCCGT [43,44]



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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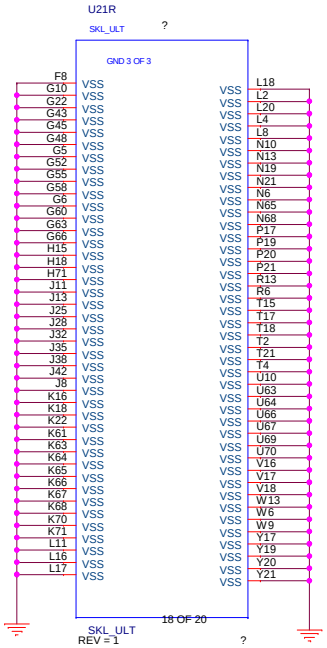

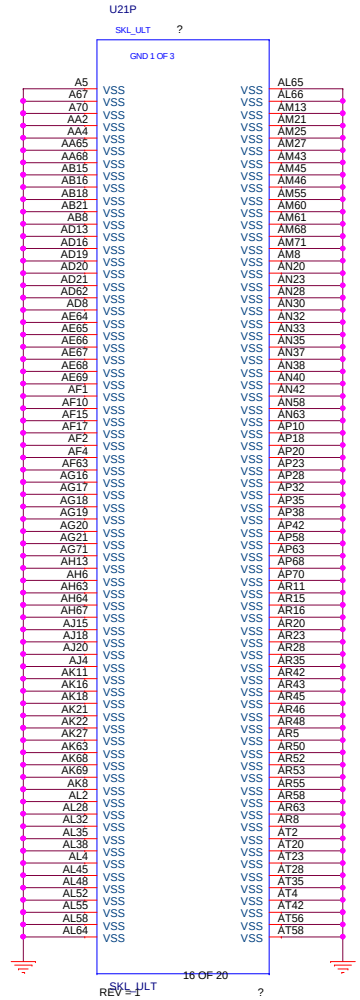

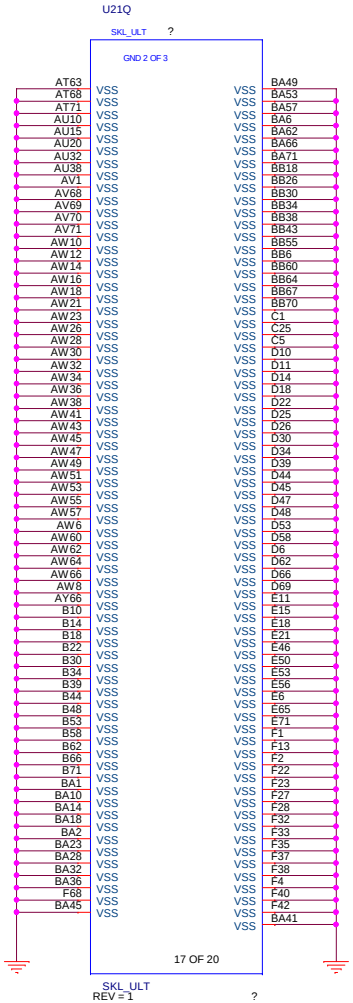

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Custom	SKL CPU GND	1A

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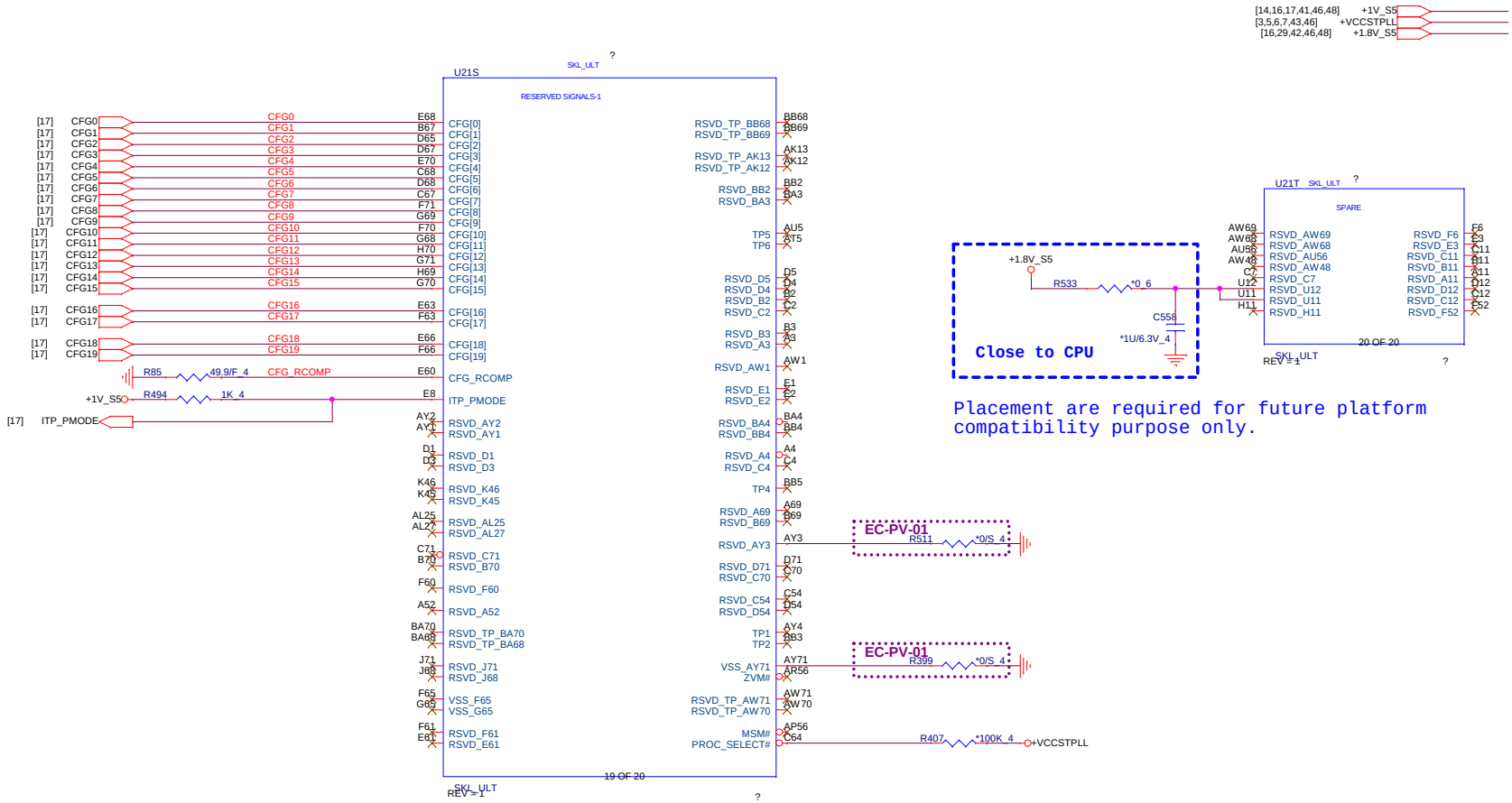

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R400 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R402 1K_4

HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU RSVD	1A

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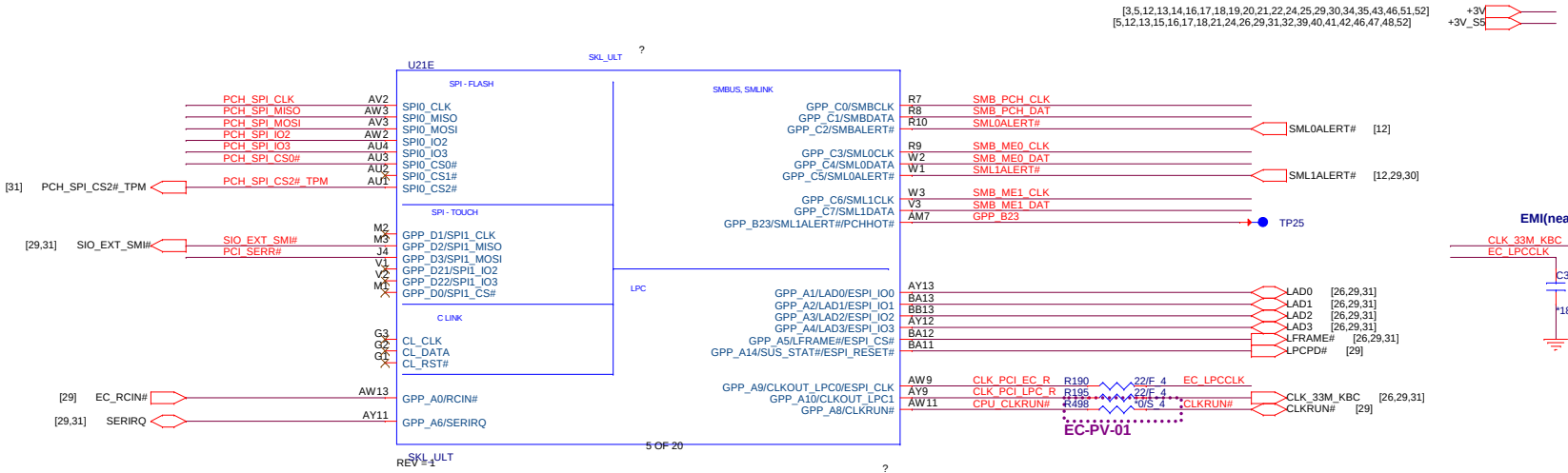
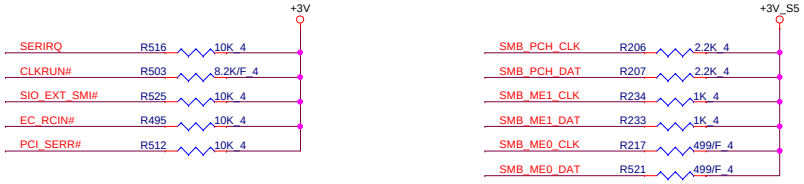
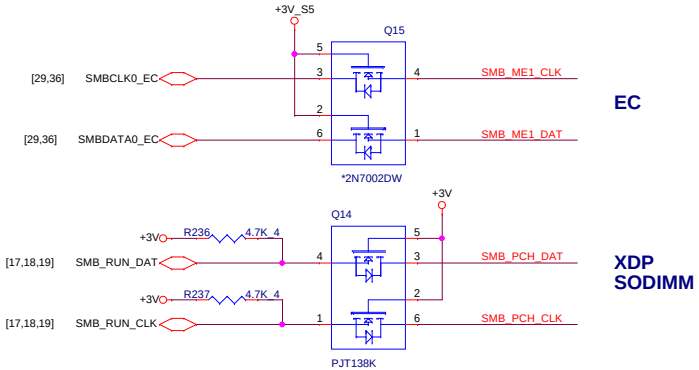


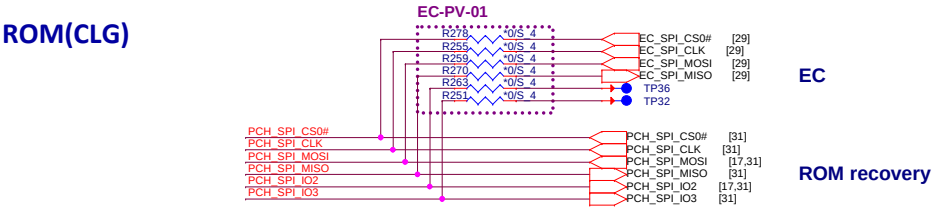
GPIO Pull UP

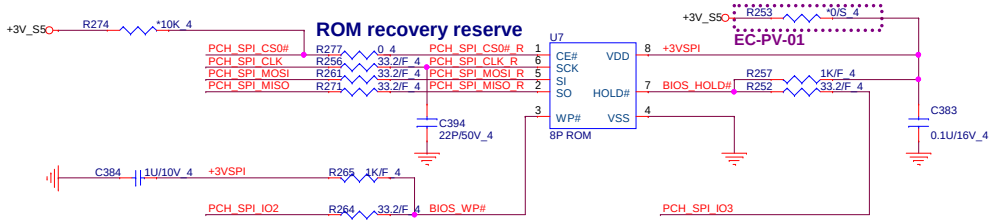


SMBus/Pull-up(CLG)



PCH SPI ROM(CLG)





Vender	Size	P/N
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GD	8MB	AKE2EZN0Q00 (GD25B64CSIGR)
Socket		DFHS08FS023

HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU SPI/LPC/SMB	1A

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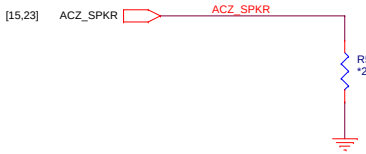
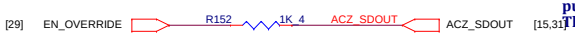
[3,5,11,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V

Functional Strap Definitions

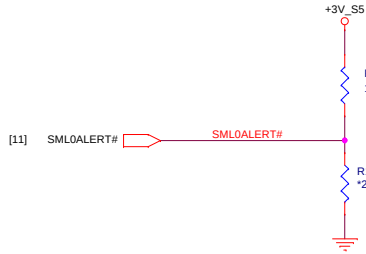
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



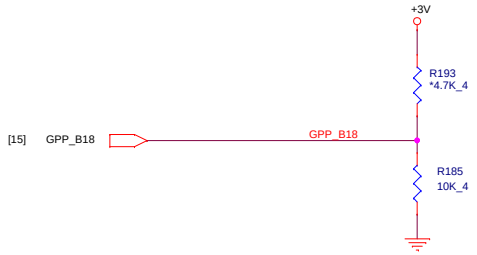
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
This function is useful when running ITP/XDP.



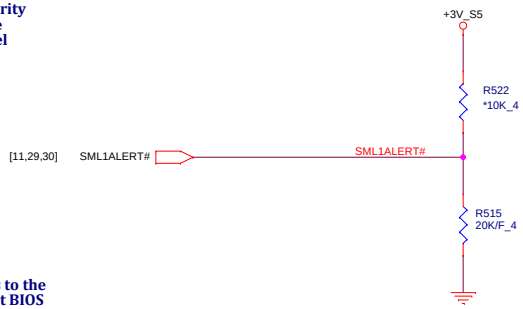
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO Timer system reboot feature).
This function is useful when running ITP/XDP.

No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

HP Restricted Secret

Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU Strap	1A

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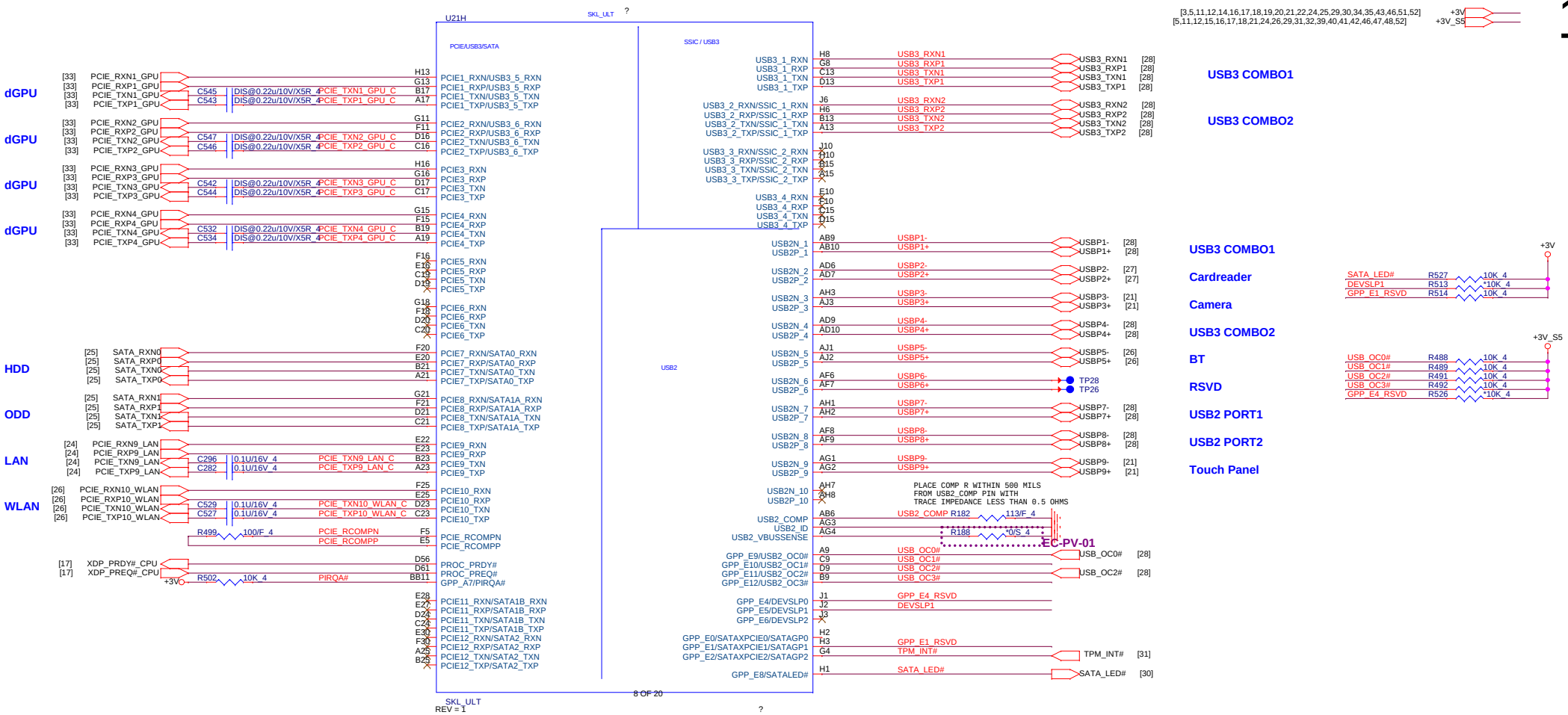

PCI-E Port Mapping Table

PCI-E	Function	CLK REQ	Function
PORT-1	dGPU	PORT-0	dGPU
PORT-2	dGPU	PORT-1	
PORT-3	dGPU	PORT-2	WLAN
PORT-4	dGPU	PORT-3	LAN
PORT-5		PORT-4	
PORT-6		PORT-5	
PORT-7	HDD		
PORT-8	ODD		
PORT-9	LAN		
PORT-10	WLAN		
PORT-11			
PORT-12			

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3 COMBO1
PORT-2	USB3 COMBO2
PORT-3	NC
PORT-4	NC

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	USB3 COMBO1
PORT-2	Cardreader
PORT-3	Camera
PORT-4	USB3 COMBO2
PORT-5	BT
PORT-6	NC
PORT-7	USB2 PORT1
PORT-8	USB2 PORT2
PORT-9	Touch Panel
PORT-10	NC

Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU PCIE/USB/SATA	1A

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[5,16] +3V_RTC_2
[3,5,11,12,13,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[10,16,17,41,46,48] +1V_S5

U21J SKL_ULT ?

CLOCK SIGNALS

[33] CLK_GFX_N → CLK_GFX_N → D42 CLKOUT_PCIE_N0
[33] CLK_GFX_P → CLK_GFX_P → C42 CLKOUT_PCIE_P0
[33] PCIE_CLKREQ_VGA# → PCIE_CLKREQ_VGA# → AR10 GPP_B5/SRCCLKREQ0#

B42 CLKOUT_PCIE_N1
A42 CLKOUT_PCIE_P1
PCIE_CLKREQ1# → AT7 GPP_B6/SRCCLKREQ1#

WLAN
[26] CLK_PCIE_WLANN → CLK_PCIE_WLANN → D41 CLKOUT_PCIE_N2
[26] CLK_PCIE_WLANP → CLK_PCIE_WLANP → C41 CLKOUT_PCIE_P2
[26] PCIE_CLKREQ_WLAN# → PCIE_CLKREQ_WLAN# → AT8 GPP_B7/SRCCLKREQ2#

LAN
[24] CLK_PCIE_LANN → CLK_PCIE_LANN → D40 CLKOUT_PCIE_N3
[24] CLK_PCIE_LANP → CLK_PCIE_LANP → C40 CLKOUT_PCIE_P3
[24] PCIE_CLKREQ_LAN# → PCIE_CLKREQ_LAN# → AT10 GPP_B8/SRCCLKREQ3#

B40 CLKOUT_PCIE_N4
A40 CLKOUT_PCIE_P4
PCIE_CLKREQ4# → AU9 GPP_B9/SRCCLKREQ4#

E40 CLKOUT_PCIE_N5
E39 CLKOUT_PCIE_P5
PCIE_CLKREQ5# → AU7 GPP_B10/SRCCLKREQ5#

SKL_ULT REV = 1
10 OF 20
?

CLKOUT_ITPXDP_N → F43 CK_XDP_N_R → 4 *0_4P2R_4 3 → CK_XDP_N [17]
CLKOUT_ITPXDP_P → E43 CK_XDP_P_R → 2 1 → CK_XDP_P [17]

RP1 install for XDP

GPD8/SUSCLK → BA17 PCH_SUSCLK → TP59

XTAL24_IN → E37 XTAL24_IN
XTAL24_OUT → E35 XTAL24_OUT → +1V_S5

XCLK_BIASREF → E42 XCLK_BIASREF → R461 2.7K/F_4 → R462 *60.4/F_4

Co-lay 60ohm 1% to GND for Cannonlake use

RTCX1 → AM18 RTC_X1
RTCX2 → AM20 RTC_X2

SRTCRST# → AN18 SRTC_RST#
RTCRST# → AM16 RTC_RST# → RTC_RST# [17]

CLK_REQ/Strap Pin(CLG)

+3V
10K_4 R212 PCIE_CLKREQ4#
10K_4 R197 PCIE_CLKREQ_WLAN#
10K_4 R196 PCIE_CLKREQ_LAN#
10K_4 R211 PCIE_CLKREQ1#
10K_4 R210 PCIE_CLKREQ5#
10K_4 R213 PCIE_CLKREQ_VGA#

U21I SKL_ULT ?

CSI-2

A36 CSI2_DN0
B36 CSI2_DP0
C36 CSI2_DN1
D36 CSI2_DP1
C35 CSI2_DN2
D35 CSI2_DP2
A35 CSI2_DN3
B35 CSI2_DP3

C31 CSI2_DN4
D31 CSI2_DP4
C33 CSI2_DN5
D33 CSI2_DP5
A31 CSI2_DN6
B31 CSI2_DP6
A33 CSI2_DN7
B33 CSI2_DP7

A29 CSI2_DN8
B29 CSI2_DP8
C28 CSI2_DN9
D28 CSI2_DP9
A27 CSI2_DN10
B27 CSI2_DP10
C27 CSI2_DN11
D27 CSI2_DP11

CSI2_CLKN0 → C37
CSI2_CLKP0 → D37
CSI2_CLKN1 → C32
CSI2_CLKP1 → D32
CSI2_CLKN2 → C29
CSI2_CLKP2 → D29
CSI2_CLKN3 → B26
CSI2_CLKP3 → A26

CSI2_COMP → E13 CSI2_RCOMP → R165 100/F_4
GPP_D4/FLASHTRIG → B7 GPP_D4 → TP61

EMMC

GPP_F13/EMMC_DATA0 → AP2
GPP_F14/EMMC_DATA1 → AP1
GPP_F15/EMMC_DATA2 → AP3
GPP_F16/EMMC_DATA3 → AN3
GPP_F17/EMMC_DATA4 → AN1
GPP_F18/EMMC_DATA5 → AN2
GPP_F19/EMMC_DATA6 → AM4
GPP_F20/EMMC_DATA7 → AM1

GPP_F21/EMMC_RCLK → AM2
GPP_F22/EMMC_CLK → AM3
GPP_F12/EMMC_CMD → AP4

EMMC_RCOMP → AT1 EMMC_RCOMP → R184 200/F_4

SKL_ULT REV = 1
9 OF 20
?

RTC Clock 32.768KHz

EC-SI-12

C355 12P/50V_4 — Y3 32.768KHz — C356 12P/50V_4
RTC_X1 — R224 10M_4 — RTC_X2

External Crystal

EC-SI-12

C360 12P/50V_4
XTAL24_IN — R130 1M_4 — Y2 24MHZ +-30PPM — XTAL24_OUT
C273 12P/50V_4

RTC Circuitry(RTC)

RTC Power trace width 20mils.

+3V_ALW → R554 1.5K_4
+3V_RTC_2
+3V_RTC_0

R555 45.3K_4 — D18 RB500V-40 — R567 20K/F_4 — RTC_RST#
R553 1K_4 +3V_RTC_1 — D17 RB500V-40 — R566 20K/F_4 — SRTC_RST#

C589 1U/6.3V_4
C590 *220P/50V_4
C581 1U/6.3V_4
C588 1U/6.3V_4

CN20 — CONNDIPHOUSING2P

RTC_RST# — Q35 2N7002K — EC_RTC_RST — EC_RTC_RST [29]
R561 10K_4

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Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU CLK/eMMC	1A

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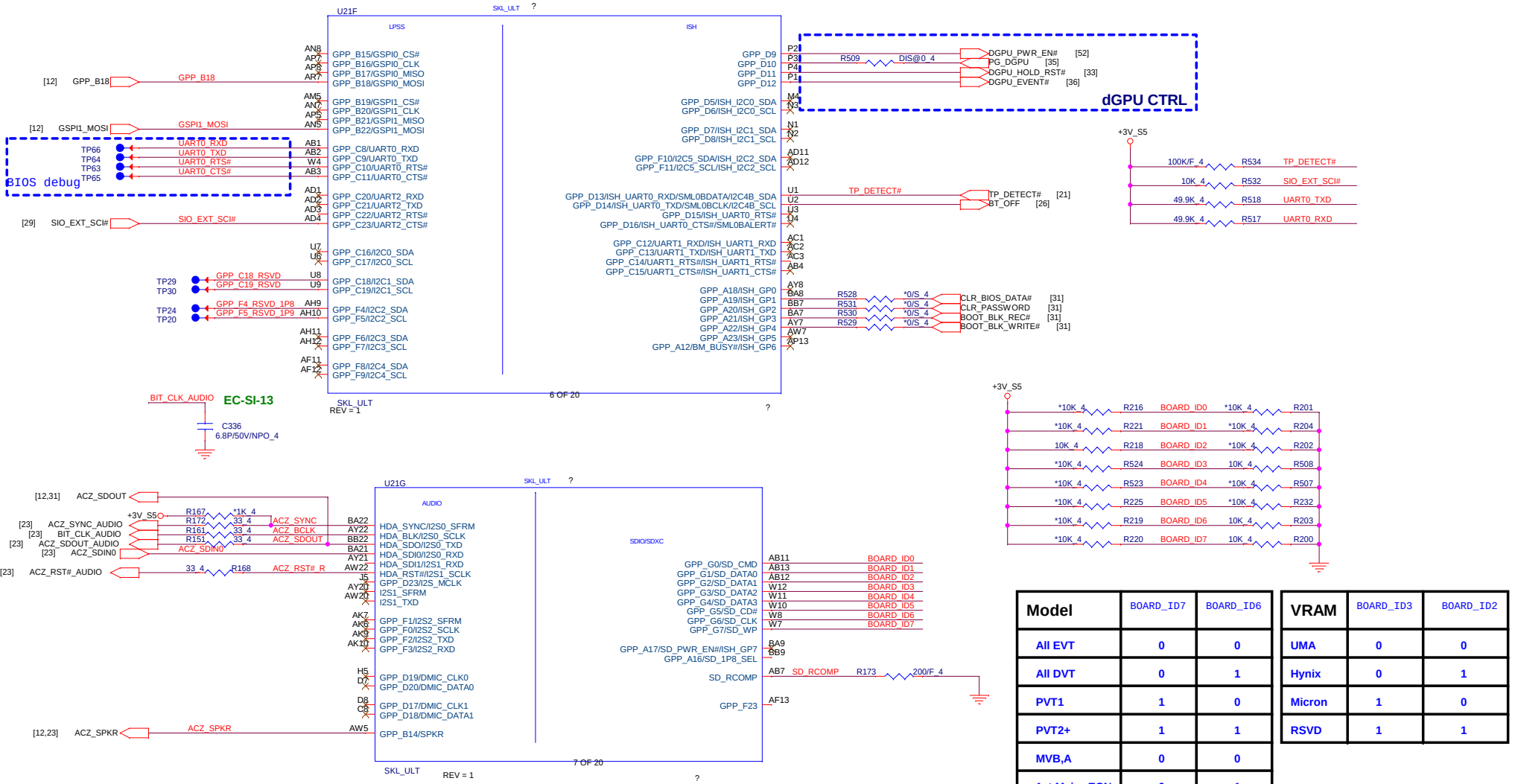
[5,11,12,13,16,17,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52]
[3,5,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52]
+3V_S5
+3V



Model	BOARD_ID7	BOARD_ID6
All EVT	0	0
All DVT	0	1
PVT1	1	0
PVT2+	1	1
MVB,A	0	0
1st Major ECN	0	1
2nd Major ECN	1	0
3rd Major ECN	1	1

VRAM	BOARD_ID3	BOARD_ID2
UMA	0	0
Hynix	0	1
Micron	1	0
RSVD	1	1

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Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU HDA/GPIO	1A

Date: Thursday, March 10, 2016 Sheet 15 of 58

[10,14,17,41,46,48] +1V_S5
[10,29,42,46,48] +1.8V_S5
[5,11,12,13,15,17,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52] +3V_S5
[5,14] +3V_RTC_2
[3,5,11,12,13,14,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V

U21O
SKL_ULT
CPU POWER 4 OF 4

VCCPRIM_1P0 AB19, AB20, P18 — 2.899A
VCCPRIM_CORE AF18, AF19, V20, V21 — 2.57A
DCPDSW_1P0 AL1
VCCMPHYAON_1P0 K17, L1
VCCMPHYGT_1P0_N15 N15, N16, N17 — 1.714A
VCCMPHYGT_1P0_P15 P15, P16
VCCAMPHYPLL_1P0 K15, L15
VCCAPLL_1P0 V15 — 0.03A
VCCPRIM_1P0_AB17 AB17, Y18
VCCDSW_3P3_AD17 AD17, AD18 — 0.09A
VCCDSW_3P3_AJ17 AJ17
VCCHDA AJ19
VCCSPI AJ16
VCCSRAM_1P0 AF20, AF21, T19, T20
VCCPRIM_3P3_AJ21 AJ21
VCCPRIM_1P0_AK20 AK20
VCCAPLLEBB N18

VCCPGPPA AK15 +VCCPGPPA
VCCPGPPB AG15 +VCCPGPPB
VCCPGPPC Y16 +VCCPGPPC
VCCPGPPD Y15 +VCCPGPPD
VCCPGPPE T16 +VCCPGPPE
VCCPGPPF AF16 +VCCPGPPF
VCCPGPPG AD15 +VCCPGPPG
VCCPRIM_3P3_V19 V19
VCCPRIM_1P0_T1 T1 +VCCPRIM_1.0V_T1
VCCATS_1P8 AA1 +VCCATS_1.8V
VCCRTCPRIM_3P3 AK17 +VCCRTCPRIM_3.3V
VCCRTC_AK19 AK19 +VCCRTC
VCCRTC_BB14 BB14
DCPRTC BB10 DCPRTC
VCCCLK1 A14 +VCCCLK1
VCCCLK2 K19 +VCCCLK2
VCCCLK3 L21 +VCCCLK3
VCCCLK4 N20 +VCCCLK4
VCCCLK5 L19 +VCCCLK5
VCCCLK6 A10 +VCCCLK6
GPP_B0/CORE_VID0 AN11 CORE_VID0
GPP_B1/CORE_VID1 AN13 CORE_VID1

SKL_ULT
REV = 1
15 OF 20

EC-PV-01
RF
20mils

TP21
TP19

+V3.3DX_1.5DX_ADO
+3V
+3V_ALW
+1V_S5
+VCCDSW_1.0V
+VCCPRIM
+VCCMPHYAON_1P0
+VCCAMPHYPLL_1P0
+VCCAPLL_1.0V
+VCCSPI
+VCCSRAM_1.0V
+VCCPRIM_3.3V
+VCCPRIM_1.0V
+VCCAPLLEBB
+VCCATS_1.8V
+VCCRTC
+VCCRTCPRIM_3.3V
+1.8V_S5

Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU Power (PCH)	1A

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[3,5,11,12,13,14,16,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[10,14,16,41,46,48] +1V_S5
[3,5,7,46,48] +VCCIO
[5,11,12,13,15,16,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52] +3V_S5

CPU XDP

CN1 — *Samtec BSH-030-01

1	XDP_PRESENT#	GND1	60
2	PROC_PREQ#	OBSFN_C0	59
3	OBSFN_A1	OBSFN_C1	58
4	GND2	GND3	57
5	OBSDATA_A0	OBSDATA_C0	56
6	OBSDATA_A1	OBSDATA_C1	55
7	GND4	GND5	54
8	OBSDATA_A2	OBSDATA_C2	53
9	OBSDATA_A3	OBSDATA_C3	52
10	GND6	GND7	51
11	OBSFN_B0	OBSFN_D0	50
12	OBSFN_B1	OBSFN_D1	49
13	GND8	GND9	48
14	OBSDATA_B0	OBSDATA_D0	47
15	OBSDATA_B1	OBSDATA_D1	46
16	GND10	GND11	45
17	OBSDATA_B2	OBSDATA_D2	44
18	OBSDATA_B3	OBSDATA_D3	43
19	GND12	GND13	42
20	HOOK0	ITPCLK/HOOK4	41
21	HOOK1	ITPCLK#/HOOK5	40
22	VCC_OBS_AB	VCC_OBS_CD	39
23	HOOK2	HOOK6/RESET#	38
24	HOOK3	HOOK7/DBR#	37
25	GND14	GND15	36
26	XDP_SDA	XDP_TDO	35
27	XDP_SCL	XDP_TRSTn	34
28	XDP_TCK1	XDP_TDI	33
29	XDP_TCK0	XDP_TMS	32
30	GND16	GND(XDP_PRESENT#)	31

[10] CFG3 — R70 *0_4 — CFG3 — 1K_4 — R69
[13] XDP_PREQ#_CPU
[13] XDP_PRDY#_CPU
[10] CFG0 — CFG0 — R78 — 1K_4
[10] CFG1 — CFG1
[10] CFG2 — CFG2
TP44 — CFG3
[3] XDP_BPM0
[3] XDP_BPM1
[10] CFG4 — CFG4
[10] CFG5 — CFG5
[10] CFG6 — CFG6
[10] CFG7 — CFG7
[5,29] RSMRST#
[5,29] DNBSWON# — 1K_4 — R67
+1V_S5 — CFG0 — R65 *0/S_4 — PWR_DEBUG
HOOK3
[11,18,19] SMB_RUN_DAT — R57 *0/S_4 — SMB_RUN_DAT_XDP
[11,18,19] SMB_RUN_CLK — R54 *0/S_4 — SMB_RUN_CLK_XDP
XDP_TCK1
XDP_TCK0
[3] XDP_TCK0

EC-PV-01

CFG17 [10] — CFG16 [10]
CFG8 [10] — CFG9 [10]
CFG10 [10] — CFG11 [10]
CFG19 [10] — CFG18 [10]
CFG12 [10] — CFG13 [10]
CFG14 [10] — CFG15 [10]
CK_XDP_P [14]
CK_XDP_N [14]
+1V_S5
ITP_PMODE [10]
ITP_PMODE
SYS_RESET#
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS
XDP_PRS — TP2

XDP_PRS — R52 *0/S_4 — R53 *0_4 — PCH_SPI_IO2 [11,31]

EC-PV-01

[11,31] PCH_SPI_MOSI — R61 *0_4 — HOOK3 — R62 *1K_4 — +3V_S5

+3V — *1K_4 — R59 — SYS_RESET#
C85 *0.1U/16V_4

+VCCIO — R398 150/F_4 — PWR_DEBUG — R64 *10K_4

+1V_S5 — C99 0.1U/16V_4 — C97 0.1U/16V_4

APS

CN2 — *50501-0180N-001

+3V_S5 — EC-PV-01 — R205 *0/S_4

SUSB# [5,29]
SLP_S5# [5,29]
SUSC# [5,29]
SLP_A# [5]
RTC_RST# [14]
DNBSWON#
SYS_RESET# [5]
R199 *0_4_S — PM_SLP_S0# [5,29]

C515 0.1U/16V_4

U19 — *SN74CBTLV3126RGYR

+3V — R463 *0_4_S — XDP_TDO
[5,29] HWPG
XDP_TDI
XDP_TMS
XDP_TRST#

14	VCC		
2	1A	1B	3
1	1OE		
5	2A	2B	6
4	2OE		
9	3A	3B	8
10	3OE		
12	4A	4B	11
13	4OE		
	DPAD		15
	GND		7

XDP_TDO_CPU [3]
XDP_TDI_CPU [3]
XDP_TMS_CPU [3]
XDP_TRST#_CPU [3]

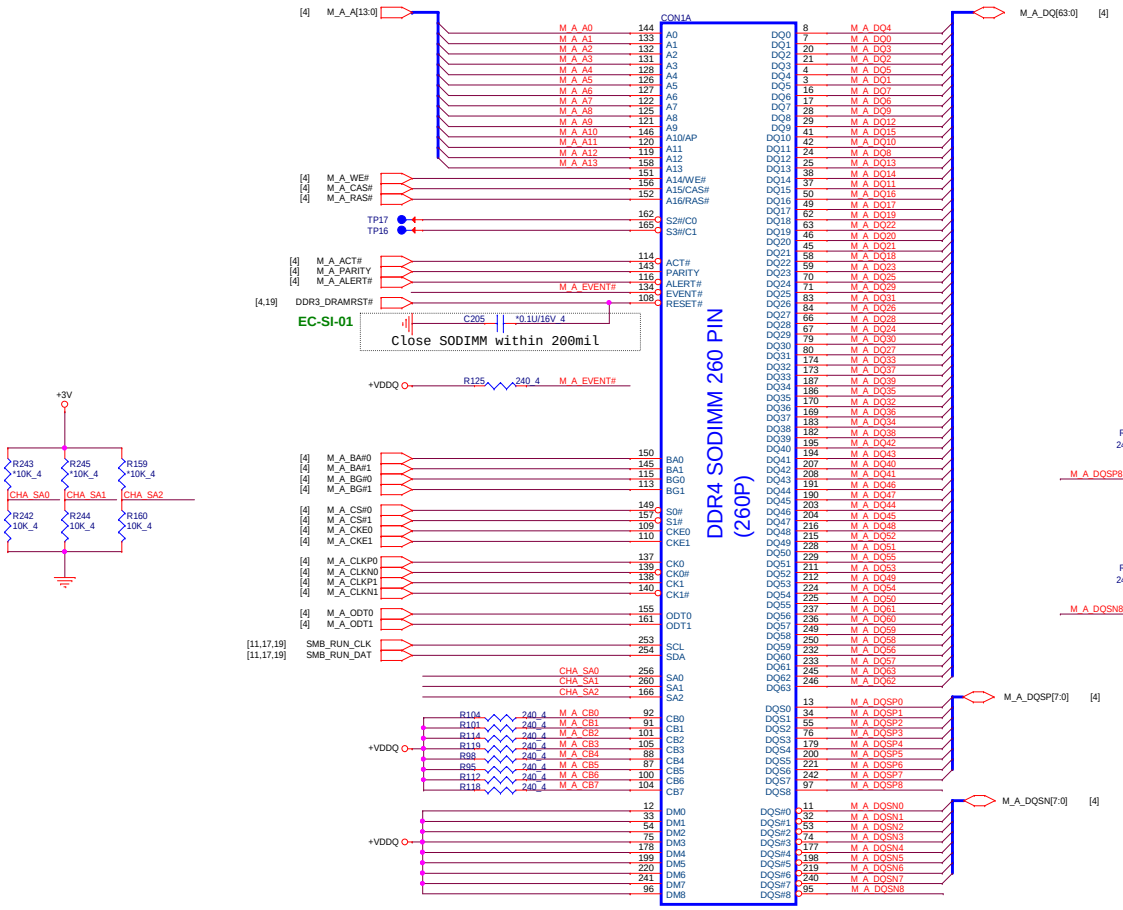
[3] JTAGX_PCH
[3] JTAG_TMS_PCH
[3] JTAG_TDI_PCH
[3] JTAG_TDO_PCH
[3] JTAG_TCK_PCH

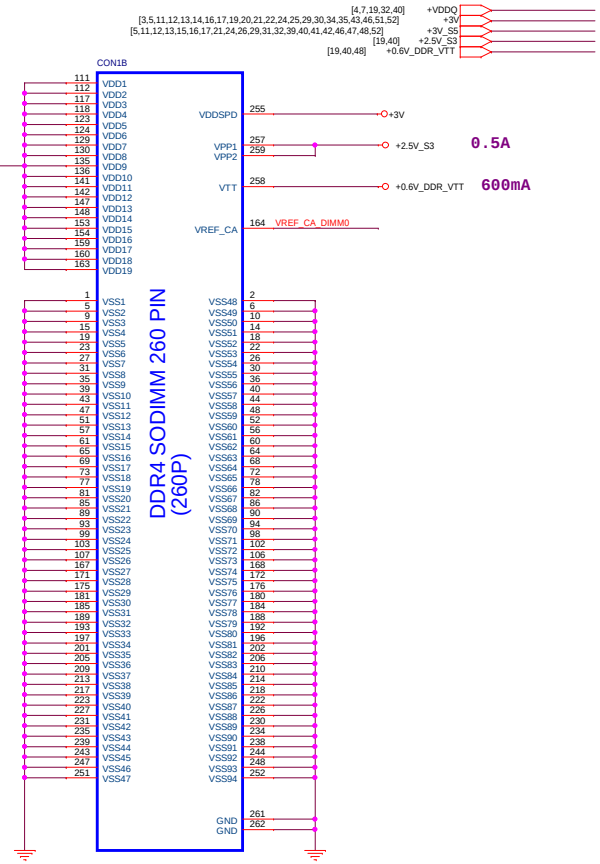
+VCCIO — R450 51_4
R449 *0_4 — XDP_TDO
XDP_TCK0
XDP_TMS
XDP_TDI
XDP_TDO
R446 *0_4 — XDP_TDI
R445 *0_4 — XDP_TCK0
XDP_TCK1

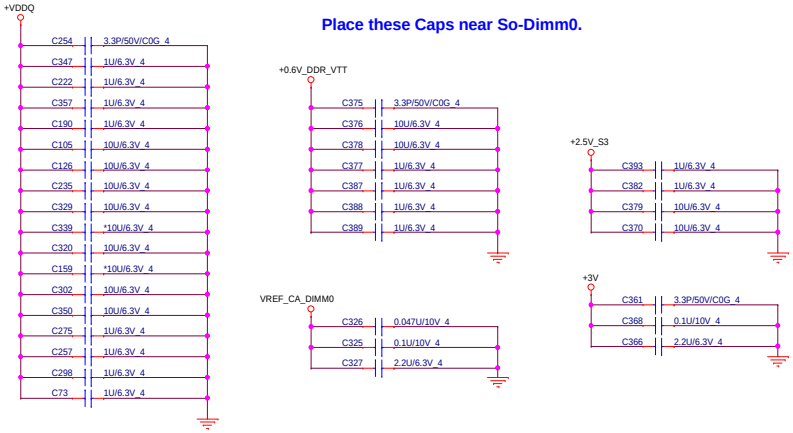
HP Restricted Secret

Quanta Computer Inc.
PROJECT: HP-Hawaii

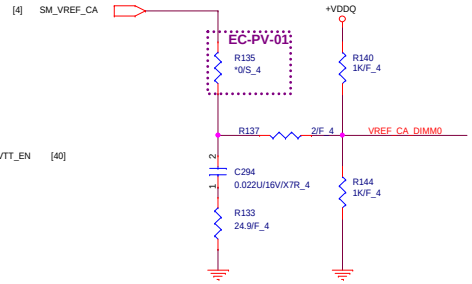
Size	Document Number	Rev
Custom	SKL CPU XDP/APS	1A
Date: Wednesday, March 09, 2016	Sheet 17 of 58	



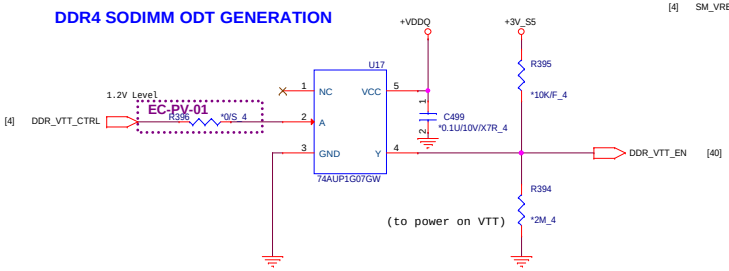




VREF CA DIMM0 Solution



DDR4 SODIMM ODT GENERATION

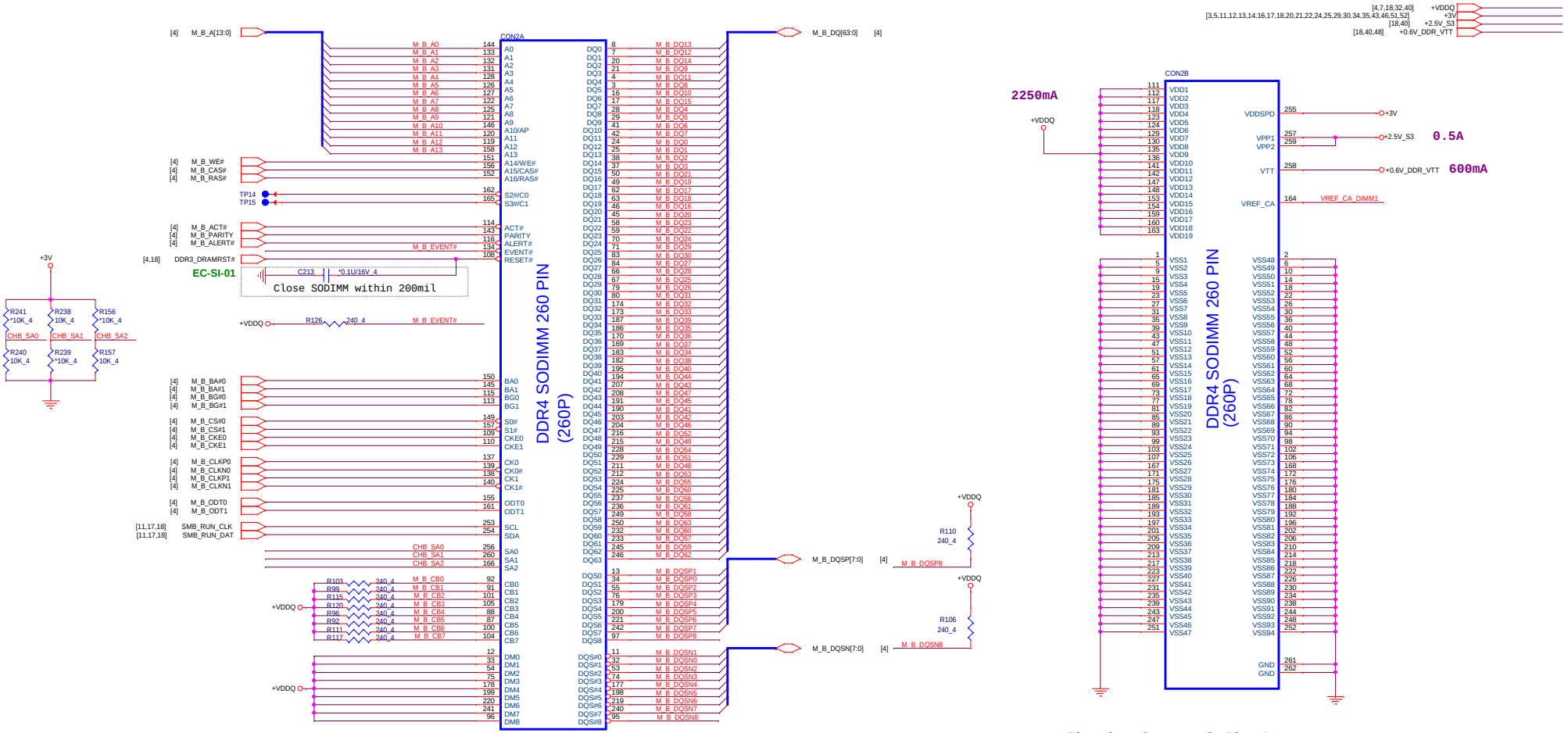


Quanta Computer Inc.

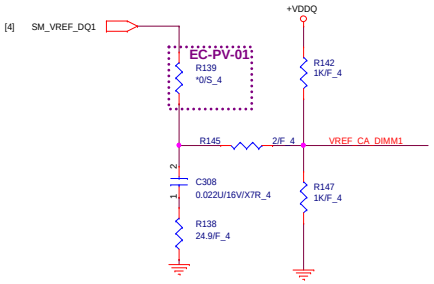
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	DDR4 SODIMM H=8	1A

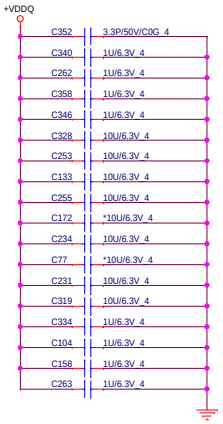
Date: Tuesday, February 02, 2016 Sheet 18 of 58

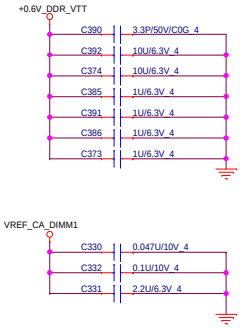


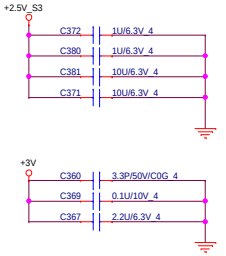
VREF CA DIMM1 Solution



Place these Caps near So-Dimm1





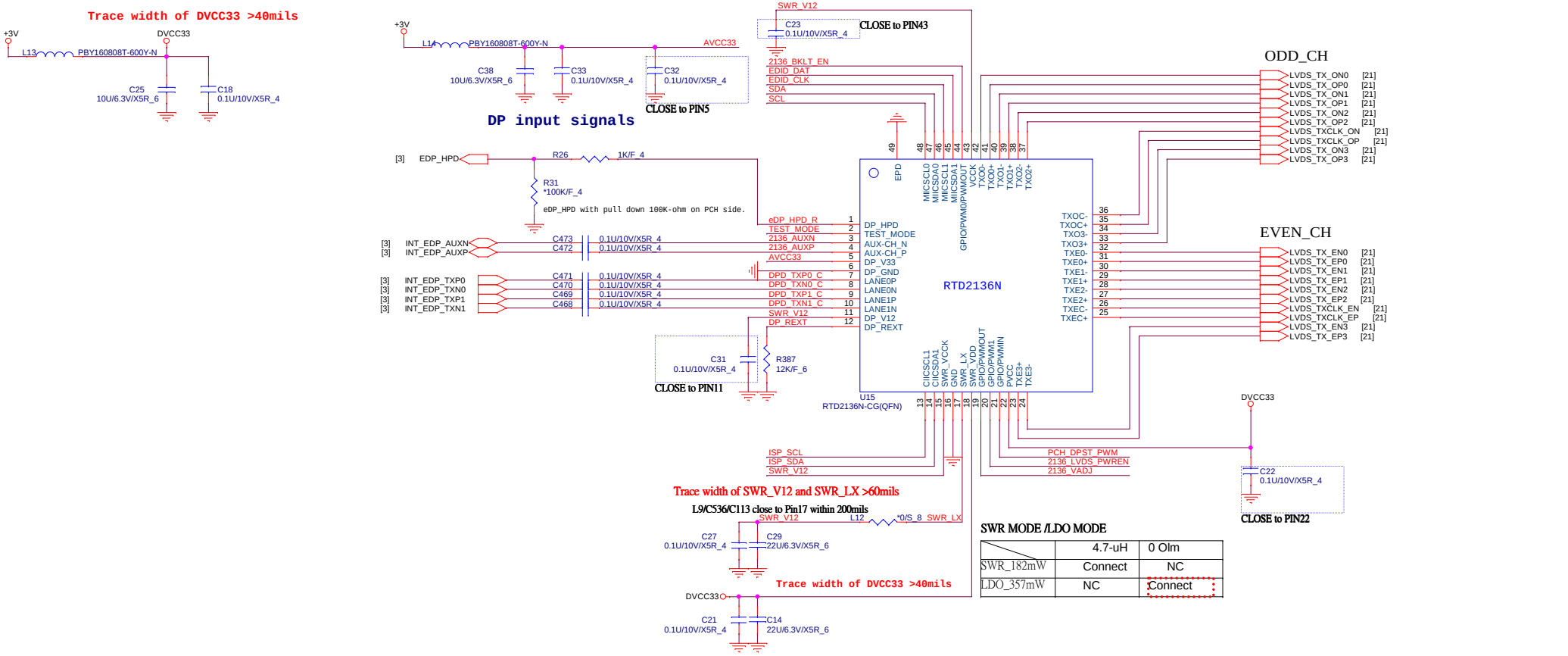


HP Restricted Secret

Quanta Computer Inc.		
PROJECT: HP-Hawaii		
Size: Custom	Document Number: DDR4 SODIMM H=4	Rev: 1A
Date: Thursday, January 28, 2016	Sheet 19 of 58	

eDP to LVDS (RTD2136N-CG)

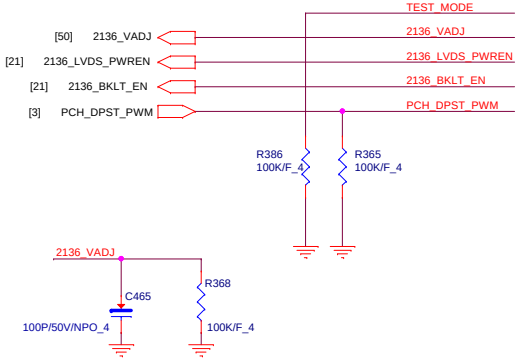
[3,5,11,12,13,14,16,17,18,19,21,22,24,25,29,30,34,35,43,46,51,52] +3V



SWR MODE /LDO MODE

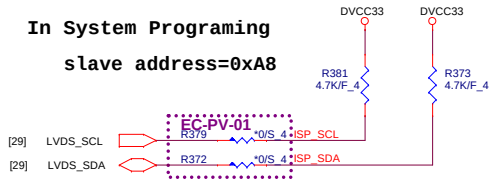
	4.7-uH	0 Olm
SWR_182mW	Connect	NC
LDO_357mW	NC	Connect

GPIO & TESTing signals



In System Programing

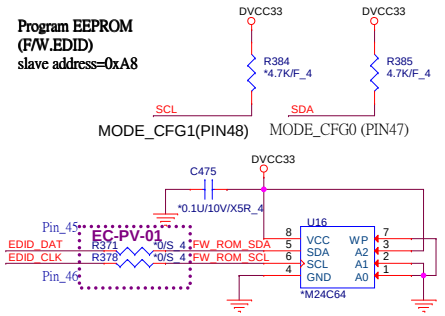
slave address=0xA8



RTD2136N: Mode Selestion		MODE_CFG0 (PIN47)	
		0	1
MODE_CFG1(PIN48)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

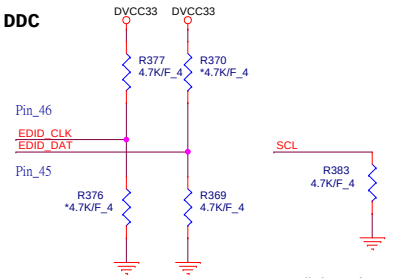
Program EEPROM (F/W.EDID)

slave address=0xA8



The Program EEPROM must be 2 byte addressing device

DDC



Reserve pull down for EPMODE

HP Restricted Secret

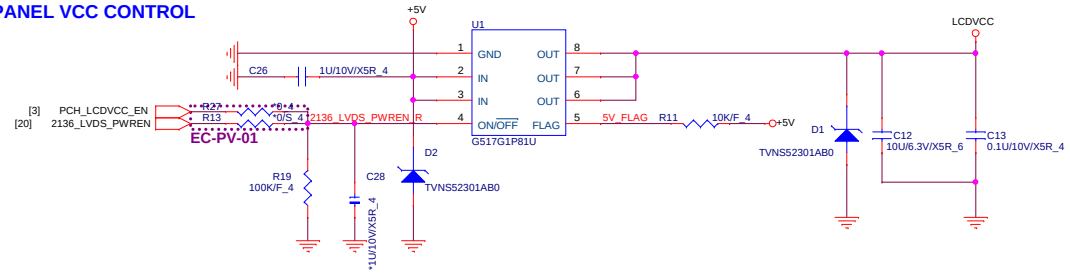
Quanta Computer Inc.

PROJECT: HP-Hawaii

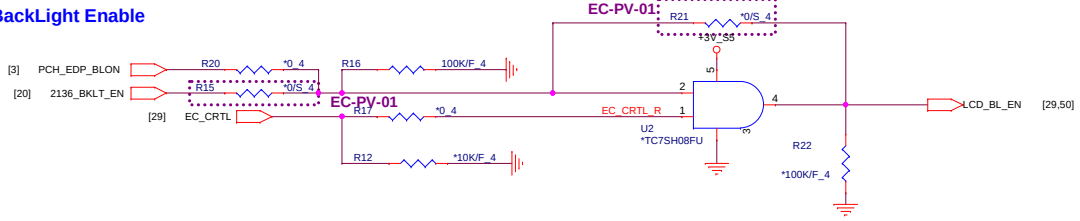
Size	Document Number	Rev
Custom	eDP to LVDS converter	1A

Date: Thursday, January 28, 2016 Sheet 20 of 58

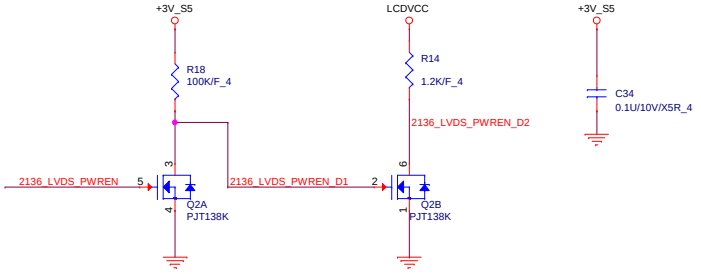
PANEL VCC CONTROL



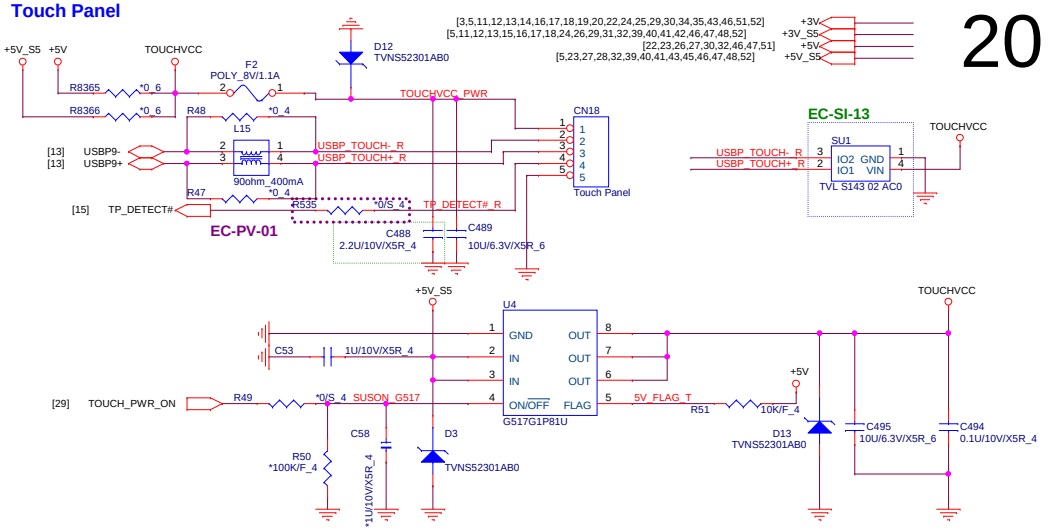
BackLight Enable



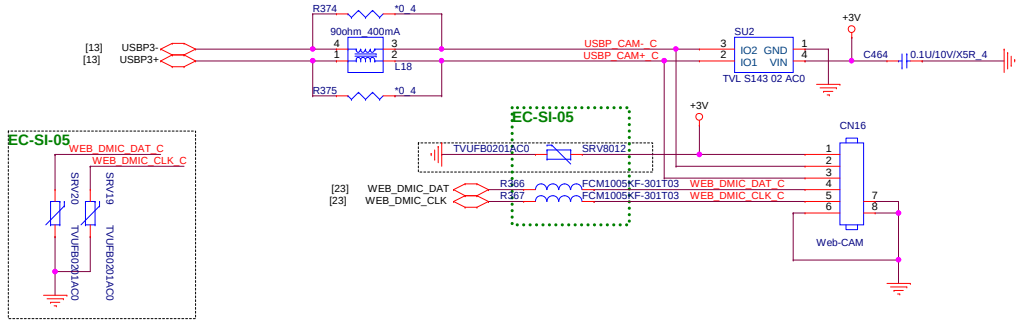
LCDVCC Discharge Circuit

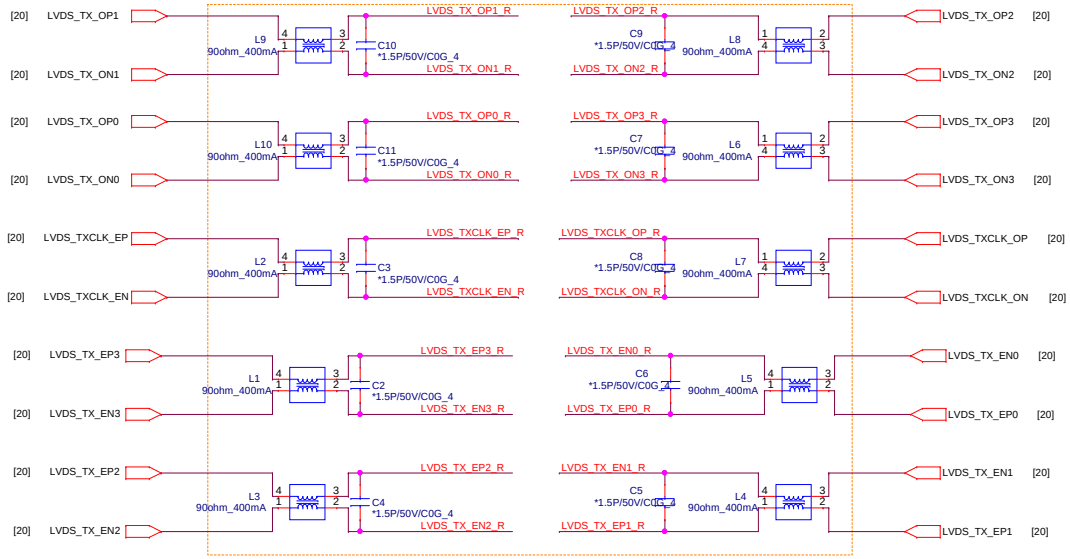


Touch Panel

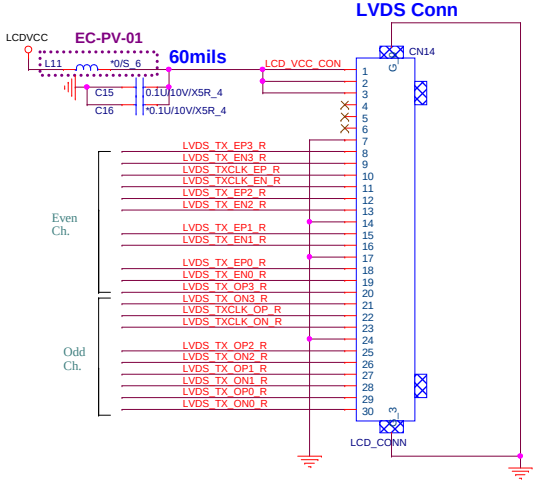


CCD CONN





LVDS Conn



HP Restricted Secret

Quanta Computer Inc.

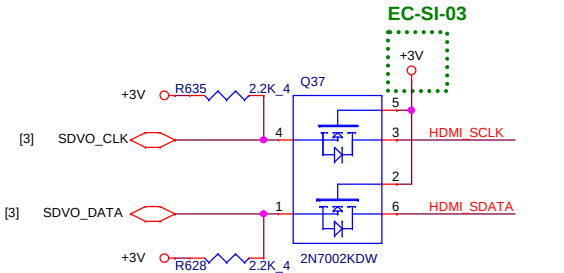
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	LVDS CONN/DDC/Touch Panel	1A
Date: Thursday, March 17, 2016	Sheet 21 of 58	

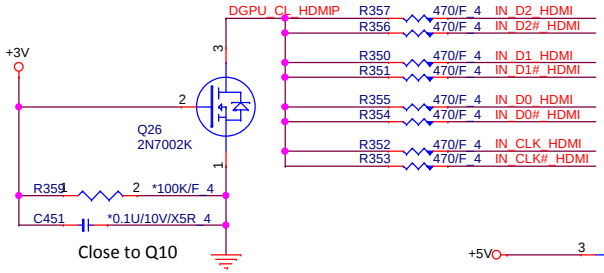
HDMI CONN

[3,5,11,12,13,14,16,17,18,19,20,21,24,25,29,30,34,35,43,46,51,52]
[21,23,26,27,30,32,46,47,51]
+3V
+5V

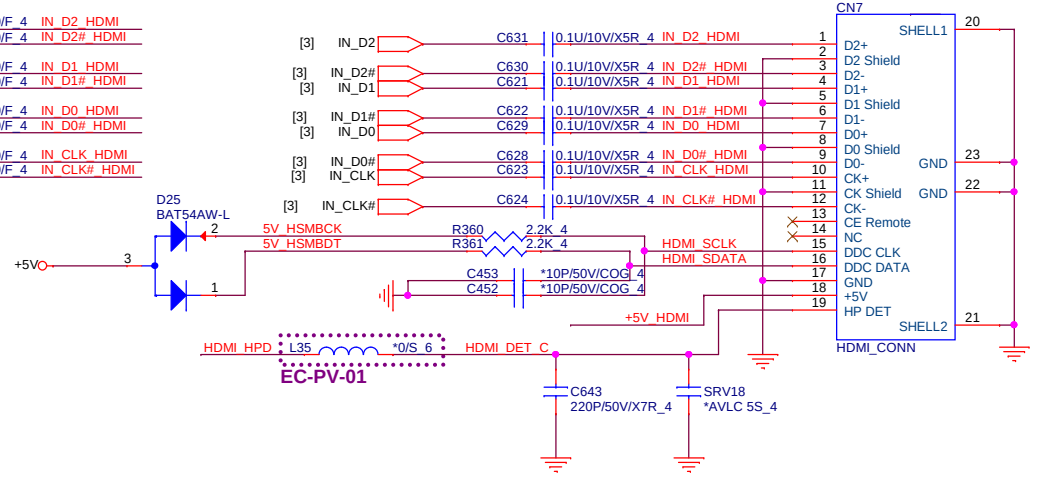
EC-SI-03



Close to HDMI connector

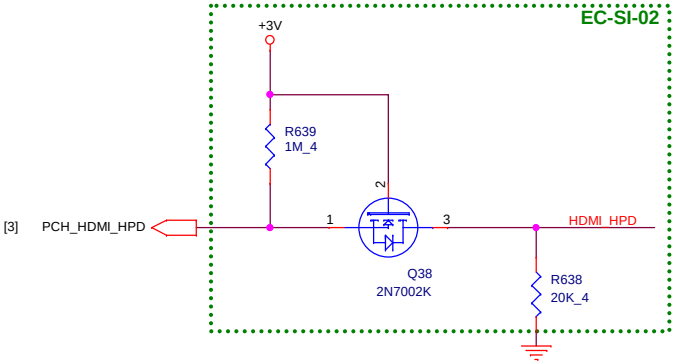


Close to Q10

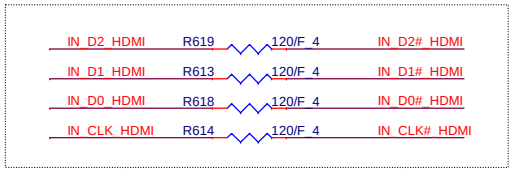


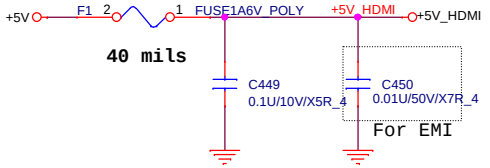
EC-PV-01

EC-SI-02

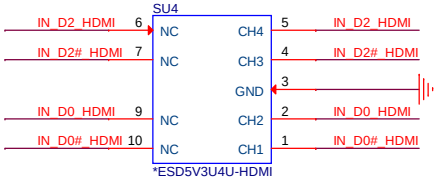


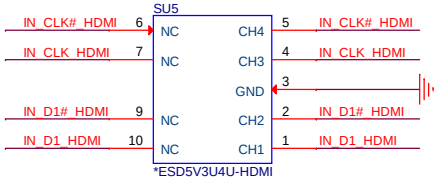
For EMI

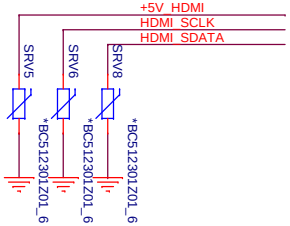




For ESD







Layout note:Place close to HDMI Conn

HP Restricted Secret

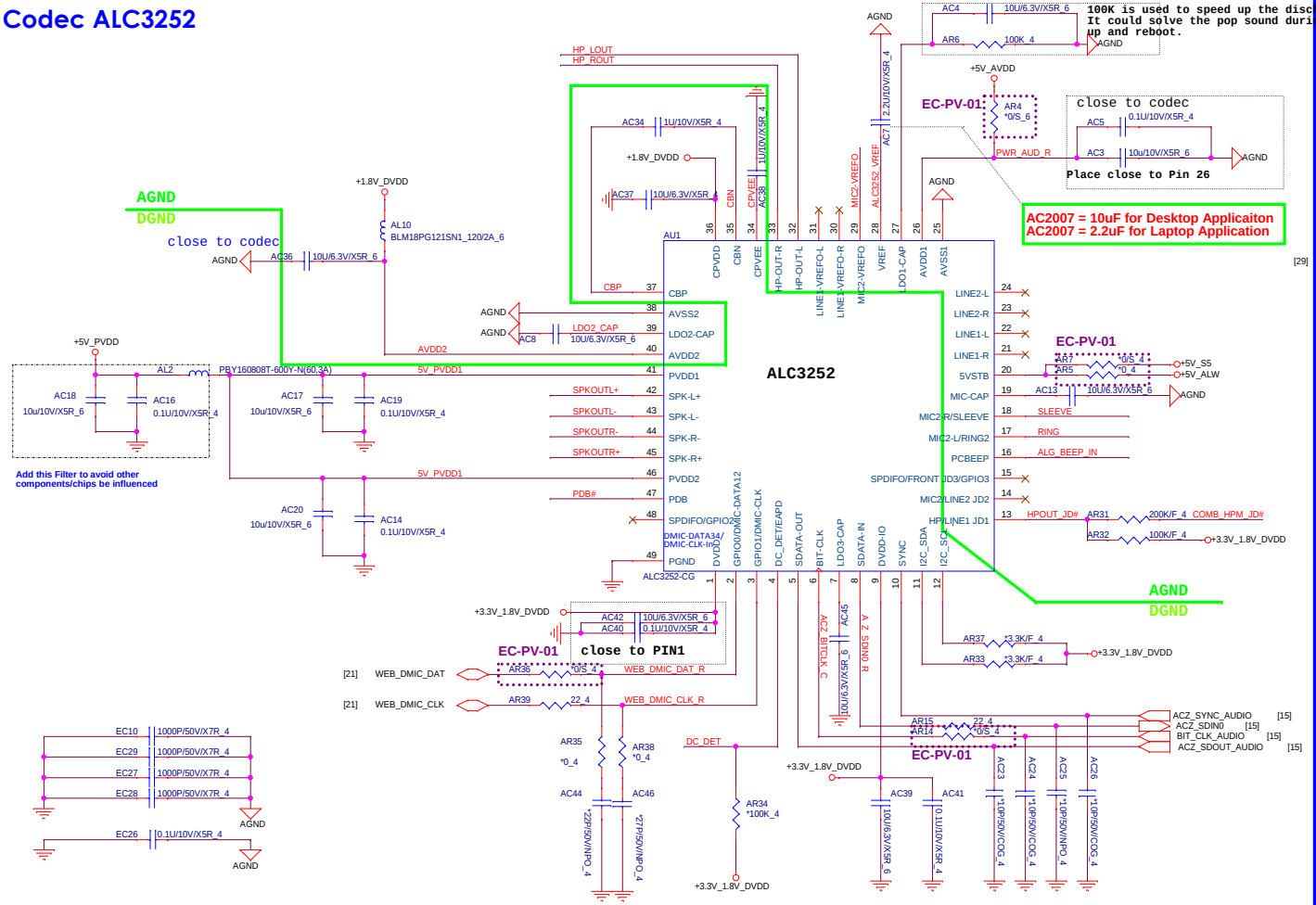
Quanta Computer Inc.

PROJECT: HP-Hawaii

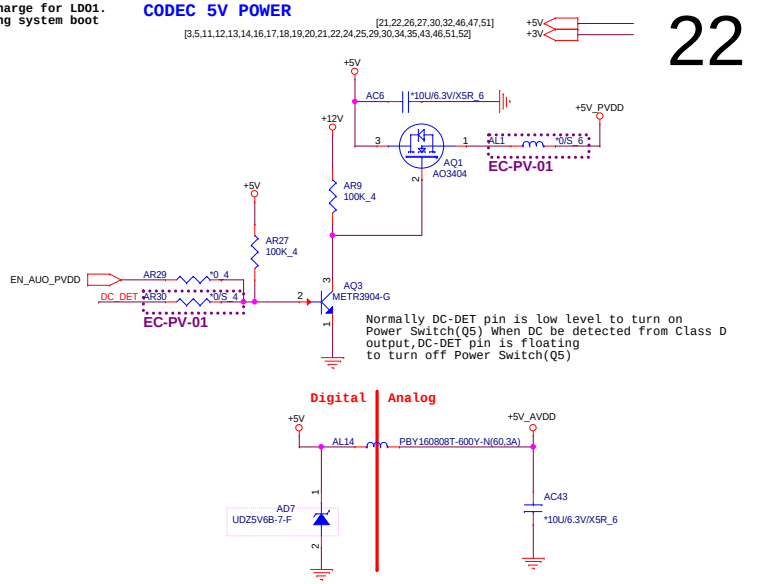
Size	Document Number	Rev
Custom	HDMI	1A

Date: Monday, February 15, 2016 Sheet 22 of 58

Codec ALC3252

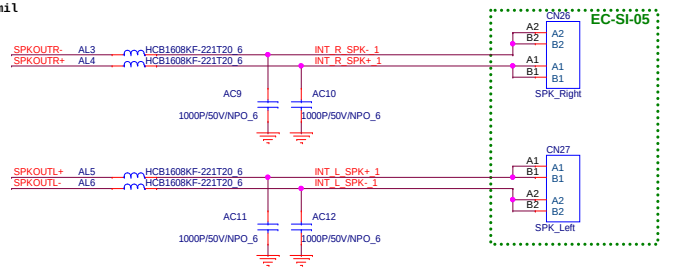


CODEC 5V POWER

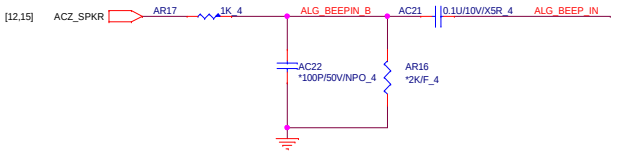


Internal Speaker (2W, 4 ohm)

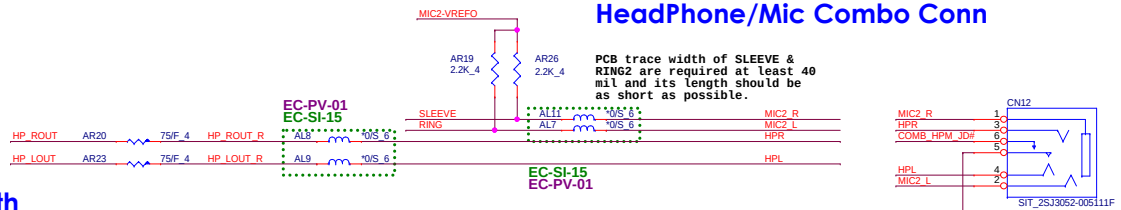
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
4 ohm : 40mil
8 ohm : 20mil



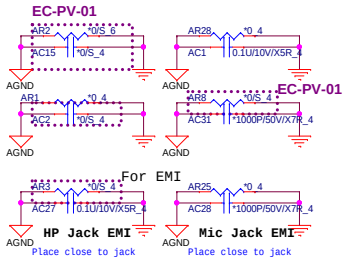
PC BEEP

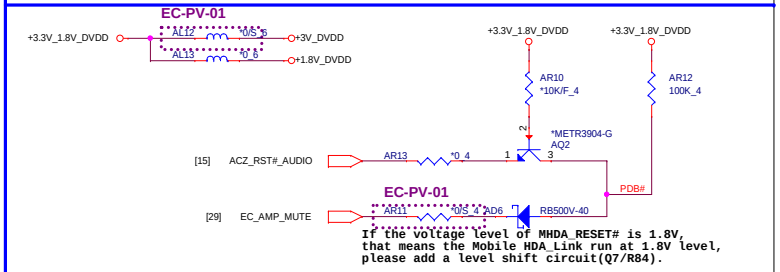


HeadPhone/Mic Combo Conn



CODEC Return Path





HP Restricted Secret

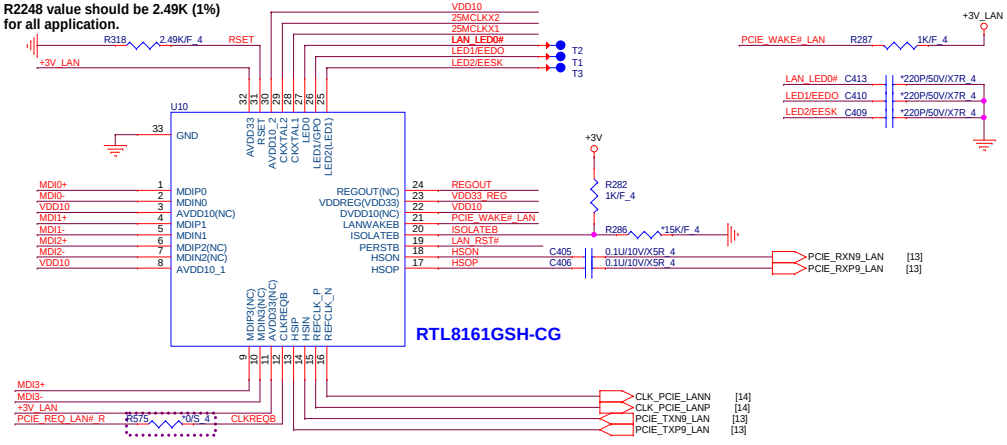
Quanta Computer Inc.

PROJECT: HP-Hawaii

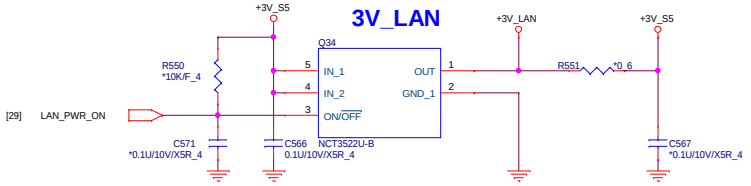
Size	Document Number	Rev
Custom	Audio CODEC	1A

Date: Tuesday, March 22, 2016 Sheet 23 of 58

R2248 value should be 2.49K (1%) for all application.

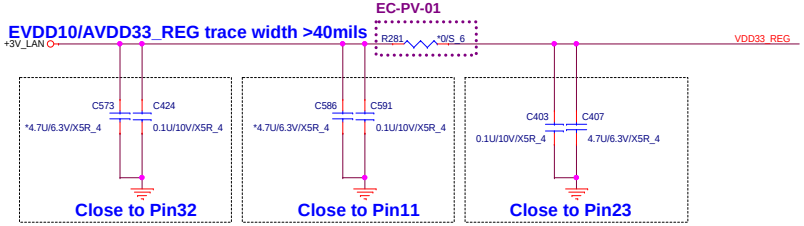


3V_LAN

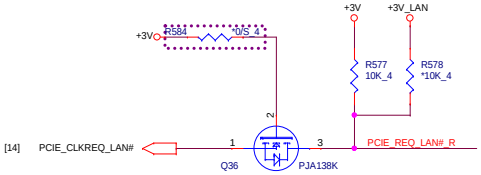


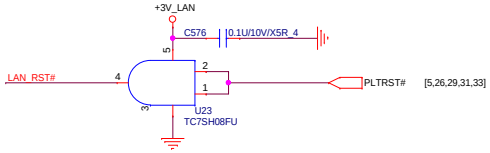
EC-PV-01

EVDD10/AVDD33_REG trace width >40mils

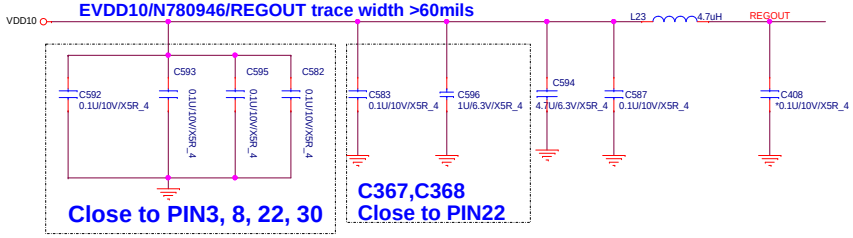


EC-PV-01

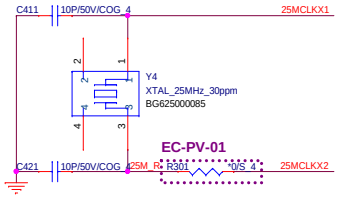




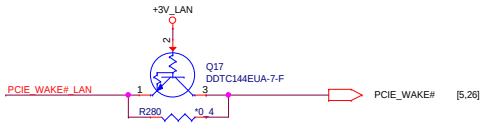
EVDD10/N780946/REGOUT trace width >60mils



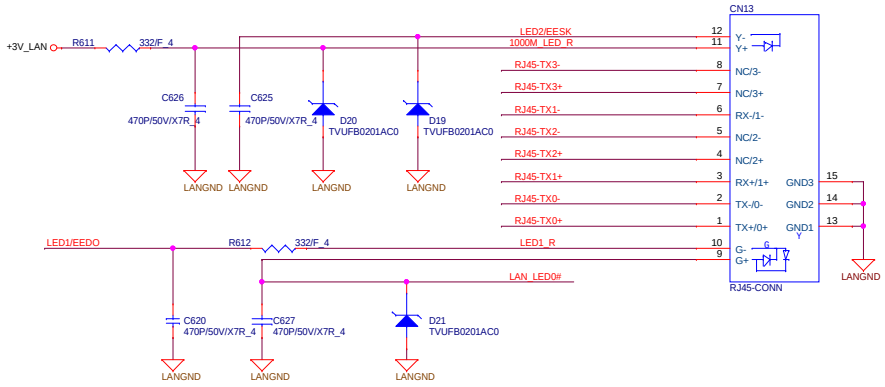
X'tal 25MHz

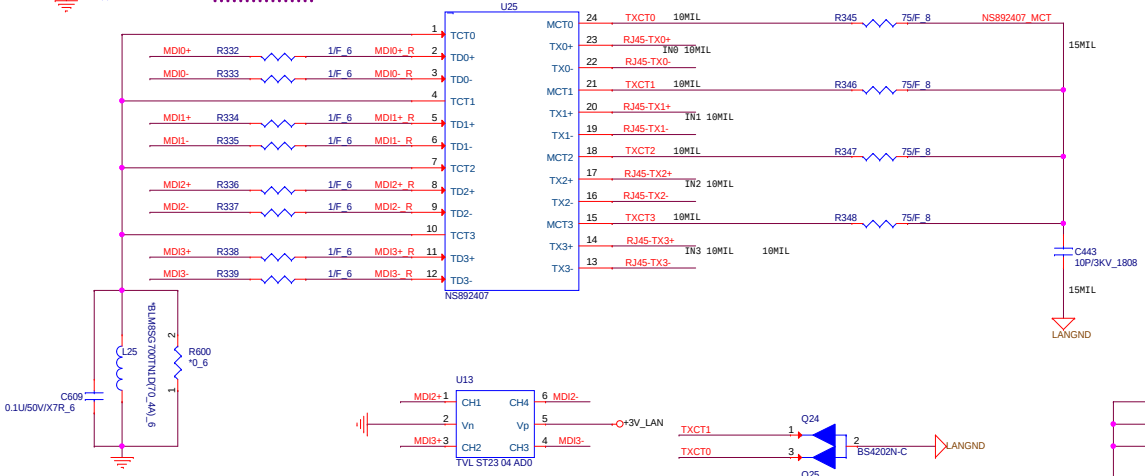


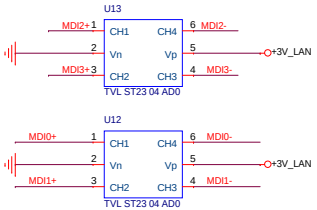
EC-PV-01

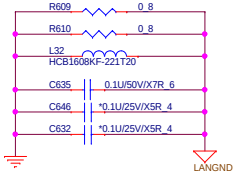


LAN Conn









HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	LAN/RJ45	1A

Date: Wednesday, March 09, 2016 Sheet 24 of 58

[3,5,11,12,13,14,16,17,18,19,20,21,22,24,29,30,34,35,43,46,51,52] +3V

HDD REDRIVER

C44,C45,C46,C47 CLOSE TO RE-DRIVER IC

[13] SATA_TXP0 — C616 *0.01U/50V/X7R_4, R341 *0/S_4 — SATA_TX0_P_RE — SATA_TX0_P_CON [26]
[13] SATA_TXN0 — C614 *0.01U/50V/X7R_4, R340 *0/S_4 — SATA_TX0_N_RE — SATA_TX0_N_CON [26]
[13] SATA_RXN0 — C612 *0.01U/50V/X7R_4, R331 *0/S_4 — SATA_RX0_N_RE — SATA_RX0_N_CON [26]
[13] SATA_RXP0 — C610 *0.01U/50V/X7R_4, R330 *0/S_4 — SATA_RX0_P_RE — SATA_RX0_P_CON [26]

3 PAD DESIGN

EC-PV-01

+3V — R592 *0/S_4 — +3V_HDD_REDRIVER

EC-PV-01

+3V_HDD_REDRIVER

C618 *4.7U/6.3V/X5R_4
C619 *0.1U/10V/X5R_4
C602 *4.7U/6.3V/X5R_4
C604 *0.1U/10V/X5R_4

U24 *PS8527BTQFN20GTR2-A2

6	VCC		
16	VCC	REXT	10 U21_REXT R598 *4.99K/F_4
HDD_A_EQ1 18	A_EQ1	B_EQ2	17 HDD_B_EQ2
HDD_A_EQ2 19	A_EQ2	B_EQ1	20 HDD_B_EQ1
SATA_TX0_P_RE 1	IN0P	OUT0P	15 SATA_TXP0+_R [26]
SATA_TX0_N_RE 2	IN0M	OUT0M	14 SATA_TXN0-_R [26]
SATA_RX0_N_RE 4	OUT1N	IN1N	12 SATA_RXN0-_R [26]
SATA_RX0_P_RE 5	OUT1P	IN1P	11 SATA_RXP0+_R [26]
+3V R593 *10K/F_4 U21_EN 7	EN	GND	3, 13, 22, EP 23, EP 24
+3V R597 *4.7K_4 U21_A_DE 9	A_DE	EP_AGND	
R595 *4.7K_4 U21_B_DE 8	B_DE		21, 25

R594 *4.7K_4, R596 *4.7K_4

+3V

R607 *4.7K_4, R606 *4.7K_4, R608 *4.7K_4, R605 *4.7K_4
HDD_A_EQ1, HDD_A_EQ2, HDD_B_EQ2, HDD_B_EQ1
R603 *4.7K_4, R602 *4.7K_4, R604 *4.7K_4, R601 *4.7K_4

ODD REDRIVER

C53,C57,C58,C59 CLOSE TO RE-DRIVER IC

[13] SATA_TXP1 — C417 *0.01U/50V/X7R_4, R573 *0/S_4 — SATA_TX1_P_RE — SATA_TX1_P_CON [26]
[13] SATA_TXN1 — C416 *0.01U/50V/X7R_4, R572 *0/S_4 — SATA_TX1_N_RE — SATA_TX1_N_CON [26]
[13] SATA_RXN1 — C415 *0.01U/50V/X7R_4, R571 *0/S_4 — SATA_RX1_N_RE — SATA_RX1_N_CON [26]
[13] SATA_RXP1 — C414 *0.01U/50V/X7R_4, R570 *0/S_4 — SATA_RX1_P_RE — SATA_RX1_P_CON [26]

3 PAD DESIGN

EC-PV-01

+3V — R599 *0/S_4 — +3V_ODD_REDRIVER

EC-PV-01

+3V_ODD_REDRIVER

C427 *4.7U/6.3V/X5R_4
C426 *0.1U/10V/X5R_4
C422 *4.7U/6.3V/X5R_4
C418 *0.1U/10V/X5R_4

U11 *PS8527BTQFN20GTR2-A2

6	VCC		
16	VCC	REXT	10 U19_REXT *4.99K/F_4 R329
ODD_A_EQ1 18	A_EQ1	B_EQ2	17 ODD_B_EQ2
ODD_A_EQ2 19	A_EQ2	B_EQ1	20 ODD_B_EQ1
SATA_TX1_P_RE 1	IN0P	OUT0P	15 SATA_TXP1+_R [26]
SATA_TX1_N_RE 2	IN0M	OUT0M	14 SATA_TXN1-_R [26]
SATA_RX1_N_RE 4	OUT1N	IN1N	12 SATA_RXN1-_R [26]
SATA_RX1_P_RE 5	OUT1P	IN1P	11 SATA_RXP1+_R [26]
+3V R320 *10K/F_4 U19_EN 7	EN	GND	3, 13, 22, EP 23, EP 24
+3V R328 *4.7K_4 U19_A_DE 9	A_DE	EP_AGND	
R325 *4.7K_4 U19_B_DE 8	B_DE		21, 25

R323 *4.7K_4, R326 *4.7K_4

+3V

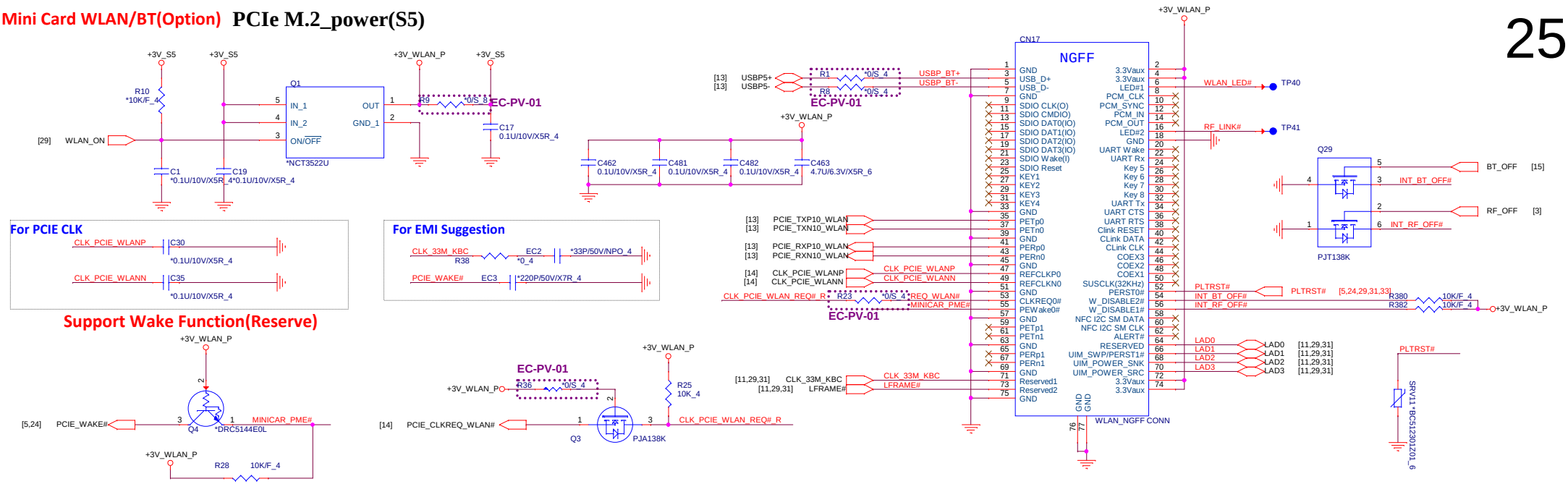
R583 *4.7K_4, R576 *4.7K_4, R586 *4.7K_4, R574 *4.7K_4
ODD_A_EQ1, ODD_A_EQ2, ODD_B_EQ2, ODD_B_EQ1
R322 *4.7K_4, R319 *4.7K_4, R324 *4.7K_4, R305 *4.7K_4

HP Restricted Secret

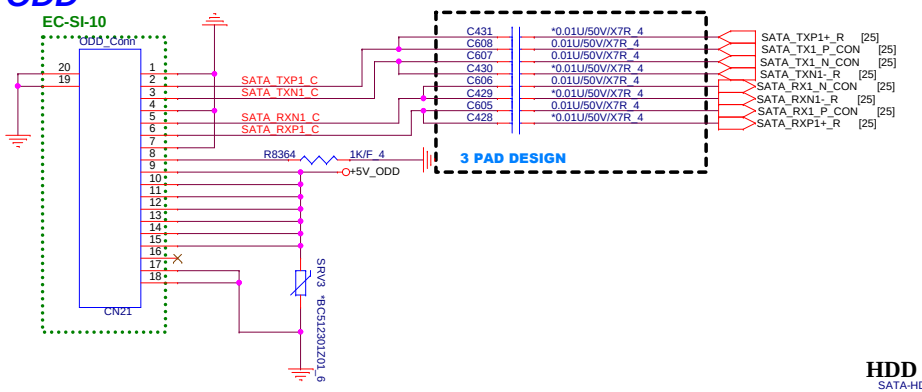
Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SATA Re-driver	1A
Date: Wednesday, January 27, 2016	Sheet 25 of 58	

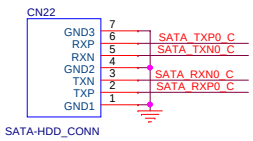
Mini Card WLAN/BT(Option) PCIe M.2_power(S5)

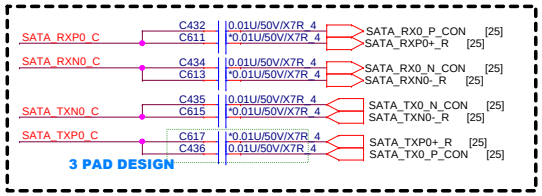


ODD

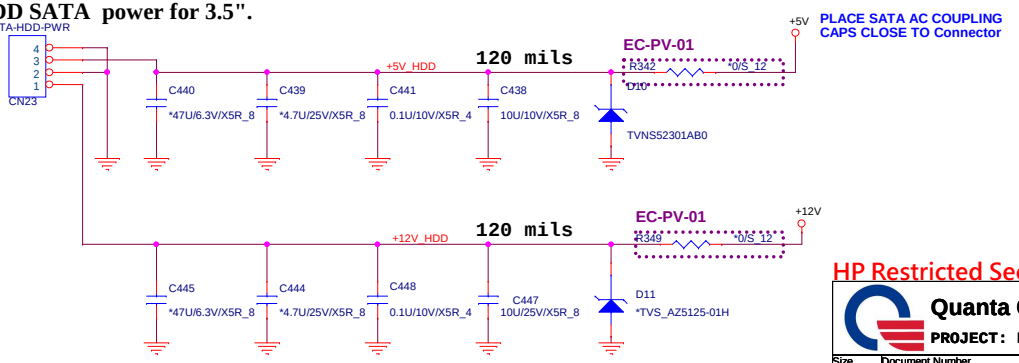


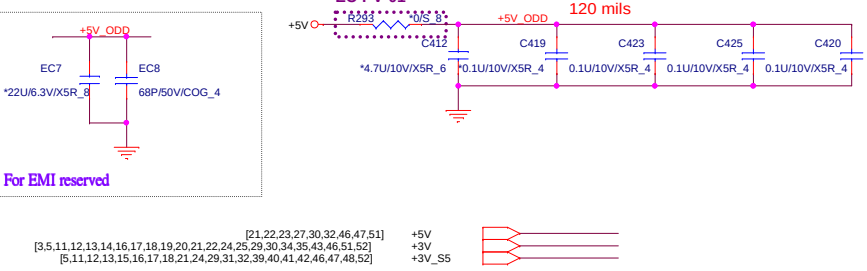
HDD SATA signal for 3.5".





HDD SATA power for 3.5".





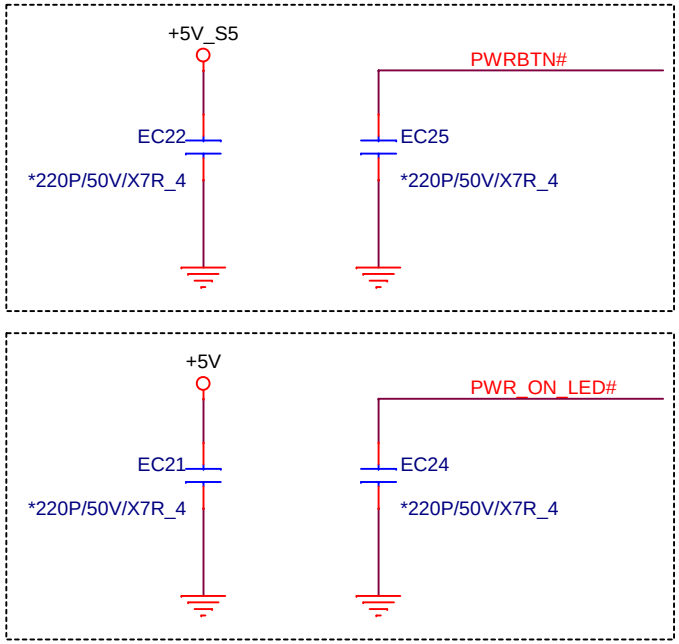
HP Restricted Secret

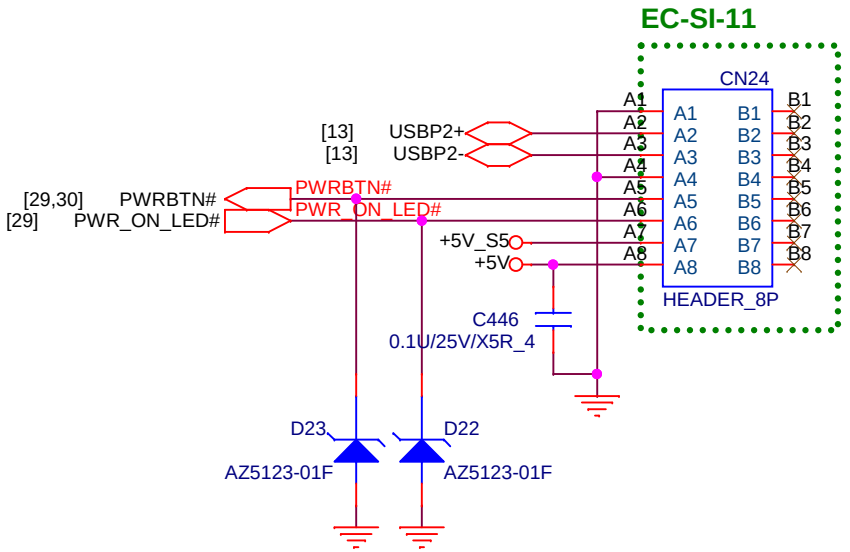
Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	WLAN/HDD/ODD	1A
Date: Tuesday, March 22, 2016	Sheet 26 of 58	

Card reader/Power button conn





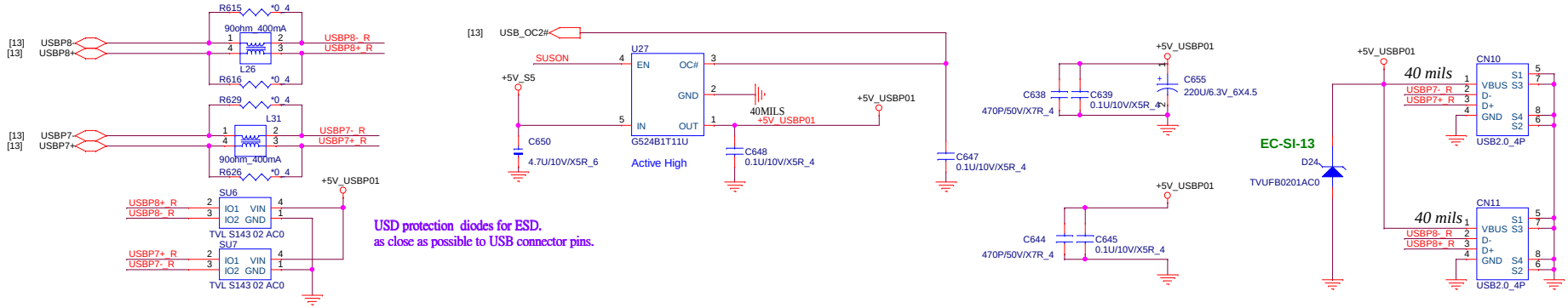
HP Restricted Secret

Quanta Computer Inc.

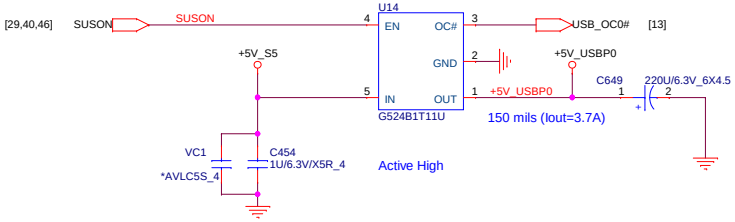
PROJECT: HP-Hawaii

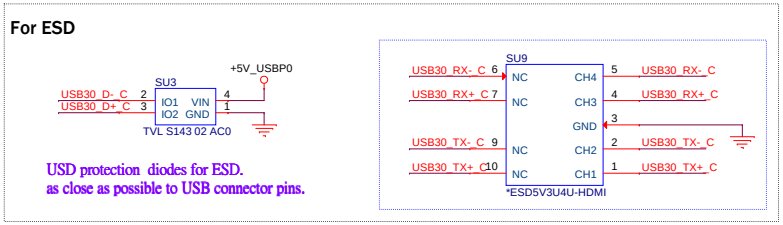
Size	Document Number	Rev
A	Card reader/PWR BTN CONN	1A
Date: Tuesday, March 08, 2016	Sheet 27 of 58	

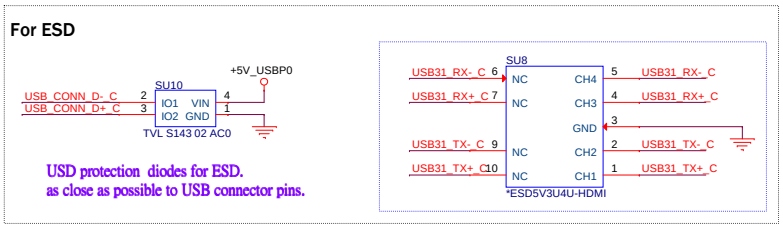
USB 2.0

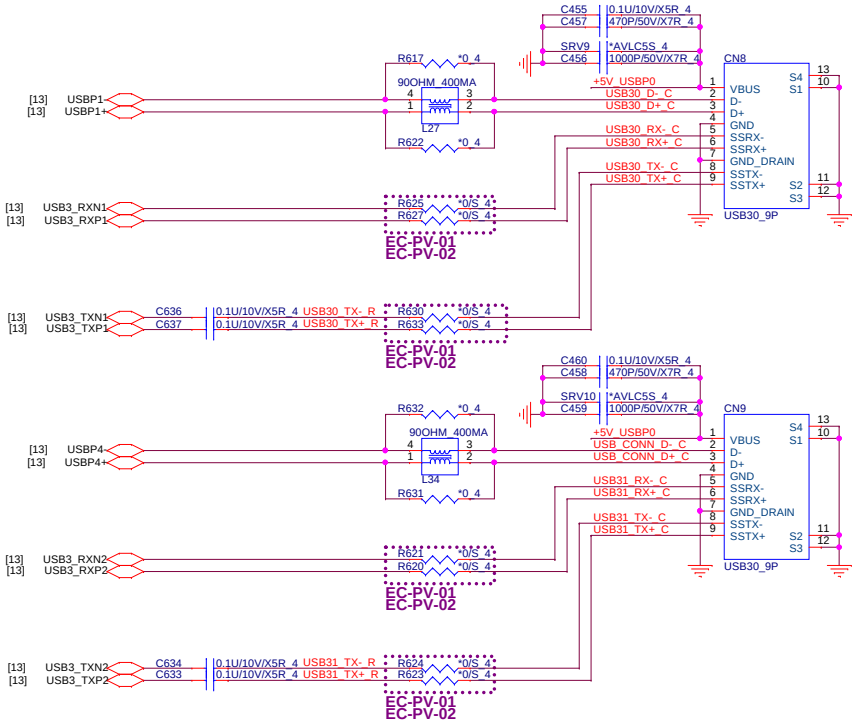


USB 2.0/3.0 Combo









[5,21,23,27,32,39,40,41,43,45,46,47,48,52] +5V_S5

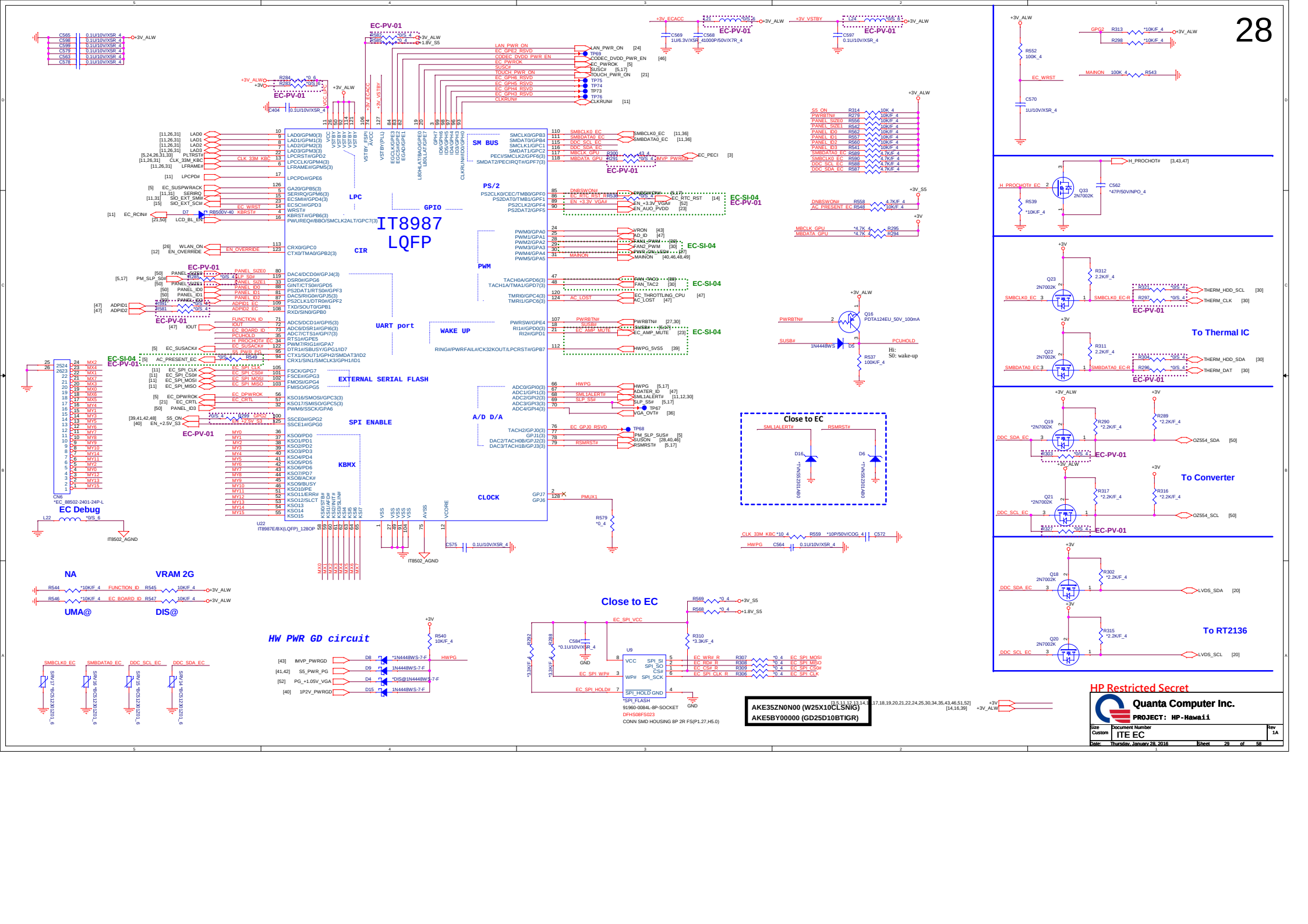
HP Restricted Secret

Quanta Computer Inc.

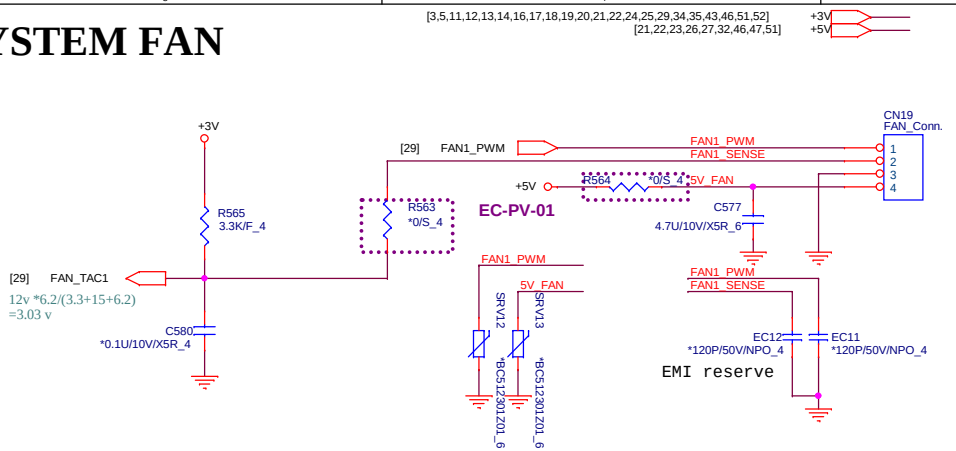
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	USB2.0/USB3.0/Hole/EMI	1A

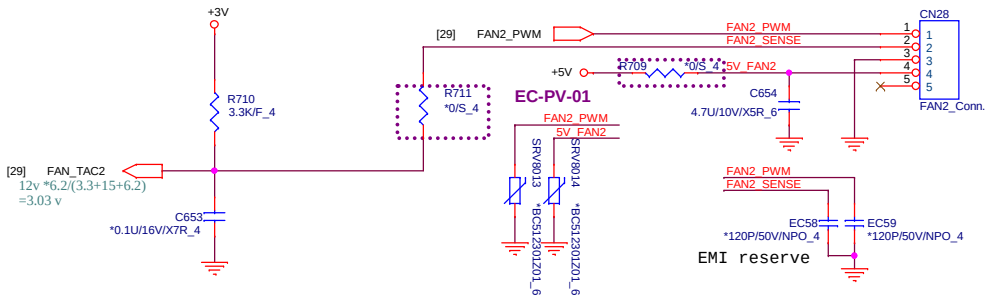
Date: Tuesday, January 26, 2016 Sheet 28 of 58


28
IT8987
LQFP
EC-PV-01
EC-SI-04
LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
A/D D/A
KBMX
CLOCK
EC Debug
Close to EC
HW PWR GD circuit
NA
VRAM 2G
UMA@
DIS@
To Thermal IC
To Converter
To RT2136
HP Restricted Secret
Quanta Computer Inc.
PROJECT: HP-Hawaii
ITE EC
AKE35ZN00N00 (W25X10CLSNIG)
AKE5BY00000 (GD25D10BTIGR)

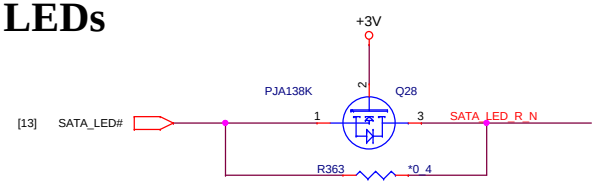
SYSTEM FAN

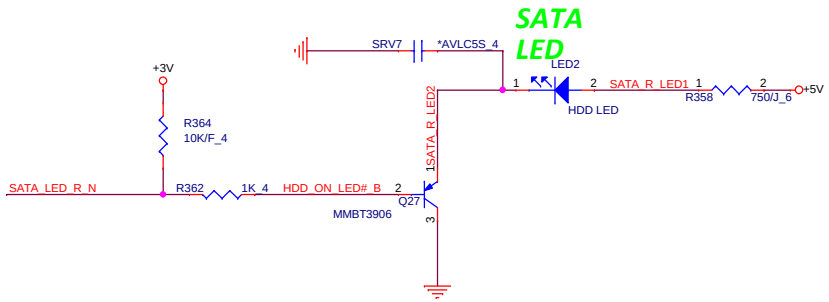


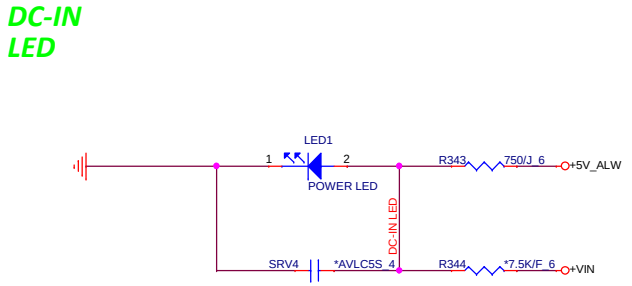
2nd SYSTEM FAN (RSVD)



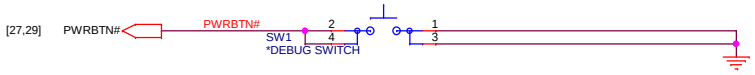
LEDs



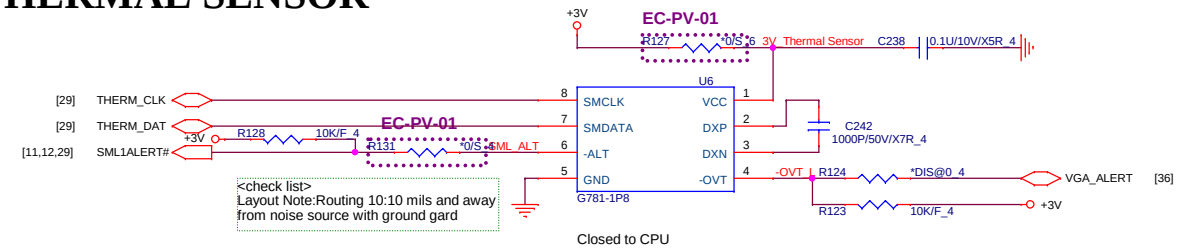




SW1 For Debug.MP will remove it.



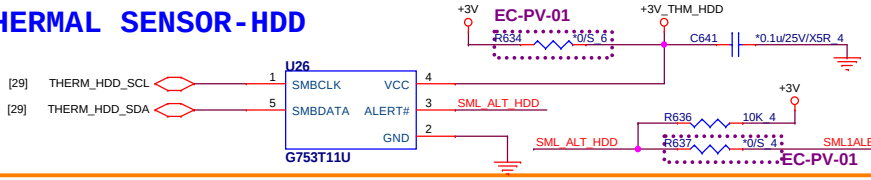
THERMAL SENSOR



Ambient

Slave Adress						
A6	A5	A4	A3	A2	A1	A0
1	0	0	1	0	0	0

THERMAL SENSOR-HDD



HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

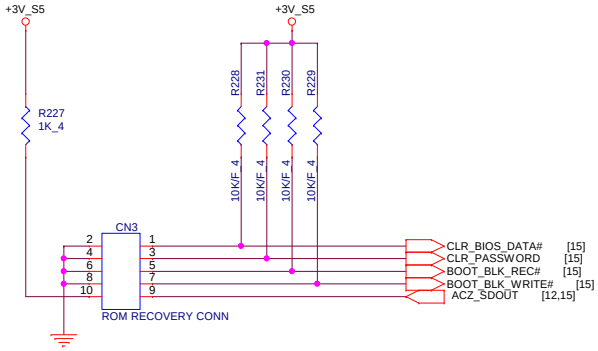
Size	Document Number	Rev
Custom	Thermal/Fan/LED	1A

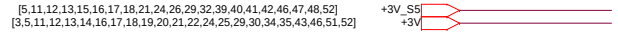
Date: Wednesday, March 09, 2016 Sheet 30 of 58

CLR_CMOS

Jumper	Pre-production	Production
BOOT_BLK_Recovery	X	X
BOOT_BLK_Enable	O	X

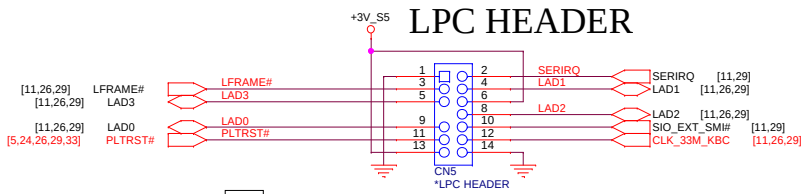
Jumper	Type
Pop	CLR_BIOS_DAT
Pop	CLR_PASSWD
Pop	BOOT_BLK_Recovery
Pop	BOOT_BLK_Enable





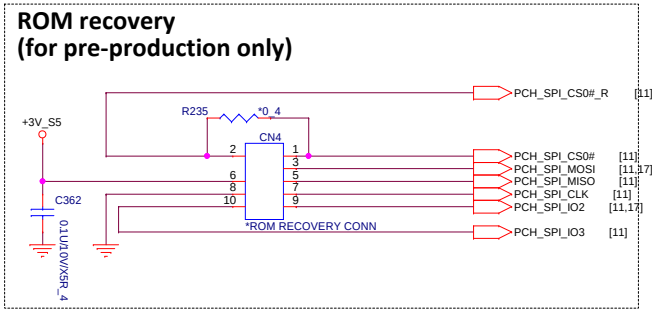
ON Chip select:Default:iinsatall (PROTO only)
CONN MINI JUMPER 2P FS (P2.0,H5.0)

LPC HEADER

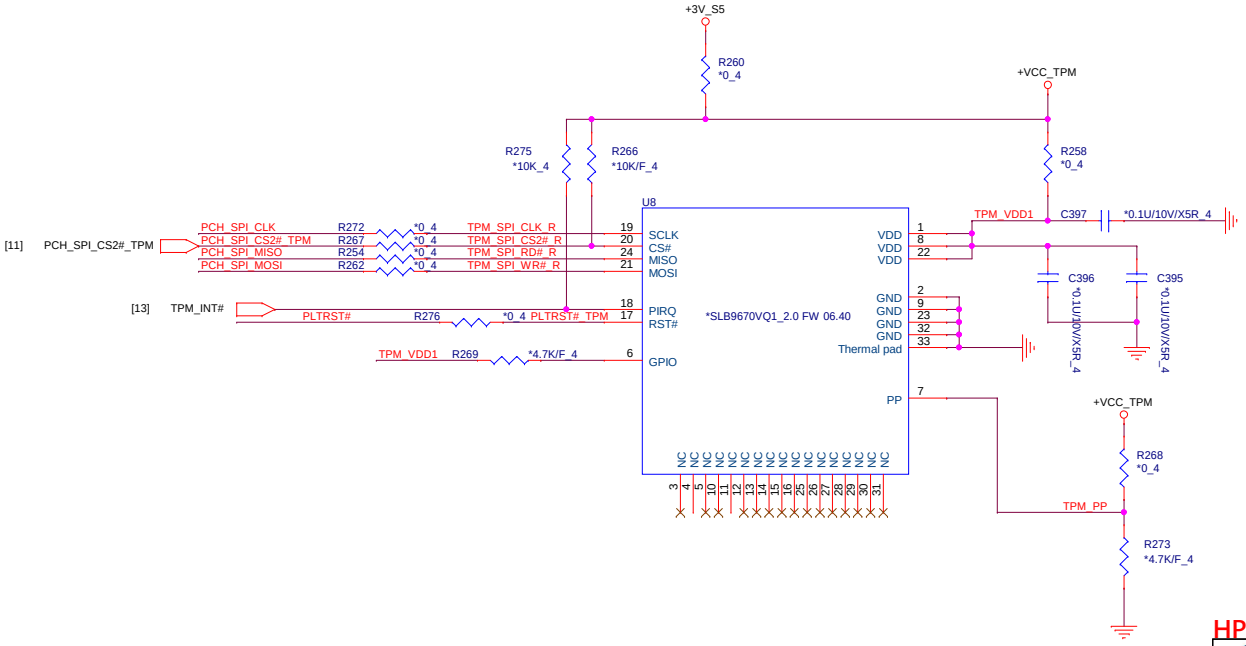


CLR_PASSWORD Default:install
CONN MINI JUMPER 2P FS (P2.0,H5.0)

ROM recovery (for pre-production only)



TPM (1.2 or 2.0)



HP Restricted Secret

Quanta Computer Inc.

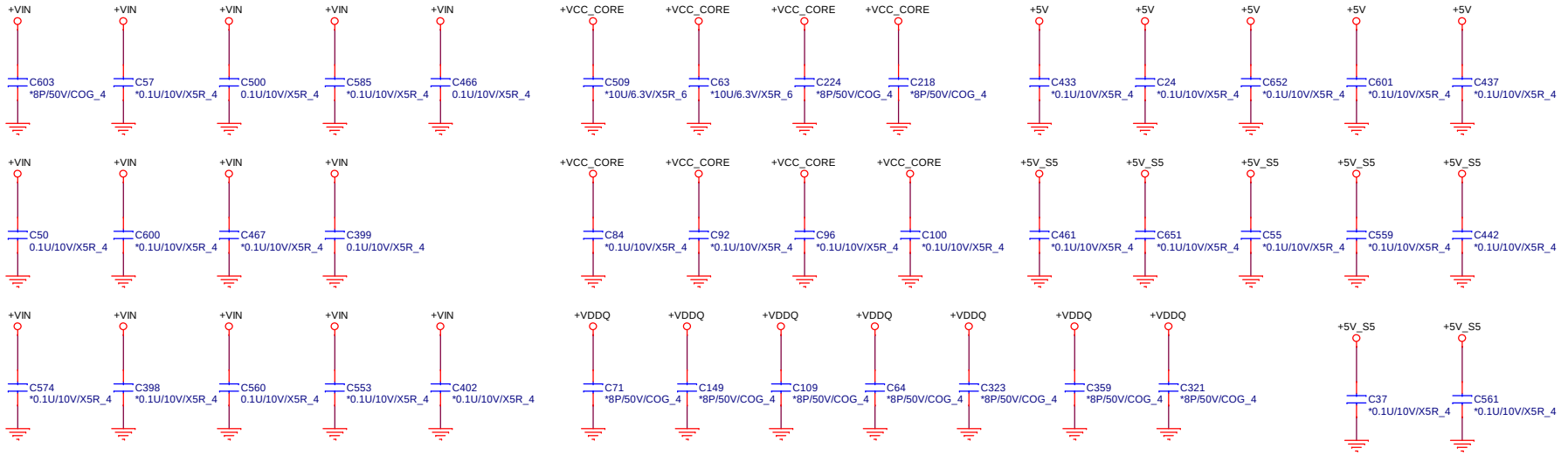
PROJECT: HP-Hawaii

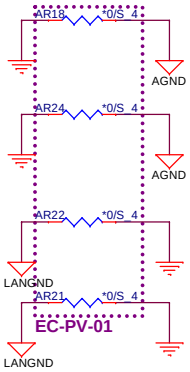
Size	Document Number	Rev
Custom	Jumper/LPC Header	1A

Date: Friday, December 18, 2015 Sheet 31 of 58

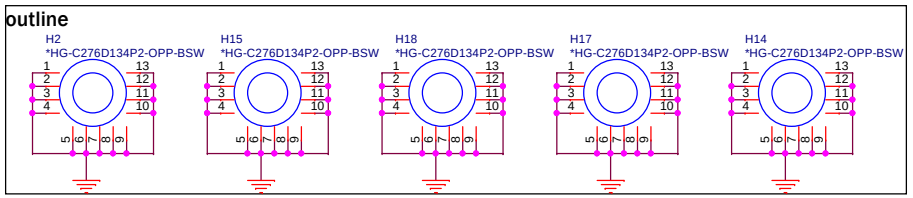
RF/EMI Suggestion

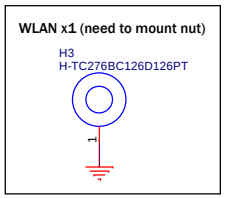
[4,7,18,19,40] +VDDQ
[6,43,44] +VCC_CORE
[30,39,40,41,43,44,45,46,47,48,49,50,51,52] +VIN

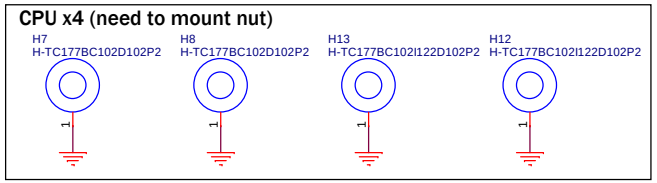


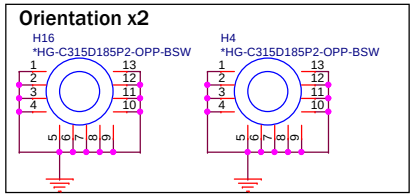


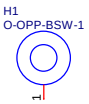
Holes

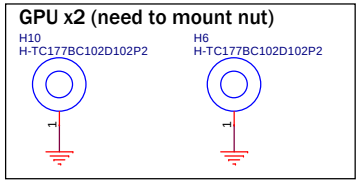


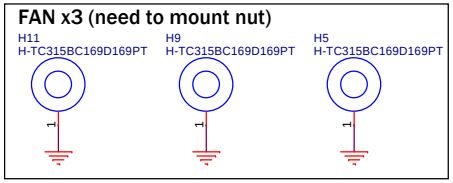


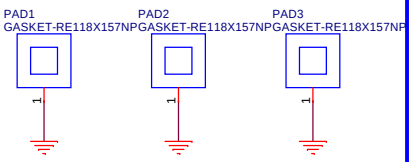


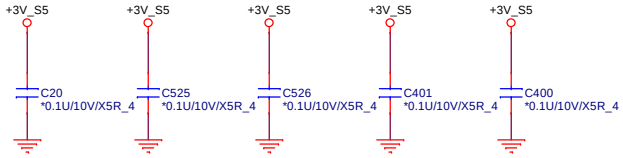












HP Restricted Secret

Quanta Computer Inc.
PROJECT: HP-Hawaii

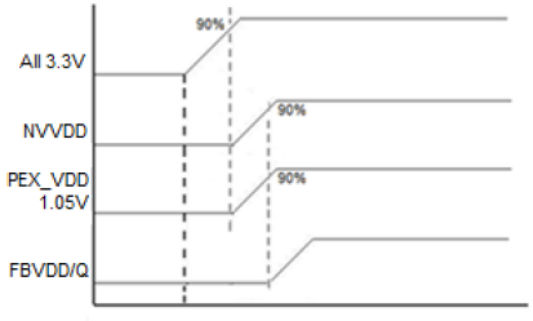
Size	Document Number	Rev
Custom	EMI/RF/Holes	1A
Date: Thursday, March 17, 2016	Sheet 32 of 58	

[34,35,52] +1.05V_VGA
[35,36,37,51,52] +3.3V_VGA

PEX_IOVDD + PEX_IOVDDQ = 1.042A

PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA

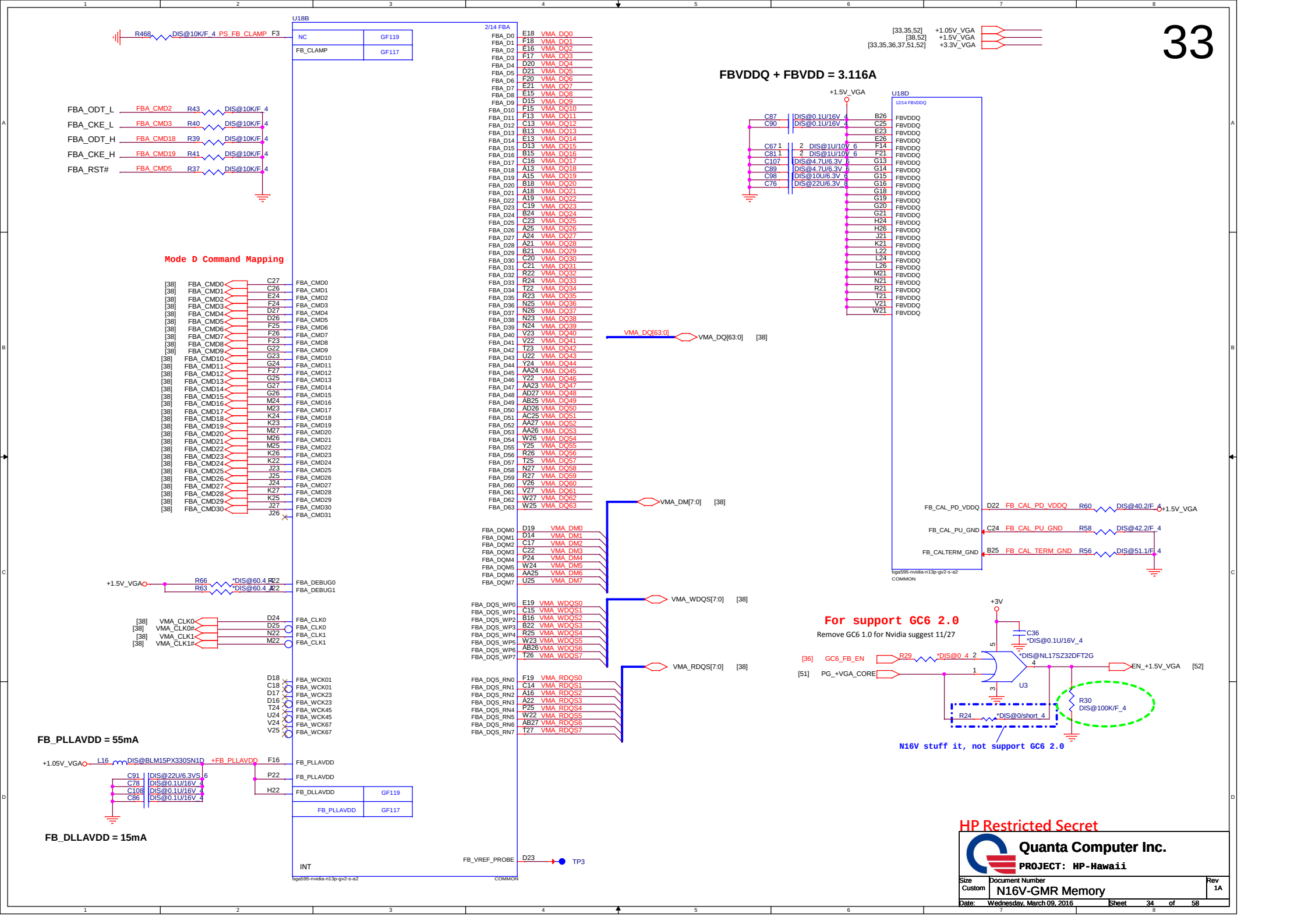
PEX_PLLVDD = 130mA

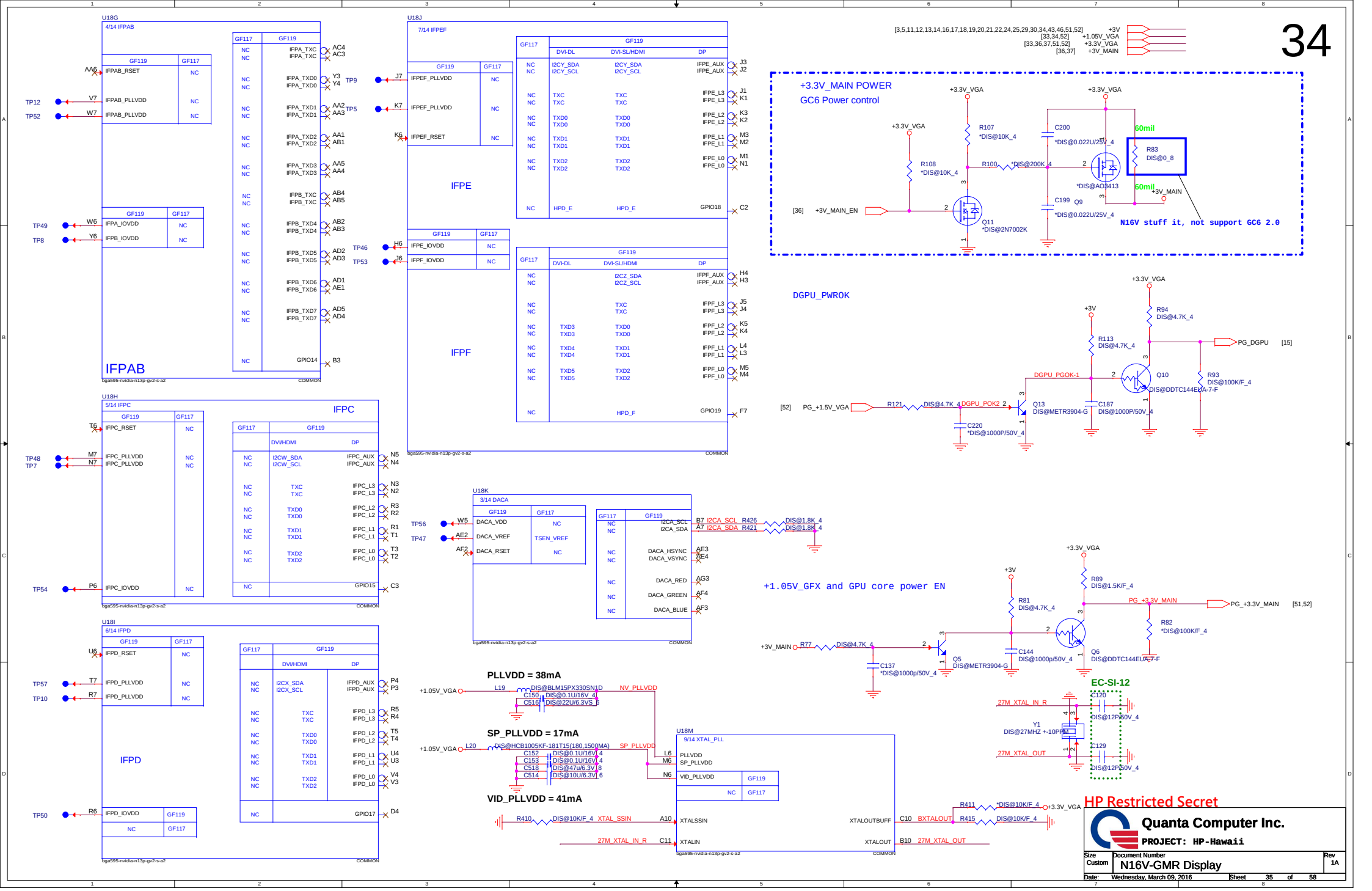


Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	N16V-GMR PCIE	1A

Date: Wednesday, March 09, 2016 Sheet 33 of 58


U18B
R468 DIS@10K/F_4 PS_FB_CLAMP F3
NC GF119
FB_CLAMP GF117
2/14 FBA
FBA_ODT_L FBA_CMD2 R43 DIS@10K/F_4
FBA_CKE_L FBA_CMD3 R40 DIS@10K/F_4
FBA_ODT_H FBA_CMD18 R39 DIS@10K/F_4
FBA_CKE_H FBA_CMD19 R41 DIS@10K/F_4
FBA_RST# FBA_CMD5 R37 DIS@10K/F_4
Mode D Command Mapping
FBA_CMD0 C27
FBA_CMD1 C26
FBA_CMD2 E24
FBA_CMD3 F24
FBA_CMD4 D27
FBA_CMD5 D26
FBA_CMD6 F25
FBA_CMD7 F26
FBA_CMD8 F23
FBA_CMD9 G22
FBA_CMD10 G23
FBA_CMD11 G24
FBA_CMD12 F27
FBA_CMD13 G25
FBA_CMD14 G27
FBA_CMD15 G26
FBA_CMD16 M24
FBA_CMD17 M23
FBA_CMD18 K24
FBA_CMD19 K23
FBA_CMD20 M27
FBA_CMD21 M26
FBA_CMD22 M25
FBA_CMD23 K26
FBA_CMD24 K22
FBA_CMD25 J23
FBA_CMD26 J25
FBA_CMD27 J24
FBA_CMD28 K27
FBA_CMD29 K25
FBA_CMD30 J27
FBA_CMD31 J26
+1.5V_VGA R66 *DIS@60.4 R22 FBA_DEBUG0
R63 *DIS@60.4 J22 FBA_DEBUG1
VMA_CLK0 D24 FBA_CLK0
VMA_CLK0# D25 FBA_CLK0
VMA_CLK1 N22 FBA_CLK1
VMA_CLK1# M22 FBA_CLK1
FBA_WCK01 D18
FBA_WCK01 C18
FBA_WCK23 D17
FBA_WCK23 D16
FBA_WCK45 T24
FBA_WCK45 U24
FBA_WCK67 V24
FBA_WCK67 V25
FB_PLLAVDD = 55mA
+1.05V_VGA L16 DIS@BLM15PX330SN1D +FB_PLLAVDD F16 FB_PLLAVDD
P22 FB_PLLAVDD
C91 DIS@22U/6.3VS_6
C78 DIS@0.1U/16V_4
C108 DIS@0.1U/16V_4
C86 DIS@0.1U/16V_4
H22 FB_DLLAVDD GF119
FB_PLLAVDD GF117
FB_DLLAVDD = 15mA
INT
bga595-nvidia-n13p-gv2-s-a2
COMMON
FBA_D0 E18 VMA_DQ0
FBA_D1 F18 VMA_DQ1
FBA_D2 E16 VMA_DQ2
FBA_D3 F17 VMA_DQ3
FBA_D4 D20 VMA_DQ4
FBA_D5 D21 VMA_DQ5
FBA_D6 F20 VMA_DQ6
FBA_D7 E21 VMA_DQ7
FBA_D8 E15 VMA_DQ8
FBA_D9 D15 VMA_DQ9
FBA_D10 F15 VMA_DQ10
FBA_D11 F13 VMA_DQ11
FBA_D12 C13 VMA_DQ12
FBA_D13 B13 VMA_DQ13
FBA_D14 E13 VMA_DQ14
FBA_D15 D13 VMA_DQ15
FBA_D16 B15 VMA_DQ16
FBA_D17 C16 VMA_DQ17
FBA_D18 A13 VMA_DQ18
FBA_D19 A15 VMA_DQ19
FBA_D20 B18 VMA_DQ20
FBA_D21 A18 VMA_DQ21
FBA_D22 A19 VMA_DQ22
FBA_D23 C19 VMA_DQ23
FBA_D24 B24 VMA_DQ24
FBA_D25 C23 VMA_DQ25
FBA_D26 A25 VMA_DQ26
FBA_D27 A24 VMA_DQ27
FBA_D28 A21 VMA_DQ28
FBA_D29 B21 VMA_DQ29
FBA_D30 C20 VMA_DQ30
FBA_D31 C21 VMA_DQ31
FBA_D32 R22 VMA_DQ32
FBA_D33 R24 VMA_DQ33
FBA_D34 T22 VMA_DQ34
FBA_D35 R23 VMA_DQ35
FBA_D36 N25 VMA_DQ36
FBA_D37 N26 VMA_DQ37
FBA_D38 N23 VMA_DQ38
FBA_D39 N24 VMA_DQ39
FBA_D40 V23 VMA_DQ40
FBA_D41 V22 VMA_DQ41
FBA_D42 T23 VMA_DQ42
FBA_D43 U22 VMA_DQ43
FBA_D44 Y24 VMA_DQ44
FBA_D45 AA24 VMA_DQ45
FBA_D46 Y22 VMA_DQ46
FBA_D47 AA23 VMA_DQ47
FBA_D48 AD27 VMA_DQ48
FBA_D49 AB25 VMA_DQ49
FBA_D50 AD26 VMA_DQ50
FBA_D51 AC25 VMA_DQ51
FBA_D52 AA27 VMA_DQ52
FBA_D53 AA26 VMA_DQ53
FBA_D54 W26 VMA_DQ54
FBA_D55 Y25 VMA_DQ55
FBA_D56 R26 VMA_DQ56
FBA_D57 T25 VMA_DQ57
FBA_D58 N27 VMA_DQ58
FBA_D59 R27 VMA_DQ59
FBA_D60 V26 VMA_DQ60
FBA_D61 V27 VMA_DQ61
FBA_D62 W27 VMA_DQ62
FBA_D63 W25 VMA_DQ63
VMA_DQ[63:0]
VMA_DQ[63:0] [38]
FBA_DQM0 D19 VMA_DM0
FBA_DQM1 D14 VMA_DM1
FBA_DQM2 C17 VMA_DM2
FBA_DQM3 C22 VMA_DM3
FBA_DQM4 P24 VMA_DM4
FBA_DQM5 W24 VMA_DM5
FBA_DQM6 AA25 VMA_DM6
FBA_DQM7 U25 VMA_DM7
VMA_DM[7:0] [38]
FBA_DQS_WP0 E19 VMA_WDQS0
FBA_DQS_WP1 C15 VMA_WDQS1
FBA_DQS_WP2 B16 VMA_WDQS2
FBA_DQS_WP3 B22 VMA_WDQS3
FBA_DQS_WP4 R25 VMA_WDQS4
FBA_DQS_WP5 W23 VMA_WDQS5
FBA_DQS_WP6 AB26 VMA_WDQS6
FBA_DQS_WP7 T26 VMA_WDQS7
VMA_WDQS[7:0] [38]
FBA_DQS_RN0 F19 VMA_RDQS0
FBA_DQS_RN1 C14 VMA_RDQS1
FBA_DQS_RN2 A16 VMA_RDQS2
FBA_DQS_RN3 A22 VMA_RDQS3
FBA_DQS_RN4 P25 VMA_RDQS4
FBA_DQS_RN5 W22 VMA_RDQS5
FBA_DQS_RN6 AB27 VMA_RDQS6
FBA_DQS_RN7 T27 VMA_RDQS7
VMA_RDQS[7:0] [38]
FB_VREF_PROBE D23 TP3
[33,35,52] +1.05V_VGA
[38,52] +1.5V_VGA
[33,35,36,37,51,52] +3.3V_VGA
FBVDDQ + FBVDD = 3.116A
+1.5V_VGA
U18D
12/14 FBVDDQ
C87 DIS@0.1U/16V_4
C90 DIS@0.1U/16V_4
C67 DIS@1U/10V_6
C81 DIS@1U/10V_6
C107 DIS@4.7U/6.3V_6
C89 DIS@4.7U/6.3V_6
C98 DIS@10U/6.3V_6
C76 DIS@22U/6.3V_6
B26 C25 E23 E26 F14 F21 G13 G14 G15 G16 G18 G19 G20 G21 H24 H26 J21 K21 L22 L24 L26 M21 N21 R21 T21 V21 W21 FBVDDQ
FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ R60 DIS@40.2/F_4 +1.5V_VGA
FB_CAL_PU_GND C24 FB_CAL_PU_GND R58 DIS@42.2/F_4
FB_CALTERM_GND B25 FB_CAL_TERM_GND R56 DIS@51.1/F_4
bga595-nvidia-n13p-gv2-s-a2
COMMON
For support GC6 2.0
Remove GC6 1.0 for Nvidia suggest 11/27
+3V
C36 *DIS@0.1U/16V_4
[36] GC6_FB_EN R29 *DIS@0_4
[51] PG_+VGA_CORE
*DIS@NL17SZ32DFT2G
U3
EN_+1.5V_VGA [52]
R30 DIS@100K/F_4
R24 *DIS@0/short_4
N16V stuff it, not support GC6 2.0
HP Restricted Secret
Quanta Computer Inc.
PROJECT: HP-Hawaii
Size Custom
Document Number N16V-GMR Memory
Rev 1A
Date: Wednesday, March 09, 2016
Sheet 34 of 58


U18G
4/14 IFPAB
IFPAB
IFPA_RSET
IFPAB_PLLVDD
IFPB_IOVDD
IFPA_TXC
IFPA_TXD0
IFPA_TXD1
IFPA_TXD2
IFPA_TXD3
IFPB_TXC
IFPB_TXD4
IFPB_TXD5
IFPB_TXD6
IFPB_TXD7
GPIO14
U18J
7/14 IFPEF
IFPE
IFPF
IFPEF_PLLVDD
IFPEF_RSET
IFPE_IOVDD
IFPF_IOVDD
HPD_E
HPD_F
GPIO18
GPIO19
U18H
5/14 IFPC
IFPC
IFPC_RSET
IFPC_PLLVDD
IFPC_IOVDD
GPIO15
U18I
6/14 IFPD
IFPD
IFPD_RSET
IFPD_PLLVDD
IFPD_IOVDD
GPIO17
U18K
3/14 DACA
DACA_VDD
DACA_VREF
DACA_RSET
TSEN_VREF
DACA_HSYNC
DACA_VSYNC
DACA_RED
DACA_GREEN
DACA_BLUE
I2CA_SCL
I2CA_SDA
U18M
9/14 XTAL_PLL
XTALSSIN
XTALIN
XTALOUTBUFF
XTALOUT
+3.3V_MAIN POWER
GC6 Power control
N16V stuff it, not support GC6 2.0
DGPU_PWROK
+1.05V_GFX and GPU core power EN
PLLVDD = 38mA
SP_PLLVDD = 17mA
VID_PLLVDD = 41mA
EC-SI-12
HP Restricted Secret
Quanta Computer Inc.
PROJECT: HP-Hawaii
N16V-GMR Display
Size Custom
Rev 1A
Date: Wednesday, March 09, 2016
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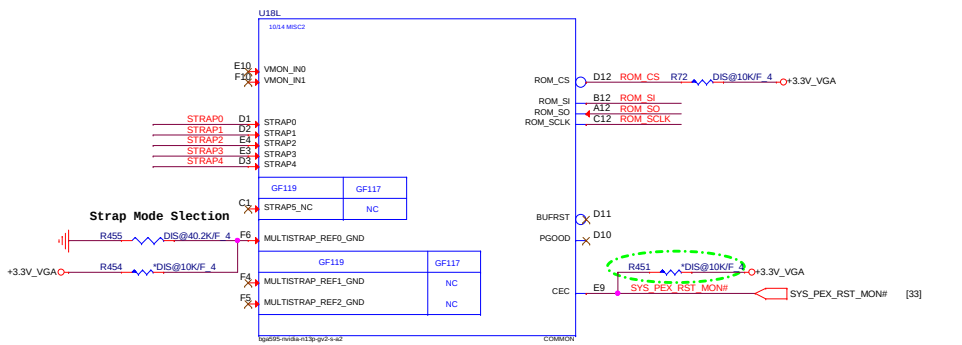
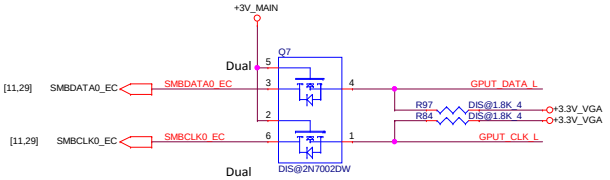
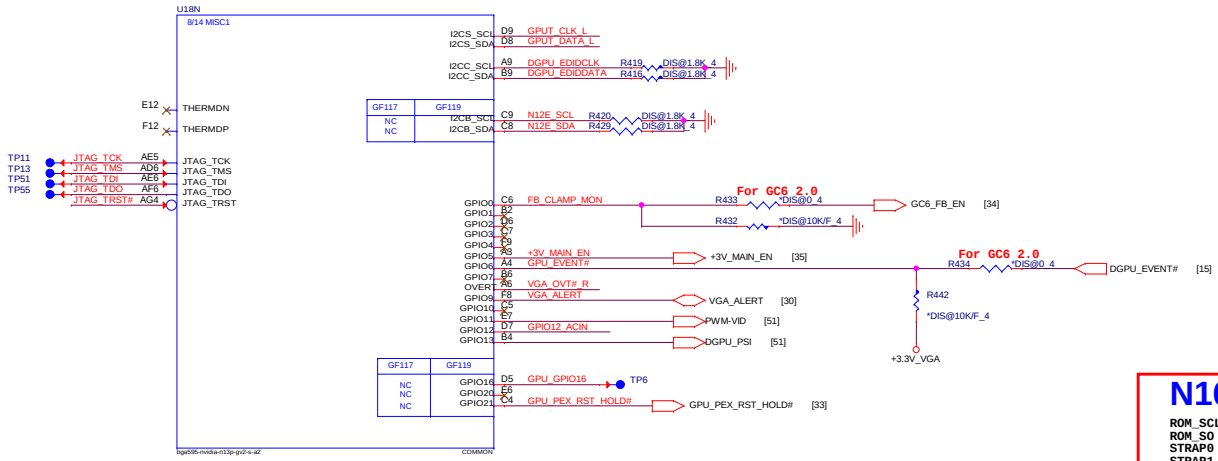
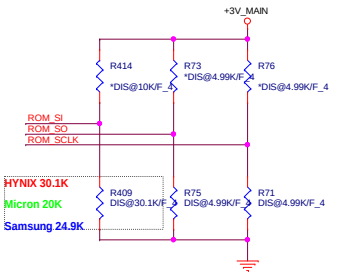
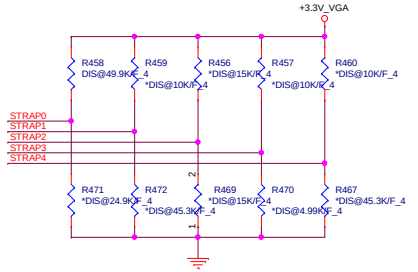


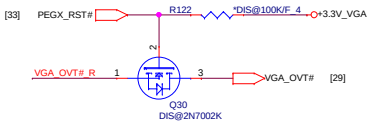


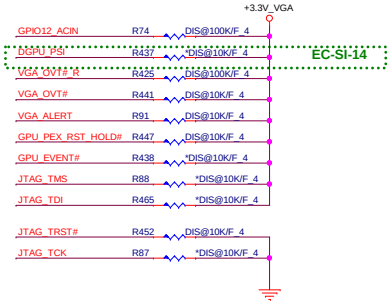
[33,35,37,51,52] +3.3V_VGA
[35,37] +3V_MAIN











GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor (GC6 1.0)
0	OUT	GC6_FB_EN	GC6 FB Enable (GC6 2.0)
5	OUT	+3V_MAIN_EN	Enable GC6 +3V_MAIN
6	OUT	FB_CLAMP_REQ#	Active low FB Clamp toggle request (GC6 1.0)
6	IN	DGPU_EVENT#	DGPU EVENT from CPU (GC6 2.0)
8	OUT	VGA_OVT#	ACTIVE LOW THERMAL OVER TEMP
9	OUT	ALERT	ACTIVE LOW THERMAL ALERT
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

N16V-GMR1 DID=0x134F

GB2B-64

```
ROM_SCLK = Stuff 4.99K pull down
ROM_SO   = Stuff 4.99K pull down
STRAP0   = Stuff 49.9K pull up
STRAP1   = NC
STRAP2   = NC
STRAP3   = NC
STRAP4   = NC
ROM_SI   = VRAM Configuration follow below table
```

Logical Strap Bit Mapping

	PU-VDD	PD	QCI P/N
4.99K	1000	0000	CS24992FB26
10K	1001	0001	CS31002FB26
15K	1010	0010	CS31502FB24
20K	1011	0011	CS32002FB29
24.9K	1100	0100	CS32492FB16
30.1K	1101	0101	CS33012FB18
34.8K	1110	0110	CS33482FB06
45.3K	1111	0111	CS34532FB18

ROM_SI

RAMCFG [3:0]	DESCRIPTION 1.5V DDR3	Vendor	Vendor P/N	ROM_SI	STN B/S	Configuration
	256Mx16					
0011	DDR3 256Mx16, 64bit, 4Gb,1000MHz	Micron	MT41J256M16LY-091G:N	PD 20K ohm	AKD59GSTL02	Single Rank or Single Rank stuffing for Dual Rank
1001	DDR3 256Mx16, 64bit, 4Gb,1000MHz	HYNIX	H5TC4G63CFR-N0C	PD 30.1K ohm	AKD5PZDTW03	
1000	DDR3 256Mx16, 64bit, 4Gb,1000MHz	Samsung	K4W4G1646E-BC1A	PD 24.9K ohm	AKD5PGDT502	

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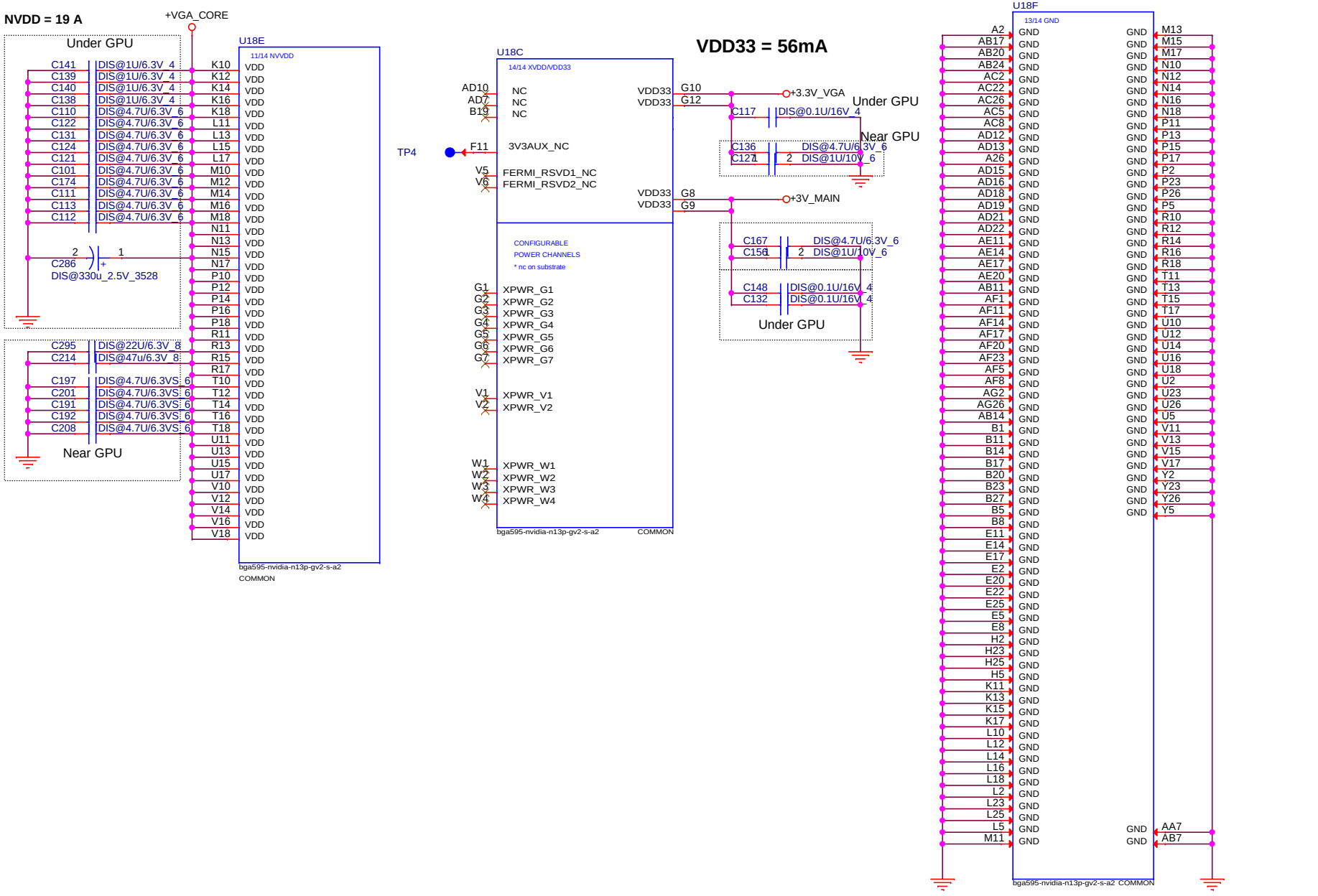
Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	N16V-GMR GPIO/Strap	1A

Date: Monday, March 21, 2016 Sheet 36 of 58



HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	N16V-GMR Power/GND	1A

Date: Wednesday, March 09, 2016 Sheet 37 of 58

CHANNEL A: 2048MB DDR3X16

[34] VMA_DQ[63..0]
[34] VMA_DM[7..0]
[34] VMA_WDQS[7..0]
[34] VMA_RDQS[7..0]

[33,34,35,52] +1.05V_VGA
[34,52] +1.5V_VGA

VRAM2 / VRAM4 / VRAM1 / VRAM3

SDRAM DDR3 96-BALL
DIS@VRAM _DDR3_256MX16

Should be 240 Ohms +-1%

R42 DIS@243/F_4
R393 DIS@243/F_4
R44 DIS@243/F_4
R392 DIS@243/F_4

+1.5V_VGA

R45 DIS@162/F_4
VMA_CLK0 / VMA_CLK0#

162_1% ohm
CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

R35 DIS@1.33K/F_4
R34 DIS@1.33K/F_4
C43 DIS@0.1u/16V_4
R390 DIS@1.33K/F_4
R391 DIS@1.33K/F_4
C483 DIS@0.1u/16V_4

[34] FBA_CMD17 → TP1
[34] FBA_CMD1 → TP42
10/14 modify

R46 DIS@162/F_4
VMA_CLK1 / VMA_CLK1#

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R388 DIS@1.33K/F_4
R389 DIS@1.33K/F_4
C477 DIS@0.1u/16V_4
R32 DIS@1.33K/F_4
R33 DIS@1.33K/F_4
C41 DIS@0.1u/16V_4

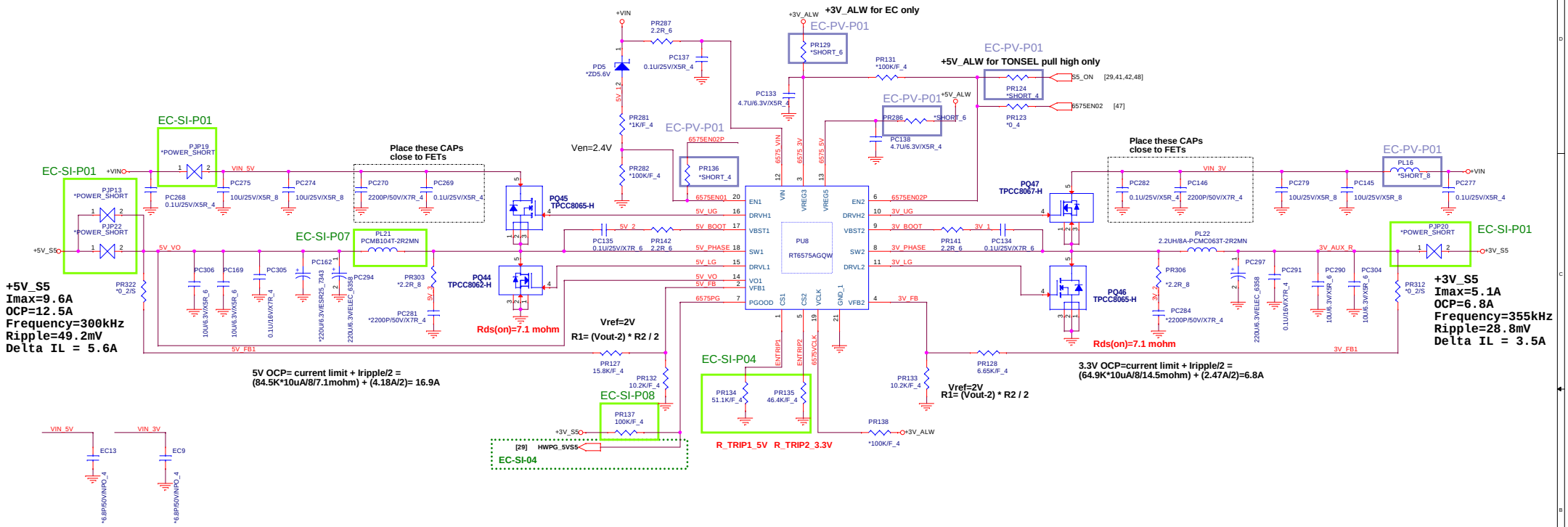
C484 C476 C45 C491 DIS@1u/10V_4
C478 C496 C46 C40 C56 C486 DIS@1u/10V_4
C39 C52 C54 C48 C44 C49 C479 C59 DIS@1u/10V_4
C42 C485 C51 C493 C492 C487 C497 DIS@0.1u/16V_4
C47 C474 C480 C490 C498 DIS@0.1u/16V_4
DIS@10u/6.3V_6

HP Restricted Secret

Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	N16V-GMR DDR3 VRAM	1A

Date: Wednesday, March 09, 2016 Sheet 38 of 58



L/S Mosfet parameter

MOSFET	Package	ID (Ta=25C)	Rds_on_max
TPCC8067-H	DFN3x3	9A	26m
TPCC8062-H	DFN3x3	27A	7.1m

Power On sequencing

EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON

HP Restricted Secret

Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	System +3V_S5/+5V_S5	1A

Date: Wednesday, March 09, 2016 Sheet 39 of 58

+VDDQ [4,7,18,19,32]

+VDDQ
Imax= 9.7A
OCP=12.7A
Frequency=400kHz
Ripple=31.4mV
Delta IL = 2.8 A

+0.6V_DDR_VTT (0.75A)
PEAK :0.75A

PU7 RT8231BGQW
PQ11 TPCA8064-H
PQ13 TPCA8059-H
PL7 1UH/11A(PCMC063T-1R0MN)
PL5 *SHORT_8

VO=(0.675(R1+R2)/R2)

+2.5V_S3 +/- 5%
Imax = 1A
OCP = 3A
Pd: 0.8W
Ripple=10mV

PU5 G9661-25ADJF12U

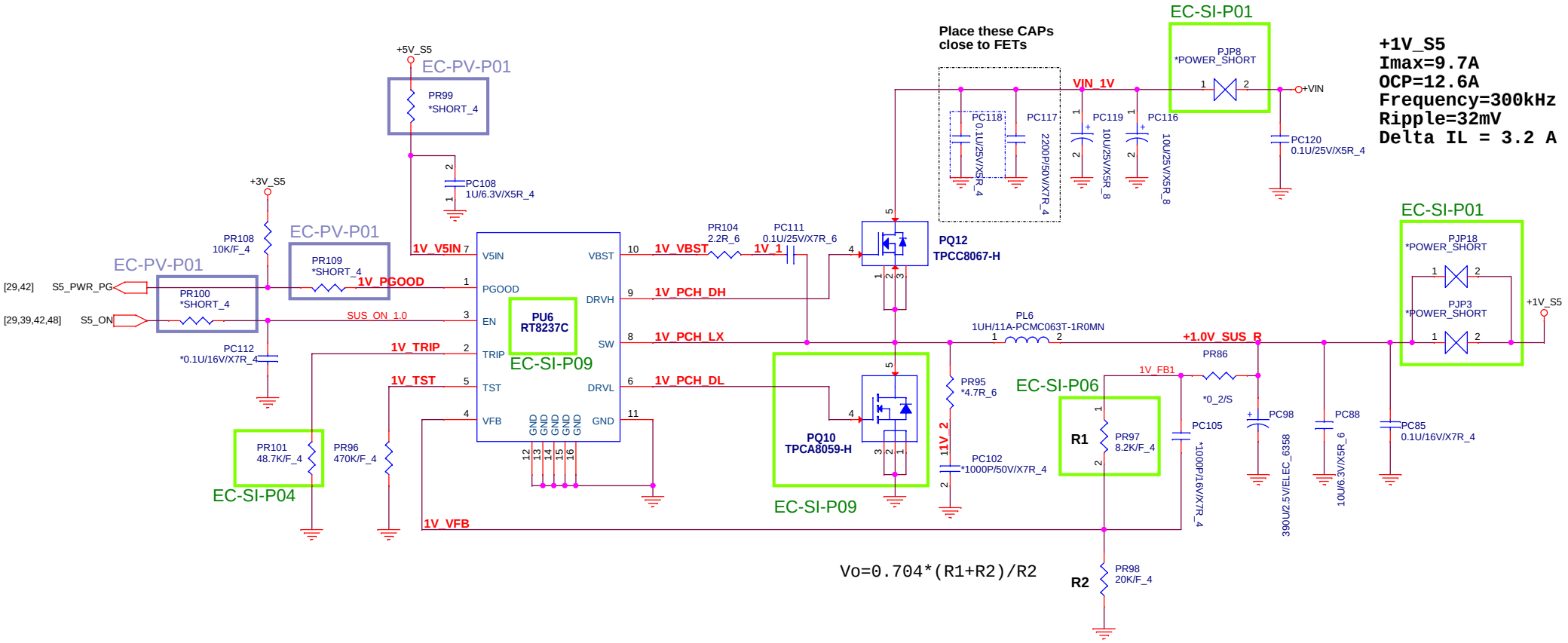
R1 PR92 21.5K/F_4
R2 PR93 10K/F_4

Vout =0.8(1+R1/R2)

HP Restricted Secret

Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	DDR4 +VDDQ/+2.5V_S3	1A
Date: Wednesday, March 09, 2016	Sheet 40 of 58	

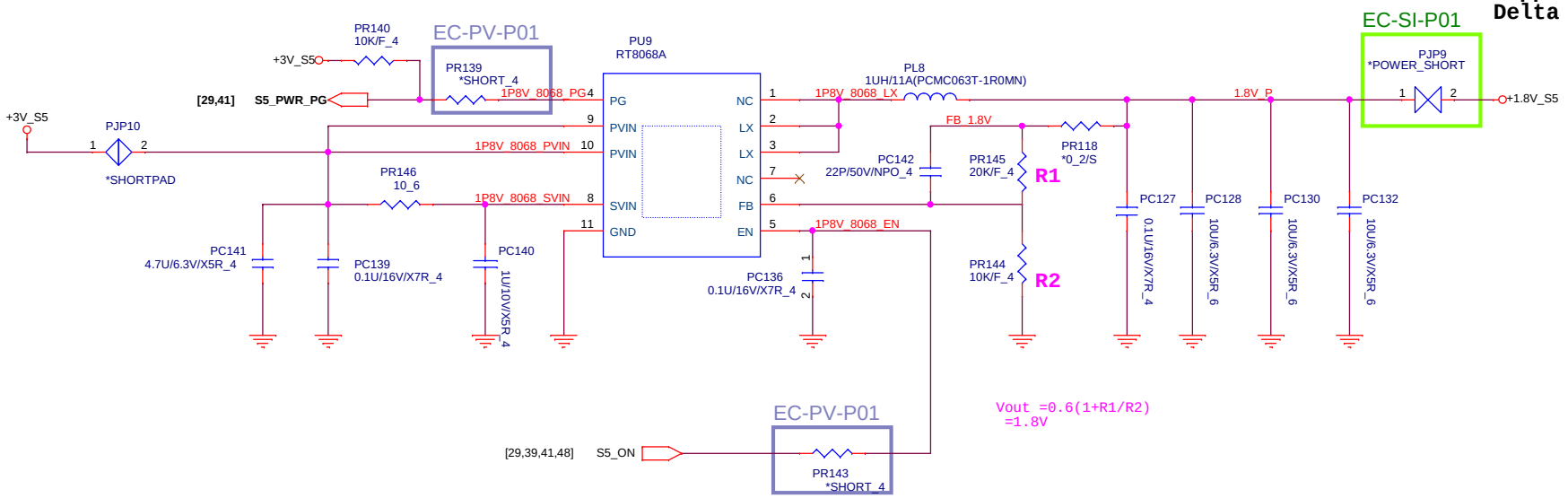


HP Restricted Secret

Quanta Computer Inc.		
PROJECT: HP-Hawaii		
Size B	Document Number +1V_S5	Rev 1A
Date: Wednesday, March 09, 2016	Sheet 41 of 58	

V1P8A (RT8068A)

+1.8V_S5
Imax=1.2A
OCP=4A
Frequency=1MHz
Ripple=12mV
Delta IL = 0.8A



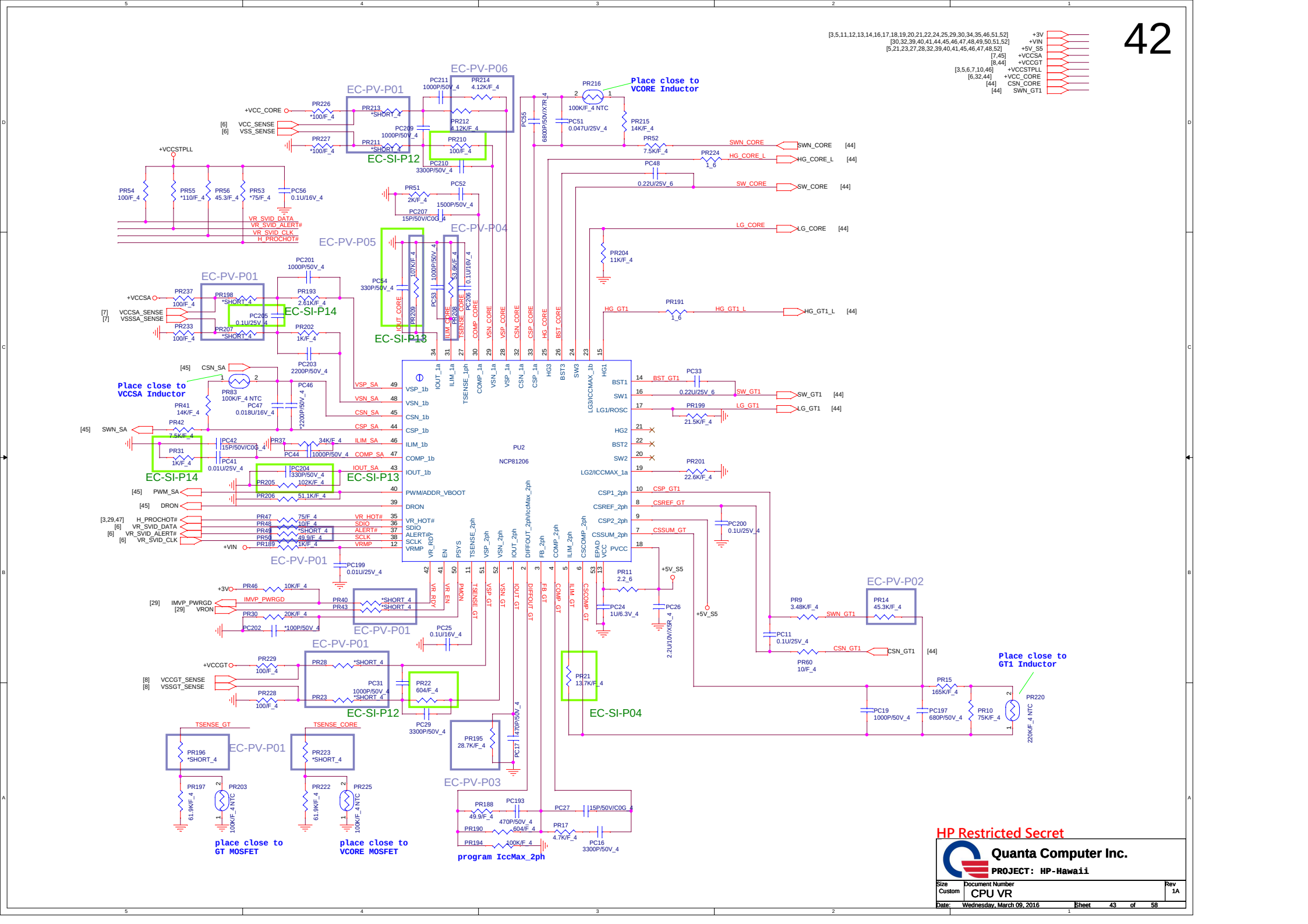
HP Restricted Secret

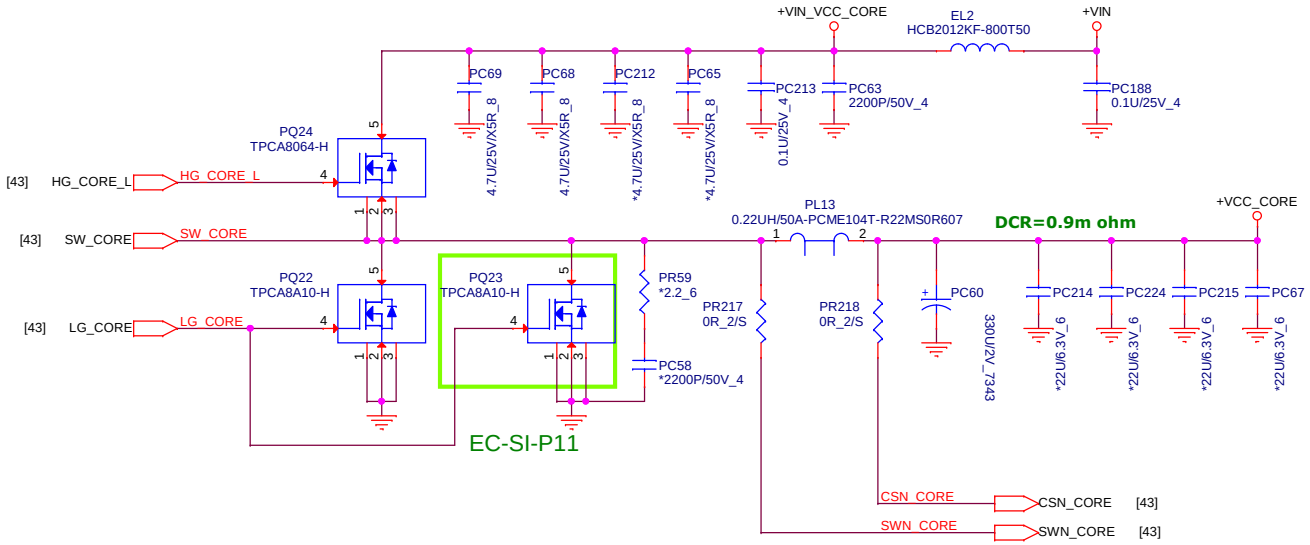
Quanta Computer Inc.

PROJECT: HP-Hawaii

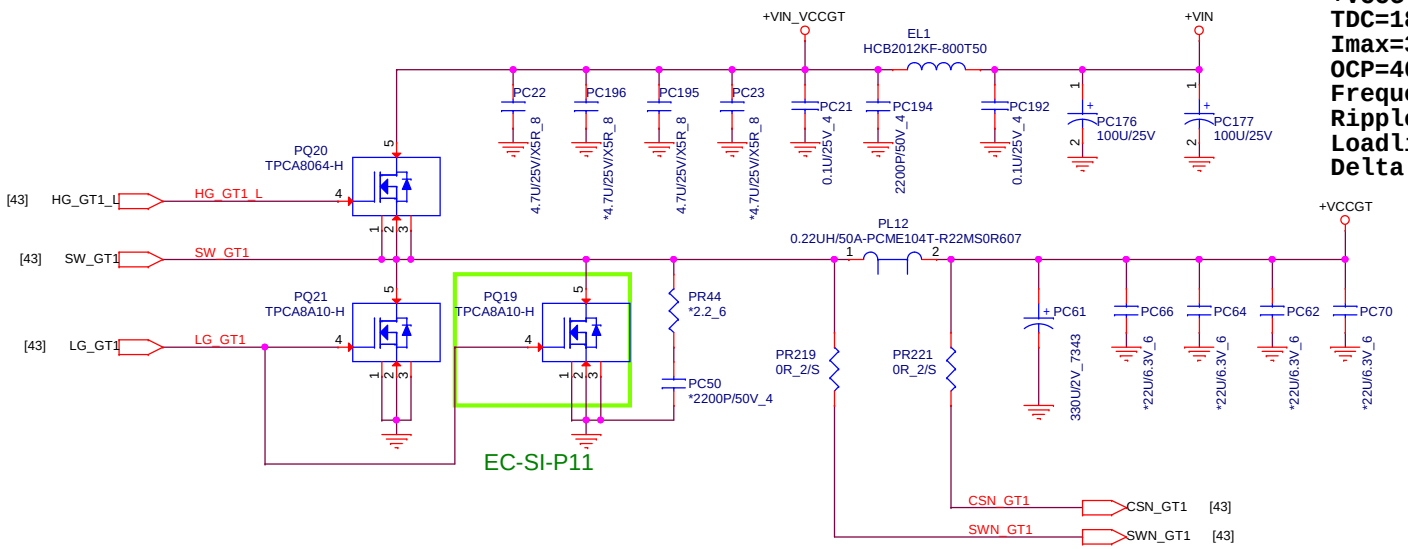
Size	Document Number	Rev
B	+1.8V_S5	1A

Date: Wednesday, March 09, 2016 Sheet 42 of 58


[3,5,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,46,51,52] +3V
[30,32,39,40,41,44,45,46,47,48,49,50,51,52] +VIN
[5,21,23,27,28,32,39,40,41,45,46,47,48,52] +5V_S5
[7,45] +VCCSA
[8,44] +VCCGT
[3,5,6,7,10,46] +VCCSTPLL
[6,32,44] +VCC_CORE
[44] CSN_CORE
[44] SWN_GT1
EC-PV-P06
EC-PV-P01
EC-SI-P12
EC-PV-P04
EC-PV-P05
EC-SI-P13
EC-SI-P14
EC-SI-P04
EC-PV-P02
EC-PV-P03
Place close to VCORE Inductor
Place close to VCCSA Inductor
Place close to GT1 Inductor
place close to GT MOSFET
place close to VCORE MOSFET
program IccMax_2ph
PU2
NCP81206
+VCC_CORE
VCC_SENSE
VSS_SENSE
+VCCSTPLL
VR_SVID_DATA
VR_SVID_ALERT#
VR_SVID_CLK
H_PROCHOT#
+VCCSA
VCCSA_SENSE
VSSSA_SENSE
CSN_SA
SWN_SA
PWM_SA
DRON
VR_HOT#
VR_SVID_DATA
VR_SVID_ALERT#
VR_SVID_CLK
+VIN
+3V
IMVP_PWRGD
VRON
+VCCGT
VCCGT_SENSE
VSSGT_SENSE
TSENSE_GT
TSENSE_CORE
SWN_CORE
HG_CORE_L
SW_CORE
LG_CORE
HG_GT1
HG_GT1_L
BST_GT1
SW_GT1
LG_GT1
CSP_GT1
CSREF_GT
CSSUM_GT
CSN_GT1
+5V_S5
VSP_SA
VSN_SA
CSN_SA
CSP_SA
ILIM_SA
COMP_SA
IOUT_SA
VRMP
VR_HOT#
SDIO
ALERT#
SCLK
VR_RDY
EN
PSYS
TSENSE_2ph
VSP_2ph
VSN_2ph
IOUT_2ph
DIFFOUT_2ph/IccMax_2ph
FB_2ph
COMP_2ph
ILIM_2ph
CSCOMP_2ph
EPAD VCC
PVCC
CSP1_2ph
CSREF_2ph
CSP2_2ph
CSSUM_2ph
LG3/ICCMAX_1b
LG1/ROSC
LG2/ICCMAX_1a
BST1
SW1
HG2
BST2
SW2
HG1
HG3
BST3
SW3
VSP_1b
VSN_1b
CSN_1b
CSP_1b
ILIM_1b
COMP_1b
IOUT_1b
PWM/ADDR_VBOOT
IOUT_1a
ILIM_1a
TSENSE_1ph
COMP_1a
VSN_1a
VSP_1a
CSN_1a
CSP_1a
PR83 100K/F_4 NTC
PR216 100K/F_4 NTC
PR220 220K/F_4 NTC
PR196 *SHORT_4
PR223 *SHORT_4
PR195 28.7K/F_4
PR21 13.7K/F_4
PR197 61.9K/F_4
PR222 61.9K/F_4
PR203 100K/F_4 NTC
PR225 100K/F_4 NTC
PC193 470P/50V_4
PC17 470P/50V_4
PC29 3300P/50V_4
PC16 3300P/50V_4
PC27 15P/50V/C0G_4
PR188 49.9/F_4
PR190 604/F_4
PR194 100K/F_4
PR17 4.7K/F_4
PC19 1000P/50V_4
PC197 680P/50V_4
PR10 75K/F_4
PR15 165K/F_4
PC11 0.1U/25V_4
PR60 10/F_4
PR9 3.48K/F_4
PR14 45.3K/F_4
PC200 0.1U/25V_4
PR11 2.2_6
PC24 1U/6.3V_4
PC26 2.2U/10V/X5R_4
PC199 0.01U/25V_4
PC25 0.1U/16V_4
PR46 10K/F_4
PR40 *SHORT_4
PR43 *SHORT_4
PR30 20K/F_4
PC202 *100P/50V_4
PR229 100/F_4
PR28 *SHORT_4
PR23 *SHORT_4
PC31 1000P/50V_4
PR228 100/F_4
PR22 604/F_4
PR54 100/F_4
PR55 *110/F_4
PR56 45.3/F_4
PR53 *75/F_4
PC56 0.1U/16V_4
PR51 2K/F_4
PC52 1500P/50V_4
PC207 15P/50V/C0G_4
PC54 330P/50V_4
PC53 1000P/50V_4
PR208 53.6K/F_4
PC206 0.1U/16V_4
PR209 107K/F_4
PC201 1000P/50V_4
PR237 100/F_4
PR198 *SHORT_4
PR193 2.61K/F_4
PC205 0.1U/25V_4
PR233 100/F_4
PR207 *SHORT_4
PR202 1K/F_4
PC203 2200P/50V_4
PC46 *2200P/50V_4
PR41 14K/F_4
PC47 0.018U/16V_4
PR42 7.5K/F_4
PC42 15P/50V/C0G_4
PR37 34K/F_4
PC44 1000P/50V_4
PR31 1K/F_4
PC41 0.01U/25V_4
PC204 330P/50V_4
PR205 102K/F_4
PR206 51.1K/F_4
PR47 75/F_4
PR48 10/F_4
PR49 *SHORT_4
PR50 49.9/F_4
PR189 1K/F_4
PR213 *SHORT_4
PR211 *SHORT_4
PR209 1000P/50V_4
PC211 1000P/50V_4
PR214 4.12K/F_4
PR212 4.12K/F_4
PR210 100/F_4
PC210 3300P/50V_4
PC55 6800P/50V/X7R_4
PC51 0.047U/25V_4
PR215 14K/F_4
PR52 7.5K/F_4
PR224 1_6
PC48 0.22U/25V_6
PR204 11K/F_4
PR191 1_6
PC33 0.22U/25V_6
PR199 21.5K/F_4
PR201 22.6K/F_4
VR_HOT
SDIO
ALERT
SCLK
VRMP
PWMON
TSENSE GT
VSP GT
VSN GT
IOUT GT
DIFFOUT GT
FB GT
COMP GT
ILIM GT
CSCOMP GT
VR RDY
VR EN
IMVP_PWRGD
VRON
[6] VCC_SENSE
[6] VSS_SENSE
[7] VCCSA_SENSE
[7] VSSSA_SENSE
[45] CSN_SA
[45] SWN_SA
[45] PWM_SA
[45] DRON
[3,29,47] H_PROCHOT#
[6] VR_SVID_DATA
[6] VR_SVID_ALERT#
[6] VR_SVID_CLK
[29] IMVP_PWRGD
[29] VRON
[8] VCCGT_SENSE
[8] VSSGT_SENSE
[44] SWN_CORE
[44] HG_CORE_L
[44] SW_CORE
[44] LG_CORE
[44] HG_GT1_L
[44] SW_GT1
[44] LG_GT1
[44] CSN_GT1
HP Restricted Secret
Quanta Computer Inc.
PROJECT: HP-Hawaii
Size Custom
Document Number CPU VR
Rev 1A
Date: Wednesday, March 09, 2016
Sheet 43 of 58



+VCC_CORE
TDC=21A
Imax=29A
OCP=36A
Frequency=450kHz
Ripple=13mV
Loadline: -2.4m ohm
Delta IL = 9.6A



+VCCGT
TDC=18A
Imax=31A
OCP=40A
Frequency=450kHz
Ripple=13mV
Loadline: -3.1m ohm
Delta IL = 9.6A

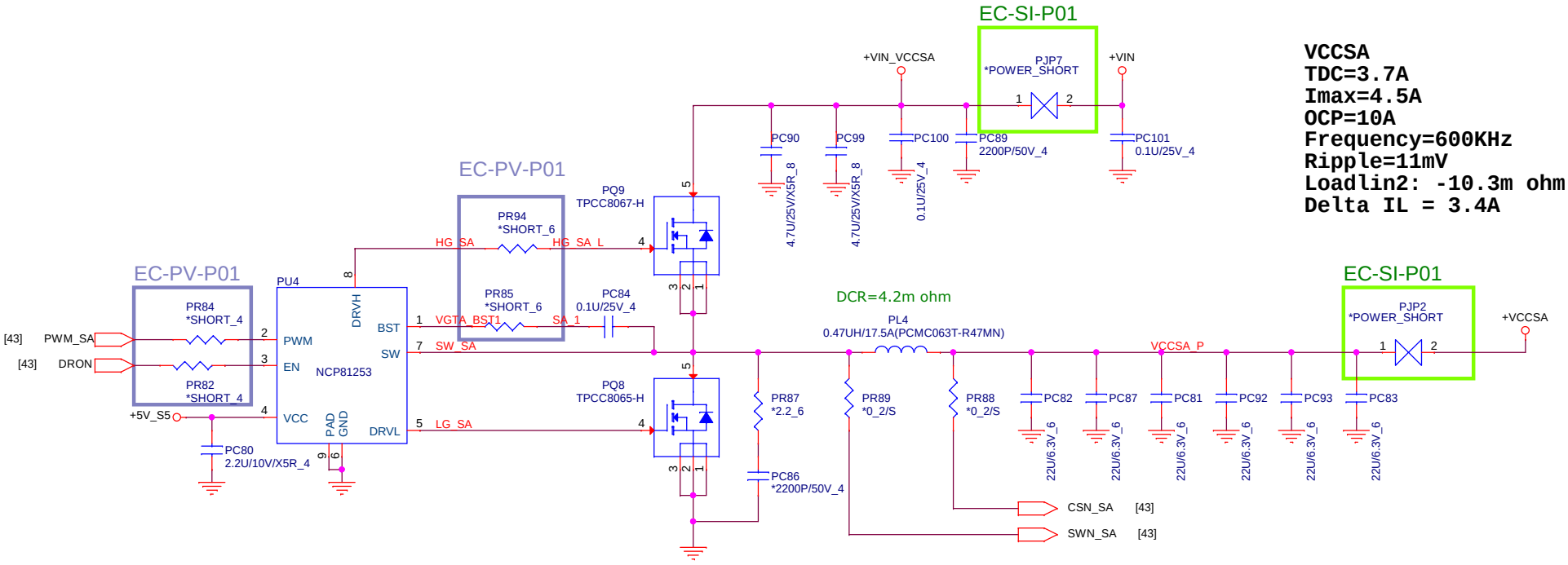
Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
B	CPU +VCC_CORE/+VCCGT	1A

Date: Wednesday, March 09, 2016 Sheet 44 of 58

[30,32,39,40,41,43,44,46,47,48,49,50,51,52] +VIN
[5,21,23,27,28,32,39,40,41,43,46,47,48,52] +5V_S5
[7,43] +VCCSA

VCCSA

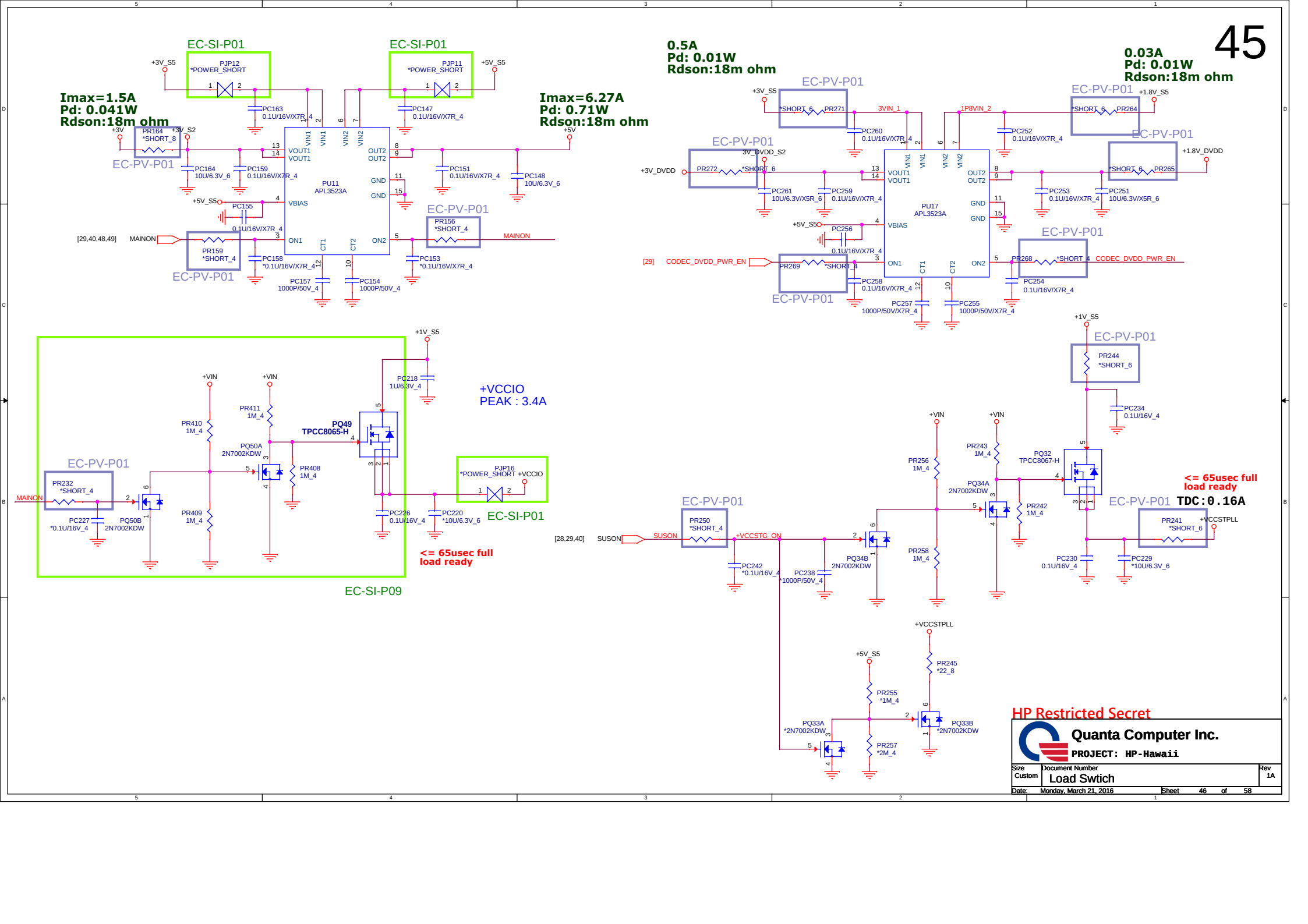


VCCSA
TDC=3.7A
Imax=4.5A
OCP=10A
Frequency=600KHz
Ripple=11mV
Loadlin2: -10.3m ohm
Delta IL = 3.4A

HP Restricted Secret

Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	CPU +VCCSA	1A
Date: Wednesday, March 09, 2016	Sheet 45 of 58	


EC-SI-P01
EC-SI-P01
Imax=1.5A
Pd: 0.041W
Rdson:18m ohm
Imax=6.27A
Pd: 0.71W
Rdson:18m ohm
0.5A
Pd: 0.01W
Rdson:18m ohm
0.03A
Pd: 0.01W
Rdson:18m ohm
PU11
APL3523A
PU17
APL3523A
EC-PV-P01
+VCCIO
PEAK : 3.4A
PQ49
TPCC8065-H
<= 65usec full load ready
EC-SI-P09
TDC:0.16A
HP Restricted Secret
Quanta Computer Inc.
PROJECT: HP-Hawaii
Load Swtich
Monday, March 21, 2016
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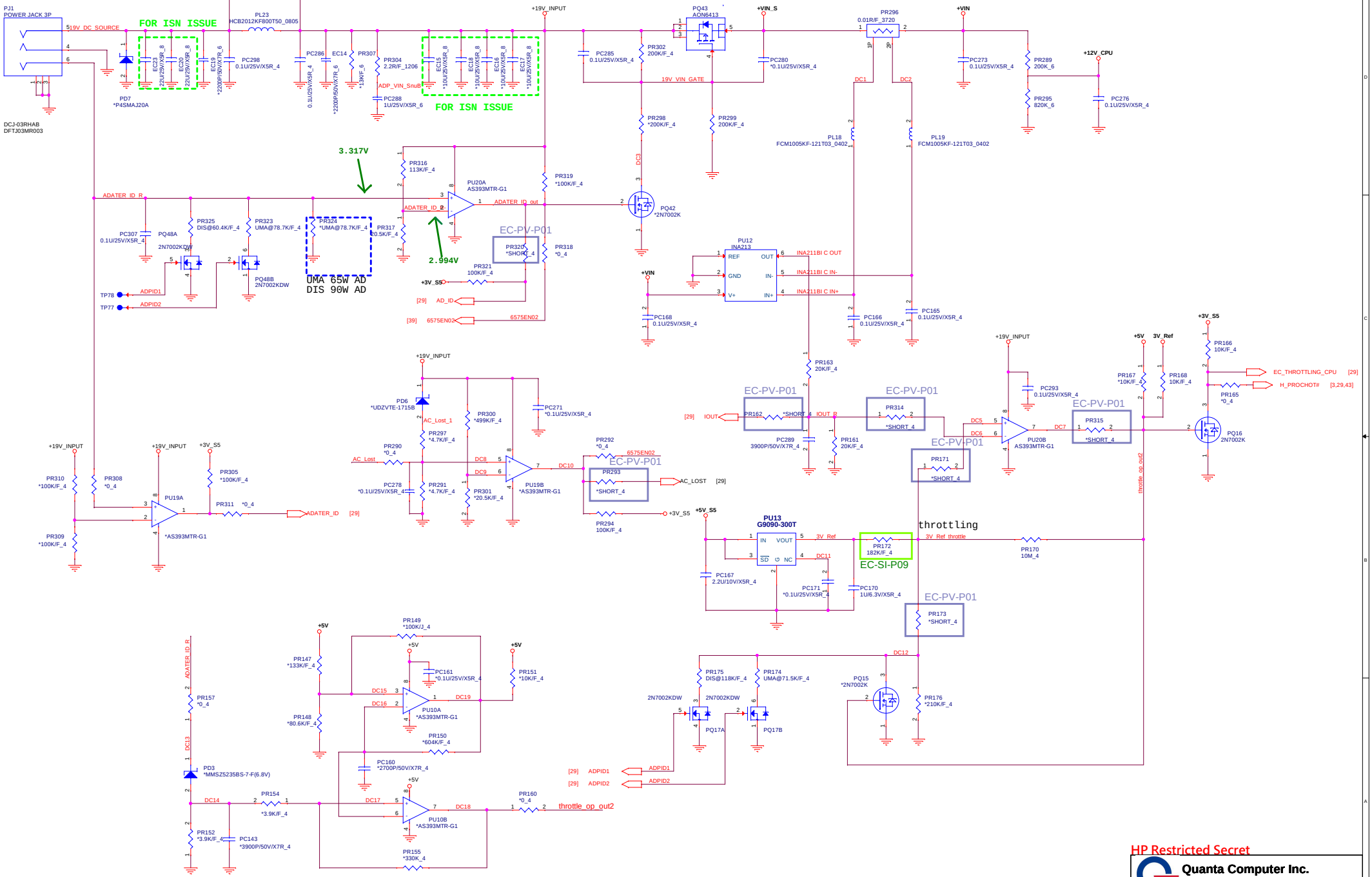
Id=16A
Qg=41~58nC
Rdson=6.9~8.5mOHM



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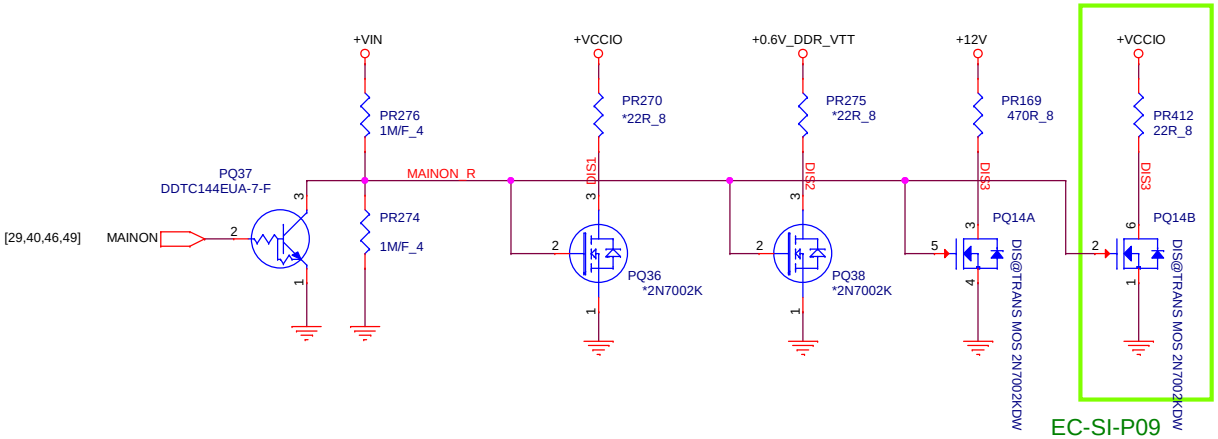
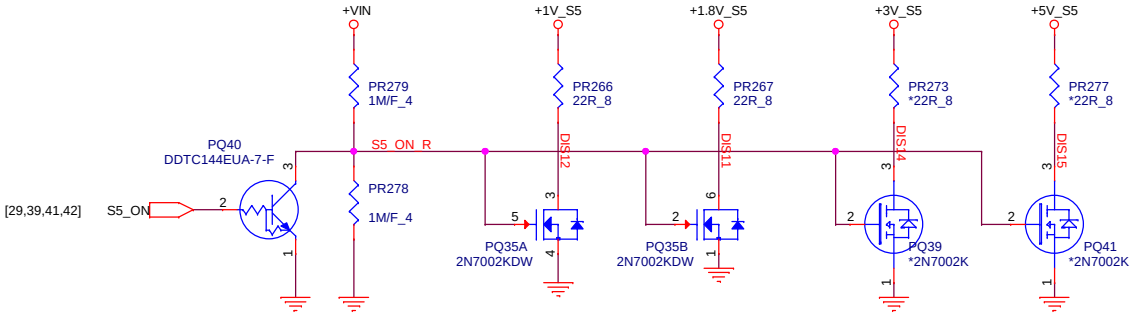
Quanta Computer Inc.		
PROJECT: HP-Hawaii		
Size: Custom	Document Number: DC IN	Rev: 1A
Date: Wednesday, March 09, 2016	Sheet 47 of 56	

CONFIDENTIAL

DISCHARGE

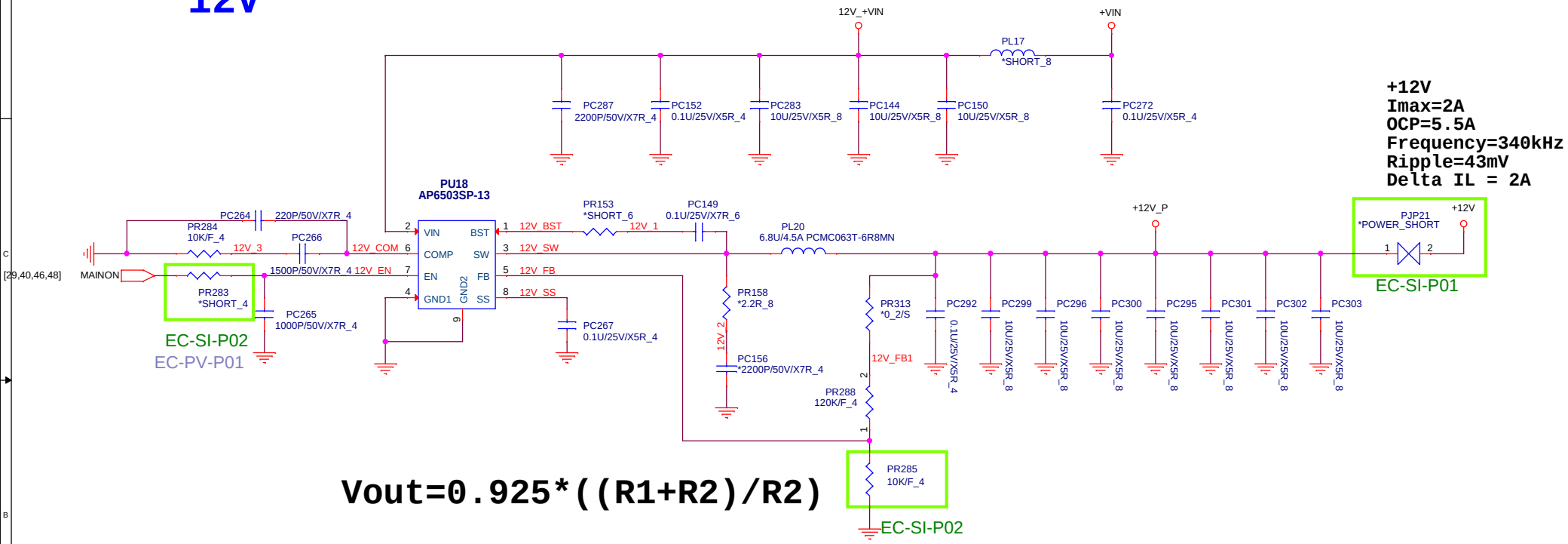




HP Restricted Secret

Quanta Computer Inc.		
PROJECT: HP-Hawaii		
Size: B	Document Number: Discharge	Rev: 1A
Date: Wednesday, March 09, 2016	Sheet 48 of 58	

12V

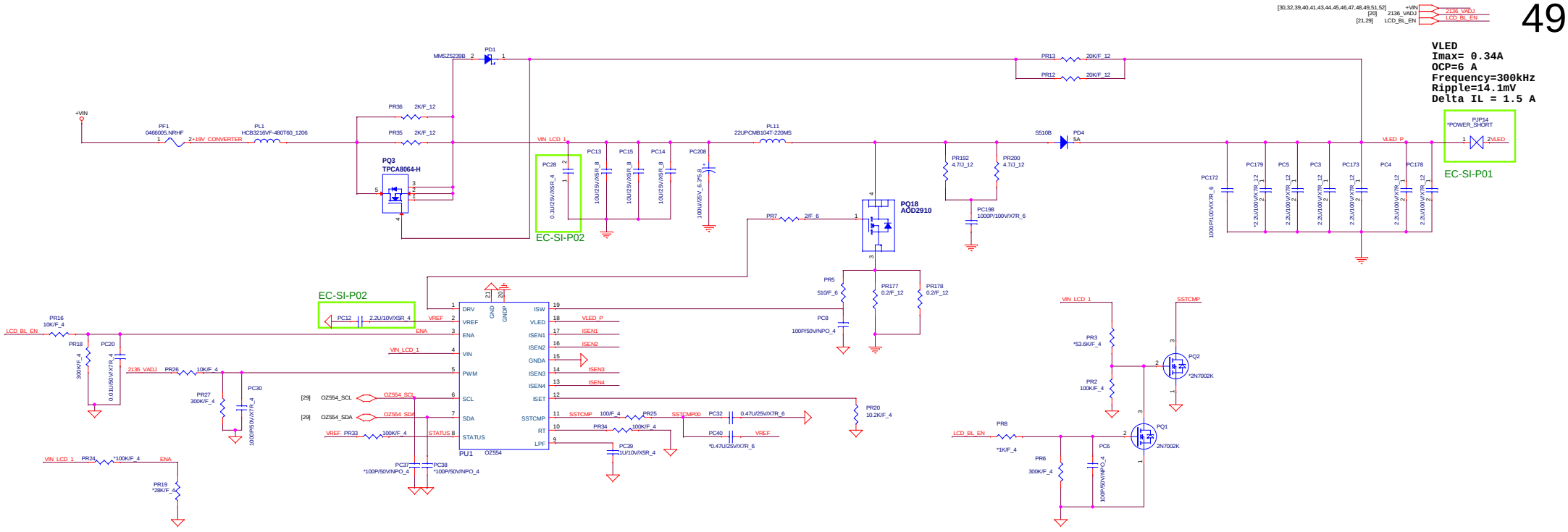


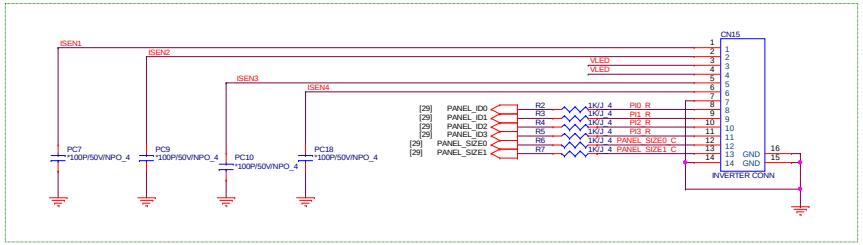
+12V
Imax=2A
OCP=5.5A
Frequency=340kHz
Ripple=43mV
Delta IL = 2A

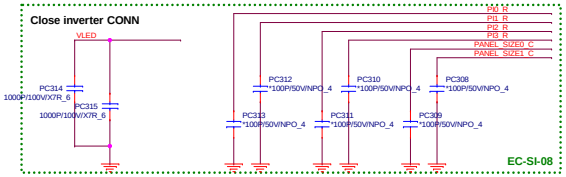
Vout=0.925*((R1+R2)/R2)

HP Restricted Secret

Quanta Computer Inc.		
PROJECT: HP-Hawaii		
Size: B	Document Number: +12V	Rev: 1A
Date: Wednesday, March 09, 2016	Sheet 49 of 58	







PANEL_SIZE Table

PANEL_Size[1:0]	Size
00	19.5/9.53"
01	21.5"
10	23.6"/23.8"
11	Reserve

19.45" /19.53" PANEL_ID Table

PANEL_ID[3:0]	Panel model
1111	No Connect
1110	INX M200HJJ-L20 FHD
1101	AUO M195RTN01.0 HD+
1100	LGD LM195WD1-TLA1 HD+
1010	Reserve

21.5" PANEL_ID Table

PANEL_ID[3:0]	Panel model
1111	No Connect
1110	INX M215HJK-L3B FHD eDP
1101	SDC LTM215HL01 FHD
1100	LGD LM215WF3-SLN1 FHD
1011	Reserve

23.6" /23.8" PANEL_ID Table

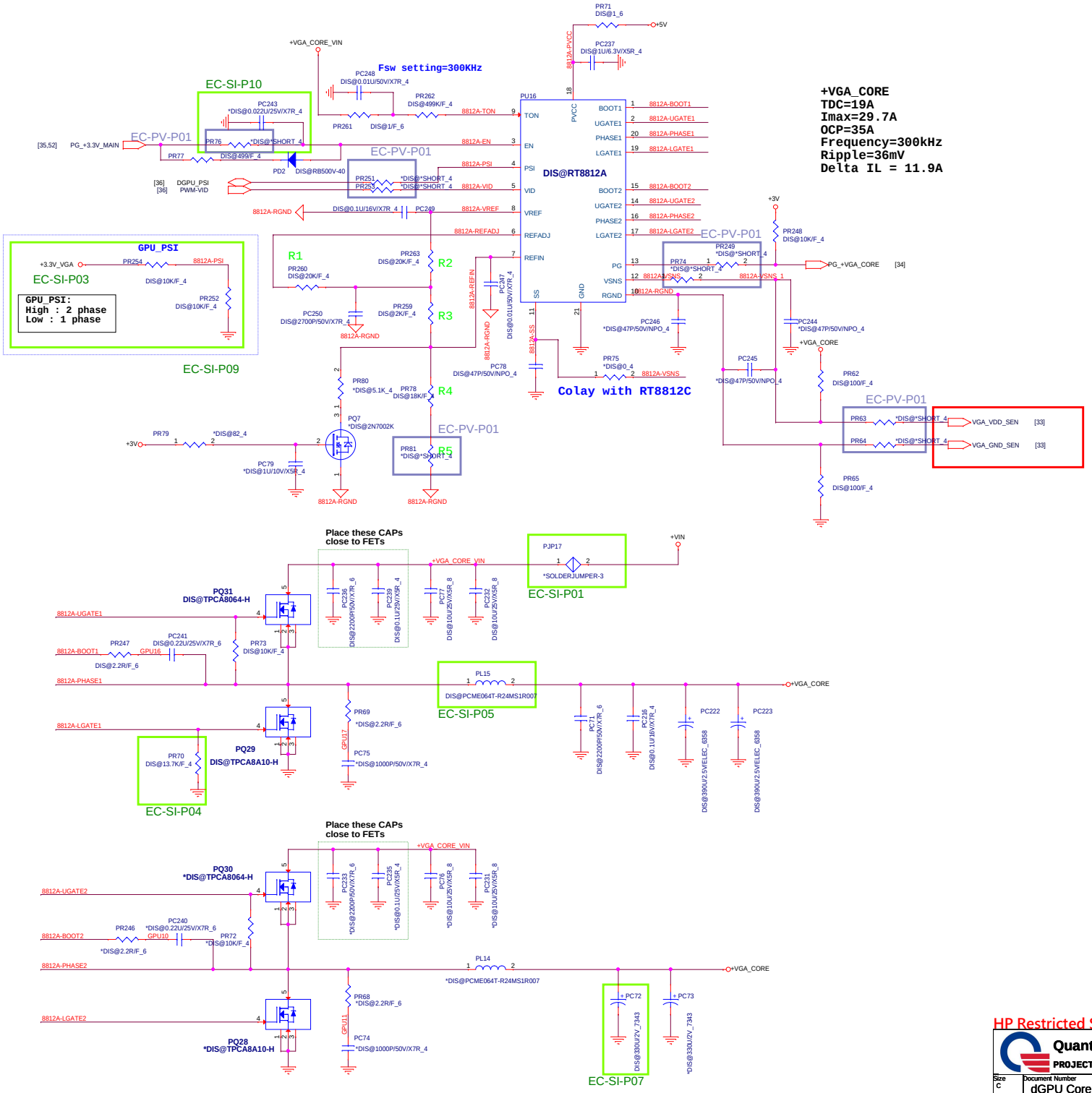
PANEL_ID[3:0]	Panel model
1111	No Connect
1110	INX M236HJK-L5B FHD eDP
1101	AUO M238HAN01.0 FHD
1100	LGD LM238WF1-SLE1 FHD
1011	SDC LTM238HL02 FHD
1010	Reserve

Panel_ID[3:0] = 1111 & Panel_Size[1:0] = 11 is reserved for cabling detection by "No connection".

Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	OZ554	1A

Date: Thursday, March 17, 2016 Sheet 50 of 58



HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
C	dGPU Core	1A

Date: Wednesday, March 09, 2016 Sheet 51 of 58

VGA POWER

AO6402A
Rdson=24m ohm
Imax=0.2A
Pd: 0.01W

+1.05V_VGA
Imax=1.5A
OCP=4A
Frequency=1MHz
Ripple=12mV
Delta IL = 0.8A

+1.5V_VGA
Imax=4.7A
OCP=8A
Frequency=500KHz
Ripple=22mV
Delta IL = 2.8A

+1.05V VGA

40mil

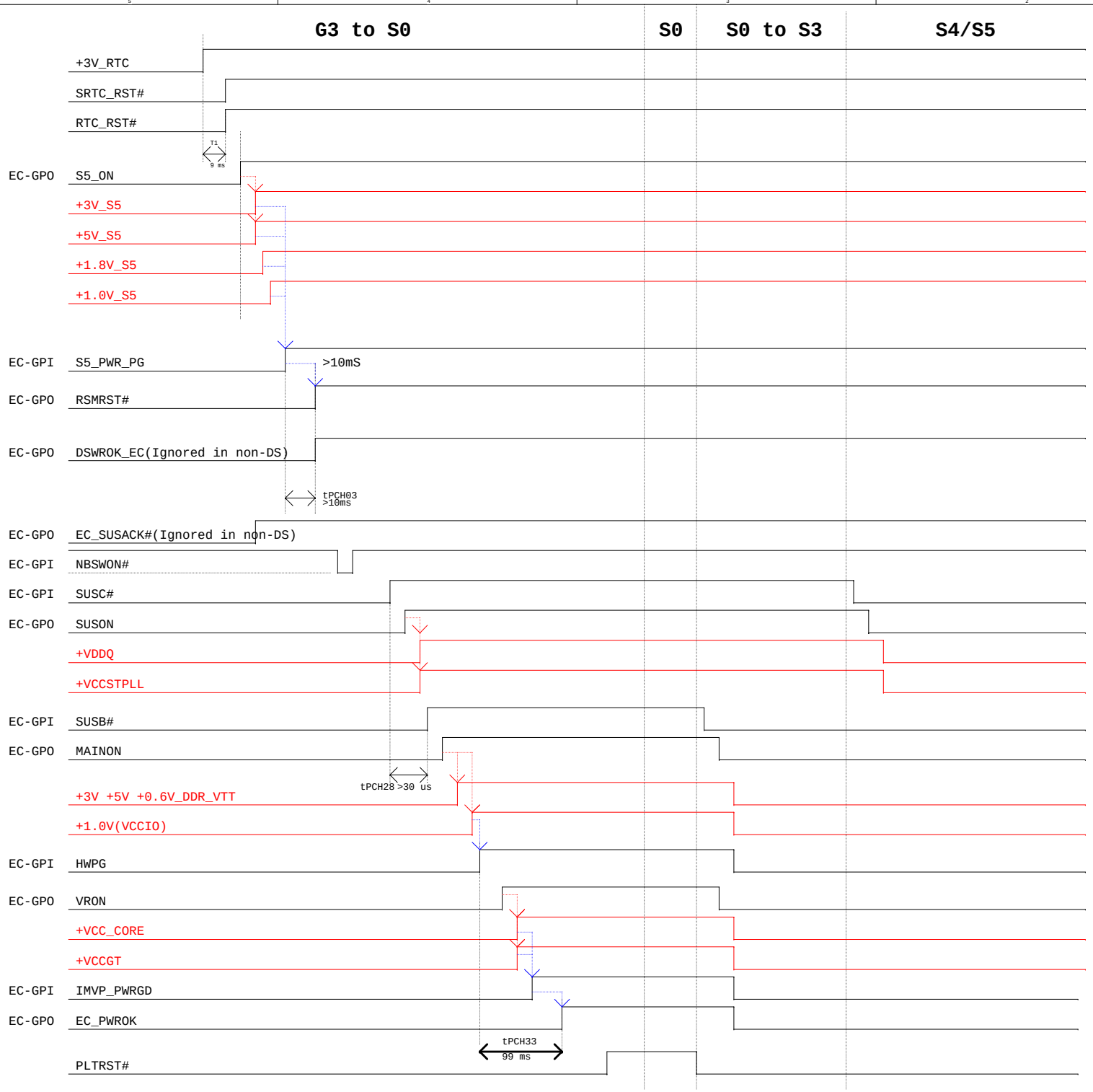
V0=0.6*(R1+R2)/R2

VREF=0.604V

Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	dGPU +1.05V/+1.5V	1A

Date: Wednesday, March 09, 2016 Sheet 52 of 58



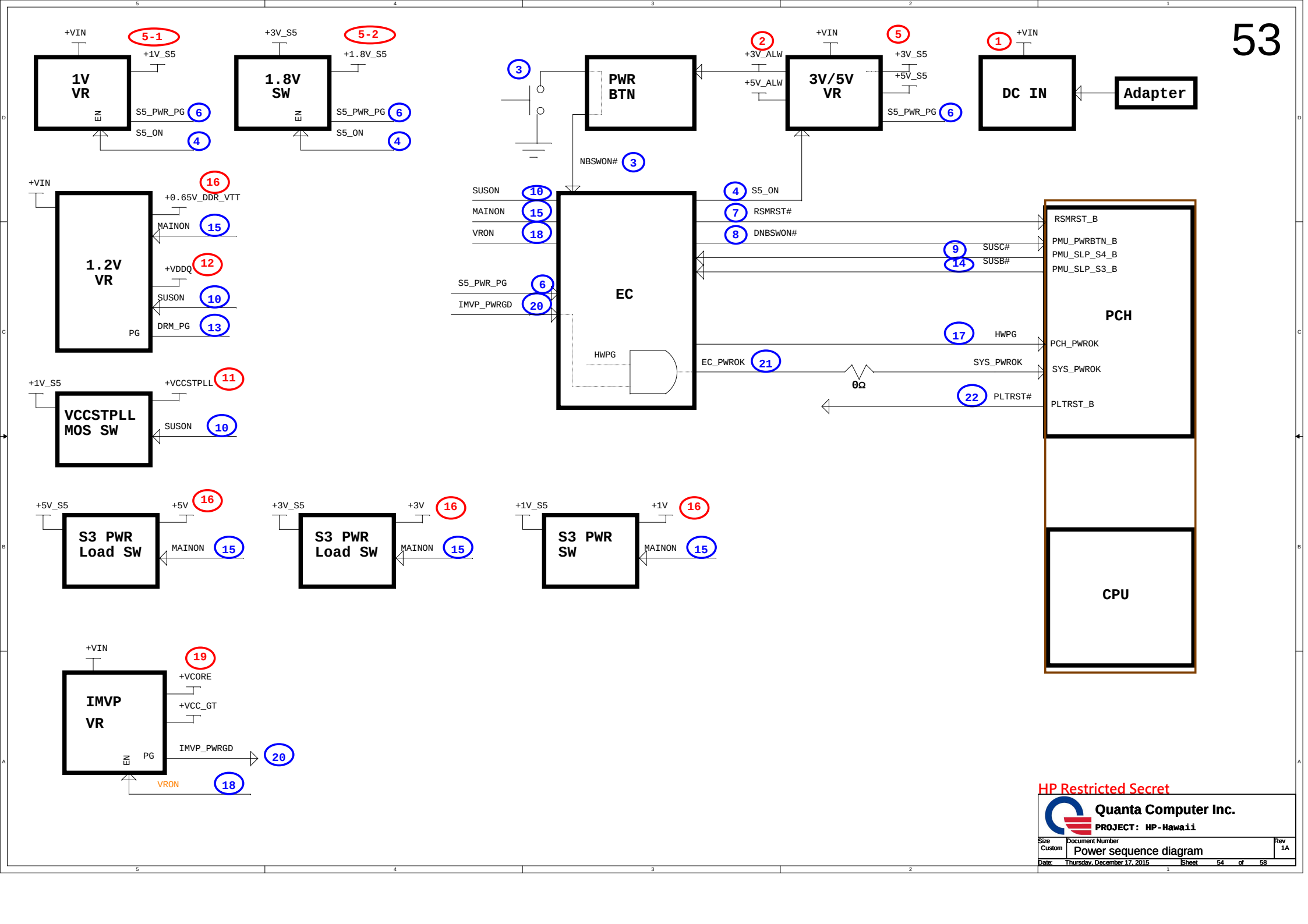
HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
C	Power Sequence	1A

Date: Thursday, December 17, 2015 Sheet 53 of 58



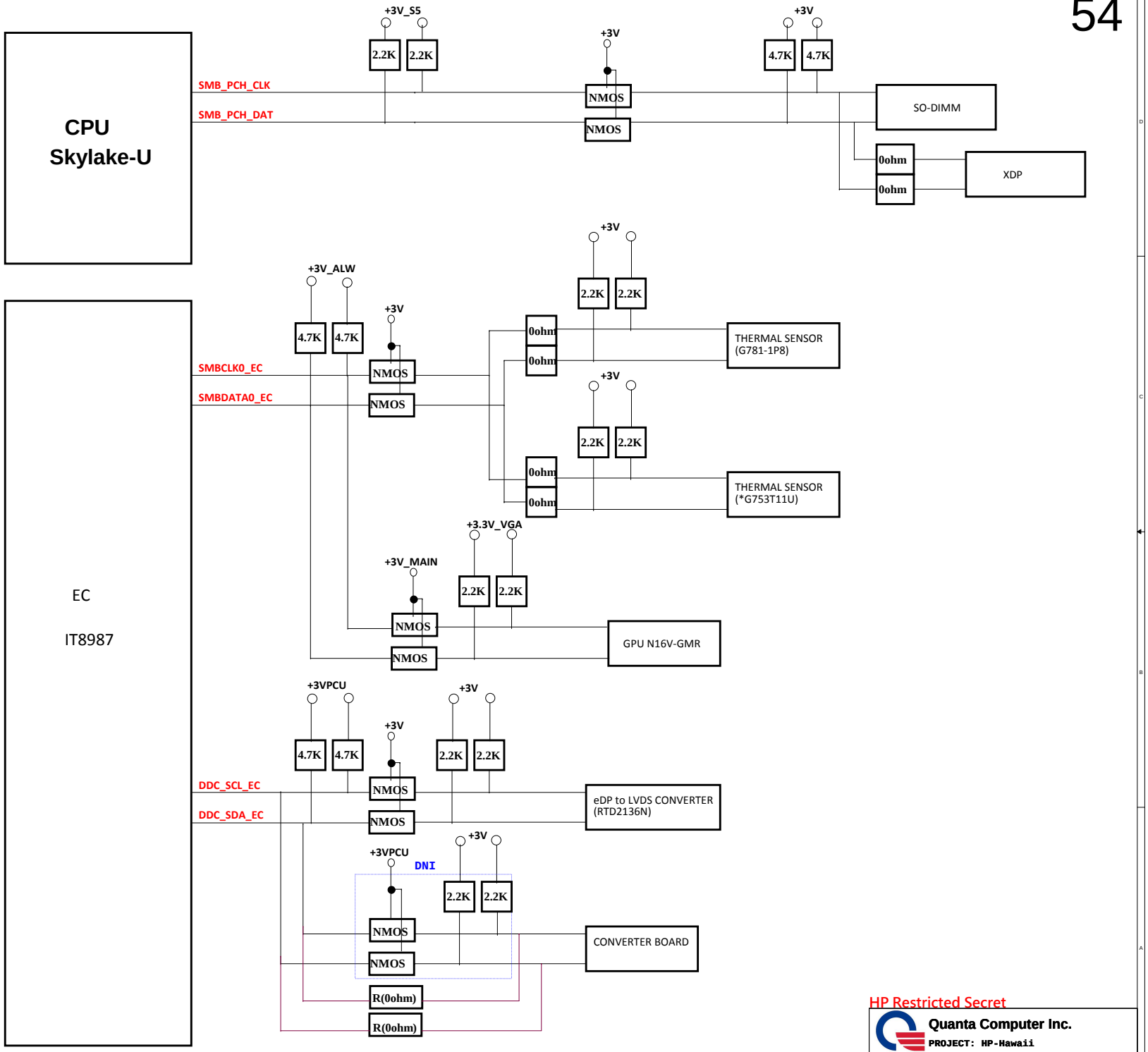
HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	Power sequence diagram	1A

Date: Thursday, December 17, 2015 Sheet 54 of 58



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Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SMBUS map	1A

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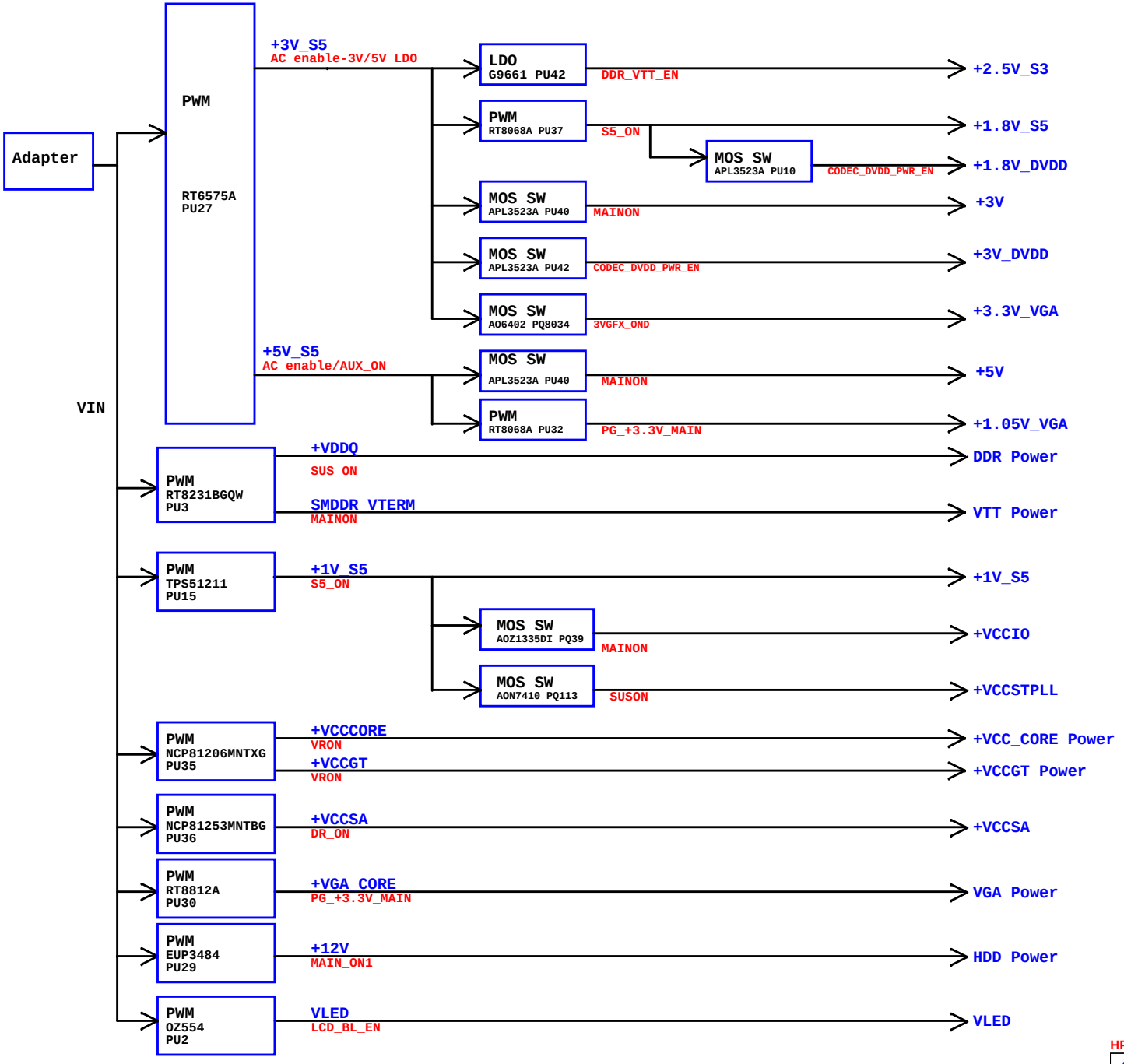
Power Delivery Map



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Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
C	Power Delivery Map	1A

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N91 EE Schematic DB to SI Change List

EC#	Page	Description	Part Affected
EC-SI-01	17,18	Unstuff C205/C213 for DDR4 Issue	C205,C213
EC-SI-02	21	Change HDMI HPD signal from low active to high active	Q38,R638,R639
EC-SI-03	21	Modify Q37 MOSFET gate power source from +5V to +3V	Q37
EC-SI-04	28	Swap EC GPIO for reserving 2nd fan control	
EC-SI-05	22	Separate L/R channels for spkeaker connector	CN26,CN27
EC-SI-06	20	Add ESD protection for CCD	
EC-SI-07	29	Reserve 2nd FAN	
EC-SI-08	49	Reserve 100pF for CN15 (EMI suggestion)	
EC-SI-09	31	Add 2 GND pad for EMI	
EC-SI-10	25	Change ODD connector	CN21
EC-SI-11	26	Change connector of card reader daughter board	CN24
EC-SI-12	13,34	Change load cap for 32.768K/24M/27M due to vendor suggest	
EC-SI-13	All	Stuff EMC/ESD/RF materials	
EC-SI-14	35	Unstuff R437 for correct PSI setting	R437
EC-SI-15	22	Change AL7/AL8/AL9/AL11 as 0ohm from Realtek suggest	AL7,AL8,AL9,AL11

N91 EE Schematic SI to PV Change List

EC#	Page	Description	Part Affected
EC-PV-01	All	Change 0ohm resistor to be short pad	
EC-PV-02	27	Remove reserved CMC of USB3.0	L28,L29,L30,L33

N91 Power Schematic DB to SI Change List

EC#	Page	Description	Part Affected
EC-SI-P01	38~51	Change default open to default short	PJP1~PJP22
EC-SI-P02	48,49,51	Downsize components	PR283, PR285, PC12, PC28, PC184, PC185, PC174, PL3
EC-SI-P03	50, 51	Correct connection	
EC-SI-P04	38,40,42,50	Fine tune OCP function	PR134, PR135, PR101, PR21, PR70
EC-SI-P05	50	Change choke for transient	PL15
EC-SI-P06	40,51	Fine tune offset voltage	PR97, PR186
EC-SI-P07	38, 50	Change components for ripple voltage	PL21, PC72
EC-SI-P08	38,39	Add components for PG function	PR137, PR122
EC-SI-P09	39,40,45~47,50,51	Change components for common part using	PU6, PQ10, PQ13, PQ14, PQ49, PQ50, PR408~PR412, PR254, PR252, PQ4, PQ5, PQ26, PR172
EC-SI-P10	50	Fine tune soft start	PR76, PC243
EC-SI-P11	43	Add components for Efficiency	PQ19, PQ23
EC-SI-P12	42	Fine tune DVID setting	PR210, PR22
EC-SI-P13	42	Fine tune Iout function	PR205, PR209, PC54, PC204
EC-SI-P14	42	Fine tune compensation	PR31, PC205

N91 EE Schematic SI to PV Change List

EC#	Page	Description	Part Affected
EC-PV-P01	All	Change 0ohm resistor to short pad	
EC-PV-P02	42	Fine tune +VCCGT load line	PR14
EC-PV-P03	42	Fine tune +VCCGT Iout function	PR195
EC-PV-P04	42	Fine tune Vcore OCP	PR208
EC-PV-P05	42	Fine tune Vcore Iout function	PR209
EC-PV-P06	42	Fine tune Vcore Loadline	PR212,PR214