

# 01



Size Custom	Document Number <b>SKLU (1/14)</b>	Rev
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## KABYLAKE ULT Processor DDR4

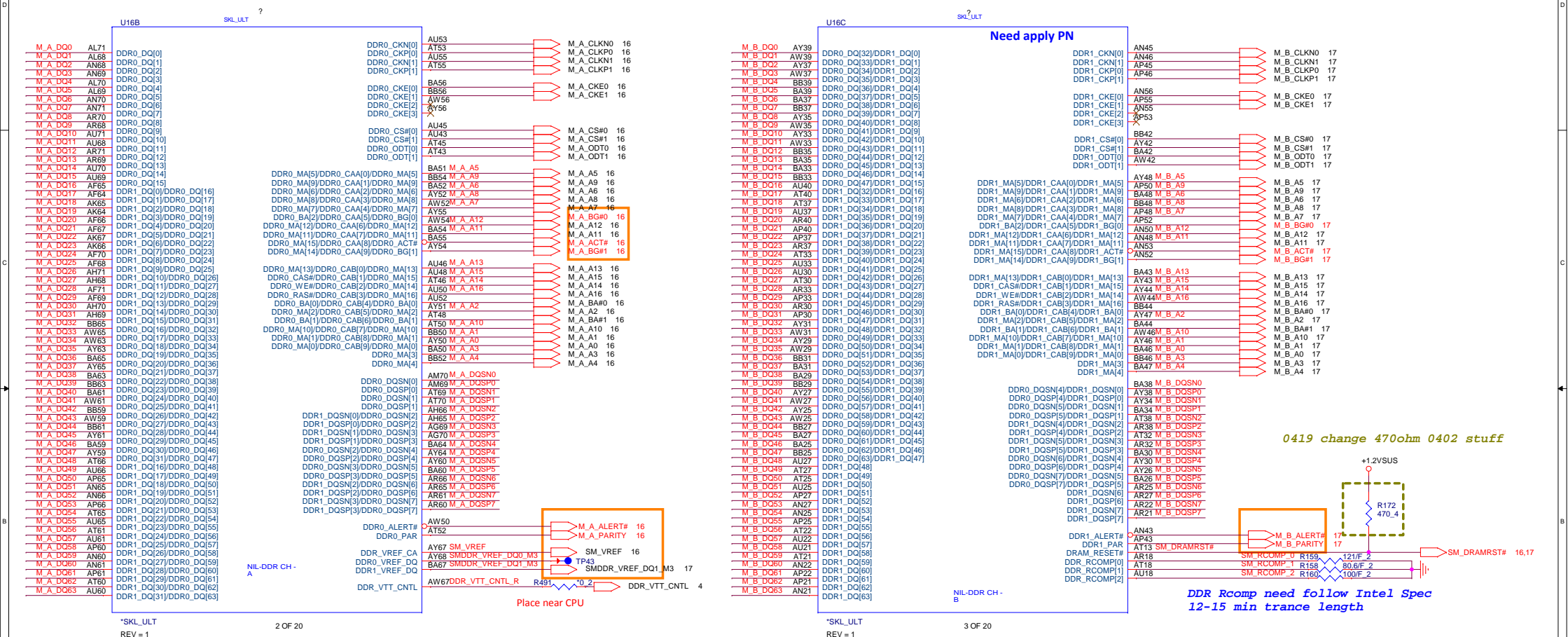
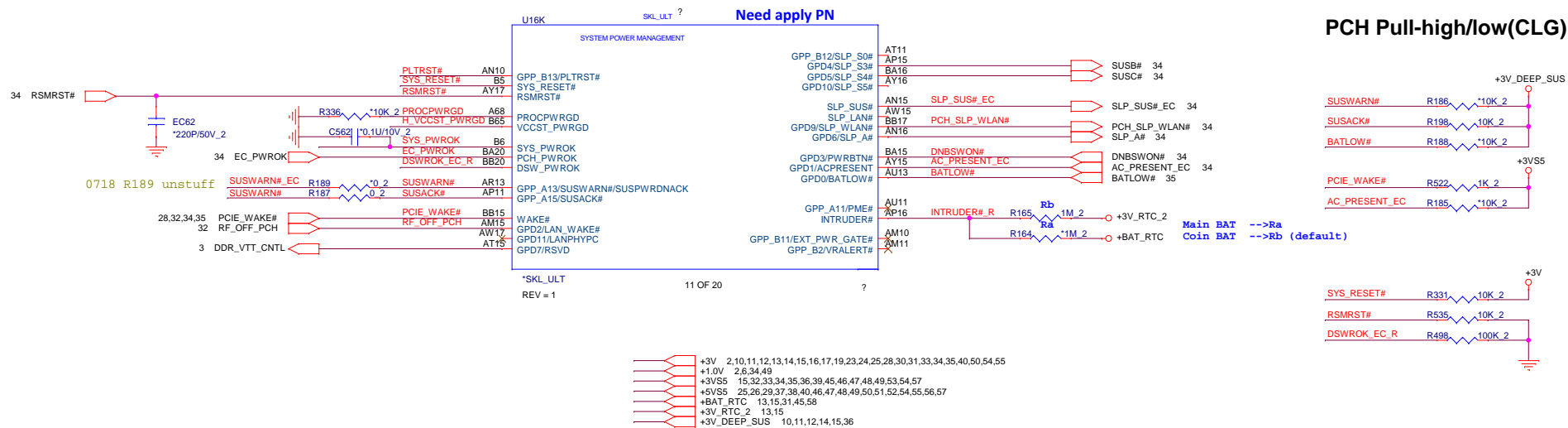


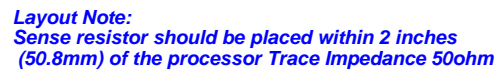
Table 4-34. KBL U DDR4/-RS SODIMM T3/8L Inline NIL Signal Routing Guidelines (Sh

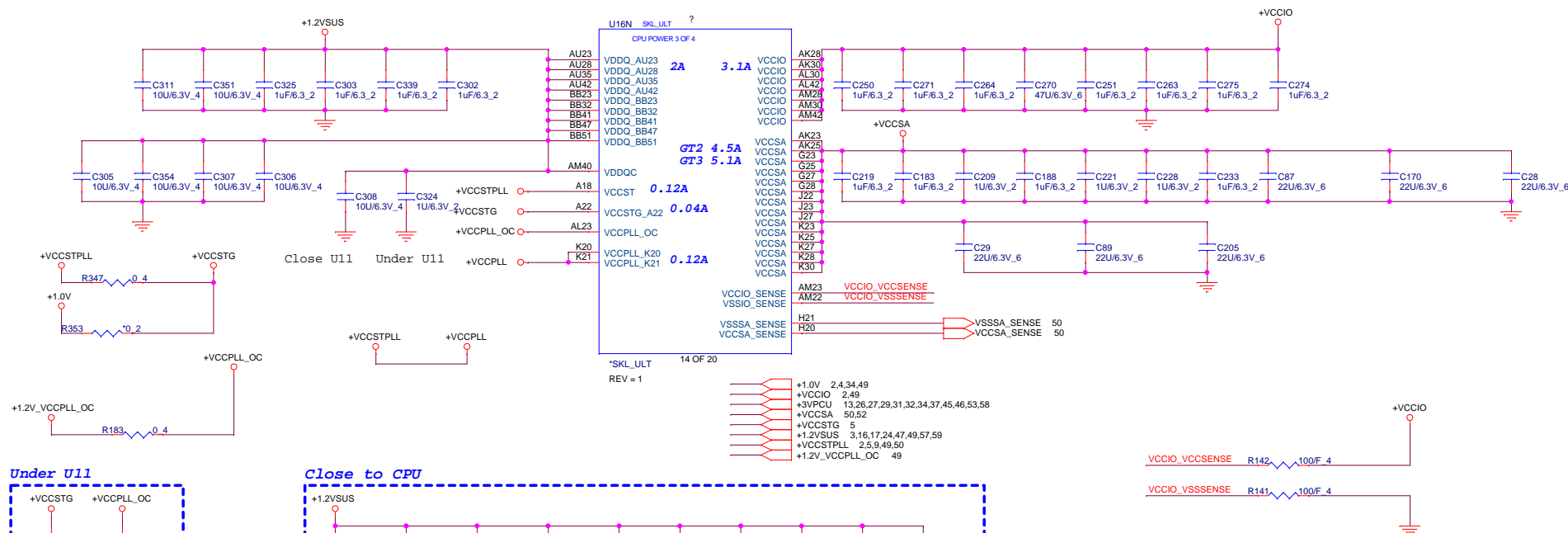
Signal Group	Region	Layer Route	Reference	Via Count	Trace Width (mils)	Target Impedance (Ω)		Min Trace Spacing (mils)				Max (mils) Length		R (045/50 (µF)	
						Diff	Single Ended Tolerance (%)	Diff	Group	Group to Group (1&2)	Byte (1&2)	Region	Breakout		Total
RCOMP[0]	M	MS	VSS	2	12-15				20	25		500	500	121	
RCOMP[1]	M	MS	VSS	2	12-15				20	25		500	500	80.6	
RCOMP[2]	M	MS	VSS	2	12-15				20	25		500	500	100	



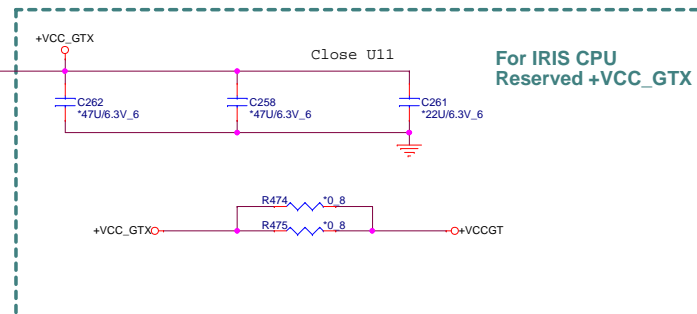
**PROJECT : X31**  
Quanta Computer Inc.


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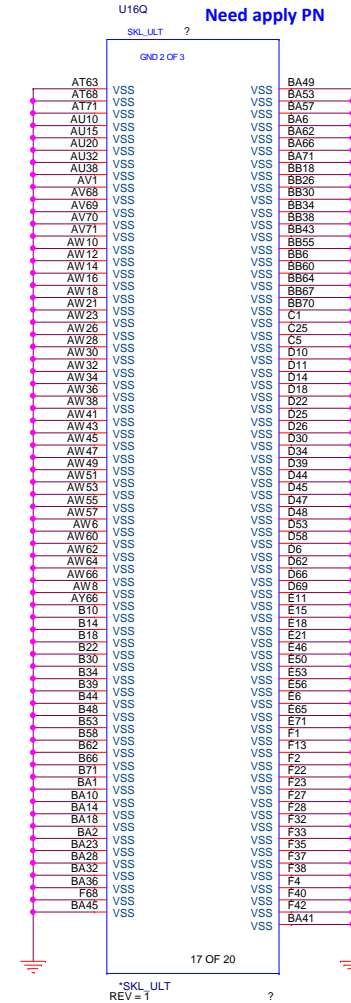
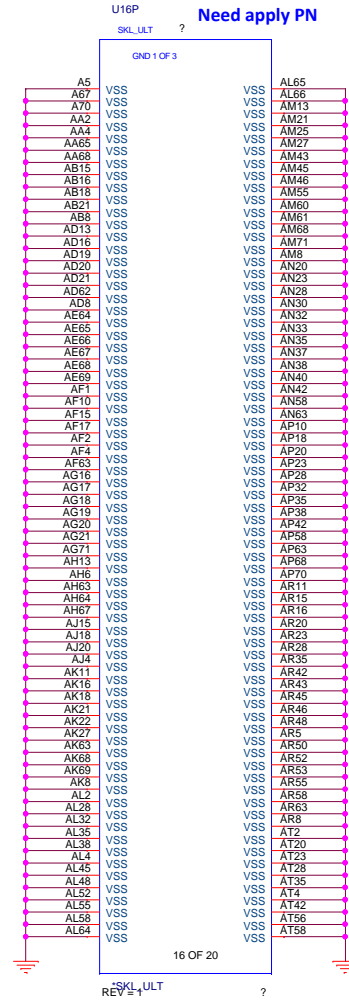
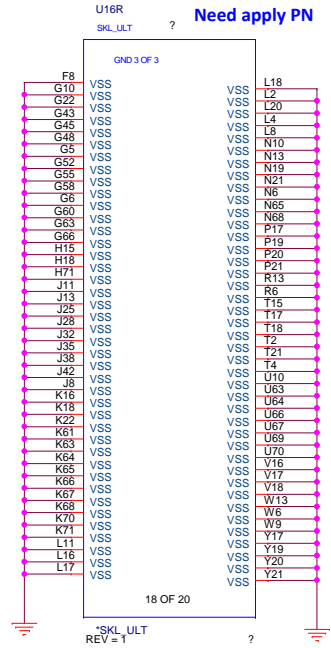
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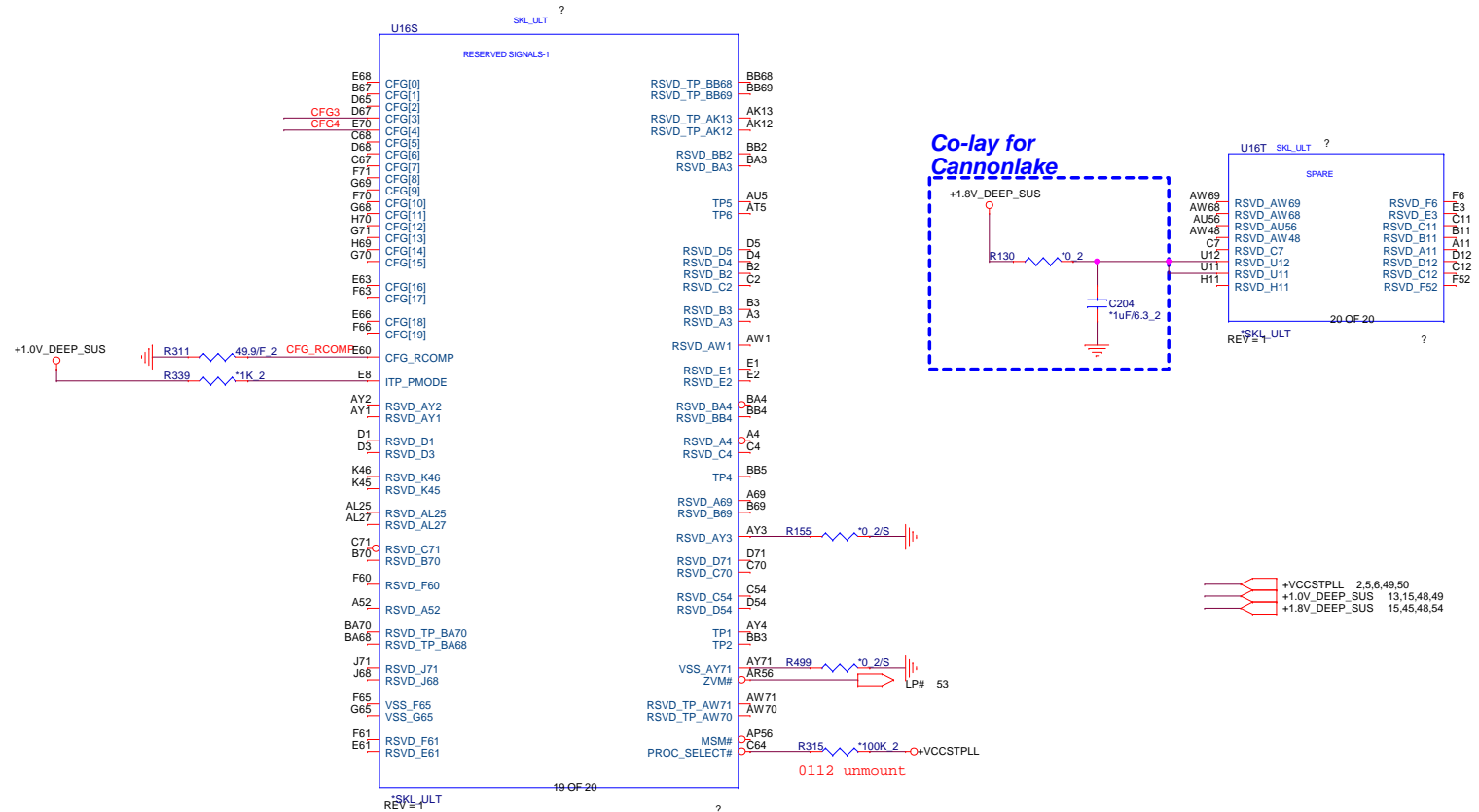


Power Rail	Description	Control
V <sub>CC</sub>	Processor IA Cores Power Rail	SVID
V <sub>CCGT</sub>	Processor Graphics Power Rails	SVID
V <sub>CCGTX</sub>	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V <sub>CCSA</sub>	System Agent Power Rail	SVID/Fixed (SKU dependent)
V <sub>CCIO</sub>	IO Power Rail	Fixed
V <sub>CCST</sub>	Sustain Power Rail	Fixed
V <sub>CCPLL</sub>	Processor PLLs power rail	Fixed
V <sub>DDQ</sub>	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V <sub>CCOPC</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCOPC_1P8</sub>	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V <sub>CCEOPIO</sub>	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



	<b>PROJECT : X31</b> Quanta Computer Inc.		
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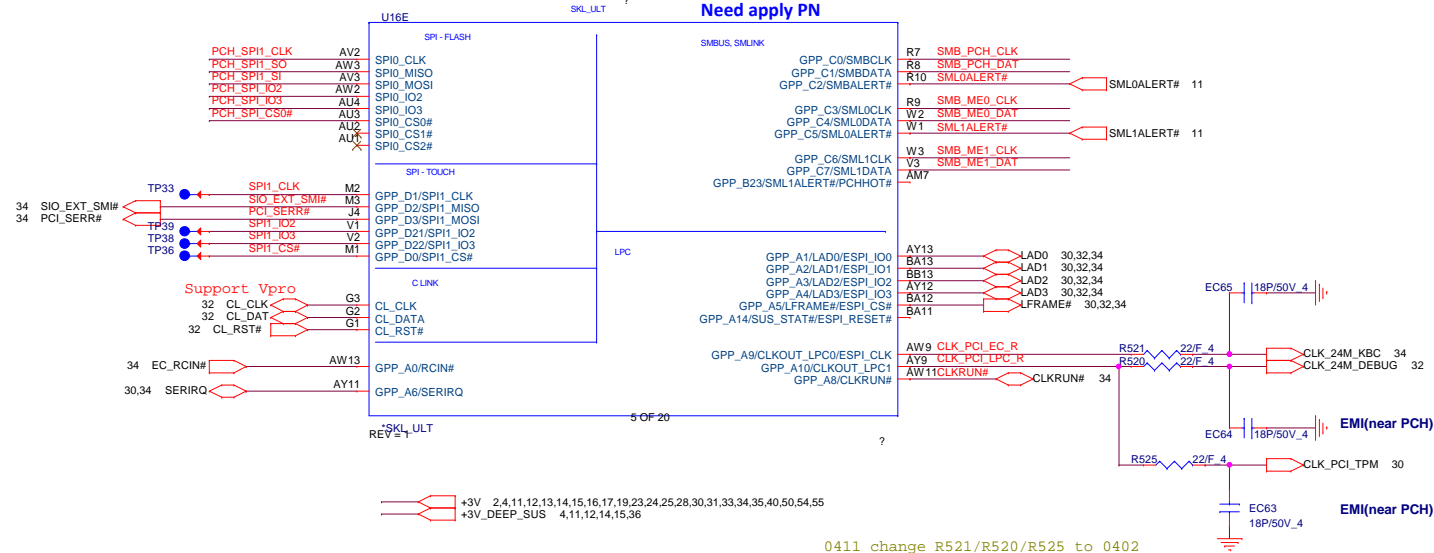




Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	

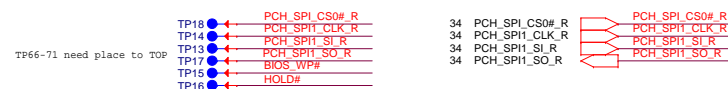


## ***GPIO Pull UP***

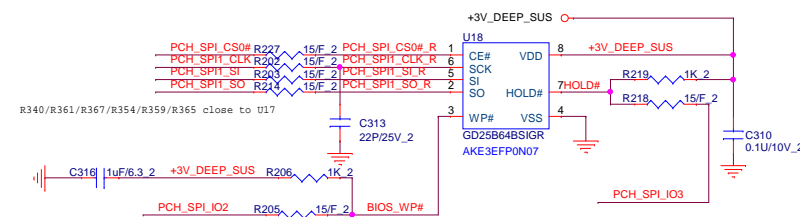
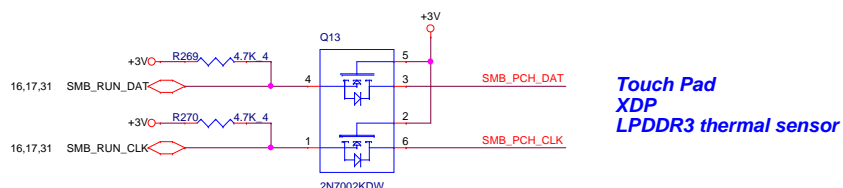


### PCH SPI ROM(CLG)

Vender	Size	P/N
EON	8MB	AKE3EZ0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

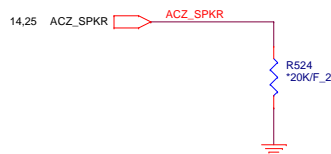


### SMBus/Pull-up(CLG)



# Functional Strap Definitions

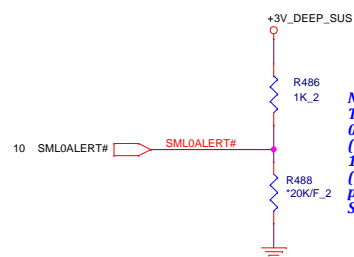
**DESIGN NOTE:**  
WEAK PULL UP RESISTOR PRESENT ON THIS NET



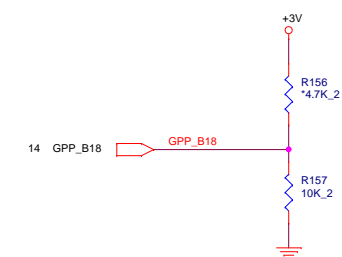
**TOP SWAP OVERRIDE**  
**HIGH - TOP SWAP ENABLE**  
**LOW-DISABLED**  
**HIGH: LPC SELECTED FOR SYSTEM FLASH**  
**WEAK INTERNAL PD**



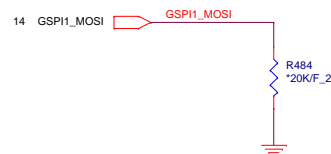
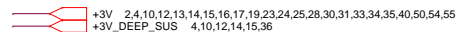
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Enable security measures defined in the Flash Descriptor.  
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



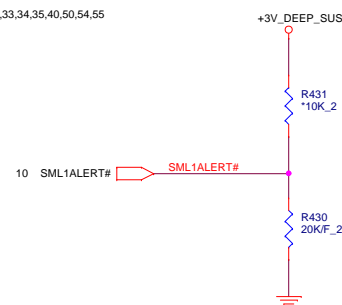
**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).  
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



**No Boot:**  
The signal has a weak internal pull-down.  
0 = Disable No Reboot mode.  
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



**No Boot:**  
The signal has a weak internal pull-down.  
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.  
**Bit 10**      **Boot BIOS Destination**  
0              SPI  
1              LPC

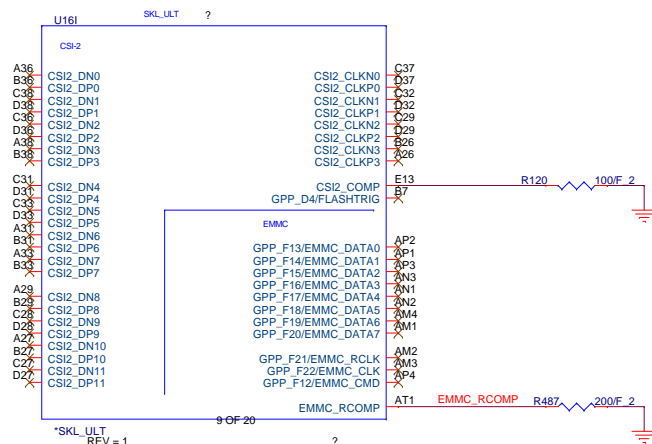
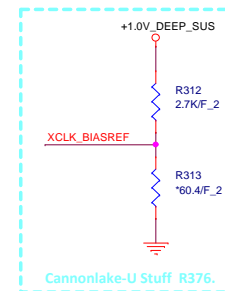


**No Boot:**  
The signal has a weak internal pull-down.  
0 = LPC Is selected for EC.  
1 = eSPI Is selected for EC.

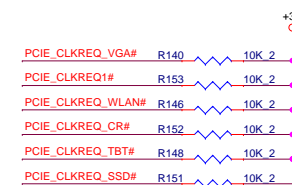
H


H

H

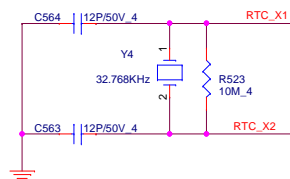


**CLK\_REQ/Strap Pin(CLG)**

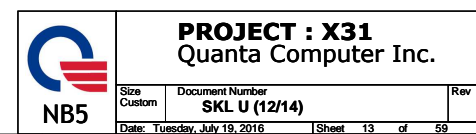
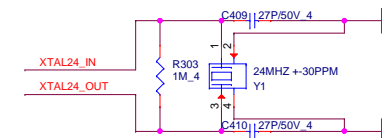
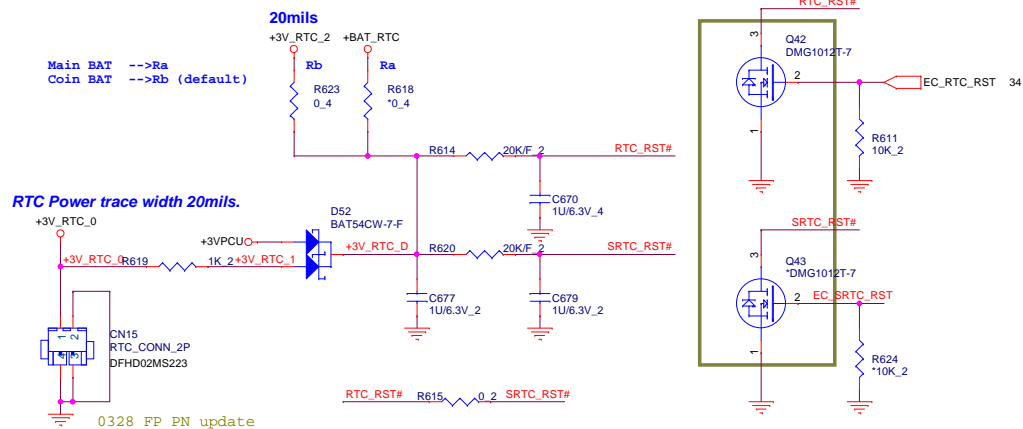



  
 +3V 2,4,10,11,12,14,15,16,17,19,23,24,25,28,30,31,33,34,35,40,50,54,55
   
 +3VPCU 6,26,27,29,31,32,34,37,45,46,53,58
   
 +BAT\_RTC 4,15,31,45,58
   
 +3V\_RTC\_2 4,15
   
 +1.0V\_DEEP\_SUS 9,15,48,49

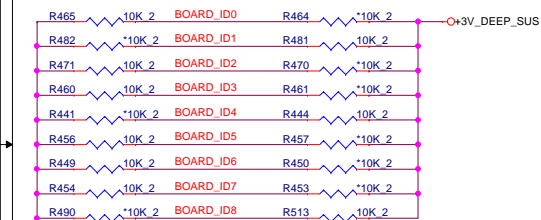
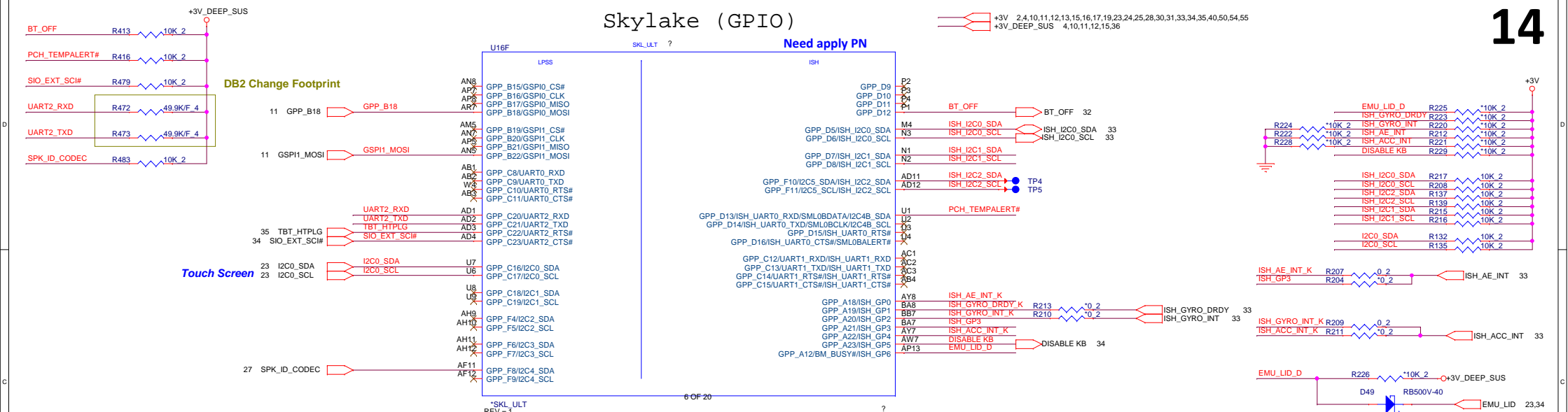
### External Crystal



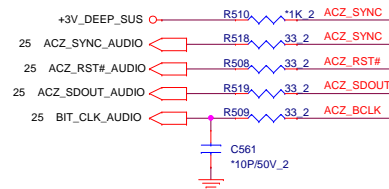
0523 SI Change to 12PF



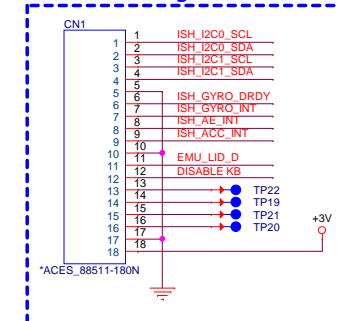
## Skylake (GPIO)



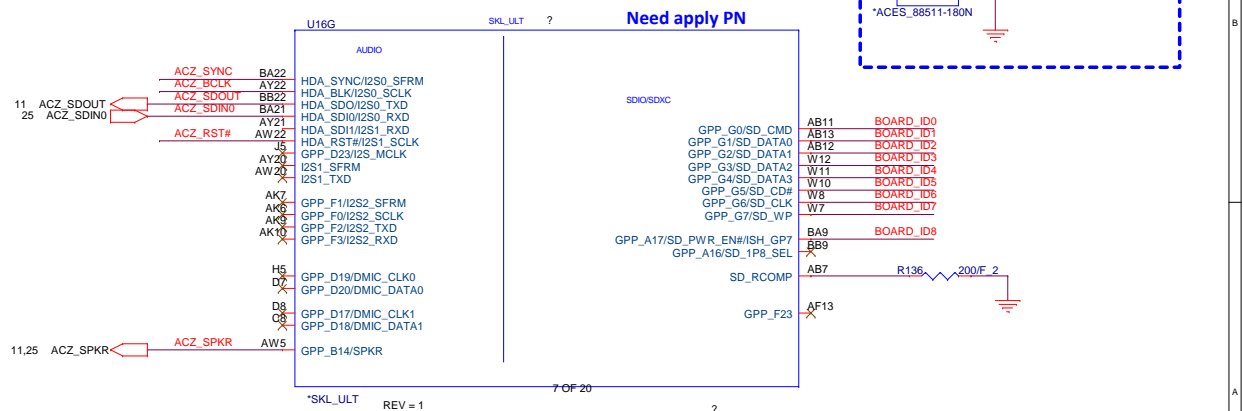
## HDA Bus(CLG)

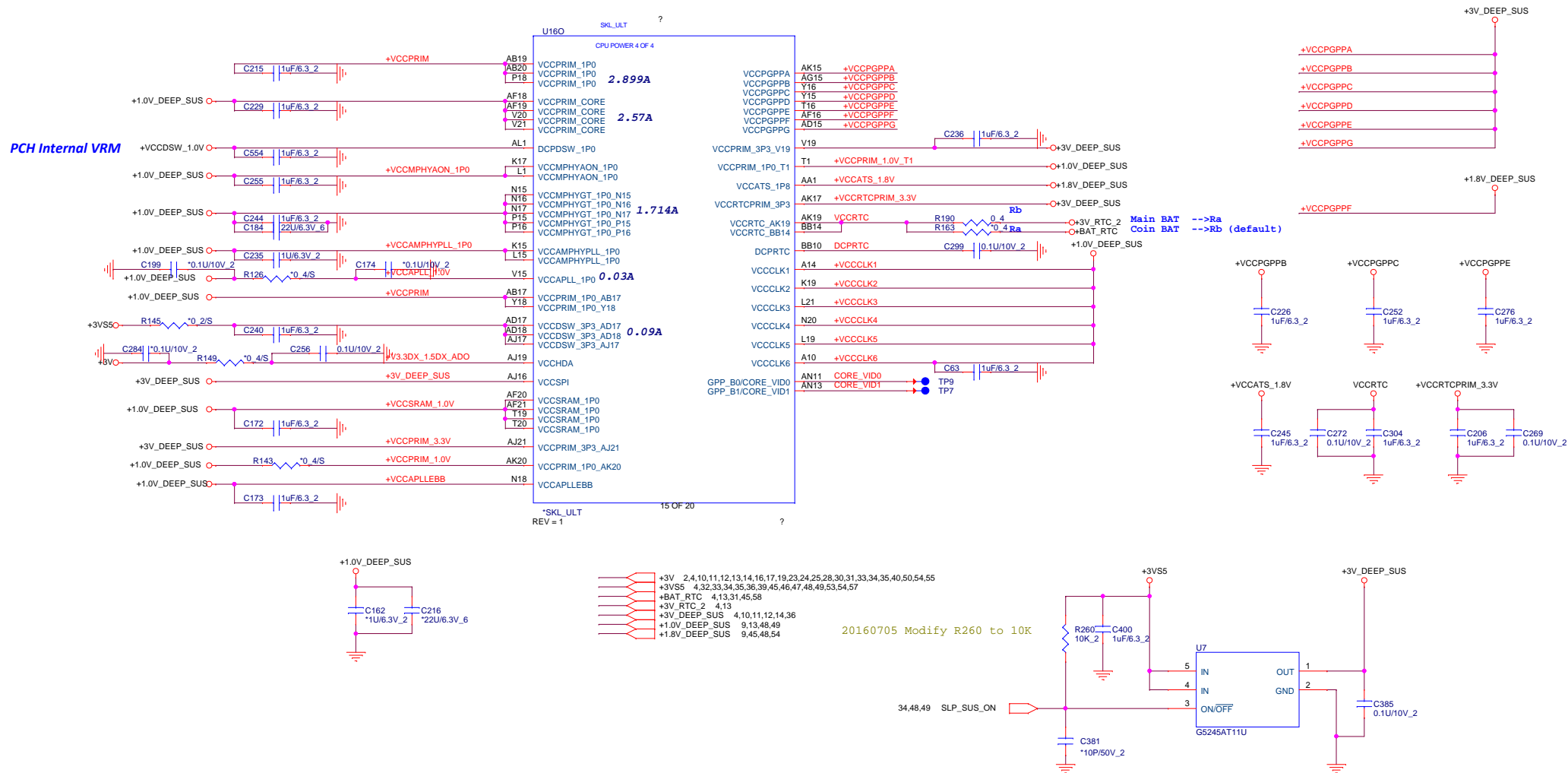


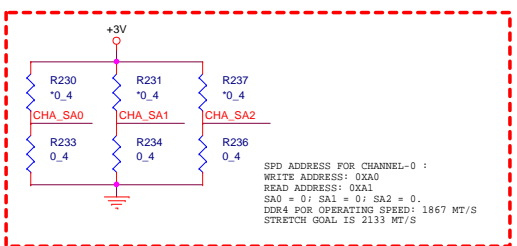
## Sensors Debug CONN



KBL-U	BOARD_ID8	BOARD_ID7	BOARD_ID6	Board ID [5:4]	BOARD_ID[3:0]				
Model	ID8	ID7	ID6	ID5 ID4	ID3	ID2	ID1	ID0	
X32	0 VPRO 1 Non VPRO	0 2+2 CPU 1 2+3E CPU	0 ESH 1 ISH	0 DIS (Default = 01)	0	0	0	0	Hynix 8Gb
					0	0	0	1	Samsung 8Gb
					0	0	1	0	Micron 8Gb
					0	0	1	1	Hynix 16G
					0	1	0	0	Samsung 16G
					0	1	0	1	Micron 16G
					0	1	1	1	
					1	0	0	0	
					1	0	0	1	
					1	0	1	0	
					1	0	1	1	



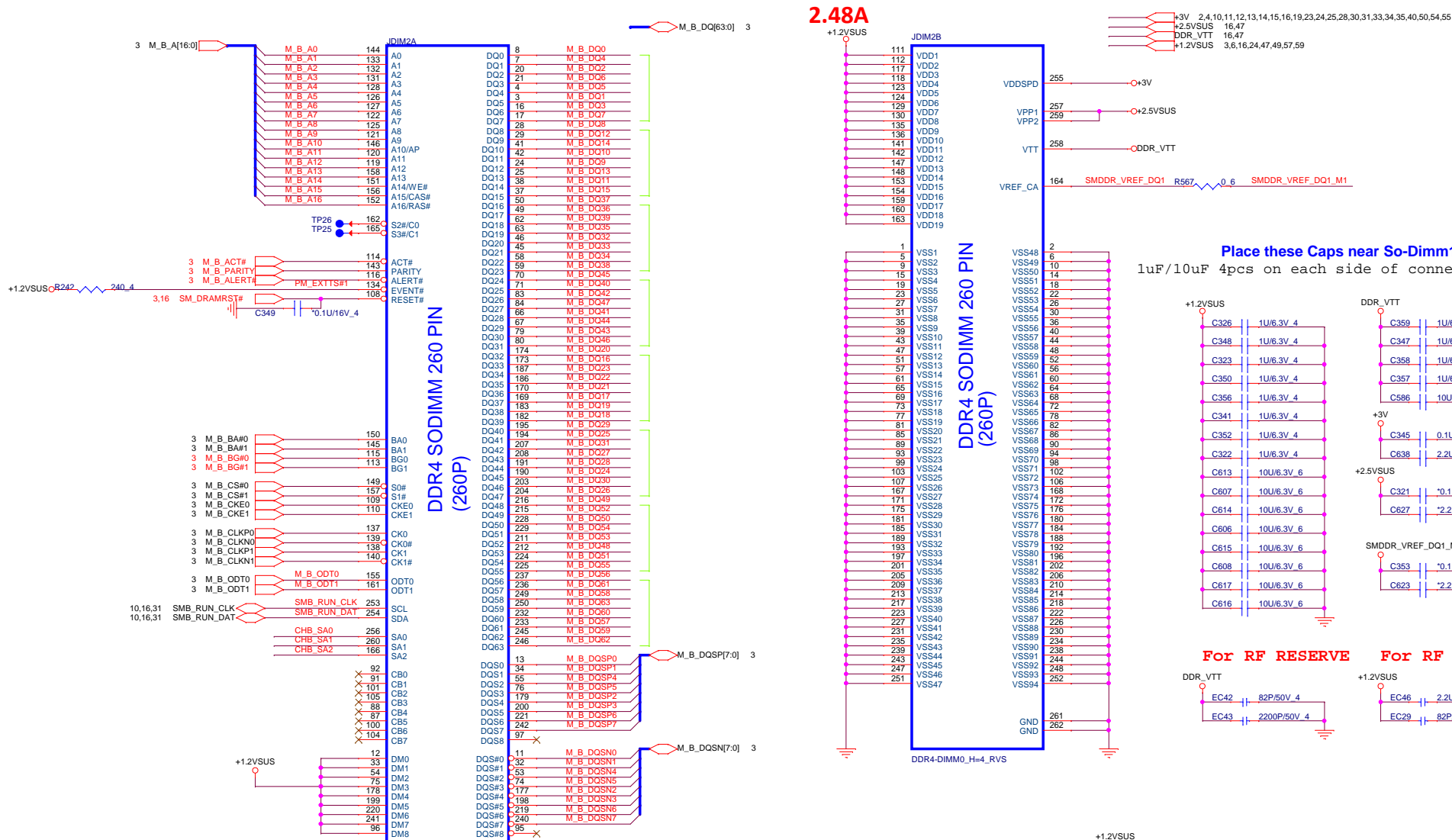


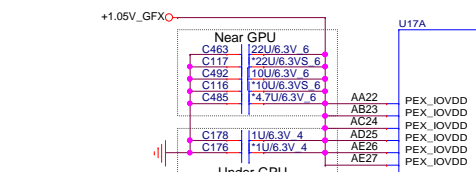


```
SPD ADDRESS FOR CHANNEL-0 :  
WRITE ADDRESS: 0XA0  
READ ADDRESS: 0XA1  
SA0 = 0; SA1 = 0; SA2 = 0.  
DDR4 POR OPERATING SPEED: 1867 MT/S  
STRETCH GOAL IS 2133 MT/S
```

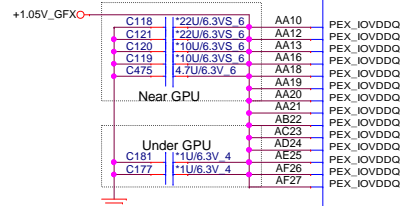


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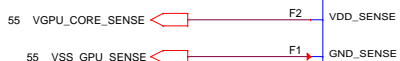
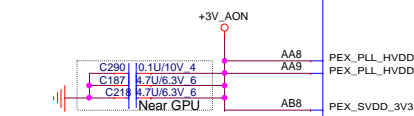




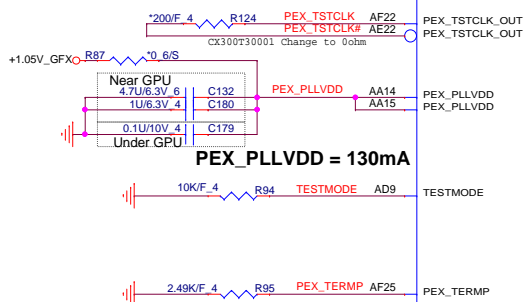
PEX\_IOVDD + PEX\_IOVDDQ = 1.042A



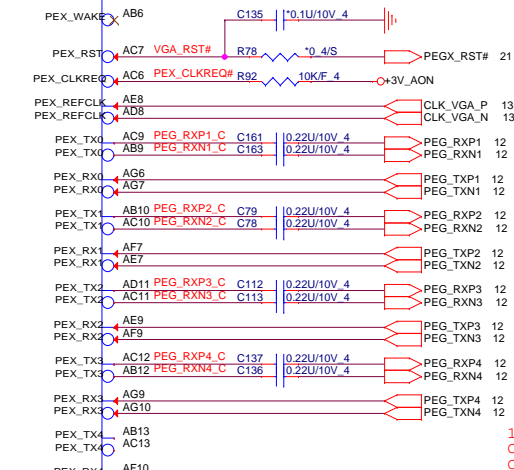
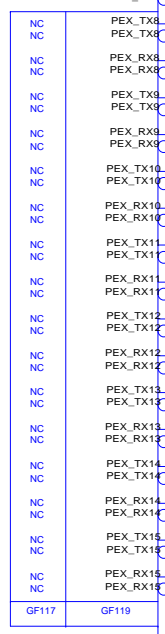
PEX\_PLL\_HVDD +  
PEX\_SVDD\_3V3 = 143mA



0611  
Change R433 to short pad



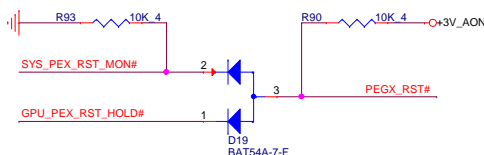
PEX\_PLLVDD = 130mA



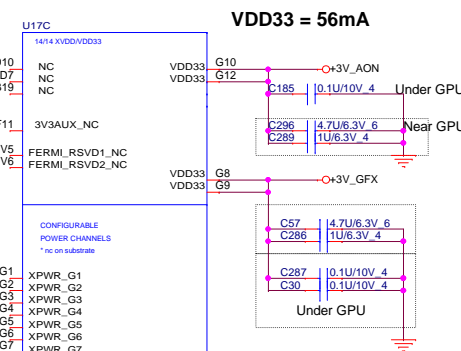
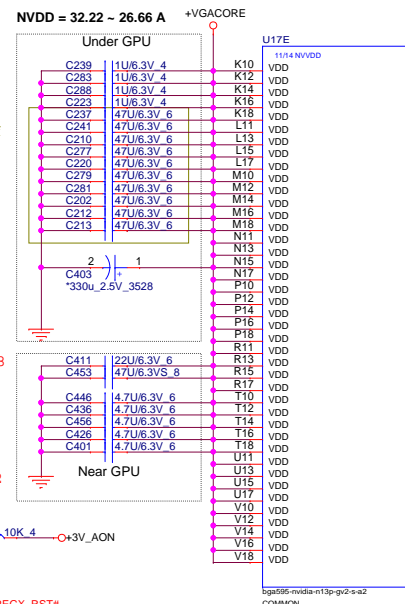
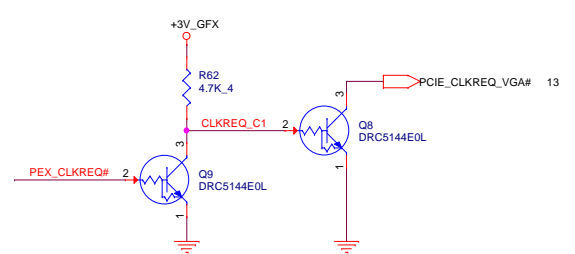
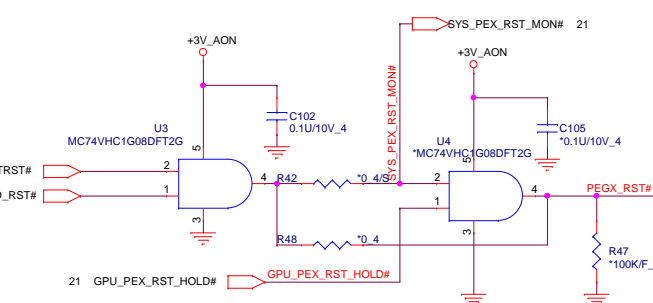
0602 Change  
4.7uF to 47uF

1230 Change C338  
size to 0603

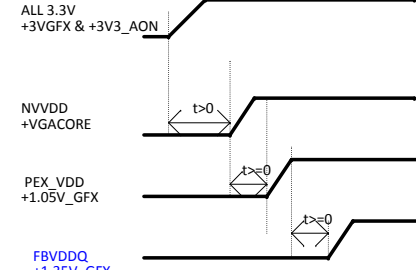
1230 Change C395,  
C370, C386, C349,  
C403 size to 0402



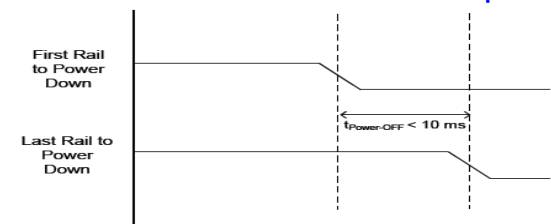
0611  
Change R196, R155 to short pad

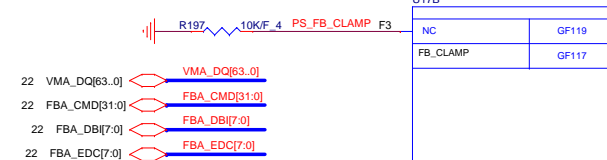


Power up sequence



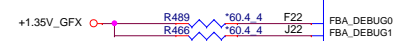
Power down sequence





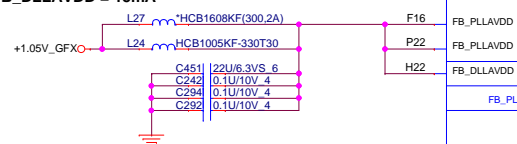
0310 Del  
R631/R644/R612/R670/R600  
for nVIDIA review

- FBA\_CMD0 C27
- FBA\_CMD1 C26
- FBA\_CMD2 E24
- FBA\_CMD3 F24
- FBA\_CMD4 D27
- FBA\_CMD5 D26
- FBA\_CMD6 F25
- FBA\_CMD7 F26
- FBA\_CMD8 F23
- FBA\_CMD9 G22
- FBA\_CMD10 G23
- FBA\_CMD11 G24
- FBA\_CMD12 F27
- FBA\_CMD13 G26
- FBA\_CMD14 G27
- FBA\_CMD15 G26
- FBA\_CMD16 M24
- FBA\_CMD17 M23
- FBA\_CMD18 K24
- FBA\_CMD19 K23
- FBA\_CMD20 M27
- FBA\_CMD21 M26
- FBA\_CMD22 M25
- FBA\_CMD23 K26
- FBA\_CMD24 K22
- FBA\_CMD25 J23
- FBA\_CMD26 J25
- FBA\_CMD27 J24
- FBA\_CMD28 K27
- FBA\_CMD29 K25
- FBA\_CMD30 J27
- FBA\_CMD31 J26



- 22 VMA\_CLK0 D24
- 22 VMA\_CLK0# D25
- 22 VMA\_CLK1 N22
- 22 VMA\_CLK1# M22

FB\_PLLAVDD = 55mA  
FB\_DLLAVDD = 15mA

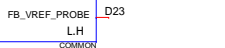


- FBA\_D0 E18
- FBA\_D1 F18
- FBA\_D2 E16
- FBA\_D3 F17
- FBA\_D4 D20
- FBA\_D5 D21
- FBA\_D6 F20
- FBA\_D7 E21
- FBA\_D8 E15
- FBA\_D9 D15
- FBA\_D10 F15
- FBA\_D11 F13
- FBA\_D12 C13
- FBA\_D13 B13
- FBA\_D14 E13
- FBA\_D15 D13
- FBA\_D16 B15
- FBA\_D17 C16
- FBA\_D18 A13
- FBA\_D19 A15
- FBA\_D20 B18
- FBA\_D21 A18
- FBA\_D22 A19
- FBA\_D23 C19
- FBA\_D24 B24
- FBA\_D25 C23
- FBA\_D26 A25
- FBA\_D27 A24
- FBA\_D28 A21
- FBA\_D29 B21
- FBA\_D30 C20
- FBA\_D31 C21
- FBA\_D32 R22
- FBA\_D33 R24
- FBA\_D34 T22
- FBA\_D35 R23
- FBA\_D36 N25
- FBA\_D37 N26
- FBA\_D38 N23
- FBA\_D39 N24
- FBA\_D40 V23
- FBA\_D41 V22
- FBA\_D42 T23
- FBA\_D43 U22
- FBA\_D44 Y24
- FBA\_D45 AA24
- FBA\_D46 Y22
- FBA\_D47 AA23
- FBA\_D48 AD27
- FBA\_D49 AB25
- FBA\_D50 AD26
- FBA\_D51 AC25
- FBA\_D52 AA27
- FBA\_D53 AA26
- FBA\_D54 W26
- FBA\_D55 Y25
- FBA\_D56 R26
- FBA\_D57 T25
- FBA\_D58 N27
- FBA\_D59 R27
- FBA\_D60 V26
- FBA\_D61 V27
- FBA\_D62 W27
- FBA\_D63 W25

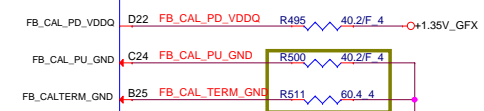
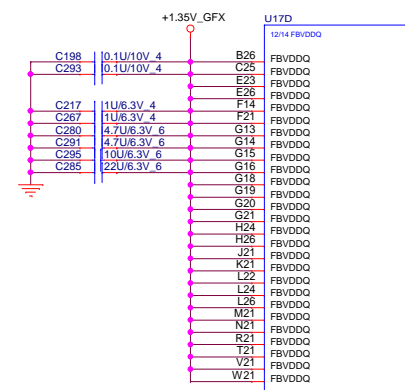
- FBA\_DQM0 D19
- FBA\_DQM1 D14
- FBA\_DQM2 C22
- FBA\_DQM3 P24
- FBA\_DQM4 W24
- FBA\_DQM5 AA25
- FBA\_DQM6 AA25
- FBA\_DQM7 U25

- FBA\_DQS\_WP0 E19
- FBA\_DQS\_WP1 C15
- FBA\_DQS\_WP2 B16
- FBA\_DQS\_WP3 B22
- FBA\_DQS\_WP4 R25
- FBA\_DQS\_WP5 W23
- FBA\_DQS\_WP6 AB26
- FBA\_DQS\_WP7 T26

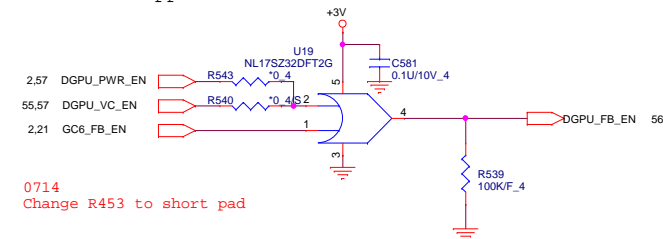
- FBA\_DQS\_RN0 F19
- FBA\_DQS\_RN1 C14
- FBA\_DQS\_RN2 A16
- FBA\_DQS\_RN3 A22
- FBA\_DQS\_RN4 C25
- FBA\_DQS\_RN5 Y22
- FBA\_DQS\_RN6 AB27
- FBA\_DQS\_RN7 C27



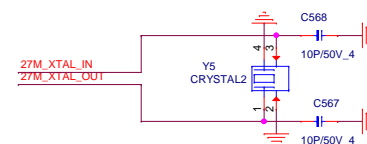
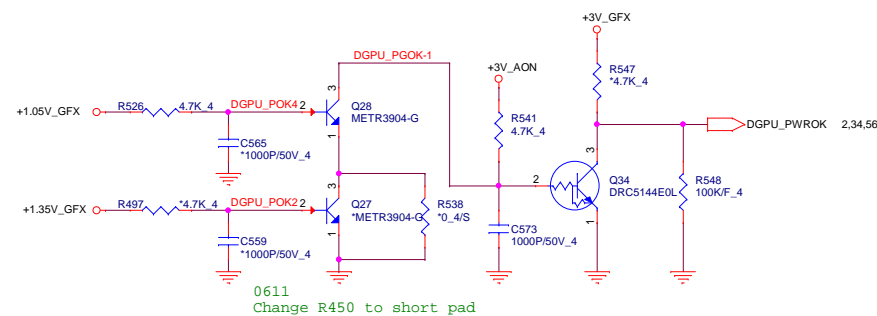
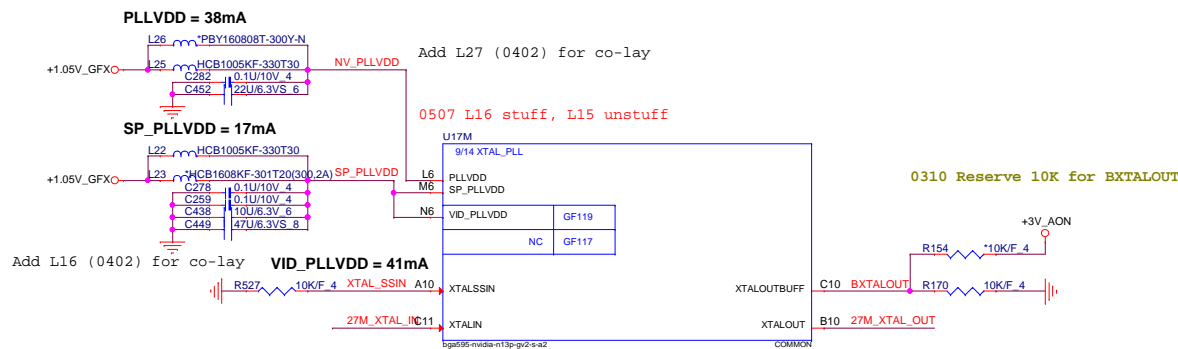
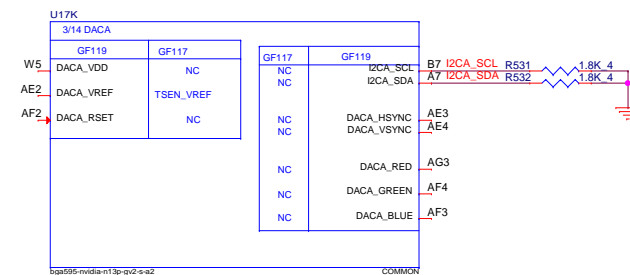
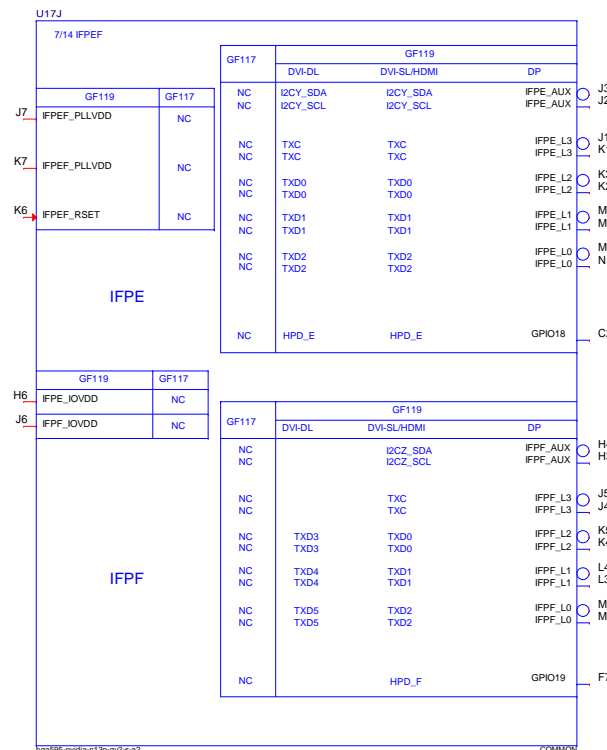
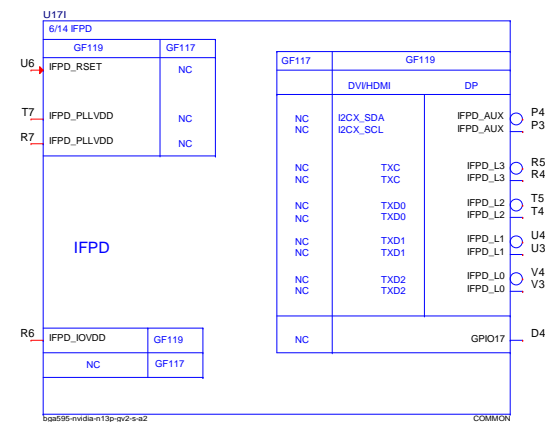
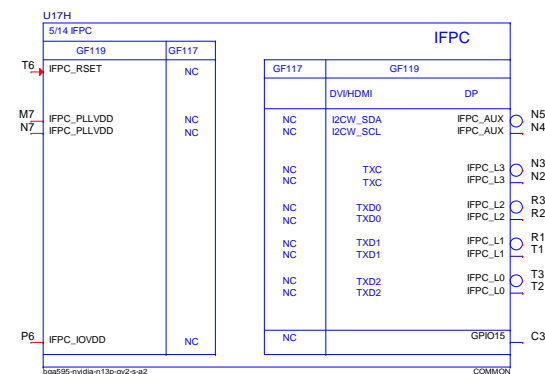
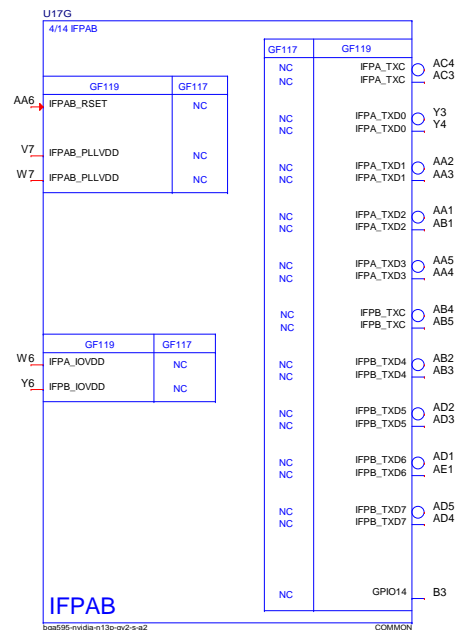
FBVDDQ + FBVDD = 3.116A

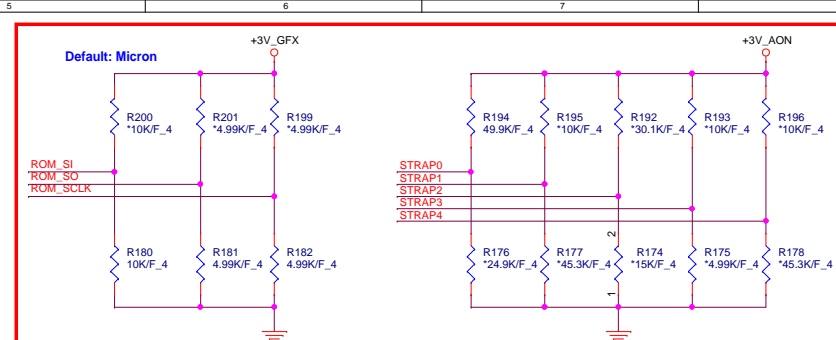


For support GC6 2.0



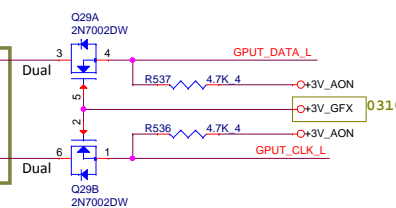
0714  
Change R453 to short pad





R180 for X32	HYNIX	0101	30.1k	CS33012FB1
	Micron	0001	10k	CS31002FB2
	SAMSUNG	0000	4.99k	CS24992FB2

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



ROM SI S F

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	Strapping	TOP B/S	QBC
0101	DDR4 256Mx32, 64bit, 8Gb	HYNIX	H5GC8H24MJR-T2C	0x5	AKD5QFUTW00	AKD5QFUTW00
0001	DDR4 256Mx32, 64bit, 8Gb	Micron	MT51U-256M32HF-60:A	0x1	AKG5LGUTL02	AKG5LGUTL02
0000	DDR4 256Mx32, 64bit, 8Gb	SAMSUNG	KA480325FB-HC03	0x0	AKG5QGD7503	AKG5QGD7503

The schematic diagram illustrates the power management section of the i.MX8M Mini EVK. It features several input signals connected to specific resistors and capacitors:

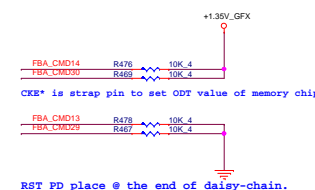
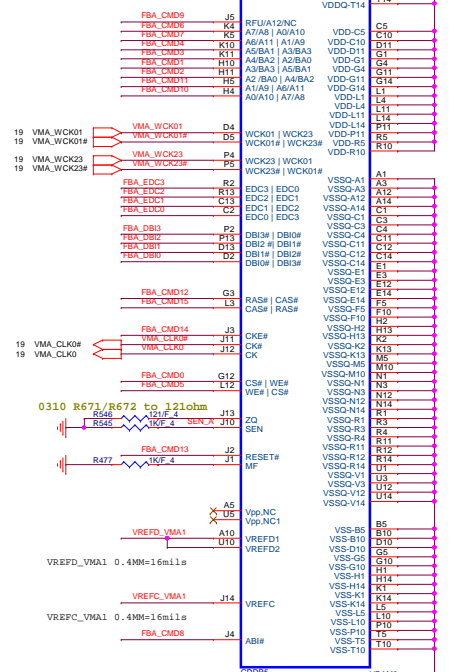
- PWR\_LEVEL**: Connected to R184 (0310) and a 100K/F capacitor.
- PSI**: Connected to R529 and a 10K/F capacitor.
- VGA\_OVT#**: Connected to R530 and a 10K/F capacitor.
- ALERT**: Connected to R171 and a 10K/F capacitor.
- GPU\_PEX\_RST\_HOLD#**: Connected to R173 and a 10K/F capacitor.
- GPU\_EVENT#\_GPU**: Connected to R191 and a 10K/F capacitor.
- GPU**: Connected to R191 and a 10K/F capacitor.
- +3V\_MAIN\_EN**: Connected to R528 and a 10K/F capacitor.
- GC6\_FB\_EN**: Connected to R166 and a 10K/F capacitor.
- JTAG\_TRST#**: Connected to R379 (0310) and a 10K/F capacitor.
- GPIO10\_VREF**: Connected to R485 and a 100K/F capacitor.

The diagram also shows a +3V\_AOI supply and a ground connection.

GPI/O	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D_VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMORY_VREF CONTROL
11	OUT	PWR_VID	GPU_CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

Memory Type	FBVDD/ FBVDDQ	Memory Density	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed CK Grade(MHz)	Memory Date Code Minimum	Status
GDDR5	1.35V/ 1.35V	256Mx16	Samsung	K4G41325FE-HC28	E-die	0x7	2500	N/A	Post production ready
			Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Production ready
			Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready
		Samsung	K4G41325FE-HC28	E-die	0x7	2500	N/A	Post production ready	
		128Mx32	Samsung	K4G41325FC-HC03	C-die	0x3	2500	N/A	Production ready
			Hynix	H5GC4H24AJR-T2C	A-die	0x6	2500	N/A	Production ready
			Micron	EDW4032BABG-60-F	A-die	0x4	2500	N/A	Production ready
		256Mx32	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
			Micron	MT51J256M32HF-60-A	A-die	0x1	2500	N/A	Production ready
		512Mx16	Samsung	K4G80325FB-HC03	B-die	0x0	2500	N/A	Production ready
			Micron	MT51J256M32HF-60-A	A-die	0x1	2500	N/A	Production ready

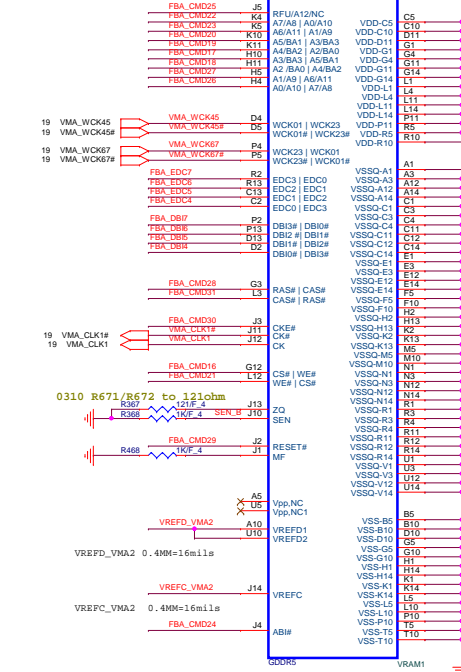
## MF=0 Non-mirrored



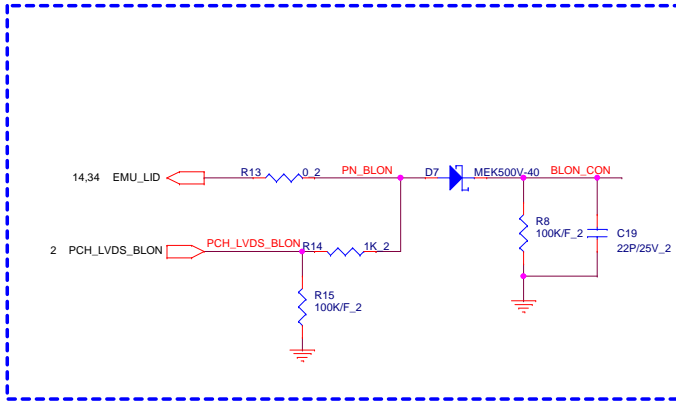
GDDR5 Mode H Mapping		
< 0-31 >	< 32-63 >	Memory
CM00	CM016	CS*
CM01	CM017	A3-B
CM02	CM018	A2-B
CM03	CM019	A1-B
CM04	CM020	A5-B
CM05	CM021	WE*
CM06	CM022	A7-A
CM07	CM023	A6-A
CM08	CM024	AB1*
CM09	CM025	A1-A
CM010	CM026	AB0*
CM011	CM027	A1-A
CM012	CM028	RAS*
CM013	CM029	RST*
CM014	CM030	CKS*
CM015	CM031	

```
GDDR5 CMD Mapping Table
<0..31> <32..63> MEMORY
```

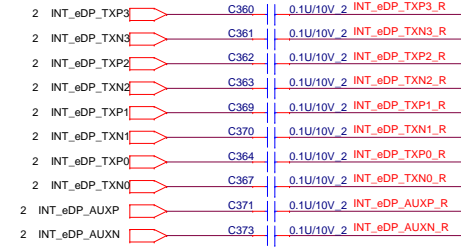
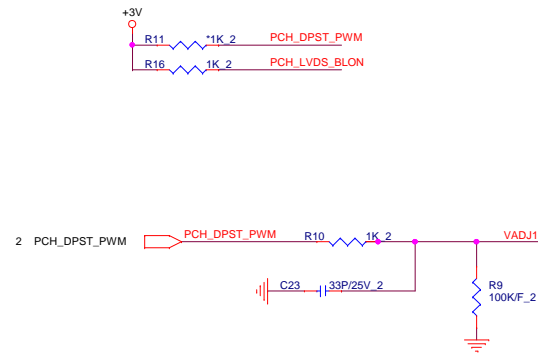
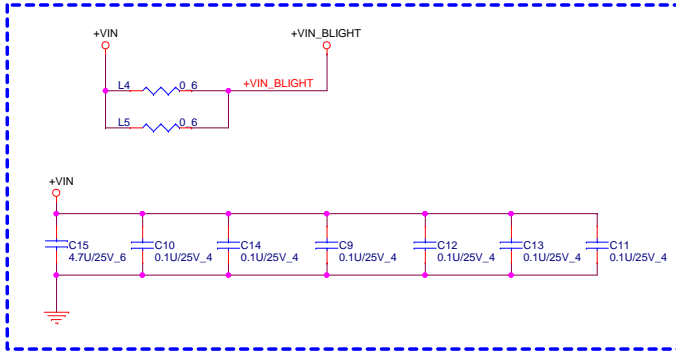
12	28
15	31
5	21
0	16
8	24
10	26
11	27
2	18
1	17
3	19
4	20
7	23
6	22
9	25
13	29
14	30



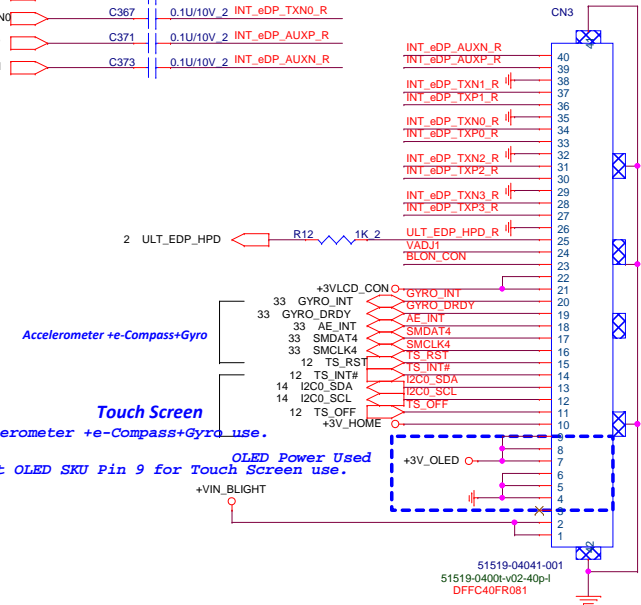
## LID Switch



## Panel Vin Cap



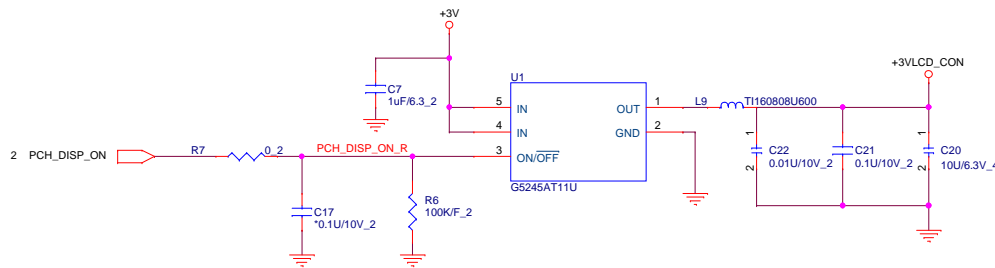
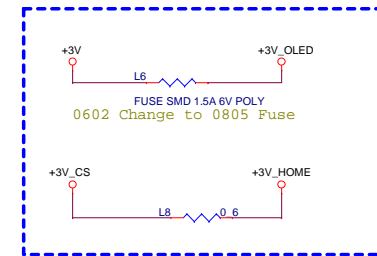
## eDP Conn.



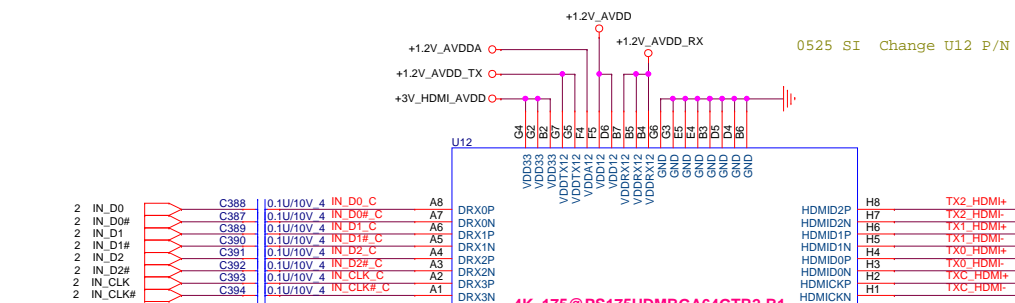
Accelerometer +e-Compass+Gyro  
Touch Screen  
+3V\_HOME Power for Accelerometer +e-Compass+Gyro use.

OLED Power Used  
No support OLED SKU Pin 9 for Touch Screen use.

## OLED Power Used



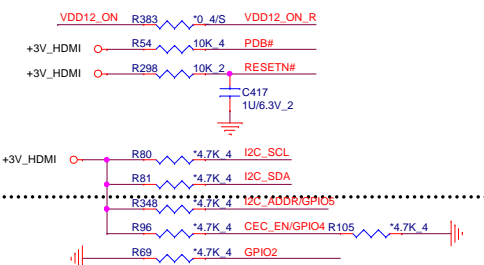
+3V 2,4,10,11,12,13,14,15,16,17,19,24,25,28,30,31,33,34,35,40,50,54,55  
+VIN 26,31,45,46,47,48,50,51,52,53,55,56,59  
+3V\_CS 33



Need Check Connection Jun 20160414

Jun Modify 20160414

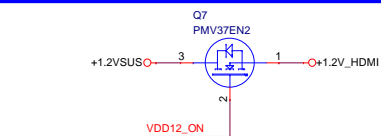
0323 modify



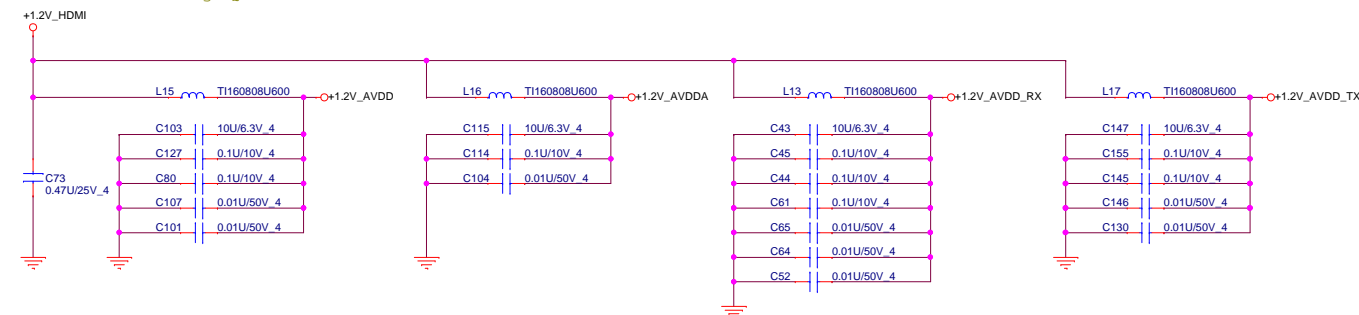
GPIO2: Firmware Initial Address, internal pull-up ~80K  
0: Start from Bank 7 1: Start from Bank 3 (default)

I2C\_ADDR/GPIO5: Control I2C slave address selection, internal pull-down ~80K  
0: 0x10h - 0x2Fh (default) 1: 0x90h - 0x9Fh, 0xD0h - 0xD7h

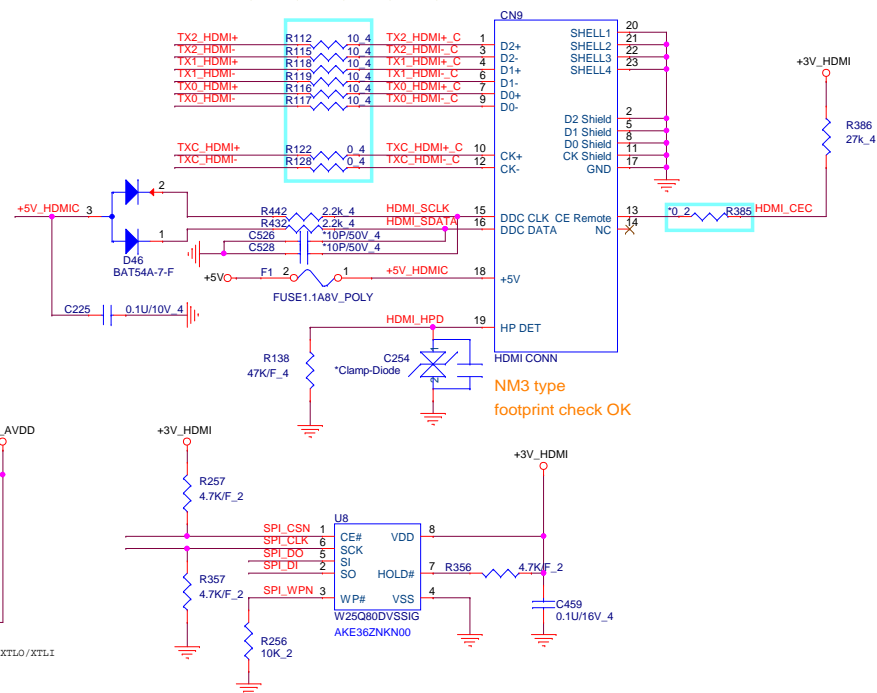
CEC\_EN/GPIO4: For debug purpose



0523 change Q7 to BAM37EN0000



0512 SI Change R112/R115/R116/R117/R118/R119 to 10ohm

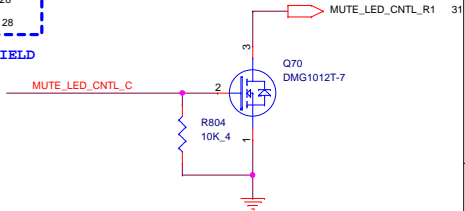
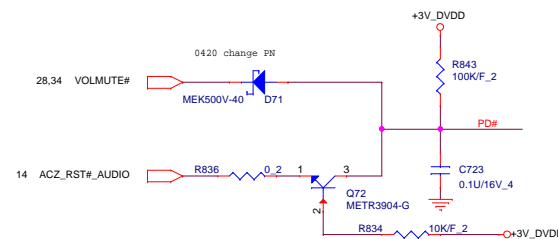
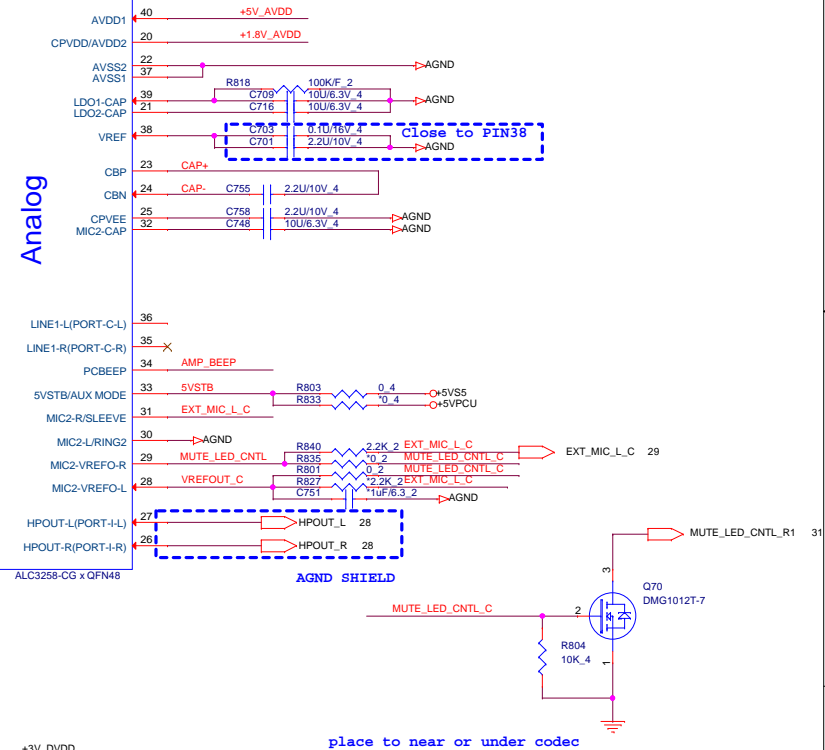
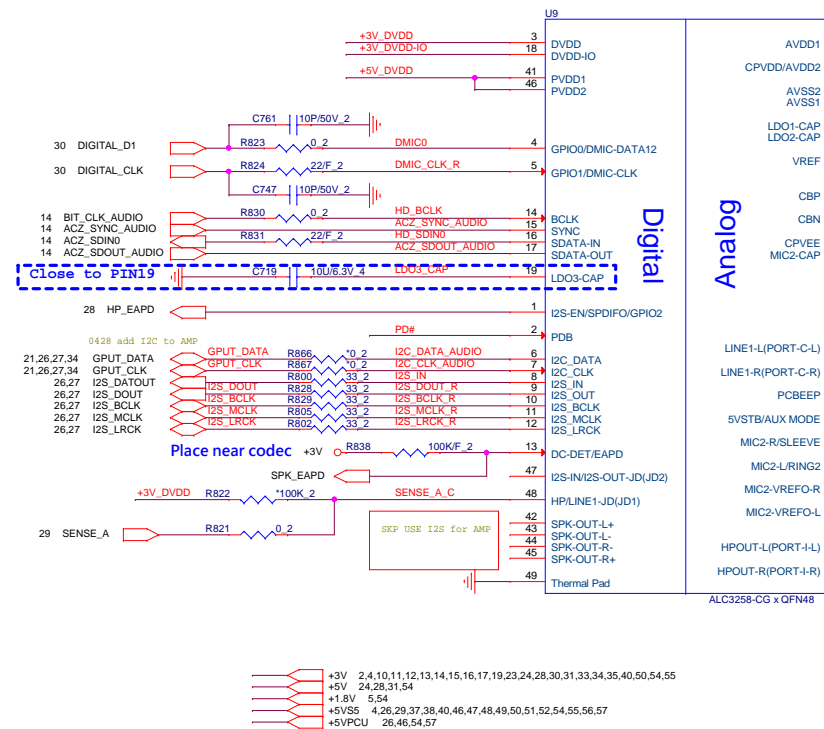
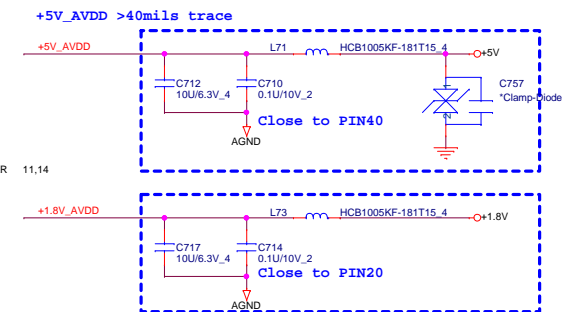
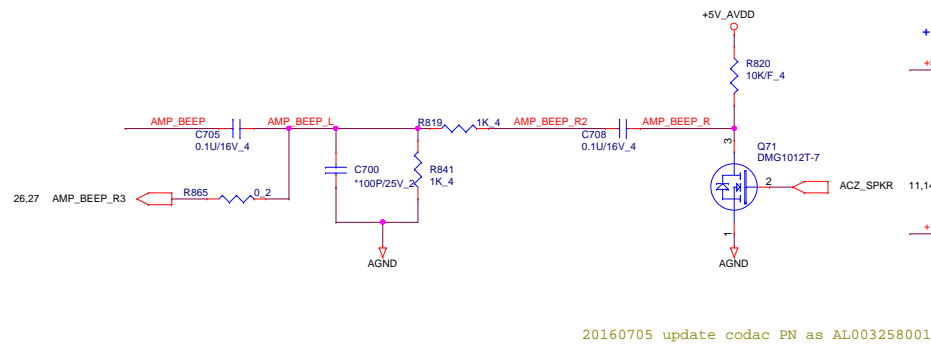
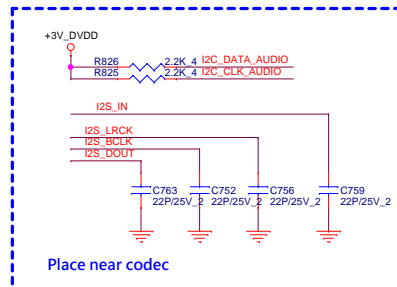
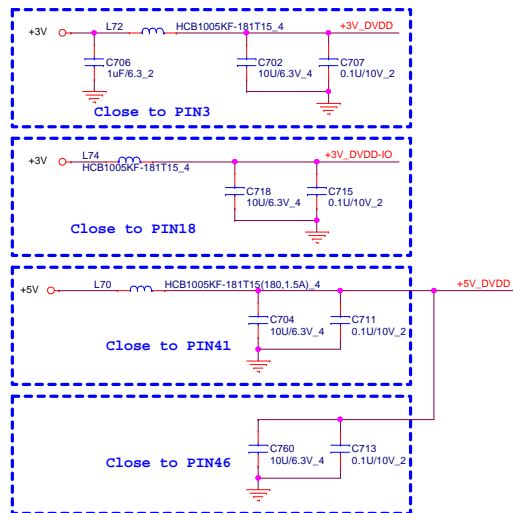


Add ground shielding between REXT and XTLO/XTL1

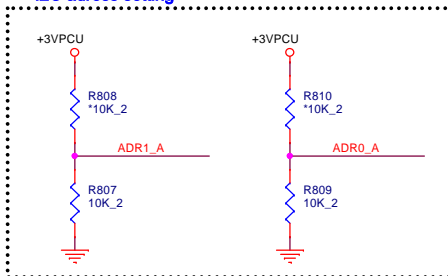


PROJECT : Pegasus  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI	1A
Date: Tuesday, July 19, 2016	Sheet 24 of 59	

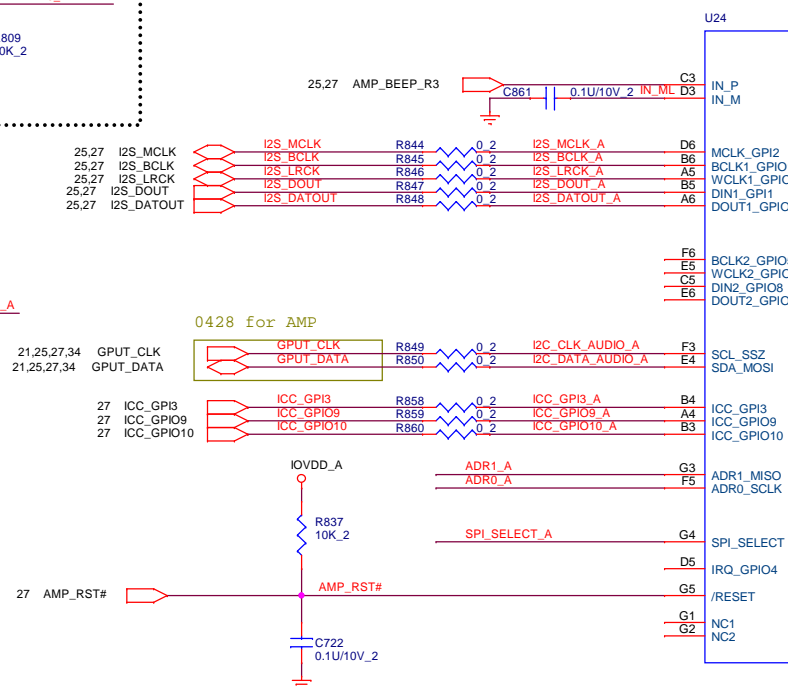


## I2C address setting



ADR0 / ADR1	
00 : 0x4C	10 : 0X4E
01 : 0X4D	11 : 0X4F

20160705 update AMP PN as AL002555T02

I2C/SPI select  
low:I2C  
high:SPITAS2555  
DSBGA 42P

need change PN

L75

2.2uH/3A\_4020

VBOOST\_A

VBOOST

VBAT

DVDD\_A

AVDD

IOVDD

VREG

SPK\_P

SPK\_M

VSENSE\_P

VSENSE\_M

PGND

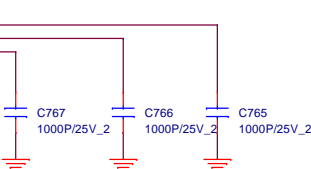
PGND\_B

PGND\_B

IOGND

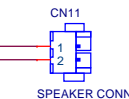
AGND

DGND

+5V\_SAMP +/- 5%  
S5 -- max output:100mA  
S3 -- max output:2A

0420 change C765/C766/C767

SPK-AMP-L

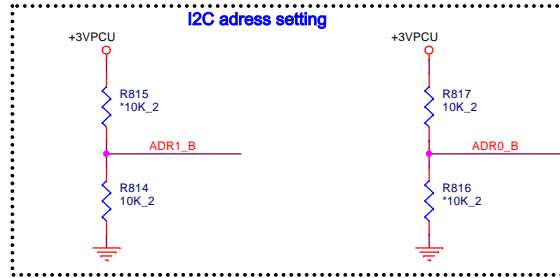
Wire White  
Wire Black

+5V_SAMP	27
+5VPCU	25,46,54,57
+5VSS	4,25,29,37,38,40,46,47,48,49,50,51,52,53,54,55,56,57
+VIN	23,31,45,46,47,48,50,51,52,53,55,56,59
+3VPCU	6,13,27,29,31,32,34,37,45,46,53,58
+5V	24,25,28,31,54
+1.8VPCU	27,46

PROJECT : X31  
Quanta Computer Inc.

Size	Document Number	Rev
A3	AUDIO AMP TAS2555	1A
Date: Tuesday, July 19, 2016	Sheet 26 of 59	

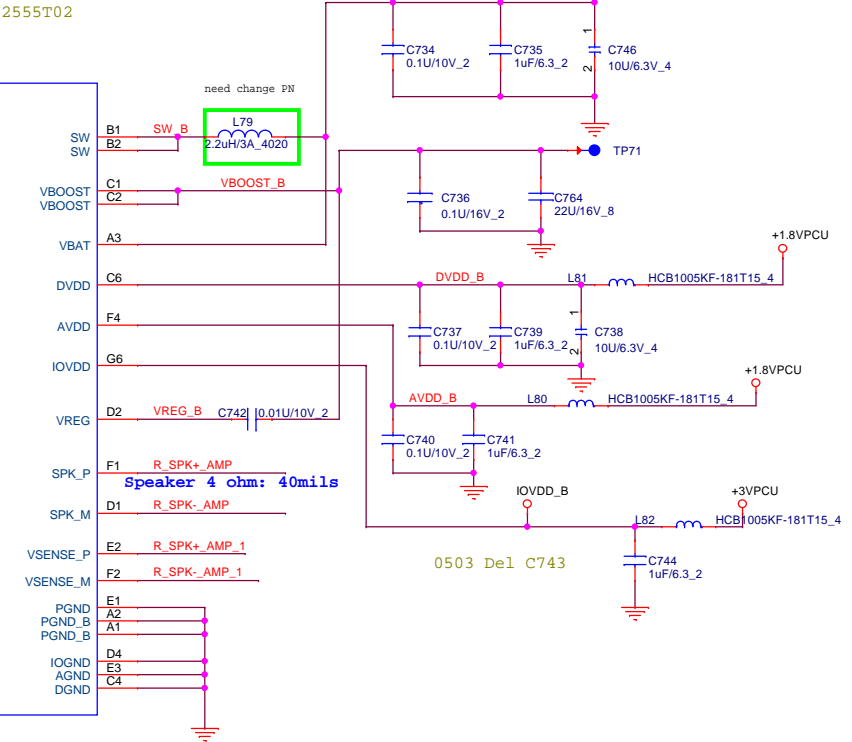
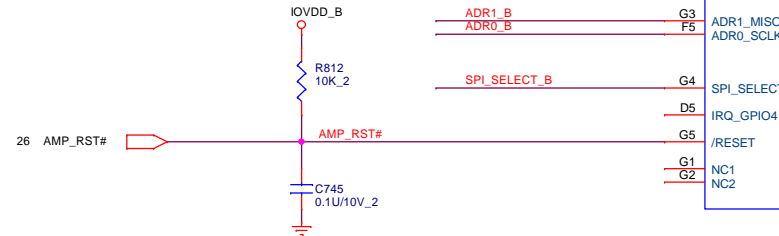
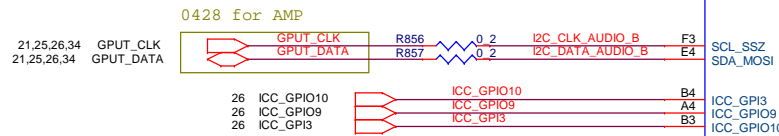
ADR0/ADR1	
00 : 0x4C	10 : 0X4E
01 : 0X4D	11 : 0X4F



20160705 update AMP PN as AL002555T02

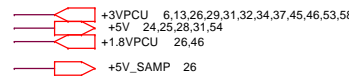
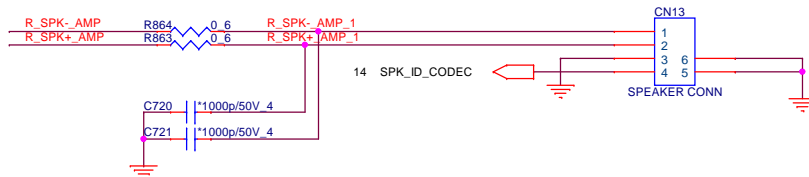


**TAS2555 DSBGA 42P**



**SPK-AMP-R**

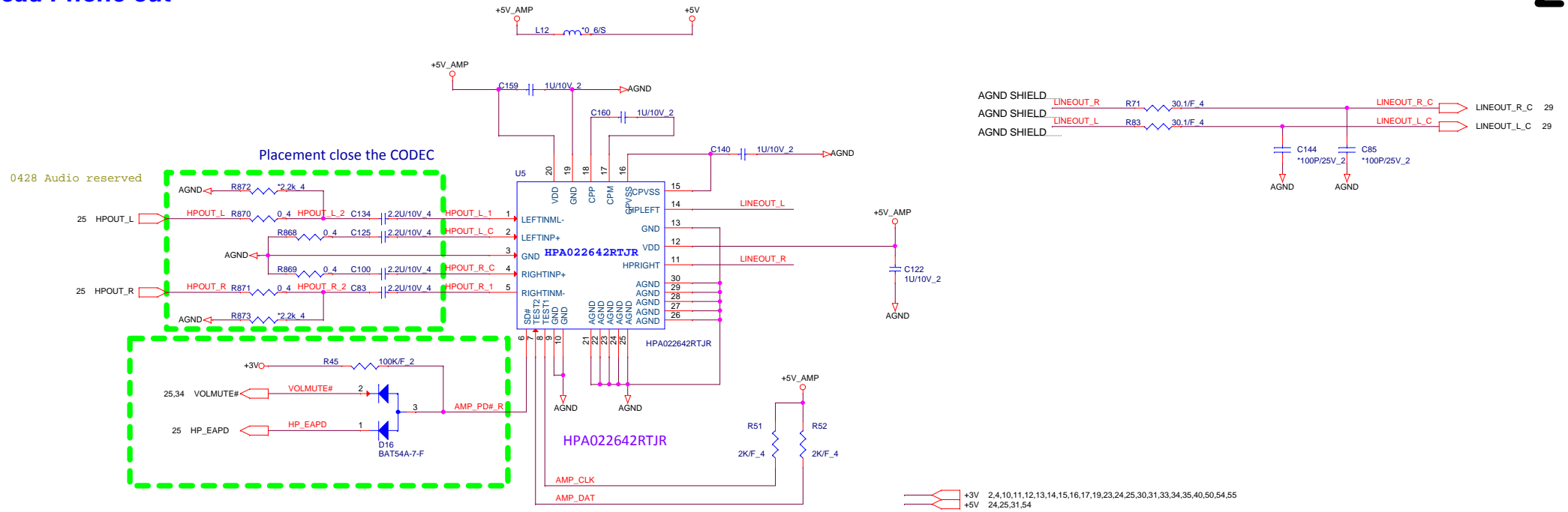
Wire Black  
Wire Red



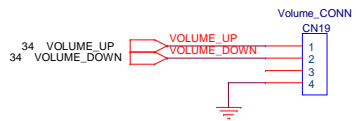
**PROJECT : X31**  
Quanta Computer Inc.

Size A3	Document Number AUDIO AMP TAS2555	Rev 1A
Date: Tuesday, July 19, 2016	Sheet 27 of 59	

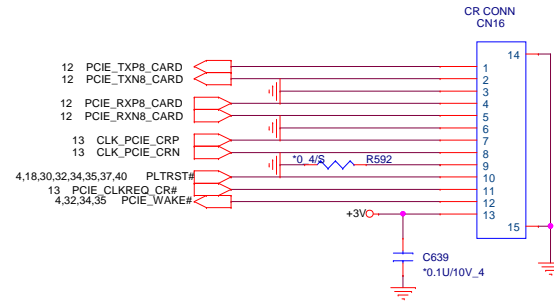
## Head Phone out



## Volume up/down Button

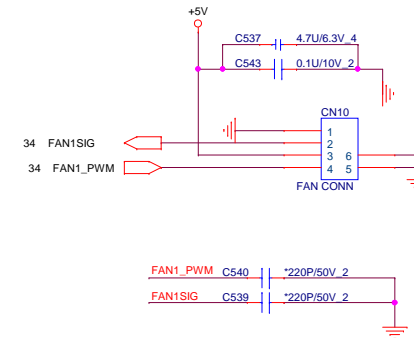


## Card Reader CONN



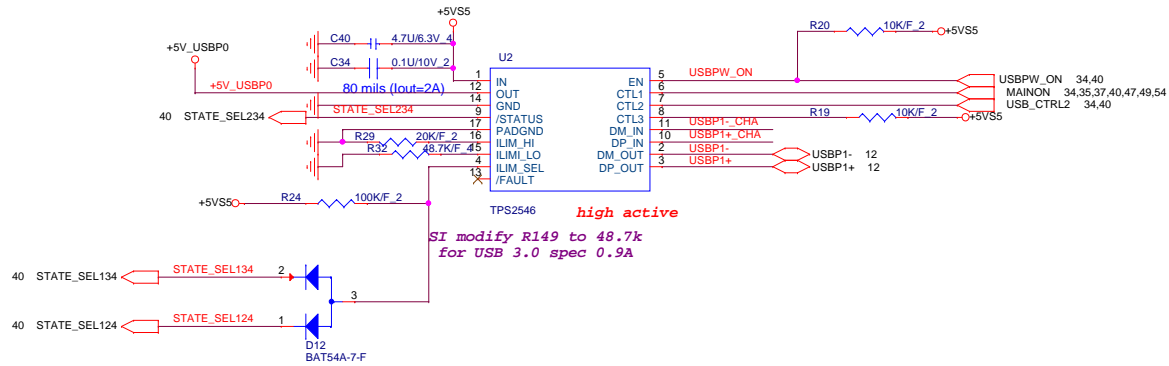
## FAN

0426 Update CN10/CN12 PN and FP



## For Daughter USB3.0 CN

+5VS5 4,25,26,37,38,40,46,47,48,49,50,51,52,54,55,56,57  
+3VPCU 6,13,26,27,31,32,34,37,45,46,53,58  
+5VPCU 25,26,46,54,57

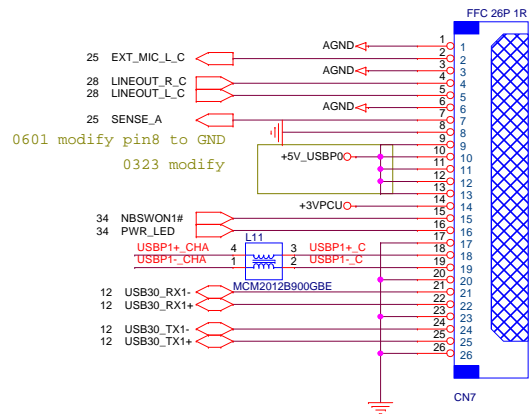


## UART for DEBUG

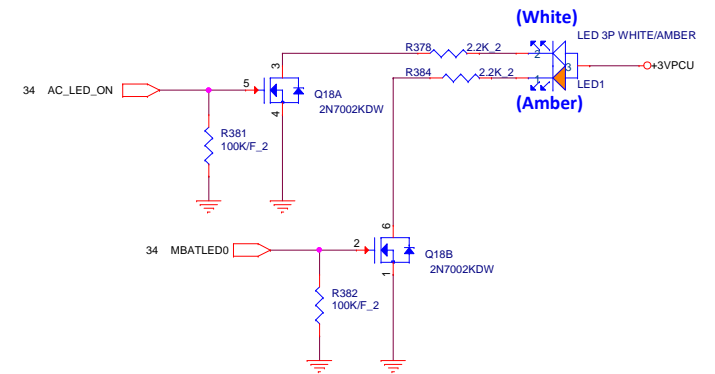
27

## UART for Win7 DEBUG

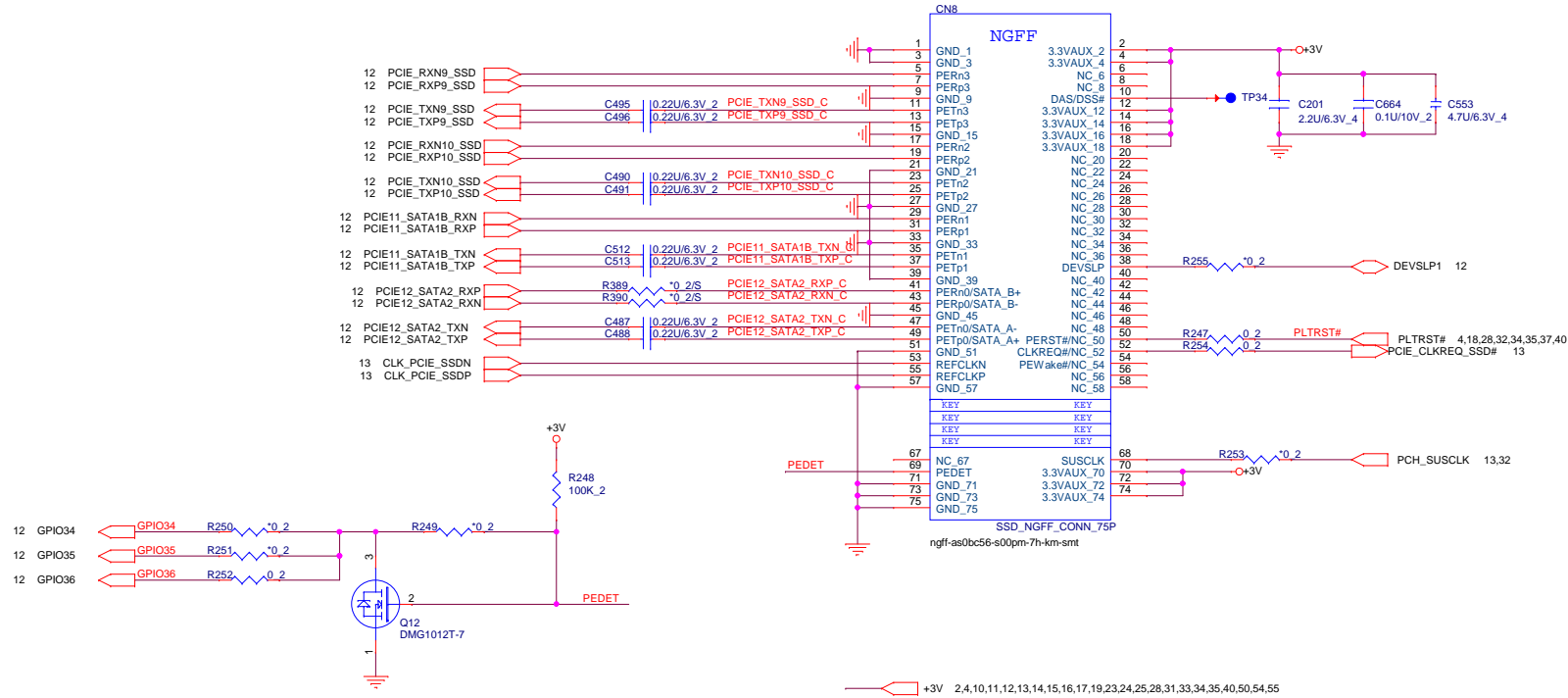
## Audio Combo Jack + USB3.0 Daughter Board+PW BTM



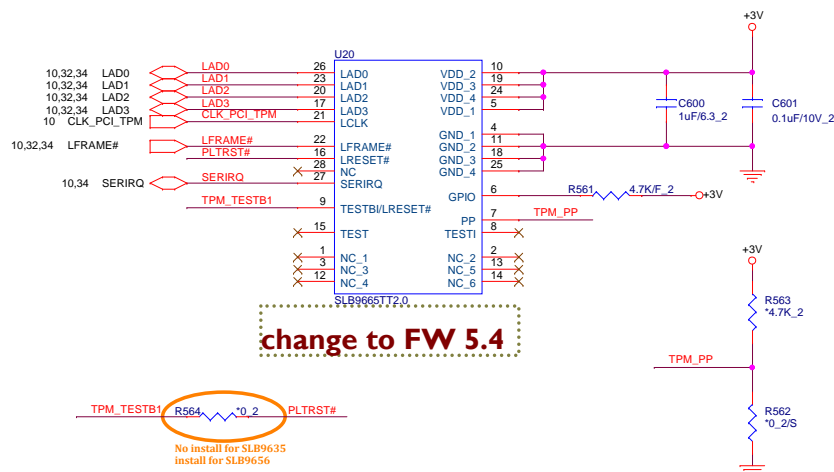
## AC\_IN / BATTERY LOW LED



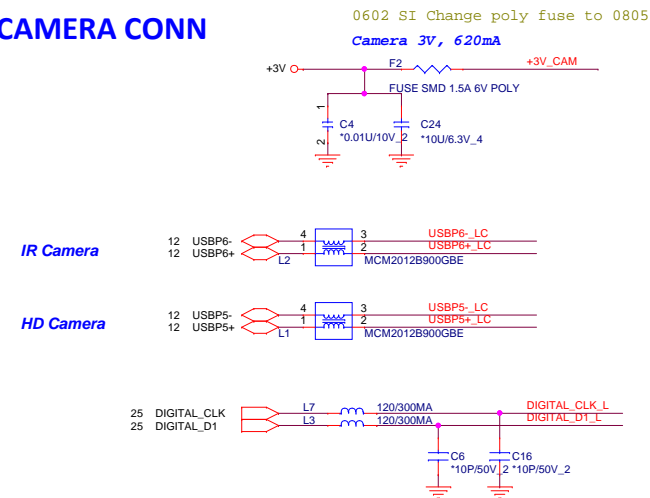
## SSD CONN

CONN: M KEY  
MODULE: N/A

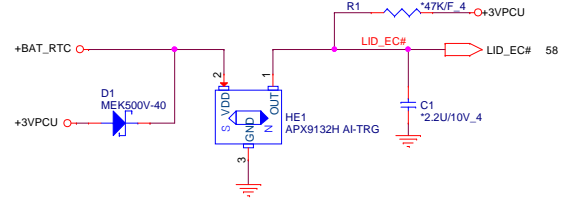
## TPM (2.0)



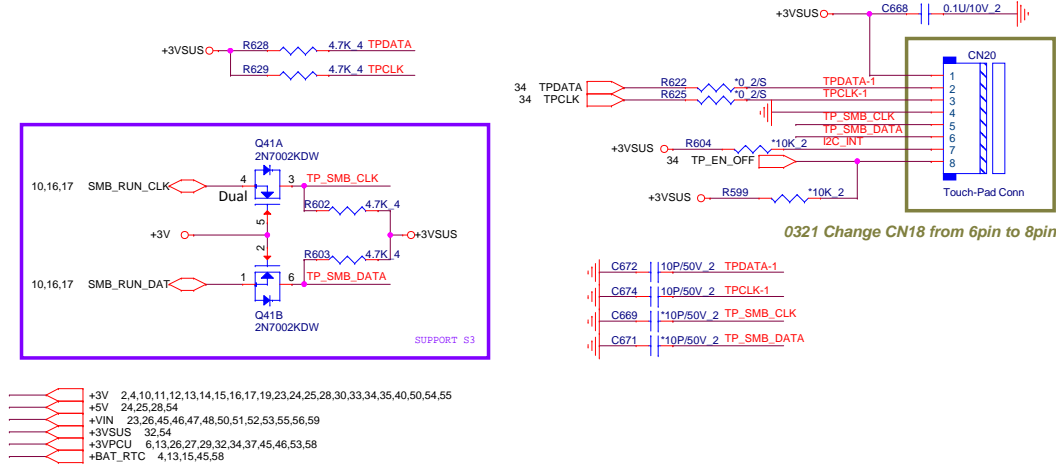
## CAMERA CONN



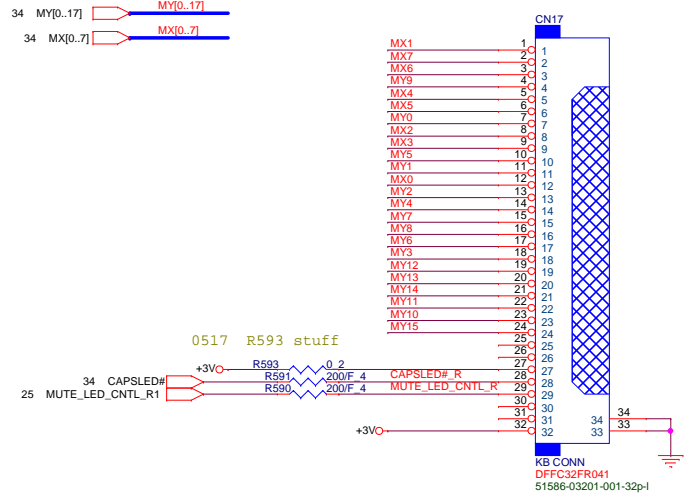
# LID switch



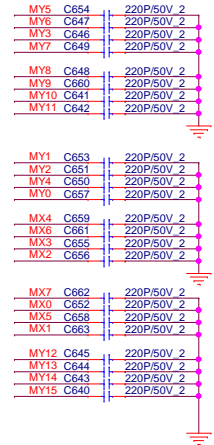
# Touch Pad Connector



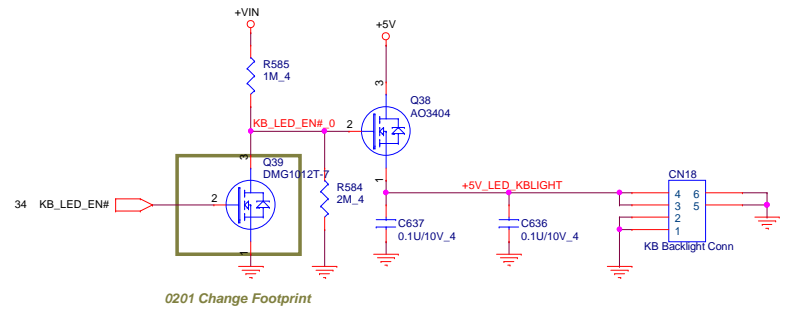
# KEYBOARD Con.



# KEYBOARD PULL-UP



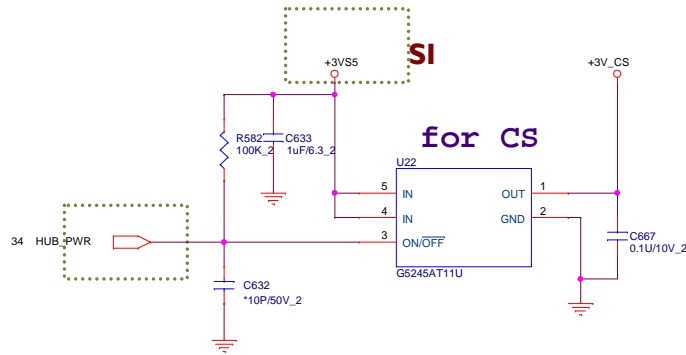
# KB backlight



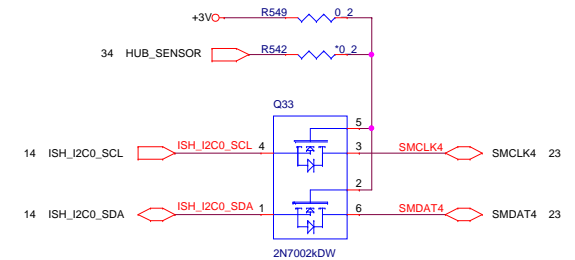
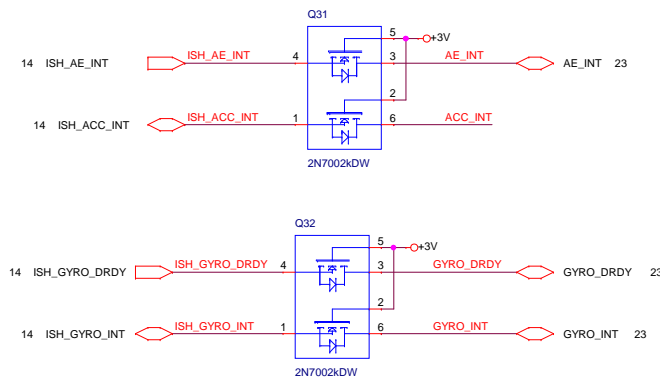
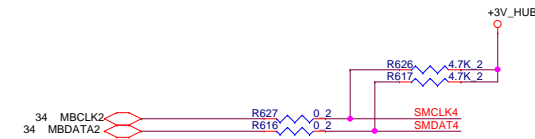
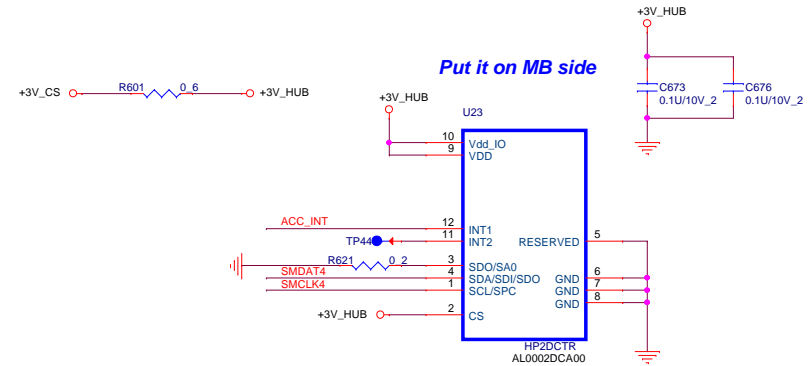
20160705 Del Q40,R589,MUTE\_LED\_EC



# Accelerometer Sensor

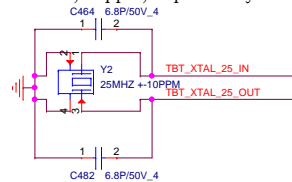


+3V 2,4,10,11,12,13,14,15,16,17,19,23,24,25,28,30,31,34,35,40,50,54,55  
 +3VS5 4,15,32,34,35,36,39,45,46,47,48,49,53,54,57  
 +3VSUS 31,32,54  
 +3V\_CS 23





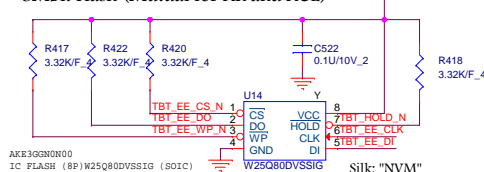
## 25MHz, 30ppm, 20pF AR Crystal



## Jun 20160124 Modify



## 8Mbit Flash (Mutual for AR and ACE)



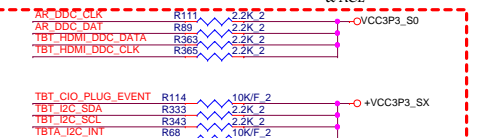
AKR30GN0N00

1C FLASH (8P) W25Q80DVSSIG (SO1C)

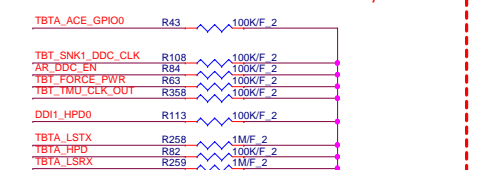
Silk: "NVM"

SPI/EE: AR to/from NVM

&amp; ACE



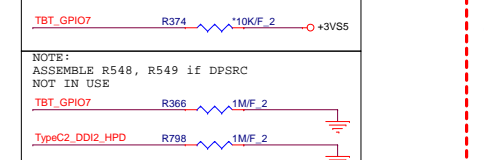
## Jun Modify 20160414



## Jun Modify 20160601

TBT\_SRC\_CFG1 = 0, AUX CONNECTS TO AR

TBT\_SRC\_CFG1 = 1, ddc CONNECTS TO AR



NOTE: ASSEMBLE R548, R549 if DPSRC NOT IN USE

TBT\_GPIO7

TypeC2\_DDI2\_HPD

IF SOME OF GPIOs ARE NOT IN USE FOLLOW TABLE BELOW:

GPIO	TERMINATION	Power Rail
GPIO_0	10K PU	VCC3V3_LC
GPIO_1	10K PU	VCC3V3_LC
GPIO_2	100K PD	VCC3V3_LC
GPIO_3	100K PD	VCC3V3_LC
GPIO_4	10K PU	VCC3V3_LC
GPIO_5	10K PU	VCC3V3_LC
GPIO_6	100K PD	VCC3V3_LC
GPIO_7	100K PD	VCC3V3_LC
GPIO_8	100K PD	VCC3V3_LC
POC_GPIO_0	10K PU	VCC3V3_TBT_SX
POC_GPIO_1	10K PU	VCC3V3_TBT_SX
POC_GPIO_2	100K PD	VCC3V3_TBT_SX
POC_GPIO_3	100K PD	VCC3V3_TBT_SX
POC_GPIO_4	10K PU	VCC3V3_TBT_SX
POC_GPIO_5	10K PU	VCC3V3_TBT_SX
POC_GPIO_6	100K PD	VCC3V3_TBT_SX

## NOTE:

SNK0\_DDC\_data/clk ?connect to 2k PU only if SRC0 is connected and support HDMI (a.i HDMI or DP++ connector). Otherwise can be 100k PD.

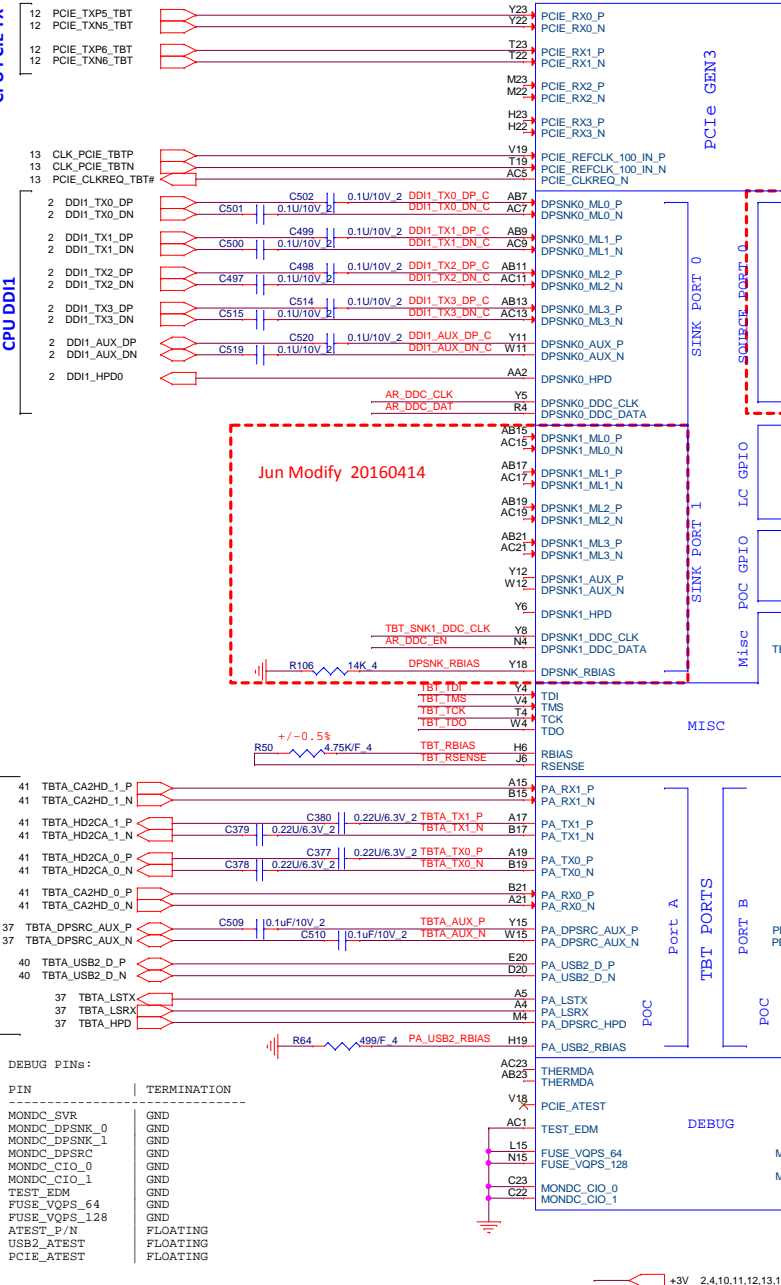
SNK1\_DDC\_data ?connect to 100k PD. If SRC0 support HDMI, connect as SNK0\_CFG1 to GPU and/or appropriate AUX/DDC demux control

SNK1\_DDC\_clk ?connect to 100k PD.

CPU PCIe TX

CPU DDI1

TBT PORT A



PCIe GEN3

SINK PORT 0

SINK PORT 1

MISC

Port A

Port B

Port C

Port D

Port E

Port F

Port G

Port H

Port I

Port J

Port K

Port L

Port M

Port N

Port O

Port P

Port Q

Port R

Port S

Port T

Port U

Port V

Port W

Port X

Port Y

Port Z

Port AA

Port AB

Port AC

Port AD

Port AE

Port AF

Port AG

Port AH

Port AI

Port AJ

Port AK

Port AL

Port AM

Port AN

Port AO

Port AP

Port AQ

Port AR

Port AS

Port AT

Port AU

Port AV

Port AW

Port AX

Port AY

Port AZ

Port BA

Port BB

Port BC

Port BD

Port BE

Port BF

Port BG

Port BH

Port BI

Port BJ

Port BK

Port BL

Port BM

Port BN

Port BO

Port BP

Port BQ

Port BR

Port BS

Port BT

Port BU

Port BV

Port BW

Port BX

Port BY

Port BZ

Port CA

Port CB

Port CC

Port CD

Port CE

Port CF

Port CG

Port CH

Port CI

Port CJ

Port CK

Port CL

Port CM

Port CN

Port CO

Port CP

Port CQ

Port CR

Port CS

Port CT

Port CU

Port CV

Port CW

Port CX

Port CY

Port CZ

Port DA

Port DB

Port DC

Port DD

Port DE

Port DF

Port DG

Port DH

Port DI

Port DJ

Port DK

Port DL

Port DM

Port DN

Port DO

Port DP

Port DQ

Port DR

Port DS

Port DT

Port DU

Port DV

Port DW

Port DX

Port DY

Port DZ

Port EA

Port EB

Port EC

Port ED

Port EE

Port EF

Port EG

Port EH

Port EI

Port EJ

Port EK

Port EL

Port EM

Port EN

Port EO

Port EP

Port EQ

Port ER

Port ES

Port ET

Port EU

Port EV

Port EW

Port EX

Port EY

Port EZ

Port FA

Port FB

Port FC

Port FD

Port FE

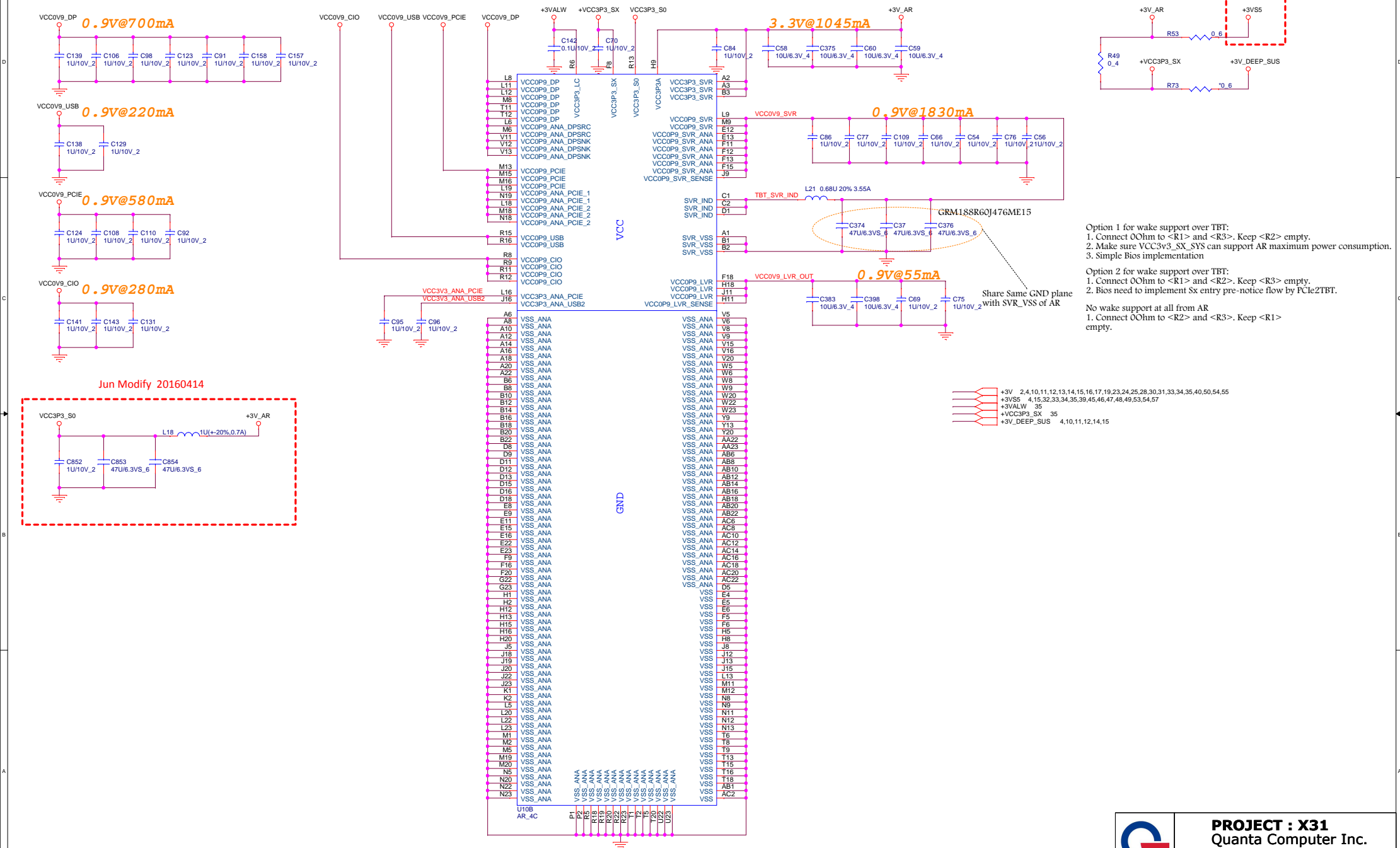
Port FG

Port FH

Port FI

Port FJ

Port FK



# Port A Controller - ACE

TPS65982 (ACE) -  
USB3.1 PD

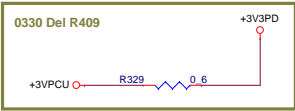
0318 Del R414 R413

PP\_EXT circuit

W = 200 mils

35

Supporting up to 60W to VBUS  
ACE configuration:  
\* SENSEP & SENSEN should be  
connected to 10mOhm resistor  
\* PP\_HV should be tied to GND.



0330

I2C\_ADDR  
'0' - Sets ACE as Primary  
'1' - Sets ACE as Secondary

I2C1  
Connect to AR and PD2  
I2C2  
Directly to EC

Primary

W = 120 mils

0512 SI SWAP TBTA\_SENN/P  
20160705 Modify PD PN to AJ659820T02

Type-C USB1 Top

Type-C USB1 Bot

Jun Modify 20160414

Dual Power Role:  
BUSPOWERZ < 0.8v --> Receiving VBUS  
Power through the PP\_EXT path (Host  
Charging mode from USB)  
BUSPOWERZ > 2.4v --> Disabling system  
power from VBUS (Host providing power  
to the USB)

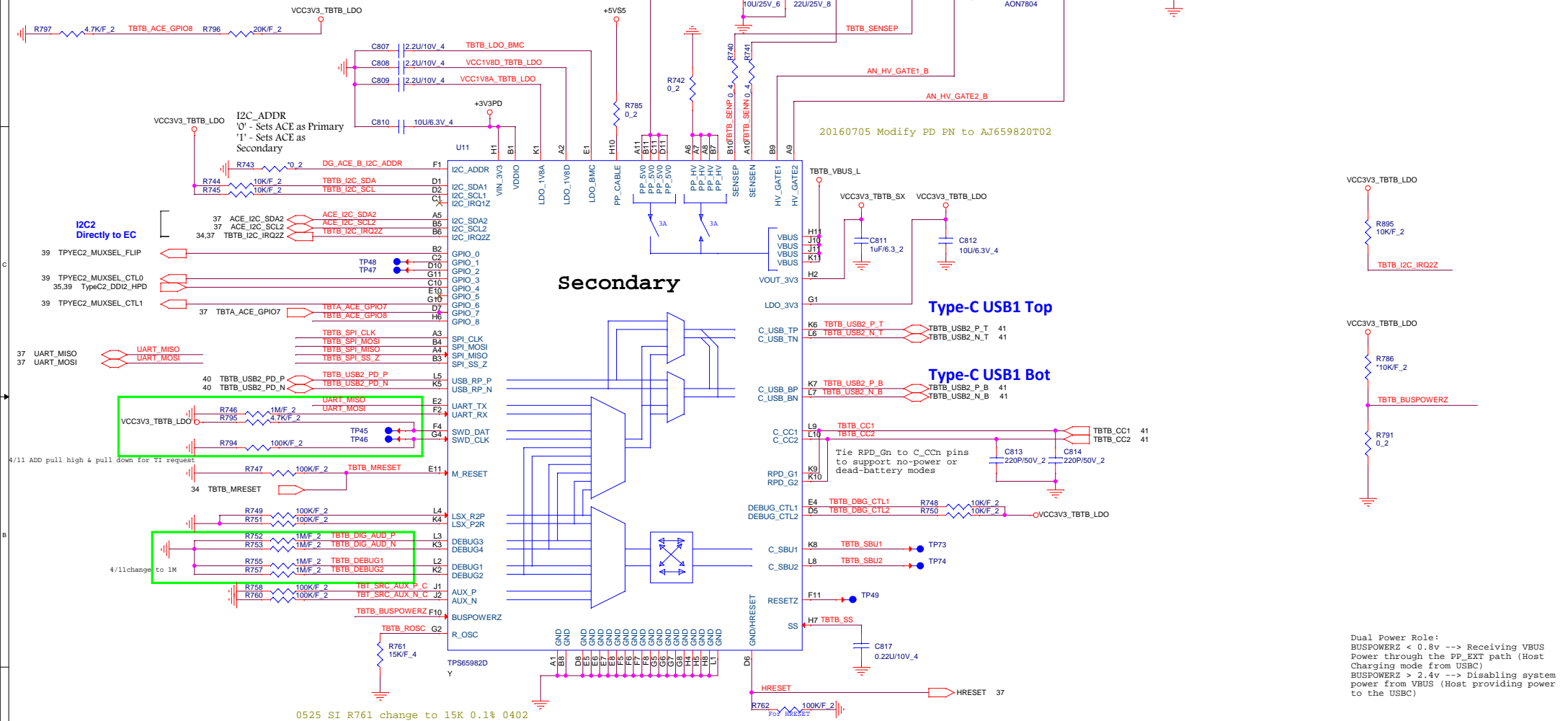
NOTE:  
GPIO MAPPING SUBJECT TO  
CHANGES BASED ON VENDOR  
REQUIREMENTS. PLEASE REFER TO  
DATASHEET FOR MORE DETAILS.



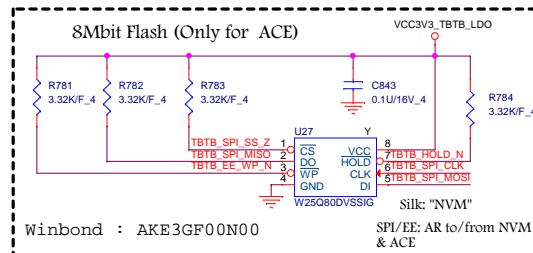
PROJECT : X31  
Quanta Computer Inc.

Size	Document Number	Rev
	AR - TBT (USB2 & DP Part)	1A
Date: Tuesday, July 19, 2016	Sheet 37 of 59	

### Port B Controller - ACE

TPS65982 (ACE) - USB3.1  
PD

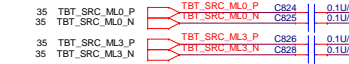
NOTE:  
GPIO MAPPING SUBJECT TO  
CHANGES BASED ON VENDOR  
REQUIREMENTS. PLEASE REFER TO  
DATASHEET FOR MORE DETAILS.



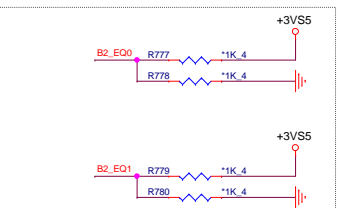
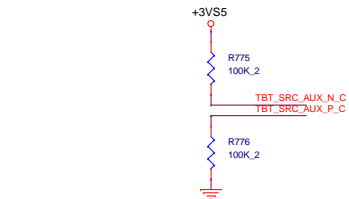
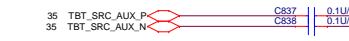
## 4 Level Input:

- L: Option1 Tie 1Kohm 5% to GND  
Option2 Directly tie to GND  
R: Tie 20kohm 5% to GND  
F: Float(leave pin open)  
1: Option1 Tie 1Kohm 5% to Vcc  
Option2 Directly tie to Vcc

## DisplayPort Source

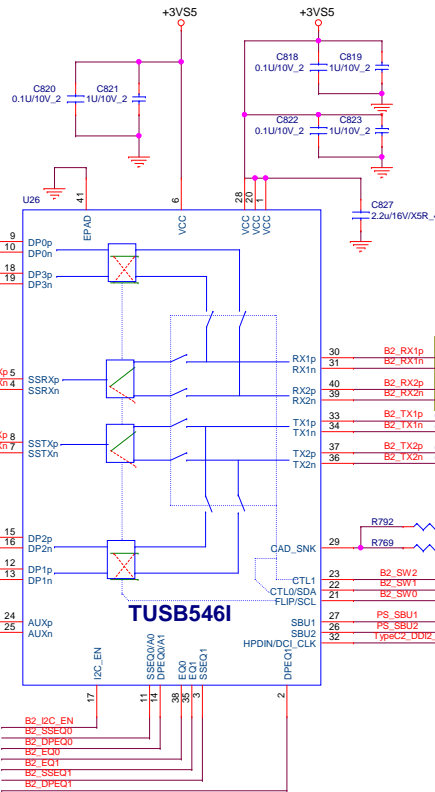


## USB3.0 HOST



EQ0,EQ1 : USB receiver equalizer gain  
for downstream facing RX1 & RX2  
F,F(Default)

I2C Programming or pin strap programming select.  
I2C is only disable when this pin is '0'  
0 : Pin Strap(I2C disable)(Default)  
1 : TI test mode(I2C enable at 3.3V)  
F : I2C enabled at 1.8V  
1 : I2C enabled at 3.3V



CTL1	CTL0	FLIP	TUSB546 Mode Selection
L	L	L	Chip Power Down
L	L	H	Chip Power Down
L	H	L	One Port USB 3.1 - No Flip
L	H	H	One Port USB 3.1 - With Flip
H	L	L	4 Lane DP - No Flip
H	L	H	4 Lane DP - With Flip
H	H	L	One Port USB 3.1 + 2 Lane DP - No Flip
H	H	H	One Port USB 3.1 + 2 Lane DP - With Flip

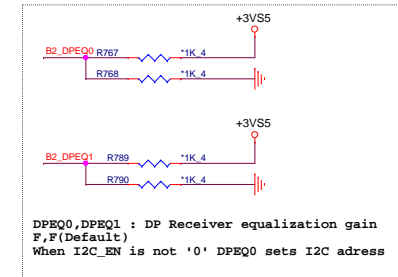
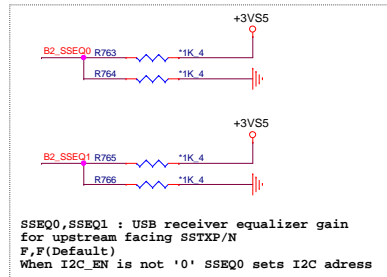
## TUSB546 Pin Control Mode

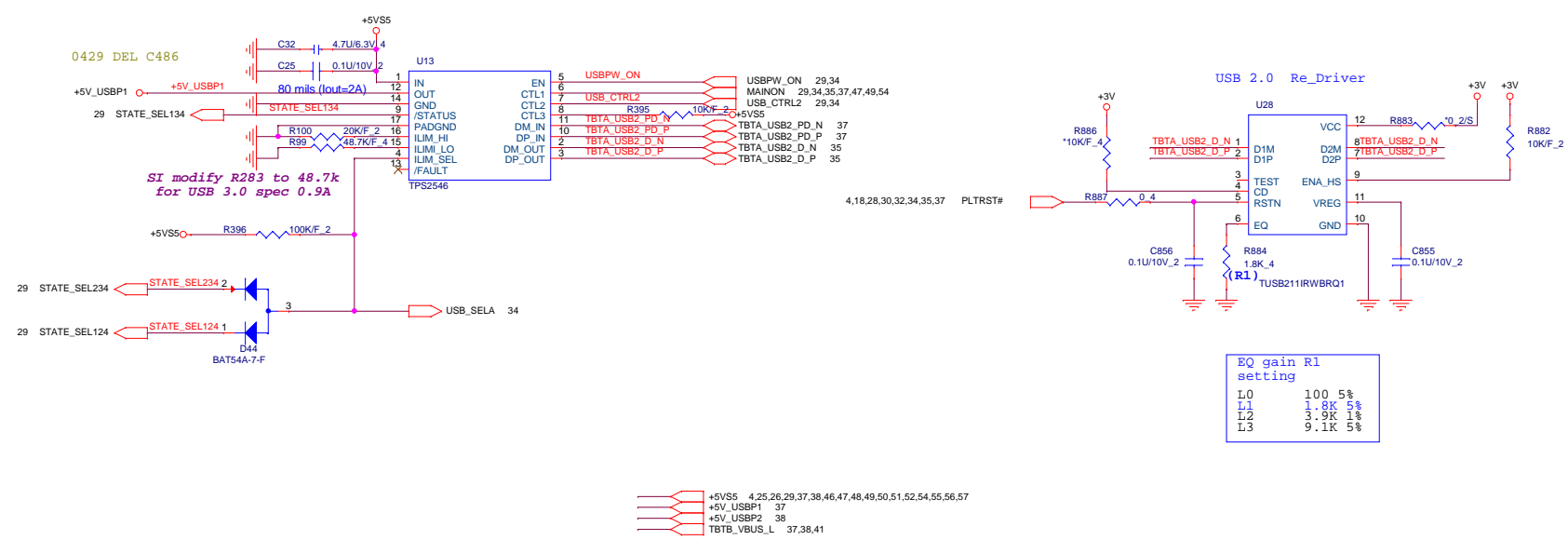
CTL1	FLIP	AUX Select
H	L	AUXP->SBU1, AUXN->SBU2
H	H	AUXP->SBU2, AUXN->SBU1
L>2ms	X	One Port USB 3.1 - No Flip

## AUX Pin Control Mode

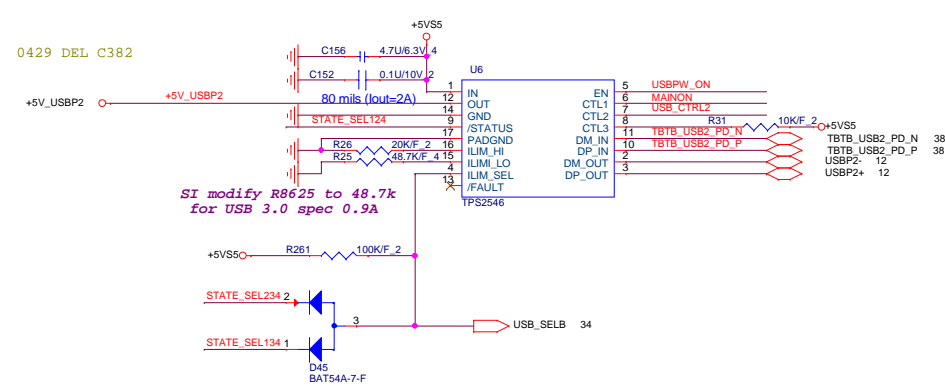
Table 8-7 TUSB546 Receiver Equalization GPIO Control

USB3.1 Downstream Facing Ports			USB 3.1 Upstream Facing Ports			All DisplayPort Lanes		
EQ1 pin Level	EQ0 pin Level	EQ GAIN @2.5GHz (dB)	SSEQ1 pin Level	SSEQ0 pin Level	EQ GAIN @2.5GHz (dB)	DPEQ1 pin Level	DPEQ0 pin Level	EQ GAIN @2.5GHz (dB)
0	0	0	0	0	0	0	0	0
0	R	1	0	R	1	0	R	1
0	F	2	0	F	2	0	F	2
0	1	3	0	1	3	0	1	3
R	0	4	R	0	4	R	0	4
R	R	5	R	R	5	R	R	5
R	F	6	R	F	6	R	F	6
R	1	7	R	1	7	R	1	7
F	0	8	F	0	8	F	0	8
F	R	9	F	R	9	F	R	9
F	1	10	F	1	10	F	1	10
F	F	11	F	F	11	F	F	11
1	0	12	1	0	12	1	0	12
1	R	13	1	R	13	1	R	13
1	F	14	1	F	14	1	F	14
1	1	15	1	1	15	1	1	15

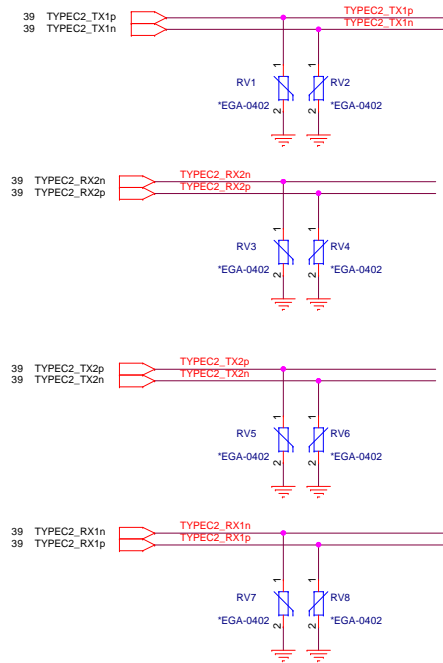




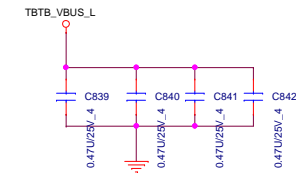
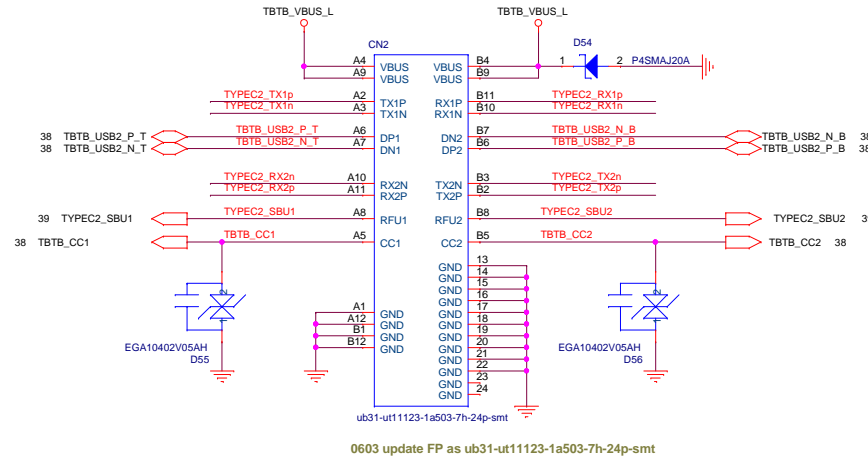
# PortB Support BC1.2



## Type C2\_HSIO\_ESD

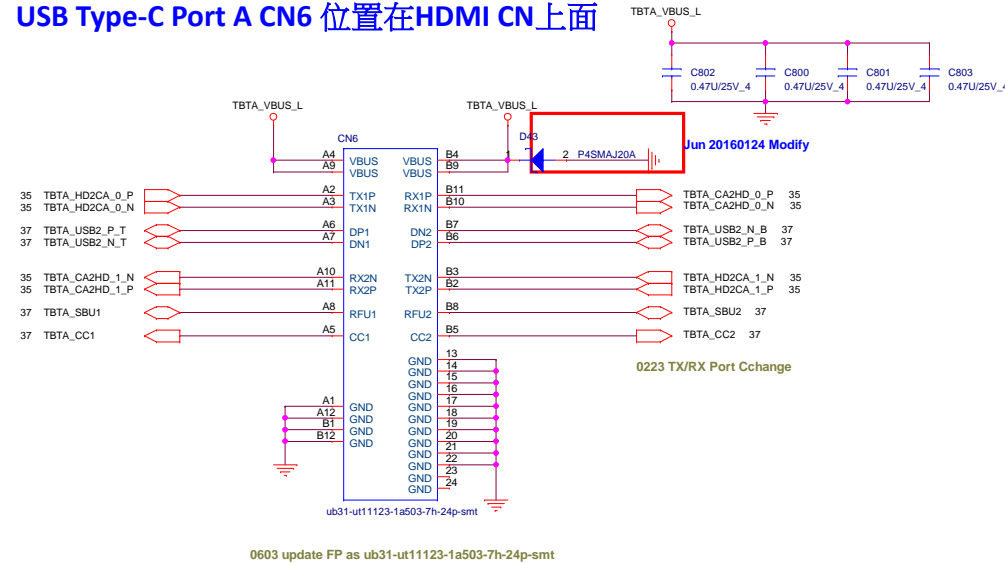


## USB Type-C Port B



+3V 2,4,10,11,12,13,14,15,16,17,19,23,24,25,28,30,31,33,34,35,40,50,54,55  
TBTB\_VBUS\_L 37  
TBTB\_VBUS\_L 37,38

## USB Type-C Port A CN6 位置在HDMI CN上面



0604 update PN as BC0101B1201

0503 update FP as d-0\_62x0\_32-0\_32h

TBTA_USB2_P_T	1	2	ESD101-B1-02ELS
TBTA_USB2_N_T	D33	1	ESD101-B1-02ELS
TBTA_USB2_P_B	D34	2	ESD101-B1-02ELS
TBTA_USB2_N_B	D14	1	ESD101-B1-02ELS
TBTA_CC1	D13	2	ESD101-B1-02ELS
TBTA_CC2	D32	1	ESD101-B1-02ELS
TBTA_SBU1	D18	2	ESD101-B1-02ELS
TBTA_SBU2	D38	1	ESD101-B1-02ELS
	D36	2	ESD101-B1-02ELS
TBTA_HD2CA_0_P	1	2	ESD101-B1-02ELS
TBTA_HD2CA_0_N	D30	1	ESD101-B1-02ELS
TBTA_CA2HD_0_P	D31	1	ESD101-B1-02ELS
TBTA_CA2HD_0_N	D10	2	ESD101-B1-02ELS
TBTA_CA2HD_1_N	D11	1	ESD101-B1-02ELS
TBTA_CA2HD_1_P	D40	2	ESD101-B1-02ELS
TBTA_HD2CA_1_N	2	1	ESD101-B1-02ELS
TBTA_HD2CA_1_P	D15	2	ESD101-B1-02ELS
	D17	1	ESD101-B1-02ELS

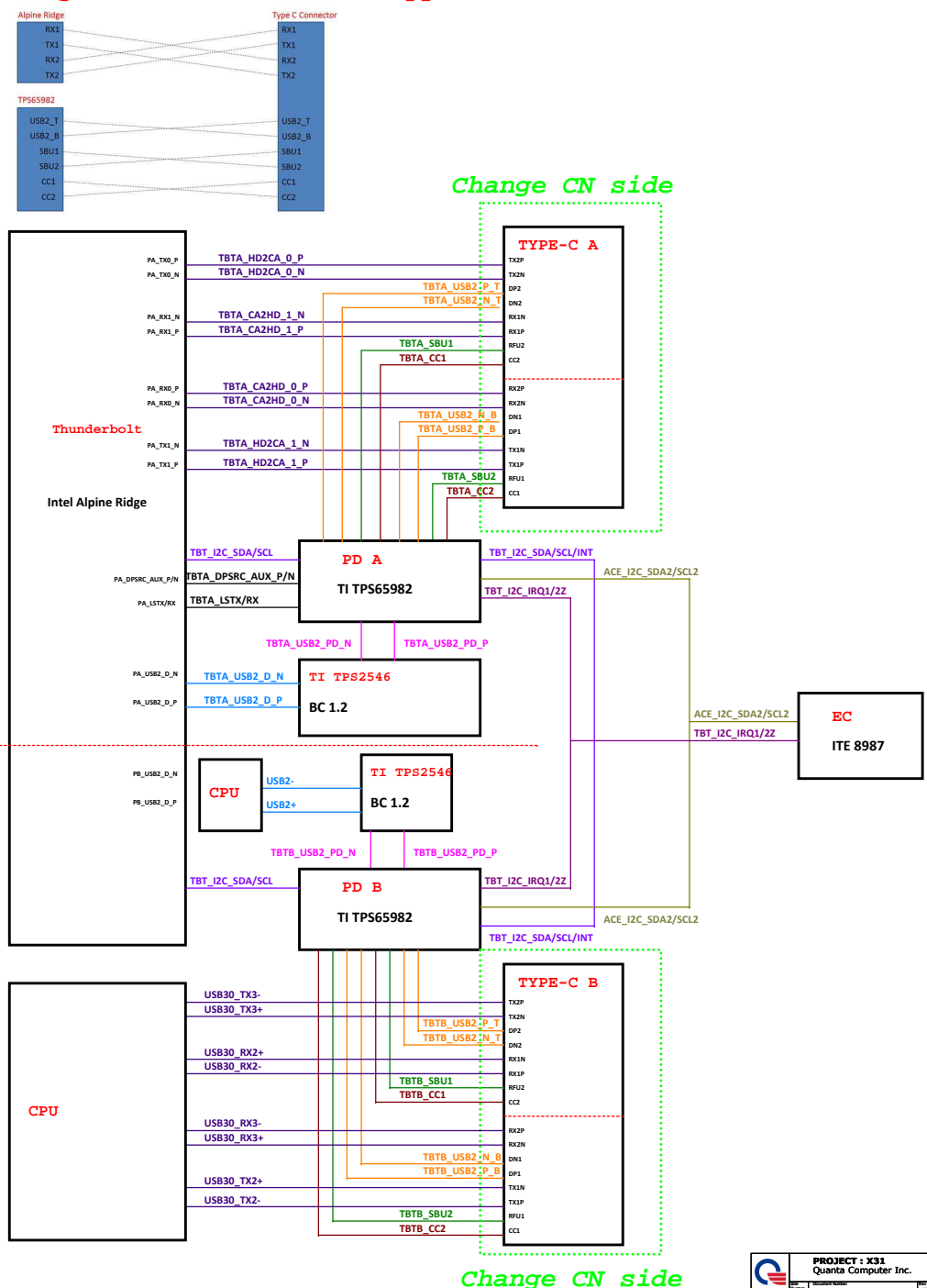
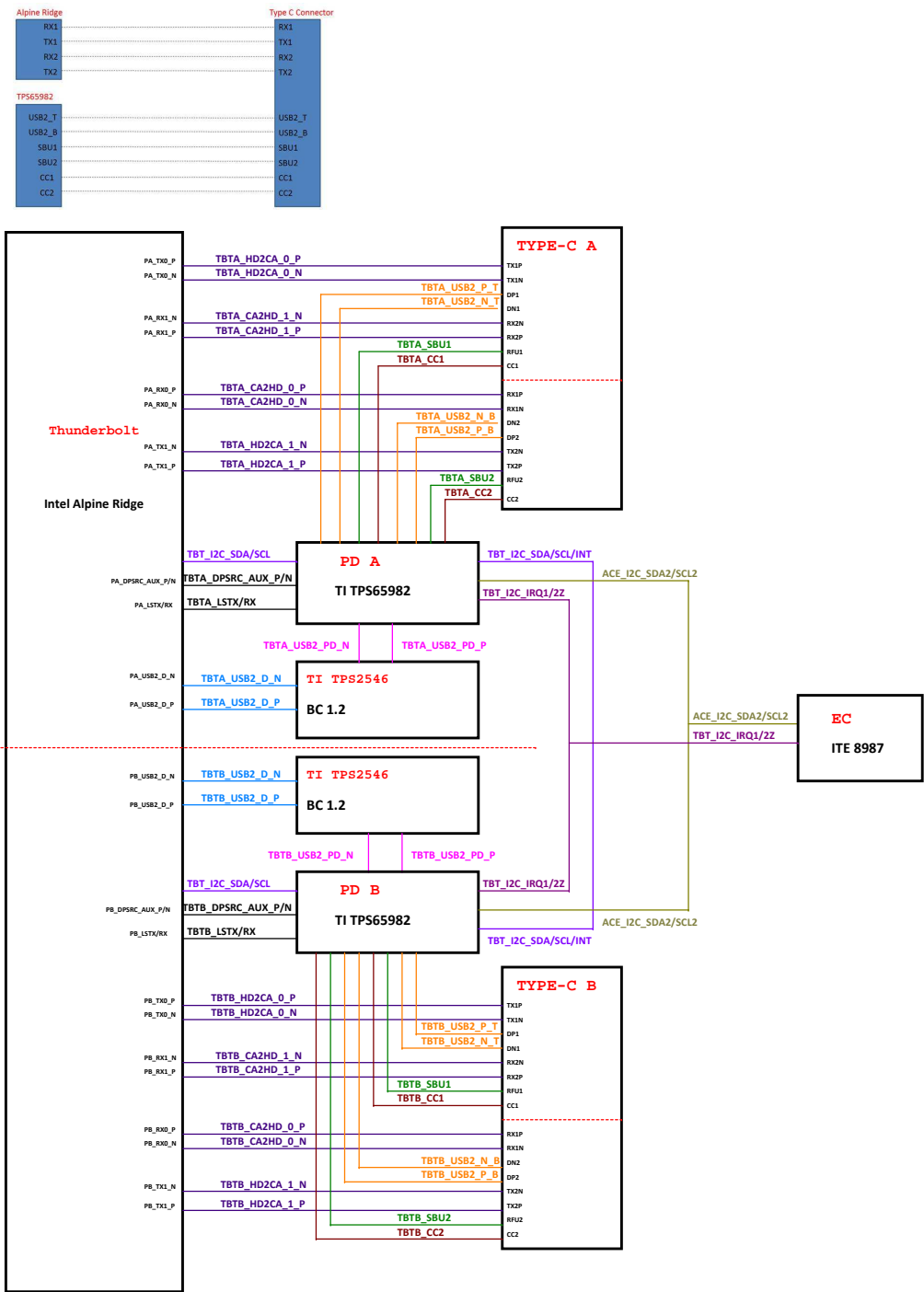


**PROJECT : X31**  
**Quanta Computer Inc.**

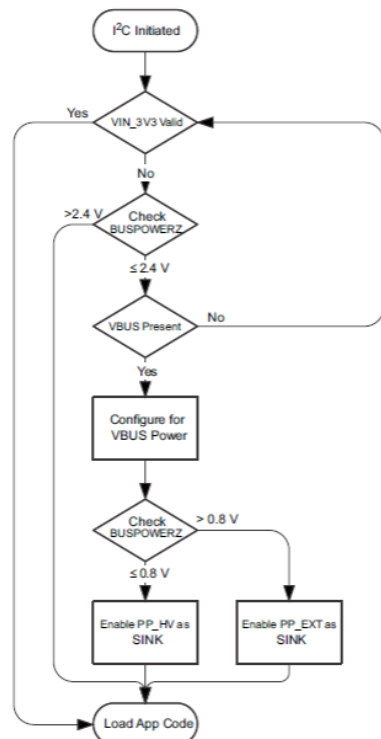
Size	Document Number	Rev
NB5	AR - TBT (USB2 & DP Part)	1A
Date: Tuesday, July 19, 2016	Sheet 41 of 59	

Keep the same Typc-C CN as the same as Intel AR CRB Board

Change CIO connection in Type-C Connector side

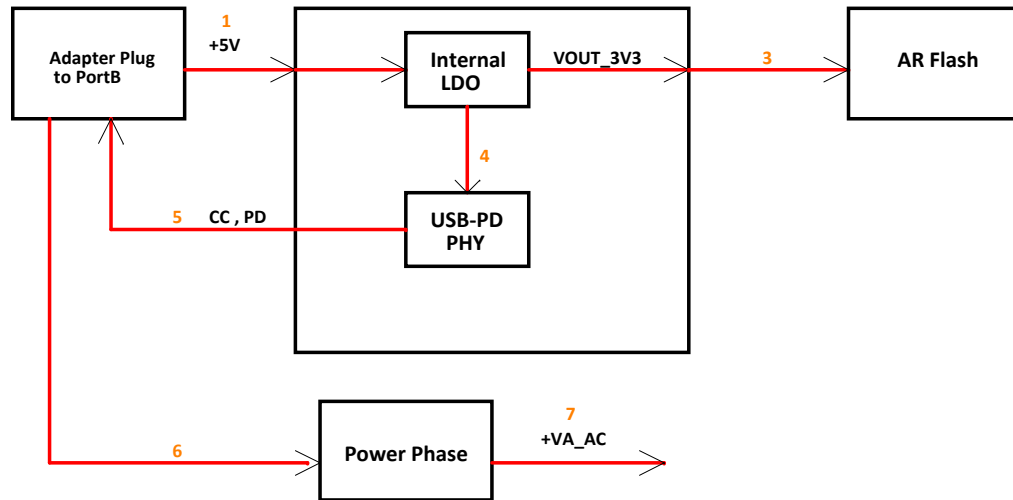


## Dead Battery Block

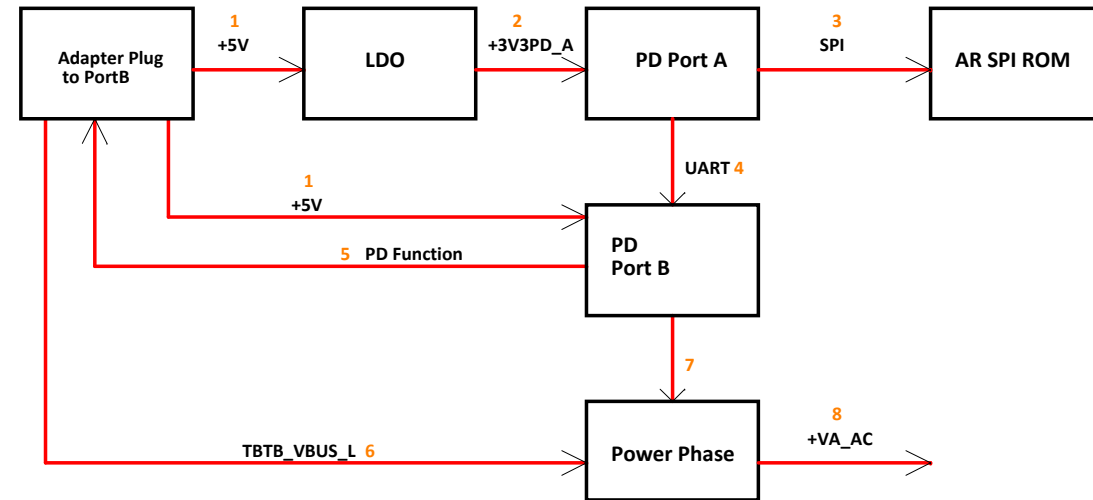


## PortA Dead Battery

Figure 65. Dead-Battery Condition Flow Diagram  
TI PD TPS65982 Port A



## PortB Dead Battery



## USB Type-C Connector – Pinout and Alignment



Receptacle (Front View)

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC1	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2	D-	D+	CC2	VBUS	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

USB3.0                      USB2.0                      USB3.0



Normal Plug



Reverse Plug



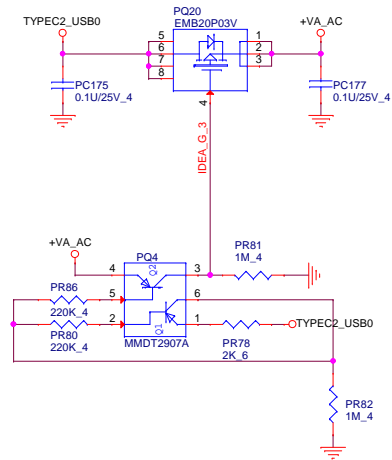
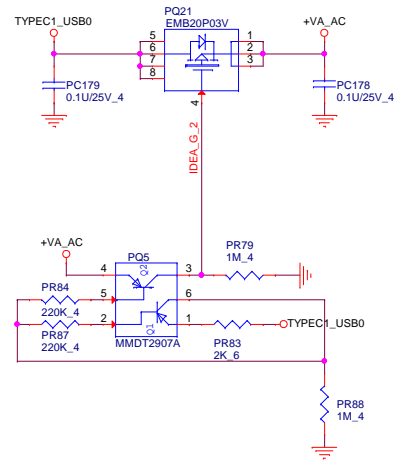
A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1
GND	RX2+	RX2-	VBUS	SBU1	D-	D+	CC	VBUS	TX1-	TX1+	GND
GND	TX2+	TX2-	VBUS	VCONN			SBU2	VBUS	RX1-	RX1+	GND
B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12

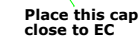


**PROJECT : X31**  
Quanta Computer Inc.

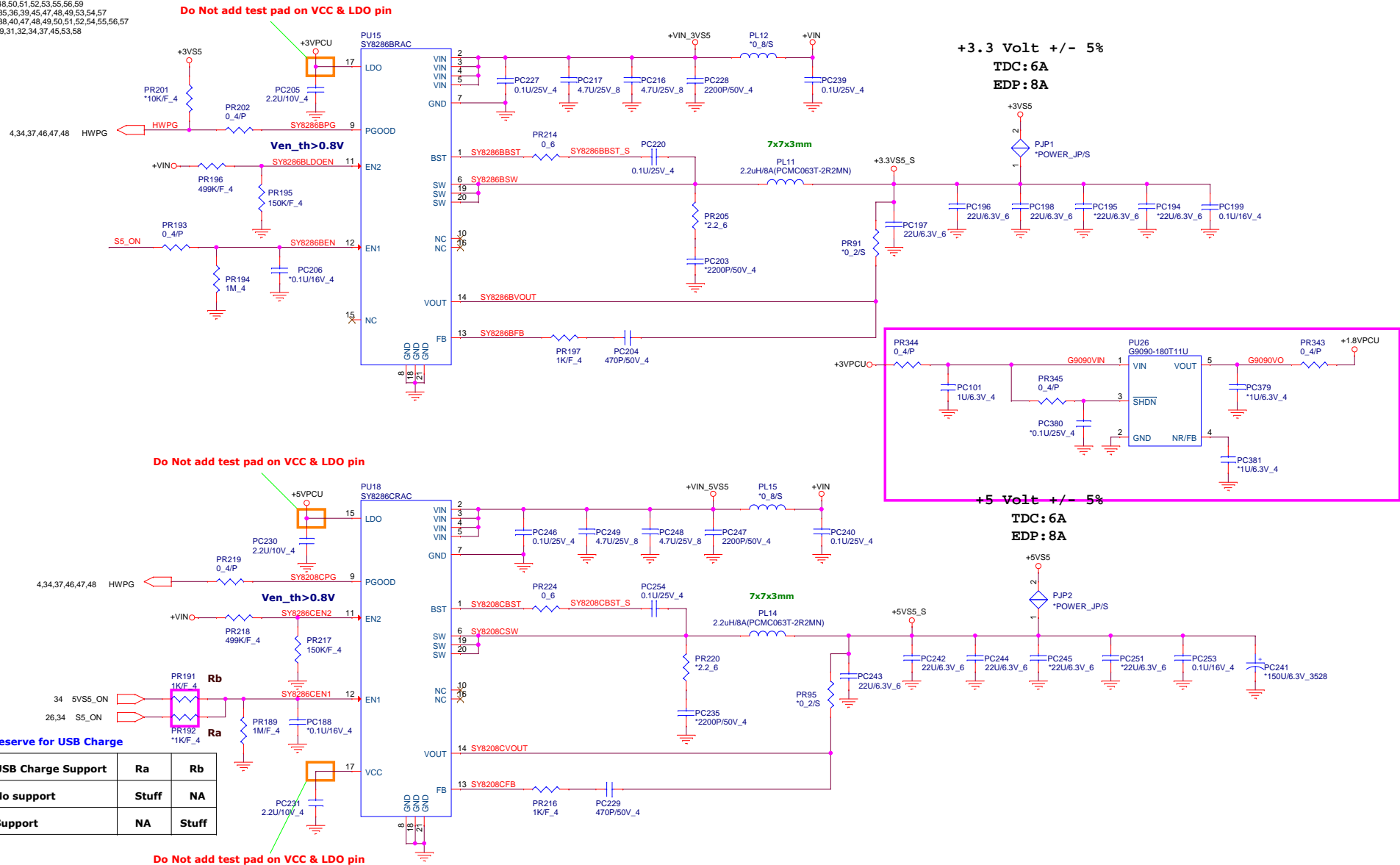
Size	Document Number	Rev
Custom	Load switch IC	
Date: Tuesday, July 19, 2016	Sheet 43 of 59	

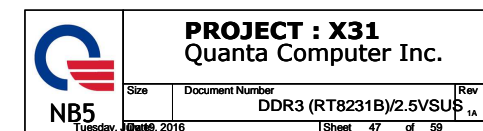
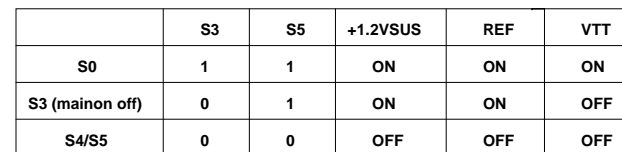
+VA\_AC 45.59  
TYPEC1\_USB0 37  
TYPEC2\_USB0 38



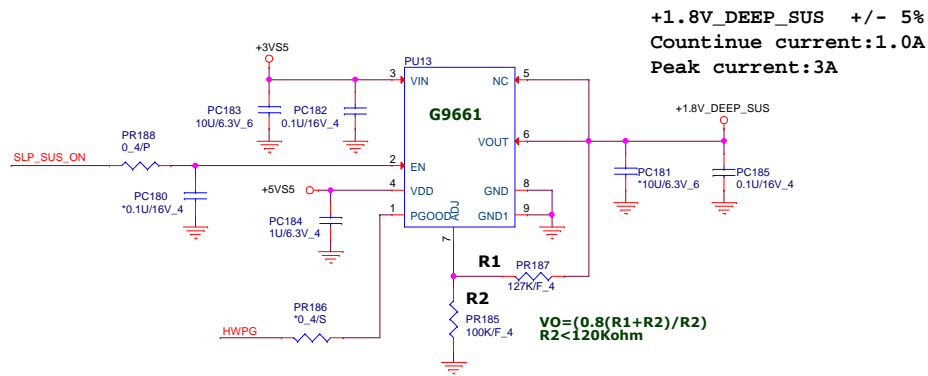
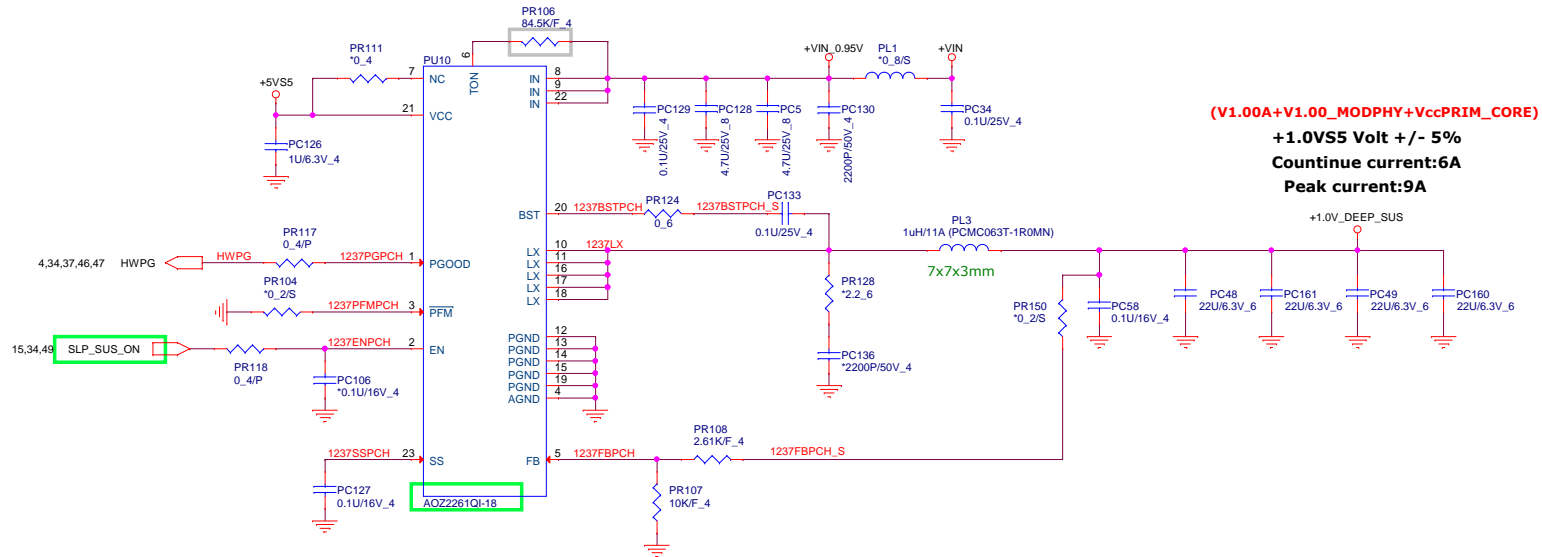


+VIN 23,26,31,45,47,48,50,51,52,53,55,56,59  
 +3VS5 4,15,32,33,34,35,36,39,45,47,48,49,53,54,57  
 +5VS5 4,25,26,29,37,38,40,47,48,49,50,51,52,54,55,56,57  
 +3VPCU 6,13,26,27,29,31,32,34,37,45,53,58  
 +5VPCU 25,26,54,57

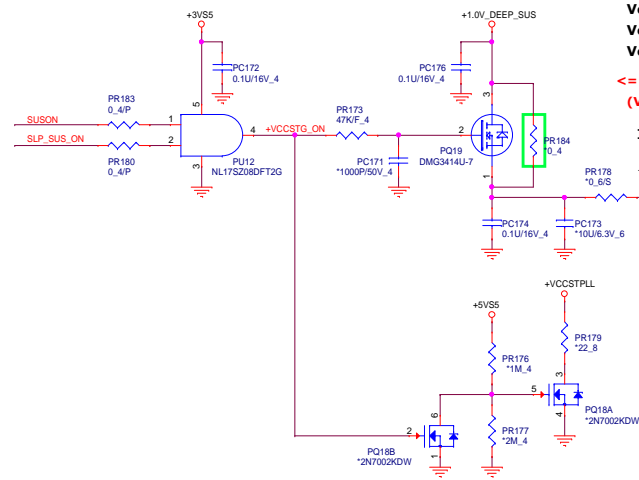




+VIN 23,26,31,45,46,47,50,51,52,53,55,56,59  
 +3VS5 4,15,32,33,34,35,36,39,45,46,47,49,53,54,57  
 +5VS5 4,25,26,29,37,38,40,46,47,49,50,51,52,54,55,56,57  
 +1.0V\_DEEP\_SUS 9,13,15,49  
 +1.8V\_DEEP\_SUS 9,15,45,54



+1.0V 2,4,6,34  
 +3V5S 4,15,32,33,34,35,36,39,45,46,47,48,53,54,57  
 +5V5S 4,25,26,29,37,38,40,46,47,48,50,51,52,54,55,56,57  
 +VCCIO 2,6  
 +1.2V5US 3,6,16,17,24,47,57,59  
 +VCCSTPLL 2,5,6,9,50  
 +1.0V\_DEEP\_SUS 9,13,15,48  
 +1.2V\_VCCPLL\_OC 6



**Volume Segment**

**Vcc\_ST: 0.12A**

**Vcc\_PLL: 0.12A**

**<= 10ms, full load ready**  
**(Vcc\_ST+Vcc\_PLL)**

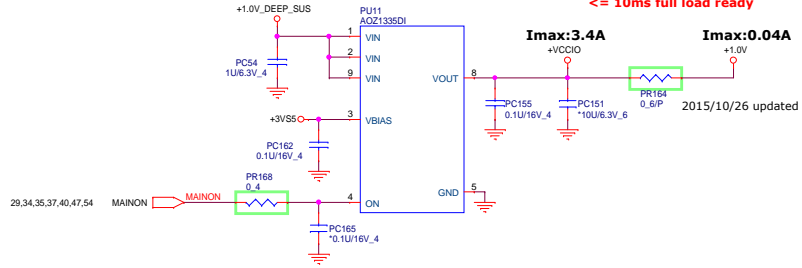
**Imax:0.24A**

**Volume Segment**

**Vcc\_STG: 0.04A**

**Vcc\_IO: 3.4A**

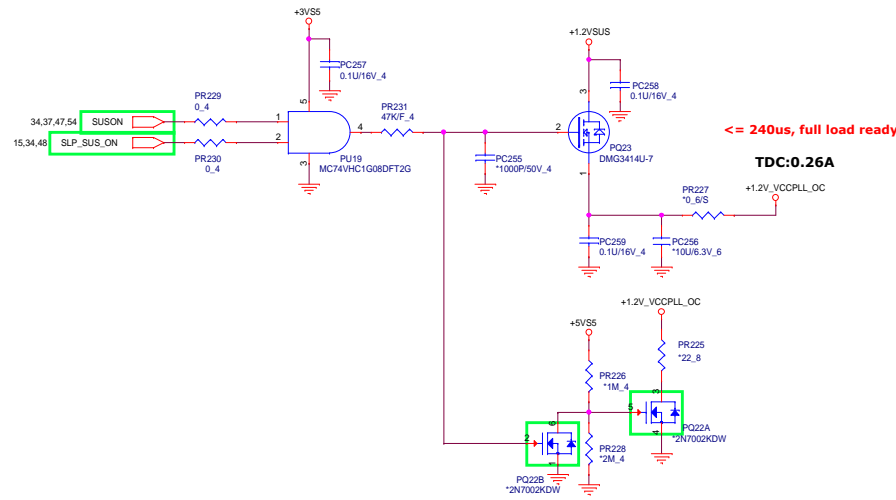
**<= 10ms full load ready**



**Imax:3.4A**

**Imax:0.04A**

2015/10/26 updated



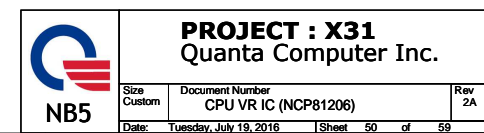
**<= 240us, full load ready**

**TDC:0.26A**

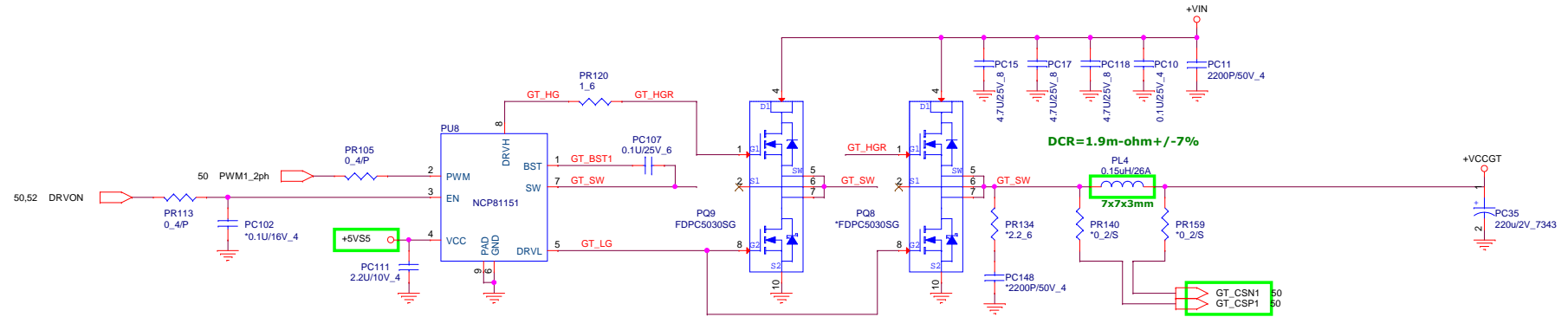


**PROJECT : X31**  
**Quanta Computer Inc.**

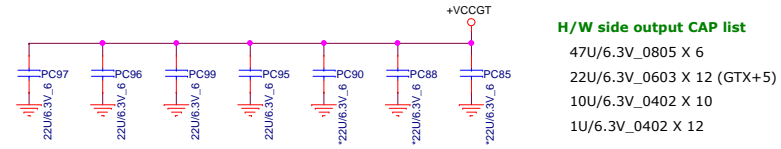
Size C	Document Number	Rev 1A
	<b>+1.0V/+VCCSTPLL</b>	
Date: Tuesday, July 19, 2016	Sheet 49 of 59	



+VIN 23,26,31,45,46,47,48,50,52,53,55,56,59  
+5VSS 4,25,26,29,37,38,40,46,47,48,49,50,52,54,55,56,57  
+VCCGT 7,50



For U23e --> Add These Components

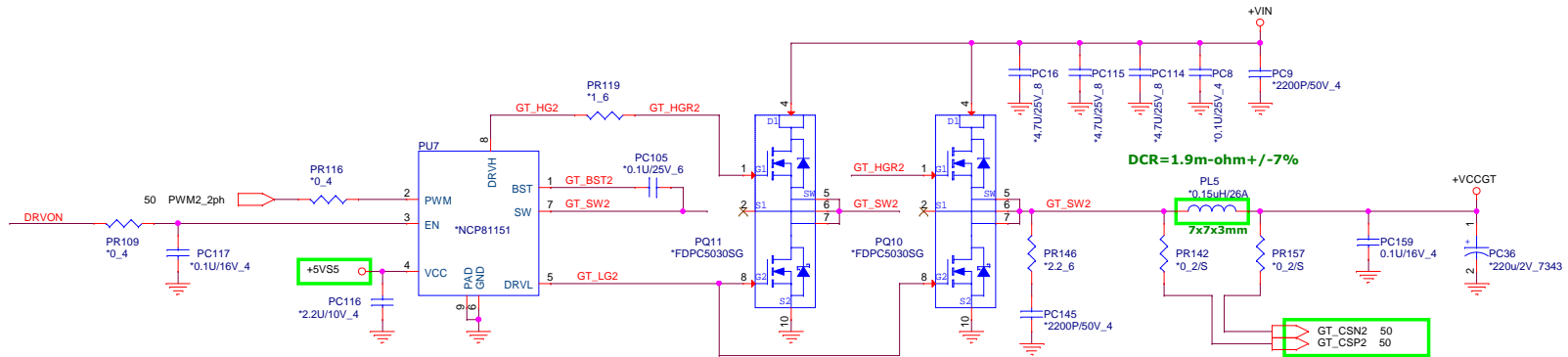


#### H/W side output CAP list

47U/6.3V\_0805 X 6  
22U/6.3V\_0603 X 12 (GTX+5)  
10U/6.3V\_0402 X 10  
1U/6.3V\_0402 X 12

#### +VCCGT

U-line 22 (15W)  
TDC:18A(22)  
Icc max:31A(22)  
L/L=3.1mV/A  
U-line 23e(28W)  
TDC:35A(23e)  
Icc max =64A(GT+GTx)  
L/L=2mV/A

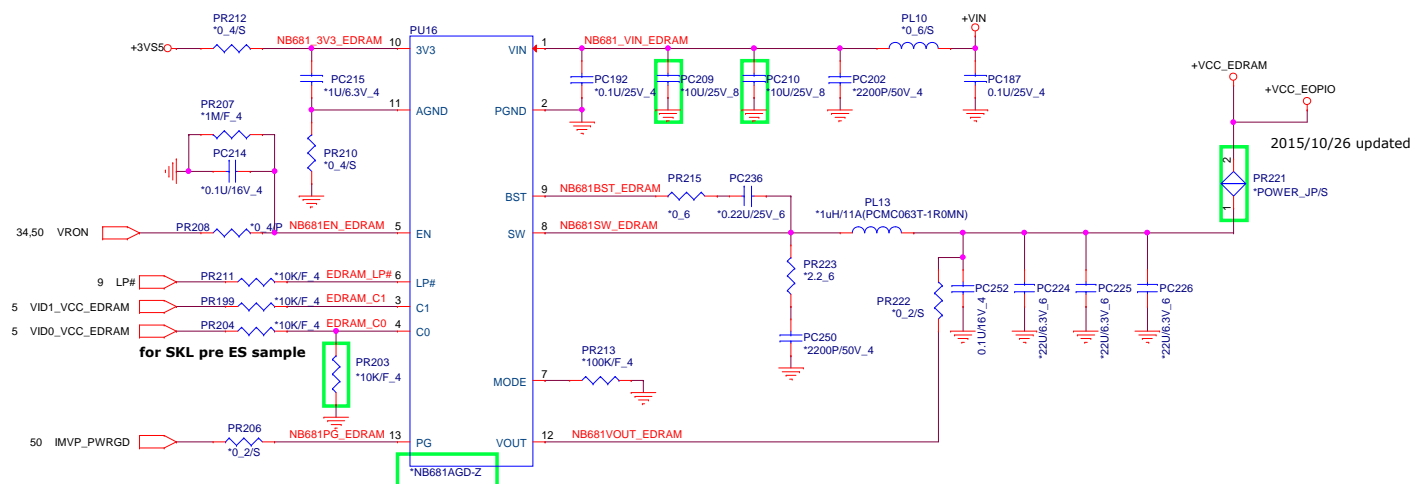
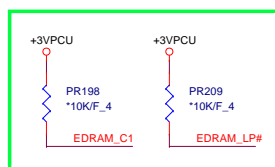




- 47U/6.3V 0805 X 9  
22U/6.3V 0805 X 1  
22U/6.3V 0603 X 13  
10U/6.3V 0603 X 1  
10U/6.3V 0402 X 15  
1U/6.3V 0402 X 15

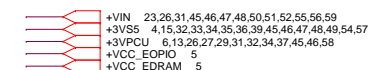
```
+VCCSA
U-line 22&23e
TDC:5A
Icc max:5A
L/L=10.5mV/A
```

Size Custom	Document Number <b>+VCORE/VCCSA (NCP81253)</b>	Rev
Date: Tuesday, July 19, 2016	Sheet 52 of 59	

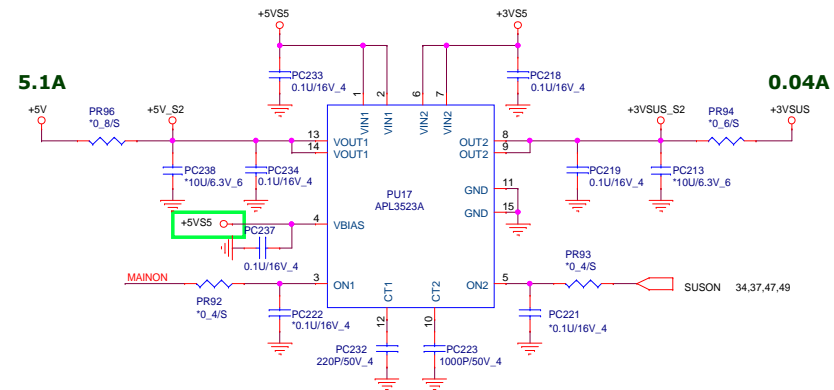
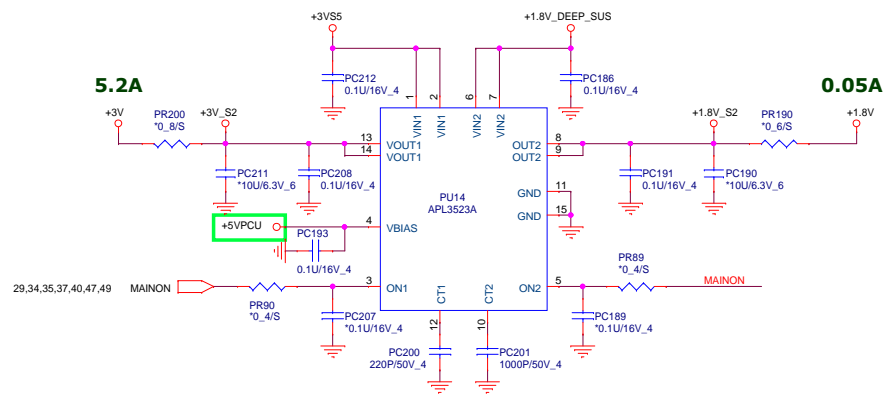


LP#	C1	C0	Vout
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1.0
1	1	1	1.05

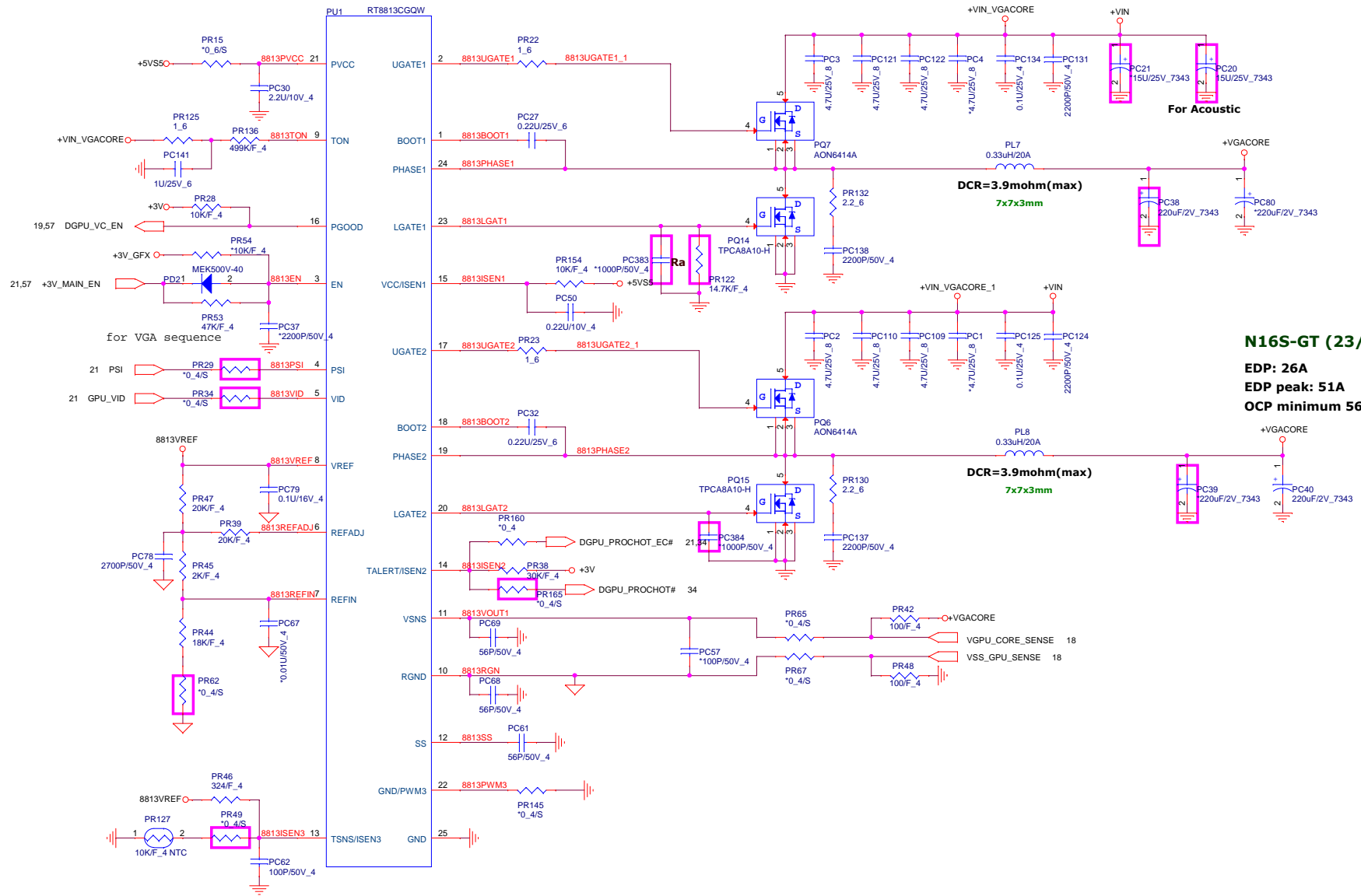
MODE		
	VR rail	Resistor
M1	VCCIO	0
M2	PRIMCORE	Float
M3	EDRAM/EOPIO	100K
M4	other	150K



+3V	2,4,10,11,12,13,14,15,16,17,19,23,24,25,28,30,31,33,34,35,40,50,55
+5V	24,25,28,31
+1.8V	5,25
+3VS5	4,15,32,33,34,35,36,39,45,46,47,48,49,53,57
+5VS5	4,25,26,29,37,38,40,46,47,48,49,50,51,52,55,56,57
+3VSUS	31,32
+5VPCU	25,26,46,57

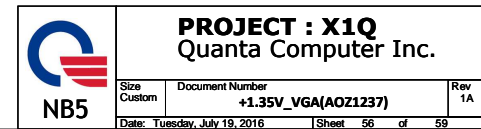


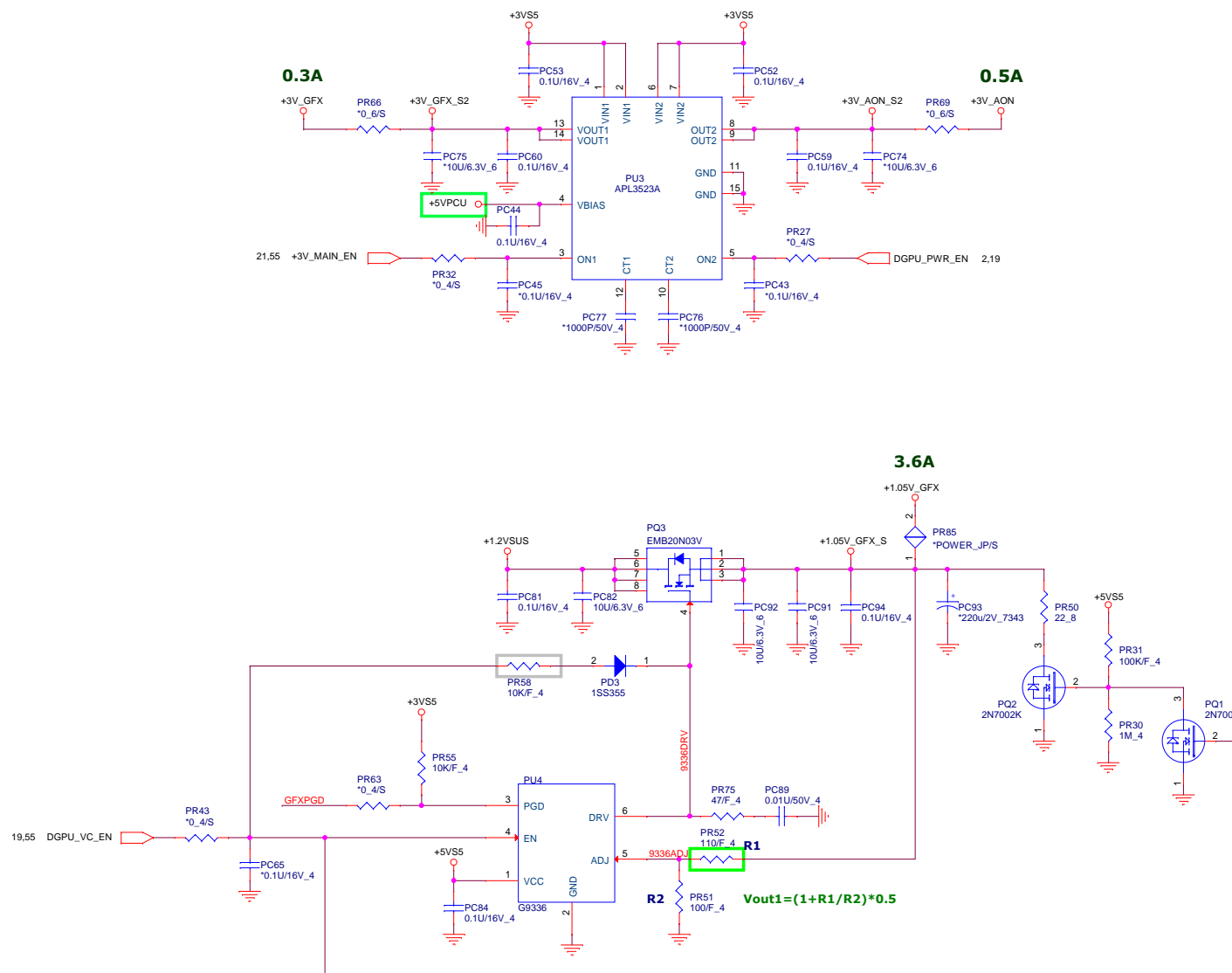
+3V 2,4,10,11,12,13,14,15,16,17,19,23,24,25,28,30,31,33,34,35,40,50,54  
 +VIN 23,26,31,45,46,47,48,50,51,52,53,56,59  
 +5VSS 4,25,26,29,37,38,40,46,47,48,49,50,51,52,54,56,57  
 +3V\_GFX 18,20,21,56,57  
 +VGACORE 18



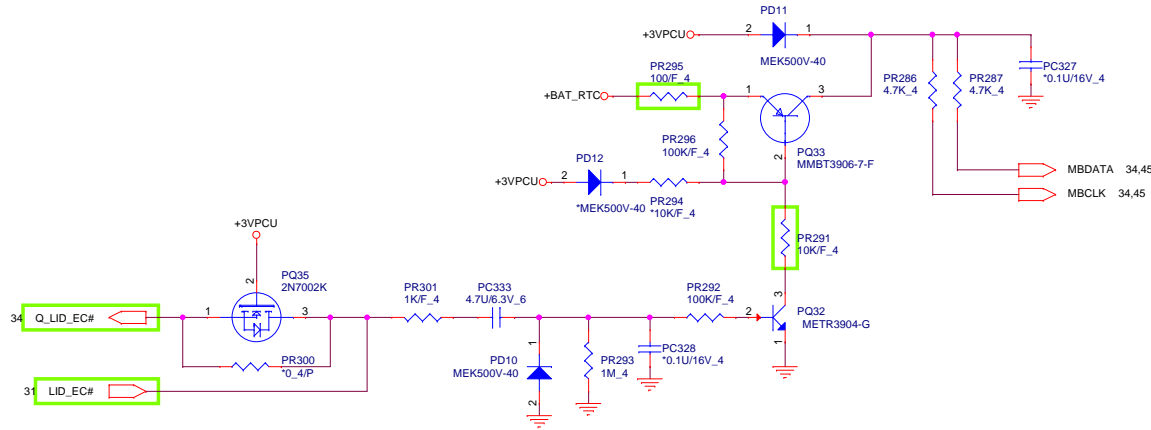
**PROJECT : X1Q**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8813A)	2A
Date:	Tuesday, July 19, 2016	Sheet 55 of 59



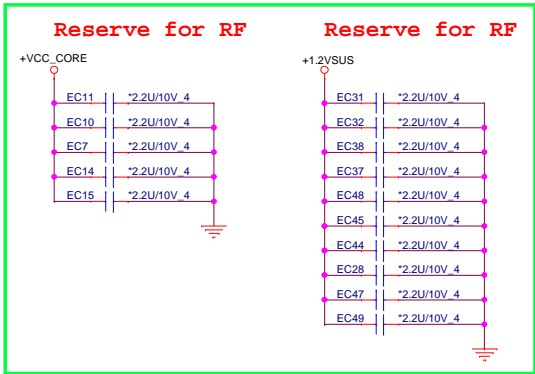


+3VPCU 6,13,26,27,29,31,32,34,37,45,46,53  
+BAT\_RTC 4,13,15,31,45

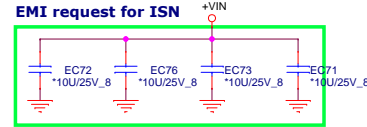


+VIN 23,26,31,45,46,47,48,50,51,52,53,55,56  
+PRWSRC 45  
+VA\_AC 44,45

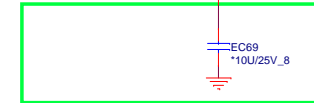
0329



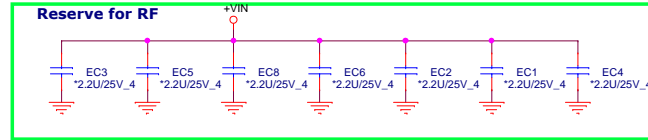
EMI request for ISN



EMI request for ISN +PRWSRC



Reserve for RF



Reserve for RF

