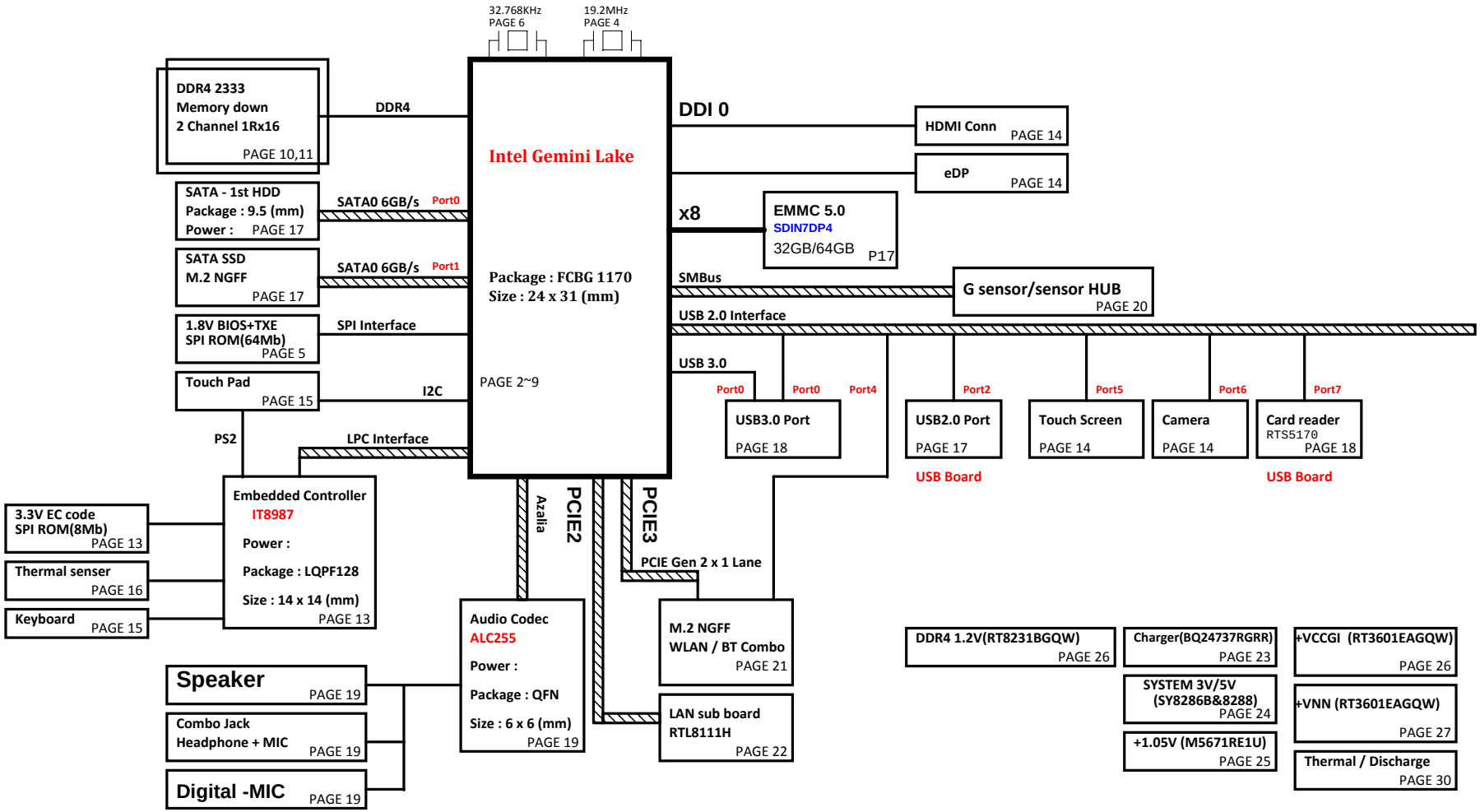
ZHVA Virgo_GL UMA(11.6")
Intel Gemini Lake Platform Block Diagram



Vinafix

Quanta Computer Inc.
PROJECT : ZHVA

Size	Document Number	Rev
	Intel Block Diagram	1A

Date: Thursday, August 09, 2018 Sheet 1 of 34

GLK ULT (DDR4)

02

[7] +1.2VSUS_Q

[10] M_A_DQ[63:0]

[11] M_B_DQ[63:0]

U23A

DDR4_LP3_LP4

DDR0

1 OF 13

U23B

DDR4_LP3_LP4

DDR1

2 OF 13

Confidential

Default no stuff

VREF trace must be at least 20 mils wide and space

R179 , R183 close to CPU

Trace length < 500 mils

Trace width = 15 mils

Trace spacing = 20 mils

colsed to CPU pin within 100 mils

C125 *1000p/50V_4

R137 *10_5%_4

C129 *1000p/50V_4

R148 *10_5%_4

DRAMRST-MEMORY DOWN

Trace length < 4500 mils, 50 ohm impendence

Trace spacing = 15 mils

CPU

MEMORY DOWN

+1.2VSUS_Q

R144 1K_1%_4

MA_DRAMRST#

R152 *5_4

C132 *0.1u/16V_4

M_A_DRAMRST# [10]

Trace length < 4500 mils, 50 ohm impendence

Trace spacing = 15 mils

CPU

MEMORY DOWN

+1.2VSUS_Q

R153 1K_1%_4

MB_DRAMRST#

R149 *5_4

C134 *0.1u/16V_4

M_B_DRAMRST# [11]

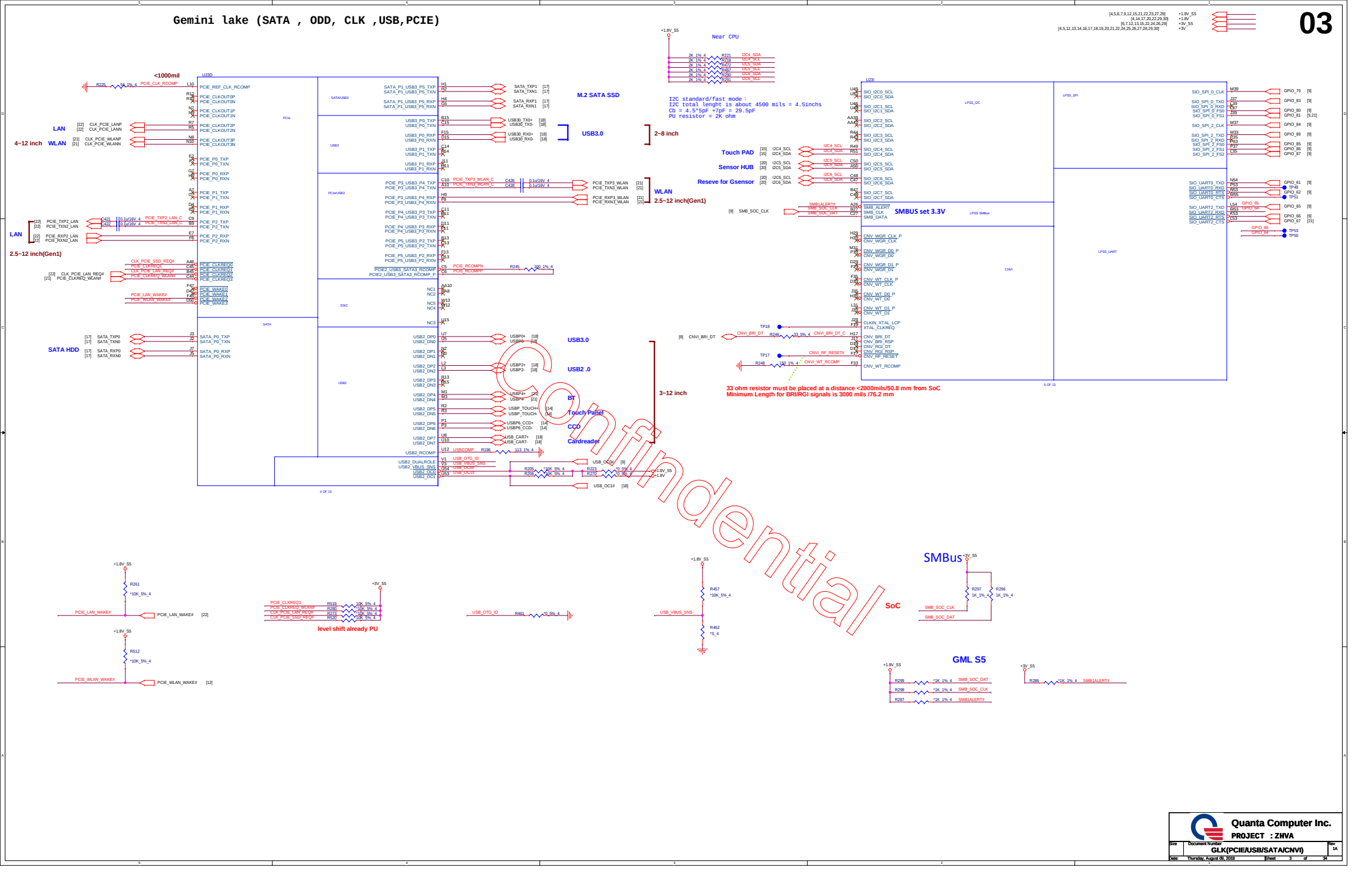
Quanta Computer Inc.

PROJECT : ZHVA

Size	Document Number	Rev
	GLK(MEMORY)	1A

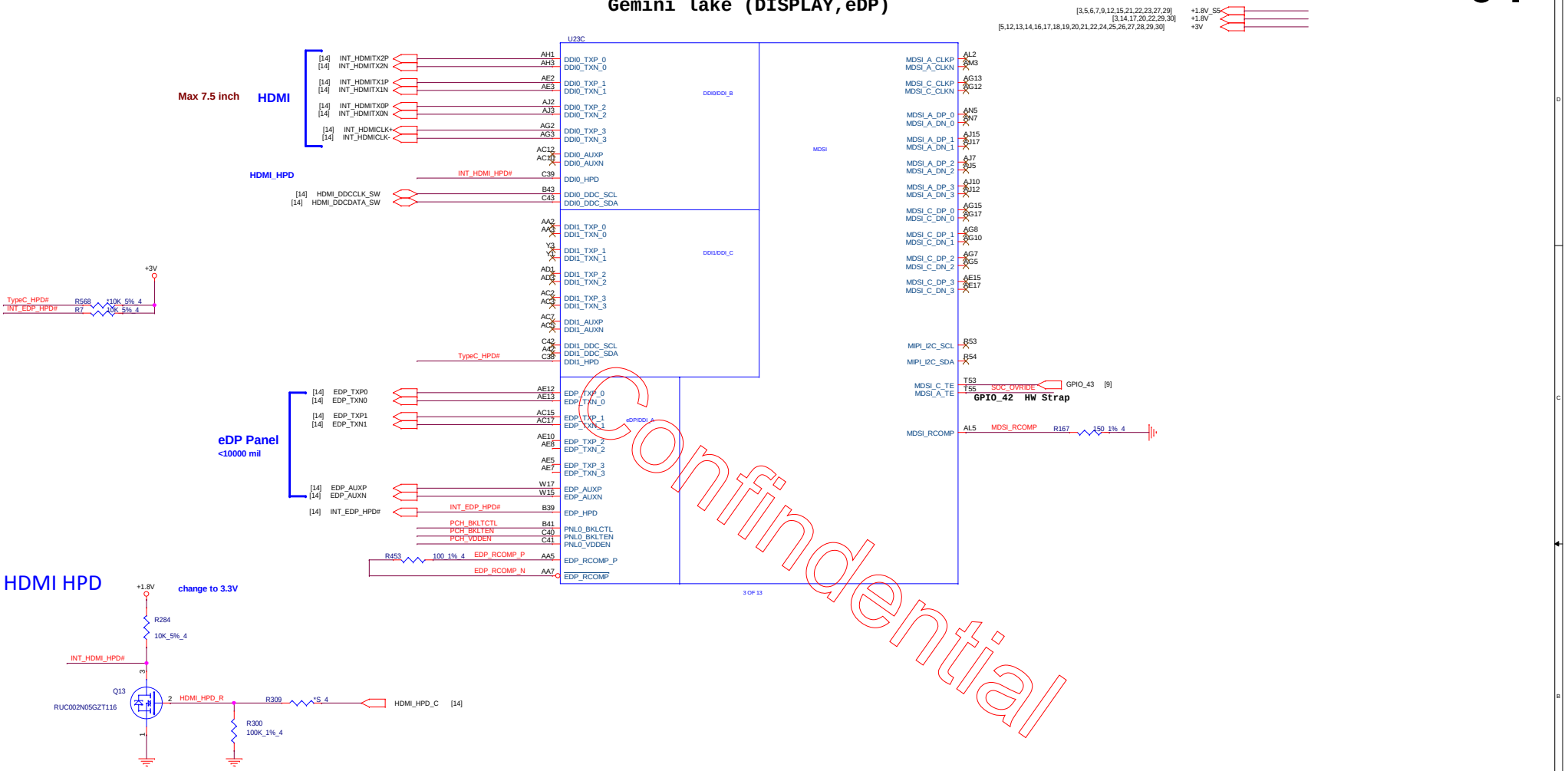
Date: Thursday, August 09, 2018 Sheet 2 of 34

Gemini lake (SATA , ODD, CLK ,USB,PCIE)

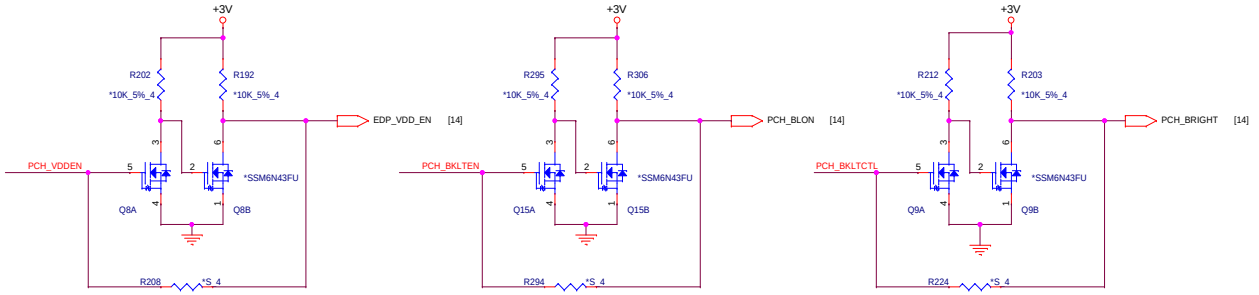


Quanta Computer Inc.			
PROJECT : ZHVA			
Size	Document Number		Rev
	GLK(PCIE/USB/SATA/CNVI)		1A
Date: Thursday, August 09, 2018	Sheet 3 of 34		

Gemini lake (DISPLAY,eDP)

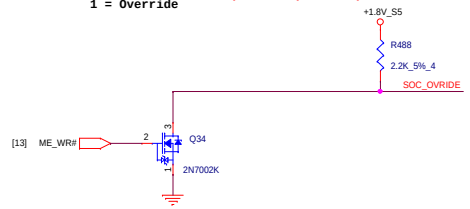


HDMI HPD



Override

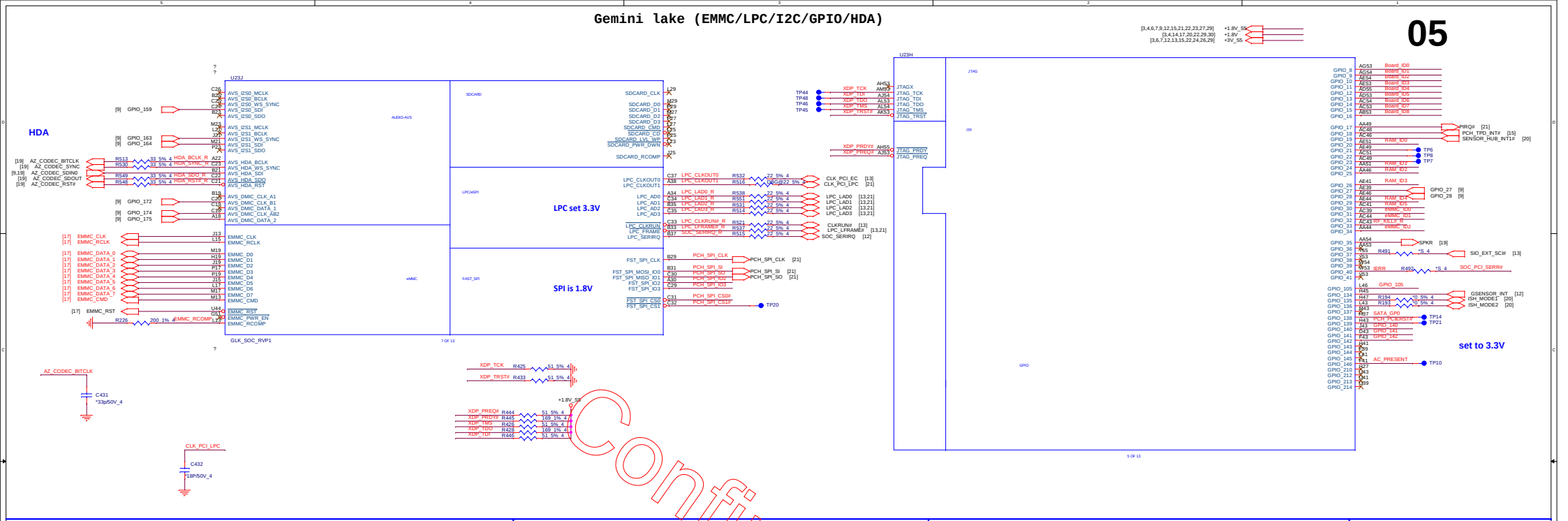
Flash Descriptor Override (SOC_OVRIDE)
0 = Normal Override(Normal operation)
1 = Override



Quanta Computer Inc.		
PROJECT : ZHVA		
Size	Document Number: GLK (HDMI/eDP)	Rev: 1A
Date: Thursday, August 09, 2018	Sheet 4 of 34	

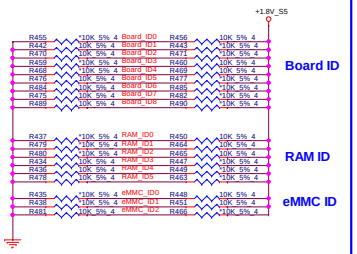
Gemini lake (EMMC/LPC/I2C/GPIO/HDA)

05



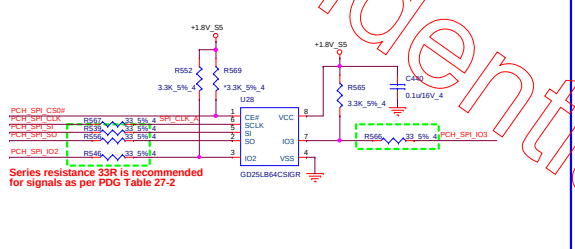
BOARD ID SETTING

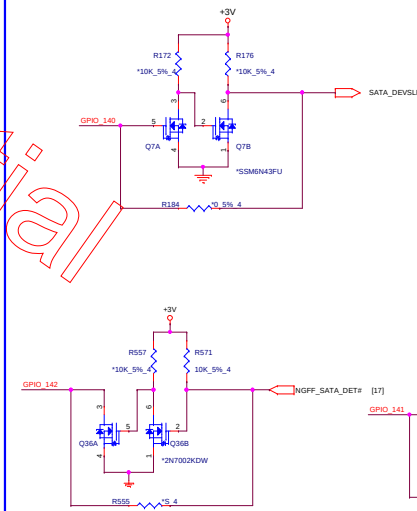
HW strap ID	Strap pin Description
Board_ID0	0 = Non Touch Screen 1 = Touch Screen
Board_ID1	0 = with EMMC 1 = without EMMC <HDD only>
Board_ID2	0 = M.2 SATA SSD 1 = M.2 PCIE SSD
Board_ID3	0 = none G sensor 1 = G sensor
Board_ID4	0 = none TPM 1 = TPM
Board_ID5	0 = With SATA Port 0 Connector 1 = Without SATA Port 0 Connector
Board_ID6	0 = With SATA Port 1 Connector 1 = Without SATA Port 1 Connector
Board_ID7	0 = Convertible model (360') 1 = Clamshell model
Board_ID8	Reserve
RAM_ID0	0 = Single chanel (A) 1 = Dual chanel(A&B)
RAM_ID1	0 = Channel A On board RAM 2GB 1 = Channel A On board RAM 4GB
RAM_ID2	0 = Channel B On board RAM 2GB 1 = Channel B On board RAM 4GB

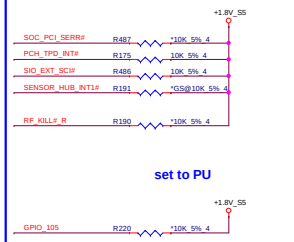


RAM_ID5	RAM_ID4	RAM_ID3	Vender
0	0	0	Miron
0	0	1	Hynix
0	1	0	Samsung
0	1	1	

eMMC_ID2	eMMC_ID1	eMMC_ID0	Vender
0	0	0	Samsung 32/64GB
0	0	1	Hynix 32/64GB
0	1	0	Kingston 32/64GB
0	1	1	Sandisk 32G/64G/128GB
1	1	1	Toshiba 128GB







Quanta Computer Inc.

PROJECT : ZHVA

Size	Document Number	Rev
	GLK (GPIO/LPC/I2C/HDA)	1A
Date: Thursday, August 09, 2018	Sheet 5 of 34	

Gemini lake (PMU/PMIC/RTC)

06

PMU set to 3.3V

check list use 20k

RTC is 3.3V

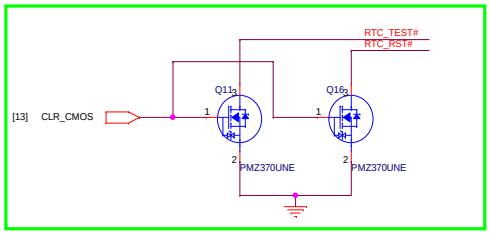
PMU set 3.3V

1.8V

colsed to CPU pin within 100 mils

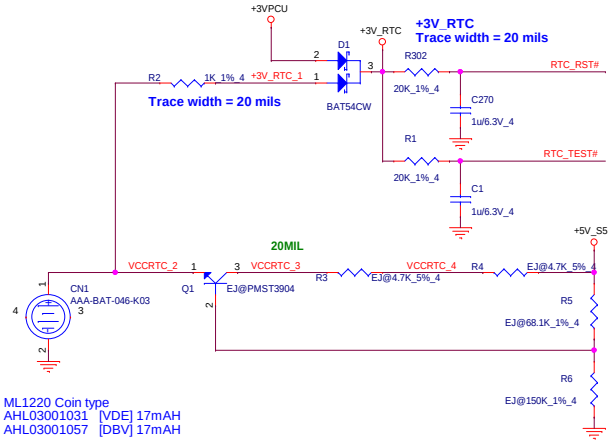
colsed to CPU pin within 100 mils

EC reset RTC



Confidential

RTC Circuitry (RTC)

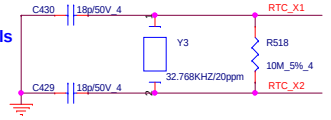


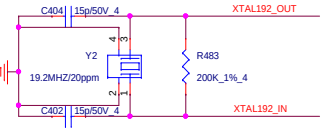
ML1220 Coin type
AHL03001031 [VDE] 17mAH
AHL03001057 [DBV] 17mAH

RTC Clock 32.768KHz (CPU)

CH01006JB08 -> 10p
CH01506JB06 -> 15p
CH-6806TB01 -> 6.8p

Trace length < 1000 mils





Quanta Computer Inc.
PROJECT : ZHVA

Size	Document Number	Rev
	GLK (PMU/PMIC/SMB/RTC)	1A

Date: Thursday, August 09, 2018 Sheet 6 of 34

EDGE DECAPS
FOR EXPOSED POWER PLANES

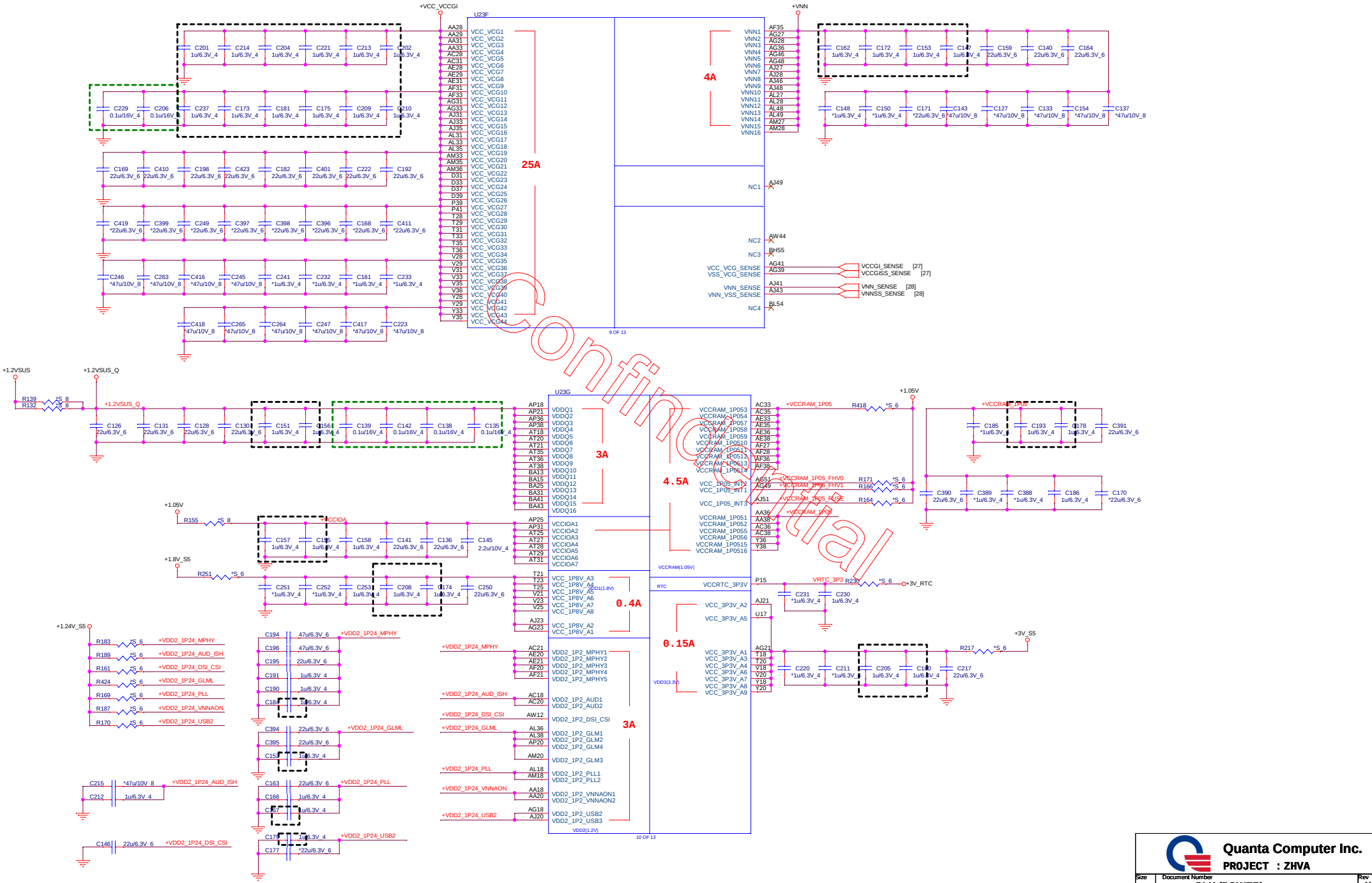
BACK side cap

Gemini (POWER)

07

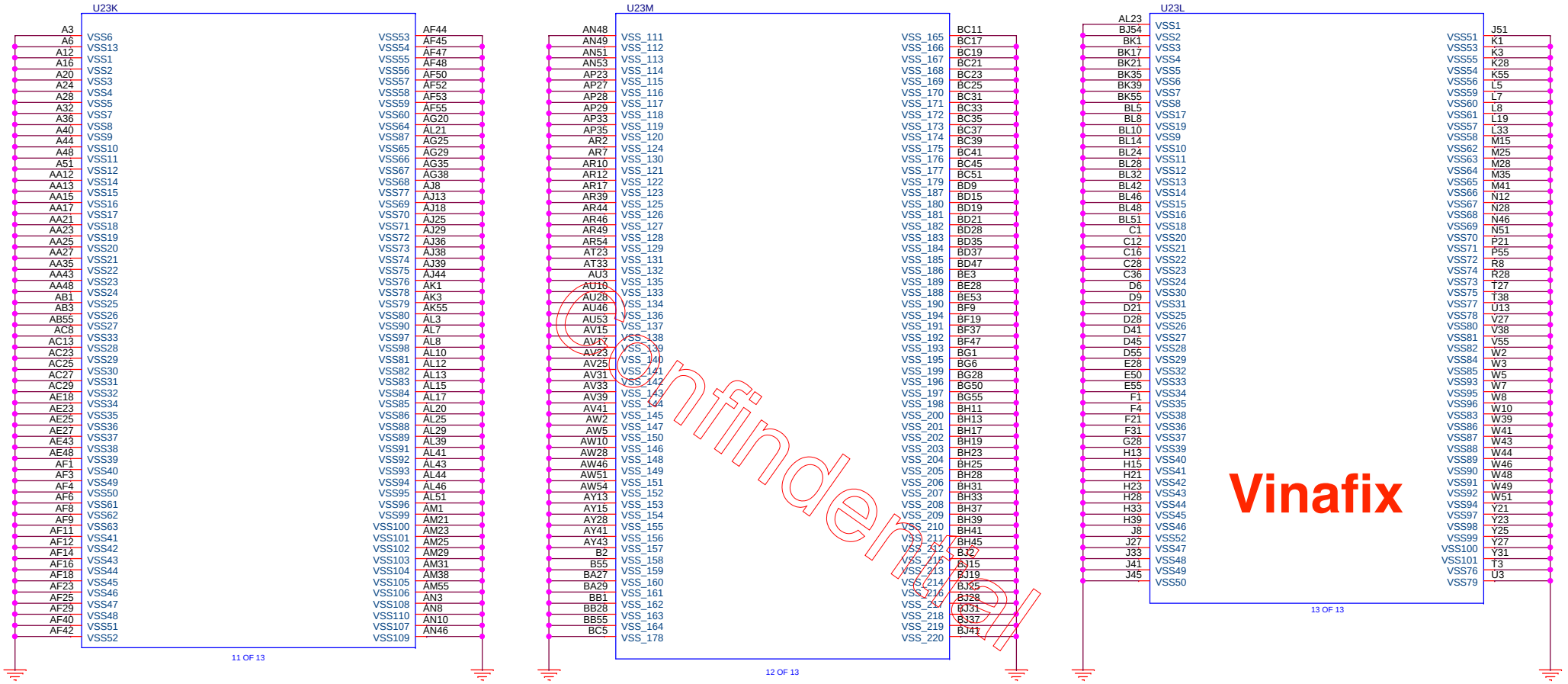
[3,6,12,13,15,22,24,26,29] +3V_S5
[29] +1.24V_S5
[3,4,5,6,9,12,15,21,22,23,27,29] +1.8V_S5
[6,13] +3V_RTC
[2] +1.2VSUS_Q

[28] +VNN
[27] +VCC_VCCGI
[6,25,27,28] +1.05V



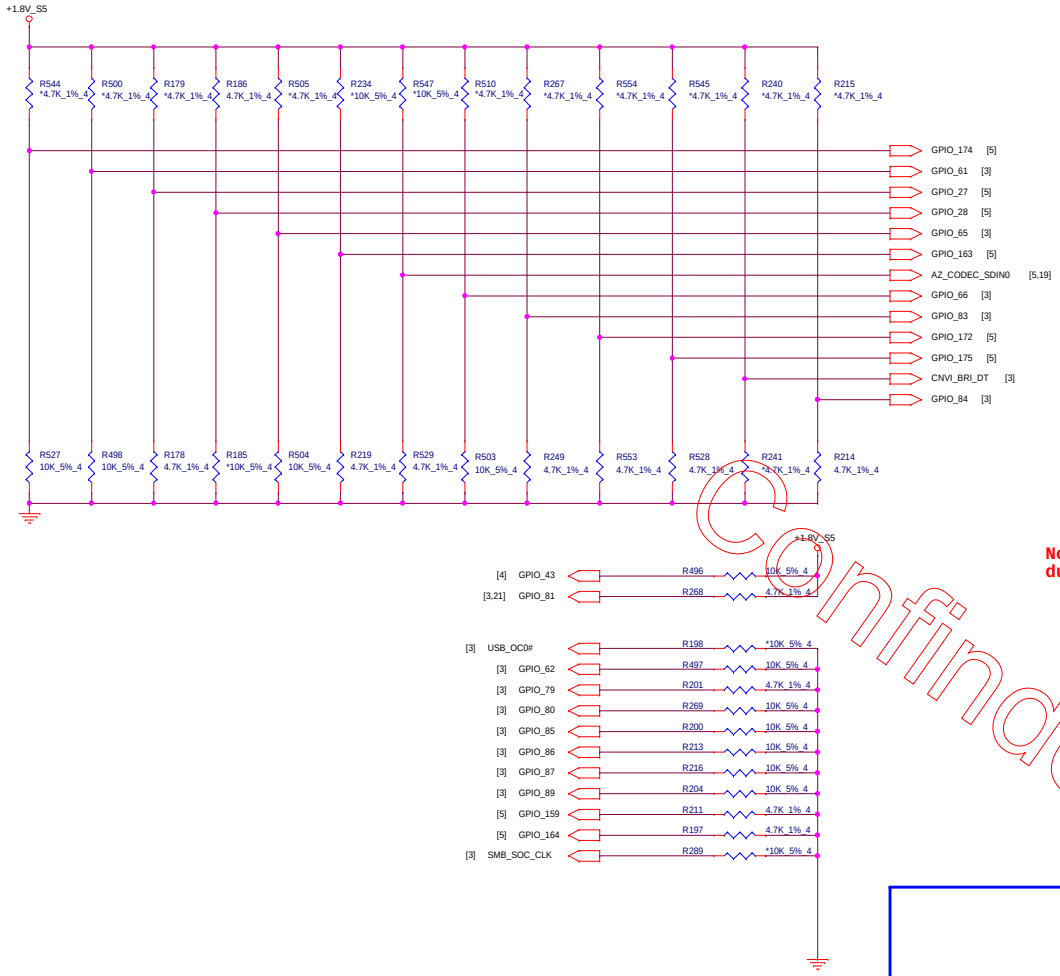
Quanta Computer Inc.		
PROJECT : ZHVA		
Size	Document Number: GLK (POWER)	Rev: 1A
Date: Thursday, August 09, 2018	Sheet 7 of 34	

GLK ULT (GND)



Quanta Computer Inc.		
PROJECT : ZHVA		
Size	Document Number: GLK (GND)	Rev: 1A
Date: Thursday, August 09, 2018	Sheet 8 of 34	

HARDWARE STRAPS



Note: If platform is using eMMC as boot device, then provide a pull down for this strap to disable SPI.

Hardware Strap	Strap Description	Value
GPIO_174	VDD2 1.24V vs.1.20V select 0 = 1.2V(default) 1 = 1.24V	1
GPIO_61	Enable CSE(TXE3.0) ROM Bypass 0 = Disable bypass 1 = Enable Bypass	0
GPIO_27	Allow eMMC as a boot source 0 = Disable 1 = Enable	0
GPIO_28	Allow SPI as a boot source 0 = Disable 1 = Enable	1
GPIO_65	Force DNX FW Load 0 = Do not force 1 = Force	0
GPIO_163	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V 1=buffers set to 1.8V	0
AZ_CODEC_SDIN0	PMU 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode	0
GPIO_66	LPC No Re-Boot 0 = Disable (default) 1 = Enable	0
GPIO_83	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode	0
		0
GPIO_172	SMbus No Re-Boot 0 = Disable (default) 1 = Enable	0
GPIO_42	Top swap override 0 = Disable 1 = Enable	0
GPIO_175	eSPI vs. LPC 0 = LPC mode (default) 1 = eSPI mode	0
CNVI_BRI_DT	eSPI Flash Sharing Mode: 0 = master attached flash sharing (MAFS; default) 1 = slave attached flash sharing (SAFS)	0
GPIO_84	Allow SPI as a boot source 0 = Enable (default) 1 = Disable	0

Note: The default for A0 will be eSPI due to a bug on LPC.

Quanta Computer Inc.
PROJECT : ZHVA

Size	Document Number	Rev
	HW STRAPS/XDP	1A

Date: Thursday, August 09, 2018 Sheet 9 of 34

BYTE4_32-39
BYTE7_56-63

BYTE6_48-55
BYTE5_40-47

BYTE3_24-31
BYTE2_16-23

BYTE1_8-15
BYTE0_0-7

DB1 change

U3 U21 U4 U22

RAM@DDR4_96P

AKD5QGSTW00

DB1 Option for 16Gbx16 die

SI1C, 0615

SI1, 0427 RF

DB1 Option for 16Gbx16 die
Close DDR ball

Place these Caps near Channel A
1uF/10uF 4pcs on each side of connector

SI1, 0421 add

DB1 Intel

SI1B, 0603

VREF DQ1 M1 Solution

DB1 12/11, close memory

In the middle of CPU and Double-

Memory 8G & Memory 16G TABLE			
	Memory 8G	Memory 16G	
R278	0Ω	CS00002JB38	240Ω CS12402FB03
R279	0Ω	CS00002JB38	240Ω CS12402FB03
R280	0Ω	CS00002JB38	240Ω CS12402FB03
R281	0Ω	CS00002JB38	240Ω CS12402FB03
R282	UNINSTAL	INSTAL	
R283	UNINSTAL	INSTAL	
R284	UNINSTAL	INSTAL	
R285	UNINSTAL	INSTAL	
R290	INSTAL	UNINSTAL	
R291	INSTAL	UNINSTAL	
R292	INSTAL	UNINSTAL	
R293	INSTAL	UNINSTAL	

0Ω resistors should be low ESL
BG1 should be approx 5ps shorter
L1 < 0.1mm
L2 < 0.25mm
L3 < 2mm

	SDP x16	DDP x16
Re9	0Ω	240Ω
Rm9	open	0Ω
Rm9b	0Ω	open

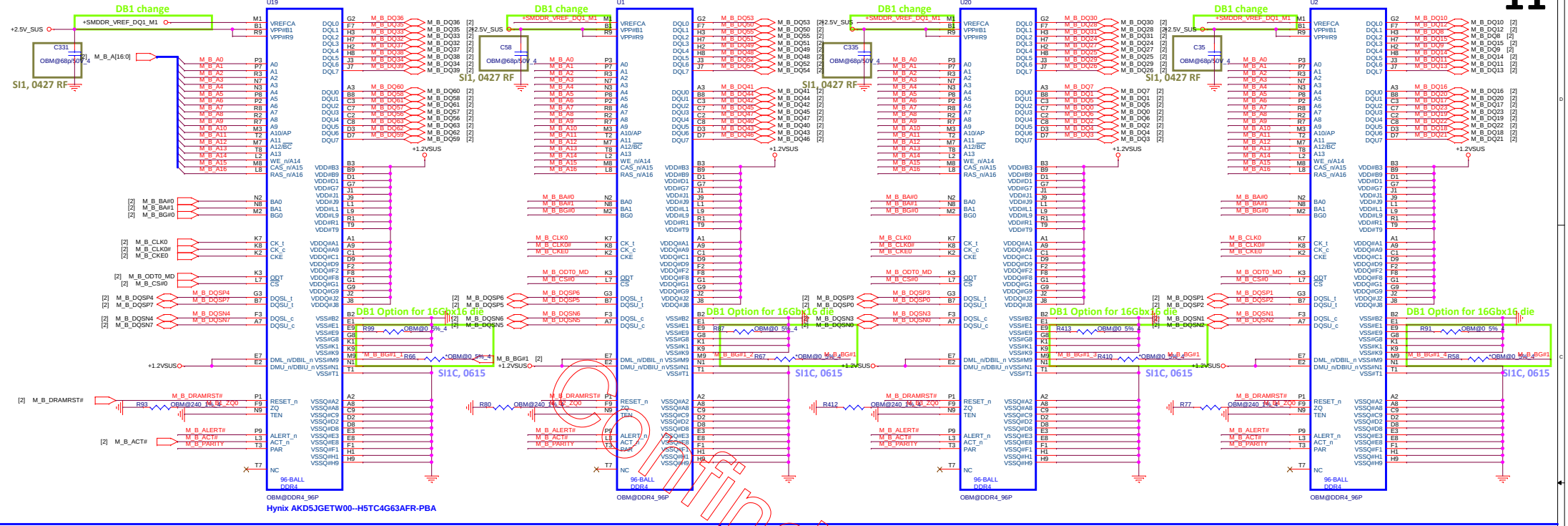
Quanta Computer Inc.		
PROJECT : ZHVA		
Size	Document Number	Rev
	DDR4 Memory Down (CH. A)	1A
Date: Thursday, August 09, 2018	Sheet 10 of 34	

BYTE4_32-39
BYTE7_56-63

BYTE6_48-55
BYTE5_40-47

BYTE3_24-31
BYTE0_0-7

BYTE1_8-15
BYTE2_16-23



DB1 12/11, close memory

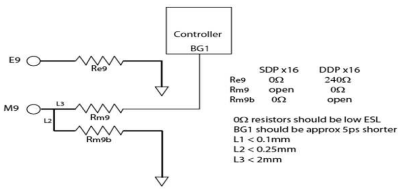
DB1 Option for 16Gbx16 die
Close DDR ball

DG 0.5 7/12, close T routing

DB1 12/11, close memory

Memory 8G & Memory 16G TABLE

	Memory 8G	Memory 16G
R278	0Ω CS00002JB38	240Ω CS12402FB03
R279	0Ω CS00002JB38	240Ω CS12402FB03
R280	0Ω CS00002JB38	240Ω CS12402FB03
R281	0Ω CS00002JB38	240Ω CS12402FB03
R282	UNINSTAL	INSTAL
R283	UNINSTAL	INSTAL
R284	UNINSTAL	INSTAL
R285	UNINSTAL	INSTAL
R290	INSTAL	UNINSTAL
R291	INSTAL	UNINSTAL
R292	INSTAL	UNINSTAL
R293	INSTAL	UNINSTAL



Place these Caps near Channel B

1uF /10uF 4pcs on each side of connector

SI1, 0421 add

DB1 Intel

SI1B, 0603

DB1 Intel

VREF DQ1 M1 Solution

SI1, 0417 RF

DB1 RF

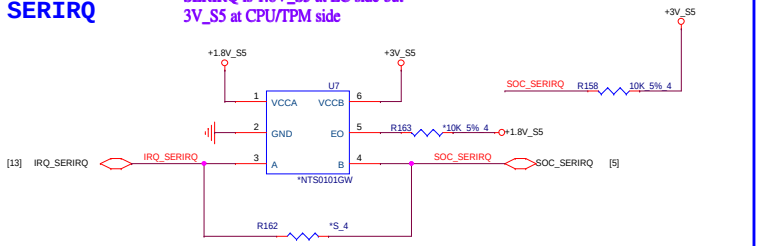
SI1, 0417 RF

DB1 RF

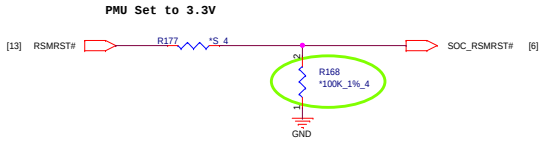
Quanta Computer Inc.	
PROJECT : ZHVA	
Size	Document Number: DDR4 Memory Down (CH. B) — Rev: 1A
Date: Thursday, August 09, 2018	Sheet 11 of 34

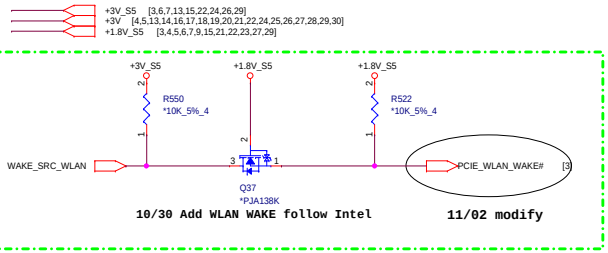
SERIRQ

SERIRQ is 1.8V_S5 at EC side but
3V_S5 at CPU/TPM side

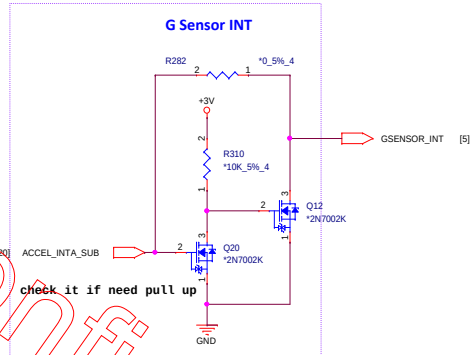


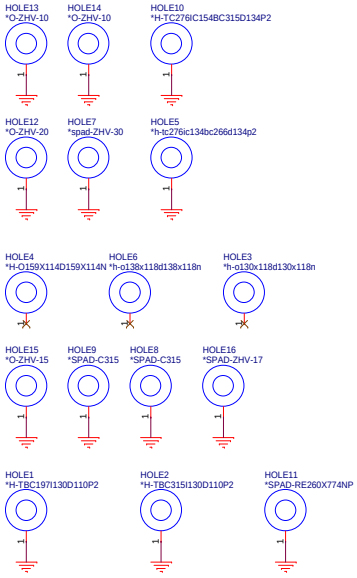
PMU Set to 3.3V





G Sensor INT





Quanta Computer Inc.
PROJECT : ZHVA

Size	Document Number	Rev
	Level Shift/Hole	1A
Date: Thursday, August 09, 2018	Sheet 12 of 34	

EC(KBC)

+3VPCU_EC and +3V_RTC minimum trace width 12mils.

12 mils

IT8987

(For PLL Power)

PU/PD (KBC)

Battery Disable (FSW)

SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	Thermal sensor
SM Bus 3	
SM Bus 4	

Reserve power on switch for test (MP remove)

SPI ROM(KBC)

W25X10CLSNIG

Power_Auto_Recovery

15 mils

20 mils

HWPG(KBC)

Prevent ESD/EOS Layout near device

Prevent ESD/EOS Layout near EC

Pin124 is a board ID for Cloud book (PD) EC has internal PU for EJ series

colsed to EC pin within 100 mils

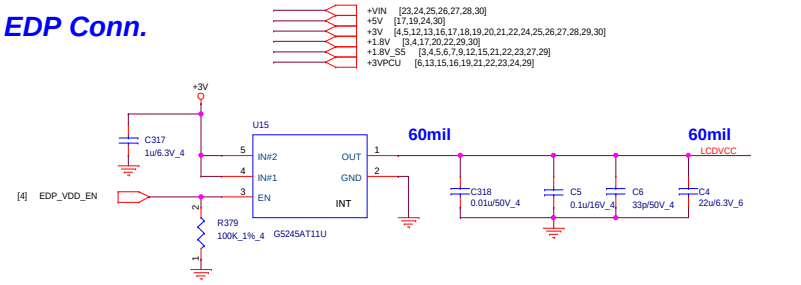
Output for type-c Apling ridge reset timming"Low " Active

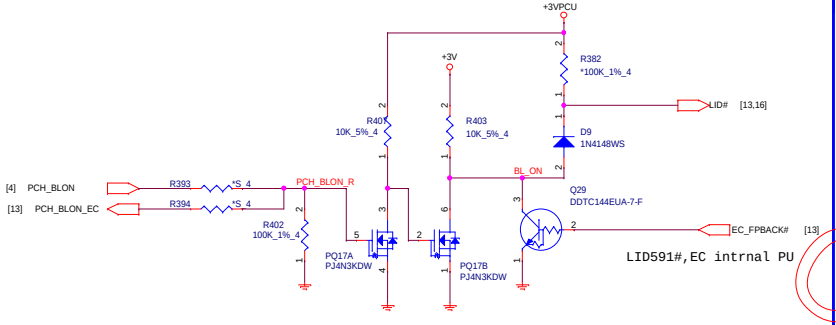
PROJECT : ZHVA

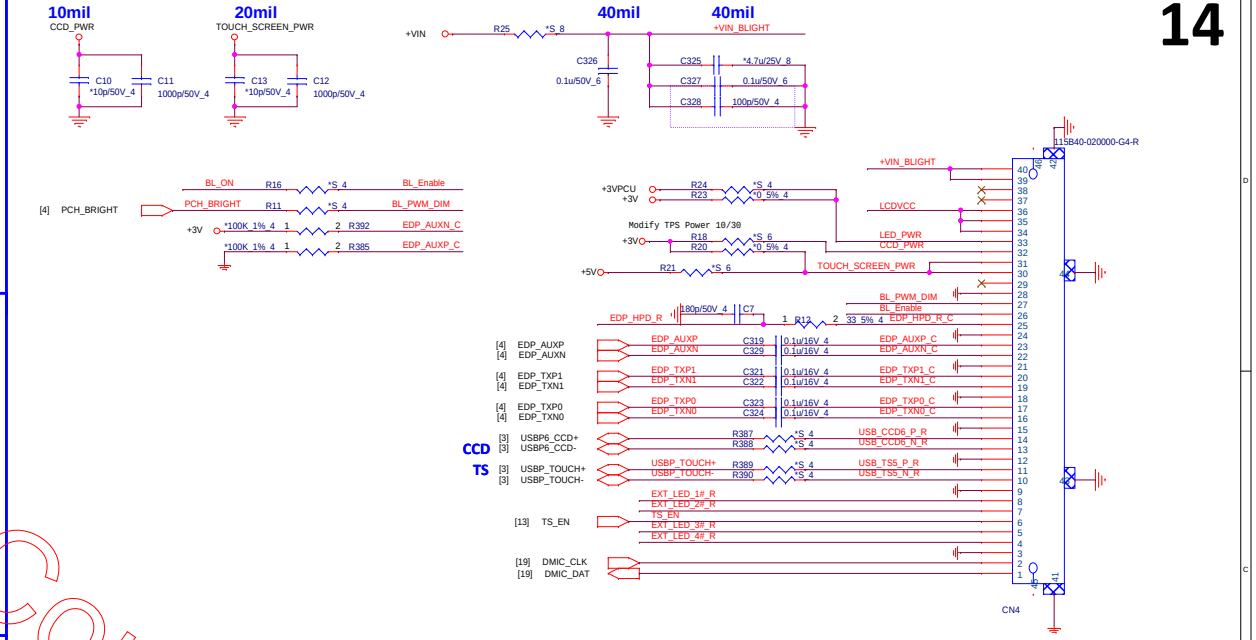
Size	Document Number	Rev
	KBC IT8987E_BX	1A

Date: Thursday, August 09, 2018 Sheet 13 of 34

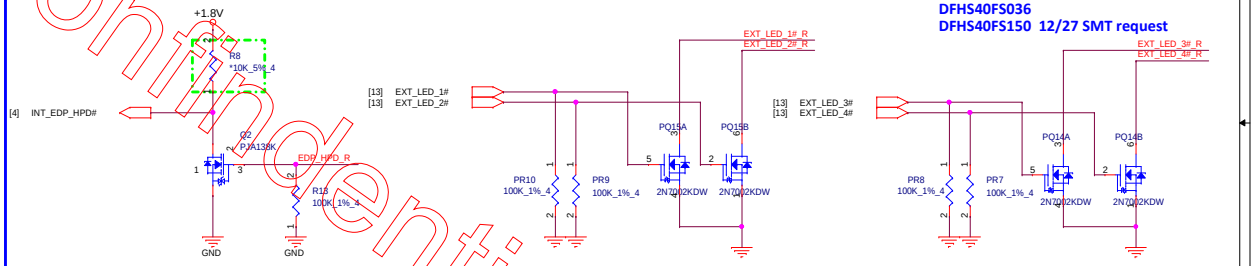
EDP Conn.





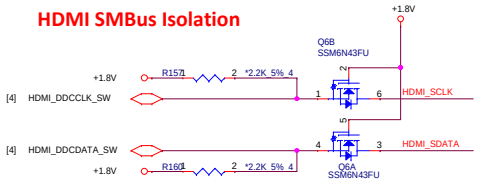


DFHS40FS036
DFHS40FS150 12/27 SMT request



HDMI Conn.

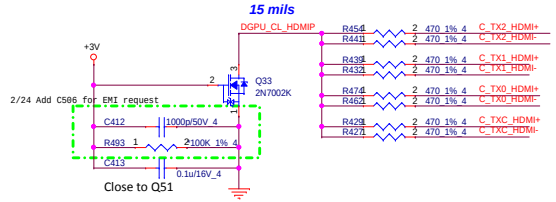
HDMI SMBus Isolation



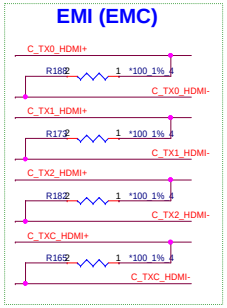
Intel Requesrt Rds_ON <3.5ohm

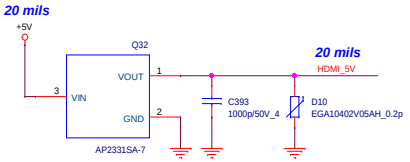
HDMI-Level shift (HDM)

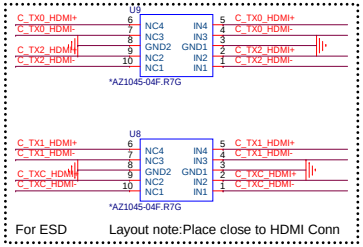
Close to HDMI connector



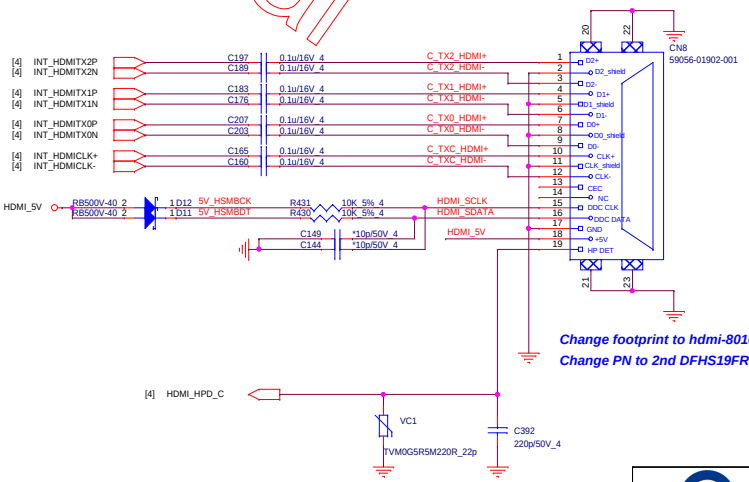
EMI (EMC)







For ESD Layout note:Place close to HDMI Conn

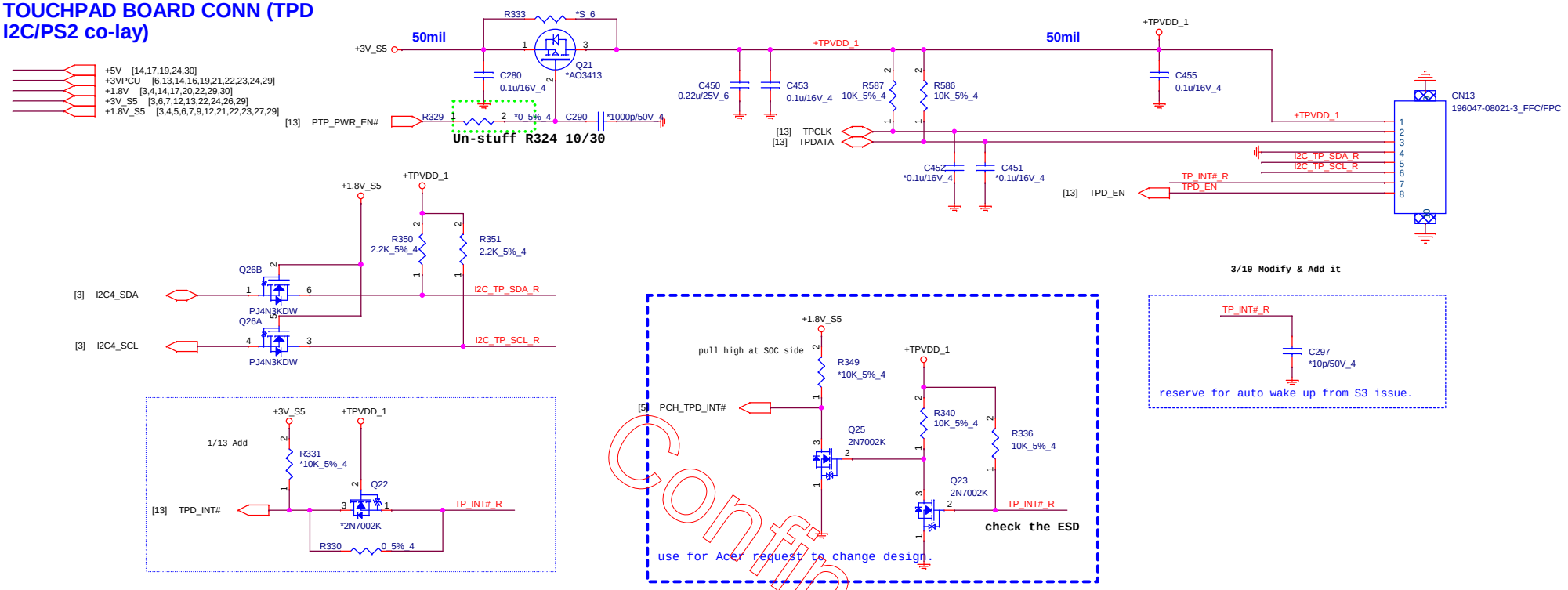


Change footprint to hdmi-80103-1121-19p-ldv-smt
Change PN to 2nd DFHS19FR072 due to DFHS19FR079 SDA test fail

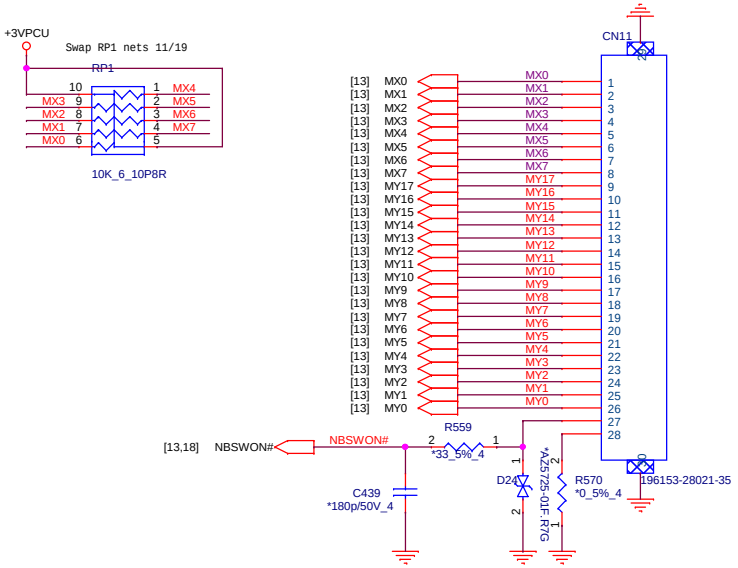
Quanta Computer Inc.
PROJECT : ZHVA

Size	Document Number	Rev
	eDP/HDMI/Camera	1A
Date: Thursday, August 09, 2018	Sheet 14 of 34	

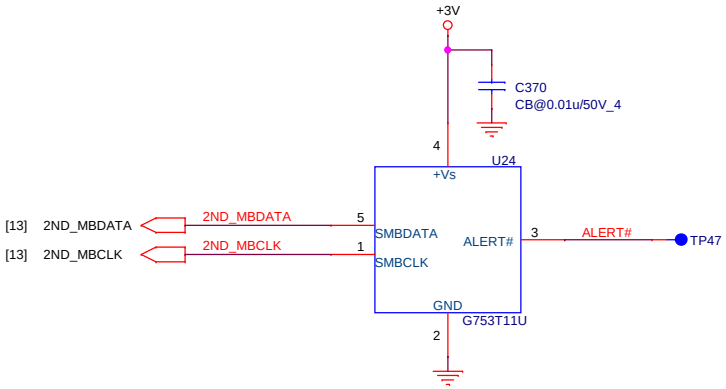
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)



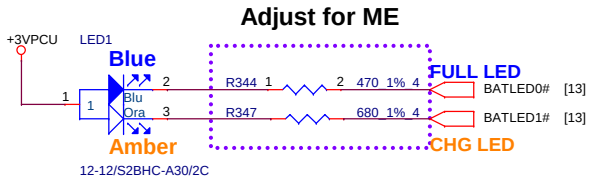
KEYBOARD (KBC)



CPU Thermal sensor(THS) / MB Local TEMP (THM)

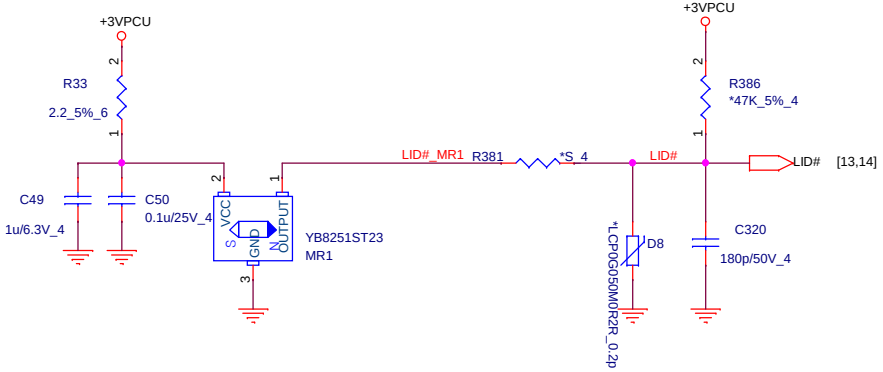


LED(UIF)



Del option Power SW

Lid

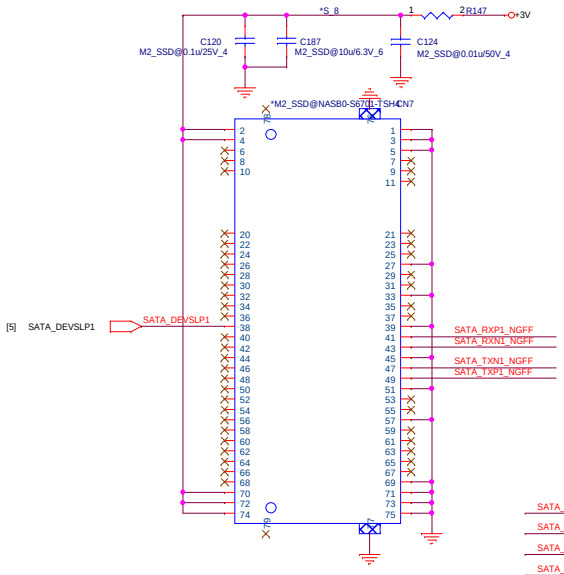


GMR(option)

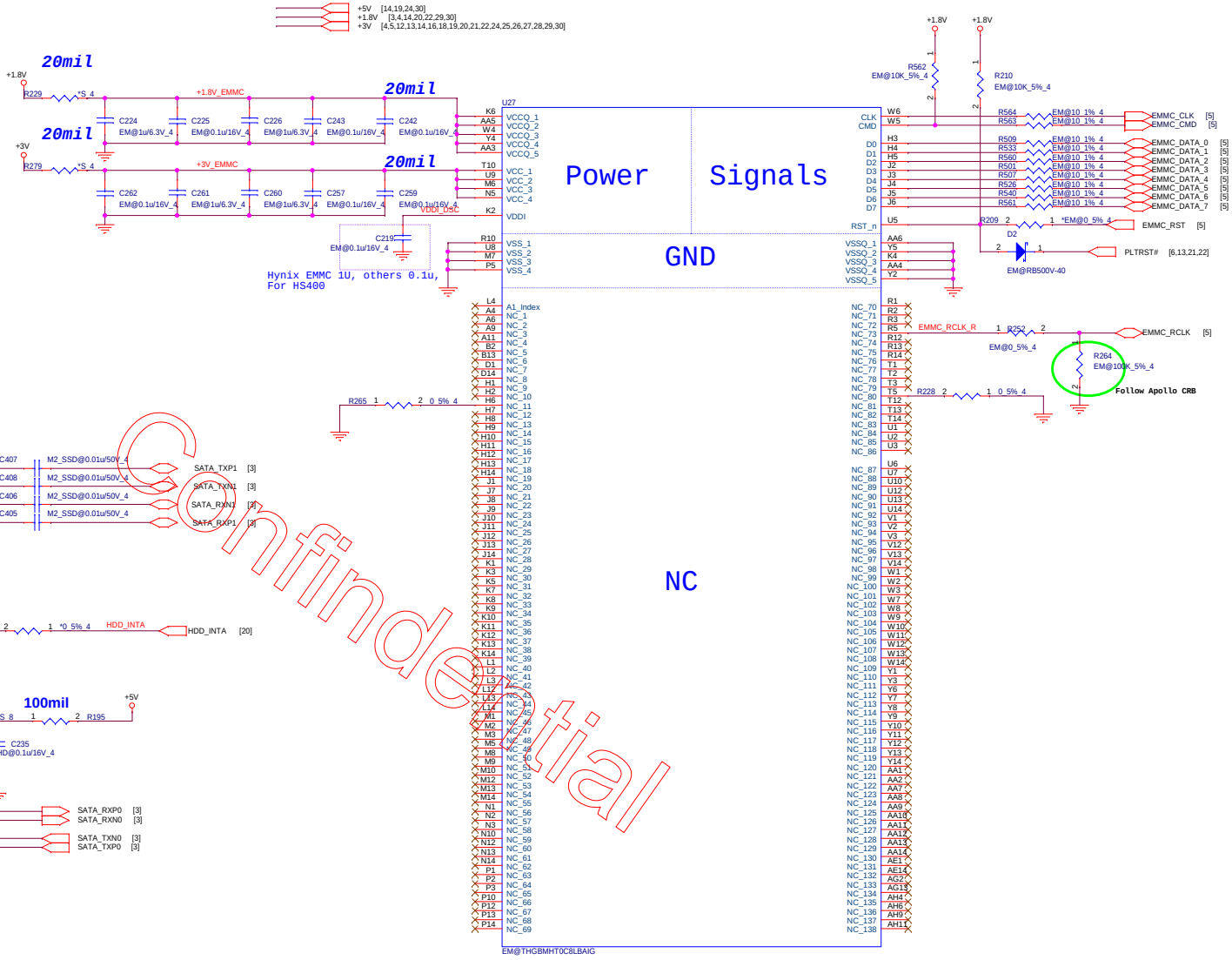
Del option GMR

Quanta Computer Inc. PROJECT ZHVA		
Size	Document Number Thm/Lid/LED	Rev 1A
Date: Thursday, August 09, 2018	Sheet 16 of 34	

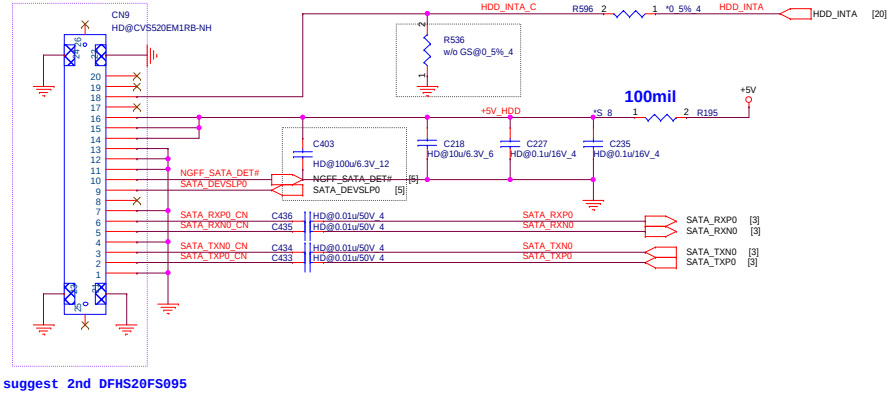
SATA HDD Conn



eMMC



SATA HDD



SMT suggest 2nd DFHS20FS095

USB 3.0 Connector

2/26 add

Enable: Low Active /2A

+5V_S5

C420 4.7u/10V_6

AP2822HKETR-G1

IN VOUT GND EN FLAG

5VUSB_0

[13] USBON#

USBON#

U26

USB_OC1#

[3] USB30_RX0-
[3] USB30_RX0+

USB30_RX0-
USB30_RX0+

R283 0_5%_4

R276 0_5%_4
R511 0_5%_4

[3] USBP0+
[3] USBP0-

R508 0_5%_4
R271 0_5%_4

[3] USB30_TX0-
[3] USB30_TX0+

C239 0.1u/25V_4
C238 0.1u/25V_4

USB30_TX0-_C
USB30_TX0+_C

R263 0_5%_4

USB30_RX1-_R
GND
USB30_RX1+_R
USBP0+_R
GND
USBP0-_R
USB30_TX1-_R
5VUSB_0
USB30_TX1+_R

Shield Shield Shield Shield

StdA_SSRX- GND StdA_SSRX+ D+ GND_Drain D- StdA_SSTX- VBUS StdA_SSTX+

CN10
53065-00902-001

7/16 change to 0 ohm for ESD data pin issue.

Close USB3.0

5VUSB_0

D15
AZ5725-01F.R7G

C415 470p/50V_4
C414 0.1u/25V_4
C409 100u/6.3V_12

USBP0+_R
USBP0-_R

D20
PESD5V0X2UM

U10

USB30_RX1-_R
USB30_RX1+_R
GND#1
USB30_TX1-_R
USB30_TX1+_R

Line-1 Line-2 Line-3 Line-4 NC#4 NC#3 NC#2 NC#1

AZ1043-04F.R7G

USB 2.0 X 1

Enable: Low Active /2A

+5V_S5

C361 4.7u/10V_6

AP2822HKETR-G1

IN VOUT GND EN FLAG

5VUSB_1

USBON#

U17

USB_OC1# [3]

Close to CN6

7/16 rreserve 0 ohm for ESD data pin issue.

[3] USBP2+
[3] USBP2-

R597 0_5%_4
R598 0_5%_4

USB2.0_CONN2+
USB2.0_CONN2-

D28
*PESD5V0X2UM

+3V_S5 [3,6,7,12,13,15,22,24,26,29]
+3V [4,5,12,13,14,16,17,19,20,21,22,24,25,26,27,28,29,30]
+5V_S5 [6,24,26,27,28]

D/B Port USB 2.0

<Layout note>
Close to CONN

5VUSB_1

C345 100u/6.3V_12
C346 0.1u/16V_4

USB2.0_CONN2+
USB2.0_CONN2-

[3] USB_CAR7-
[3] USB_CAR7+

[13,15] NBSWON#

NBSWON#

+3V

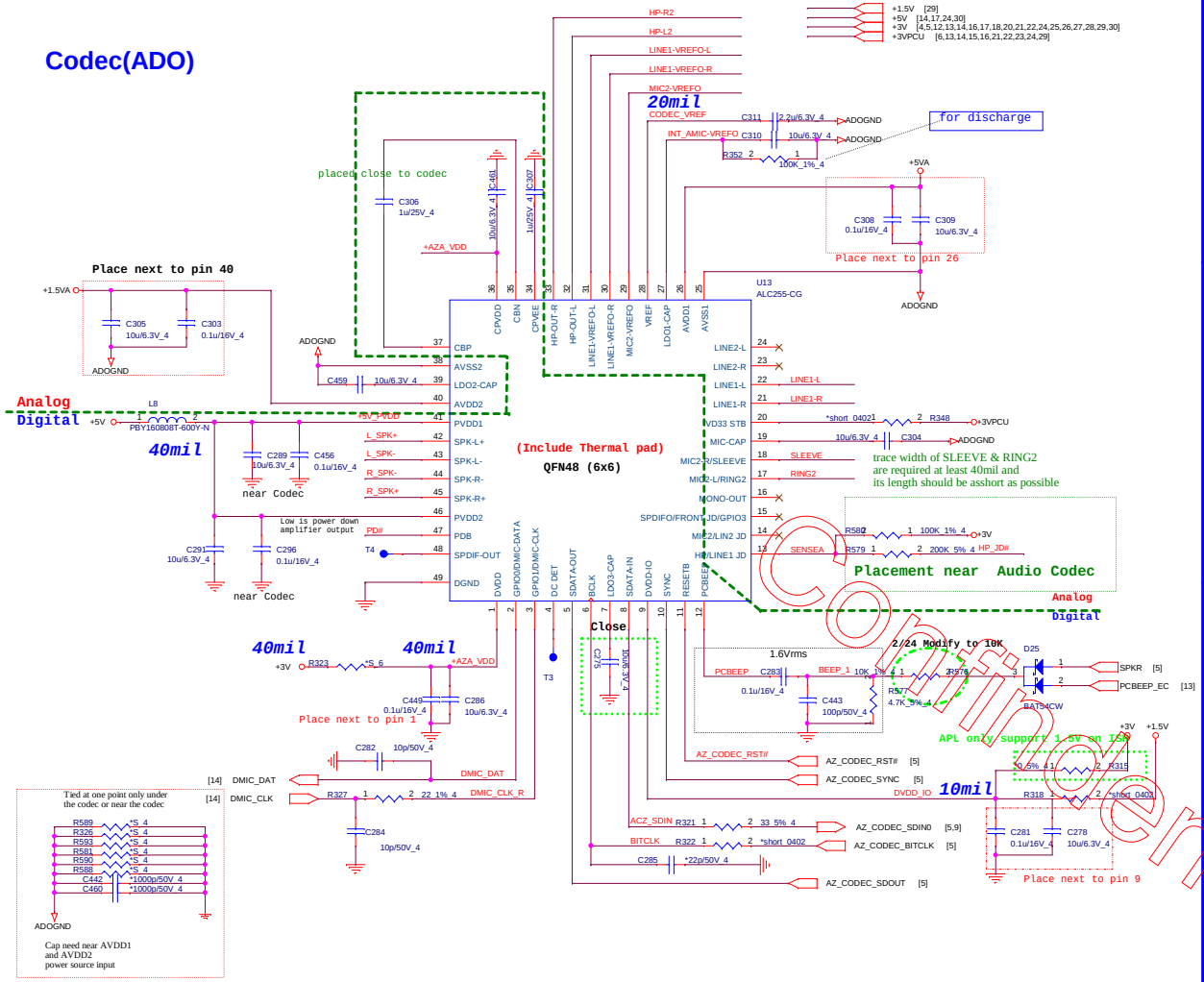
C381 *100u/6.3V_12
C368 0.1u/16V_4

CN6

1619-01601-V05

Quanta Computer Inc. PROJECT : ZHVA		
Size	Document Number: USB CONN	Rev: 1A
Date: Thursday, August 09, 2018	Sheet 18 of 34	

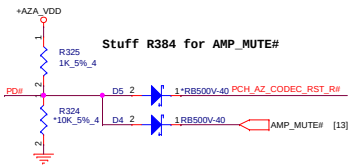
Codec(ADO)



Grounding circuit(ADO)

If IC pin20 connect to always power,
Grounding circuit can be remove

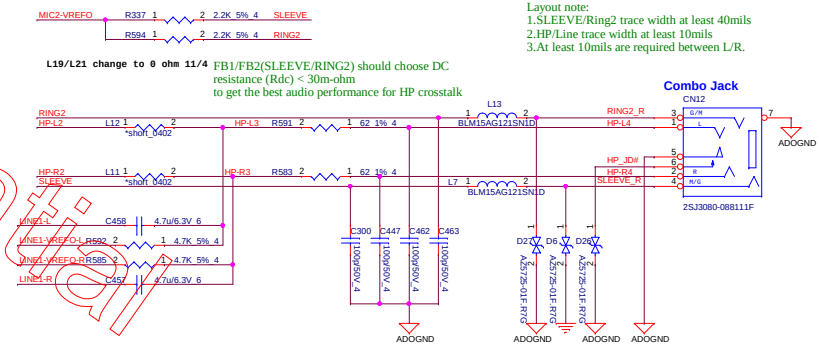
Mute(ADO)



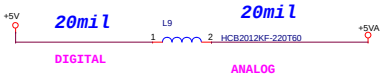
Power (ADO)

For A-MIC LDO

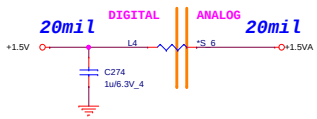
HEADPHONE/MIC/LINE combo (ADO)



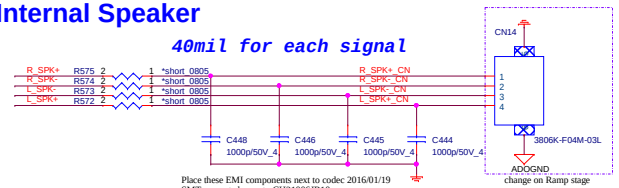
Codec PWR 5V(ADO)



Codec PWR 1.5V(ADO)



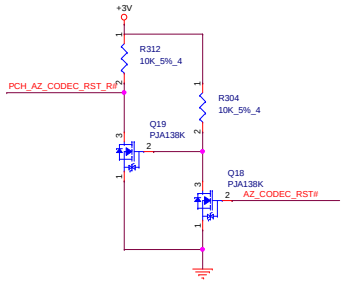
Internal Speaker



Place these EMI components next to codec 2016/01/19
SMT request change to CH21006JB10

A-Mic

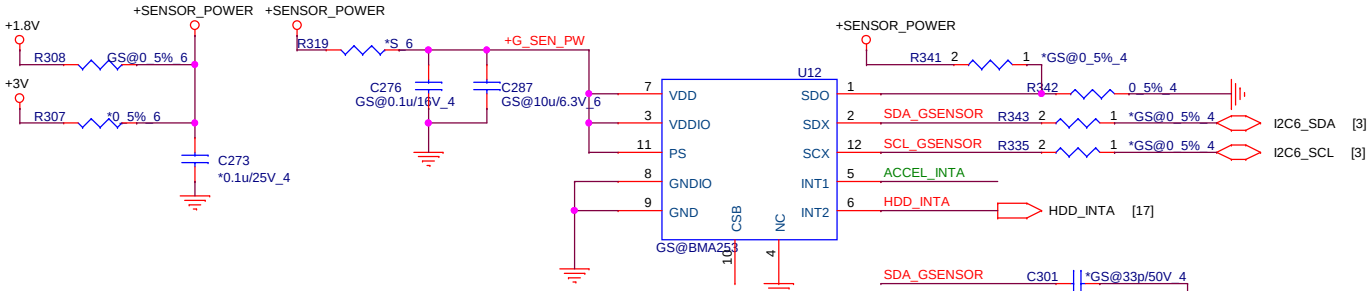
Level shift



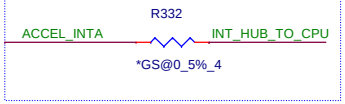
Quanta Computer Inc.
PROJECT : ZHVA

Size	Document Number	Rev
	Codec ALC225	1A
Date: Thursday, August 09, 2018	Sheet 19 of 34	

G-sensor

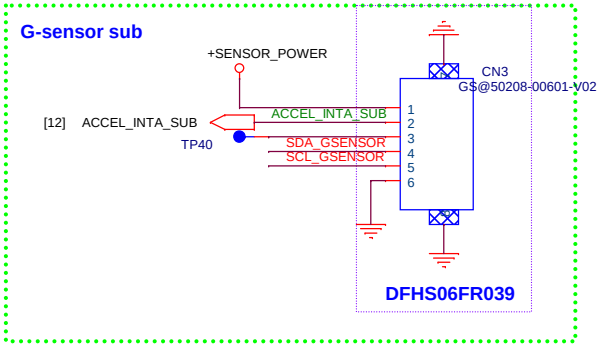


Reserve

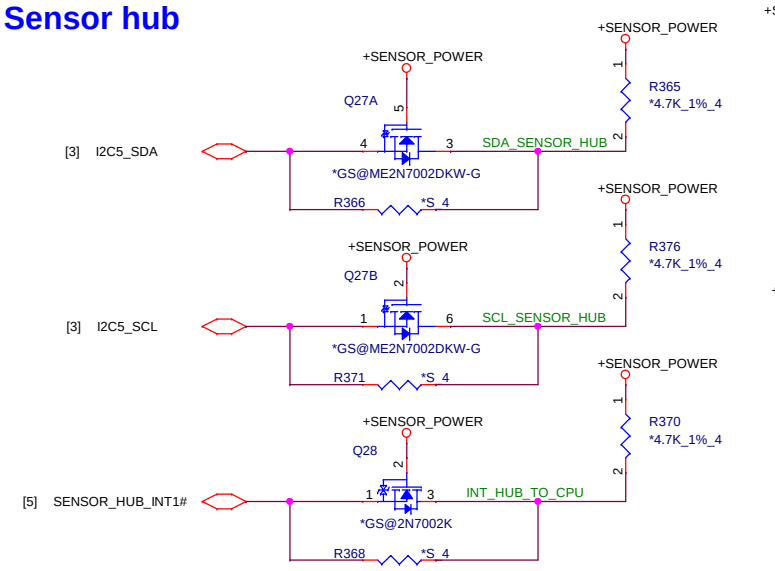


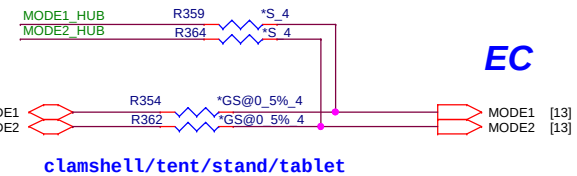
Address: I2C mode,SDO pin
PD:0X18
PU:0X19

G-sensor sub



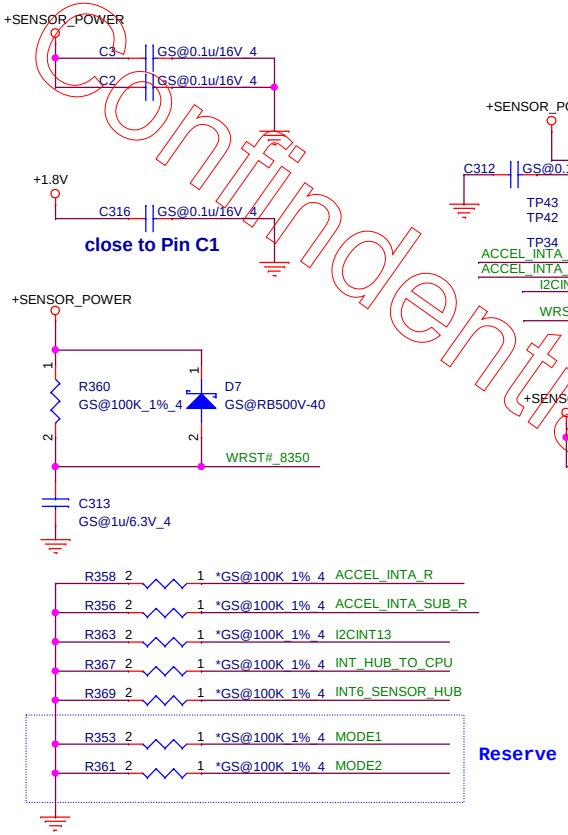
Sensor hub



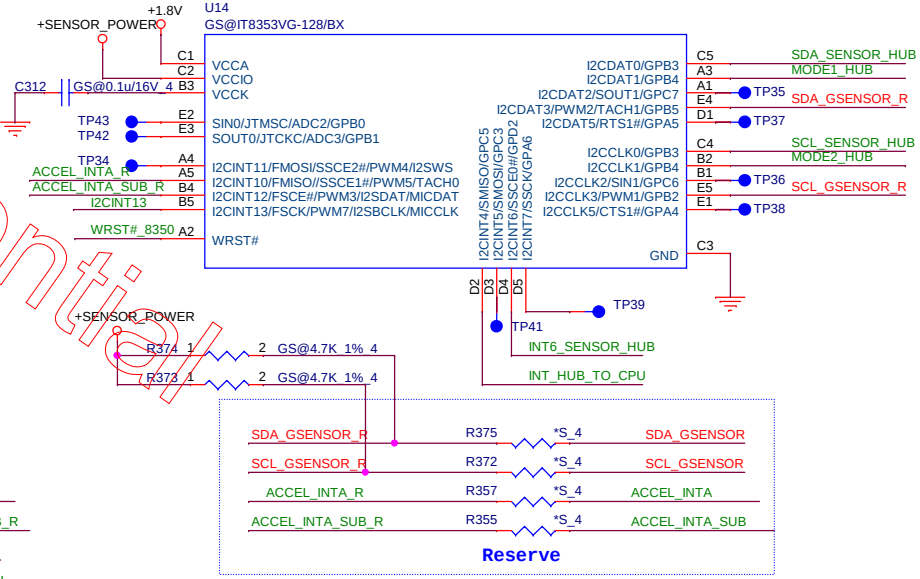


clamshell/tent/stand/tablet

EC



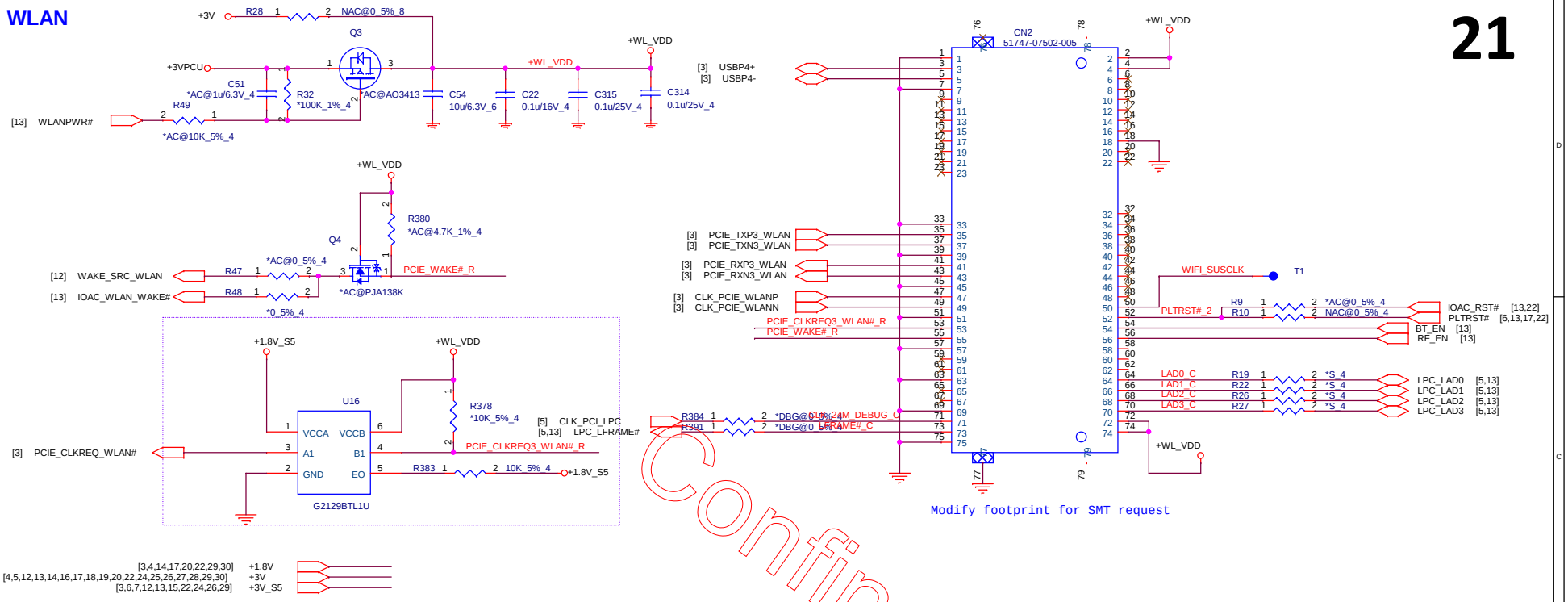
Reserve



Reserve

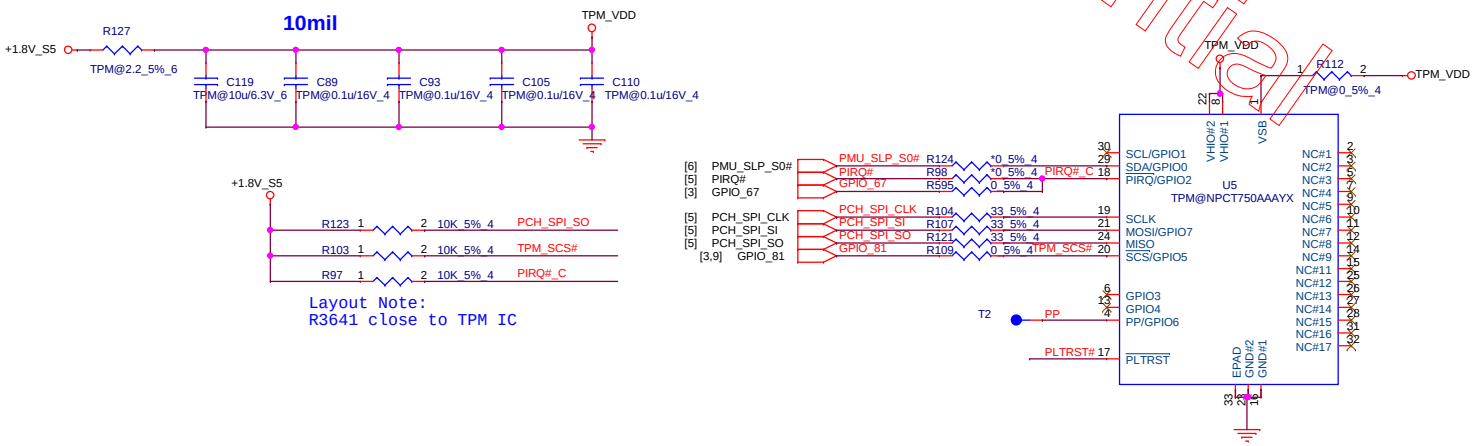
Quanta Computer Inc.		
PROJECT : ZHVA		
Size	Document Number: SENSOR HUB	Rev: 1A
Date: Thursday, August 09, 2018	Sheet 20 of 34	

WLAN



Modify footprint for SMT request

TPM (TPM)



Layout Note:
R3641 close to TPM IC

NOTE:
- Place 0.1 uF capacitors as close as possible to the device power pins.
- VHIO can be either +3.3V or +1.8V.
- It is recommended to connect VHIO to V_RUN.
- VALW can be either +3.3V or +1.8V.
- VALW power rail should be powered whenever the system is powered by any power source.
- For details regarding the TPM power sequence, see the NPCT75x Datasheet and Board Design Guidelines.

Quanta Computer Inc.		
PROJECT : ZHVA		
Size	Document Number: NGFF/BT/TPM	Rev: 1A
Date: Thursday, August 09, 2018	Sheet 21 of 34	

(1.5A) 60 mils

+3V_S5 R94 2 1 0_5%_8 Q5 +3VPCU 1 3 +LAN_POWER
C57 *AC@1u/6.3V_4 R34 *AC@100K_1%_4 *AC@AO3413
[13] LANPWR# R30 *AC@10K_1%_4

+3V [4,5,12,13,14,16,17,18,19,20,21,24,25,26,27,28,29,30]
+3VPCU [6,13,14,15,16,19,21,23,24,29]

For RTL8111H
* Place 0.1uF CAP close to each VDD10 pin-- 3, 8, 22, 30

For RTL8111H
* Place 1uF CAP close to each VDD10 pin-- 22 (reserve)

REGOUT 60 mils R125 *S_8 60 mils
C376 0.1u/16V_4 C384 0.1u/16V_4 C377 0.1u/16V_4 C380 0.1u/16V_4 C378 0.1u/16V_4
VDD10 C385 1u/6.3V_4 C383 0.1u/16V_4

+LAN_POWER 40 mils
C98 0.1u/16V_4 C85 0.1u/16V_4 C387 *4.7u/6.3V_6 C86 *4.7u/6.3V_6

IOAC circuit (MPC)

For RTL8111H
* Place 0.1uF/4.7uF CAP close to each VDD33 pin-- 11, 32

+1.8V_S5 R419 10K_5%_4 +LAN_POWER R422 10K_5%_4
[3] PCIE_LAN_WAKE# R420 0_5%_4 Q30 2N7002K PCIE_LAN_WAKE#_R
[13] LAN_WAKE# R421 2 1 *0_5%_4

+1.8V R311 2 1 0_5%_4
+1.8V_S5 R317 2 1 *0_5%_4 R313 10K_5%_4
[3] CLK_PCIE_LAN_REQ# Q17 PJA138K PCIE_REQ_LAN#_R
R314 2 1 *0_5%_4

2/6 Change from 10pF to 12pF

XTAL2 C102 12p/50V_4 Y1 25MHZ/30ppm C108 12p/50V_4 XTAL1
VDD10 R101 2.49K_1%_4 RSET 10 mils
C117 *10p/50V_4 TP2 TP3 TP1
C116 *10p/50V_4
+LAN_POWER

PERSTB R130 *AC@0_4 IOAC_RST# [13,21]
R129 NAC@0/J_4 PLTRST# [6,13,17,21]

default Non-IOAC 11/6

U6 RTL8111H-CG
GND AVDD33#2 RSET AVDD10#3 CKXTAL2 CKXTAL1 LED0 LED1/GPO LED2
MDI_0+ MDI_0- MDIP0 MDIN0 AVDD10#1 MDIP1 MDIN1 MDIP2 MDIN2 AVDD10#2
REGOUT VDDREG DVDD10 LANWAKEB ISOLATEB PERSTB HSON HSOP
MDIP3 MDIN3 AVDD33#1 CLKREQB HSIP HSIN REFCLK_P REFCLK_N
MDI_3+ MDI_3-

REGOUT +LAN_POWER VDD10 PCIE_LAN_WAKE#_R
ISOLATEB PERSTB
C112 0.1u/16V_4 PCIE_RXN2_LAN C107 0.1u/16V_4 PCIE_RXP2_LAN
PCIE_RXN2_LAN [3] PCIE_RXP2_LAN [3]
+3V R416 1K_5%_4 R417 15K_5%_4

CLK_PCIE_LANN CLK_PCIE_LANP PCIE_TXN2_LAN PCIE_TXP2_LAN
CLK_PCIE_LANN [3] CLK_PCIE_LANP [3] PCIE_TXN2_LAN [3] PCIE_TXP2_LAN [3]
PCIE_REQ_LAN#_R

Consider VCC33 may be connected to Main Power or chipset/bios's GPO, the pull-low resistor R14 can be NC only when Main Power or chipset/bios's GPO can ensure to drive the ISOLATEB pin to a voltage level < 0.8V at the system state S1~S5.

If the ISOLATEB pin can not be well-controlled to a voltage level < 0.8V at S1~S5, the pull-low resistor R14 is needed to make sure the LAN chip is well isolated.

SQ Transformer

U18 A-8300G
MDI_0+ MDI_0- MDI_1+ MDI_1- MDI_2+ MDI_2- MDI_3+ MDI_3-
TCT1 TD1+ TD1- TC2 TD2+ TD2- TC3 TD3+ TD3- TC4 TD4+ TD4- GND
NC#4 MX1+ MX1- NC#3 MX2+ MX2- NC#2 MX3+ MX3- NC#1 MX4+ MX4-
LAN_MCT0 LAN_MX0+ LAN_MX0- LAN_MCT1 LAN_MX1+ LAN_MX1- LAN_MCT2 LAN_MX2+ LAN_MX2- LAN_MCT3 LAN_MX3+ LAN_MX3-
R41 R53 R72 R85 75_1%_12
LANCT3
C343 0.01u/50V_4
C332 10p/3KV_1808

GST5009B LF H=4.0mm

Layout:All termination signal should have 30 mil trace

RJ45 Connector

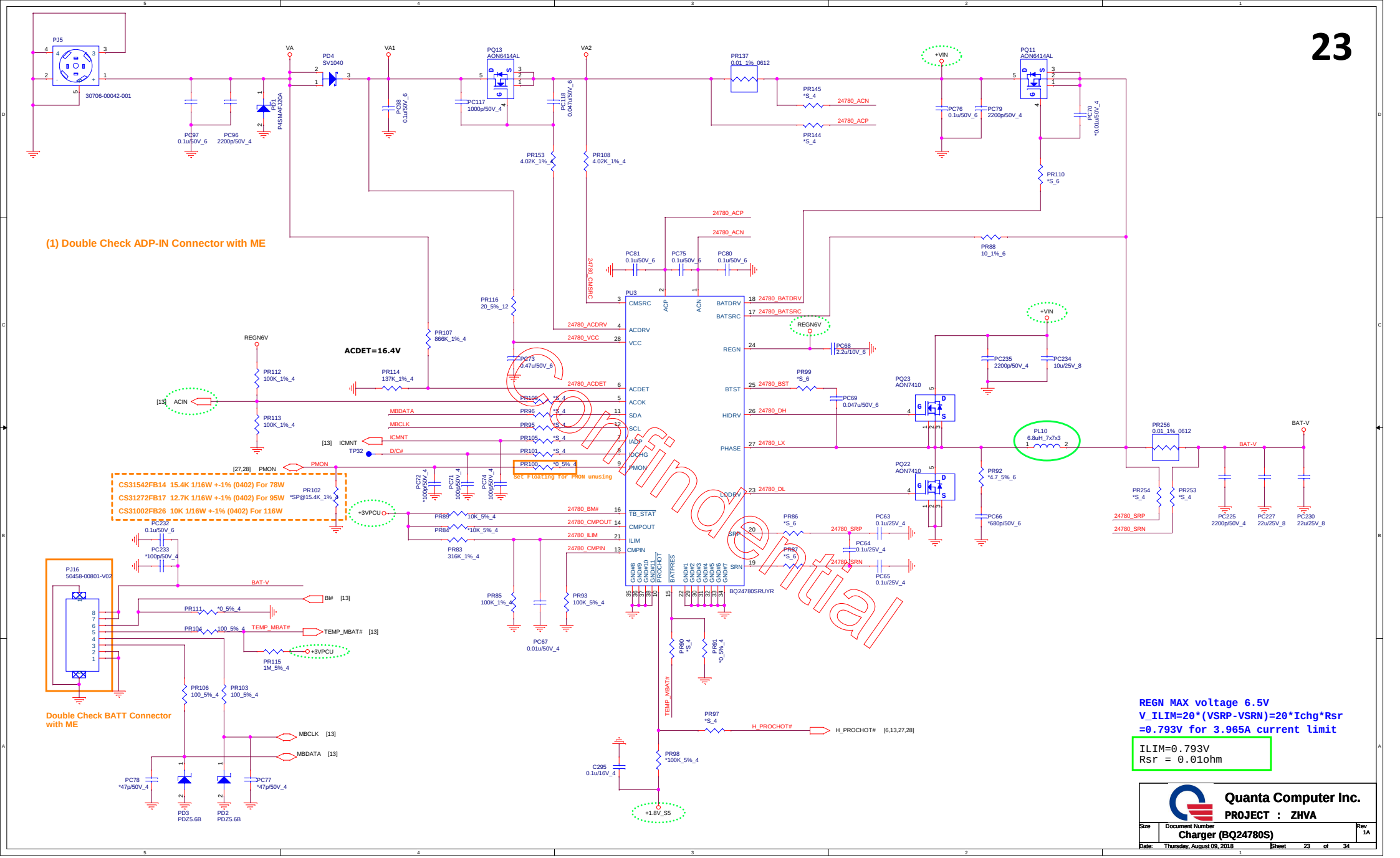
CN5 60404-08GAX
LAN_MX0+ LAN_MX0- LAN_MX1+ LAN_MX2+ LAN_MX2- LAN_MX1- LAN_MX3+ LAN_MX3-

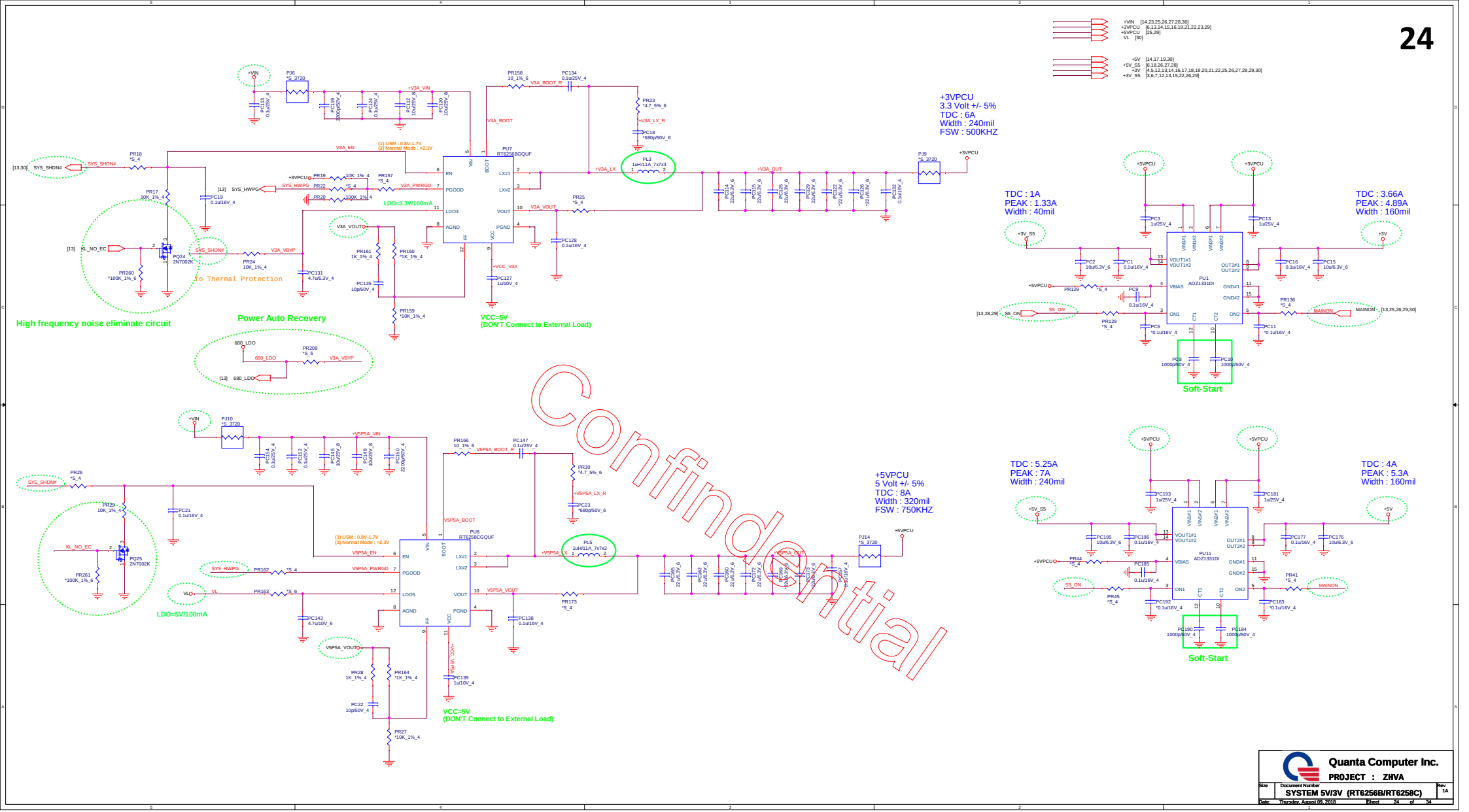
SYMBOL AOP,PN YMI

Quanta Computer Inc.
PROJECT : ZHVA

Size	Document Number	Rev
	LAN(RTL8111H-CG)	1A

Date: Thursday, August 09, 2018 Sheet 22 of 34


(1) Double Check ADP-IN Connector with ME
ACDET=16.4V
CS31542FB14 15.4K 1/16W +-1% (0402) For 78W
CS31272FB17 12.7K 1/16W +-1% (0402) For 95W
CS31002FB26 10K 1/16W +-1% (0402) For 116W
Set Floating for PMON unusing
Double Check BATT Connector with ME
REGN MAX voltage 6.5V
V_ILIM=20*(VSRP-VSRN)=20*Ichg*Rsr
=0.793V for 3.965A current limit
ILIM=0.793V
Rsr = 0.01ohm
Quanta Computer Inc.
PROJECT : ZHVA
Charger (BQ24780S)
Thursday, August 09, 2018
BQ24780SRUYR
Orifinal

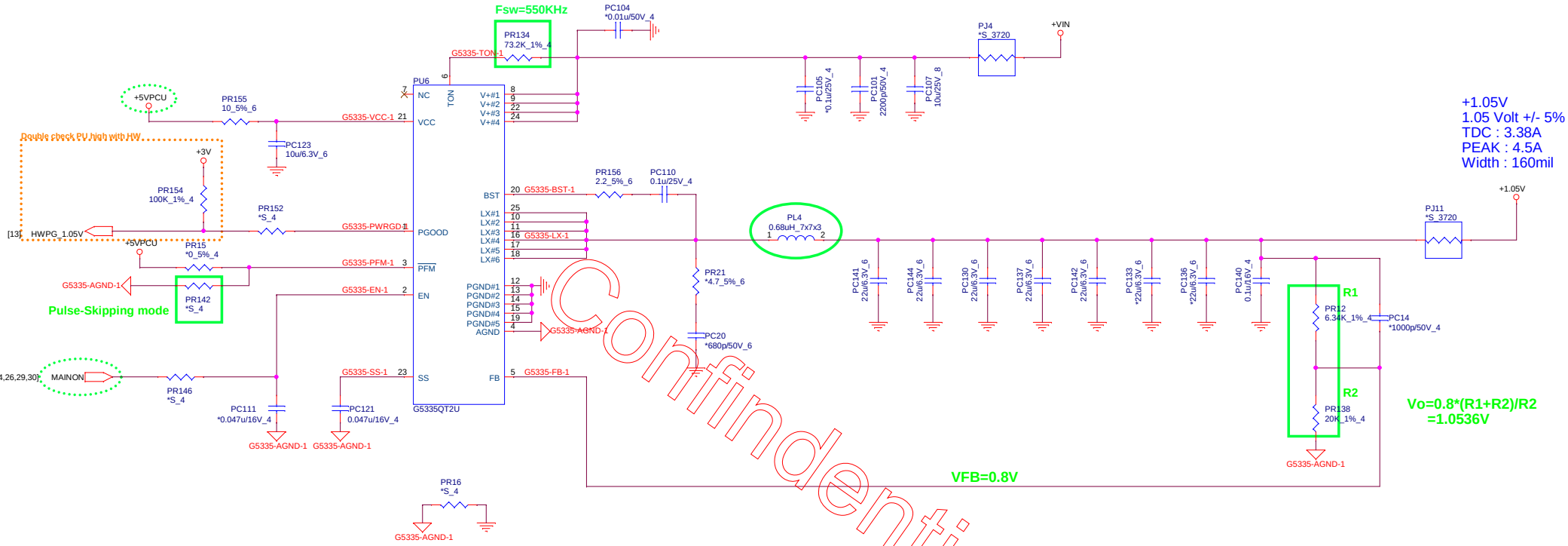


Quanta Computer Inc.
PROJECT : ZHVA

Size	Document Number	Rev
	SYSTEM 5V/3V (RT6256B/RT6258C)	1A

Date: Thursday, August 09, 2018 Sheet 24 of 34

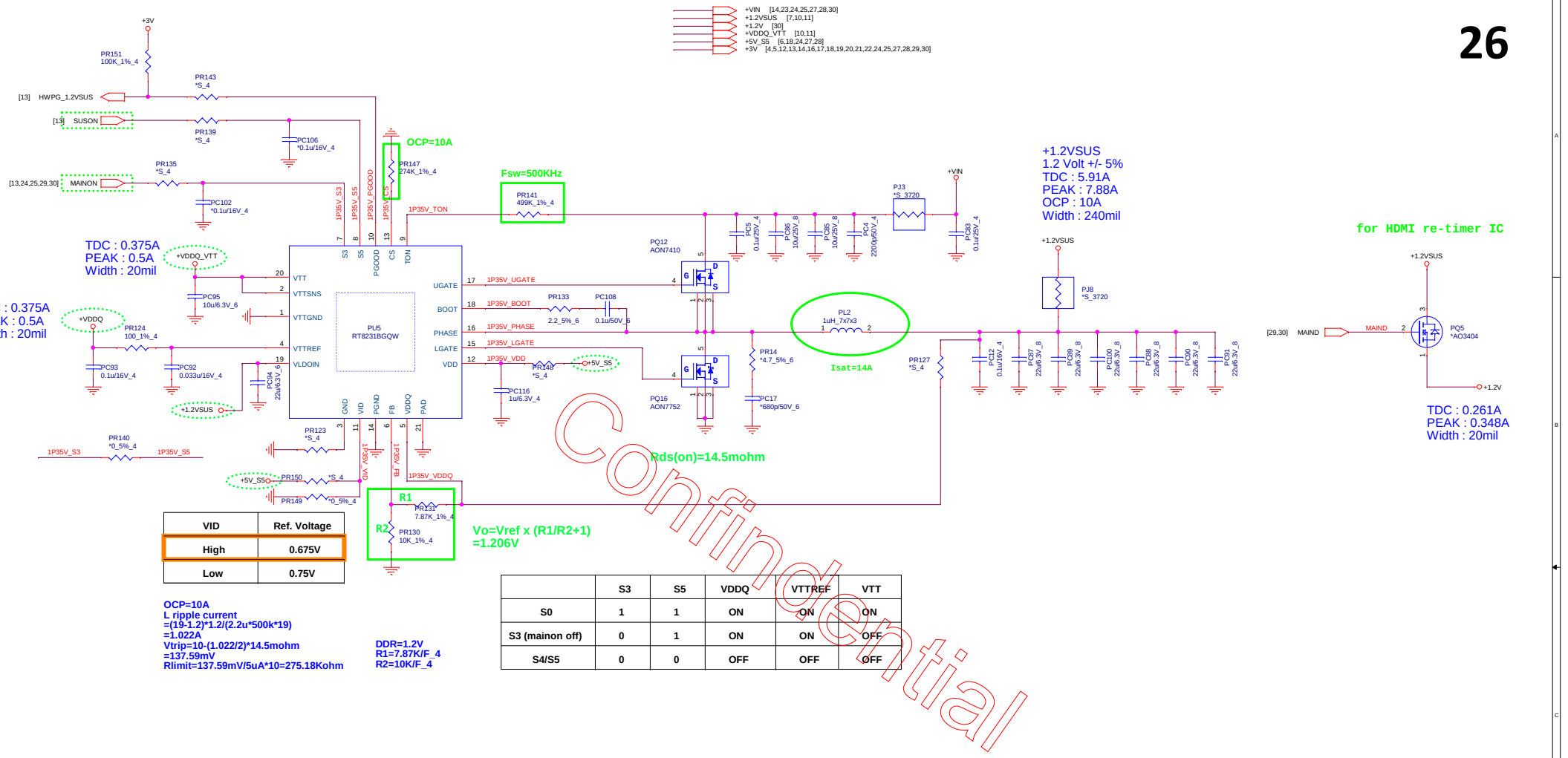
+VIN [14,23,24,26,27,28,30]
+1.05V [6,7,27,28]
+5VPCU [24,29]
+3V [4,5,12,13,14,16,17,18,19,20,21,22,24,26,27,28,29,30]



+1.05V
1.05 Volt +/- 5%
TDC : 3.38A
PEAK : 4.5A
Width : 160mil

Quanta Computer Inc.
PROJECT : ZHVA

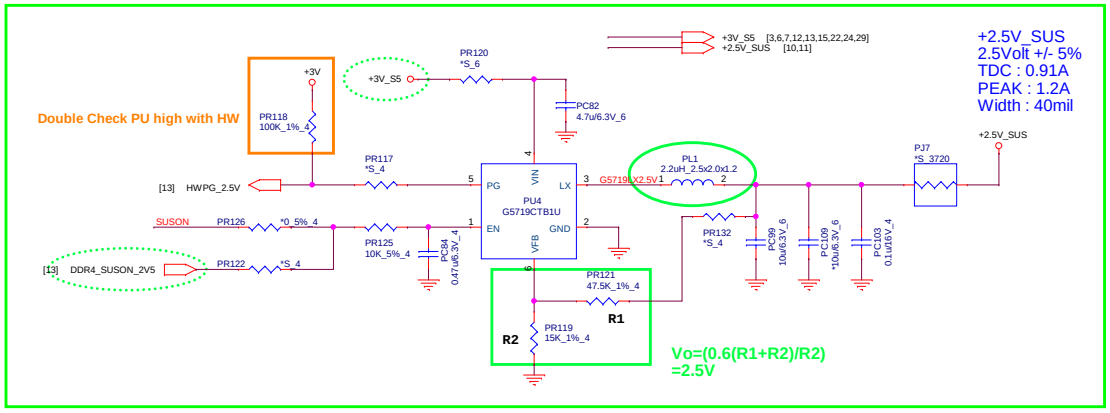
Size	Document Number	Rev
	+1.05V (G5335QT2U)	1A
Date: Thursday, August 09, 2018	Sheet 25 of 34	



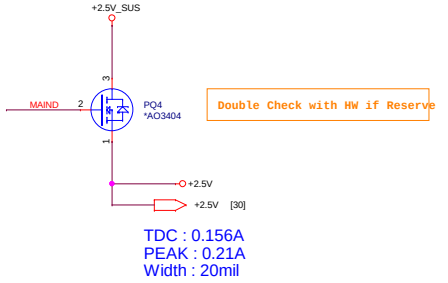
VID	Ref. Voltage
High	0.675V
Low	0.75V

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

+2.5VSUS Power Rail For DDR4



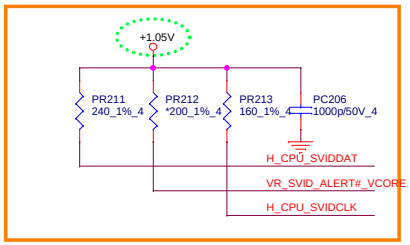
Reserve +2.5V for DDR4 VDDSPD



Quanta Computer Inc.	PROJECT : ZHVA	
Size	Document Number: DDR4 (RT8231BGQW)	Rev: 1A
Date: Thursday, August 09, 2018	Sheet 26 of 34	

SVID_CLK : UP:160 ohm Series:95 ohm
SVID_ALERT : UP:68 ohm Series:220 ohm
SVID_DATA : UP:240 ohm Series:20 ohm

+VIN [14,23,24,25,26,28,30]
+VCC_VCCGI [7]
+3V [4,5,12,13,14,16,17,18,19,20,21,22,24,25,26,28,29,30]
+5V_S5 [6,18,24,26,28]
+1.8V_S5 [3,4,5,6,7,9,12,15,21,22,23,29]
+1.05V [6,7,25,28]



Check SVID PU UP R/Series R with HW

Check EN Sequence with HW

PU12 RT3601EAGQW

Isat=45A
DCR=0.66m ohm

Place close with VCORE Inductor B=3650

B=4250
PUT COLSE TO VCCGI HOT SPOT

Total 20pcs 22u_0603 (with HW)

+VCCGI

Icc Max：25A
Icc TDC：18A
Vboot：0V
OCP：35A
Fsw：550KHZ

VCCGI L/L :

R_DC_LL：6mV/A
R_AC_LL：6mV/A

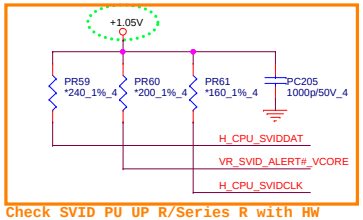
Vset1	1425mV
Delta Vset1	901mV
Vset2	675mV
Delta Vset2	49.8mV
Vset3	974mV
Delta Vset3	950mV
VTsen	448mV

Quanta Computer Inc.
PROJECT : ZHVA

Size	Document Number	Rev
	+VCC_VCCGI (RT3601EAGQW)	1A

Date: Thursday, August 09, 2018 Sheet 27 of 34

SVID_CLK : UP:160 ohm Series:95 ohm
SVID_ALERT : UP:68 ohm Series:220 ohm
SVID_DATA : UP:240 ohm Series:20 ohm



Check SVID PU UP R/Series R with HW

Check EN Sequence with HW

+VIN [14,23,24,25,26,27,30]
+VNN [7]
+5V_S5 [6,18,24,26,27]
+1.05V [6,7,25,27]
+3V [4,5,12,13,14,16,17,18,19,20,21,22,24,25,26,27,29,30]

Vset1	124.9mV
Delta Vset1	899mV
Vset2	373.4mV
Delta Vset2	1.14V
Vset3	176mV
Delta Vset3	950mV
VTsen	548mV

+VNN

Icc Max：5.6A
Icc TDC：N/A
Vboot：1.05V
OCP：10A
Fsw：600KHZ

Quanta Computer Inc.
PROJECT : ZHVA

Size	Document Number	Rev
	+VNN (RT3601EAGQW)	1A
Date: Thursday, August 09, 2018	Sheet 28 of 34	

[6,13,14,15,16,19,21,22,23,24] +3VPCU
[3,4,5,6,7,9,12,15,21,22,23,27] +1.8V_S5
[7] +1.24V_S5
[3,4,14,17,20,22,30] +1.8V
[19] +1.5V

[3,6,7,12,13,15,22,24,26] +3V_S5
[24,25] +5VPCU
[4,5,12,13,14,16,17,18,19,20,21,22,24,25,26,27,28,30] +3V

+1.8V_S5
1.8Volt +/- 5%
TDC : 0.85A
PEAK : 1.13A
Width : 40mil

H cha _ pull up to 3 _

+3V_S5, +3VPCU
PR165 100K_1%_4
PR168 *S_6
PC146 4.7u/6.3V_4
PR169 *S_4
[13] HWPG_1.8V_S5
[13,24,28] S5_ON
PR171 120K_1%_4
PC153 0.1u/16V_4
PU9 G5719CTB1U (PG, VIN, LX, EN, GND, VFB)
G5719LX_1.8V
PL6 2.2uH_2.5x2.0x1.2
PR174 *S_4
PC151 10u/6.3V_6
PC155 *10u/6.3V_6
PC149 0.1u/16V_4
PJ13 *S_3720
+1.8V_S5

Check RC delay time with HW
(follow ZHP RC dealy time)

R1 PR167 30K_1%_4
R2 PR170 15K_1%_4

Vo=(0.6(R1+R2)/R2
=1.8V

[26,30] MAIND
PQ7 AO3404
+1.8V_S5
+1.8V

TDC : 0.173A
PEAK : 0.23A
Width : 20mil

+1.24V_S5
1.24Volt +/- 5%
TDC : 1.875A
PEAK : 2.5A
Width : 80mil

h c Hi h u c with HW

+3V_S5
PR184 100K_1%_4
PR182 *S_4
[13] HWPG_1.24V_S5
5671PG_1.24V
+3VPCU
PJ12 *S_3720
PR172 10_5%_6
5671SVIN_1.24V
PC156 0.01u/50V_4
PC159 10u/6.3V_6
PC163 1u/6.3V_4
PC24 *2200p/50V_4
PR31 *2.2_5%_6
PU10 M5671RE1U (POK, VIN#1, VIN#2, VCC, GND, NC#1, SW#1, SW#2, NC#2, FB, EN)
5671LX_1.24V
PL7 1uH_7x7x3
PC170 *22p/50V_4
PC164 *68p/50V_4
5671NC_1.24V
5671FB_1.24V
5671EN_1.24V
PR183 *S_4
PC171 *0.1u/16V_4
R1 PR179 10K_1%_4
R2 PR180 10K_1%_4
HWPG_1.8V_S5

+1.24V_S5
PJ1 *S_3720
5671FB_1.24V_S
PR175 *S_4
PC158 0.1u/25V_4
PC161 22u/6.3V_6

Vo=0.6*(R1+R2)/R2
=1.24V

Confidential

+1.5V
1.5Volt +/- 5%
TDC : 0.39A
PEAK : 0.52A
Width : 20mil

+3VPCU
PR259 *S_8
PC226 10u/6.3V_6
PC229 0.1u/50V_6
[13,24,25,26,30] MAINON
PR251 *S_4
PR250 100K_5%_4
PC224 *0.1u/50V_6
PU14 G9661MF11U (VIN, NC, VO, VEN, VPP, GND#1, POK, GND#2, ADJ)
PR258 *S_8
+1.5V
+5VPCU
PR257 *S_4
PC231 1u/25V_4
[13] HWPG_1.5V
+3V
PR249 100K_5%_4
PC228 10u/6.3V_6
R1 PR255 30K_1%_4
R2 PR252 34K_1%_4

Vref=0.8V

Vo =0.8(1+R1/R2)
=1.506V

Quanta Computer Inc.
PROJECT : ZHVA

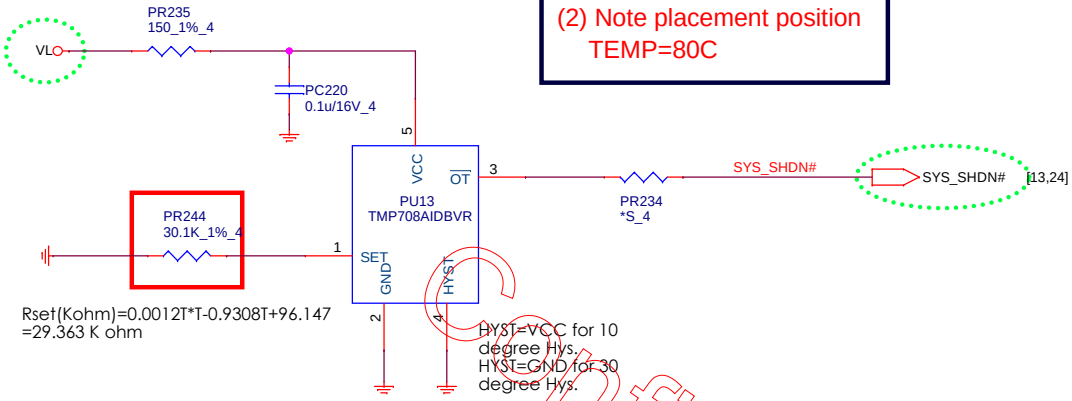
Size	Document Number	Rev
	+1.8V_S5 / +1.24V_S5 / +1.5V	1A

Date: Thursday, August 09, 2018 Sheet 29 of 34

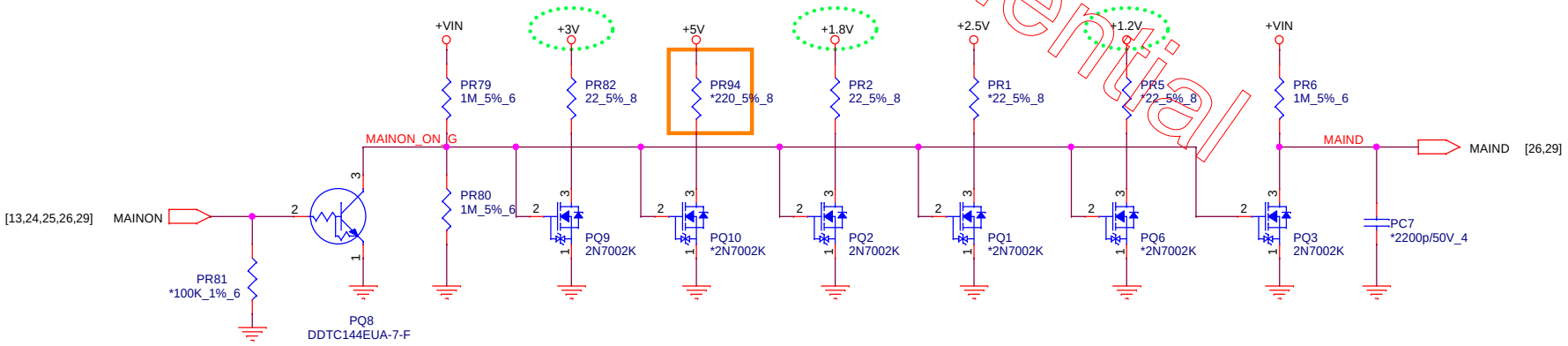
[24] VL
[14,23,24,25,26,27,28] +VIN
[4,5,12,13,14,16,17,18,19,20,21,22,24,25,26,27,28,29] +3V
[14,17,19,24] +5V
[3,4,14,17,20,22,29] +1.8V
[26] +2.5V

Thermal Protection

(1) Need fine tune for thermal protect point
(2) Note placement position TEMP=80C

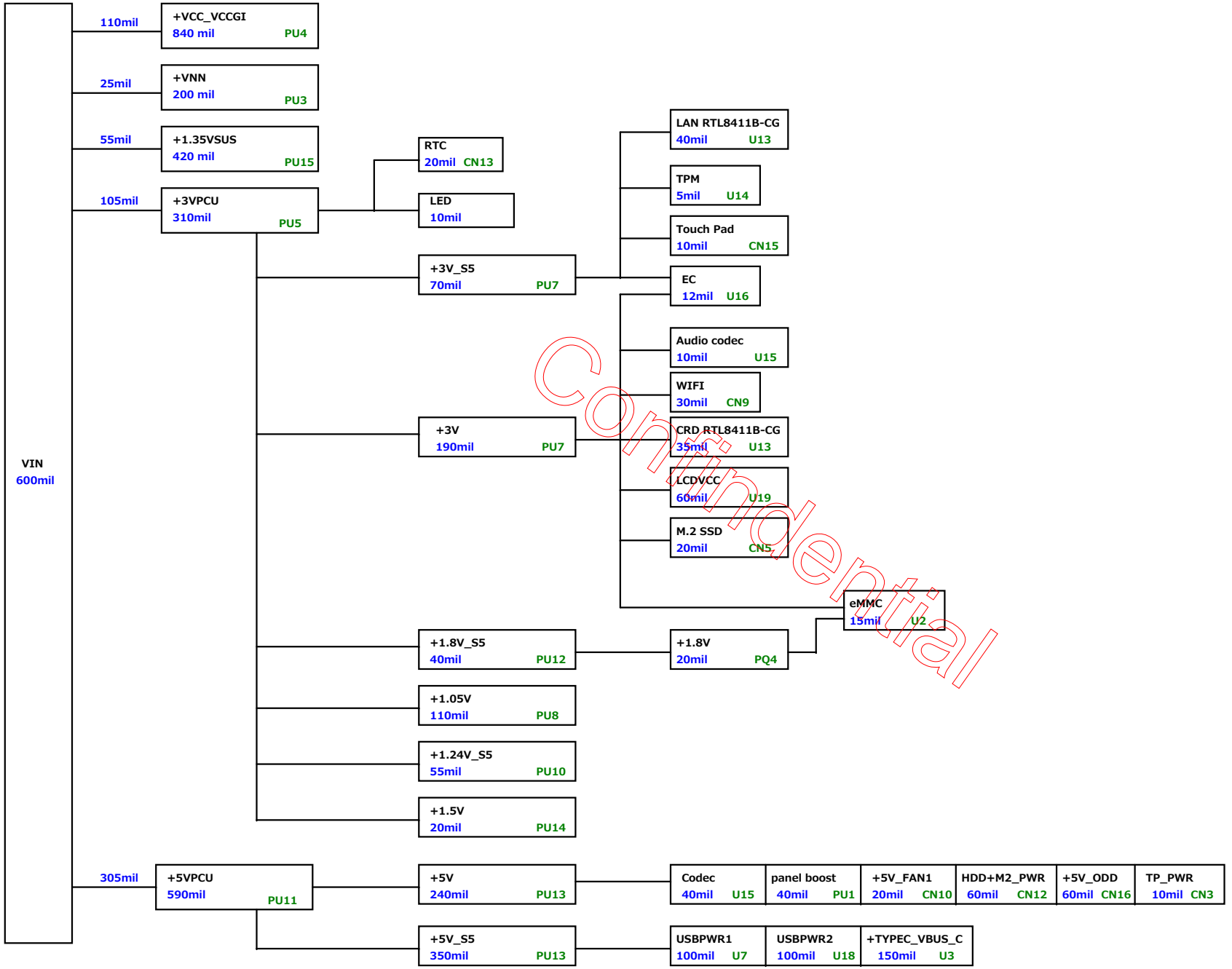


+5V PU High R= 220 ohm for Bo-Bo sound issue.

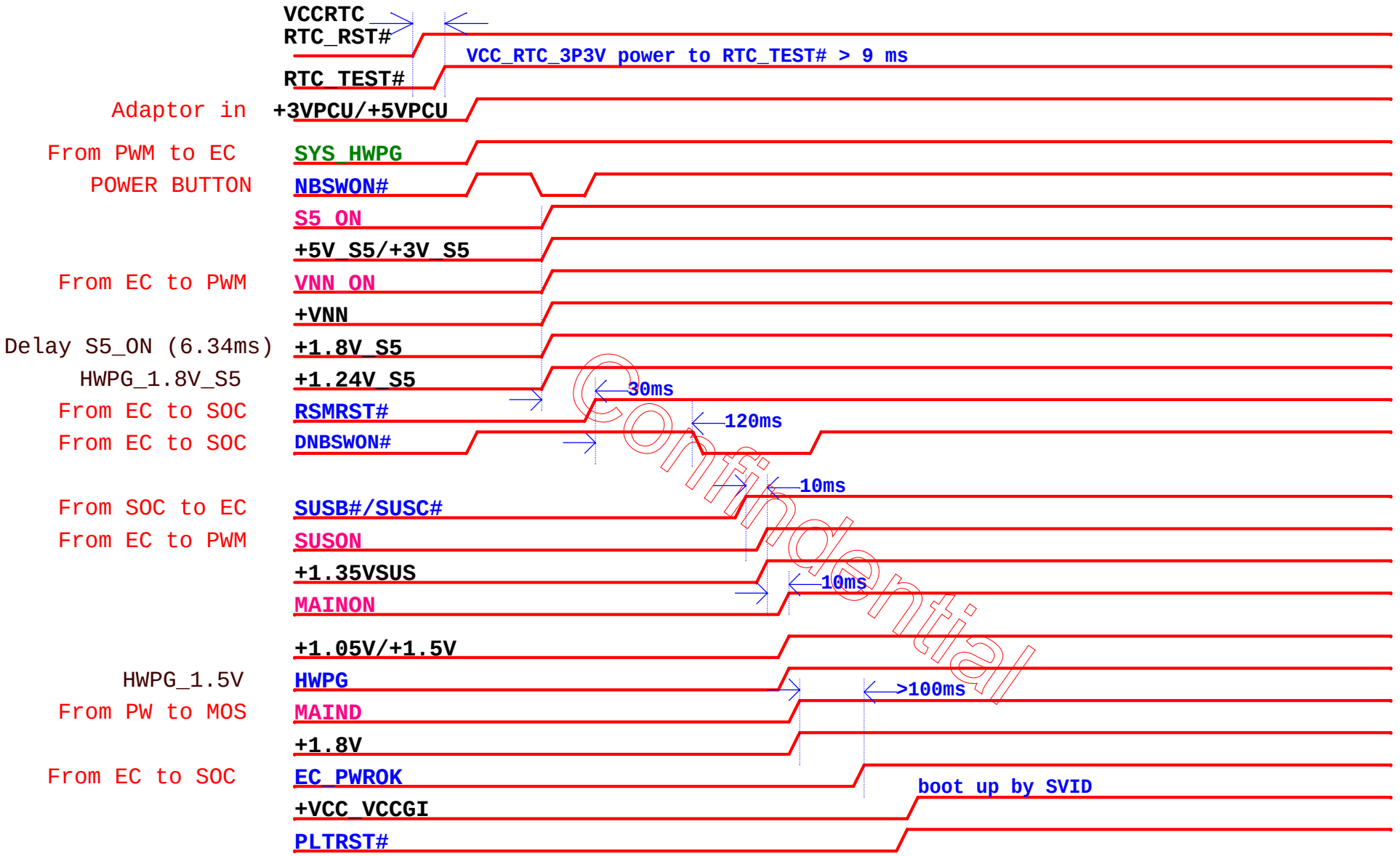


Quanta Computer Inc.		
PROJECT : ZHVA		
Size	Document Number: Thermal / Discharge	Rev: 1A
Date: Thursday, August 09, 2018	Sheet 30 of 34	

Gemini lake Power Tree



Quanta Computer Inc.
PROJECT : ZHVA
Size | Document Number | Rev 1A
POWER TREE
Date: Thursday, August 09, 2018 Sheet 31 of 34



Quanta Computer Inc.
PROJECT : ZHVA

Size	Document Number	Rev
	Power on Sequence	1A
Date: Thursday, August 09, 2018	Sheet 32 of 34	

Power plane	Description	S0	S3	S5
+VIN	Adaptor power supply	ON	ON	ON
+VCC_VCCGI	Variable voltage supply to CPU and Graphics Core and ISP logic	ON	OFF	OFF
+VNN	Variable voltage supply to other (non core) logic	ON	OFF	OFF
+1.05V	Fixed voltage rail for SRAM,I/O,internal Logic	ON	OFF	OFF
+1.24V_S5	Fixed voltage rail for SoC L2/ Audio & ISH I/O Logic and PLLs MPHY Logic/ USB2-I/O/MIPI I/Os	ON	ON	ON
+1.8V_S5	Fixed voltage rail for all GPIOs	ON	ON	ON
+1.35VSUS	Fixed voltage rail for DDR3L IO	ON	ON	OFF
+3V_RTC	Fixed Voltage rail for RTC (Real Time Clock)	ON	ON	ON
+1.8V	1.8V S0 power rail	ON	OFF	OFF
+1.5V	1.5V S0 power rail	ON	OFF	OFF
+5VPCU	5V always on power rail	ON	ON	ON
+5V_S5	5V S5 power rail	ON	ON	ON
+5V	5V S0 power rail	ON	OFF	OFF
+3VPCU	3V always on power rail	ON	ON	ON
+3V_S5	3V S5 power rail	ON	ON	ON
+3V	3V S0 power rail	ON	OFF	OFF