

Compal Confidential

FH5VF

MB Schematic Document

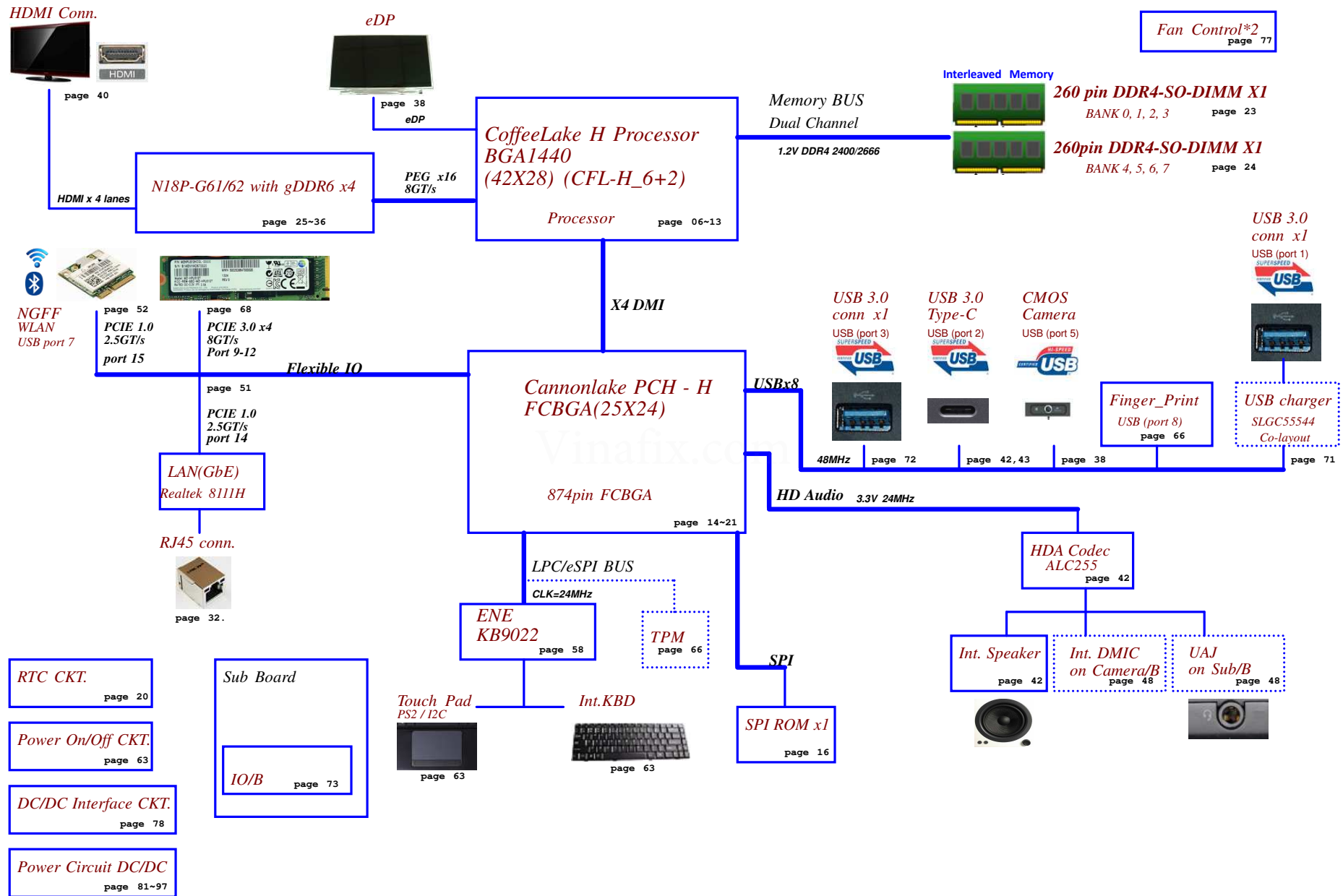
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LA-J861P

Rev:1A

2020.02.05

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Issued Date	2017/10/30	Deciphered Date	2018/10/30	Title	Cover Sheet
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Vcc		3.3V +/- 5%					
Ra		100K +/- 1%					
Board ID	Rb	V _{BI} D	min	V _{BI} D	typ	V _{BI} D	max
0	0			0.000 V		0.300 V	0x00 - 0x13
1	12K +/- 1%	0.347 V		0.345 V		0.360 V	0x14 - 0x1E
2	15K +/- 1%	0.423 V		0.430 V		0.438 V	0x1F - 0x25
3	20K +/- 1%	0.541 V		0.550 V		0.559 V	0x26 - 0x30
4	27K +/- 1%	0.691 V		0.702 V		0.713 V	0x31 - 0x3A
5	33K +/- 1%	0.807 V		0.819 V		0.831 V	0x3B - 0x45
6	43K +/- 1%	0.978 V		0.992 V		1.006 V	0x46 - 0x54
7	56K +/- 1%	1.169 V		1.185 V		1.200 V	0x55 - 0x64
8	75K +/- 1%	1.398 V		1.414 V		1.430 V	0x65 - 0x76
9	100K +/- 1%	1.634 V		1.650 V		1.667 V	0x77 - 0x87
10	130K +/- 1%	1.849 V		1.865 V		1.881 V	0x88 - 0x96
11	160K +/- 1%	2.015 V		2.031 V		2.046 V	0x97 - 0xA4
12	200K +/- 1%	2.185 V		2.200 V		2.215 V	0xA5 - 0xAF
13	240K +/- 1%	2.316 V		2.329 V		2.343 V	0xB0 - 0xB7
14	270K +/- 1%	2.395 V		2.408 V		2.421 V	0xB8 - 0xBF
15	330K +/- 1%	2.521 V		2.533 V		2.544 V	0xC0 - 0xC9
16	430K +/- 1%	2.667 V		2.677 V		2.687 V	0xCA - 0xD4
17	560K +/- 1%	2.791 V		2.800 V		2.808 V	0xD5 - 0xDD
18	750K +/- 1%	2.905 V		2.912 V		2.919 V	0xDE - 0xF0
19	NC	3.000 V		3.000 V			0xF1 - 0xFF

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)				
I2C_1 (+3VS)	TM-P3393-003 (Touch Pad)			
	SA577C-12A0 (Touch Pad)			
PCH_SMBCLK (+3VS)	DIMM1			
	DIMM2			
PCH_SML1CLK EC_SMB_CK2 (+3VS)	N18P-G0/N17P-G0-K1 (VGA)	0x9E		
	Thermal Sensor (NCT7718W)	1001_100xb	1001_1001b	1001_1000b
	PCH	0x90		
	Thermal Sensor (G781-1P8F)	1001_101xb	1001_1011b	1001_1010b
EC_SMB_CK1 (+3VLP)	BQ24781 (Charger IC)	0x12		
	BATTERY PACK	0x16		

[illegible]

Item	BOM Structure
Unpop	@
Connector	CONN@
CMC	CMC@
dGPU circuit	VGA@
N18P GPU	N18P@
VRAM	X76@
OVRM-ON	ON_X76@
OVRM-uPI	uPI_X76@
TPM	TPM@
For Acer IOAC	IOAC@
No Acer IOAC	NIOAC@
Thermal sensor	TMS@
for UART BT module	UBT@
for SW debug board	UART@
Intel CNVi	CNVi@
Finger Print	FP@
FinerPrint(with PBA)	PBA@
LAN LDO mode	LDO@
LAN Switch mode	SWR@
EMI requirement	EMI@
EMI require reserve	XEMI@
ESD requirement	ESD@
ESD require reserve	XESD@
FP ESD requirement	FPESD@
H62 CPU	H62@
H82 CPU	H82@

<i>SIGNAL</i>	<i>SLP_S3#</i>	<i>SLP_S4#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>S0 (Full ON)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>
<i>S3 (Suspend to RAM)</i>	<i>LOW</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>
<i>S4 (Suspend to Disk)</i>	<i>LOW</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>
<i>S5 (Soft OFF)</i>	<i>LOW</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>

Power Plane	Description	S0	S3	S4	S5
+RTCVCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V_VDDQ	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS_VCCSTG	+1.05VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_YTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.95VS power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+NVVDD1	Core voltage for VGA (merge core & core_s)	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

Board ID	PCB Revision	Board ID	PCB Revision
0	Rev0.1	10	
1		11	
2		12	
3		13	
4		14	
5		15	
6		16	
7		17	
8		18	A7 Rev1A
9		19	A7 Rev1.0

FH5VF_CFL_EVT Power Sequence

BIOS : 0.03

AC mode

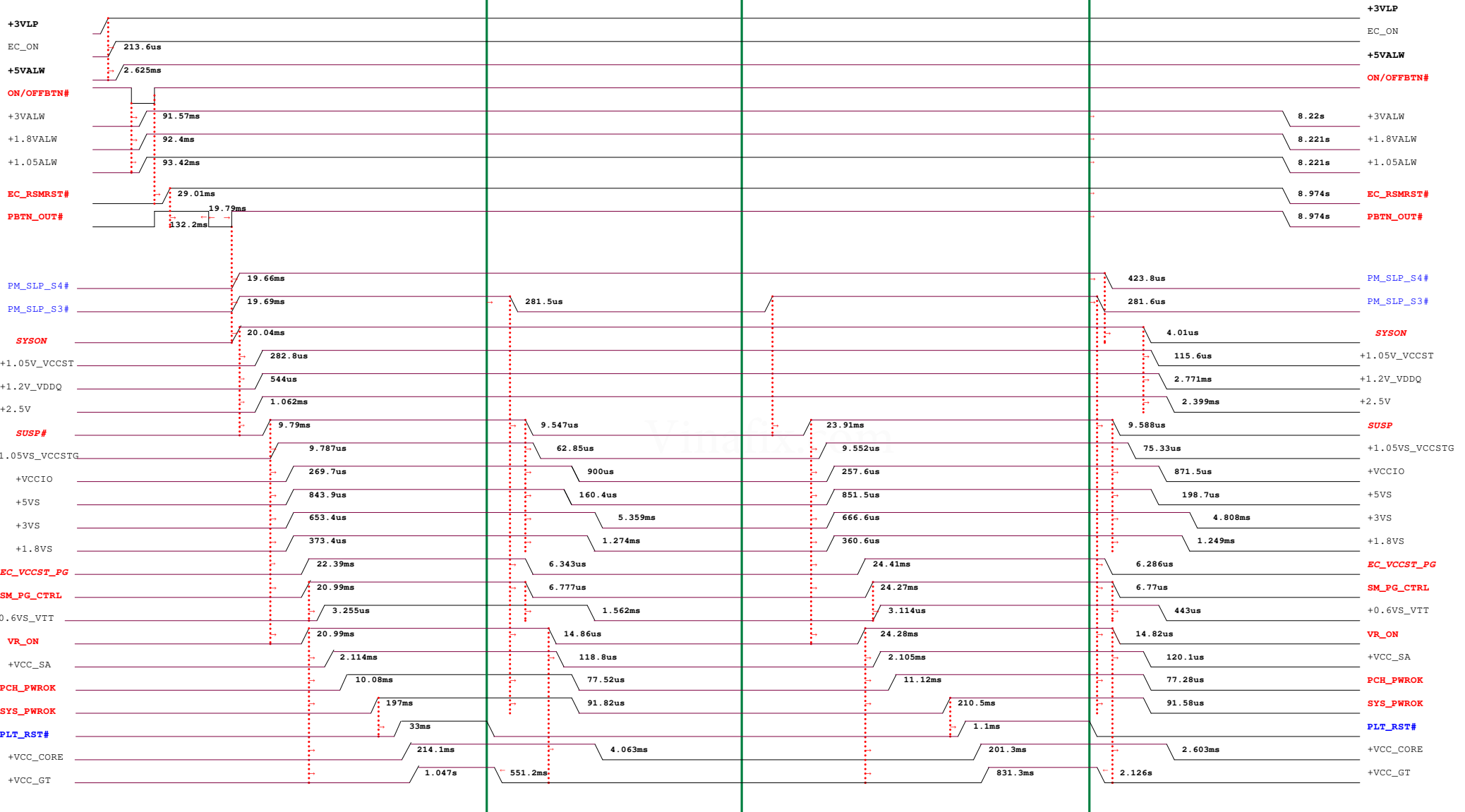
Power On

S3

S3 Resume

Power Off

Plug in



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PCB@
PCB FH5VF LA-J861P LS-J812P
DAZ2Y100200

Coffee Lake-H CPU SKU

UC1
I5@
S IC CL8068403373522 SR3Z0 U0 2.3G ABO !
SA0000BPJ40
UC1
I7@
S IC CL8068403359524 SR3YY U0 2.2G ABO !
SA0000BPZ40

Re-fresh U0 stepping

UC1
I5RU0@
S IC CL8068404121905 SRF6X U0 2.4G ABO !
SA0000COG40
UC1
I7RU0@
S IC CL8068404121817 SRF6U U0 2.6G ABO !
SA0000COF30

Re-fresh R0 stepping

UC1
I5RR0@
S IC CL8068404069606 SRF6R R0 2.4G ABO !
SA0000CSZ10
UC1
I7RR0@
S IC CL8068404069418 SRF6P R0 2.6G ABO !
SA0000CSU10

Comet Lake-H CPU SKU

UC1
QU9W@
S IC CL8070104399510 QU9W R1 2.5G FCBGA
SA0000DCP10
UC1
SRH84@
S IC CL8070104399510 SRH84 R1 2.5G ABO !
SA0000DCP40
UC1
QU9U@
S IC CL8070104399315 QU9U R1 2.6G FCBGA
SA0000DCN10
UC1
SRH8Q@
S IC CL8070104399315 SRH8Q R1 2.6G ABO !
SA0000DCN40

Cannon Lake PCH SKU

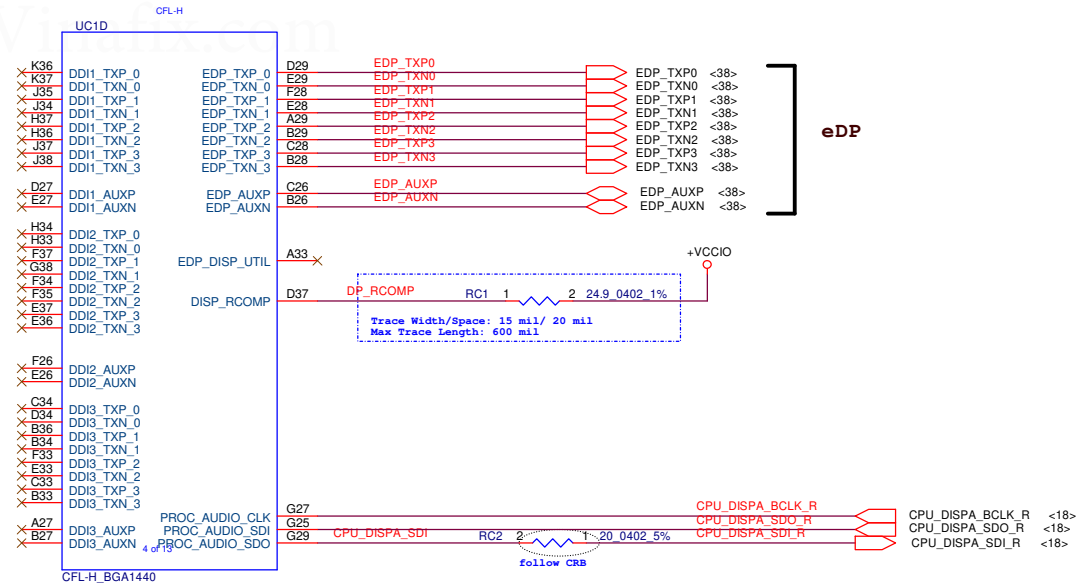
UH1
CFLPCH@
S IC FH82HM370 SR40B B0 BGA 874P PCH-H ABO !
SA0000BVP10

Comet Lake PCH SKU

UH1
CMLPCHQS@
S IC FH82HM470 QUCJ A0 FCBGA 874P PCH-H
SA0000DDP10
UH1
CMLPCH@
S IC FH82HM470 SRJAU A0 FCBGA PCH-H ABO !
SA0000DDP80

NV GPU SKU

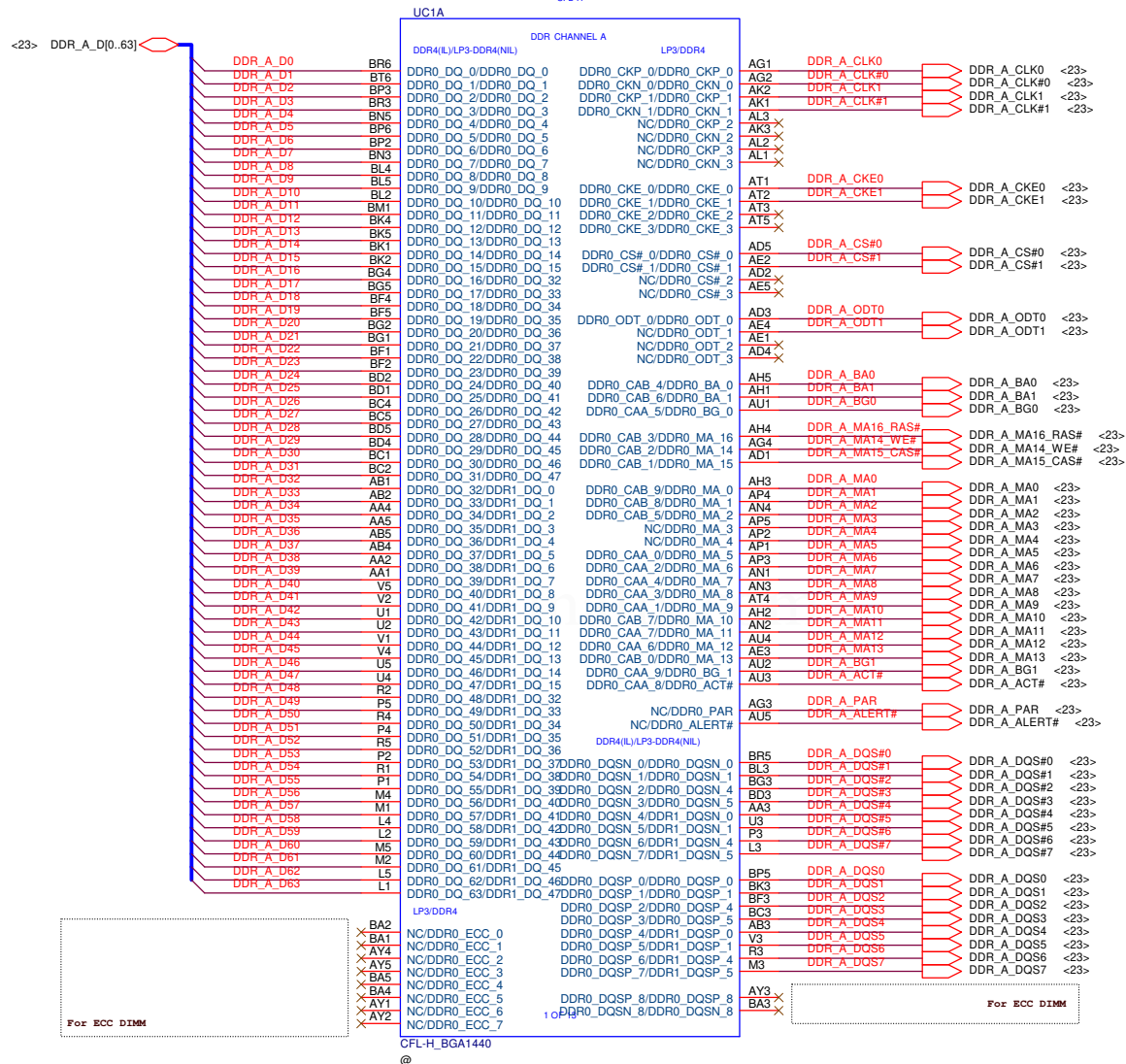
UV1
N18PG61QS@
S IC N18P-G61-A1 QS BGA 960P GPU ABO !
SA0000CZO10
UV1
N18PG61@
S IC N18P-G61-MP-A1 BGA 960P GPU ABO !
SA0000CZO30
UV1
N18PG61MP2@
S IC N18P-G61-MP2-A1 BGA 960P GPU ABO !
SA0000CZO50
UV1
N18PG62QS@
S IC N18P-G62-A1 QS BGA 960P GPU ABO !
SA0000CZP10
UV1
N18PG62@
S IC N18P-G62-A1 BGA 960P GPU ABO !
SA0000CZP30



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						Size		Document Number		Rev 1A	
						FH5VF M/B LA-J861P					
						Custom					
						Date:		Wednesday, February 05, 2020			

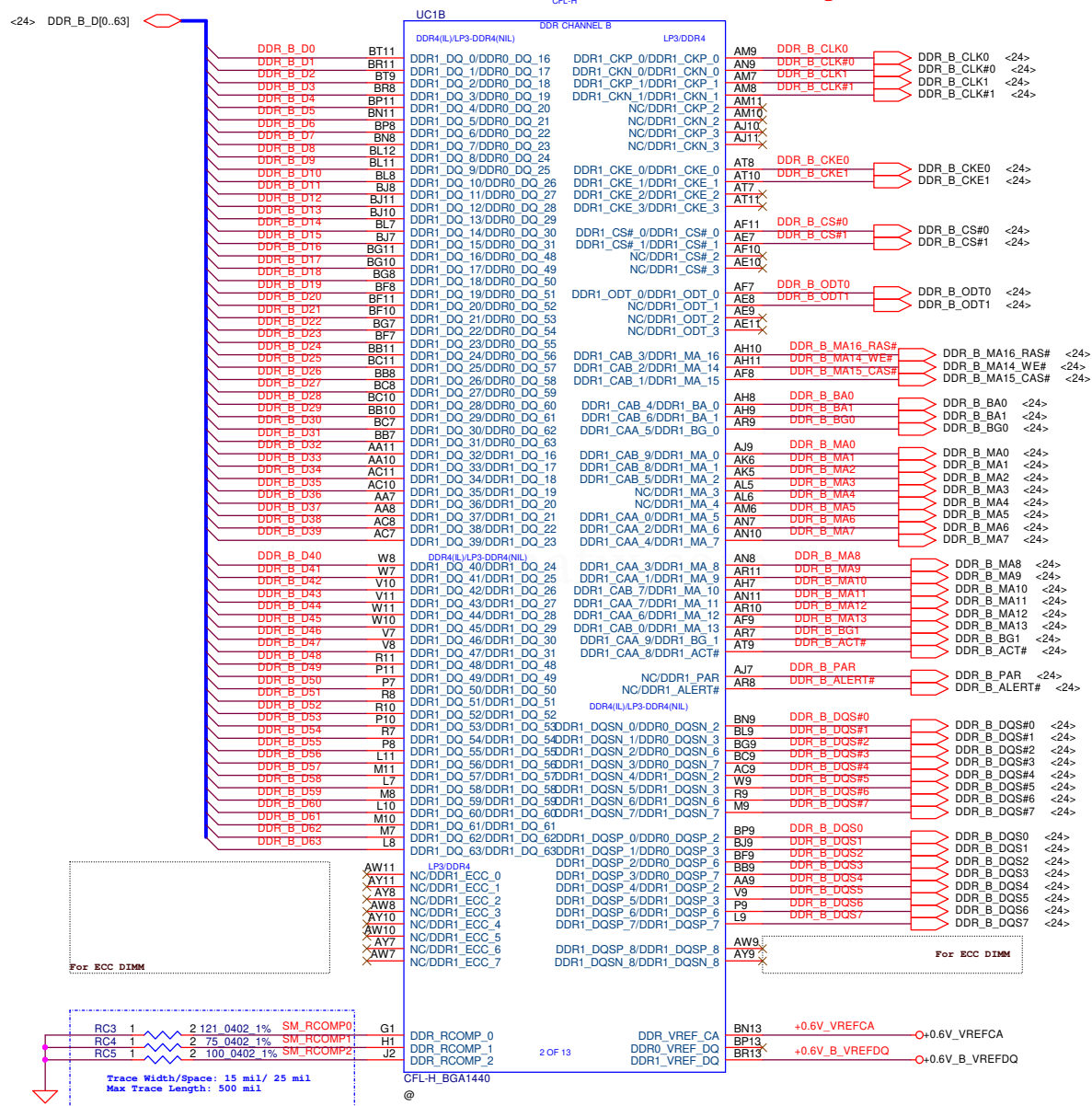
CHANNEL-A

Interleaved Memory



CHANNEL-B

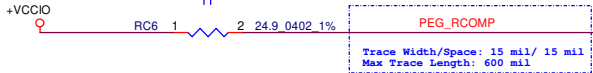
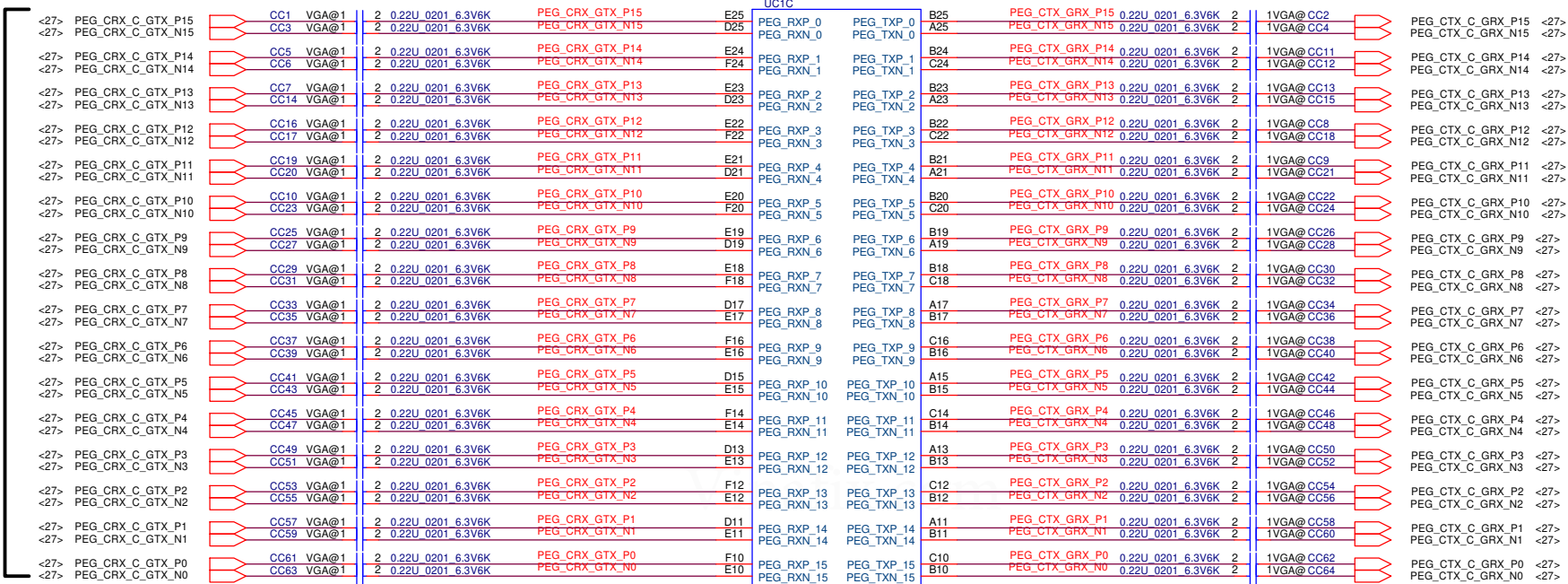
Interleaved Memory



PEG&DMI

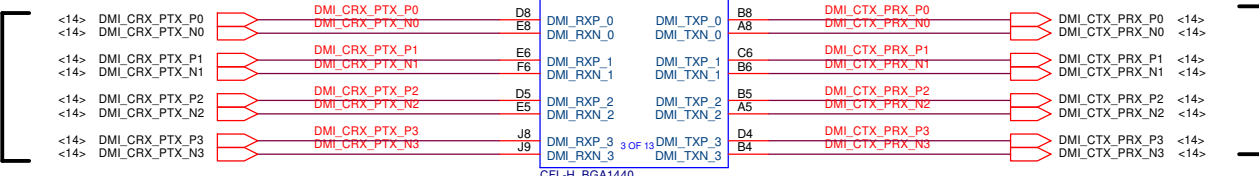
To DGPU
PEG Lane Reversed

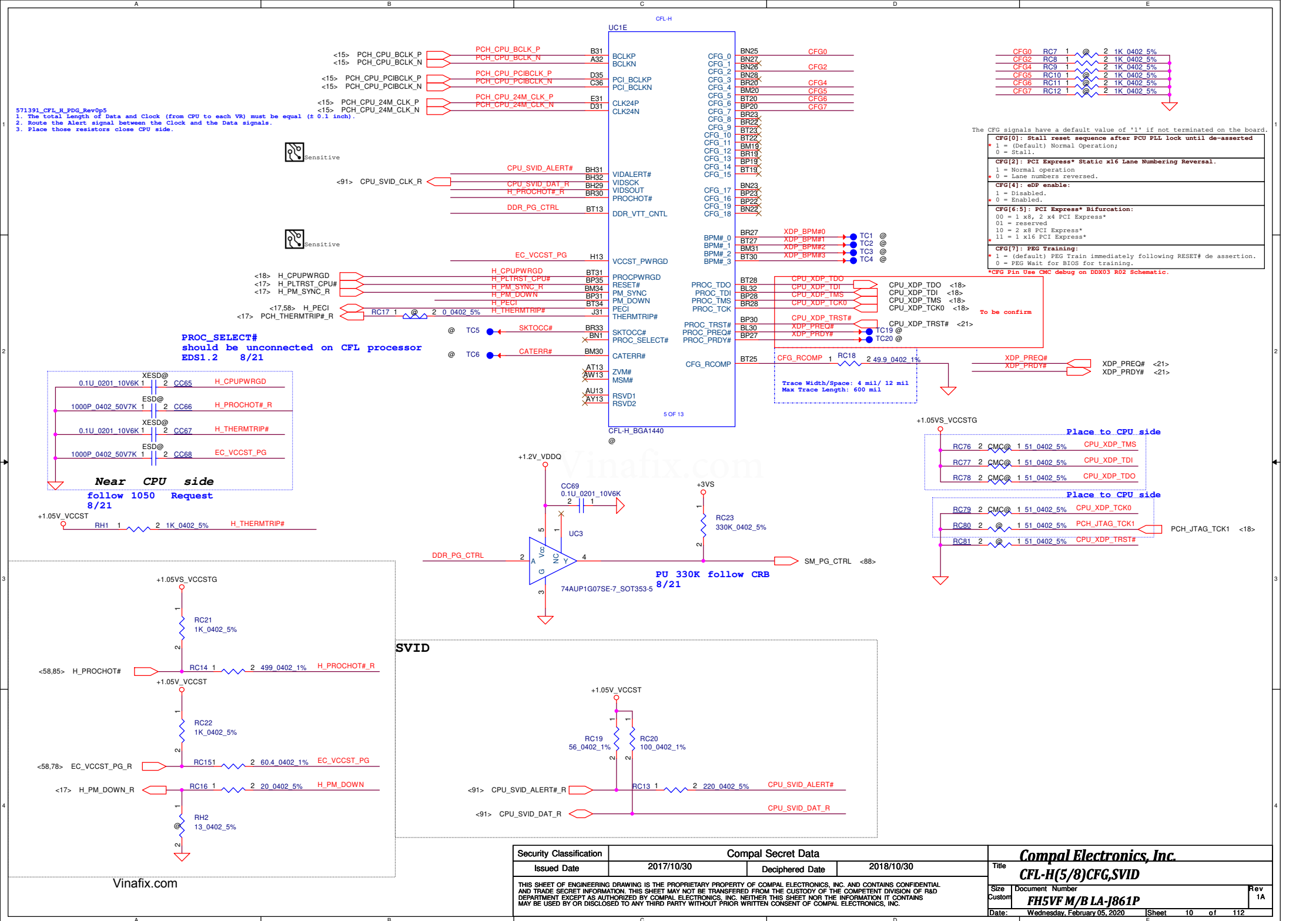
To DGPU
PEG Lane Reversed



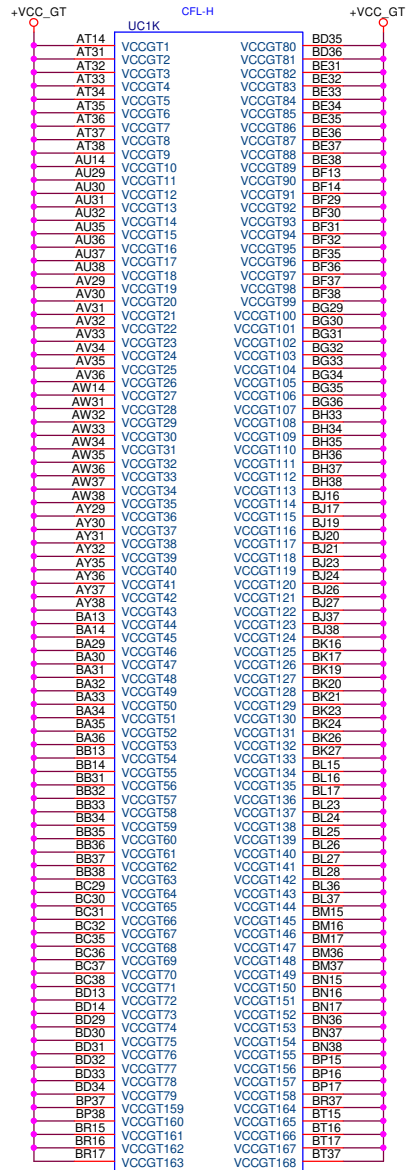
To PCH

To PCH



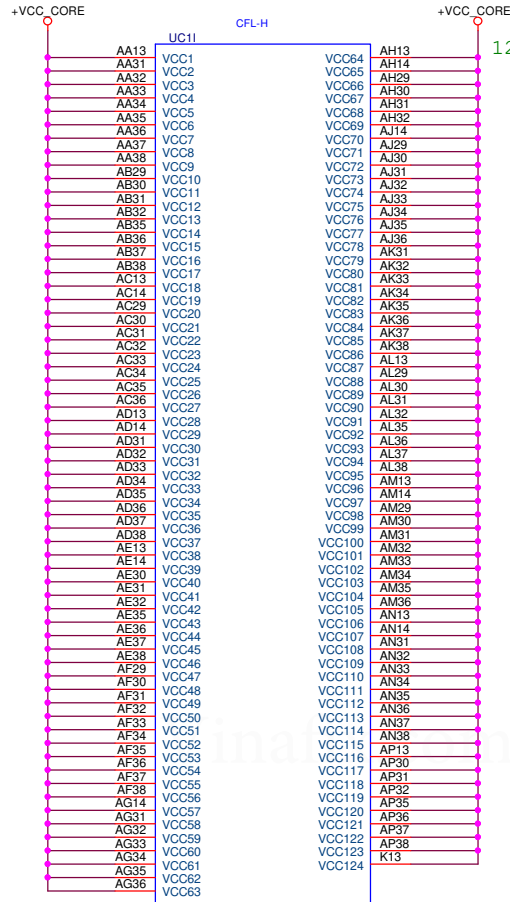


GT
32000mA (Hexa Core GT2)



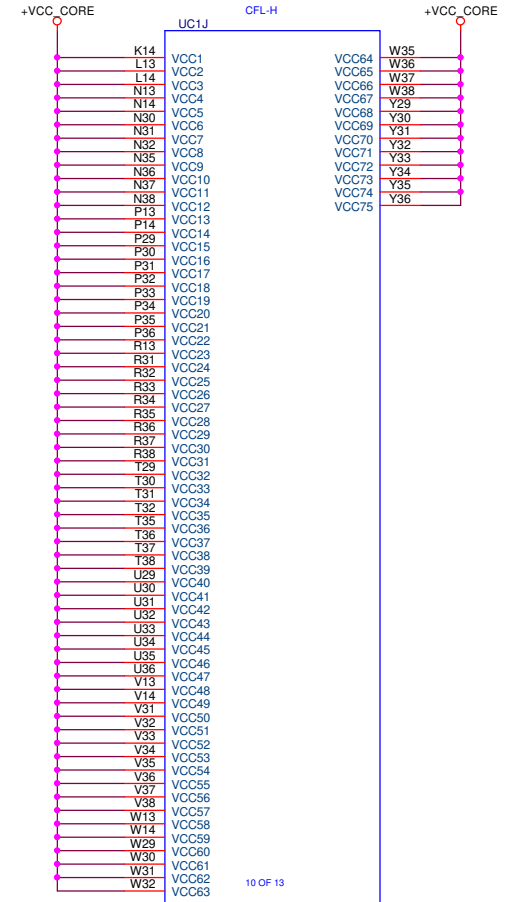
CFL-H_BGA1440
@

1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.



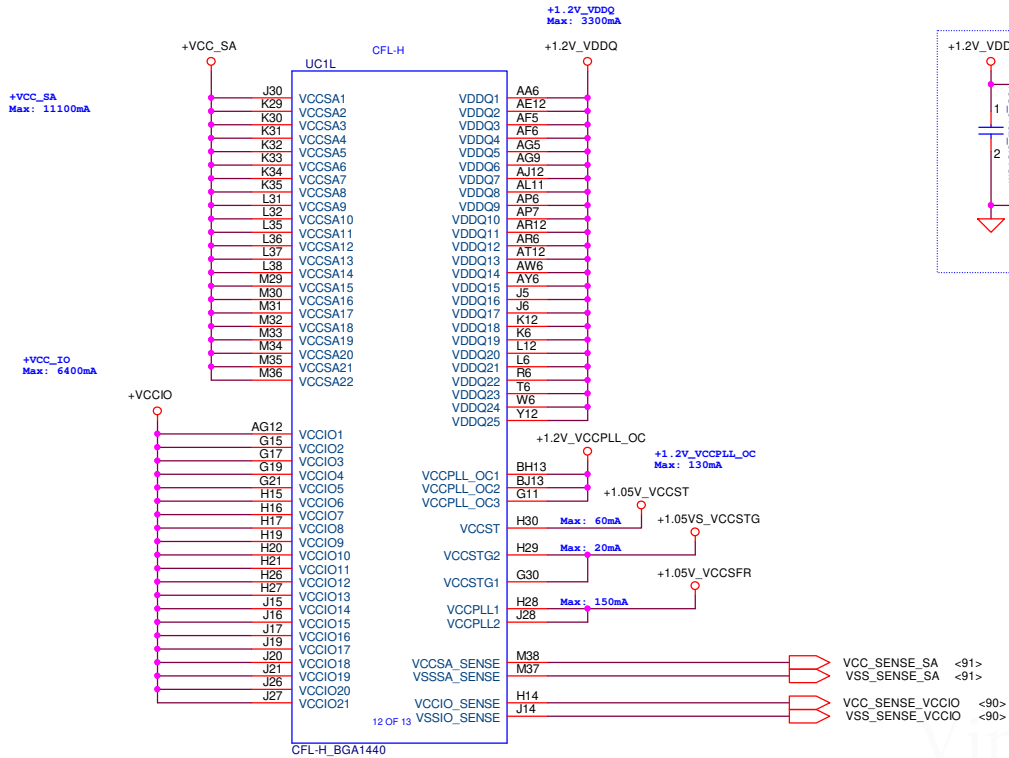
CFL-H_BGA1440
@

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2. Maintain 25-mil separation distance away from any other dynamic signals.

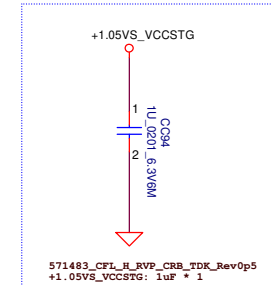
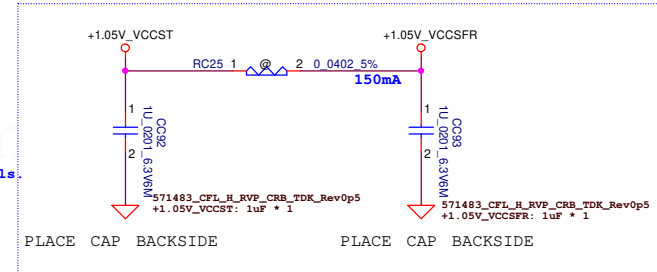
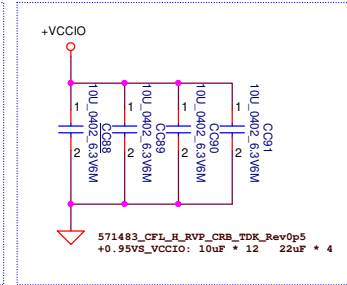
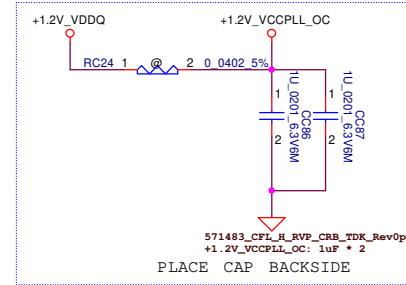
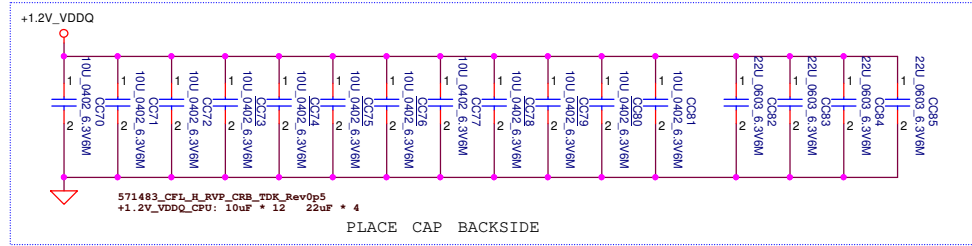


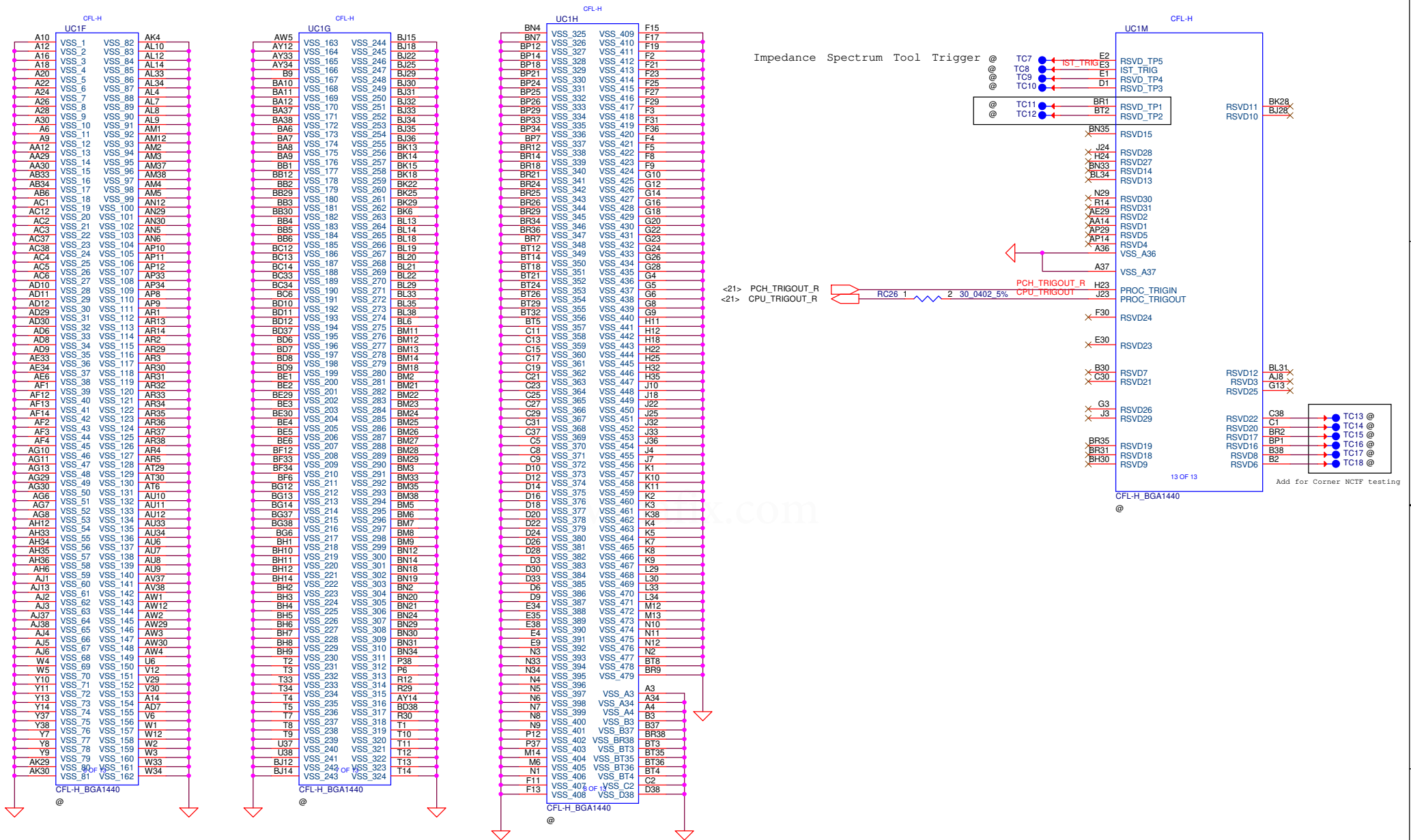
CFL-H_BGA1440
@

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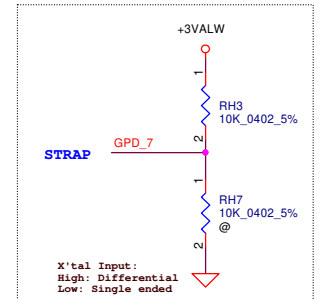
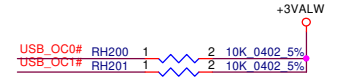
1. VccGT_SENSE / VssGT_SENSE Trace Length Match < 25 mils
2. Maintain 25-mil separation distance away from any other dynamic signals.



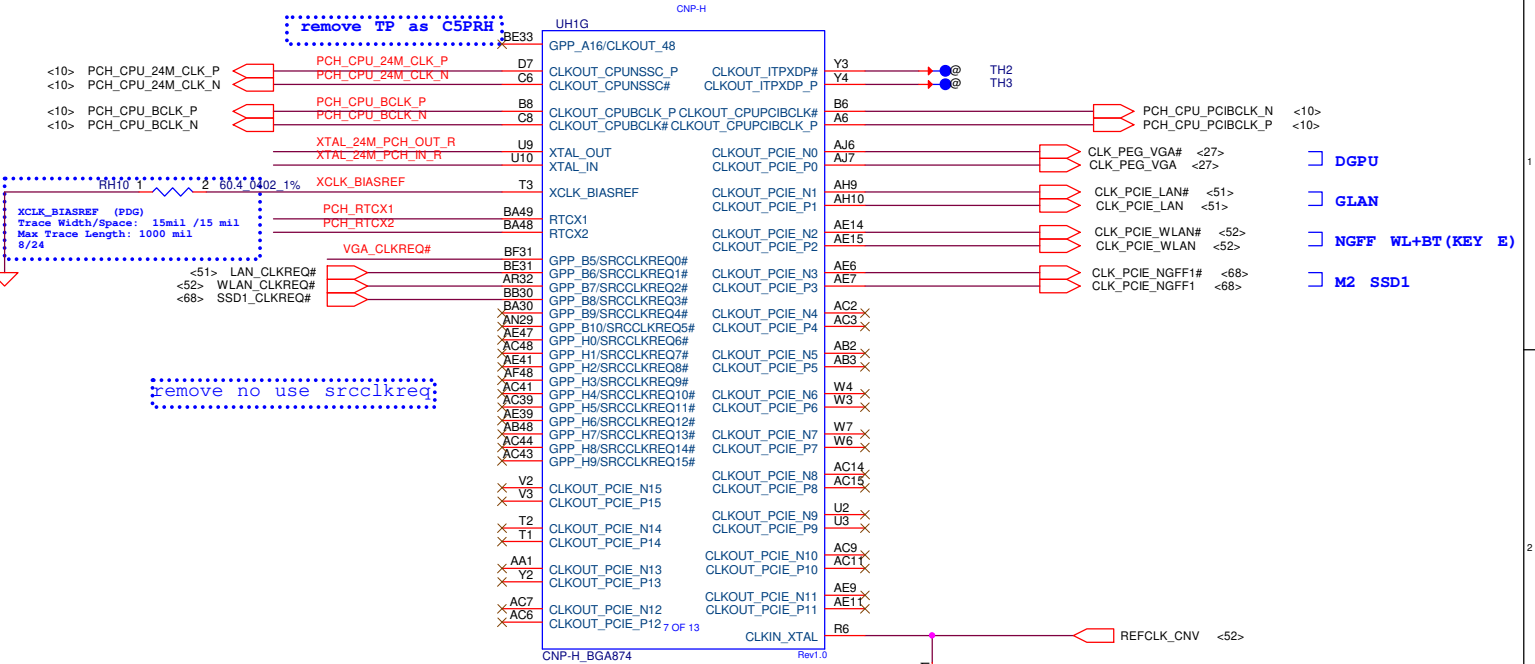
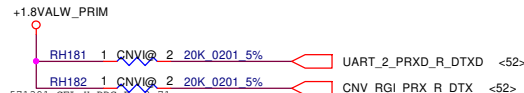
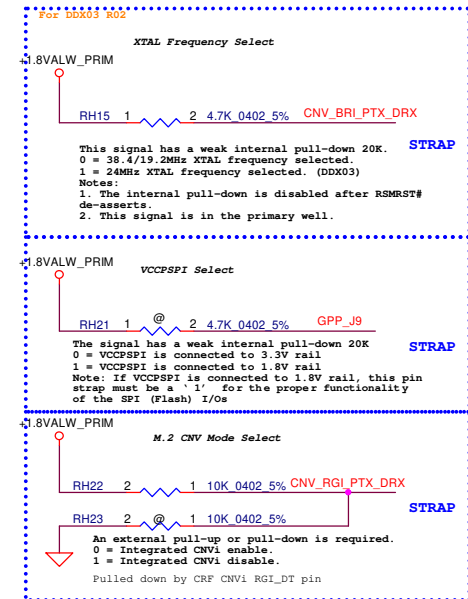
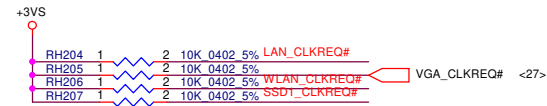
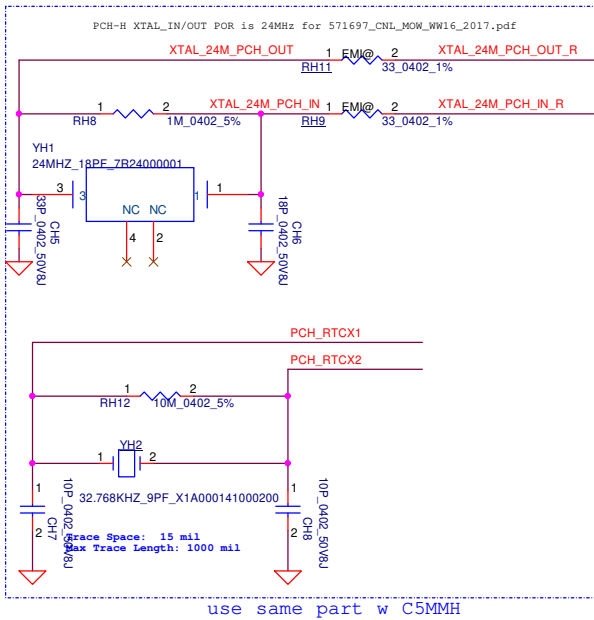


The 30 HSIO lanes on PCH-H supports the following configurations:

- Up to 24 PCIe* Lanes
 - A maximum of 16 PCIe* Ports (or devices) can be enabled
 - When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off the following:
 - Max PCIe* Ports (or devices) = 16 - GbE (0 or 1)
 - PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
- Up to 6 SATA Lanes
 - A maximum of 6 SATA Ports (or devices) can be enabled
 - SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
 - SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
- Up to 10 USB 3.1 Lanes
 - A maximum of 10 USB 3.1 Ports (or devices) can be enabled
- Up to 4 GbE Lanes
 - A maximum of 1 GbE Port (or device) can be enabled
- Supports up to 3 Remapped (Intel® Rapid Storage Technology) PCIe* storage devices
 - x2 and x4 PCIe* NVMe SSD
 - x2 Intel® Optane™ Memory Device
 - See the "PCI Express* (PCIe*)" chapter for the PCH PCIe* Controllers, configurations, and lanes that can be used for Intel® Rapid Storage Technology PCIe* storage support
- For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe Combo Port Soft Straps discussed in the SPI Programming Guide and through the Intel® Flash Image Tool (FIT) tool.



Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29										
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	PCIe* #1	PCIe* #2	USB3.1 #8	PCIe* #3	USB3.1 #9	PCIe* #4	USB3.1 #10	PCIe* #5	GfE	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	SATA 1a	SATA 1b	GfE	PCIe* #13	SATA 2	SATA 3	SATA 4	SATA 5	PCIe* #16	PCIe* #17	PCIe* #18	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
Intel® RST Support										No Support					No Support		Yes			No Support				Yes					Yes											



571391_CFL_R_PDS_Rev0p71
To avoid floating input at the I/O pin BRI_RSP and RGI_RSP it is recommended to add a weak pull up resistor to the SoC pin with a recommended value of 20K ohm.

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can remove if no use DP
08/18

remove PCH_DP_SCLK/SDATA:

DDP[B..F]CTRLDATA
This signal has a weak internal Pull-down.
0 = Port B-D is not detected.
1 = Port B,C,D is detected. (Default)
Notes:
1. The internal Pull-down is disabled after
PCH_PWRON de-asserts
2. This signal is in the primary well.

no follow naming

<27,40> HDMI_HPD_PCH

<38> EDP_HPD

<51,58> EC_PME#

1 RH24 2 EC_PME#_R 0.0402 5%

CRB connect GND

RH1861 2 0.0402 5%

TH6 2 0.0402 5%

RH258 1 NTRM 2 0.0402 5%

RH259 1 NTRM 2 0.0402 5%

RH260 1 NTRM 2 0.0402 5%

RH27 2 1 1K 0.0402 5%

RH29 2 1 100K 0.0402 5%

RH31 1 2 4.7K 0.0402 5%

RH33 0.0402 5%

RH35 0.0402 5%

RH37 0.0402 5%

RH39 0.0402 5%

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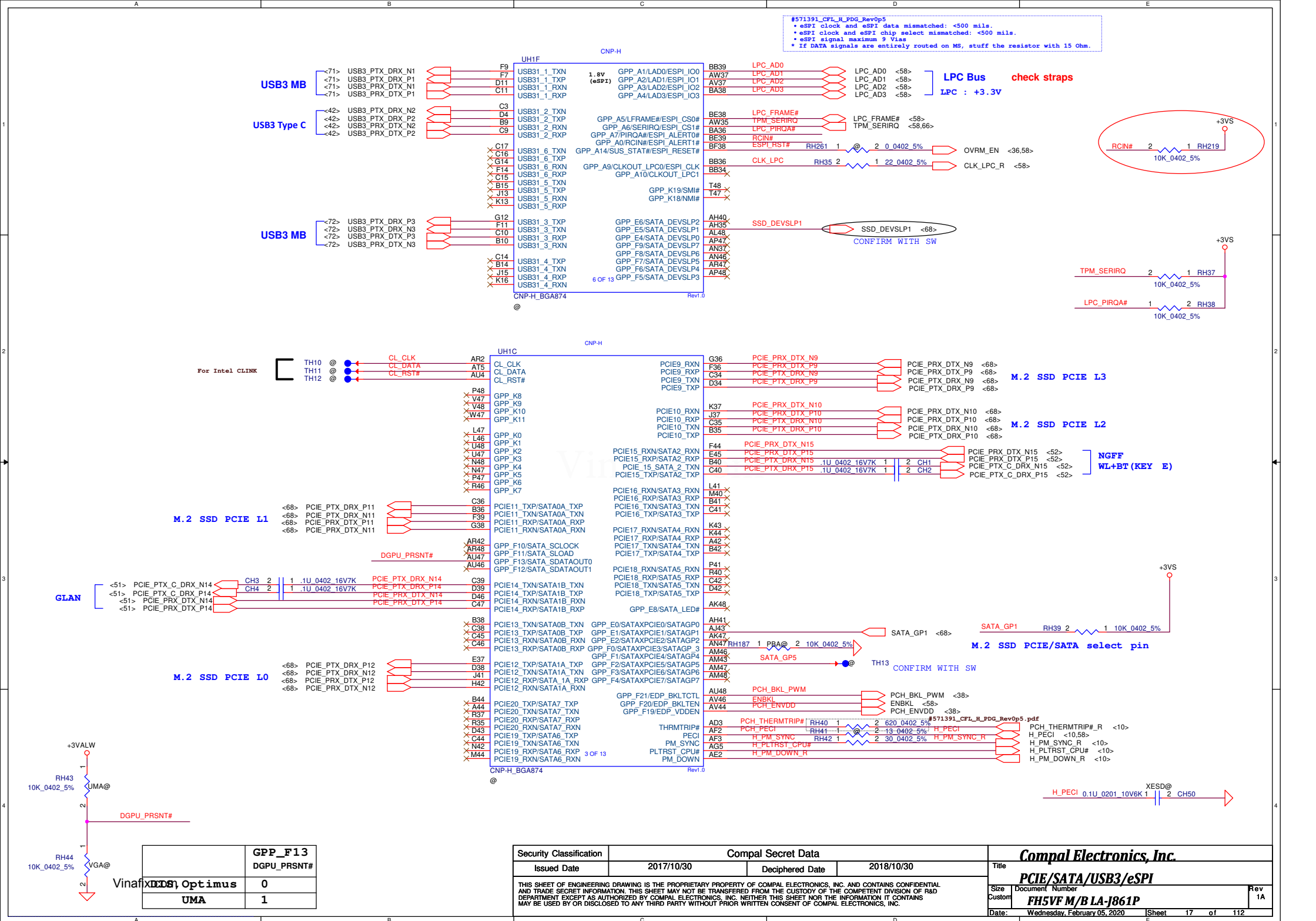
RH507 0.0402 5%

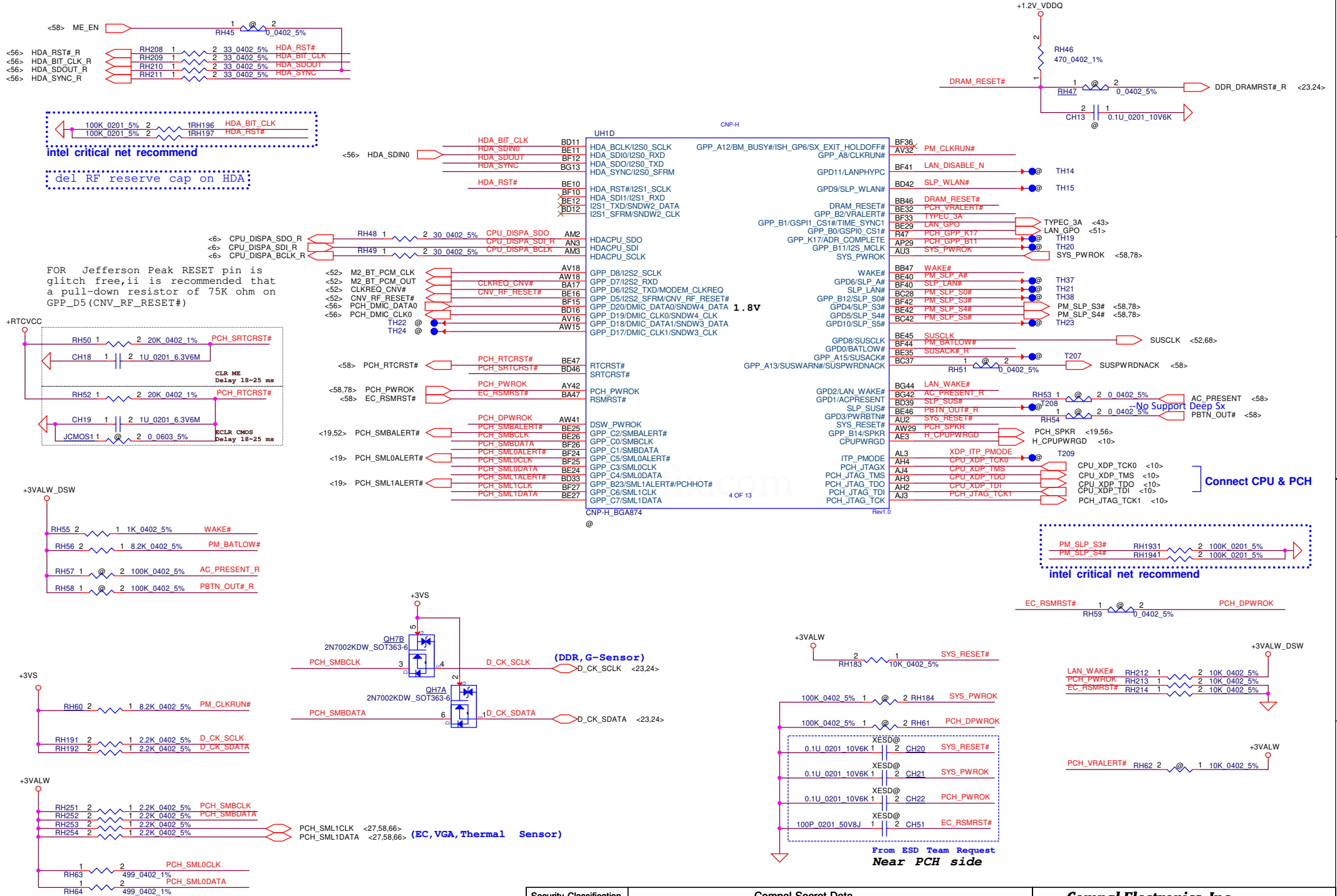
RH509 0.0402 5%

RH511 0.0402 5%

RH513 0.0402 5%

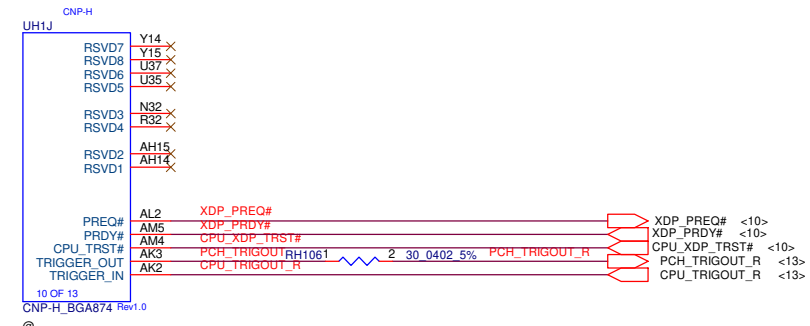
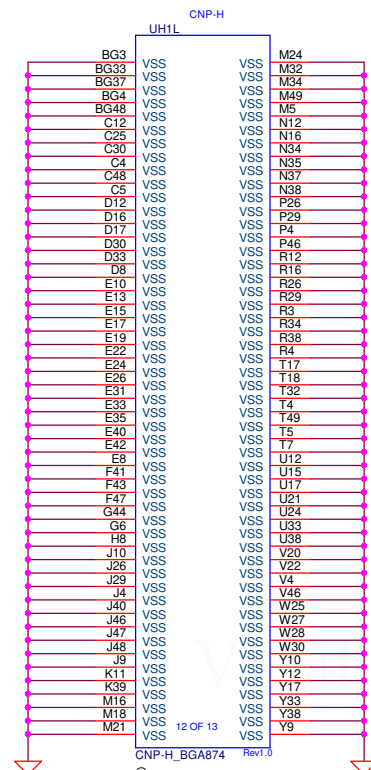
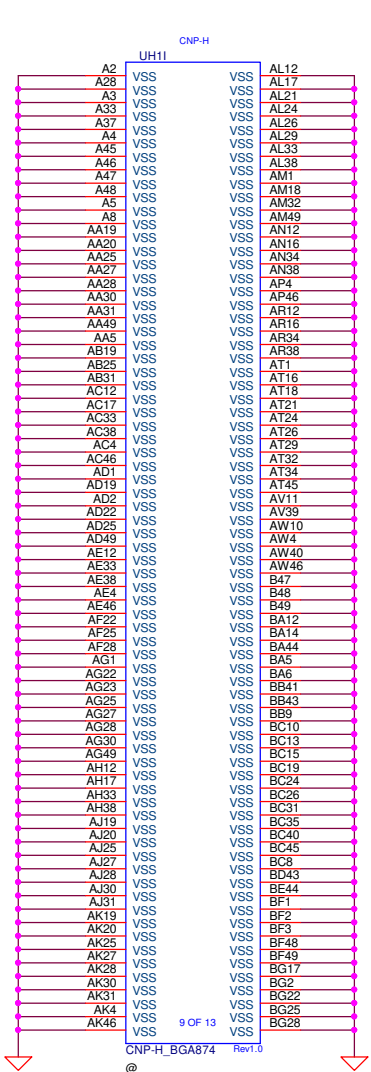
RH5





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Size	Document Number	Rev		1A	
Custom	FHSVF M/B LA-J861P				
Date:	Wednesday, February 05, 2020	Sheet	18	of	112



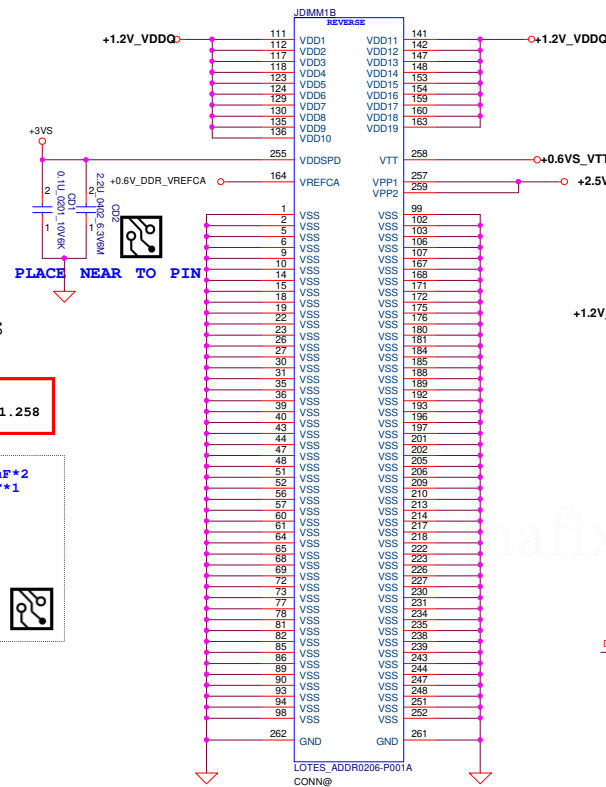
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				Date: Wednesday, February 05, 2020	Sheet 22 of 112

BOT REVERSE TYPE (4 mm)

Interleaved Memory

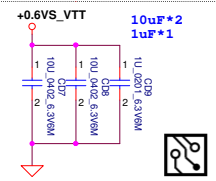
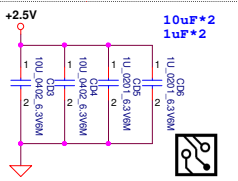
TOP: JDIMM1 CONN Non-ECC DIMM



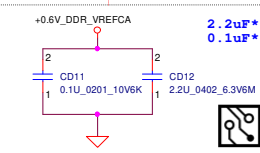
```
SPD ADDRESS FOR CHANNEL A :
WRITE ADDRESS: 0XA0
READ ADDRESS: 0XA1
SA0 = 0; SA1 = 0; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S
```

Layout Note:
Place near JDIMM1.257,259

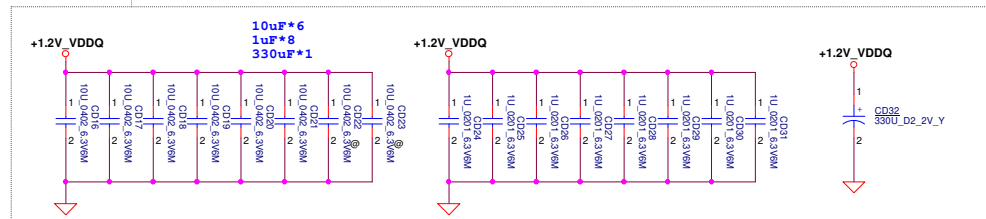
Layout Note:
Place near JDIMM1.258



Layout Note:
PLACE THE CAP near JDIMM1. 164

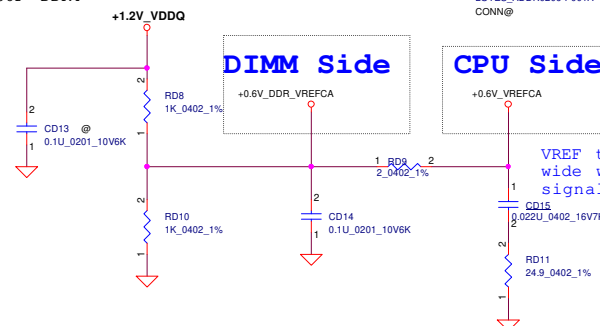


Layout Note:
Place near JDIMM1



For ECC DIMM

PLACE NEAR TO SODIMM



VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

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CHANNEL-B

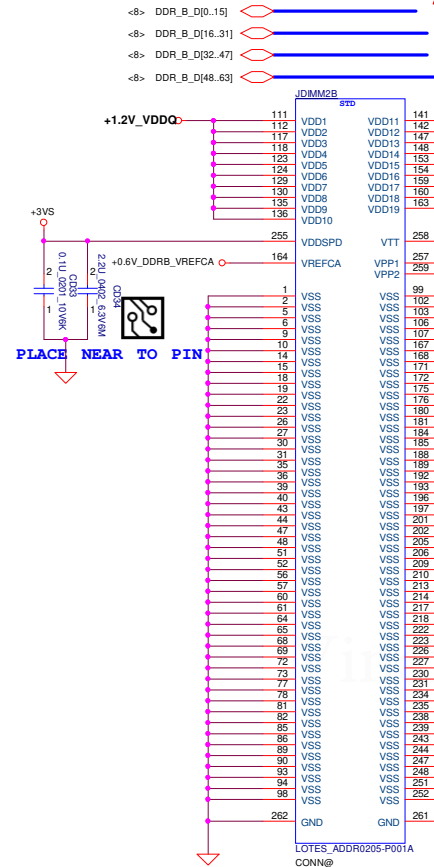
Interleaved Memory

BOT

STD (4 mm)

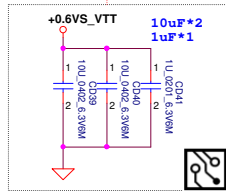
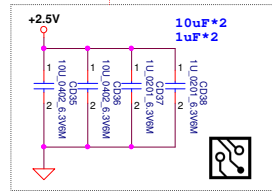
TOP: JDIMM2 CONN Non-ECC DIMM

SPD ADDRESS FOR CHANNEL B :
WRITE ADDRESS: 0XA4
READ ADDRESS: 0XA3
SA0 = 0; SA1 = 1; SA2 = 0.
DDR4 POR OPERATING SPEED: 1867 MT/S
STRETCH GOAL IS 2133 MT/S

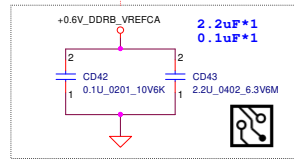


Layout Note:
Place near JDIMM3.257,259

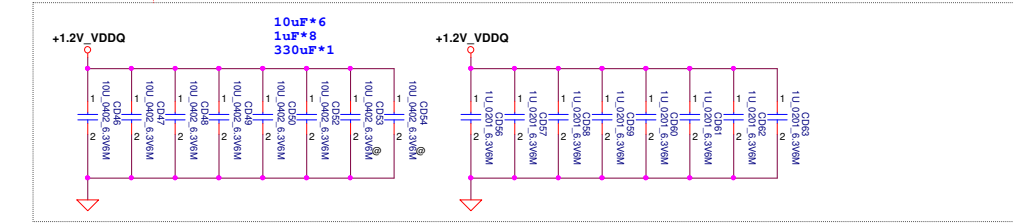
Layout Note:
Place near JDIMM3.258



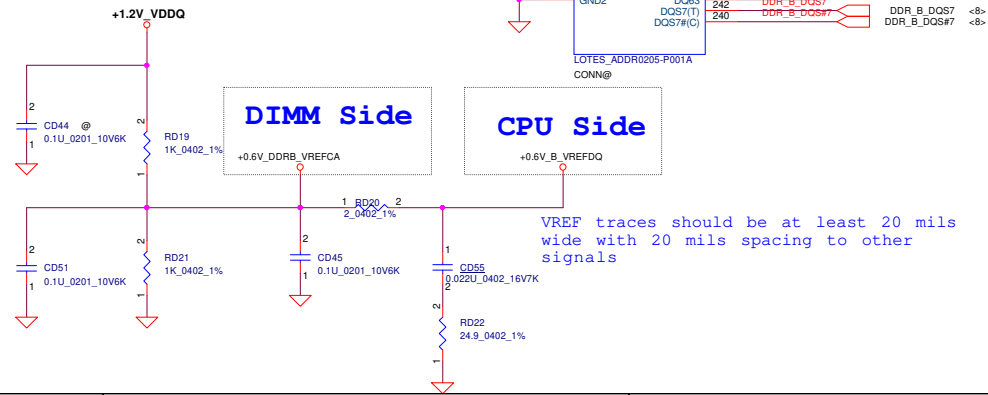
Layout Note:
PLACE THE CAP WITHIN 200 MILS
FROM THE JDIMM3



Layout Note:
Place near JDIMM3



Part Number: SP07001HW00
Part Value: S SOCKET LOTES ADDR0205-P001A DDR4 STD

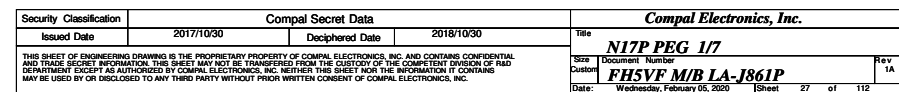


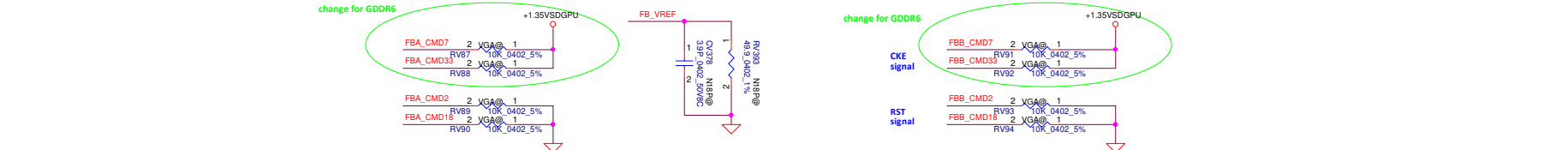
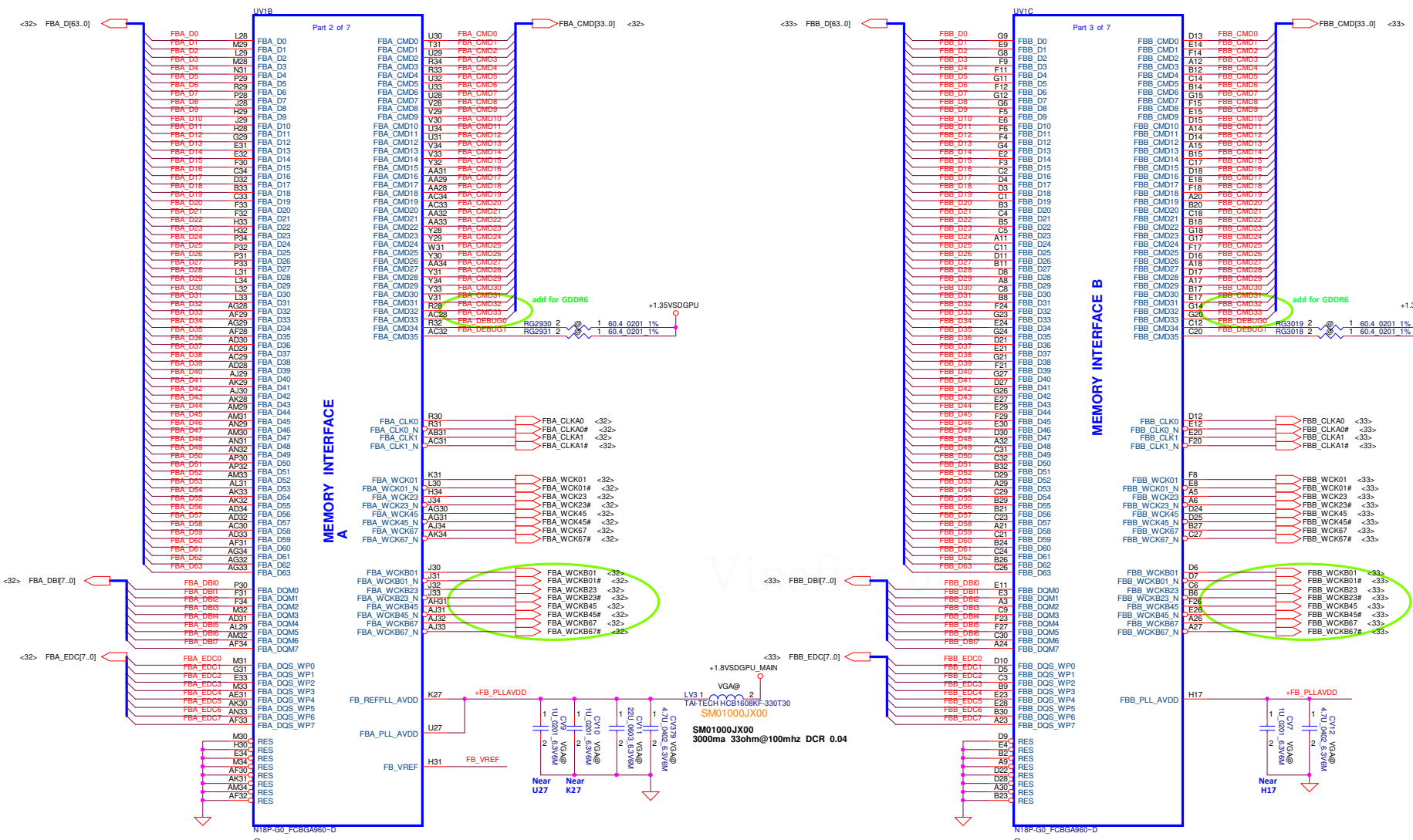
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HDMI
2.0

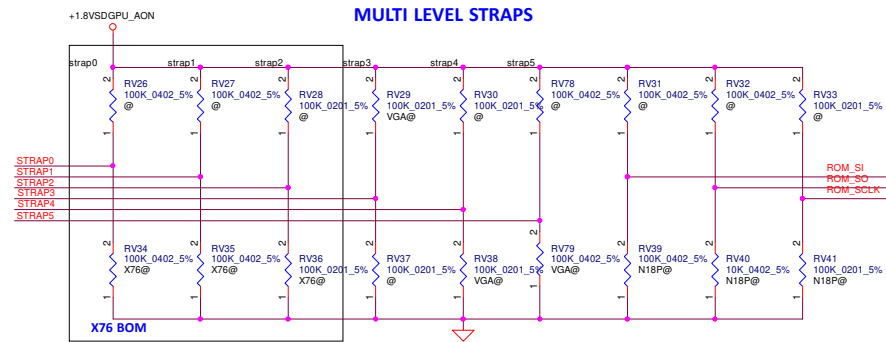
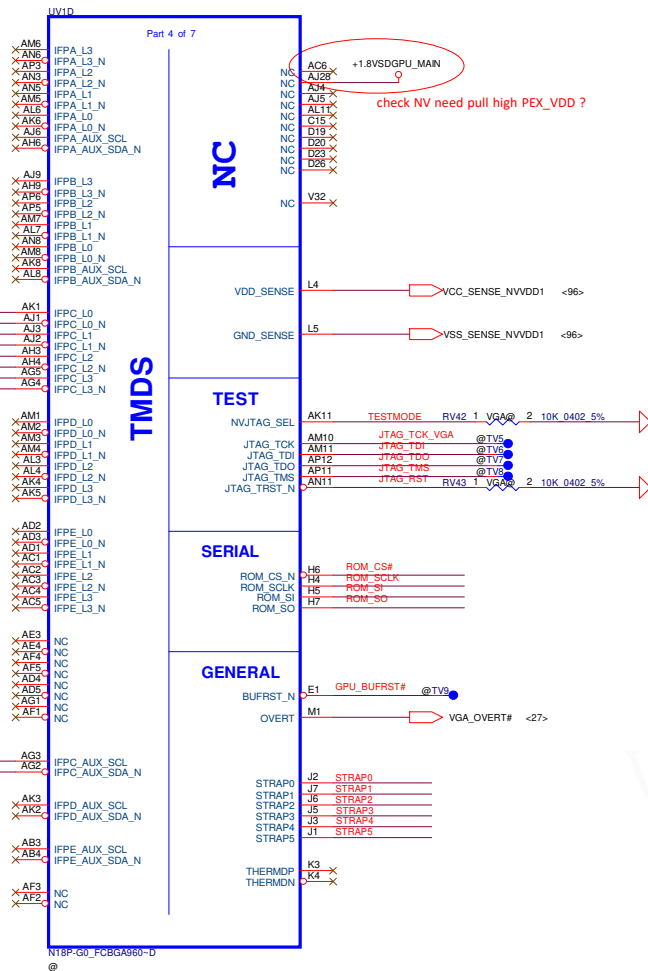


Table 12.4 FS_OVERT* Strap Enablement

Strap Pins	FS_OVERT* Strap Enablement	FS_OVERT* Function
ROM_SO	ROM_SI	ROM_SCLK
L	L	L
L	L	H
L	L	L
L	L	L

FS_OVERT* Function ENABLED
FS_OVERT* Function DISABLED
(do not configure)
(do not configure)
(do not configure)

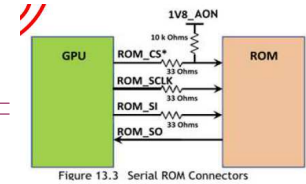
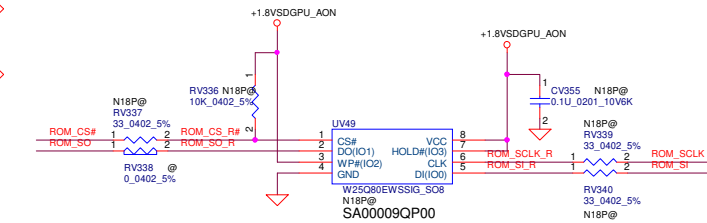


Table 8. N18P-G62/G61 GDDR6 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V and 1.25V ²	Micron	MT61K256M32JE-14:A	A-die	0x1	14 Gbps	1940 ³	Full	Production candidate
			Samsung	K4Z80325BC-HC14	C-die	0x0	14 Gbps	2001 ⁴	Full	Production candidate

Notes:

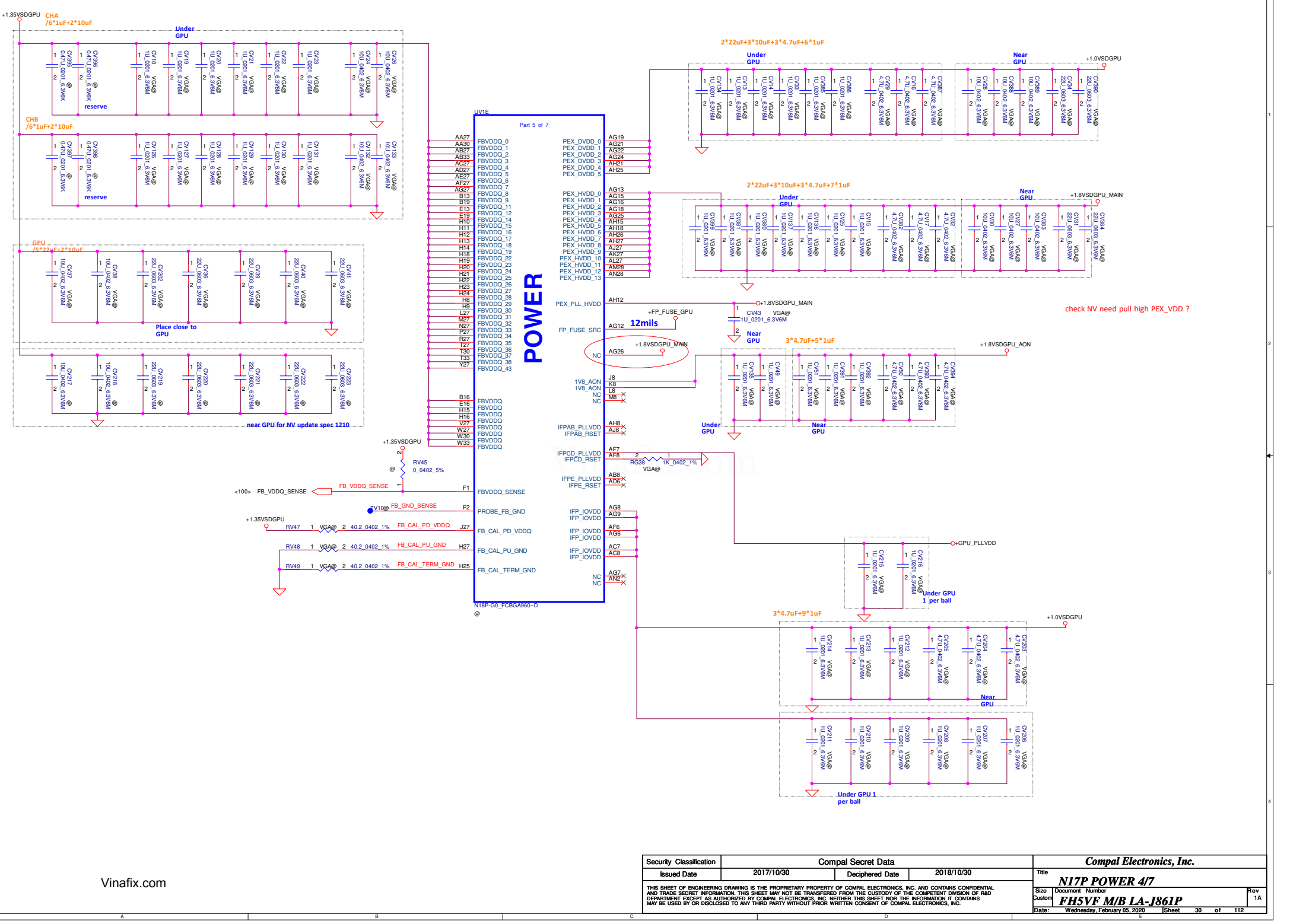
- For N18P-G62/G61, the maximum allowable memory case temperature is 95 °C.
- DVS is required to run WCLK > 5500 MHz.
- Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
- Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "SPL" letters inserted before the seven digits in its lot ID.

Table 12.3 RAMCFG

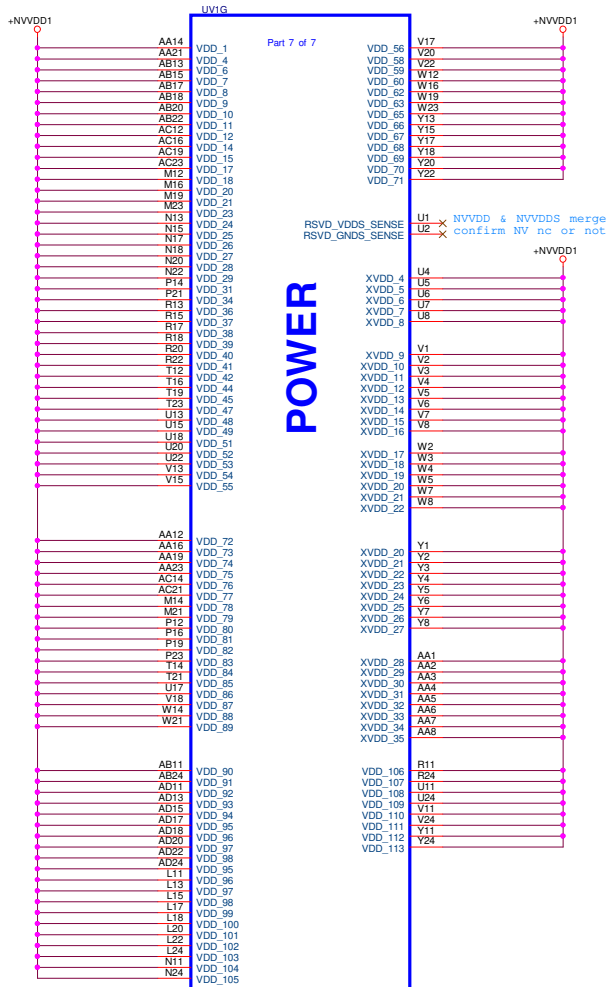
Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	0
L	H	L	0	0	1	1
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	0	0
H	H	H	0	1	0	1
L	L	M	1	0	0	0
L	M	L	1	0	0	1
L	M	H	1	0	1	0
L	H	M	1	0	1	1
M	L	L	1	0	0	0
M	L	H	1	0	0	1
M	H	L	1	1	1	0
M	H	H	1	1	1	1

SMB_ALT_ADDR	
Low	Single GPU
High	Dual GPU
DEVID_SEL	
Low	Orig. Device ID
High	Support G-Sync GPUID
VGA_DEVICE	
Low	3D Device
High	VGA Device
PCIE_CFG	
Low	Normal signal swing
High	Reduce the signal amplitude



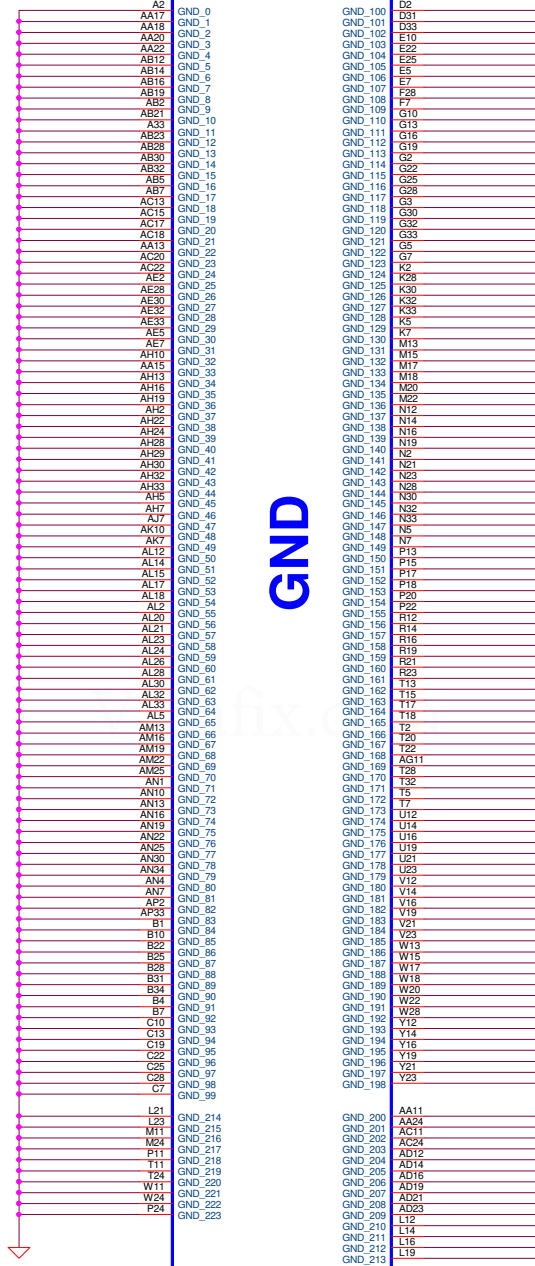
N17P VDD5
1uF*5/4.7uF*5 (under GPU)
330uF*1/22uF*3/10uF*2/4.7uF*2



N18P-G0_FCBGA960-D
@

UWIF

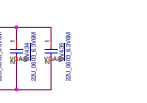
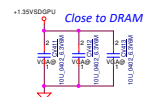
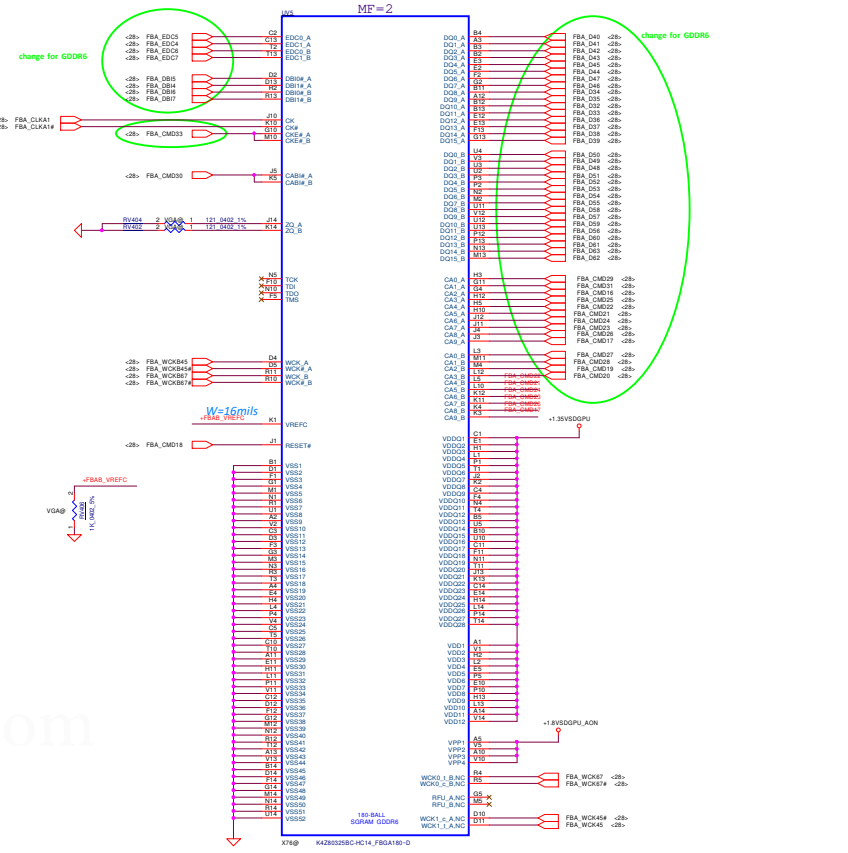
Part 6 of 7



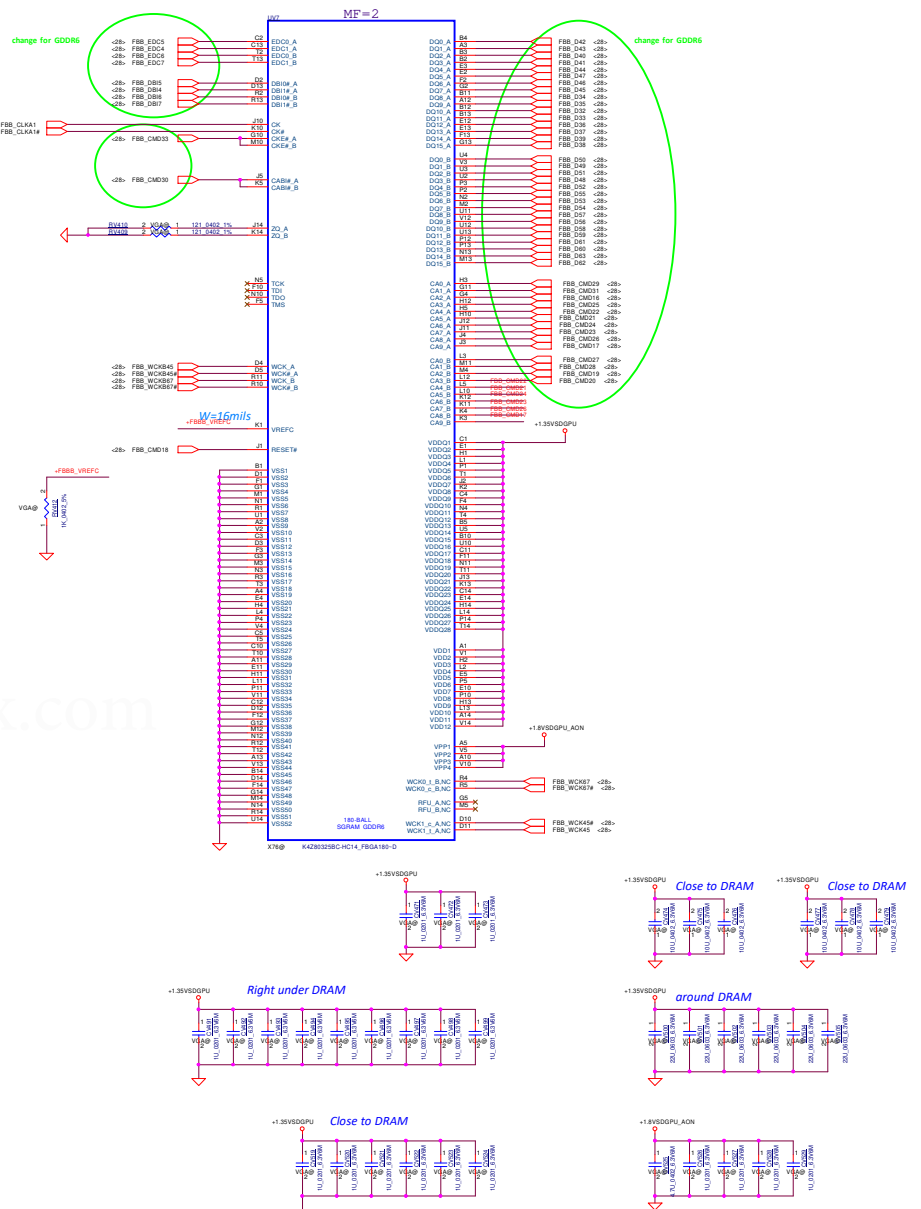
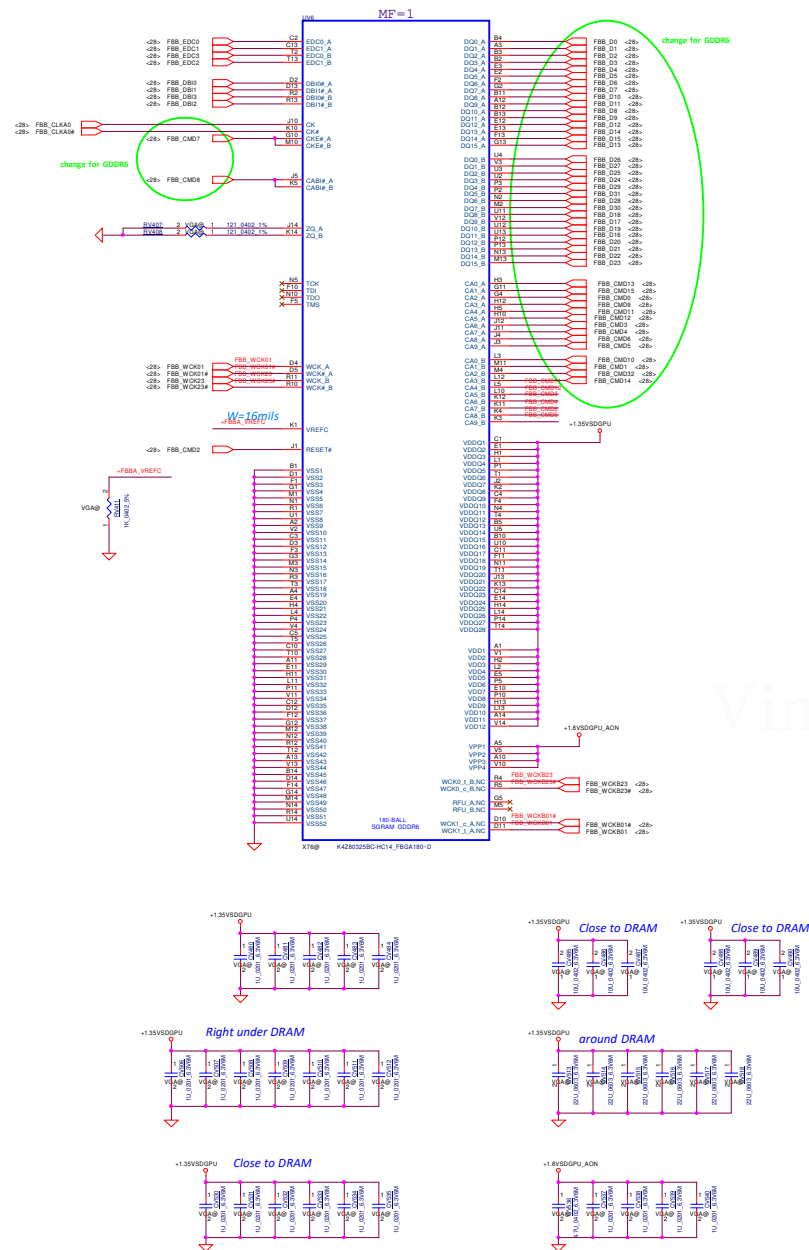
N18P-G0_FCBGA960-D
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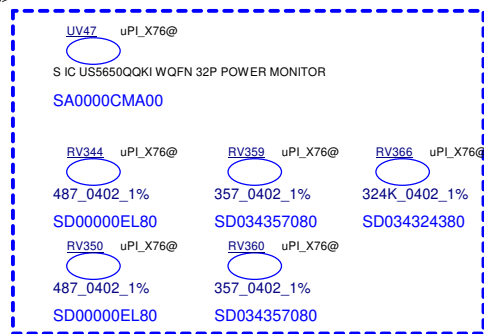
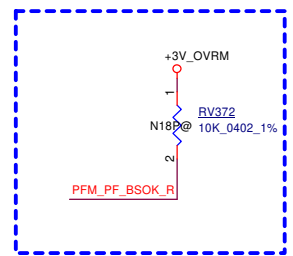
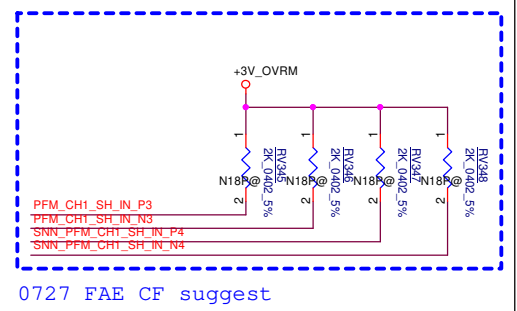
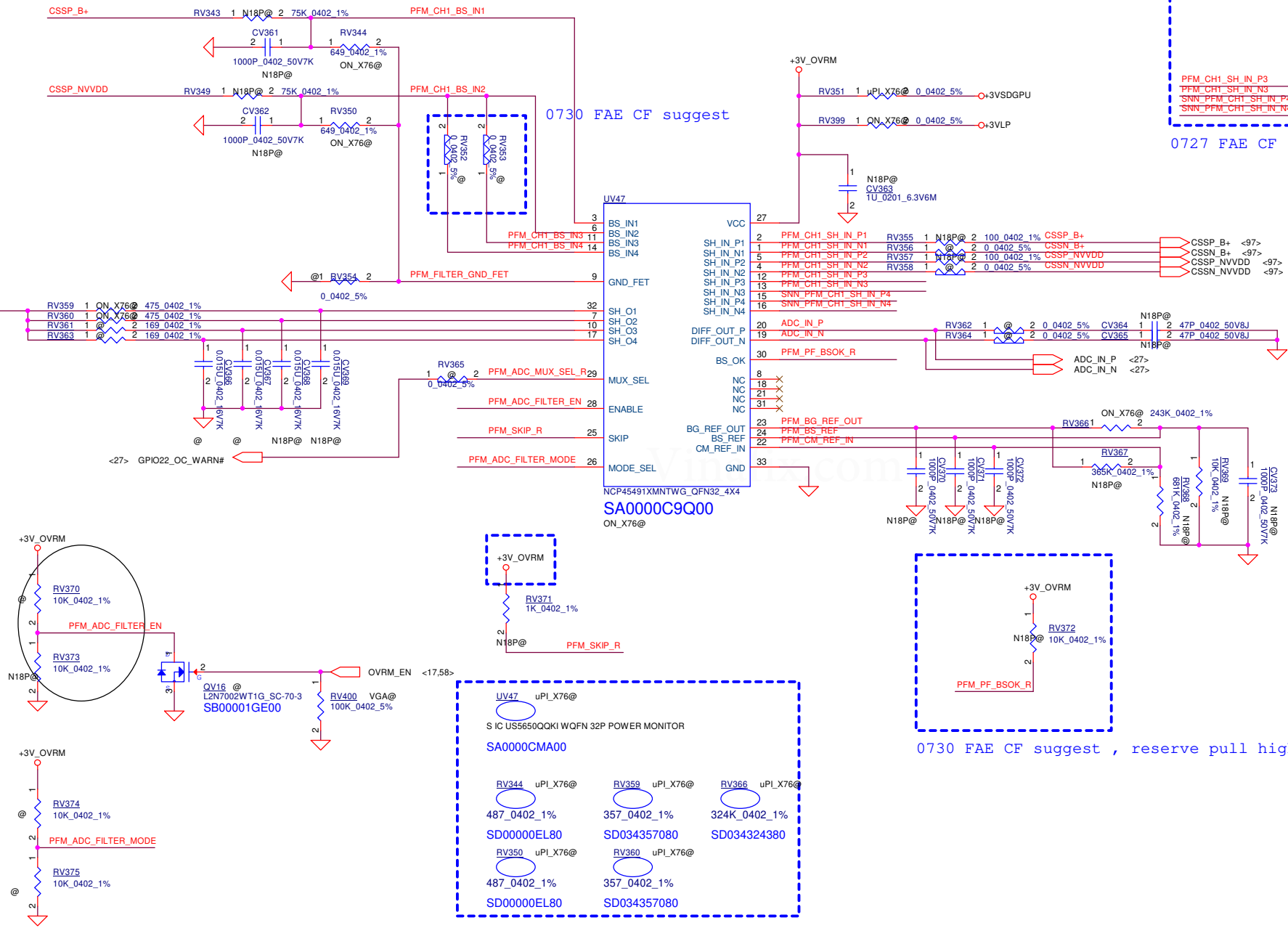
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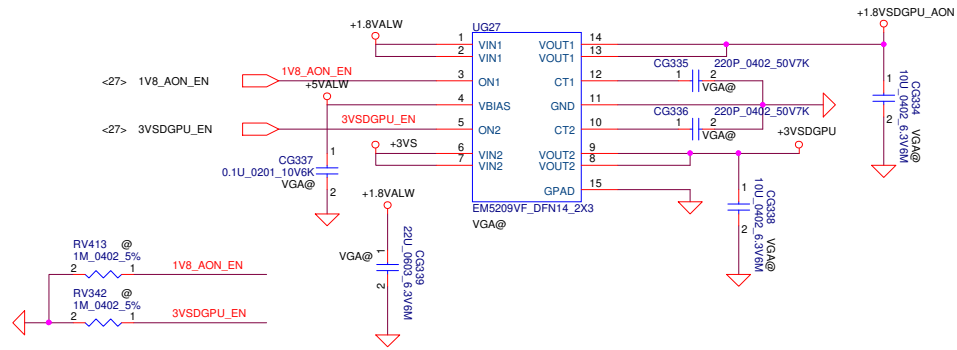
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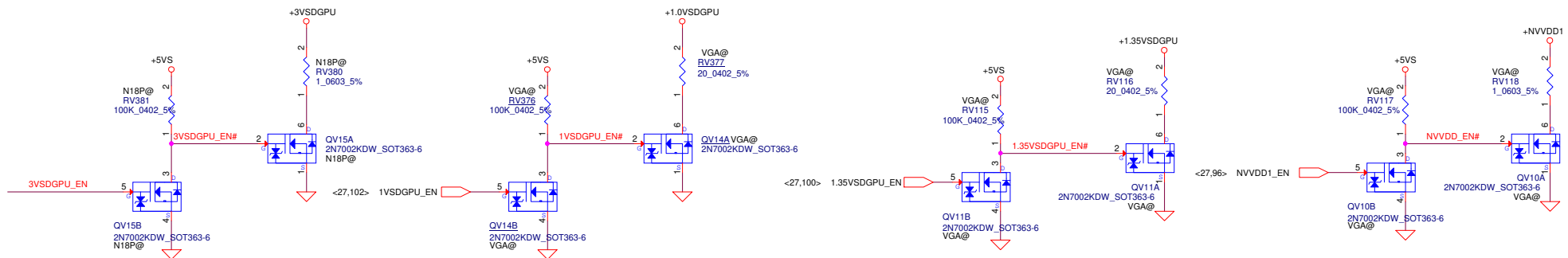
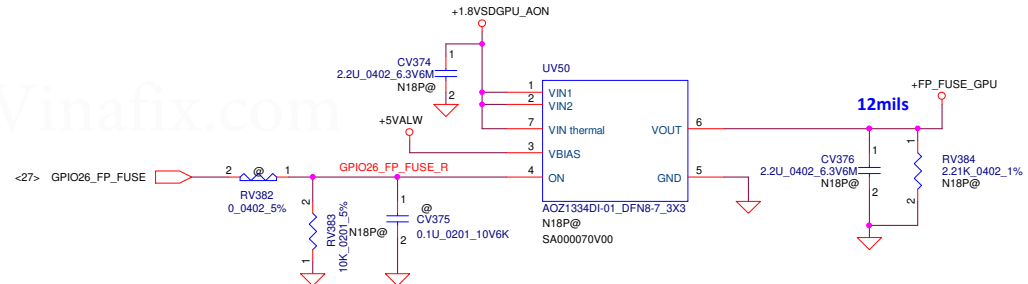
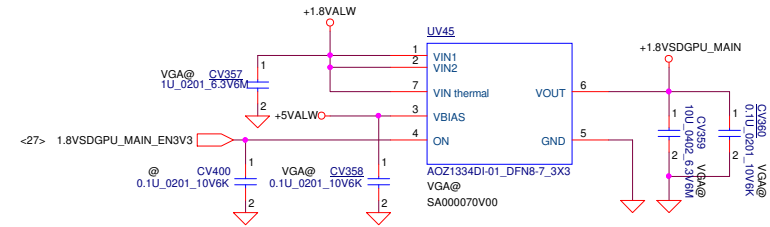
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+1.8V_AON/+3VSDGPU



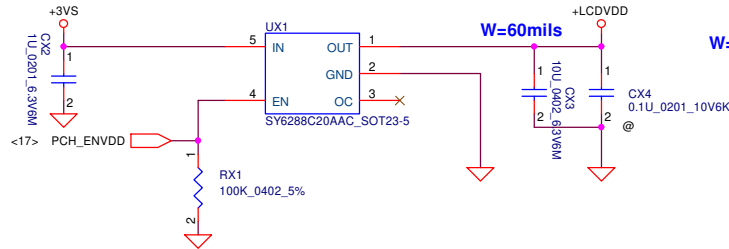
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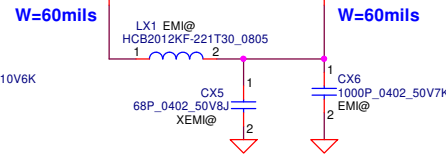
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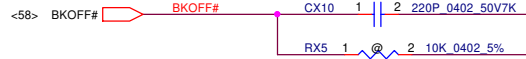
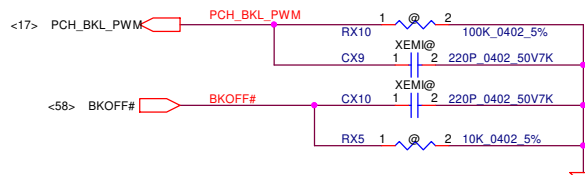
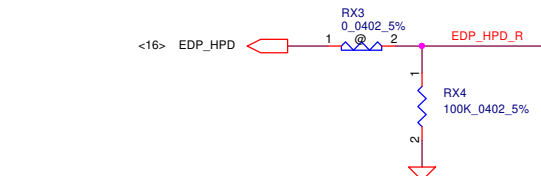
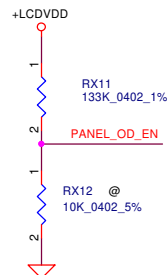
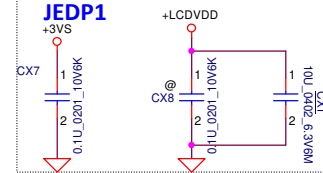
LCD POWER CIRCUIT



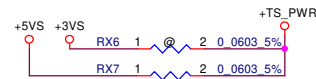
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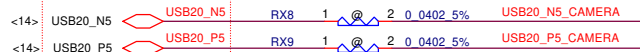
Place closed to
JEDP1



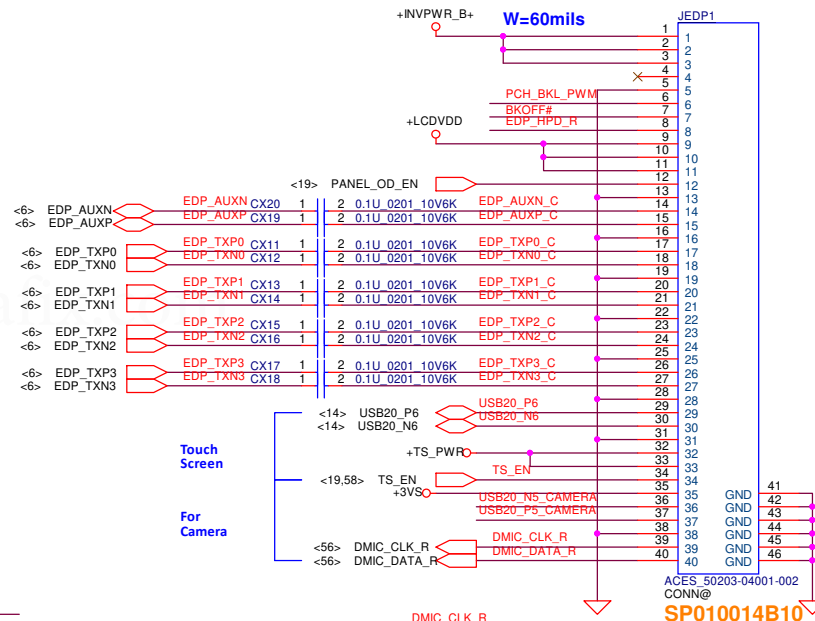
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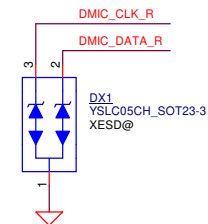
Camera



LED PANEL Conn.



Touch Screen
For Camera

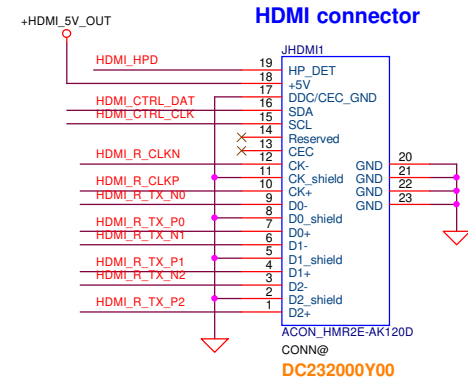
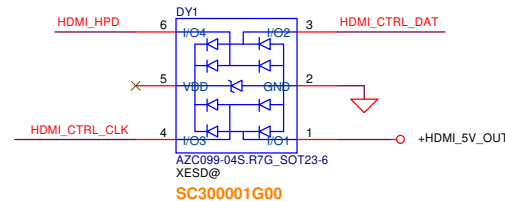
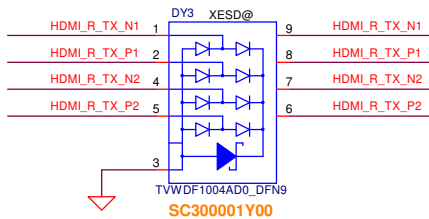
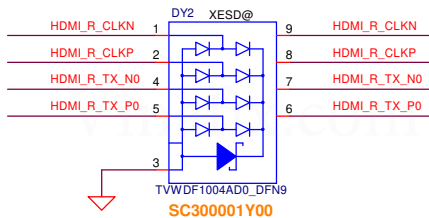
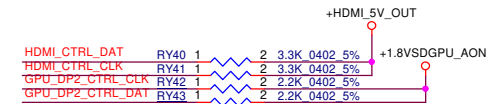
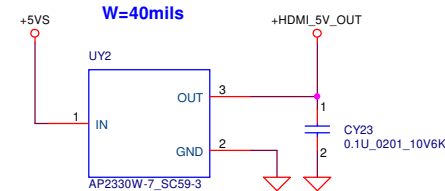
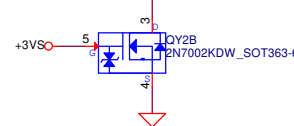
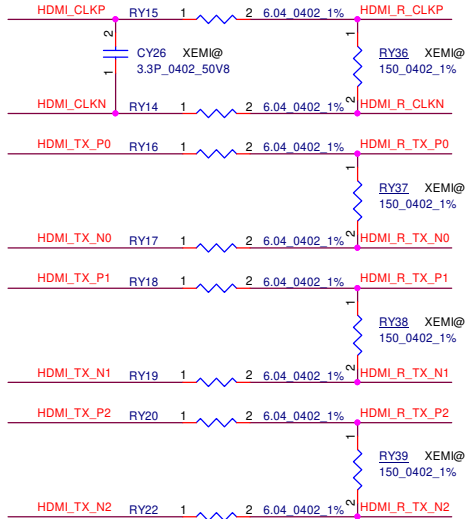
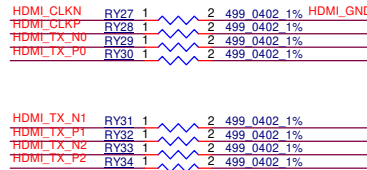
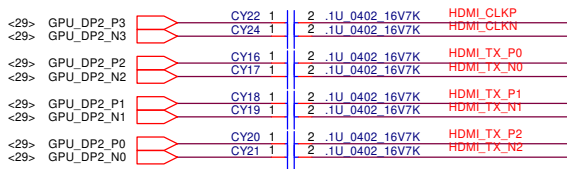


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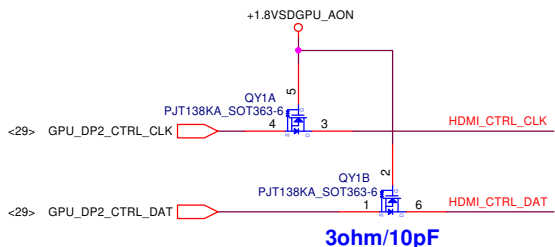
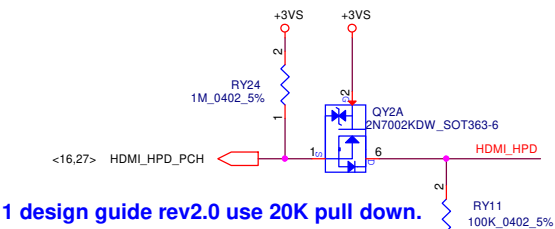
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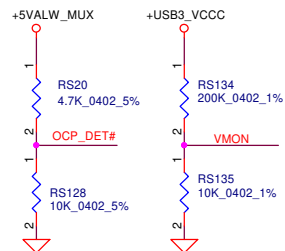
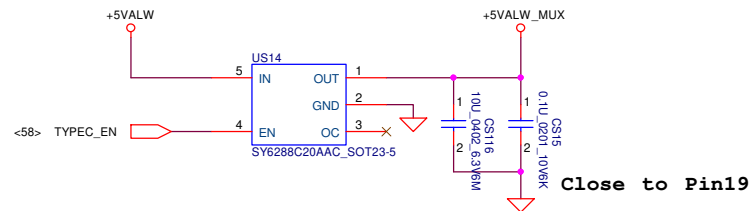
RY11 design guide rev2.0 use 20K pull down.



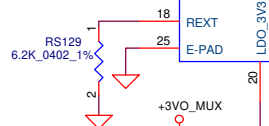
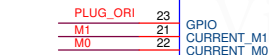
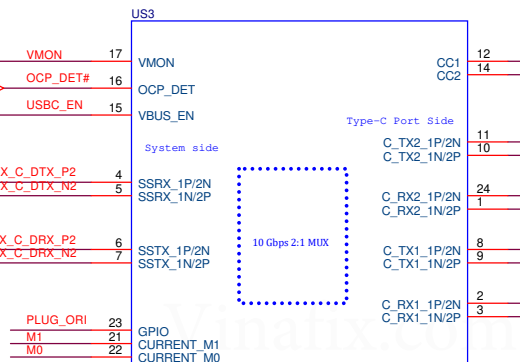
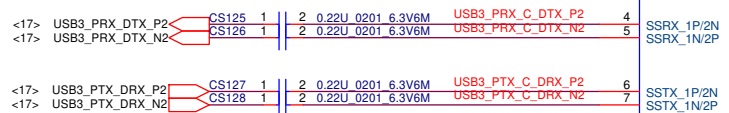
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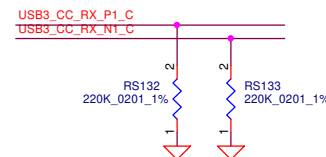
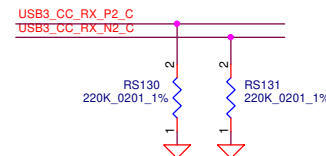
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USB3.0 (Port 2)



Close to Pin13



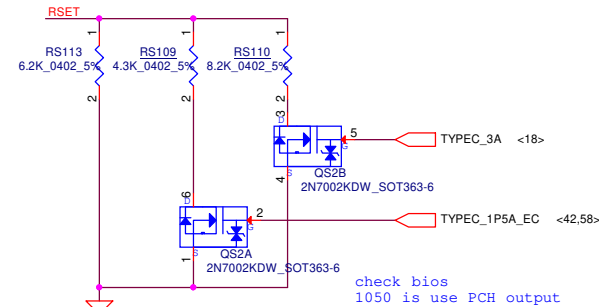
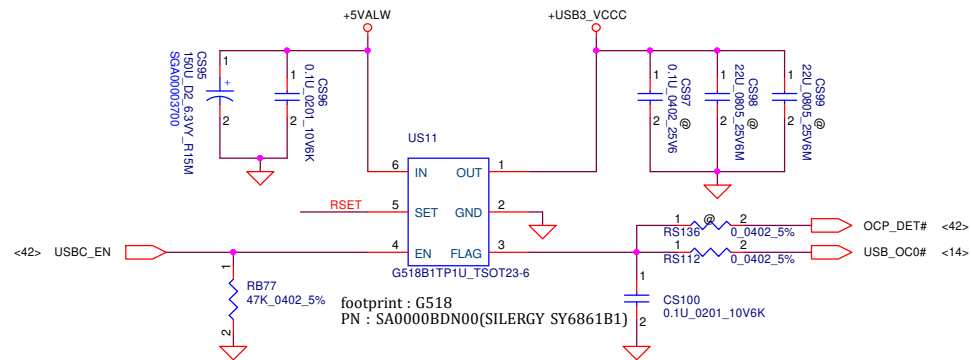
5441E Current Limit		
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

RTS5441 M0 truth table by 2018 BIOS spec			
TYPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

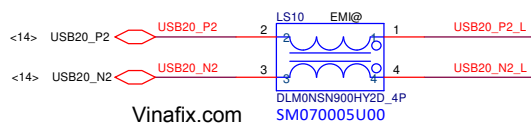
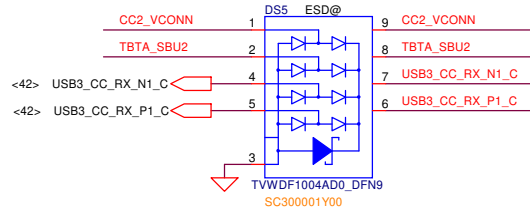
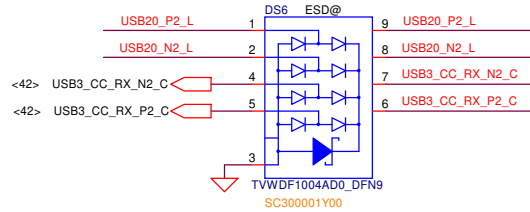
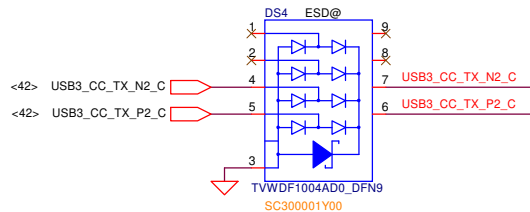
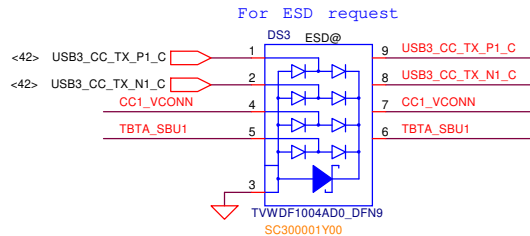
confirm realtek hand-shake

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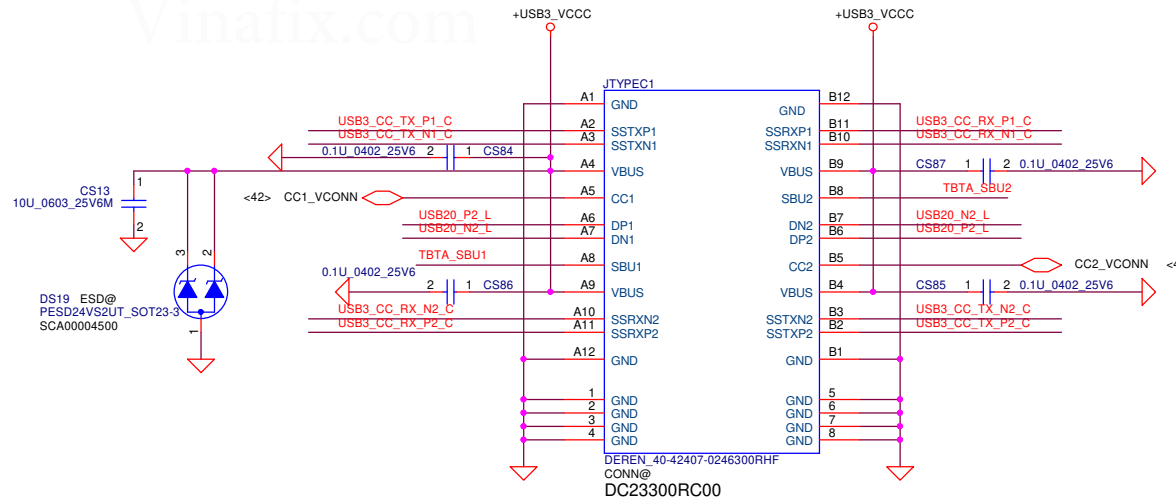
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G518 MOS Current Limit				
GPP_B1 (TYPEC_1P5A)	GPP_B4 (TYPEC_3A)	RSET(kΩ)	MODE	limit point
L	L	6.2	0.9A	1.09A
L	H	3.53	1.5A	1.92A
H	L	2.54	2A	2.67A
*H	H	1.94	3A	3.5A



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CC1_VCONN & CC2_VCONN need 20mil trace width.

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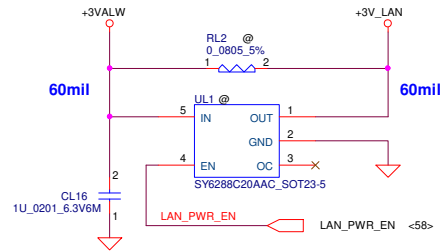
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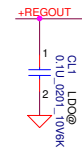
+3V_LAN Rising time (10%-90%) must >0.5mS and <100mS



From EC
High active.
EN threshold voltage min:1.2V
typ:1.6V max:2.0V
Current limit threshold 1.5~2.8A
+3V_LAN Rising time must >0.5ms and <100ms

RTL8111H LDO mode
RTL8118ASA SWR mode

W=60mil



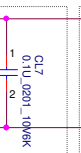
Using for Switch mode

The trace length from Lx to PIN48 (REGOUT) and from C to Lx must < 200mils.

11/27: P/N change to SH00000RT00
(S COIL 2.2UH +20%
HPC252012NF-2R2M 1.3A)

W=60mil

300mA

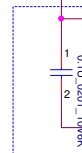


Place near Pin 3,8,22,30

Place near Pin 22

W=60mil

300mA



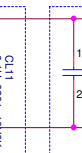
Place near Pin 11,32

Using for Switch mode

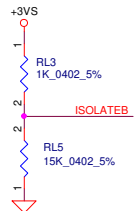
The trace length from C to PIN46,47(VDDREG) must < 200mils.

Place near Pin 11,32

W=60mil

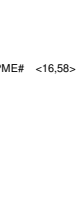
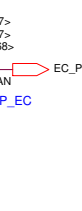
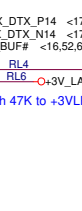
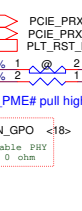
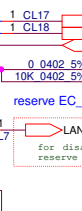
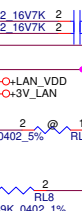
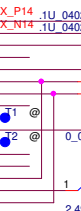
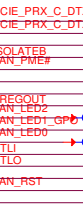
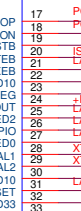
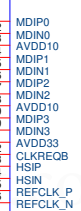
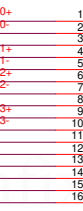


Reserve for surge improvement
Place near Pin 11,32

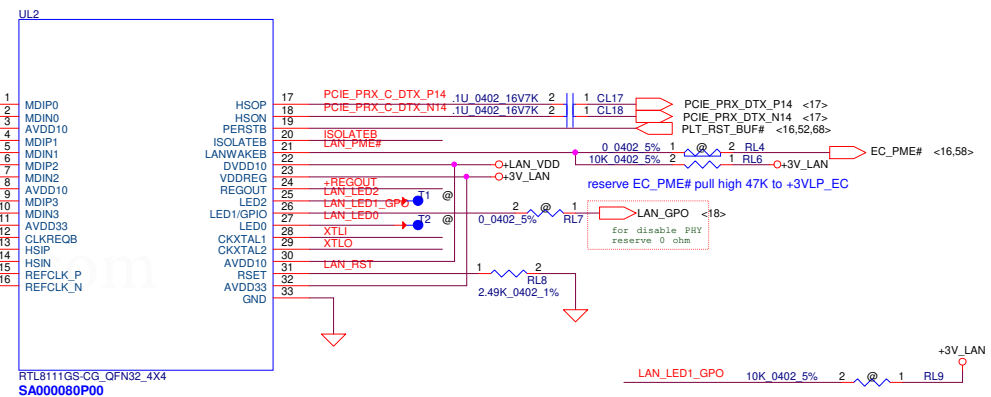
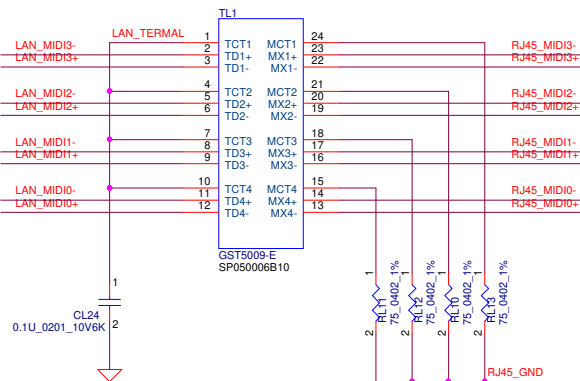


LAN_CLKREQ# pull up at PCH side

<15> LAN_CLKREQ#
<17> PCIE_PTX_C_DRX_P14
<17> PCIE_PTX_C_DRX_N14
<15> CLK_PCIE_LAN
<15> CLK_PCIE_LAN#

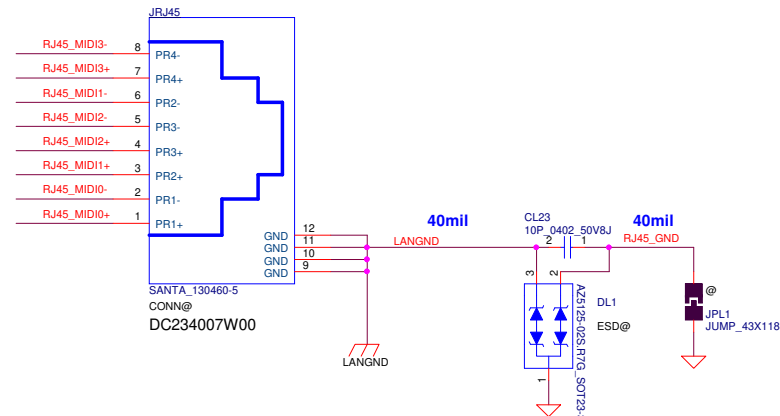


P/N: SJ10000UP00 (S CRYSTAL 25MHZ 10PF XRCGB25M000F2P34R0)



SA000080P00, S IC RTL8111H-CG QFN 32P E-LAN CTRL

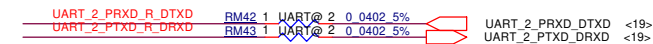
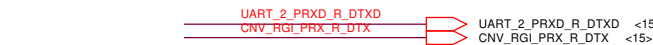
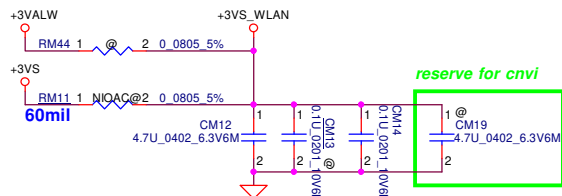
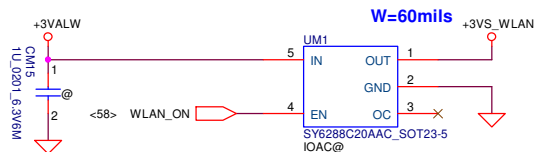
LAN Connector



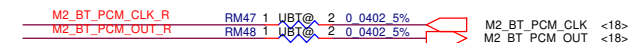
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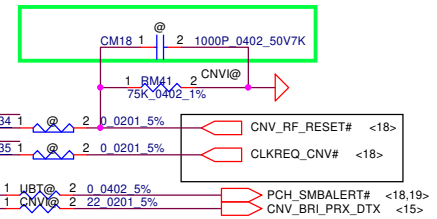
Wireless LAN



Co-layout with CNVi for SW debug

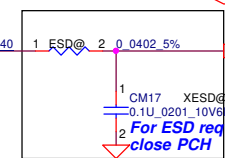


Co-layout with UART BT



Component	Signal	Direction
CNV0@	CNV_RGI_PTX_DRX	<15>
CNV0@	CNV_RGI_PRX_DTX	<15>
CNV0@	CNV_BRI_PTX_DRX	<15>
E51TXD	P80DATA	<58>
E51RXD	P80CLK	<58>
UBT@	WAKE_BT	<19>

For CNVi Feature



reserve for BT_ON OD pull high (1.0)

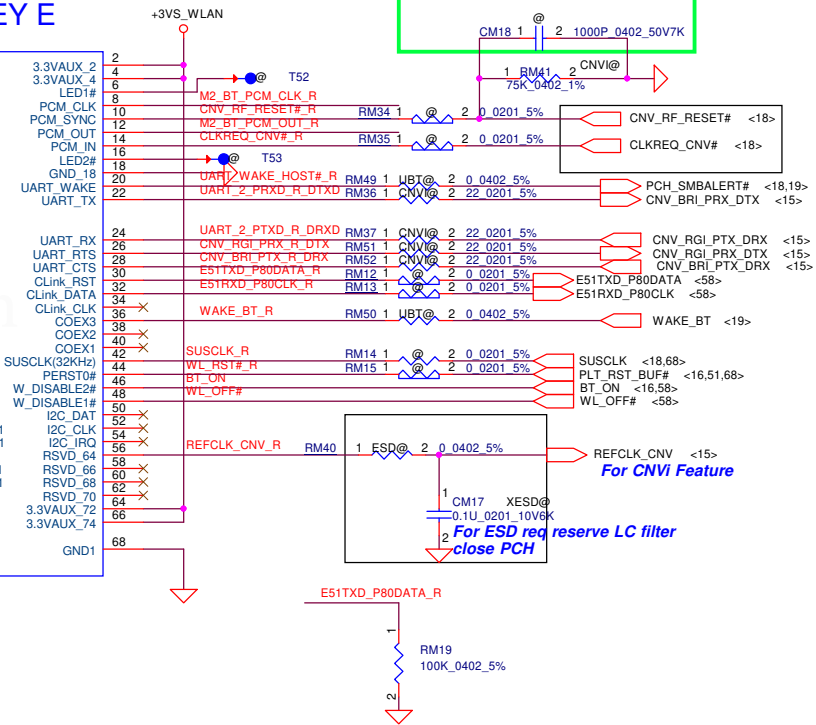
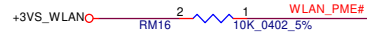
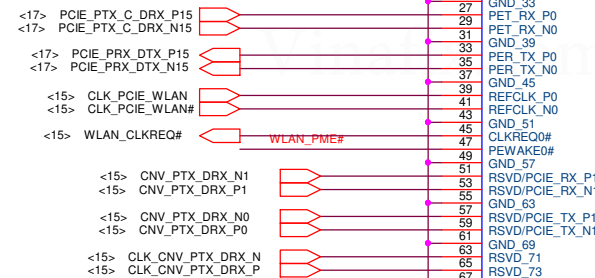
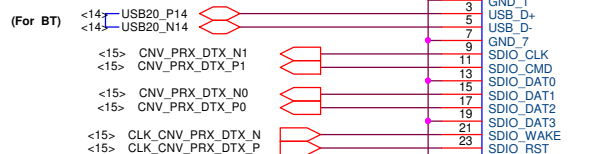


NGFF WL+BT (KEY E)

74	2.0	GND	75
72	2.0	RESERVED/REFCLK1	73
70	UM_Power_SPC/GPIO/PFWake#	RESERVED/REFCLK1	71
68	UM_Power_SNN/CLKREQ2	GND	69
66	UM_SW_PERRST#	Reserved/PErP1	67
64	RESERVED	Reserved/PErP1	65
62	ALERT# (I/O/3.3)	GND	63
60	QCC CLK (I/O/3.3)	Reserved/PErP1	61
58	QCC DATA (I/O/3.3)	Reserved/PErP1	59
56	W_DISABLE1 (I/O/3.3V)	GND	57
54	Reserved/W_DISABLE2 (I/O/3.3V)	PEWake# (I/O/3.3V)	55
52	PEB70W (I/O/3.3V)	CLKREQ0 (I/O/3.3V)	53
50	SUSCIN(20MHz) (I/O/3.3V)	GND	51
48	CODE1 (I/O/0.1.8V)	REFCLK1	49
46	CODE2(1) (I/O/1.8V)	REFCLK0	47
44	CODE3(1) (I/O/1.8V)	GND	45
42	VENDOR DEFINED	PErG0	43
40	VENDOR DEFINED	PErG0	41
38	VENDOR DEFINED	PErG0	39
36	UART RTS (I/O/1.8V)	PErTn0	37
34	UART CTS (I/O/1.8V)	PErTn0	35
32	UART Tx (I/O/1.8V)	GND	33
22	UART Rx (I/O/1.8V)	SDIO Reset# (I/O/1.8V)	23
20	UART Wake# (I/O/3.3V)	SDIO Wake# (I/O/1.8V)	21
18	GND	SDIO DAT1 (I/O/1.8V)	19
16	LED#2 (I/O/0)	SDIO DAT2 (I/O/1.8V)	17
14	PCM_DAT0/IS_DS_OUT (I/O/1.8V)	SDIO DAT3 (I/O/1.8V)	15
12	PCM_IN/IS_DS_IN (I/O/1.8V)	SDIO DAT4 (I/O/1.8V)	13
10	PCM_SYNC/IS_WS (I/O/1.8V)	SDIO CMD0 (I/O/1.8V)	11
8	PCM_CLK/IS_SCK (I/O/1.8V)	SDIO CLK (I/O/1.8V)	9
6	LED#1 (I/O/0)	GND	7
4	2.0	GND	5
2	2.0	USB_D-	3
		USB_D+	1

(link to PICE Port 3)
PCIE X1

(From PCH CLKOUT2)
PCIE CLK



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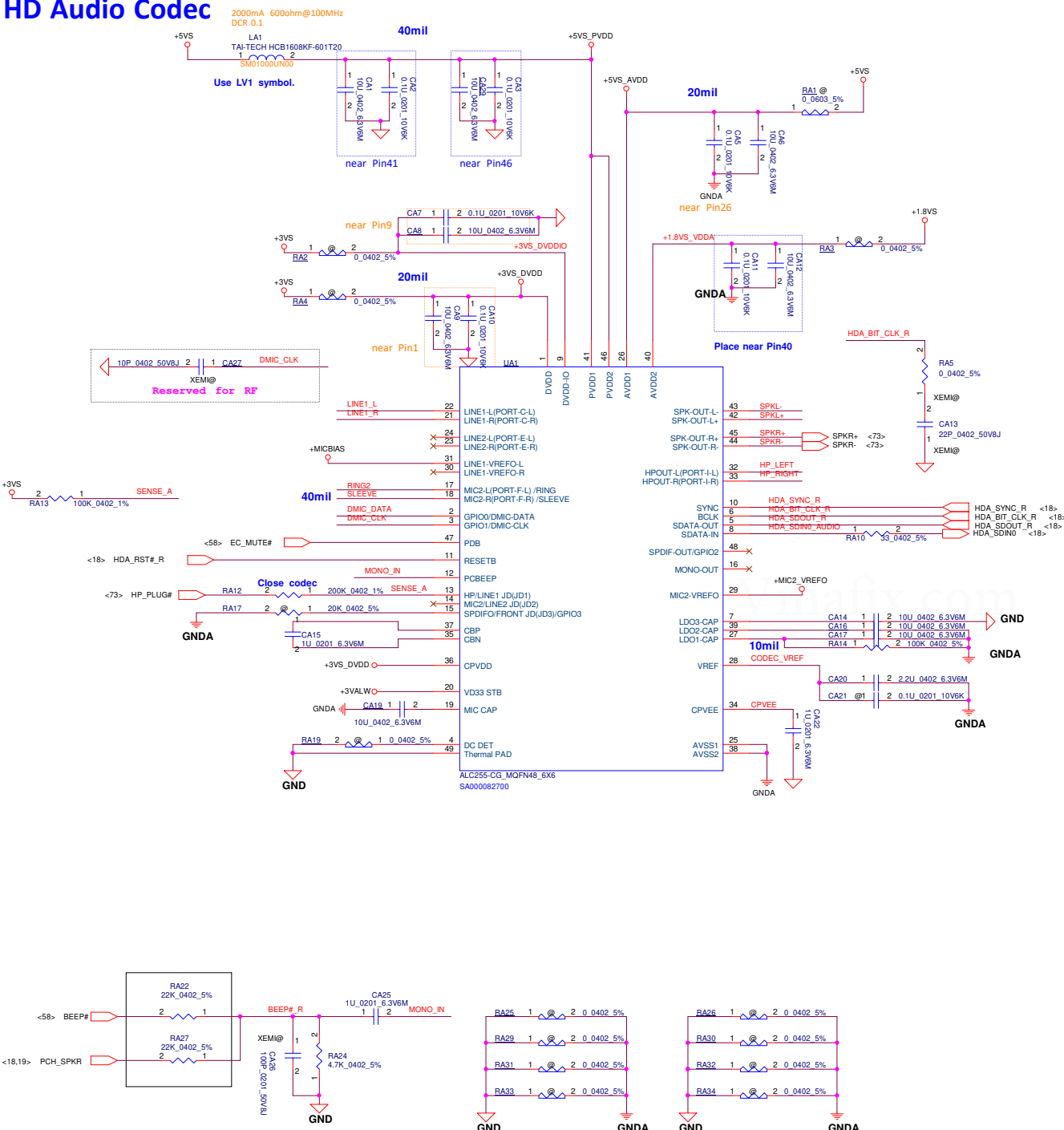
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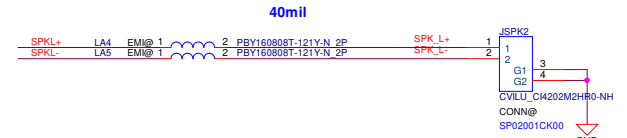
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HD Audio Codec

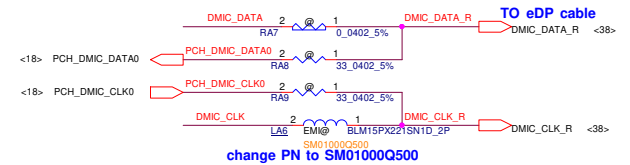


Int. Speaker Conn.

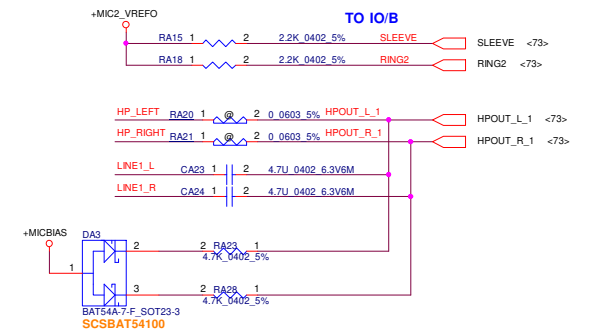


Digital MIC

MIC BOM upload by Audio Team



Headphone Out



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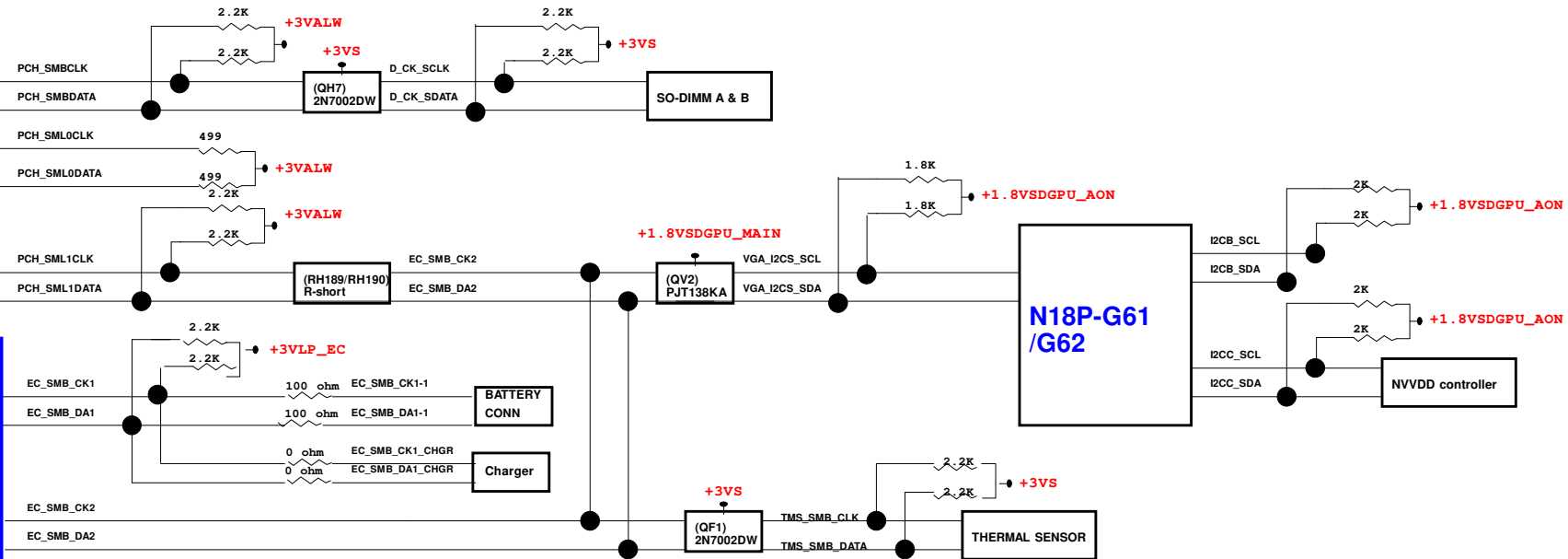
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Cannonlake
PCH - H

KB9022

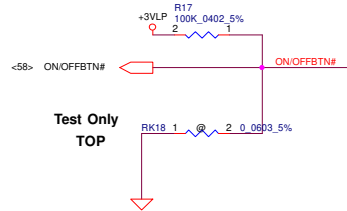


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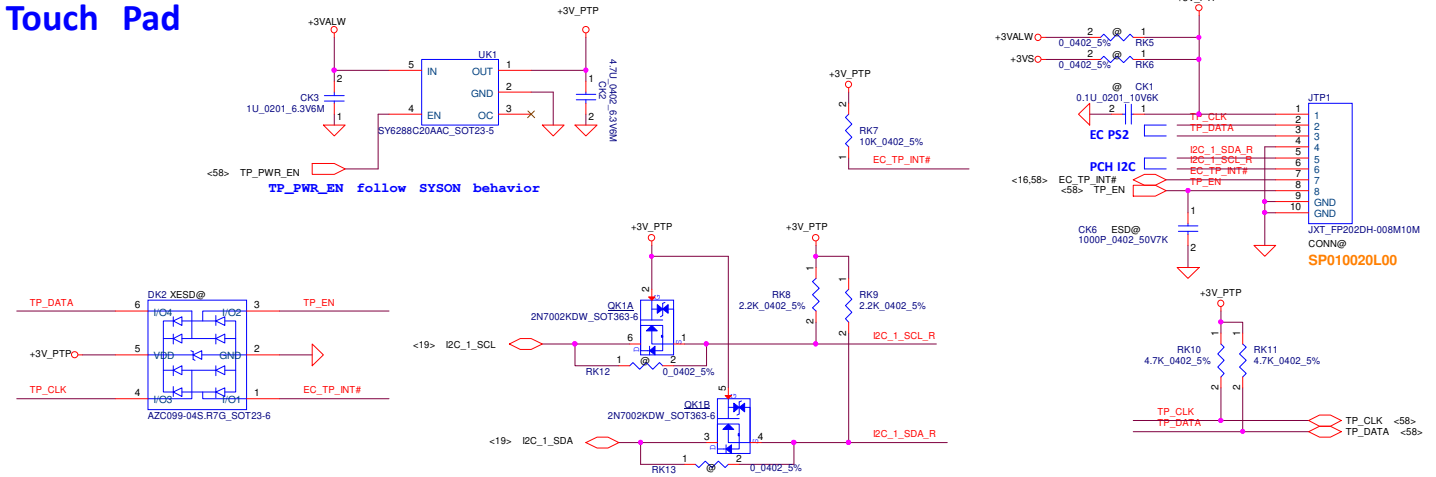
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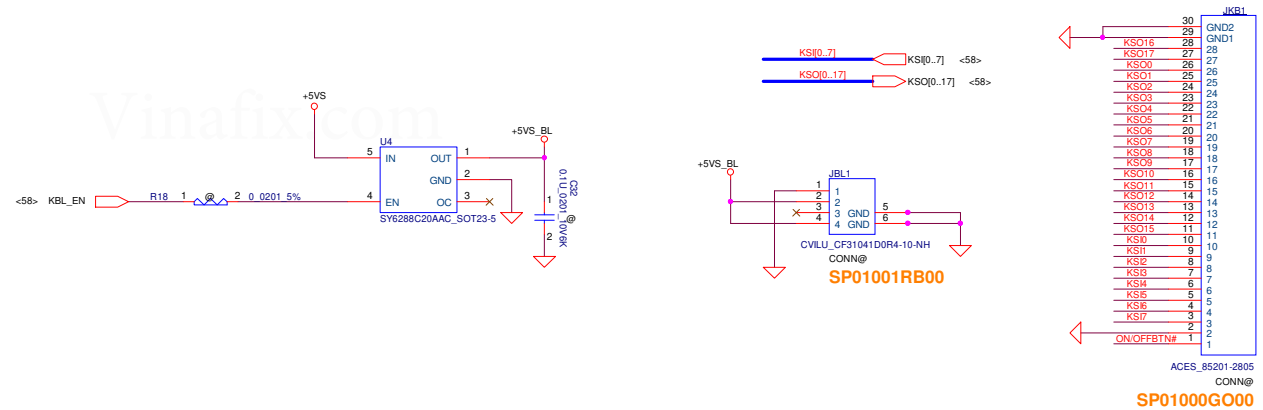
ON/OFF BTN



Touch Pad



KB Conn. / Backlight



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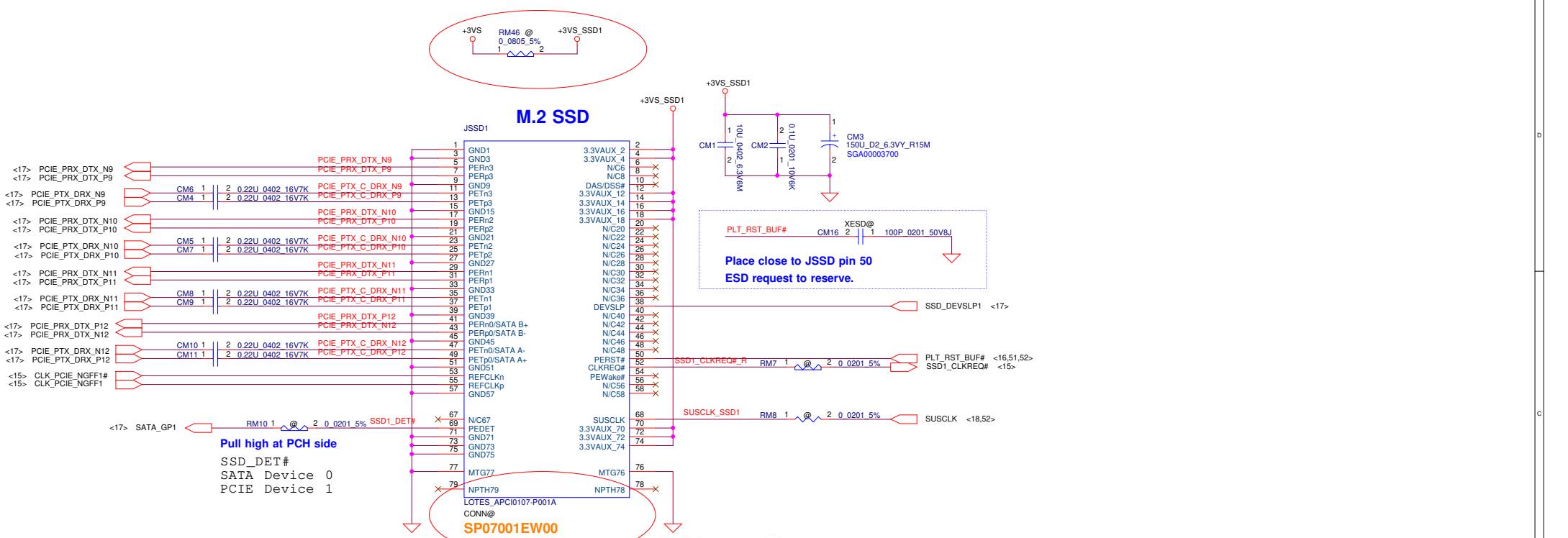
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				Size	Document Number
				Custom	Rev
				FH5VF M/B LA-J861P	
				Date:	Wednesday, February 05, 2020
				Sheet	67 of 112



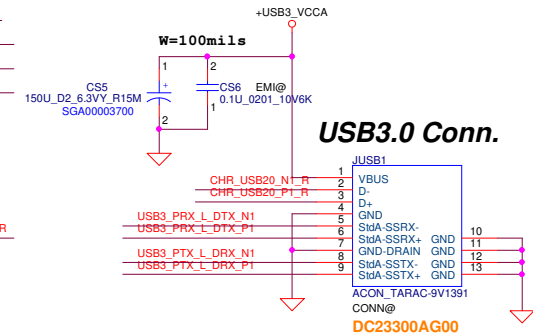
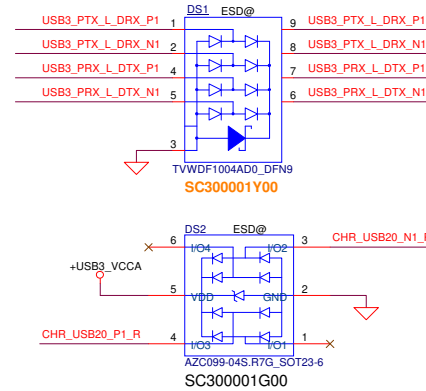
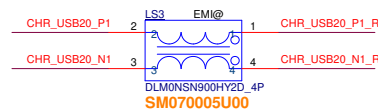
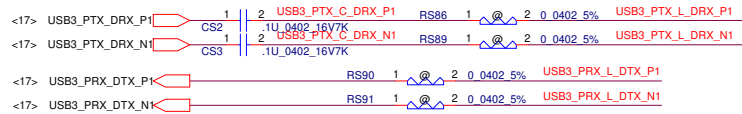
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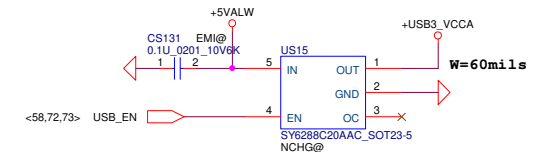
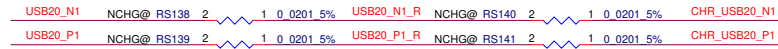
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USB3.0



USB3.0 Conn.



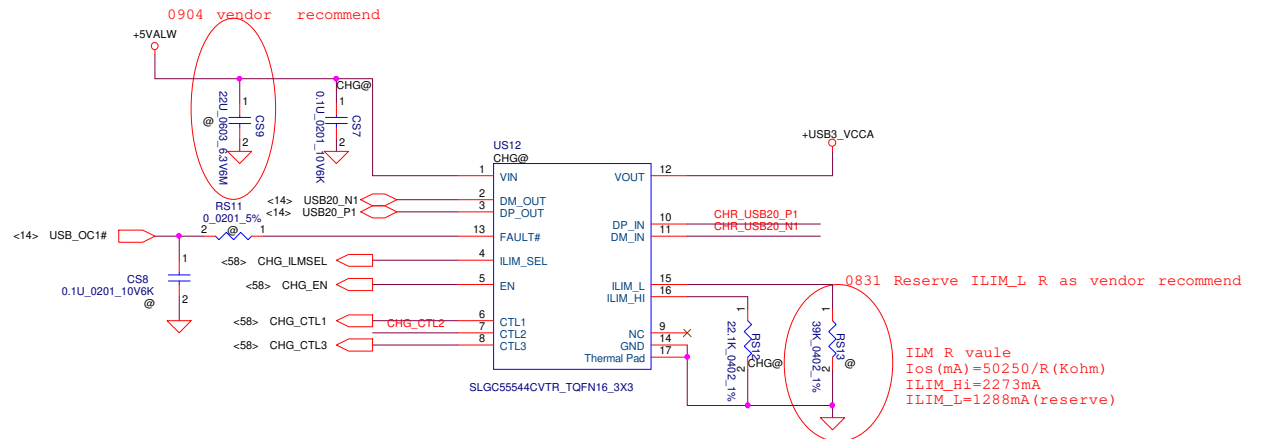
USB Host Charger



0911 Reserve PU, vendor suggest to EC control if future need support SDP2

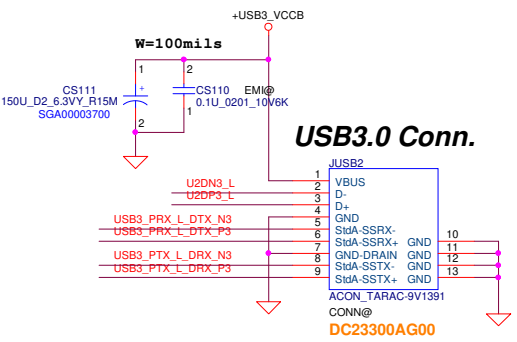
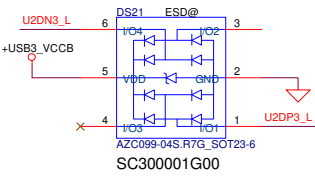
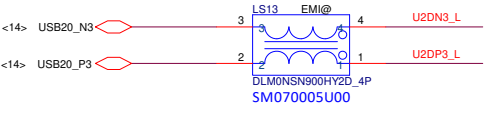
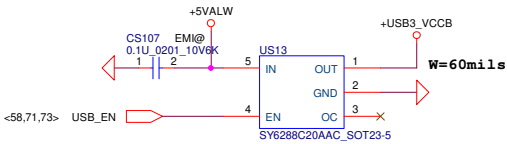
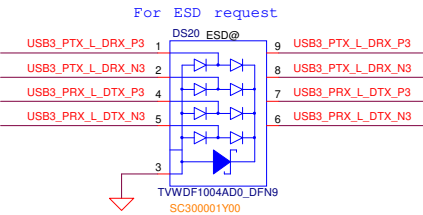
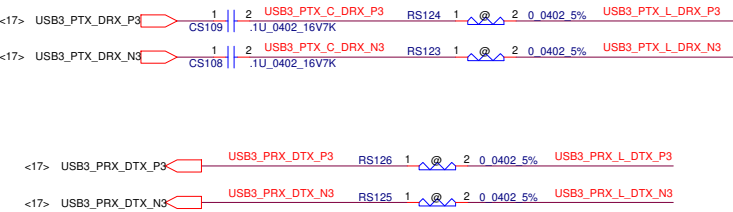
USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Setting	Limit	Note
0	1	0	1	1	SDP1-OFF	ILIM_H	Port power off	
0	1	0	1	1	SDP1	ILIM_H	Data Lines Connected	
0	1	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected	
1	1	1	1	1	CDP	ILIM_H	Data Lines Connected	

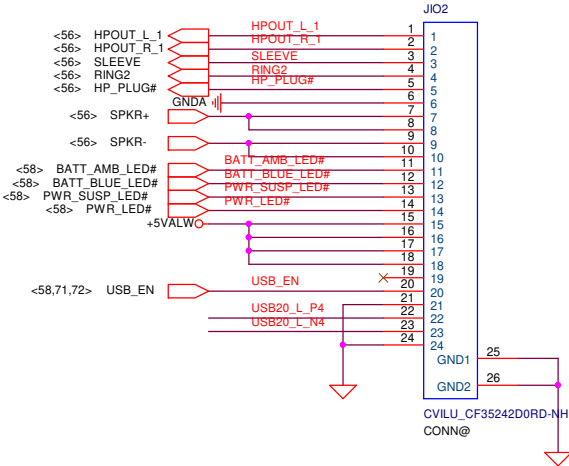
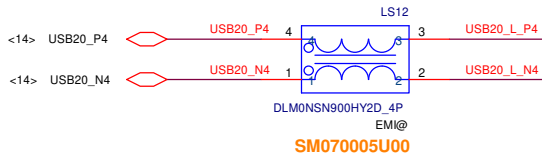


ILM R vaule
Ios (mA)=50250/R (Kohm)
ILIM_Hi=2273mA
ILIM_L=1288mA (reserve)

USB3.0



IO/B CONN



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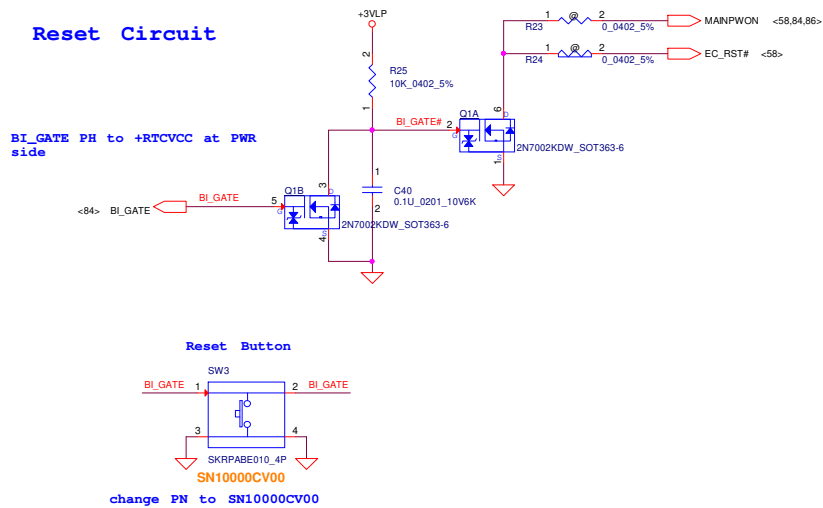
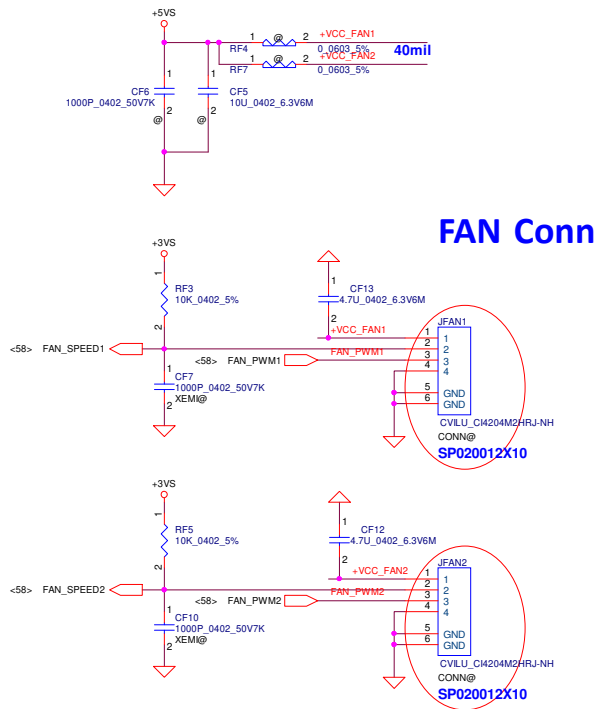
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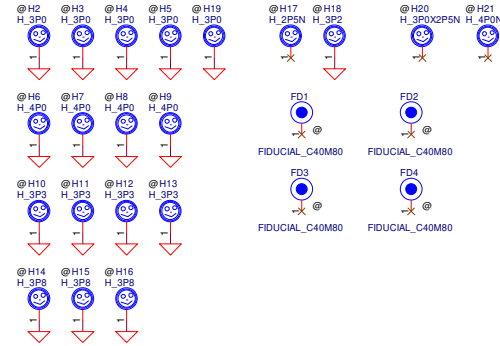
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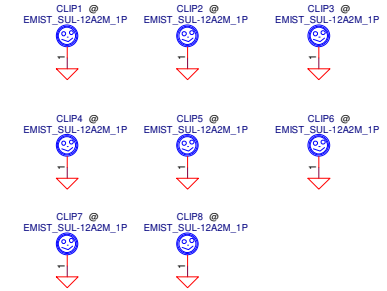
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Screw Hole



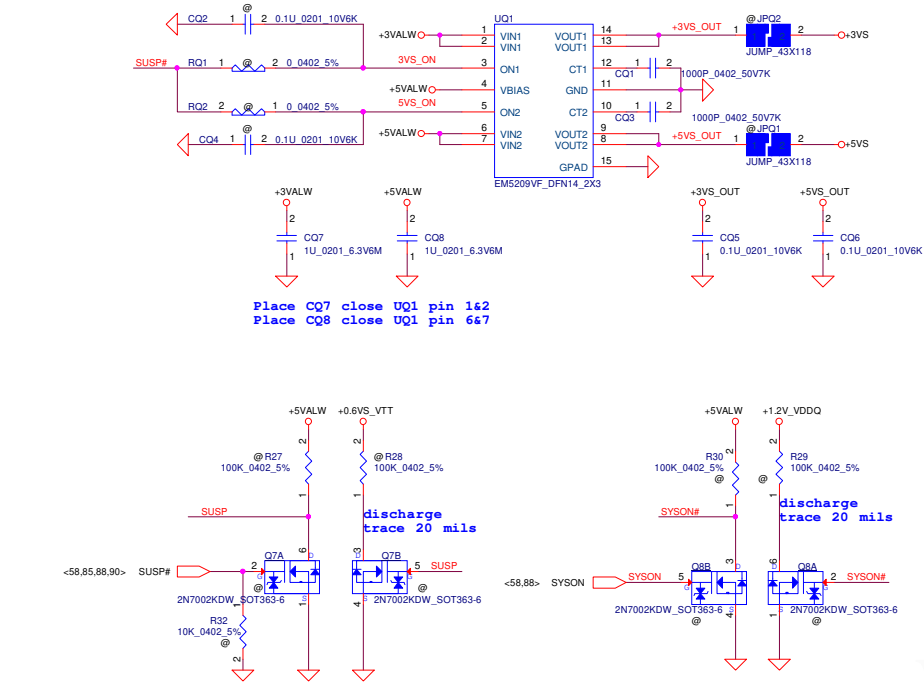
Clips



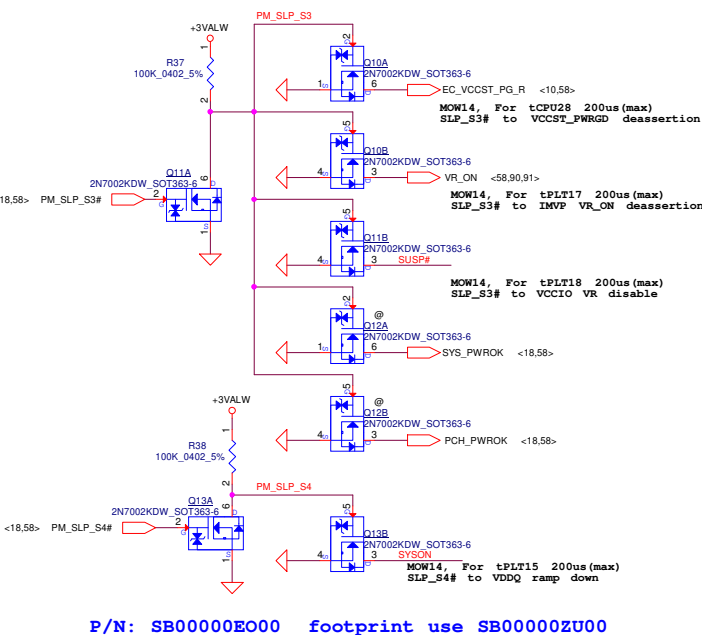
Vinafix.com

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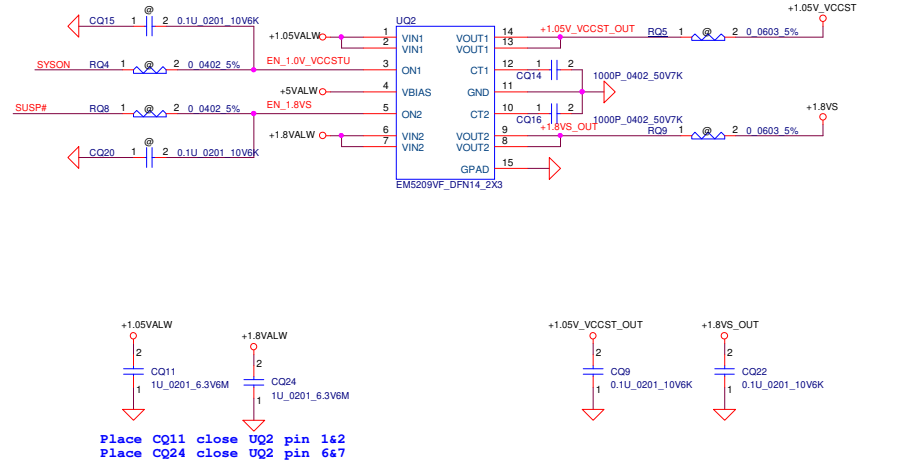
System DC interface



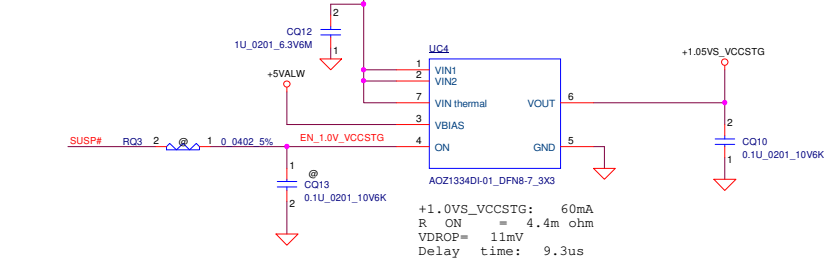
For Power ON/Off Sequence



+1.05VALW TO +1.05V_VCCST /+1.8VALW TO +1.8VS



+1.05VALW TO +1.05VS_VCCSTG



Reserve Page

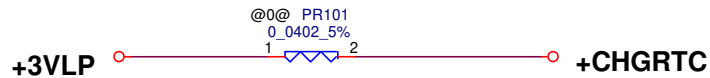
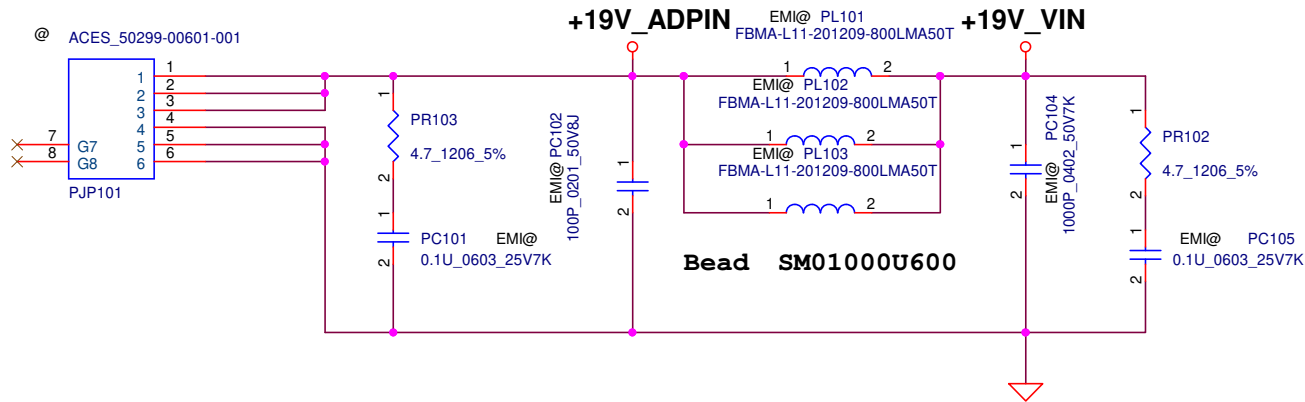
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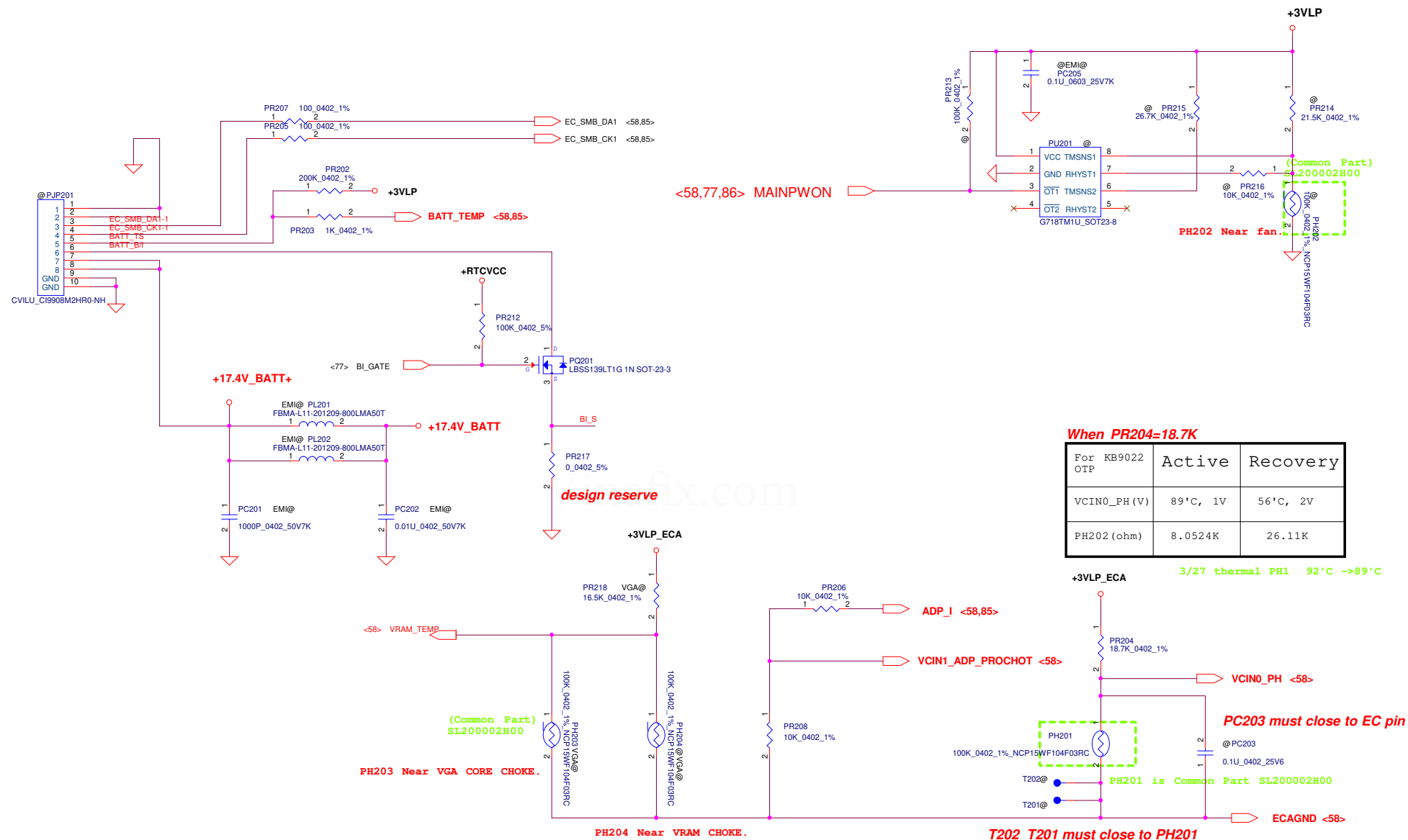
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Battery Bot Side

PIN1 GND
PIN2 GND
PIN3 SMD
PIN4 SMC
PIN5 TEMP
PIN6 BI
PIN7 Batt+
PIN8 Batt+



When PR204=18.7K

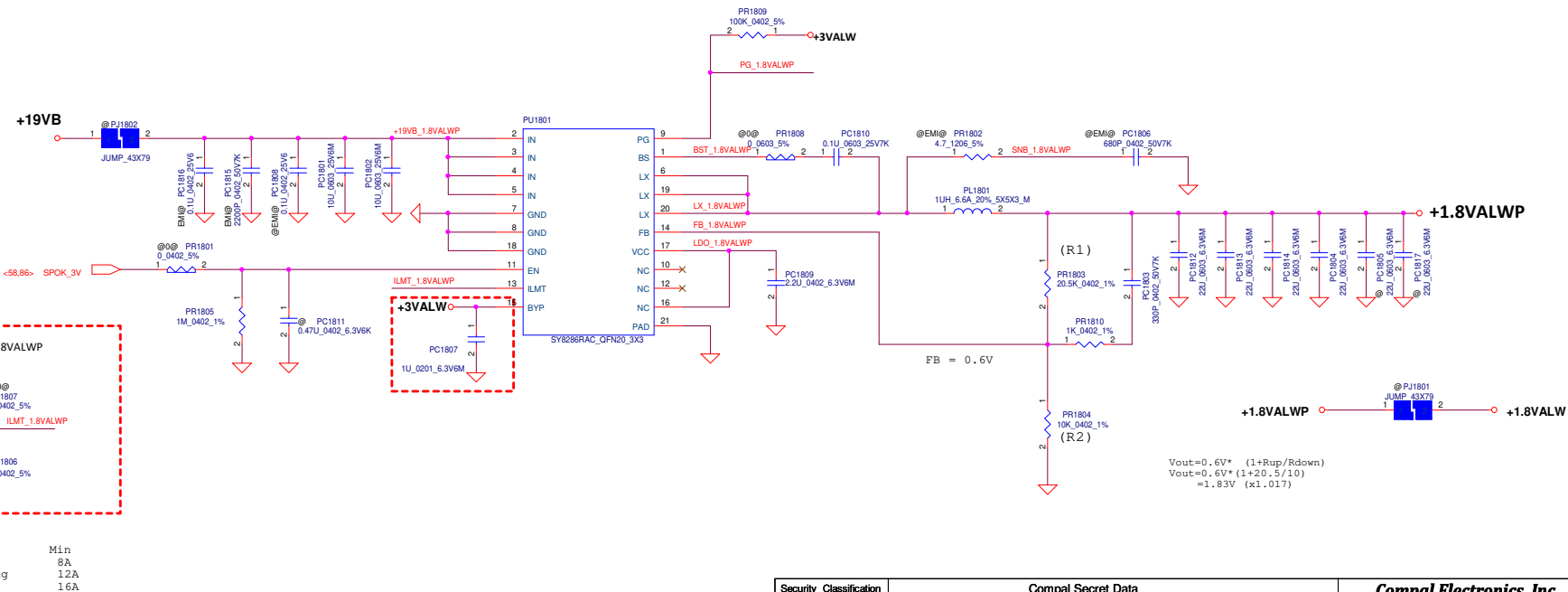
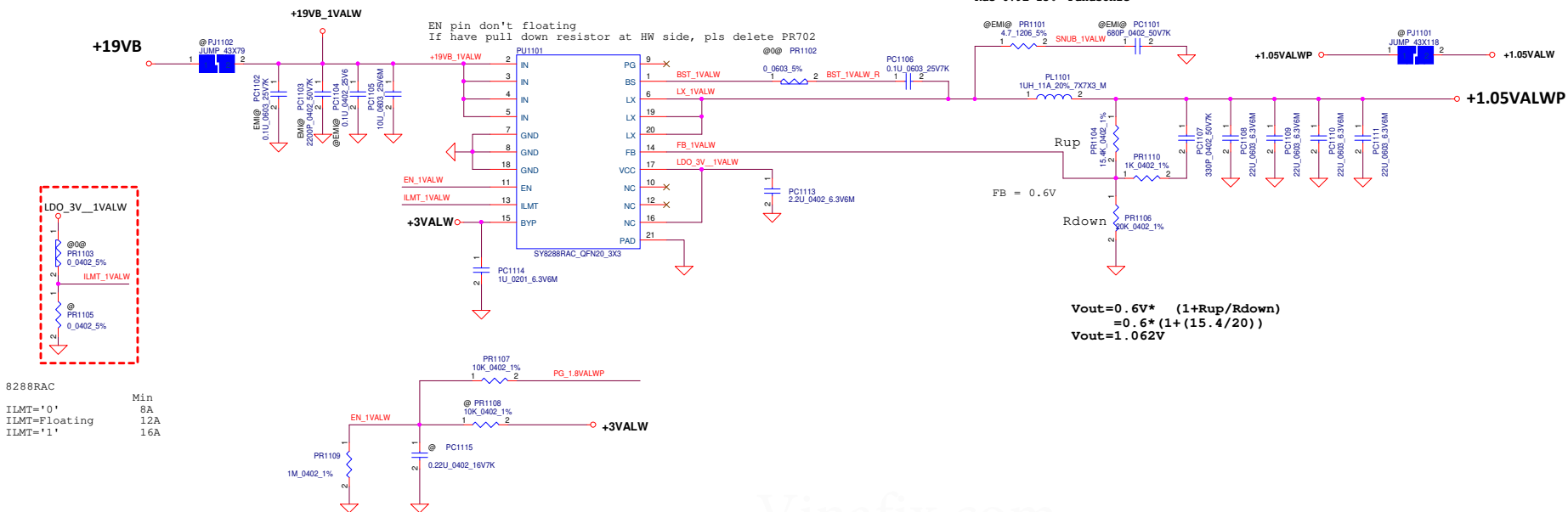
For KB9022 OTP	Active	Recovery
VCIN0_PH (V)	89'C, 1V	56'C, 2V
PH202 (ohm)	8.0524K	26.11K

3/27 thermal PH1 92'C ->89'C

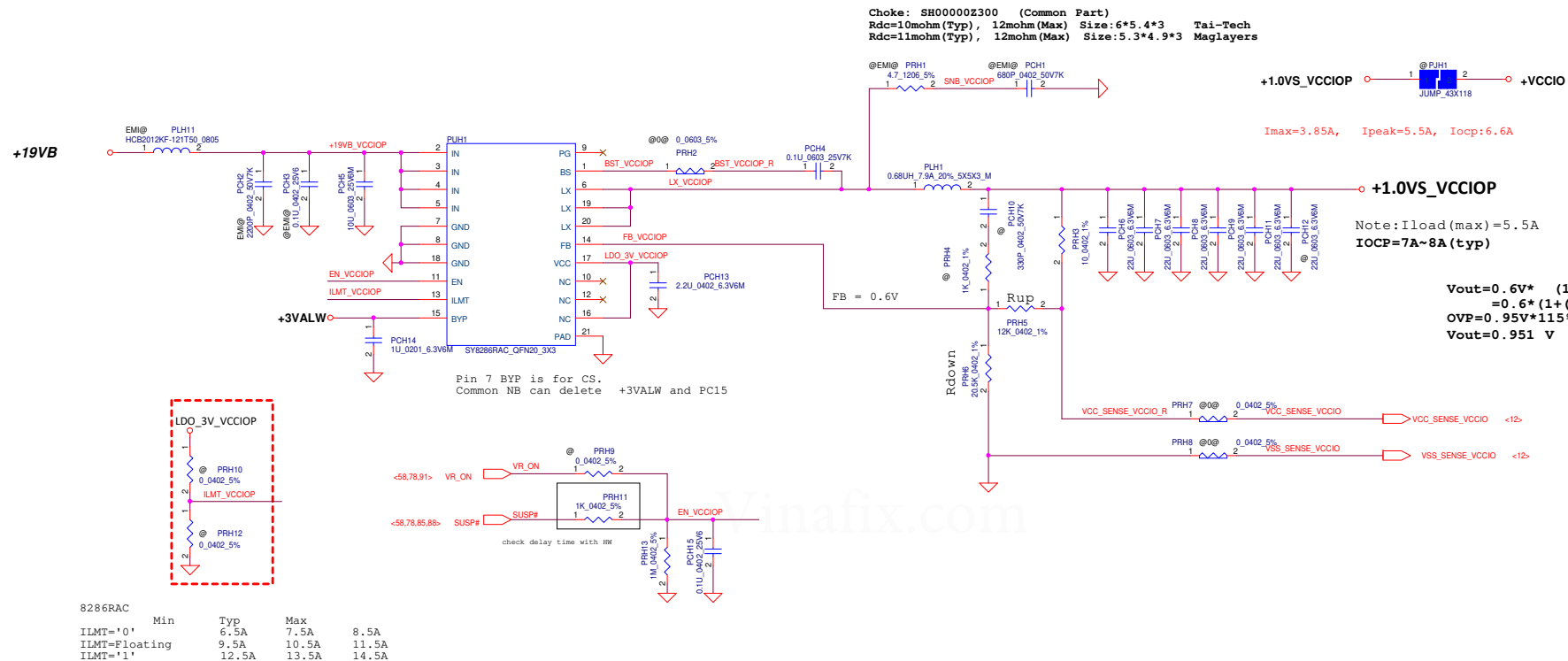
$$ADP_I = 20 * I(\text{adapter}) * 0.01$$
$$I(\text{adapter}) = \text{adapter (W)} * 130\% / 19$$

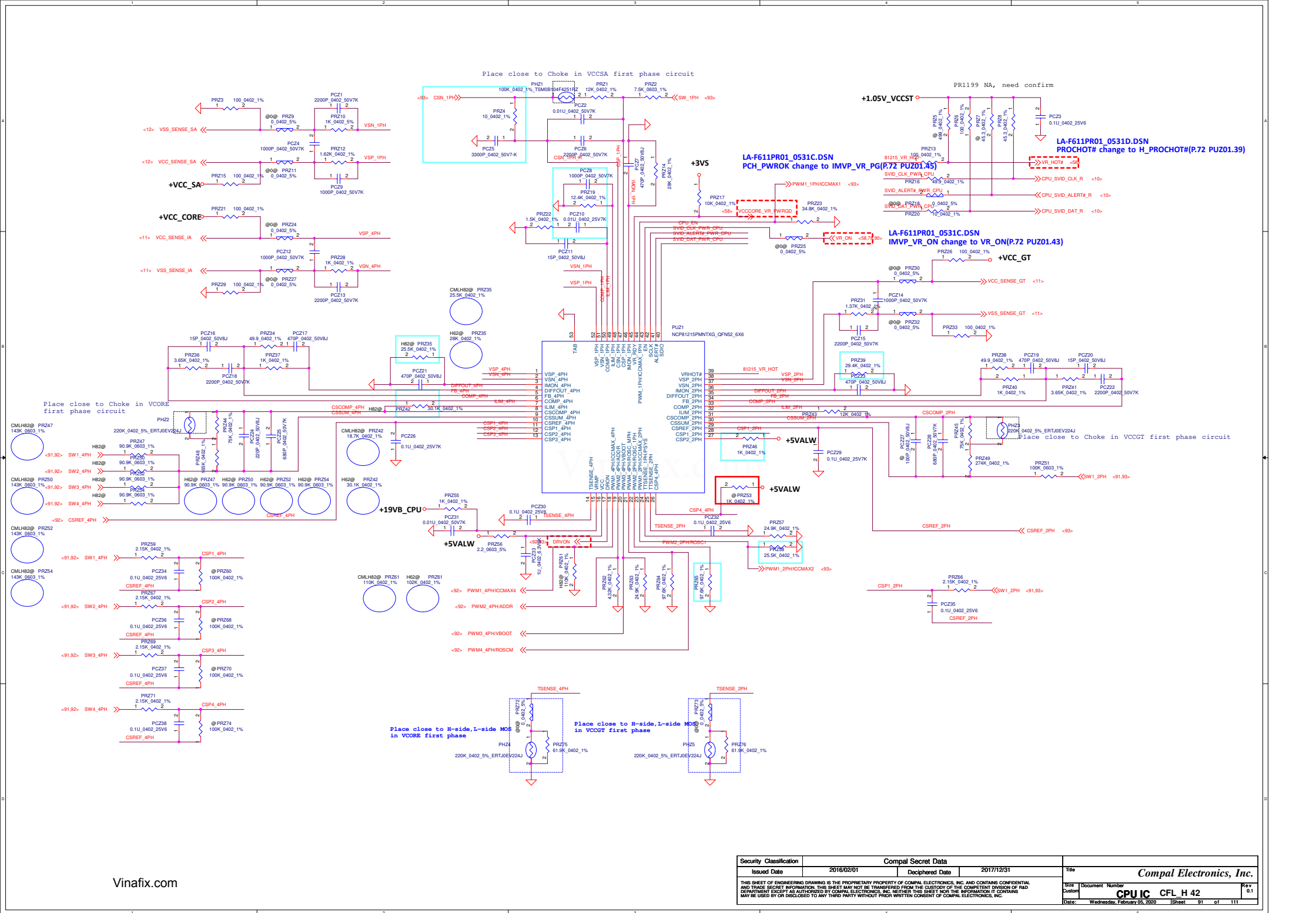
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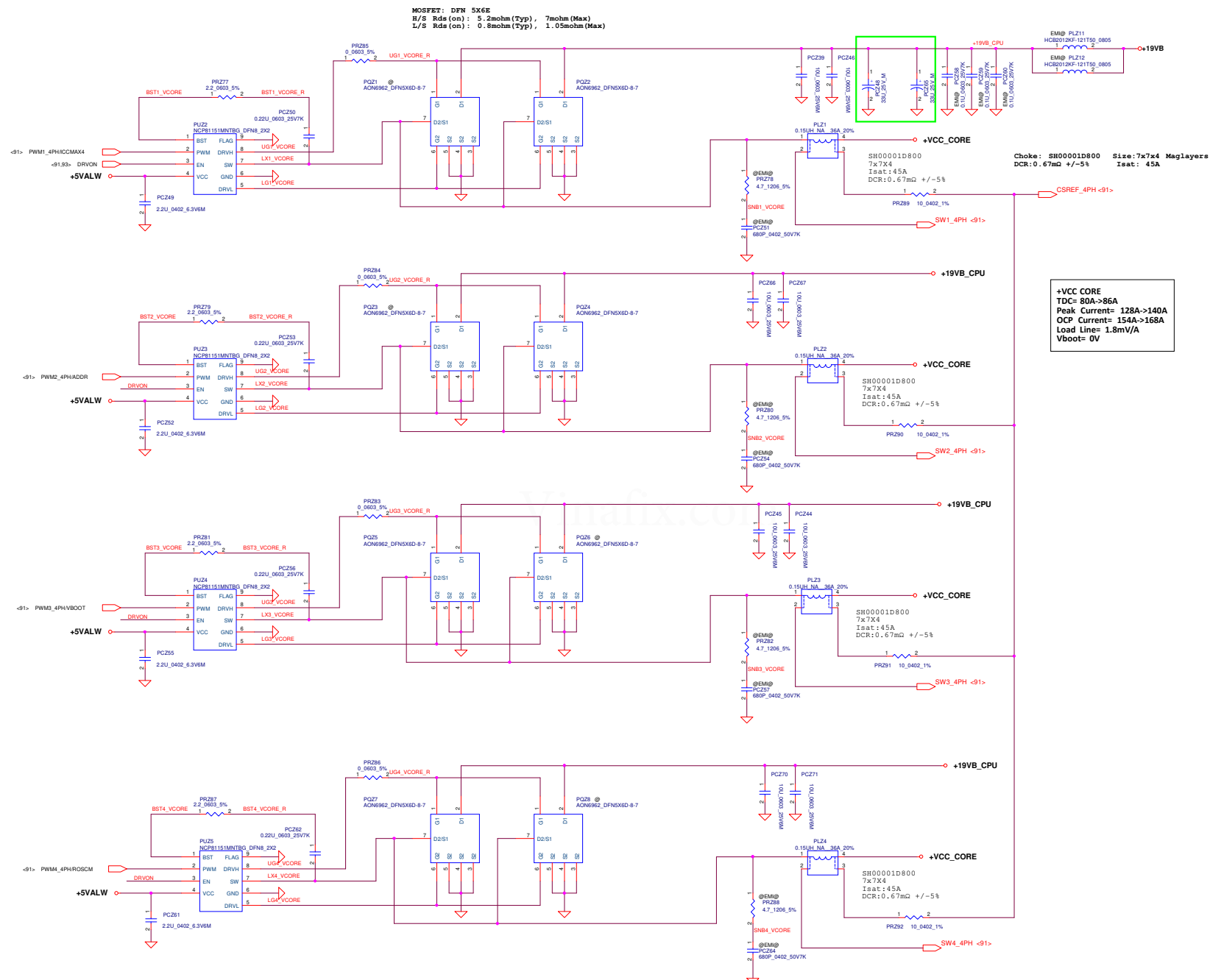
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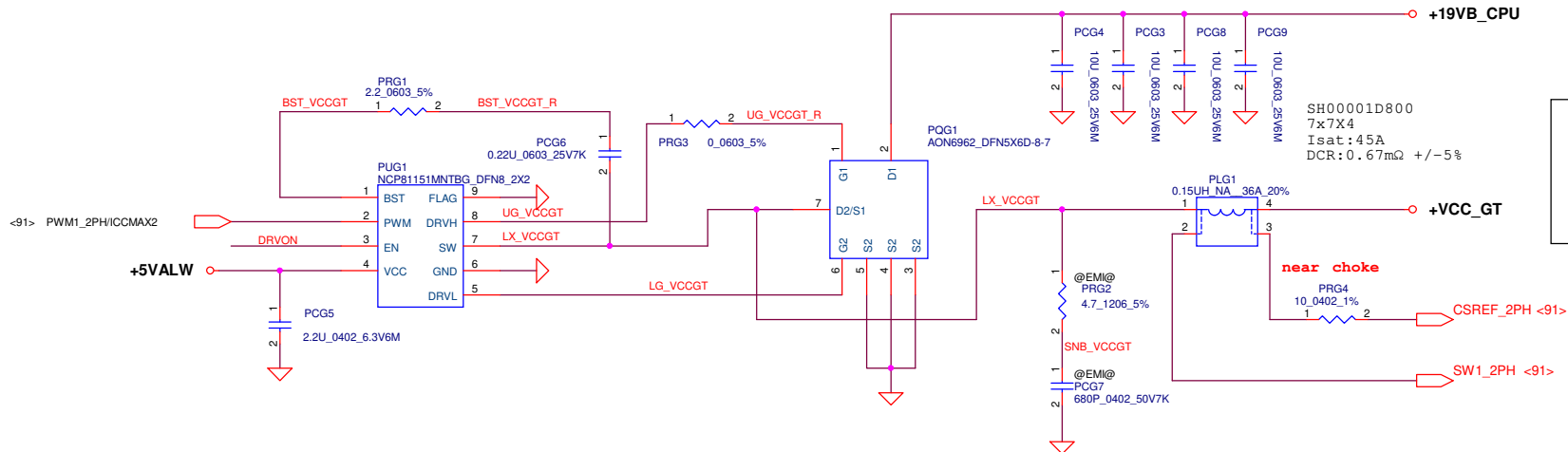
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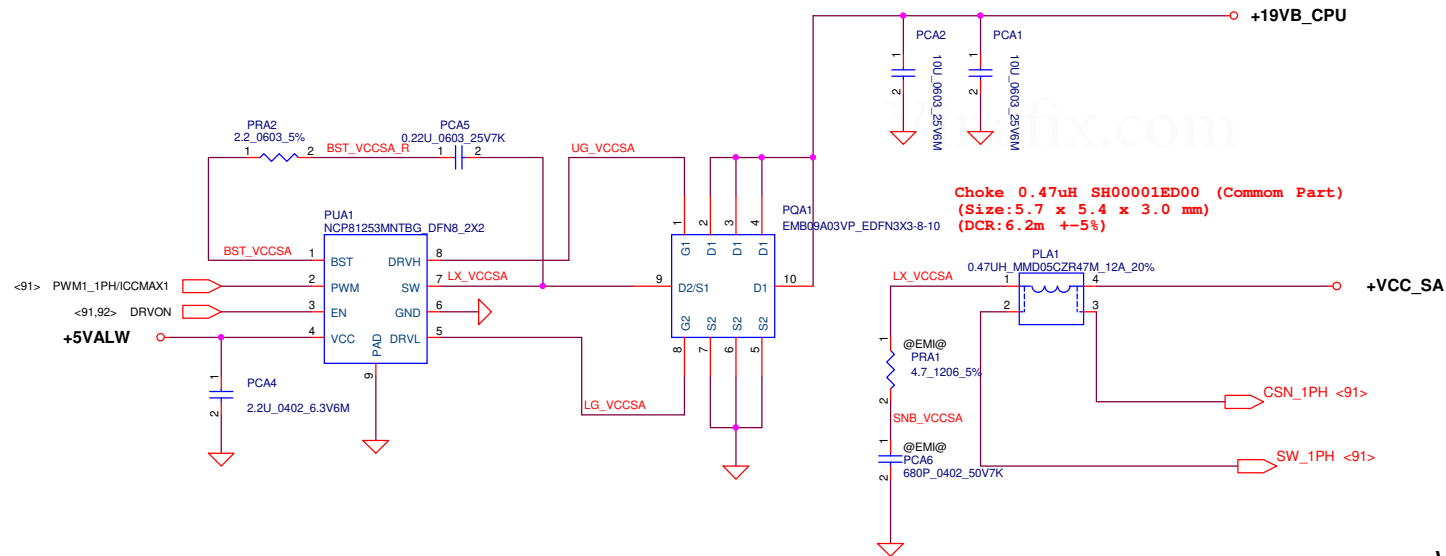




Main Func = VCCGT/+VCCSA



+VCCGT
TDC= 25A
Peak Current= 32A
OCP Current= 39A
Load Line= 2.7mV/A
Vboot= 0V



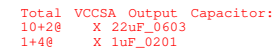
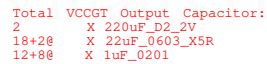
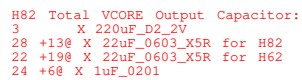
+VCCSA
TDC= 10A
Peak Current = 11A
OCP Current= 13A
Load Line= 10.3mV/A
Vboot= 1.05V

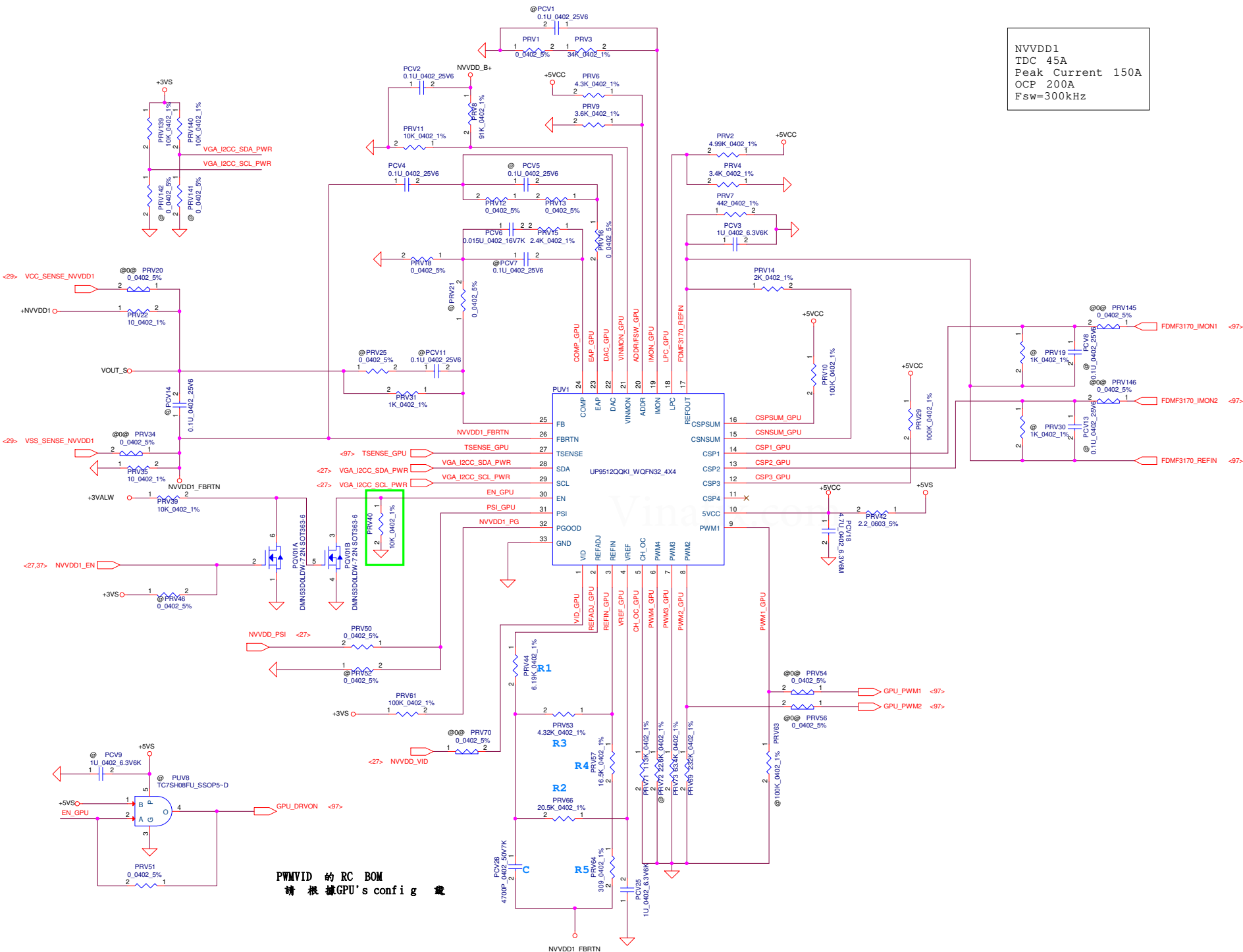
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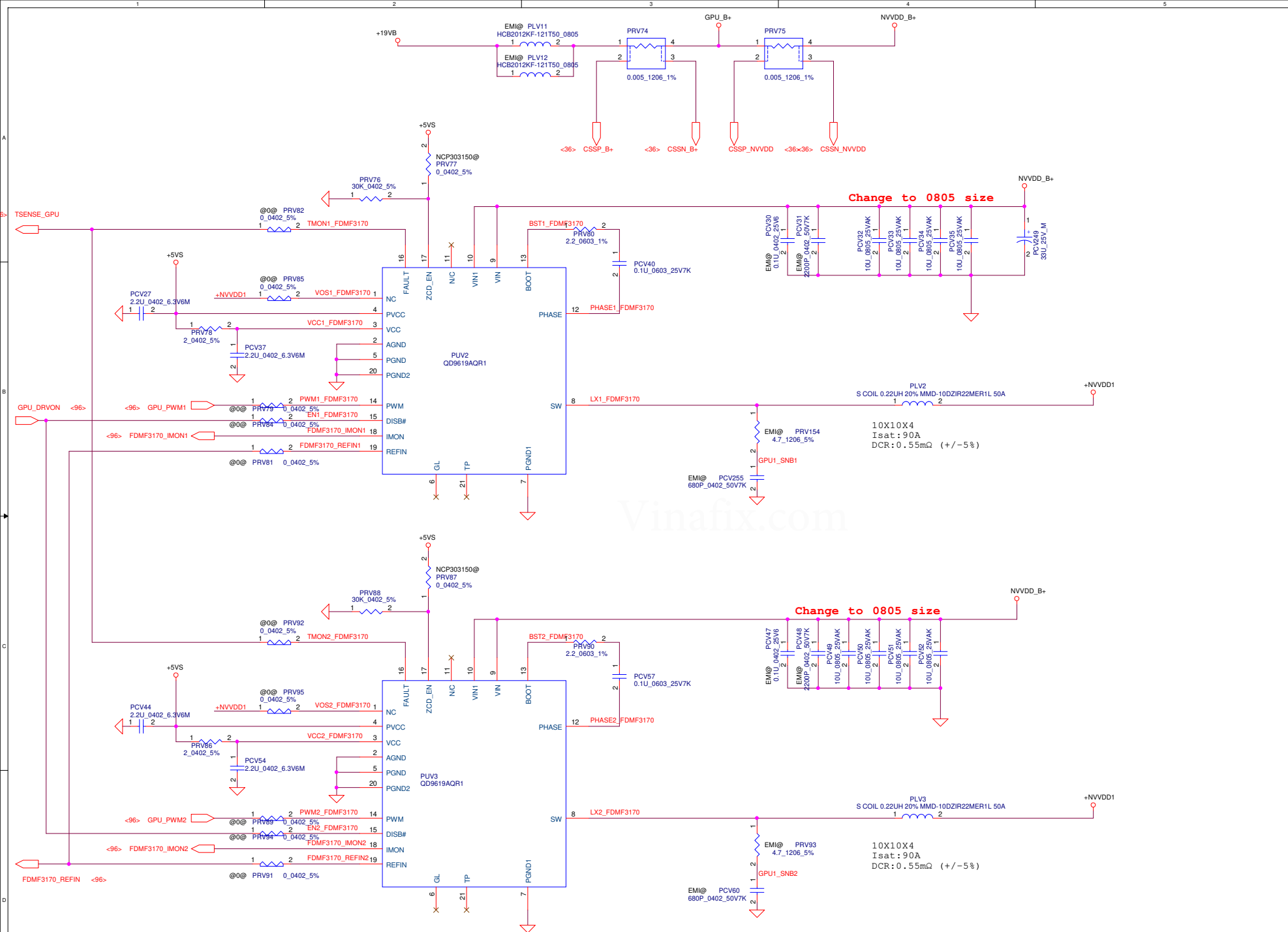
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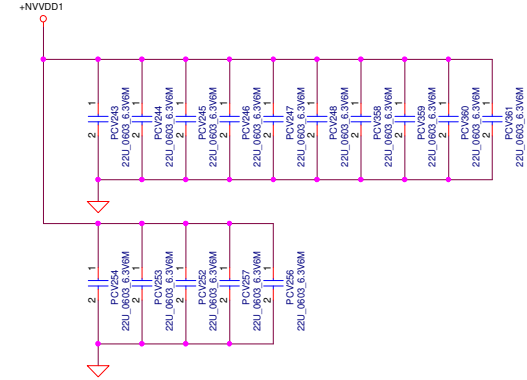
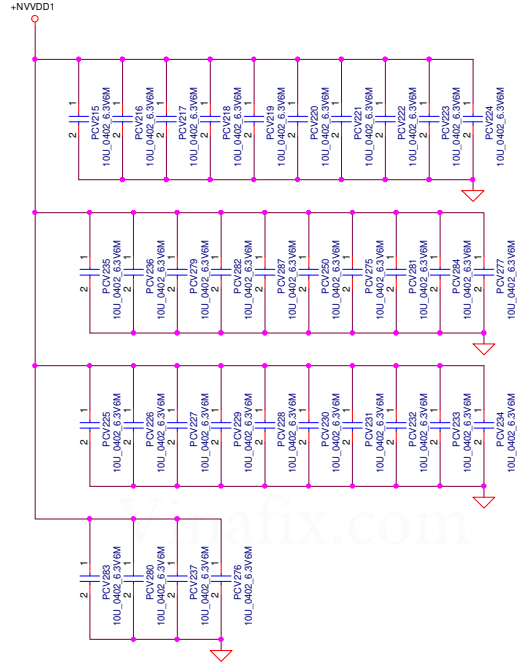
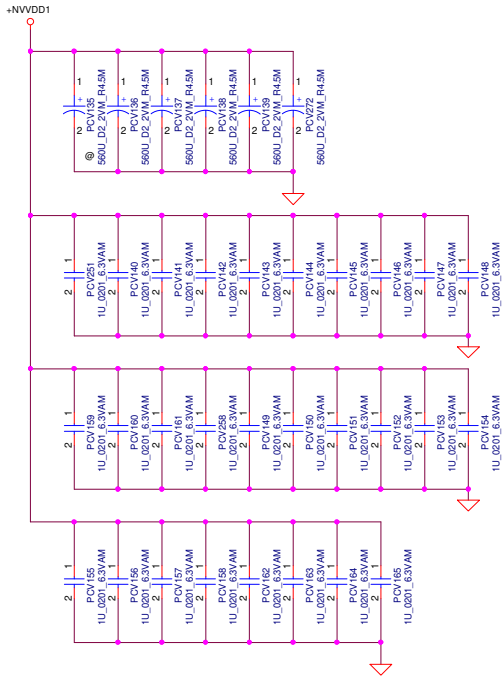
NVVDD1
TDC 45A
Peak Current 150A
OCP 200A
Fsw=300kHz

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Issued Date	2016/01/06	Deciphered Date	2017/01/06	Title	PWR_VGA_UP9512P
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+NVVDD
560uF X 5
22uF_0603 X 15
10uF_0402X 34
1uF_0201 X 28

Rail (GPU Ball) Name	Balls	Voltage	Filtering under GPU	Filtering Near GPU
GB4B-256 Package				
NVVDD		Varies	185 X 0.47uF (0201W X65) 23 X 10uF (0603 X65) 4 X 22uF (0805 X65) 3 X 47uF (0805 X65)	2 X 470uF (Poscap)
FBVDDQ (GPU side) ¹		1.25V 1.35V 1.5V 1.55V	48 X 0.47uF (0201 X65) 5 X 10uF (0603 X65)	7 X 10uF (0603 X65) 9 X 22uF (0603 X65)

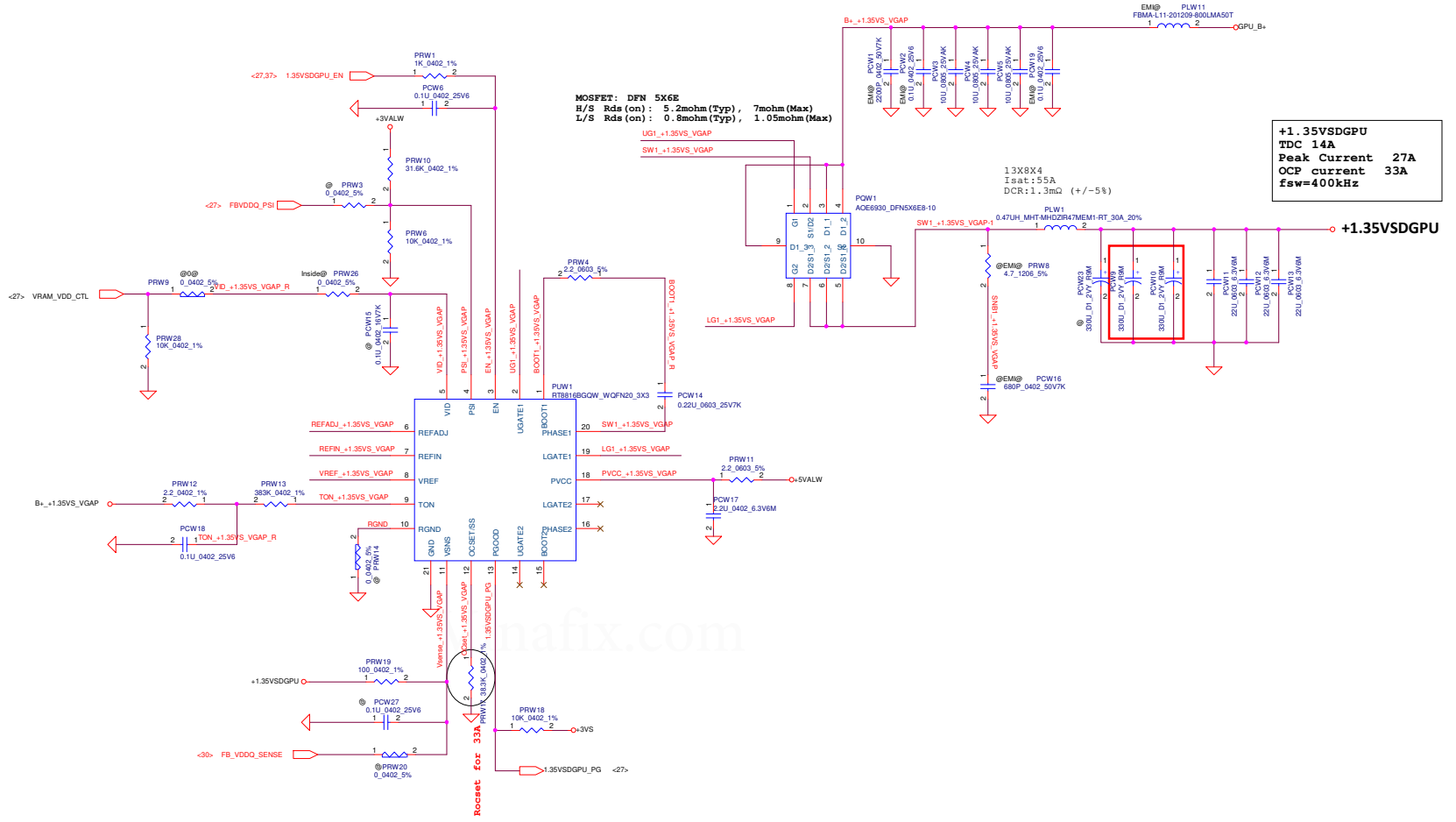
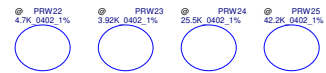
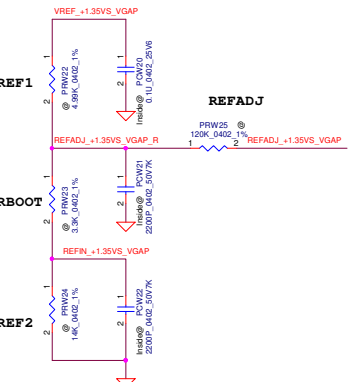


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Samsung & Micron VRAM
When, VRAM_VDD_CTL=High
Vboot=1.25V
When, VRAM_VDD_CTL=Low
Vboot=1.2V



+1.35VSDGPU
TDC 14A
Peak Current 27A
OCP current 33A
fsw=400kHz

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for PWR

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
01		Change P/N		Change PQM1 from SB000000U10(S TR EMB20N03V 1N EDFN ET88) to SB000000H800(S TR AON7408L 1N DFN) Change PQM2 from SB00001HV00(S TR EMB12N03V 1N EDFN3X3-8) to SB000010A00(S TR AON7506 1N DFN)	11/13	DVT
02		Sourcer request		Change PRB12 from to SD011100A80(S RES 1/4W 10 +-5% 1206) to SD002100A80 (S RES 1/8W 10 +-5% 0805)	11/13	DVT
03		Sourcer request		Change PCB17 from SE00000WP00(S CER CAP 2.2U 25V K X5R 0603) to SE000006S80 (S CER CAP 2.2U 16V K X5R 0603)	11/13	DVT
04		Sourcer request		Change PCB20 from SE024101J80(S CER CAP 100P 50V J NPO 0603) to SE071101J80(S CER CAP 100P 50V J NPO 0402)	11/13	DVT
05		Customer request		Add PCB21 SE071101J80(S CER CAP 100P 50V J NPO 0402)	11/13	DVT
06		Sourcer request		Change PCB1 from SE025102K80(S CER CAP 1000P 50V K X7R 0603) to SE074102K80(S CER CAP 1000P 50V K X7R 0402)	11/13	DVT
07		Sourcer request		Change PC102 SE071101J80(S CER CAP 100P 50V J NPO 0402) to SE00000SE00 (S CER CAP 100P 50V J NPO 0201)	11/13	DVT
08		Vendor request		Change PUZ1 from SA0000AQE00(S IC NCP81215MNTXG QFN 52P PWM) to SA0000CTW00(S IC NCP81215PMNTXG QFN 52P PWM)	11/13	DVT
09		Base on CPU transient result		Change PCA103 & PCA108 to un-mount Change PCA109 & PCA111 to mount	12/02	DVT
10		Base on CPU transient result		CML H82 SKU delete PCZ104,PCZ105,PCZ107,PCZ108,PCZ111,PCZ113,PCZ114,PCZ116,PCZ118,PCZ120,PCZ123,PCZ124,PCZ126, PCZ127,PCZ134,PCZ135,PCZ136,PCZ137,PCZ138(22U_0603_6.3V6M * 19pcs)	12/02	DVT
11		Base on CPU transient result		CFL H62 SKU delete PCZ101(330U_D1_2VY_R9M)	12/02	DVT
12		For PQ310 protect		Add PRB36,PRB37,PRB38(O_0402_5%,SD028000080)	12/17	PVT

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02						
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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
01			11/13	Sourcer request	1. Change CA26,CB5,CB6,CB9,CH9,CH51,CM16 from 0402 to 0201 size. 2. Change CG335,CG336,CS129,CS130 from SE082221J80 to SE074221K80. 3. Change DL1 to SCA00001A00. 4. Change CD10 from SE00000TB00 to SE00000SE00. 5. Change UH3 to SA0000BIP00. 6. Change UG28 to SA0000BJI00. 7. Change DS1,DS3,DS4,DS5,DS6,DS20 to SC300001Y00.	DVT	1.0
02	16,58	WLAN (BT_ON)	11/13	BT_ON co-lay by EC/PCH	1. Change TP_INT# connection to UH1.BC33. 2. Add RH262 for BT_ON to UH1.BF32. 3. Add RB79 for BT_ON_R.	DVT	1.0
03	58	EC	11/20	Pin definition sync.	1. Remove Thermal_ALERT# net. 2. Change EC_PME# connection to UB1.106. 3. Add IDCHG net to UB1.76. 4. Remove RB78 and TURBO_EN# net. 5. THERMAL1_ALERT# change connection to UB1.36. 6. TYPEC_EN change connection to UB1.68. 7. LAN_PWR_EN change connection to UB1.91. 8. Change RB3 to 750k for EC board ID.	DVT	1.0
04	15,52	CNVI	11/20	by intel review.	1. Change RM36,RM37,RH181,RH182 from 0402 to 0201 size. 2. Add RM51,RM52 for CNVI topology.	DVT	1.0
05			12/17	Design change.	1. Change RM46,RL2,R18 to R-short.	PVT	1A
06	58	EC	12/17	EC board ID.	1. Pop RB3.	PVT	1A
07	63	TP	12/24	ESD request.	1. Add CK6.	PVT	1A
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