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6	CPU-Power
7	CPU-GND
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10	PCH-DMI/PCIE/USB/SATA/DDI
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12	PCH-Power
13	PCH-GND
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Q470/H470 Version : 1.2

CPU :

Intel Comet Lake-S

System Chipset :

Intel Comet Lake-H Chipset

On Board Chipset :

IMVP8 -- NCP81220 4+1 Phase

Gigabit LAN -- INTEL-I219LM Co-LAY RTL8111K

HDA Codec -- Realtek ALC623

Super I/O --NCT6686D-L

SPI Flash 256Mb

Main Memory :

2 Channel DDR 4 * 4 (Max 128GB)

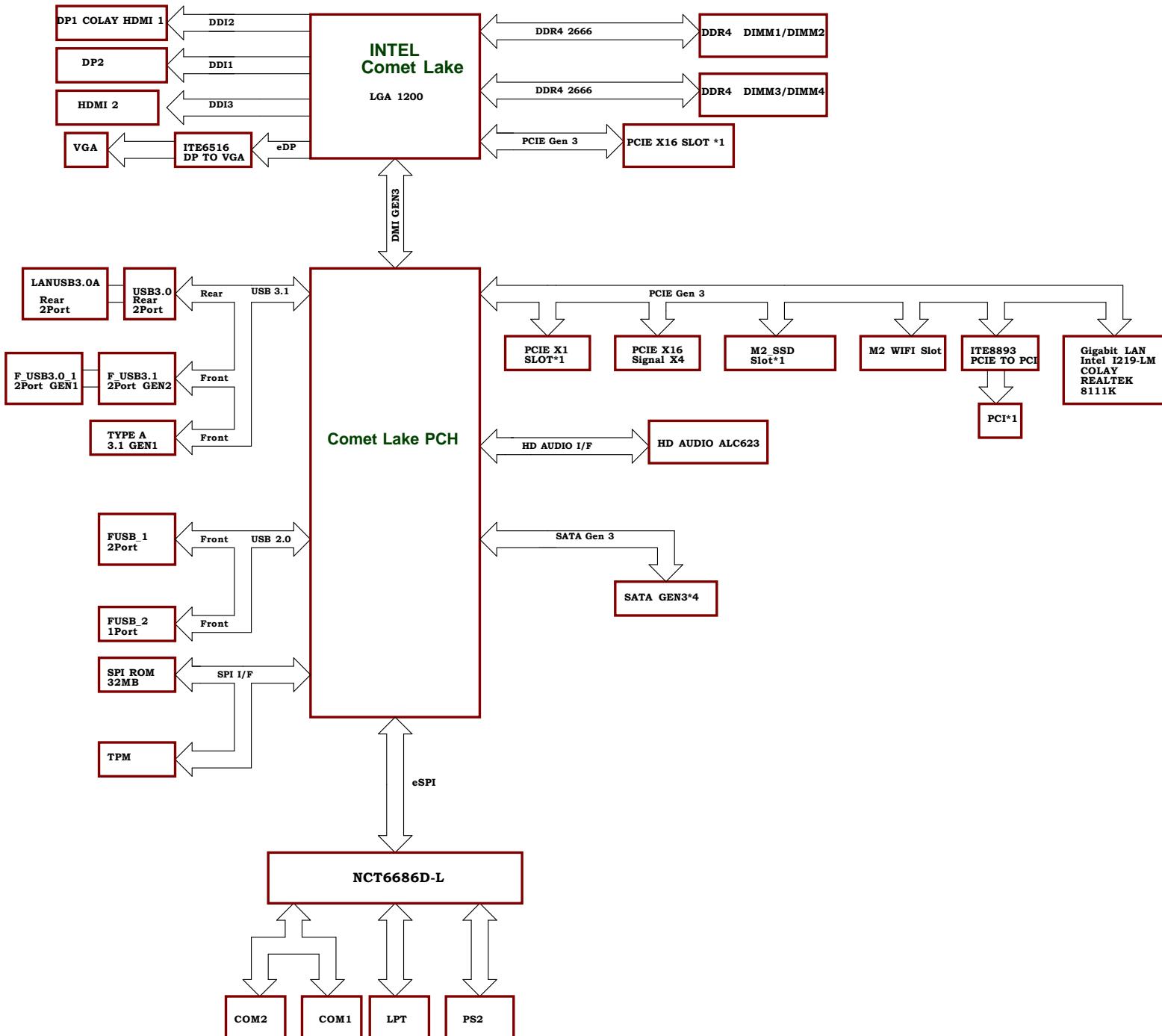
Expansion Slot :

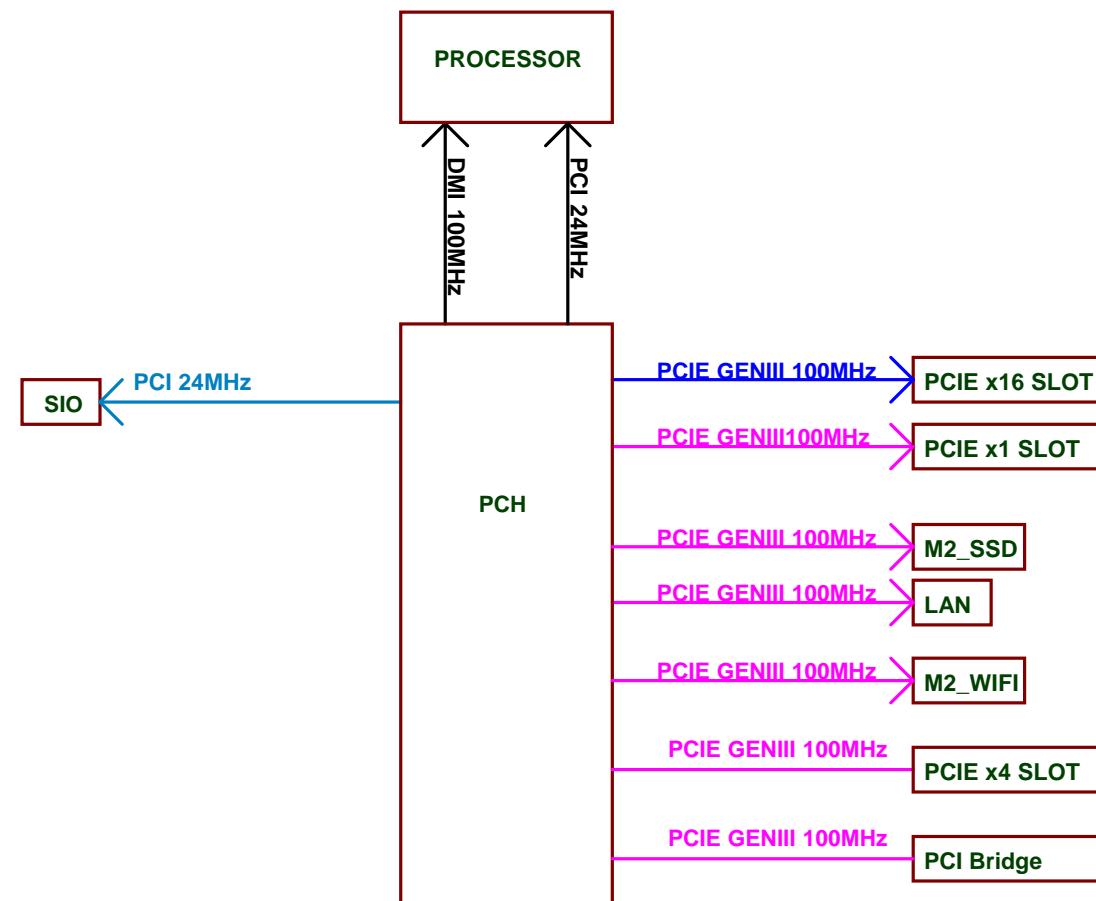
PCI Express x16 Slot * 1

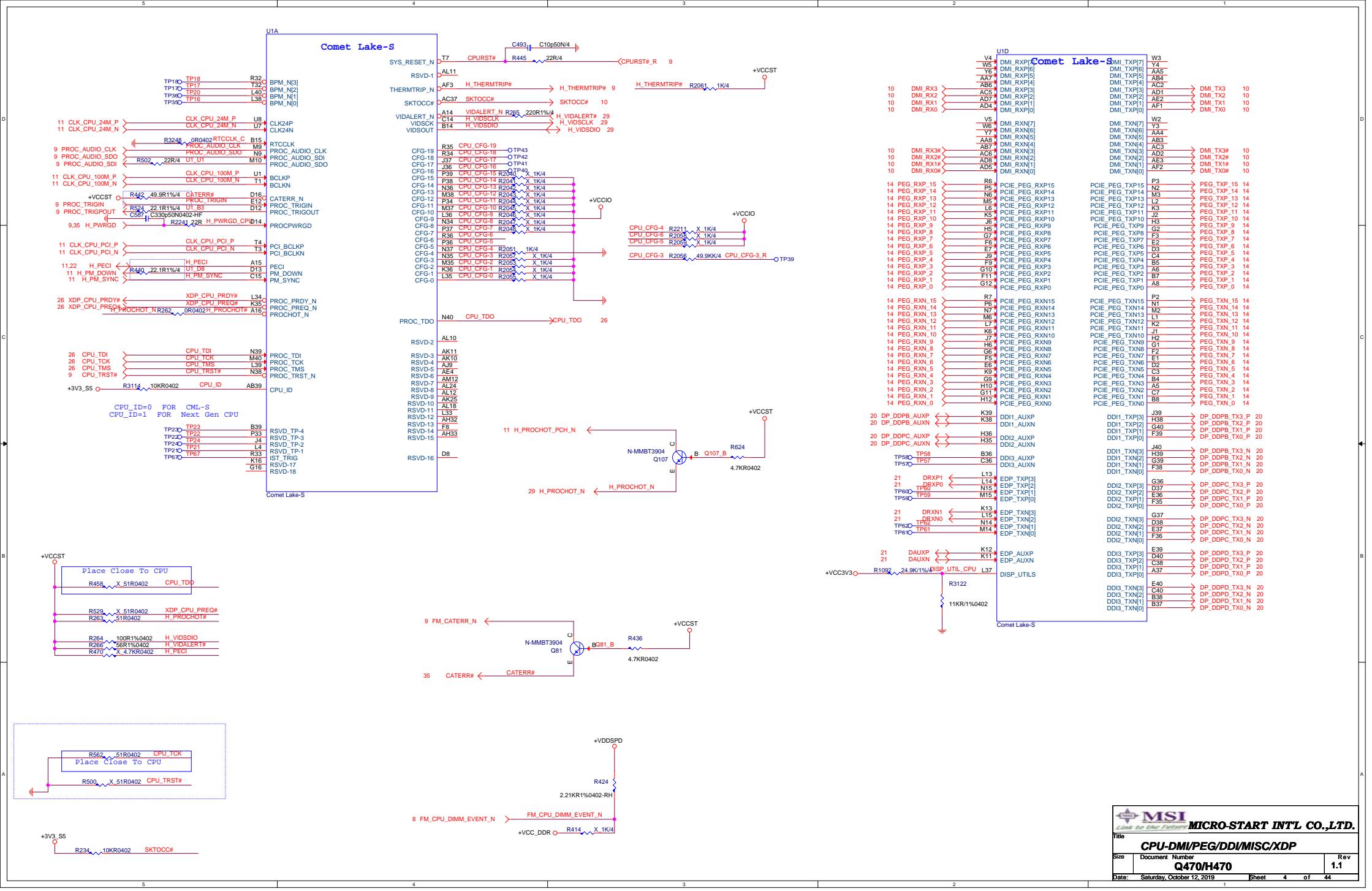
PCI Express x4 Slot * 1

PCI Express x1 Slot * 1

PCI SLOT * 1



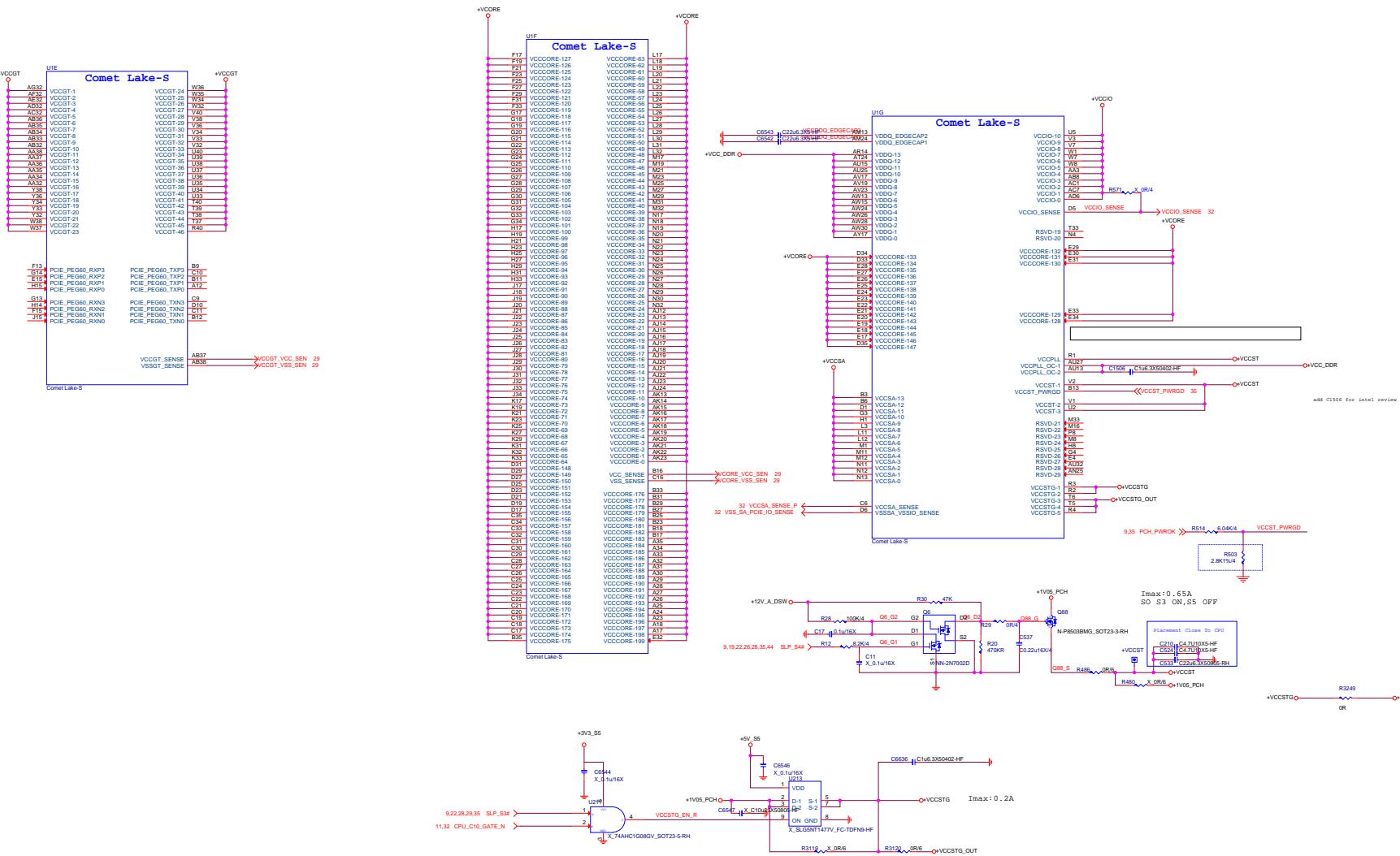


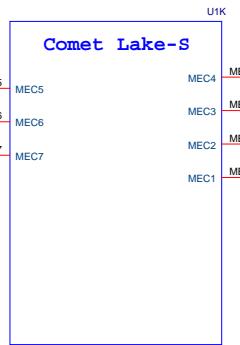
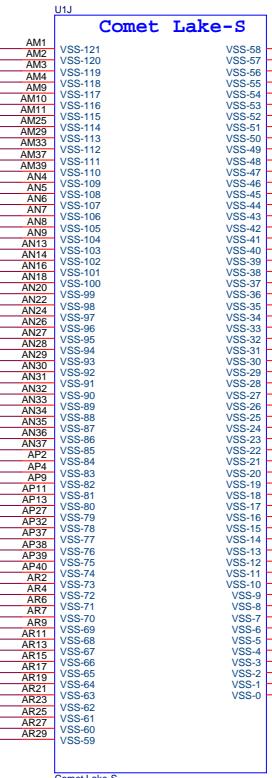
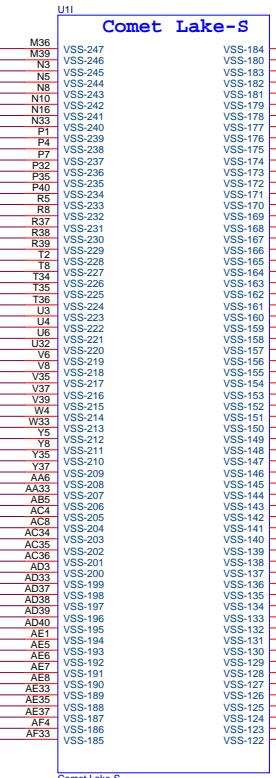
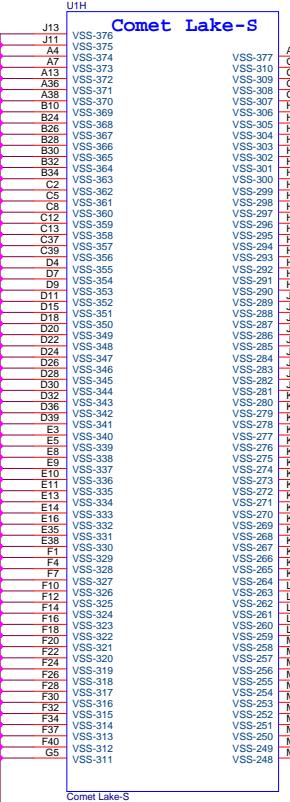




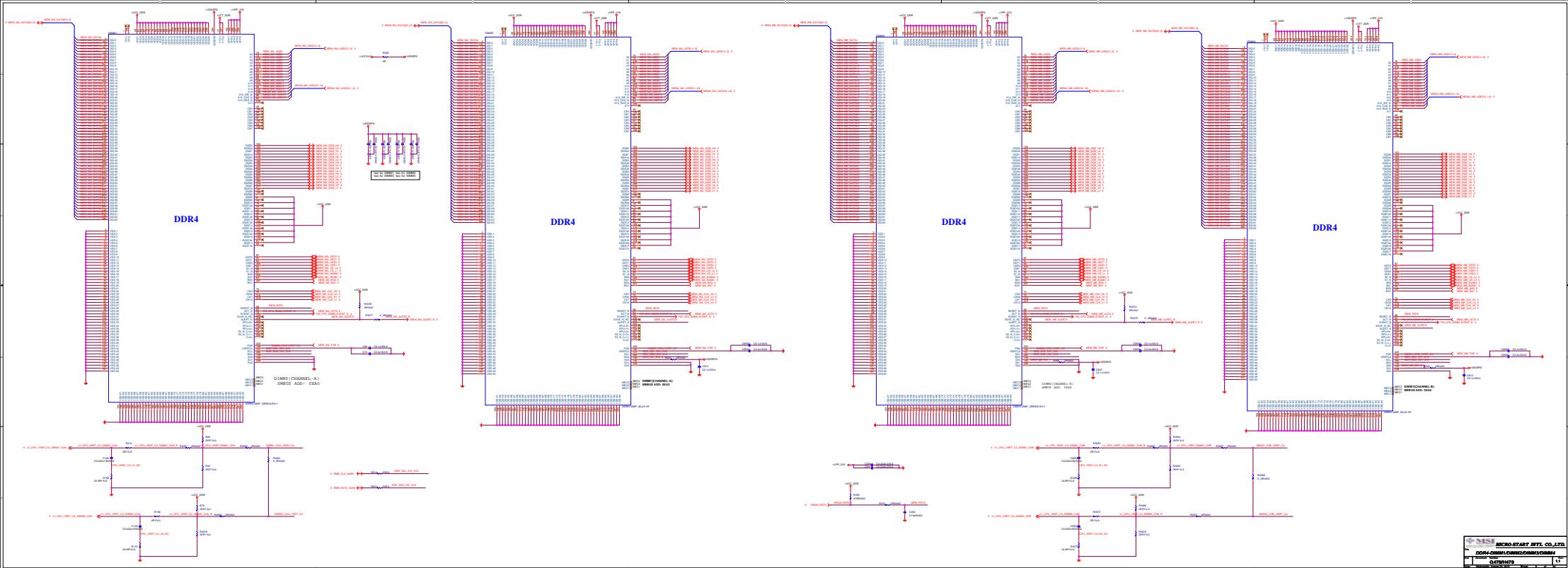
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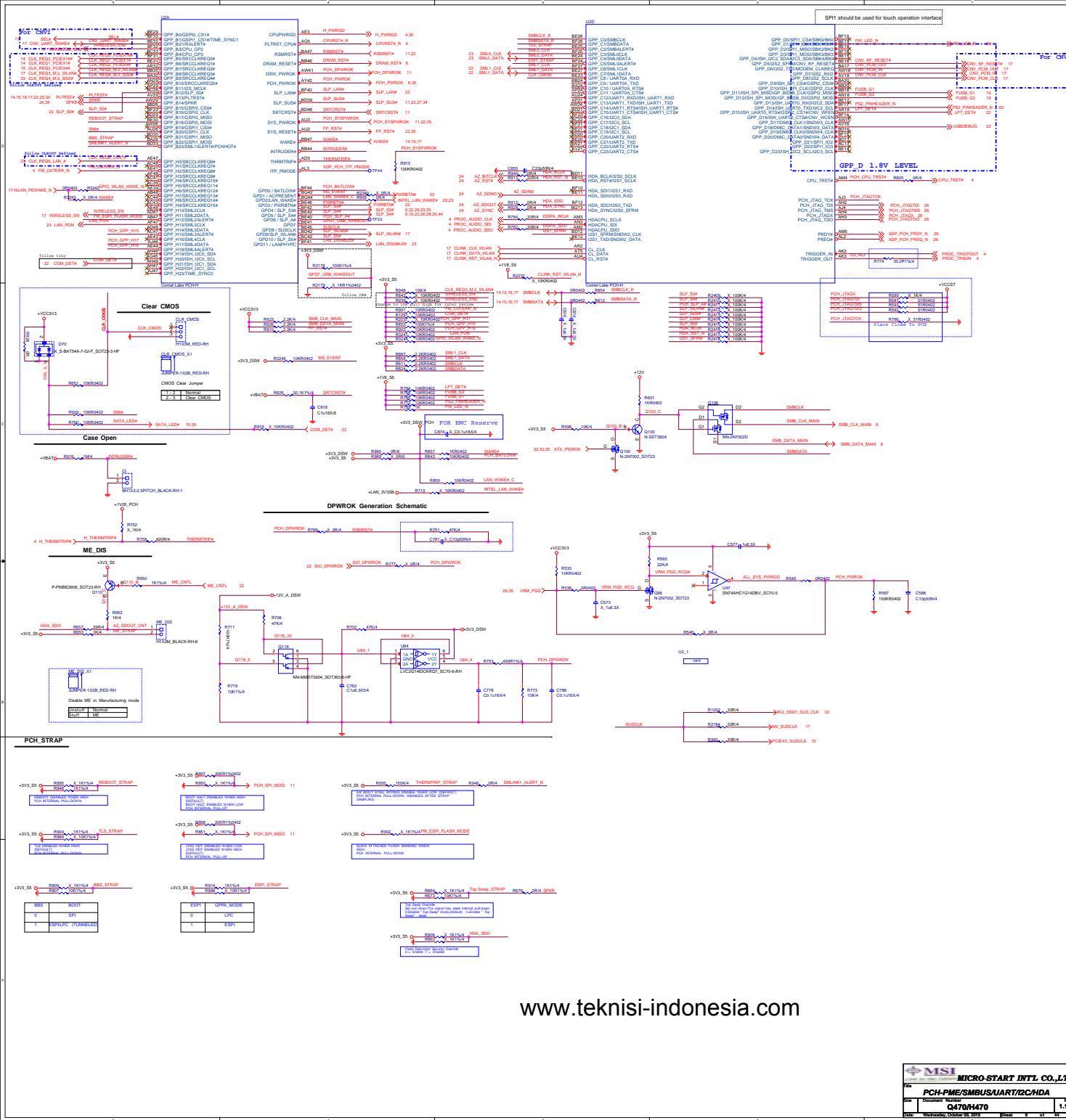


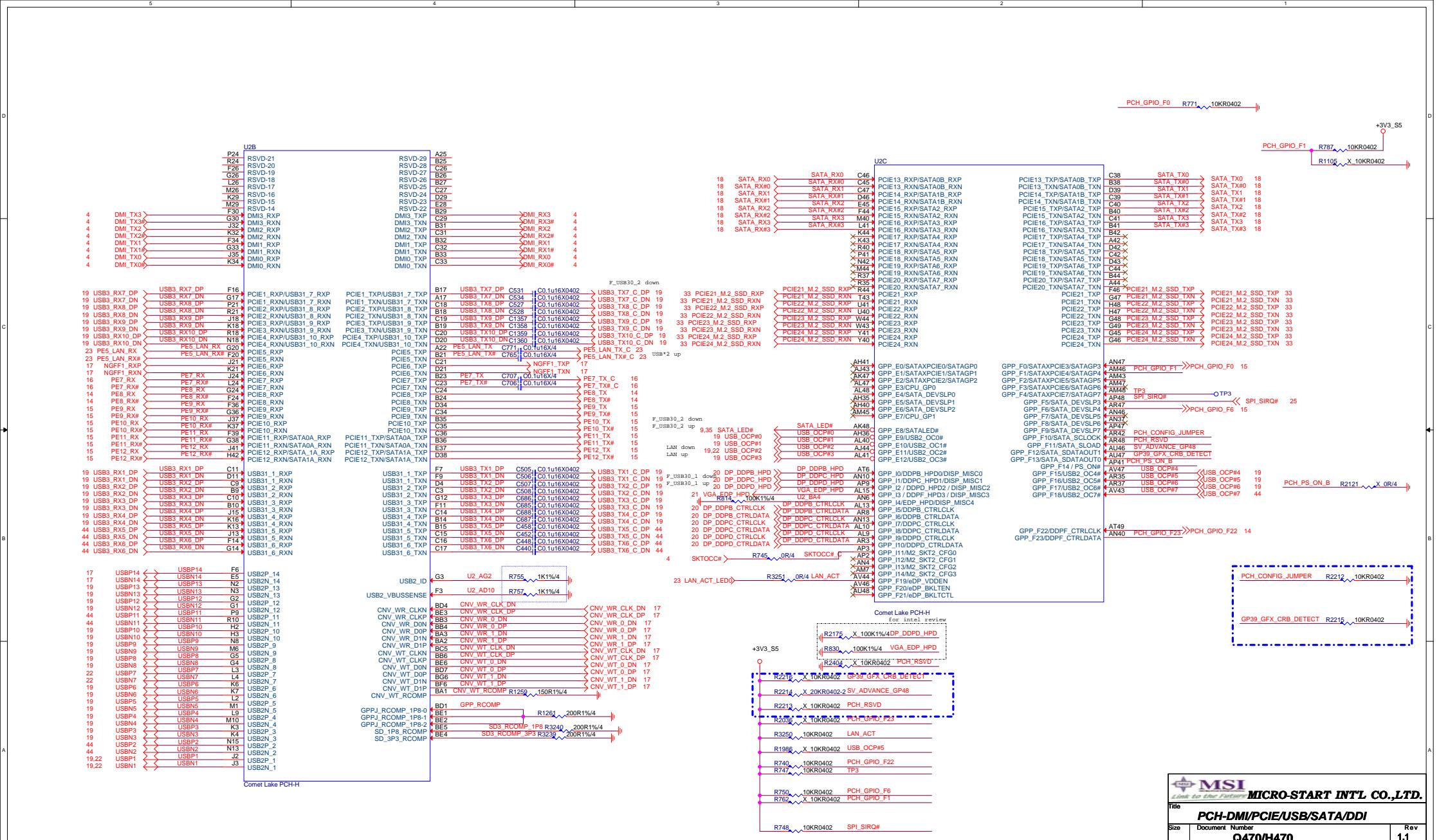


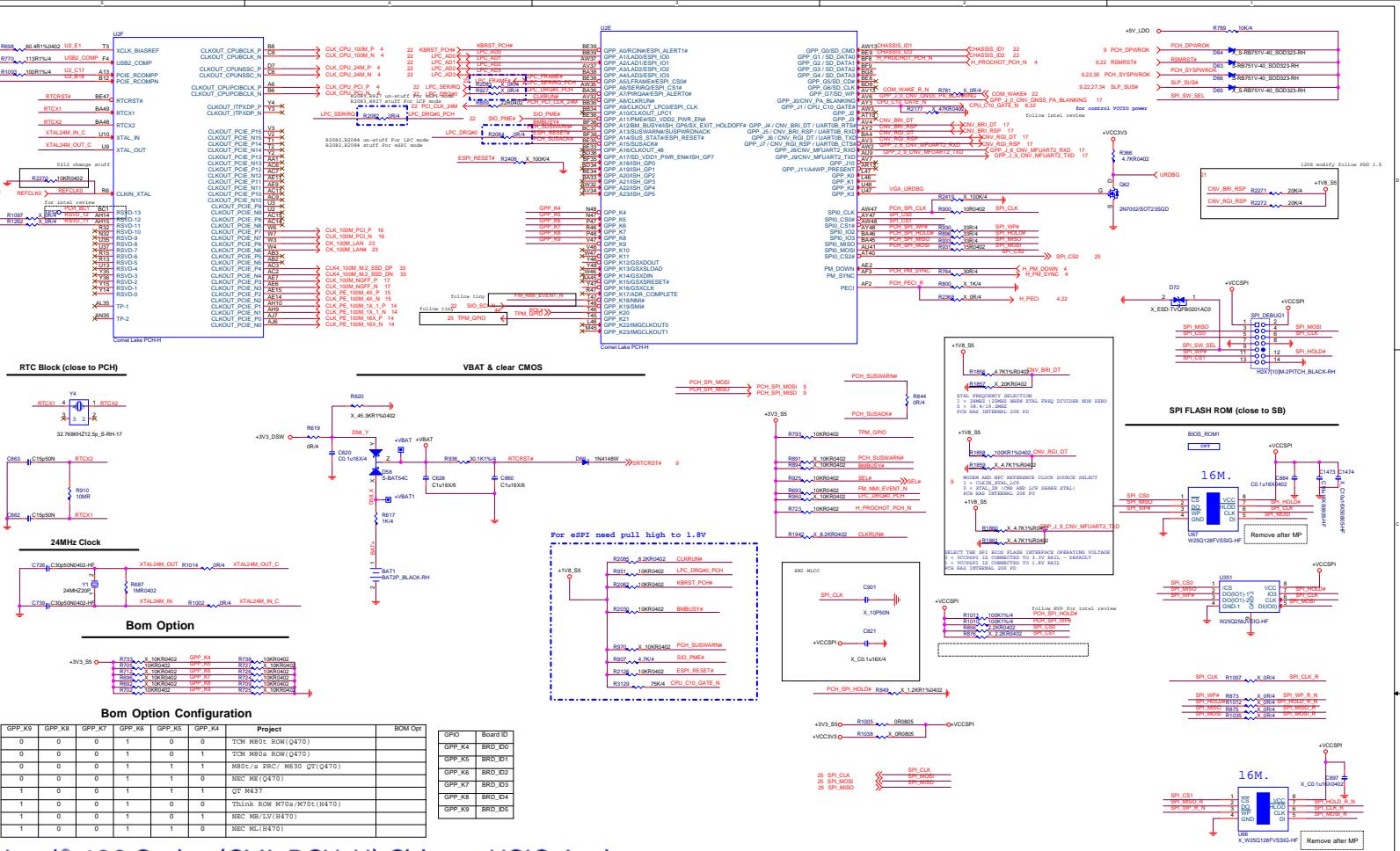


Comet Lake-S





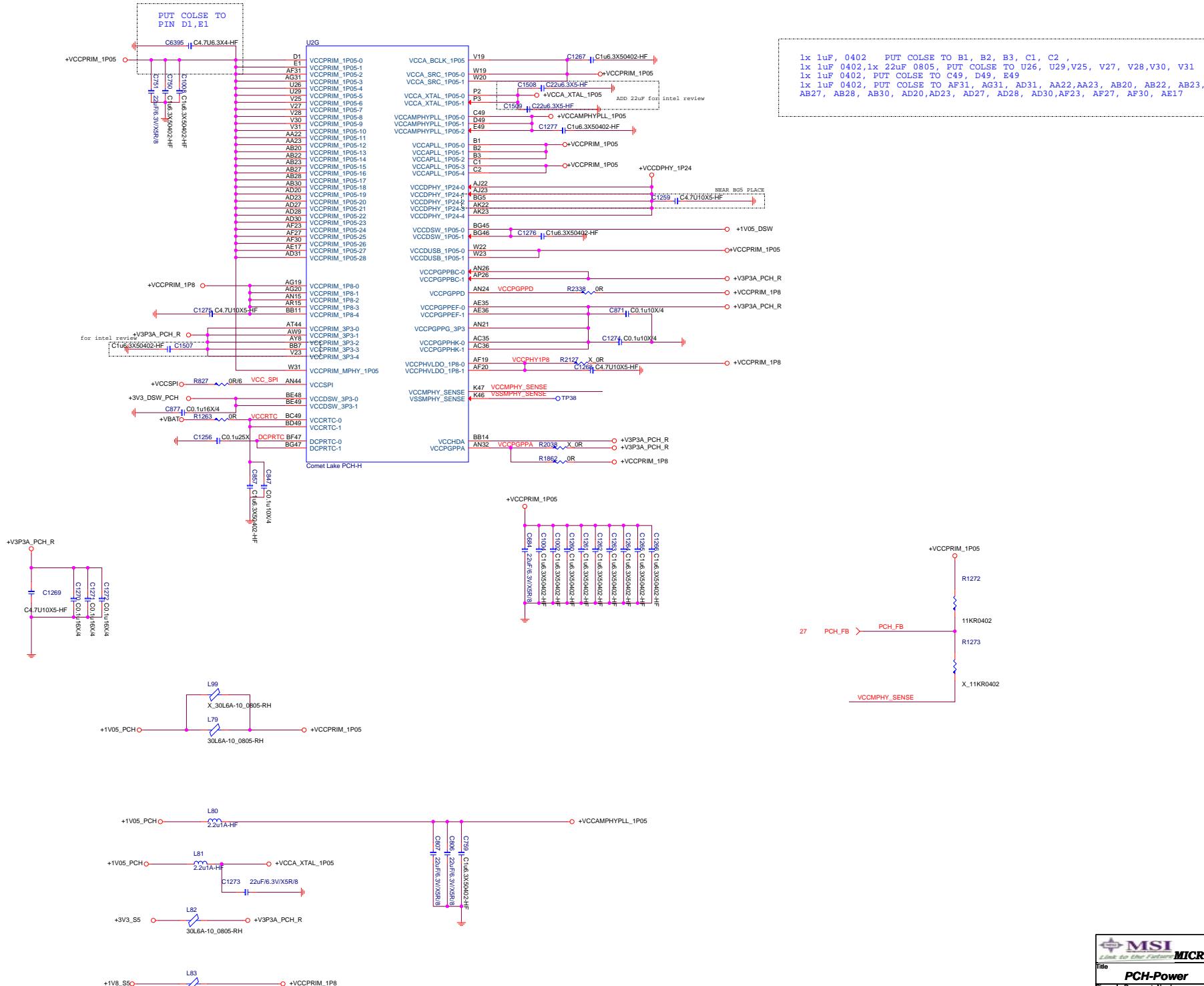


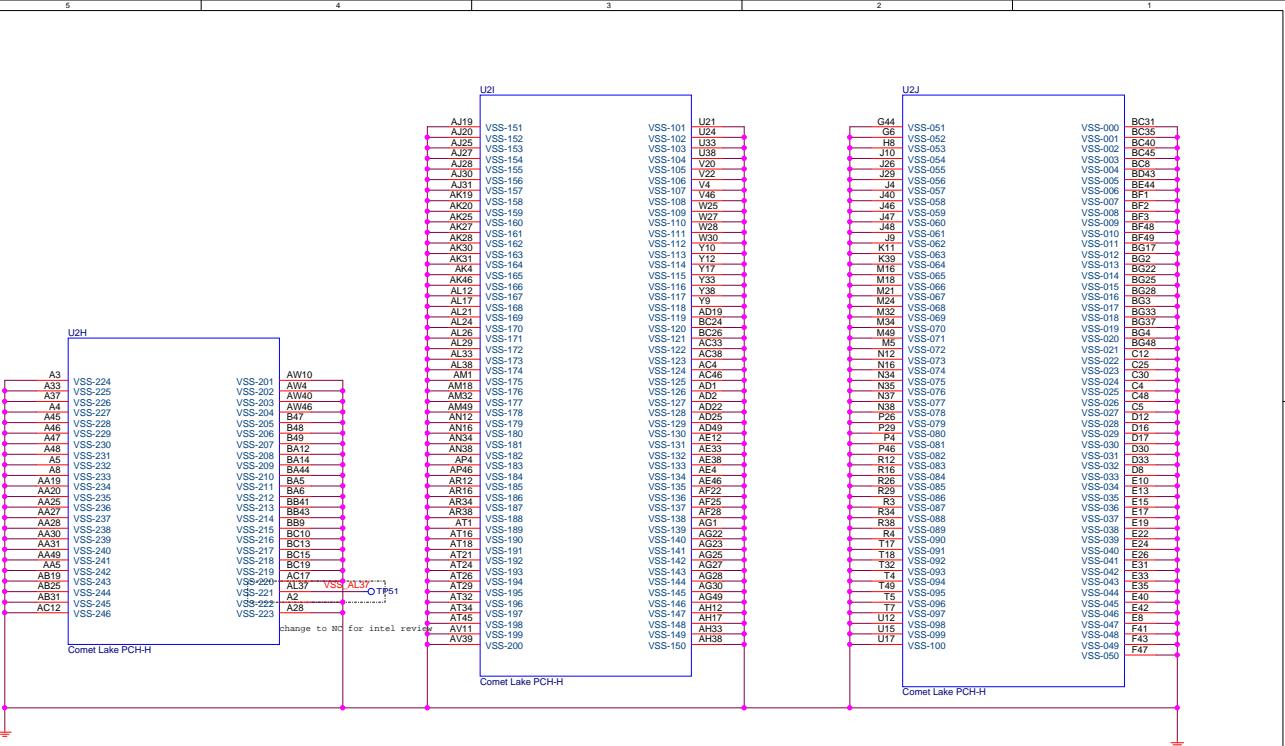


Intel® 400 Series (CML PCH-H) Chipset HSIO Assignments

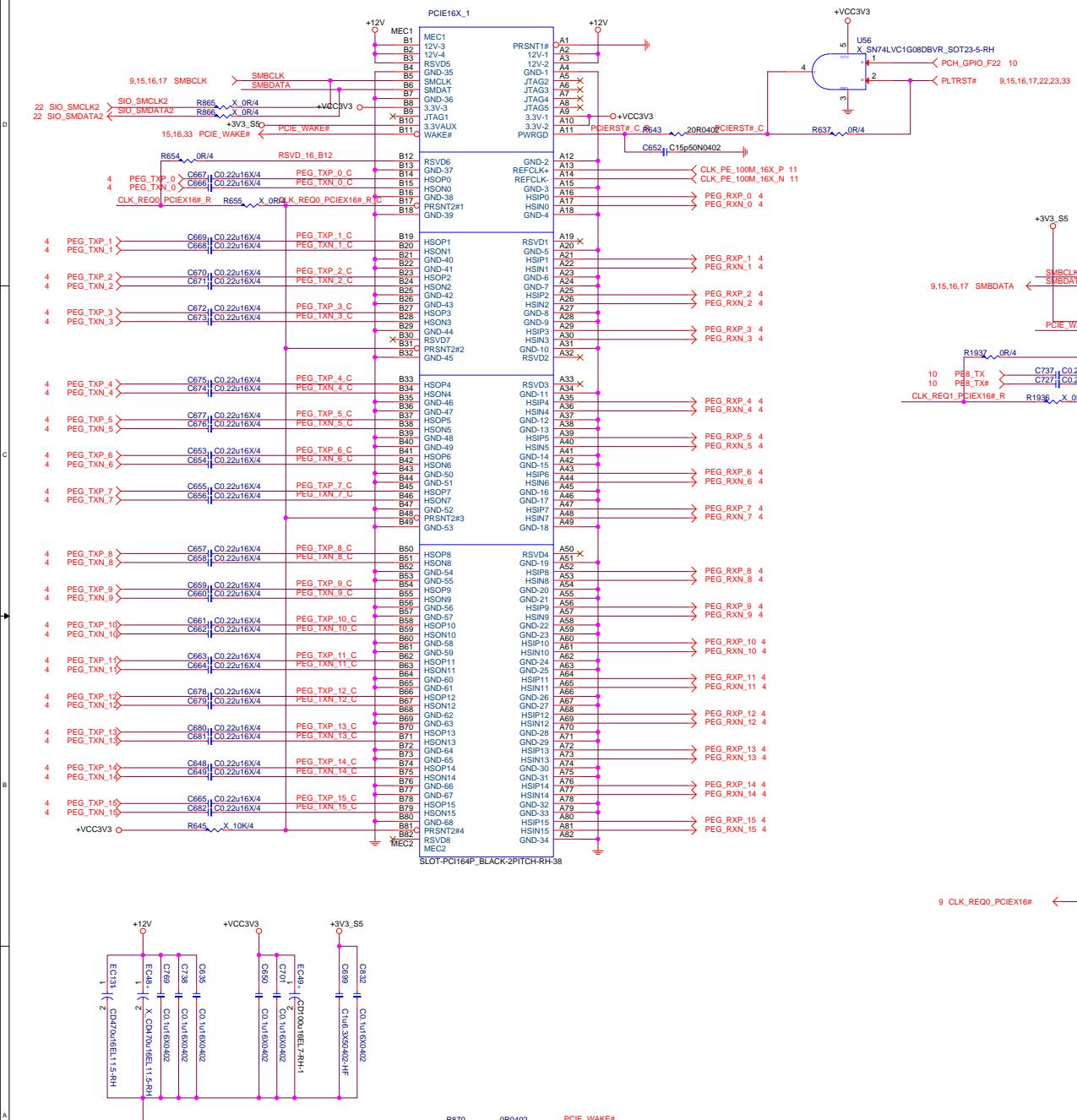
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	PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2	
U470	PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2	
Z490	PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2	
U480	PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2	
	1) SATA #0/#1 can be configured to PCIe Ports 11/12 or 13/14.																											

	No Remapping				No Remapping				PCIe Storage				No Remapping				PCIe Storage				PCIe Storage							
	PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2	
U470	PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2	
Z490	PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2	
U480	PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2		PCIe Gen 1		PCIe Gen 2	
	1) SATA #0/#1 can be configured to PCIe Ports 11/12 or 13/14.																											



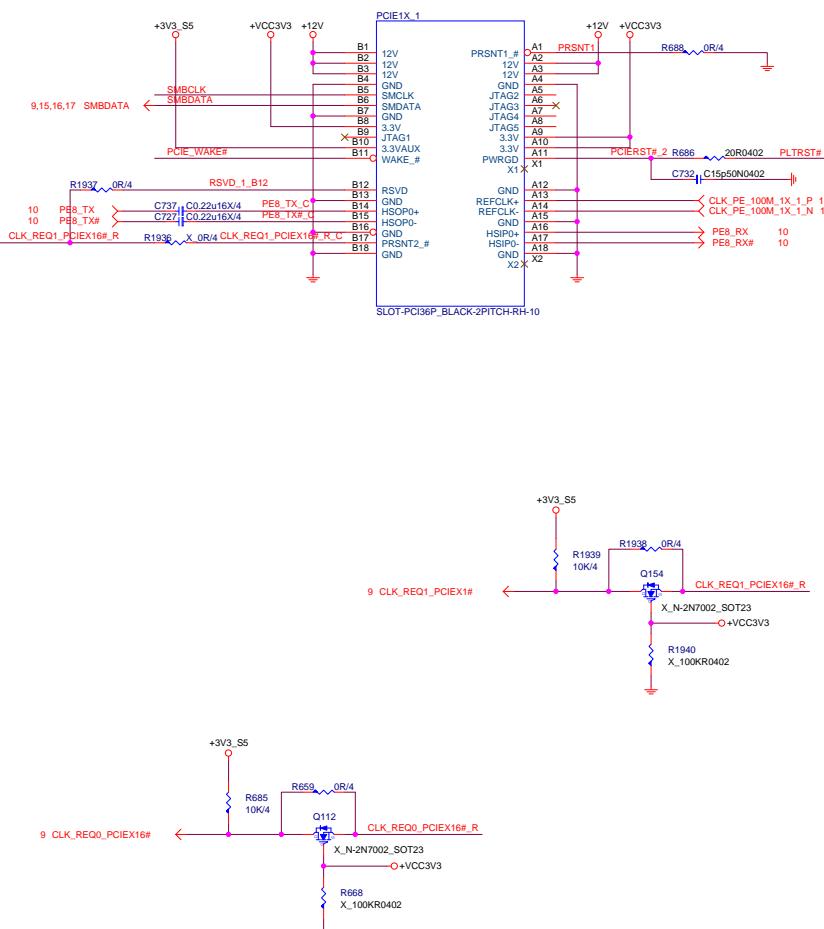


PCI EXPRESS X16 SLOT

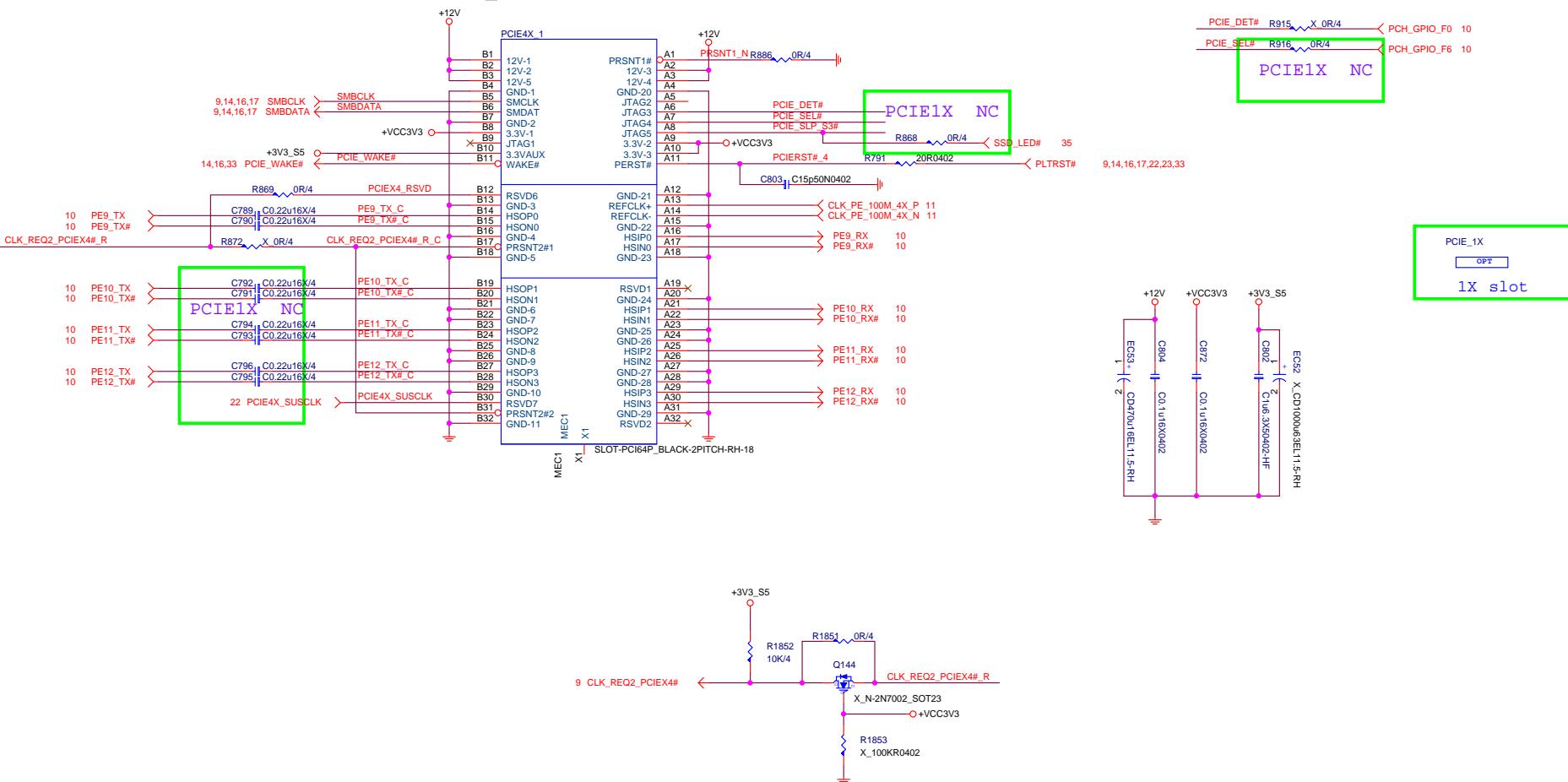


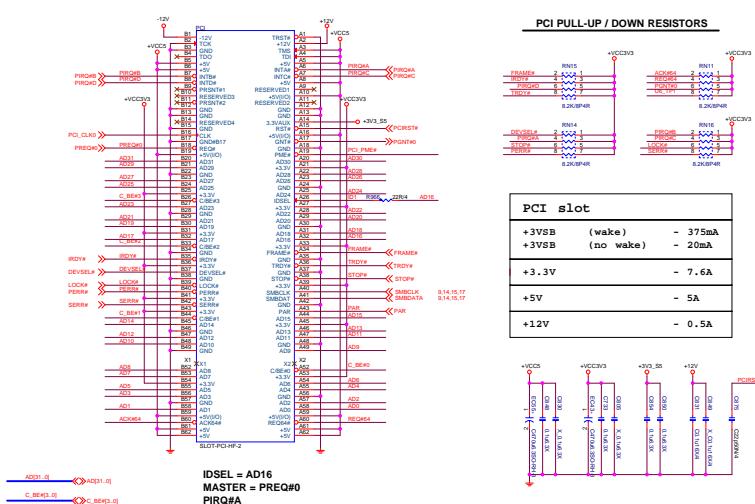
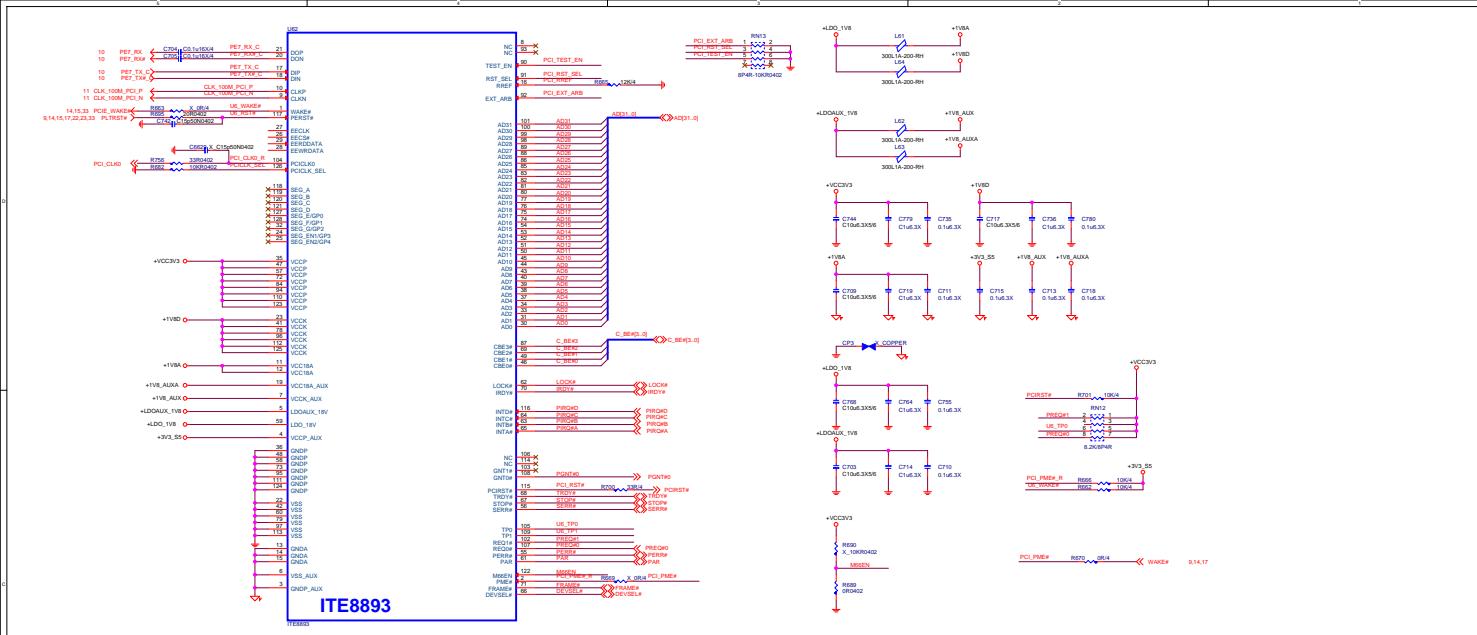
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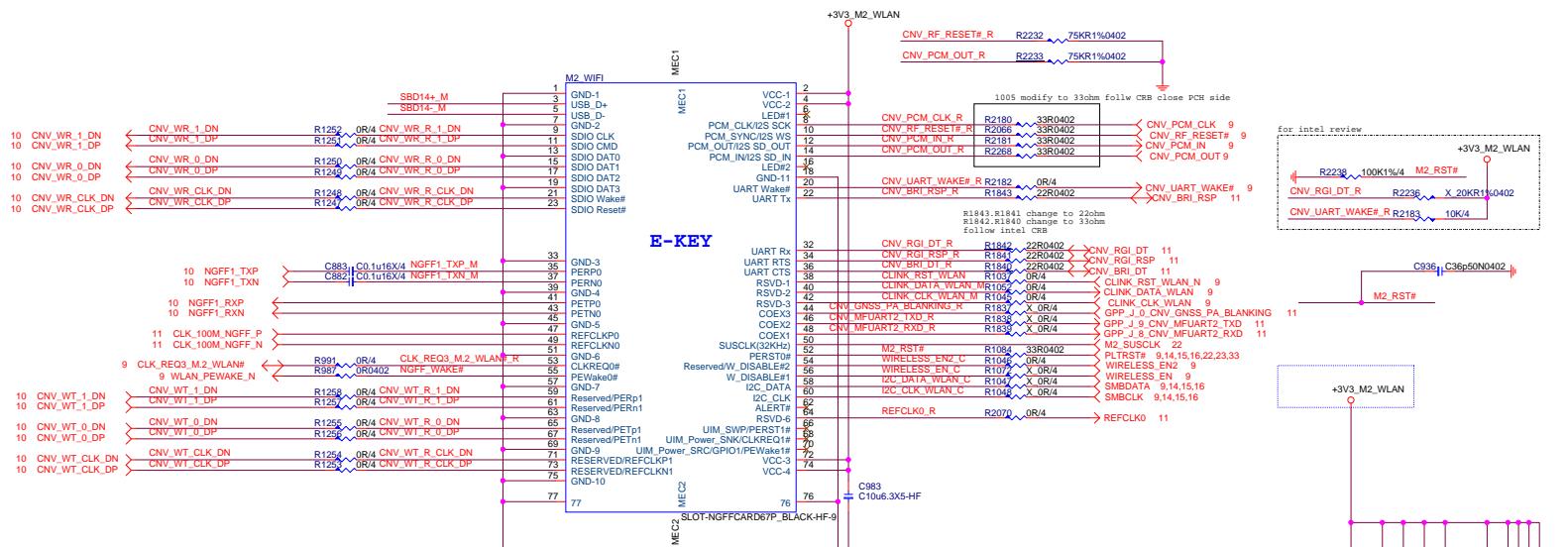
PCI EXPRESS x1-PORT



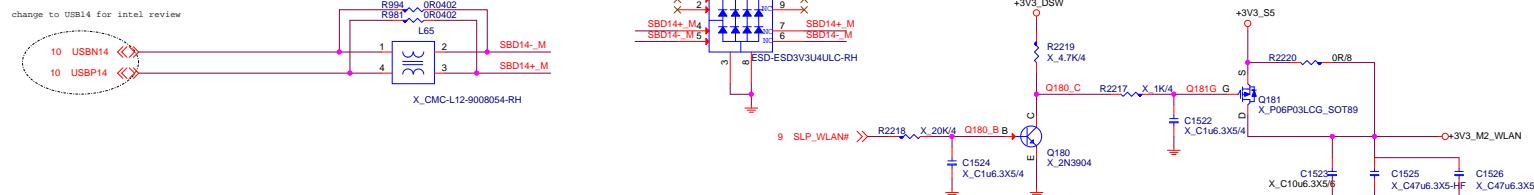
PCI EXPRESS X4 SLOT

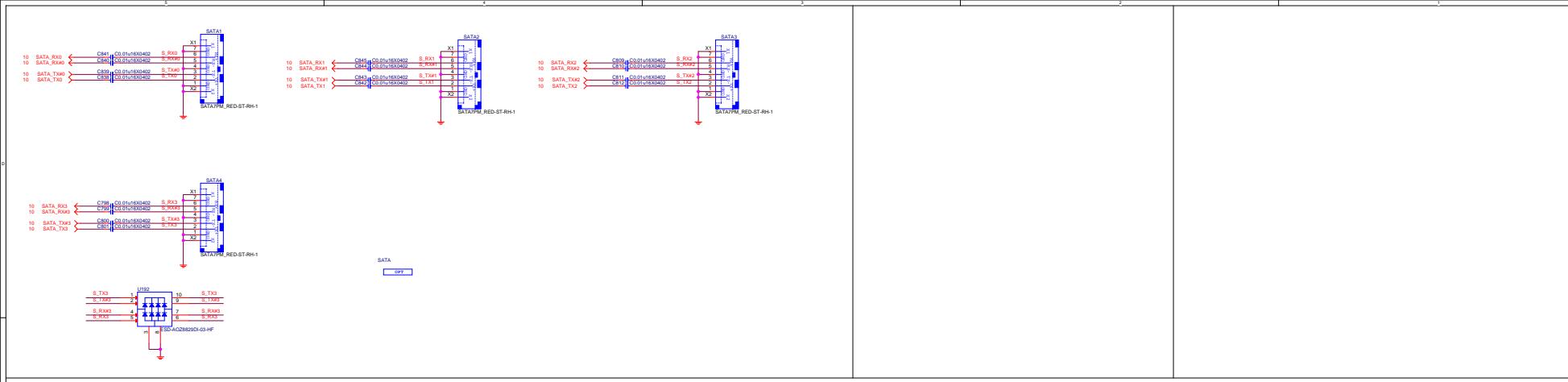




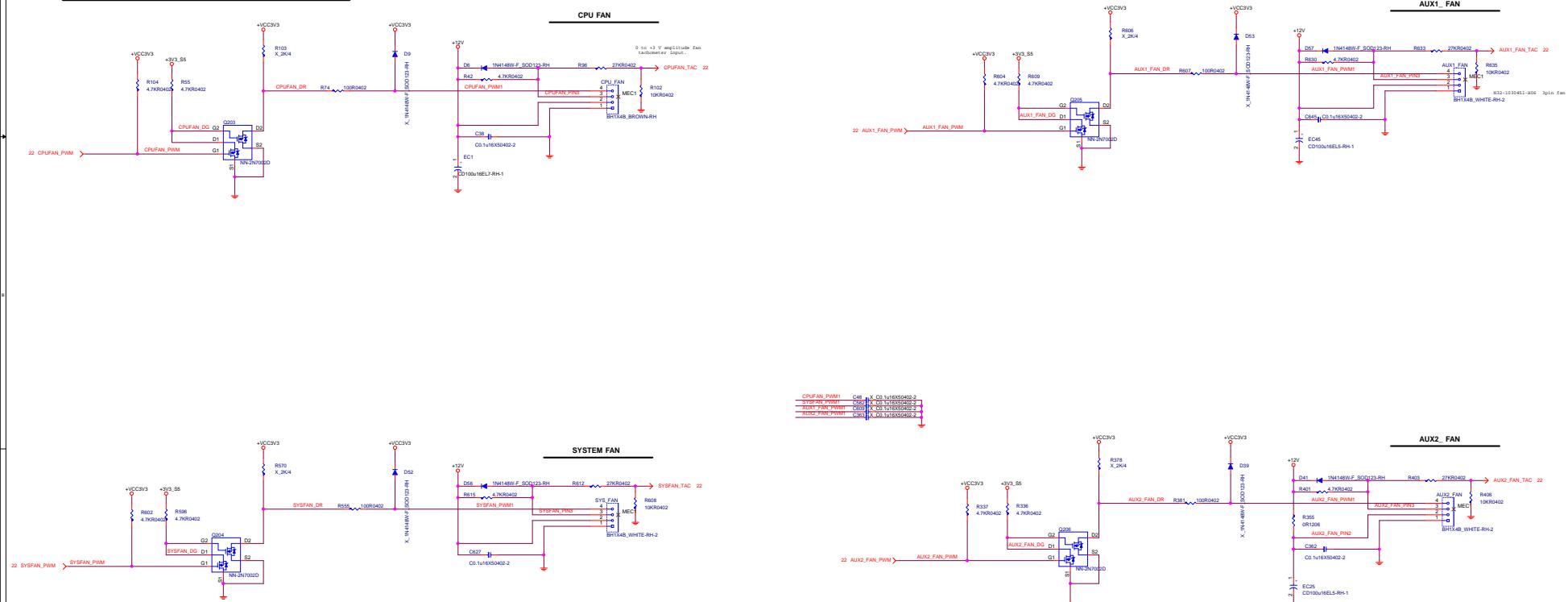


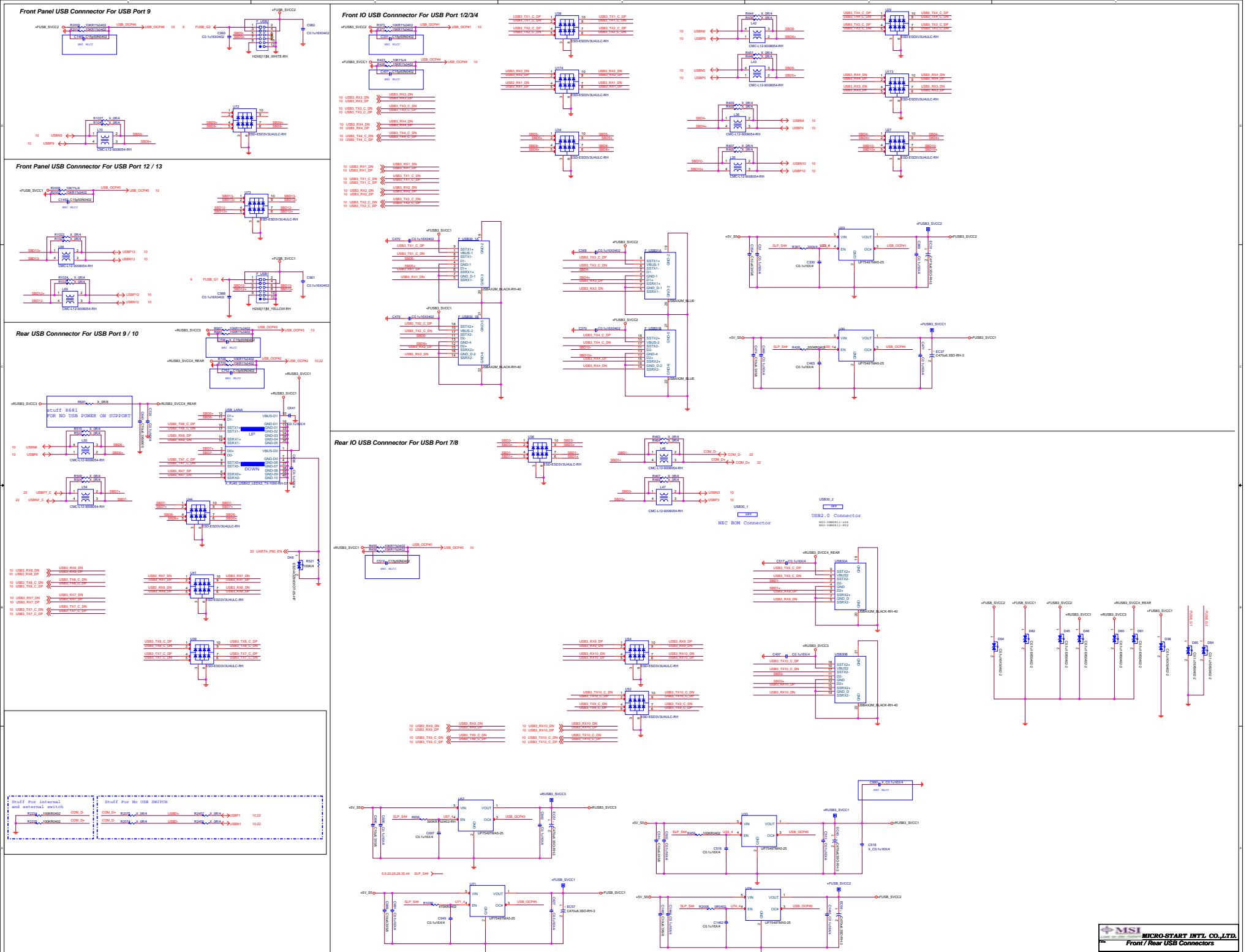
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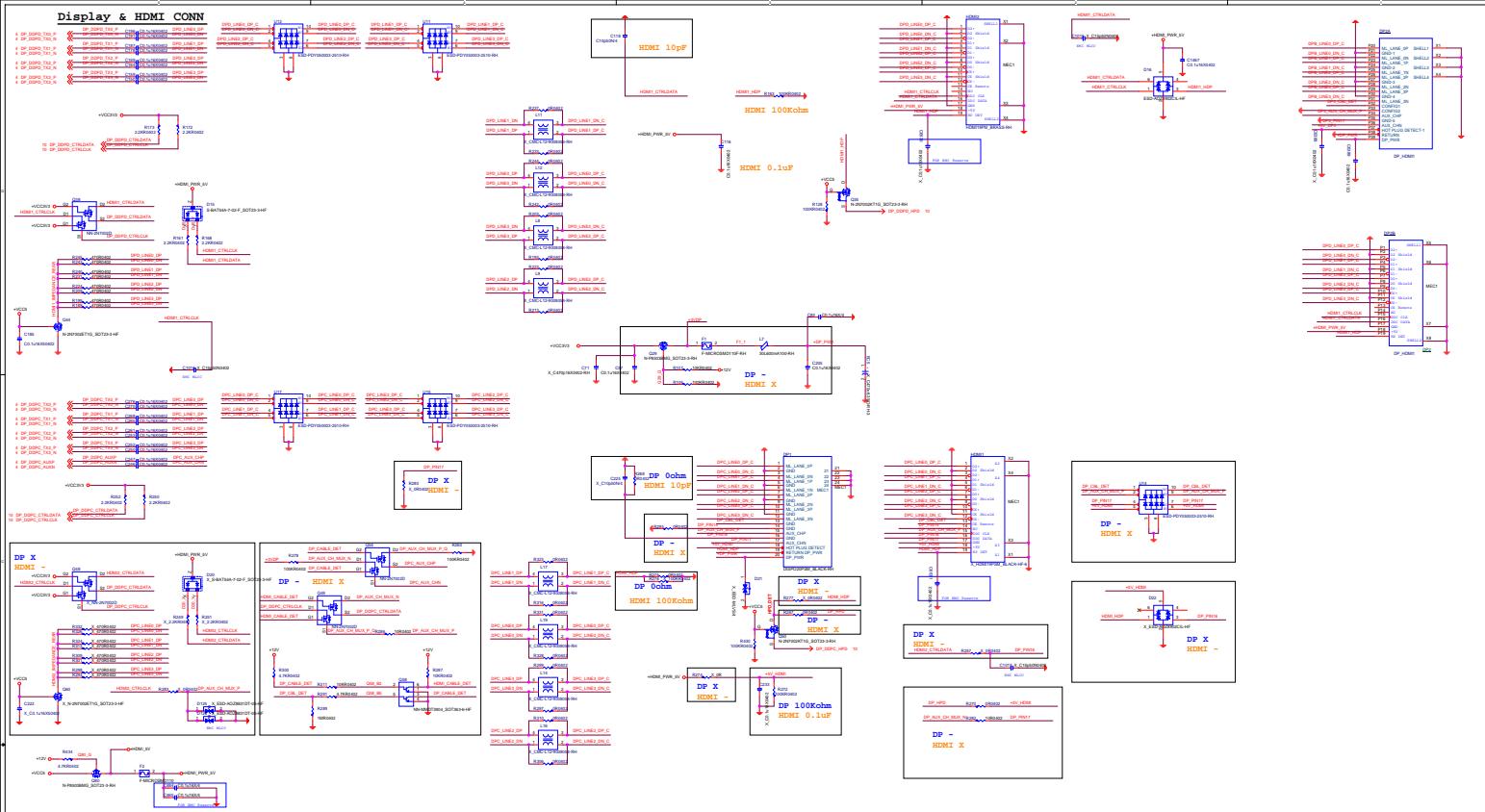


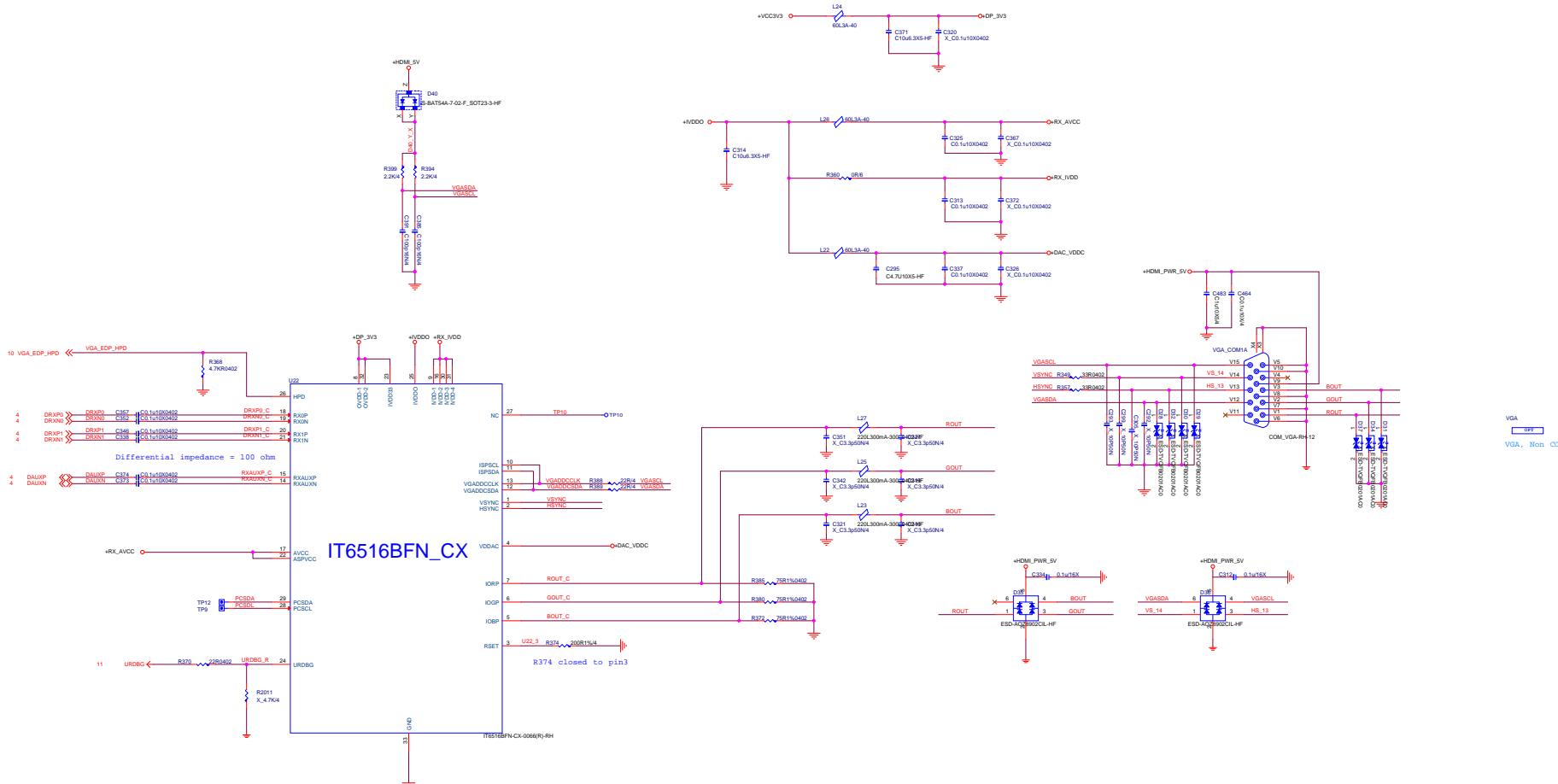


CPU FAN / SYSTEM FAN / POWER FAN

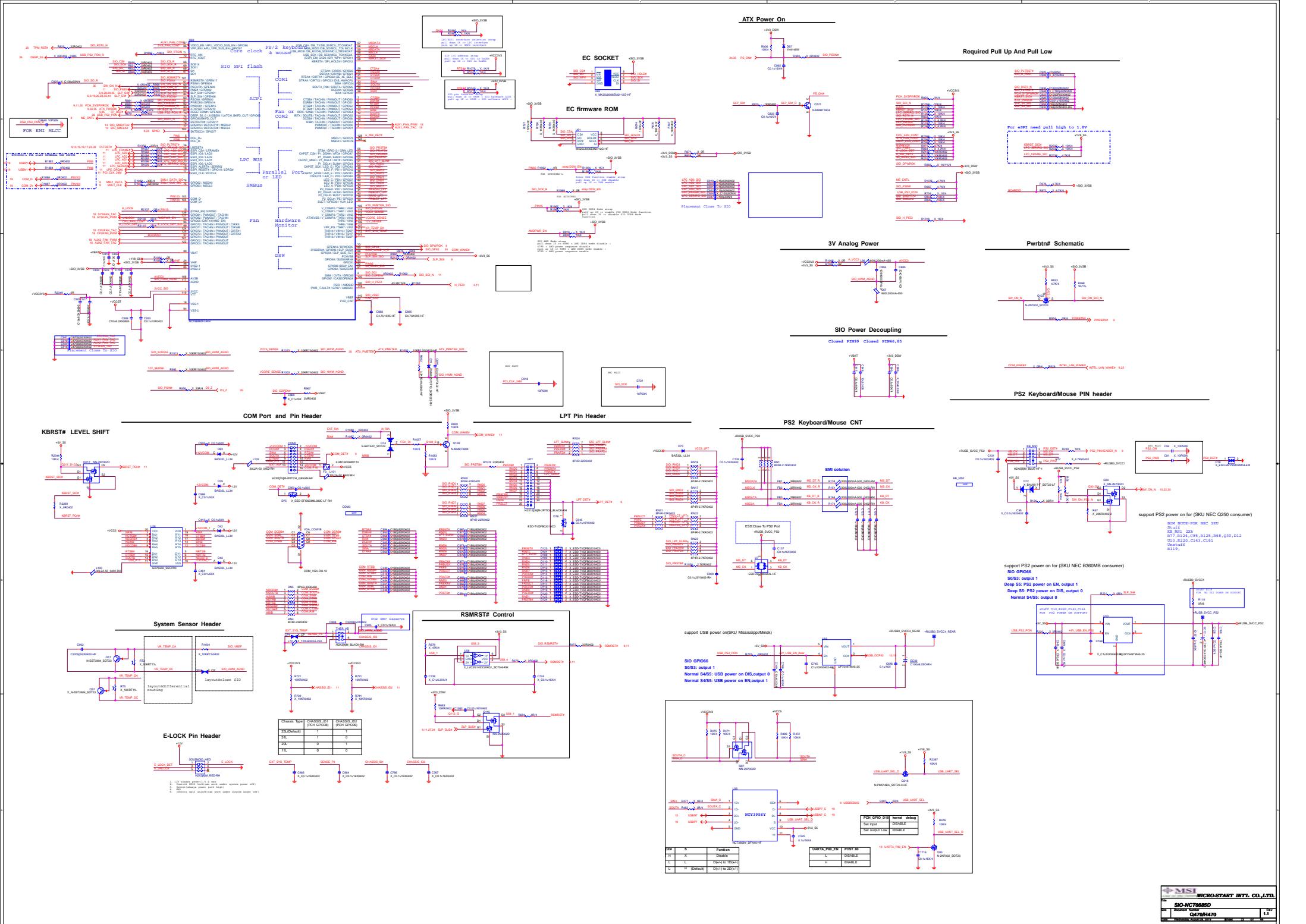


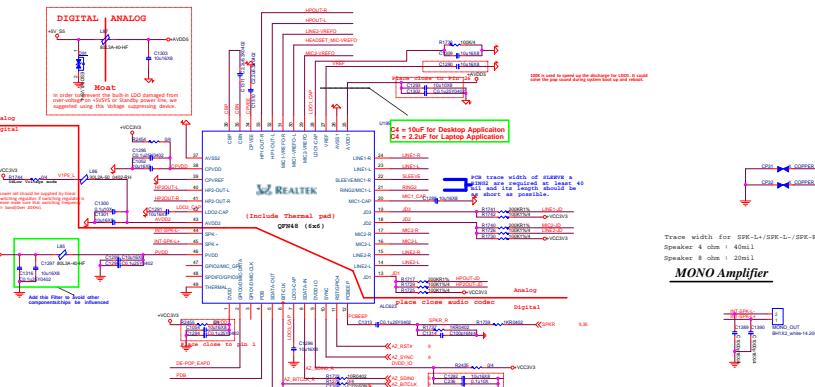




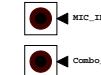
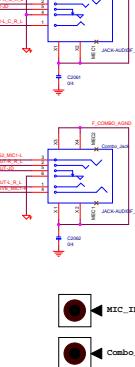
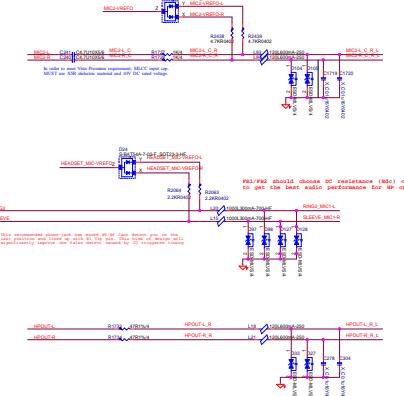
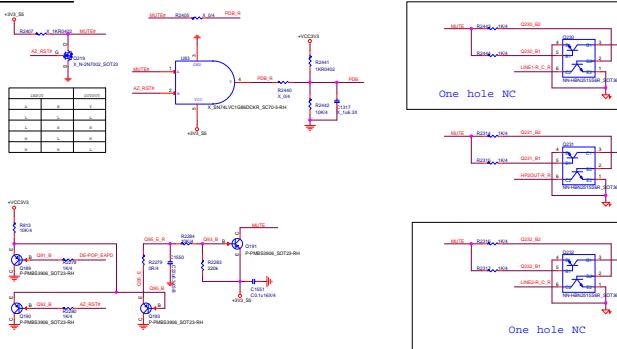
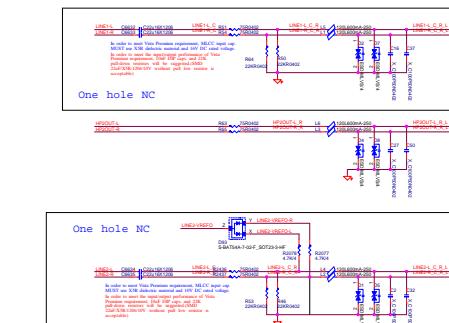


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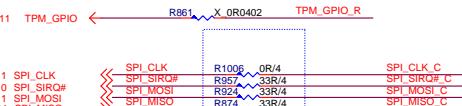
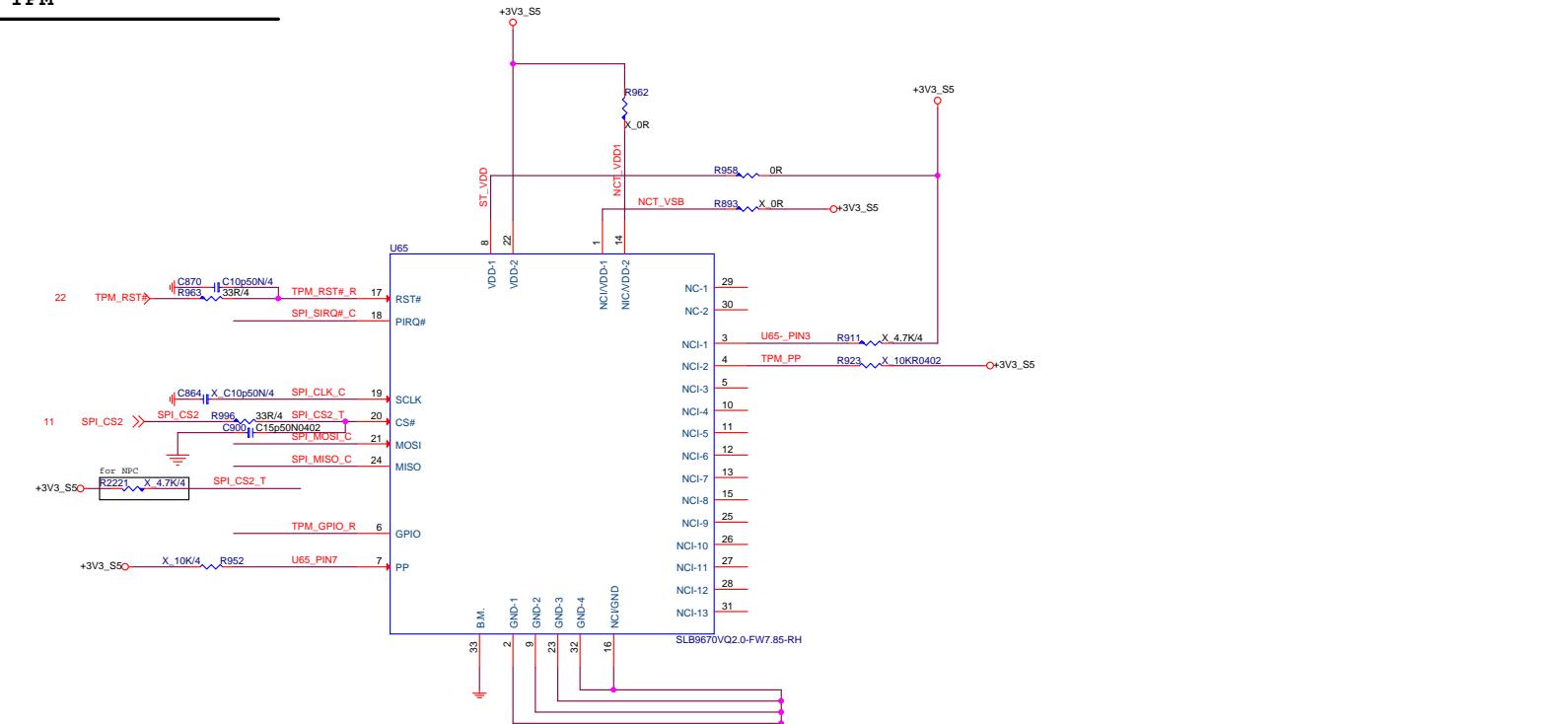
Front Jack

MONO Amplifier

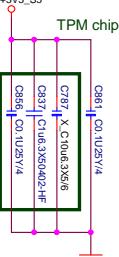
Audio DE-POPRear Jack

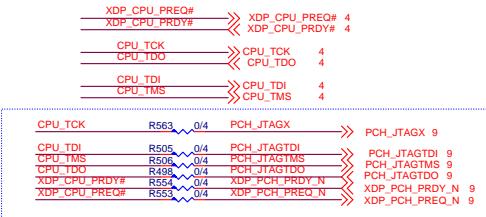
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TPM

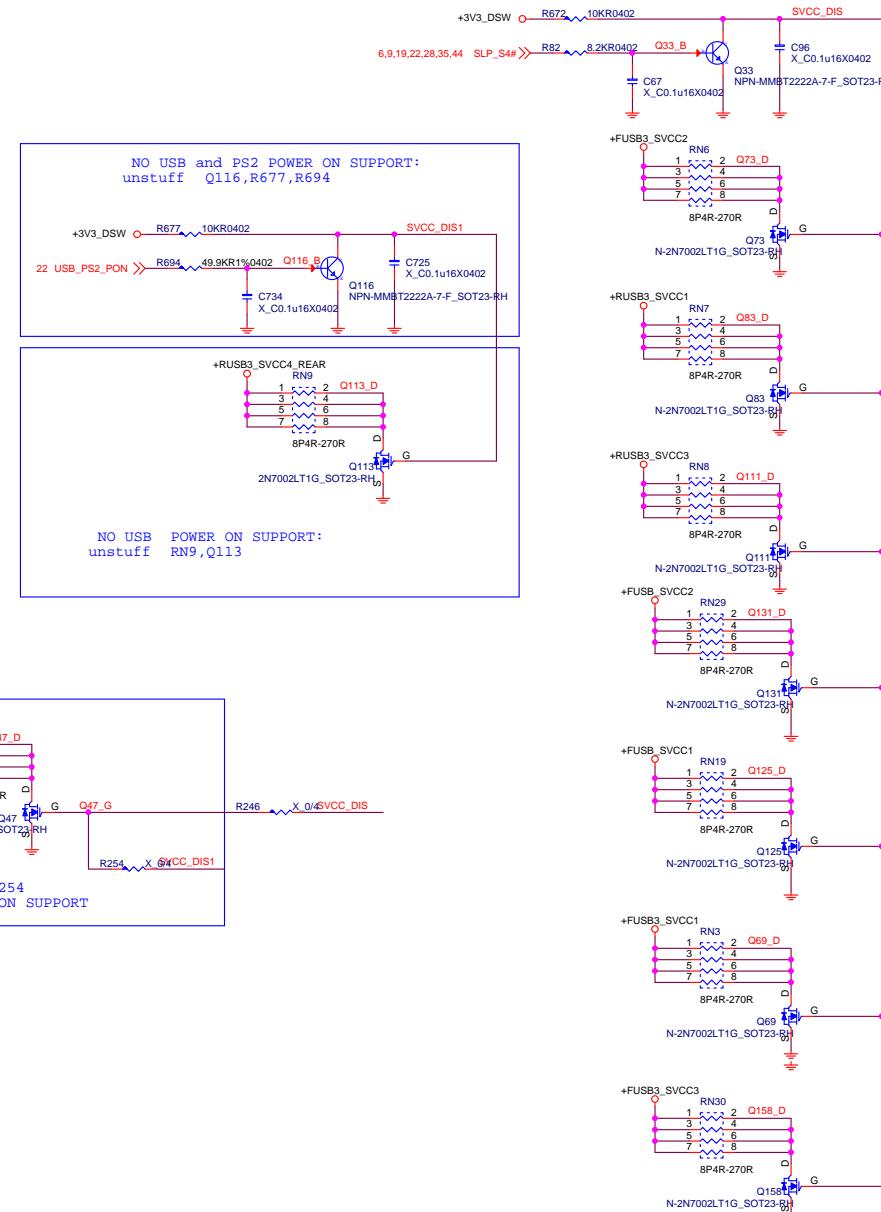


	R893	R911	R923	R920	R952	R958	R962	R861
ST----ST33HTPH2E32AHB4 (SPI)	X	X	X	X	X	X	X	X
NPC----NPCT750 SPI)	V	X	X	X	X	V	V	X
Infineon SLB 9670VQ2.0 (SPI)	X	X	X	X	X	V	X	X

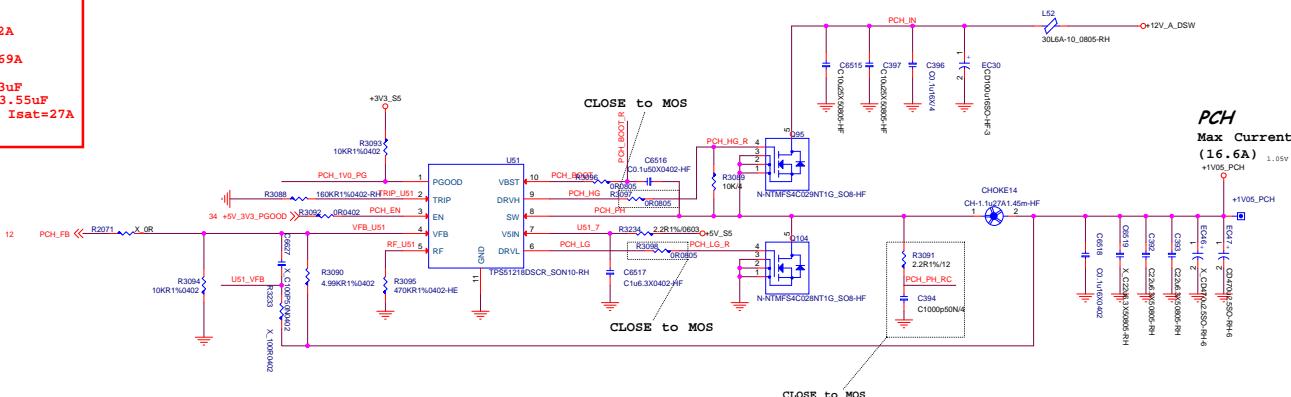




USB power discharge circuit



Vo=1.05V
 Vin=12V
 Fs=300KHz
 OCP=24.9-33.2A
 Iout=16.6A
 Vin_Irms =4.69A
 LIR=17%
 Cin_Cap=14.73uF
 Cout_Cap=1553.55uF
 Choke=1.1uH/ Isat=27A

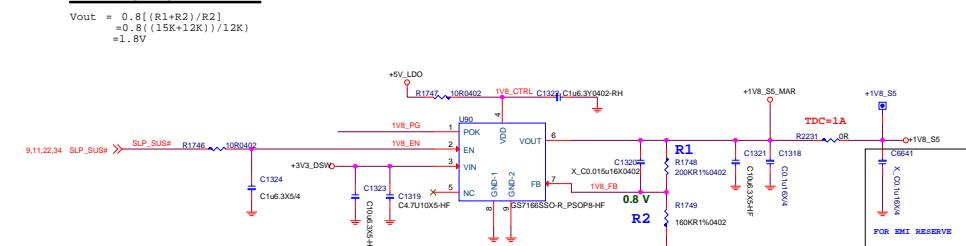


PCH

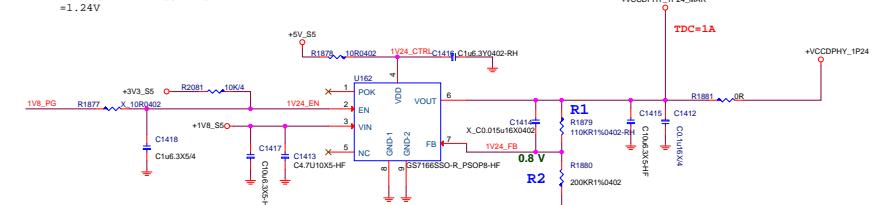
Max Current
(16.6A)

+1V0_PCH 1.05V +/-5%
 +1V05_PCH

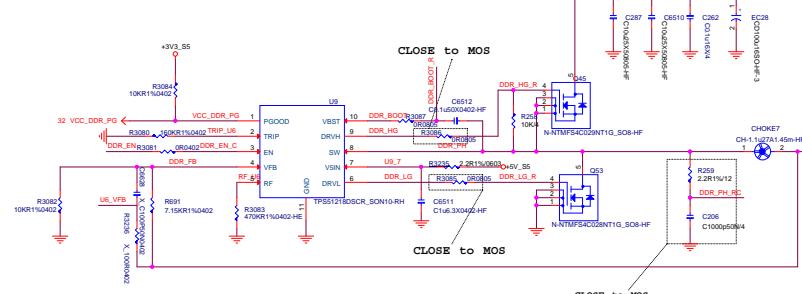
+1V8_S5



Vout = 0.8[(R1+R2)/R2]
 =0.8((15K+12K))/12K
 =1.8V



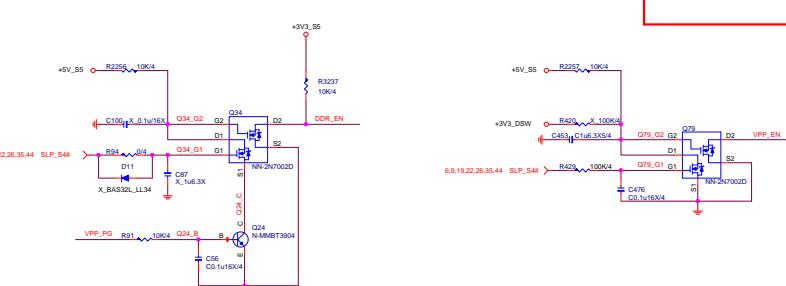
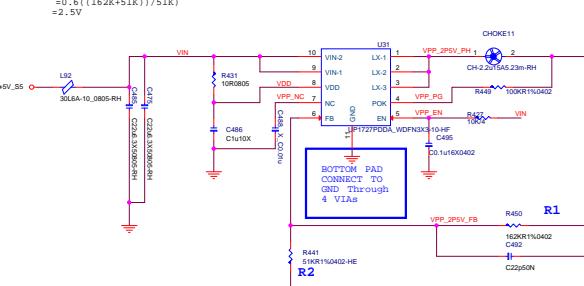
DDR4



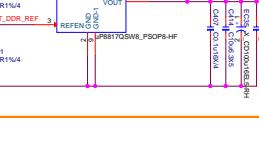
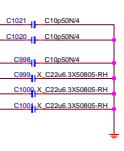
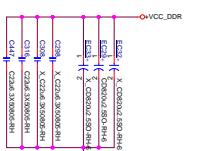
DDR Cin CAP=17.113uF
Max Current Cout CAP=1467.51uF
Choke=1.1uH/ Isat=27

VPP_2.5V

$$\begin{aligned}V_{out} &= 0.6[(R_1+R_2)/R_2] \\&= 0.6((162K+51K))/51K) \\&= 2.5V\end{aligned}$$

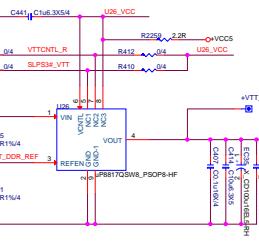


DDR III I/O power decoupling caps



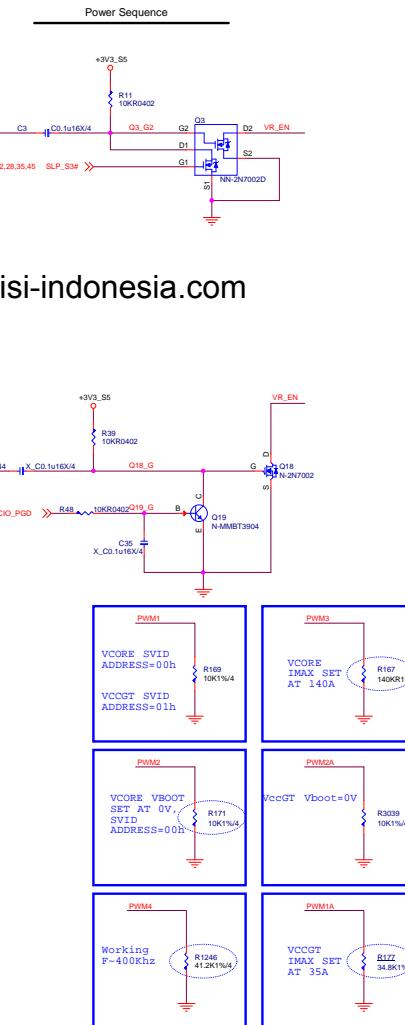
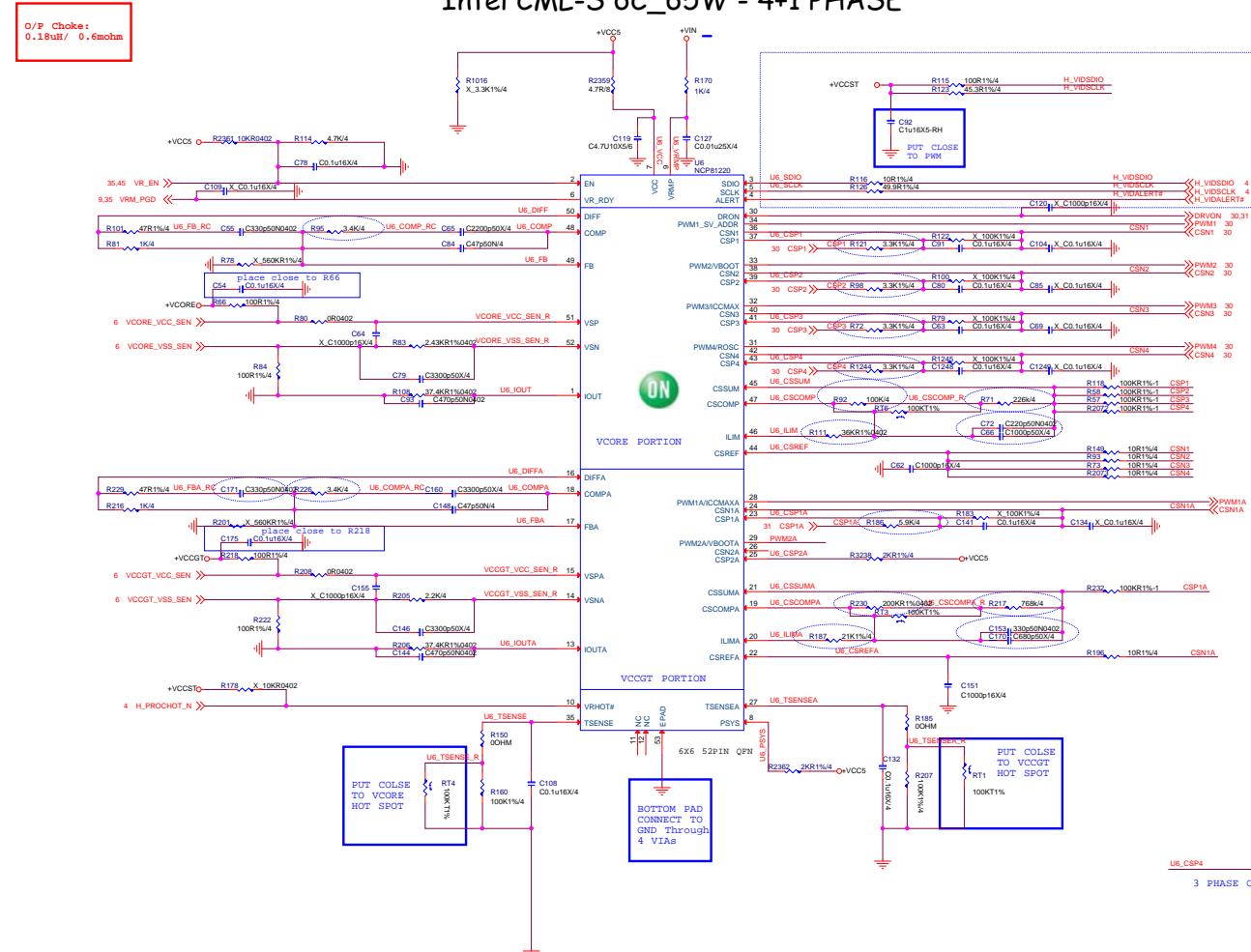
DDR4 Termination Power

0.6V - 1.3V



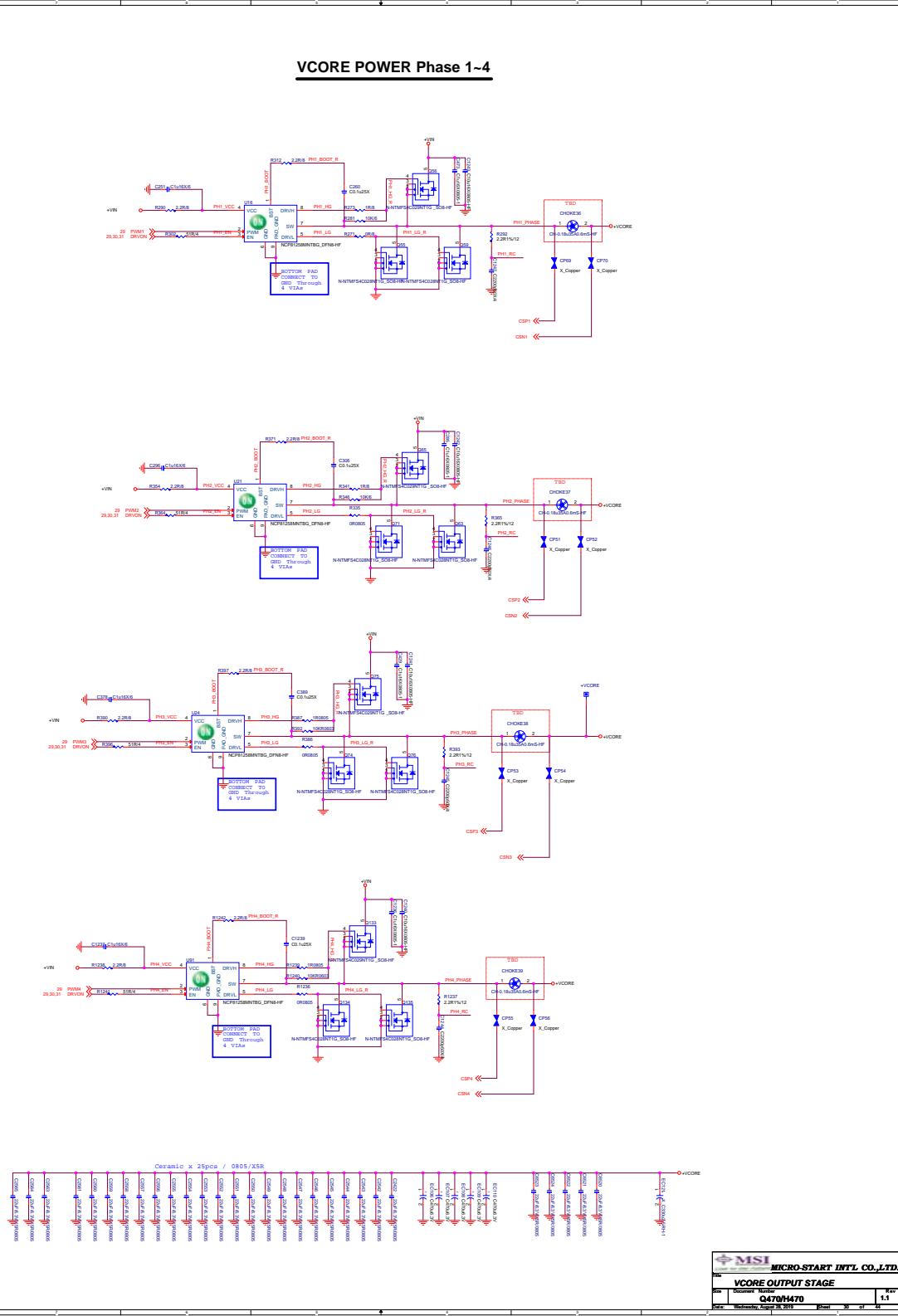
CometLake S62 65W
Vcore Iccmax=140A, PL2=100A, L/L=1.7m ohm
VccGT Iccmax=35A, PL2=28A, L/L=4mohm

Intel CML-S 6C_65W - 4+1 PHASE

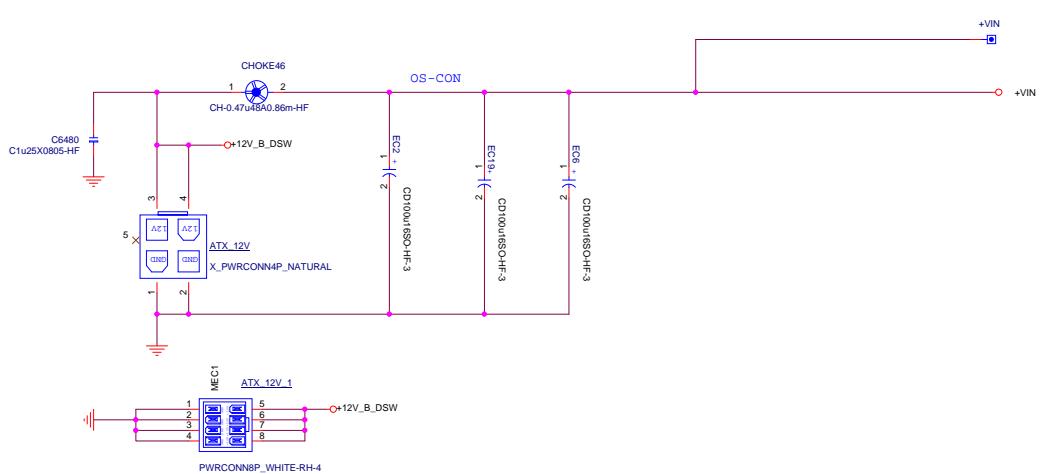
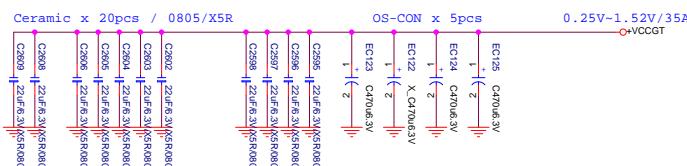
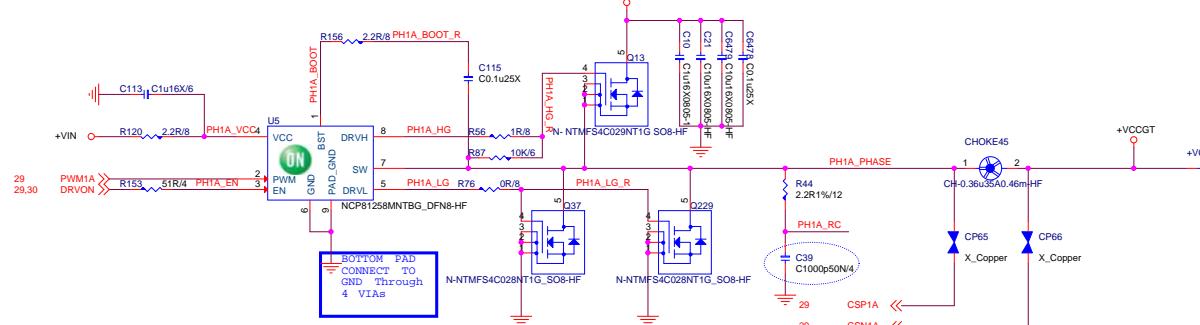


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VCORE POWER Phase 1~4

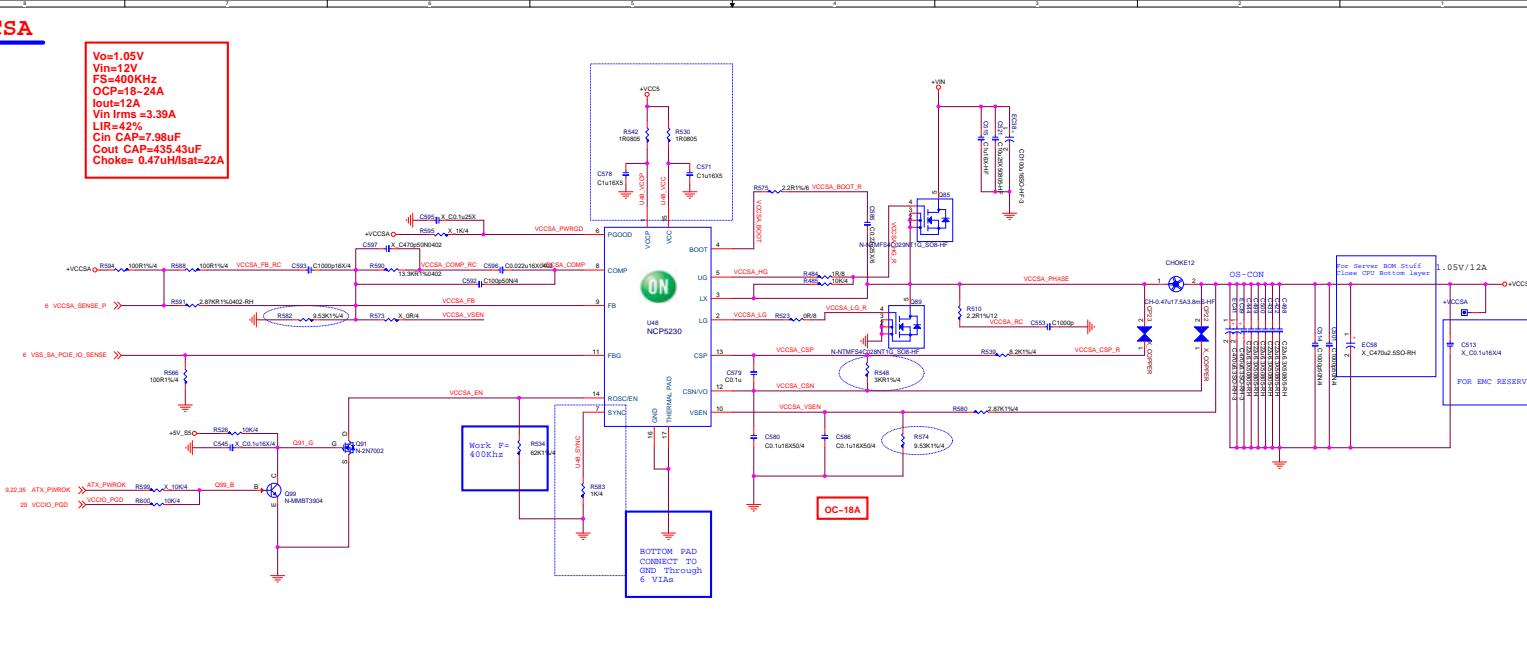


CML-S VCCGT
10C 65W baseline: TDC=28A, Iccmax=35A
LL=4.0mohm
6C 65W performance:
TDC=28A, Iccmax=35A
LL=4.0mohm



VCCSA

**V_o=1.05V
V_{in}=12V
F_S=400KHz
OCP=18-24A
I_{out}=12A
V_{in} I_{rms} =3.39A
LIR=42%
Cin CAP=7.98uF
Cout CAP=435.43uF
Choke= 0.47uH/I_{sat}=22A**

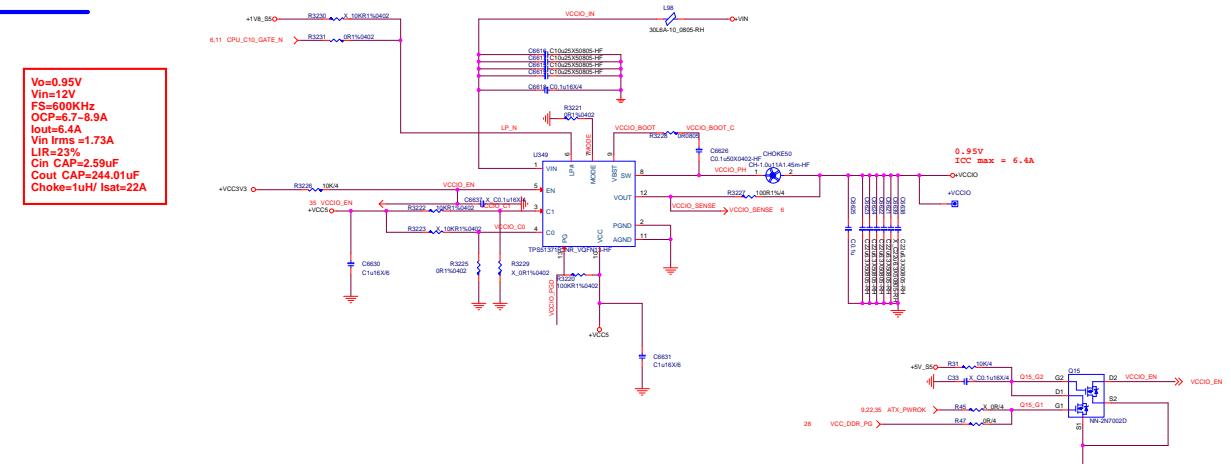


WCCIO

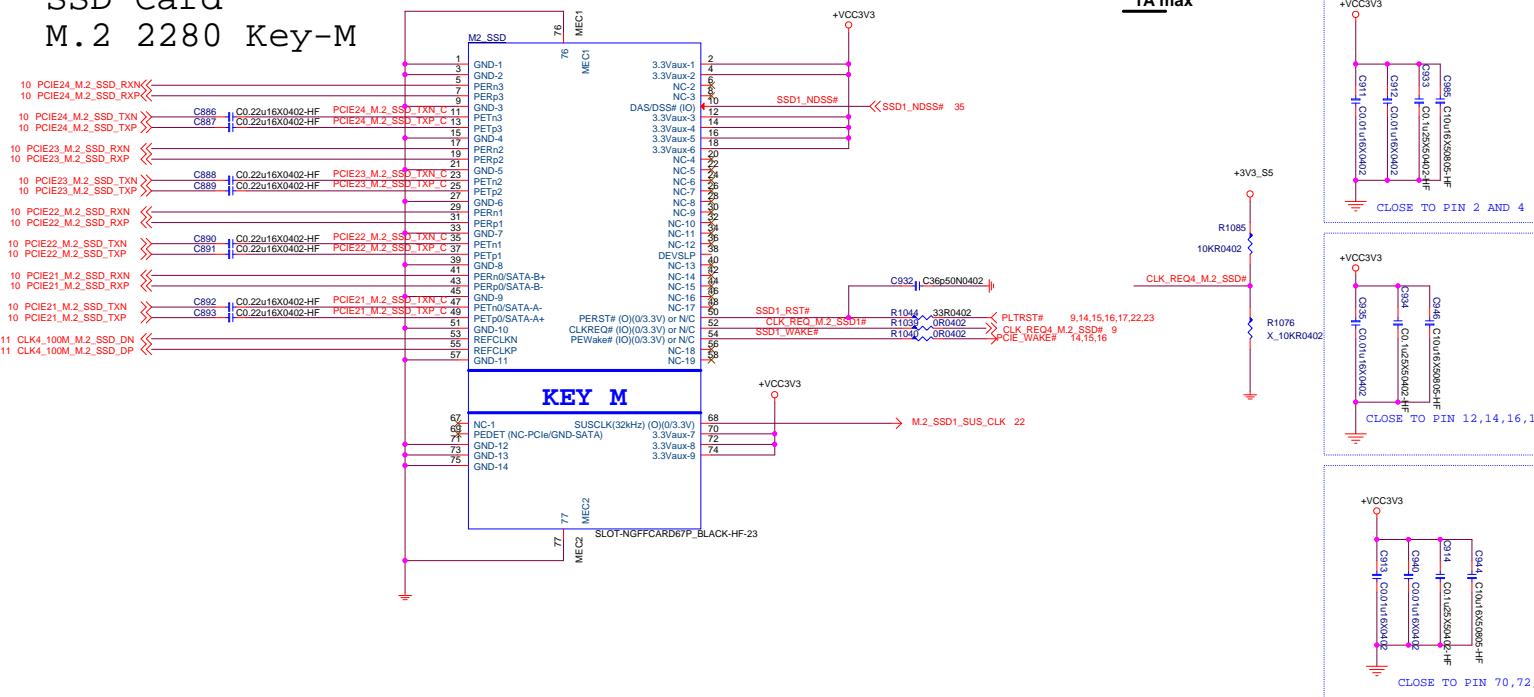
```

Vo=0.95V
Vin=12V
FS=600KHz
OCP=6.7-8.9A
Iout=6.4A
Vin Irms =1.73A
LIR=23%
Cin CAP=2.59uF
Cout CAP=244.01uF
Choke=1uH/ Lsat=22A

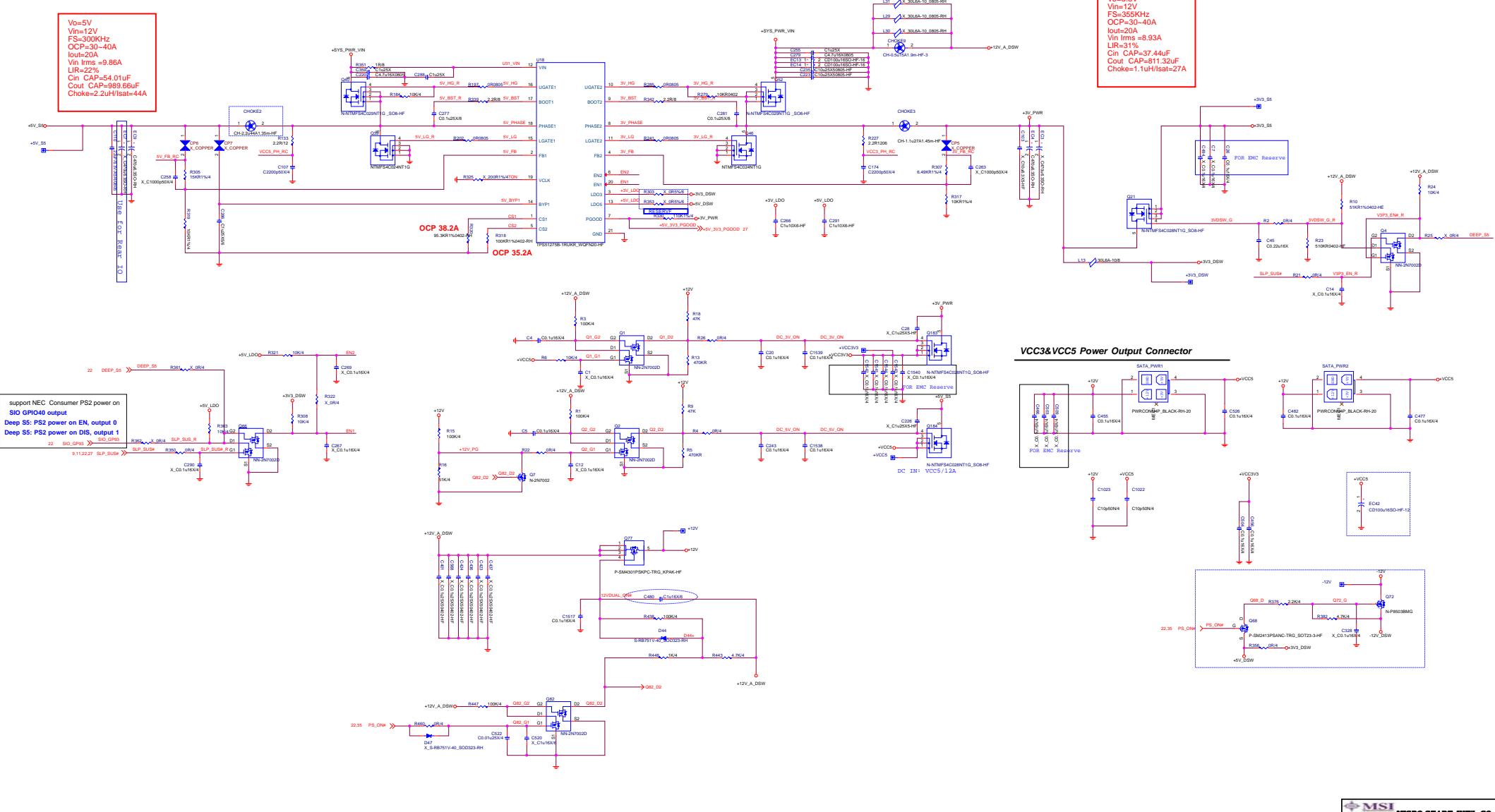
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SSD Card
M.2 2280 Key-M

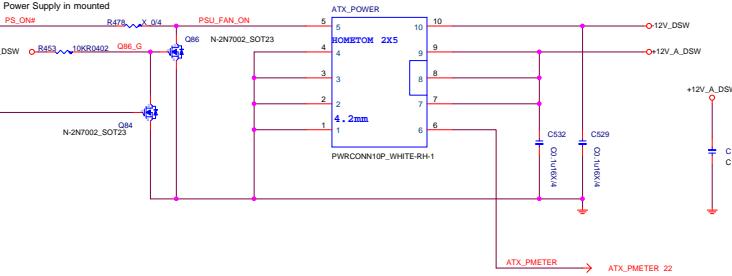


VCC3&VCC5 Power

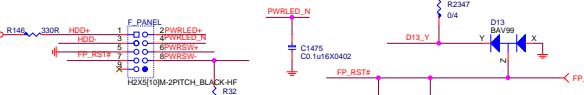


ATX Power Connector / Front Panel / LED/DSW

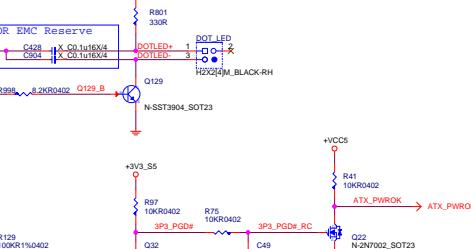
8 Pin ATX Power Connector



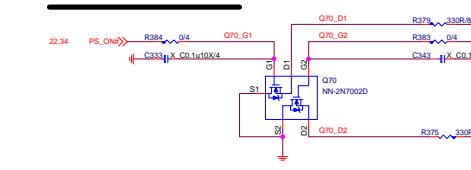
LENOVO Front Panel Connector



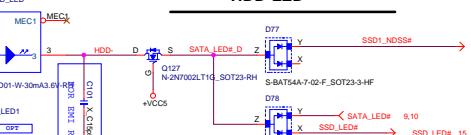
Dot LED



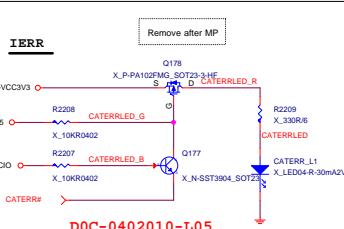
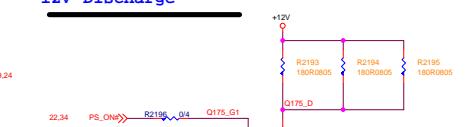
VCC3/VCC5 Discharge



HDD LED



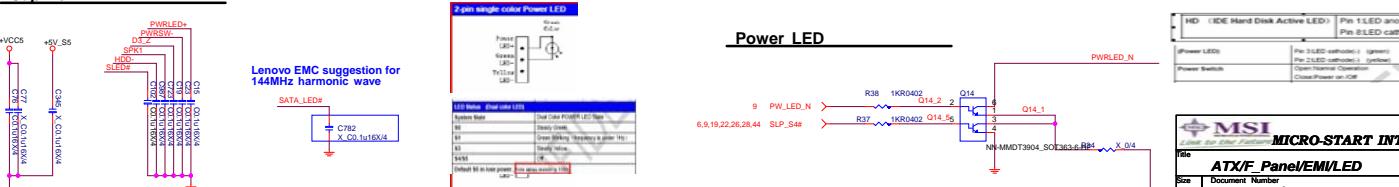
12V Discharge



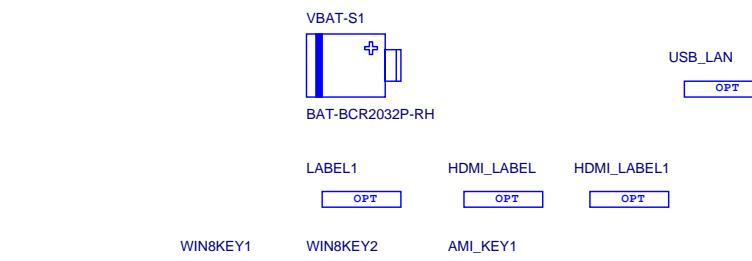
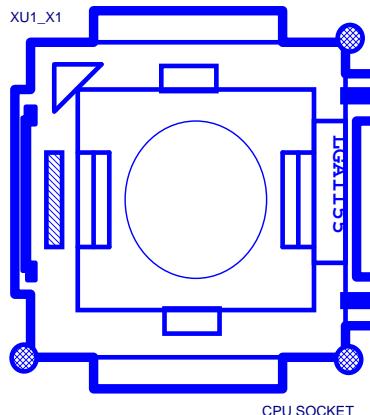
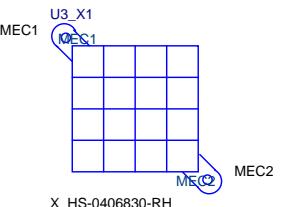
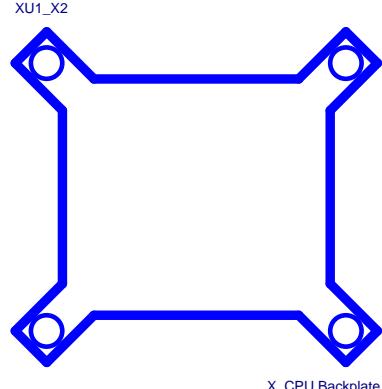
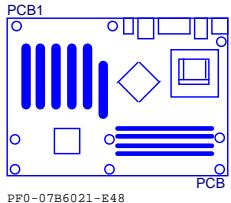
Buzzer Circuit



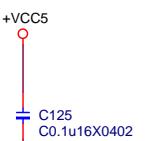
Cap For EMI



Manual Parts



For EMI

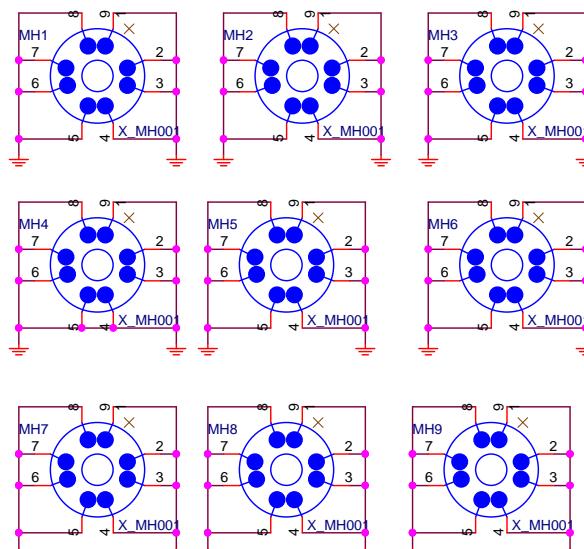


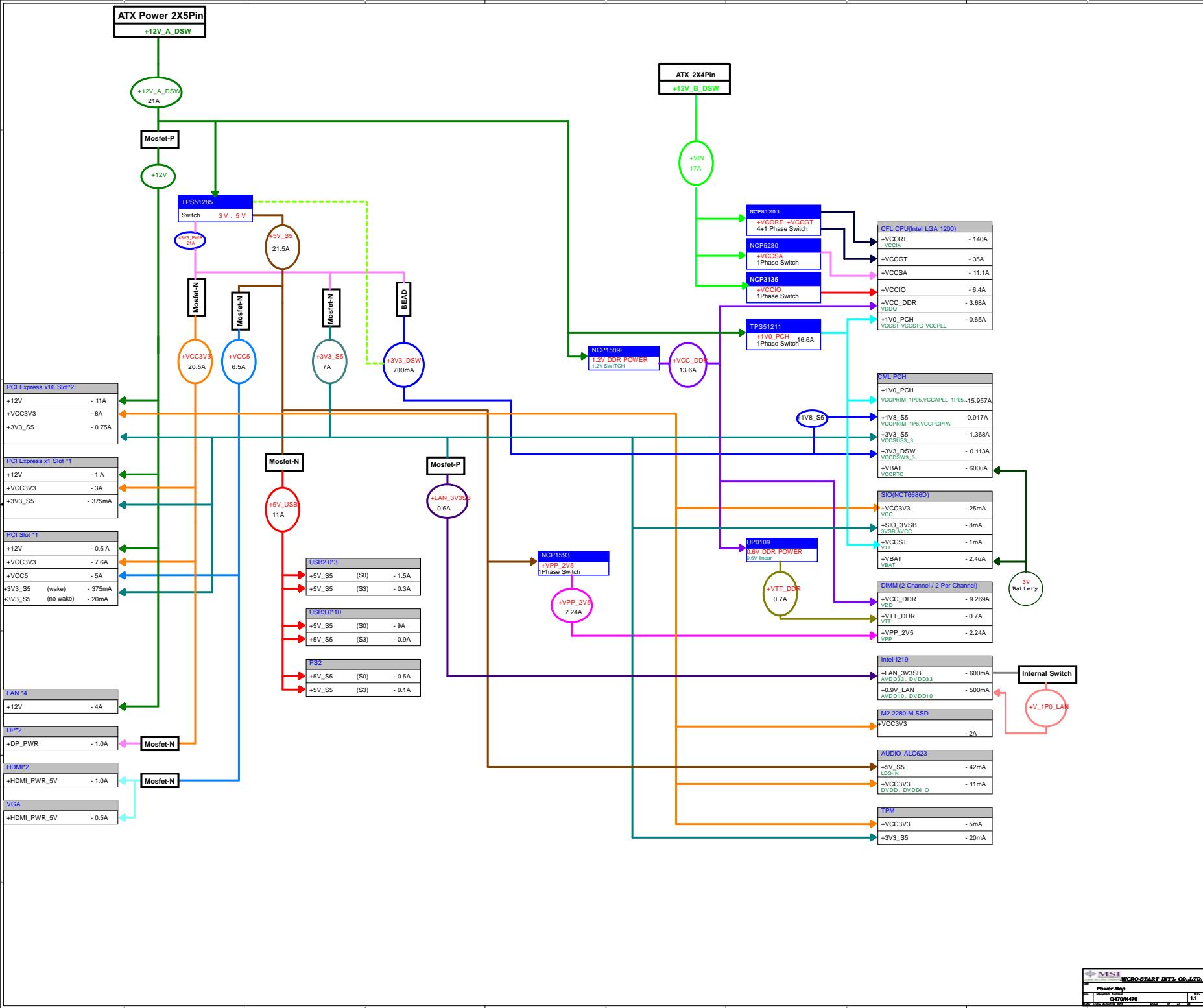
Optics Orientation Holes

Optical Fiducial Marks-120

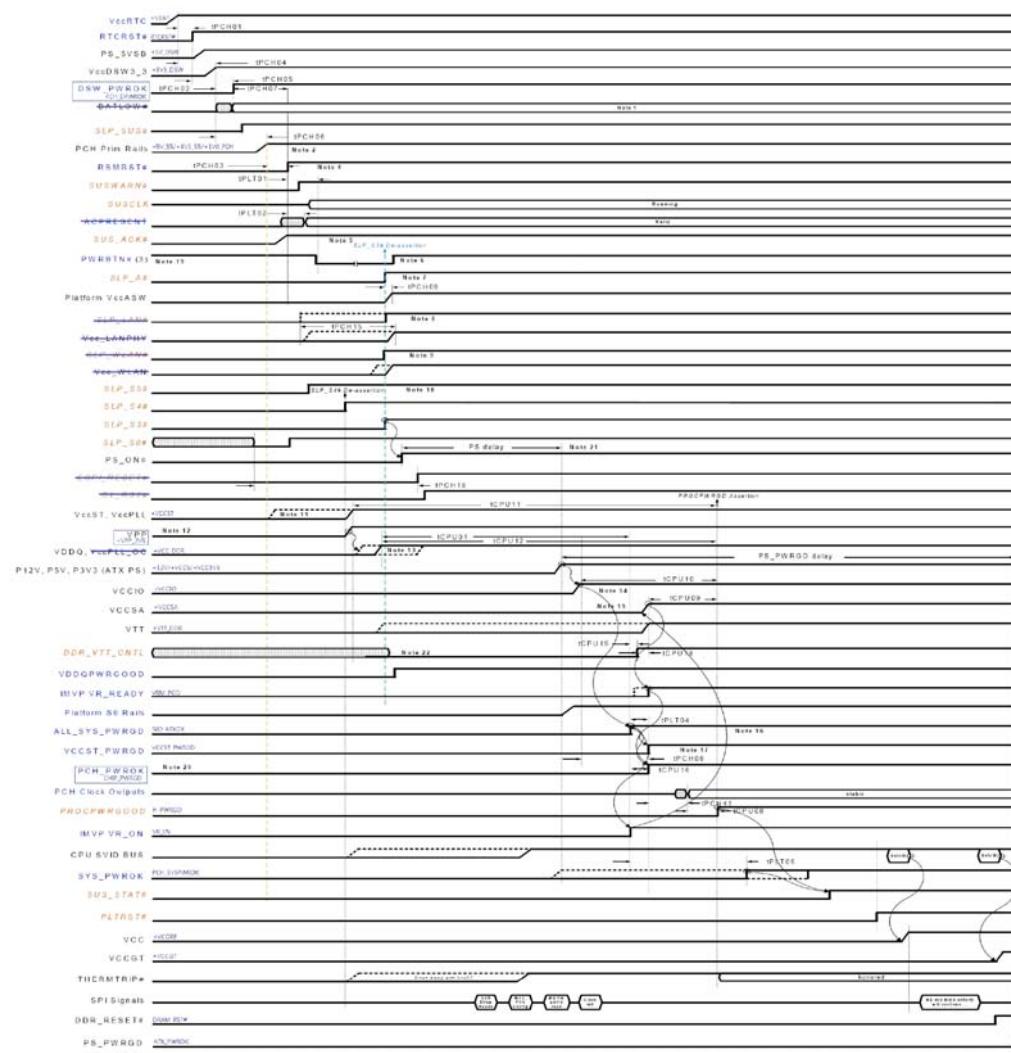


PCH Chipset

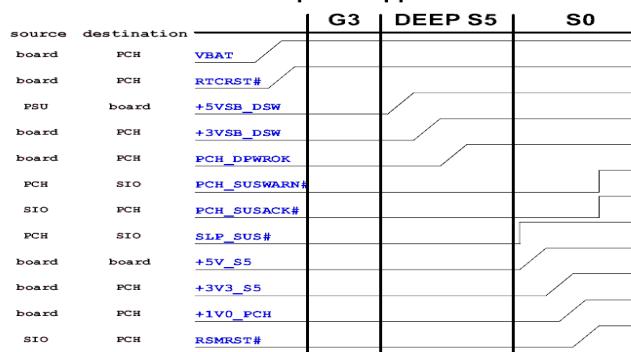


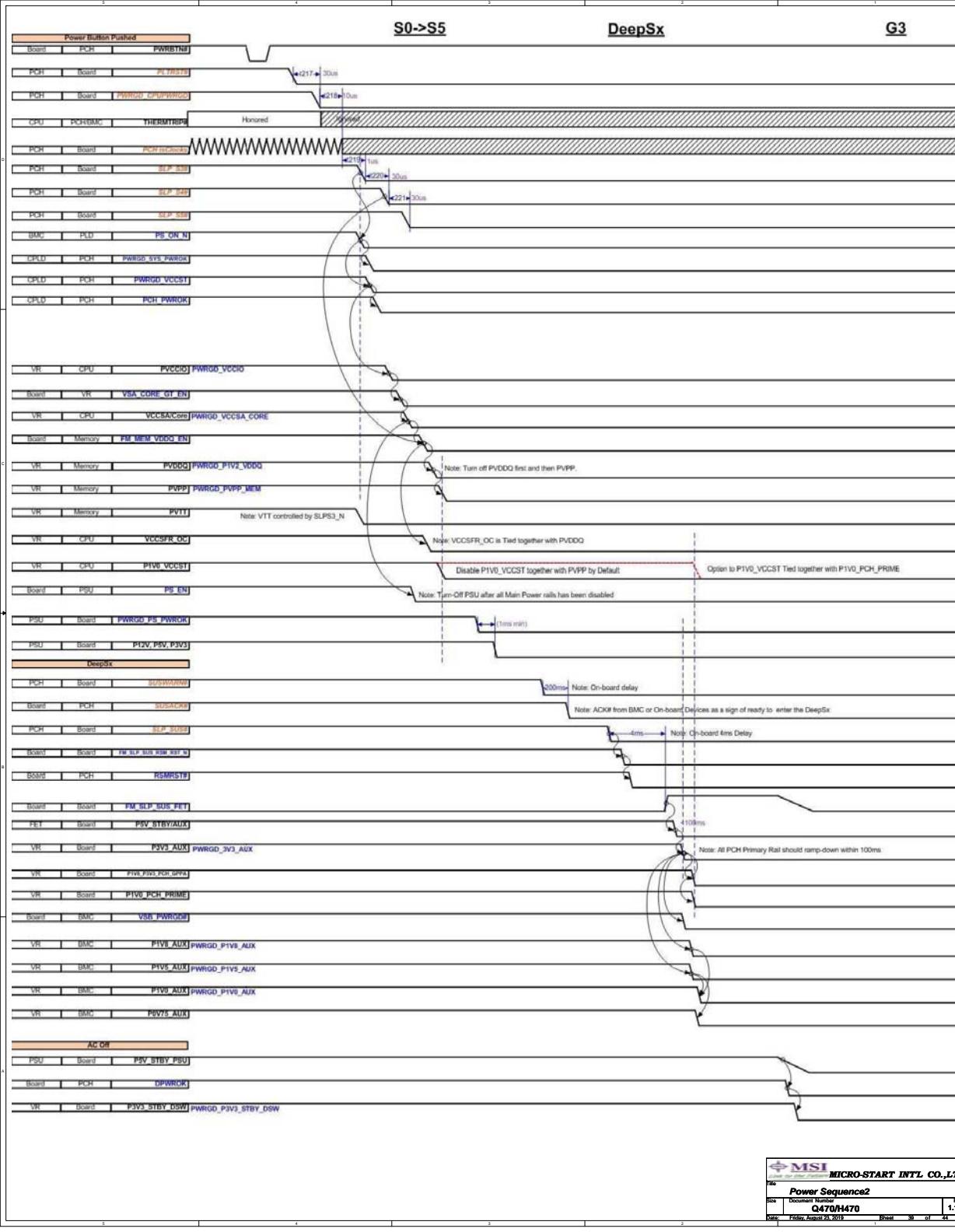


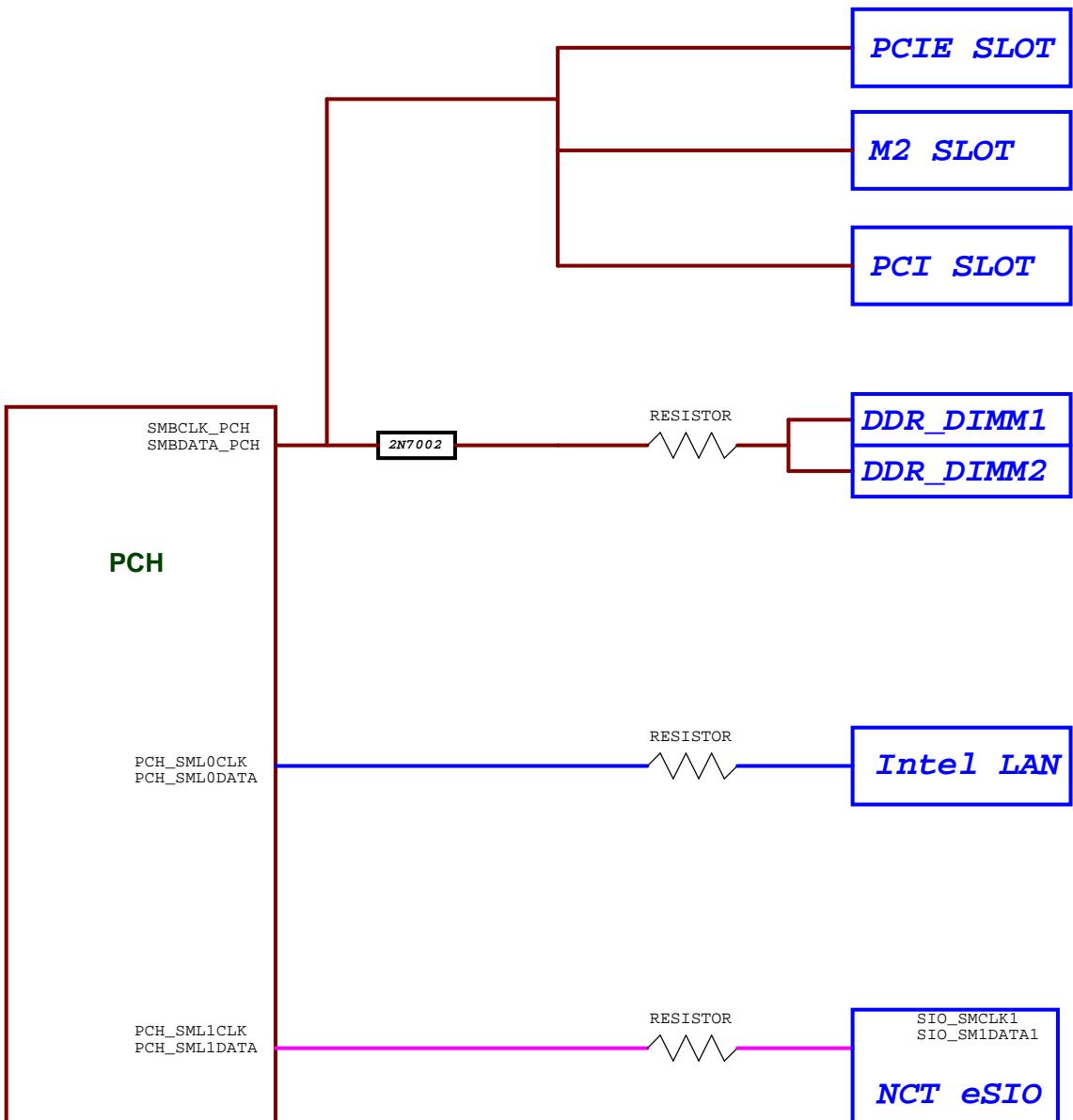
SKL-S Timing Diagram for G3 to S0 [Deep Sx Platform]



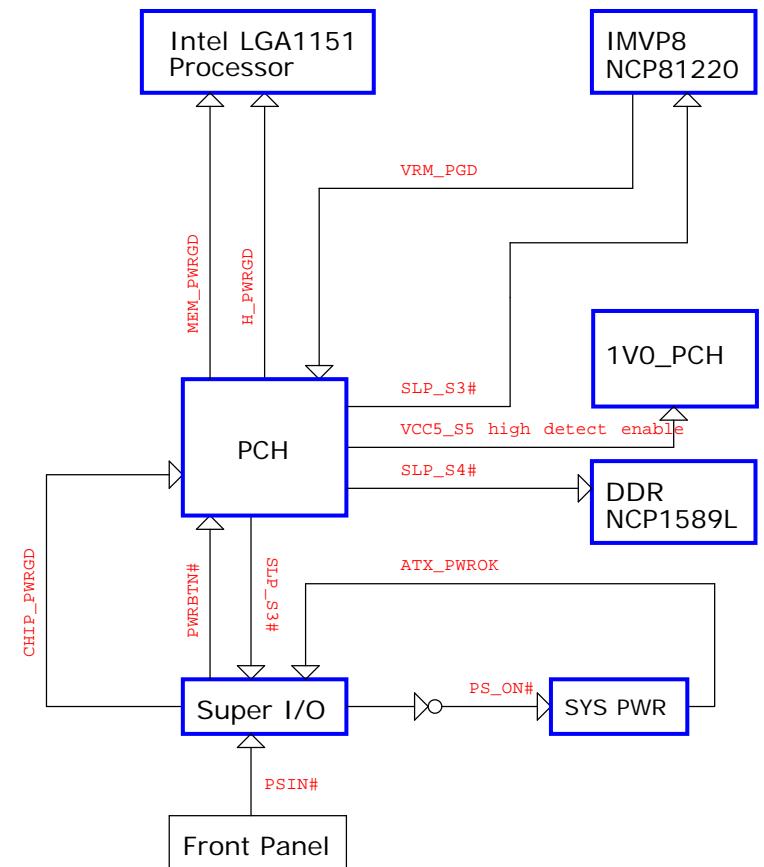
with Deep Sx support



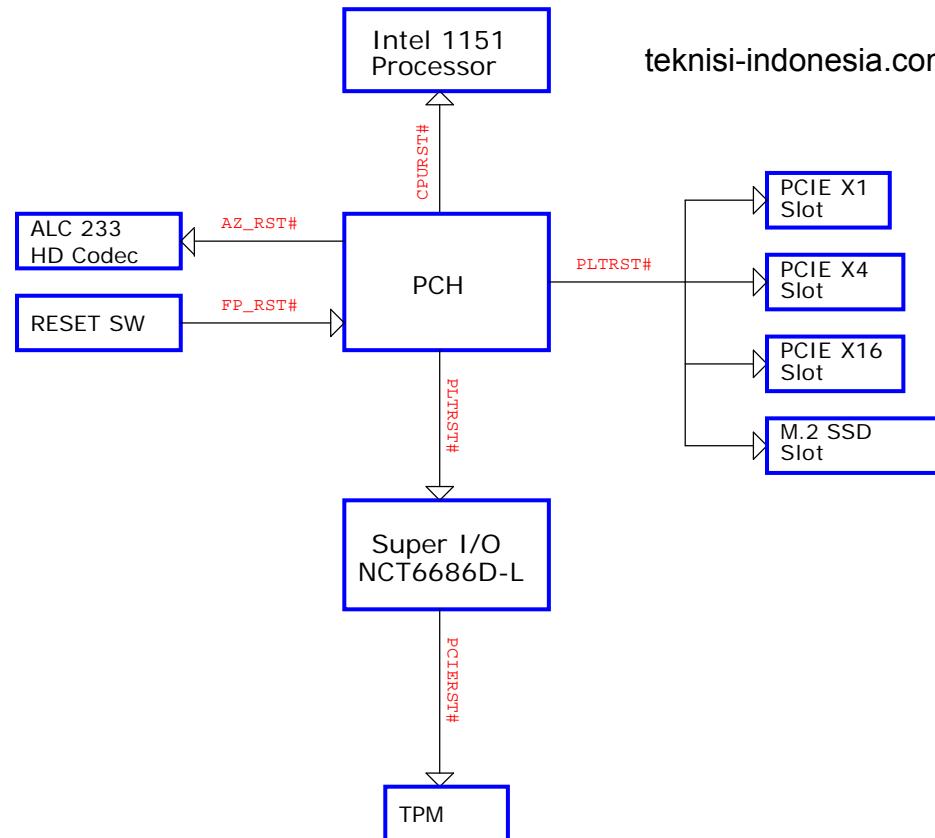




PWROK MAP



RESET MAP



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Micro-Start INTL Co., Ltd.											
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GPIO	Signal Name	Power Well	IN/OUT	Usage	GPIO	Signal Name	Power Well	IN/OUT	Usage	GPIO	Signal Name
GPP_A0	GPP_A0_RCN_N_ESP1_ALERT1_N	SBV3	Native	KBR5T#	GPP_C0	GPP_C0_SPLI_CS_N	SBV3	Native	GPP_G0_FAN_TACH_0	SBV3	IN CHASSIS_ID1
GPP_A1	GPP_A1_LAD0_ESP1_IC0	SBV3	Native	LPC_A0D	GPP_C1	GPP_C1_SPLI_CLK	SBV3	OUT PW_LED_N	GPP_G1_FAN_TACH_1	SBV3	IN CHASSIS_ID2
GPP_A2	GPP_A2_LAD0_ESP1_IC1	SBV3	Native	LPC_A0D	GPP_C2	GPP_C2_SPLI_D2	SBV3	OUT PW_LED_N	GPP_G2_FAN_TACH_2	SBV3	IN HPC_THROTTLE_PCH_N
GPP_A3	GPP_A3_LAD0_ESP1_IC2	SBV3	Native	LPC_A0D	GPP_D3	GPP_D3_ISH_1C2_MOSA	SBV3	IN PD_PCH_GPP_D_3	GPP_G3_FAN_TACH_3	SBV3	Native PCH_BMC_SOURCE_INT_N
GPP_A4	GPP_A4_LAD0_ESP1_IC3	SBV3	Native	LPC_A0D	GPP_D4	GPP_D4_ISH_1C2_MOSA	SBV3	OUT SUS_LED_N	GPP_G4_FAN_TACH_4	SBV3	Native N.C
GPP_A5	GPP_A5_LFRAME_N_ESP1_CS_N	SBV3	Native	LPC_FRAME#	GPP_D5	GPP_D5_SSP0_SRNF	SBV3	Native N.C	GPP_G5_FAN_TACH_5	SBV3	Native N.C
GPP_A6	GPP_A6_SERIRQ	SBV3	Native	LPC_SERIRQ	GPP_D6	GPP_D6_SSP0_TxD	SBV3	Native N.C	GPP_G6_FAN_TACH_6	SBV3	Native N.C
GPP_A7	GPP_A7_ESP1_ALERT0_N	SBV3	Native	LPC_ALERT0	GPP_D7	GPP_D7_SPLI_L	SBV3	Native N.C	GPP_G7_FAN_TACH_7	SBV3	Native N.C
GPP_A8	GPP_A8_CLKOUT_R	SBV3	Native	CURLINE	GPP_D8	GPP_D8_SSP0_SCLK	SBV3	Native N.C	GPP_G8_FAN_PWM_0	SBV3	Native N.C
GPP_A9	GPP_A9_CLKOUT_LPC0_ESP1_CLK	SBV3	Native	LEO_CHIP_CLK	GPP_D9	GPP_D9_ISH_SPLI_CS_N	SBV3	Native N.C	GPP_G9_FAN_PWM_1	SBV3	Native N.C
GPP_A10	GPP_A10_CLKOUT_LPC1	SBV3	Native	PO_CLK_24M	GPP_D10	GPP_D10_ISH_SPLI_CLK	SBV3	Native N.C	GPP_G10_FAN_PWM_2	SBV3	Native N.C
GPP_A11	GPP_A11_FINE_N	SBV3	Native	SIO_FINE#	GPP_D11	GPP_D11_ISH_SPLI_MISO	SBV3	IN FUSE_G1	GPP_G11_FAN_PWM_3	SBV3	IN BMC_THROTTLE_N
GPP_A12	GPP_A12_BMC_N	SBV3	Native	BIBUSY#	GPP_D12	GPP_D12_ISH_SPLI_MOSI	SBV3	IN FUSE_O2	GPP_G12_FAN_PWM_4	SBV3	IN CPU_G0
GPP_A13	GPP_A13_SHARVN_ISU_SUSPRVNACK	SBV3	Native	SHARVN_WVRN#	GPP_D13	GPP_D13_ISH_SPLI_RXD	SBV3	IN FUSE_O3	GPP_G13_FAN_PWM_5	SBV3	IN GPP_G0
GPP_A14	GPP_A14_ISU_STAT_N_ESP1_RST_N	SBV3	Native	SUS_STAT#	GPP_D14	GPP_D14_ISH_UART0_TxD	SBV3	IN PSZ_PINHEADER_N	GPP_G14_FAN_G12XIN	SBV3	IN GPP_G2
GPP_A15	GPP_A15_ISU_SUSACK#	SBV3	Native	PCH_SSUSACK#	GPP_D15	GPP_D15_ISH_UART0_RTS_N	SBV3	IN LPT_DE#	GPP_G15_G12XRESET_N	SBV3	IN GPP_G3
GPP_A16	GPP_A16_CLKOUT_48	SBV3	Native	N.C	GPP_D16	GPP_D16_ISH_UART0_CTS_N	SBV3	Native N.C	GPP_G16_G12XCLK	SBV3	IN GPP_G4
GPP_A17	GPP_A17_ISH_GPP	SBV3	OUT	B1_DISABLE_N	GPP_E1	GPP_E1_ISH_GPP	SBV3	Native COM_WAKE#	GPP_E2_GPP_COMPLETE	SBV3	IN GPP_G5
GPP_A18	GPP_A18_ISH_GP1	SBV3	Native	N.C	GPP_E3	GPP_E3_ISH_GPP	SBV3	IN GPP_E1_GPP_D18	GPP_E4_GPP_G12X	SBV3	Native SHV1_EVENT_N
GPP_A19	GPP_A19_ISH_GP1	SBV3	Native	N.C	GPP_E5	GPP_E5_ISH_GPP	SBV3	Native N.C	GPP_E6_G15_ISH_SMI_N	SBV3	IN SIO_SCI_N
GPP_A20	GPP_A20_ISH_GP2	SBV3	OUT	SEL#	GPP_E6	GPP_E6_ISH_GPP	SBV3	Native N.C	GPP_E7_G20_ISH_GPP	SBV3	Native BMC_READY
GPP_A21	GPP_A21_ISH_GP3	SBV3	Native	WLAN_DETECT_N	GPP_E7	GPP_E7_ISH_GPP	SBV3	Native N.C	GPP_E8_G21_ISH_GPP	SBV3	Native BMC_CARD_DET_R_N
GPP_A22	GPP_A22_ISH_GP4	SBV3	Native	COM_GPI01	GPP_E8	GPP_E8_ISH_GPP	SBV3	Native N.C	GPP_E9_G22_ISH_GPP	SBV3	OUT GPP_G0
GPP_B0	GPP_B0_ISH_GP5	SBV3	Native	CHIP_GPIO	GPP_E9	GPP_E9_ISH_GPP	SBV3	Native N.C	GPP_H0_GPP_H0_SRCCLKREQ0_N	SBV3	Native FM_MEM_THERM_EVENT_LT3_N
GPP_B1	GPP_B1_ISH_GP6	SBV3	Native	N.C	GPP_E9	GPP_E9_ISH_GPP	SBV3	Native N.C	GPP_H1_GPP_H1_SRCCLKREQ1_N	SBV3	Native FM_NH_THRESHOLE_N
GPP_B2	GPP_B2_VRALENT_N	SBV3	Native	PCI_VRALENT#	GPP_E9	GPP_E9_ISH_GPP	SBV3	Native N.C	GPP_H2_GPP_H2_SRCCLKREQ2_N	SBV3	OUT CATERR_N
GPP_B3	GPP_B3_CPU_GPP	SBV3	Native	N.C	GPP_E9	GPP_E9_ISH_GPP	SBV3	Native N.C	GPP_H3_GPP_H3_SRCCLKREQ3_N	SBV3	Native PCH_BMC_ALERT
GPP_B4	GPP_B4_ISH_GP7	SBV3	Native	N.C	GPP_E9	GPP_E9_ISH_GPP	SBV3	Native N.C	GPP_H4_GPP_H4_SRCCLKREQ4_N	SBV3	IN GPP_G1
GPP_B5	GPP_B5_SRCCLKREQ0_N	SBV3	Native	N.C	GPP_E9	GPP_E9_ISH_GPP	SBV3	Native N.C	GPP_H5_GPP_H5_SRCCLKREQ5_N	SBV3	Native N.C
GPP_B6	GPP_B6_SRCCLKREQ1_N	SBV3	Native	N.C	GPP_E9	GPP_E9_ISH_GPP	SBV3	Native N.C	GPP_H6_GPP_H6_SRCCLKREQ6_N	SBV3	Native N.C
GPP_B7	GPP_B7_SRCCLKREQ2_N	SBV3	Native	N.C	GPP_E9	GPP_E9_ISH_GPP	SBV3	Native N.C	GPP_H7_GPP_H7_SRCCLKREQ7_N	SBV3	Native N.C
GPP_B8	GPP_B8_SRCCLKREQ3_N	SBV3	Native	N.C	GPP_E9	GPP_E9_ISH_GPP	SBV3	Native N.C	GPP_H8_GPP_H8_SRCCLKREQ8_N	SBV3	Native N.C
GPP_B9	GPP_B9_SRCCLKREQ4_N	SBV3	Native	N.C	GPP_E9	GPP_E9_ISH_GPP	SBV3	Native N.C	GPP_H9_GPP_H9_SRCCLKREQ9_N	SBV3	Native N.C
GPP_B10	GPP_B10_SRCCLKREQ5_N	SBV3	Native	N.C	GPP_E9	GPP_E9_ISH_GPP	SBV3	Native N.C	GPP_H10_GPP_H10_SRCCLKREQ10_N	SBV3	Native N.C
GPP_B11	GPP_B11_SRCCLKREQ6_N	SBV3	Native	N.C	GPP_E9	GPP_E9_ISH_GPP	SBV3	Native N.C	GPP_H11_GPP_H11_SRCCLKREQ11_N	SBV3	Native N.C
GPP_B12	GPP_B12_SLP_S0_N	SBV3	Native	SLP_S0#	GPP_E9	GPP_E9_ISH_GPP	SBV3	Native N.C	GPP_H12_GPP_H12_SRCCLKREQ12_N	SBV3	Native N.C
GPP_B13	GPP_B13_PLTRST_N	SBV3	Native	PLTRST#	GPP_F0	GPP_F0_ISH_U8B_OCB_0	SBV3	Native N.C	GPP_H13_GPP_H13_SRCCLKREQ13_N	SBV3	Native N.C
GPP_B14	GPP_B14_SPKR	SBV3	Native	SPKR	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native M2_SSDI_PEDET#	GPP_H14_GPP_H14_SRCCLKREQ14_N	SBV3	Native N.C
GPP_B15	GPP_B15_ISH_GP1	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H15_GPP_H15_SRCCLKREQ15_N	SBV3	Native N.C
GPP_B16	GPP_B16_ISH_GP2	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H16_GPP_H16_SRCCLKREQ16_N	SBV3	Native N.C
GPP_B17	GPP_B17_ISH_GP3	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H17_GPP_H17_SRCCLKREQ17_N	SBV3	Native N.C
GPP_B18	GPP_B18_ISH_GP4	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H18_GPP_H18_SRCCLKREQ18_N	SBV3	Native N.C
GPP_B19	GPP_B19_ISH_GP5	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H19_GPP_H19_SRCCLKREQ19_N	SBV3	Native N.C
GPP_B20	GPP_B20_ISH_GP6	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H20_GPP_H20_SRCCLKREQ20_N	SBV3	Native N.C
GPP_B21	GPP_B21_ISH_GP7	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H21_GPP_H21_SRCCLKREQ21_N	SBV3	Native N.C
GPP_B22	GPP_B22_ISH_GP8	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H22_GPP_H22_SRCCLKREQ22_N	SBV3	Native N.C
GPP_B23	GPP_B23_SRCCLKREQ0_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H23_GPP_H23_SRCCLKREQ23_N	SBV3	Native N.C
GPP_B24	GPP_B24_SRCCLKREQ1_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H24_GPP_H24_SRCCLKREQ24_N	SBV3	Native N.C
GPP_B25	GPP_B25_SRCCLKREQ2_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H25_GPP_H25_SRCCLKREQ25_N	SBV3	Native N.C
GPP_B26	GPP_B26_SRCCLKREQ3_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H26_GPP_H26_SRCCLKREQ26_N	SBV3	Native N.C
GPP_B27	GPP_B27_SRCCLKREQ4_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H27_GPP_H27_SRCCLKREQ27_N	SBV3	Native N.C
GPP_B28	GPP_B28_SRCCLKREQ5_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H28_GPP_H28_SRCCLKREQ28_N	SBV3	Native N.C
GPP_B29	GPP_B29_SRCCLKREQ6_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H29_GPP_H29_SRCCLKREQ29_N	SBV3	Native N.C
GPP_B30	GPP_B30_SRCCLKREQ7_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H30_GPP_H30_SRCCLKREQ30_N	SBV3	Native N.C
GPP_B31	GPP_B31_SRCCLKREQ8_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H31_GPP_H31_SRCCLKREQ31_N	SBV3	Native N.C
GPP_B32	GPP_B32_SRCCLKREQ9_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H32_GPP_H32_SRCCLKREQ32_N	SBV3	Native N.C
GPP_B33	GPP_B33_SRCCLKREQ10_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H33_GPP_H33_SRCCLKREQ33_N	SBV3	Native N.C
GPP_B34	GPP_B34_SRCCLKREQ11_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H34_GPP_H34_SRCCLKREQ34_N	SBV3	Native N.C
GPP_B35	GPP_B35_SRCCLKREQ12_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H35_GPP_H35_SRCCLKREQ35_N	SBV3	Native N.C
GPP_B36	GPP_B36_SRCCLKREQ13_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H36_GPP_H36_SRCCLKREQ36_N	SBV3	Native N.C
GPP_B37	GPP_B37_SRCCLKREQ14_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H37_GPP_H37_SRCCLKREQ37_N	SBV3	Native N.C
GPP_B38	GPP_B38_SRCCLKREQ15_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H38_GPP_H38_SRCCLKREQ38_N	SBV3	Native N.C
GPP_B39	GPP_B39_SRCCLKREQ16_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H39_GPP_H39_SRCCLKREQ39_N	SBV3	Native N.C
GPP_B40	GPP_B40_SRCCLKREQ17_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H40_GPP_H40_SRCCLKREQ40_N	SBV3	Native N.C
GPP_B41	GPP_B41_SRCCLKREQ18_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H41_GPP_H41_SRCCLKREQ41_N	SBV3	Native N.C
GPP_B42	GPP_B42_SRCCLKREQ19_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H42_GPP_H42_SRCCLKREQ42_N	SBV3	Native N.C
GPP_B43	GPP_B43_SRCCLKREQ20_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H43_GPP_H43_SRCCLKREQ43_N	SBV3	Native N.C
GPP_B44	GPP_B44_SRCCLKREQ21_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H44_GPP_H44_SRCCLKREQ44_N	SBV3	Native N.C
GPP_B45	GPP_B45_SRCCLKREQ22_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H45_GPP_H45_SRCCLKREQ45_N	SBV3	Native N.C
GPP_B46	GPP_B46_SRCCLKREQ23_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H46_GPP_H46_SRCCLKREQ46_N	SBV3	Native N.C
GPP_B47	GPP_B47_SRCCLKREQ24_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H47_GPP_H47_SRCCLKREQ47_N	SBV3	Native N.C
GPP_B48	GPP_B48_SRCCLKREQ25_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H48_GPP_H48_SRCCLKREQ48_N	SBV3	Native N.C
GPP_B49	GPP_B49_SRCCLKREQ26_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H49_GPP_H49_SRCCLKREQ49_N	SBV3	Native N.C
GPP_B50	GPP_B50_SRCCLKREQ27_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H50_GPP_H50_SRCCLKREQ50_N	SBV3	Native N.C
GPP_B51	GPP_B51_SRCCLKREQ28_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H51_GPP_H51_SRCCLKREQ51_N	SBV3	Native N.C
GPP_B52	GPP_B52_SRCCLKREQ29_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H52_GPP_H52_SRCCLKREQ52_N	SBV3	Native N.C
GPP_B53	GPP_B53_SRCCLKREQ30_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H53_GPP_H53_SRCCLKREQ53_N	SBV3	Native N.C
GPP_B54	GPP_B54_SRCCLKREQ31_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H54_GPP_H54_SRCCLKREQ54_N	SBV3	Native N.C
GPP_B55	GPP_B55_SRCCLKREQ32_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H55_GPP_H55_SRCCLKREQ55_N	SBV3	Native N.C
GPP_B56	GPP_B56_SRCCLKREQ33_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H56_GPP_H56_SRCCLKREQ56_N	SBV3	Native N.C
GPP_B57	GPP_B57_SRCCLKREQ34_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H57_GPP_H57_SRCCLKREQ57_N	SBV3	Native N.C
GPP_B58	GPP_B58_SRCCLKREQ35_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H58_GPP_H58_SRCCLKREQ58_N	SBV3	Native N.C
GPP_B59	GPP_B59_SRCCLKREQ36_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H59_GPP_H59_SRCCLKREQ59_N	SBV3	Native N.C
GPP_B60	GPP_B60_SRCCLKREQ37_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H60_GPP_H60_SRCCLKREQ60_N	SBV3	Native N.C
GPP_B61	GPP_B61_SRCCLKREQ38_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H61_GPP_H61_SRCCLKREQ61_N	SBV3	Native N.C
GPP_B62	GPP_B62_SRCCLKREQ39_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H62_GPP_H62_SRCCLKREQ62_N	SBV3	Native N.C
GPP_B63	GPP_B63_SRCCLKREQ40_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H63_GPP_H63_SRCCLKREQ63_N	SBV3	Native N.C
GPP_B64	GPP_B64_SRCCLKREQ41_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native N.C	GPP_H64_GPP_H64_SRCCLKREQ64_N	SBV3	Native N.C
GPP_B65	GPP_B65_SRCCLKREQ42_N	SBV3	Native	N.C	GPP_F1	GPP_F1_ISH_GPP	SBV3	Native			

 MSI	MICRO-START INT'L CO., LTD.
History	
Model	Q470/H470
Color	Black
Power	45W
Size	1.1"
Unit	PCB

