

A B C D E

MODEL NAME : *EDP51*
EDB51

PCB NO : *LA-H331P*

BOM P/N :

Dell/Compal Confidential

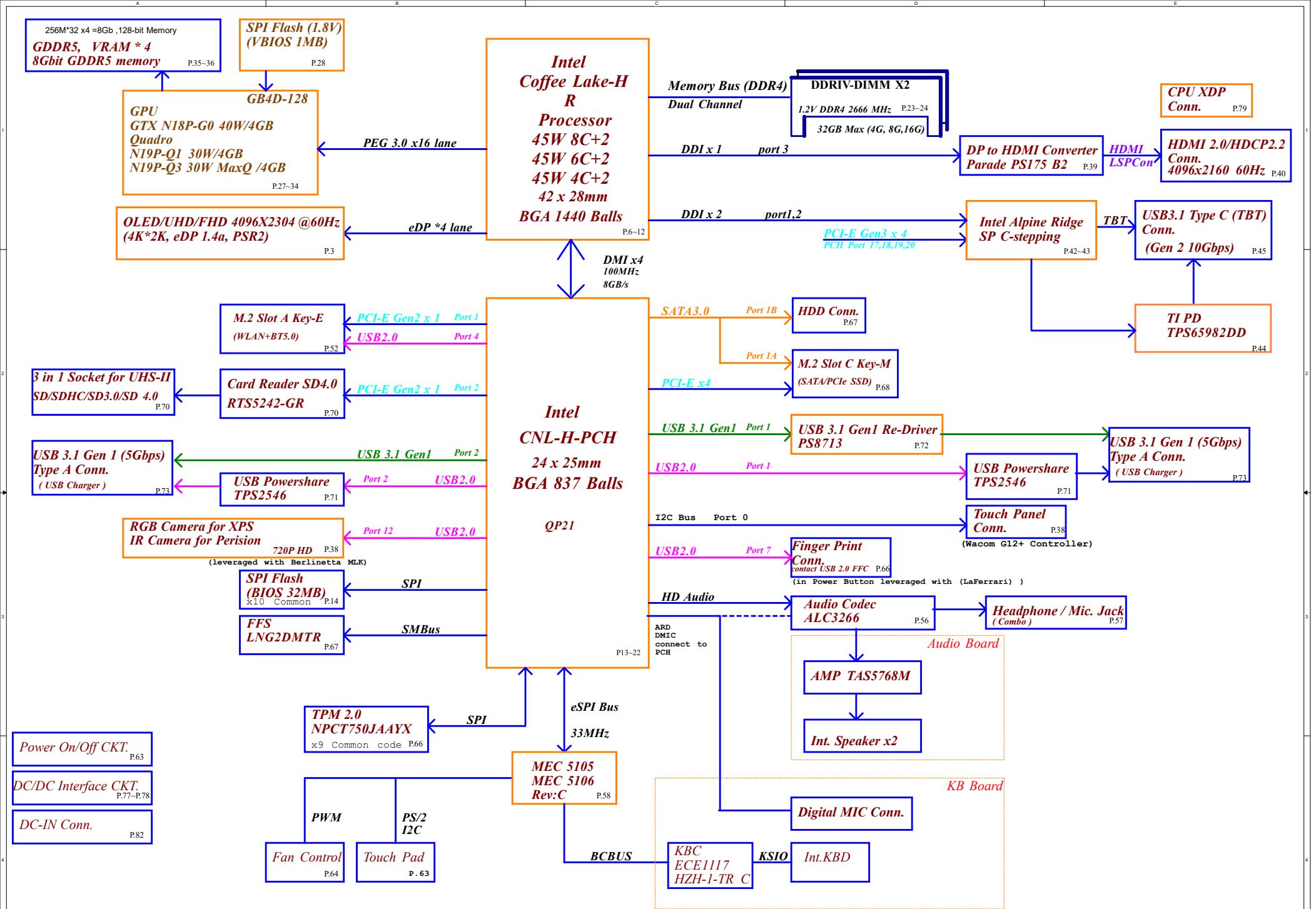
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2019-04-30

Rev: PVT 1.0 (A00)

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@EMC@	N19PQ1@
@RTD3@	N19PQ3Q@
CONN@	N18PG0VRAMH@
TP@	N18PG0VRAMM@
3PHASE15@	N18PVRAMS@
4PHASE62@	N19PQVRAMH@
4PHASE82@	N19PQVRAMM@
EMC@	NVPRO@
IRCAM@	VPRO@
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RE67	CE51	REV	PHASE
240K 4700p			PRE EVT
130K 4700p	X00		EVT
62K 4700p	X01		DVT1
33K 4700p	X02		DVT2
8.2K 4700p			
4.3K 4700p			
2K 4700p			
1K 4700p	A00		PVT

USB3.1	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	None
5	None
6	None

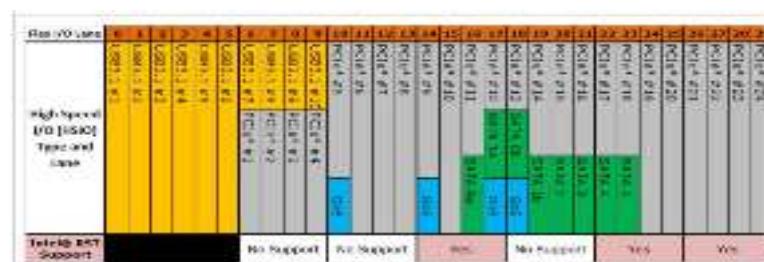
USB 2.0	DESTINATION
1	USB Conn 1 (Right Side)
2	USB Conn 2 (Left Side)
3	None
4	NGFF-1 WLAN + BT
5	None
6	None
7	Finger Print
8	None
9	None
10	None
11	None
12	RGB CAMERA

USB OC#	DESTINATION
0	USB Conn 1 (Right Side)
1	USB Conn 2 (Left Side)
2	
3	
4	
5	
6	
7	

PCI EXPRESS	DESTINATION	USB3.0	DESTINATION
Lane 1	NGFF-1 WLAN + BT	7	None
Lane 2	None	8	None
Lane 3	None	9	None
Lane 4	None	10	None
Lane 5	CARD READER		
Lane 6	None		
Lane 7	None		
Lane 8	None		
Lane 9	SSD		
Lane 10	SSD	SATA	DESTINATION
Lane 11	SSD	0A	N/A
Lane 12	SSD	1A	SSD
Lane 13	None	0B	N/A
Lane 14	None	1B	N/A
Lane 15	None	2	HDD
Lane 16	None	3	N/A
Lane 17		4	N/A
Lane 18	Alpine Ridge	5	N/A
Lane 19			
Lane 20			

DDI	DESTINATION
1	Alpine Ridge
2	Alpine Ridge
3	HDMI 2.0

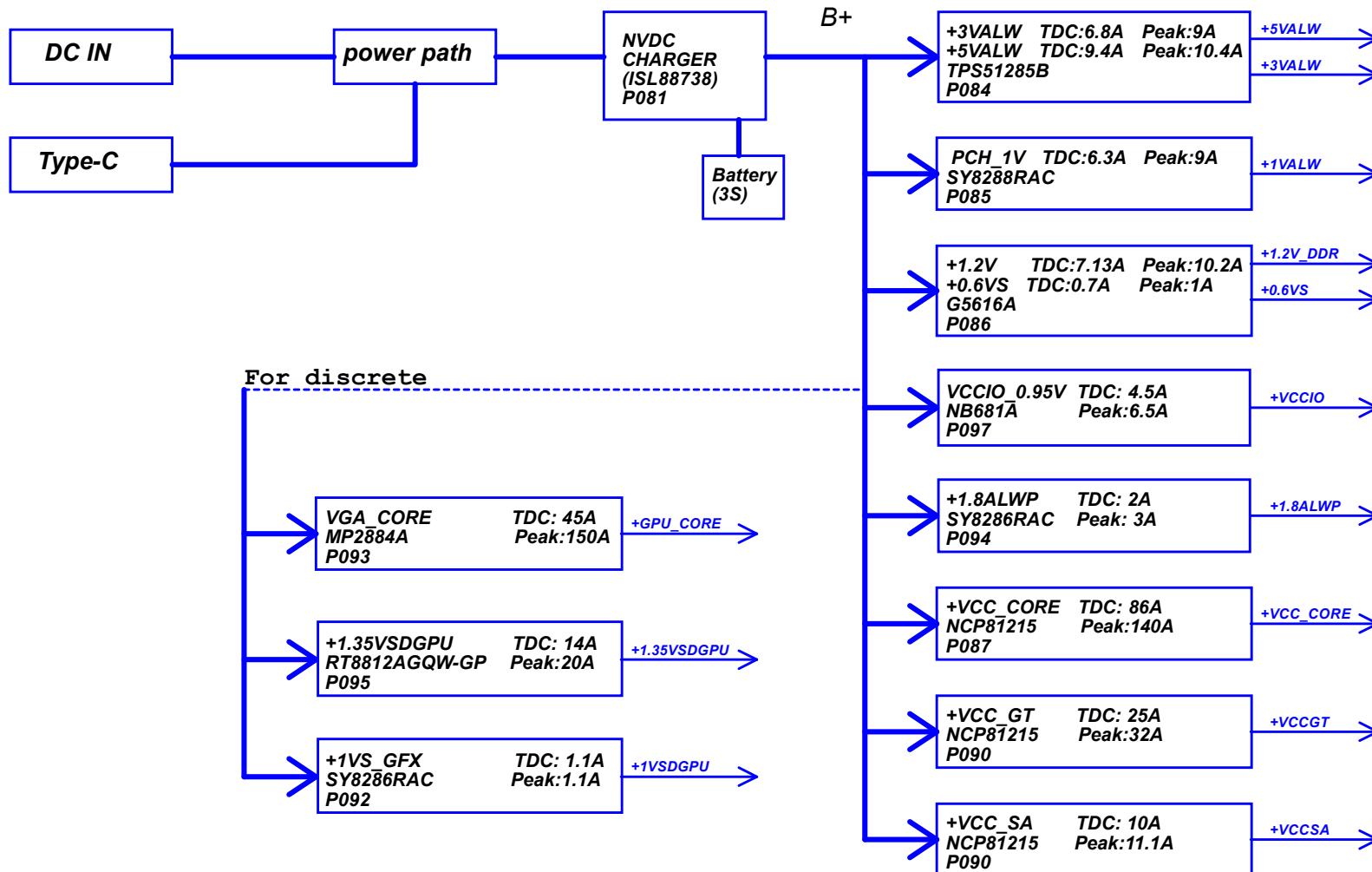
LPC	DESTINATION
ESPI/LPC0	MEC5105
LPC1	DEBUG PORT



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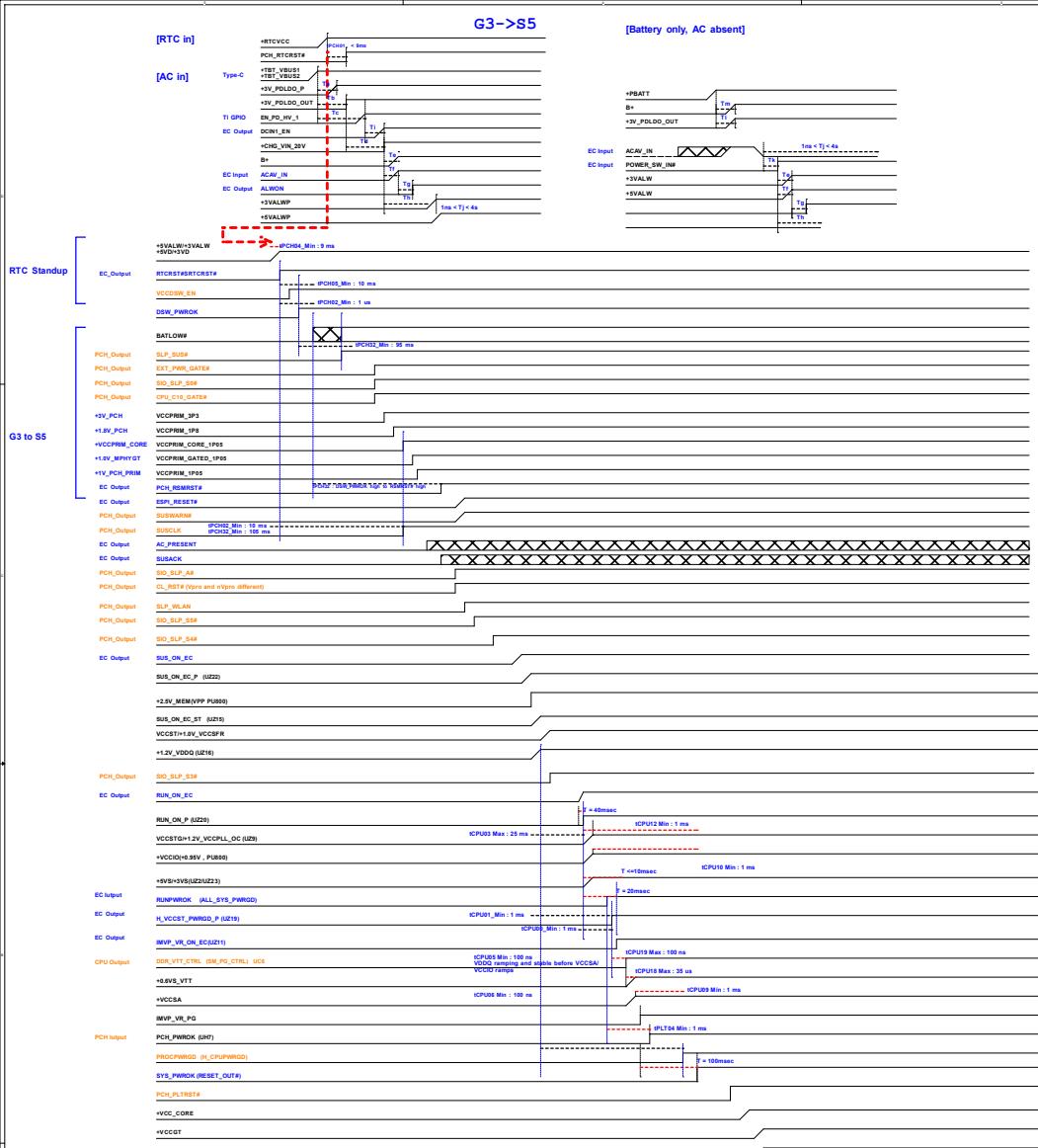
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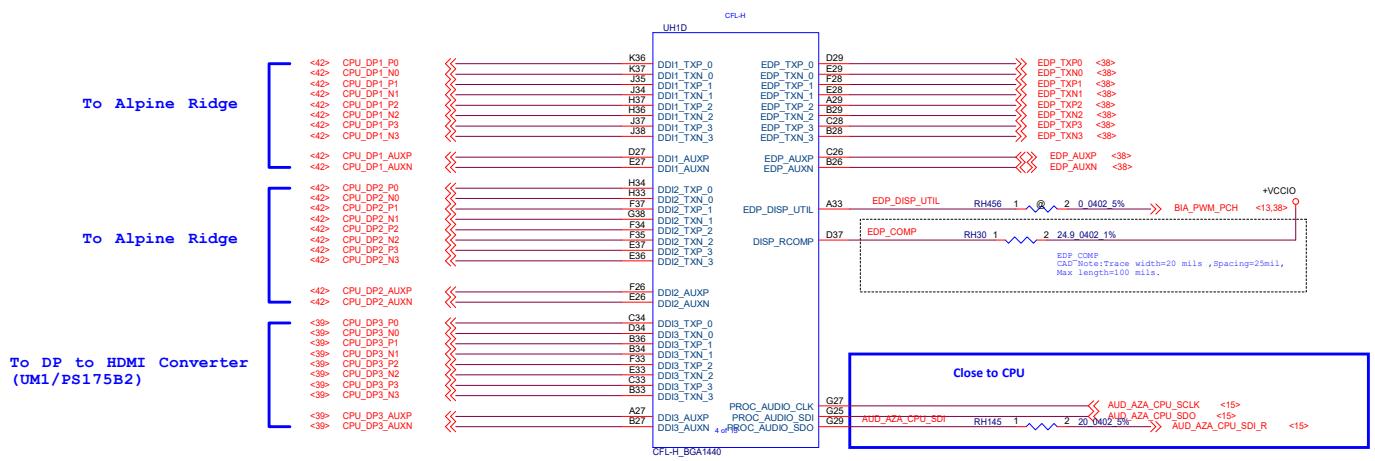
The 30 HSIO lanes on PCN-R supports the following configurations:
1. Up to 24 PCIe* Lanes
- 1x 4x PCIe* 3.0 Ports (or devices) can be enabled.
• When a GbE Port is enabled, the maximum number of PCIe* Ports (or devices) that can be enabled reduces based off of the following:
Max PCIe* Lanes (or devices) = GbE [0 ~ 1]
- PCIe* Lanes 1-4 (PCIe* Controller #1), 5-8 (PCIe* Controller #2), 9-12 (PCIe* Controller #3), 13-16 (PCIe* Controller #4), 17-20 (PCIe* Controller #5), and 21-24 (PCIe* Controller #6) can be individually configured
2. Up to 6 SATA* Lanes
- Up to a maximum of 6 SATA Ports (or devices) can be enabled.
- SATA Lane 0 has the flexibility to be mapped to Flex I/O Lane 16 or 18
- SATA Lane 1 has the flexibility to be mapped to Flex I/O Lane 17 or 19
3. Up to 10 GbE 3.1 Lanes
- Up to a maximum of 10 GbE Ports (or devices) can be enabled
4. Up to 4 GbE Lanes
- Supports up to 4 GbE Ports (or devices) can be enabled
5. Supports up to 3 Remapped (Intel Rapid Storage Technology) PCIe* storage devices
- x2 End x4 PCIe* NVMe SSD
- x2 Intel Optane™ Memory Device
- 3rd Party Remap (PCIe*) chapter for the PCN PCIe* Controllers, configuration, and lanes that can be used for Intel® Rapid Storage Technology PCIe* storage support
6. For unused SATA/PCIe* Combo Lanes, Flex I/O Lanes that can be configured as PCIe* or SATA, the lanes must be statically assigned to SATA or PCIe* via the SATA/PCIe* Combo Port Soft Switching feature in the GbE Programming Guide and through the Intel Flash Image Tool (FIT) tool.



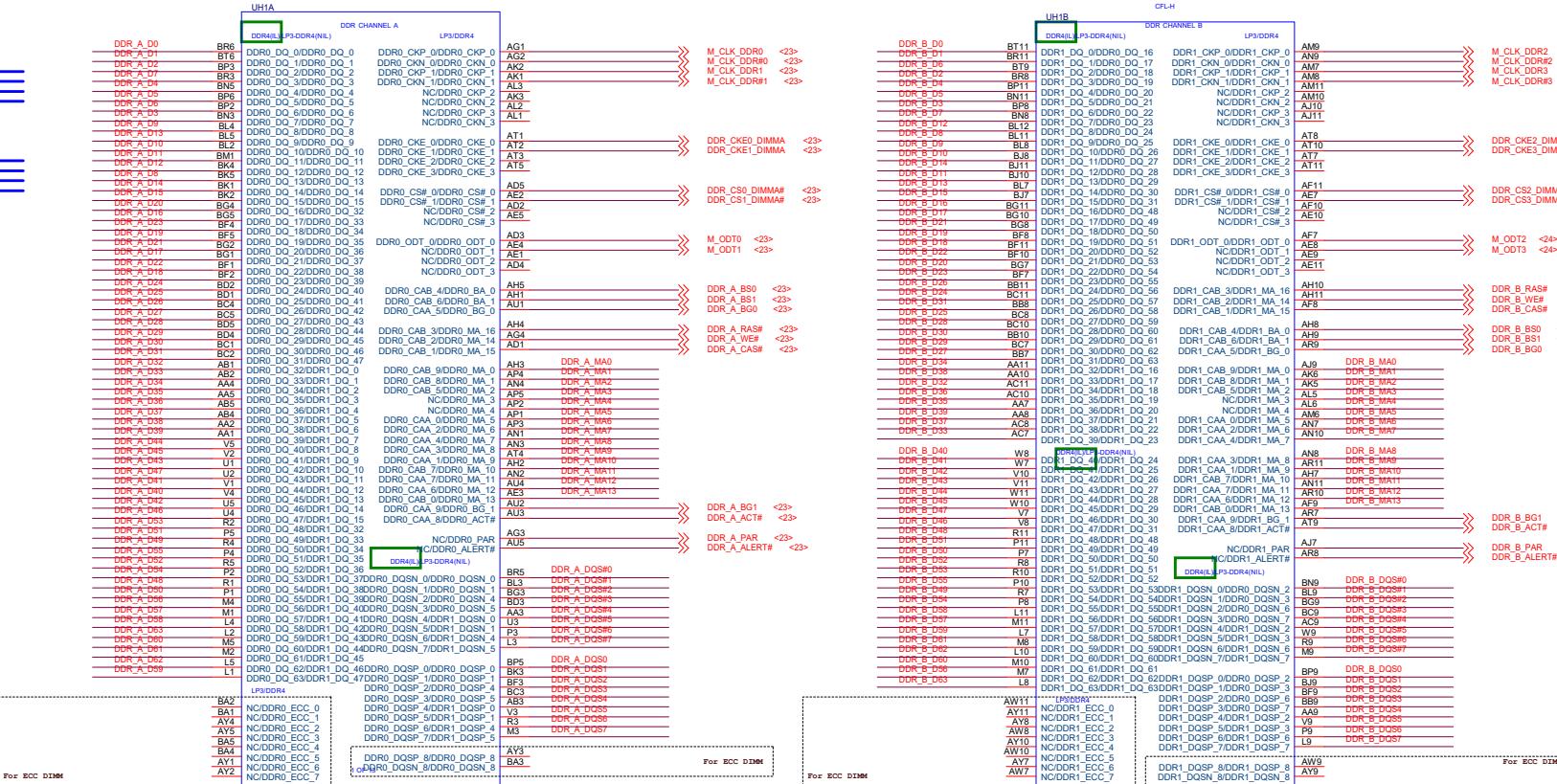
@ : Nopop Component
 @DIS@ : Nopop Component
 DIS@: POP for discrete GPU SKU

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Interleave



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CPU(2/7) DDR

umber

April 30, 2010

CFG Straps for Processor

Stall reset sequence after PCU PLL lock until de-asserted	
CFG0	<ul style="list-style-type: none"> * 1 = (Default) Normal Operation; No stall. 0 = Stall.

CFG0 1 @ 2
RH183 1K 0402 5%



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port
	* 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

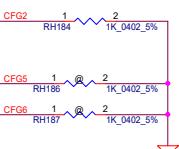
1 : Disabled; No Physical Display Port

0 : Enabled; An external Display Port device is connected to the Embedded Display Port



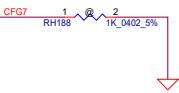
PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

```
1: (Default) x16 - Device 1 functions 1 and 2 disabled  
0: x8, x8 - Device 1 function 1 enabled ; function 2  
    disabled  
1: Reserved - (Device 1 function 1 disabled ; function  
    2 enabled)  
2: 0, 4, 8 - Device 1 function 1 and 2 enabled
```



PEG DEFER TRAINING	
CFG7	* 1: (Default) PEG Train immediately following xxRES de assertion
	0: PEG Wait for BIOS for training

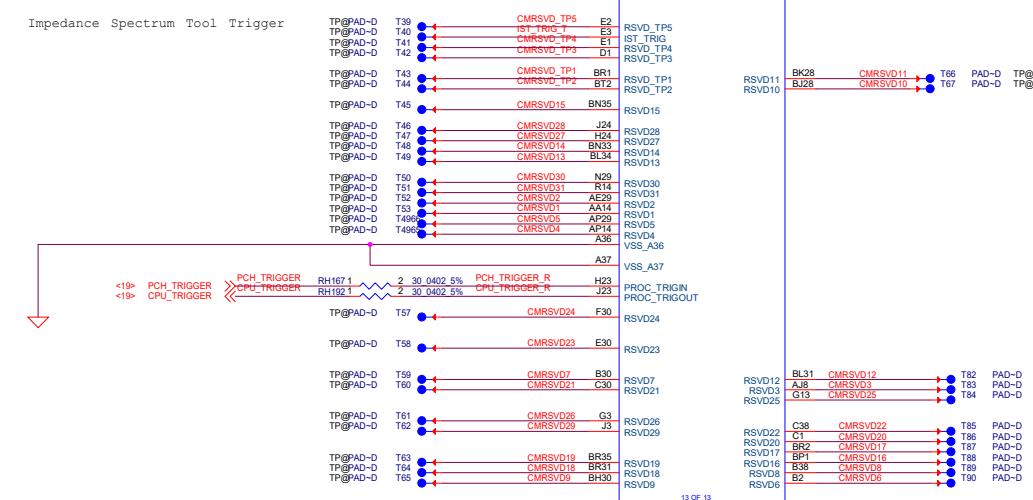
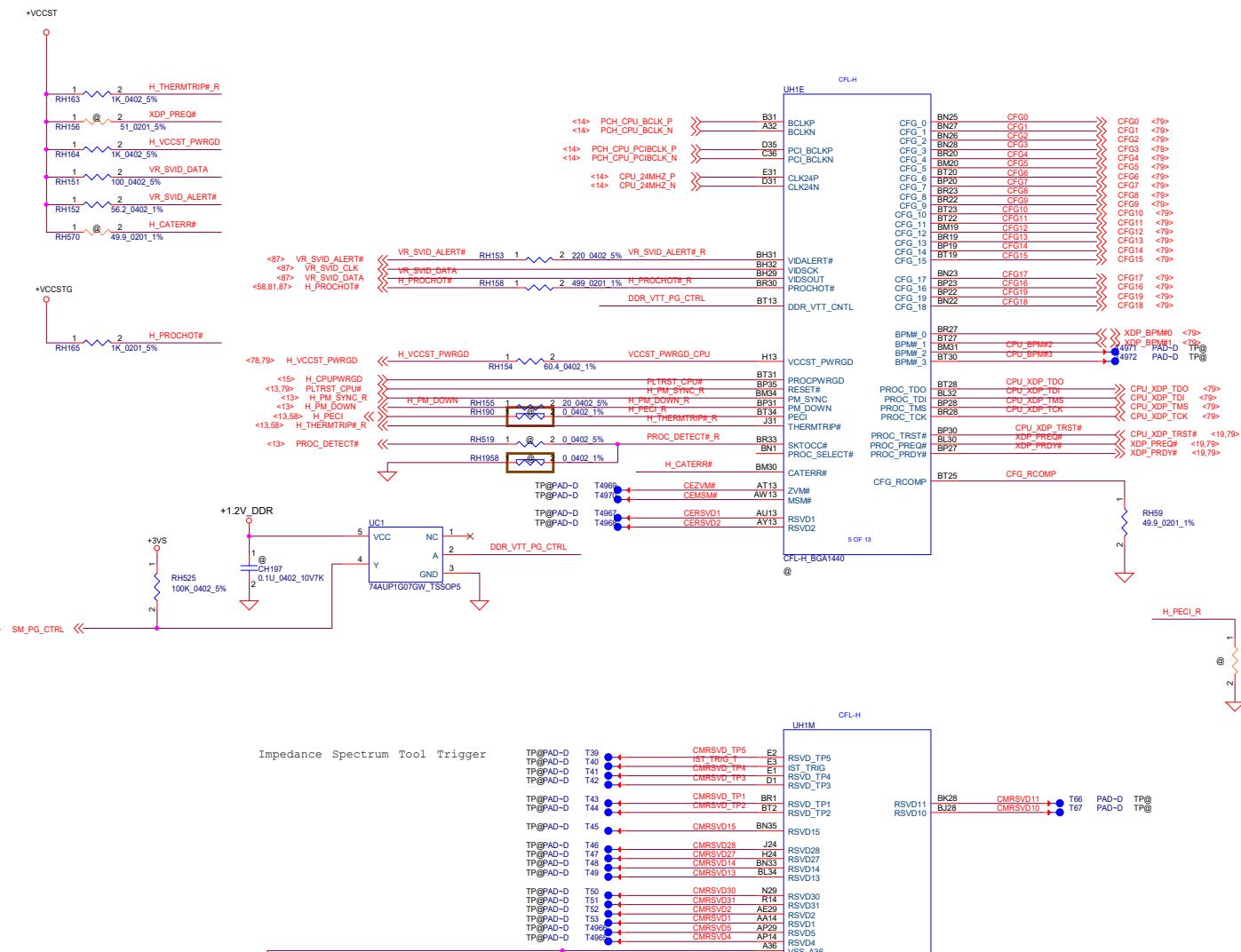
- 1: (Default) PEG Train immediately
de assertion
- 0: PEG Wait for BIOS for training



ANSWER: [ANSWER](#) | [ANSWER](#) | [ANSWER](#) | [ANSWER](#) | [ANSWER](#)

Part 2
 1. In the following sentence, underline the subject.
 2. Enclose the subject in parentheses in each sentence with fewer than two words. That is, change all of the following sentences to short subjects:
 a. The boy is playing.
 b. I am writing.
 c. The dog is barking.
 d. The children are running.

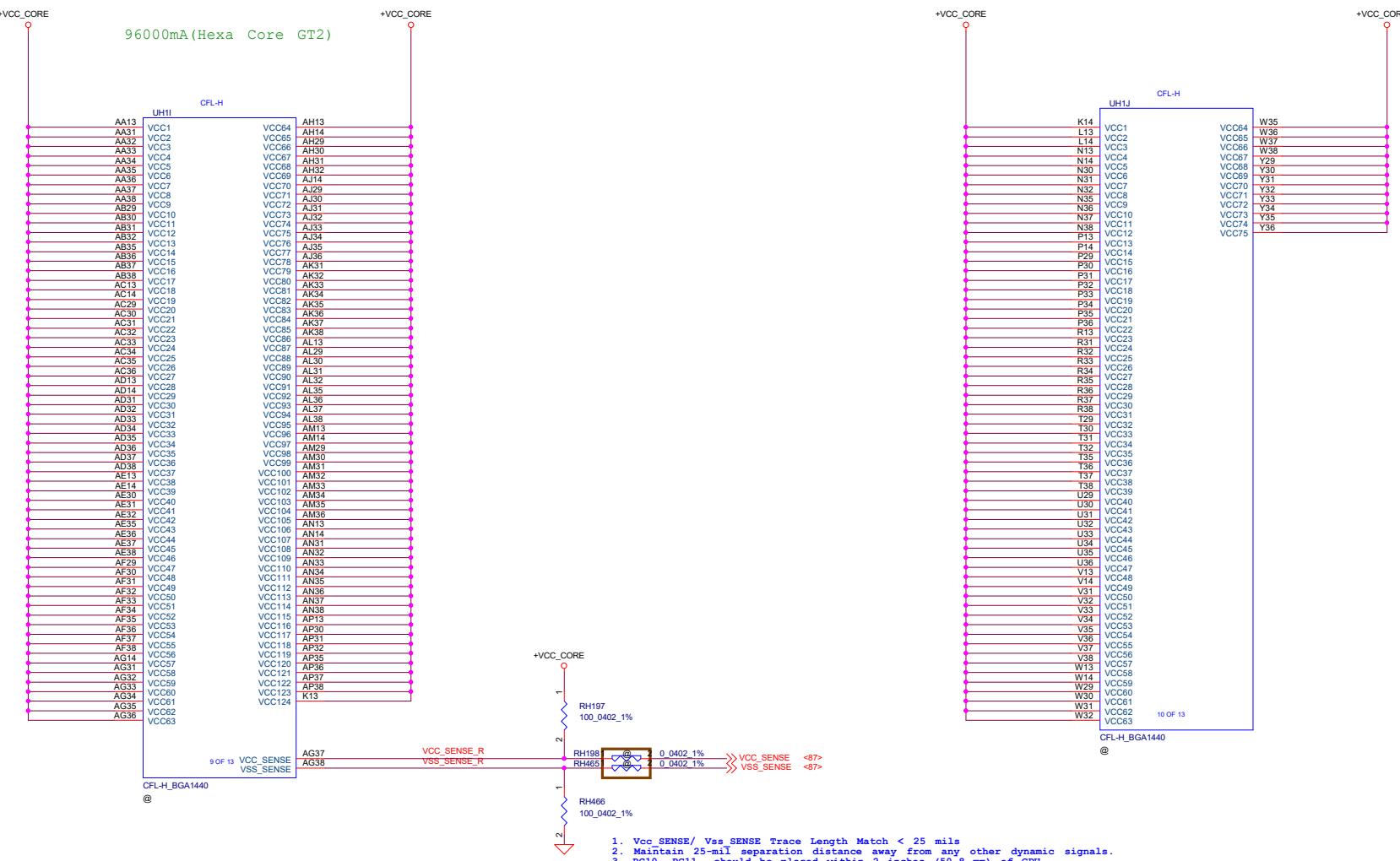
For example, if you have a 1000-kg mass, you should use 1000 kg. If you have a 100-kg mass, you should use 100 kg, and so on. Larger masses are always best, but smaller masses are also acceptable. In fact, it is better to have a small mass than a large one.



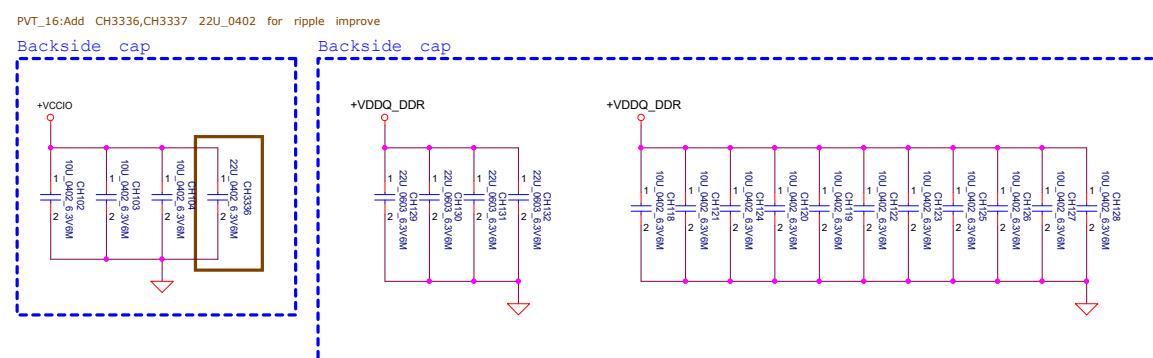
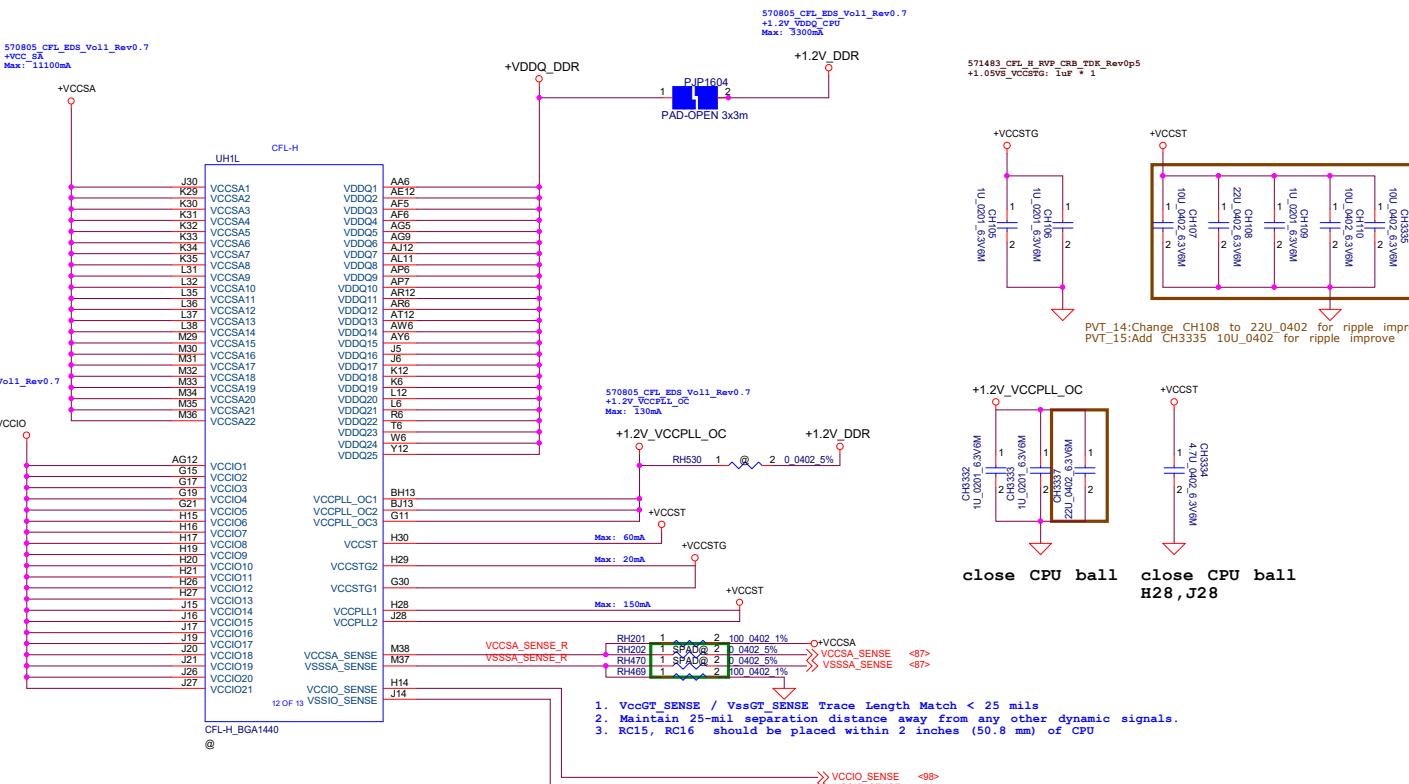
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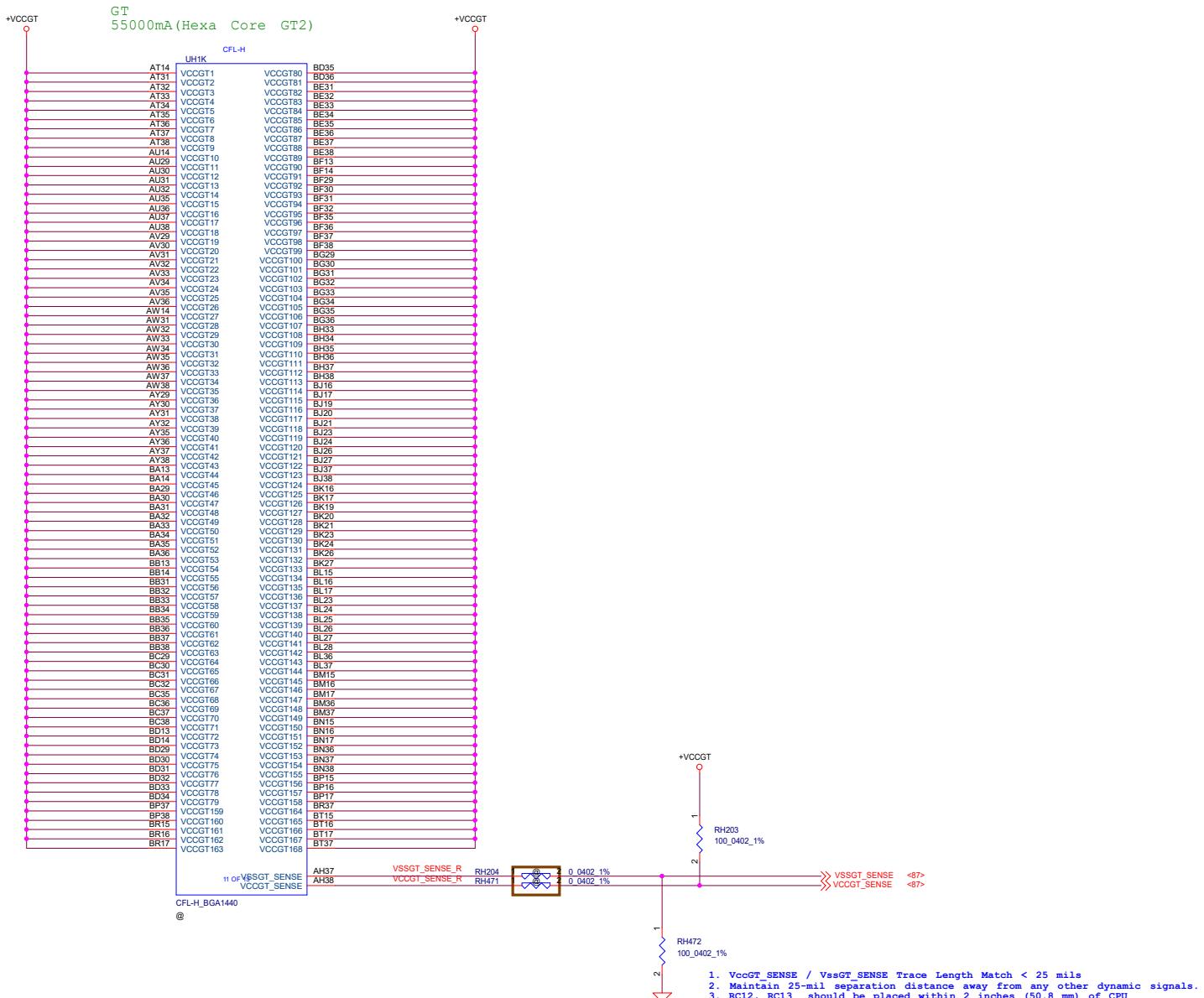
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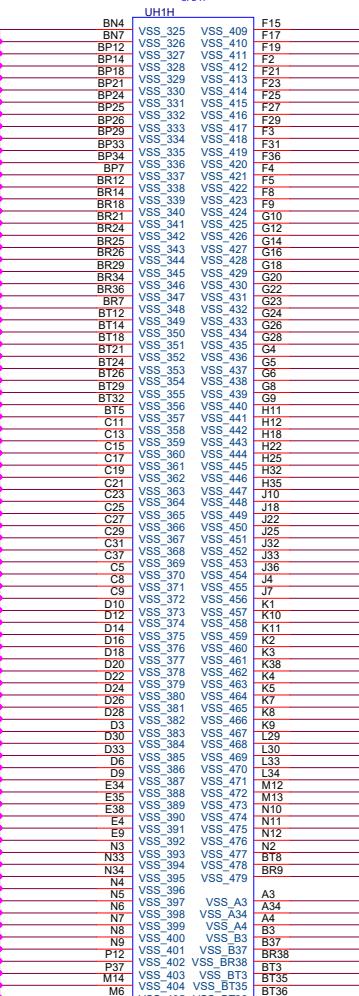
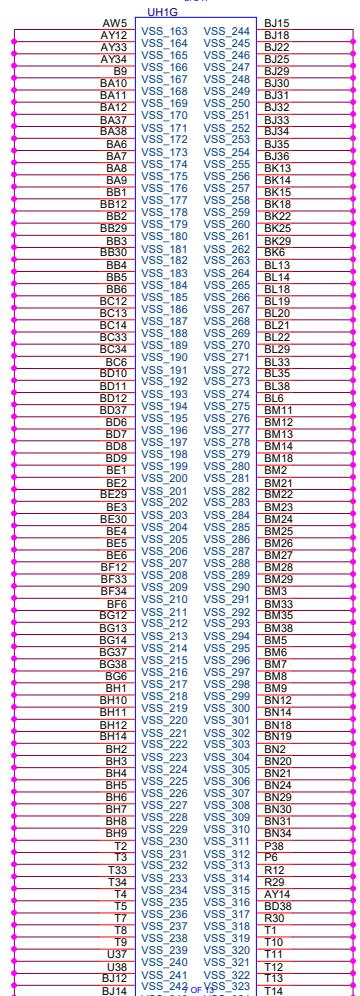
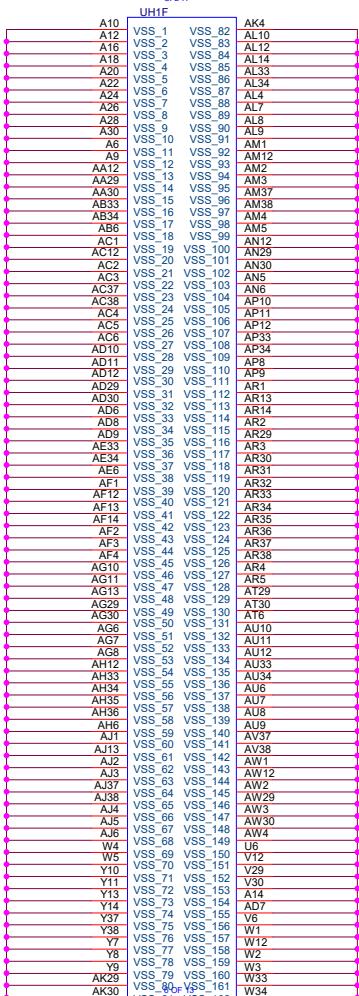
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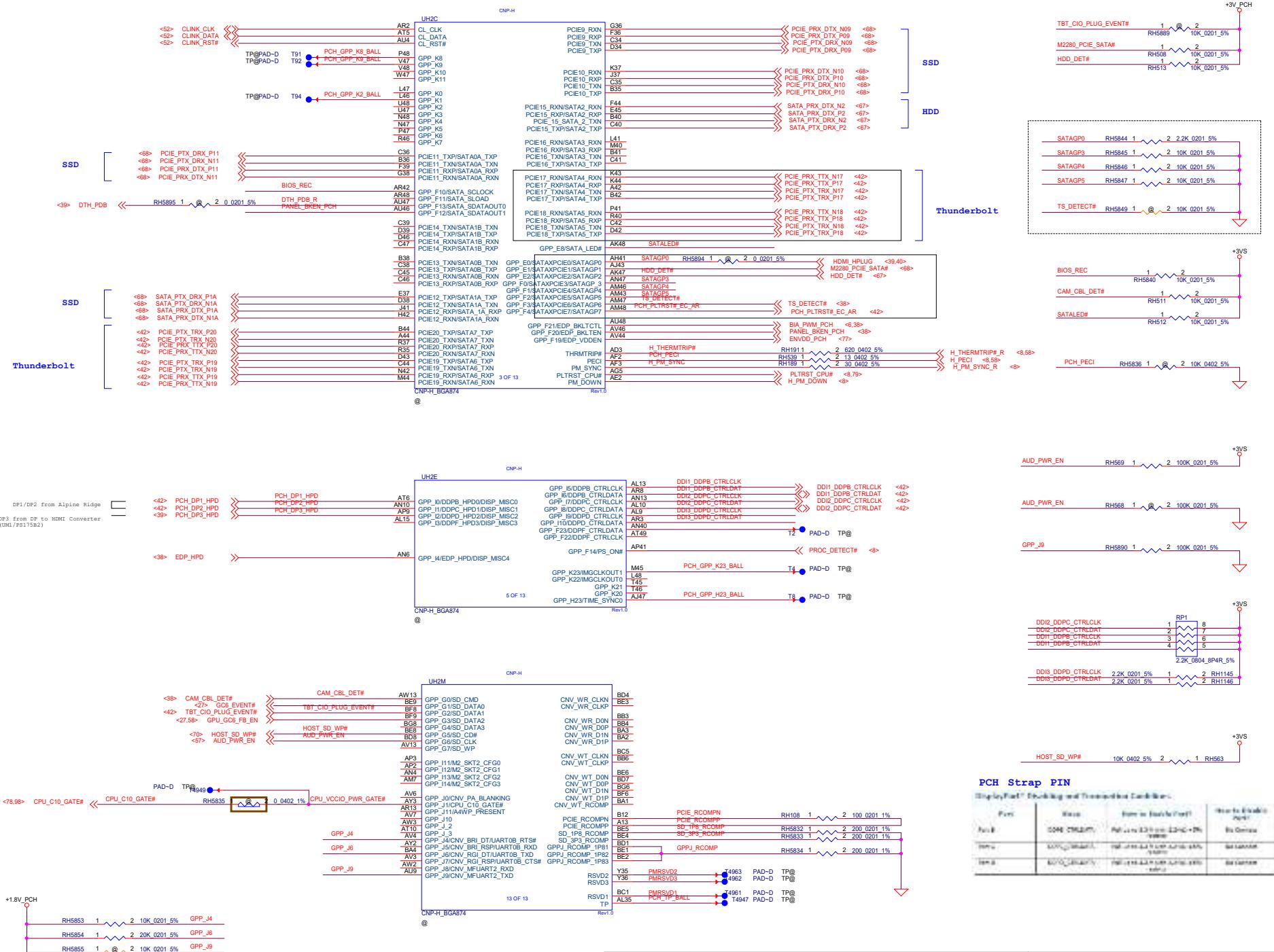
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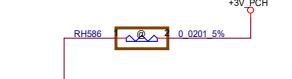
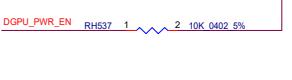
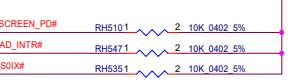
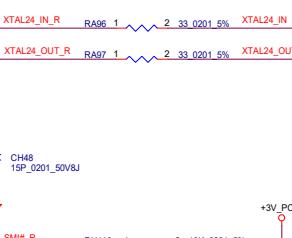
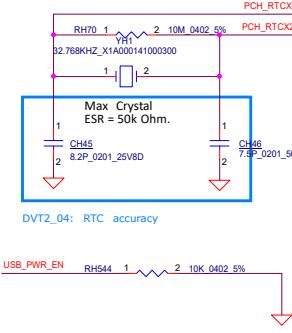
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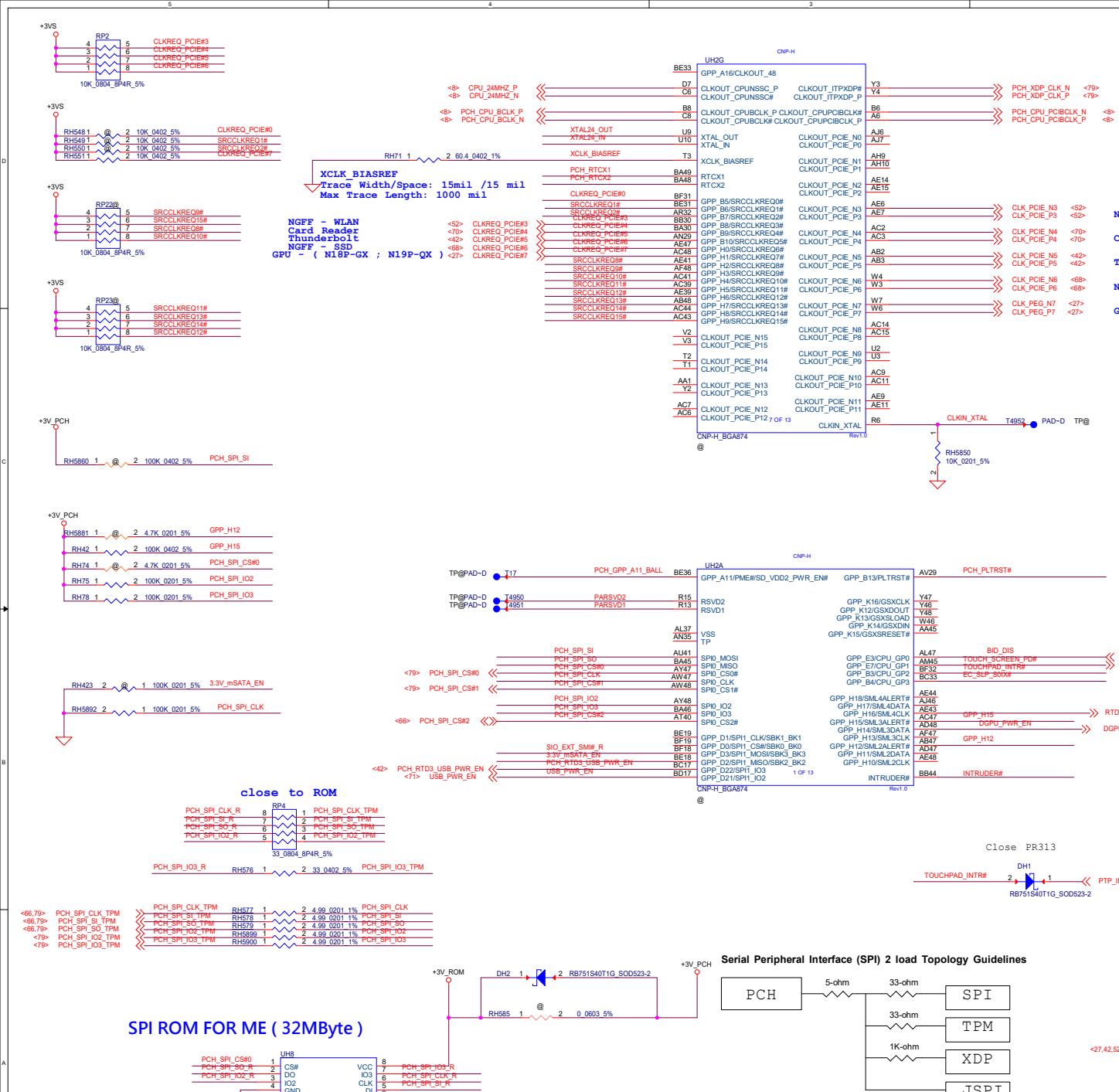
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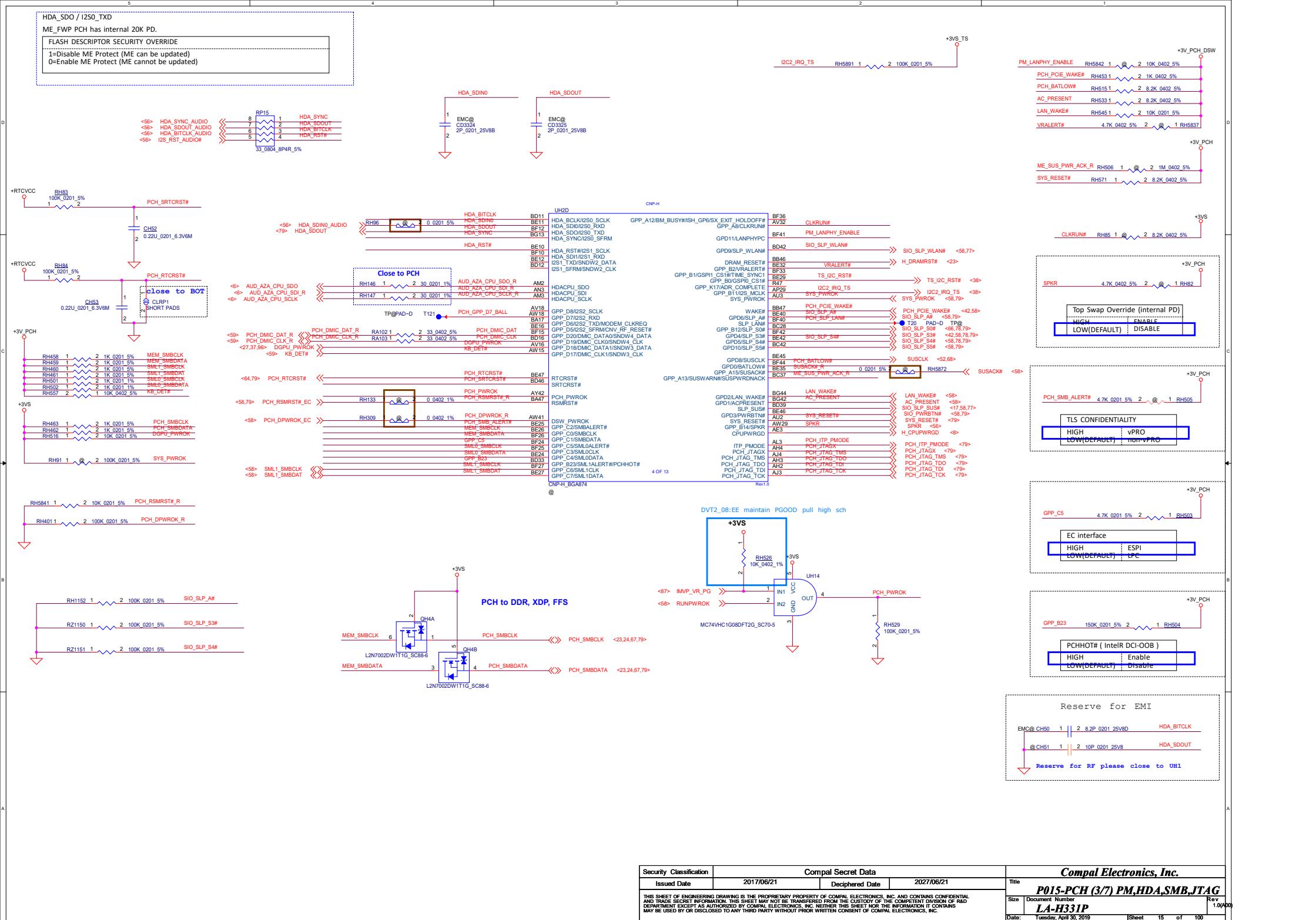
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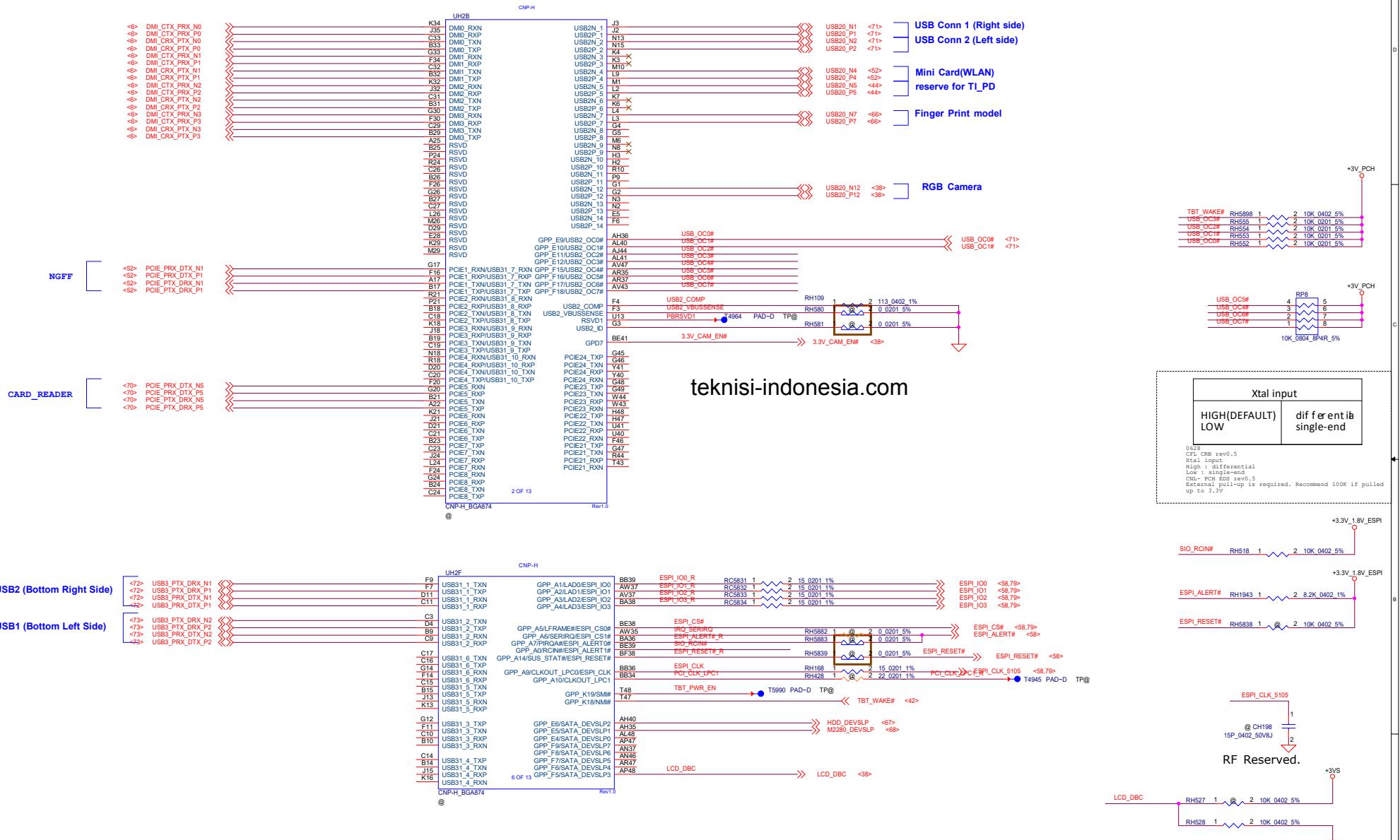
RTC CRYSTAL



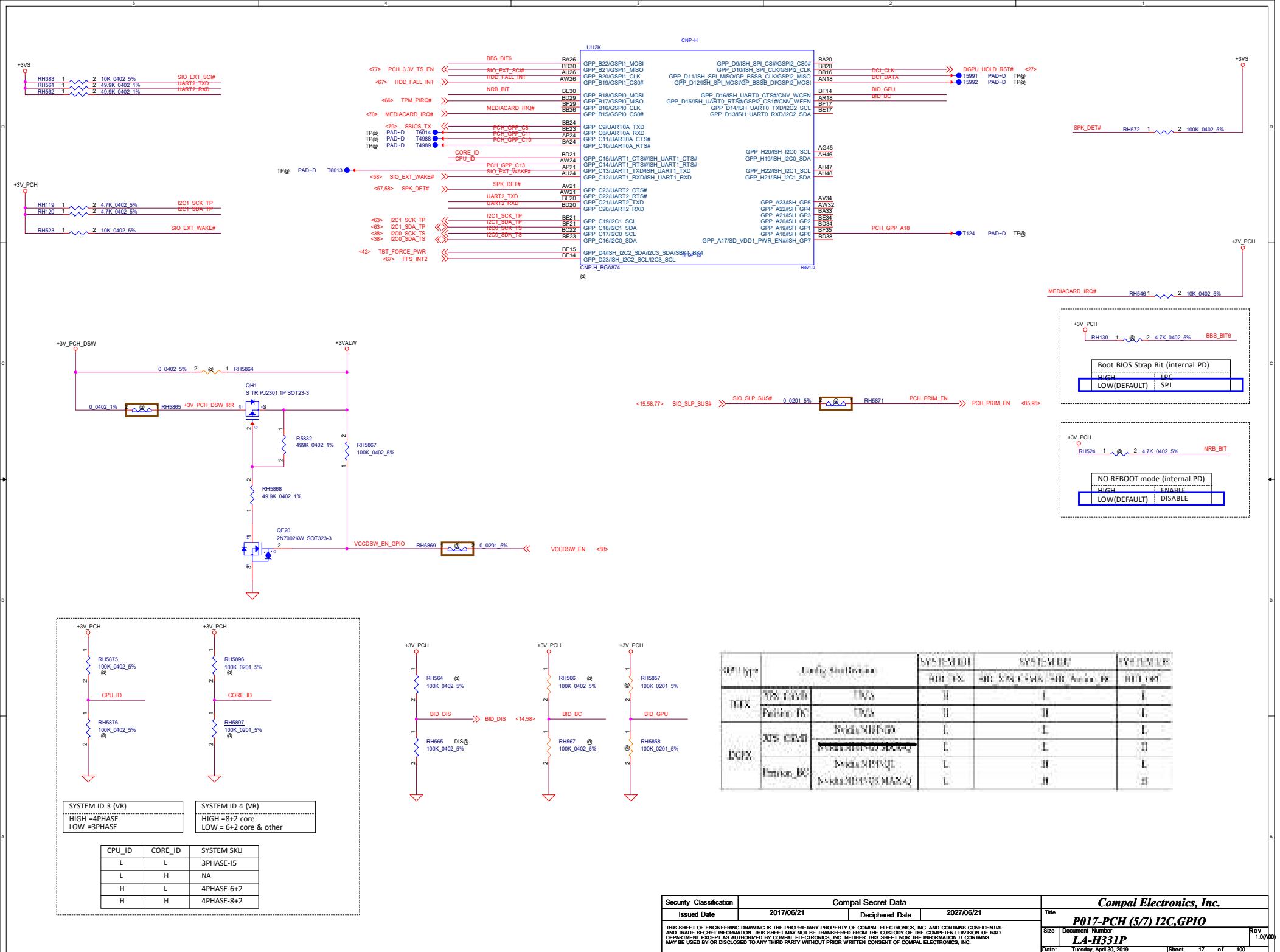
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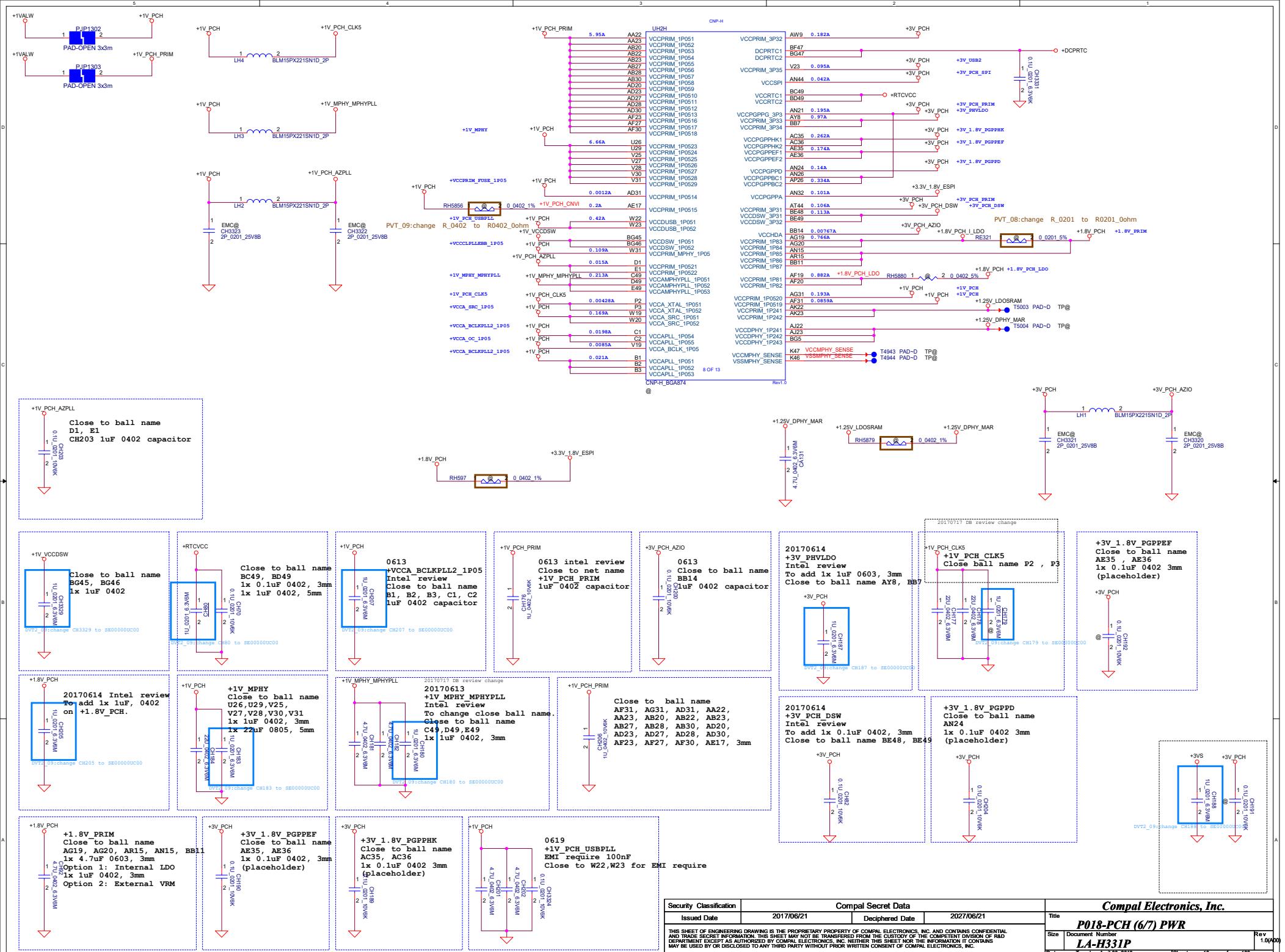


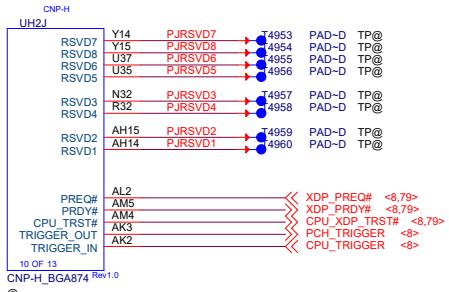
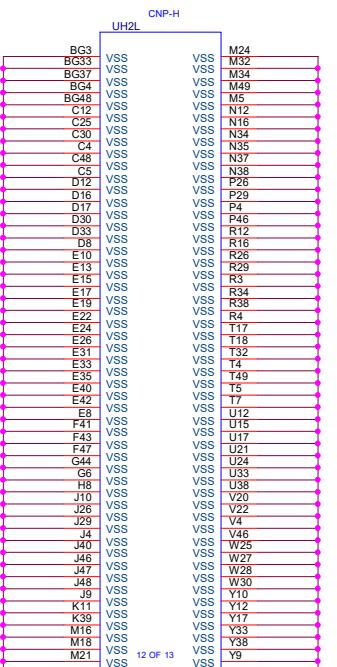
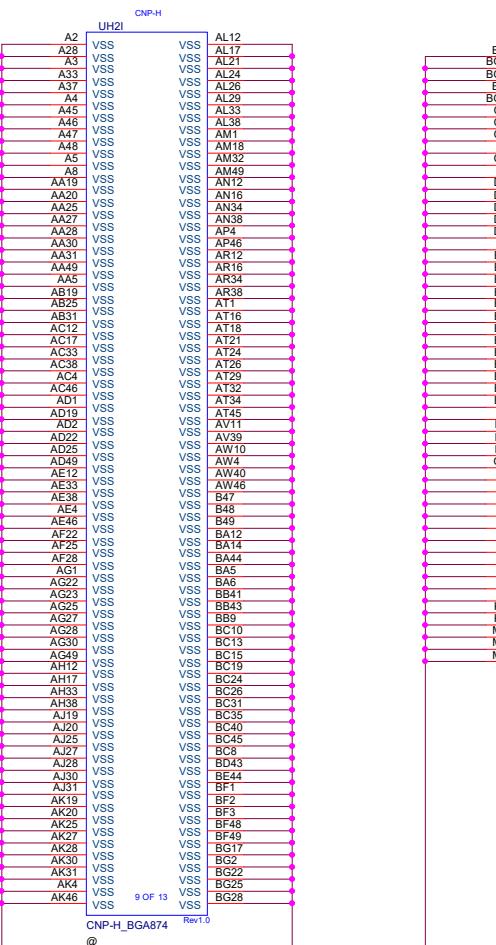




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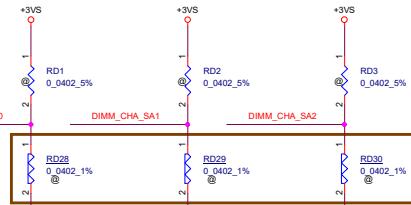
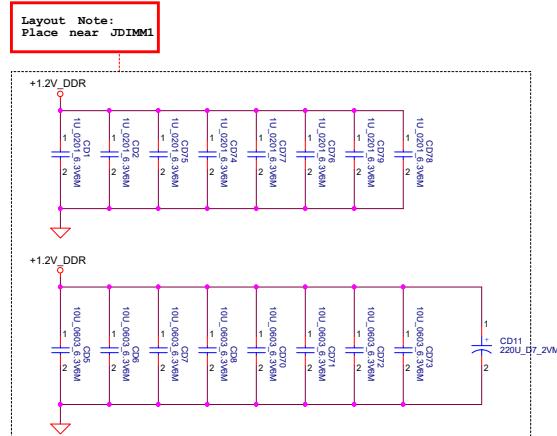
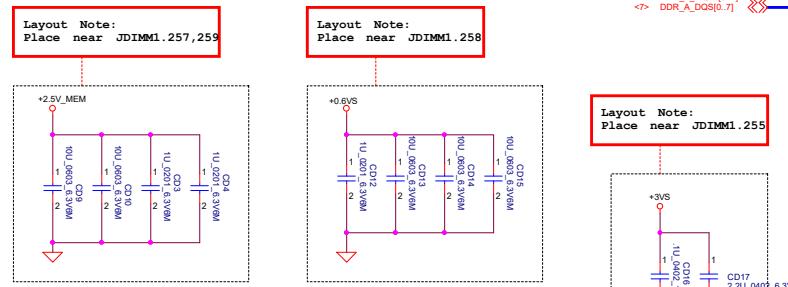
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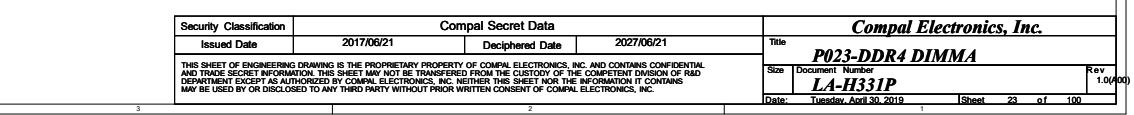
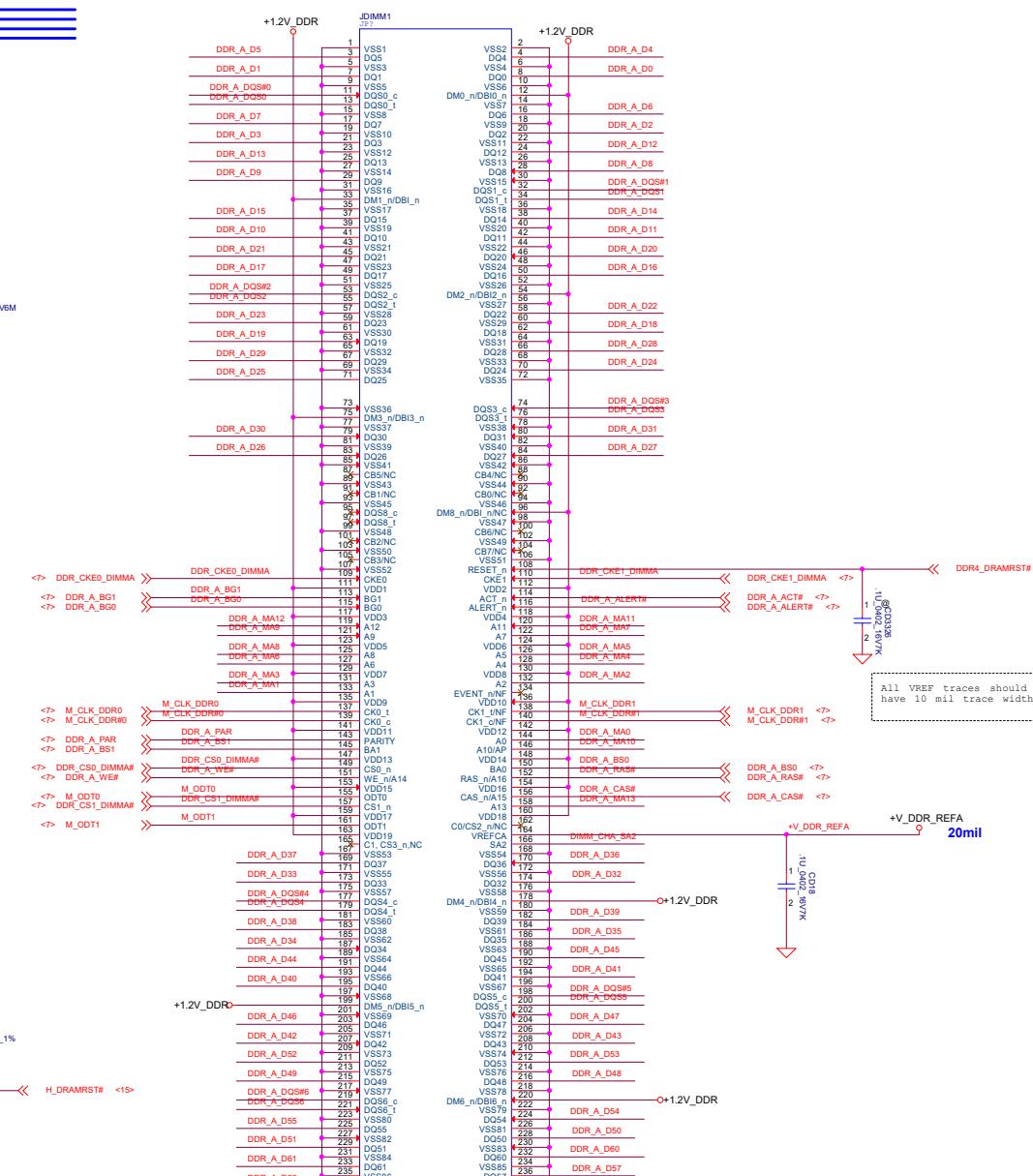
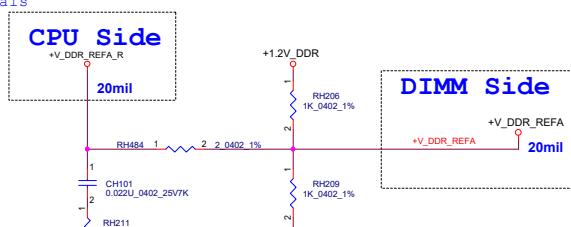
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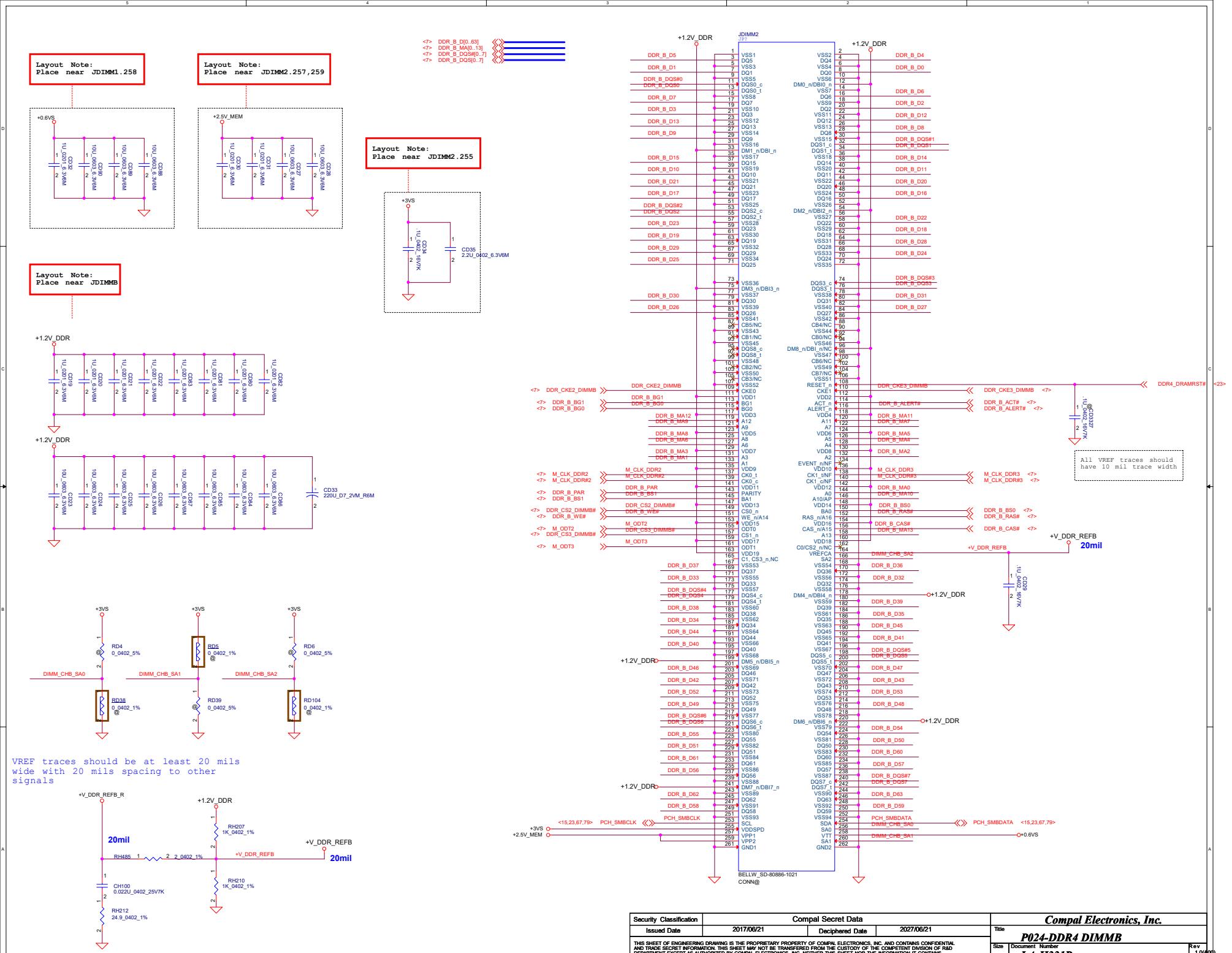
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VREF traces should be at least 20 mils wide with 20 mils spacing to other signals.





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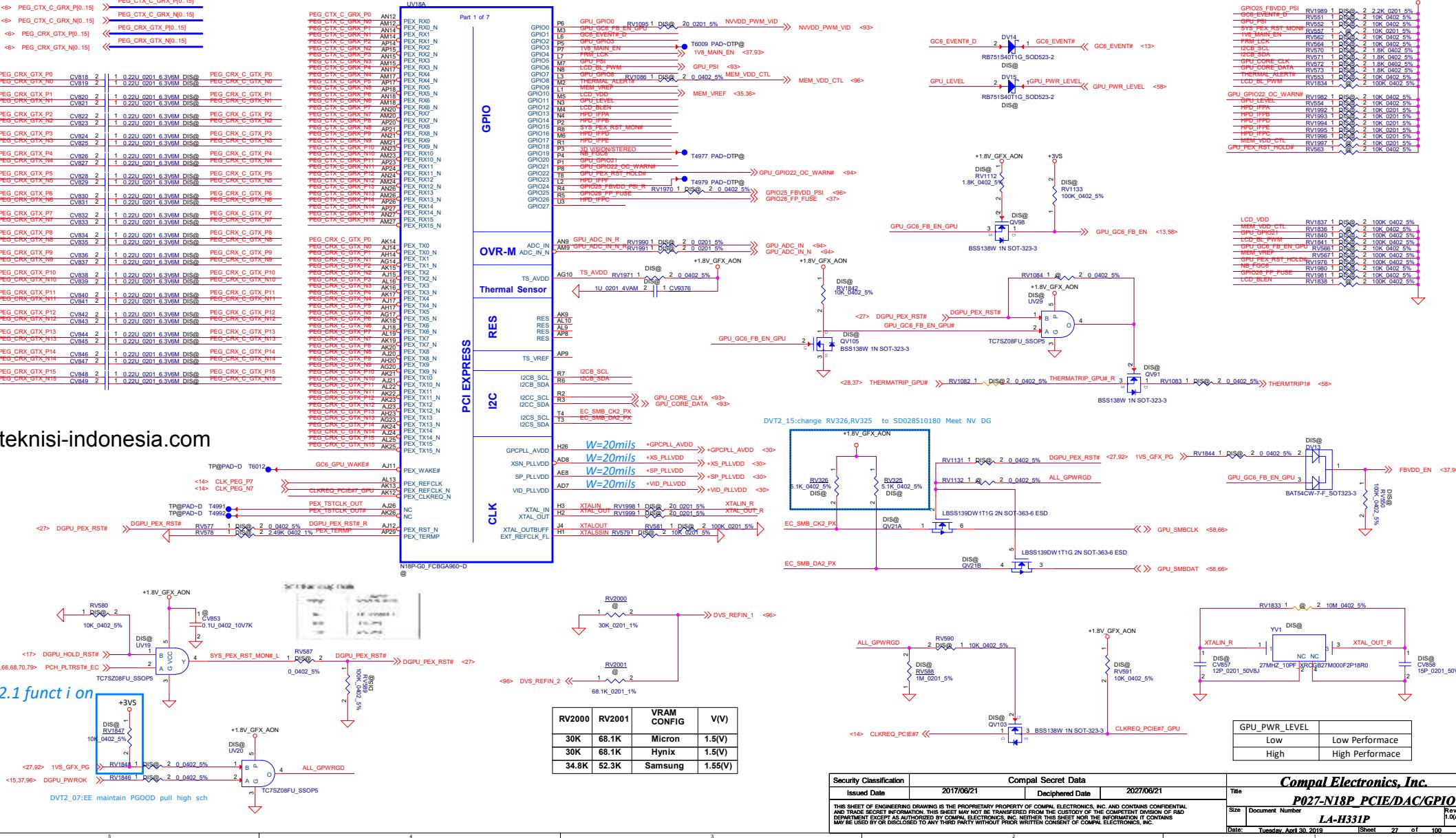
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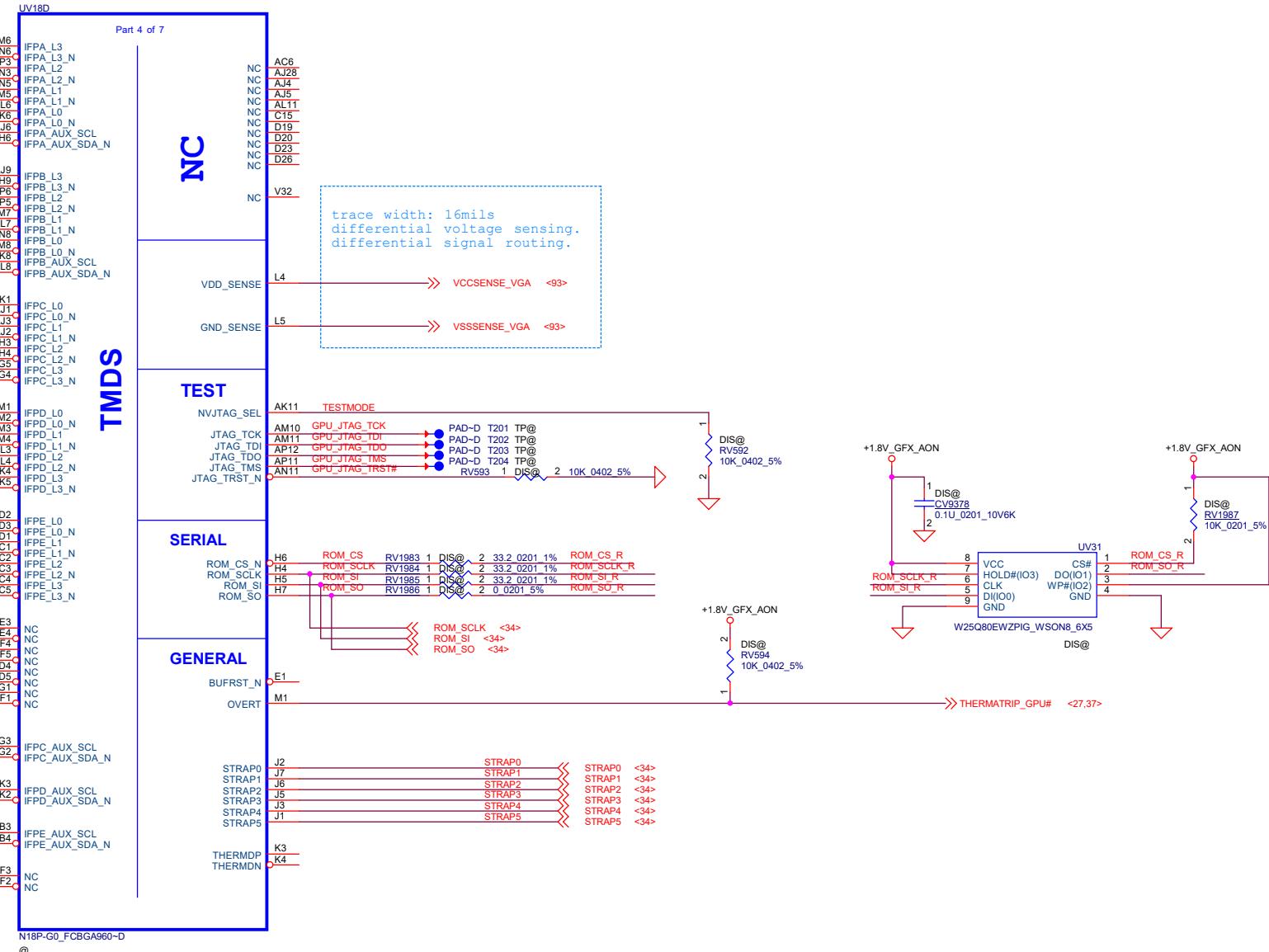
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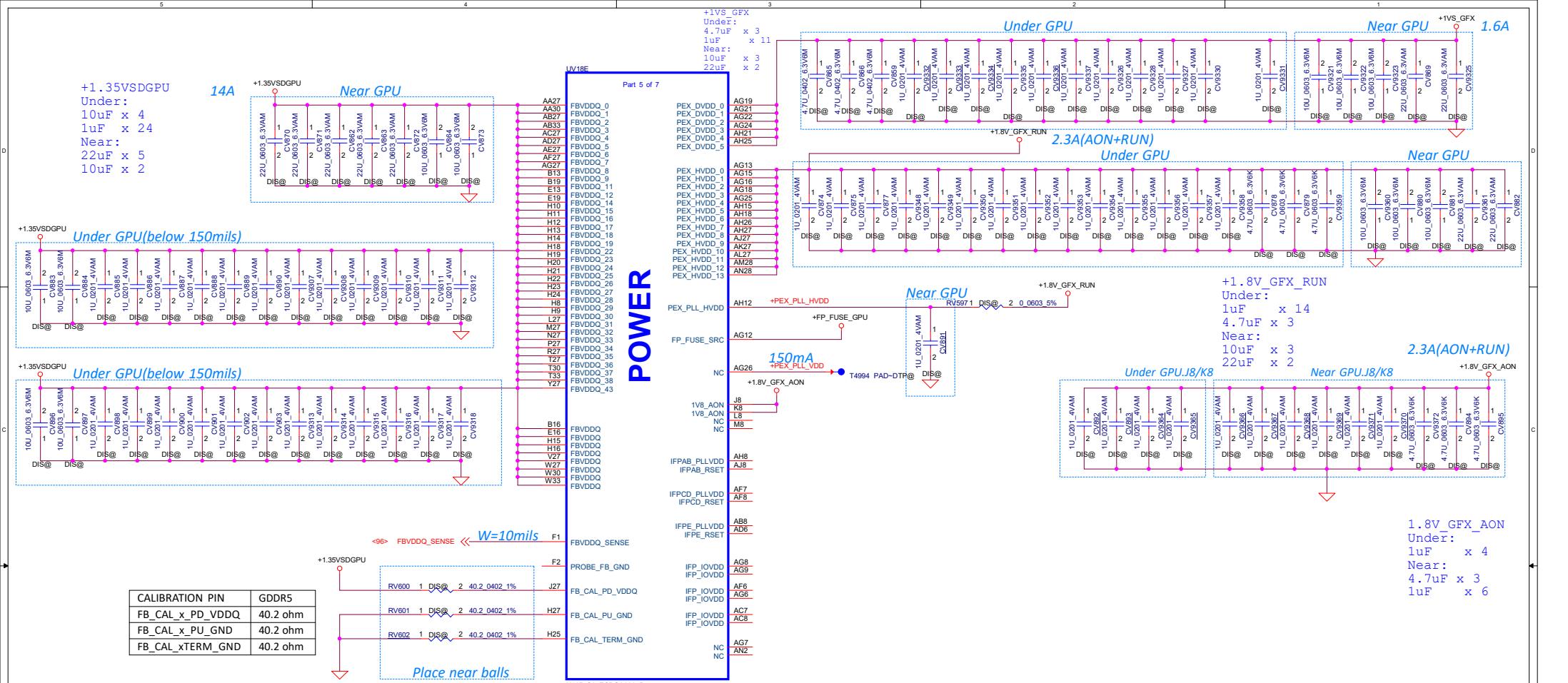
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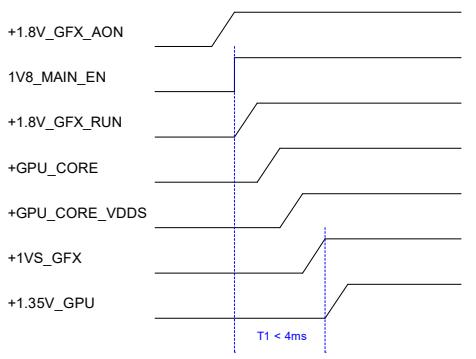




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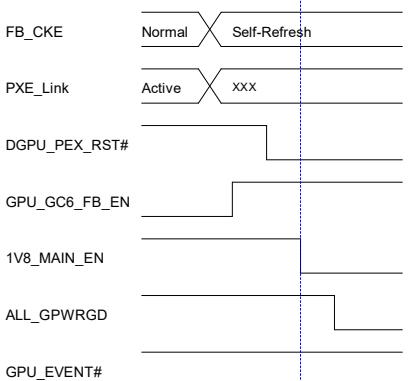


GPU Power Up Sequence



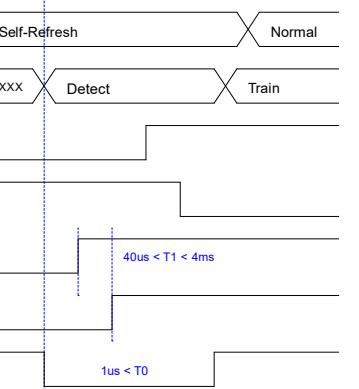
The ramp time for any rail must be more than 40us and less than 2ms.

GPU GC6 Entry Sequence

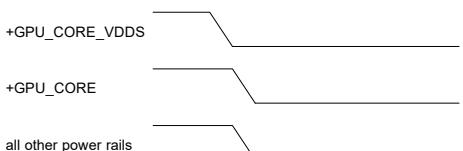


The entire entry/exit sequence must complete within 200 ms.

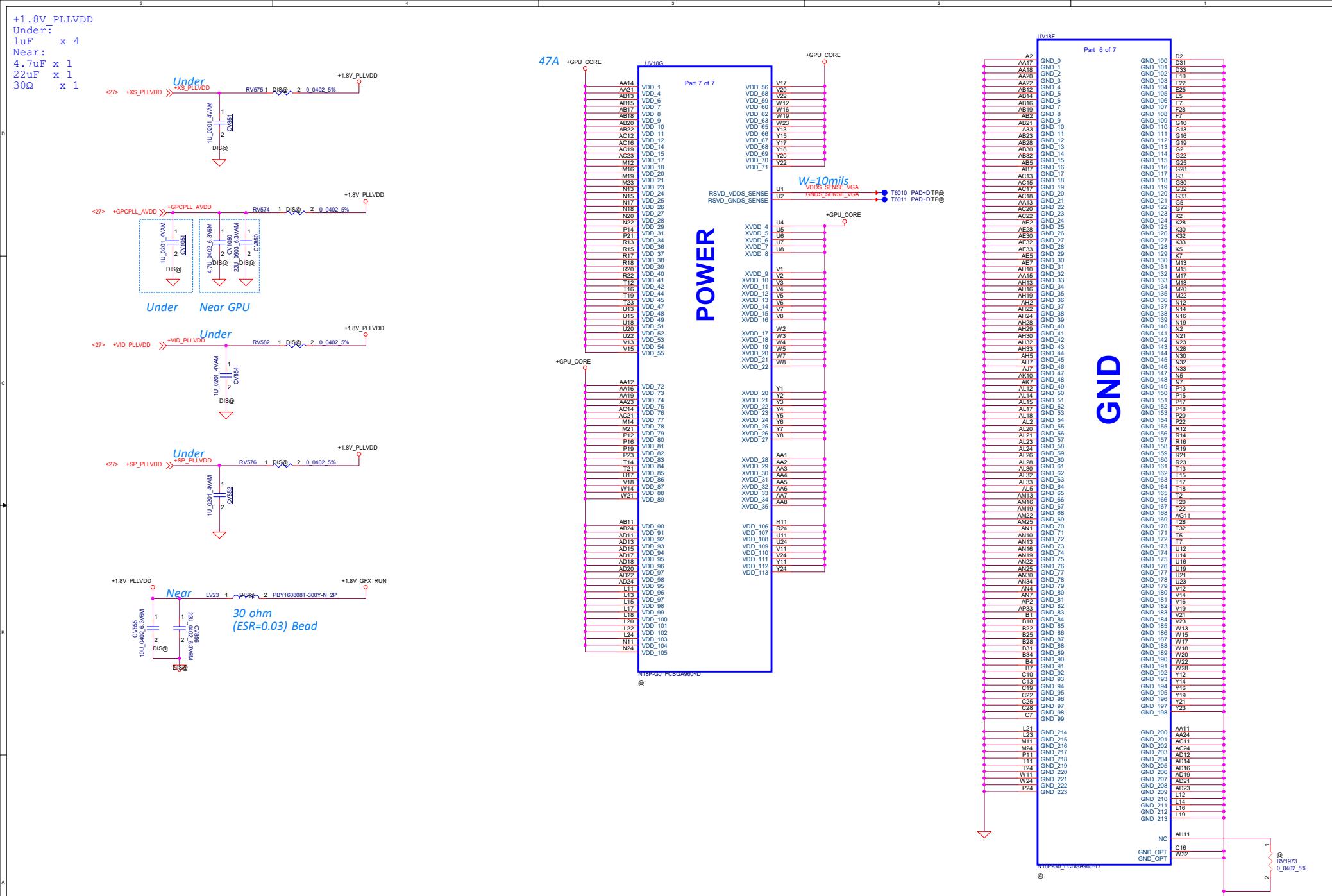
GPU GC6 Exit Sequence



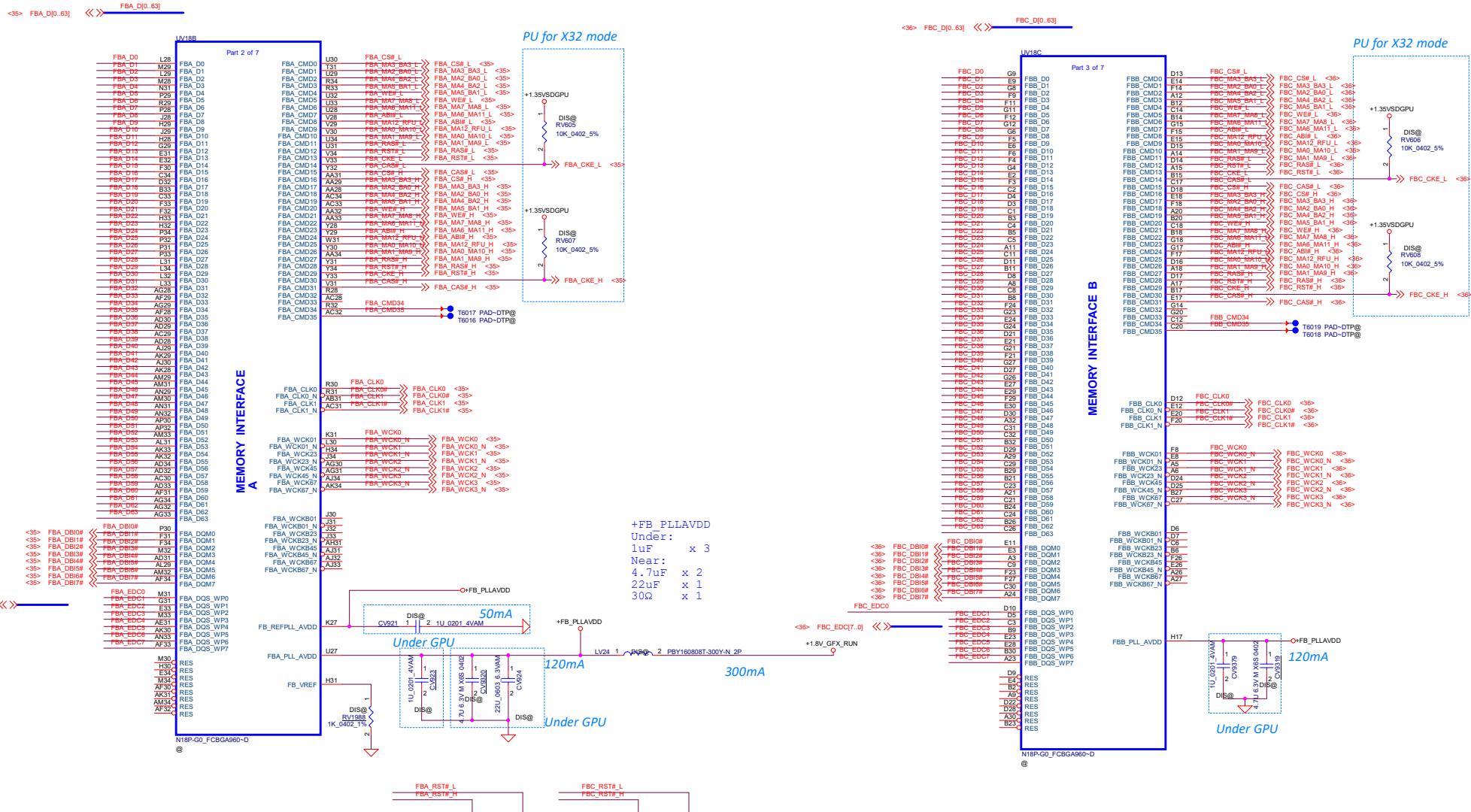
GPU Power Down Sequence



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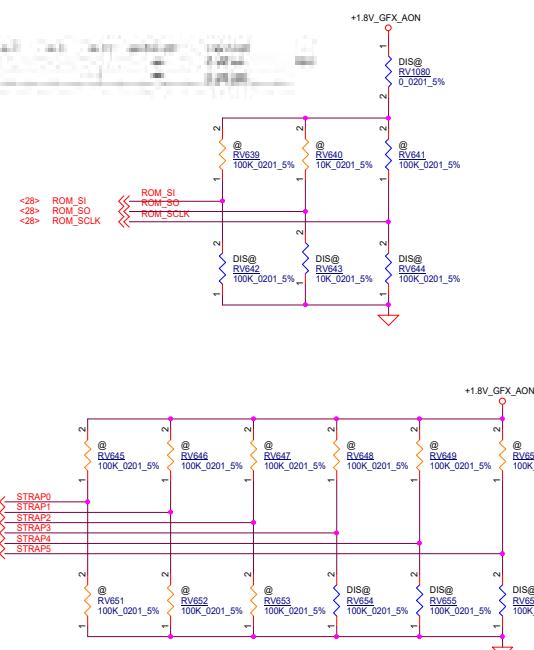


Table 4. NLRP3-GC-G1085 Recommended Members

Minerals Desire	Allowed Mining Companies	PERMIT ID	Period	More Information Number	Per- mitting	String	Authority System Grade	Water Table Alert	Dust Fines	Status
1.0% and 1.0%	Natura	M1112345678-1234	Enable	Match	100%	WTF	WTF	WTF	WTF	Production In Progress
1.0%	Synthesis	H5555555555-1234	Enable	001	0.0%	WTF	WTF	WTF	WTF	Production In Progress

1. For H13P-CD, the maximum allowable memory case temperature is 65 °C.

Table 3. N17P-GO/G-GBDRS Recommended Membrane

Memory Density	Allotted Memory Configuration	PS3000/QC Vendor	Normalized Part Number	Per Partition	Size	Memory Speed Grade	Dense Alert	Dual Plan	Status
8 GB	1x32GB and 1x8GB	Samsung	KT464S12G16H-1E25	Single	32GB	2.66GHz	N/A	N/A	Production ready
			KT464S12G16H-HE25	Single	32GB	2.66GHz	N/A	N/A	Development in progress
			ATM10256ADQ28P-70A	Single	32GB	2.66GHz	N/A	N/A	Production ready
			ATM10256ADQ28P-70C	Single	32GB	2.66GHz	N/A	N/A	Substitution allowed with 70A
			ATM10256ADQ28P-80C	Single	32GB	2.66GHz	N/A	N/A	Production ready
			ATM10256ADQ28P-90C	Single	32GB	2.66GHz	N/A	N/A	Substitution allowed with 80A
			ATM10256ADQ28P-90D	Single	32GB	2.66GHz	N/A	N/A	Production ready
			ATM10256ADQ28P-100A	Single	32GB	2.66GHz	N/A	N/A	Production ready (ES)
16 GB	2x8GB and 1x4GB	Micron	MT46H256M40H-1E25	Single	32GB	2.66GHz	N/A	N/A	Development in progress
			MT46H256M40H-HE25	Single	32GB	2.66GHz	N/A	N/A	Production ready
			MT46H256M40H-70A	Single	32GB	2.66GHz	N/A	N/A	Substitution allowed with 70A
			MT46H256M40H-70C	Single	32GB	2.66GHz	N/A	N/A	Production ready

SMB_ALT_ADDR	State	DEVID_SEL	State	PCIE_CFG	State	VGA_DEVICE	State
Low	Single GPU	Low	Original Device	Low	Normal signal swing	Low	3D Device
High	Dual GPU	High	Re-brand Device ID	High	Reduce the signal amplitude	High	VGA Device

Table 5.5 SMB_ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Table 5.5 SMB ALT_ADDR, DEVID_SEL, PCIE_CFG, VGA_DEVICE

Strap Pins Note 1			Functions Selected by This Strapping			
STRAPS	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
L	L	L	0	0	0	0

Table 5.2 RAMCFG

Strap Pins see Note			RAMCFG Setting Number	
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)	
L	L	L	0 (0x0000)	RAM16M
L	L	H	1 (0x0001)	RAM32M
L	H	L	2 (0x0002)	RAM64M

Table 4. NBBP DIV/C1 5908 Recommended Memories

Memory Capacity	Allored Memory Configuration	FBV200	Vendor	Manufacturer Part Number	Die Revision	Speed	Memory Speed Grade	Date Code	Qual Alert	Qual Plan	Status
3.2G	1.35V	Wolfs	WST1256UZM-005	E04	2G	5 Gbps	N/A	N/A	Pass	Production candidate	
	2.5V & 1.5V	Hydis	HSGC1248U-F02	E-19	2G	3 Gbps	N/A	N/A	Fail	Production candidate	

200

1. For H-99-Q3-Q1, the maximum allowable memory case temperature is 85 °C.

Table 15-3. GB18034, GB48128 and GB33256 Multi-Level Modulation

Group Name	Logical Shelves (L1)	Logical Shelves (L2)	Logical Shelves (L3)	Logical Shelves (L4)
RDM_014	1000_000000	1000_000000	0001_000000	0000_000000
RDM_015	1000_000000	1000_000000	0001_000000	0000_000000
RDM_016	1000_000000	1000_000000	0001_000000	0000_000000
RDM_017	1000_000000	1000_000000	0001_000000	0000_000000

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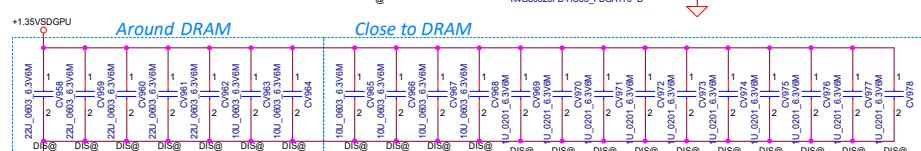
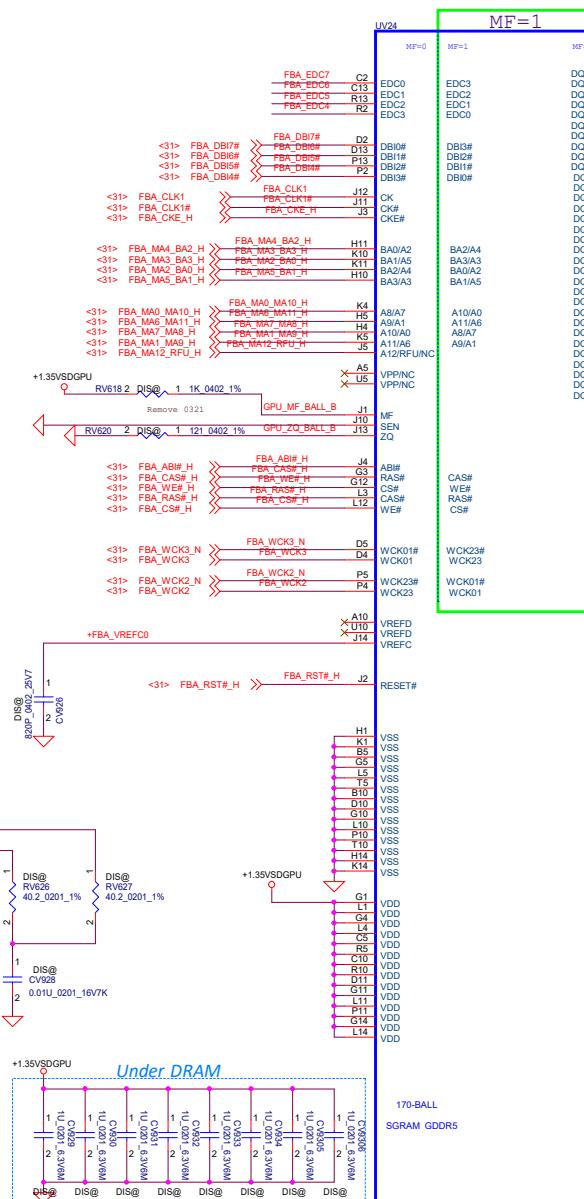
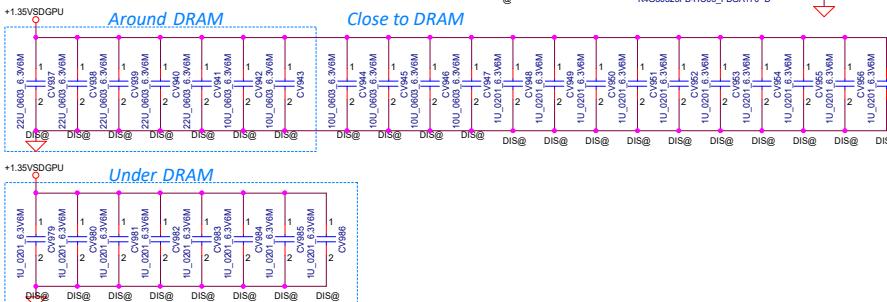
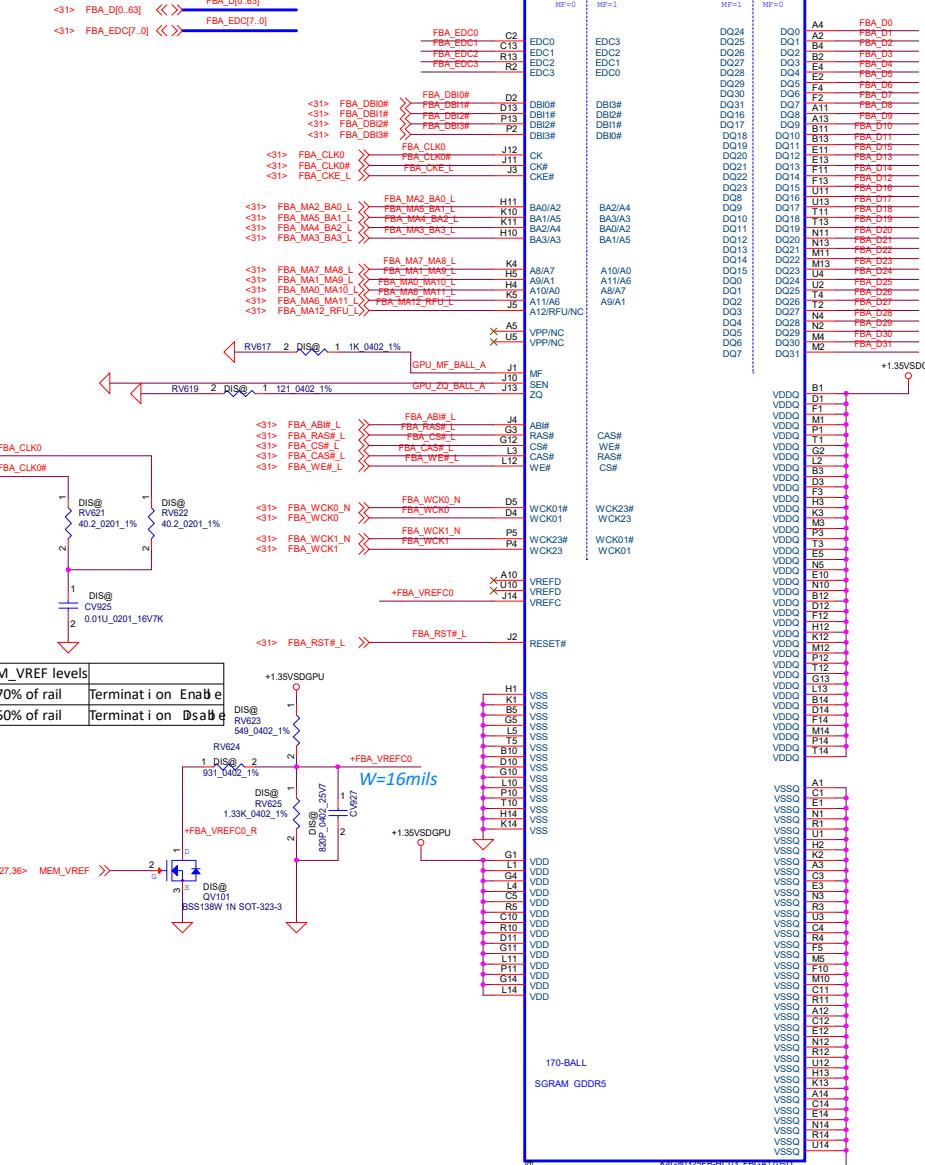
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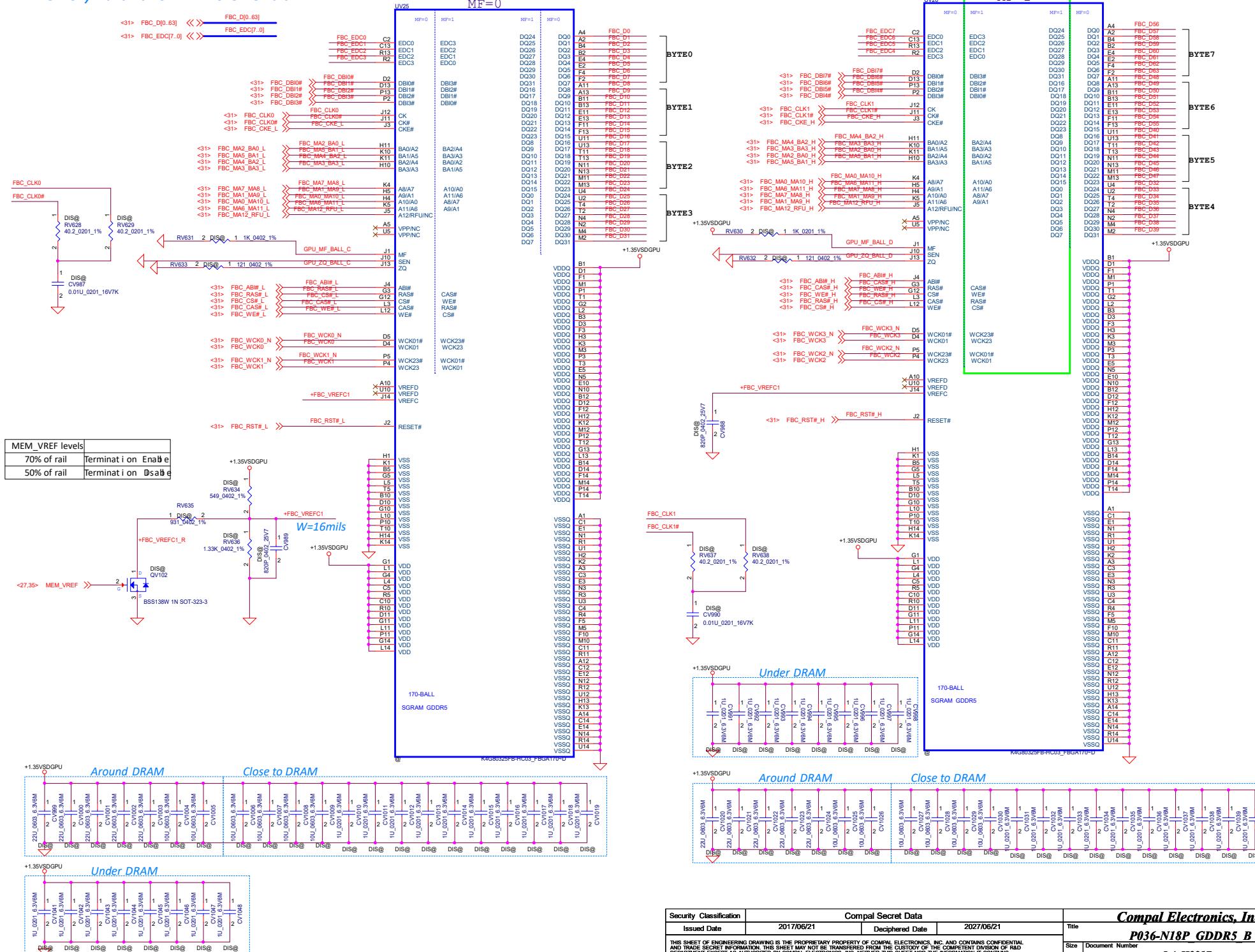
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Memory Partition A- Lower 32 bit



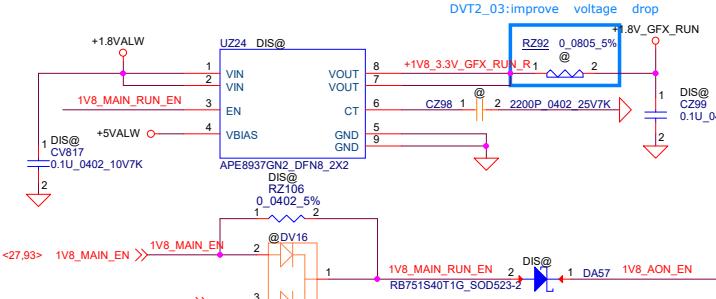
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Memory Partition A- Lower 32 bit



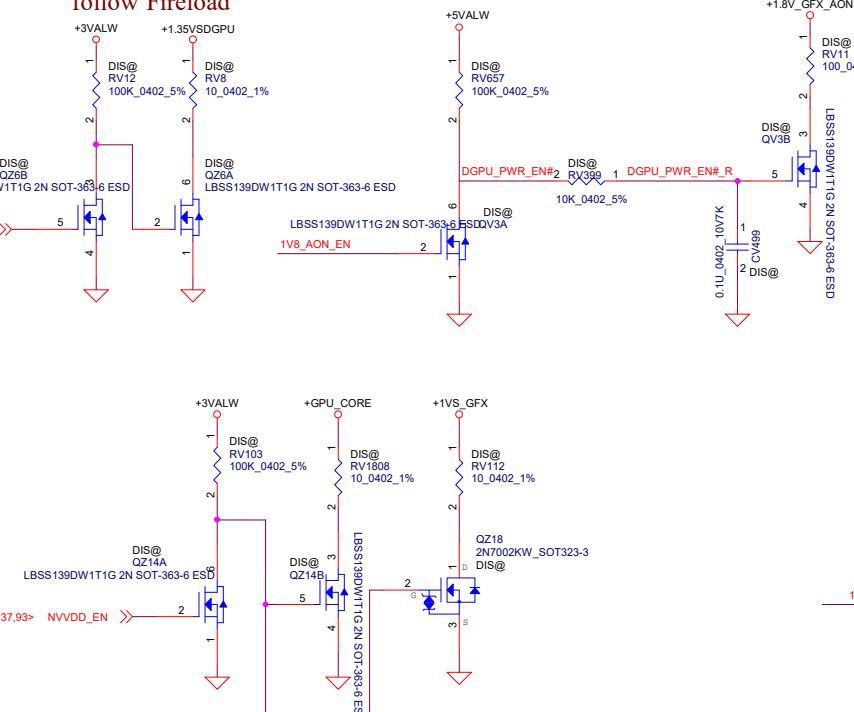
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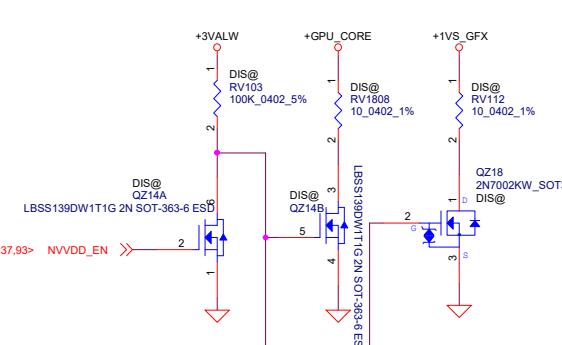
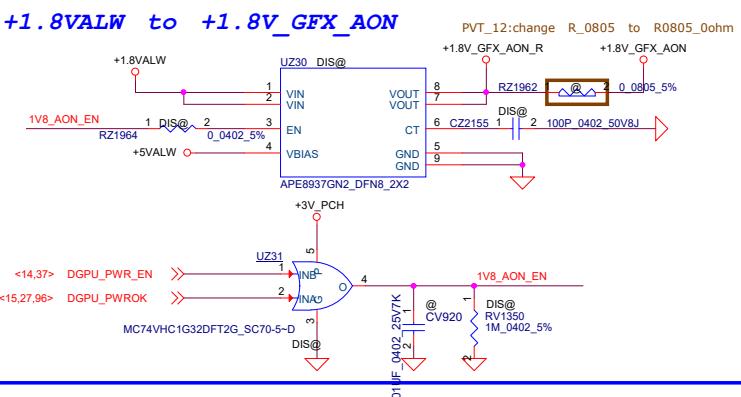


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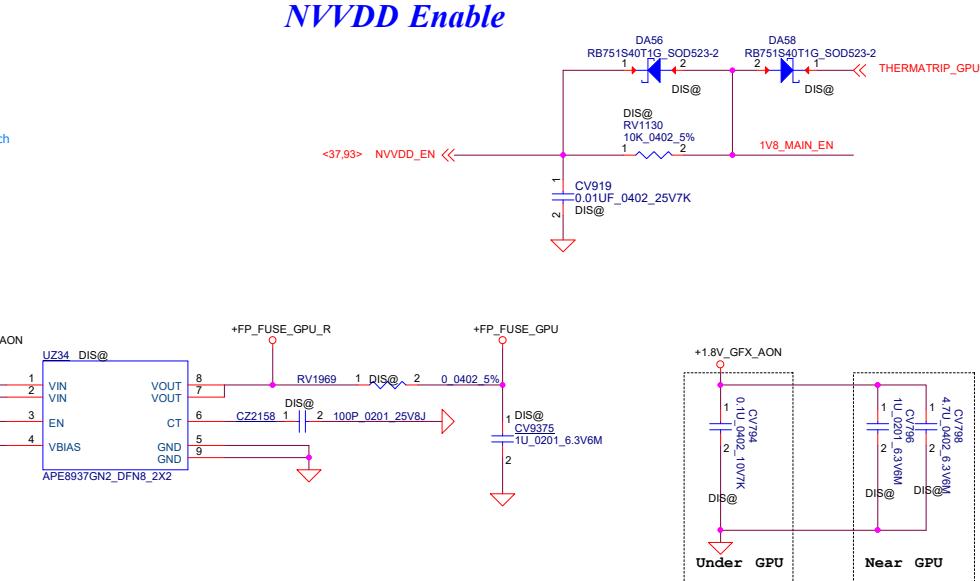
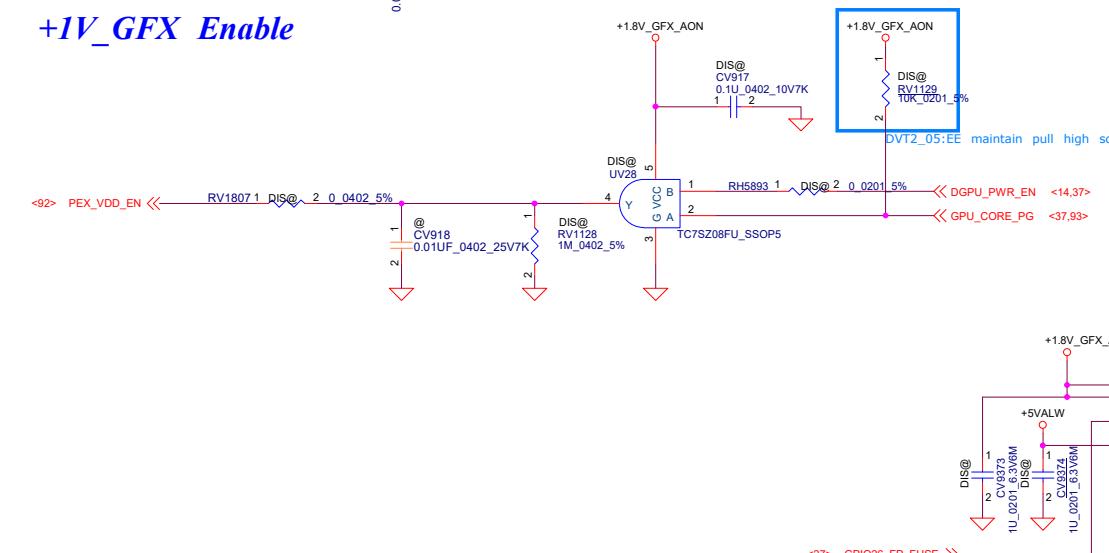
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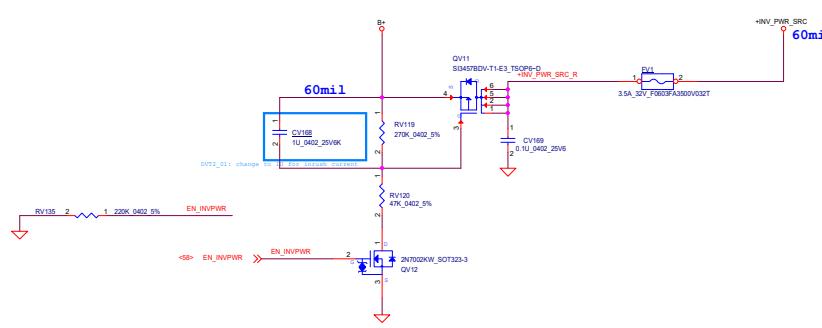
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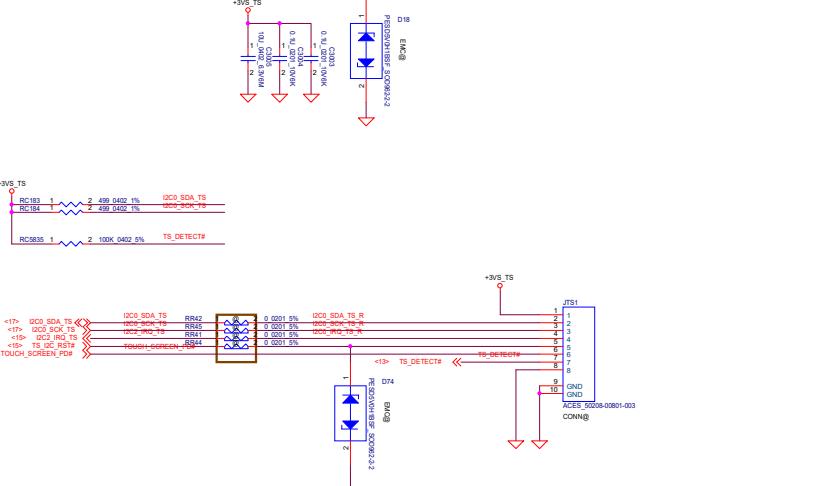
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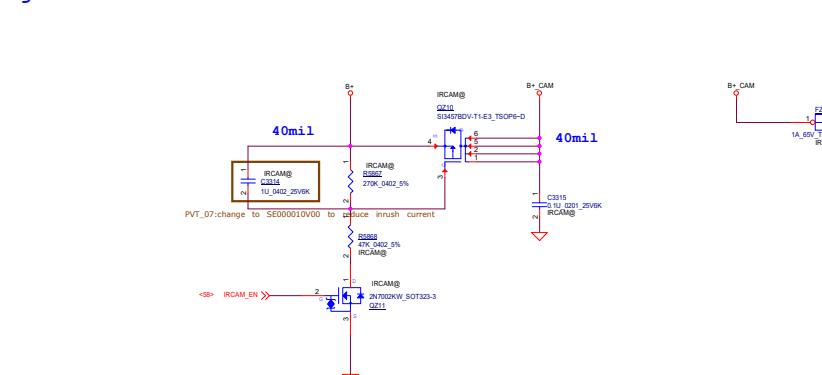
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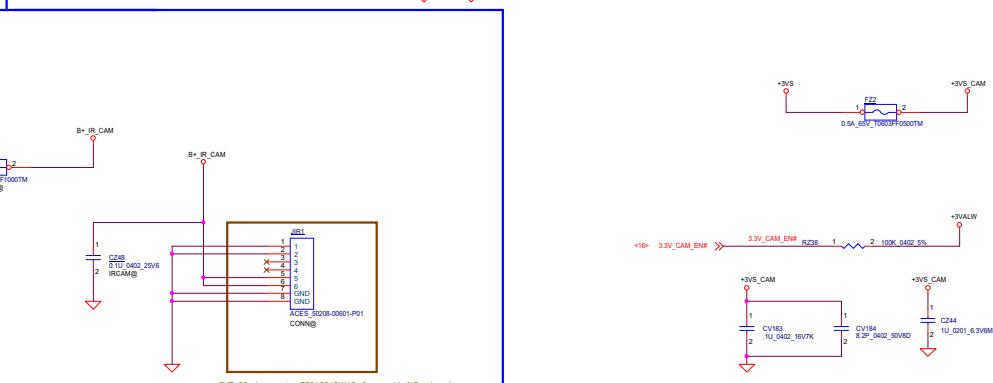
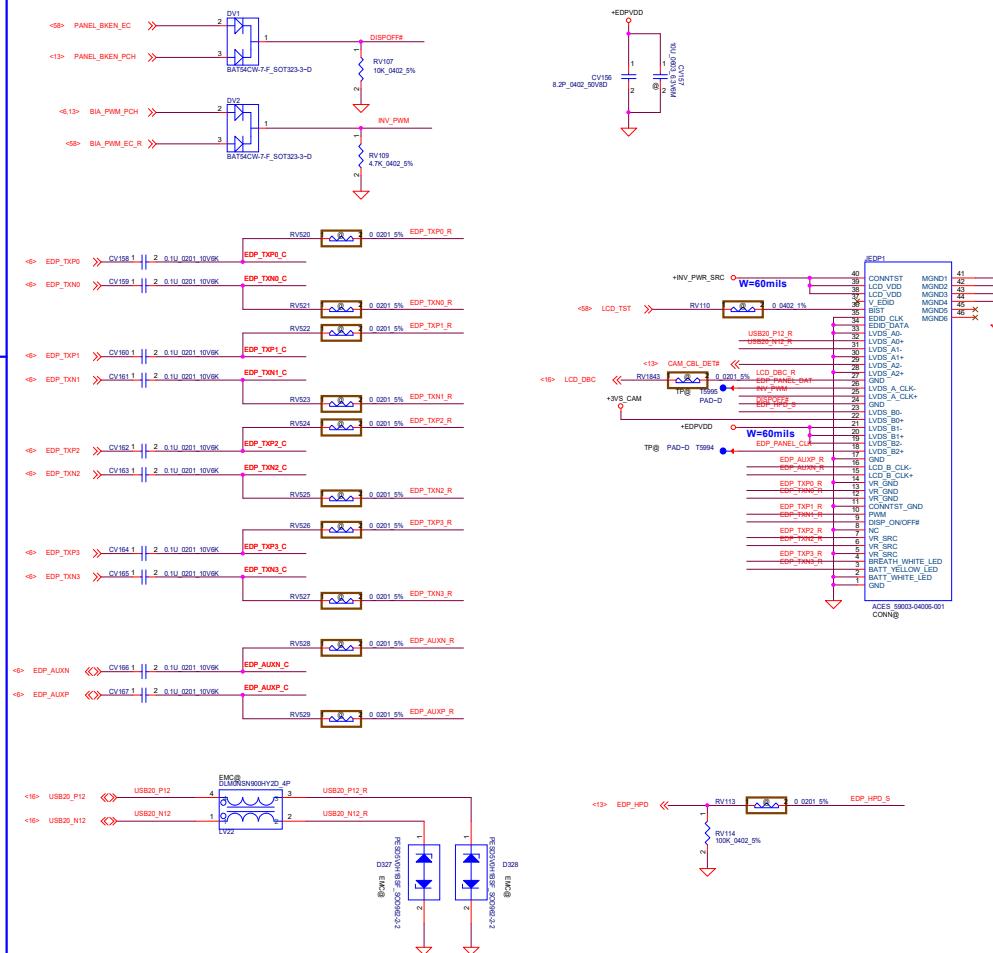
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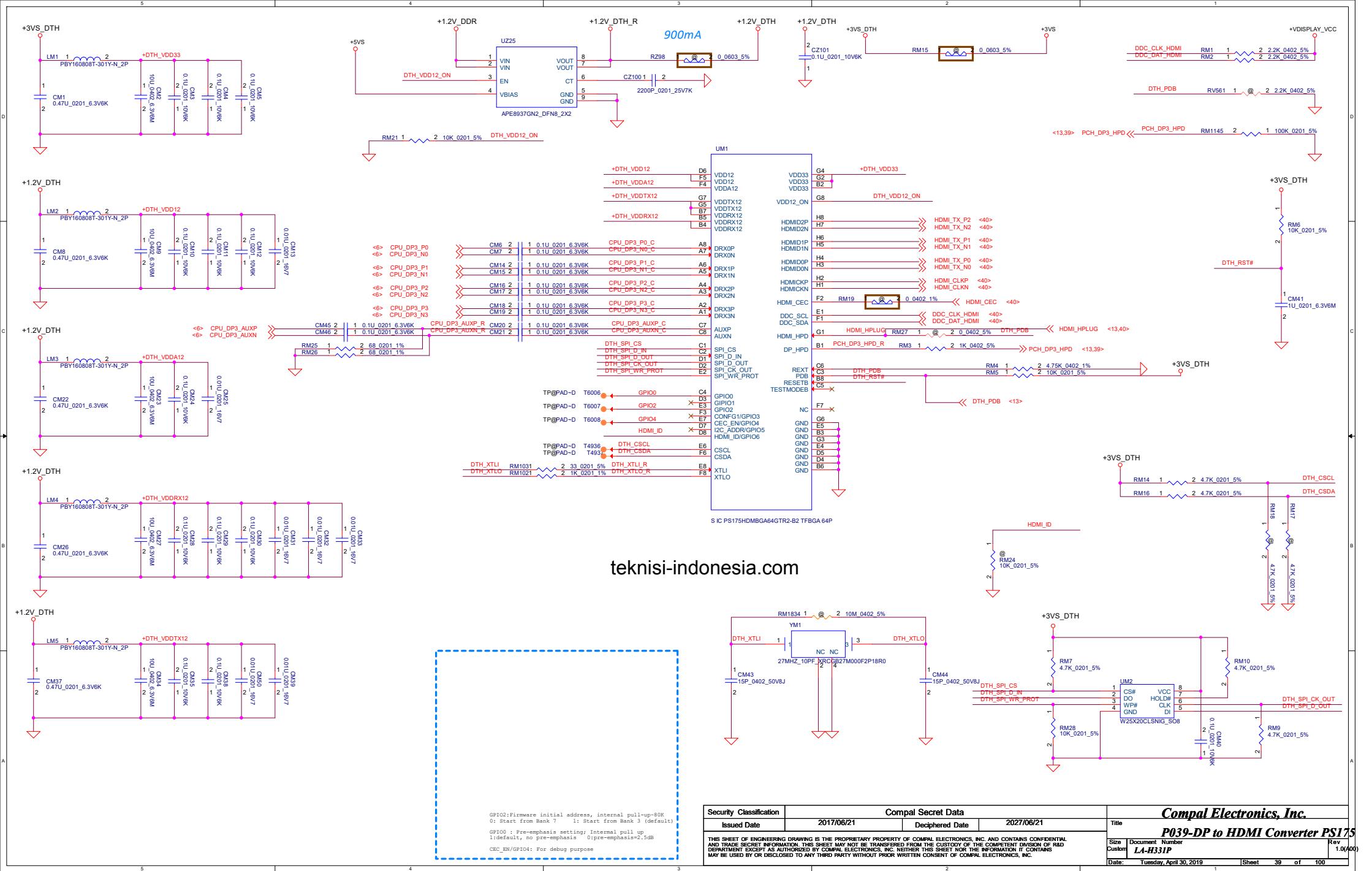
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eDP & CCD(RGB) Conn

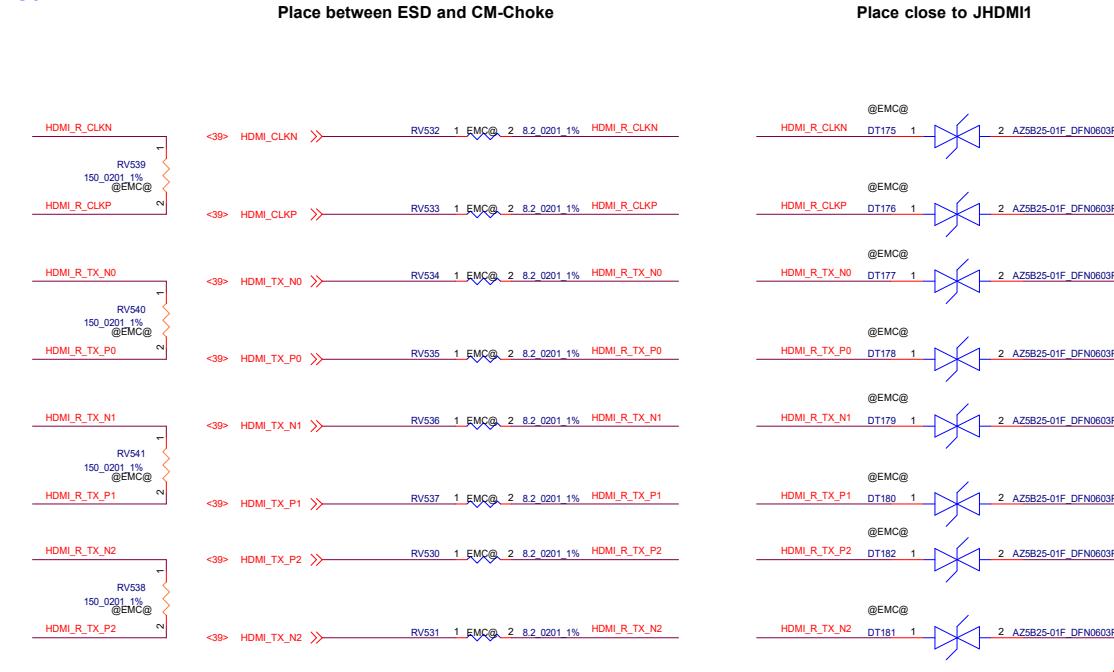


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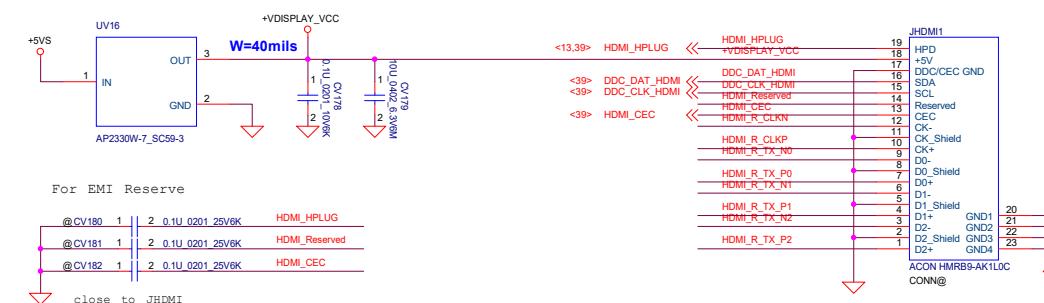


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HDMI change to CPU to PS185 to CONN

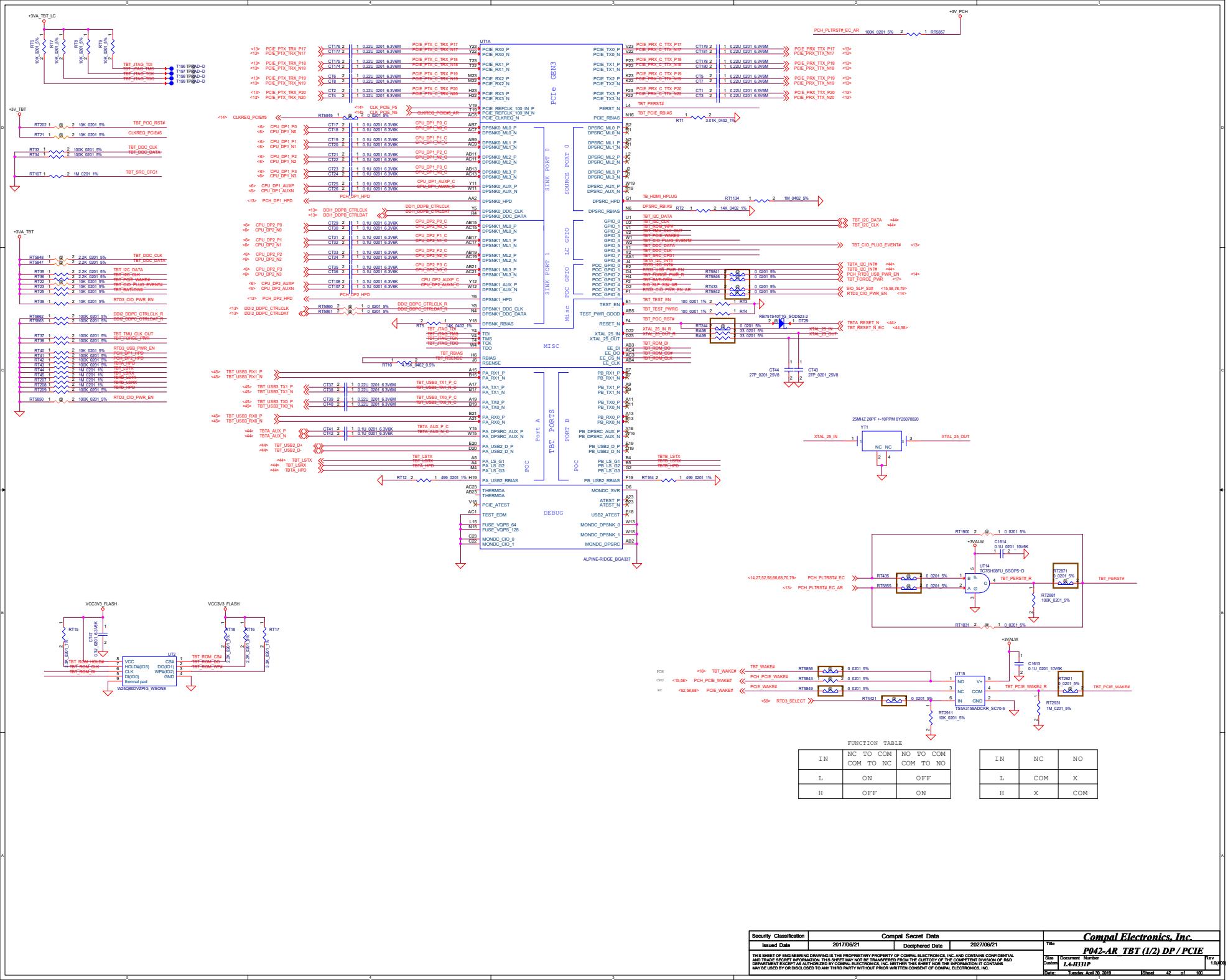


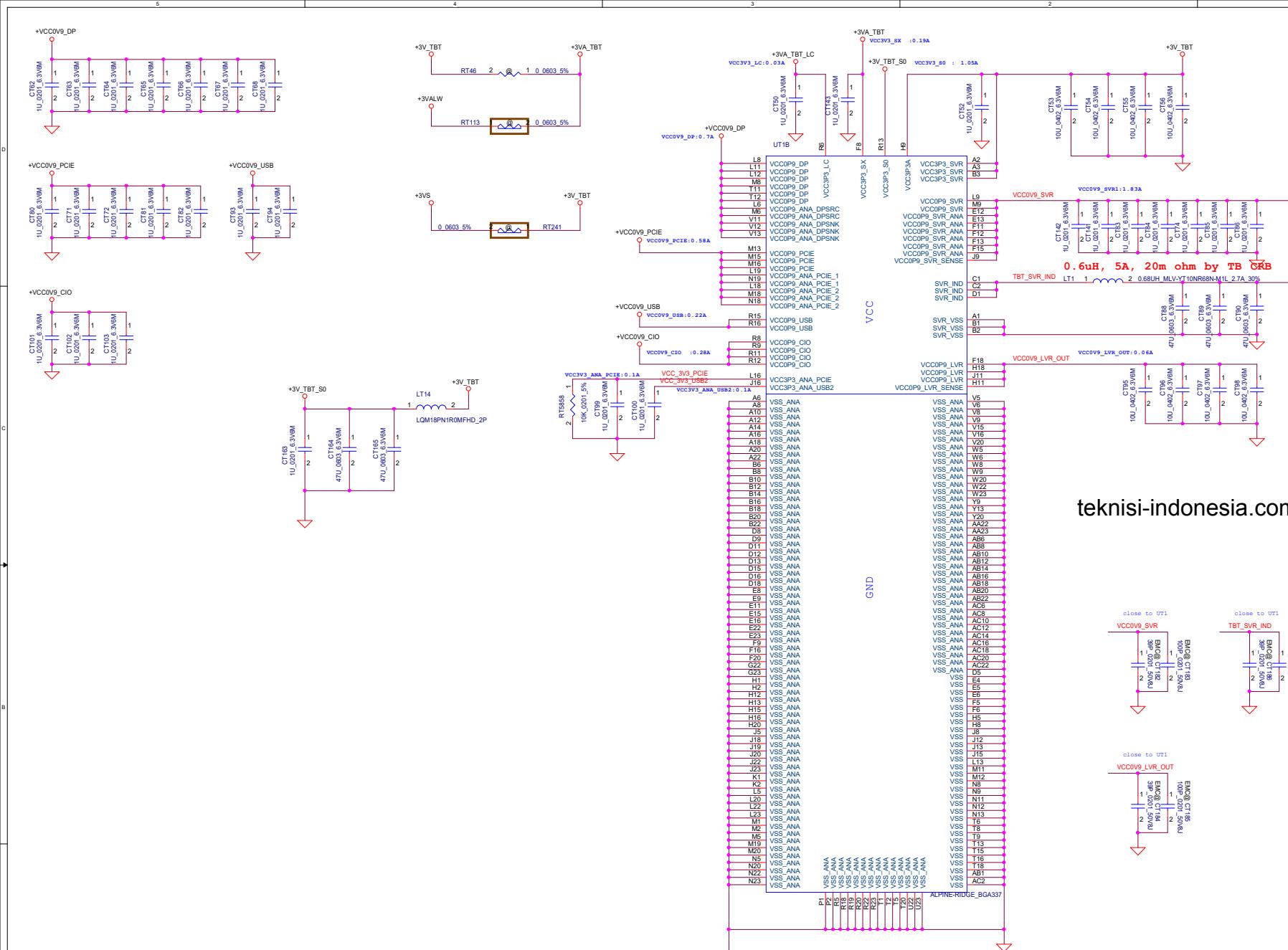
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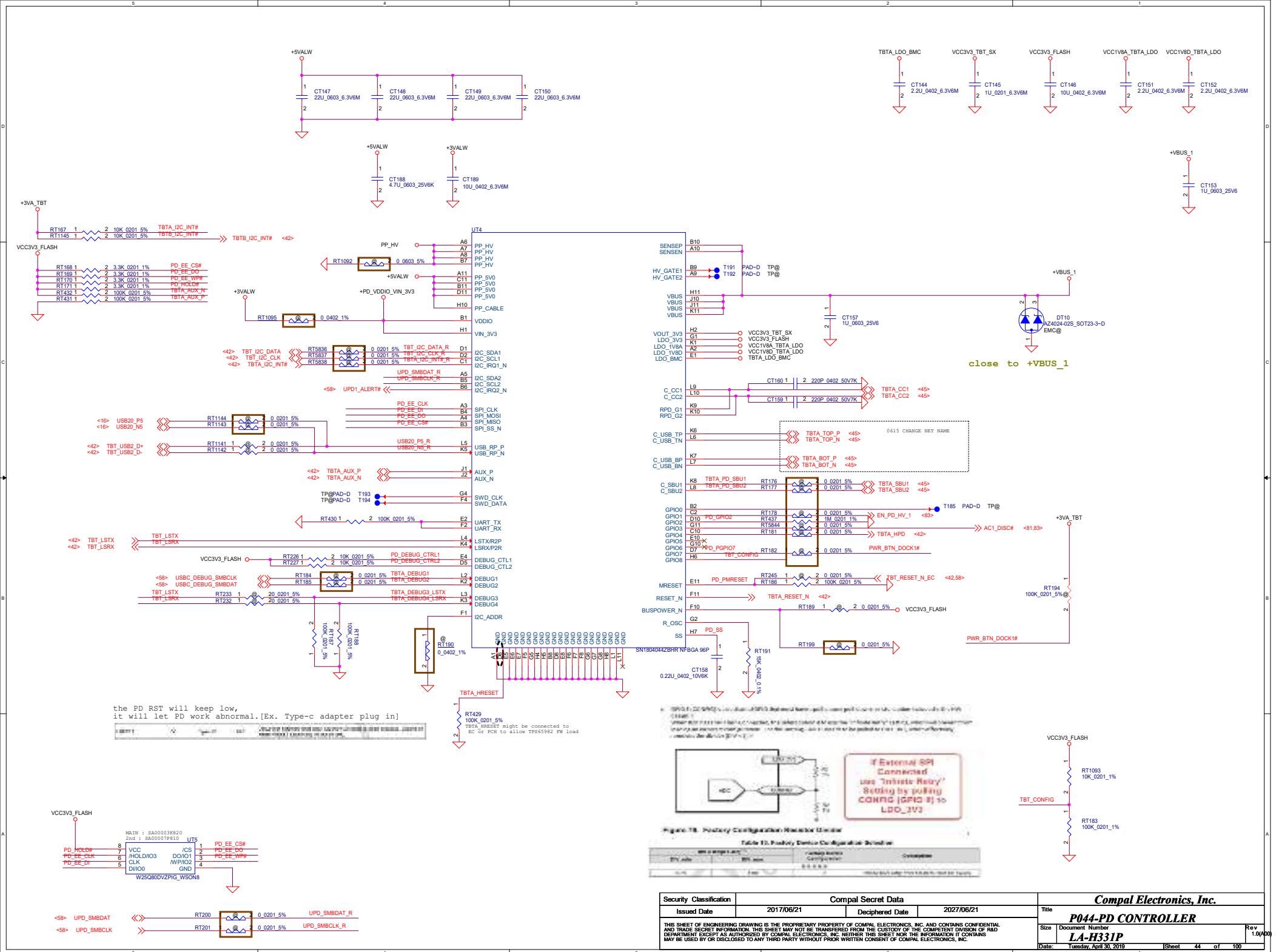


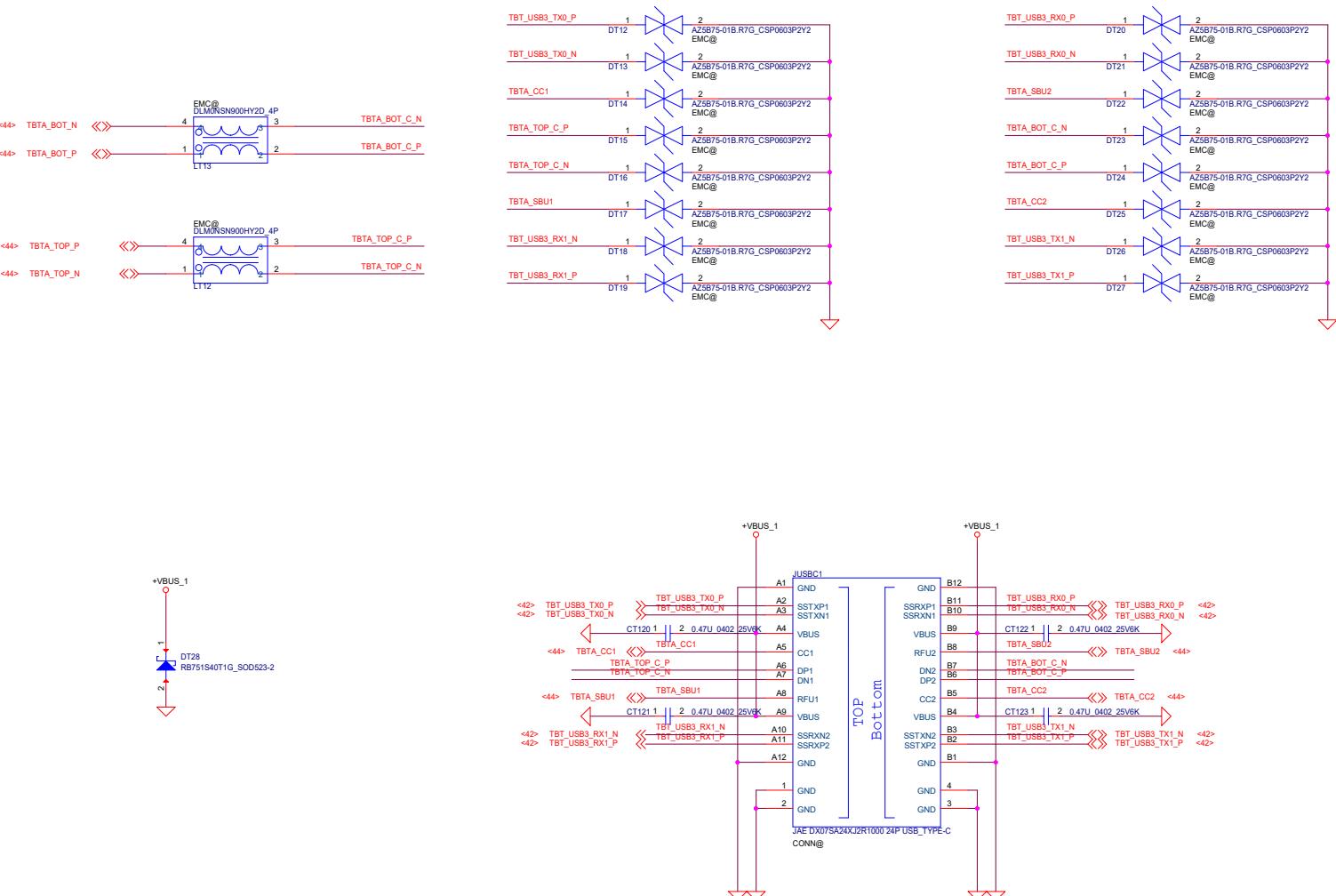
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Issued Date	2017/06/21	Deciphered Date	2027/06/21	P040-HDMI Connector
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Date: Tuesday, April 30, 2019 Sheet 41 of 100				
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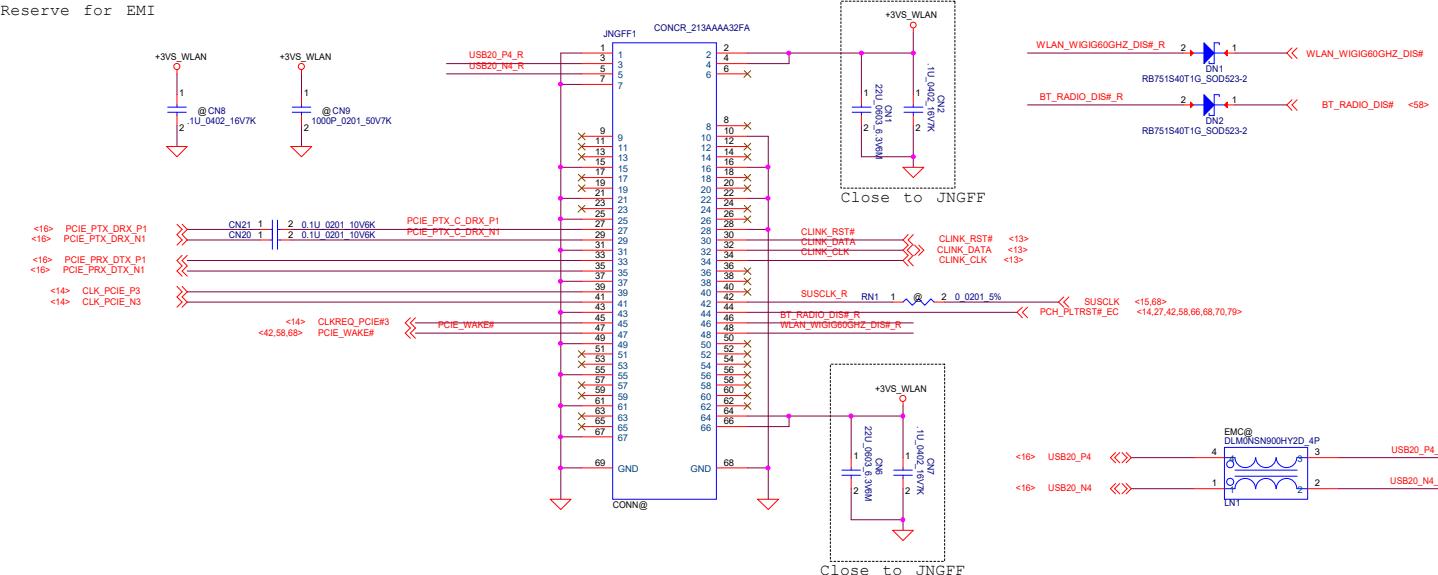
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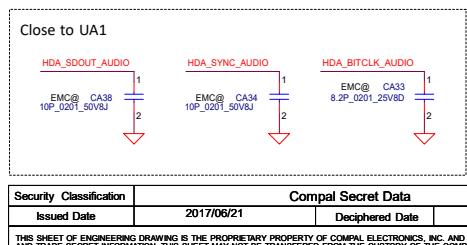
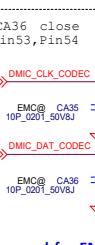
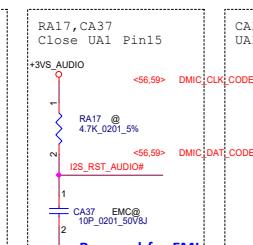
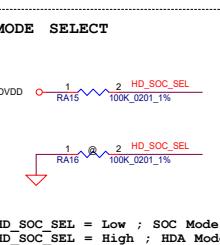
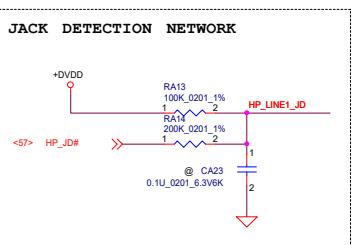
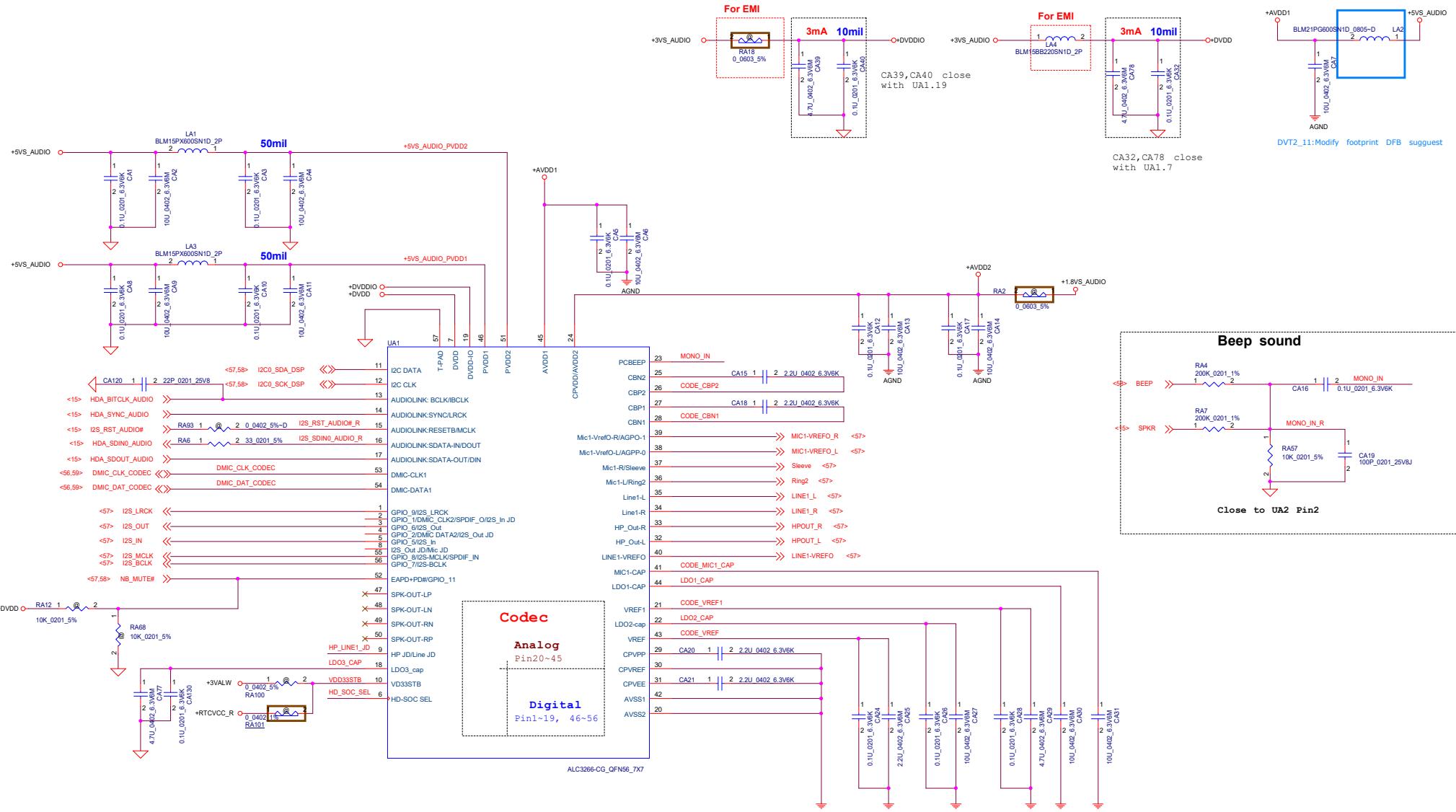
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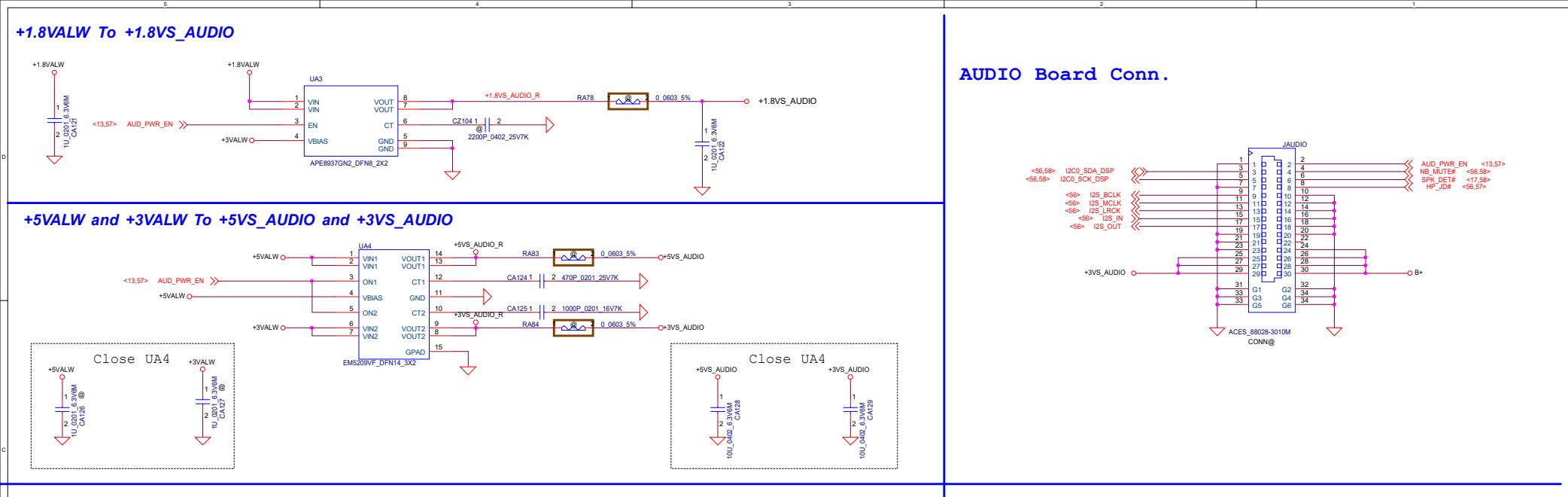
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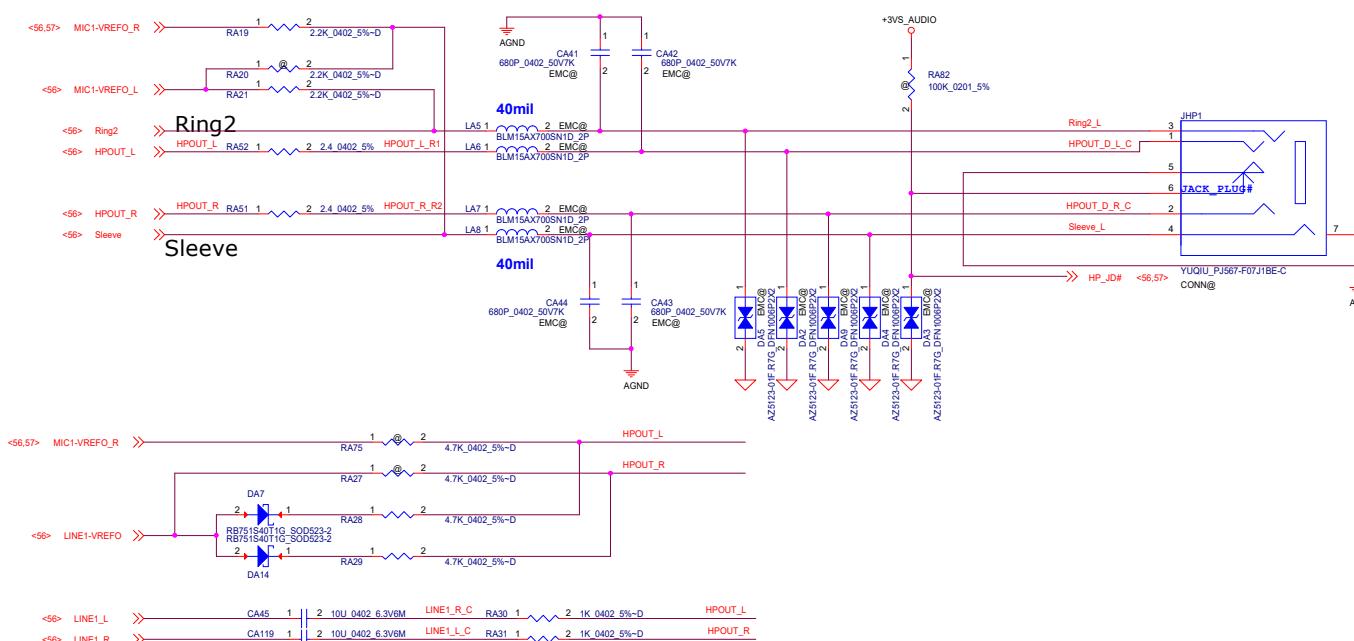
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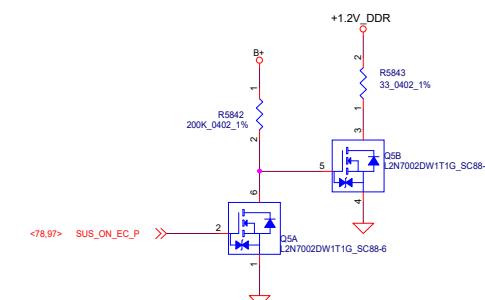
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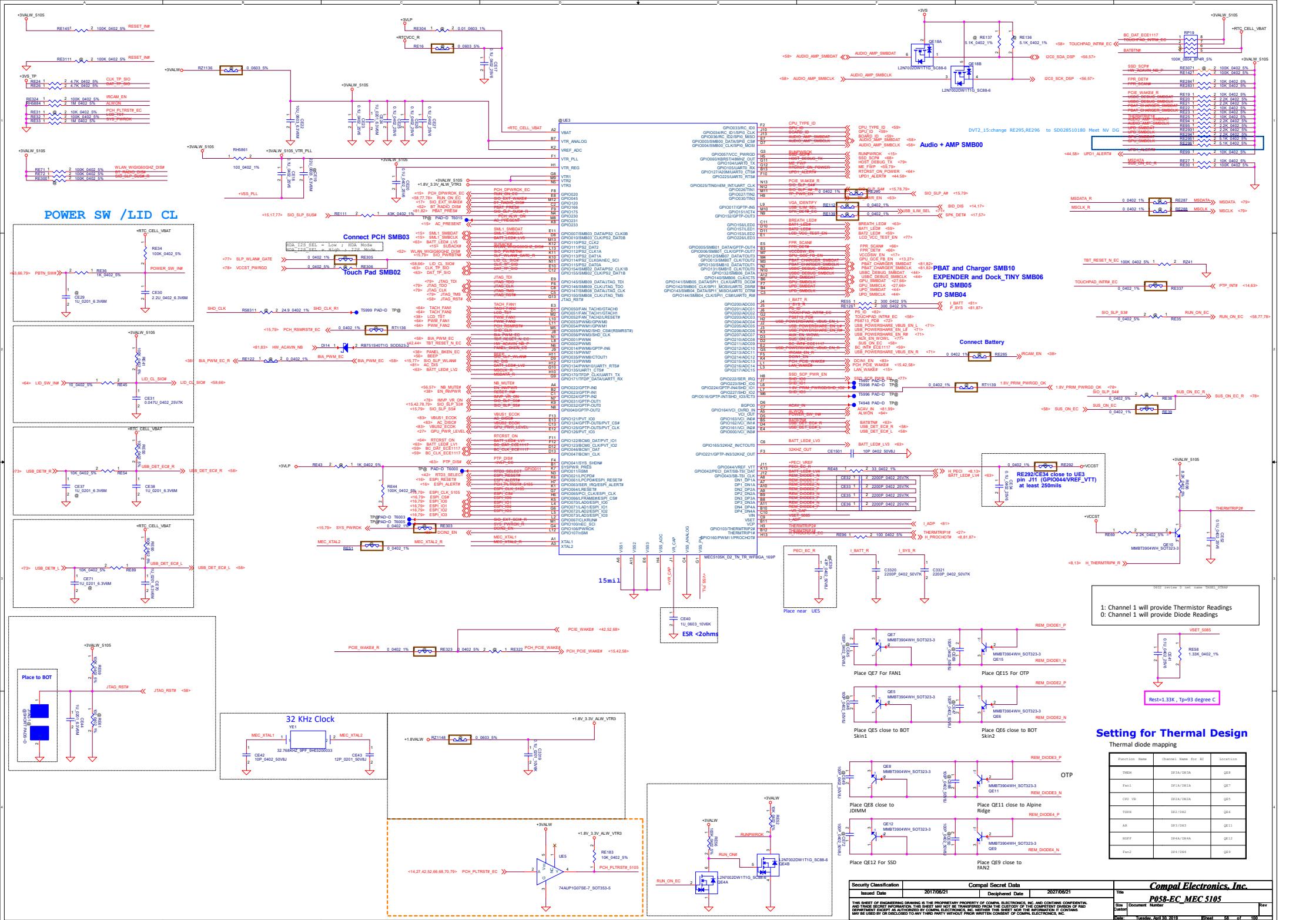


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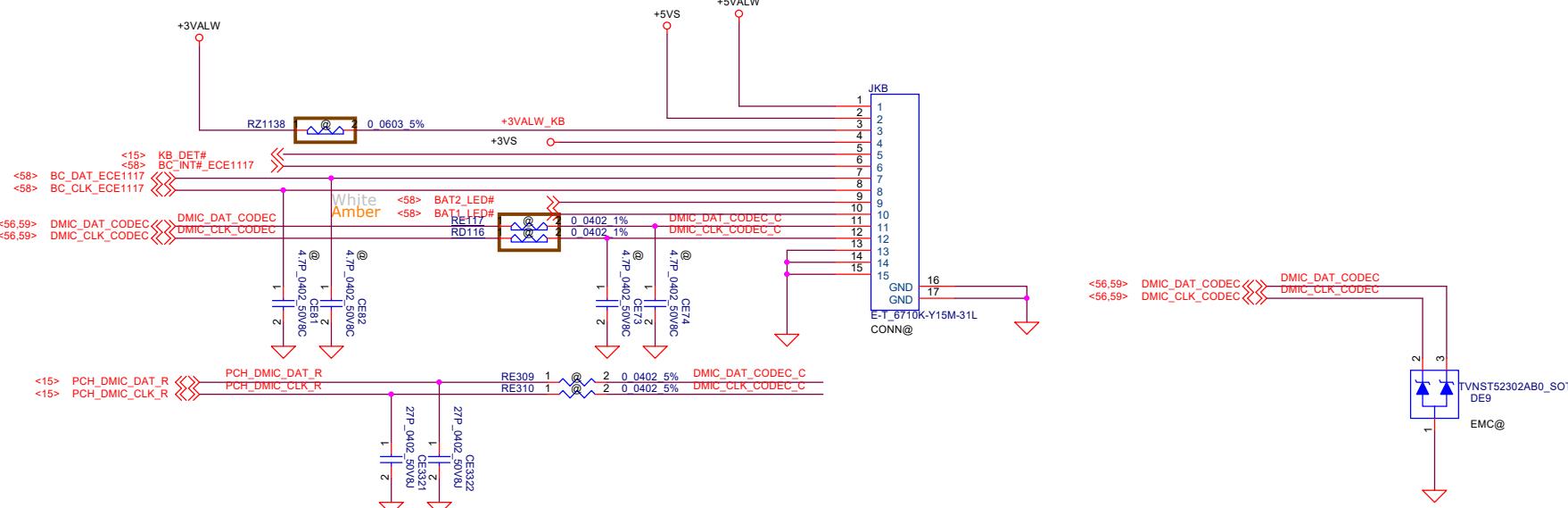


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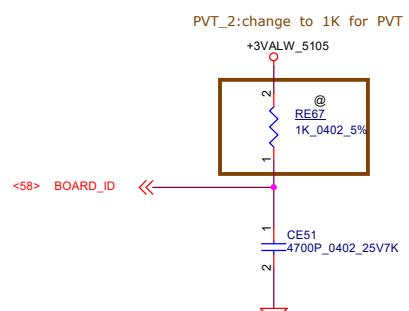
Keyboard Controller board + DMIC



EC Strap

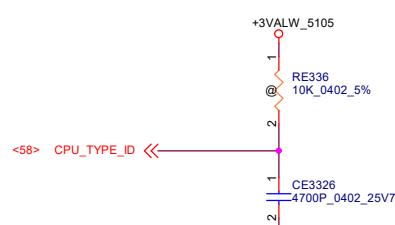
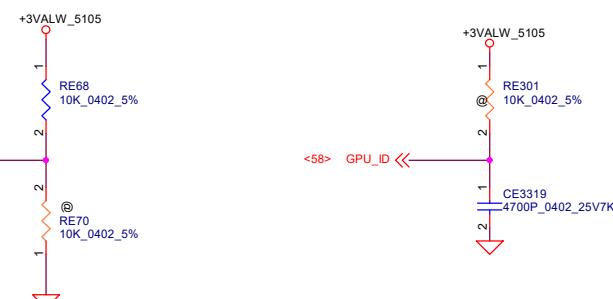
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240K4700p			PRE EVT
130K4700p	X00		EVT
62K 4700p	X01		DVT1
33K 4700p	X02		DVT2
8.2K 4700p			
4.3K 4700p			
2K 4700p			
1K 4700p	A00		PVT

BOARD_ID rise time is measured from 5%~68%.

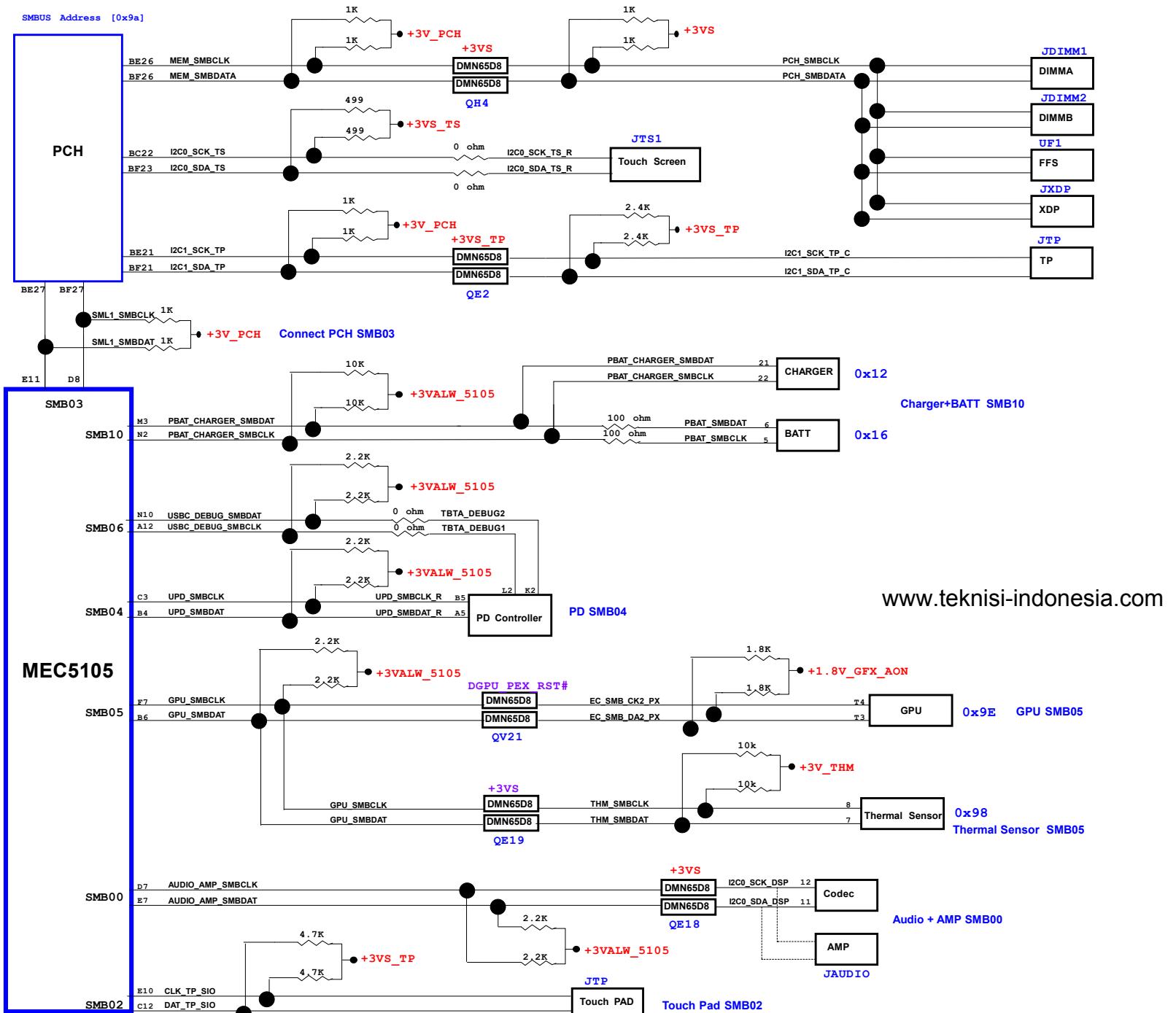


RE301	CE3319	CONFIG
240K4700p		
130K4700p	UMA	
62K 4700p	N18P-G0	
33K 4700p		
8.2K 4700p	N19P-Q1	
4.3K 4700p	N19P-Q3 MAXQ	
2K 4700p		
1K 4700p		

RE336	CE3326	CONFIG
240K4700p		
130K4700p	3PHASE-I5	
62K 4700p		
33K 4700p		
8.2K 4700p	4PHASE-6+2	
4.3K 4700p		
2K 4700p		
1K 4700p	4PHASE-8+2	



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B				B																			
A				A																			
DELL CONFIDENTIAL/PROPRIETARY																							
<i>Compal Electronics, Inc.</i>																							
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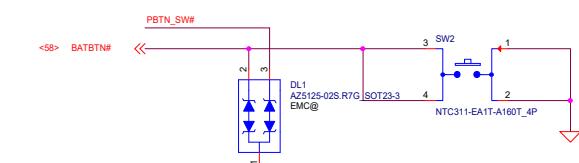


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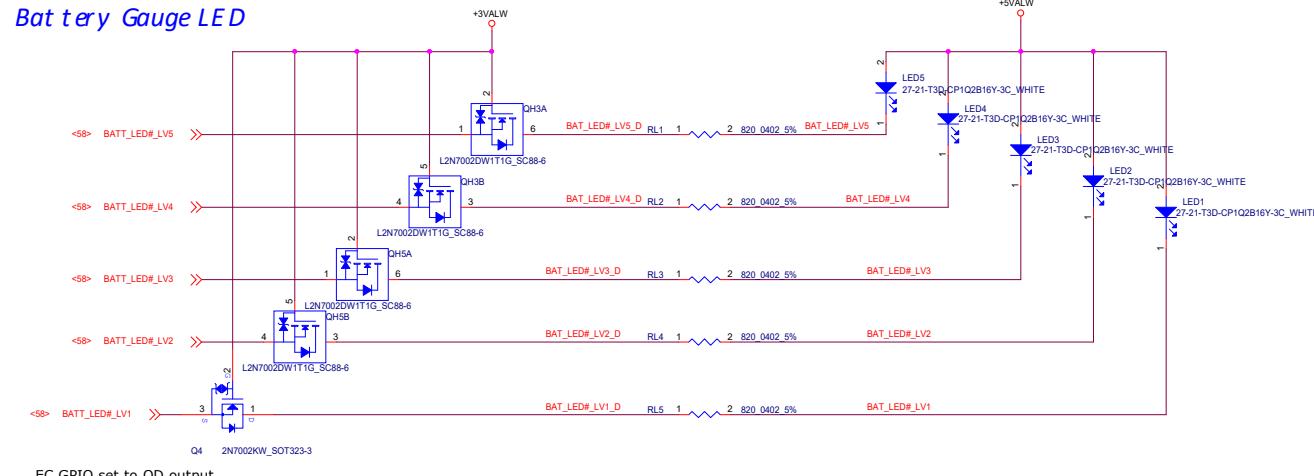
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LA-H331P				Date: Tuesday, April 30, 2019																													
Sheet 62 of 100				1																													

BATT LED Power Button



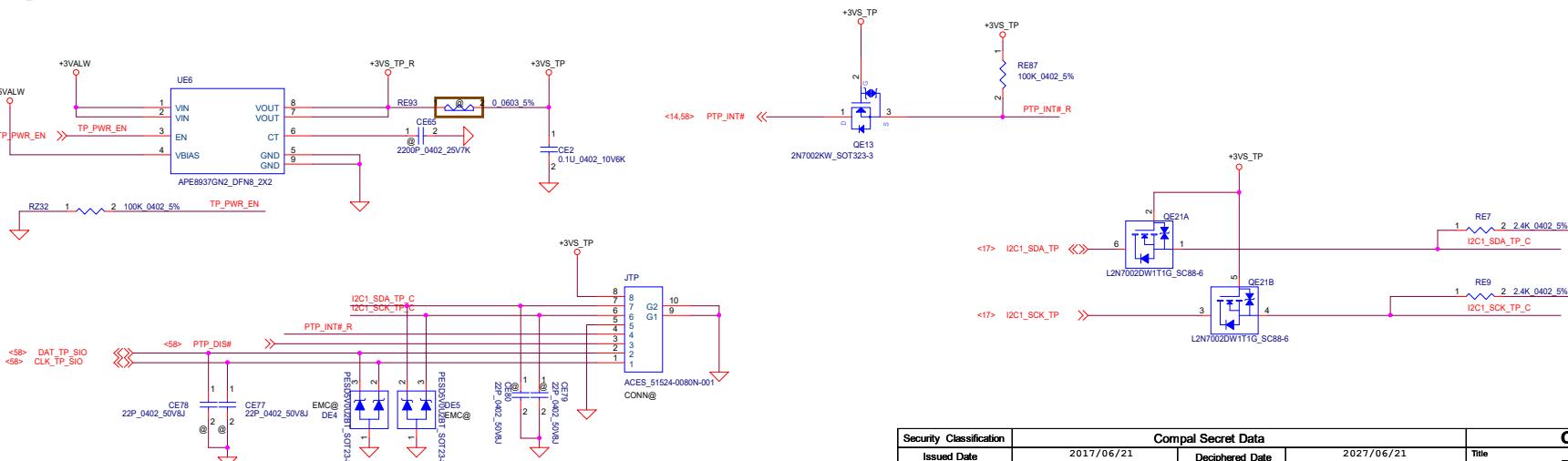
Battery Gauge LED



Power Button and LED



Touch pad

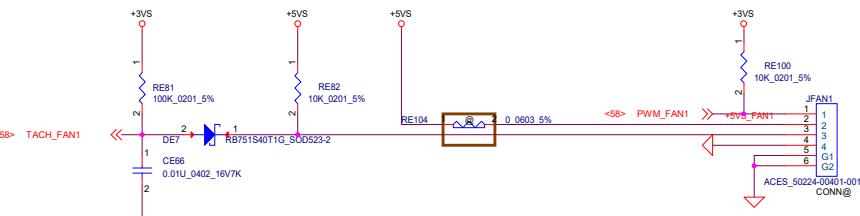
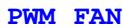


Fingerprint Reader CONN

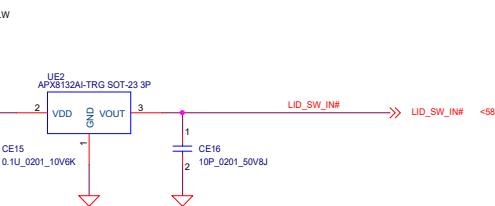
Compal Electronics, Inc.

P063-BAT | LED/TP/SW

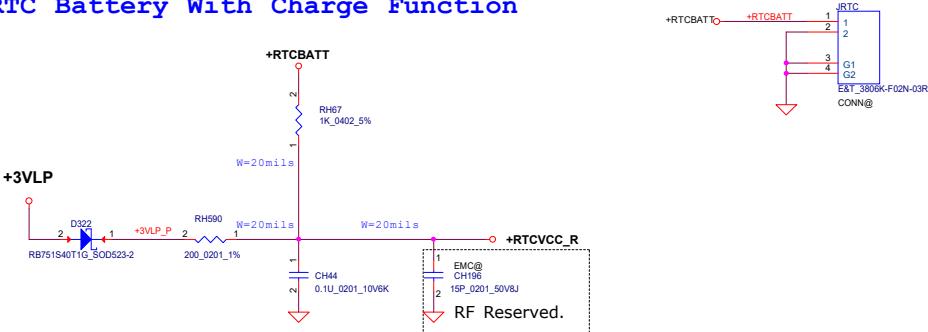
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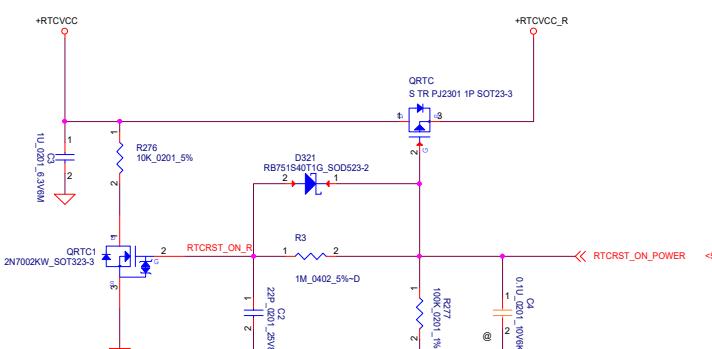
Lid Switch



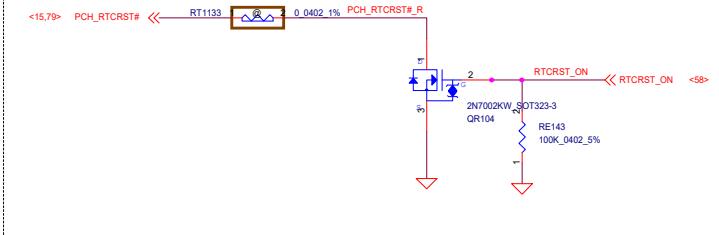
RTC Battery With Charge Function



Default: OD EC drives GPIOs to LOW to turn ON power to VCCRTC



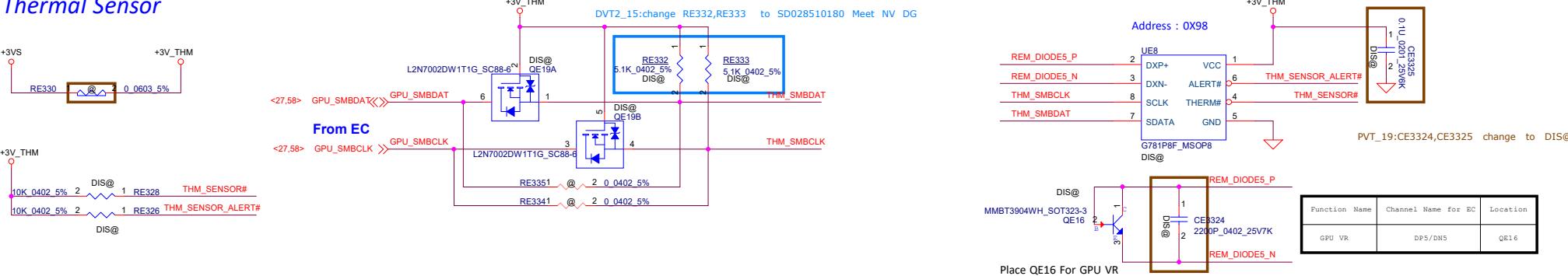
follow Intel Keep old RTC



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				Date:	Tuesday, April 30, 2019	Sheet 64 of 100

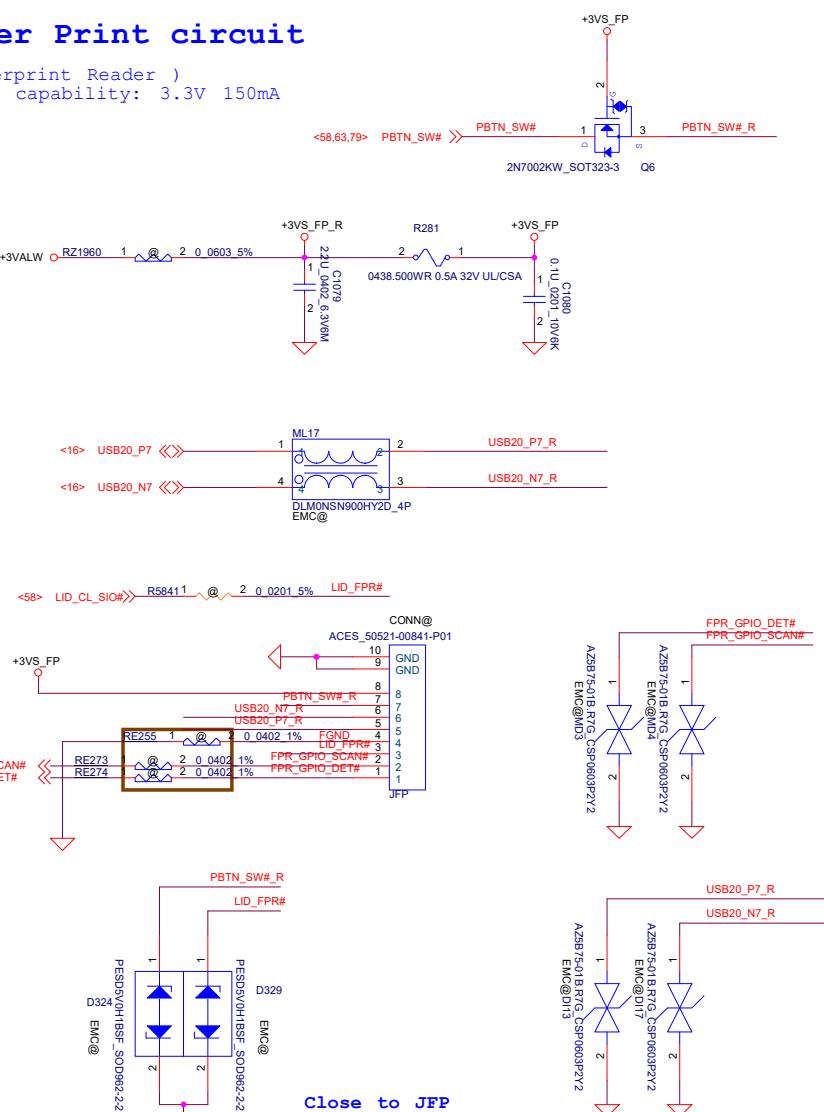
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Thermal Sensor

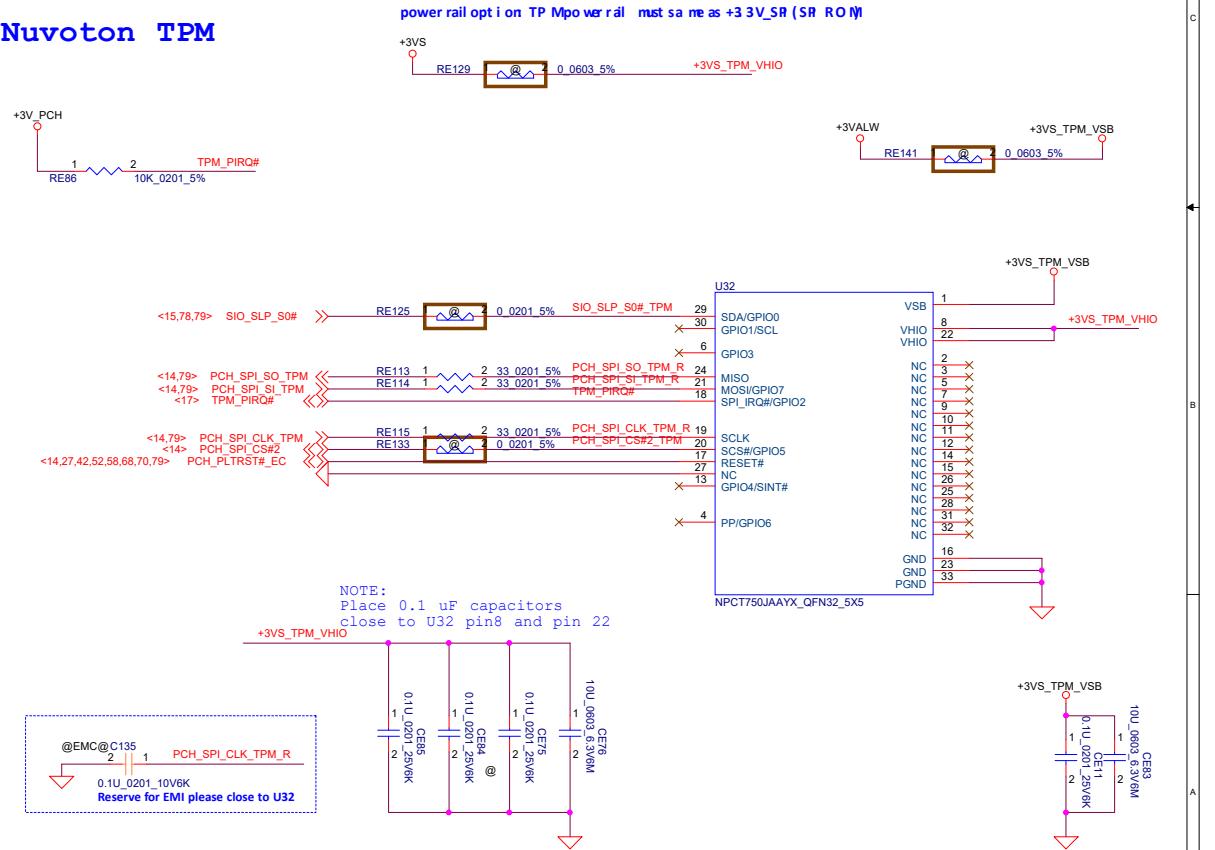


Finger Print circuit

(Fingerprint Reader)
Current capability: 3.3V 150mA



Nuvoton TPM



Security Classification

Compal Secret Data

Issued Date

Deciphered Date

2017/06/21

2027/06/21

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Compal Electronics, Inc.

P066-TPM/FP/THM Senso

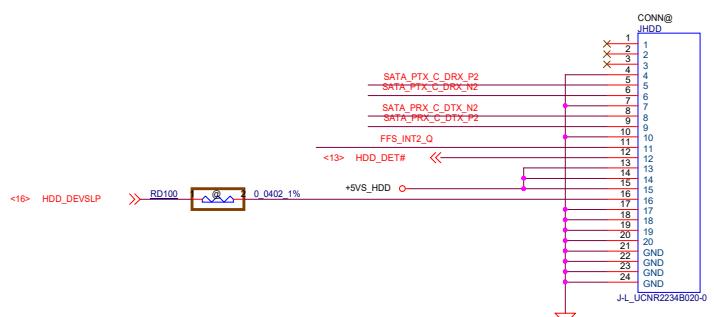
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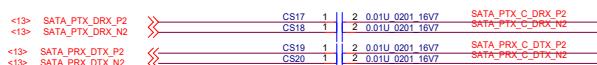
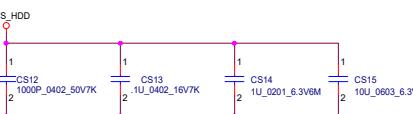
Date: Tuesday, April 30, 2019

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HDD CONN

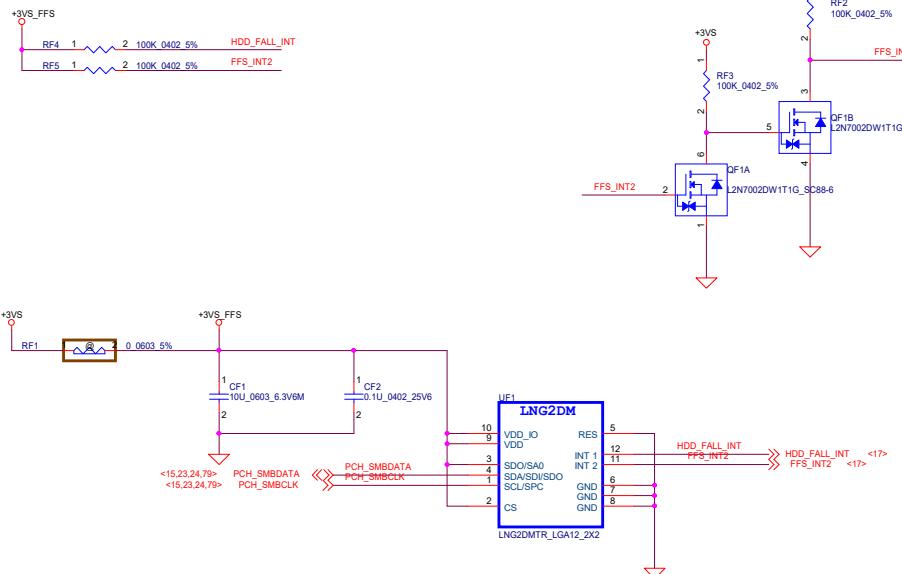


Place near HDD CONN (JHDD1)



BYPASS Circuit

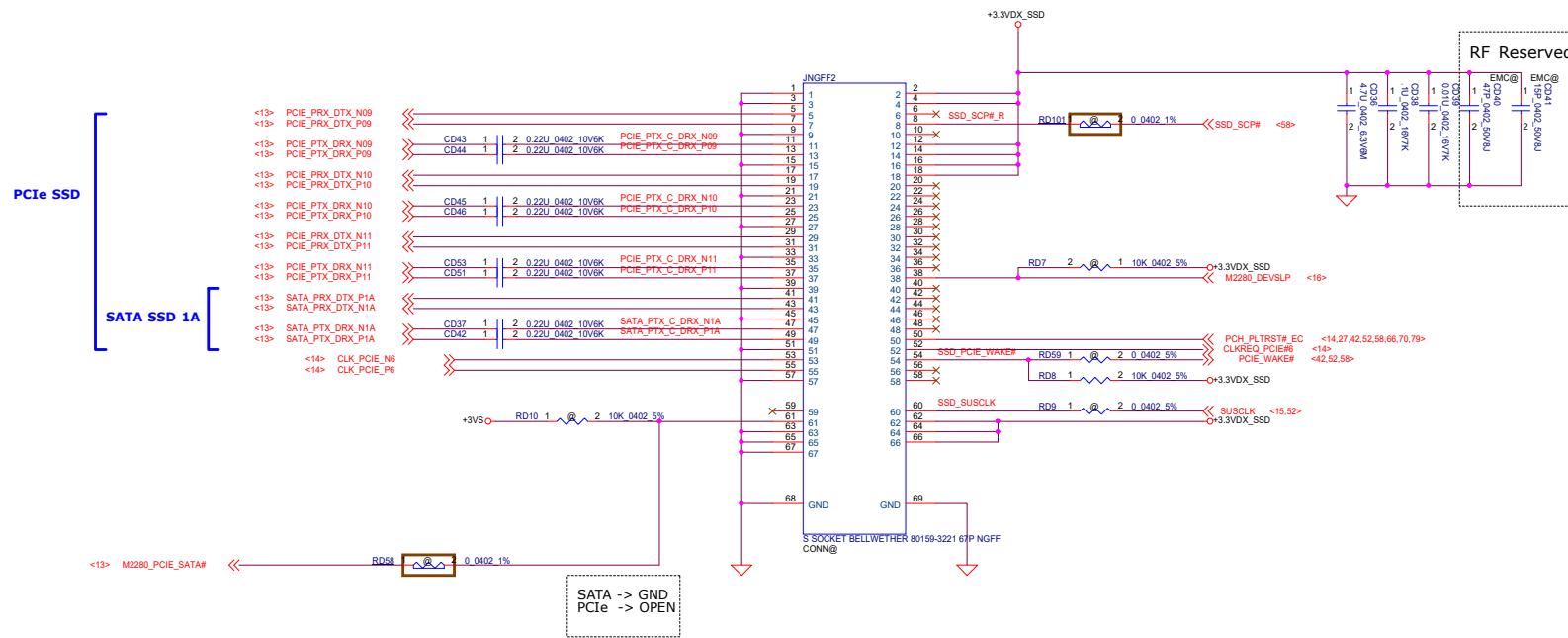
Free Fall Sensor



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M.2 Slot-C Key-M (SSD)

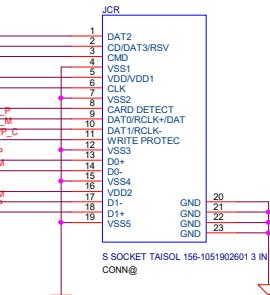
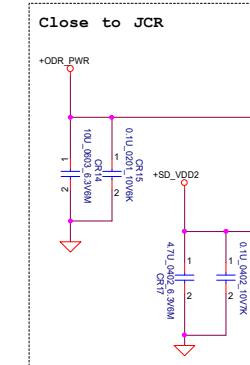
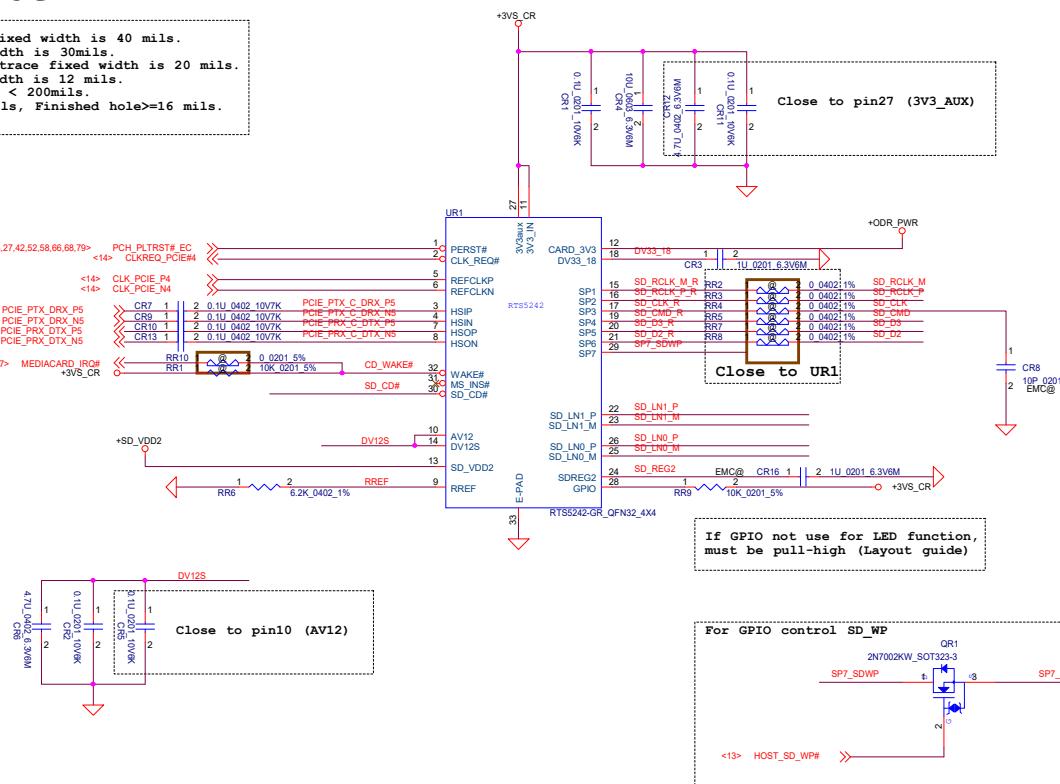


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Date	Tuesday, April 30, 2019	Sheet 68 of 100		

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Card Reader

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Pin11, Pin12 trace fixed width is 40 mils.  
Pin27 trace fixed width is 30mils.  
Pin10, pin14, pin18 trace fixed width is 20 mils.  
Pin 9 trace fixed width is 12 mils.  
Trace routing length < 200mils.  
Via size: Pad>28 mils, Finished hole>=16 mils.
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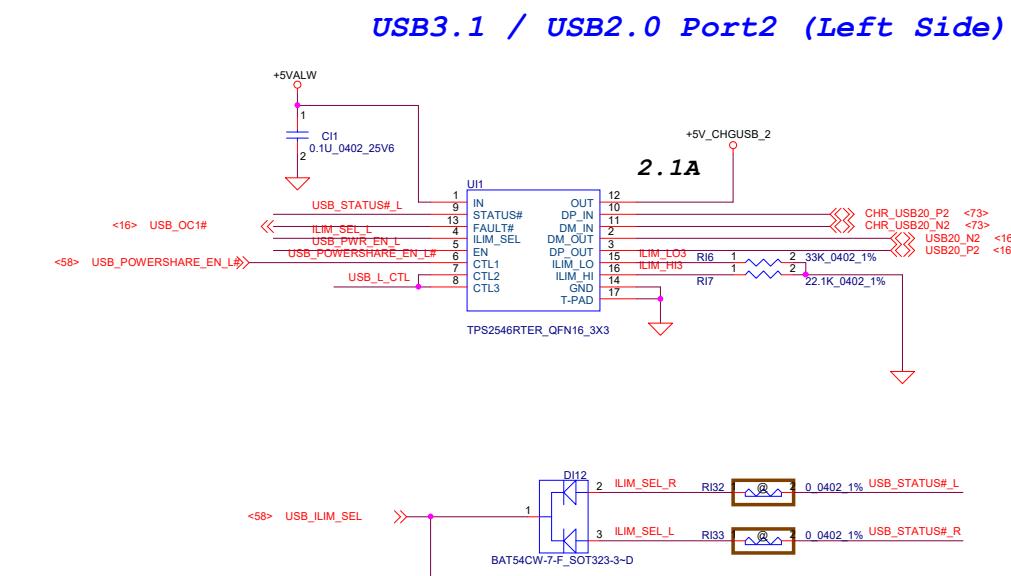
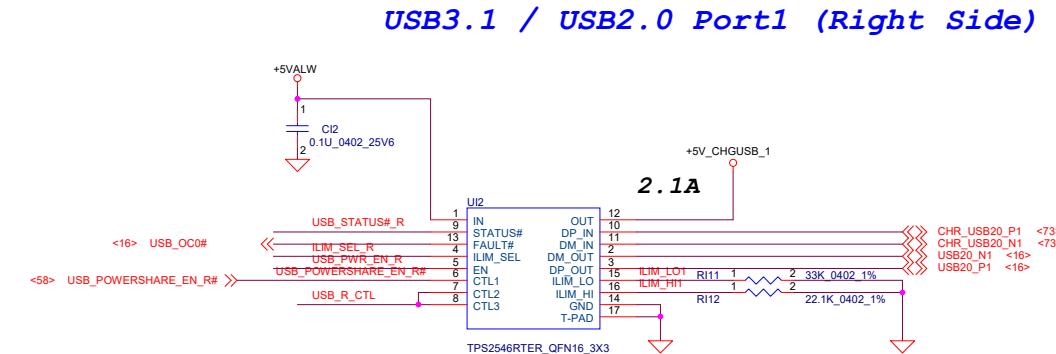
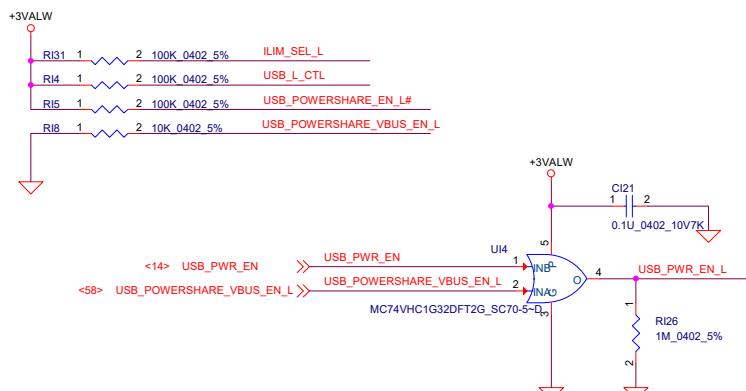
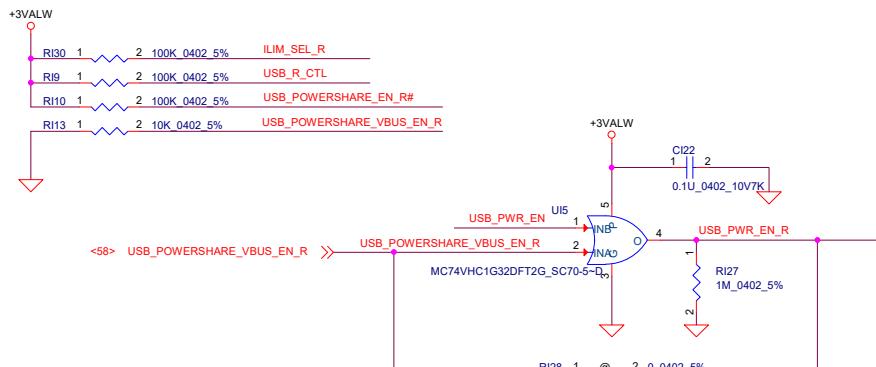


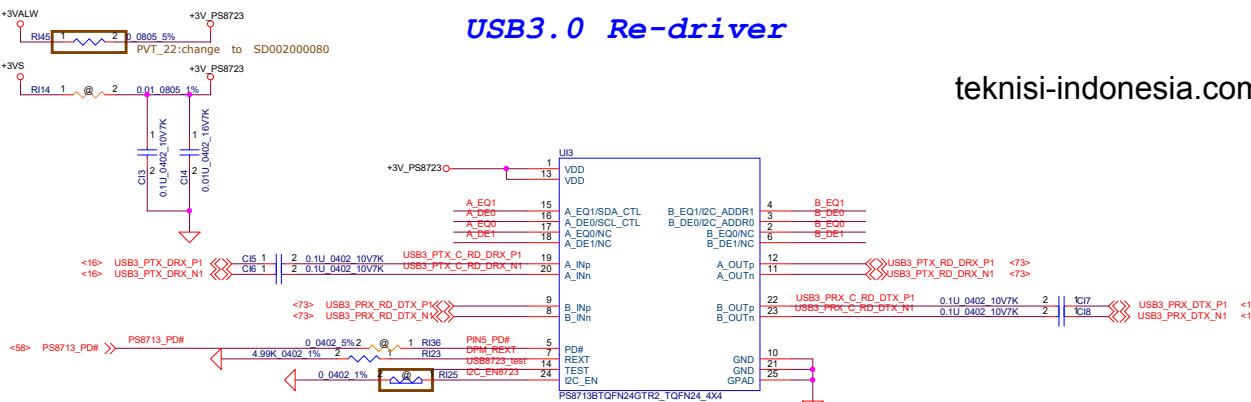
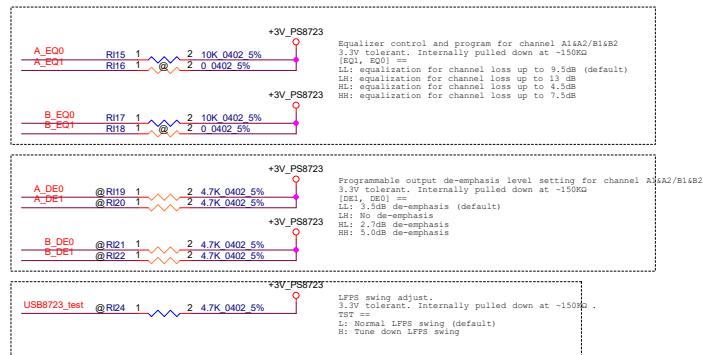
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Date:	Tuesday, April 30, 2019	Sheet	70	of	100	

USB Powershare

Device Control Pins				Flow Line Condition
CTL1	CTL2	CTL3	ILIM_SEL	
0	1	1	X	DCP AUTO
1	1	1	0	SDP
1	1	1	1	CDP

Suspend mode	CTL1 = 0 : Enable Power Share DCP mode in Suspend mode CTL1 = 1 : Disable Power Share in Suspend mode (For Support USB wake)
S0 mode	ILIM_SEL = 0 : SDP mode (0.9A by ILIM_LO setting) ILIM_SEL = 1 : CDP mode (STATUS# trigger by ILIM_HI = 2.2A)





Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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2017/06/21	2027/06/21	PS8713_PDI#	P072-USB3.1 retimer	Rev 1.0/100	
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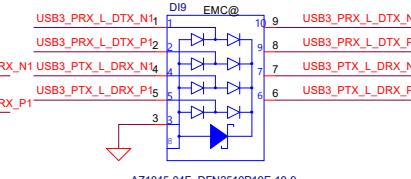
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 <71> CHR_USB20_P1<>

1 L12 2 CHR_USB20_N1_R
 4 3 CHR_USB20_P1_R
 DLM0NSN900HY2D_4P
 EMC@

<72> USB3_PTX_RD_DRX_N<>
 CI16 1 2 USB3_PTX_C_DRX_N1 RI37 0.0402 1% USB3_PTX_L_DRX_N1 USB3_PTX_L_DRX_N1
 <72> USB3_PTX_RD_DRX_P<>
 CI20 1 2 USB3_PTX_C_DRX_P1 RI38 0.0402 1% USB3_PTX_L_DRX_P1

0.1U_0402_10V7K
 0.1U_0402_10V7K

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 RI39 0.0402 1% USB3_PRX_L_DTX_P1
 <72> USB3_PRX_RD_DTX_N1 <>
 RI40 0.0402 1% USB3_PRX_L_DTX_N1



USB3.1 / USB2.0 Port1 (Left Side (BOT))

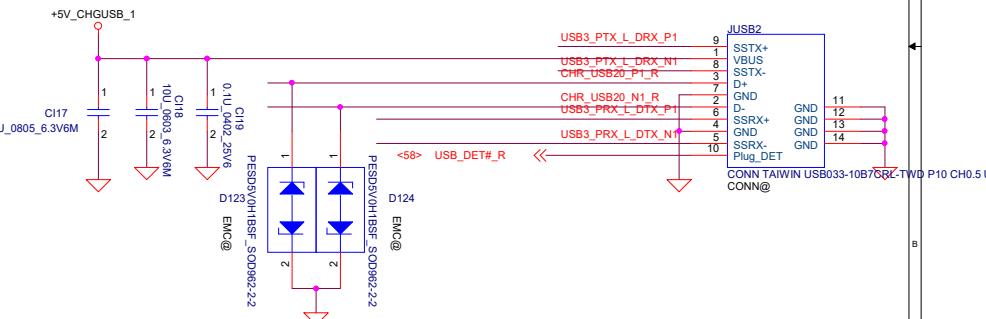
Place close to JUSB2

<71> CHR_USB20_N2<>
 <71> CHR_USB20_P2<>

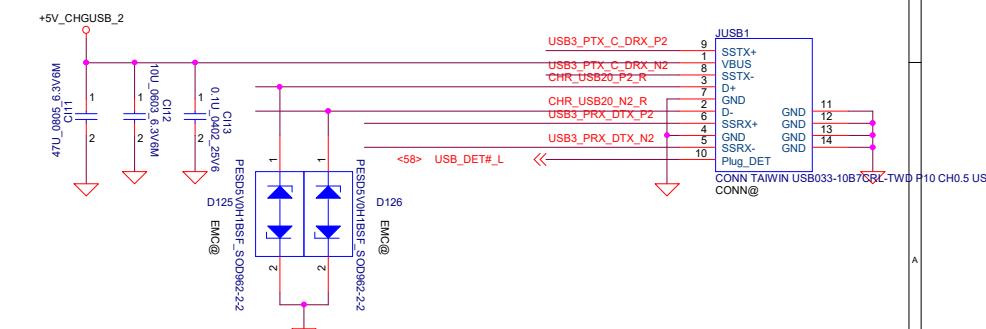
1 L15 2 CHR_USB20_N2_R
 4 3 CHR_USB20_P2_R
 DLM0NSN900HY2D_4P
 EMC@

<16> USB3_PRX_DTX_N2 <>
 CI9 1 2 USB3_PTX_C_DRX_N2
 <16> USB3_PRX_DTX_P2 <>
 CI10 1 2 0.1U_0201_10V6K
 <16> USB3_PTX_DRX_N2 <>
 CI9 1 2 0.1U_0201_10V6K
 <16> USB3_PTX_DRX_P2 <>
 CI10 1 2 0.1U_0201_10V6K

Place close to JUSB1



USB3.1 / USB2.0 Port2 (Right Side (BOT))



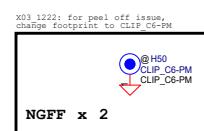
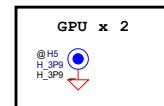
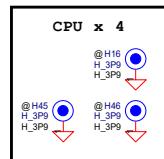
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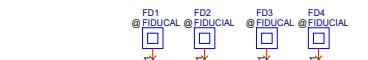
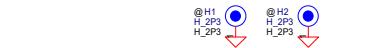
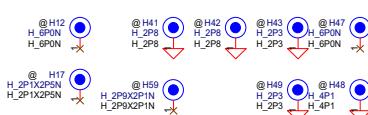
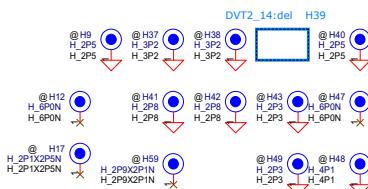
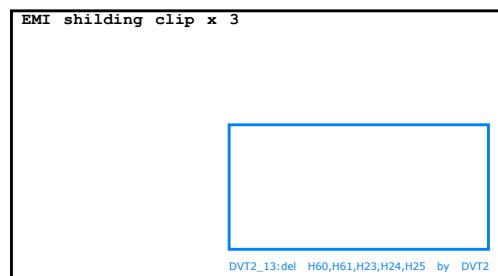
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Issued Date	2018/05/08	Deciphered Date	2018/05/08				
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Screw Hole

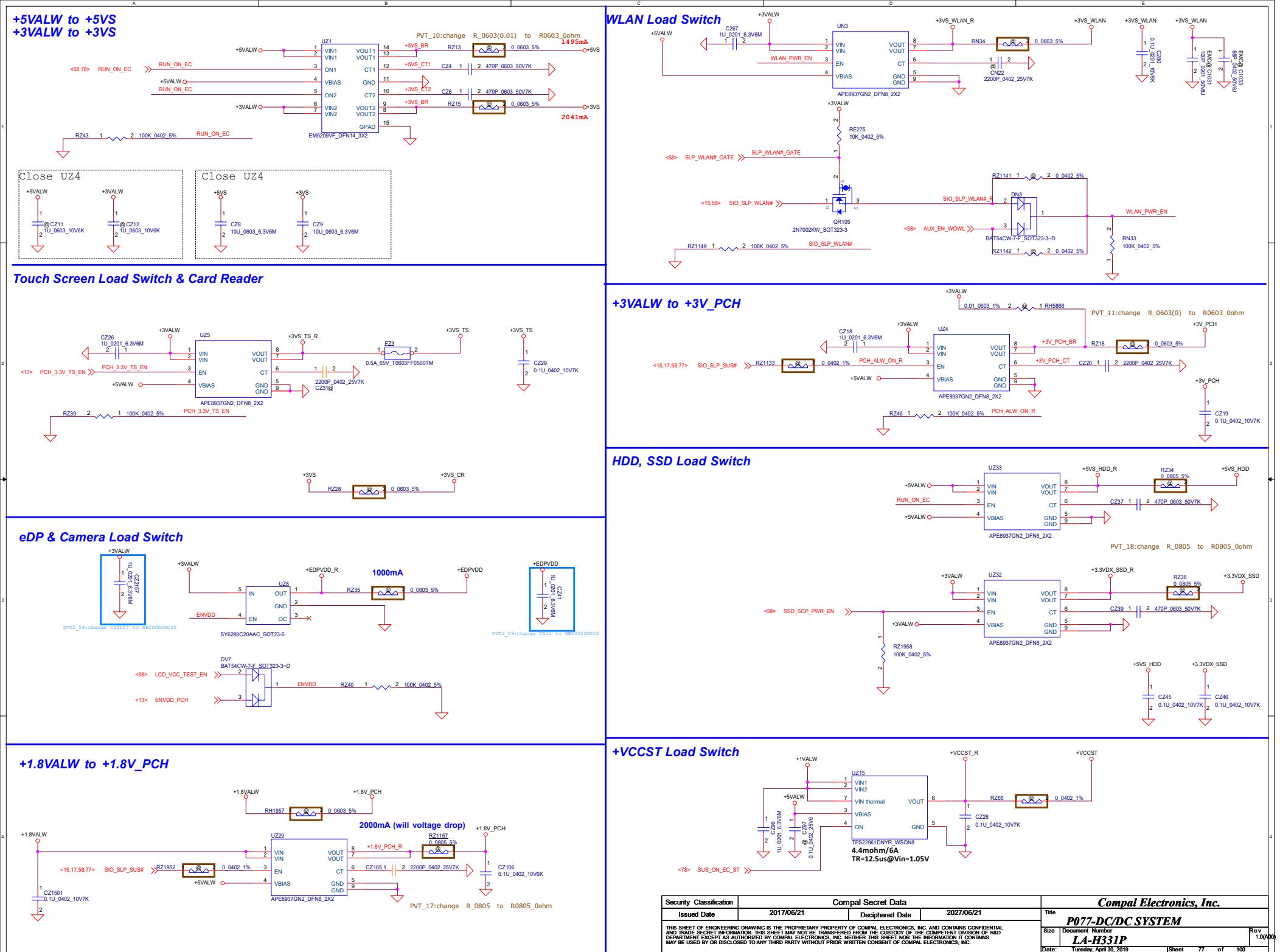


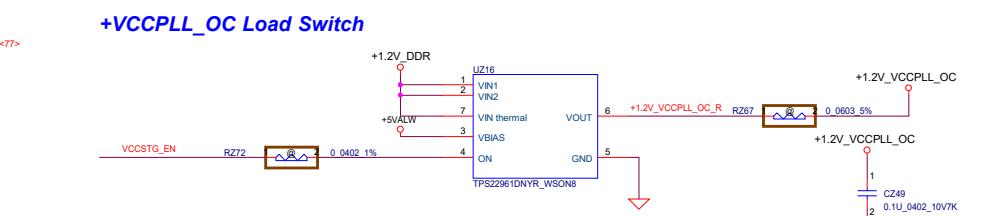
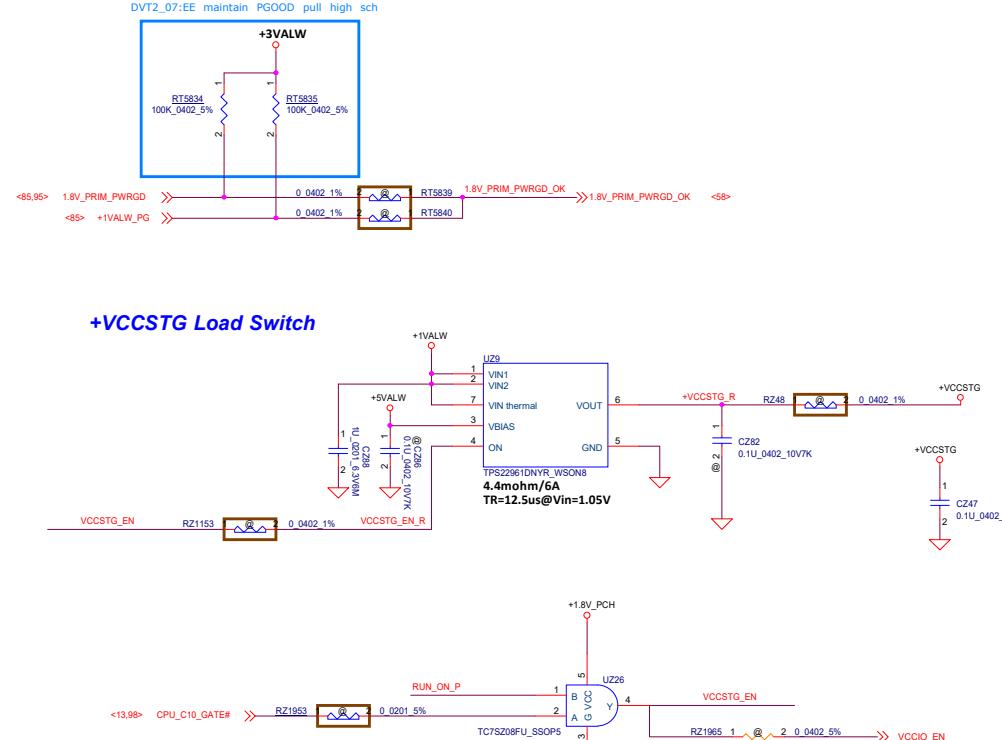
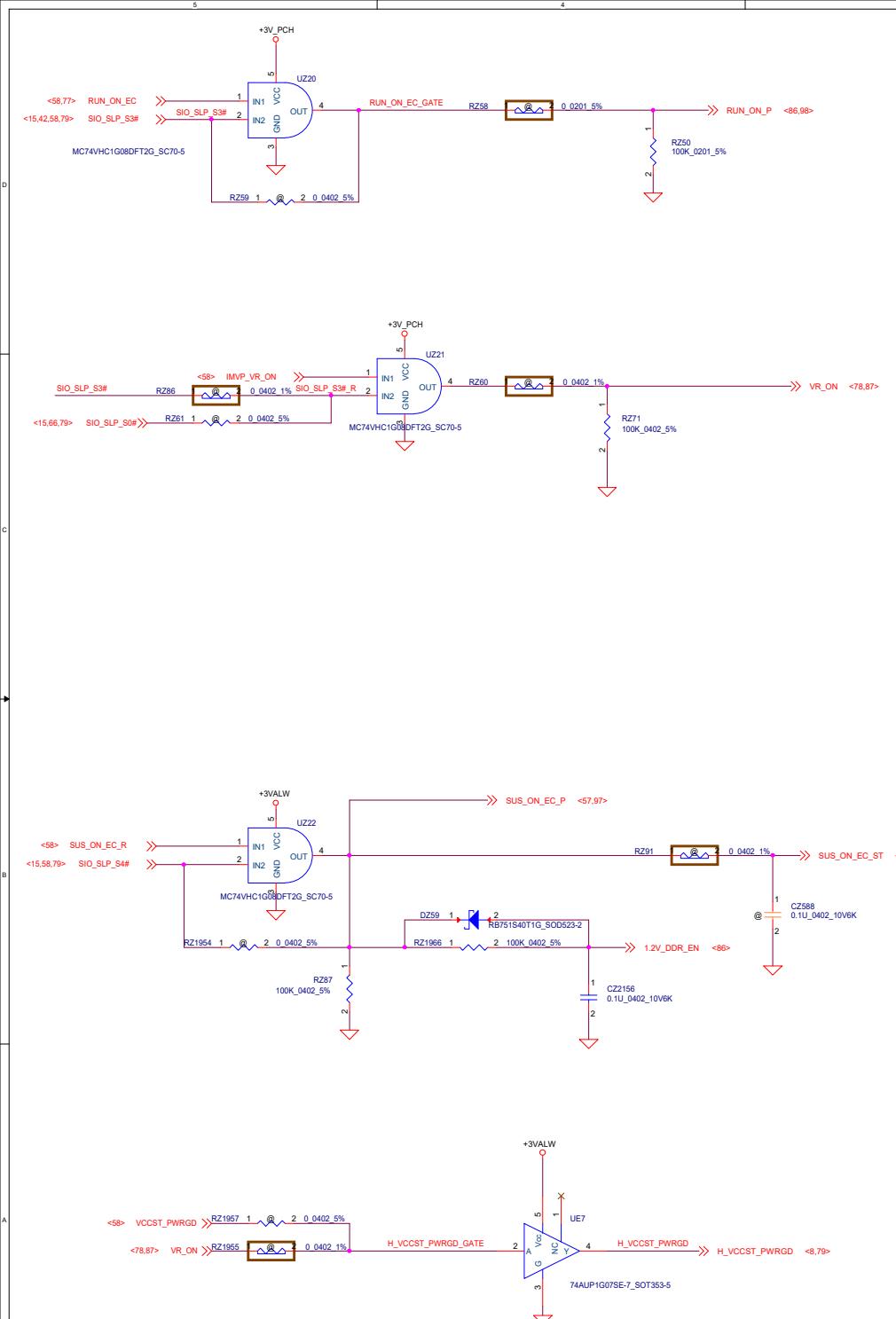
EMI shilding clip x 3



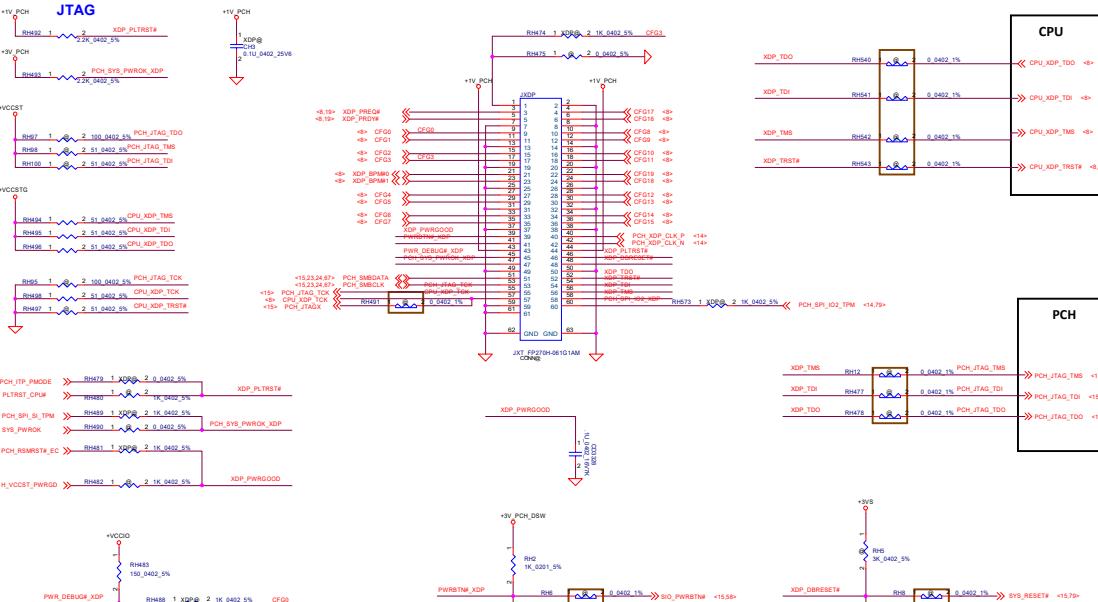
www.teknisi-indonesia.com

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Date:	Tuesday, April 30, 2019	Sheet	76	of	100

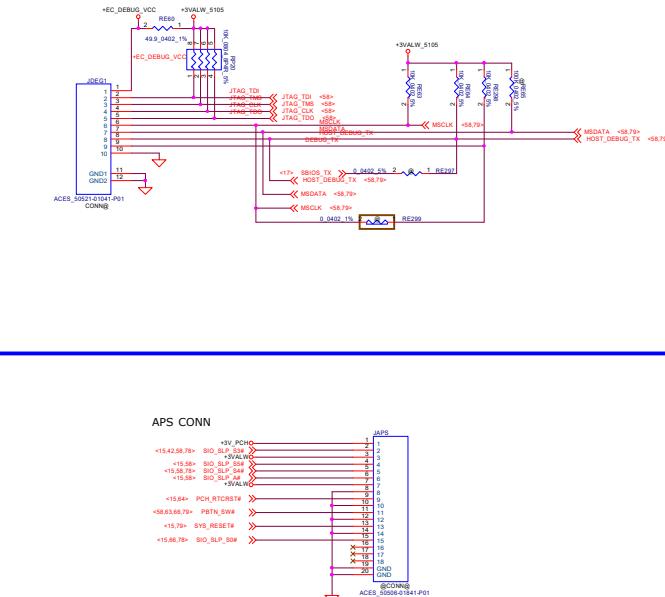




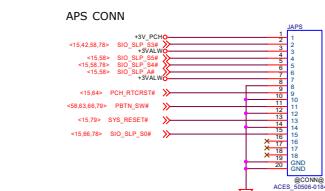
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	Date:	Tuesday, April 30, 2019	Sheet	78	of	100



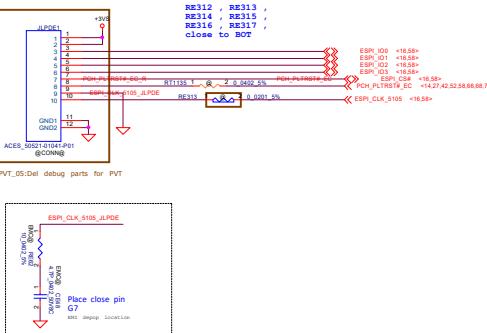
JDEC



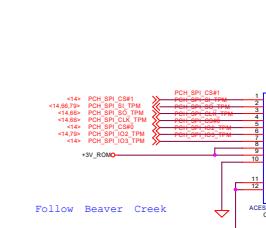
JAPS



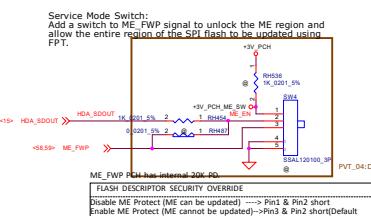
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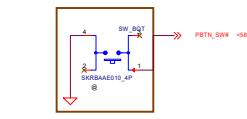
JSP



ME LOCK SW



Debug Power Button

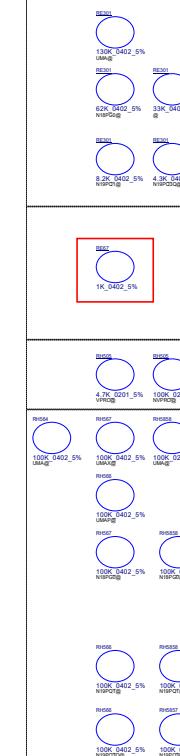
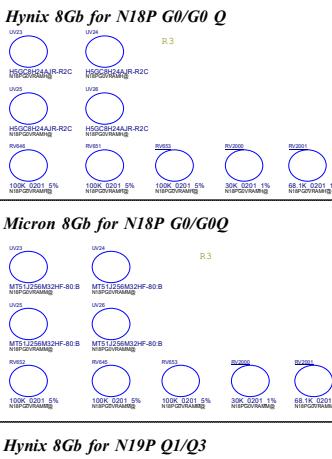
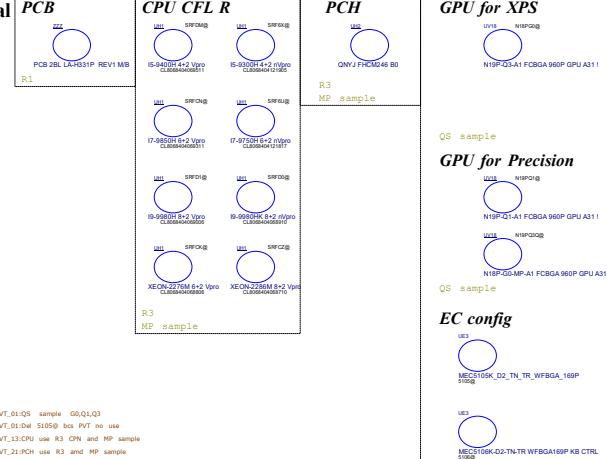


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Deciphered Date	2027/06/21			Title
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Compal Confidential

Project Code :

File Name :



RE301	CE3319	CONFIG
240K	4700p	
130K	4700p	UMA
62K	4700p	N18P-G0
33K	4700p	NA
8.2K	4700p	N19P-Q1
4.3K	4700p	N19P-Q3 M
2K	4700p	
1K	4700p	

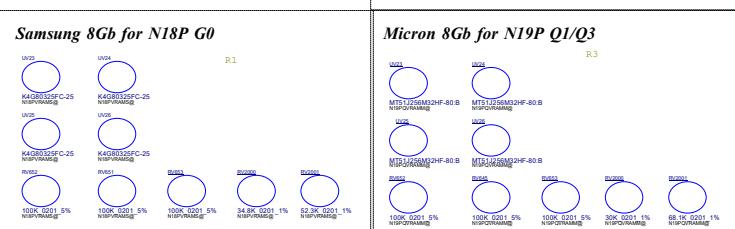
RE67	CE51	REV	PH
240K	4700p		PRE
130K	4700p	X00	EV
62K	4700p	X01	DV
33K	4700p	X02	DV
8.2K	4700p		
4.3K	4700p		
2K	4700p		
1K	4700p	A00	PV

TLS CONFIDENTIALITY	
HIGH(4.7K)	
5%	LOW(DEFAULT)(100K) BIOS 20k Internal pull-down

BRIDGE	BRIDGE
100K 0420 5%	100K 0201 5%
4PINS 0420	4PINS 0201
100K 0420 5%	100K 0201 5%
4PINS 0420	4PINS 0201
100K 0420 5%	100K 0201 5%
4PINS 0420	4PINS 0201
130K 0420 5%	82K 0420 5%
4PINS 0420	4PINS 0420
1K 0420 5%	1P 0420 5%
4PINS 0420	4PINS 0420

RE336	CE3326	CONFIG
240K	4700p	2PHASE-15
130K	4700p	3PHASE-15
62K	4700p	
33K	4700p	
8.2K	4700p	4PHASE-6+2
4.3K	4700p	
2K	4700p	
1K	4700p	4PHASE-8+2

GPU type	Config Sku/Division	SYSTEM ID1		SYSTEM ID2		SYSTEM ID3			
		BID	DIS	BID	XPS_CSBM	BID	PersisBC	BID	DIS
IGFX	XPS_CSBM	UMA	H	L		L			
	PersisBC	UMA	H	H		L			
DGFX	XPS_CSBM	Nvidia N18P-G0	L	L	L	L			
	PersisBC	Nvidia N18P-Q0_MX.0Q	L	L	L	H			



DRAM Option

DRAM Config Option

DRAFT Config option

DRAM SDR / DDR Option

R COMP X3

SDP
MICRON 8G/2400

SDP
HYNTX 8G/2400

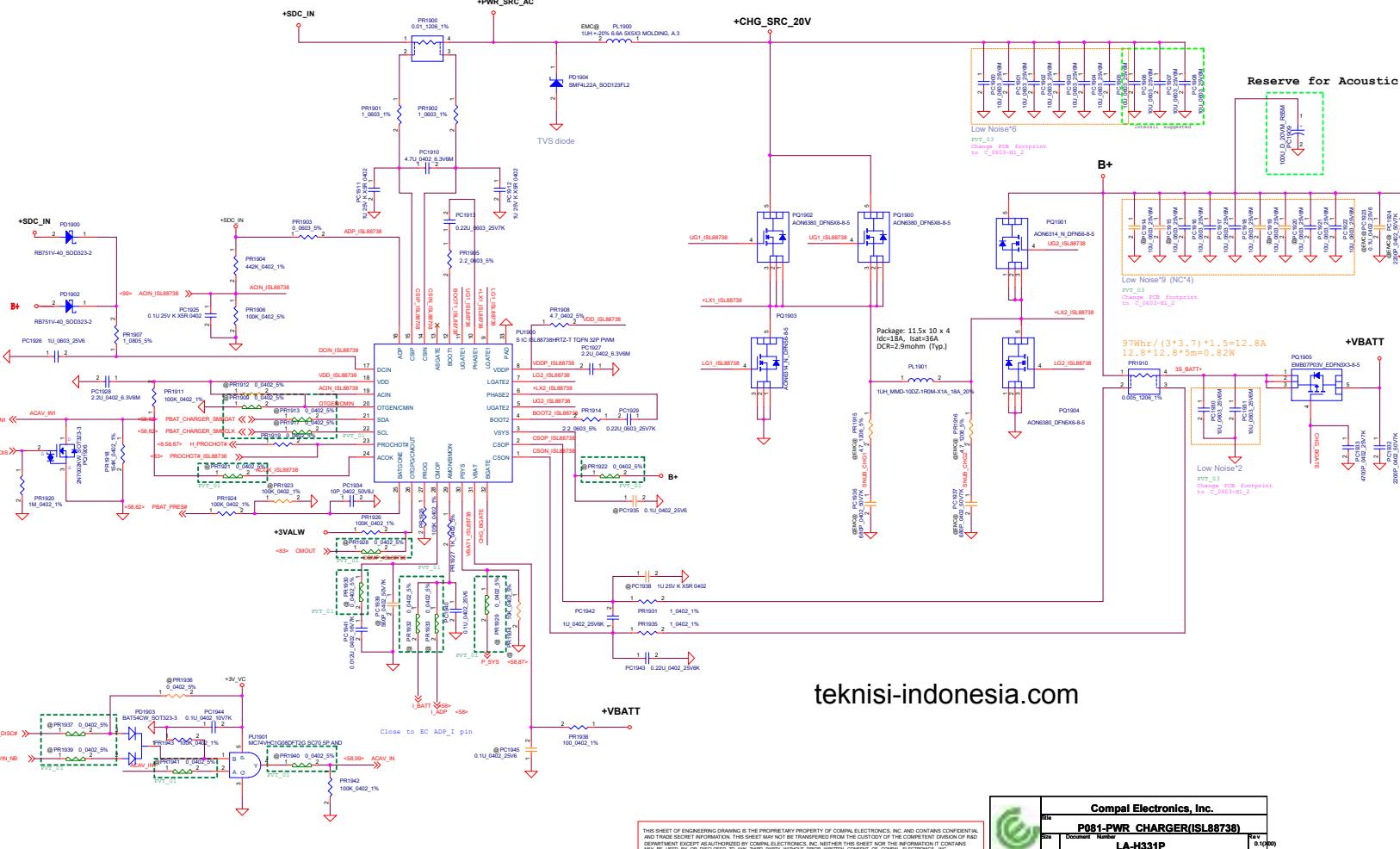
SDP
SAMSUNG 8G/2400

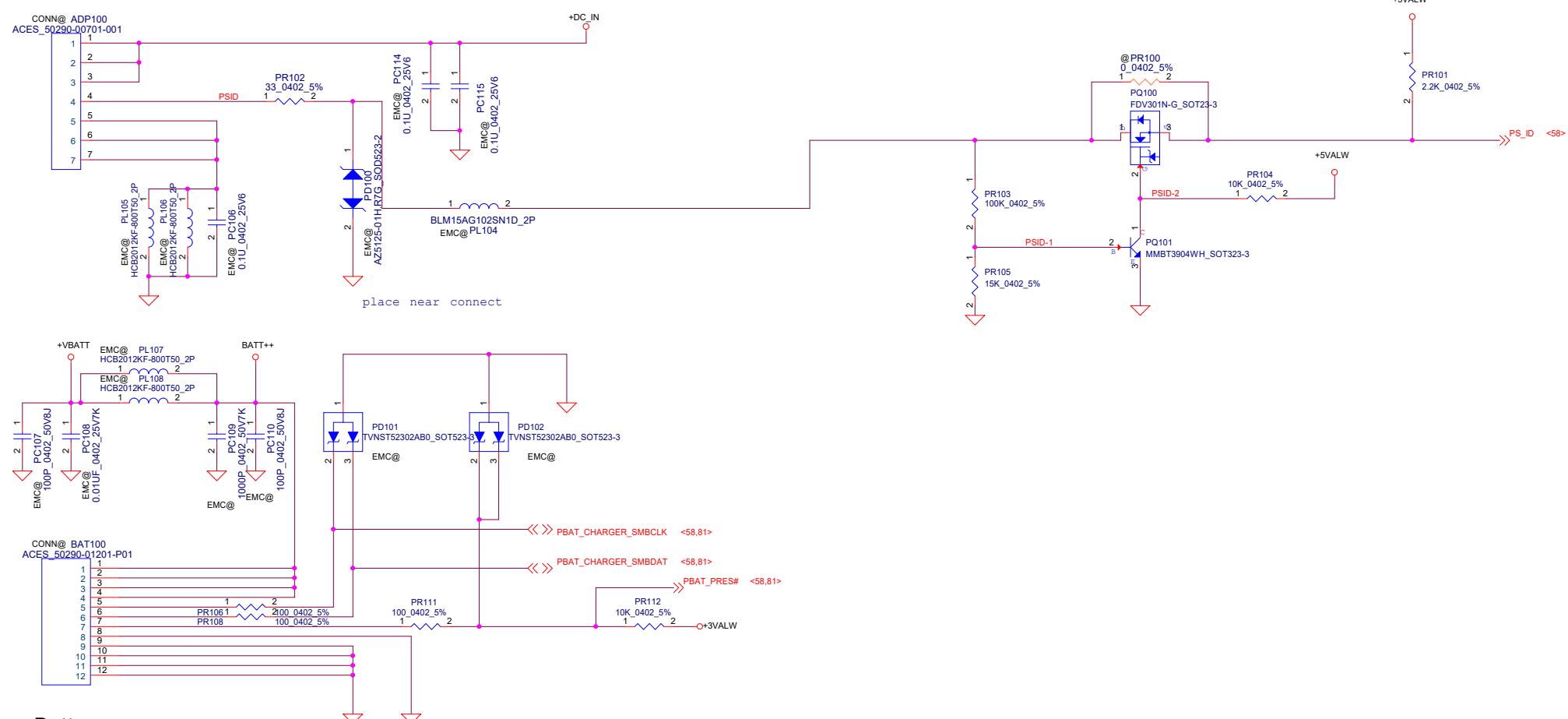
DDP
MICRON 16G/2400

DDP
HYNIX 16G/2400

DDP
SAMSUNG 16G/2400

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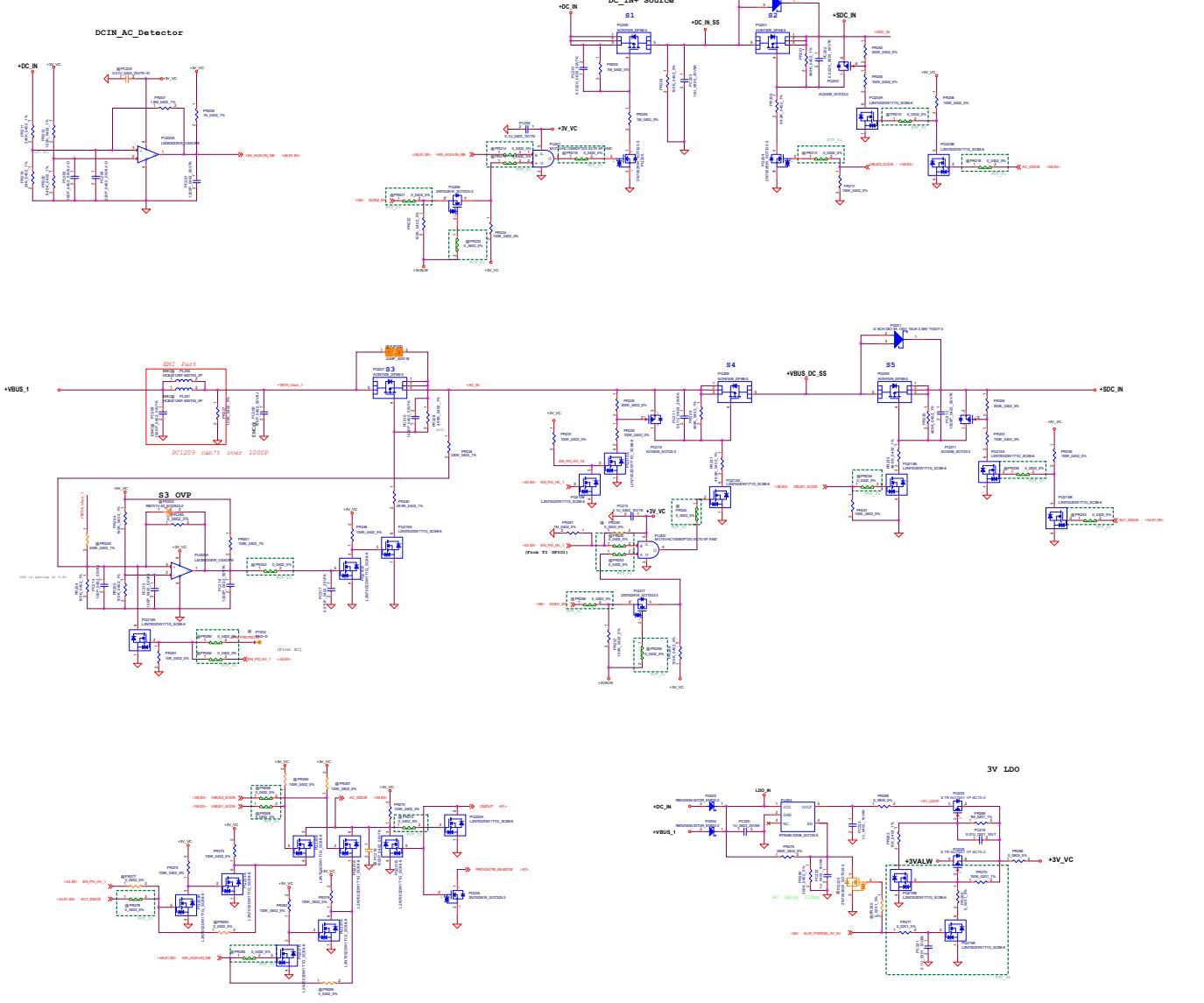
Battery (3S2P) 97W (3S1P) 56W

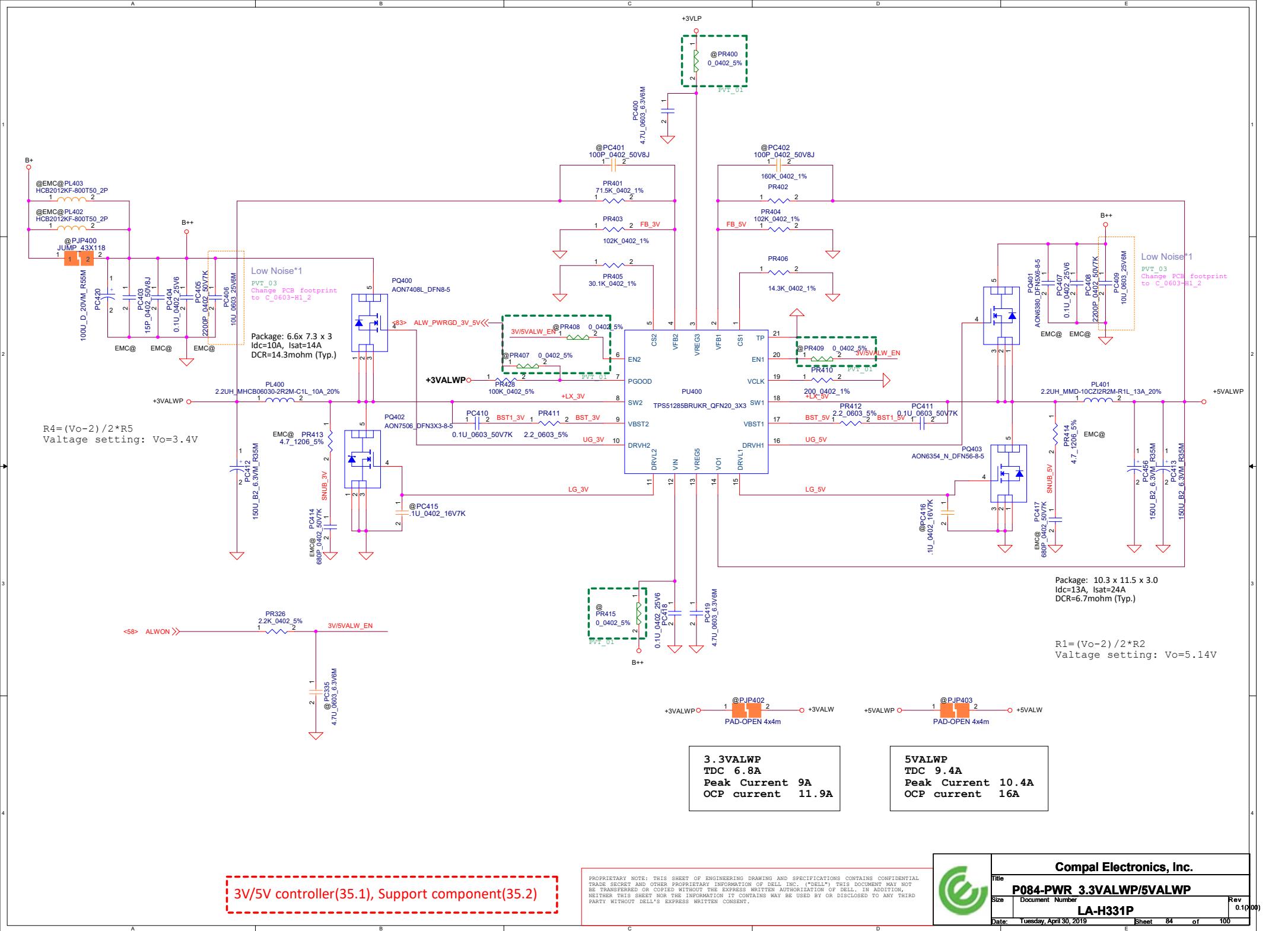
JIMBTY battery connector

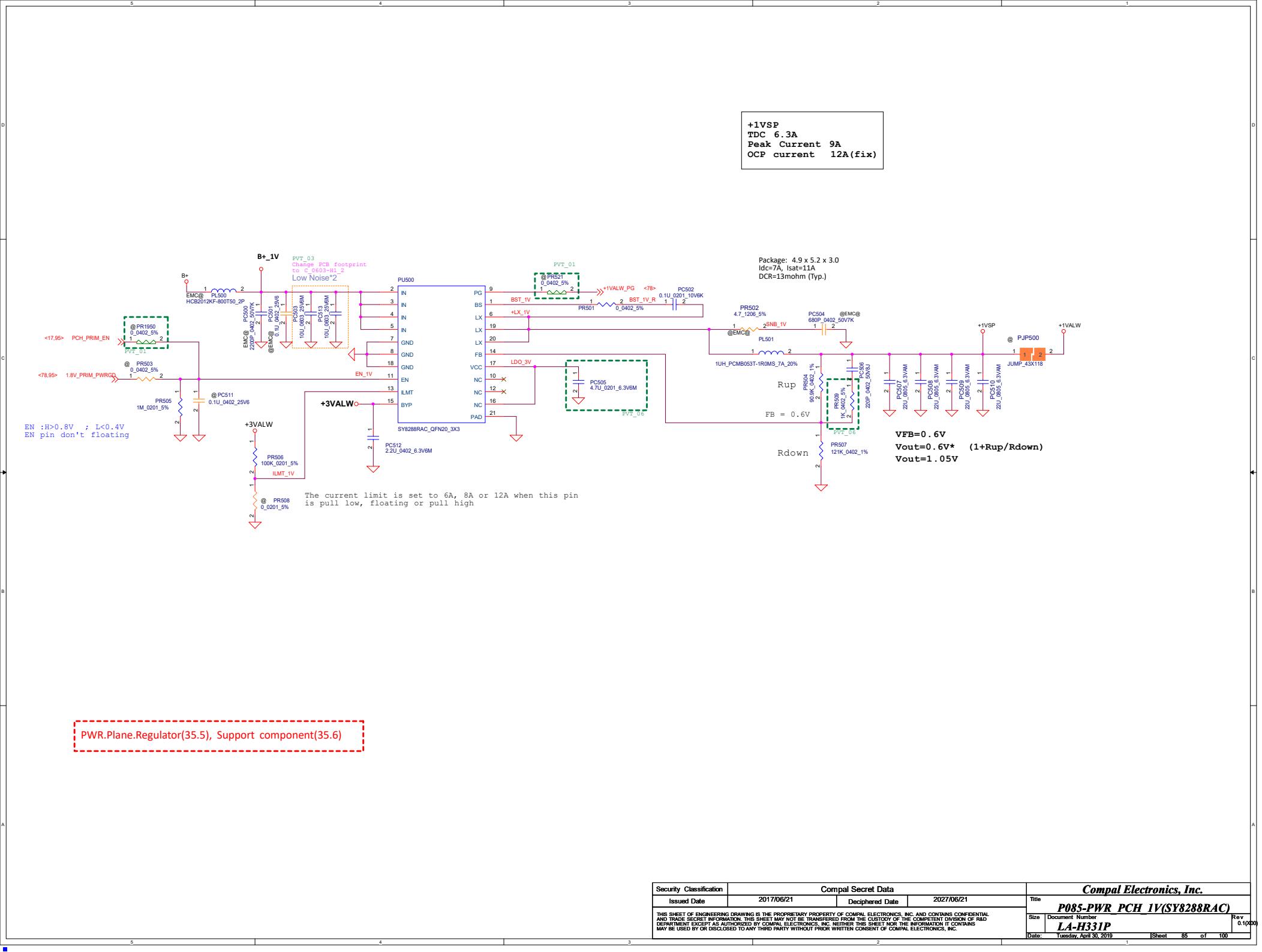
SMART
Battery:
01.BAT+
02.BAT+
03.BAT+
04.BAT+
05.CLK_SMB
06.DAT_SMB
07.BATT_PRS
08.SYS_PRS
09.GND
10.GND
11.GND
12.GND

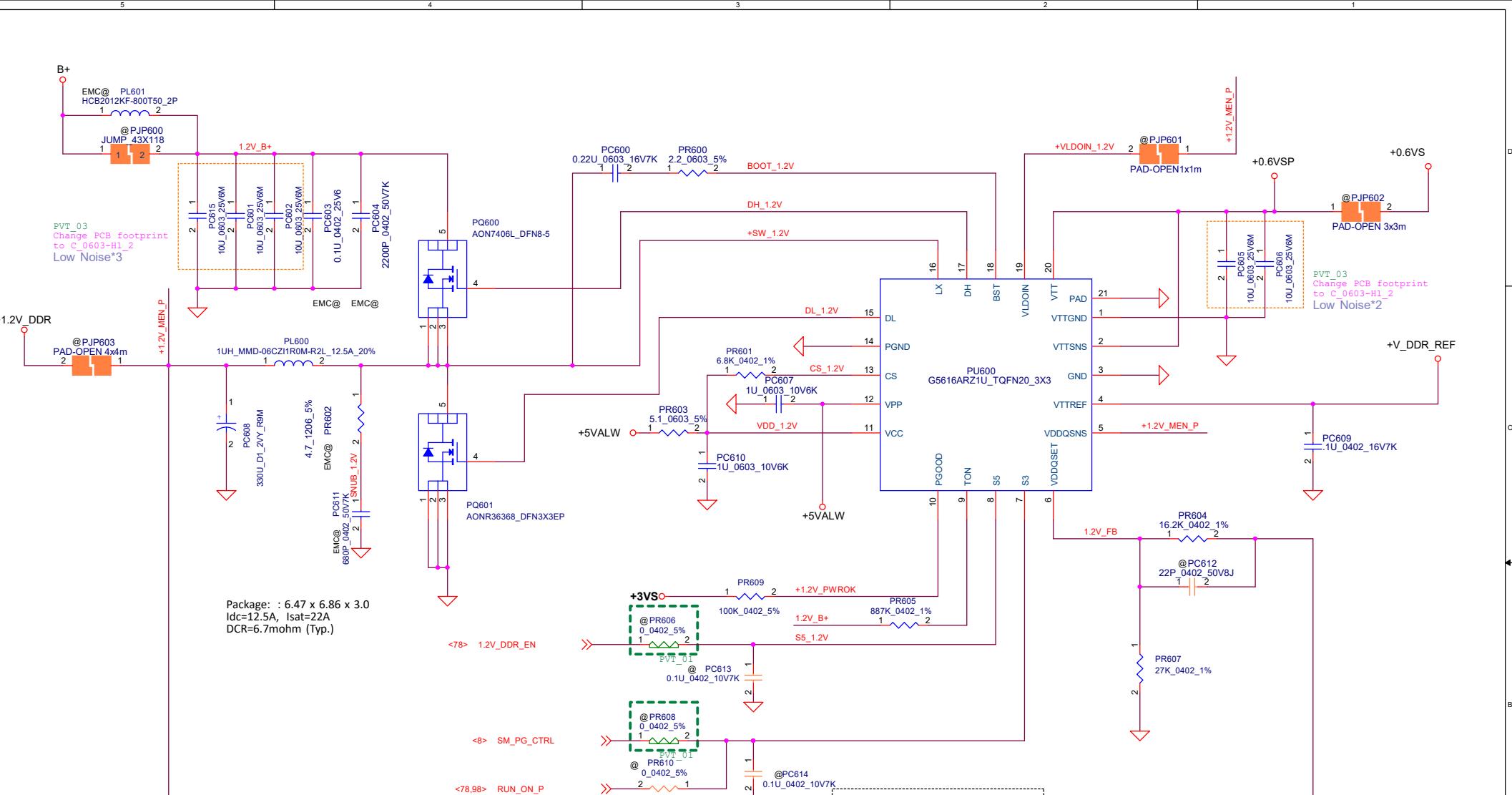
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Smart Adapter circuit (39.1)







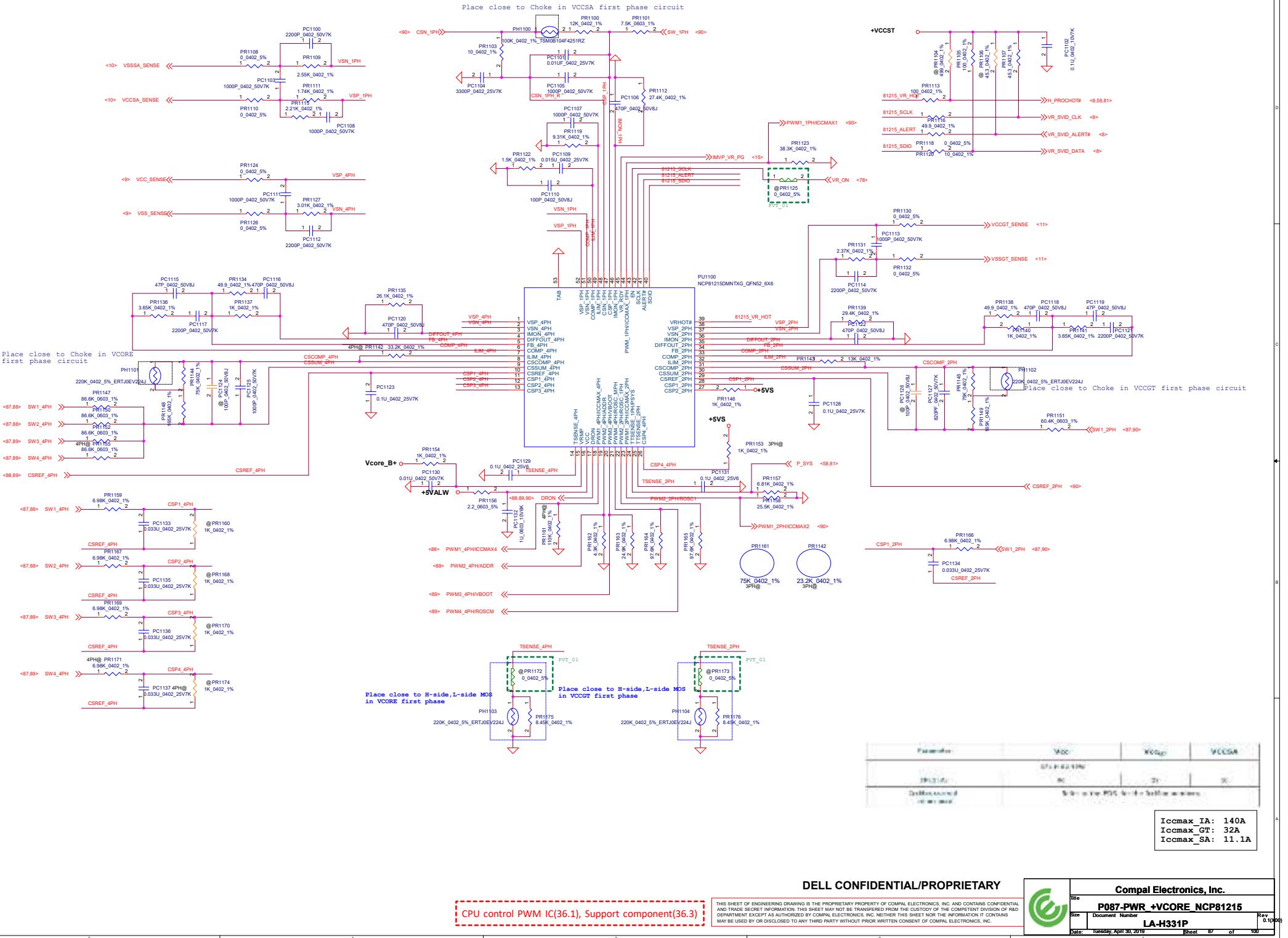


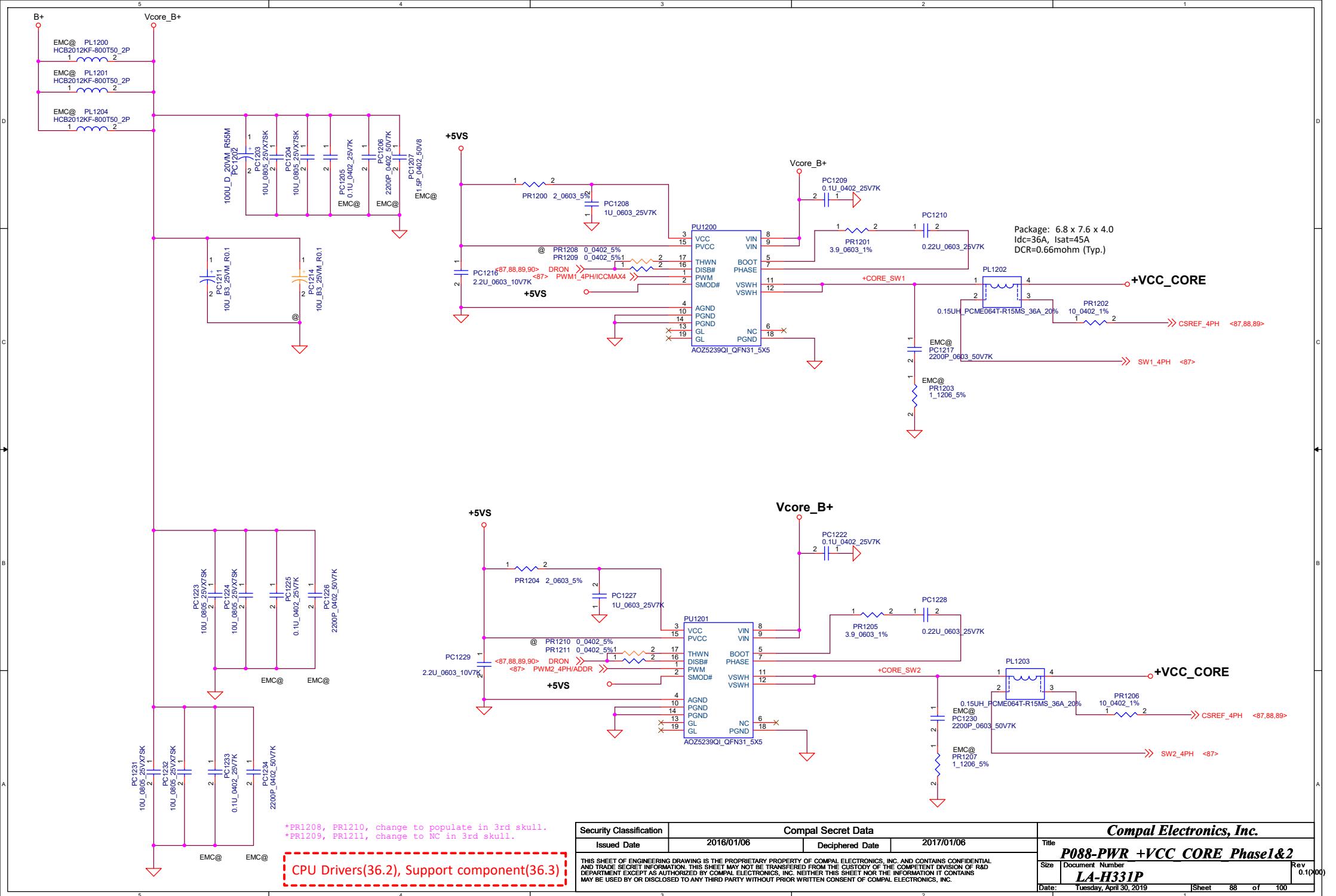
1.2Volt +/- 5%
 TDC 7.13A
 Peak Current 10.2A
 OCP current 12.12A

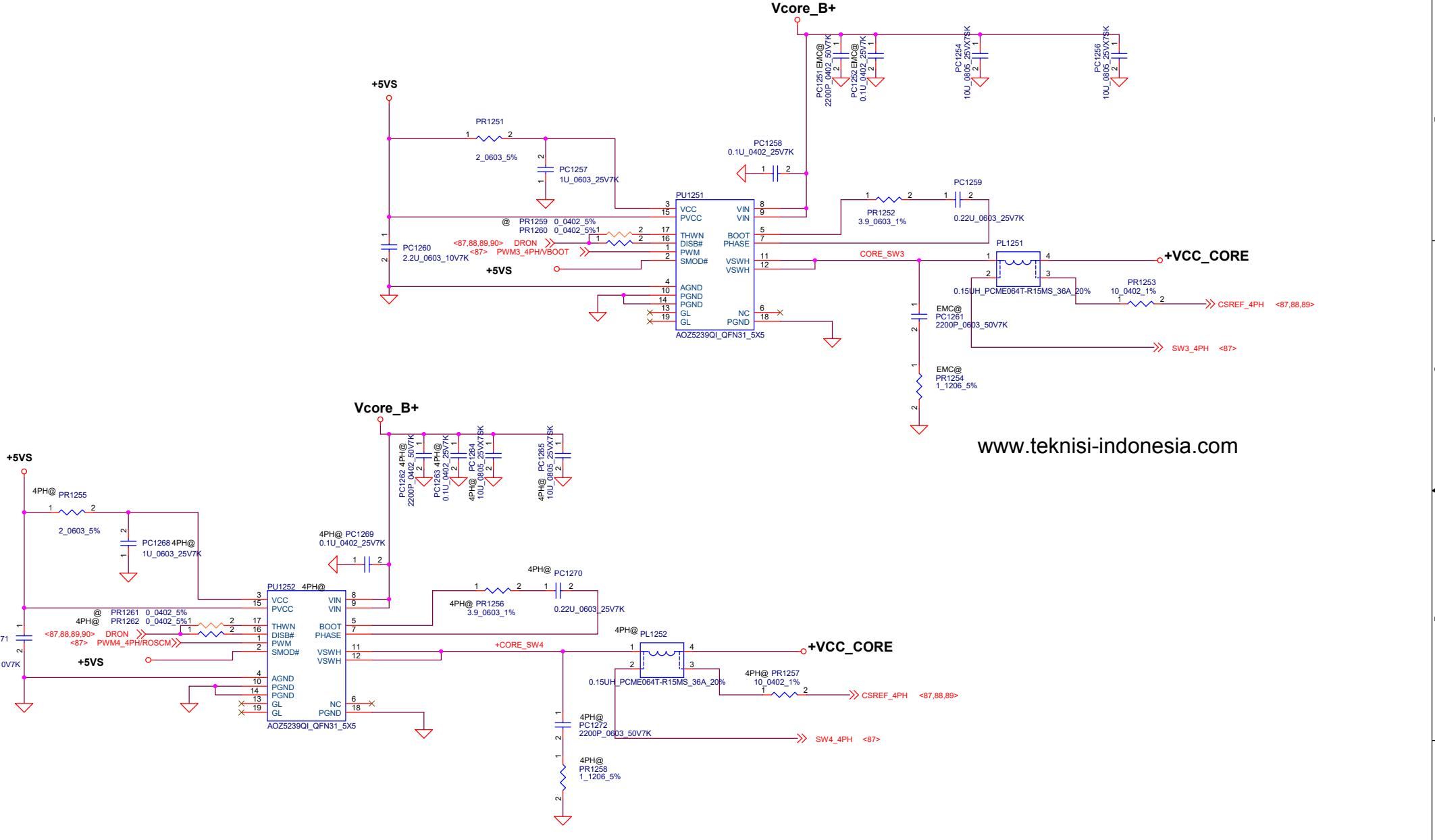
0.6Volt +/- 5%
 TDC 0.7A
 Peak Current 1A
 OCP Current 1.19A

DDR controller(35.3), Support component(35.4)

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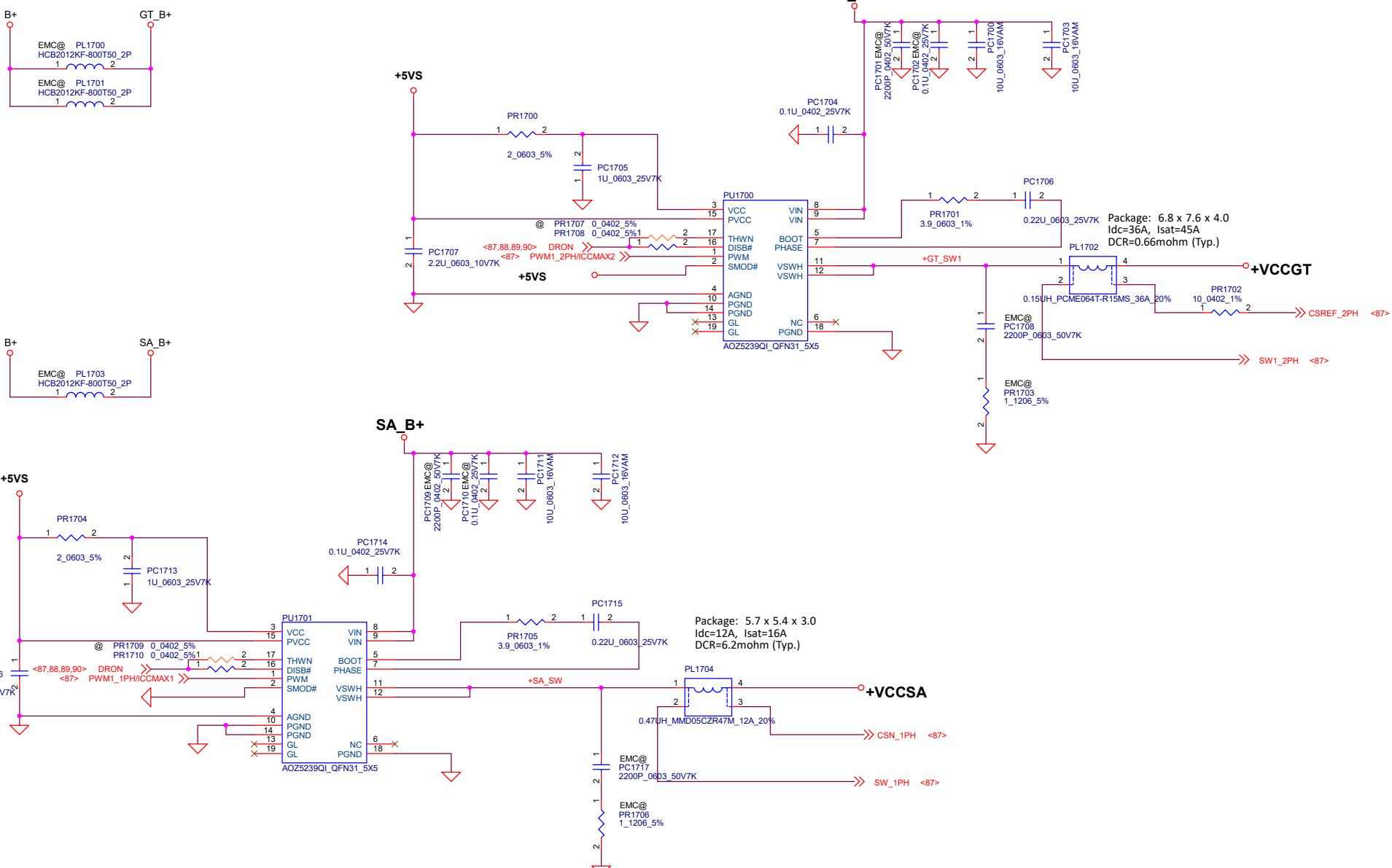




*PR1259, PR1261, change to populate in 3rd skull.
*PR1260, PR1262, change to NC in 3rd skull.

CPU Drivers(36.2), Support component(36.3)

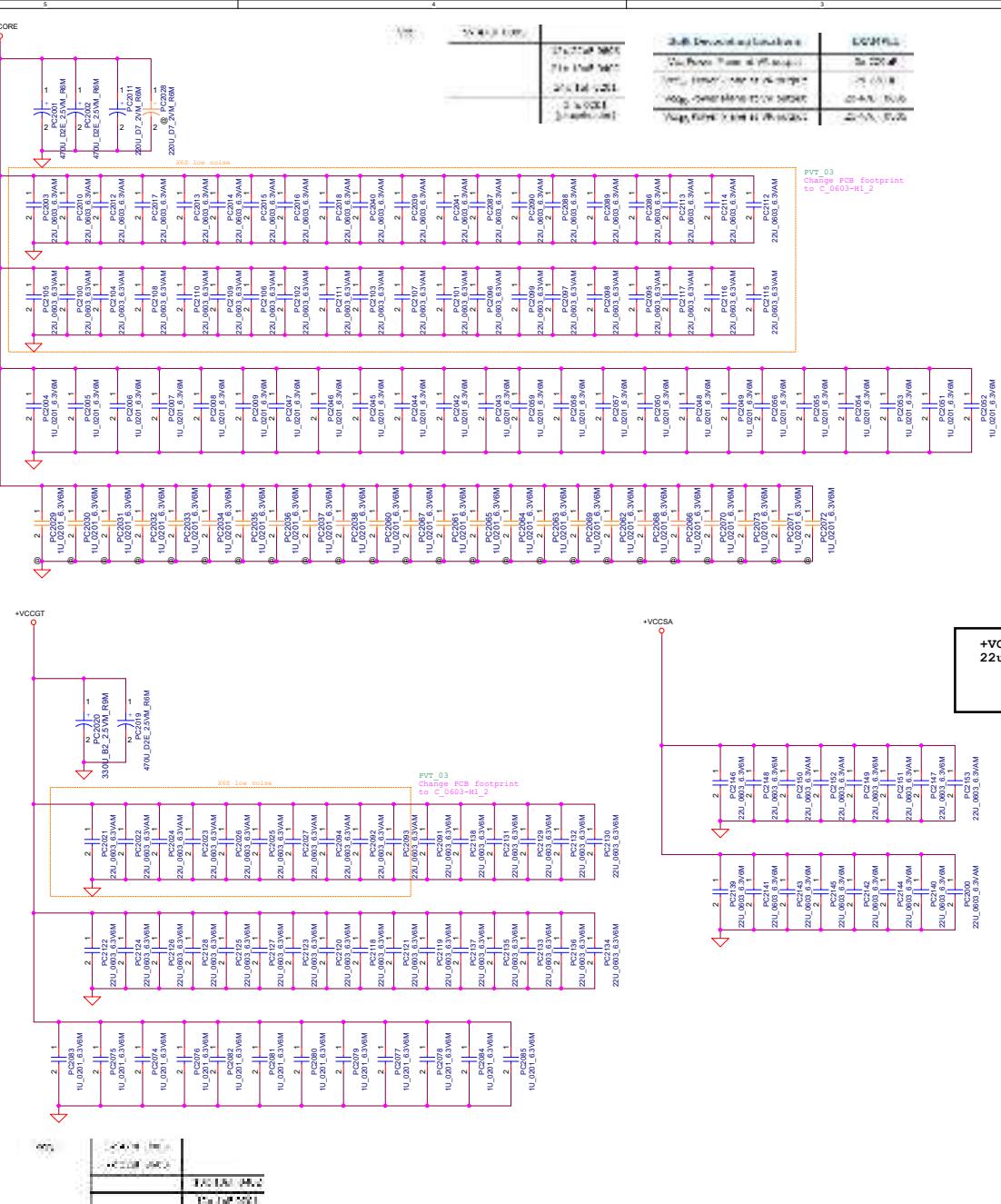
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Issued Date	2016/01/06	Deciphered Date	2017/01/06 <th>Title</th> <td>P089-PWR +VCC CORE Phase3&4</td>	Title	P089-PWR +VCC CORE Phase3&4
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Size	Document Number	Rev		LA-H331P	0.1(N00)
Date:	Tuesday, April 30, 2019	Sheet	89	of	100



*PR1707, PR1709, change to populate in 3rd skull.
*PR1708, PR1710, change to NC in 3rd skull.

CPU Drivers(36.2), Support component(36.3)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/01/06	Deciphered Date	2017/01/06 <th>Title</th> <td>P090-PWR +VCC GT/+VCC SA</td>	Title	P090-PWR +VCC GT/+VCC SA
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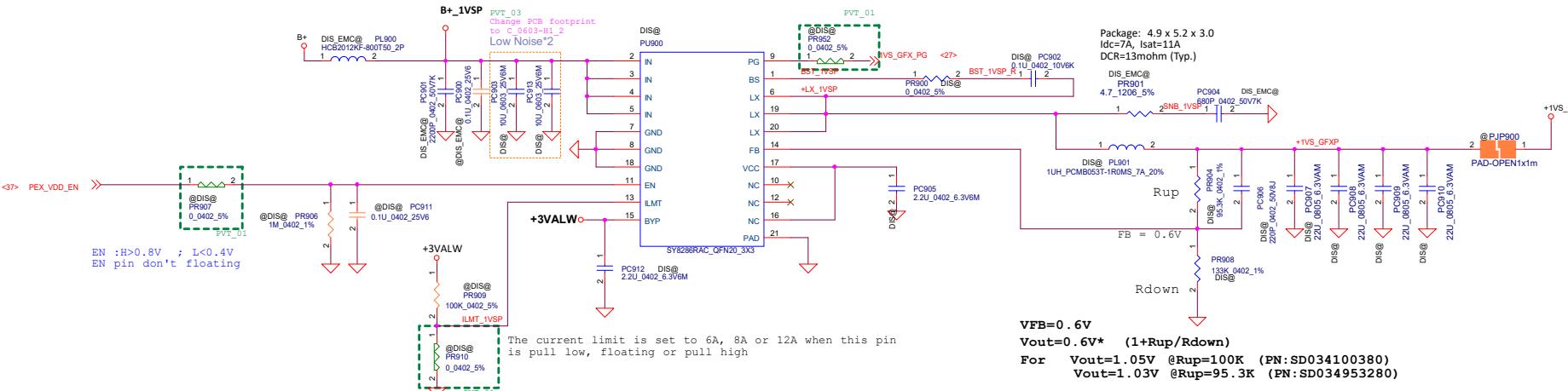
Security Classification	Compal Secret Data			Title
Issued Date	Deciphered Date	2027/06/21		P091-PWR PROCESSOR DECOUPLING
2017/06/21				Compal Electronics, Inc.
				LA-H331P

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CPU Output CAPS(36.4)

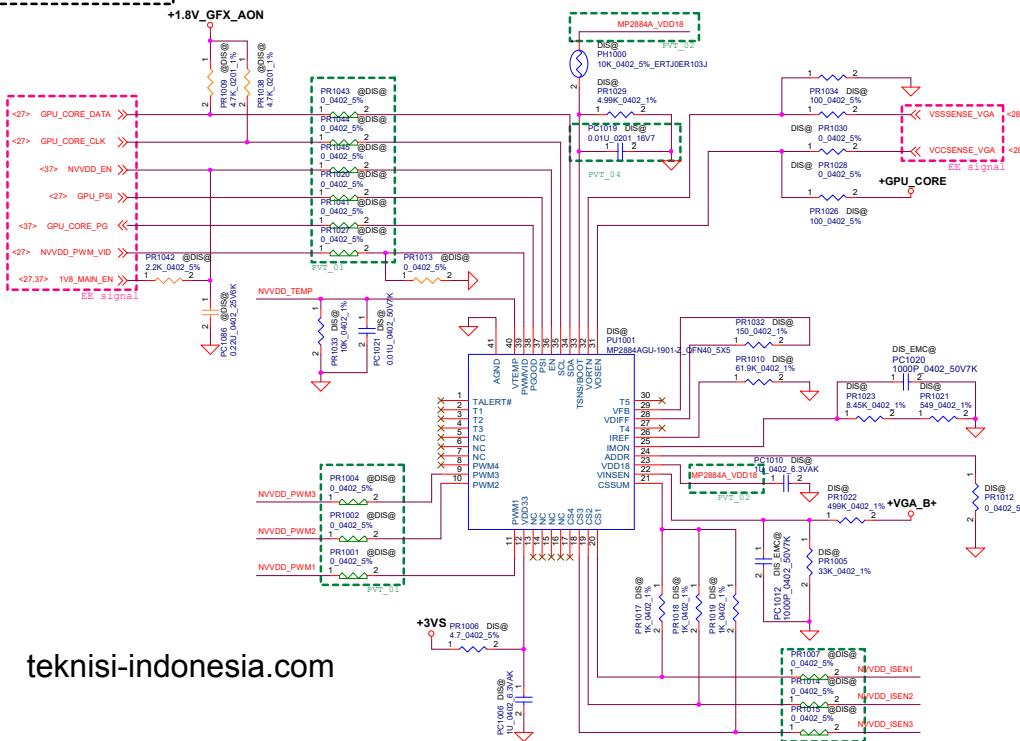
for dGPU SKU
 @DIS@ : Nopop Component
 DIS@ : POP for dGPU SKU

+1.0VSP/1.05VSP
 TDC 1.1A
 Peak Current 1.1A
 OCP current 6A(fix)

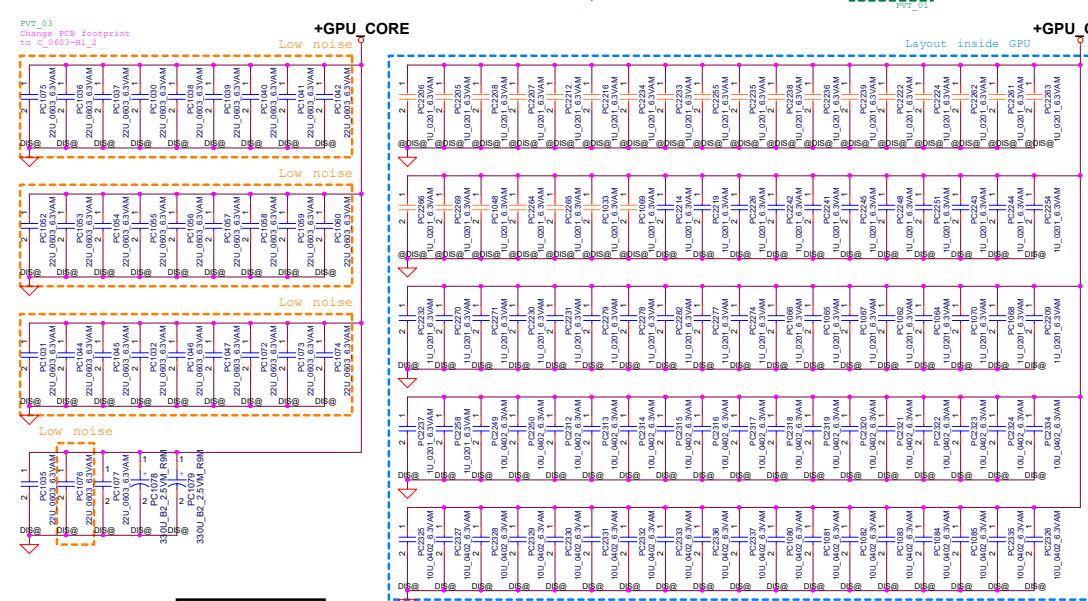


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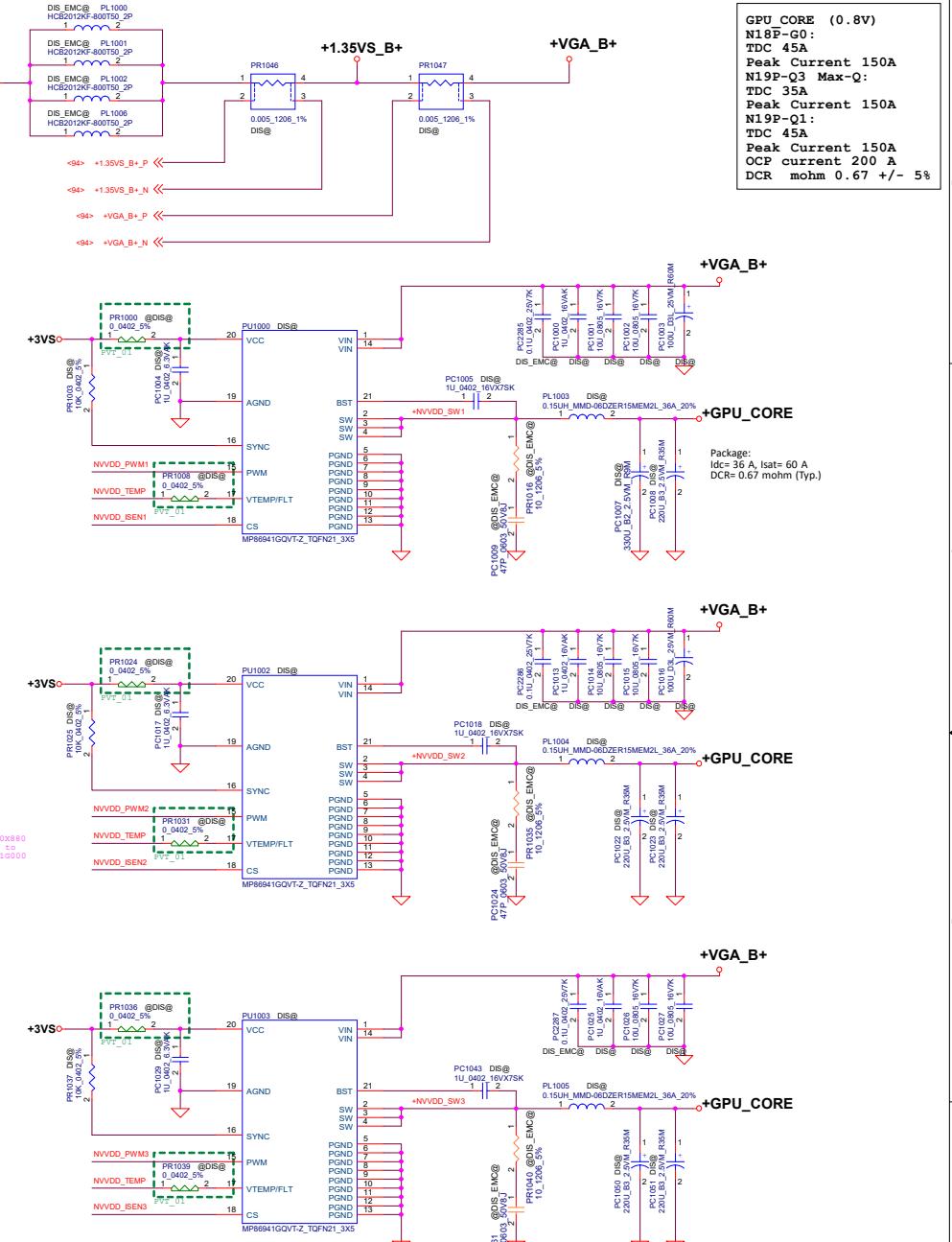
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for dGPU SKU  
@DIS@ : Nopop Component  
DIS@: POP for dGPU SKU
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GPU_CORE
330uF*3
220uF*5
22uF*30
10uF*34
1uF*56 (25NC)



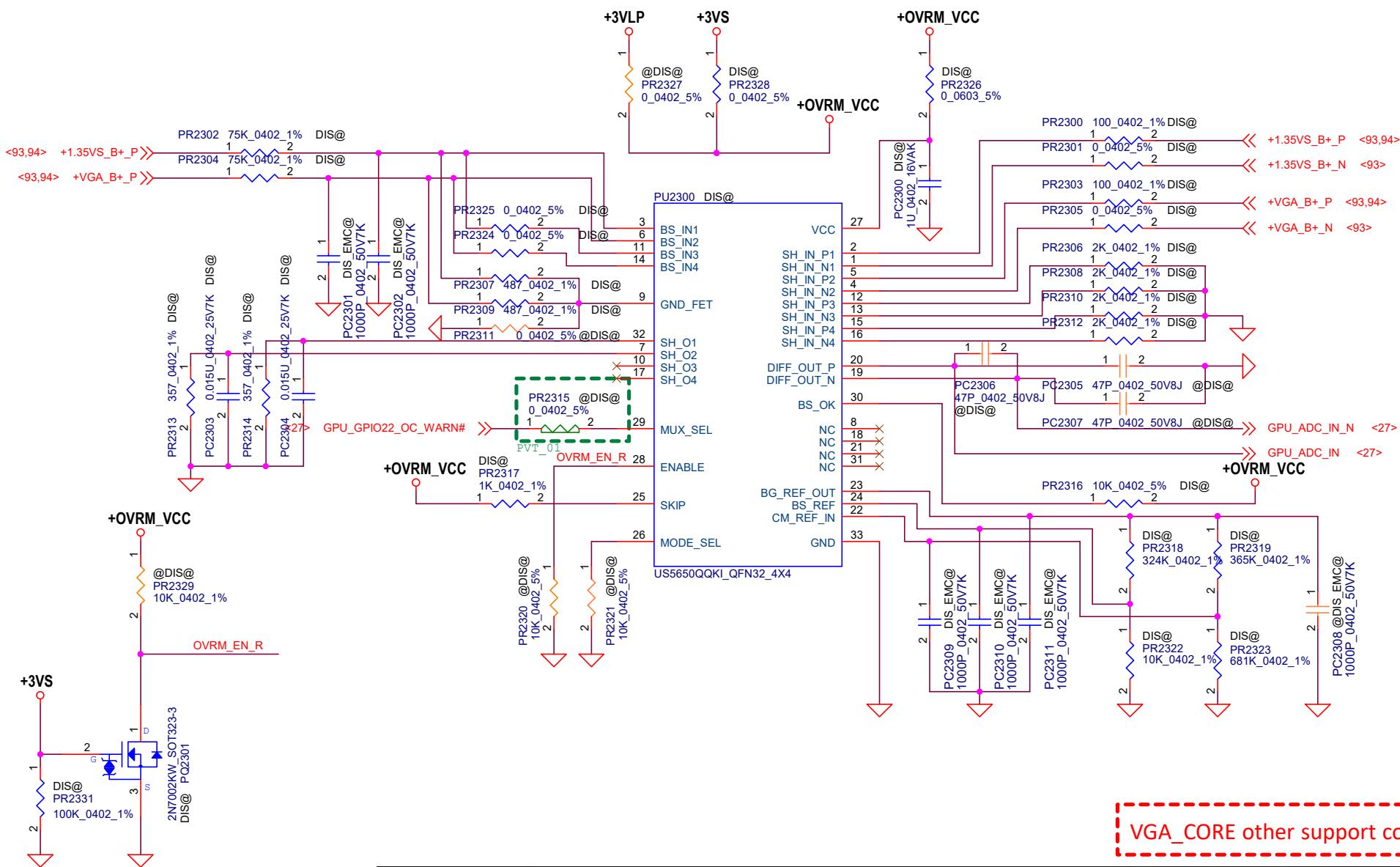
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VGA_CORE controller(43.1), Support component(43.2)
VGA_CORE Drivers (43.3), GPU Core Output CAP (43.9)

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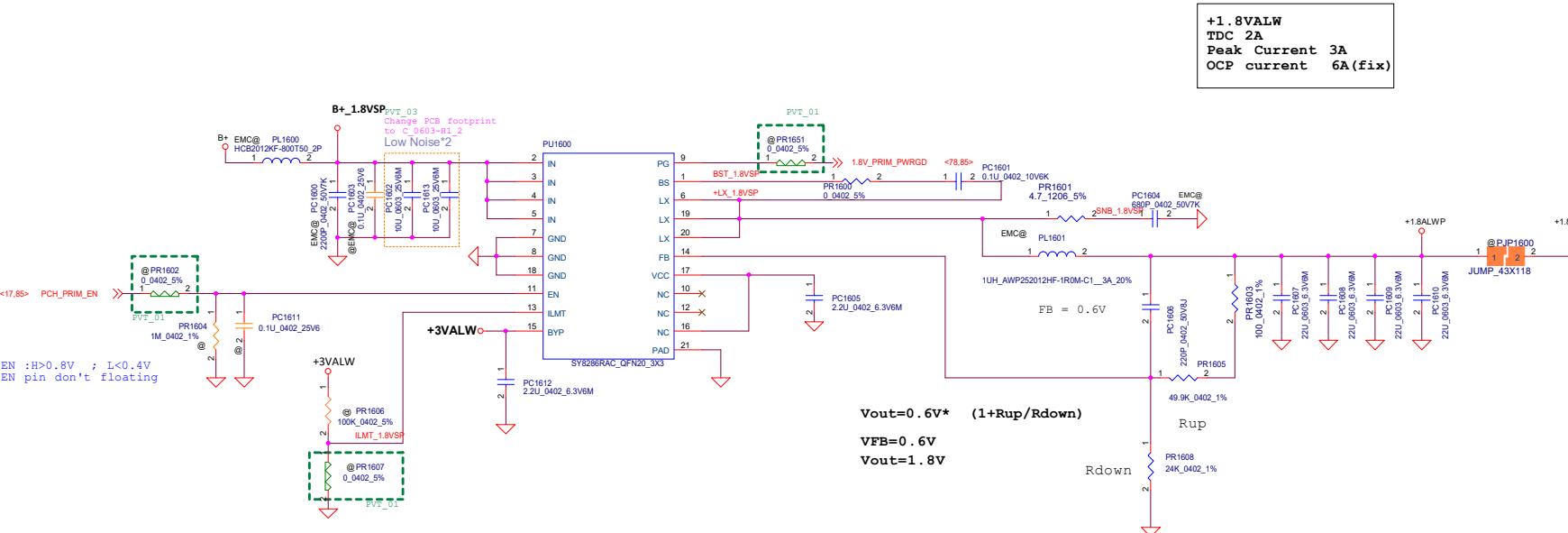
```

GPU_CORE (0.8V)
I18P-G0:
  VDC 45A
  Peak Current 150A
I19P-Q3 Max-Q:
  VDC 35A
  Peak Current 150A
I19P-Q1:
  VDC 45A
  Peak Current 150A
I2CP current 200 A
I2CR mohm 0.67 +/-
```

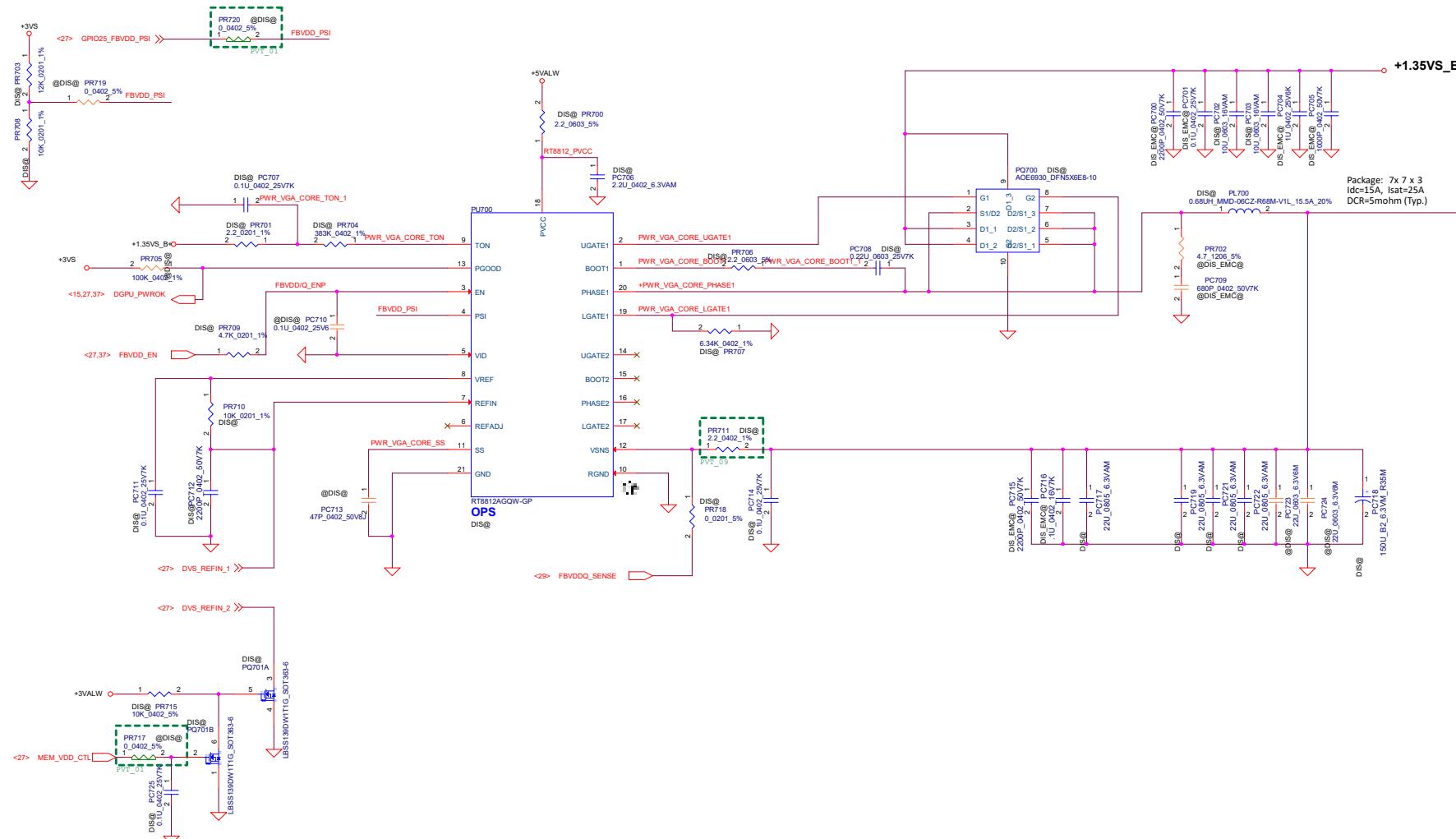


VGA_CORE other support component(43.8)

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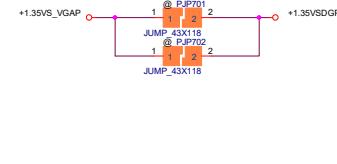
```
for dGPU SKU  
@DIS@ : Nopop Component  
DIS@: POP for dGPU SKU
```



```

1.35VS VGAP
TDC=14A
Ipeak=20A
OCP=24A
Switching Frequency: 400kHz
                           TYP      MAX
H/S Rds(on): 5.2mohm , 7.0mohm
L/S Rds(on): 0.8mohm , 1.05mohm

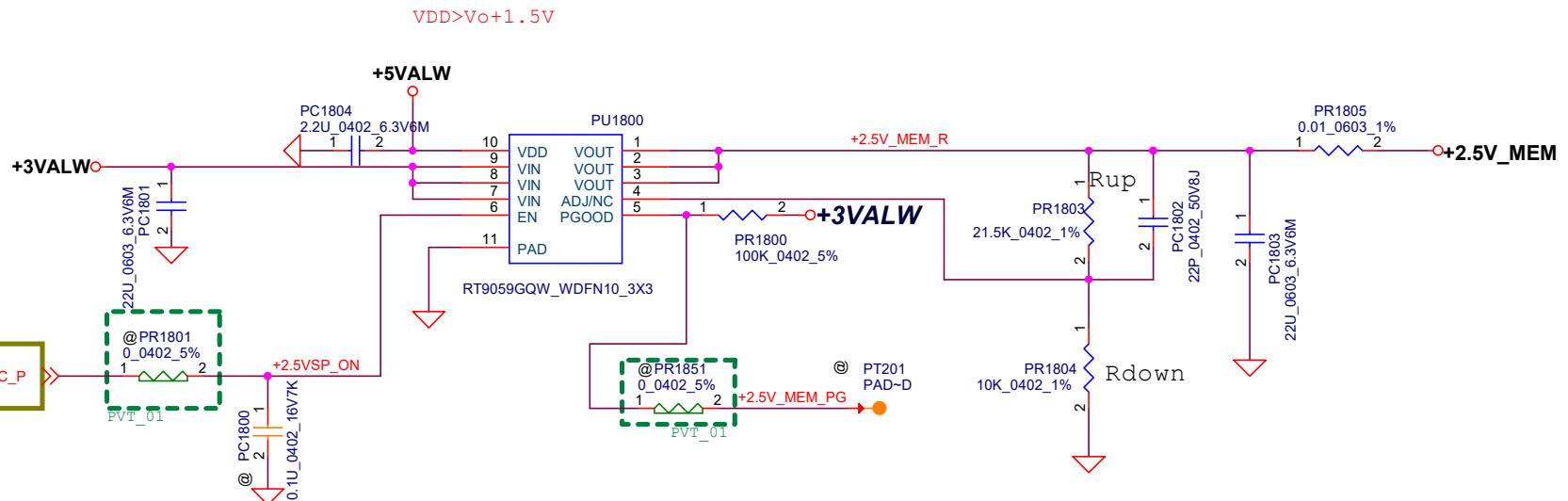
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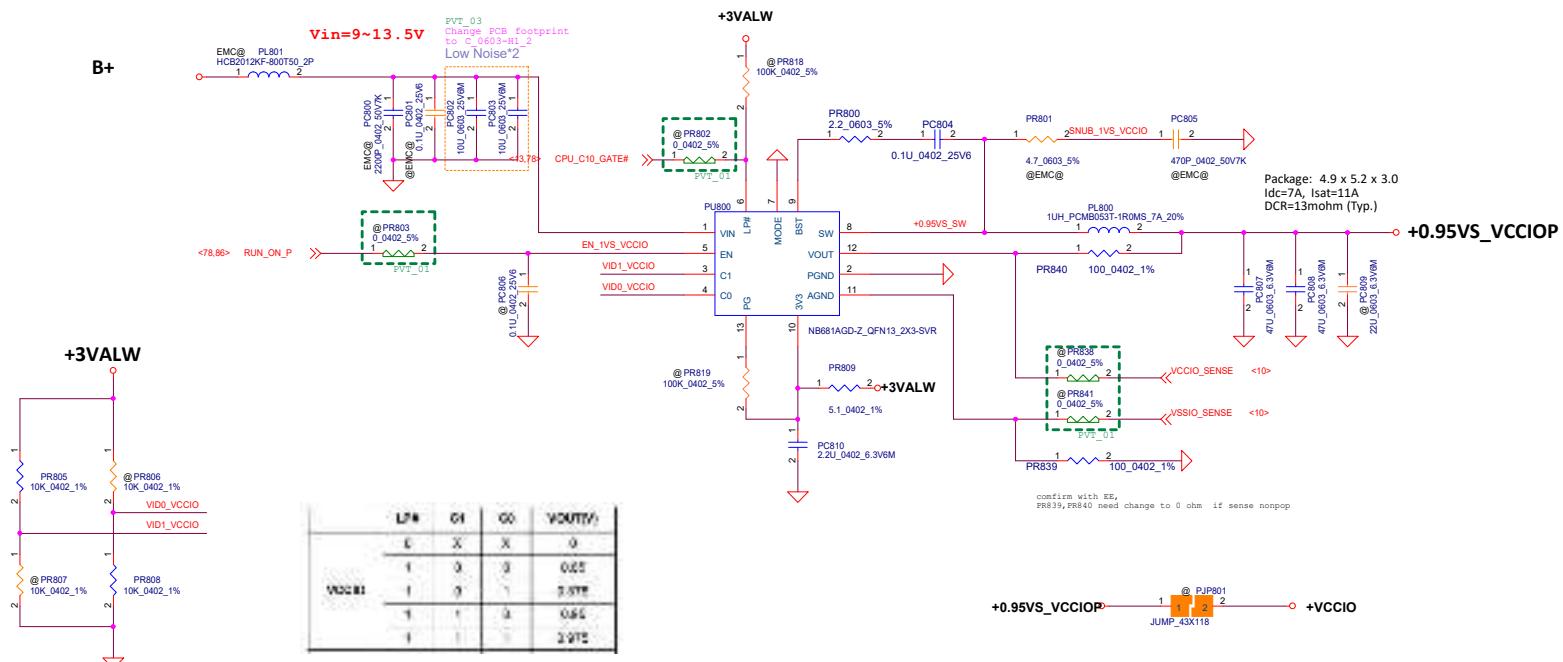
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2.5V_MEM controller(35.11), Support component(35.12)

+2.5V_MEM
TDC 1.6A
Peak Current 1.6A
OCP Current 3A



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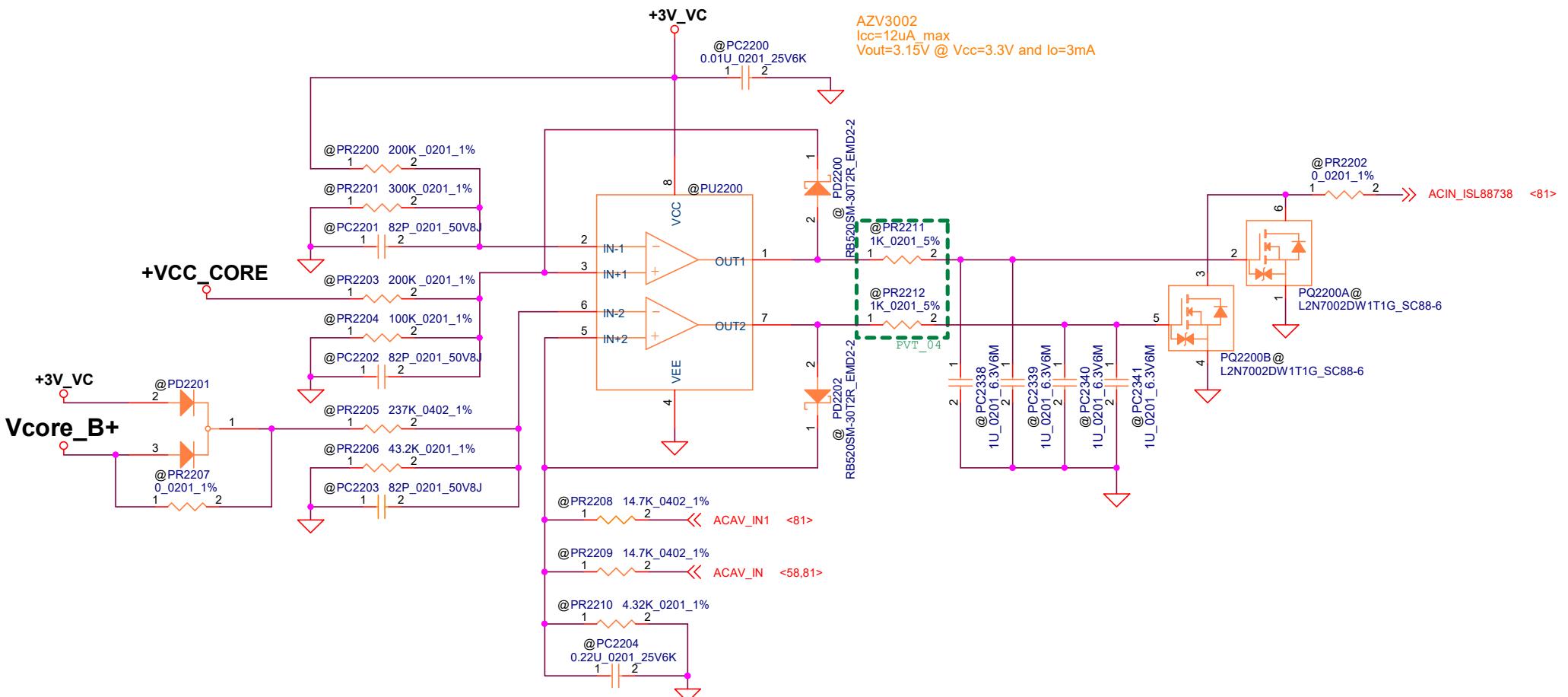


+0.95VS_VCCIOP
TDC 4.5A
Peak Current 6.5A
OCP Current 7.65A Fix by IC
TYP MAX

	L7N	O1	O2	VOUT(V)
VOCBI	0	X	X	0
	1	0	0	0.65
	1	0	1	2.97E-05
	1	1	0	0.65
	1	1	1	2.97E-05

PWR Plane Regulator VCCIO(35.37), Support component(35.38)

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