

# Compal Confidential

## FH5VF

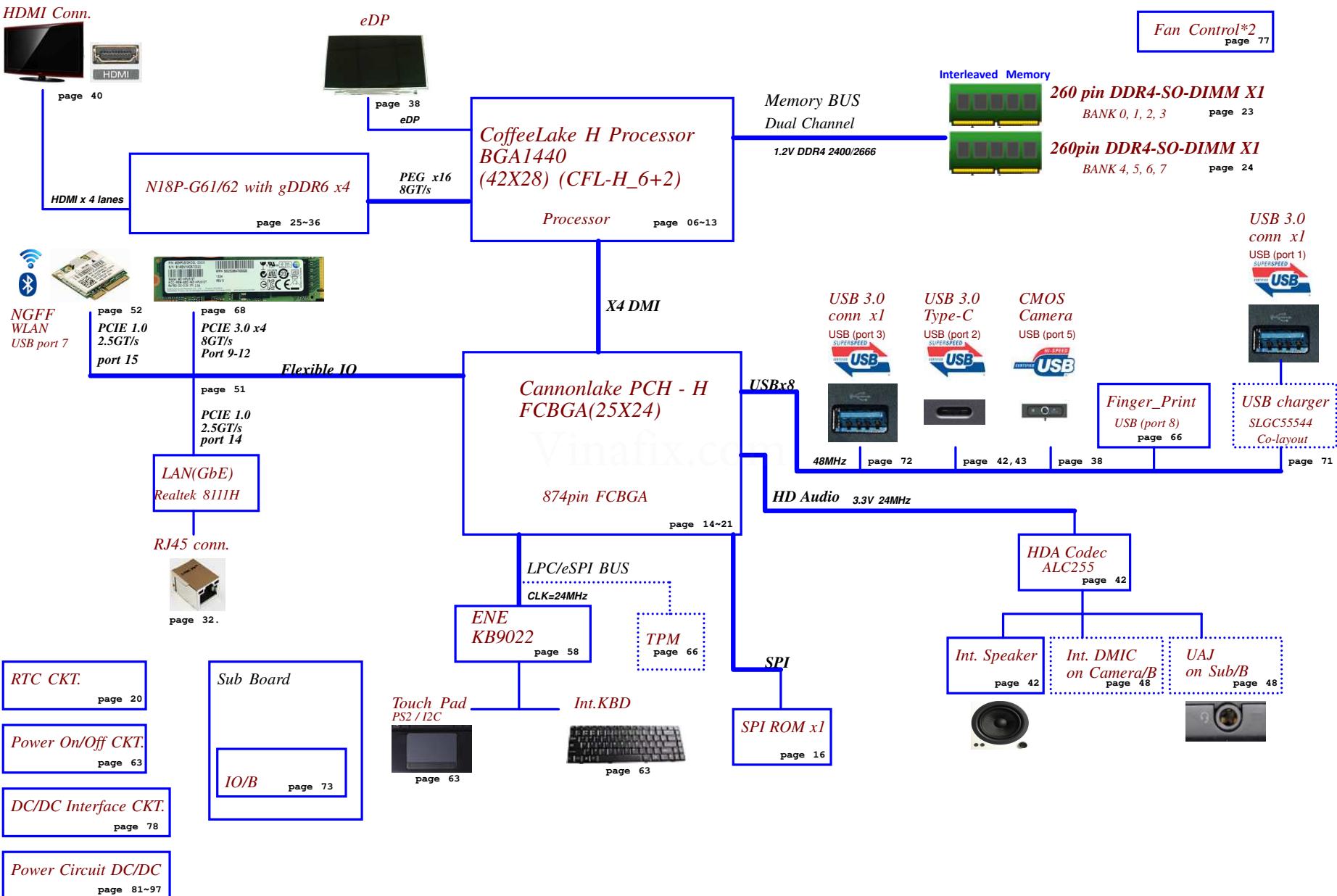
### MB Schematic Document

#### LA-J861P

Rev:1A

2020.02.05

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Issued Date	2017/10/30	Deciphered Date	2018/10/30	Title	<i>Cover Sheet</i>
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2017/07/20	2018/07/20			
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## Board ID Table for AD channel

Vcc	3.3V	+/- 5%							
Ra	100K	+/- 1%							
Board ID	Rb	V <sub>BID</sub>	min	V <sub>BID</sub>	typ	V <sub>BID</sub>	max	EC	AD
0	0			0.000	V	0.300	V	0x00	- 0x1F
1	12K	+/- 1%	0.347	V	0.345	V	0.360	V	0x14 - 0x1E
2	15K	+/- 1%	0.423	V	0.430	V	0.438	V	0x1F - 0x22
3	20K	+/- 1%	0.541	V	0.550	V	0.559	V	0x26 - 0x30
4	27K	+/- 1%	0.691	V	0.702	V	0.713	V	0x31 - 0x37
5	33K	+/- 1%	0.807	V	0.819	V	0.831	V	0x3B - 0x45
6	43K	+/- 1%	0.978	V	0.992	V	1.006	V	0x46 - 0x5A
7	56K	+/- 1%	1.169	V	1.185	V	1.200	V	0x55 - 0x64
8	75K	+/- 1%	1.398	V	1.414	V	1.430	V	0x65 - 0x70
9	100K	+/- 1%	1.634	V	1.650	V	1.667	V	0x77 - 0x87
10	130K	+/- 1%	1.849	V	1.865	V	1.881	V	0x88 - 0x96
11	160K	+/- 1%	2.015	V	2.031	V	2.046	V	0x97 - 0xA4
12	200K	+/- 1%	2.185	V	2.200	V	2.215	V	0xA5 - 0xAB
13	240K	+/- 1%	2.316	V	2.329	V	2.343	V	0xB0 - 0xB7
14	270K	+/- 1%	2.395	V	2.408	V	2.421	V	0xBB8 - 0xBBF
15	330K	+/- 1%	2.521	V	2.533	V	2.544	V	0xC0 - 0xC5
16	430K	+/- 1%	2.667	V	2.677	V	2.687	V	0xCA - 0xD0
17	560K	+/- 1%	2.791	V	2.800	V	2.808	V	0xD5 - 0xDD0
18	750K	+/- 1%	2.905	V	2.912	V	2.919	V	0xDE - 0xFFE
19	NC		3.000	V	3.000	V			0xF1 - 0xFF

## I2C Address Table

BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)				
I2C_1 (+3VS)	TM-P3393-003 (Touch Pad)			
	SA577C-12A0 (Touch Pad)			
PCH_SMBCLK (+3VS)	DIMM1			
	DIMM2			
PCH_SML1CLK EC_SMB_CK2 (+3VS)	N18P-G0/N17P-G0-K1 (VGA)	0x9E		
	Thermal Sensor (NCT7718W)	1001_100xb	1001_1001b	1001_1000b
	PCH	0x90		
	Thermal Sensor (G781-1P8F)	1001_101xb	1001_1011b	1001_1010b
EC_SMB_CK1 (+3VLP)	BQ24781 (Charger IC)	0x12		
	BATTERY PACK	0x16		

## 43 level BOM table

## BOM Structure Table

## BOM Option Table

BOM Option Table		
Item	BOM	Structure
Unpop	@	
Connector	CONN@	
CMC	CMC@	
dGPU circuit	VGA@	
N18P GPU	N18P@	
VRAM	X76@	
OVRM-ON	ON_X76@	
OVRM-uPI	uPI_X76@	
TPM	TPM@	
For Acer IOAC	IOAC@	
No Acer IOAC	NIOAC@	
Thermal sensor	TMS@	
for UART BT module	UBT@	
for SW debug board	UART@	
Intel CNVi	CNVI@	
Finger Print	FP@	
FinerPrint(with PBA)	PBA@	
LAN LDO mode	LDO@	
LAN Switch mode	SWR@	
EMI requirement	EMI@	
EMI require reserve	XEMI@	
ESD requirement	ESD@	
ESD require reserve	XESD@	
FP ESD requirement	FPESD@	
H62 CPU	H62@	
H82 CPU	H82@	

## Power State

<i>STATE</i>	<i>SIGNAL</i>			<i>SLP_S3#</i>	<i>SLP_S4#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>S0 (Full ON)</i>		<i>HIGH</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>		
<i>S3 (Suspend to RAM)</i>		<i>LOW</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>		
<i>S4 (Suspend to Disk)</i>		<i>LOW</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>		
<i>S5 (Soft OFF)</i>		<i>LOW</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>		

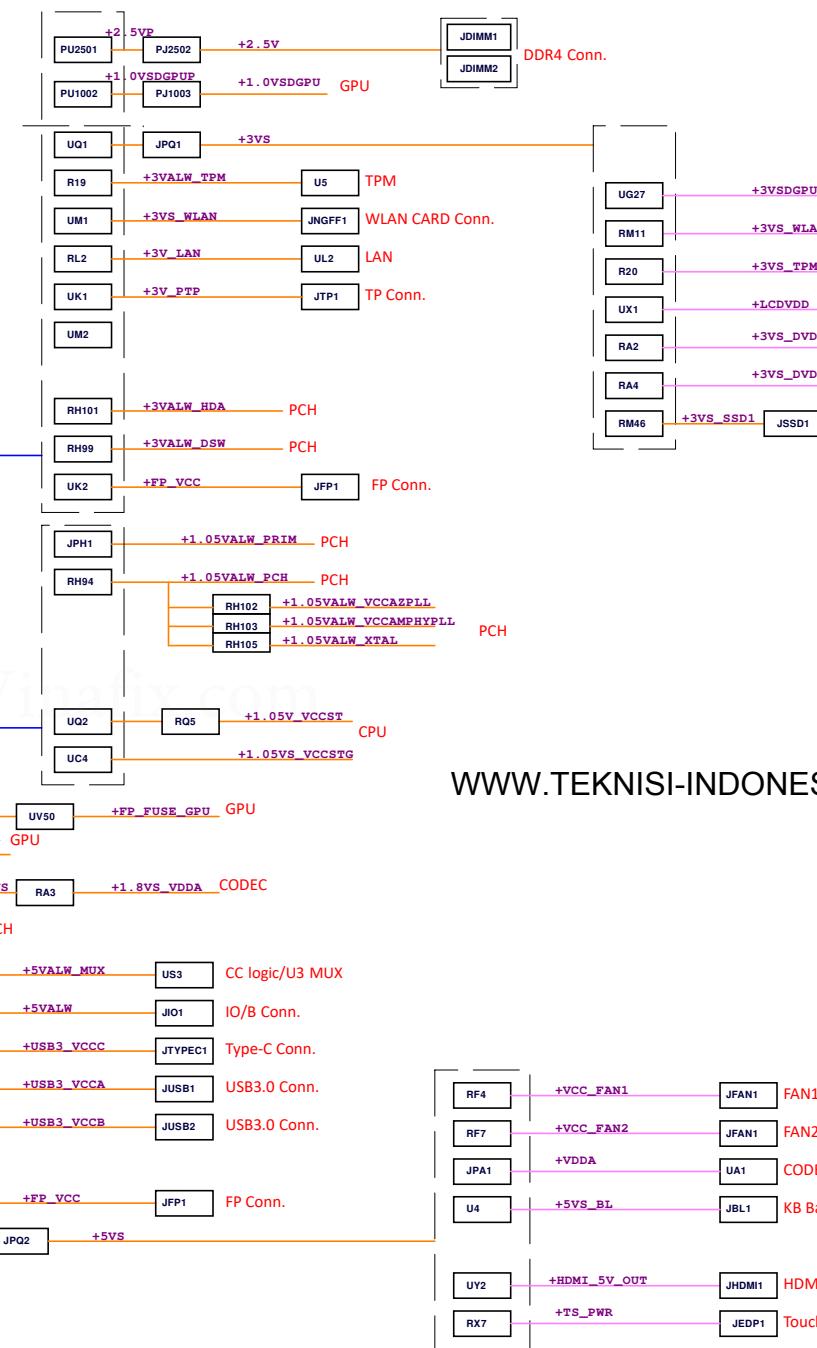
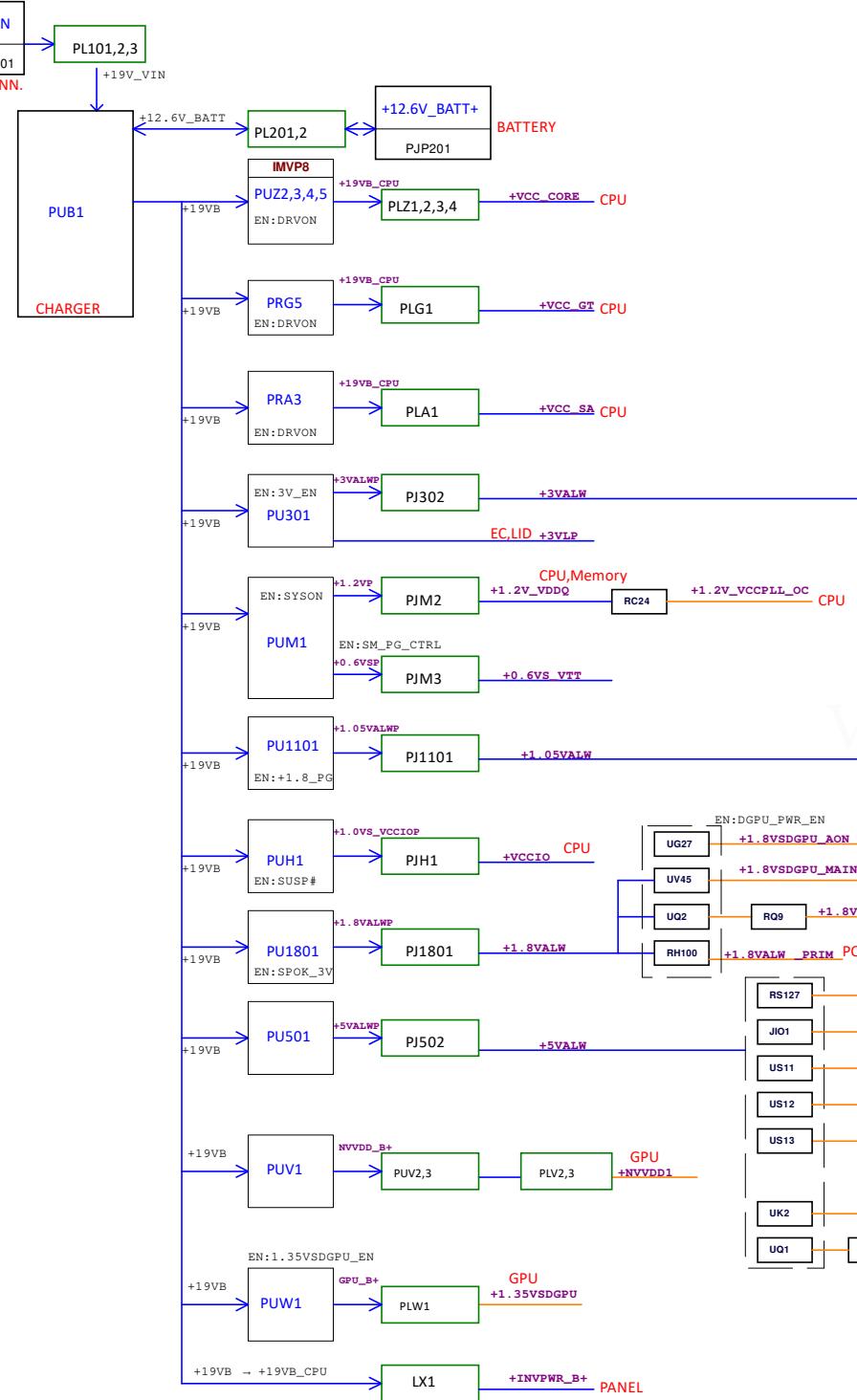
## Voltage Rails

Power Plane	Description	S0	S3	S4	S5
+RTC_VCC	RTC Battery Power	ON	ON	ON	ON
+19V_VIN	Adapter power supply	N/A	N/A	N/A	N/A
+12.6V_BATT	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A	N/A
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	ON
+5VALW	+5V Always power rail	ON	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON	ON*
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON	ON
+1.05VALW	+1.05V Always power rail	ON	ON	ON	ON
+1.2V_VDDO	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+1.05V_VCCST	Sustain voltage for processor in Standby modes	ON	ON	OFF	OFF
+5VS	System +5V power rail	ON	OFF	OFF	OFF
+3VS	System +3V power rail	ON	OFF	OFF	OFF
+1.05VS_VCCSTG	+1.05VALW_PRIM Gated version of VCCST	ON	OFF	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF	OFF
+VCC_GT	Sliced graphics power rail	ON	OFF	OFF	OFF
+VCCIO	CPU IO +0.95VS power rail	ON	OFF	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF	OFF
+1.8VSDGPU_AON	+1.8VS power rail for GPU(AON rails)	ON	OFF	OFF	OFF
+1.8VSDGPU_MAIN	+1.8VS power rail for GPU GC6	ON	OFF	OFF	OFF
+NVVDD1	Core voltage for VGA (merge core & core_s)	ON	OFF	OFF	OFF
+1.35VSDGPU	+1.35VS power rail for GPU	ON	OFF	OFF	OFF
+1.0VSDGPU	+1.0VS power rail for GPU	ON	OFF	OFF	OFF
+1.8VALW	System +1.8VALW always on power rail	ON	ON	ON	ON*

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## BOARD ID Table

Board ID	PCB Revision	Board ID	PCB Revision
0	Rev0.1	10	
1		11	
2		12	
3		13	
4		14	
5		15	
6		16	
7		17	
8		18	A7 Rev1A
9		19	A7 Rev1.0



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BIOS : 0.03

AC mode

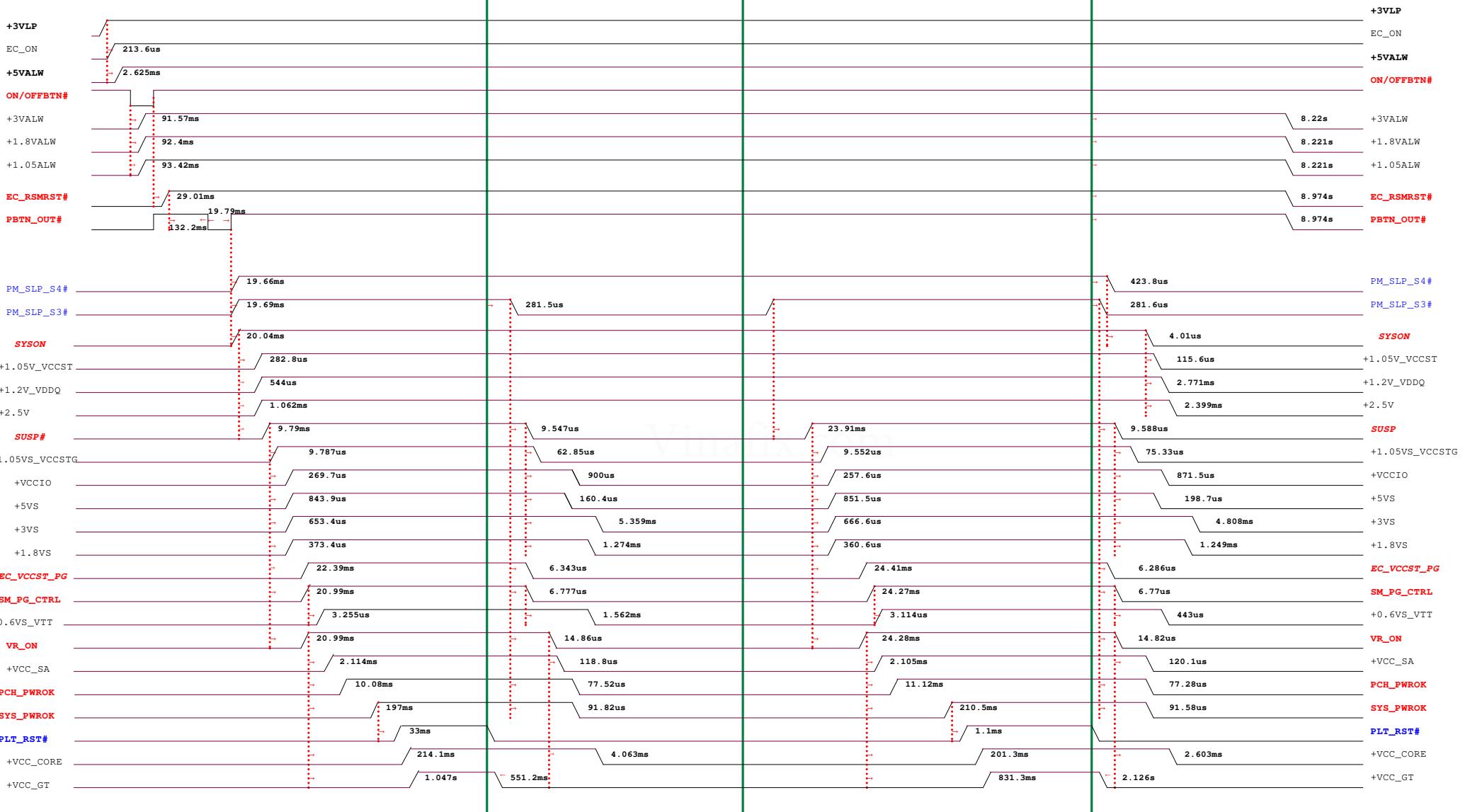
Plug in

Power On

S3

S3 Resume

Power Off



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ZZZ  
PCB@

PCB FH5VF LA-J861P LS-J812P  
DAZZY100200

### Coffee Lake-H CPU SKU

UC1  
15@  
S IC CL8068403373522 SR3Z0 U0 2.3G ABO!  
**SA0000BPJ40**  
UC1  
17@  
S IC CL8068403359524 SR3YY U0 2.2G ABO!  
**SA0000BPZ40**

### Re-fresh U0 stepping

UC1  
15RU0@  
S IC CL8068404121905 SRF6X U0 2.4G ABO!  
**SA0000COG40**  
UC1  
17RU0@  
S IC CL8068404121817 SRF6U U0 2.6G ABO!  
**SA0000COF30**

### Re-fresh R0 stepping

UC1  
15RR0@  
S IC CL8068404069606 SRFCR R0 2.4G ABO!  
**SA0000CSZ10**  
UC1  
17RR0@  
S IC CL8068404069418 SRFCP R0 2.6G ABO!  
**SA0000CSU10**

### Comet Lake-H CPU SKU

UC1  
QU9W@  
S IC CL8070104399510 QU9W R1 2.5G FCBGA  
**SA0000DCP10**  
UC1  
QU9U@  
S IC CL8070104399315 QU9U R1 2.6G FCBGA  
**SA0000DCN10**

UC1  
SRH84@  
S IC CL8070104399510 SRH84 R1 2.5G ABO!  
**SA0000DCP40**  
UC1  
SRH8Q@  
S IC CL8070104399315 SRH8Q R1 2.6G ABO!  
**SA0000DCN40**

### Cannon Lake PCH SKU

UH1  
CFLPCH@  
S IC FH82HM370 SR40B B0 BGA 874P PCH-H ABO!  
**SA0000BVP10**

### Comet Lake PCH SKU

UH1  
CMLPCHQS@  
S IC FH82HM470 QUCJ A0 FCBGA 874P PCH-H  
**SA0000DDP10**  
UH1  
CMLPCH@  
S IC FH82HM470 SRJAU A0 FCBGA PCH-H ABO!  
**SA0000DDP80**

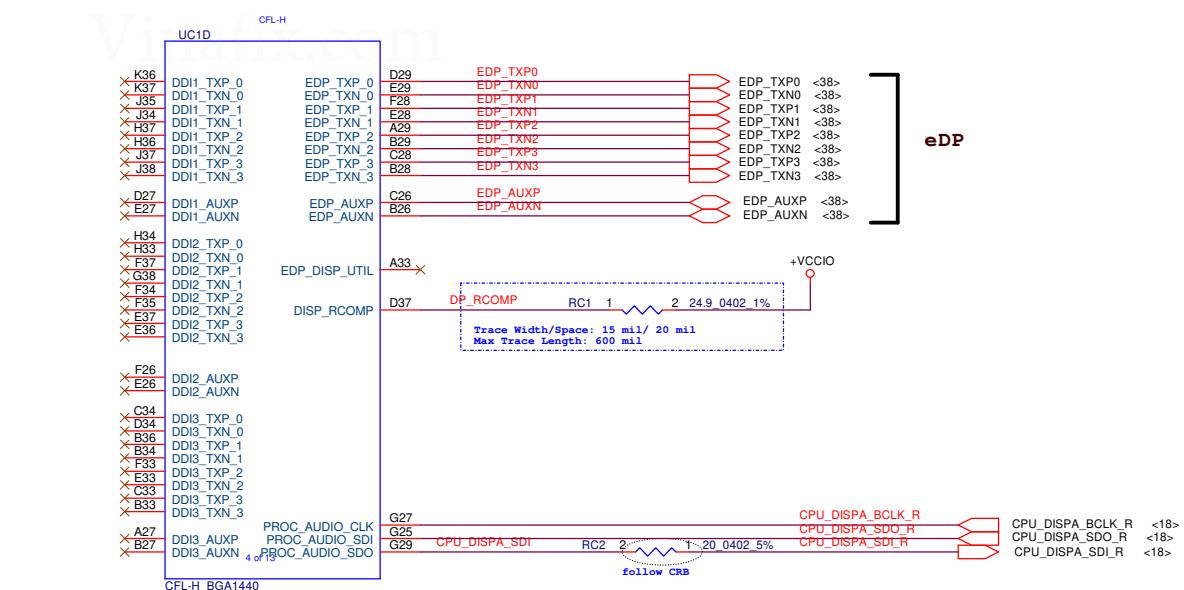
### NV GPU SKU

UV1  
N18PG61QS@  
S IC N18P-G61-A1 QS BGA 960P GPU ABO!  
**SA0000CZO10**

UV1  
N18PG61@  
S IC N18P-G61-MP-A1 BGA 960P GPU ABO!  
**SA0000CZO30**

UV1  
N18PG61MP2@  
S IC N18P-G61-MP2-A1 BGA 960P GPU ABO!  
**SA0000CZO50**

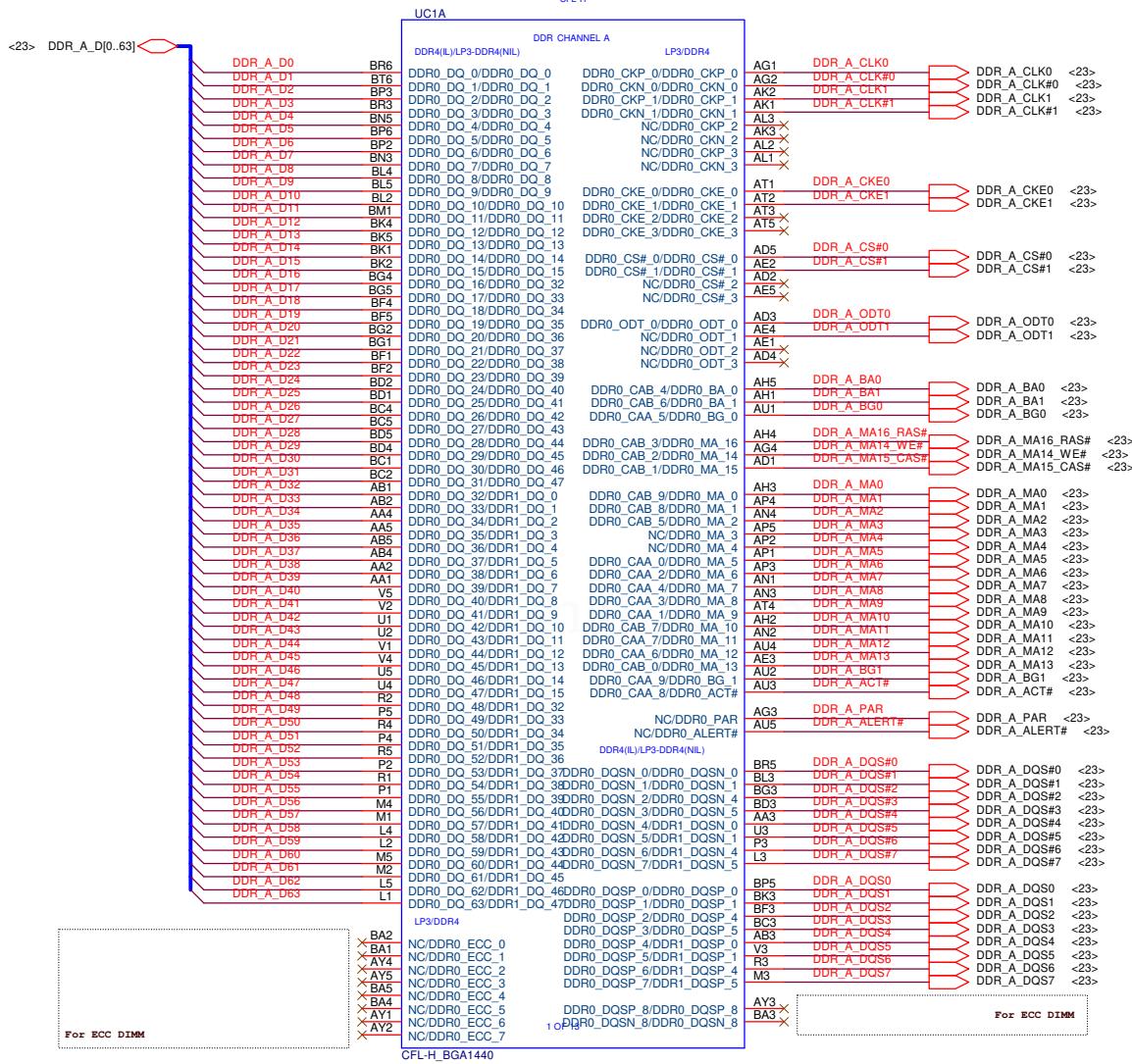
UV1  
N18PG62@  
S IC N18P-G62-A1 BGA 960P GPU ABO!  
**SA0000CZP30**



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# CHANNEL-A

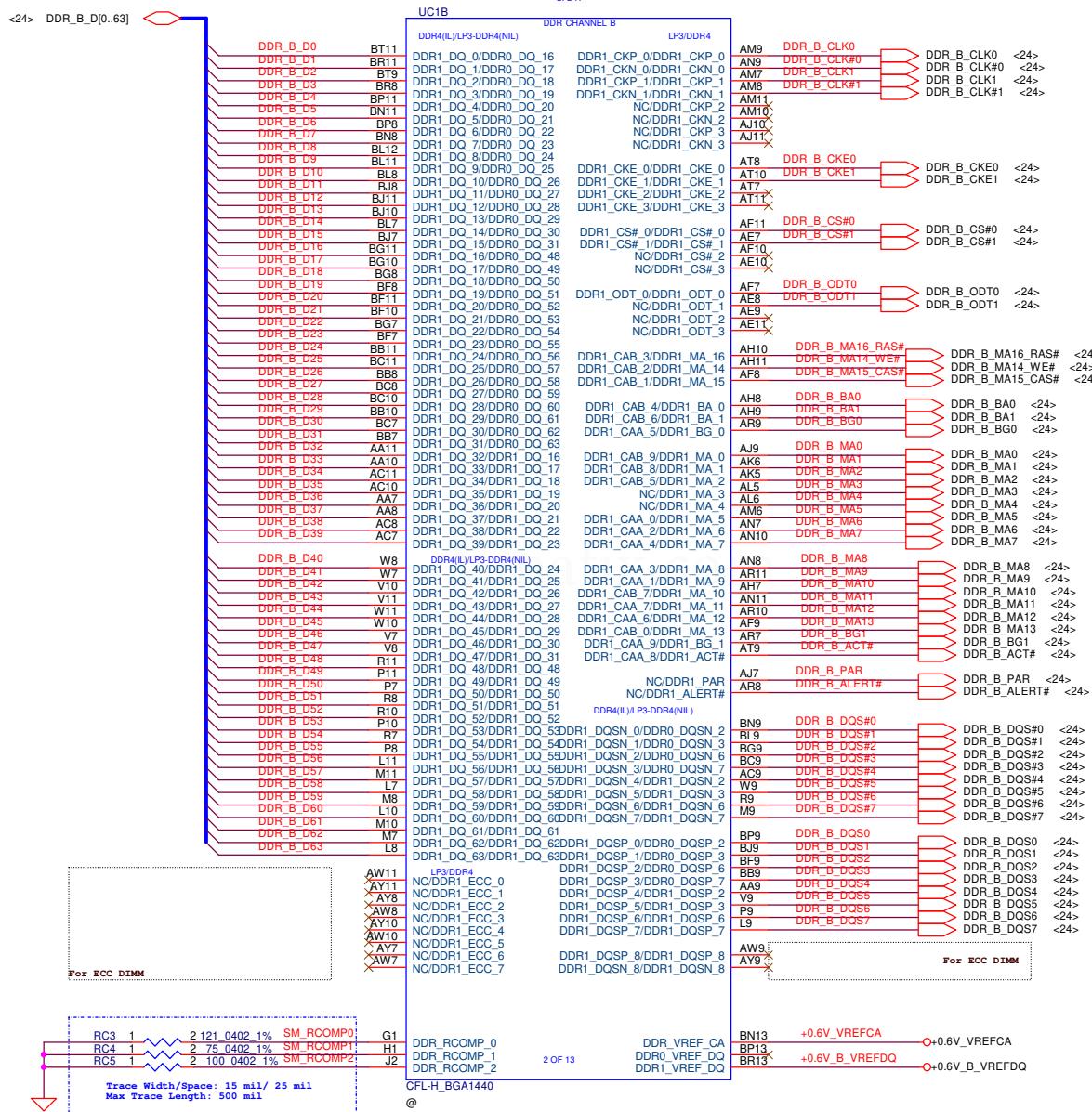
## Interleaved Memory



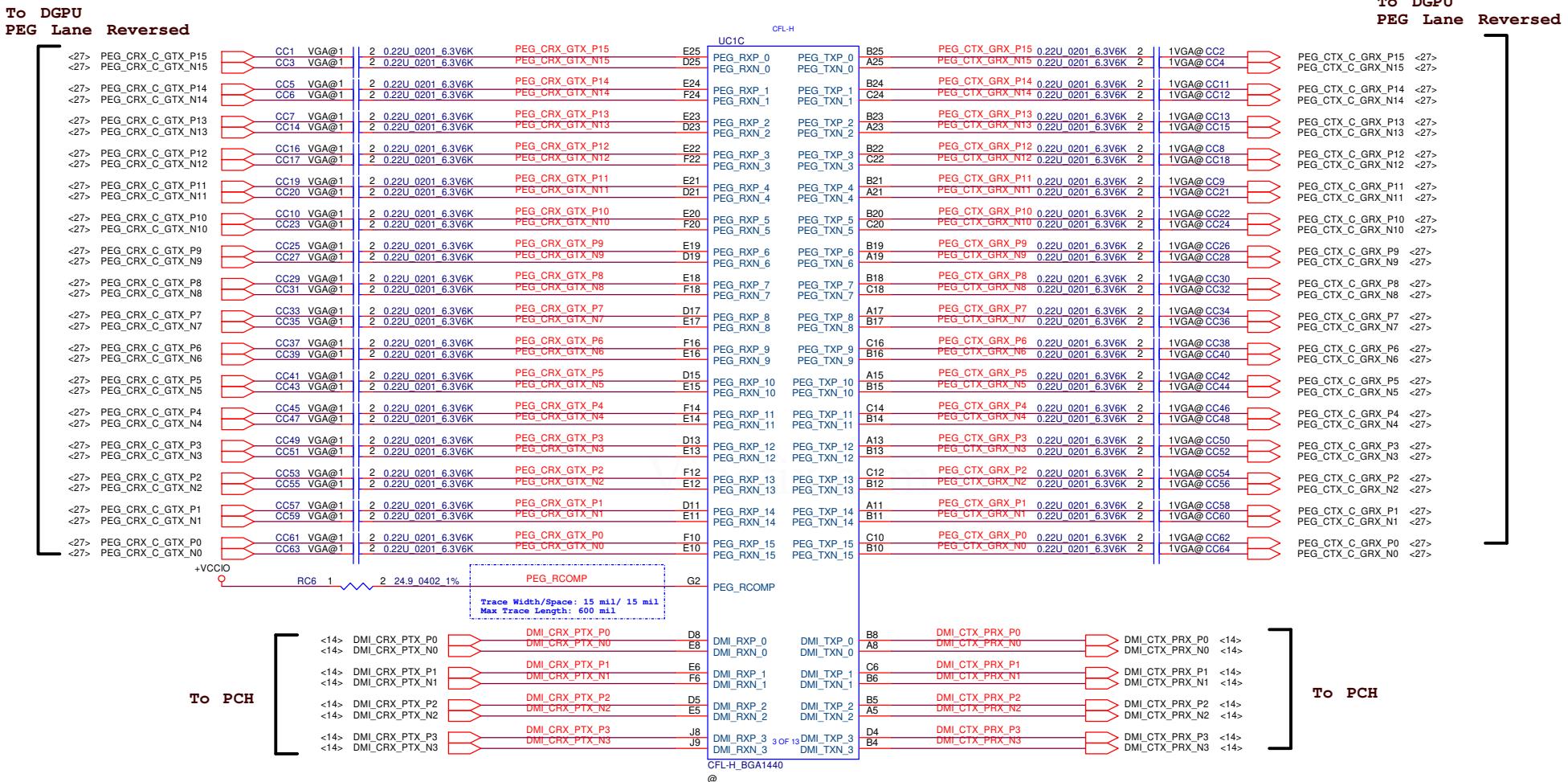
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# CHANNEL-B

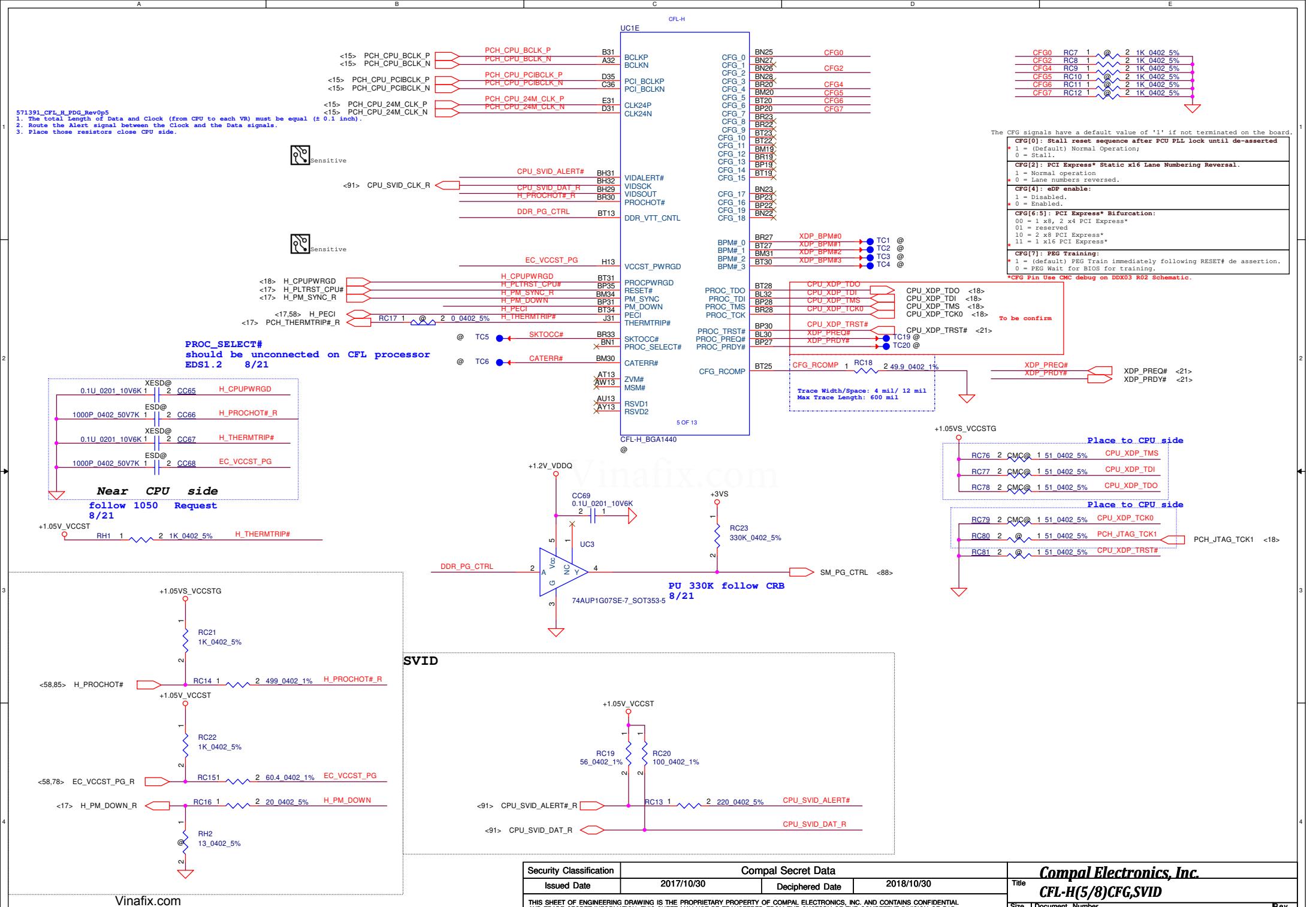
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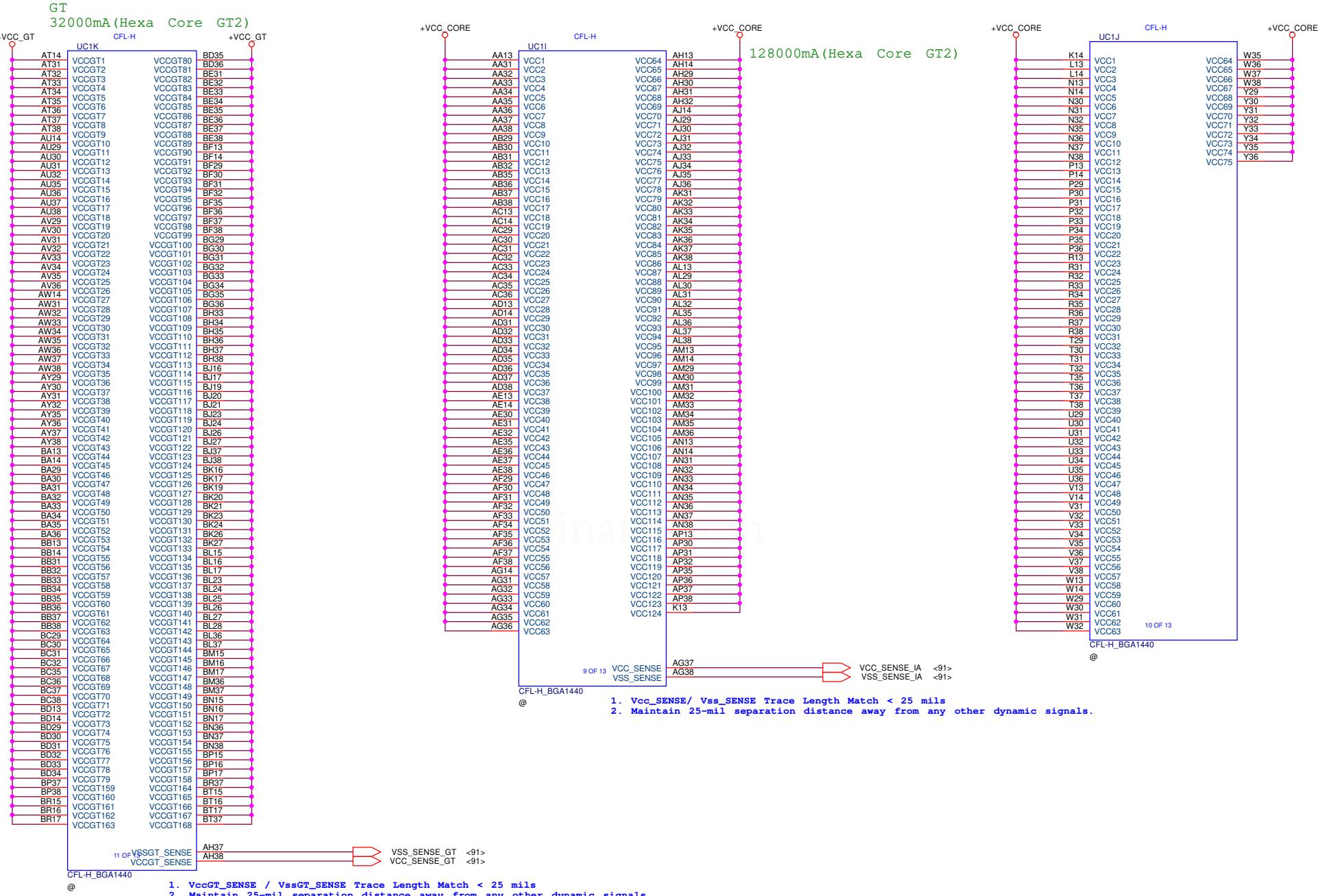


# PEG&DMI



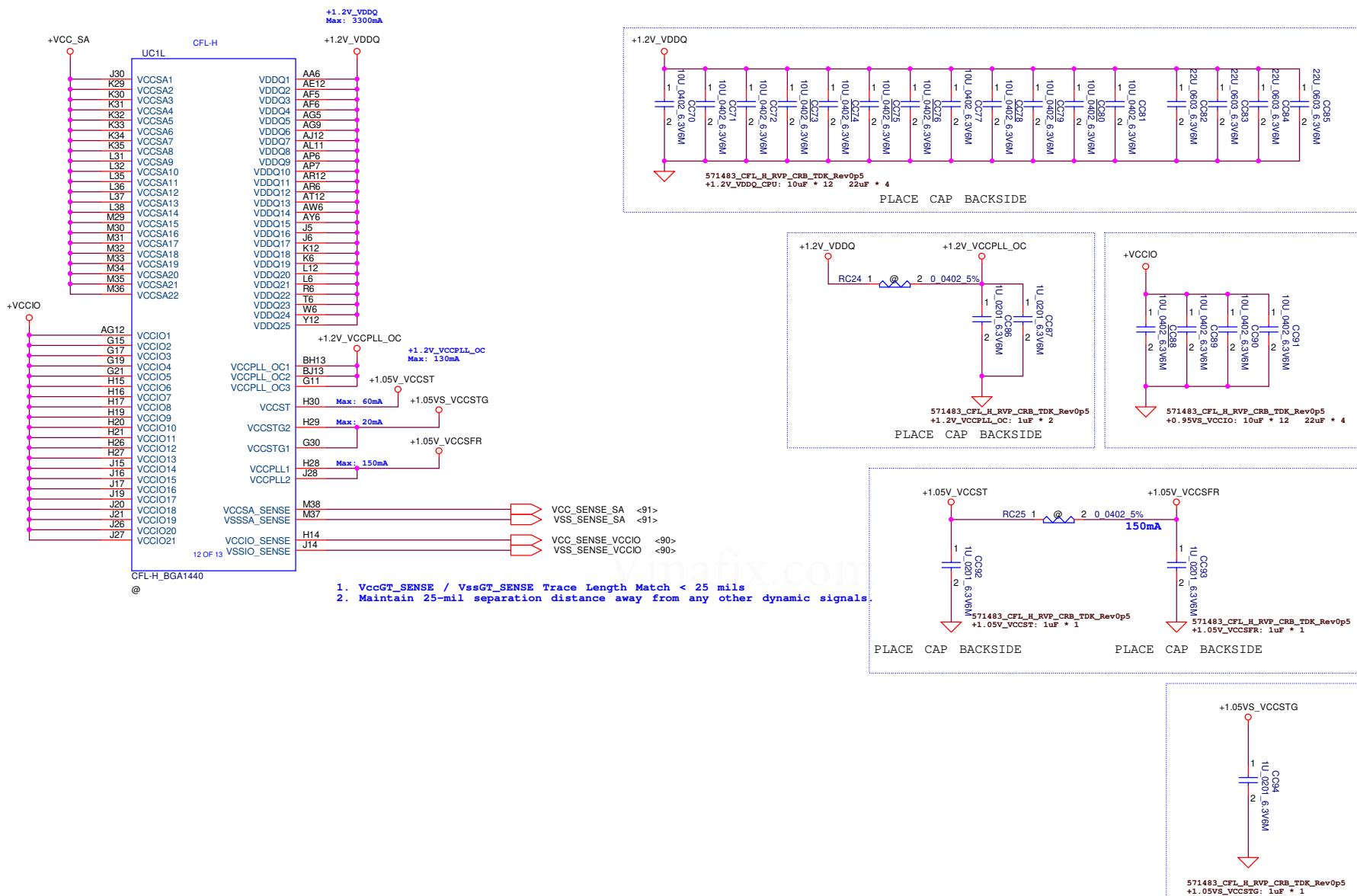
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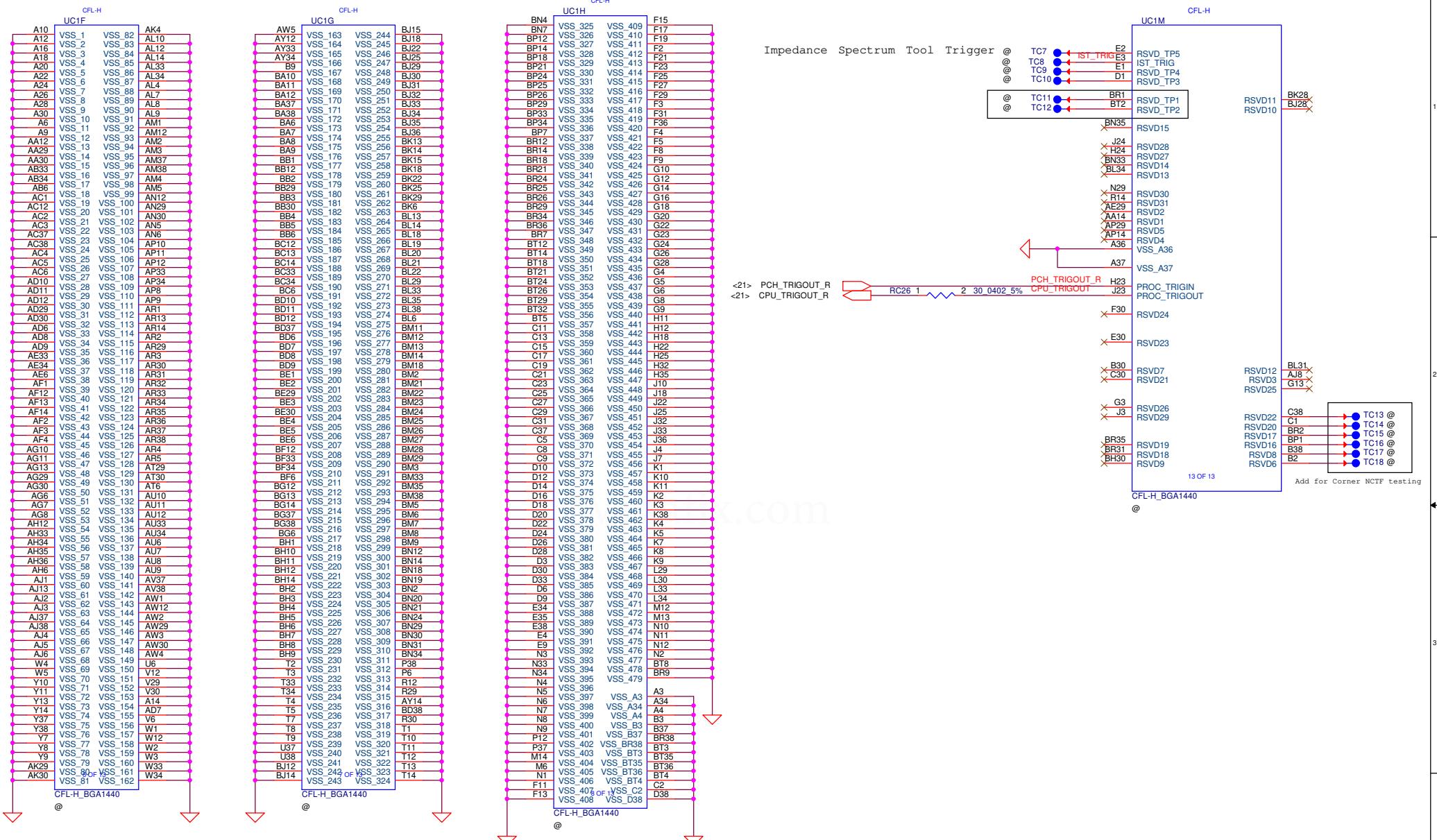


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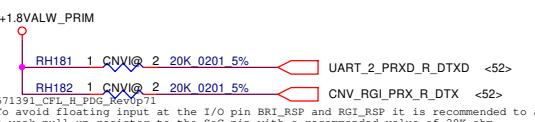
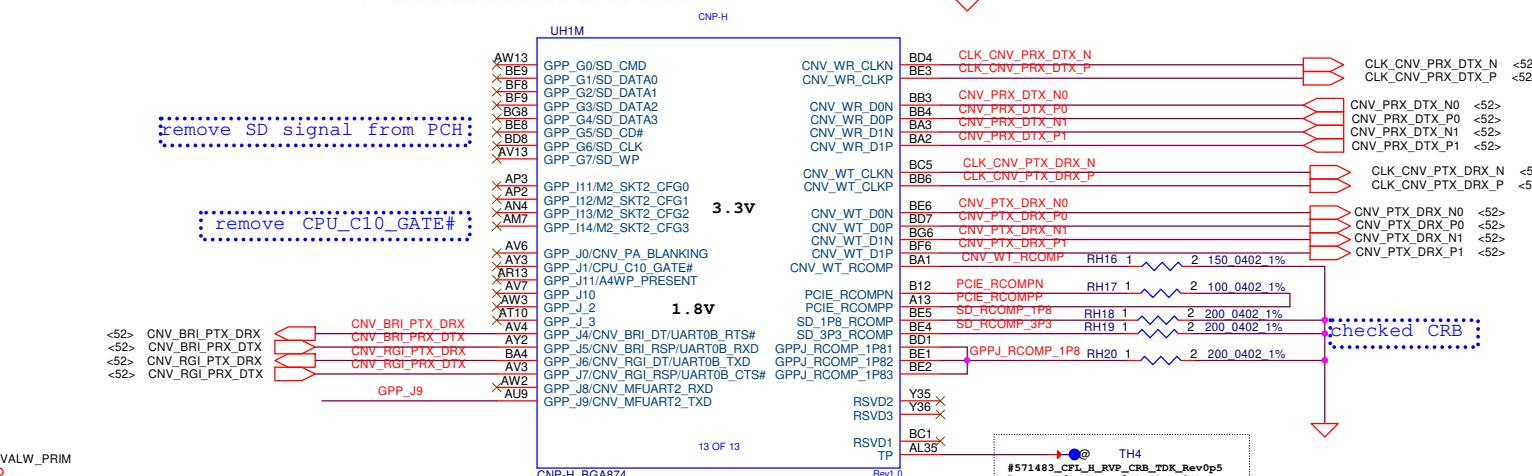
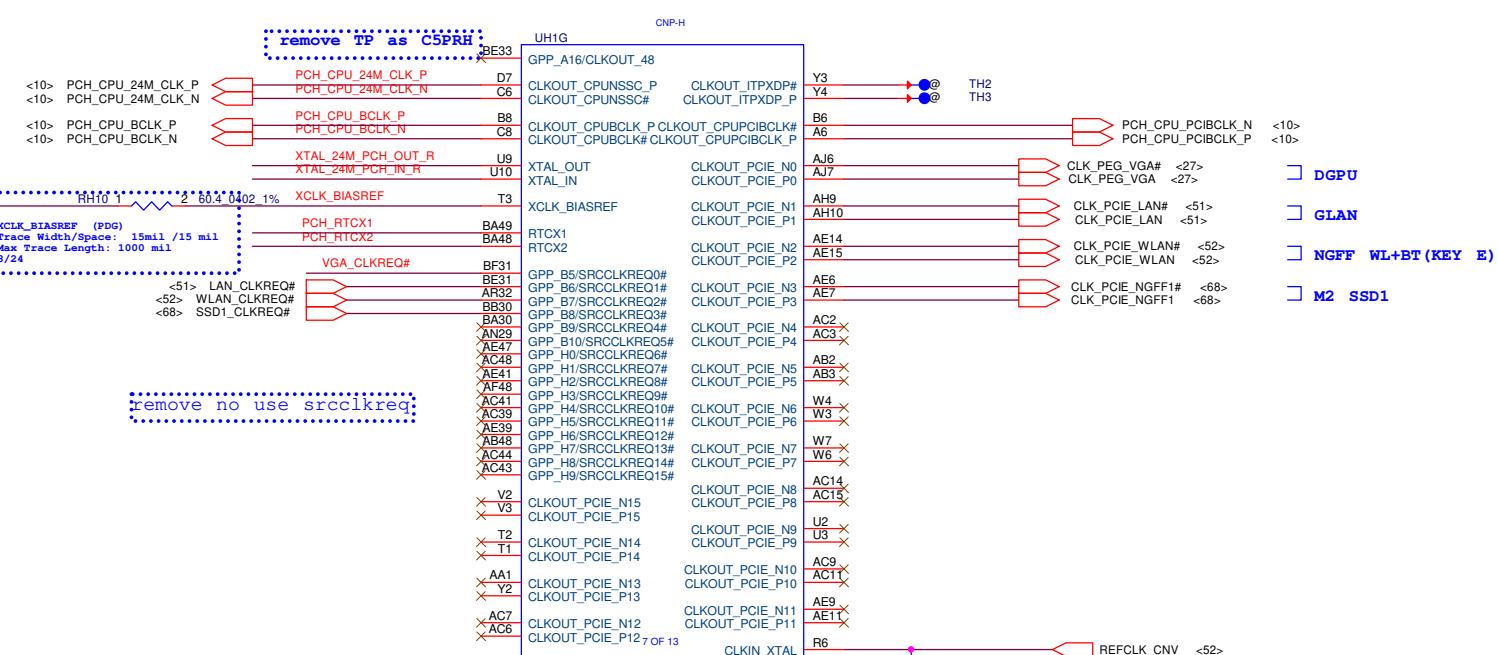
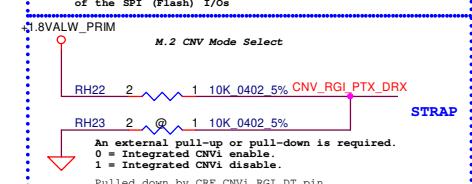
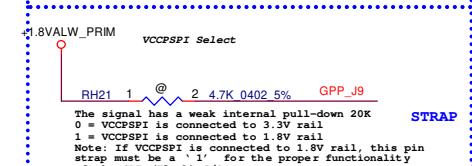
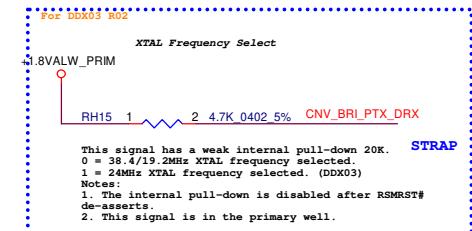
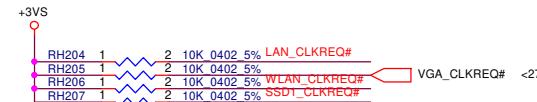
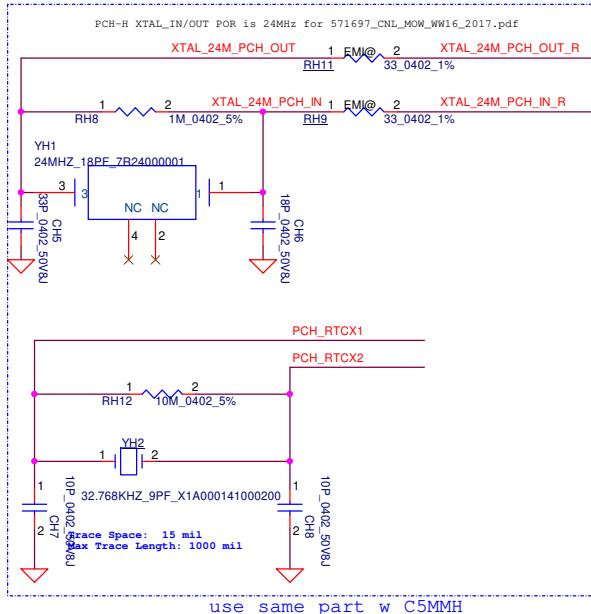
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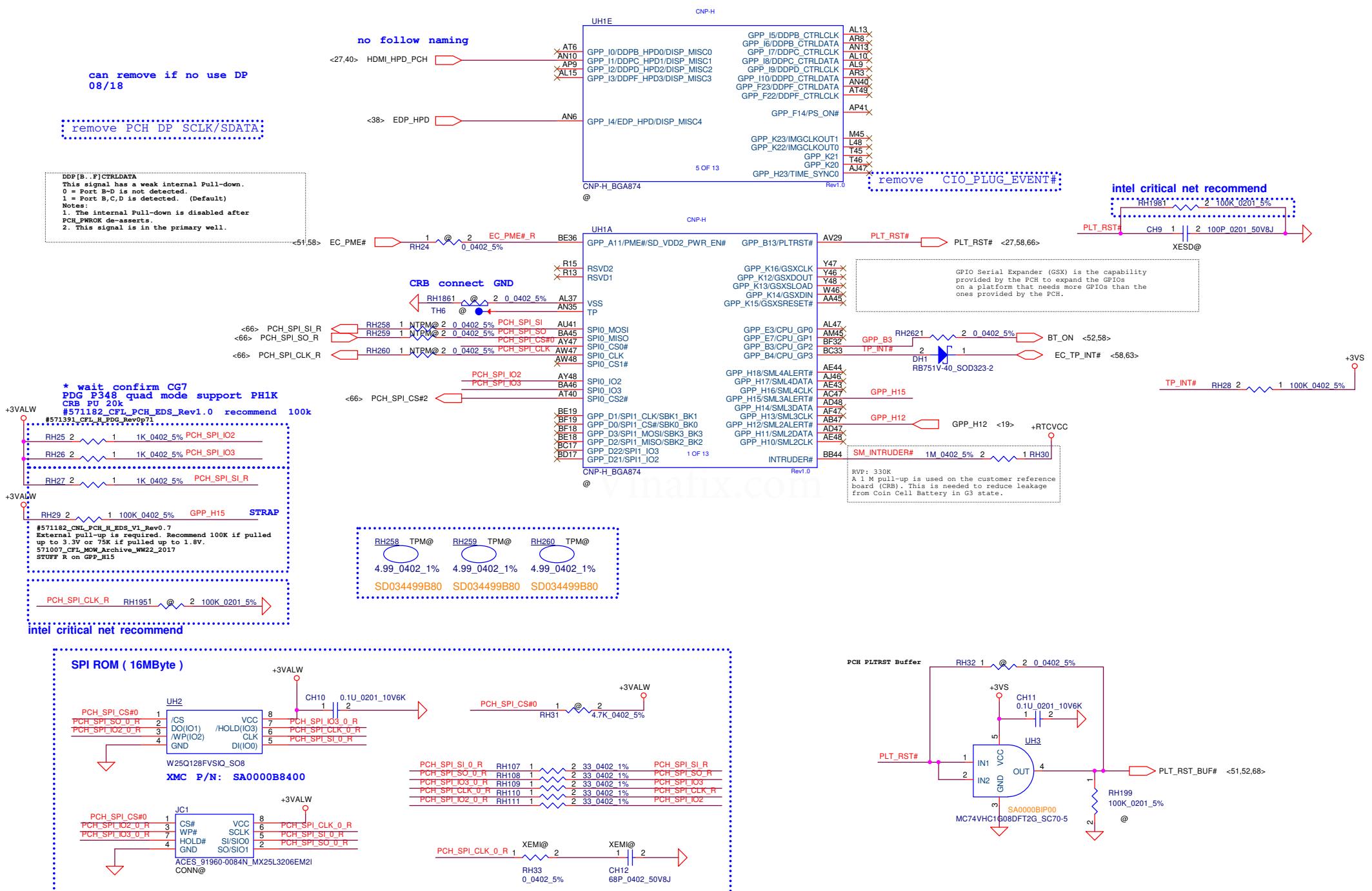




Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	PCIe* #24	
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	PCIe* #5	PCIe* #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16	PCIe* #17	PCIe* #18	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
Intel® RST Support	No Support	No Support	No Support	Yes	No Support	No Support	Yes	No Support	No Support	Yes	No Support																				

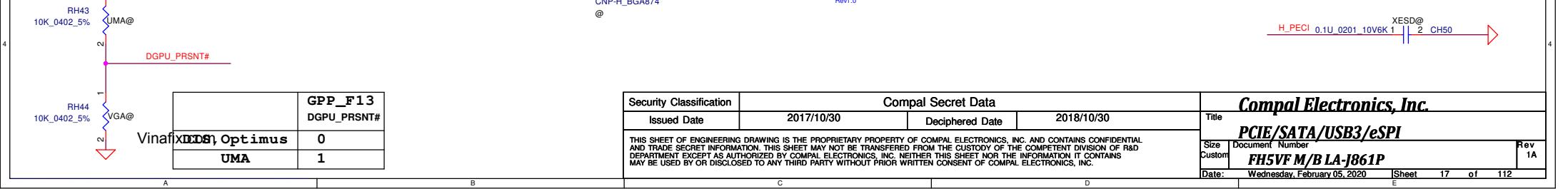
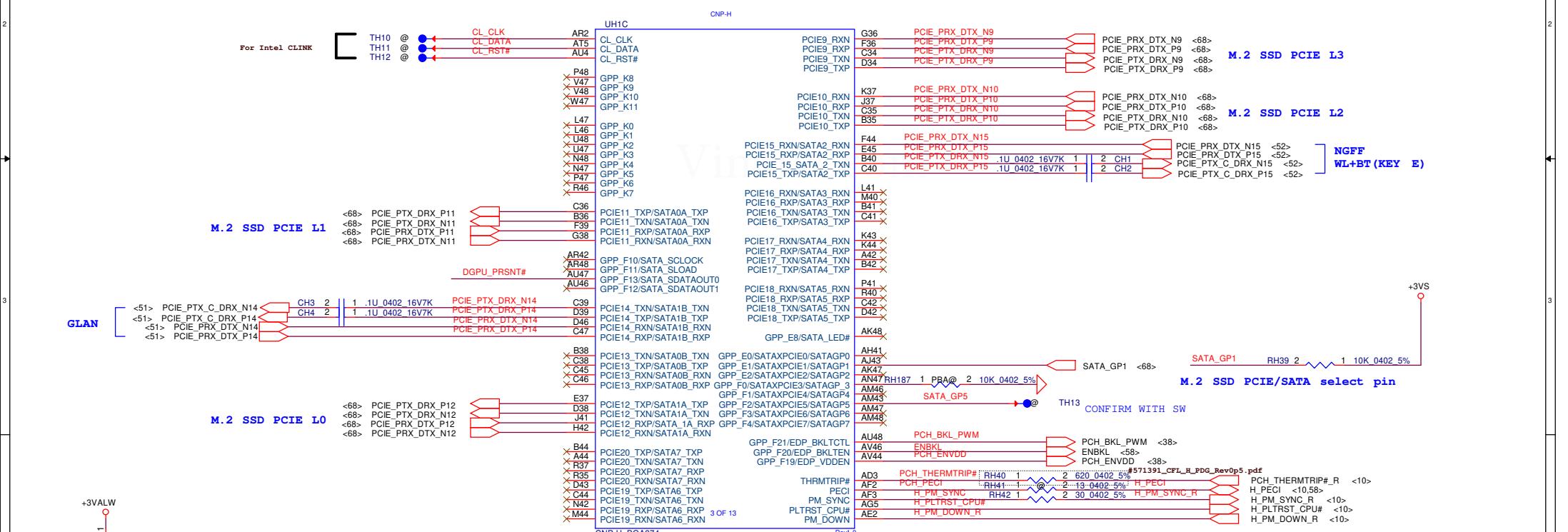
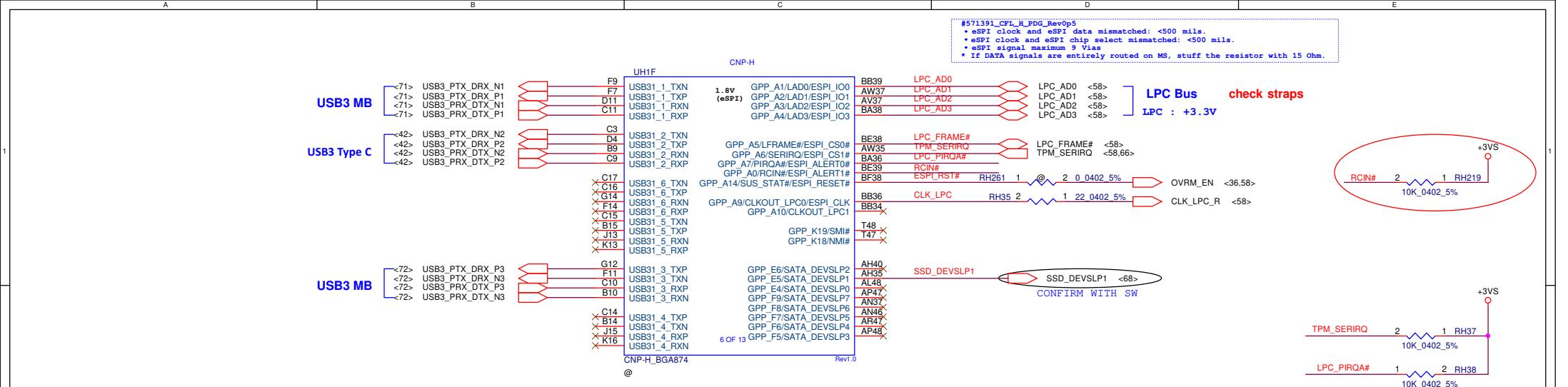
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PCH(1/8)DMI/PCIE/USB2				Size
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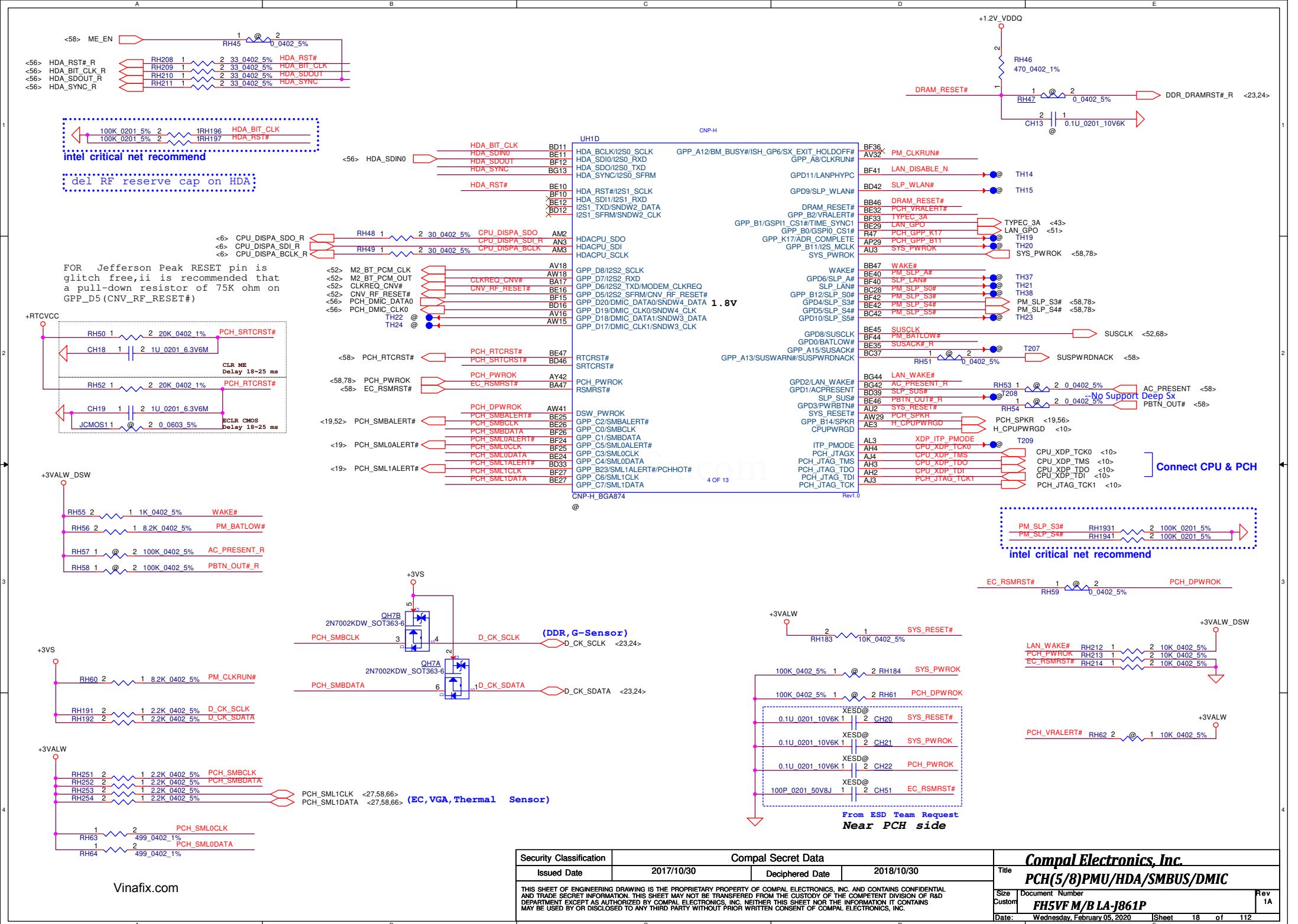


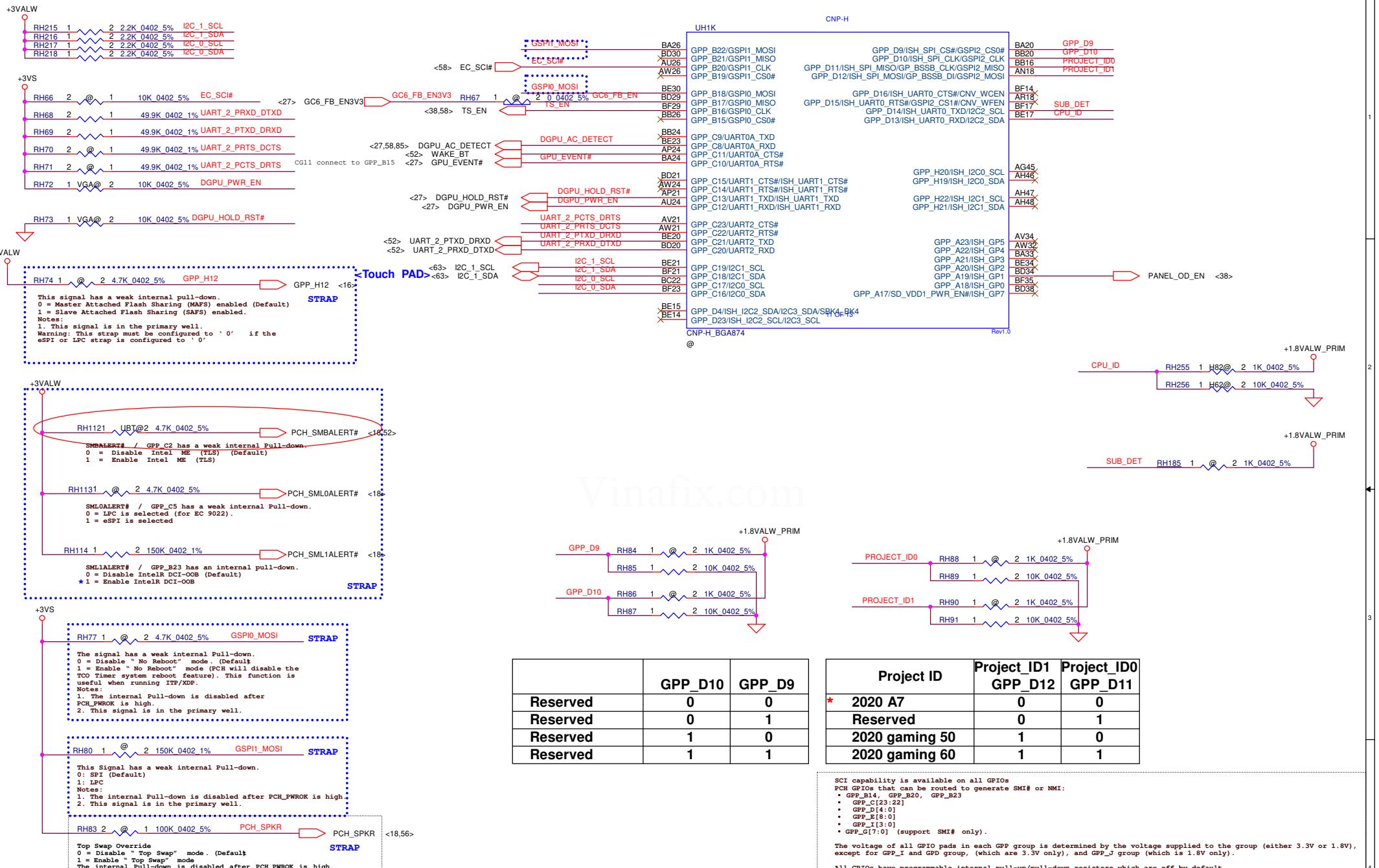


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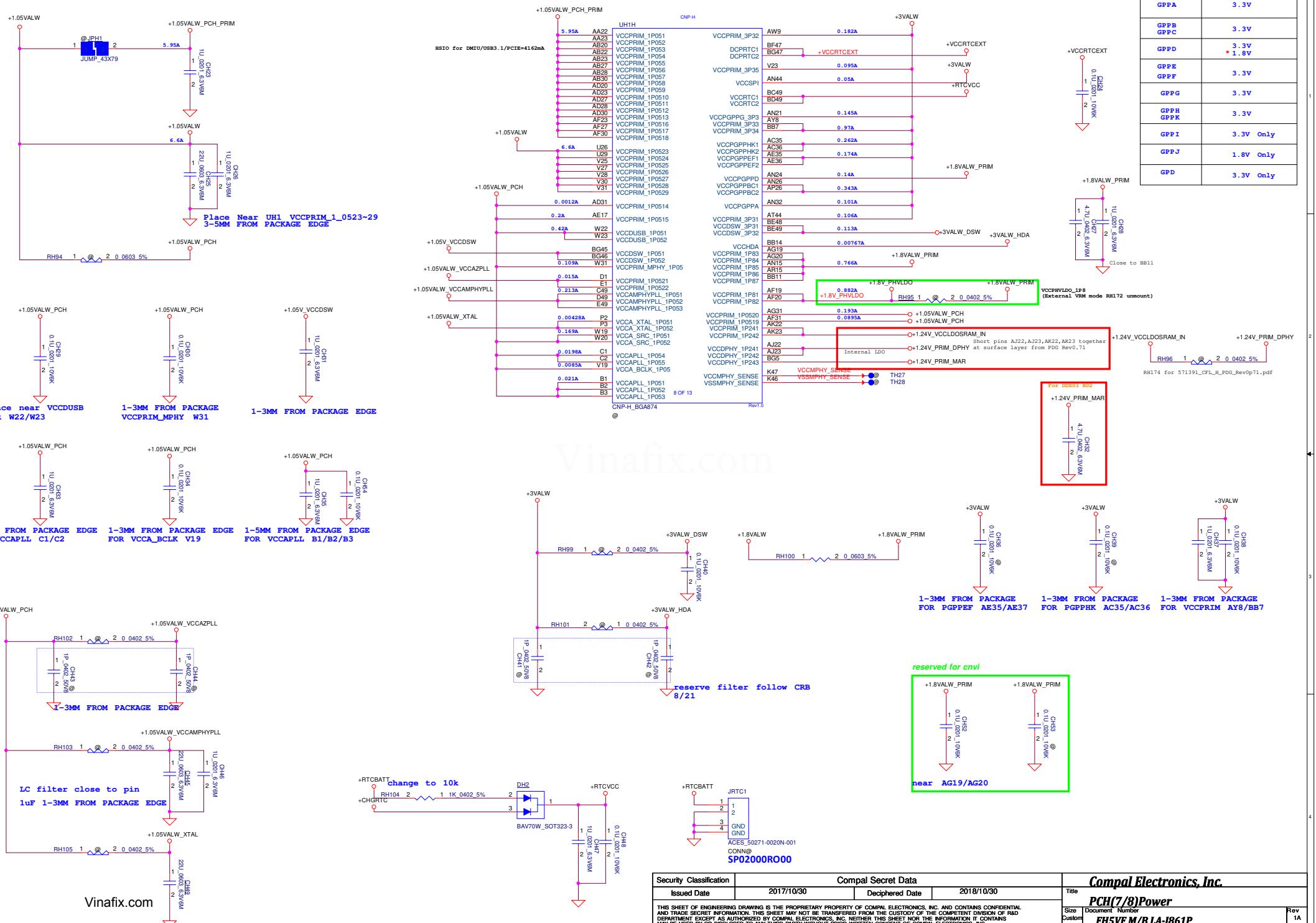
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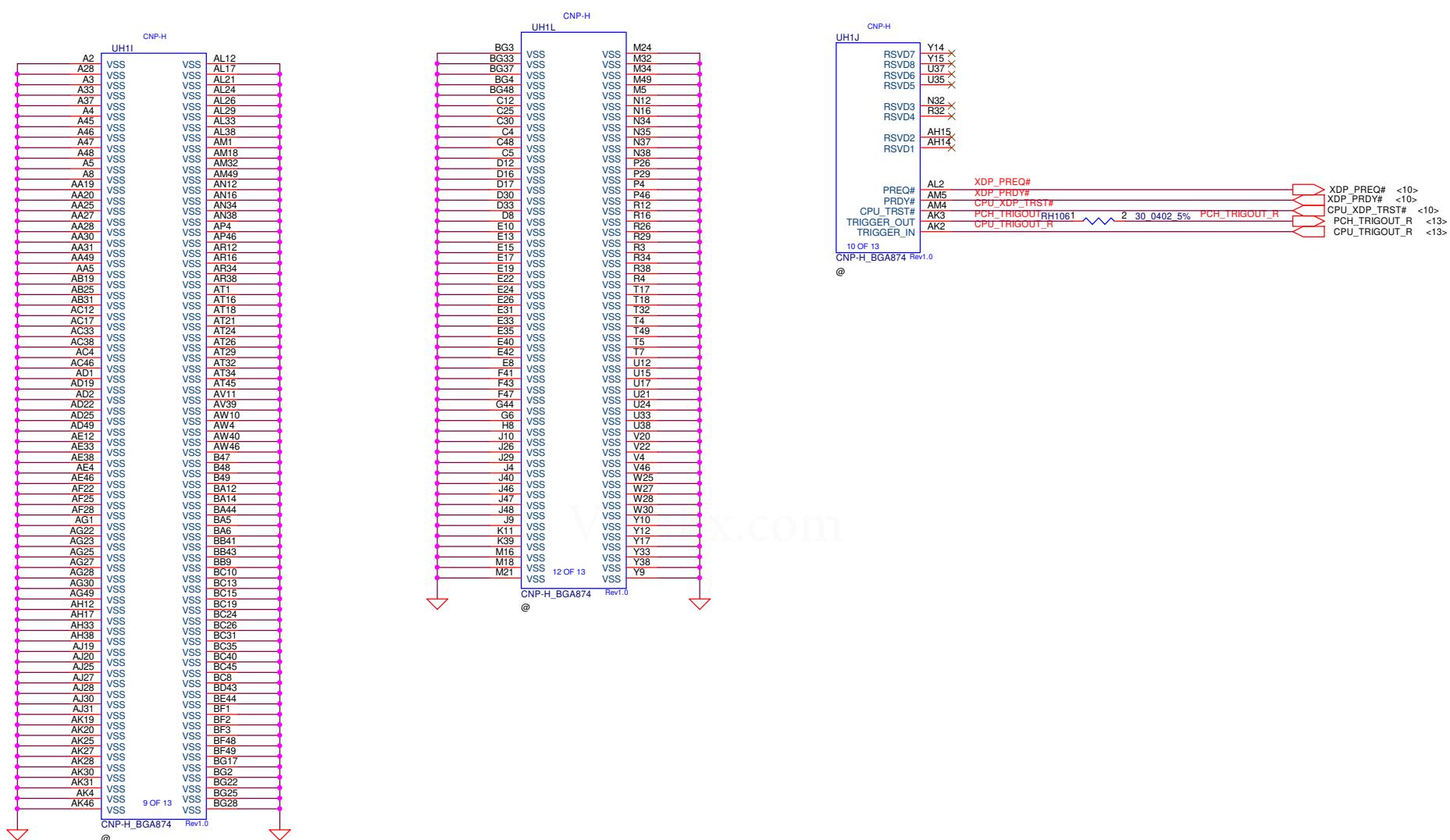






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# CHANNEL-A

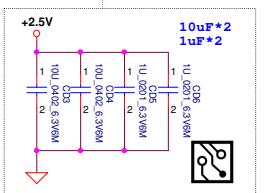
## BOT REVERSE TYPE (4 mm)

### Interleaved Memory

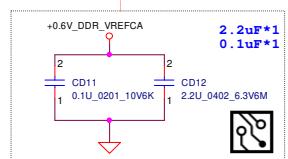
TOP: JDIMM1 CONN Non-ECC DIMM

SPD ADDRESS FOR CHANNEL A :  
 WRITE ADDRESS: 0XA0  
 READ ADDRESS: 0XA1  
 SA0 = 0; SA1 = 0; SA2 = 0.  
 DDR4 POR OPERATING SPEED: 1867 MT/S  
 STRETCH GOAL IS 2133 MT/S

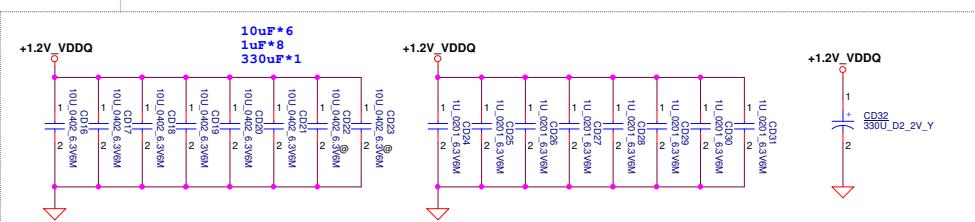
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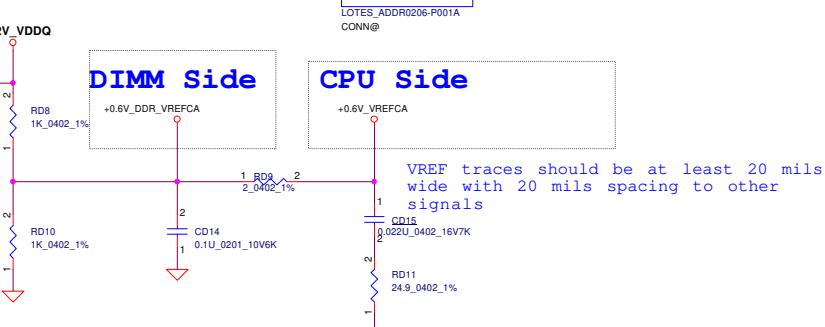
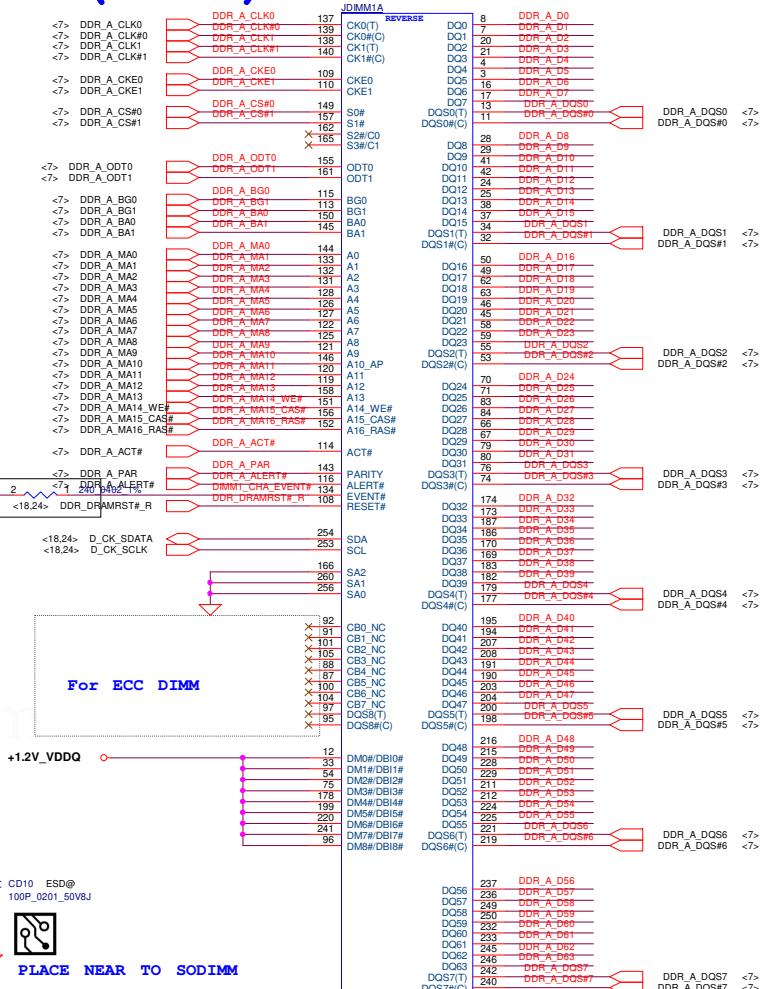
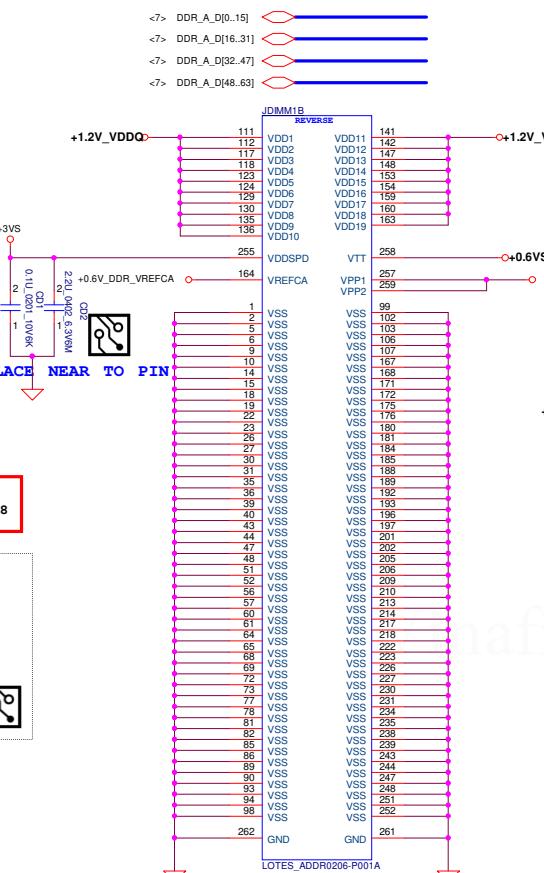
Layout Note:  
 PLACE THE CAP near JDIMM1. 164



Layout Note:  
 Place near JDIMM1



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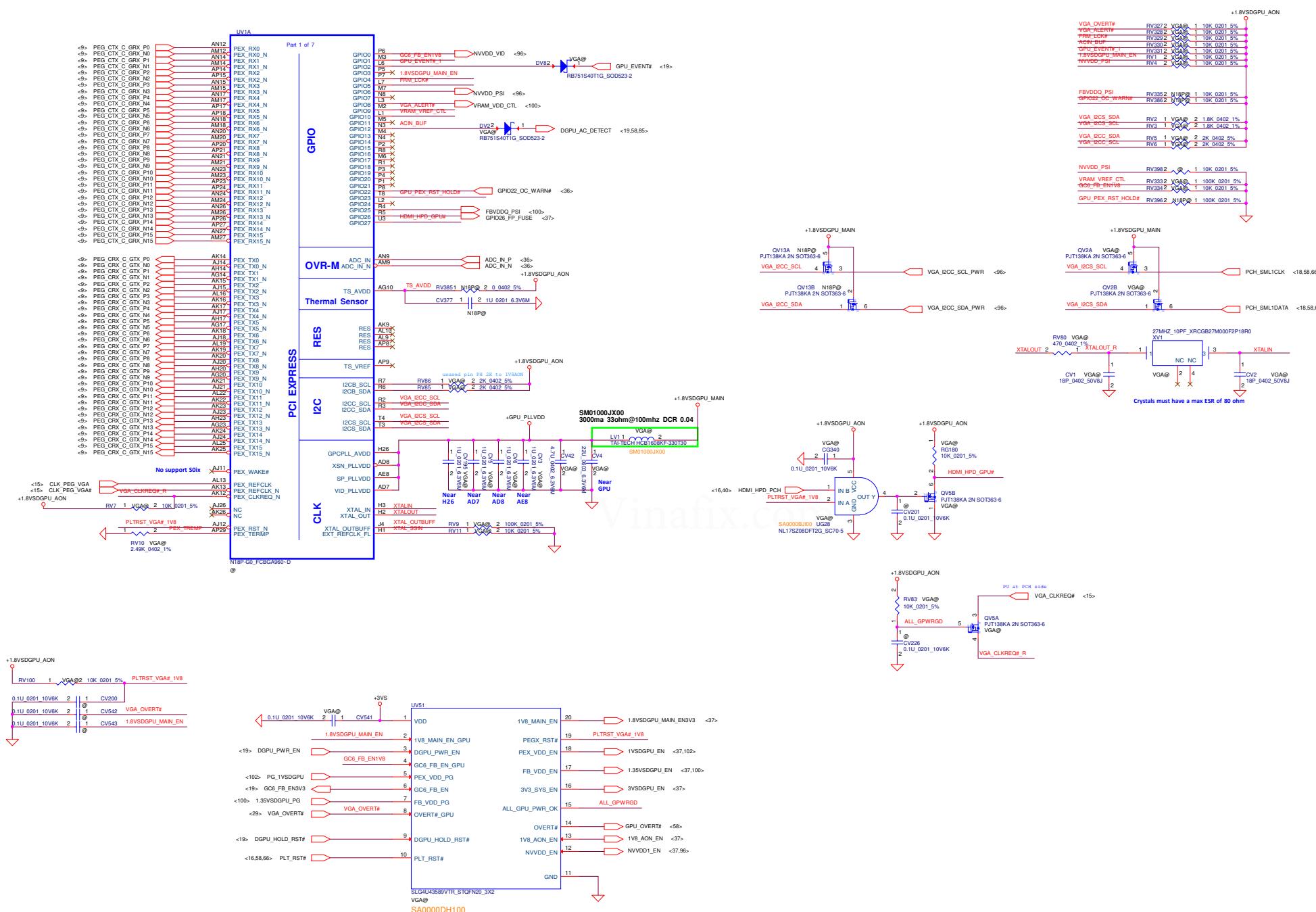


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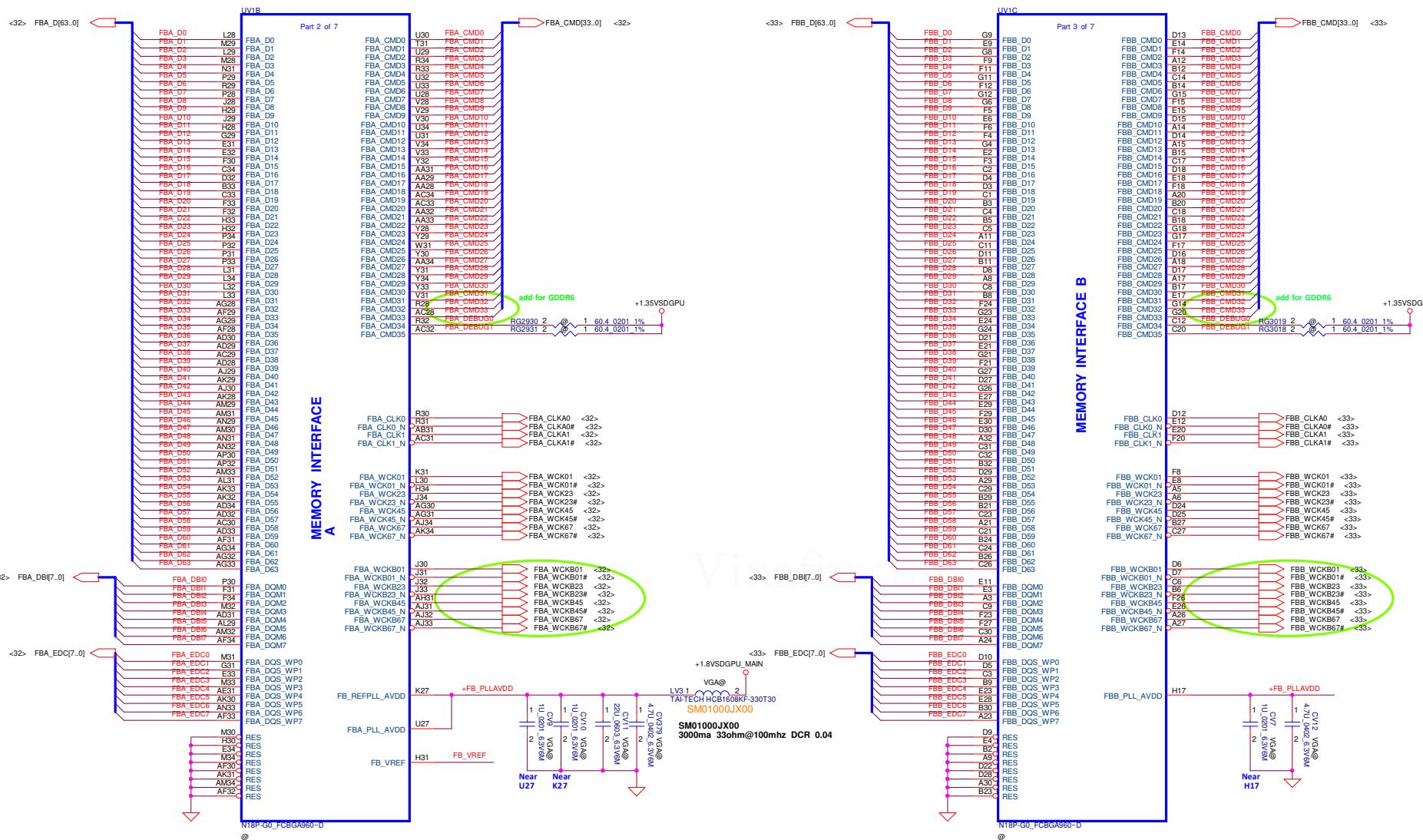
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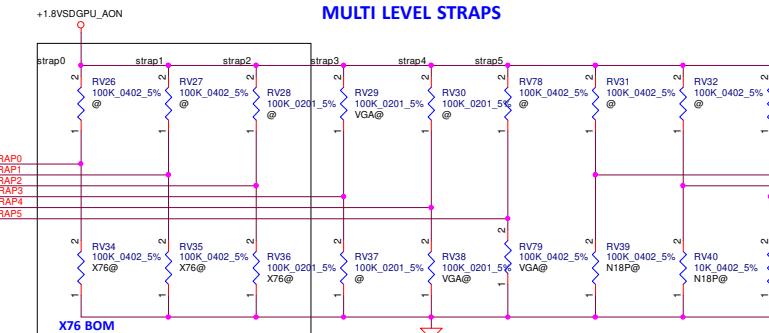
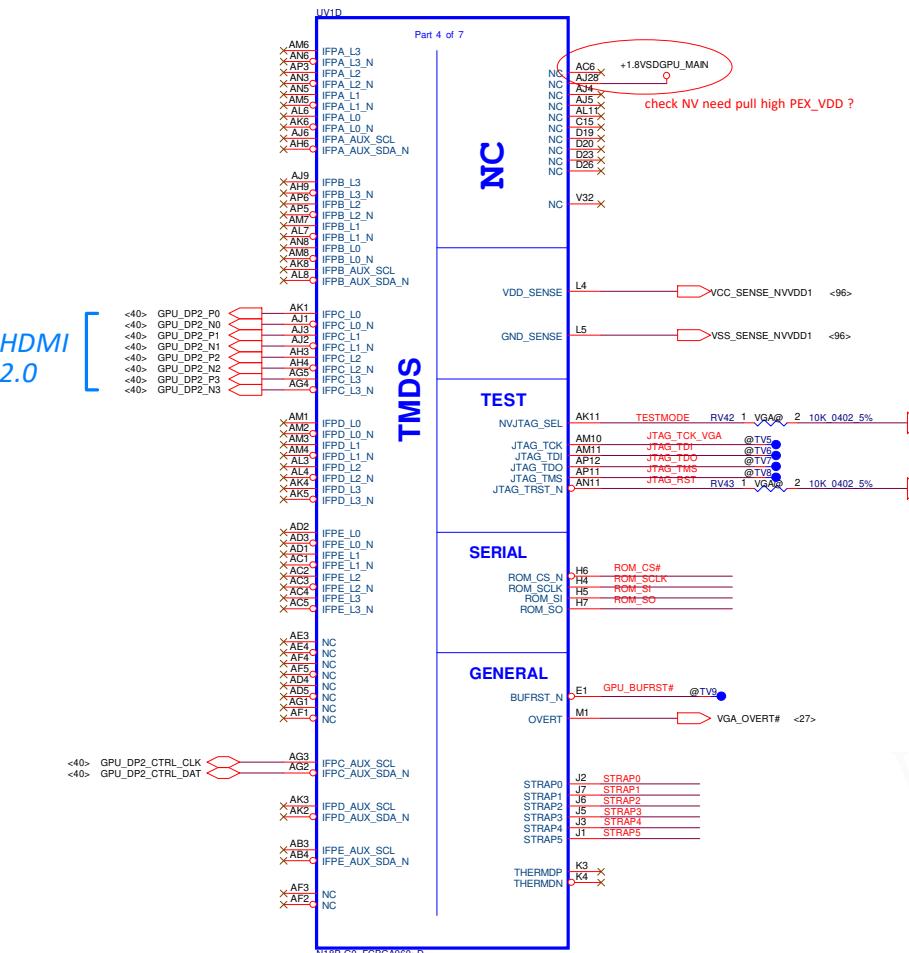
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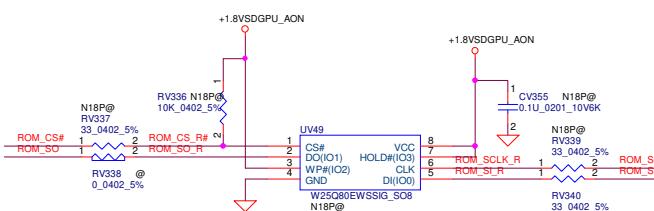


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Strap Pins			Note 1	FS_OVERT* Function
ROM_SO see Note 2	ROM_SI	ROM_SCLK		
L	L	L		FS_OVERT* function ENABLED
L	H	H		FS_OVERT* function DISABLED (Required, do not configure)
all other configurations				(invalid, do not configure)



QGPU VBIOS ROM 8Mb

Table 8. N18P-G62/G61 GDDR6 Recommended Memory

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert	Qual Plan	Status
8 Gb	2Chx256Mx16	1.2V and 1.25V <sup>2</sup>	Micron	MT61K256M32 JE-14:A	A-die	0x1	14 Gbps	1940 <sup>3</sup>	Full	Production candidate
			Samsung	K4ZB0325BC-HC14	C-die	0x0	14 Gbps	2001 <sup>4</sup>	Full	Production candidate

**Notes:**

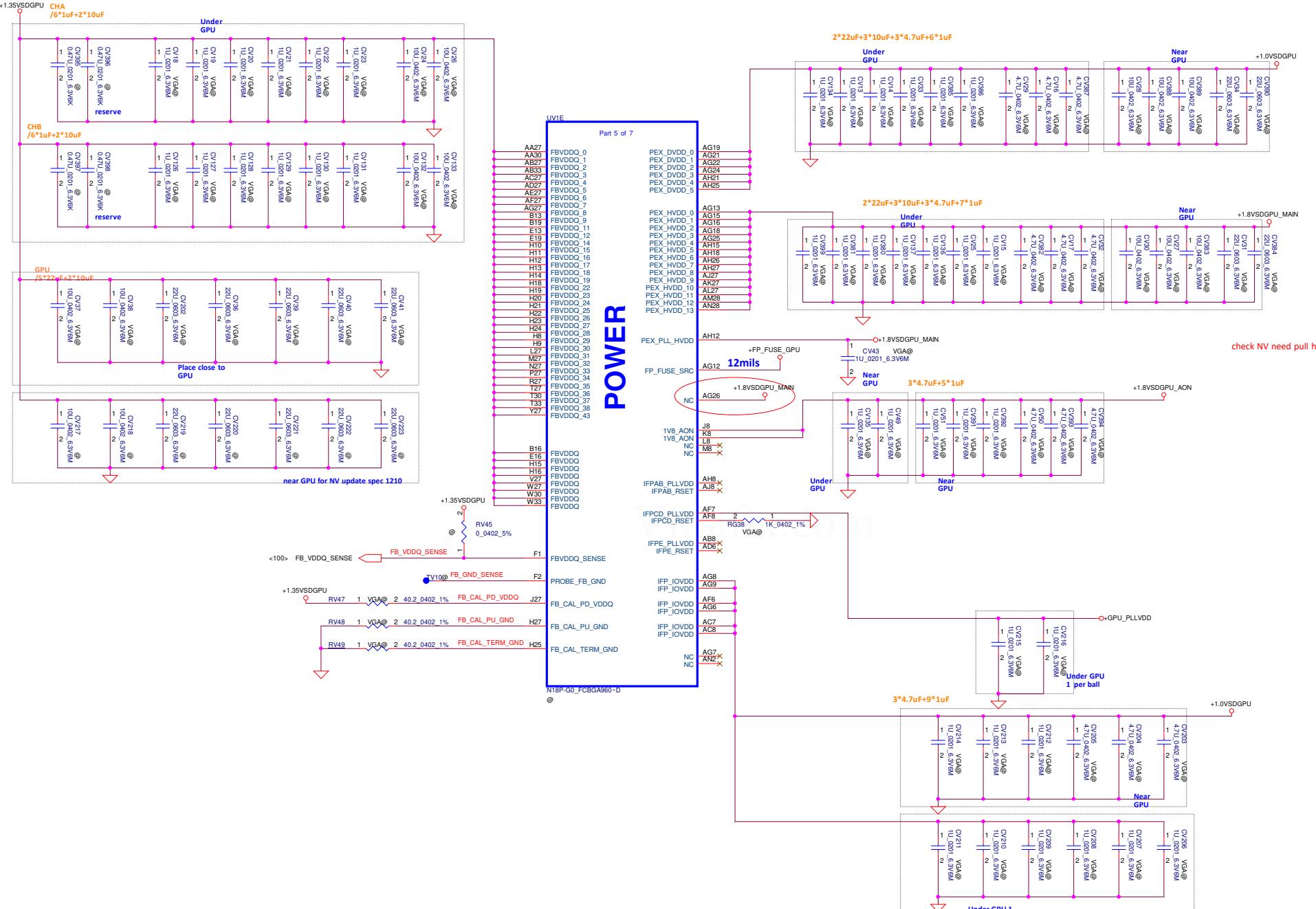
- For N18P-G62/G61, the maximum allowable memory case temperature is 95 °C.
- DVS is required to run WCLK > 5500 MHz.
- Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Micron memory will include the "GDDR6 1.2V @ 11 Gbps" words in the label.
- Before the date code is available, the specially screened (for 11 Gbps @ 1.2V support) Samsung memory is identified by "SPL" letters inserted

Table 12.3 RAMCEG

Strap Pins see Note			RAMCFG Setting Number (see Memory RVL for memory configs corresponding to these numbers)
STRAP2	STRAP1	STRAP0	
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Strap Pins Note 1			Functions Selected by This Strapping				
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
L	L	L	0	0	0	0	
L	L	H	0	0	0	1	
L	M	M	0	0	1	0	
L	H	H	0	0	1	1	
H	L	L	0	1	0	0	
H	L	H	0	1	0	1	
H	H	L	0	1	0	0	
H	H	H	0	1	1	1	
L	L	M	1	0	0	0	
L	M	L	1	0	0	1	
L	M	H	1	0	1	0	
L	H	M	1	0	1	1	
M	L	L	1	1	0	0	
M	L	H	1	1	0	1	
M	H	L	1	1	1	0	
M	H	H	1	1	1	1	

SMB_ATL_ADDR	
★ LOW	Single GPU
High	Dual GPU
DEVID_SEL	
★ LOW	Orig. Device ID
High	Support G-Sync GUID
VGA_DEVICE	
LOW	3D Device
★ High	VGA Device
PCIE_CFG	
★ LOW	Normal signal swing
High	Reduce the signal amplitude



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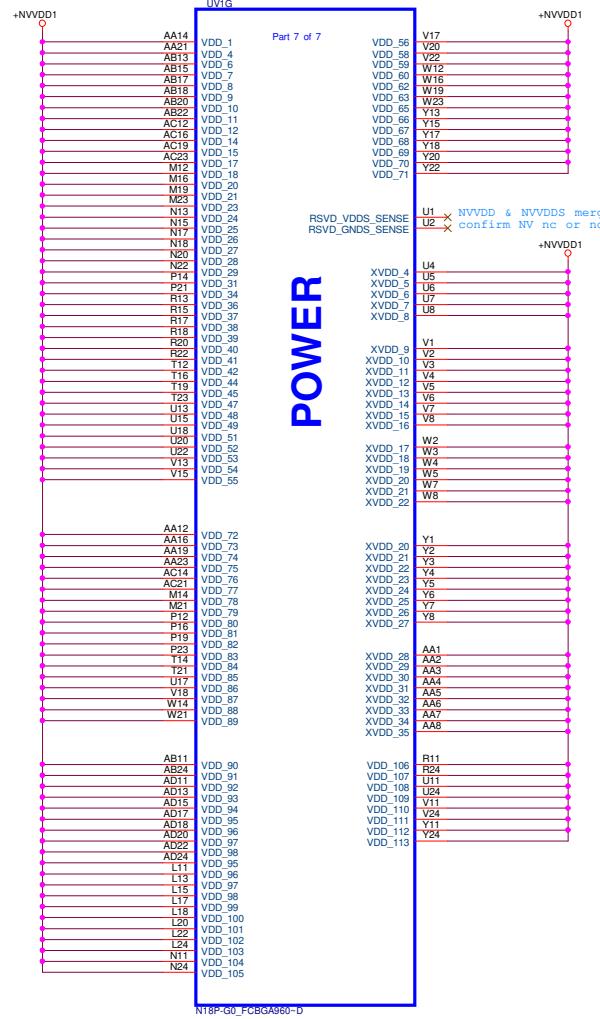
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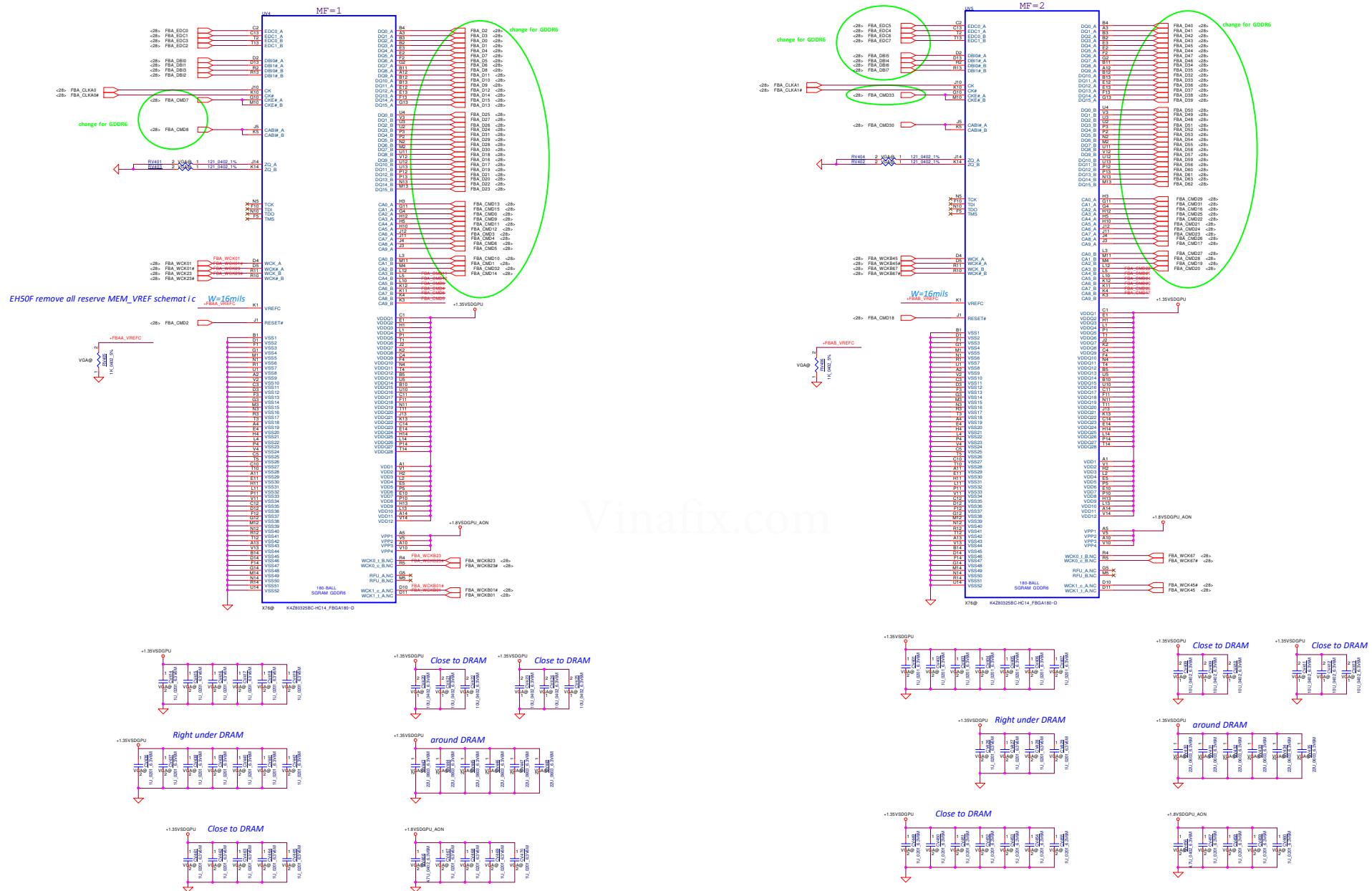
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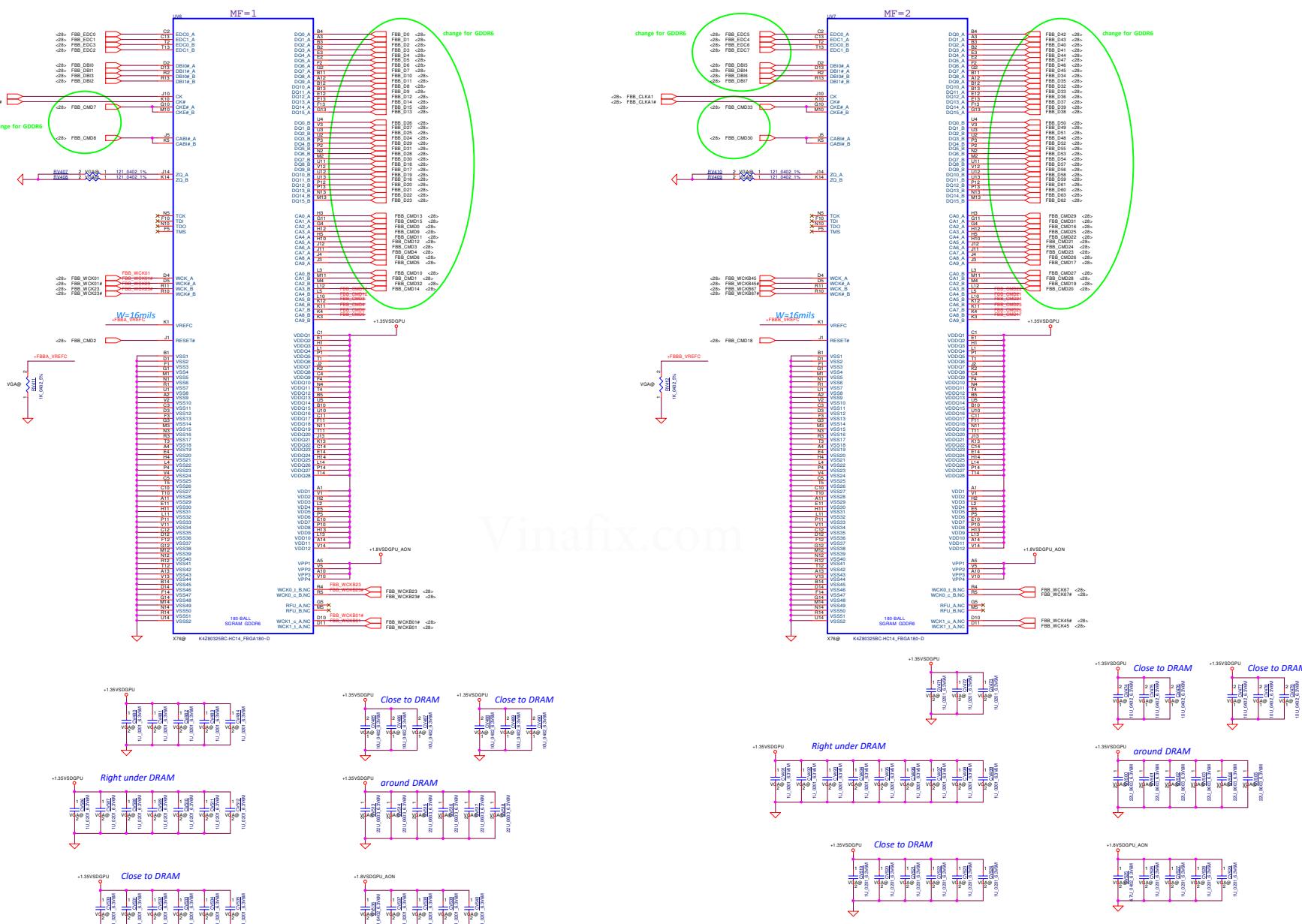
**H5VF M/B LA-J861P**

Wednesday, February 05, 2020

N17P\_VDDS  
1uF\*5/4.7uF\*5 (under GPU)  
330uF\*1/22uF\*3/10uF\*2/4.7uF\*2







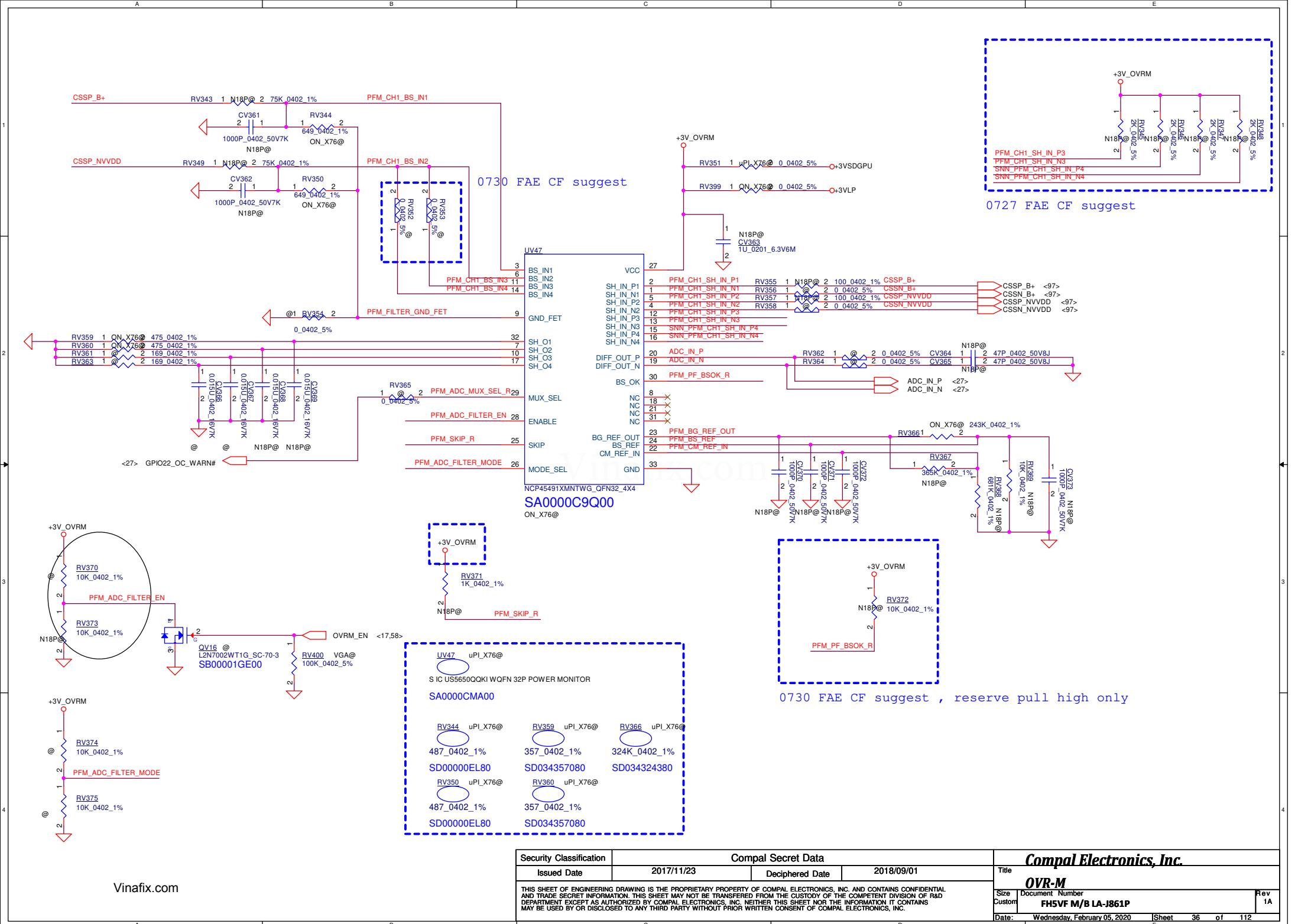
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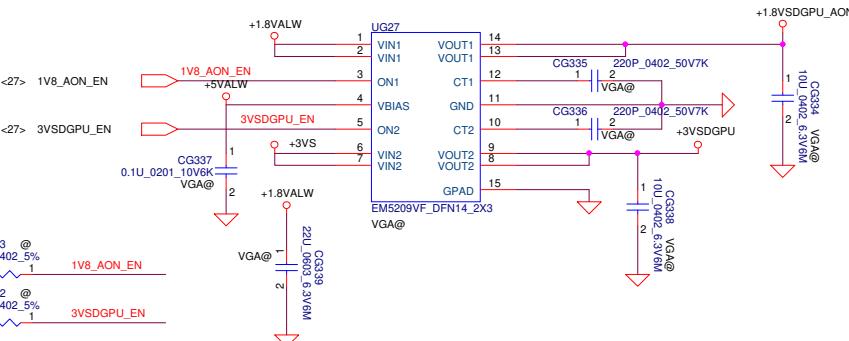
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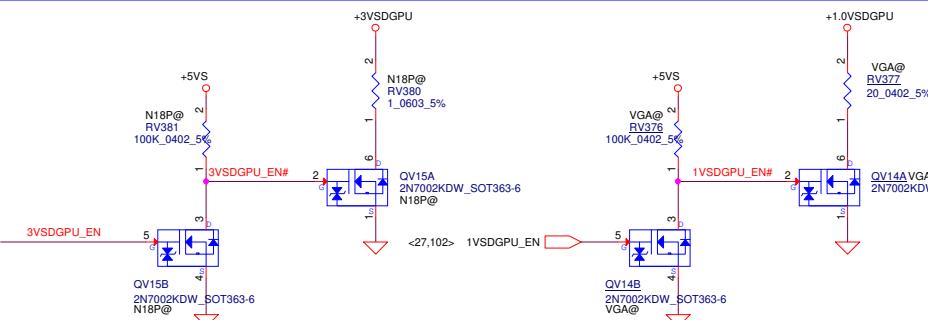
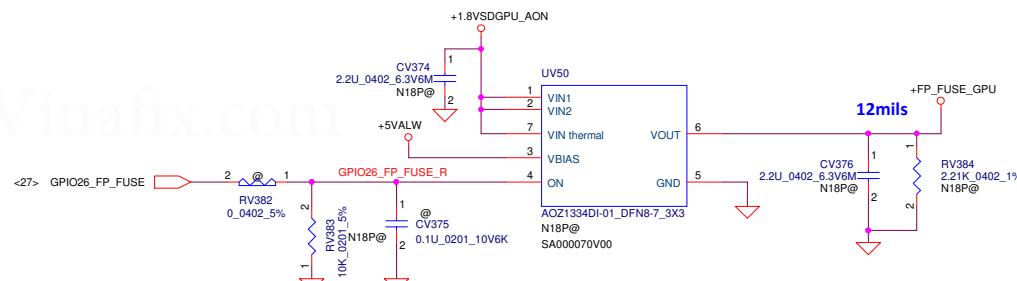
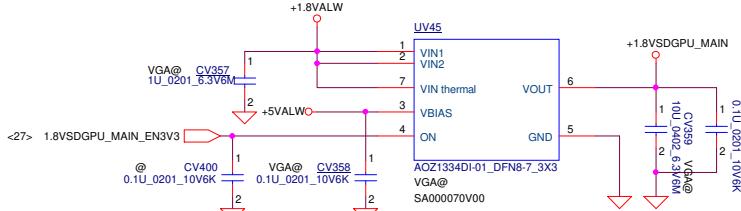
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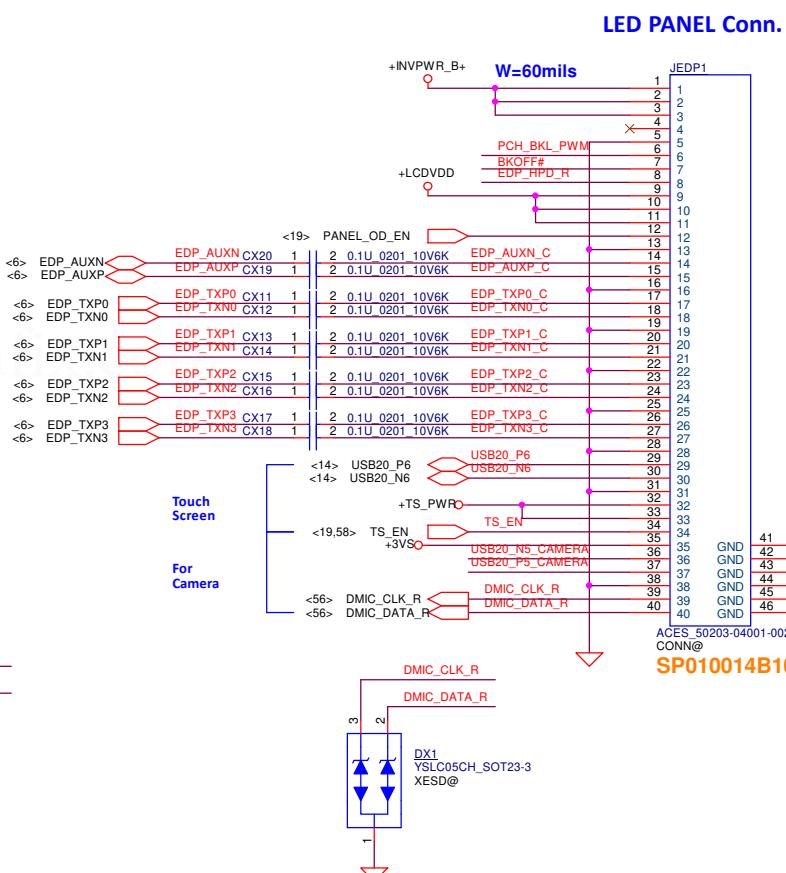
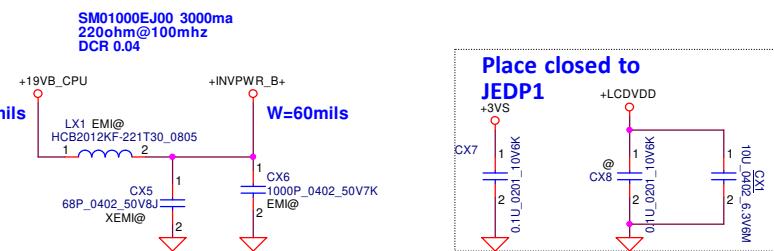
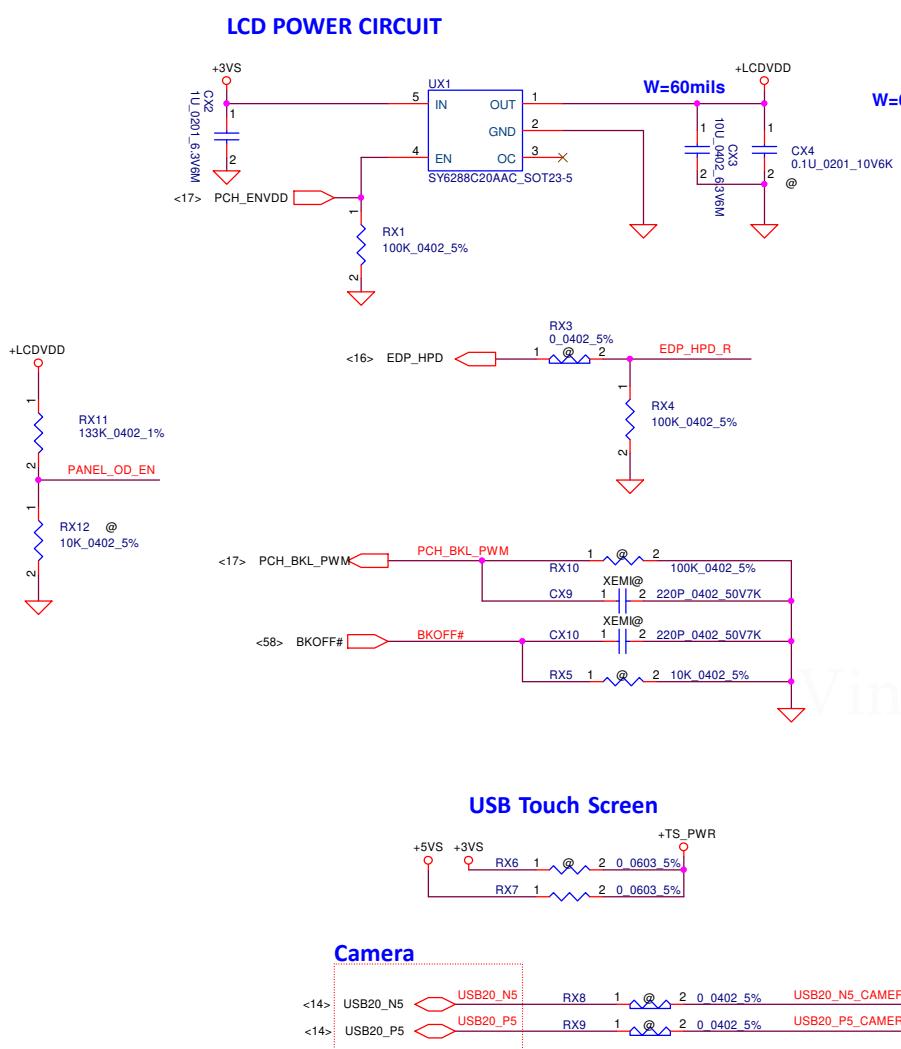
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# +1.8V\_MAIN



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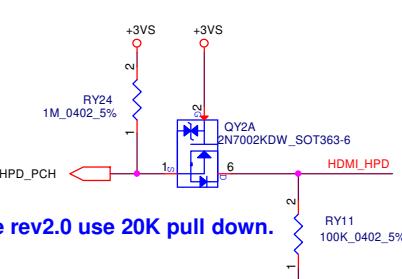
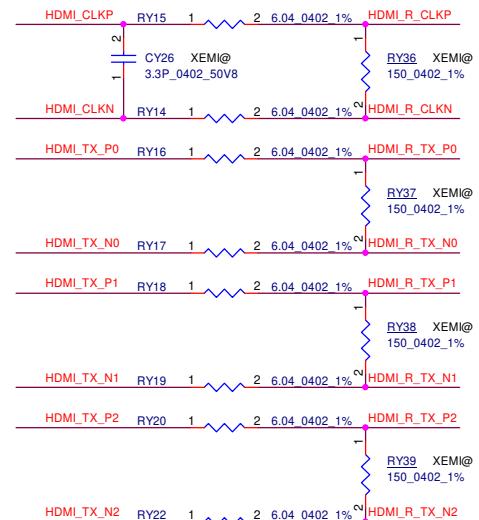
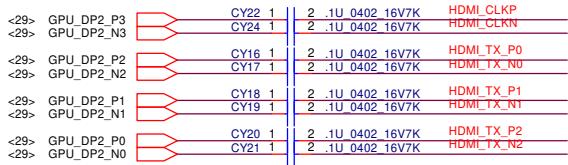


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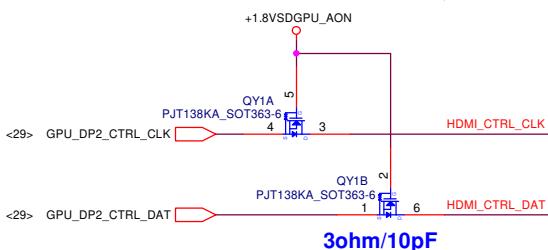
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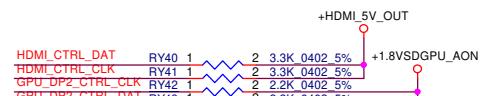
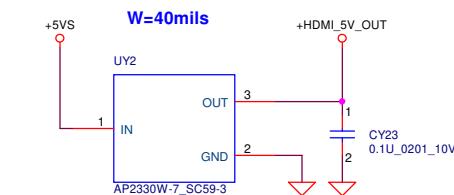
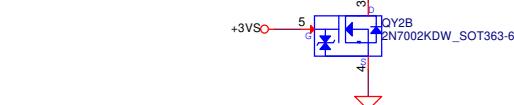


**RY11 design guide rev2.0 use 20K pull down.**

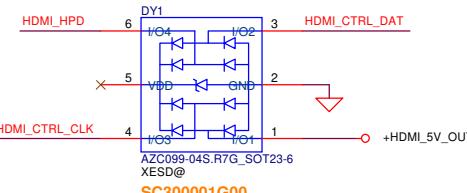
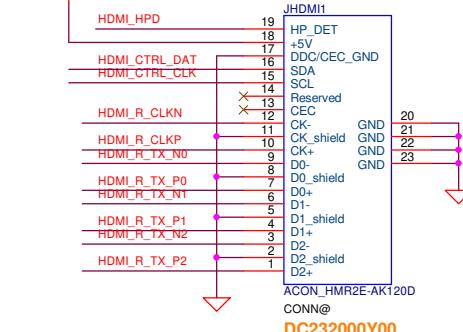


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**3ohm/10pF**



### HDMI connector



C

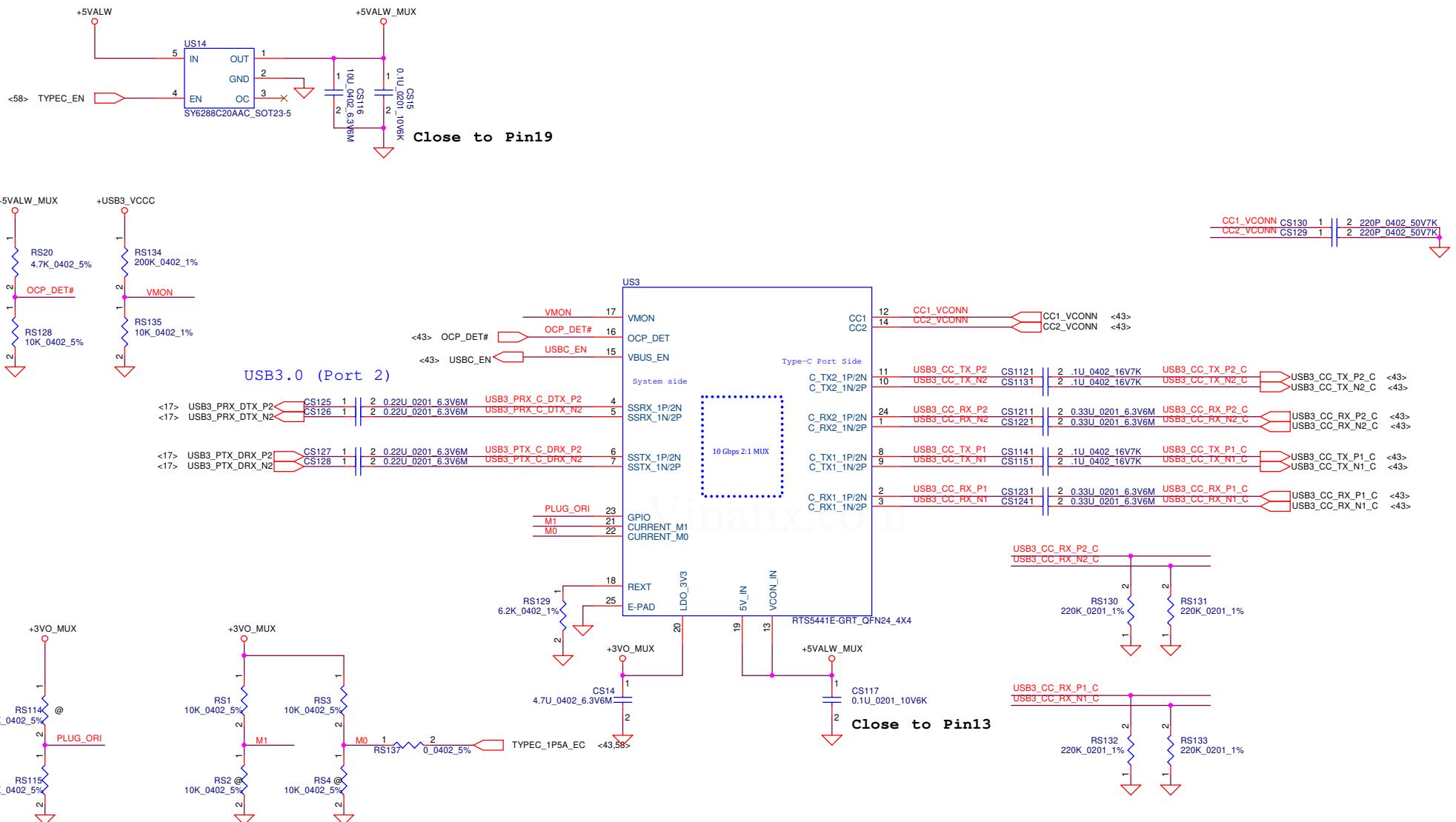
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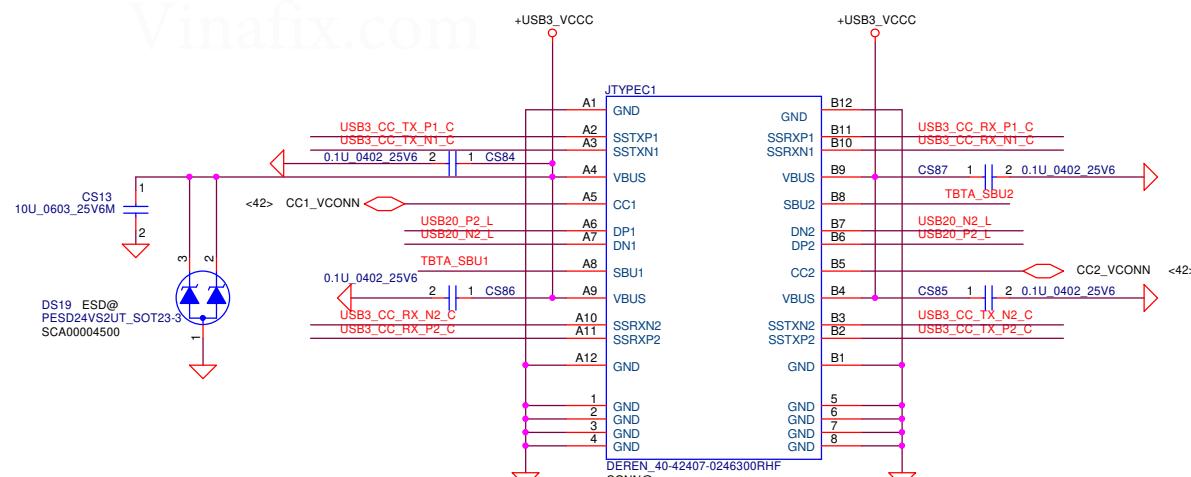
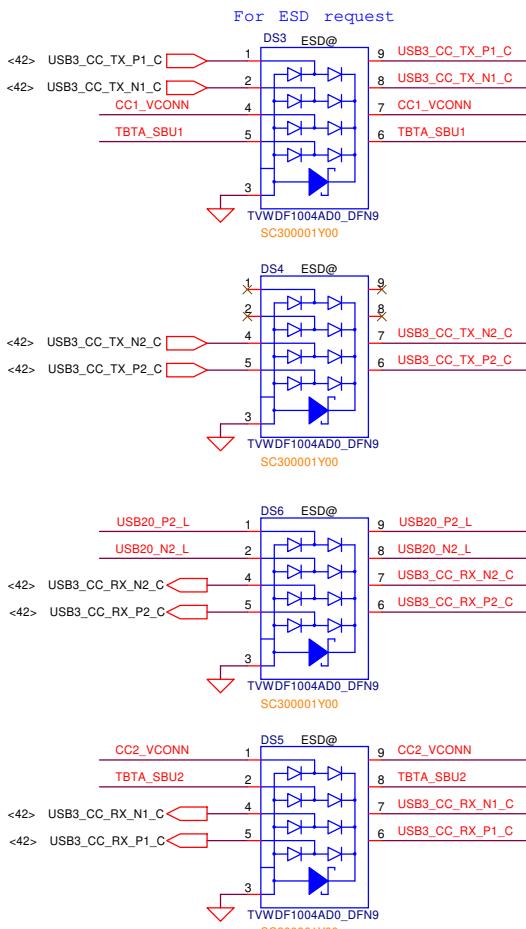
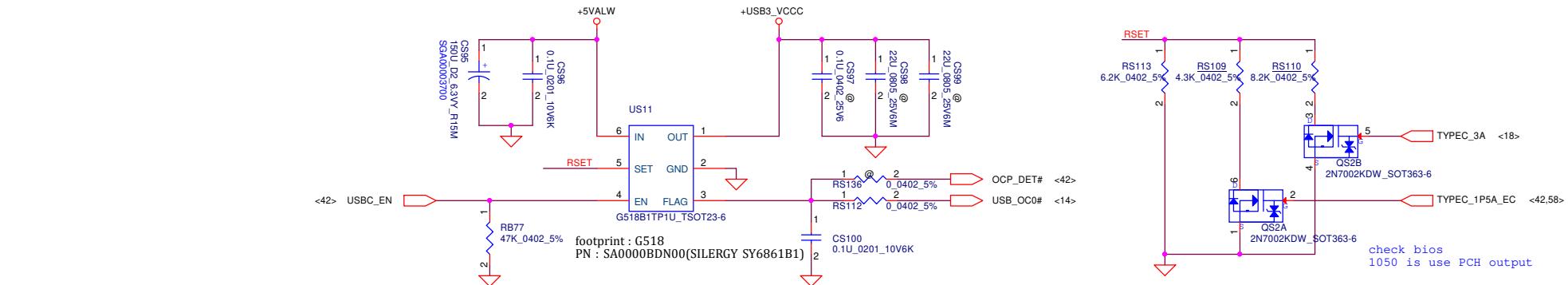
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5441E Current Limit		
M1	M0	MODE
L	H	0.9A
H	L	1.5A
H	H	3A

RTS5441 M0 truth table by 2018 BIOS spec			
TYPEC_1P5A_EC	MODE	limit point	Condition
H	3A	3.5A	AC mode or Battery >30%
L	1.5A	1.92A	Battery <30% when DC mode

confirm realtek hand-shake



CC1\_VCONN & CC2\_VCONN need 20mil trace width.

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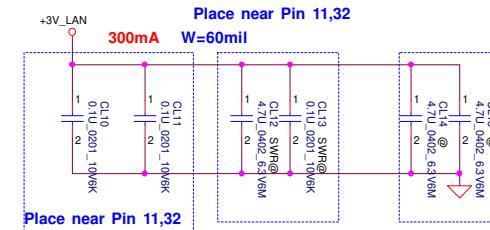
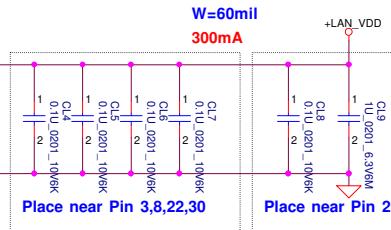
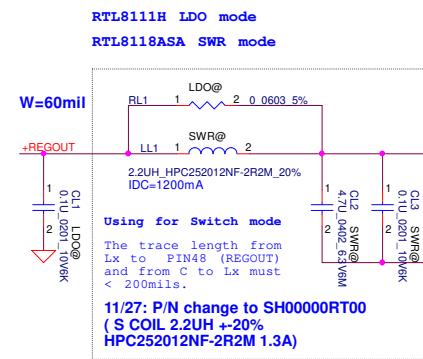
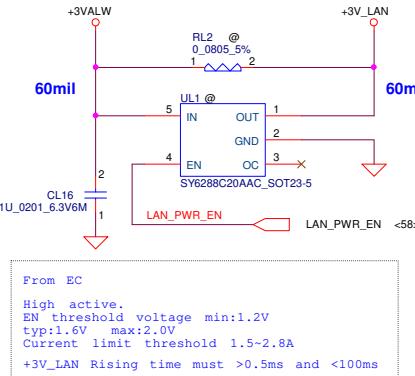
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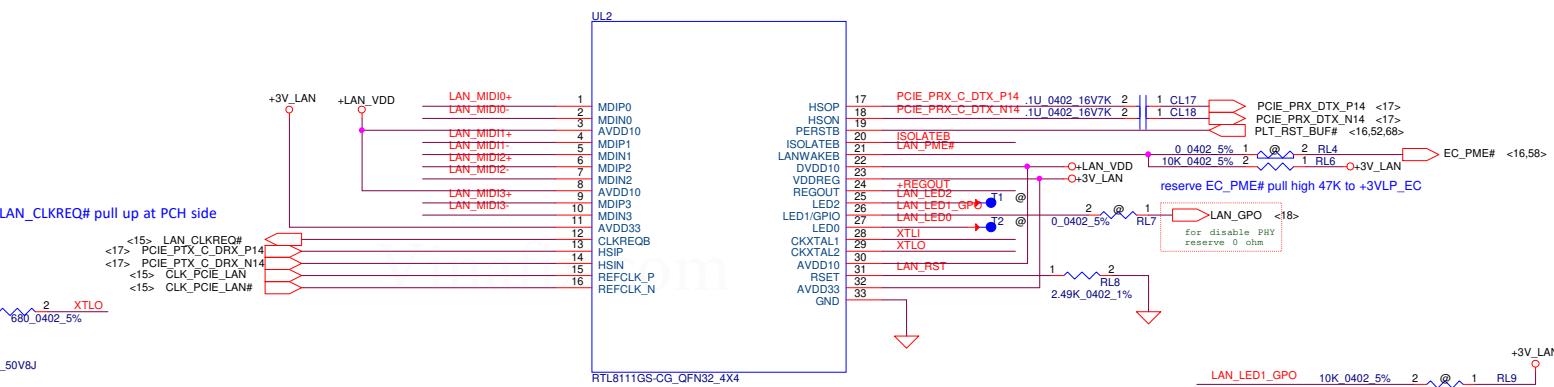
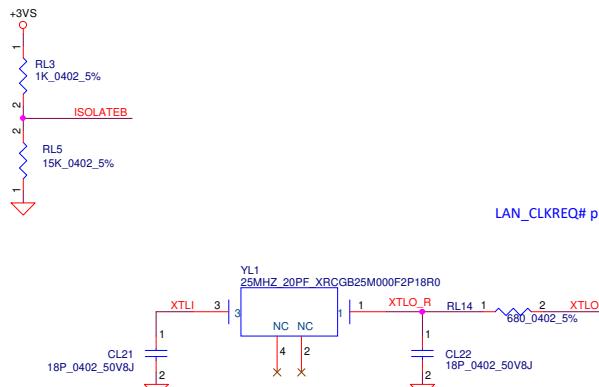
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+3V\_LAN Rising time (10%~90%) must >0.5mS and <100mS

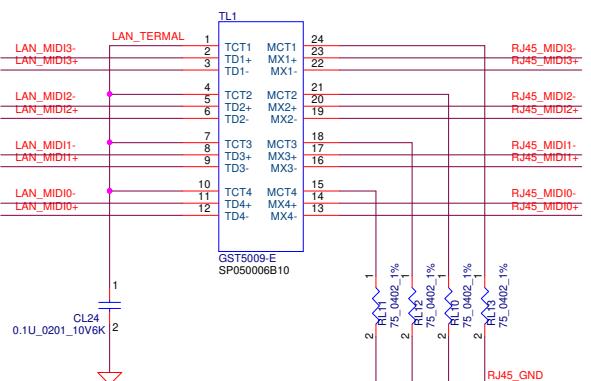


Reserve for surge improvement  
Place near Pin 11,32

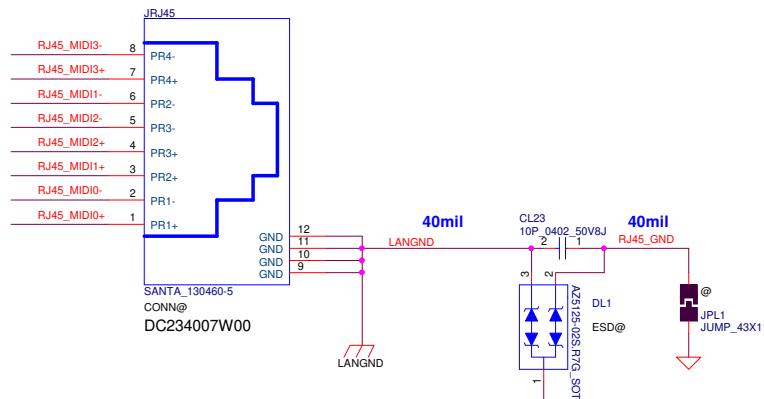


P/N: SJ10000UP00 (S CRYSTAL 25MHZ 10PF XRCGB25M000F2P34R0)

SA000080P00, SIC RTL8111H-CG QFN 32P E-LAN CTRL



### LAN Connector



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Compal Electronics, Inc.

Issued Date 2017/10/30 Deciphered Date 2018/10/30

Title LAN RTL8111H

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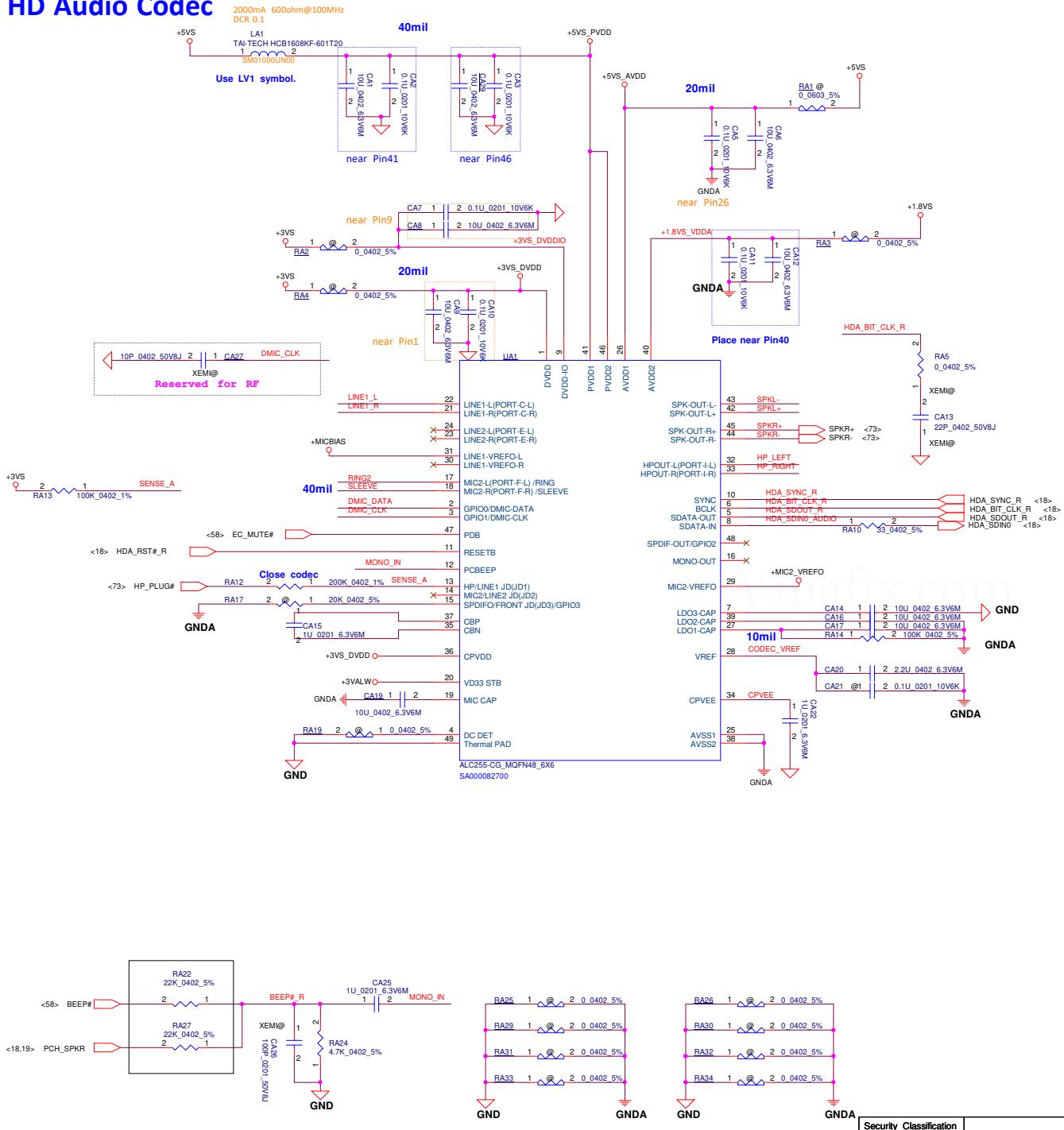
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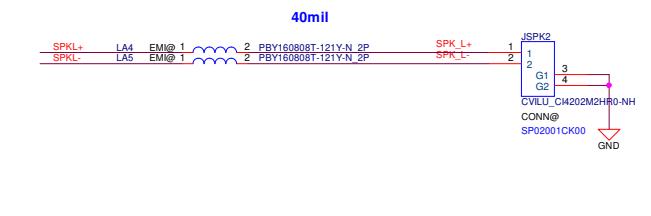
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# HD Audio Codec

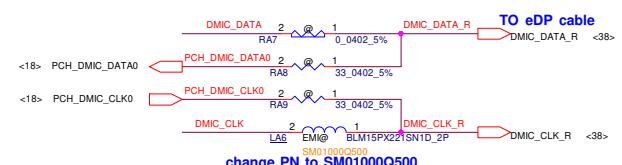


## Int. Speaker Conn.

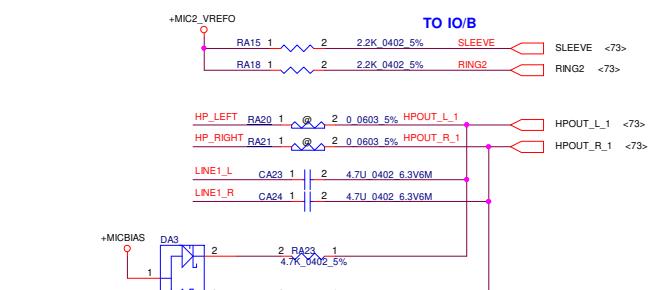


## Digital MIC

MIC BOM upload by Audio Team



## Headphone Out



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2017/10/30

2018/10/30

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HD Audio Codec ALC255

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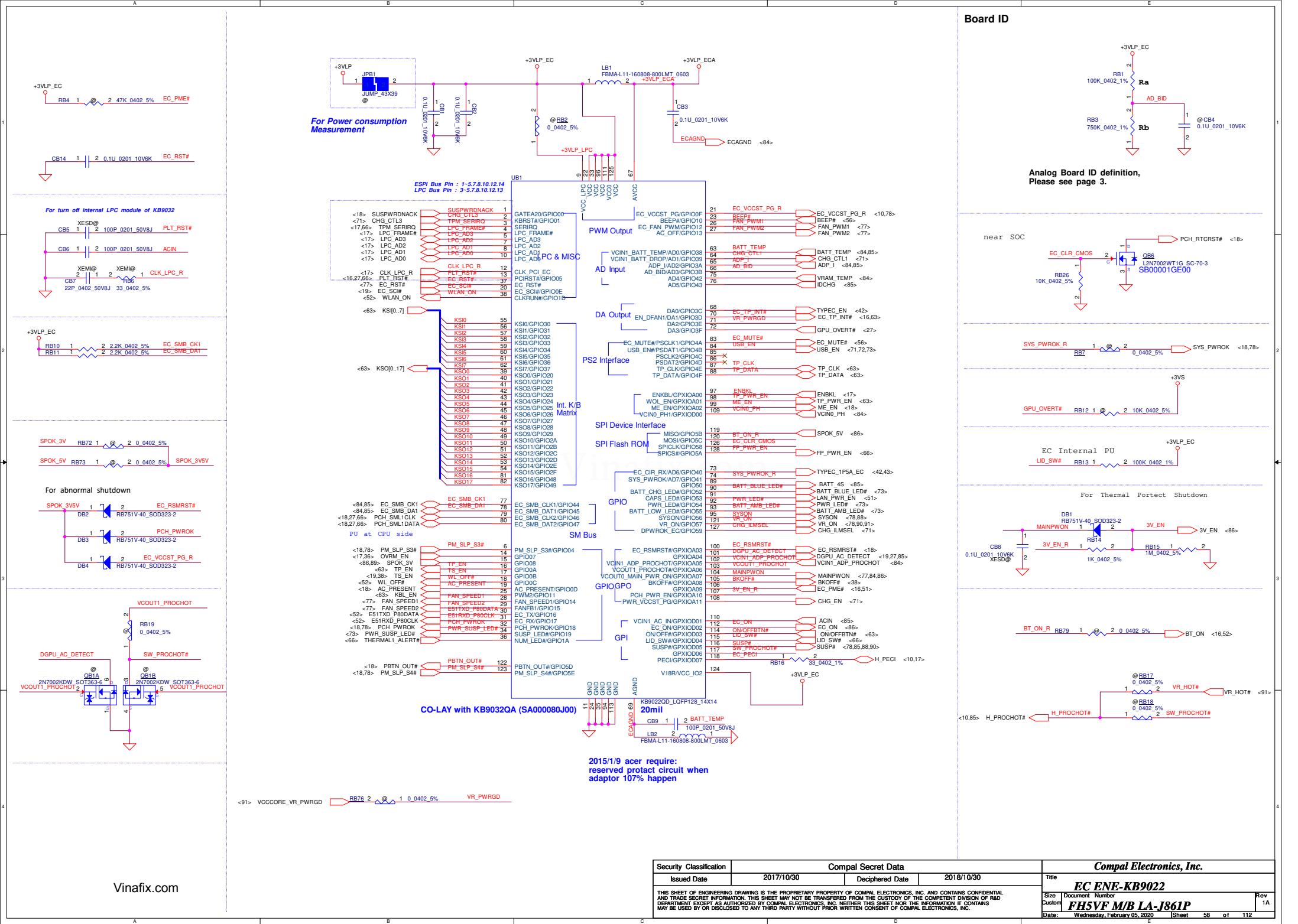
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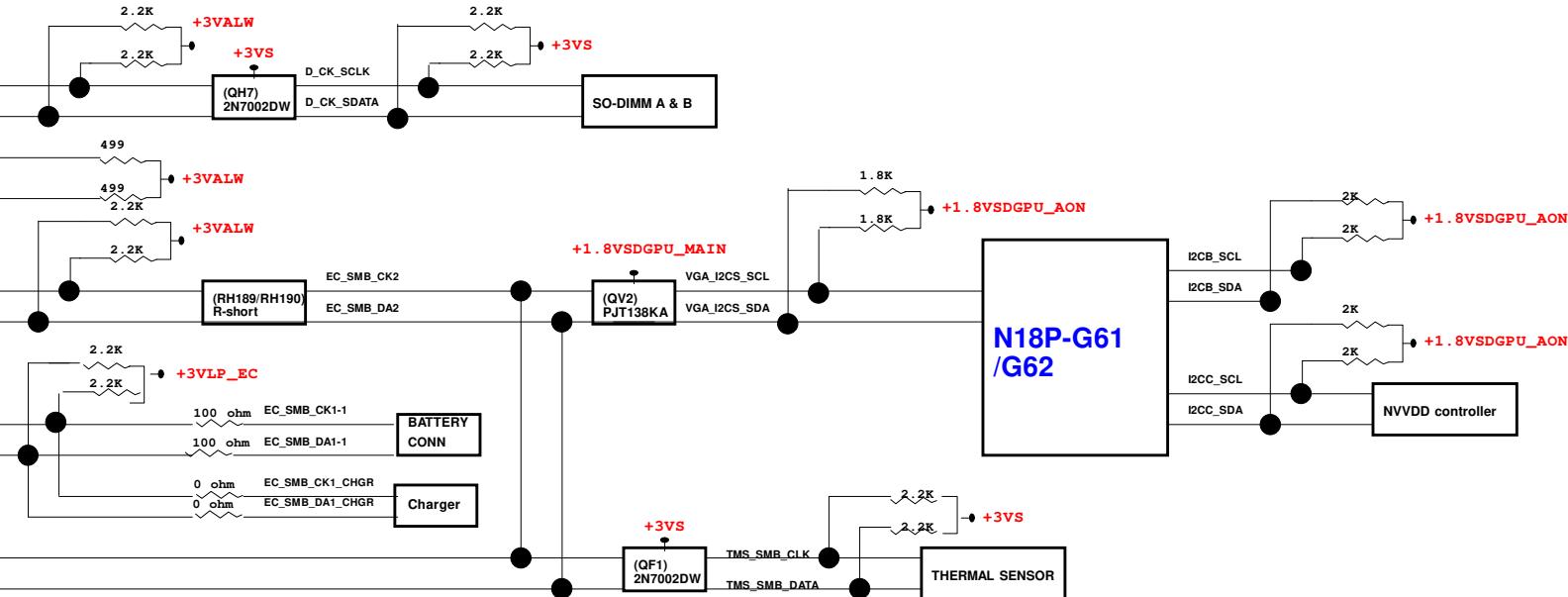
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**Cannonlake**  
**PCH - H**

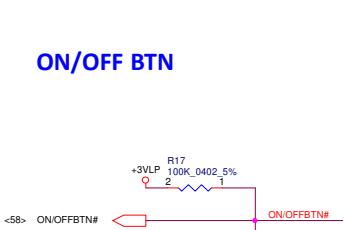
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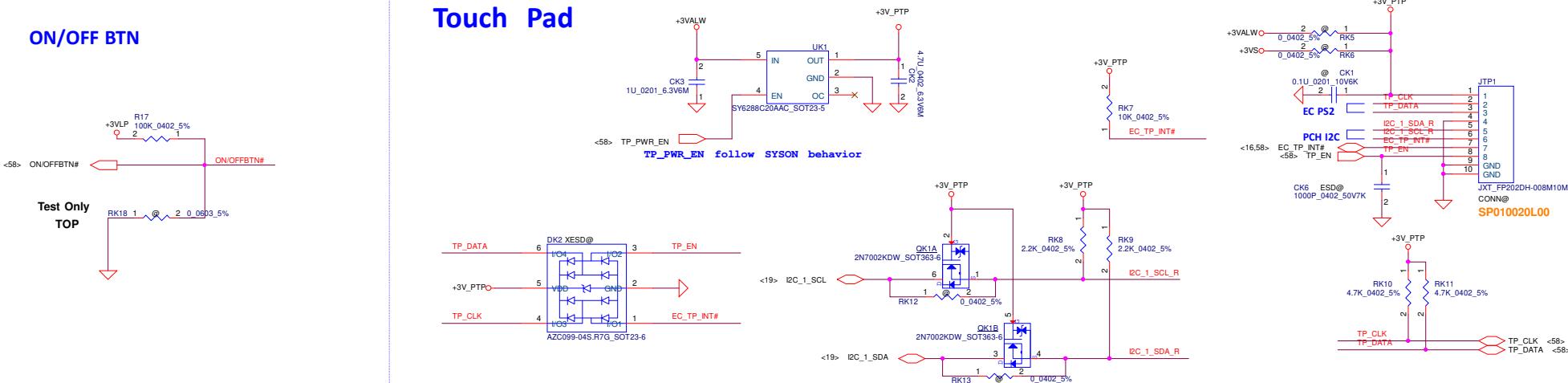
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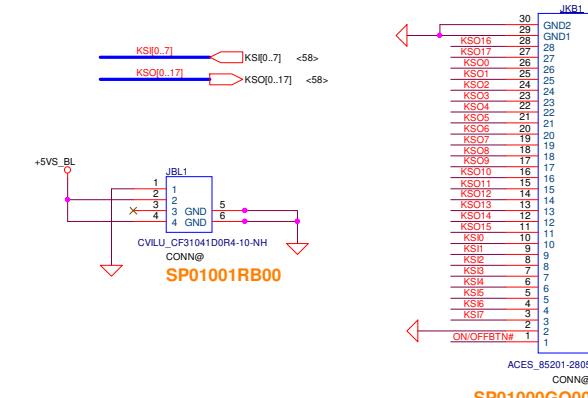
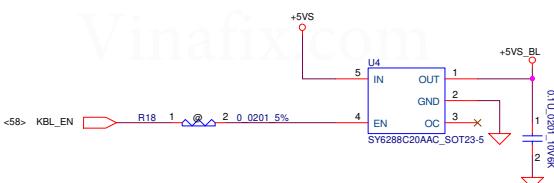
## ON/OFF BTN



## Touch Pad



## KB Conn. / Backlight



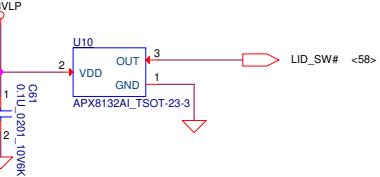
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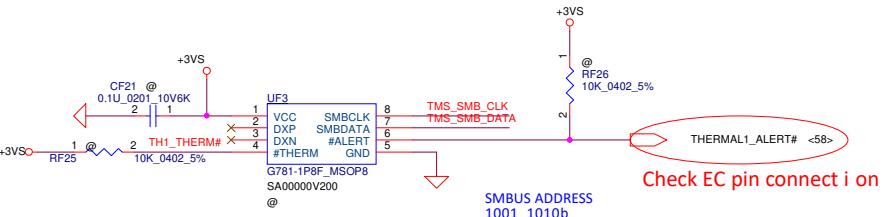
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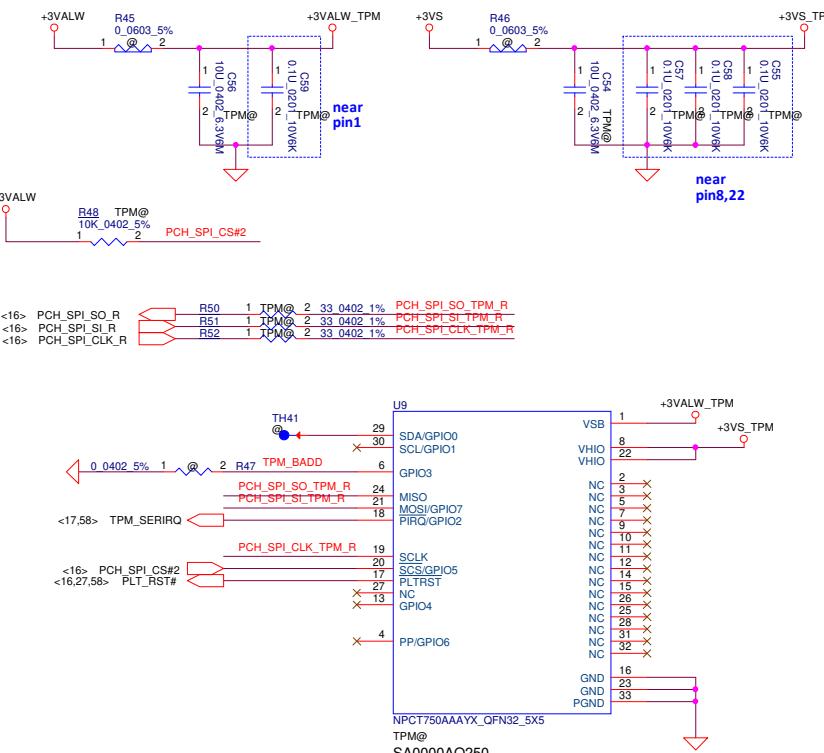
## Hall sensor



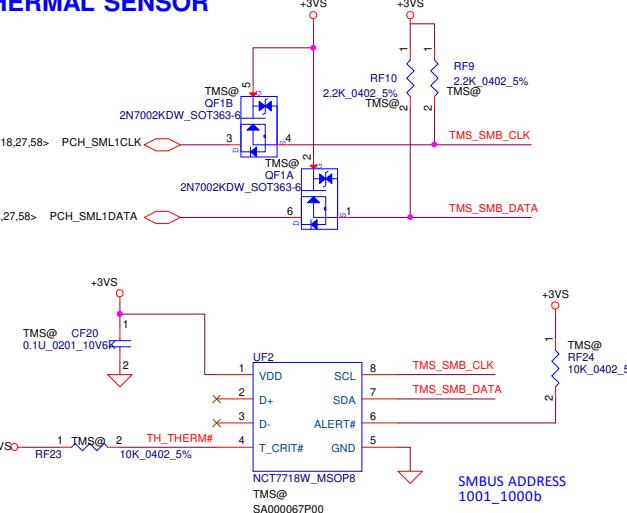
## Thermal sensor for safety



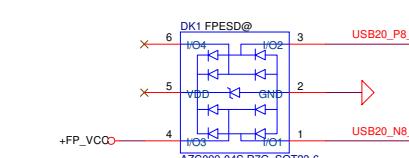
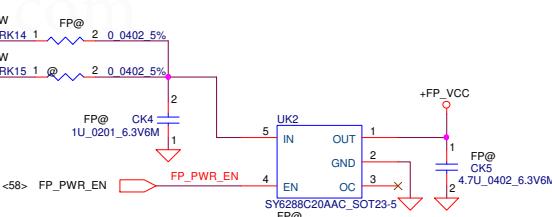
## TPM



## THERMAL SENSOR



## Finger Print



PIN	ETU801	FA577E-1200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7	NC	NC
8	NC	NC

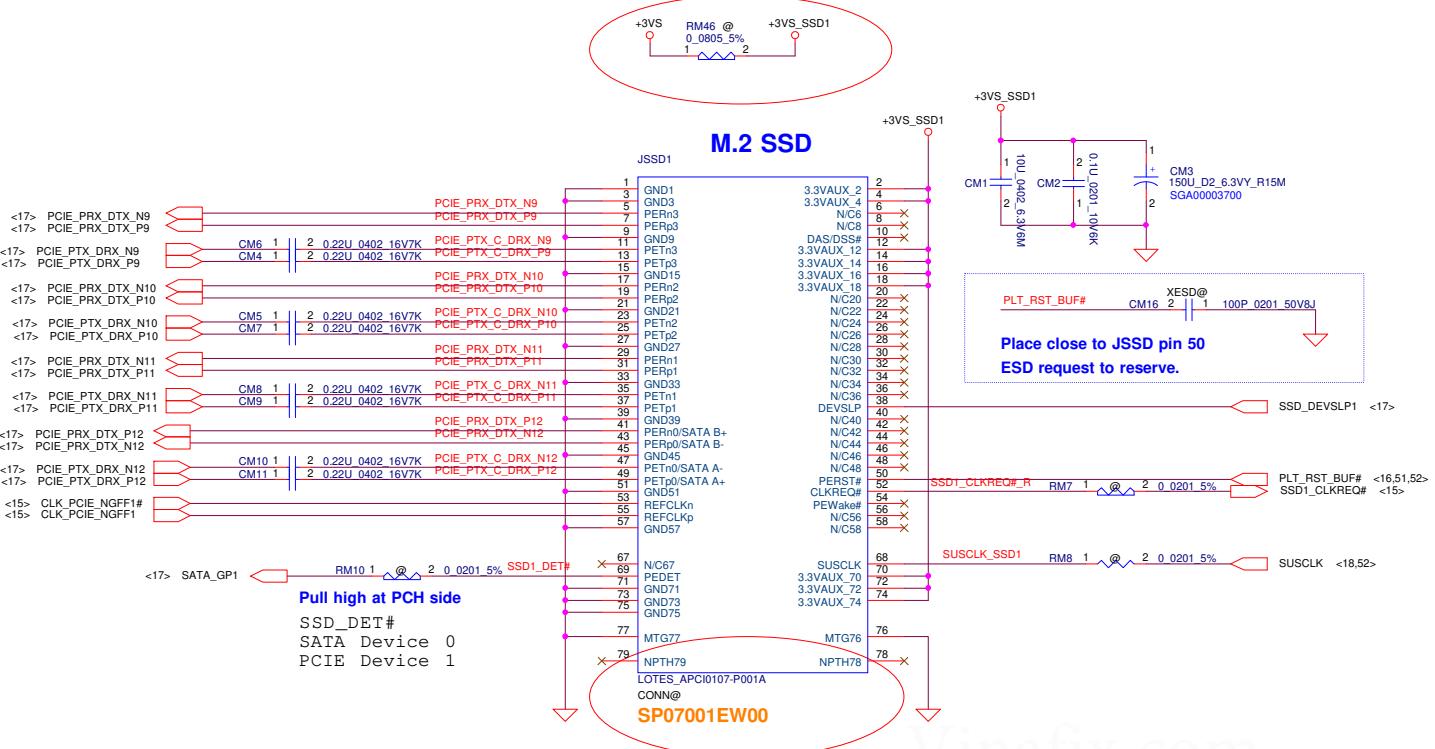
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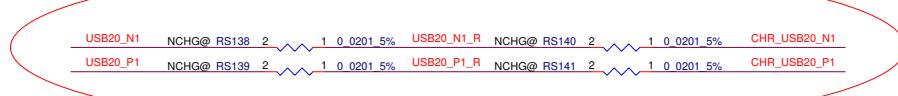
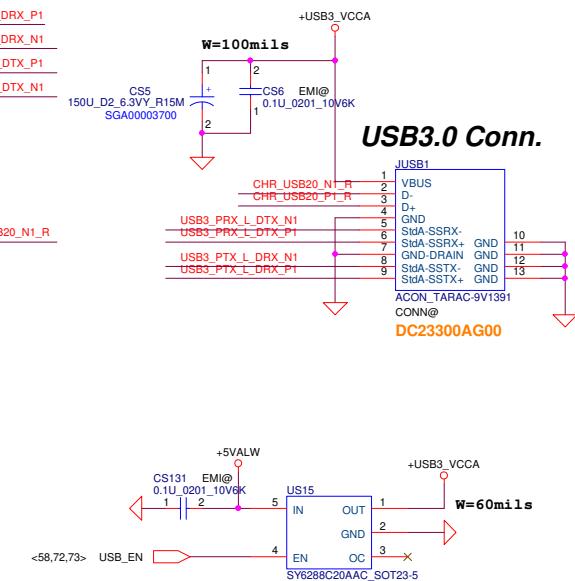
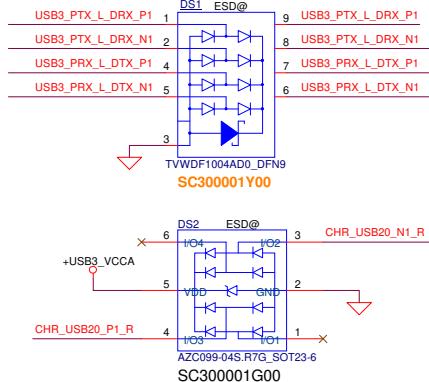
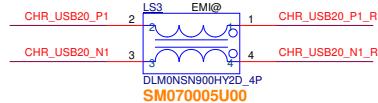
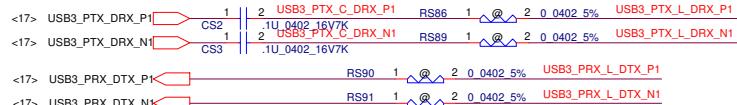
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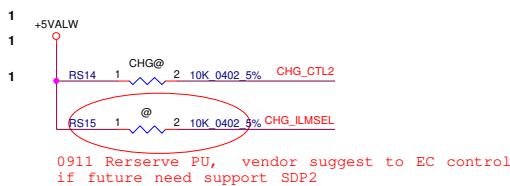
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## USB3.0

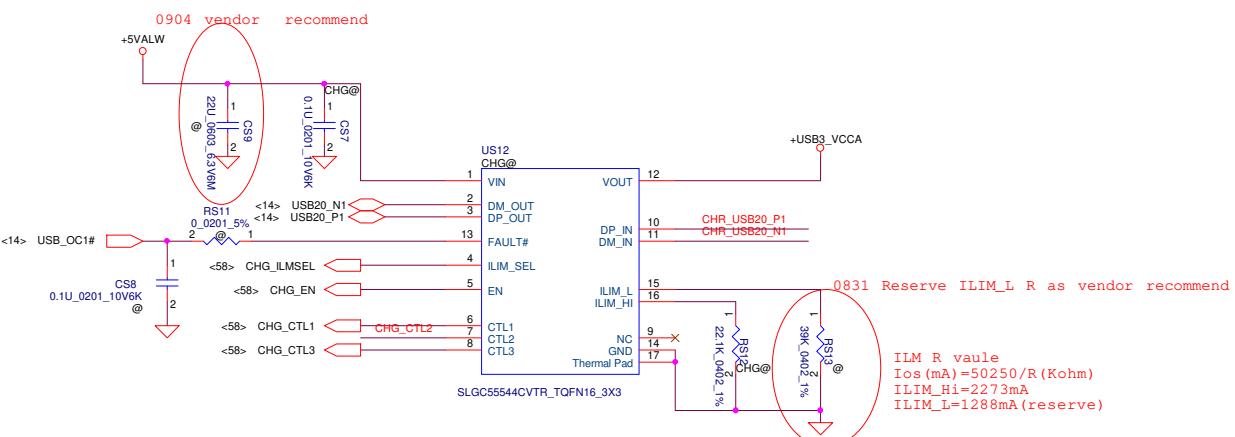


## USB Host Charger

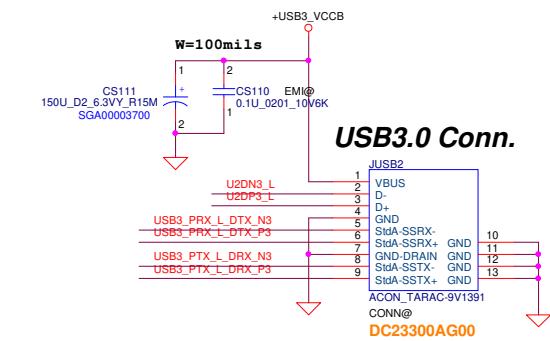
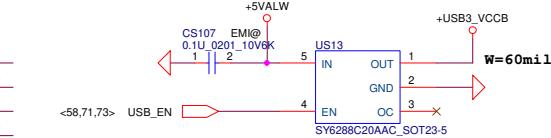
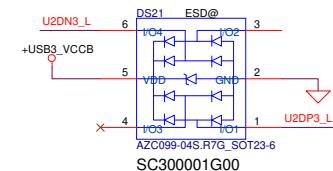
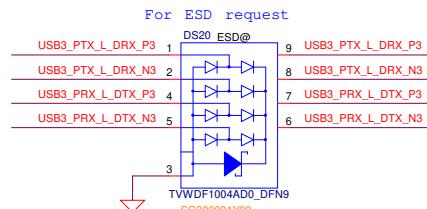
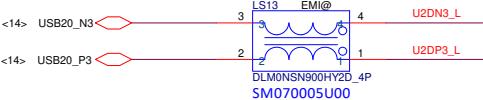
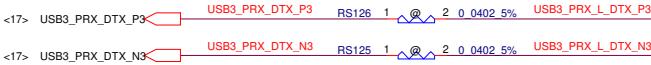
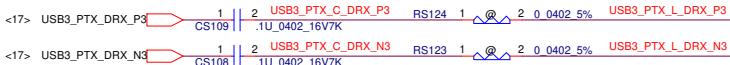


## USB Host Charger Truth Table

CHG_EN	CTL1	CTL2	CTL3	ILIM_SEL	MODE	Current Limit Setting	Note
0	1	0	1	SDP1-OFF	ILIM_H	Port power off	
0	1	0	1	SDP1	ILIM_H	Data Lines Connected	
0	1	1	1	DCP Auto	ILIM_H	Data Lines Disconnected	
1	1	1	1	CDP	ILIM_H	Data Lines Connected	



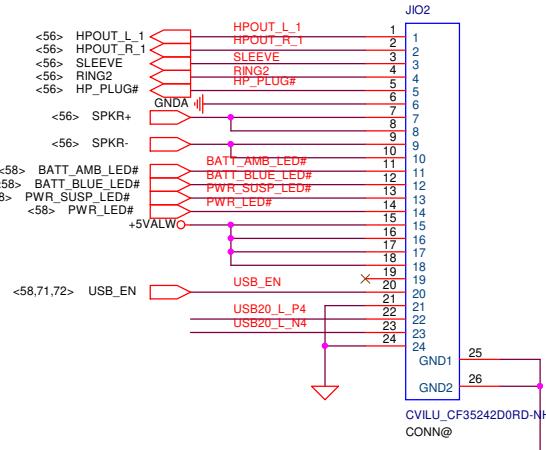
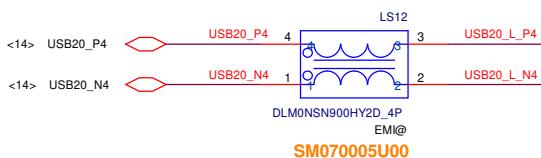
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## USB3.0 Conn.

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# IO/B CONN



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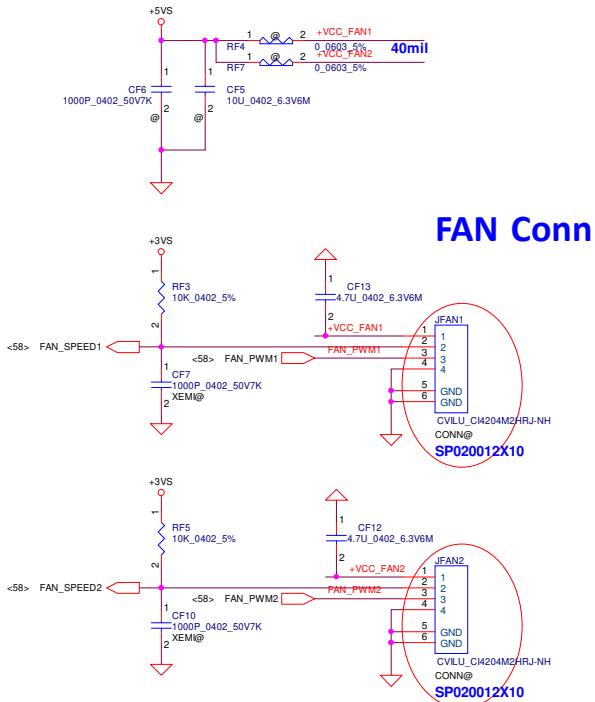
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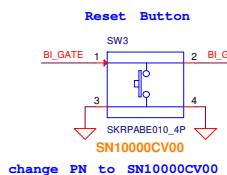
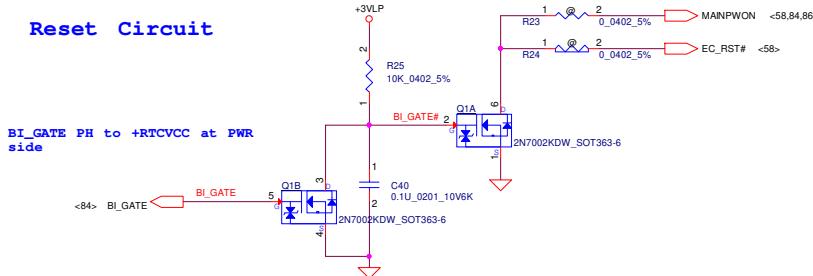
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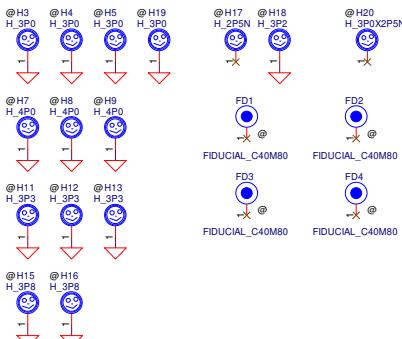
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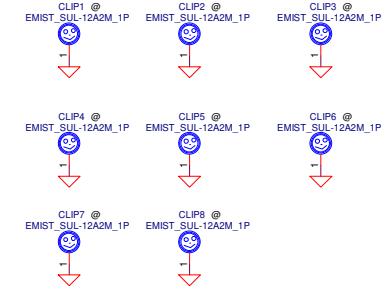
### Reset Circuit



### Screw Hole



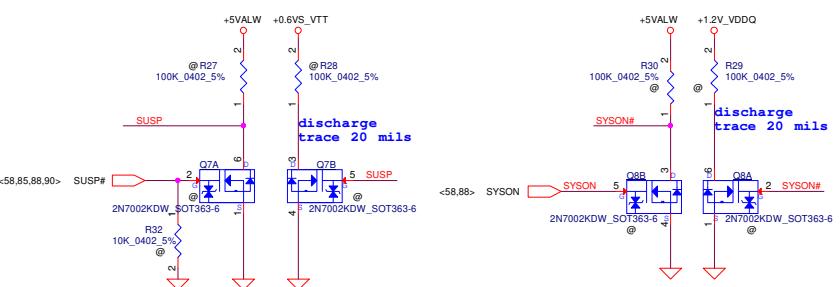
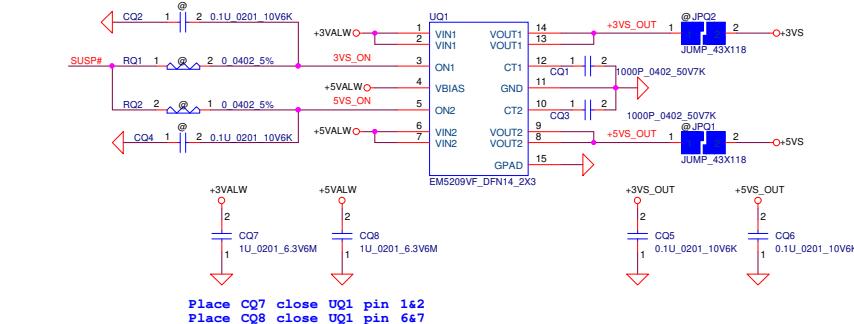
### Clips



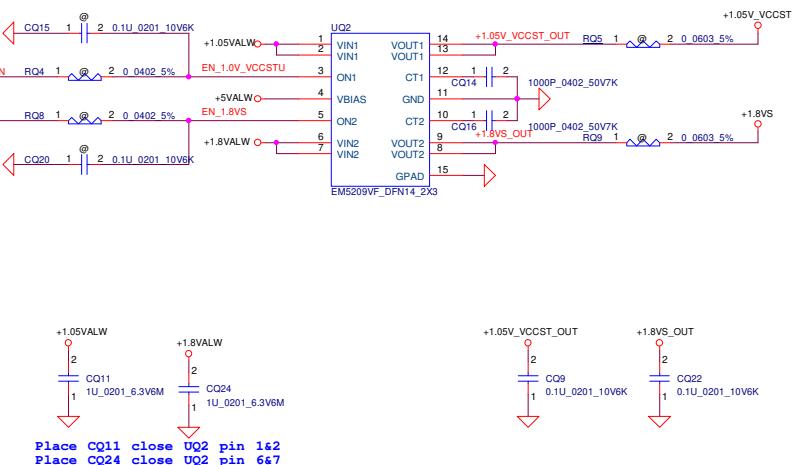
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# System DC interface

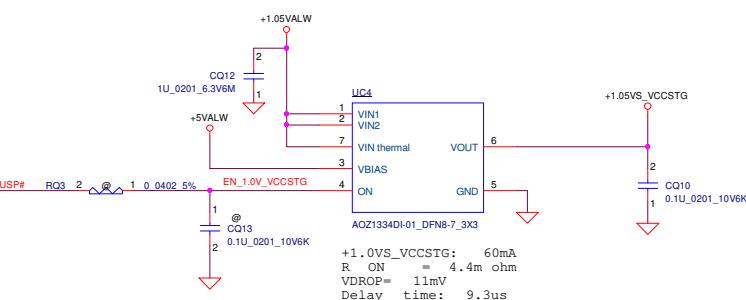
## For Power ON/Off Sequence



+1.05VALW TO +1.05V\_VCCST /+1.8VALW TO +1.8VS



+1.05VALW TO +1.05VS\_VCCSTG



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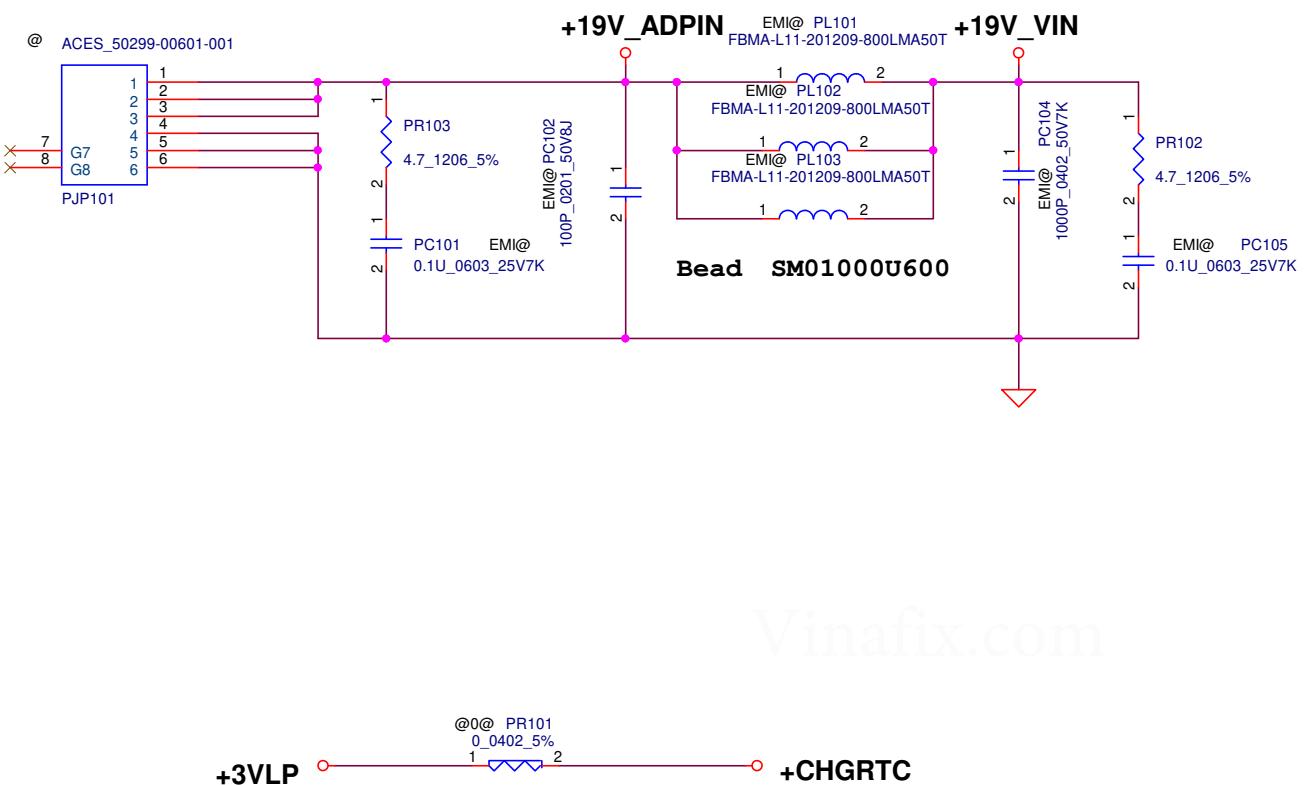
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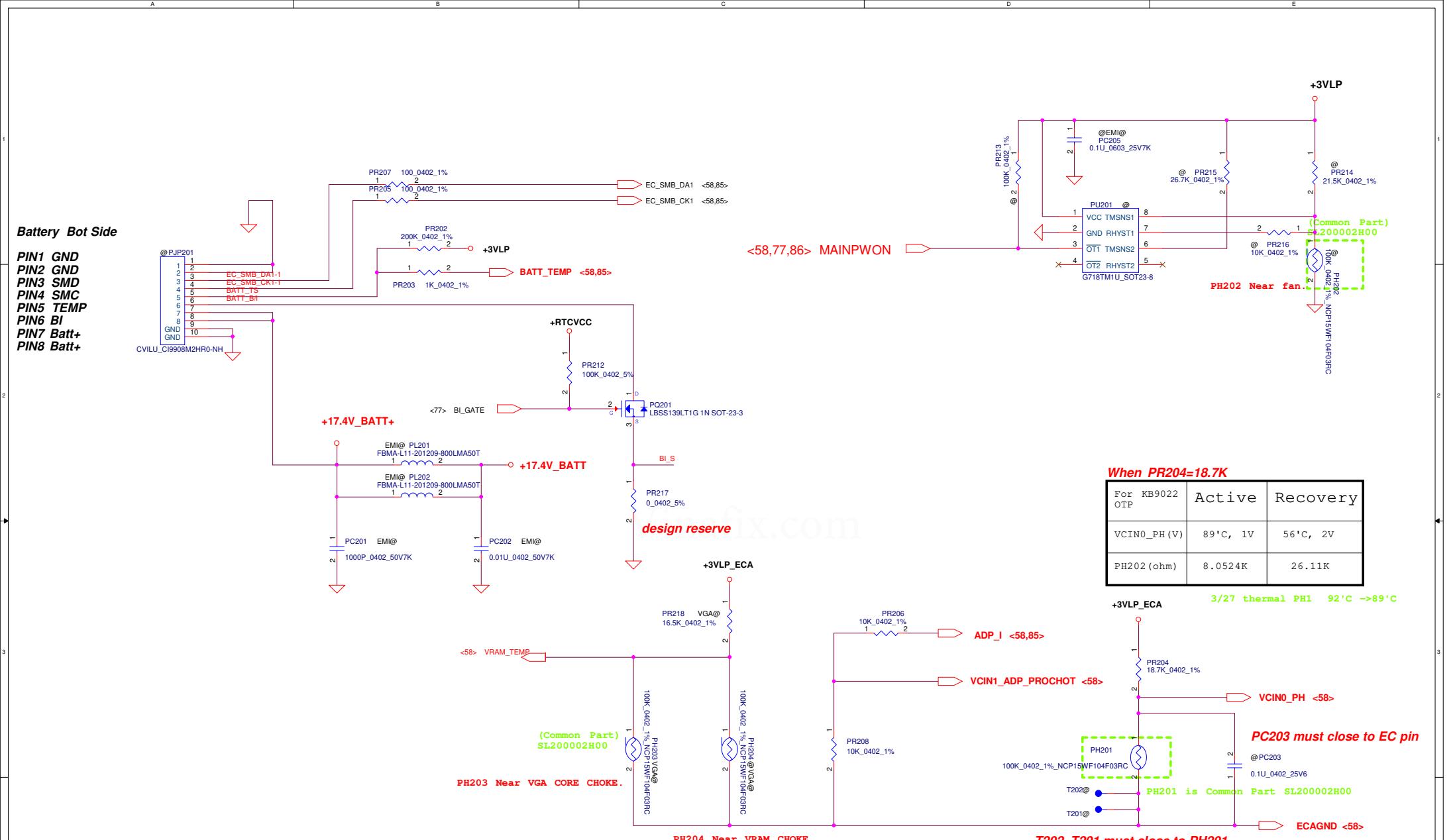
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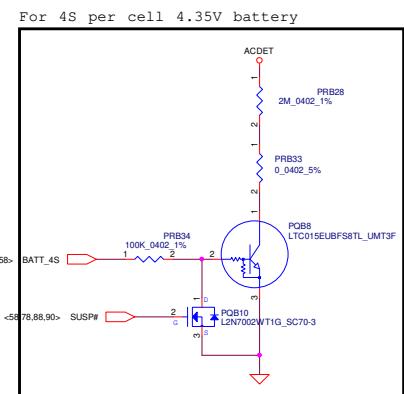
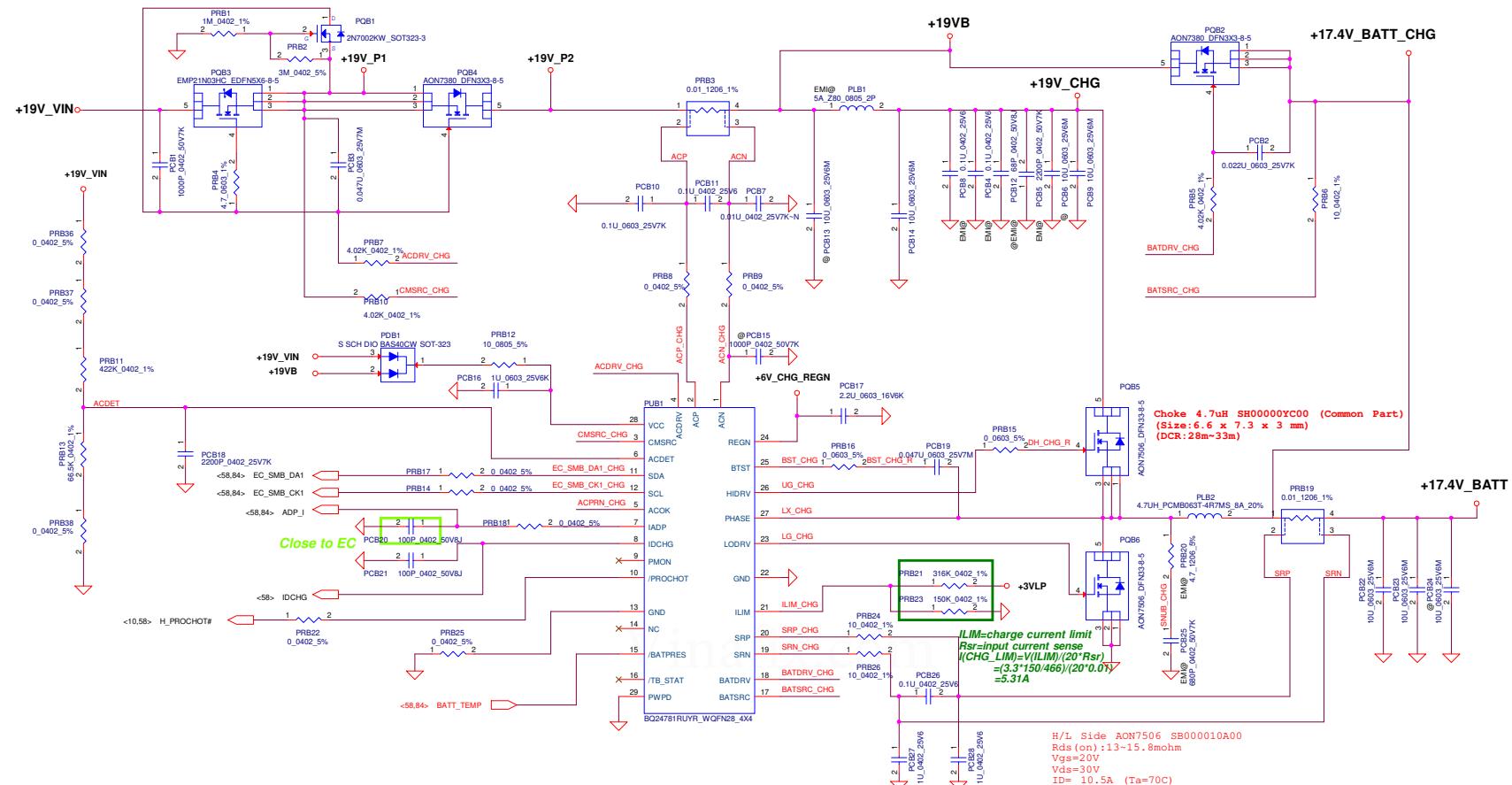
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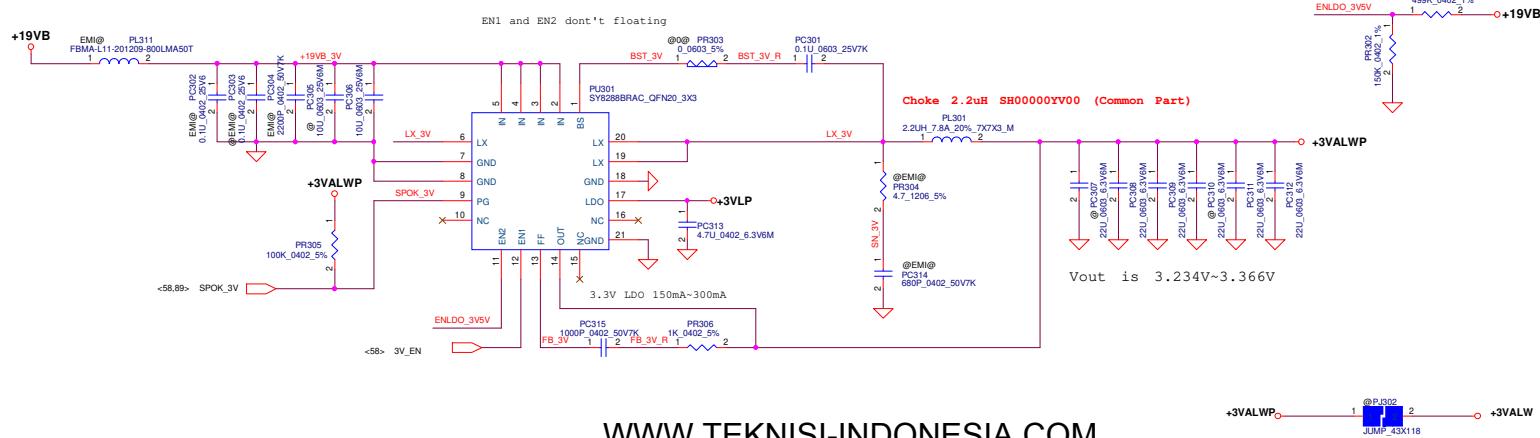
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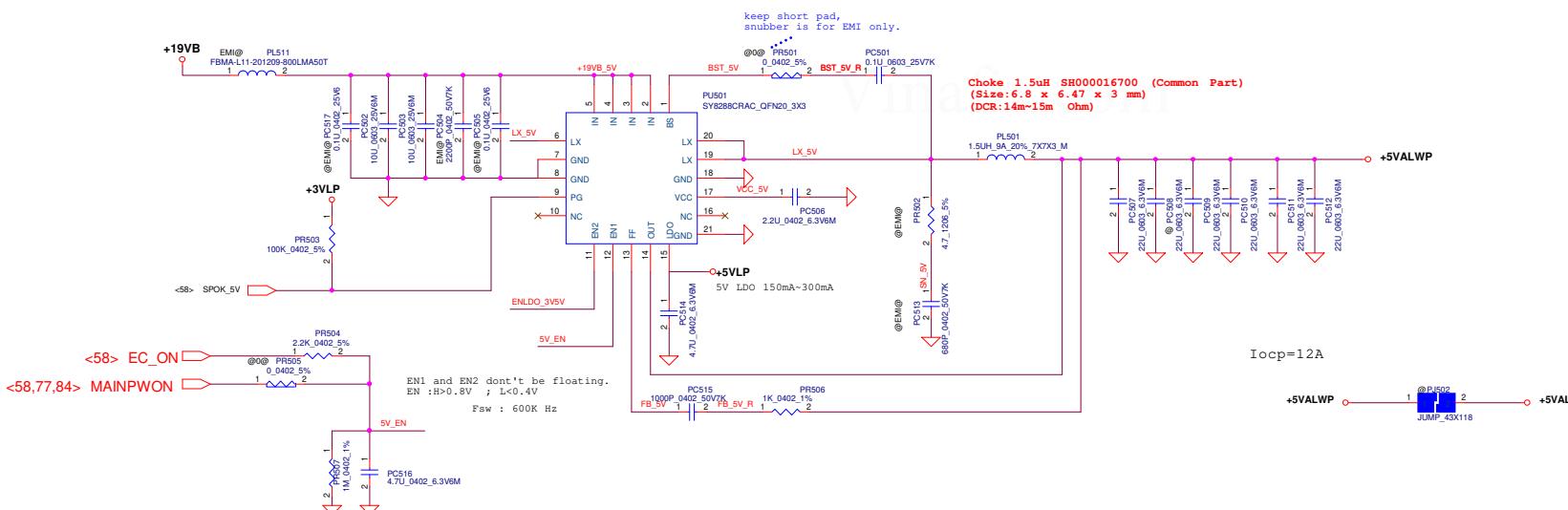
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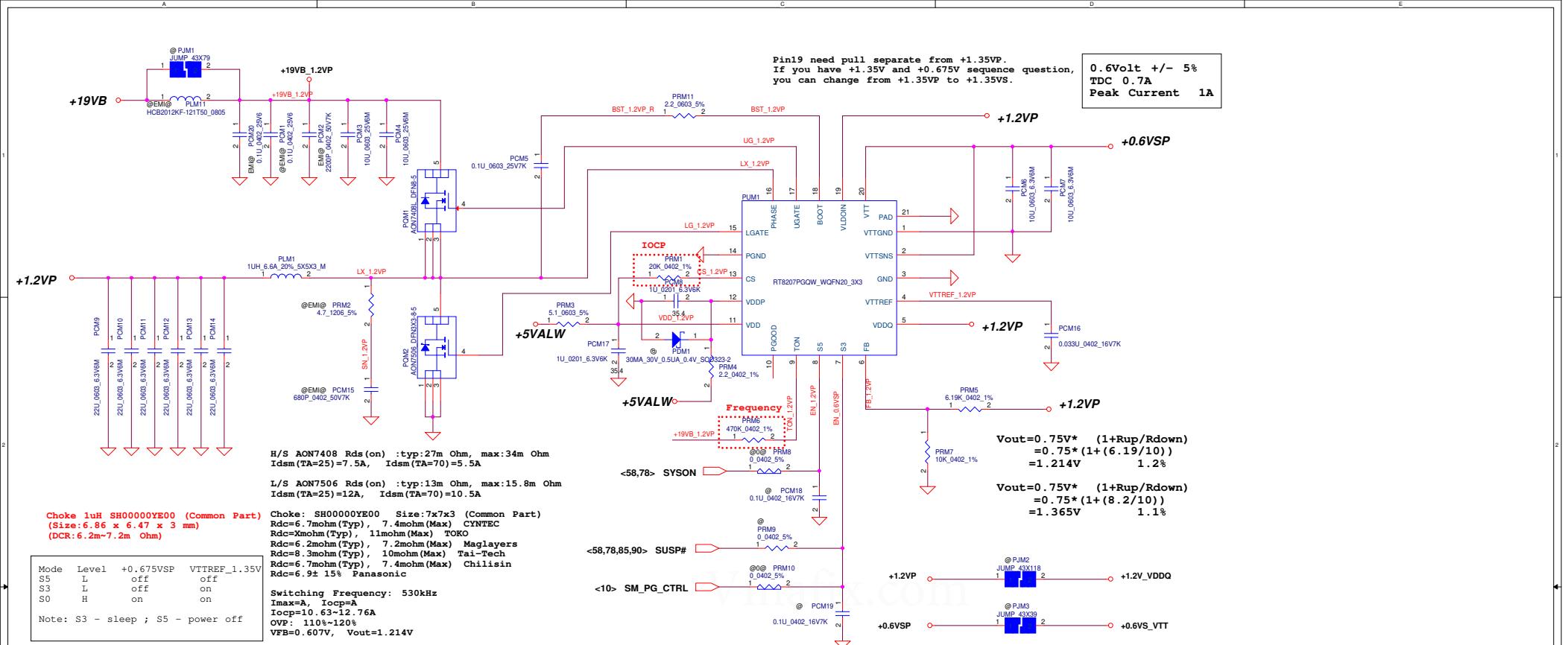


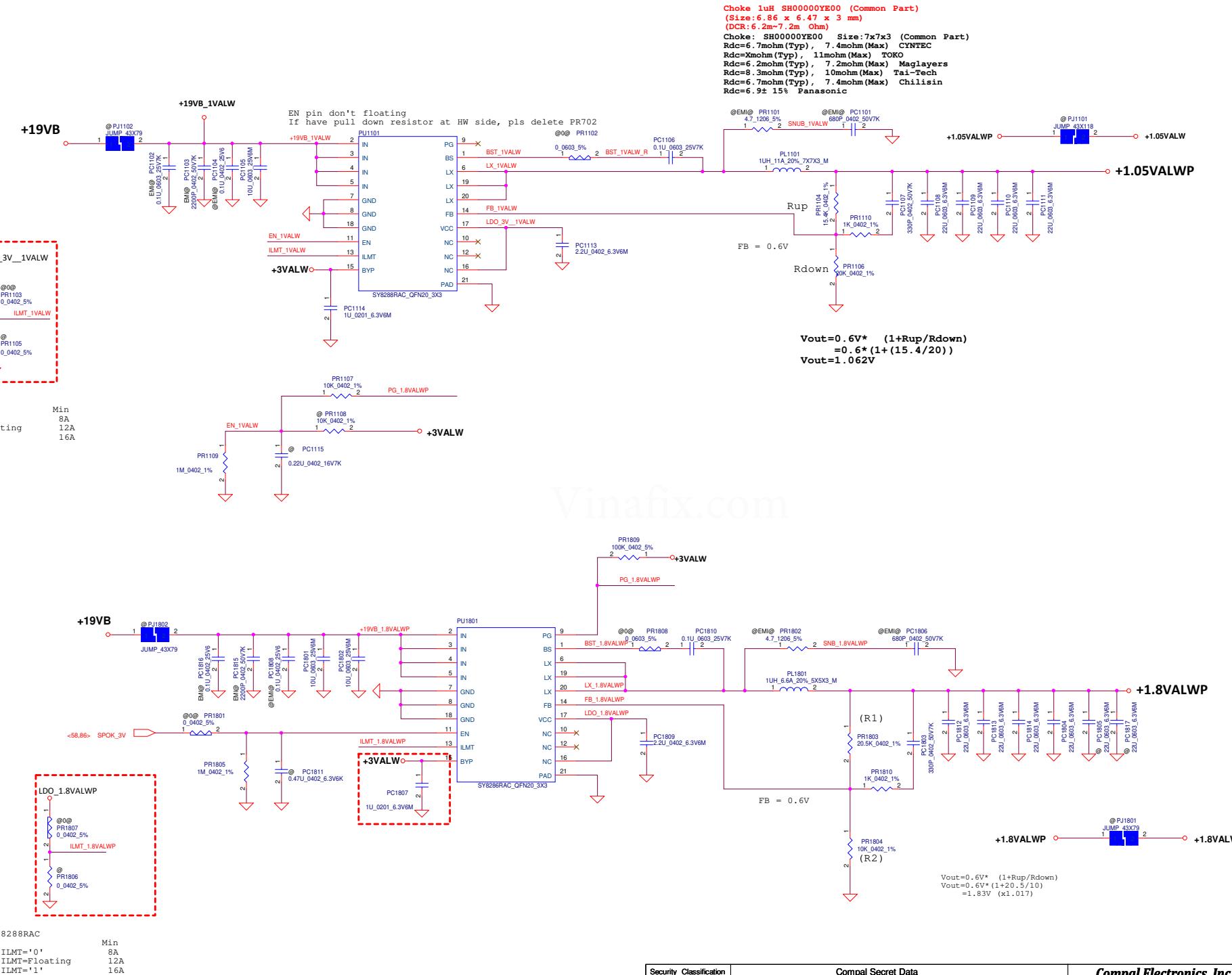
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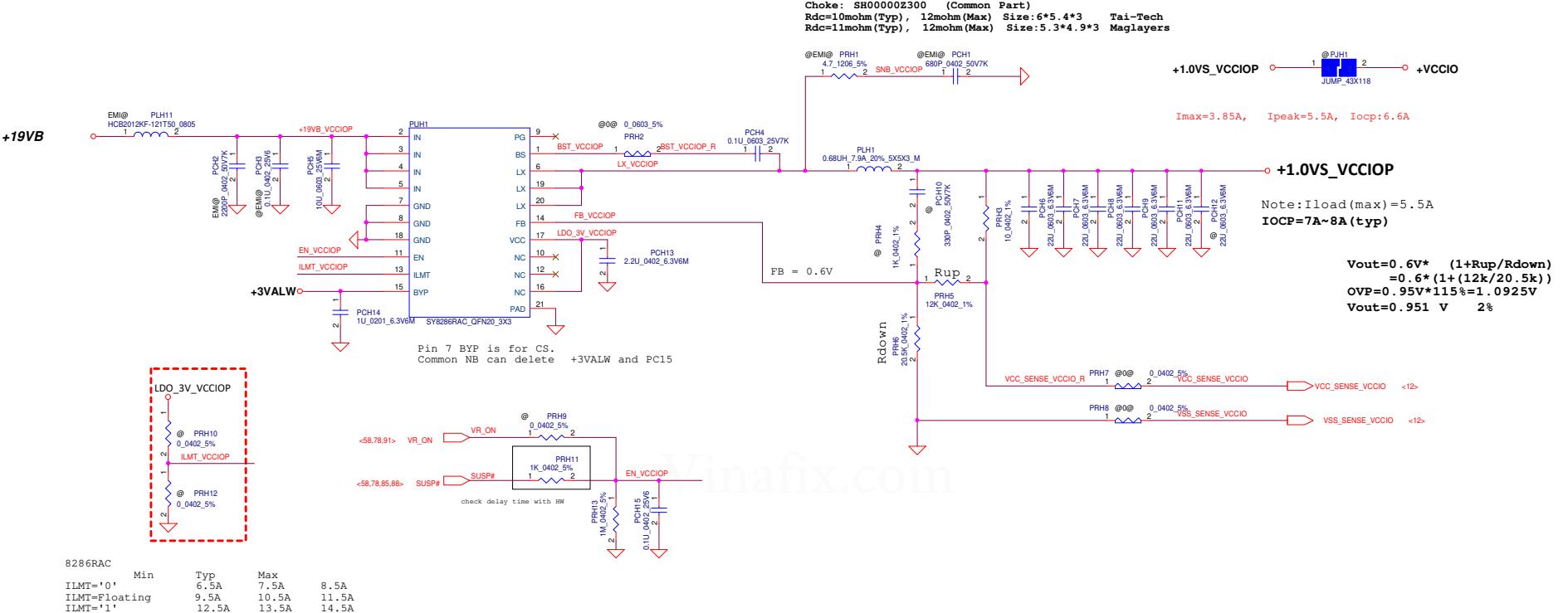
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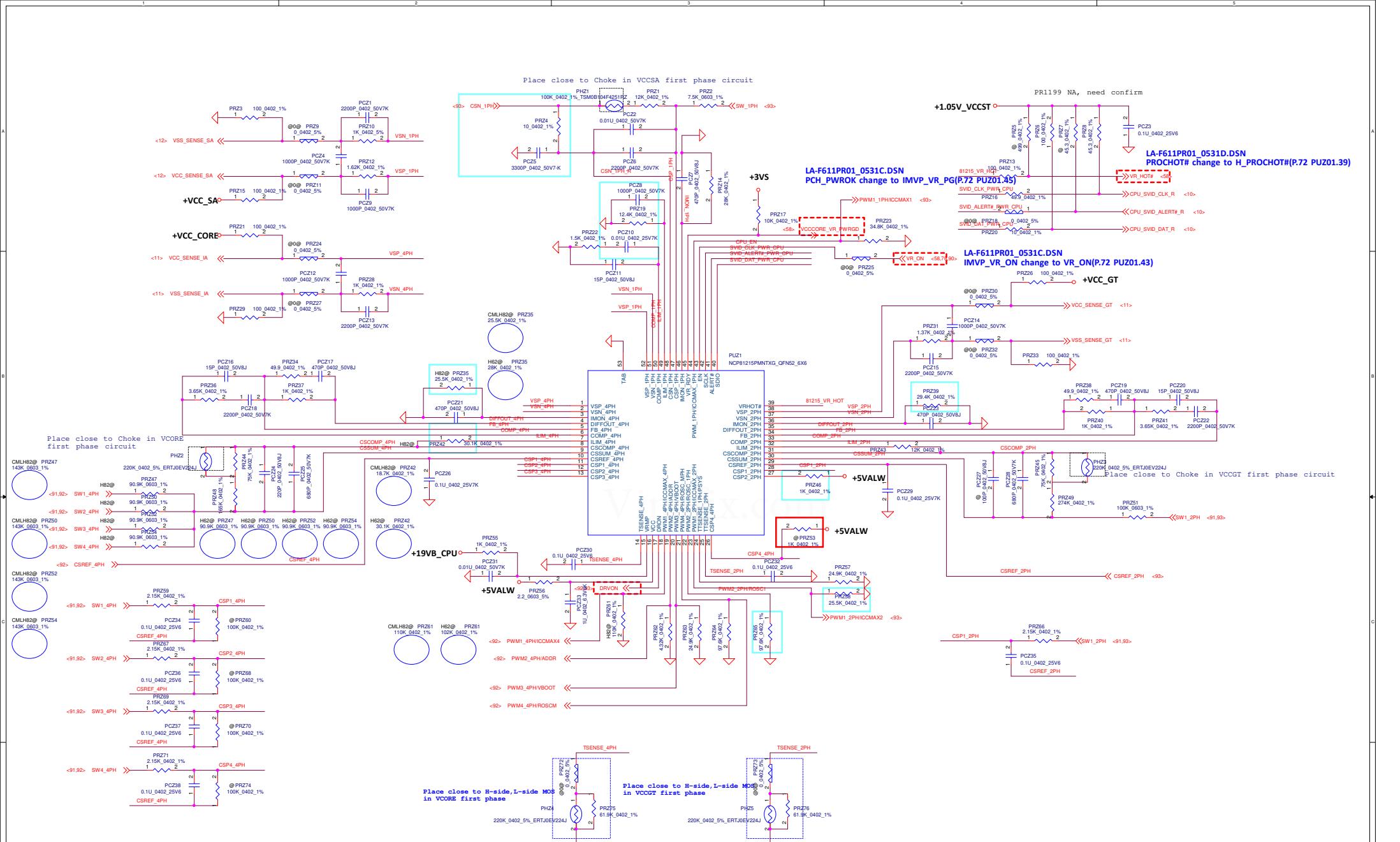
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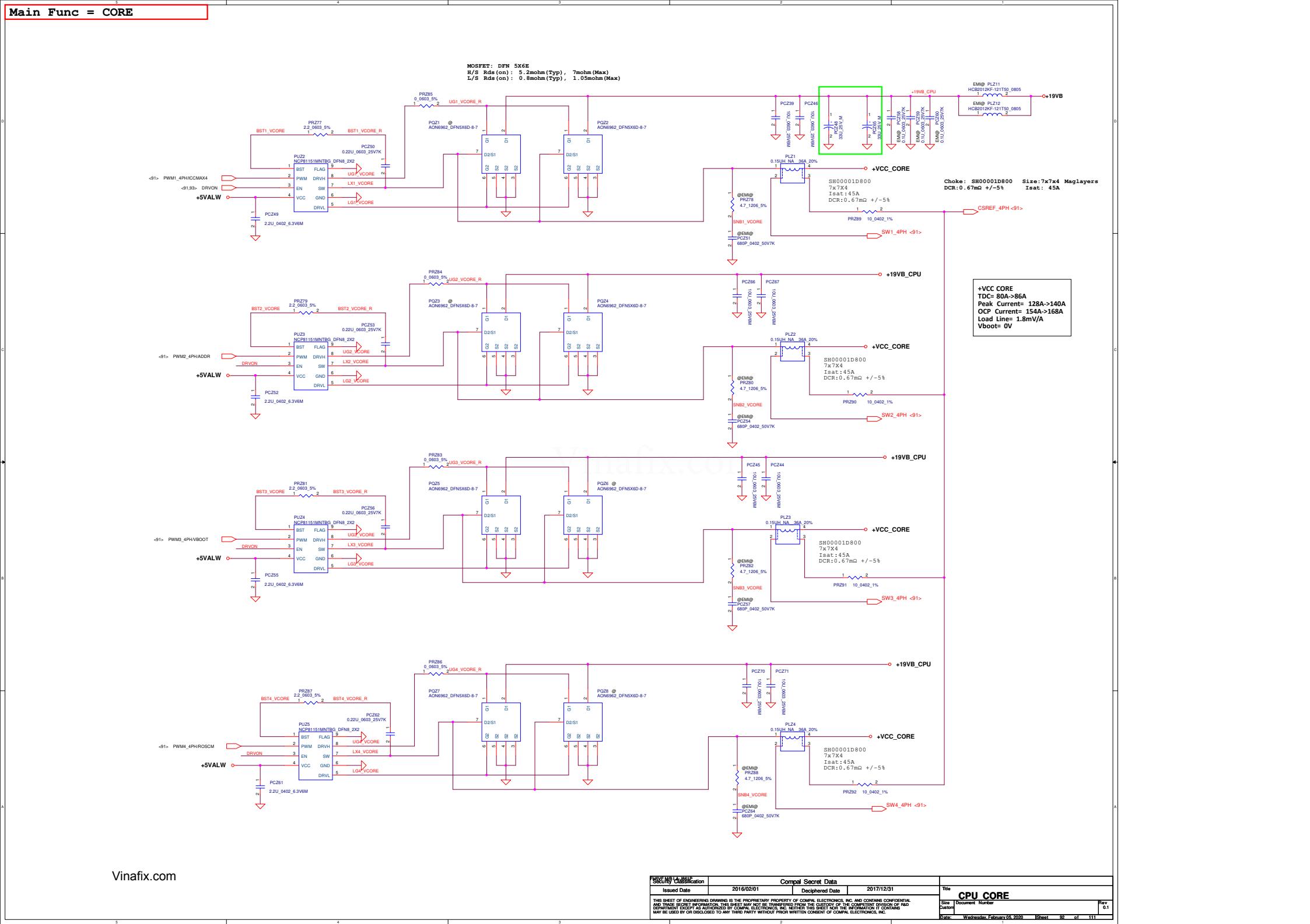


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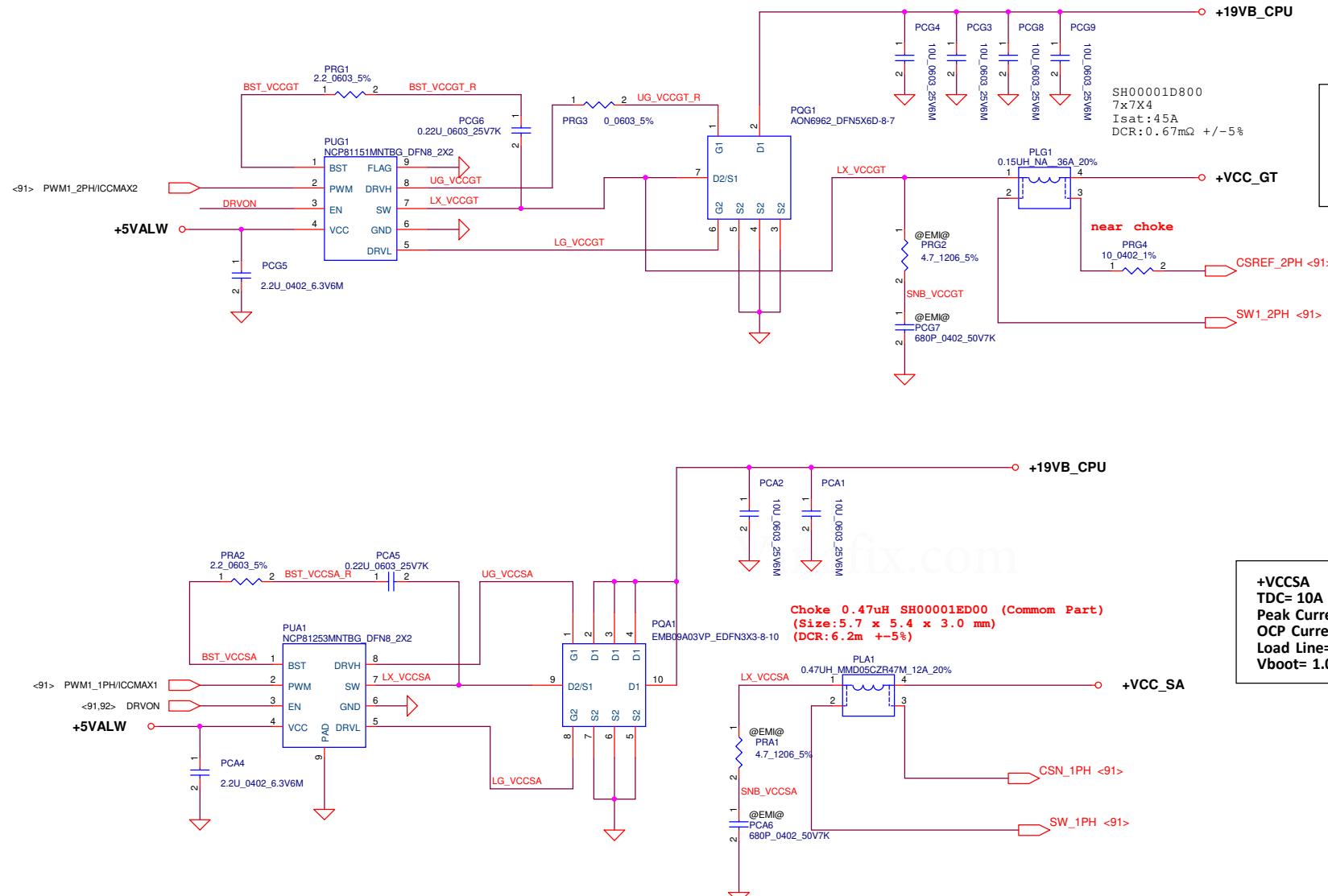




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Custom						<b>CPU IC</b>	<b>CFL_H 42</b>
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Main Func = VCCGT/+VCCSA



+VCCGT  
TDC= 25A  
Peak Current= 32A  
OCP Current= 39A  
Load Line= 2.7mV/A  
Vboot= 0V

+VCCSA  
TDC= 10A  
Peak Current = 11A  
OCP Current= 13A  
Load Line= 10.3mV/A  
Vboot= 1.05V

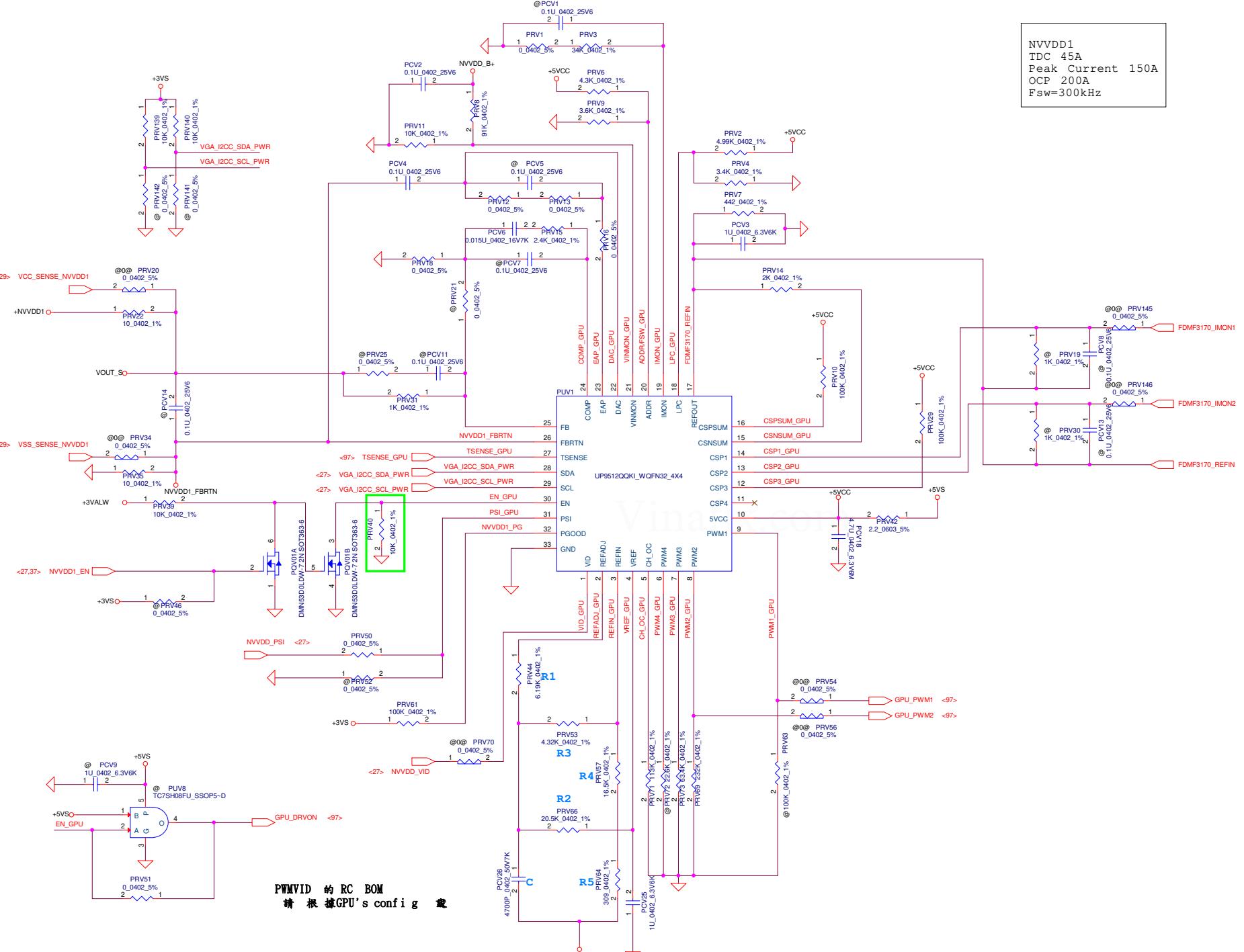
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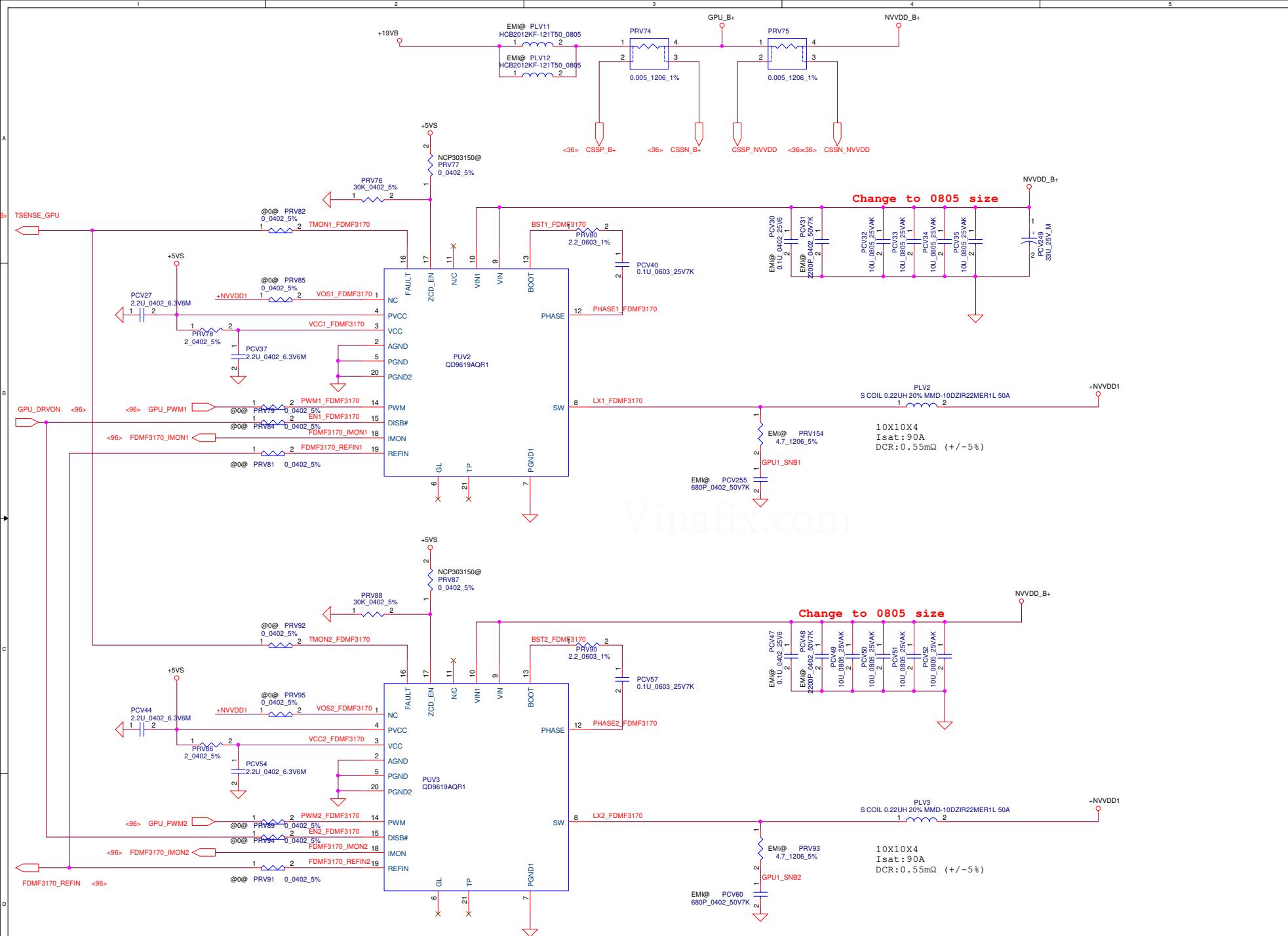
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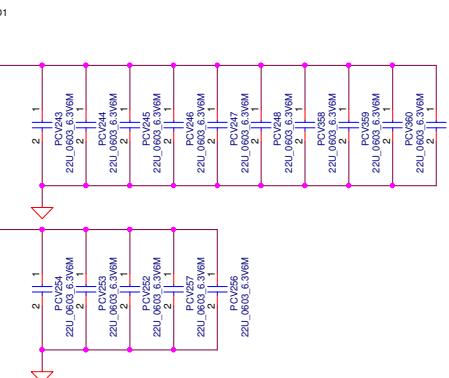
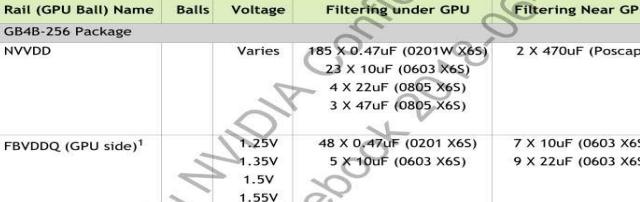
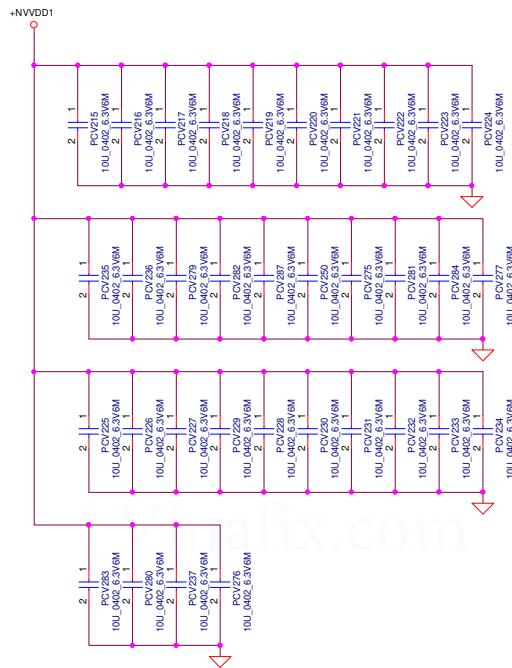
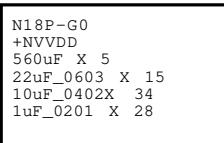
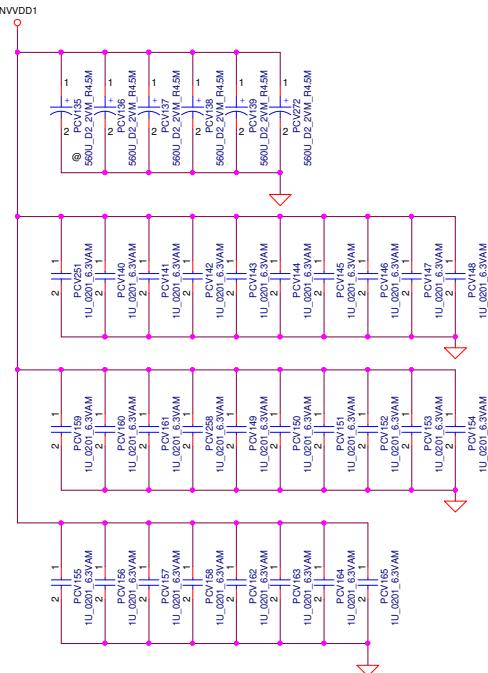
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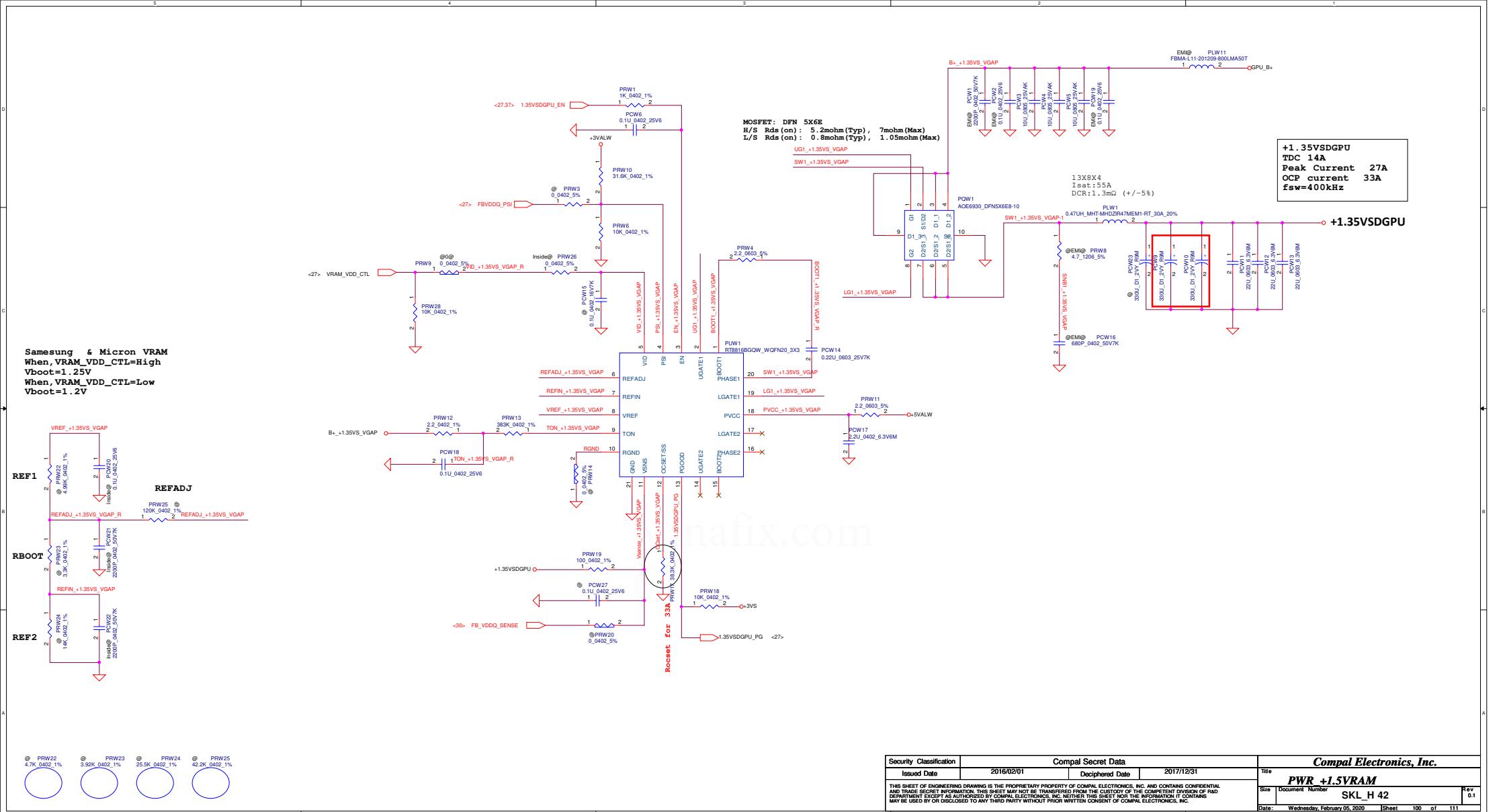
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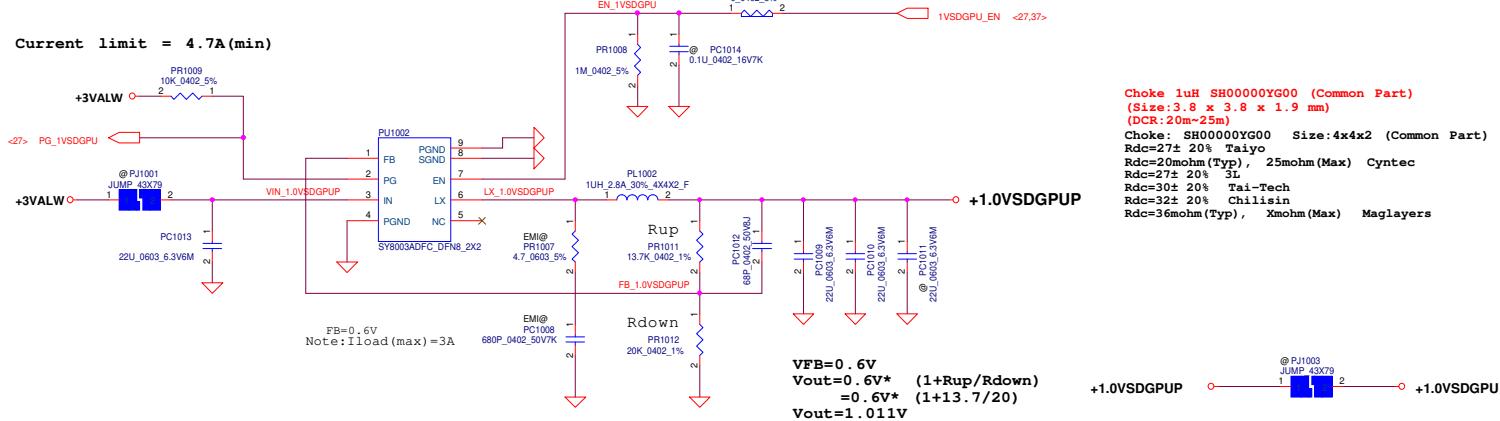
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Version  
change list  
(P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	PG#	Modify List	Date	Phase
01		Change P/N		Change PQM1 from SB00000OU10(S TR EMB20N03V 1N EDFN ET88) to SB00000H800(S TR AON7408L 1N DFN) Change PQM2 from SB00001HV00(S TR EMB12N03V 1N EDFN3X3-8) to SB000010A00(S TR AON7506 1N DFN)	11/13	DVT
02		Sourcer request		Change PRB12 from to SD011100A80(S RES 1/4W 10 +-5% 1206) to SD002100A80 (S RES 1/8W 10 +-5% 0805 )	11/13	DVT
03		Sourcer request		Change PCB17 from SE00000WP00(S CER CAP 2.2U 25V K X5R 0603) to SE000006S80 (S CER CAP 2.2U 16V K X5R 0603 )	11/13	DVT
04		Sourcer request		Change PCB20 from SE024101J80(S CER CAP 100P 50V J NPO 0603) to SE071101J80(S CER CAP 100P 50V J NPO 0402 )	11/13	DVT
05		Customer request		Add PCB21 SE071101J80(S CER CAP 100P 50V J NPO 0402 )	11/13	DVT
06		Sourcer request		Change PCB1 from SE025102K80(S CER CAP 1000P 50V K X7R 0603) to SE074102K80(S CER CAP 1000P 50V K X7R 0402 )	11/13	DVT
07		Sourcer request		Change PC102 SE071101J80(S CER CAP 100P 50V J NPO 0402) to SE00000SE00 (S CER CAP 100P 50V J NPO 0201 )	11/13	DVT
08		Vendor request		Change PUZ1 from SA0000AQE00(S IC NCP81215MNTXG QFN 52P PWM) to SA0000CTW00(S IC NCP81215PMNTXG QFN 52P PWM)	11/13	DVT
09		Base on CPU transient result		Change PCA103 & PCA108 to un-mount Change PCA109 & PCA111 to mount	12/02	DVT
10		Base on CPU transient result		CML H82 SKU delete PCZ104,PCZ105,PCZ107,PCZ108,PCZ111,PCZ113,PCZ114,PCZ116,PCZ118,PCZ120,PCZ123,PCZ124,PCZ126, PCZ127,PCZ134,PCZ135,PCZ136,PCZ137,PCZ138(22U_0603_6.3V6M * 19pcs)	12/02	DVT
11		Base on CPU transient result		CFL H62 SKU delete PCZ101(330U_D1_2VY_R9M)	12/02	DVT
12		For PQ310 protect		Add PRB36,PRB37,PRB38(0_0402_5%,SD028000080)	12/17	PVT

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Item Fixed Issue Reason for change

PG#

Modify List

Date Phase

01

02

03

04

05

06

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Item	Page	Title	Date	Issue Description	Solution Description	Phase	Rev.
D 01			11/13	Source request	1. Change CA26,CB5,CB6,CB9,CH9,CH51,CM16 from 0402 to 0201 size. 2. Change CG335,CG336,CS129,CS130 from SE082221J80 to SE074221K80. 3. Change DL1 to SCA00001A00. 4. Change CD10 from SE00000TBOO to SE00000SE00. 5. Change UH3 to SA0000BIP00. 6. Change UG28 to SA0000BJI00. 7. Change DS1,DS3,DS4,DS5,DS6,DS20 to SC300001Y00.	DVT	1.0
02	16,58	WLAN (BT_ON)	11/13	BT_ON co-lay by EC/PCH	1. Change TP_INT# connection to UH1.BC33. 2. Add RH26Z for BT_ON to UH1.BF32. 3. Add RB79 for BT_ON_R.	DVT	1.0
03	58	EC	11/20	Pin definition sync.	1. Remove Thermal_ALERT# net. 2. Change EC_PME# connection to UB1.106. 3. Add IDCH6 net to UB1.76. 4. Remove RB78 and TURBO_EN# net. 5. THERMAL1_ALERT# change connection to UB1.36. 6. TYPEC_EN change connection to UB1.68. 7. LAN_PWR_EN change connection to UB1.91. 8. Change RB3 to 750k for EC board ID.	DVT	1.0
04	15,52	CNVI	11/20	by intel review.	1. Change RM36,RM37,RH181,RH182 from 0402 to 0201 size. 2. Add RM51,RM52 for CNVI topology.	DVT	1.0
05			12/17	Design change.	1. Change RM46,RL2,R18 to R-short.	PVT	1A
06	58	EC	12/17	EC board ID.	1. Pop RB3.	PVT	1A
07	63	TP	12/24	ESD request.	1. Add CK6.	PVT	1A

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