ARN33 AMD Rembrandt-H

Title	Cover Page	LCFC
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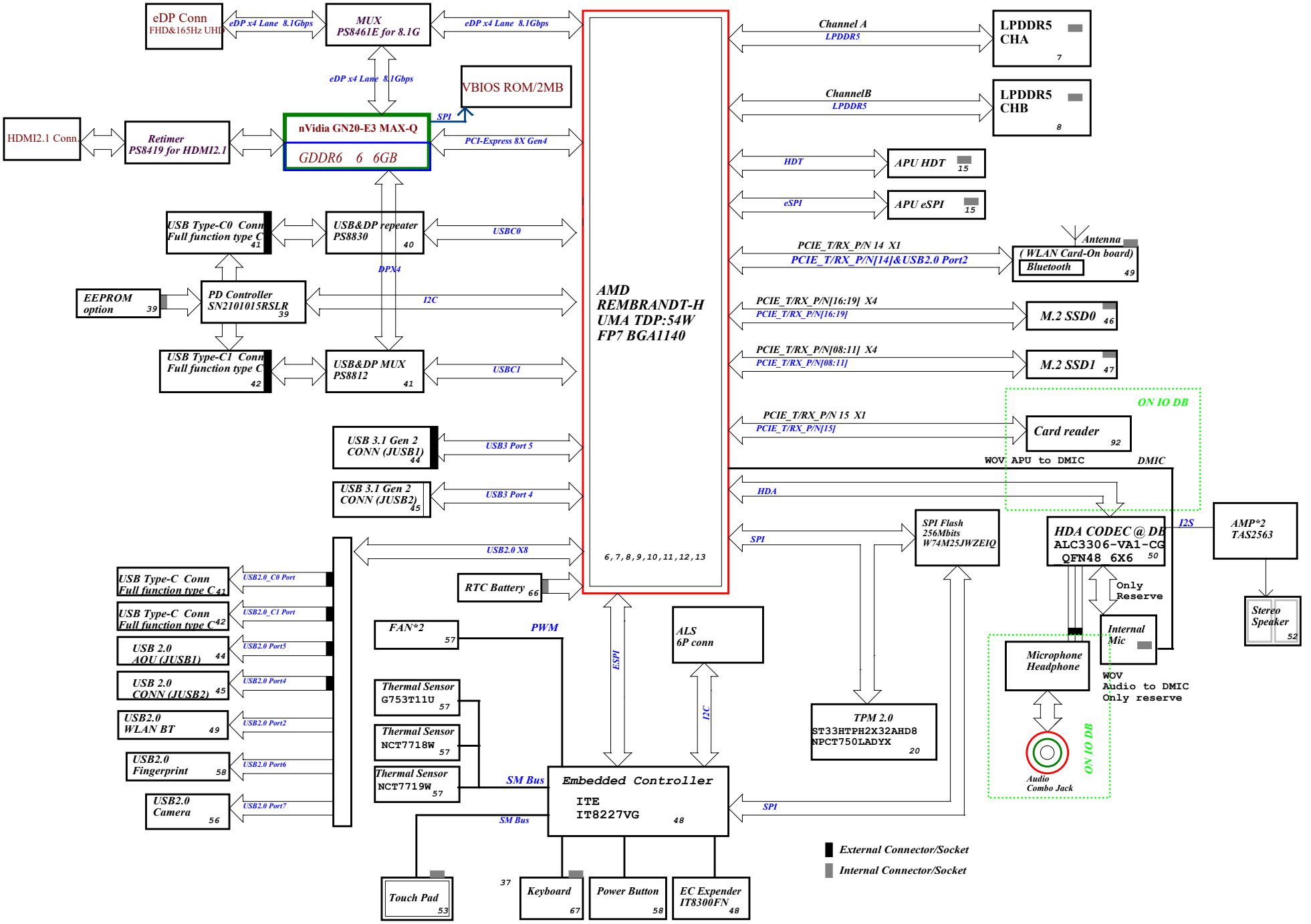

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Title	Block Diagram_PWR	LCFC	
Size C	Document Number ARN35 AMD Rembrandt-H		Rev 1
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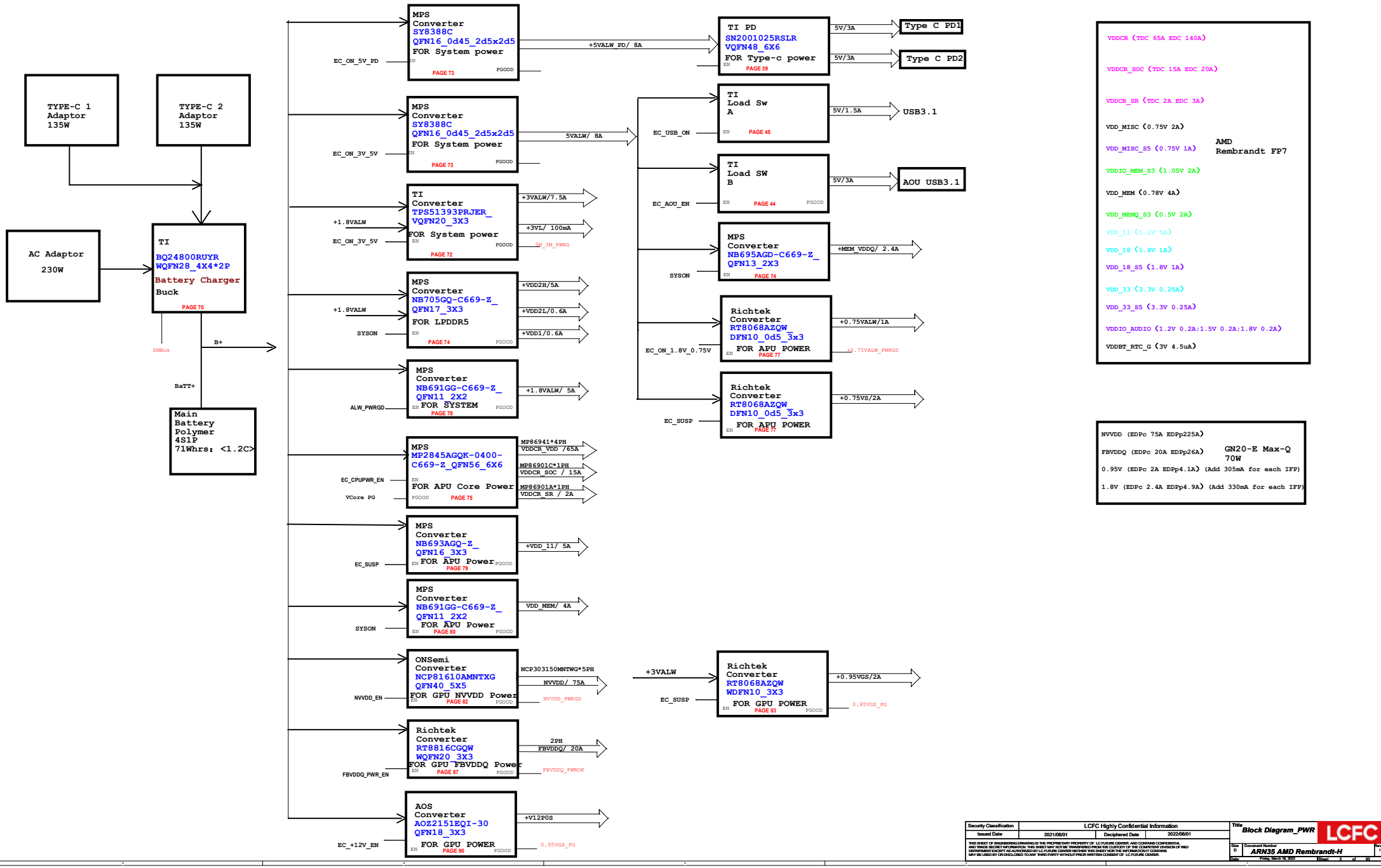

Title: Block Diagram_PWR
LCFC
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PD I2C address table

Port	Master	Slave	End Port	Address	Description
I2C_EC	EC	PD	PORTA	0x23	ADCIN1=0.18032 #3 ; ADCIN2=1 #7 ADCIN1 decoded value = 3 ADCIN2 decoded value = 7 I2C address index = #4 A port: 0100011 B port: 0100111
			PORTB	0x27	
I2C2S	APU	PD	PORTA	0x23	Confirm with Max
			PORTB	0x27	
I2C3M	PD	APU	USBC0	0x54	The USB PD I2C Slave responds to a 7-bit address.
			USBC1	0x58	
	PD	EEPROM	EEPROM	0x50	
	PD	Redriver-C0	Redriver-C0	PS8812: GPIO mode	For PS8828:I2C slave Address [ADDR1,ADDR0]=[GPIO1,GPIO0] LL:0X10~0X23 LH:0X30~0X43 HL:0X50~0X63 HH:0X90~0XD3 For PS8830:[GPIO1,GPIO0] LL:0x10; LH:0x20; HL:0x30; HH:0X40;
		Redriver-C1	Redriver-C1	PS8828:0X90 PS8830:0X40	

APU I2C address table

Port	Master	Slave	End Port	Address	Description
I2C0	APU	PD	PORTA	0x23	Confirm with Max
			PORTB	0x27	
	APU	ALS	ALS	0x44	SY3079AS22-J01
I2C1	APU	T_PANEL	T_PANEL	0x10 ELAN	
I2C2	APU	Touch_PAD	Touch_PAD	0x15 0x2c	SB974A-22H0 I2C device address: 0x15 TM-P3652 I2C device address: 0x2C
I2C3 (SMBUS)	APU	TYPEC0 REDRIVE	TYPEC	PS8812:0XD0	
	APU	TYPEC1 REDRIVE	TYPEC	PS8828:0X90~0XD3 PS8830:0X40	
	APU	AMPR1	AMPR1	0X4F	TAS2563 I2C/SMBUSTM address is 0x4F(7-bit) connected NDD
	APU	AMPR2	AMPR1	0X4E	TAS2563 I2C/SMBUSTM address is 0x4E(7-bit) pull down 10K to GND

APU HSIO table

AMD Rembrandt HS I/O port assignment

Port#	FP7 Rembrandt	16P GEN3	Notes
1	DP0	EDP Panel	
2	DP1	NA	
3	USBC0/DP2/USB3_0	Type-C Port0	USB4.0
4	USBC1/DP3/USB3_1	Type-C Port1	USB3.2
5	USBC4/DP4/USB3_4	Type-A Port0	USB3.2
6	USB3_5	Type-A Port1	USB3.2
7	USB2_0	Type-C Port0	
8	USB2_1	Type-C Port1	
9	USB2_2	M.2 BT	
10	USB2_3	NA	
11	USB2_4	Type-A Port0	
12	USB2_5	Type-A Port1	
13	USB2_6	Frigerprint	
14	USB2_7	CAMERA	
1	PCIE0~PCIE7	GPU	
9	PCIE8	SSD1	GEN4
10	PCIE9		
11	PCIE10/SATA1		
12	PCIE11/SATA0		
13	PCIE12	NA	
14	PCIE13	NA	
15	PCIE14	WLAN	GEN3
16	PCIE15	SD Card	GEN1
17	PCIE16	SSD0	GEN4
18	PCIE17		
19	PCIE18		
20	PCIE19		

EC I2C address table

Port	Master	Slave	End Port	Address	Description
SMCLK0 SMDAT0	EC	VRM	VRM	0x20	To support multiple VR devices used with the same PMBusTM interface, PMBusTM address programming either by ADDR
	EC	CHARGER	CHARGER	0x12	The device performs only as a SMBus slave device with address 0b00010010 (0x12H) and does not initiate communication on the bus.
	EC	Battery	Battery	0x16	Confirm with changxia
	EC	TS 1	TS 1	0x4D	NCT7719W I2C/SMBUSTM address is 1001_101xb
	EC	TS 2	TS 2	0x4C	NCT7718W I2C/ SMBusTM address is 1001100xb
SMCLK1 SMDAT1	EC	PD	PD	N/A	Refer to PD table
	EC	TYPEA Port Debug	TYPEA		
SMCLK2 SMDAT2	EC	HDMI	HDMI	0x80h / 0x81h	PS8409A
	EC	APU	APU Thermal	0x98	confirm with dingyanlong
	EC	ALS	ALS	0x44	SY3079AS22-J01

SMCLK3
SMDAT3

Title: Map/SMBUS/HSIO

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+3VALW_PCH	+1.2V	+5VS +3VS VCCIO VCCSA VCCSTG VCCCPUCORE VCCGFXCORE +1.8VS_AON +1.8VGS NVVDD +1.0VGS FBVDDQ
S0	O	O	O	O	O
S3	O	O	O	O	X
S3 Battery only	O	O	O	O	X
S5 S4/AC Only	O	O	O	X	X
S5 S4 Battery only	O	X	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

POWER X76

ZZZ GPU_ONX76@ — ON_GPU_PWRCTRL — X764G312009

ZZZ FBV_RTX76@ — RICHTEK_FBVDDQ — X764G31200B

ZZZ OVRM_ONX76@ — ON_OVRM — X764G31200D

USB4@ ZZZ — S IC PS8828ABGA105GTR-A2 USB 3.2 RETIMER — X764G31200H

DII_AOU@ UU12 — S IC PS8828ABGA105GTR-A2 USB 3.2 RETIMER — SA0000BPE00

VRAM X76

ZZZ VRAM_SAMX76@ — MICRON 32Gb — X764G312001

GPU FBVDDQ IC

PU4001 UP1666@ — UP1666QQKF WQFN 20P — SA00008G000

DRAM X76

ZZZ1 X76M4GB@ — MICRON 32Gb — X764G312007

ZZZ6 X765BGB@ — MICRON 64Gb — X764G312008

PCB

MainBD_PCB@ — PCBJY630 NM-E661 REV0 M/B — DAZ2KZ00100

GPU

UG1 GPU@ — S IC GN20-E3-A1 FCBGA 2714 GPU MP 12 — SA000BBKU10

CPU

UC1 R5_PR@ — S IC AMD FP7 R5-xx00H PC — SA0000CS940

UC1 R7_PR@ — S IC AMD FP7 R7-xx00H PC — SA0000CS840

UC1 R9_PR@ — S IC AMD FP7 R9-xx00H PC — SA0000CS830

USB2.0 Port table	
Port	Function
0	USB-C0
1	USB-C1
2	FP
3	NC
4	USB3.0 PA
5	USB3.0 PB(AOU)
6	BT
7	CAMERA

USB3.0 Port table	
Port	Function
USBC0	Type-C port 0
USB1	Type-C port 1
USBC4	USB3.0 PA
USB5	USB3.0 PB(AOU)

SATA Port table	
Port	Function
0	NA
1	NA

PCIE Port table	
Port	Function
0-7	GPU
8-11	M.2 SSD1
14	SD
15	WLAN
16-19	M.2 SSD0

BOM Structure Control Table

BOM Structure	BTO Item
@	Not stuff
2.5K_165Hz@	165Hz Panel
2.5K_60Hz@	60Hz Panel
81611@	ONS GPU CORE IC NCP81611
ALS@	ALS function
AOU_Cellwise@	Cellwise CHG IC
AOU_Pericom@	Pericom CHG IC
AOU_TI@	TI CHG IC
QD9619@	QD9619 GPU CORE DrMOS
CAMERA@	For Camera Function
DDS@	For DDS Function
Debug@	For debug Function
Debug_NS@	For non-debug Function
EDP@	For EDP Function
EE_Noise@	For EE Noise Function
EMC@	EMC Part
EMC_NS@	EMC Part no stuff
GEN2_ON@	ONS OVR_M IC
GEN2_UPI@	UPI OVR_M IC
GPU@	GPU IC
H32Gb@	LPDDR5 Hynix 32Gbit IC
H32GbX4@	LPDDR5 Hynix 32Gbit of X76
H64Gb@	LPDDR5 Hynix 64Gbit IC
H64GbX4@	LPDDR5 Hynix 64Gbit of X76

BOM Structure	BTO Item
HDMI@	HDMI part
HDT@	HDT Debug Header
HVRAM@	Hynix VRAM GDDR6
OVP_Kinetic@	CC OVP Kinetic IC
M32Gb@	LPDDR5 Micron 32Gbit IC
M32GbX4@	LPDDR5 Micron 32Gbit of X76
M64Gb@	LPDDR5 Micron 64Gbit IC
M64GbX4@	LPDDR5 Micron 64Gbit of X76
ME@	ME part
MIC@	MIC Part
MS@	Modern standby part
MUX@	Display MUX part
NCP303152@	GPU CORE DrMOS ONS IC stuff
Non_EE_Noise	EE_Noise no stuff,colay with EE noise part
Non_SMT	RTC Battery with cable,SMT no stuff
NPI@	NPI part
OPT@	GPU part
OPT_NS@	GPU part nostuff
OVP_TI@	CC OVP TI IC
PCB@	For PCB part
PS8828@	For PS8828 part stuff
PS8830@	For PS8830 part stuff
PS8830_NS@	For PS8830 part nostuff

BOM Structure	BTO Item
R5_ES@	R5 ES sample CPU
R5_PC@	R5 PC sample CPU
R7_PC@	R7 PC sample CPU
R9_ES@	R9 ES sample CPU
R9_PC@	R9 PC sample CPU
RF_NEW@	RF part
RF_NS@	RF part nostuff
RT8816@	FBVDDQ power RT8816 part stuff
S32Gb@	LPDDR5 Samsung 32Gbit IC
S32GbX4@	LPDDR5 Samsung 32Gbit of X76
S64Gb@	LPDDR5 Samsung 64Gbit IC
S64GbX4@	LPDDR5 Samsung 64Gbit of X76
SVRAM@	Samsung VRAM GDDR6
TPM@	TPM part stuff
UART@	UART part stuff
UP1666@	FBVDDQ power UP1666 part stuff
up9512@	GPU CORE IC UP9512 part stuff
up9512_NS@	GPU CORE IC UP9512 part unstuff
GEN2_ON@	ON OVRM IC NCP45495 part stuff
GEN2_UPI@	UPI OVRM IC US5651 part number

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Title: Notes_For BOM

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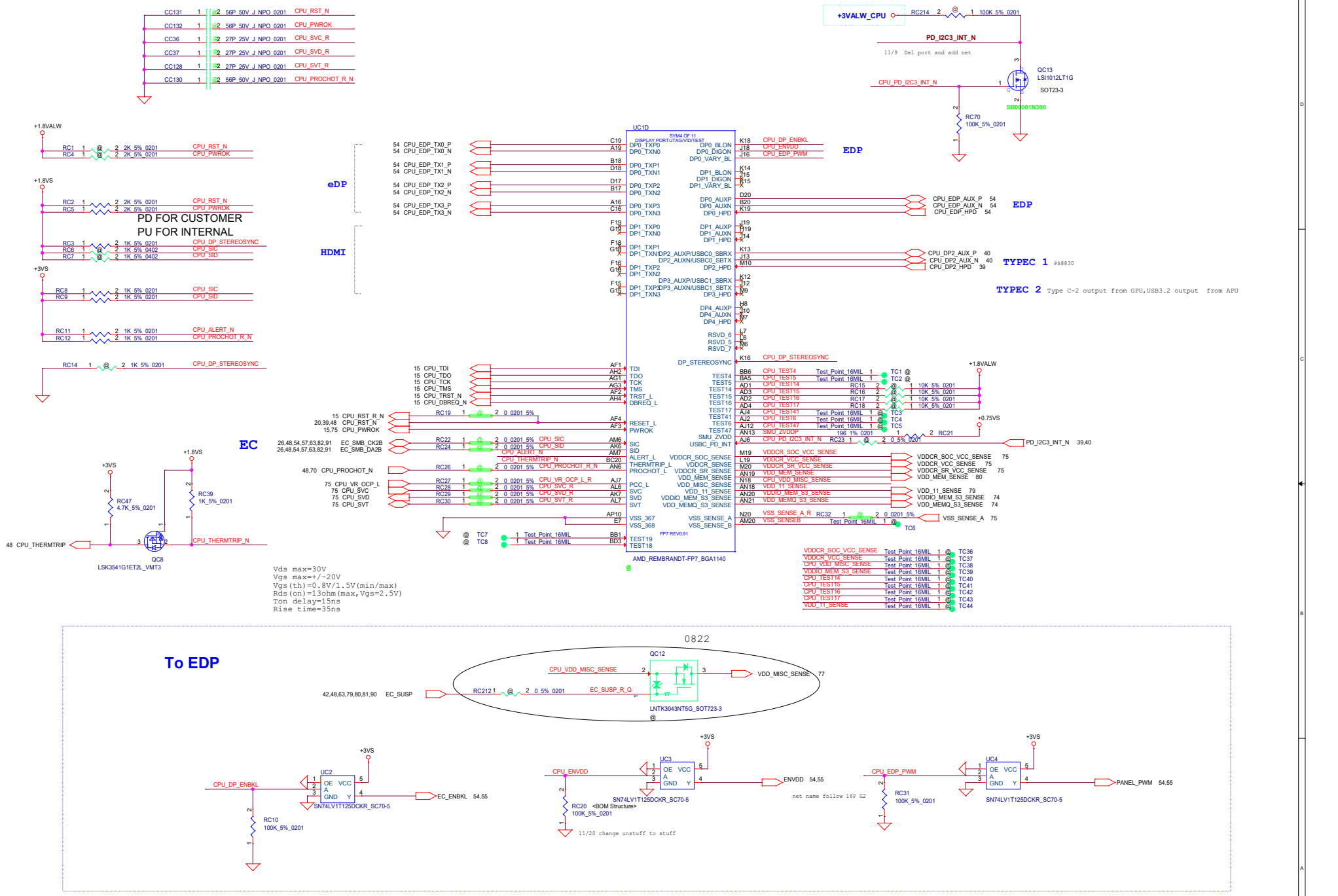

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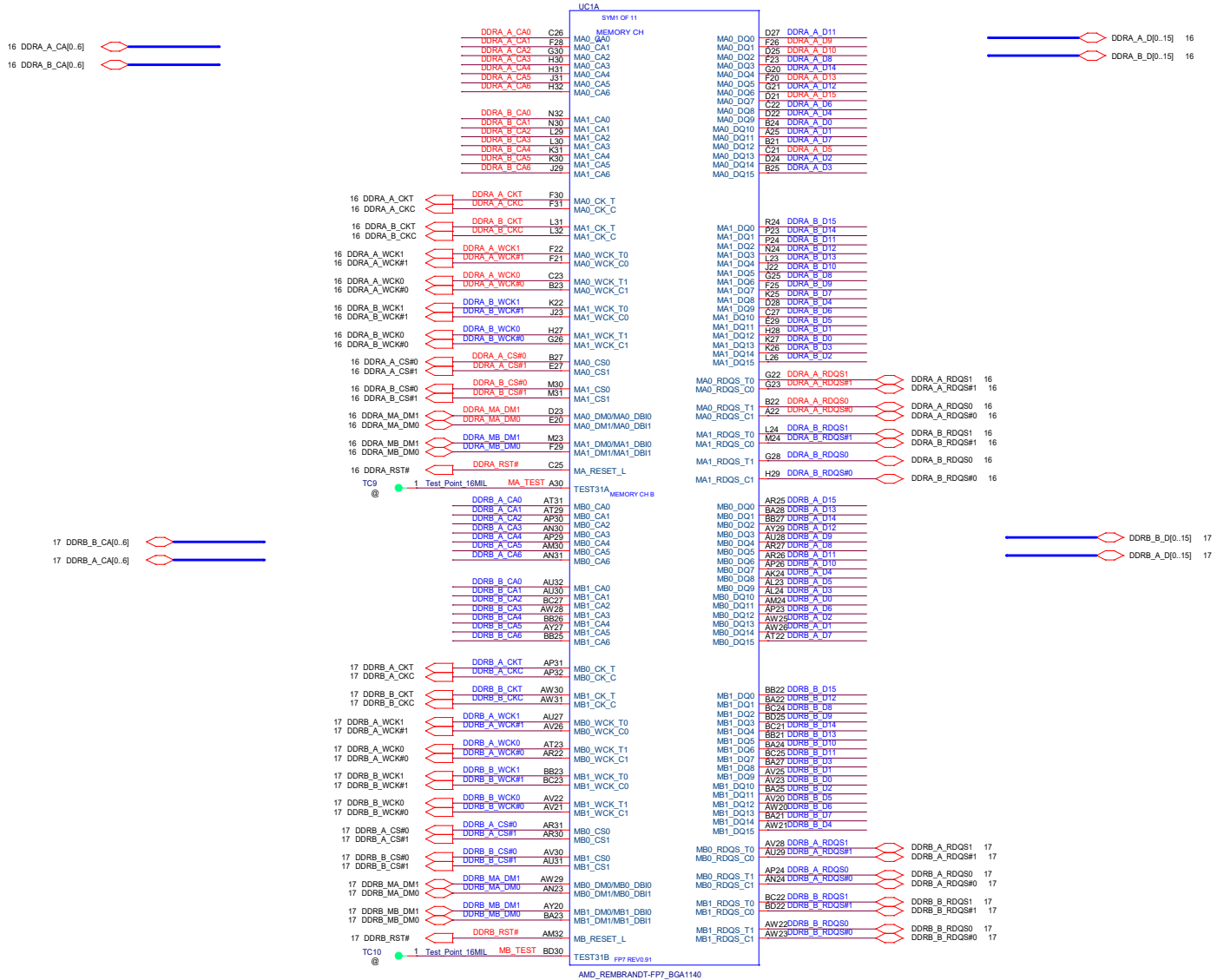

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Title: LPDDR5-CHA

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Title: LPDDR5-CHB

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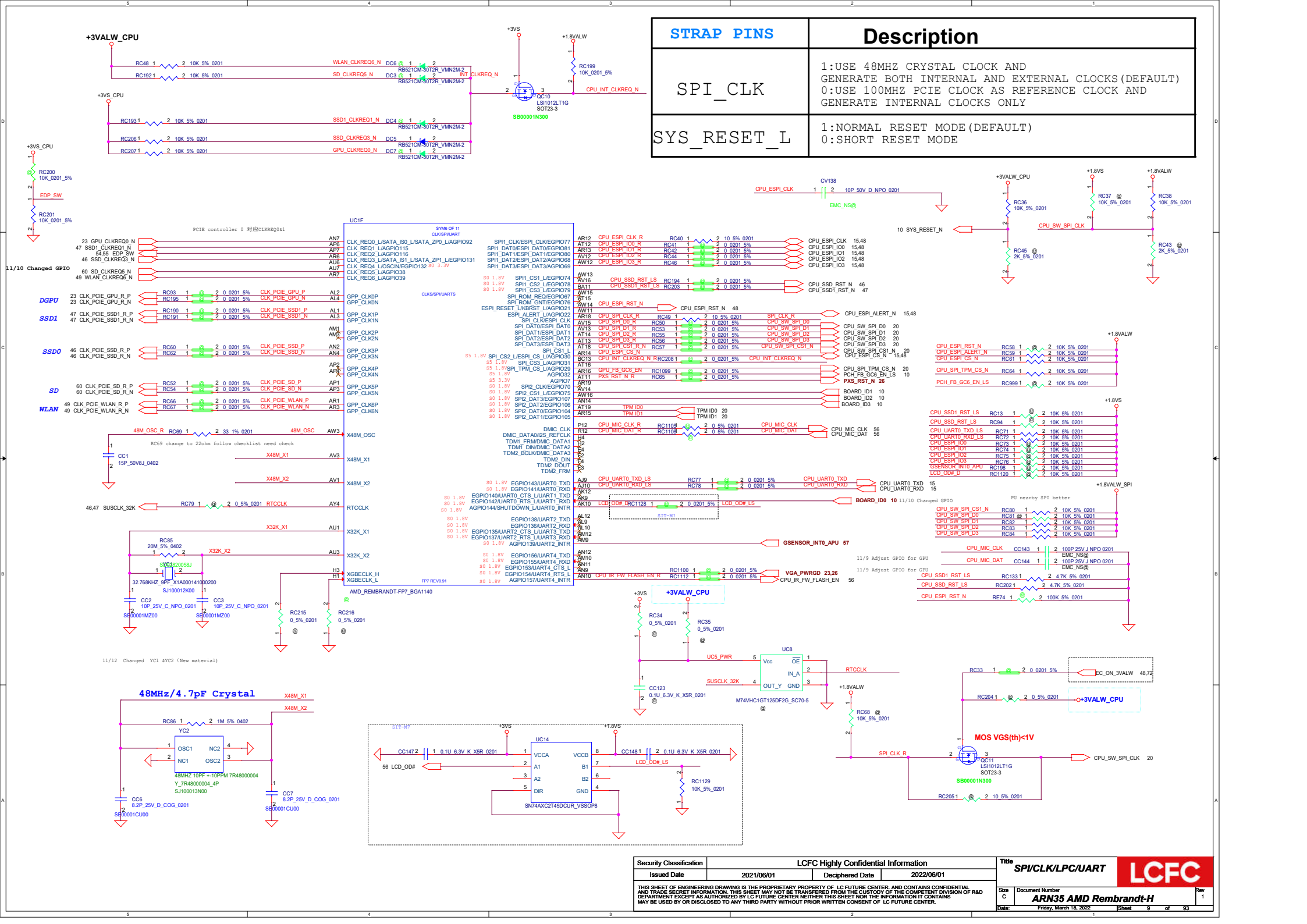
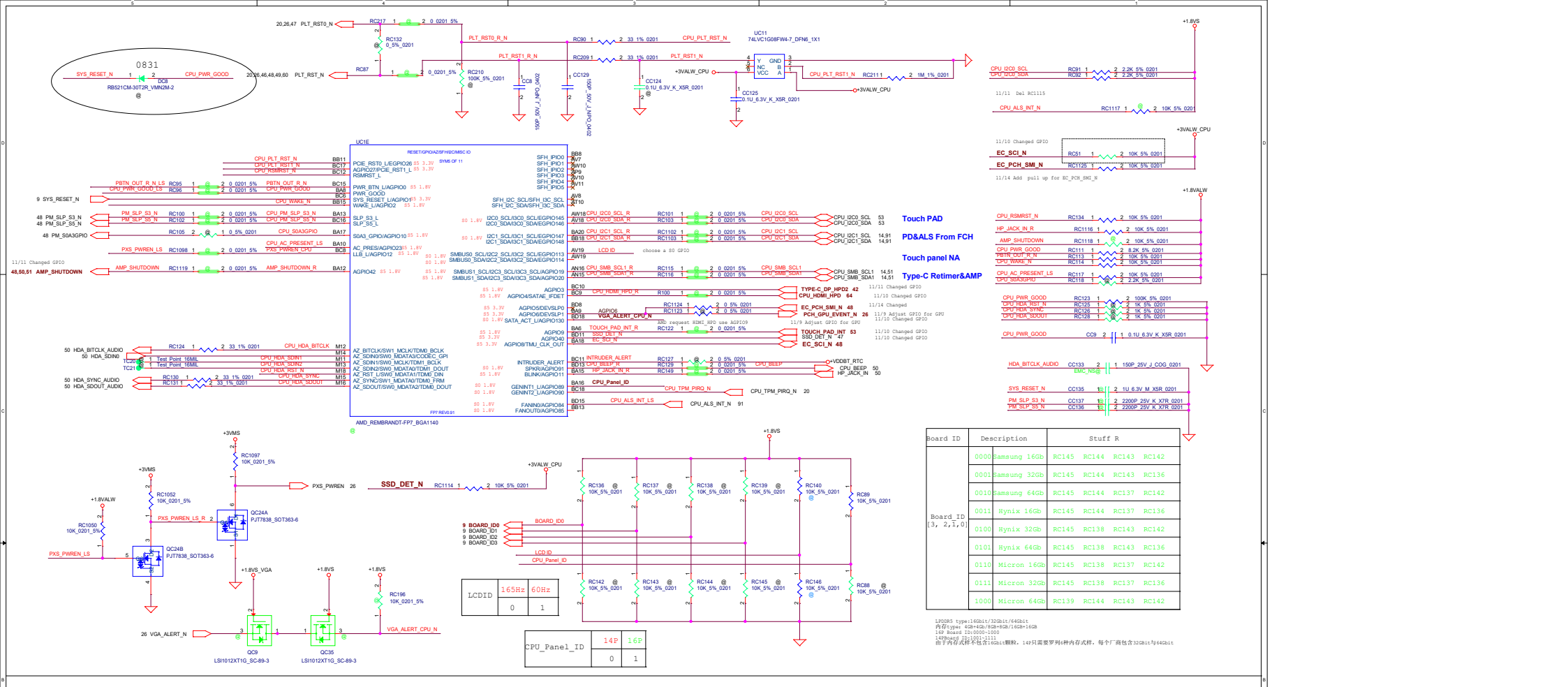
STRAP PINS	Description
SPI_CLK	1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RESET_L	1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE





CPU Level Shift

reversed EC 1.8V GPIO by OD setting,UC6/UC13 will cost down

EVT verify cost down

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Title: I2C/HDA/GPIO

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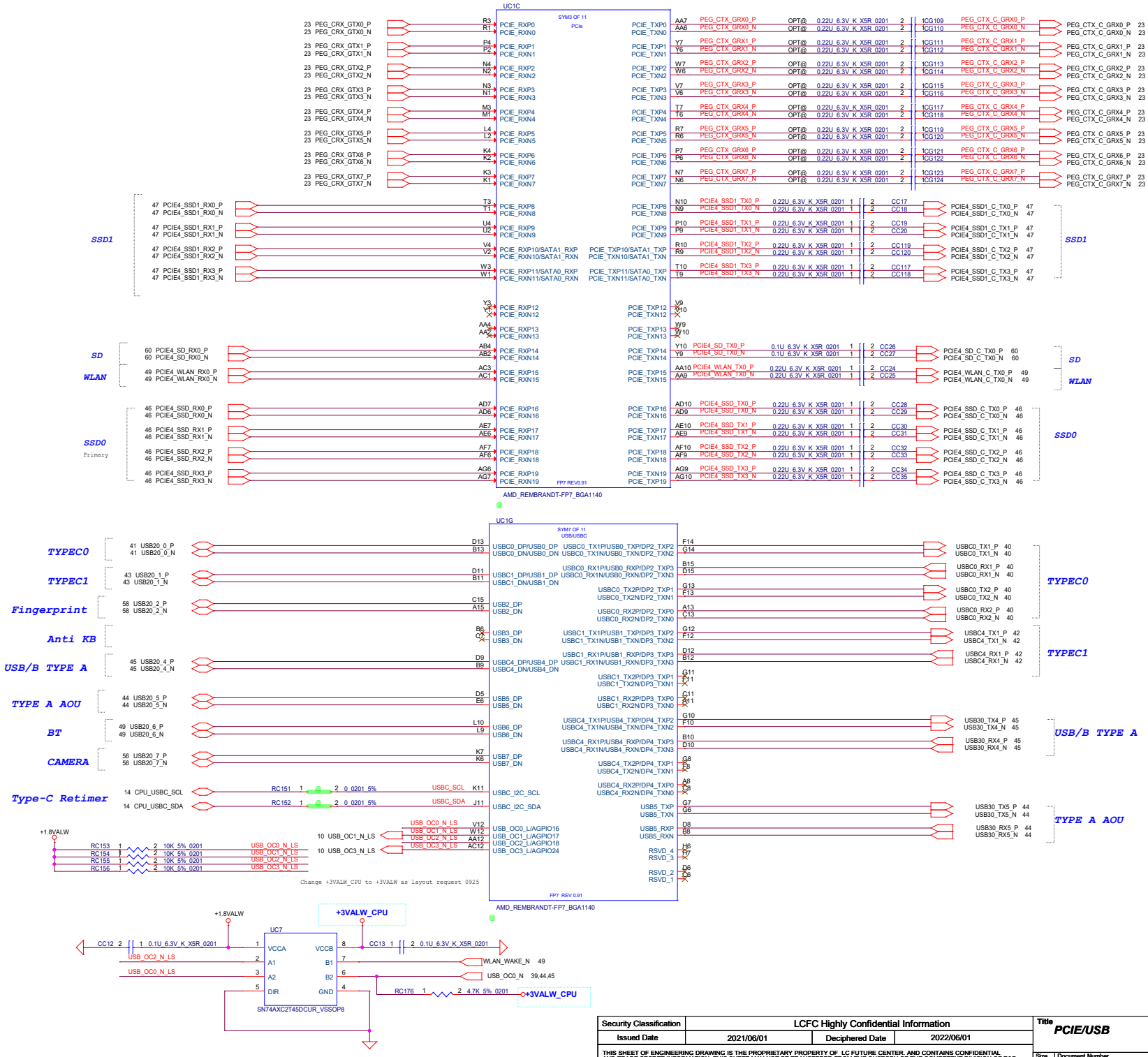

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Title	PCIE/USB		
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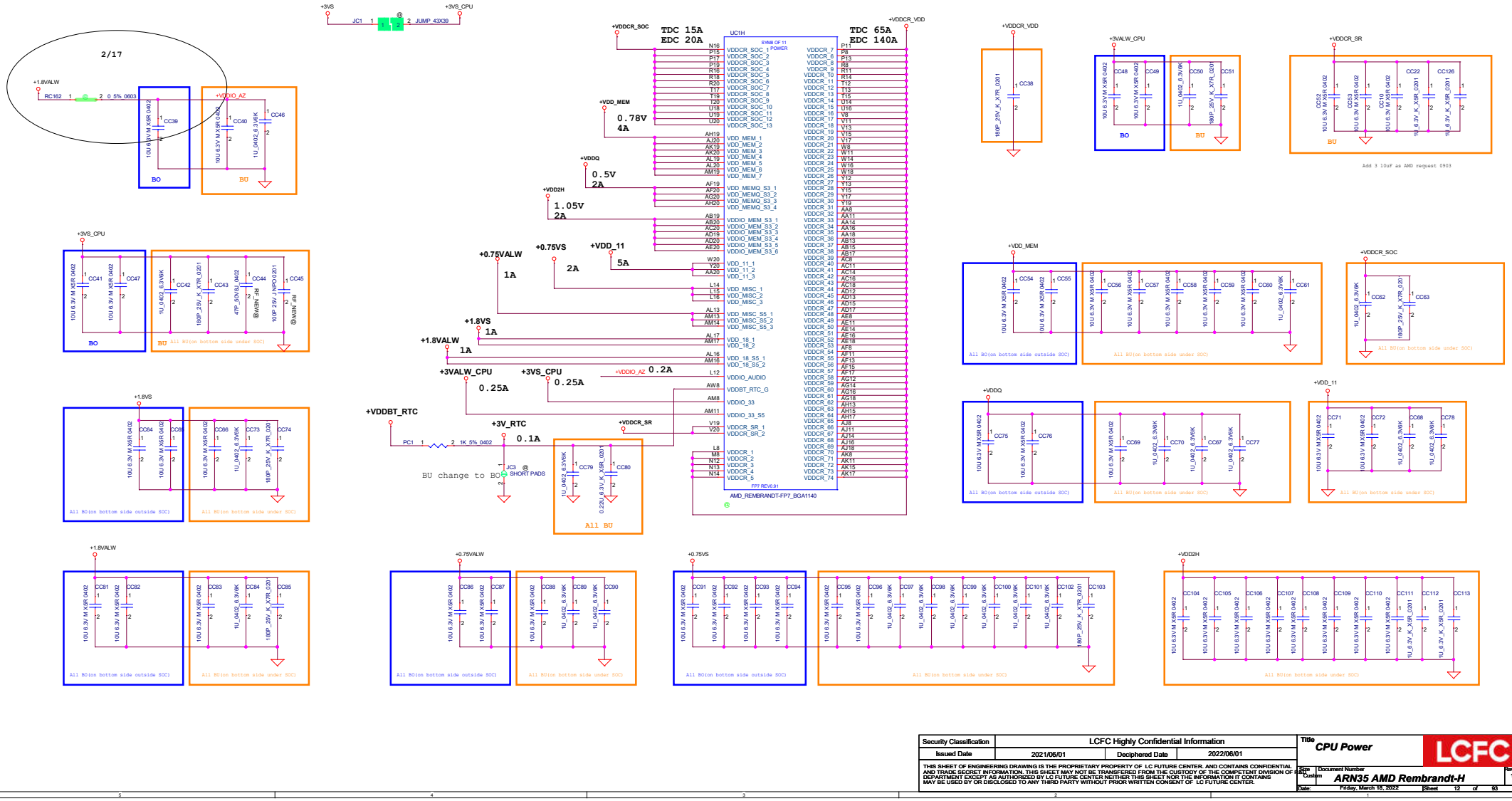

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Title: **CPU Power**

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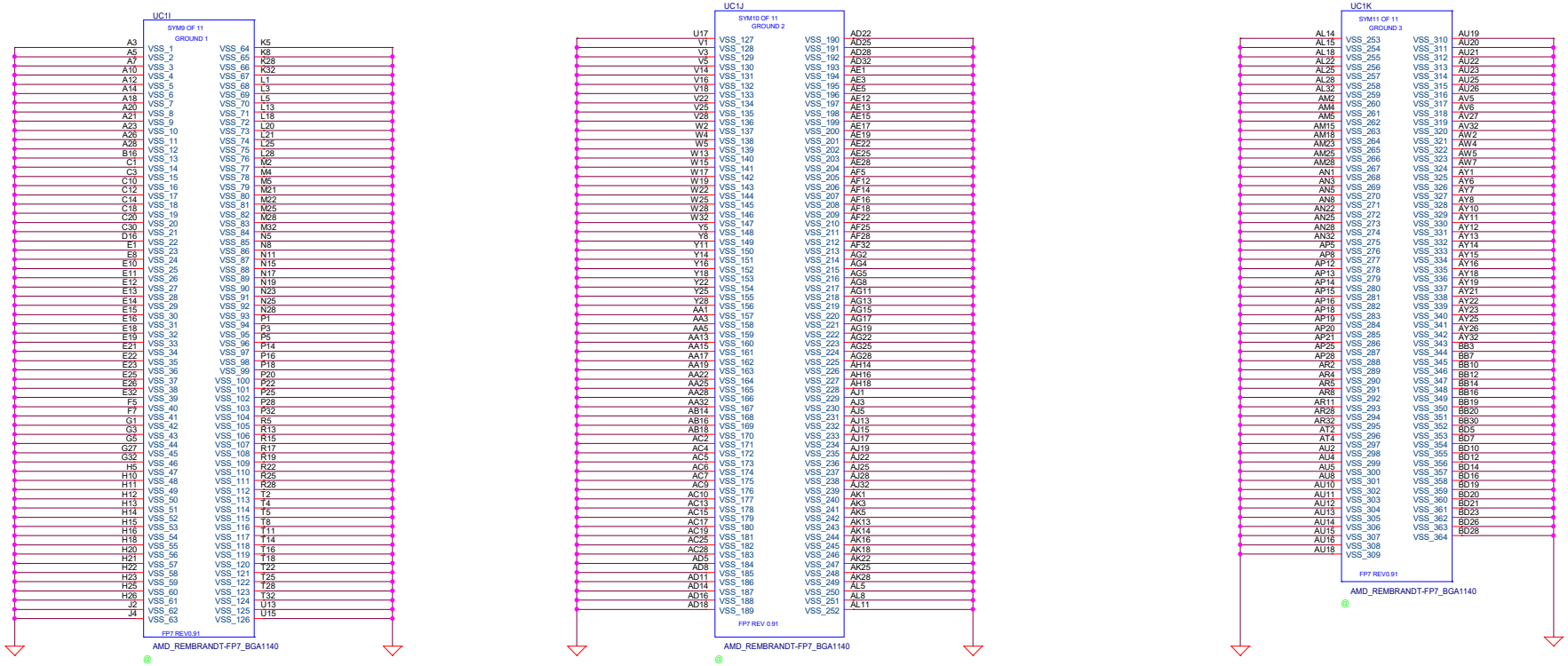

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Title: GND

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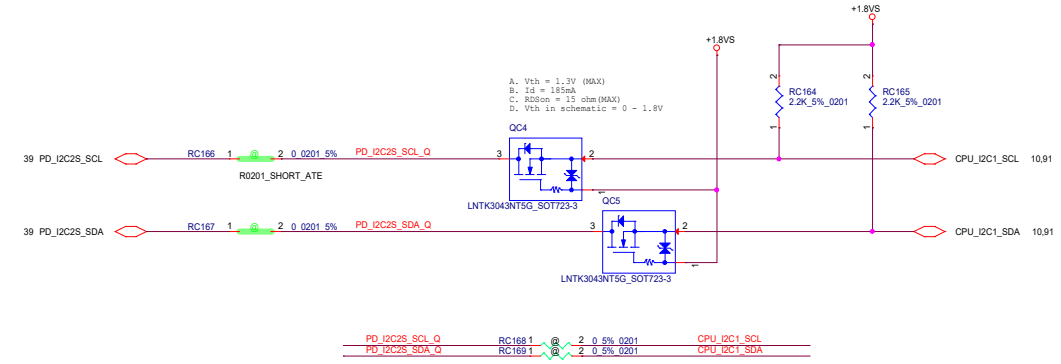
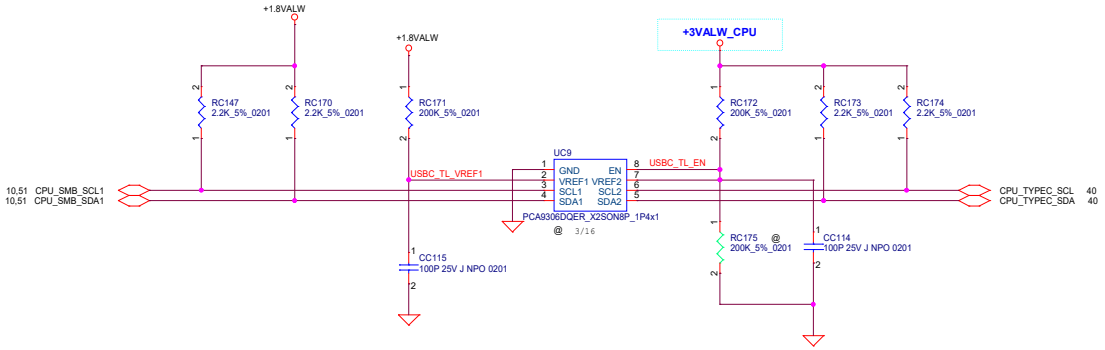
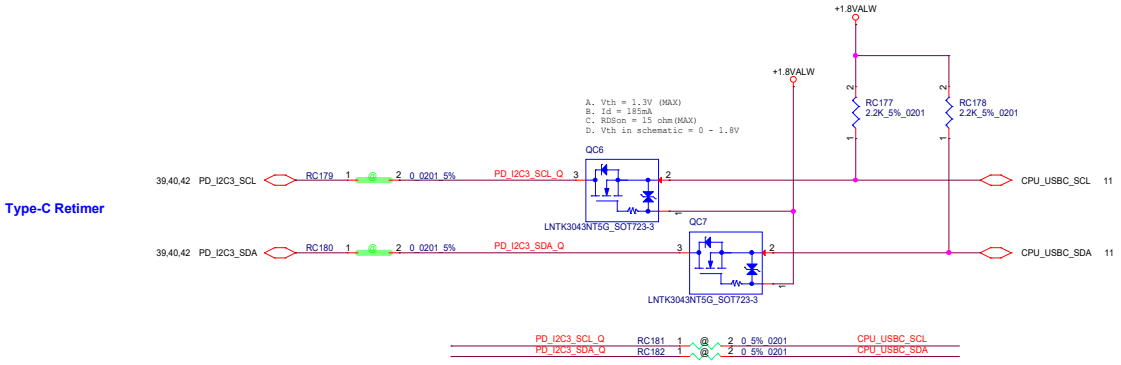
TO PD





Type-C Retimer



Type-C Retimer

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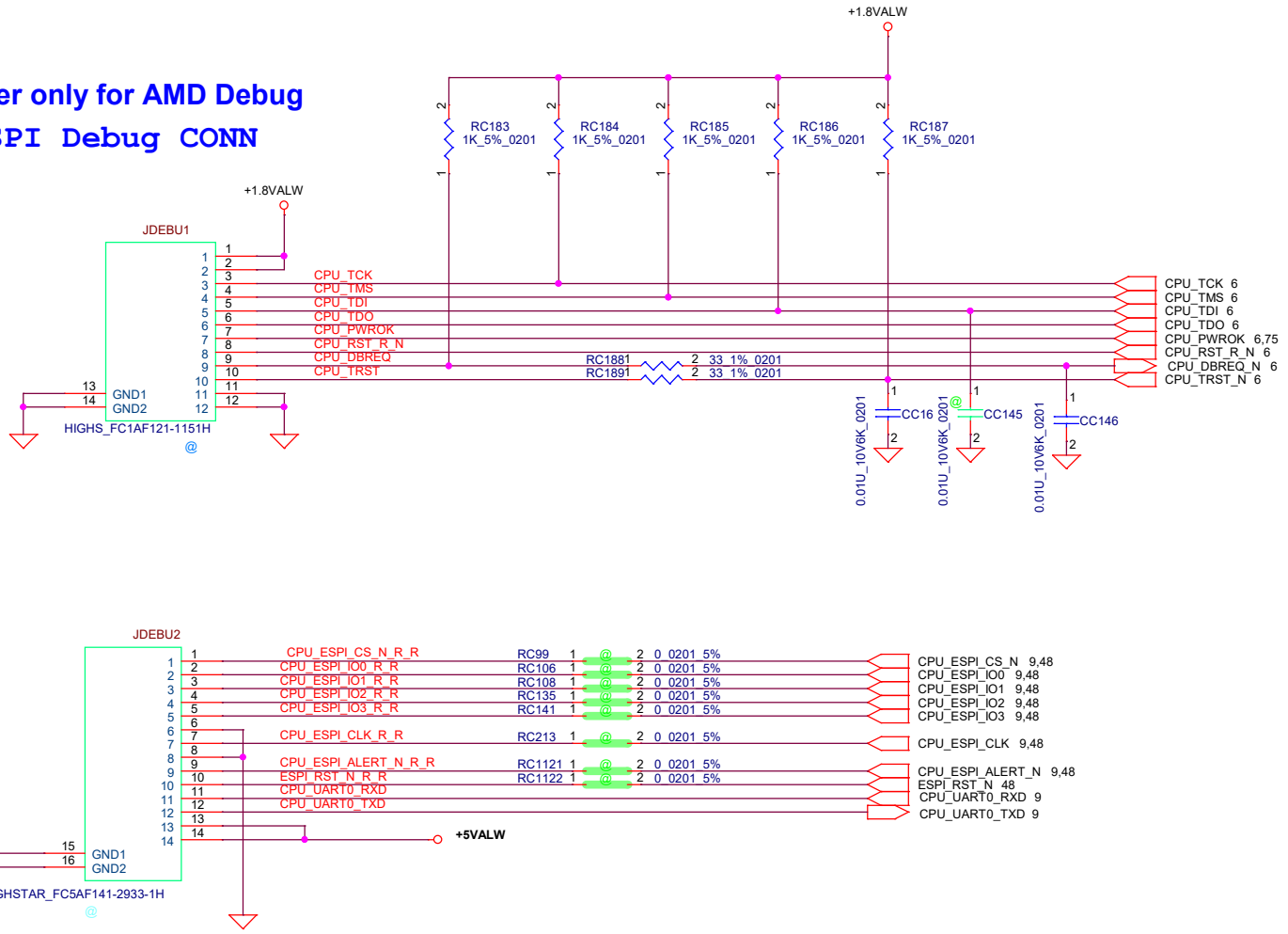
HDT Header only for AMD Debug

HDT&ESPI Debug CONN



to sovle old debug board placement problems or hot plug problems

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Title	HDT/eSPI Debug		
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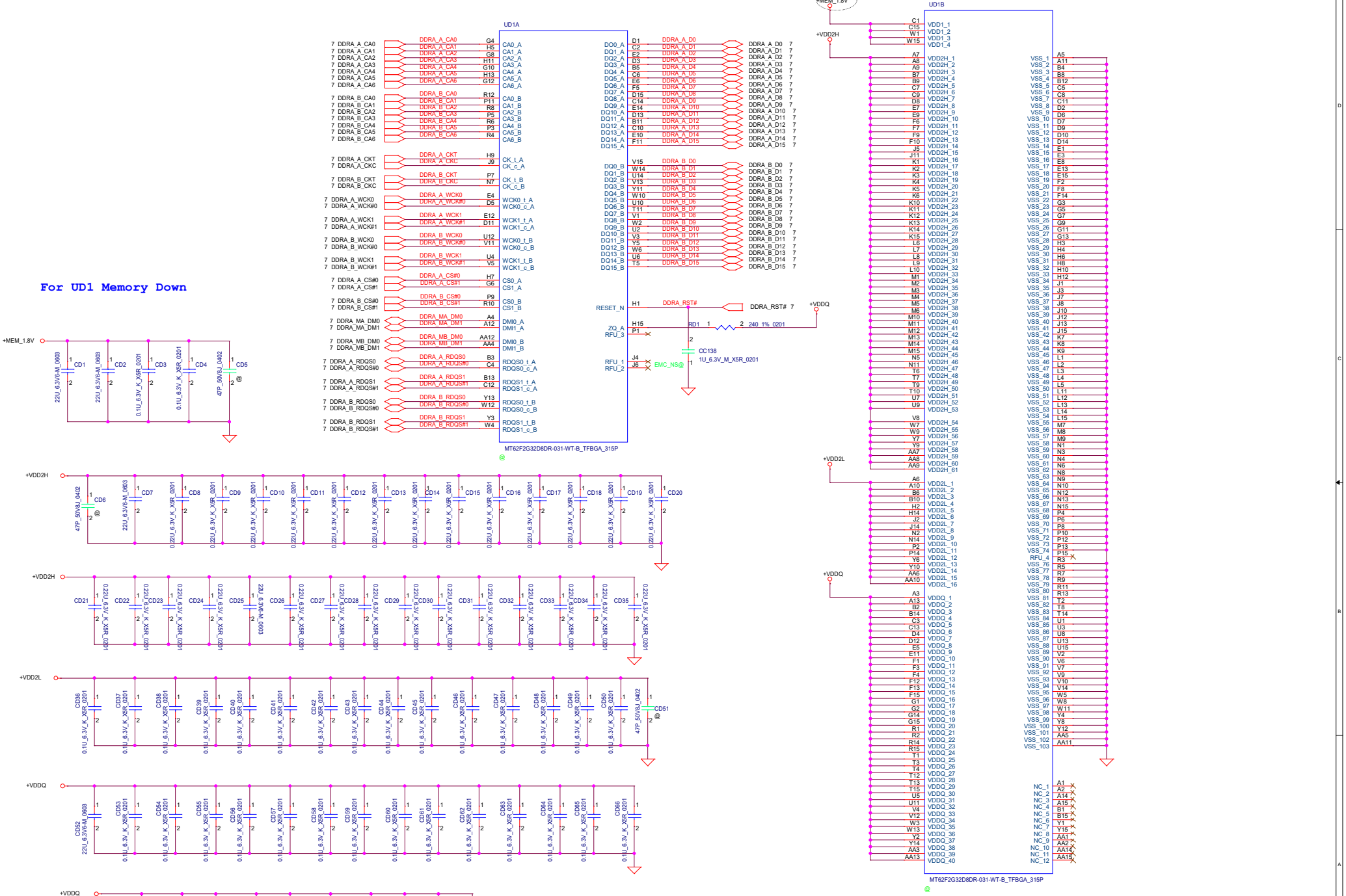
For UD1 Memory Down



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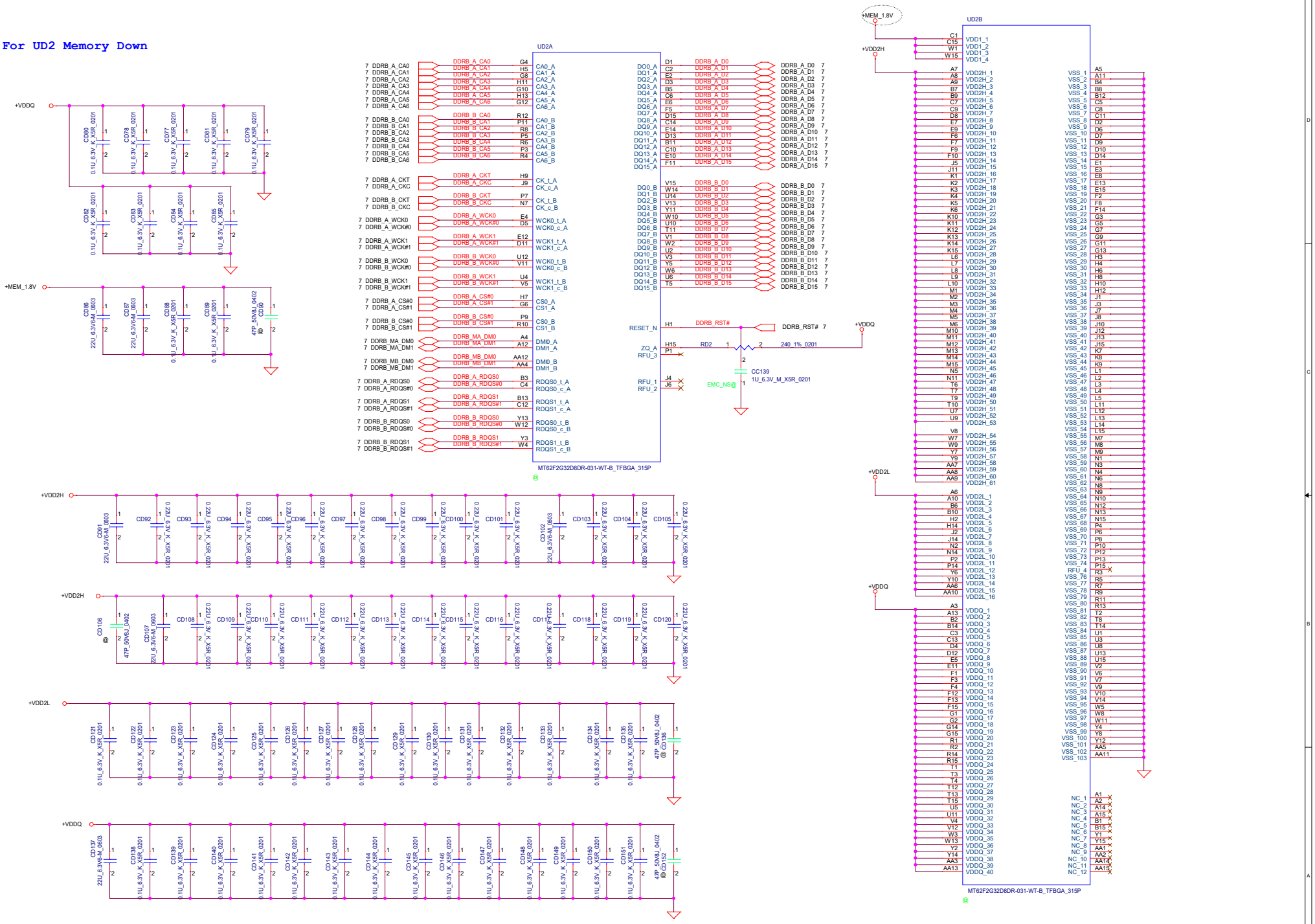
For UD2 Memory Down



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Title	Memory_CHA2		
Size	Document Number		Rev
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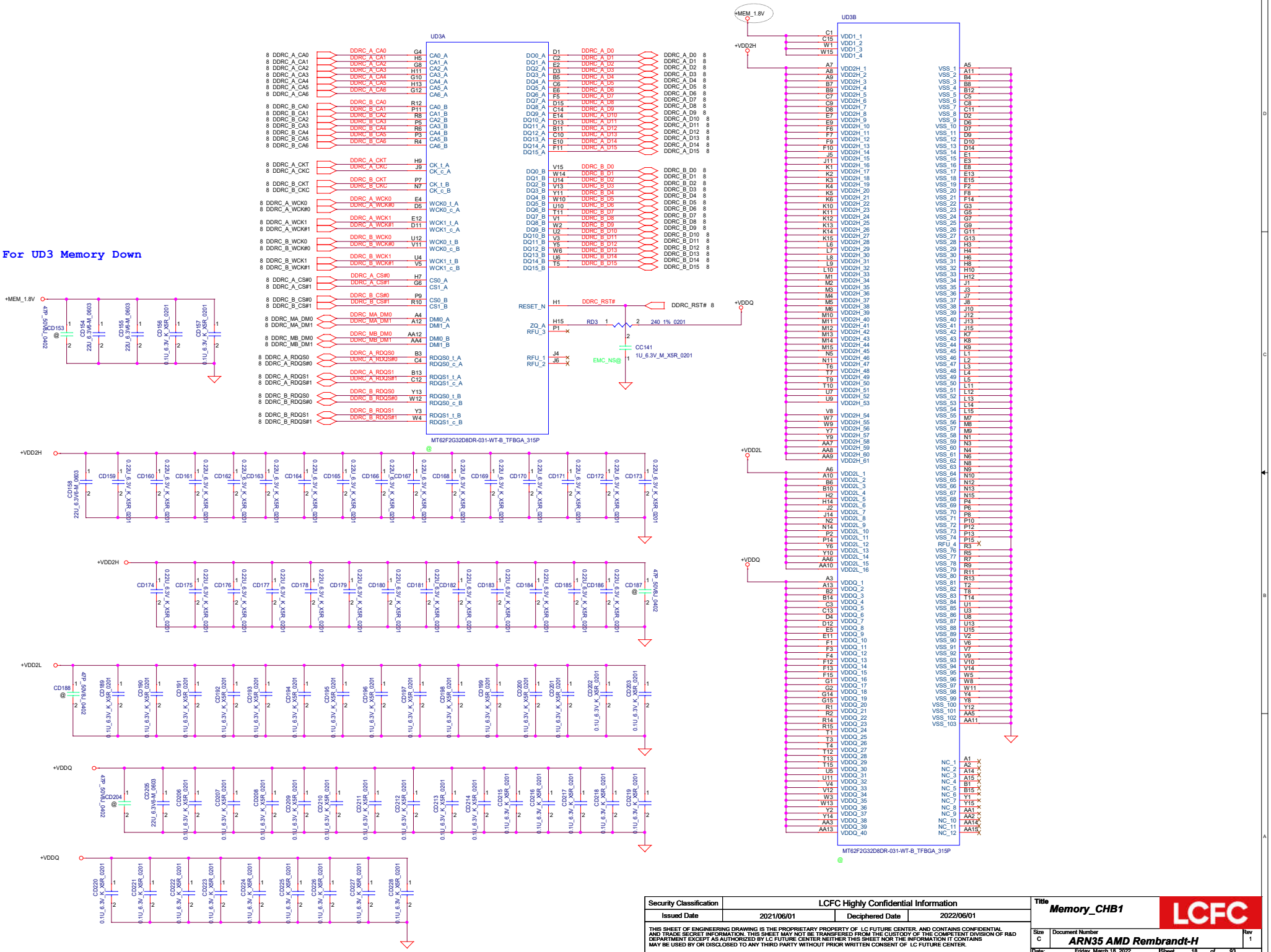
For UD3 Memory Down



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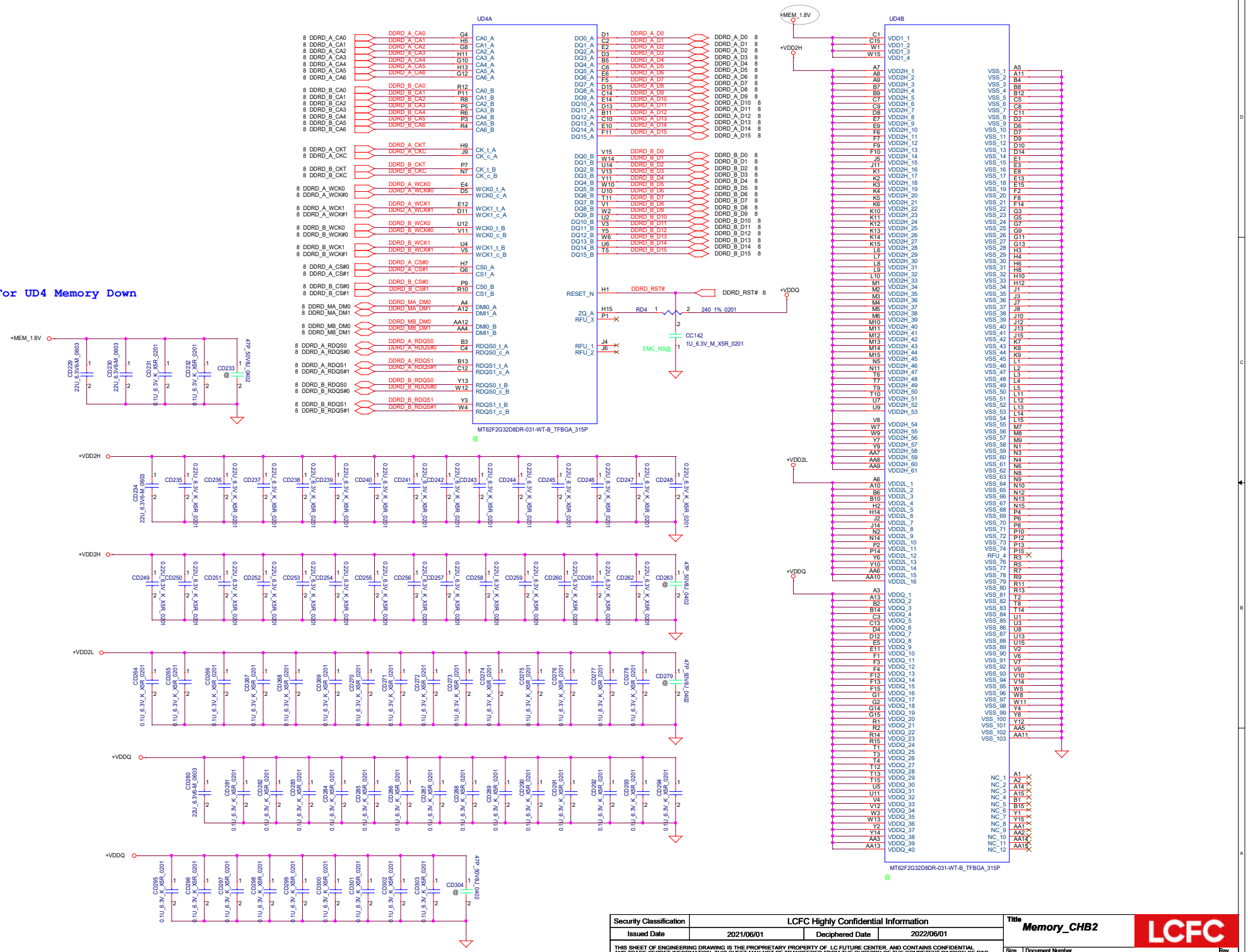

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Title: Memory_CHB2

LCFC

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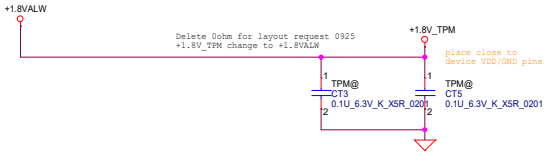
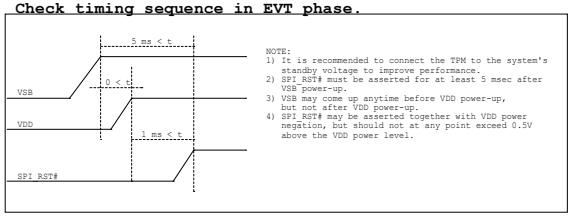
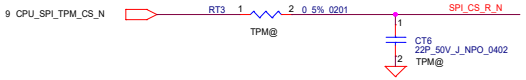


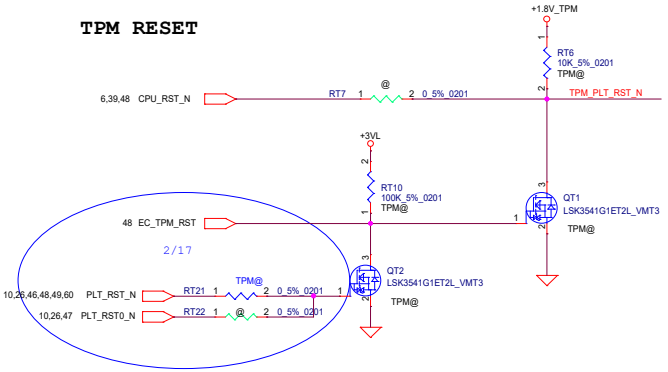
TABLE of TPM		
Vendor	P/N	LCFC P/N
Nuvoton	NPCT750LADYX	SA00008KS30
ST Micro	ST33HTPH2X32AHD8	SA0000AB720

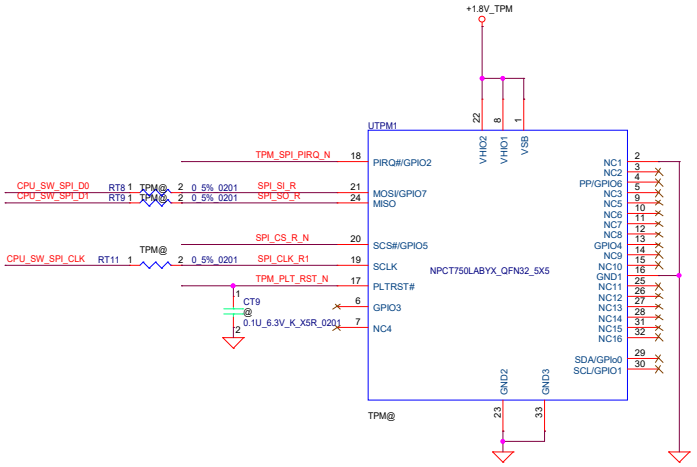
NOTE:
Check timing sequence in EVT phase.

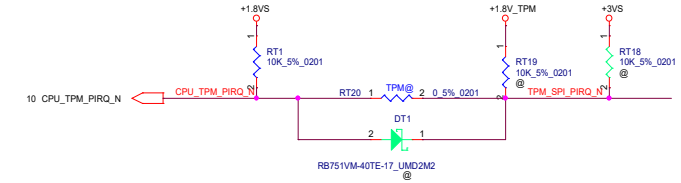


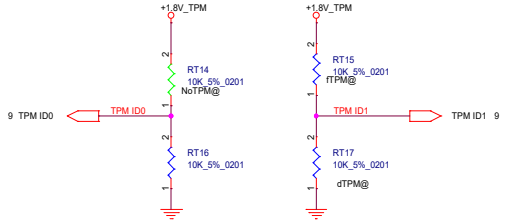


TPM RESET







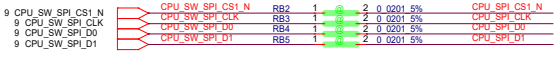


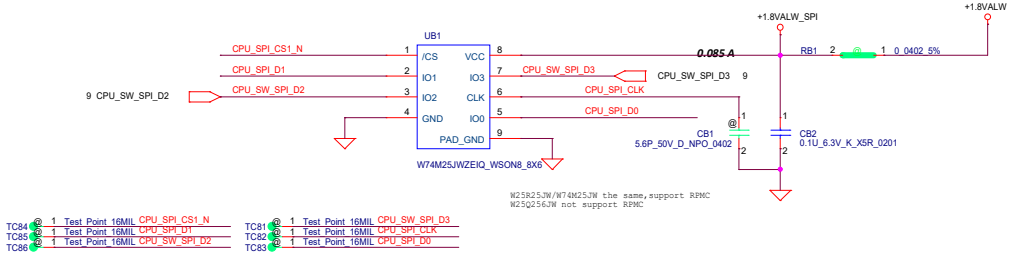
备注：做BOM时需注意TPM 配置（dTPM and fTPM）电阻,Default 为fTPM.

TPM ID	dTPM	fTPM	NoTPM
ID0	0	0	1
ID1	0	1	0

TABLE

Pin No	TCG PTP Spec (v38)	Nuvoton NPCT750LADYX	ST Micro ST33HTPH2X32AHD8
1	VDD	VSB	NC
2	GND	NC	GND
3	NC	NC	NC
4	GPIO	GPIO/PP	PP
5	NC	NC	NC
6	GPIO	GPIO3	NC
7	GPIO	NC	GPIO
8	VDD	VHIO	NC
9	NC	NC	NC
10	NC	NC	NC
11	NC	NC	NC
12	NC	NC	NC
13	GPIO	GPIO4	NC
14	NC	NC	NC
15	NC	NC	NC
16	GND	GND	NC
17	SPI_RST#	RST#	SPI_RST#
18	SPI_PIRQ#	PIRQ#/GPIO2	SPI_PIRQ#
19	SPI_CLK	SCLK	SPI_CLK
20	SPI_CS#	SCS#/GPIO5	SPI_CS#
21	MOSI	MOSI/GPIO7	MOSI
22	VDD	VHIO	VPS
23	GND	GND	NC
24	MISO	MISO	MISO
25	NC	NC	NC
26	NC	NC	NC
27	NC	NC	NC
28	NC	NC	NC
29	SDA/GPIO1	SDA/GPIO1	NC
30	SDA/GPIO0	SDA/GPIO0	NC
31	NC	NC	NC
32	NC	NC	NC





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Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: *SPI ROM/TPM*

LCFC

Size	Document Number	Rev
C	*ARN35 AMD Rembrandt-H*	1

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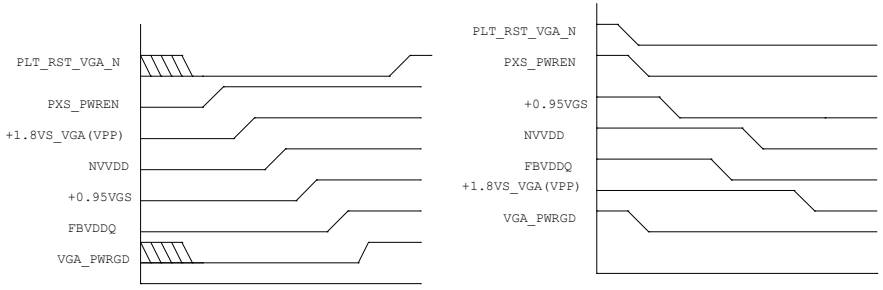
GN20x-E GPIO

GPIO	I/O	GPIO Name	Function Description	Net name	I/O Termination
GPIO0	OUT	NVVDD_PWM_VID	PWM Output to control NVVDD	NVVDD_PWM_VID	
GPIO1	OUT	GC6:GC6_FB_EN	FB Enable for GC6	FB_GC6_EN	(10K PD)
GPIO2	IN	GC6:GPU_EVENT*	Wake the GPU from GC6 state	GPU_EVENT#_R	(10K PU)
GPIO3	OUT	DISP_MUX_CNTL	Display MUX control signal	GPU_MUX_CNTL	(10K PD)
GPIO4	OUT	MSVDD_EN	GPU power sequencing for GC6 ---MSVDD_EN	GPIO4_GC6_MSVDD_EN	(10K PU)
GPIO5	OUT	FRAME_LOCK*	Active low Frame Lock for NVSR panel	UNUSED	
GPIO6	OUT	NVVDD_PSI*	Phase Shedding, NVVDD_PSI	NVVDD_PSI	(10K PU) RSVD
GPIO7	OUT	LCD_BL_PWM	LCD Panel Backlight PWM	GPU_EDP_PWM	(100K PD)
GPIO8	OUT	MEM_VDD_CTL	Memory voltage Control	FBVDDQ_SEL	(10K PD)
GPIO9	I/O	THERM_ALERT*	Active Low Thermal Alert	VGA_ALERT#	(10K PU)
GPIO10	OUT	MEM_VREF_CTL	Memory VREF Control	MEM_VREF_CTL	(100K PD)
GPIO11	OUT	LCD_VDD	LED Panel power enable	GPU_EDP_ENVDD	(10K PD)
GPIO12	IN	PWR_LEVEL	AC power detect or power supply overdraw input	VGA_AC_DET_R	(10K PU)
GPIO13	IN	IGPU_BL_EN	Signal indicating when the IGPU has EN the BL	iGPU_EDP_ENBKL	(100K PU)
GPIO14	IN	HPD_IFPA*	Hot Plug Detect for IFPA	IFPA_HPD	(10K PU)
GPIO15	IN	HPD_IFPB*	Hot Plug Detect for IFPB	IFPB_HPD	(10K PU)
GPIO16	OUT	DISP_MUX_PWM_CNTL	Allows switching the PWM between IGPU & DGPU	PWM_SW_SELECT	(10K PD)
GPIO17	IN	HPD_IFPD*	Hot Plug Detect for IFPD	GPU_EDP_HPD	(10K PU)
GPIO18	IN	HPD_IFPE*	Hot Plug Detect for IFPE	UNUSED	
GPIO19	OUT	UNUSED			
GPIO20	OUT	UNUSED			
GPIO21	OUT	LCD_BLEN	LCD Panel Backlight Enable	GPU_EDP_ENBKL	(100K PD)
GPIO22	OUT	ADC_MUX_SEL	OVRM MUX Input SEL	ADC_MUX_SEL	(2.2K PU)
GPIO23	OUT	UNUSED	UNUSED		
GPIO24	IN	HPD_IFPF*/USBC_HPD* or DONGLE_DET*	Hot Plug Detect for IFPF or USBC	UNUSED	
GPIO25	OUT	FBVDD_PSI	Turns off phases of the Frame buffer power supply	FBVDDQ_PSI	(5.1K PU)
GPIO26	OUT	ROM_WP* FP_FUSE	Connect to WP pin of the GPU EEPROM N18P-G61-A Control FP_FUSE	GPIO26_ROM_WP GPIO26_FP_FUSE	(10K PD) (10K PD) RSVD
GPIO27	IN	HPD_IFPC*	Hot Plug Detect for IFPC	IFPC_HPD	(10K PU)
GPIO28	OUT	MSVDD_PWM_VID	PWM Ooutput to CNTL MSVDD	UNUSED	
GPIO29	OUT	NVVDD_EN	NVVDD Enable RSVD	GPIO29_NVVDD_EN	(100K PU)RSVD
GPIO30	OUT	MSVDD_PSI*	Phase Shedding	UNUSED	

GN20x-E Power Sequence



1. The ramp time for any rail must be more than 40us and is recommended to be less than 2ms.
2. It is recommended that the delay from 1V8 on to PEXVDD/GPU_PGOOD assertion not exceed 20ms.
3. The ramp-up overshoot should not exceed the silicon reliability limit voltage.
4. Power up NVVDD must be 90% before PEXVDD can ramp-up.
5. Refer to the JEDEC Memory SPEC for memory-related power sequencing.
7. FBVDD/Q, USB_VDDP and 1V8_AON don't need power cycle for GC6

1. For GDDR6, VPP must be equal to or higher than FBVDD/Q at all times;use gate logic and discharge circuit as needed
2. All 3.3V devices that connect to the GPU must be ramp down before 1V8; GPU can NOT have any 3.3V leakage path after 1V8 power down.
3. Power down of PEXVDD must be less than 10% before NVVDD can start ramp-down.

H=High: Tied to 1.8V
M=Middle: Tied to 0.9V
L=Low: Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	GN20x-E VRAM
L	L	L	0 (0x0000)	Samsung K4Z80325BC-HC14
L	L	H	1 (0x0001)	Micron MT61K256M32JE-14:A
L	H	L	2 (0x0002)	Hynix H56C8H24AIR-S2C
L	H	H	3 (0x0003)	
H	L	L	4 (0x0004)	
H	L	H	5 (0x0005)	
H	H	L	6 (0x0006)	
H	H	H	7 (0x0007)	
L	L	M	8 (0x0008)	
L	M	L	9 (0x0009)	Samsung(for E7) K4ZAF325BM-HC 14
L	M	H	10 (0x000A)	
L	H	M	11 (0x000B)	
M	L	L	12 (0x000C)	
M	L	H	13 (0x000D)	

FS_OVERT# FUNCTION

ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT# FUNCTION
L	L	H	FS_OVERT# function ENABLE
L	L	L	FS_OVERT# function DISABLED Reserved; do not configure

GN20x-E ES sample Delete

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

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Title: *N18E VGA Notes List*

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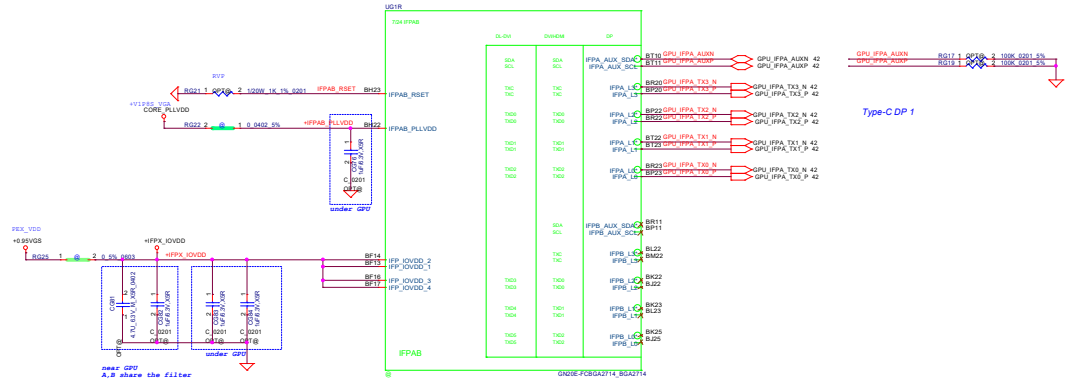
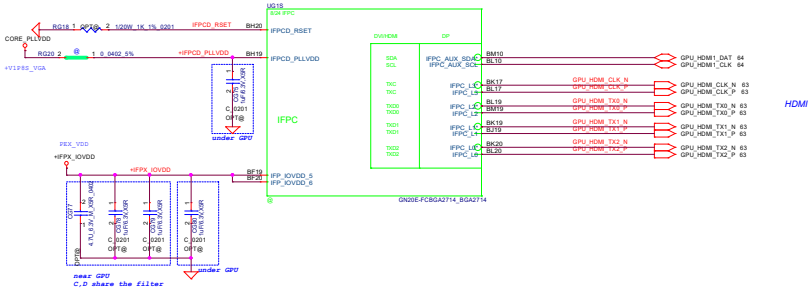
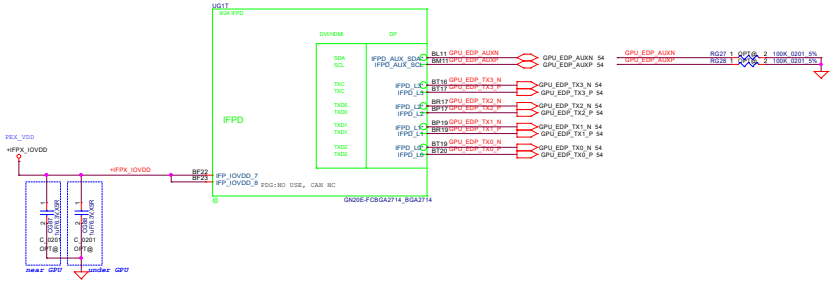
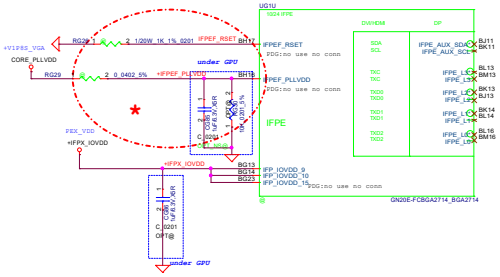






1.If an IFP link is unused, The main and AUX links, IFPxy_RSET can be left unconnected,and IFPxy_PLLVDD should be 10K PD to GND.

2.IFP_IOVDD rail can be left unconnected if no IFP link is used,"If any IFP is used, all IFP_IOVDD balls must be connected to power rail.



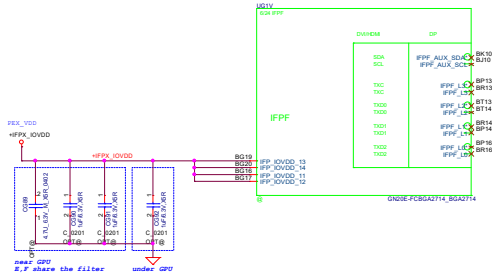


Table 9.4 GB4B-256 Standard Configurations

Link	Standard Display Configurations	
Link A	DisplayPort, DVI (Single Link)	DVI (Dual Link)
Link B	DisplayPort, DVI (Single Link)	
Link C	DisplayPort, HDMI, DVI (Single Link)	
Link D	eDP only (does not support drive of an external display)	
Link E	DisplayPort, HDMI, DVI (Single Link)	
Link F	USBC, Dongle support for DP	

Note: Maximum of four independent simultaneously served display heads supported.
Note: eDP is supported on IFPD only

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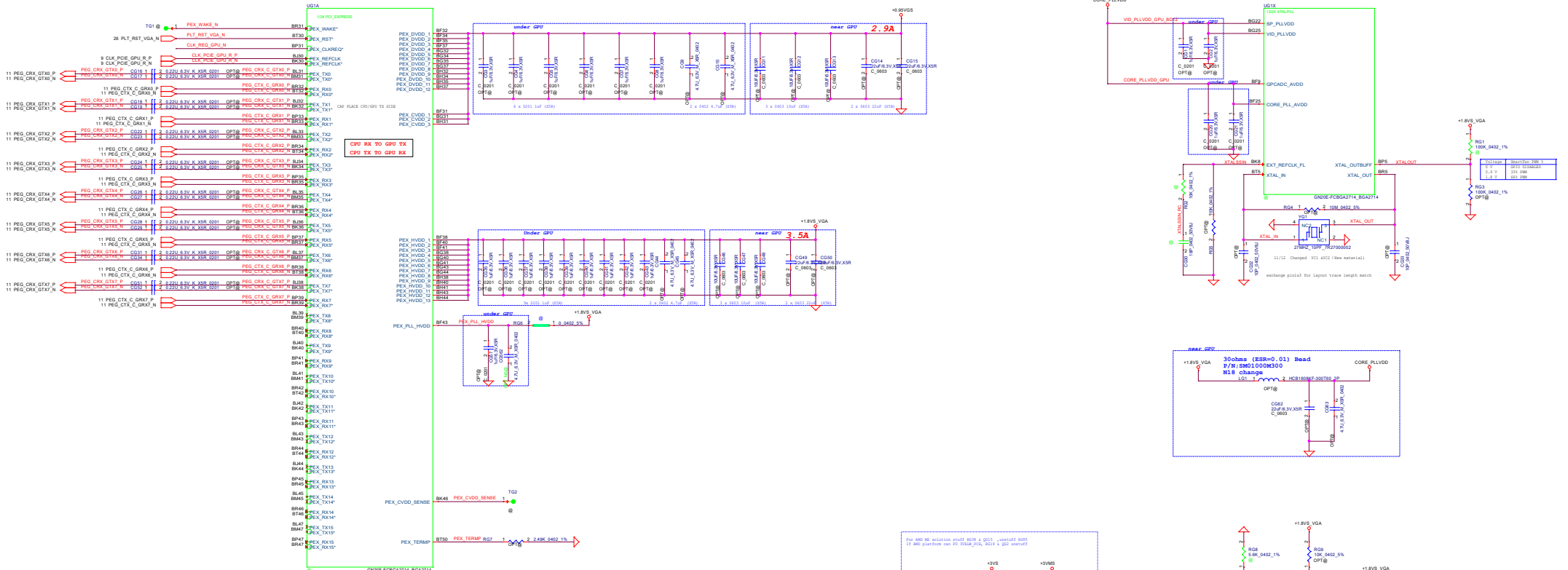
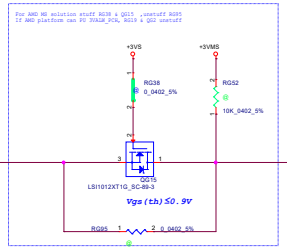
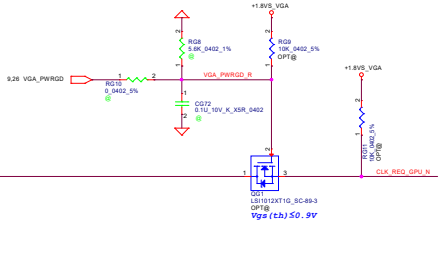
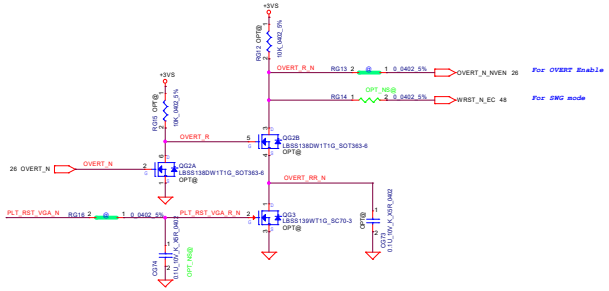
Date: Friday, March 18, 2022	Sheet 22 of 93		







FS_OVERT# FUNCTION



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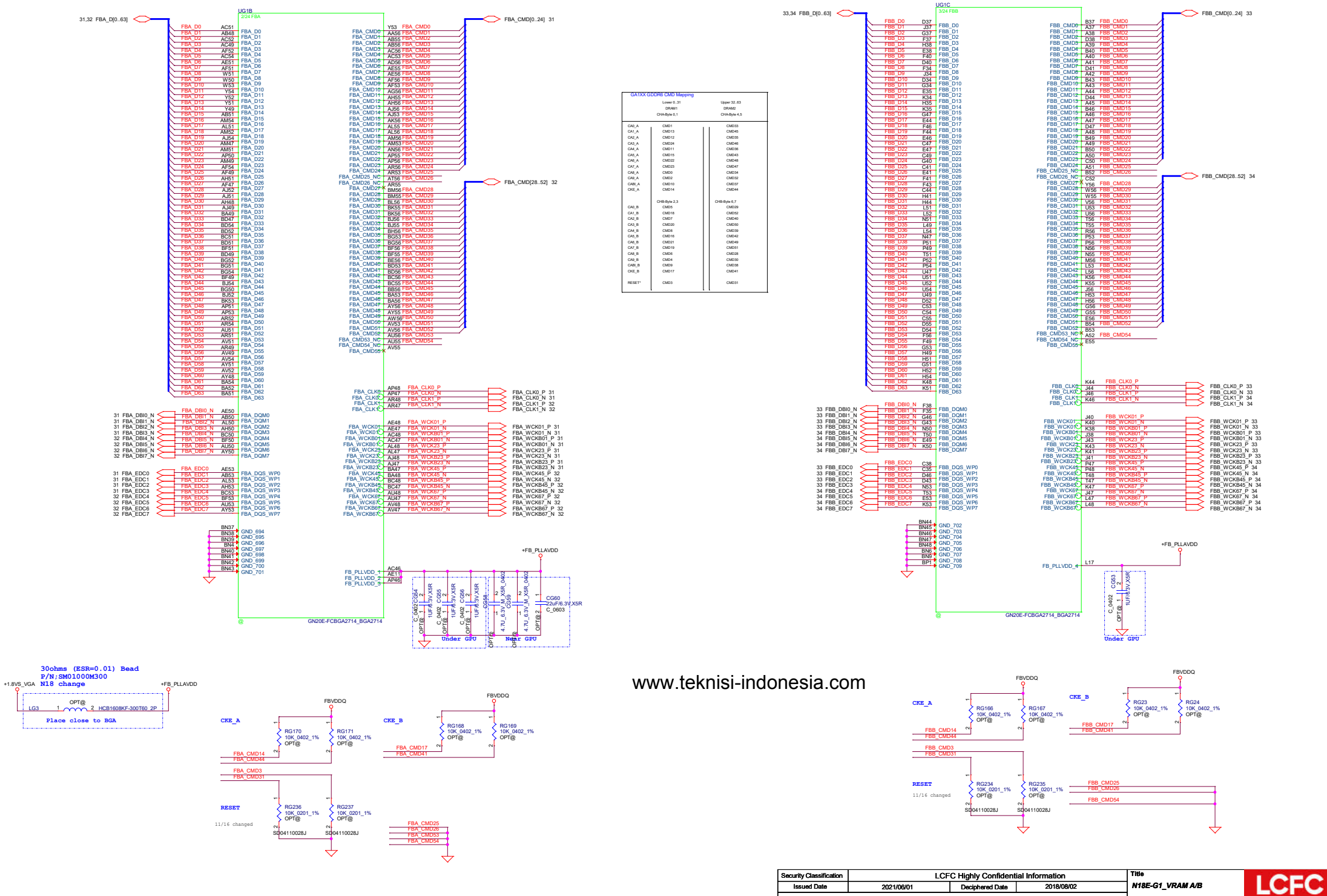

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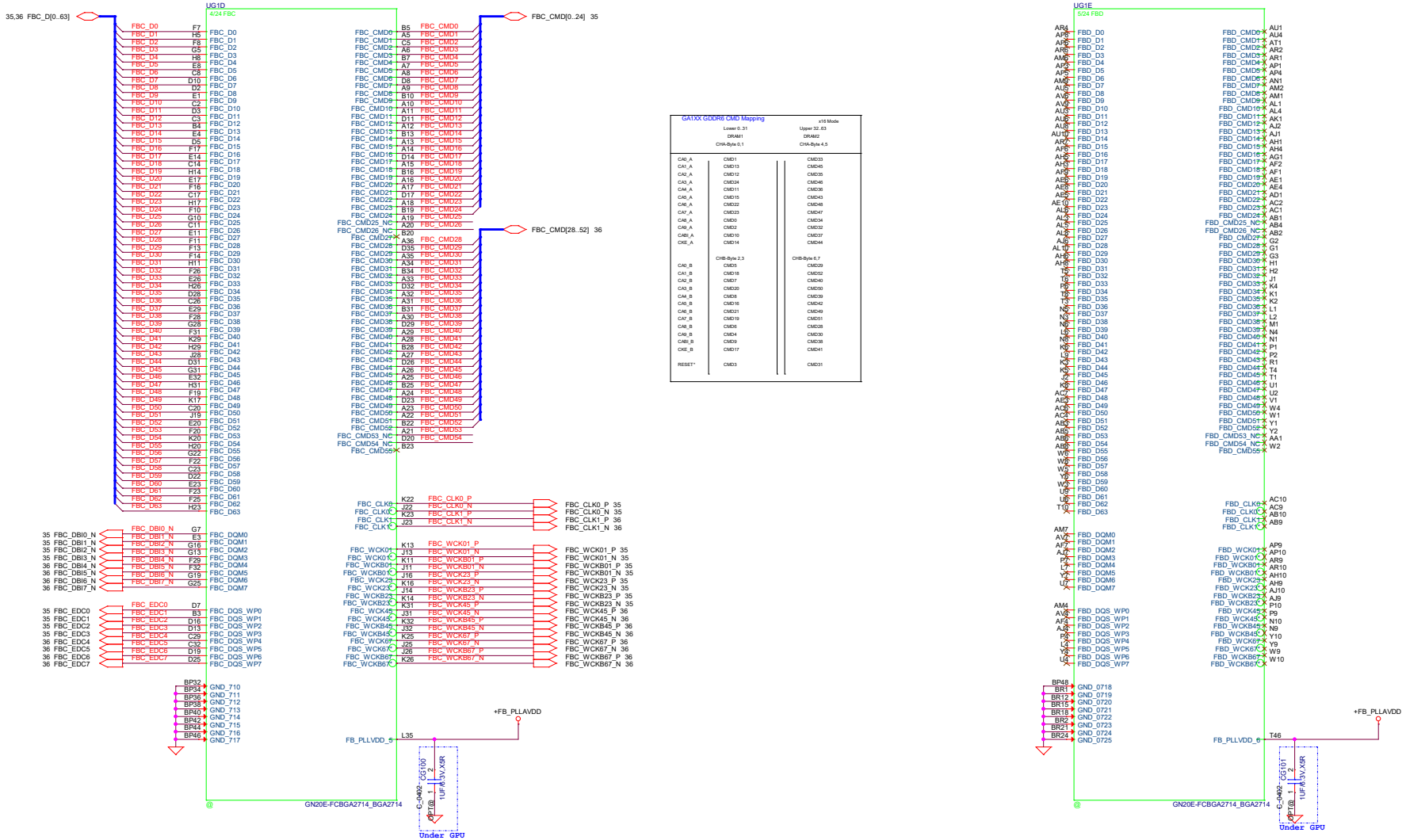
Title			
N18E-G1_VRAM A/B			
Size: A2	Document Number: ARN35 AMD Rembrandt-H		Rev: 1
Date: Friday, March 18, 2022	Sheet 24 of 93		



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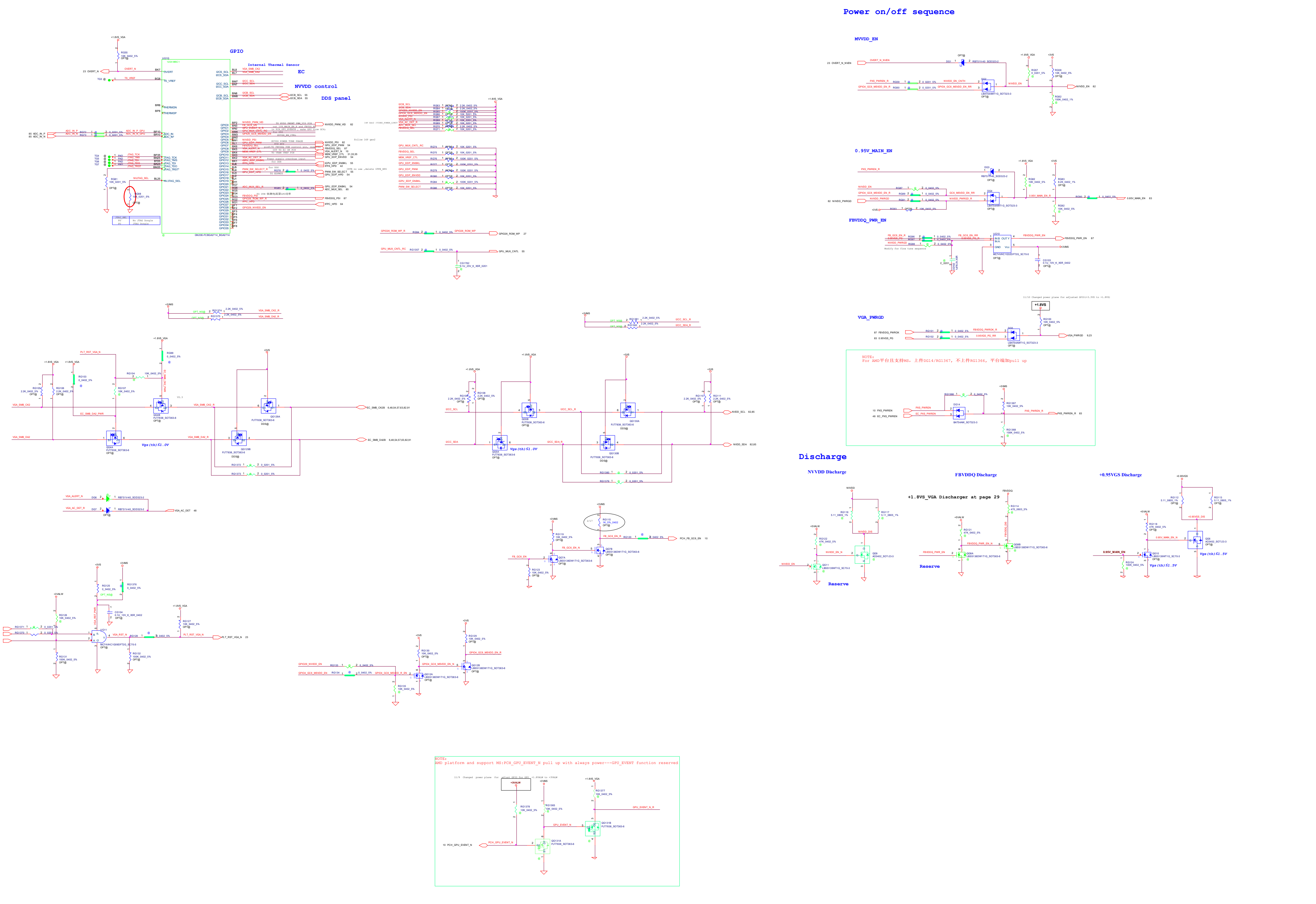
Title	N18E-G1_VRAM C/D		
Size	A2	Document Number	ARN35 AMD Rembrandt-H
Rev	1		
Date:	Friday, March 18, 2022	Sheet	25 of 93



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Title: N18E-G1_GPIO I/F

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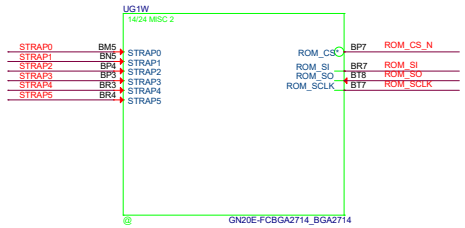
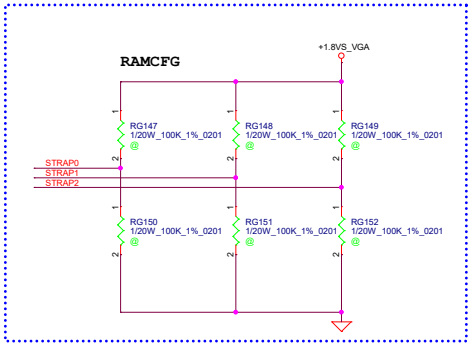
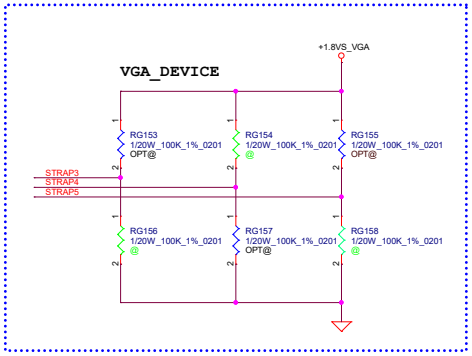
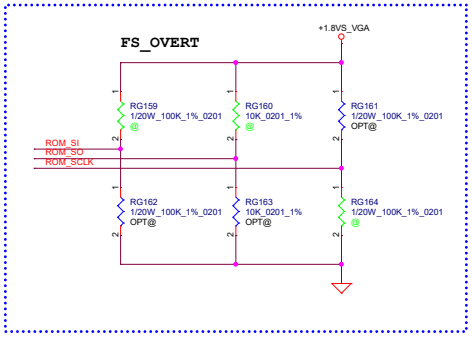
Size: A0 | Document Number: ARN35 AMD Rembrandt-H | Rev: 1

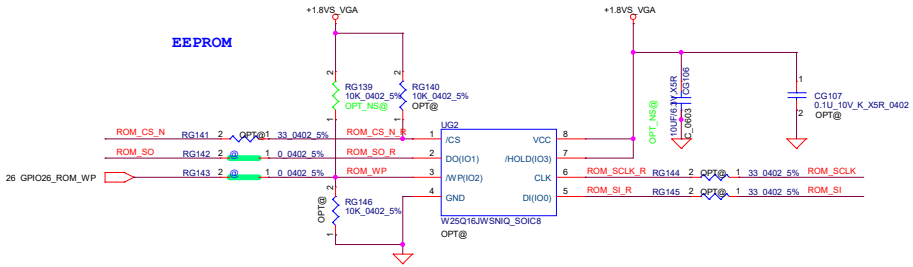
Date: Friday, March 18, 2022 |











VRAMCFG

GPU VRAM	FB Memory (GDDR6)		RAMCFG[2:0]	STRAP2	STRAP1	STRAP0
GN20x-E7	Samsung 8Gb	K4Z80325BC-HC14	0(0x0000)	L	L	L
	Samsung 16Gb	K4ZAF325BM-HC 14	9(0x0009)	L	M	L

GPU VRAM	FB Memory (GDDR6)		RAMCFG[2:0]	STRAP2	STRAP1	STRAP0
GN20x-E5 GN20x-E3	Samsung 8Gb	K4Z80325BC-HC14	0(0x0000)	L	L	L
	Micron 8Gb	MT61K256M32JE-14:A	1(0x0001)	L	L	H
	Hynix 8Gb	H56G32CS4DX005N	2(0x0002)	L	H	L

VGA_DEVICE E3/E5/E7

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
H	L	H	0	1	0	1

* 1:DEVID_SEL for G-SYNC SKU

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

YX70 Y770S 0101
Gen2 0001
Gen3 0101

FS_OVERT

GPU	ROM_SO	ROM_SI	ROM_SCLK	FS_OVERT
GN20x	L	L	H	ENABLE

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Title: N18E-G1_NVHS I/F

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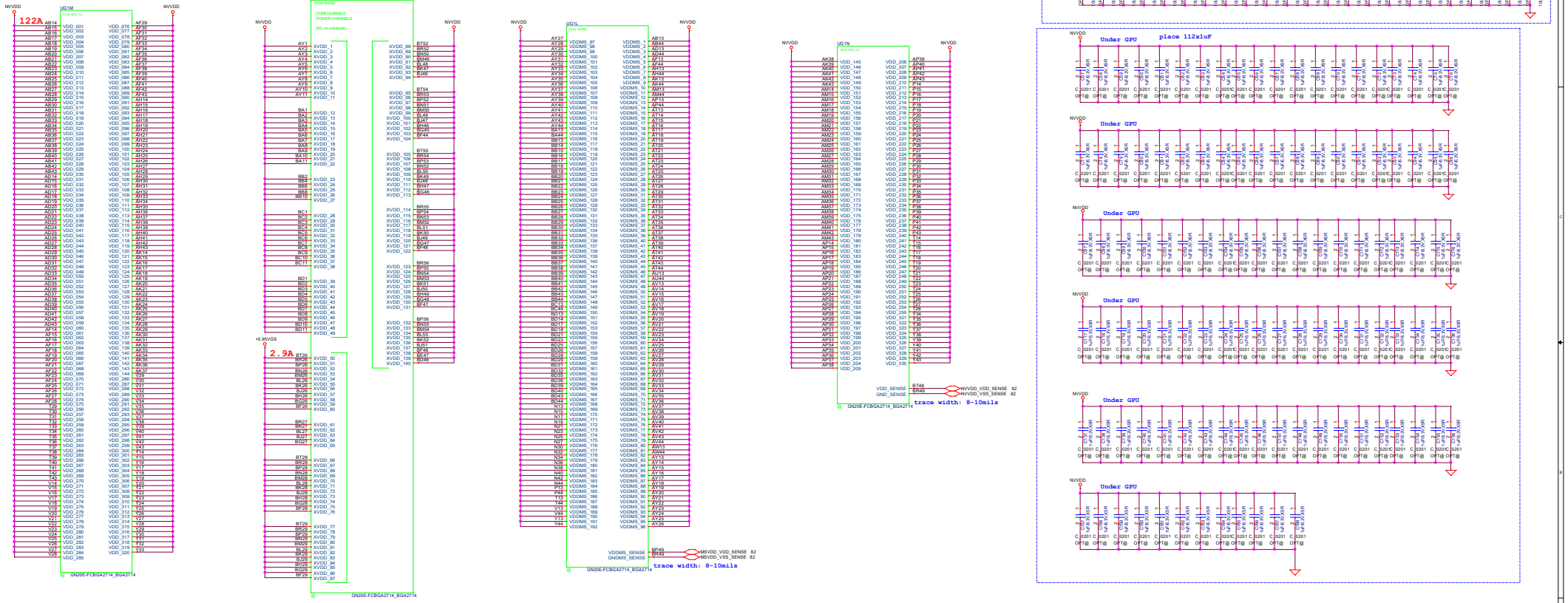
* Follow 16P Gen2 As Cost Consideration

GN20-E3 Max-Q
+NVVDD
330uF X3 at GPU page
330uF X8 at Power IC
22uF X7 X6S
10UF*23
1uF X112



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Title: N18E-G1_POWER GPU CORE

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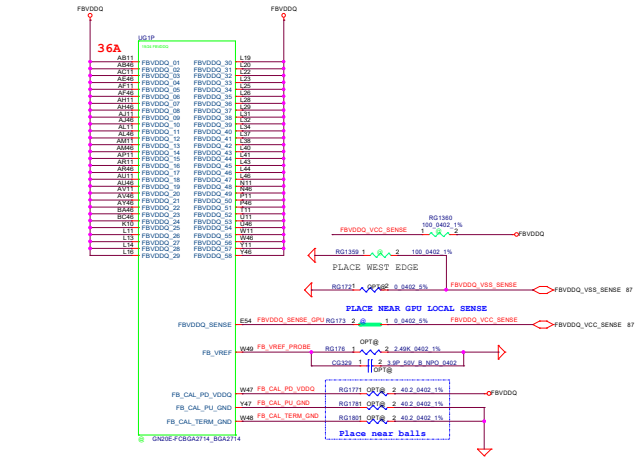
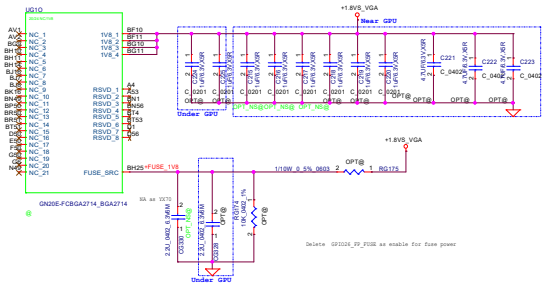
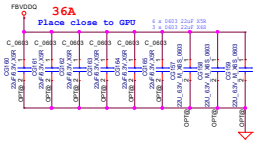
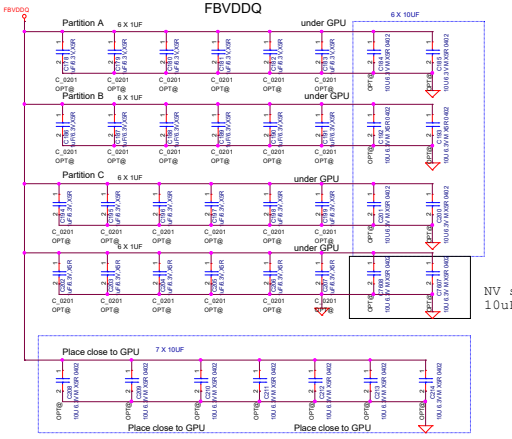






GN20-E3 Max-Q
FBVDDQ
22uF X9
10uF X 13
1uF X24



NV suggestion for Partition D
10uF*2

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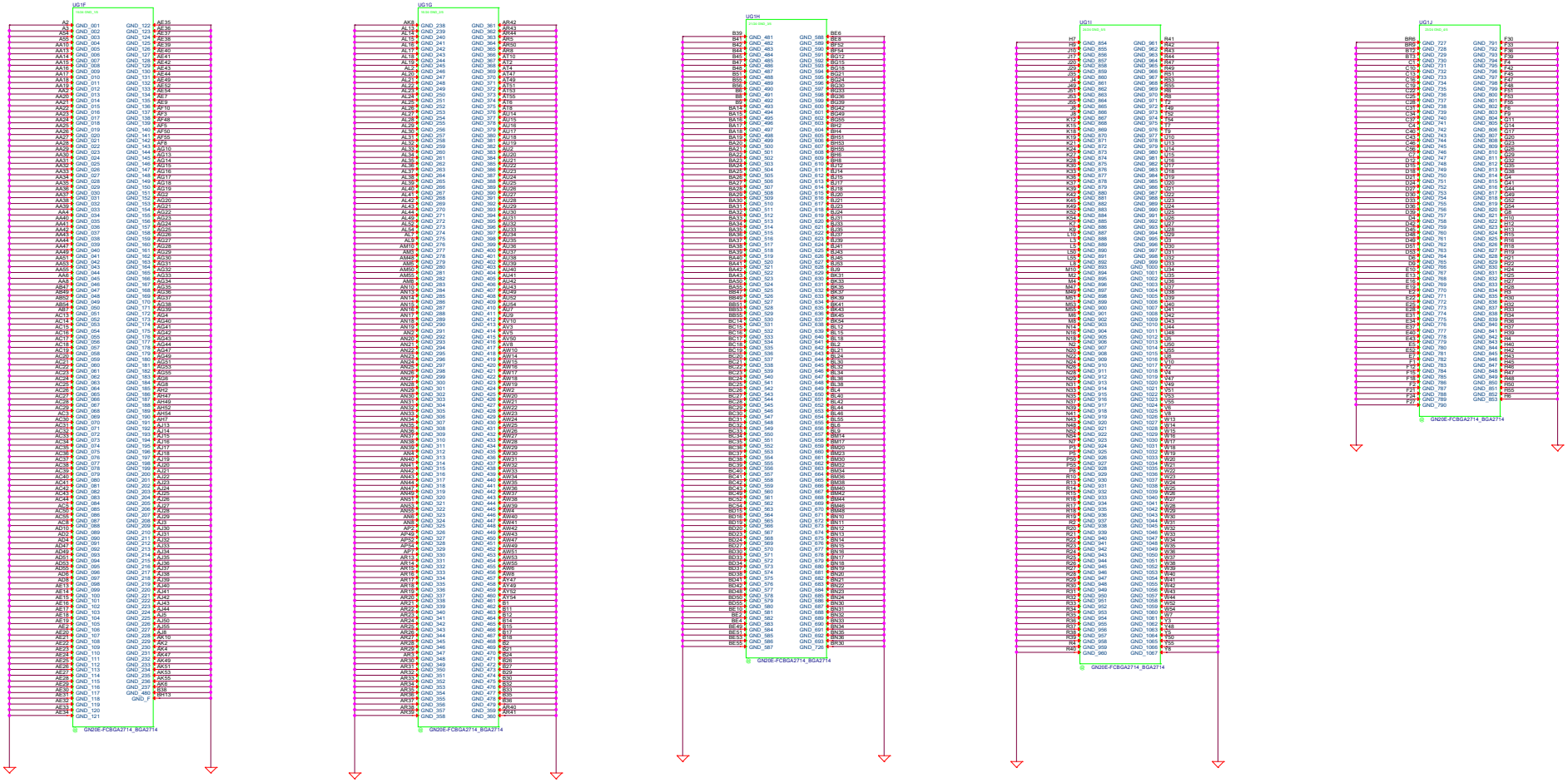
Issued Date	2021/06/01	Deciphered Date	2016/08/02
Size: D	Document Number: ARN35 AMD Rembrandt-H		Rev: 1
Date: Friday, March 18, 2022	Sheet 29 of 93		



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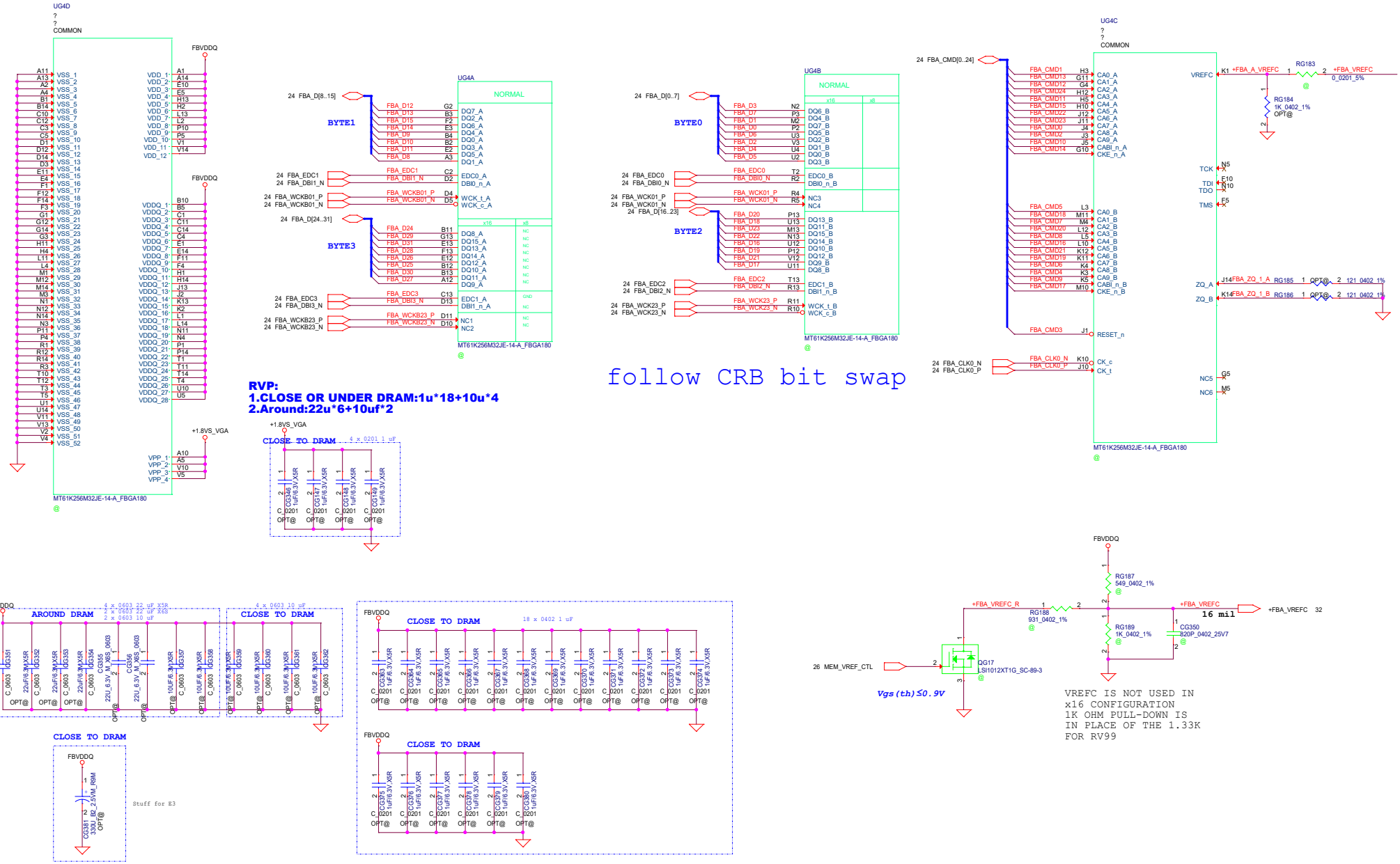
Title	N18E-G1_GND	LCFC	
Size D	Document Number AR35 AMD Rembrandt-H		Rev 1
Date: Friday, March 18, 2022	Sheet 30 of 93		



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Title: N18E-G1_GDDR6_A_[31_0]

LCFC

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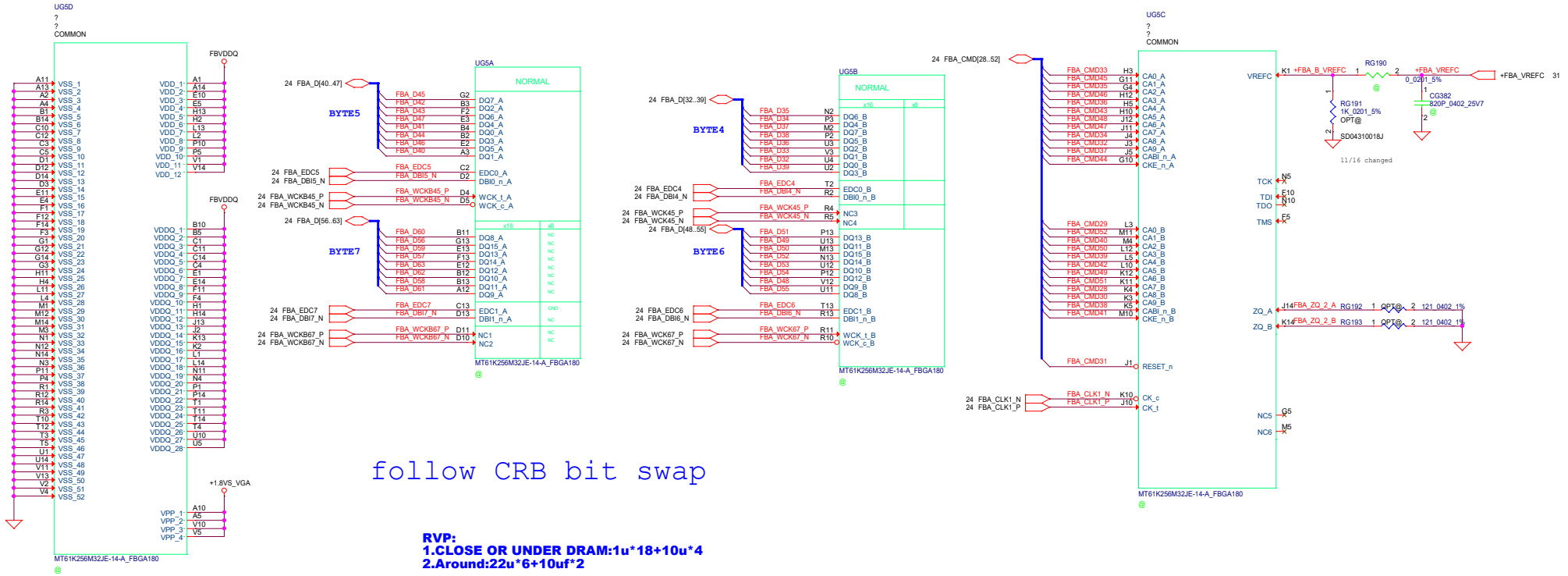

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Title: *N18E-G1_GDDR6_A_[63_32]*

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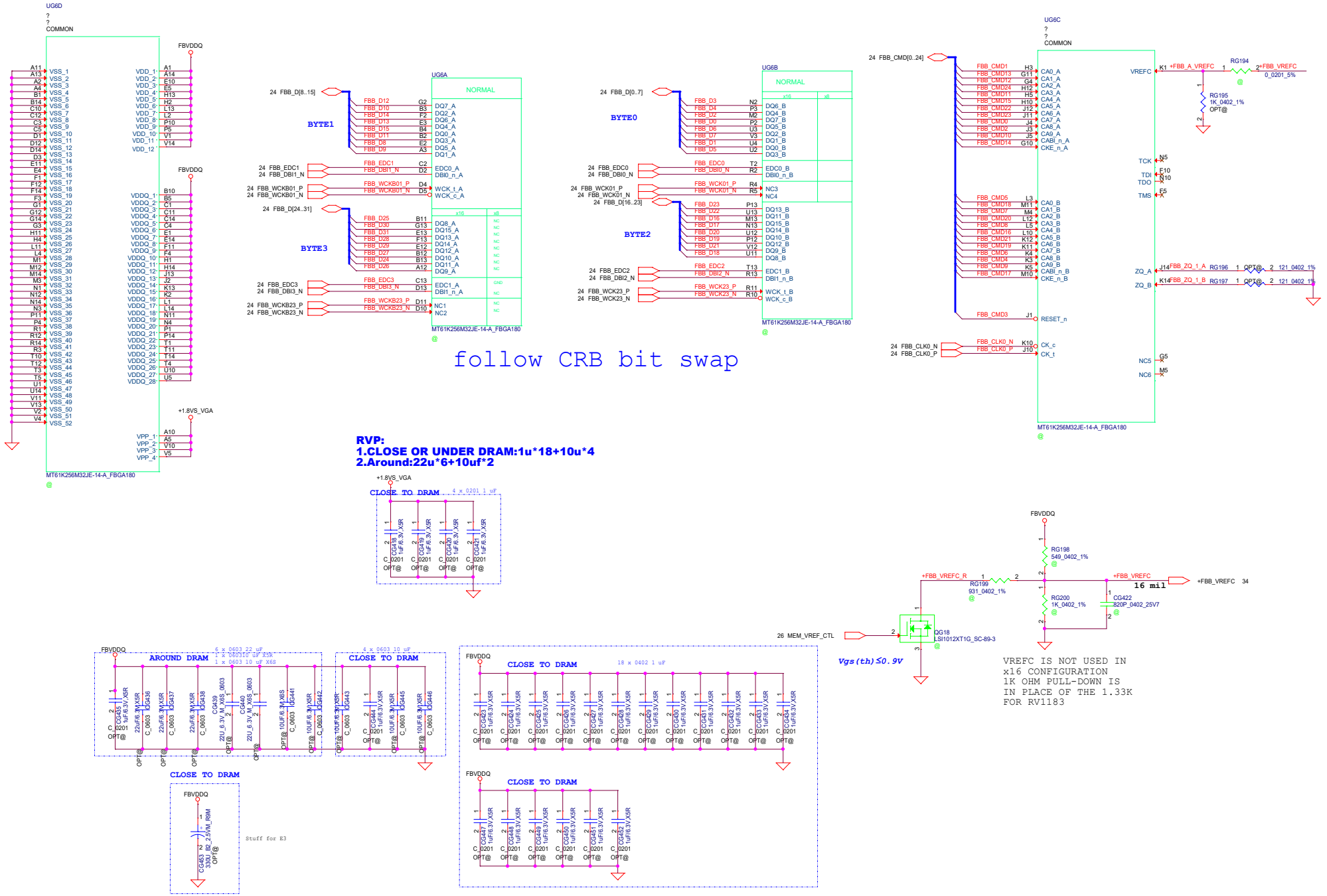
Date: Friday, March 18, 2022 | Sheet 32 of 93



Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2018/08/02

Title: N18E-G1_GDDR6_B_[31_0]

LCFC

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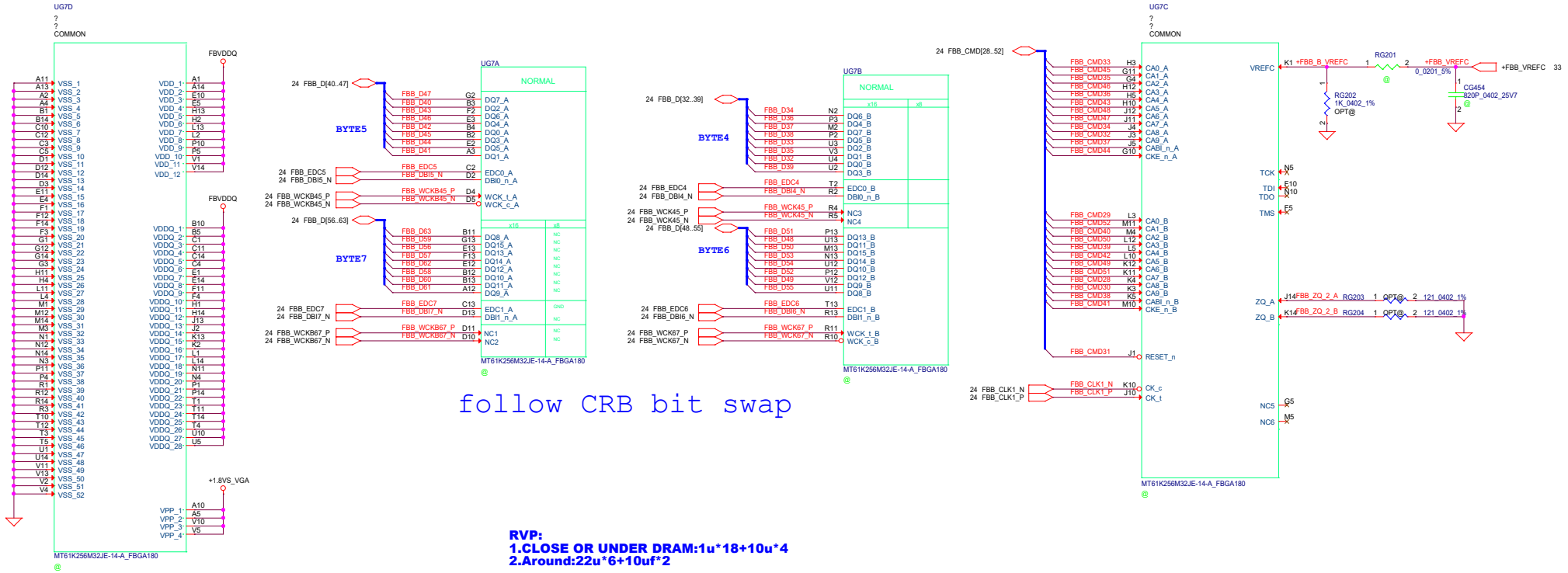
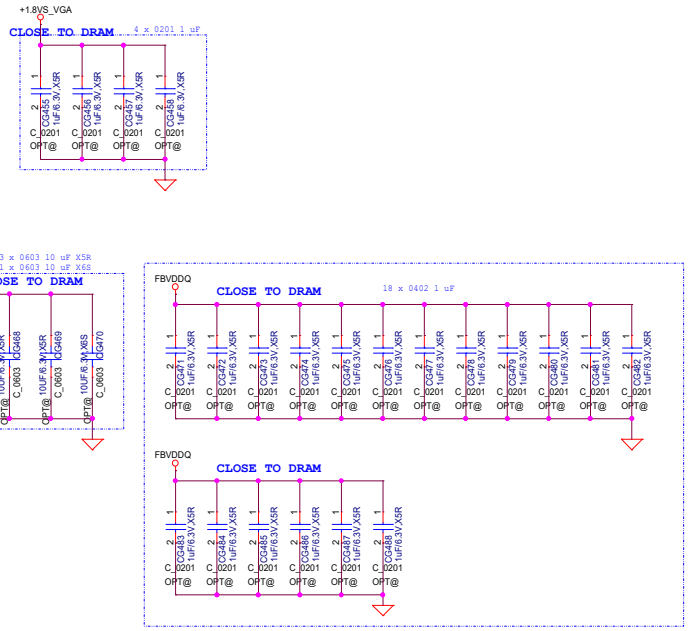
Date: Friday, March 18, 2022 Sheet 33 of 93



RVP:
1.CLOSE OR UNDER DRAM:1u*18+10u*4
2.Around:22u*6+10uf*2



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Title: *N18E-G1_GDDR6_B_[63_32]*

LCFC

Size	Document Number	Rev
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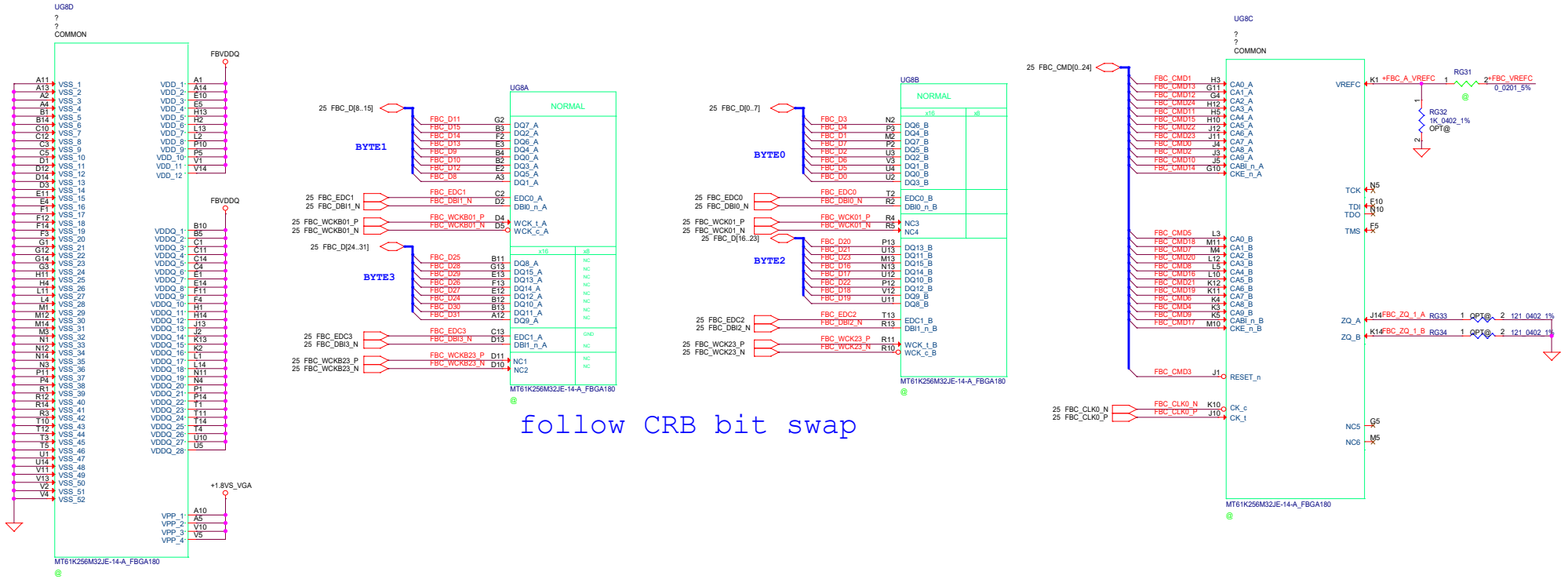
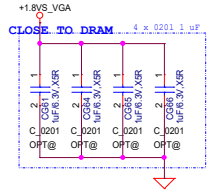
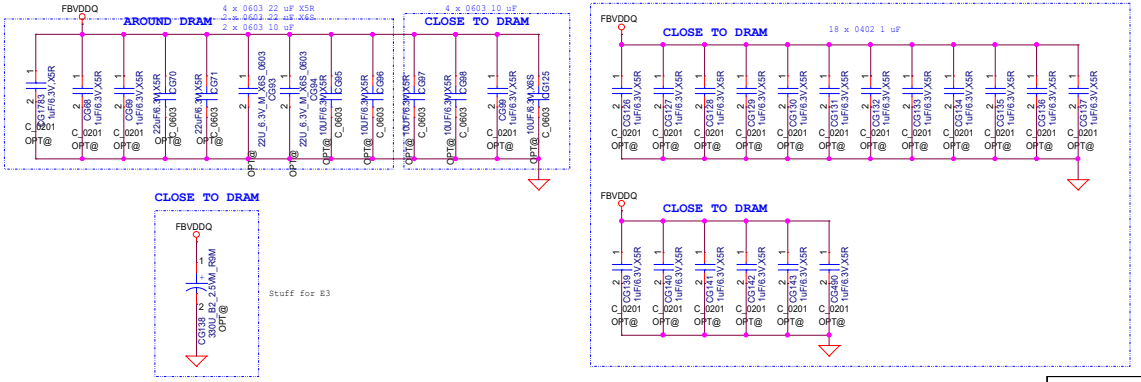
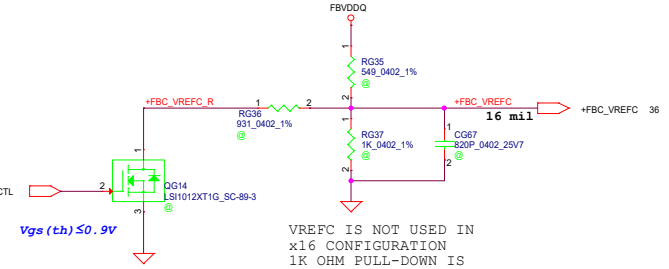


RVP:
1.CLOSE OR UNDER DRAM:1u*18+10u*4
2.Around:22u*6+10uf*2







VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR RV1189

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Title: N18E-G1_GDDR6_C_[31_0]

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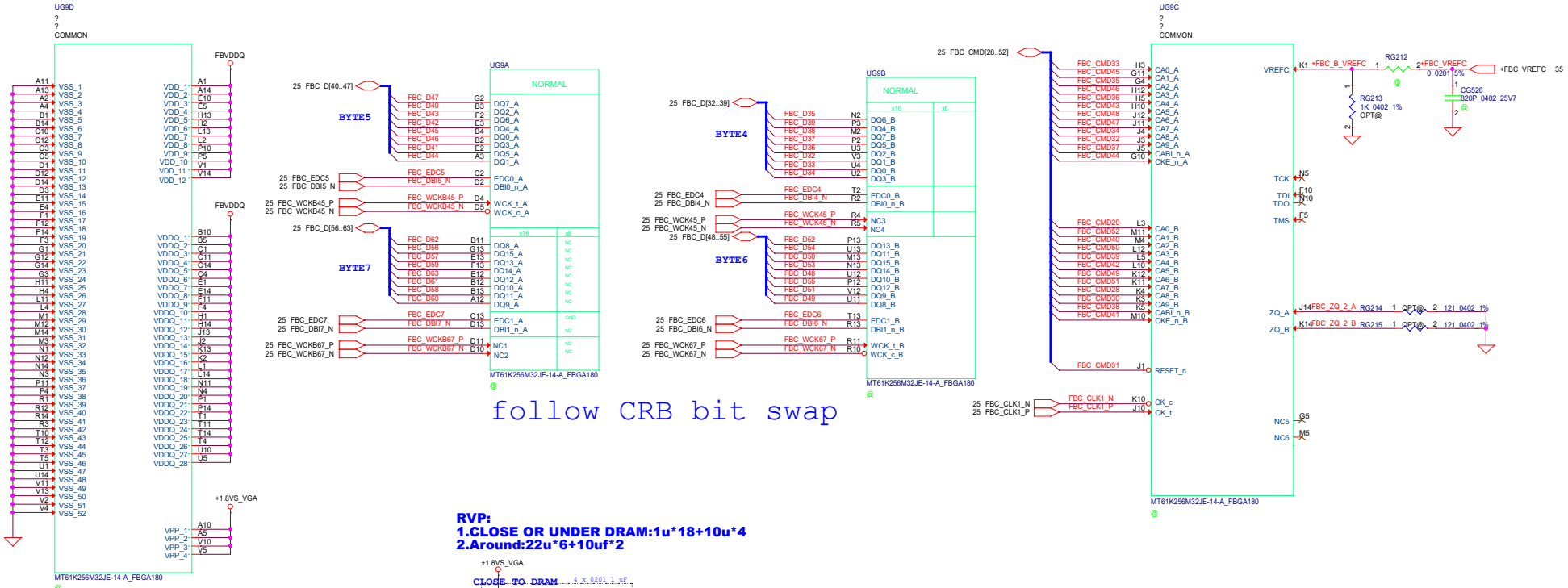

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Title: *N18E-G1_GDDR6_C_[63_32]*

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Title

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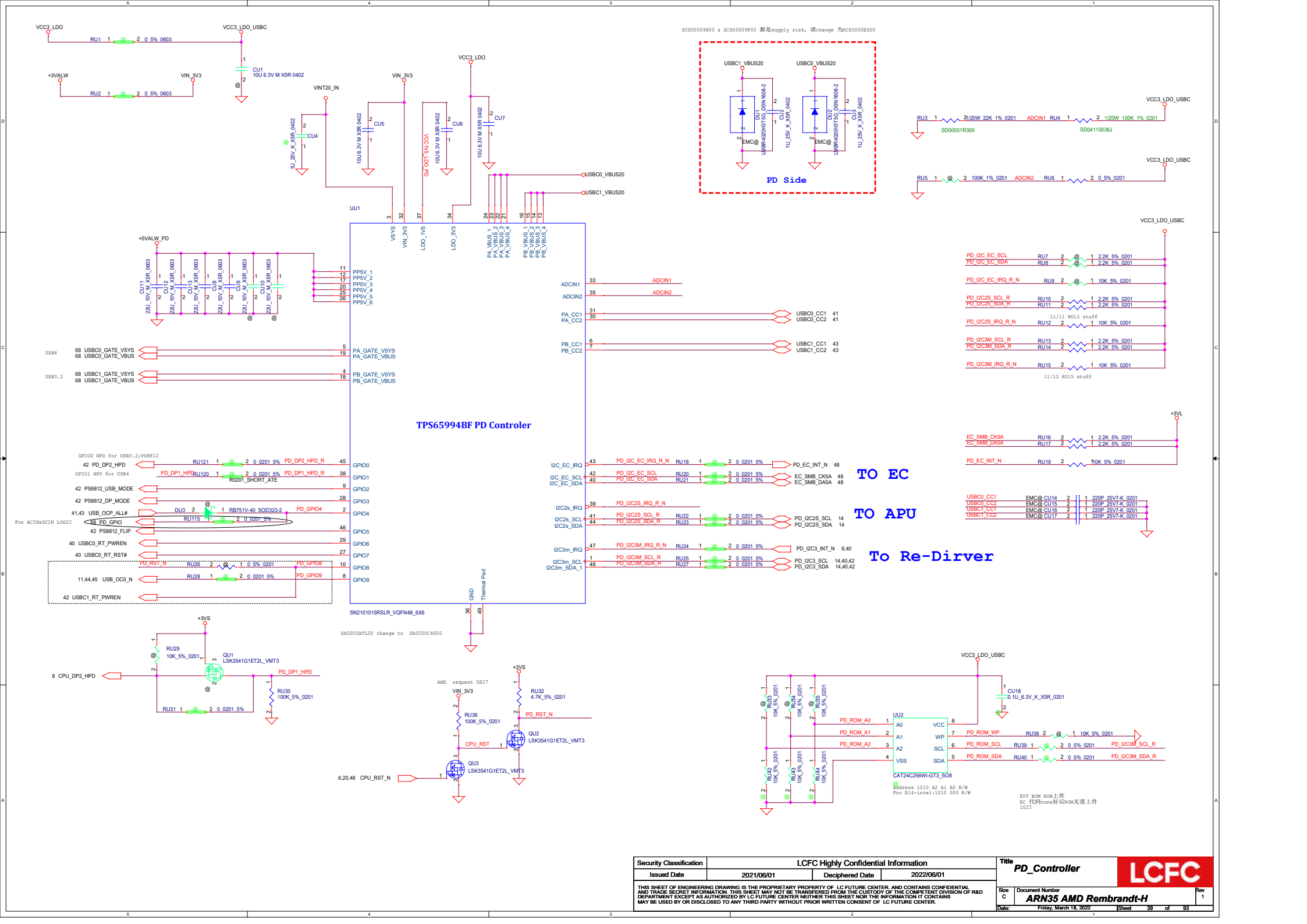
SCS00009800 & SCS00009P00 都是supply risk, 请change 为SCS0000E200
PD Side
TPS65994BF PD Controler
TO EC
TO APU
To Re-Dirver
SN2101015RSLR_VQFN48_6X6
SA0000ATL00 change to SA0000C4600
CAT24C256WI-GT3_SO8
Address 1010 A2 A1 A0 R/W
For E14-intel:1010 000 R/W
EVT BOM ROM上件
EC 代码tune好后ROM无需上件
1023
AMD request 0827
11/11 RU12 stuff
11/12 RU15 stuff
R0201_SHORT_ATE
For ACIN&DCIN LOGIC
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Issued Date
2021/06/01
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2022/06/01
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Title
PD_Controller
LCFC
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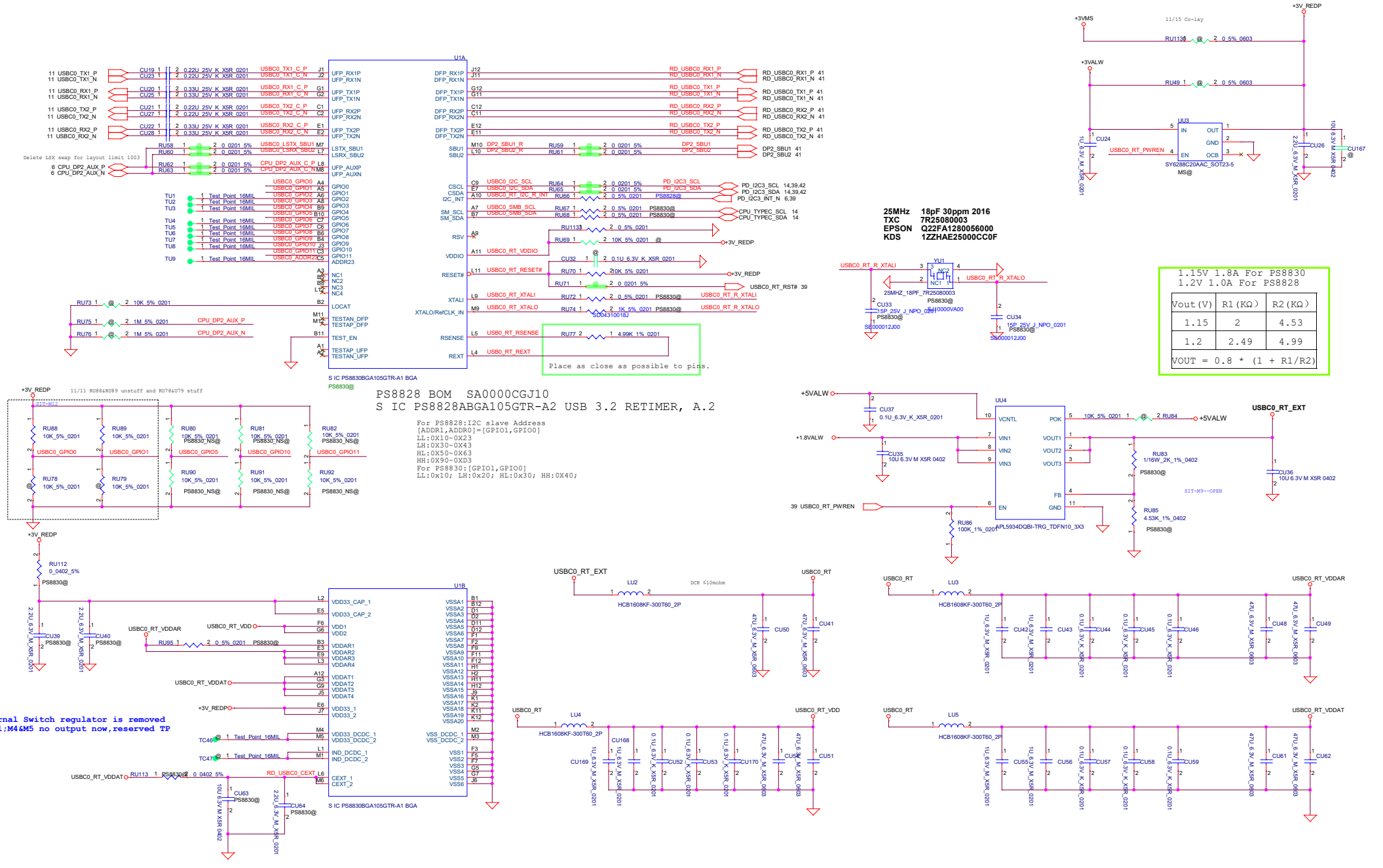
U1A
U1B
PS8828 BOM SA0000CGJ10
S IC PS8828ABGA105GTR-A2 USB 3.2 RETIMER, A.2
For PS8828:I2C slave Address
[ADDR1,ADDR0]=[GPIO1,GPIO0]
LL:0X10~0X23
LH:0X30~0X43
HL:0X50~0X63
HH:0X90~0XD3
For PS8830:[GPIO1,GPIO0]
LL:0x10; LH:0x20; HL:0x30; HH:0X40;
S IC PS8830BGA105GTR-A1 BGA
PS8830@
Place as close as possible to pins.
25MHz 18pF 30ppm 2016
TXC 7R25080003
EPSON Q22FA1280056000
KDS 1ZZHAE25000CC0F
1.15V 1.8A For PS8830
1.2V 1.0A For PS8828
Vout(V) R1(KΩ) R2(KΩ)
1.15 2 4.53
1.2 2.49 4.99
VOUT = 0.8 * (1 + R1/R2)
Internal Switch regulator is removed
L1&M1;M4&M5 no output now,reserved TP
SY6288C20AAC_SOT23-5
APL5934DQBI-TRG_TDFN10_3X3
HCB1608KF-300T60_2P
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Issued Date
2021/06/01
Deciphered Date
2022/06/01
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Title
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LCFC
Size
Custom
Document Number
ARN35 AMD Rembrandt-H
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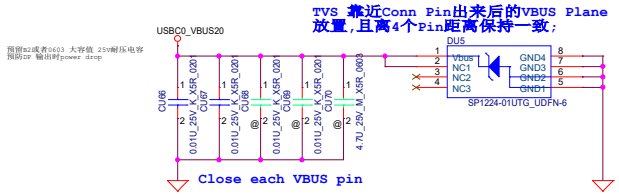

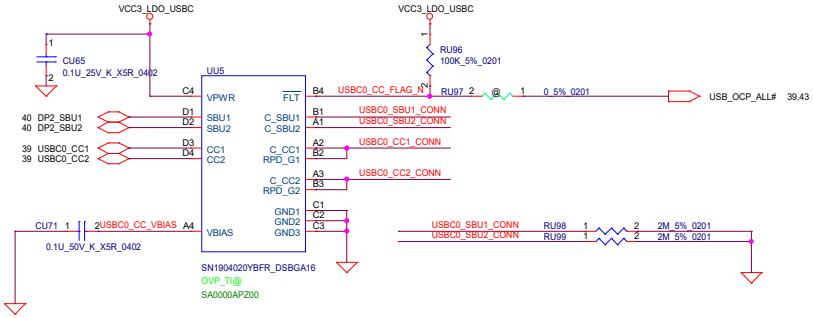

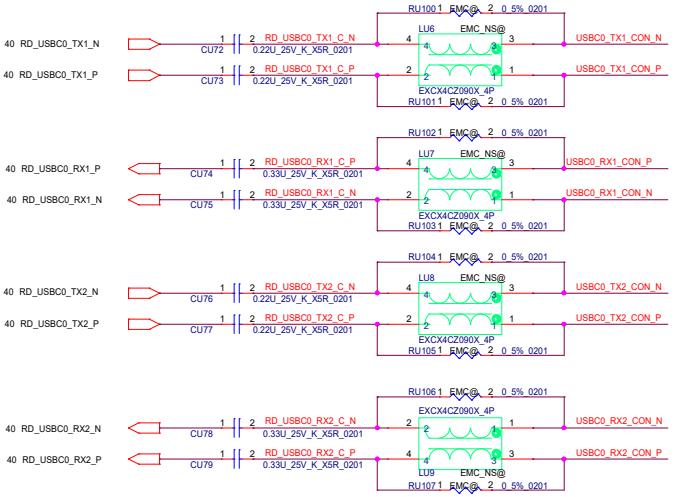

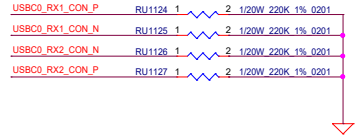

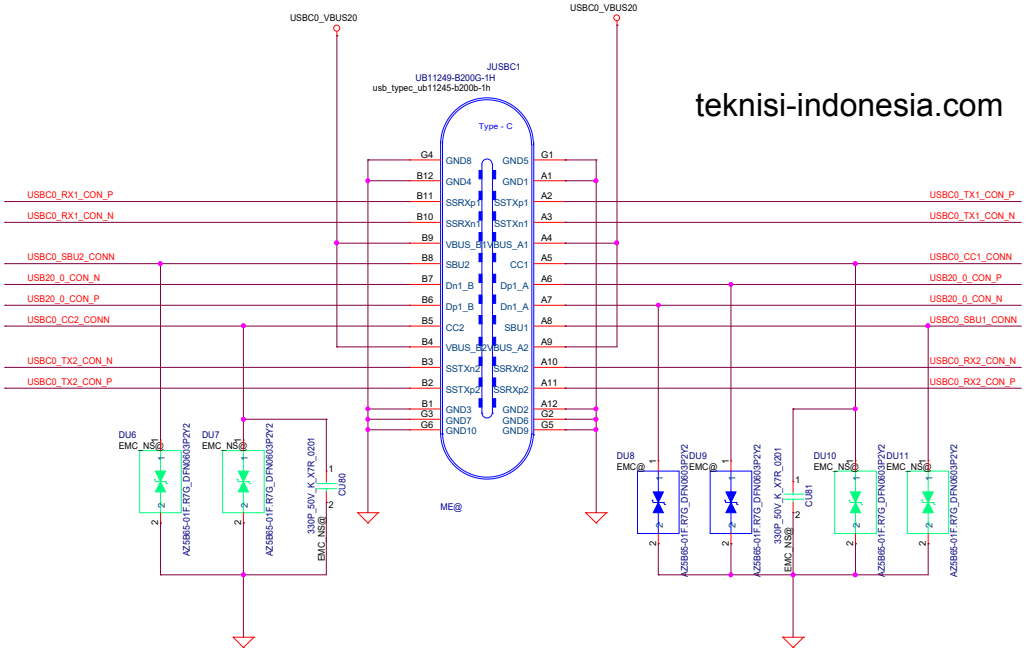

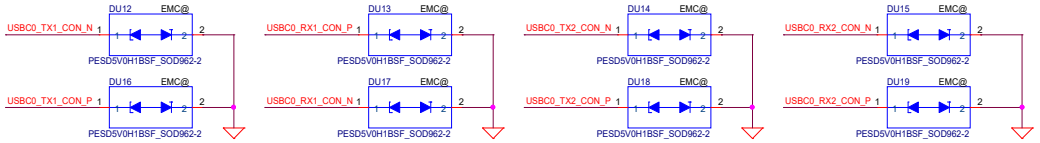

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Title	TYPEC0_CONN		
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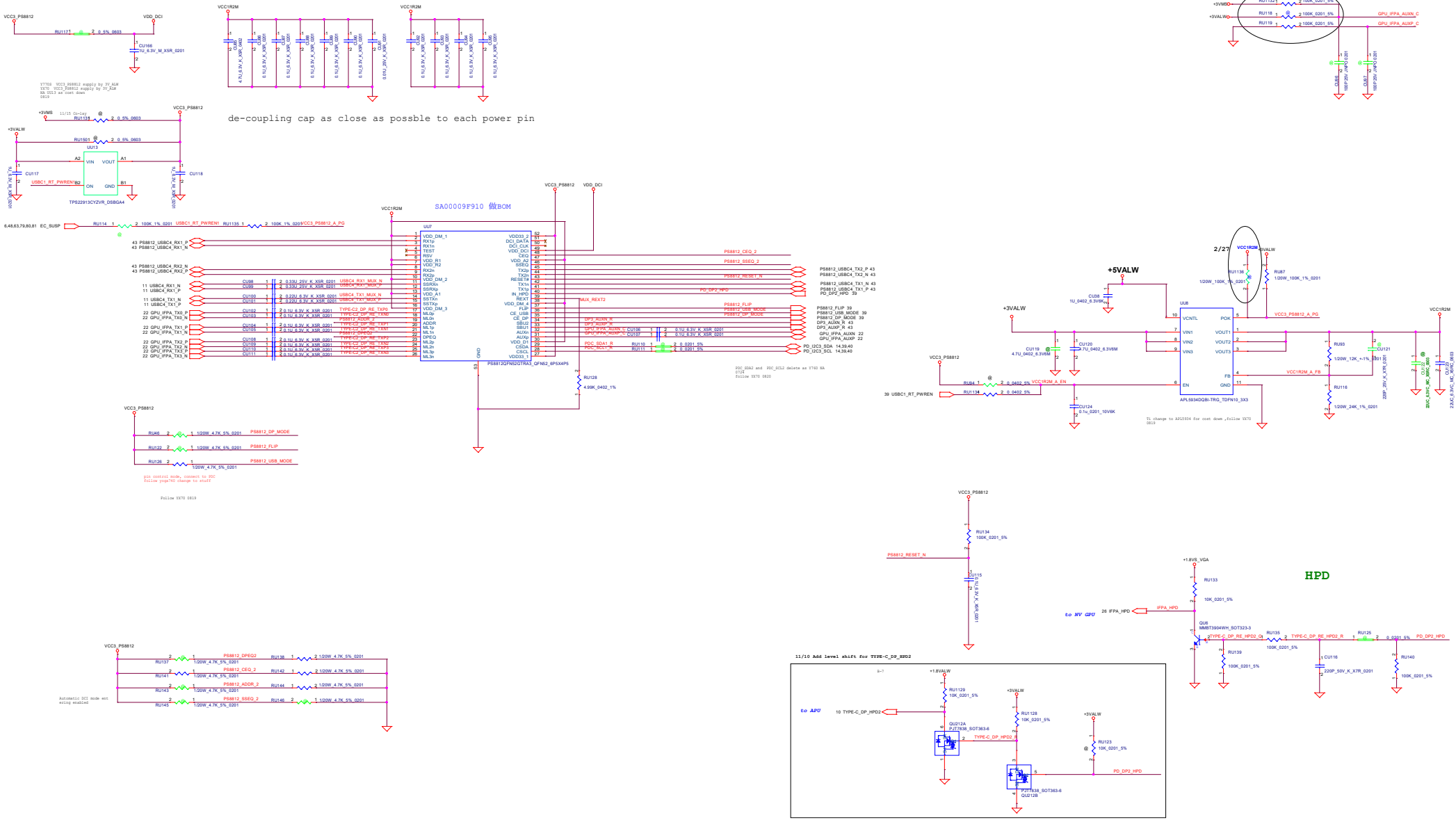

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Size	D	Document Number	ARN35 AMD Rembrandt-H
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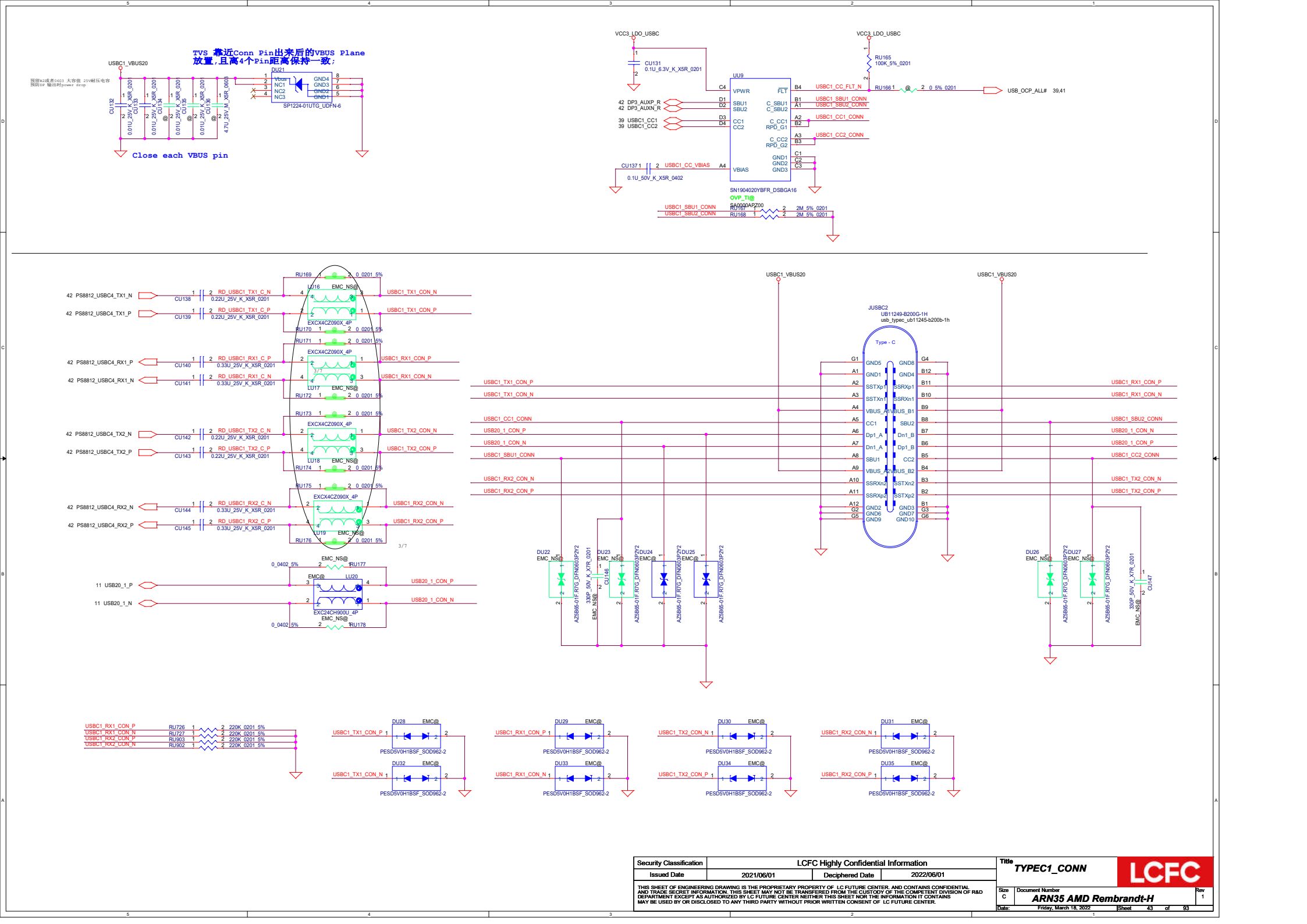

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: TYPEC1_CONN

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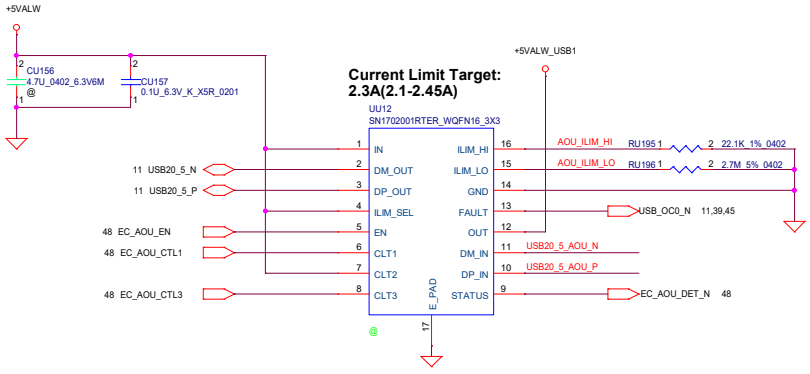

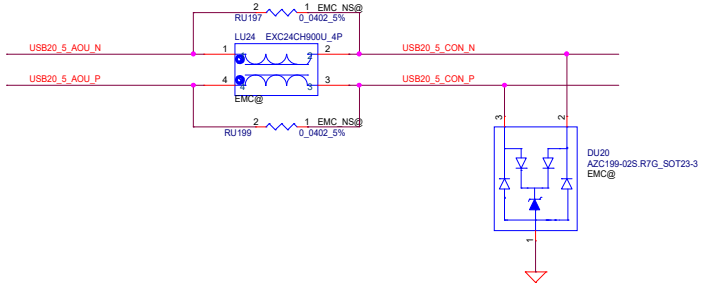

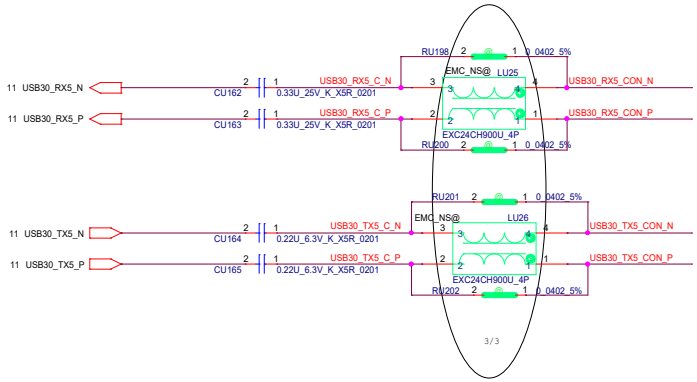

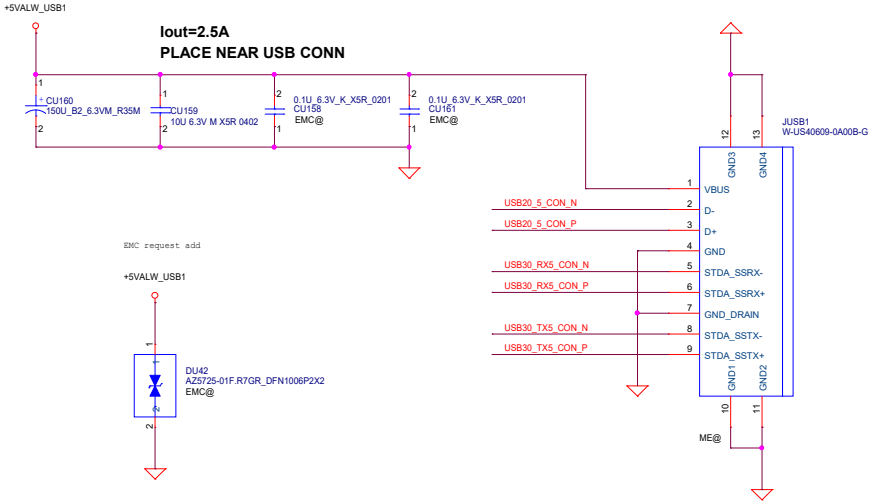

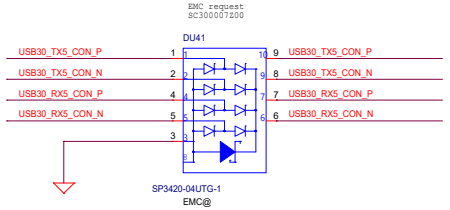

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: USBA_PortB

LCFC

Size	Document Number	Rev
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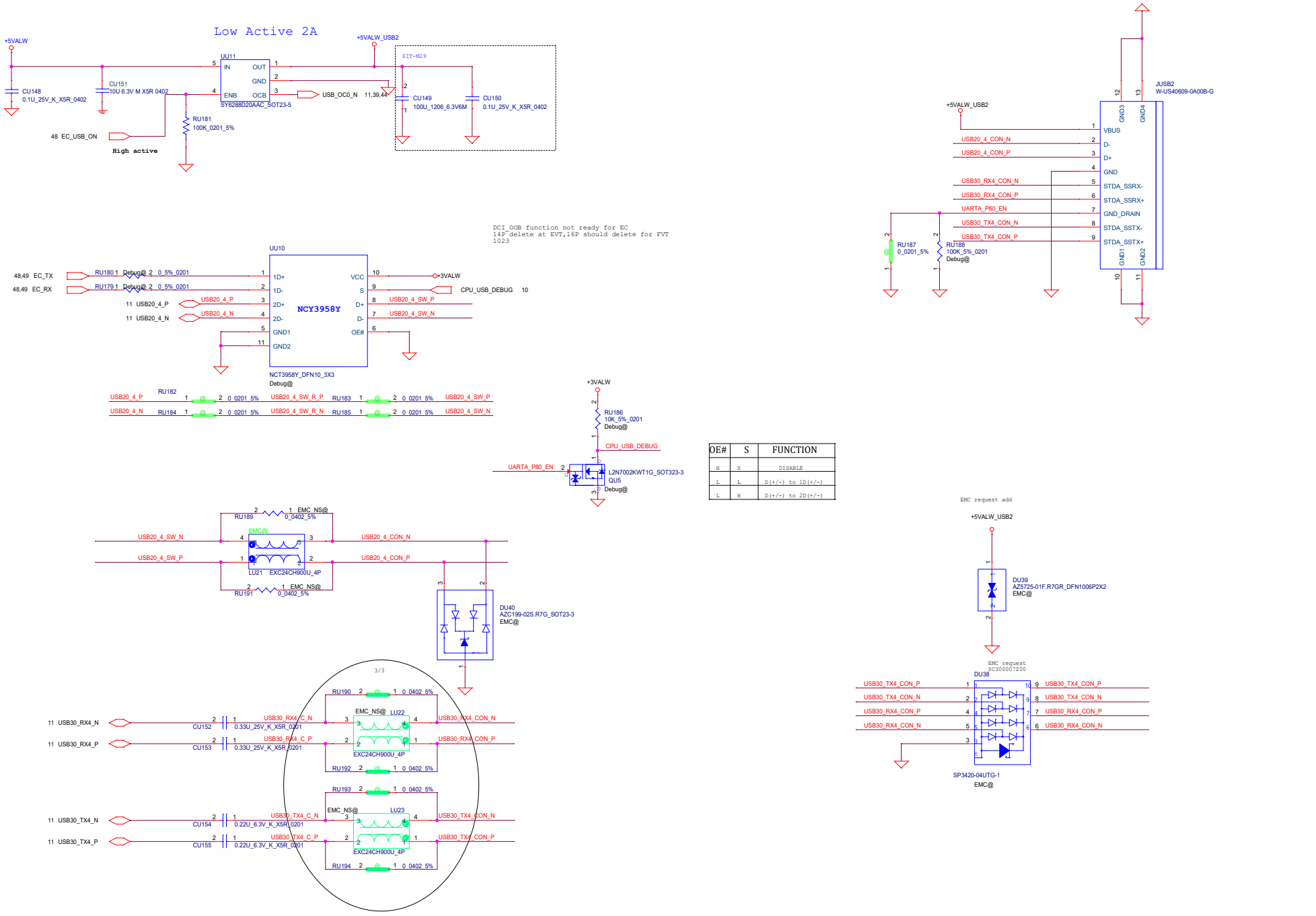

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: *USBA_PortA*

LCFC

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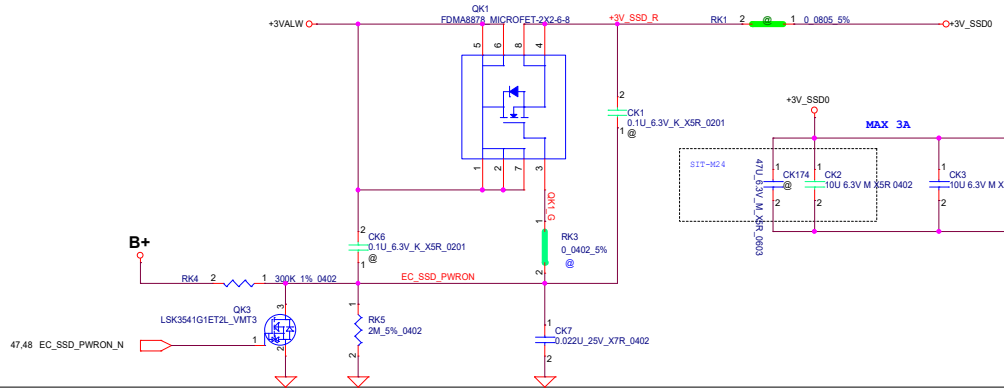
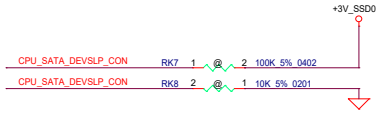
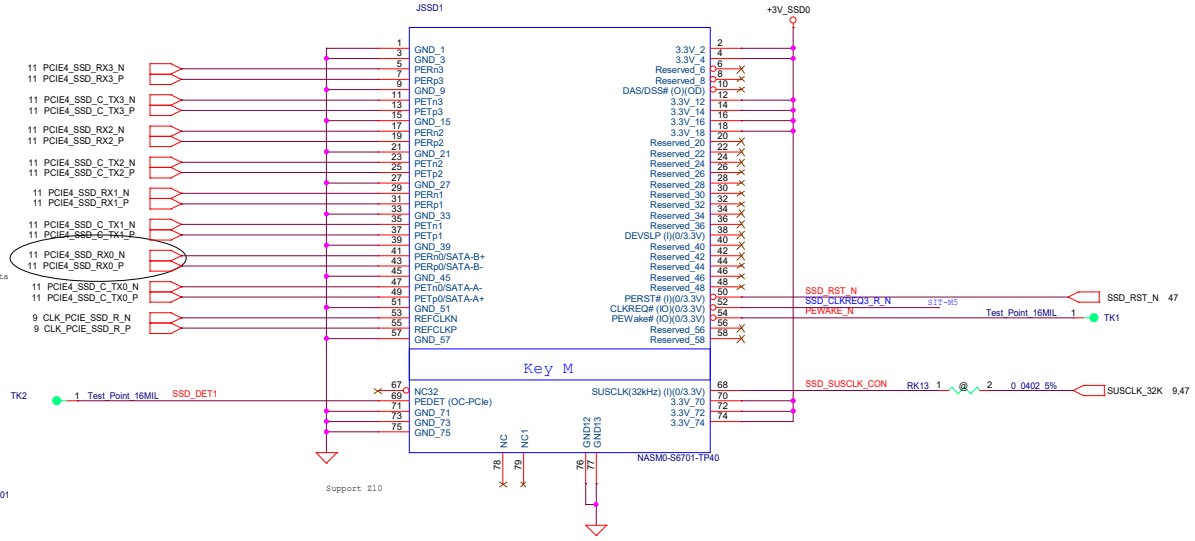
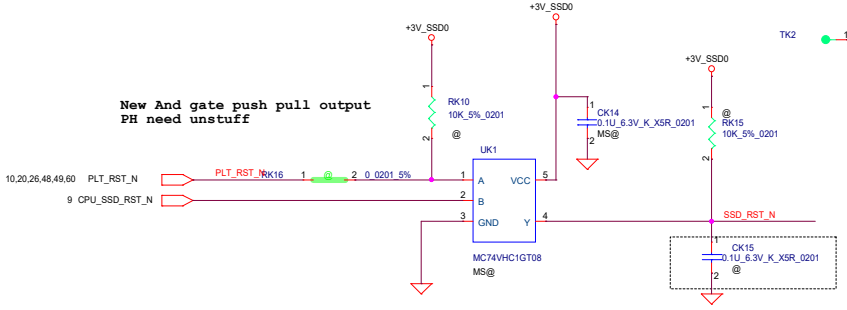


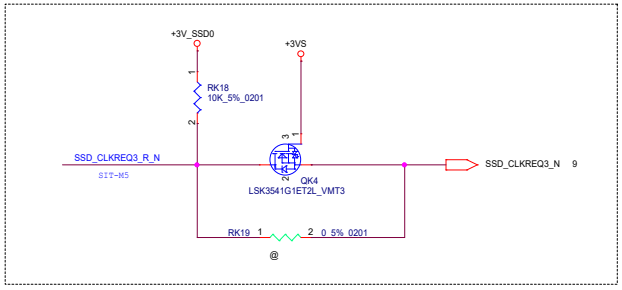






And gate ViH=1.4V(Vcc=3.3V)

74AHC1G08 VIH=2.0V when VCC=3.3V,不可替代



Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

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C	ARN35 AMD Rembrandt-H		1
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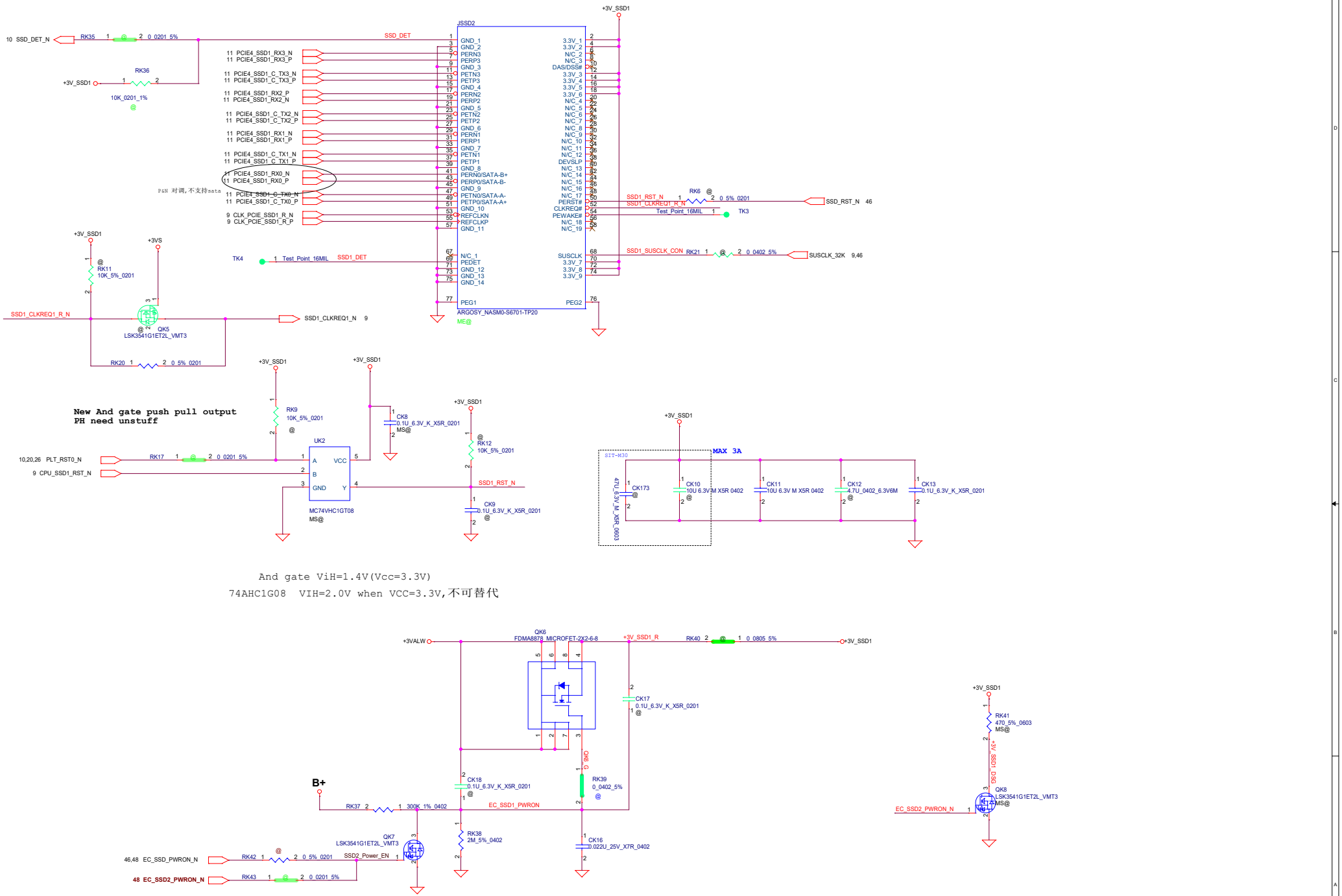


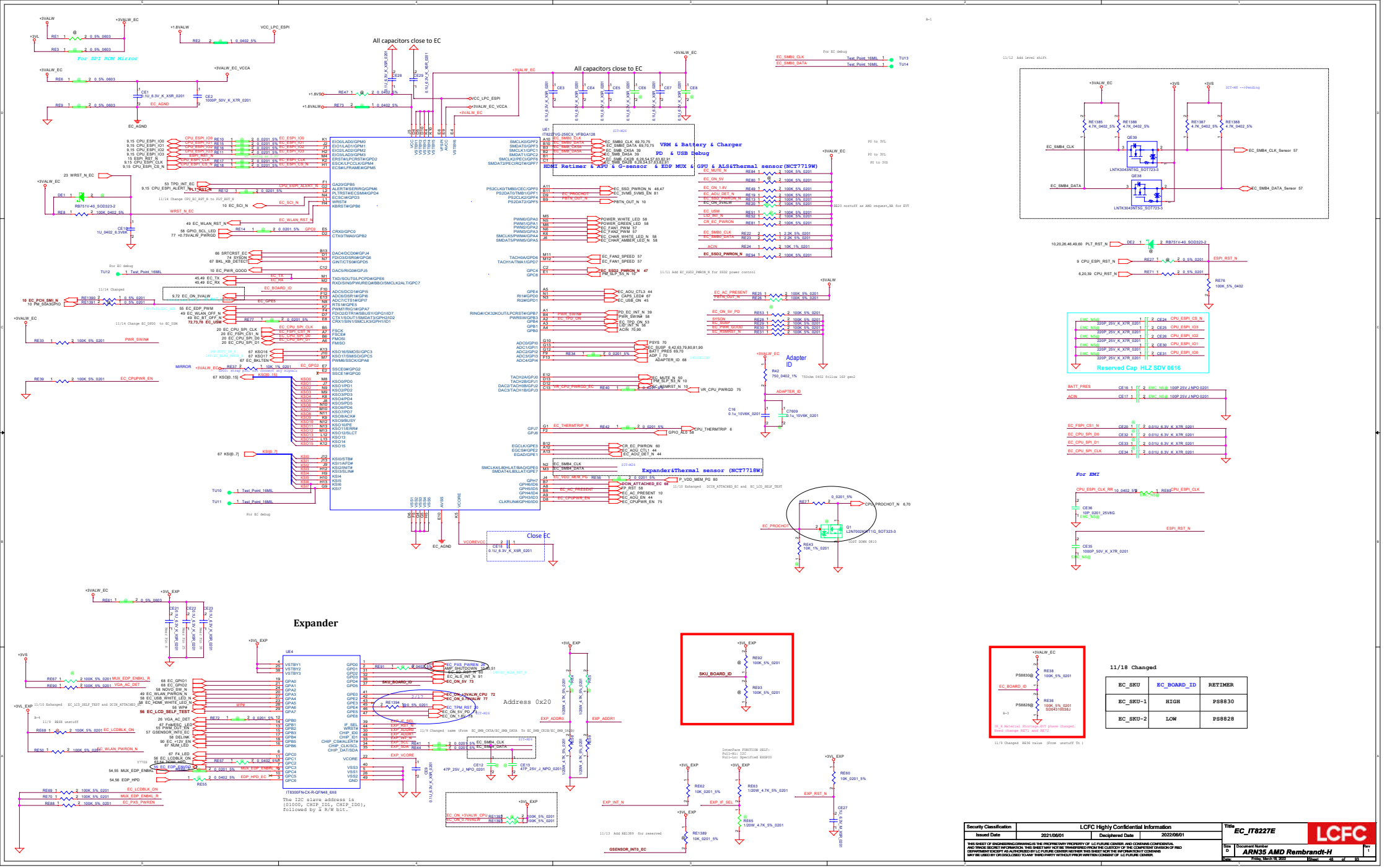
Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: M.2 SSD1

LCFC

Size	Document Number	Rev
C	ARN35 AMD Rembrandt-H	1

Date: Friday, March 18, 2022 Sheet 47 of 93


All capacitors close to EC
All capacitors close to EC
For SPI ROM Mirror
VRM & Battery & Charger
PD & USB Debug
HDMI Retimer & APU & G-sensor & EDP MUX &
GPU & ALS&Thermal sensor(NCT7719W)
Expander&Thermal sensor (NCT7719W)
Adapter ID
Reserved Cap HLZ SDV 0616
For EMI
Close EC
Expander
Address 0x20
The I2C slave address is (01000, CHIP_ID1, CHIP_ID0), followed by a R/W bit.
SKU_BOARD_ID
EC_BOARD_ID
11/18 Changed
EC_SKU | EC_BOARD_ID | RETIMER
EC_SKU-1 | HIGH | PS8830
EC_SKU-2 | LOW | PS8828
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Size D
Document Number ARN35 AMD Rembrandt-H
Rev 1
Date: Friday, March 18, 2022
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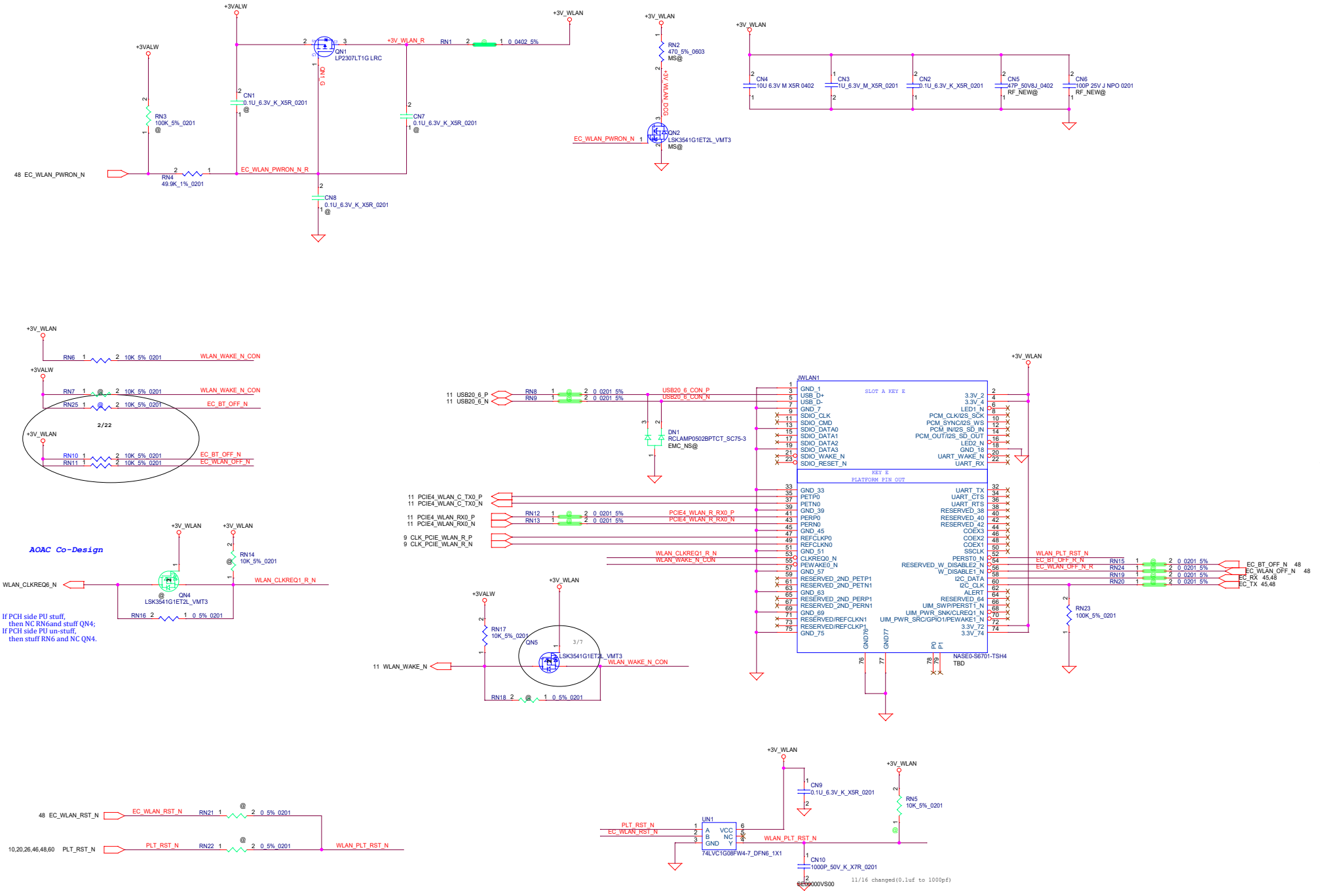

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Title: *M.2 WLAN*

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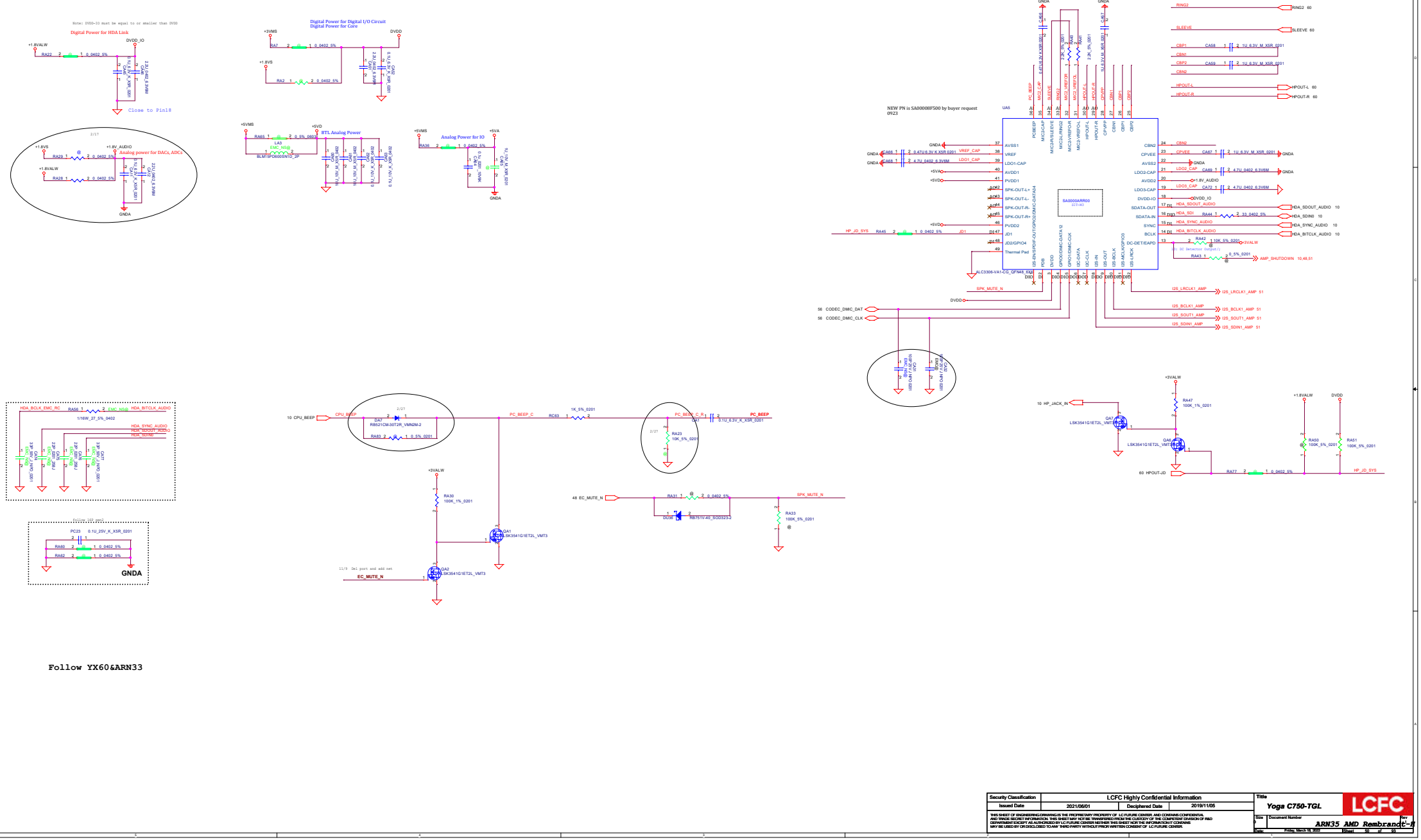
Size	Document Number	Rev
C	*ARN35 AMD Rembrandt-H*	1

Date: Friday, March 18, 2022 Sheet 49 of 93



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Issued Date	2021/06/01	Deciphered Date	2019/11/05

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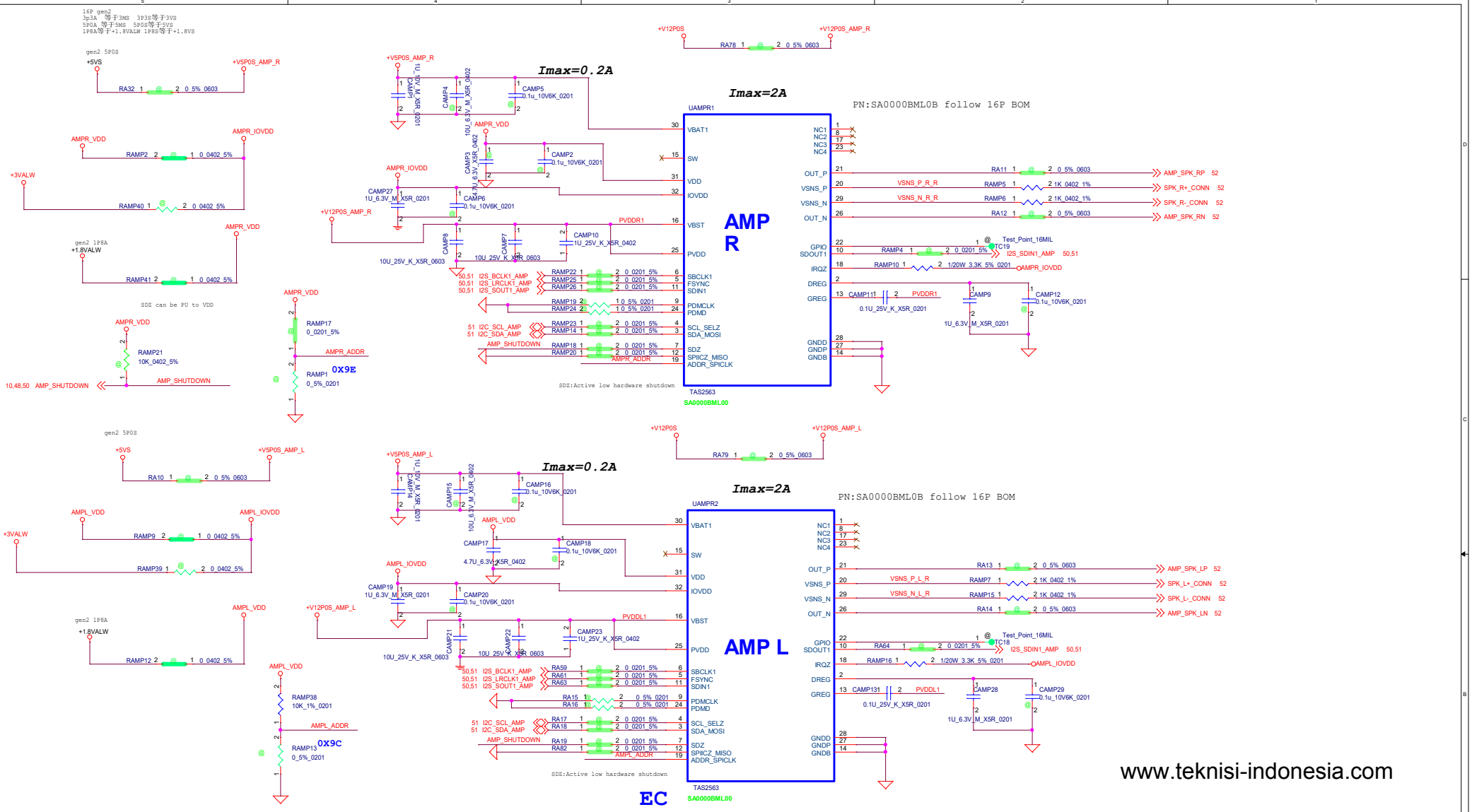
Title: Yoga C750-TGL

LCFC

Size: D | Document Number: ARN35 AMD Rembrandt-R | Rev:

Date: Friday, March 18, 2022 | Sheet 50 of 93



Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: AMP

LCFC

Size	Document Number	Rev
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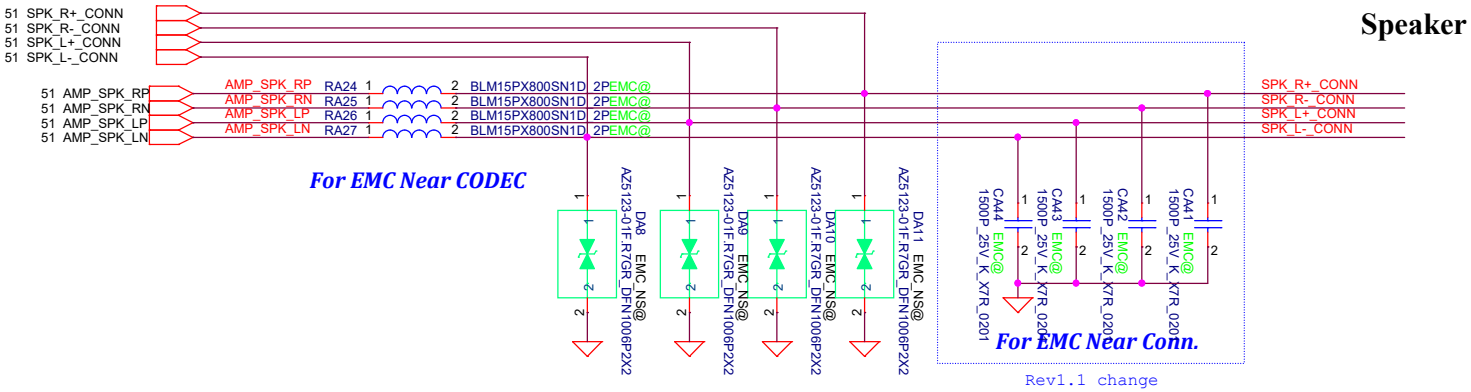
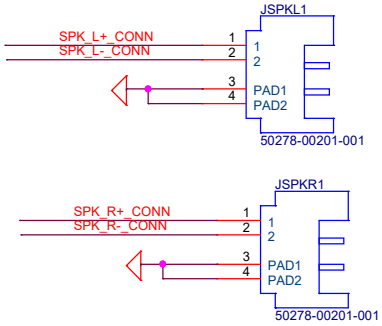
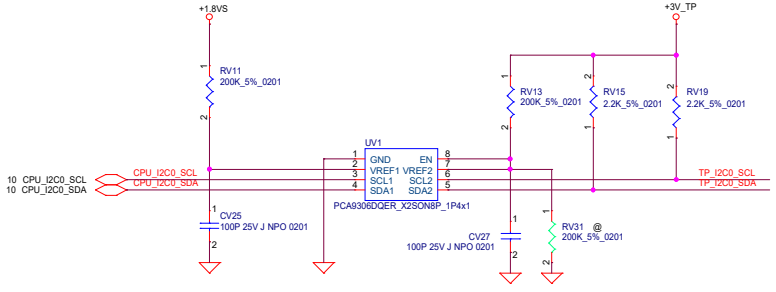
Speaker

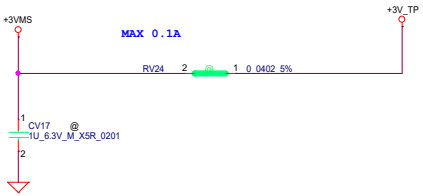




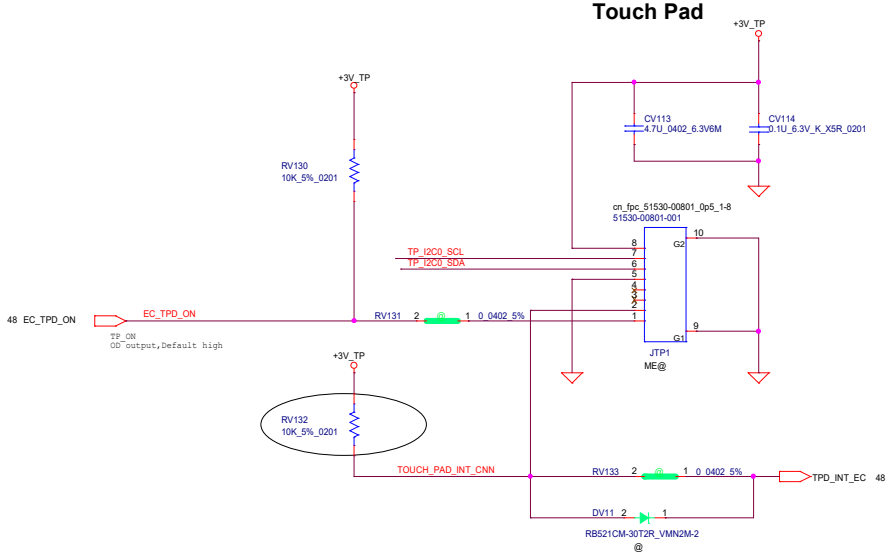
Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title	Audio_SPK/Jack		
Size B	Document Number ARN35 AMD Rembrandt-H		Rev 1
Date: Friday, March 18, 2022	Sheet 52 of 93		



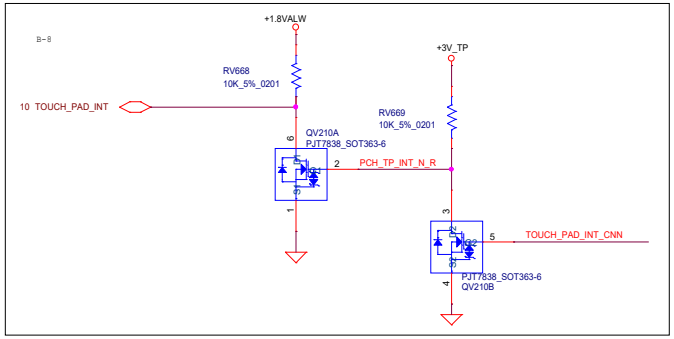


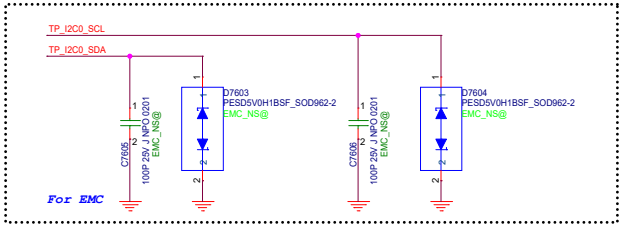
Touch Pad



Pin Number	Pin Name	Description
1	VDD	Power
2	I2C-CLK	I2C_Clock
3	I2C-DAT	I2C_Data
4	GND	Ground
5	N/C	N/C
6	N/C	N/C
7	ATTN	Attention/Interrupt (Active Low, Open Drain)
8	LID CLOSE	Input for LID Close event/Disable Touch Pad (Active Low)

11/10 Add level shift for Touchpad_INT





Follow Y770S

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Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: TouchPad CONN

LCFC

Size	Document Number	Rev
C	ARN35 AMD Rembrandt-H	1

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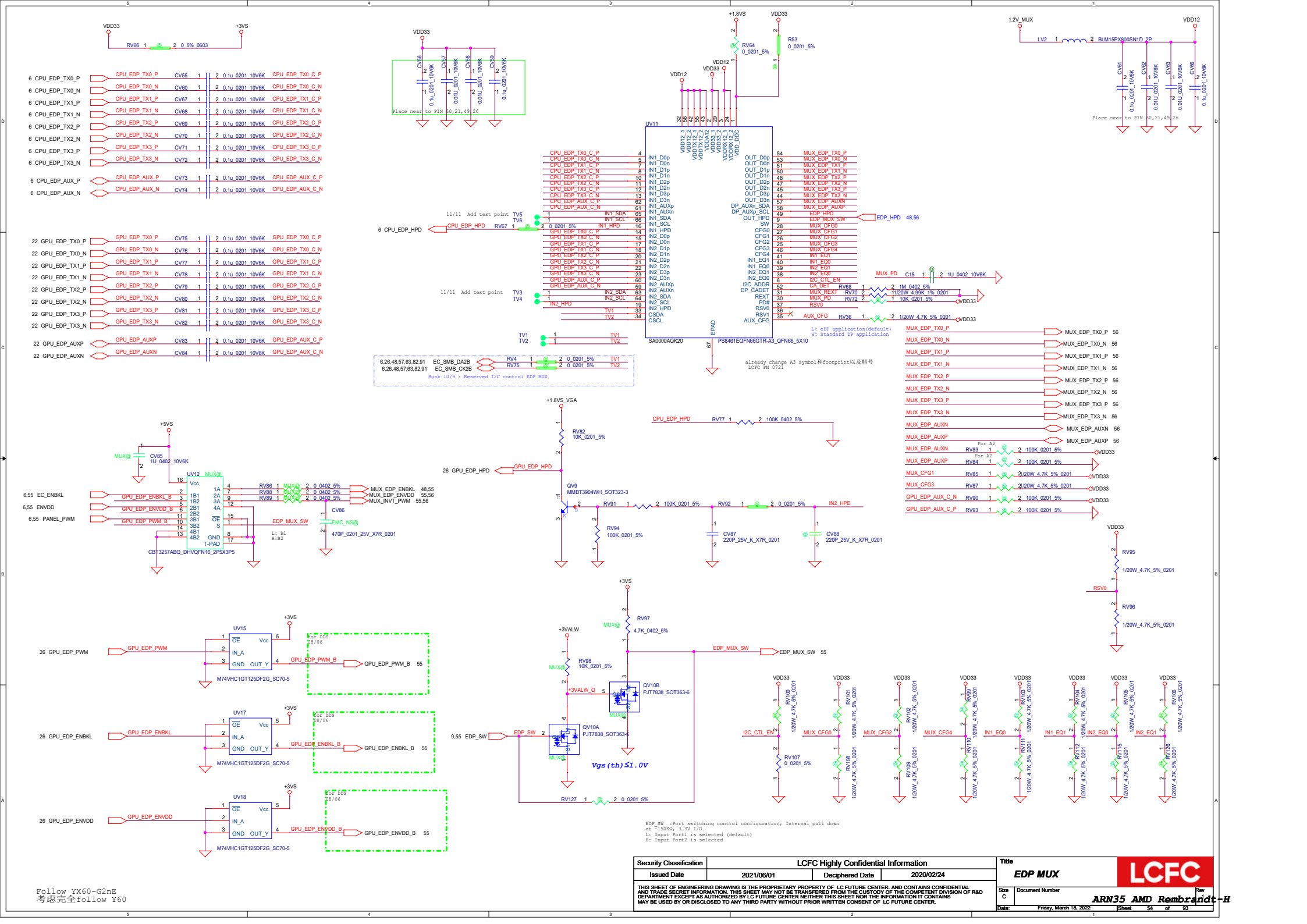
UV11
PS8461EQFN66GTR-A3_QFN66_5X10
UV12 MUX@
CBT3257ABQ_DHVQFN16_2P5X3P5
UV15
UV17
UV18
M74VHC1GT125DF2G_SC70-5
QV9 MMBT3904WH_SOT323-3
QV10A PJT7838_SOT363-6
QV10B PJT7838_SOT363-6
Vgs(th)≤1.0V
EDP_SW :Port switching control configuration; Internal pull down at ~150KΩ, 3.3V I/O.
L: Input Port1 is selected (default)
H: Input Port2 is selected
Follow YX60-G2nE
考虑完全follow Y60
Security Classification
LCFC Highly Confidential Information
Issued Date
2021/06/01
Deciphered Date
2020/02/24
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EDP MUX
LCFC
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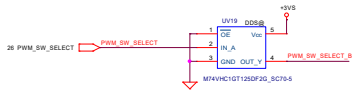
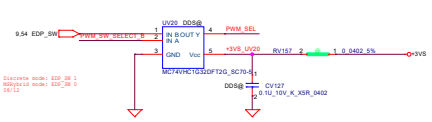
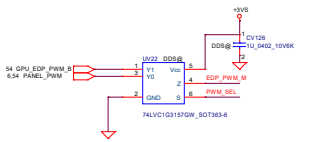
need fine tune RG107 RG108 RG88 BOM structure
08/08

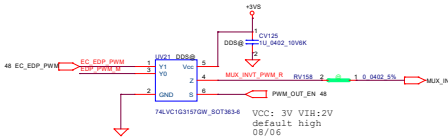
EDP PWM LOGIC CONTROL



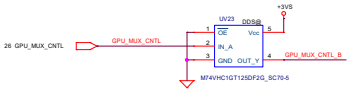


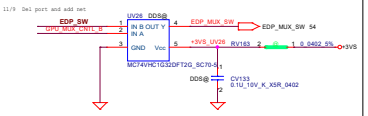


S	z
H	Y1
L	Y0

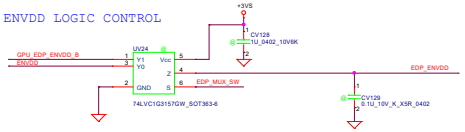


VCC: 3V VIH:2V
default high
08/06



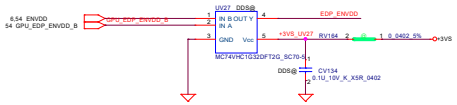


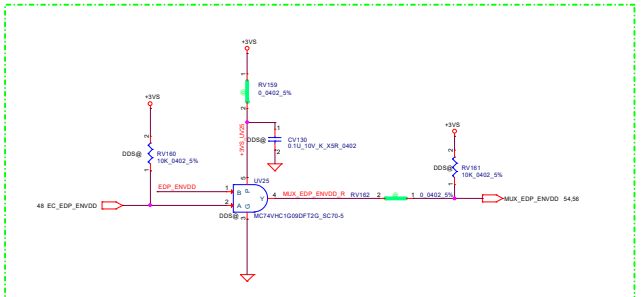
Co-lay EDP ENVDD LOGIC CONTROL



EDP ENVDD LOGIC CONTROL

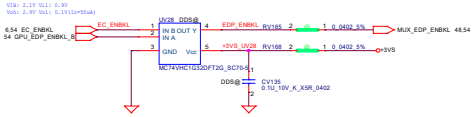
VIH: 2.1V Vil: 0.9V
Voh: 2.9V Vol: 0.1V(Io=50uA)

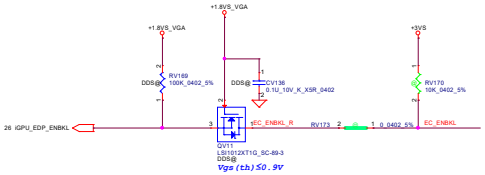




EDP backlight LOGIC CONTROL

VIH: 2.1V Vil: 0.9V
Voh: 2.9V Vol: 0.1V(Io=50uA)

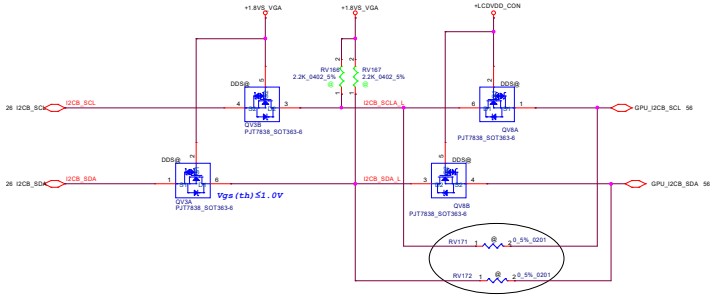




Vgs(th)≤0.9V

GPU drive need read IGPU backlight state for DDS driver;

level shift for I2C



Vgs(th)≤1.0V

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Title	DC V TO VS INTERFACE	LCFC	
Size D	Document Number ARN35 AMD Rembrandt-H		Rev 1
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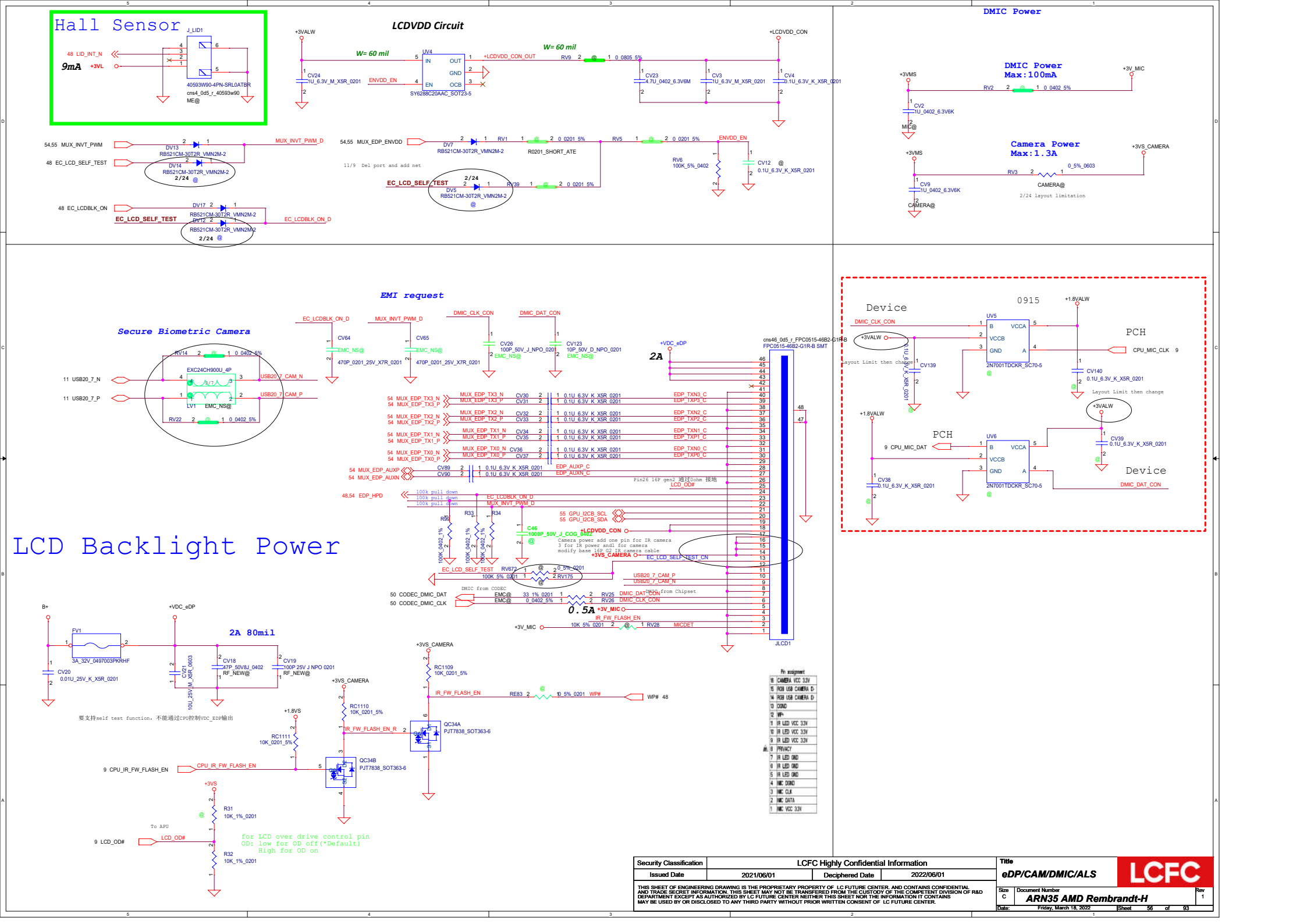

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Title	eDP/CAM/DMIC/ALS		
Size	Document Number		Rev
C	ARN35 AMD Rembrandt-H		1
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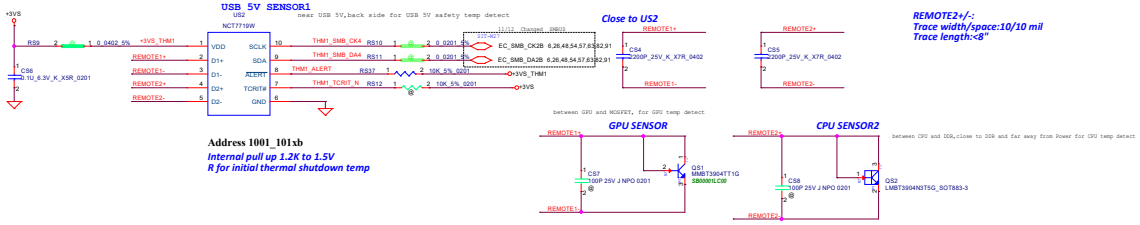
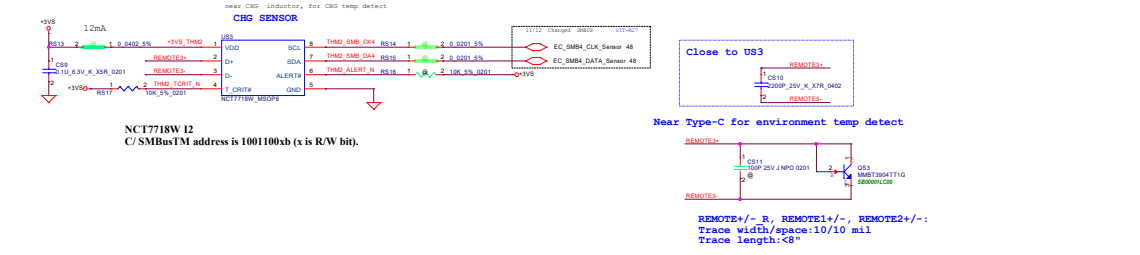
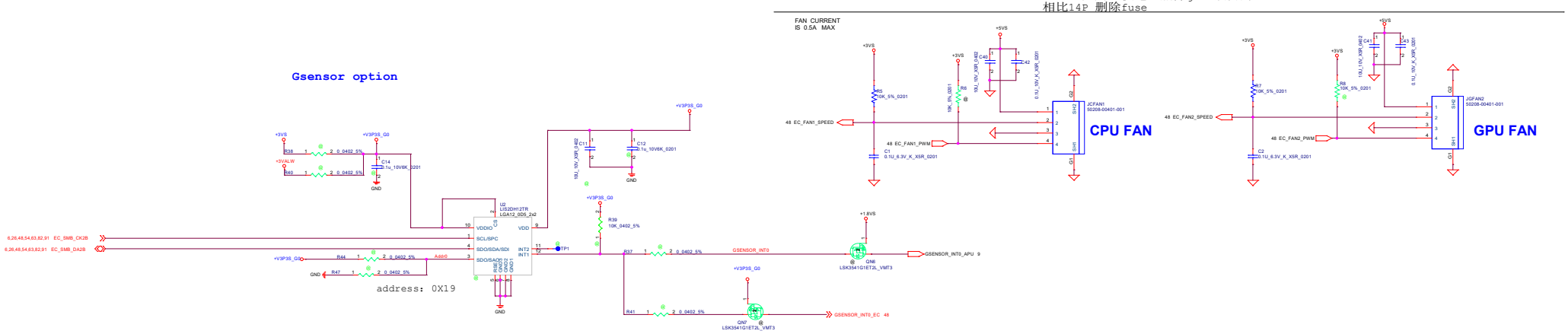


Delete Q8 G753T11U for layout optimize 0928



FAN 只用5V供电，删除gen2预留的12V
相比14P 删除fuse



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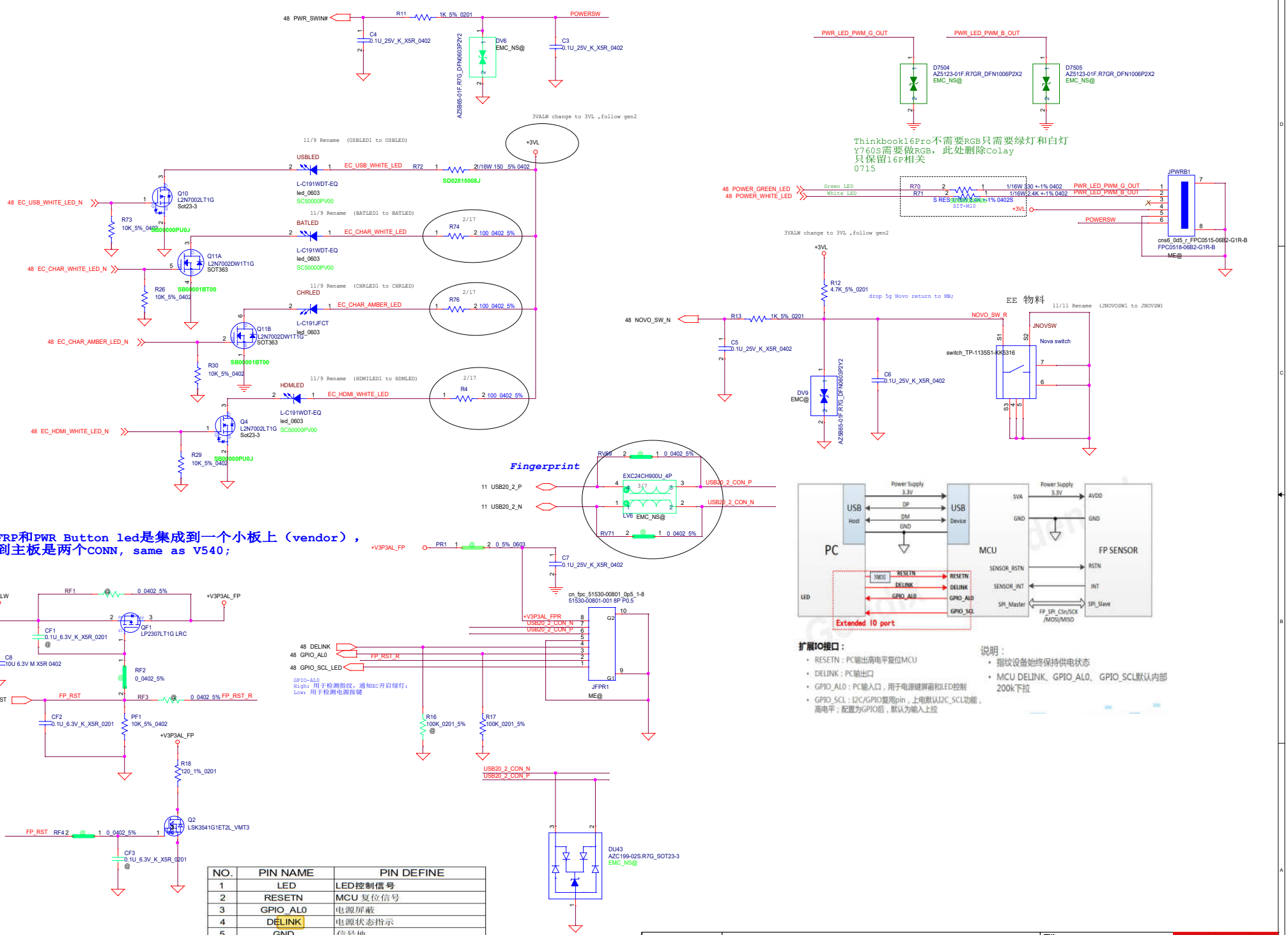
Title	Thermal		
Size	Document Number		Rev
D	ARN35 AMD Rembrandt-H		1
Date:	Friday, March 18, 2022	Sheet	57 of 93



NO.	PIN NAME	PIN DEFINE
1	LED	LED控制信号
2	RESETN	MCU 复位信号
3	GPIO_AL0	电源屏蔽
4	DELINK	电源状态指示
5	GND	信号地
6	DP	USB信号DP
7	DM	USB信号DM
8	D3V3	3.3V电源

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Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: BATTERY LED

LCFC

Size	Document Number	Rev
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Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: ***Blank***

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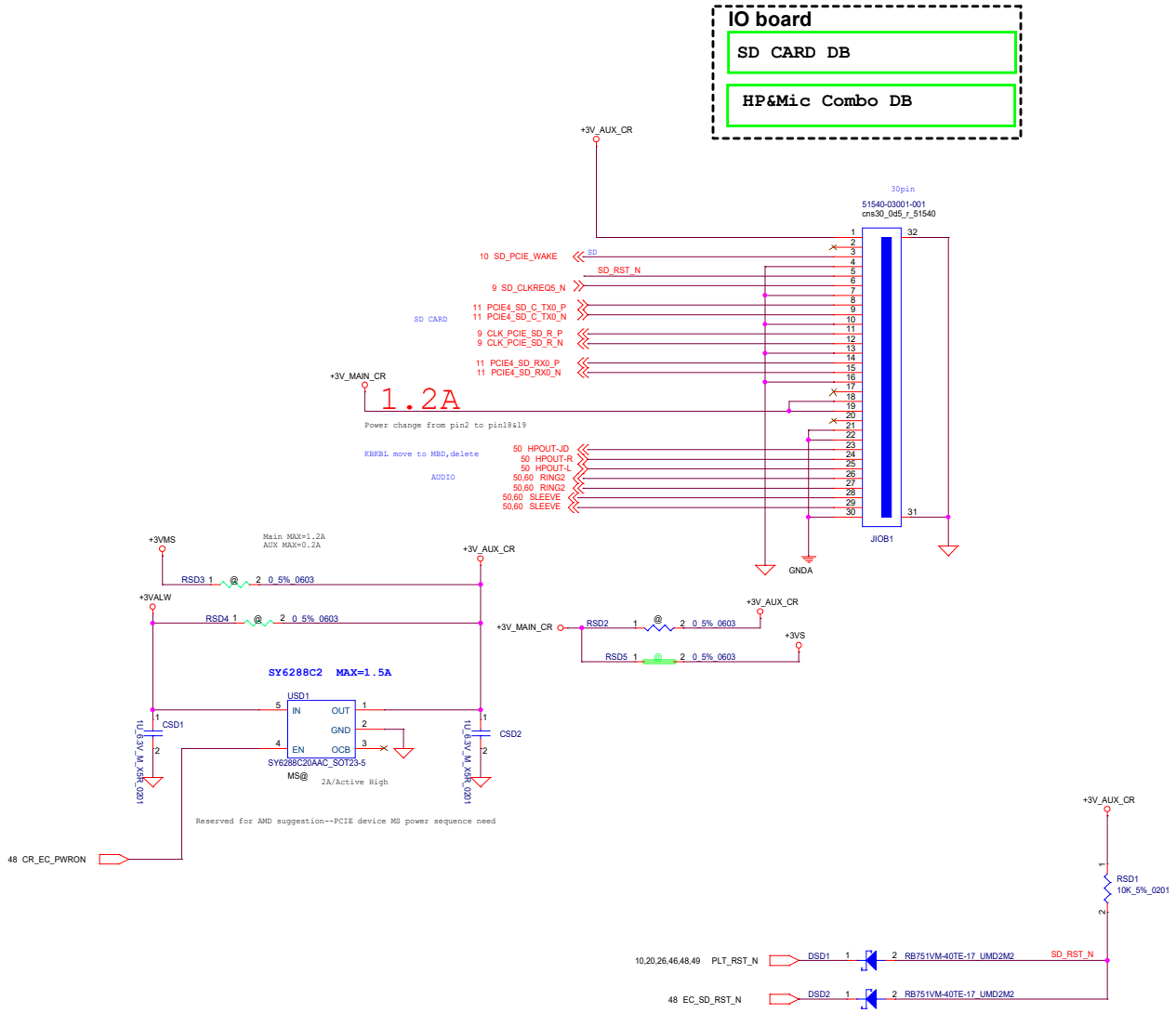
Size	Document Number	Rev
C	***ARN35 AMD Rembrandt-H***	1

Date: Friday, March 18, 2022 | Sheet 59 of 93



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Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: Blank

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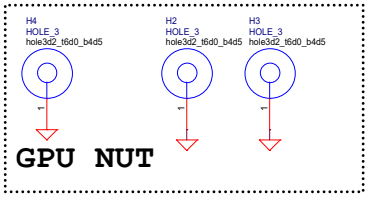
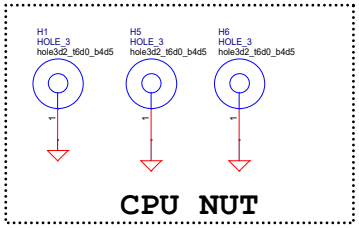
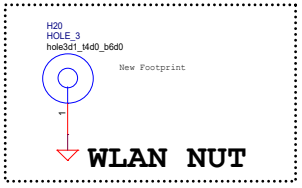
Memory Shielding



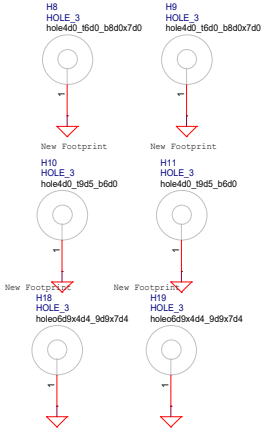


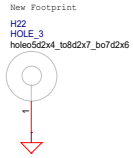
Delete 0728
check with ME winters

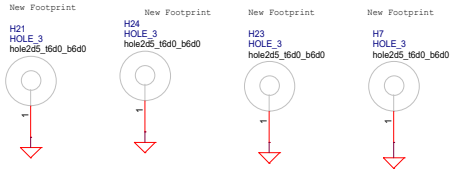


hole3d2_t6d0_b4d5 x6--CPU&GPU
hole3d1_t4d0_b4d6 x1--wlan

hole4d0_t6d0_b8d0x7d0 x2
holeo5d2x4_to9d2x8_bo7d2x6 x1
hole4d0_t9d5_b6d0 x2
holeo6d9x4d4_9d9x7d4x2
hole2d5_t6d0_b6d0 x4

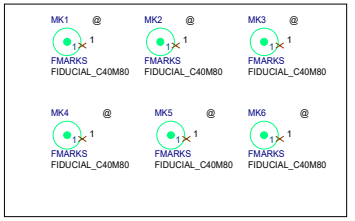






MB HOLE
not install

optical dot
top 3pcs
bot 3pcs



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Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title	Hole/Shielding		LCFC
Size C	Document Number ARN35 AMD Rembrandt-H		Rev 1
Date: Friday, March 18, 2022	Sheet 61 of 93		

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

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Size	Document Number	Rev
C	***ARN35 AMD Rembrandt-H***	1

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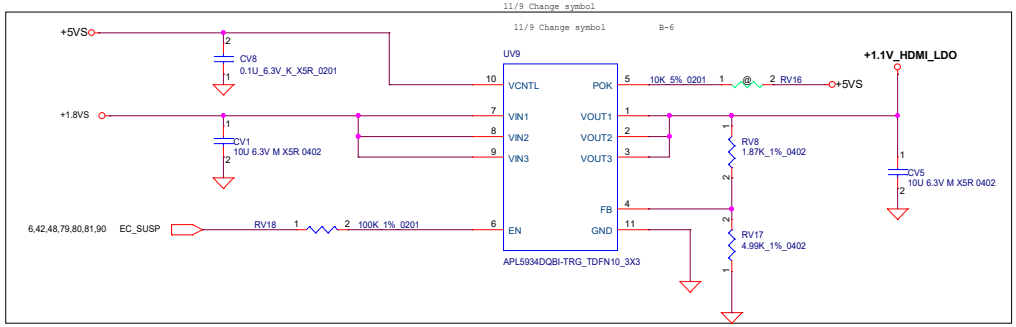
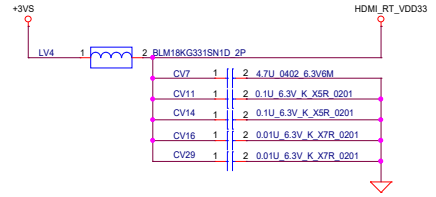
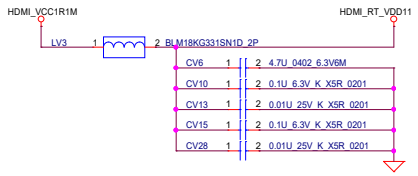
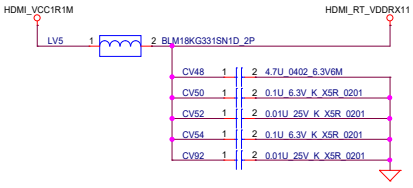
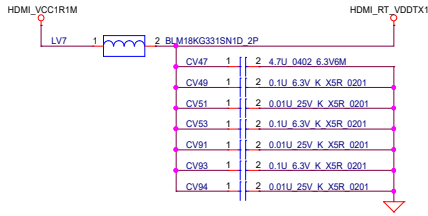
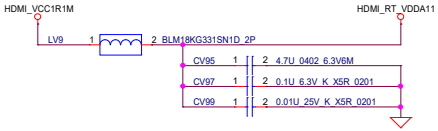


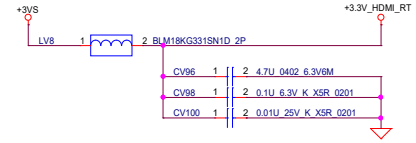




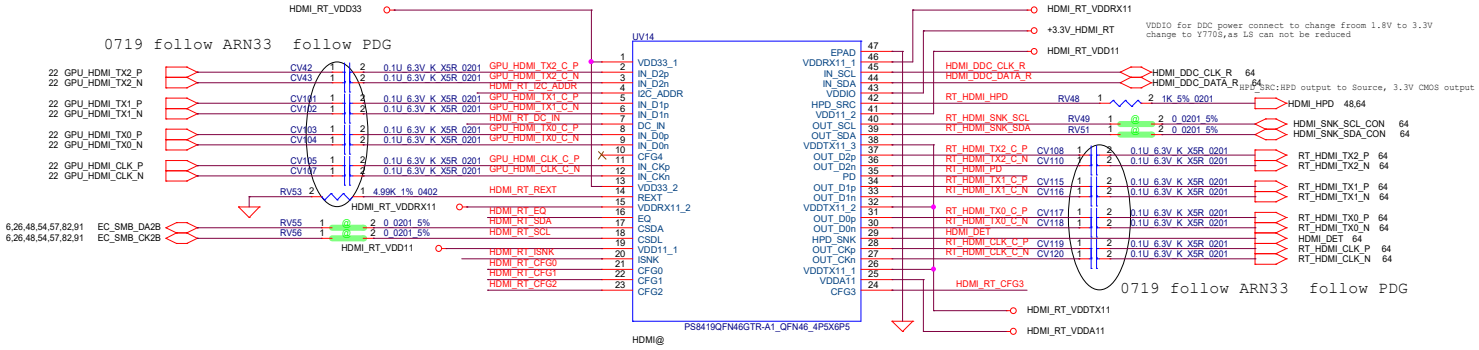


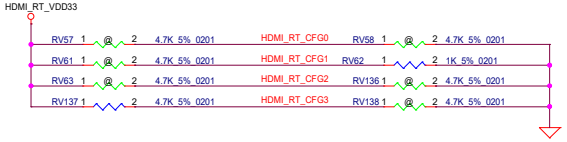


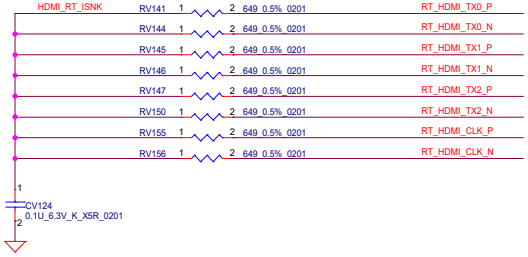


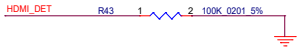


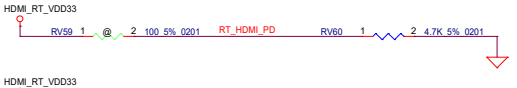
HDMI2.1 Re-timer

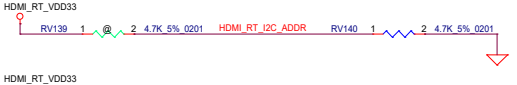


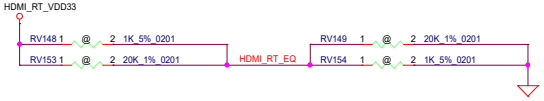












PD =
L:Normal Operation
H:Chip Power-down

I2C_ADDR =
L:0x10 - 0x2F (Default).
M:0x30 - 0x4F .
H:0x90 - 0xAF

DC_IN =
L:HDMI Input is AC Coupled.
H:HDMI Input is DC Coupled.

EQ=
L0: Pull Down with 1k, EQ=19dB
L1: Pull Down with 20k, EQ=18dB
L2: Floating, EQ=16dB
L3: Pull Up with 20k, EQ=13dB
L4: Pull Up with 1k, EQ=7dB

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title	HDMI2.1_RETIMER		
Size	Document Number		Rev
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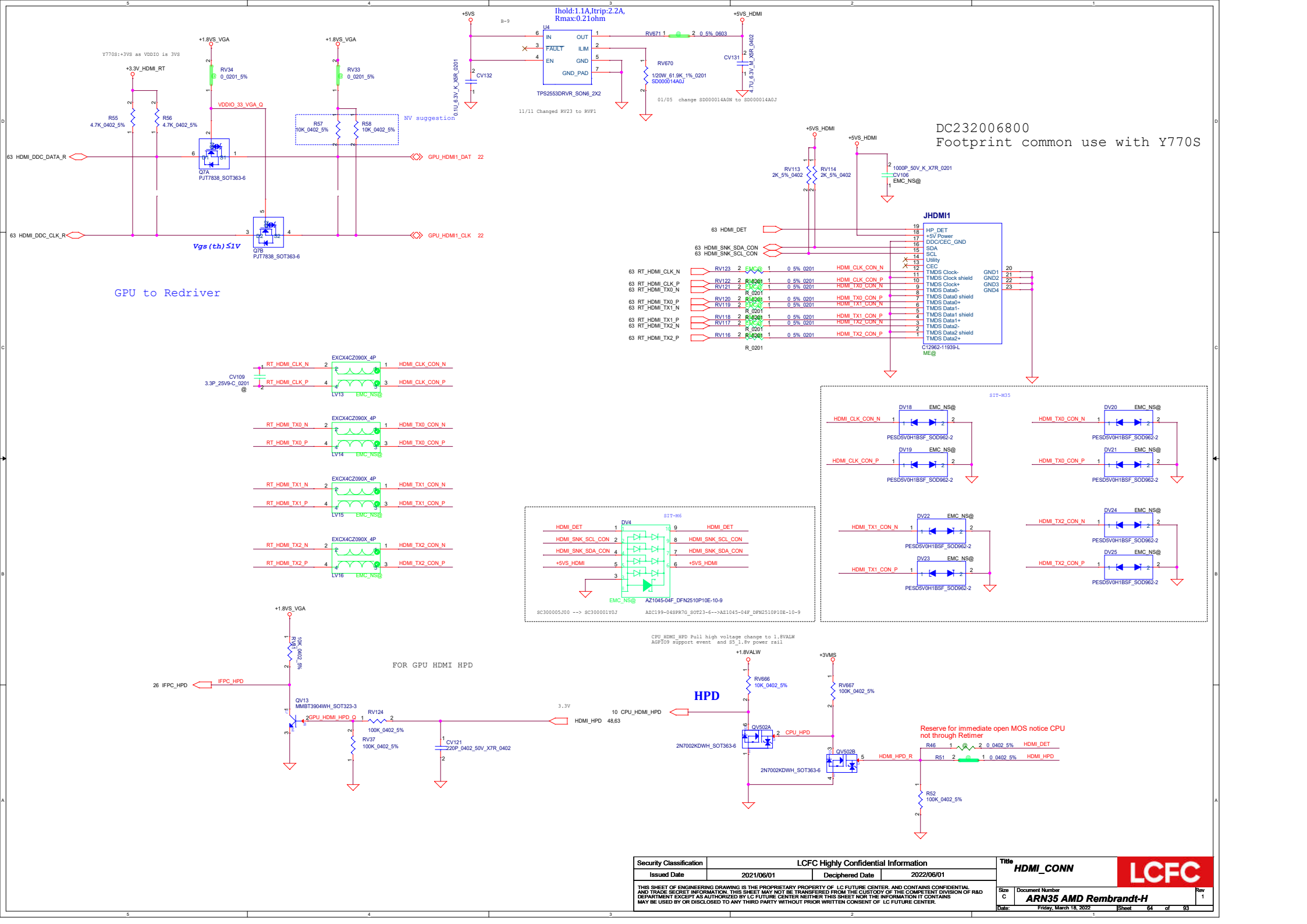

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: HDMI_CONN

LCFC

Size	Document Number	Rev
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Title: ***TOF HUB***

LCFC

Size	Document Number	Rev
C	***ARN33 AMD Rembrandt-H***	1

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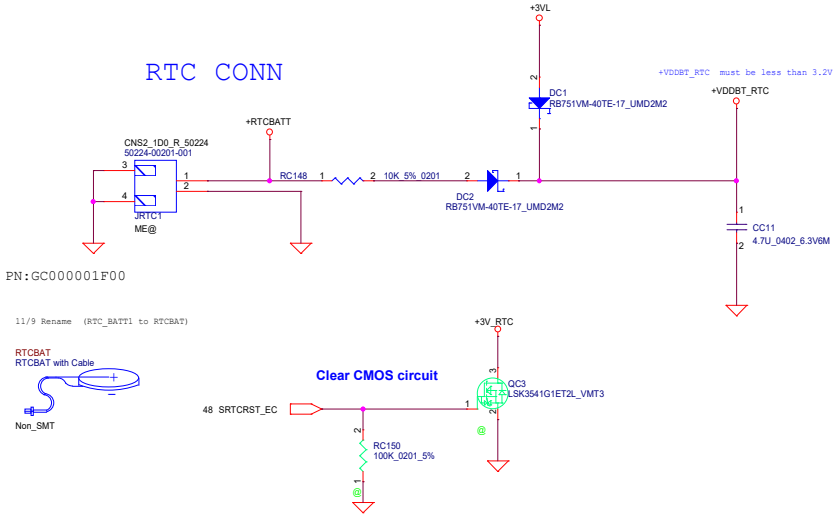

Copy from BLD 0714
RTC reset 需要预留

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: RTC

LCFC

Size	Document Number	Rev
C	ARN35 AMD Rembrandt-H	1

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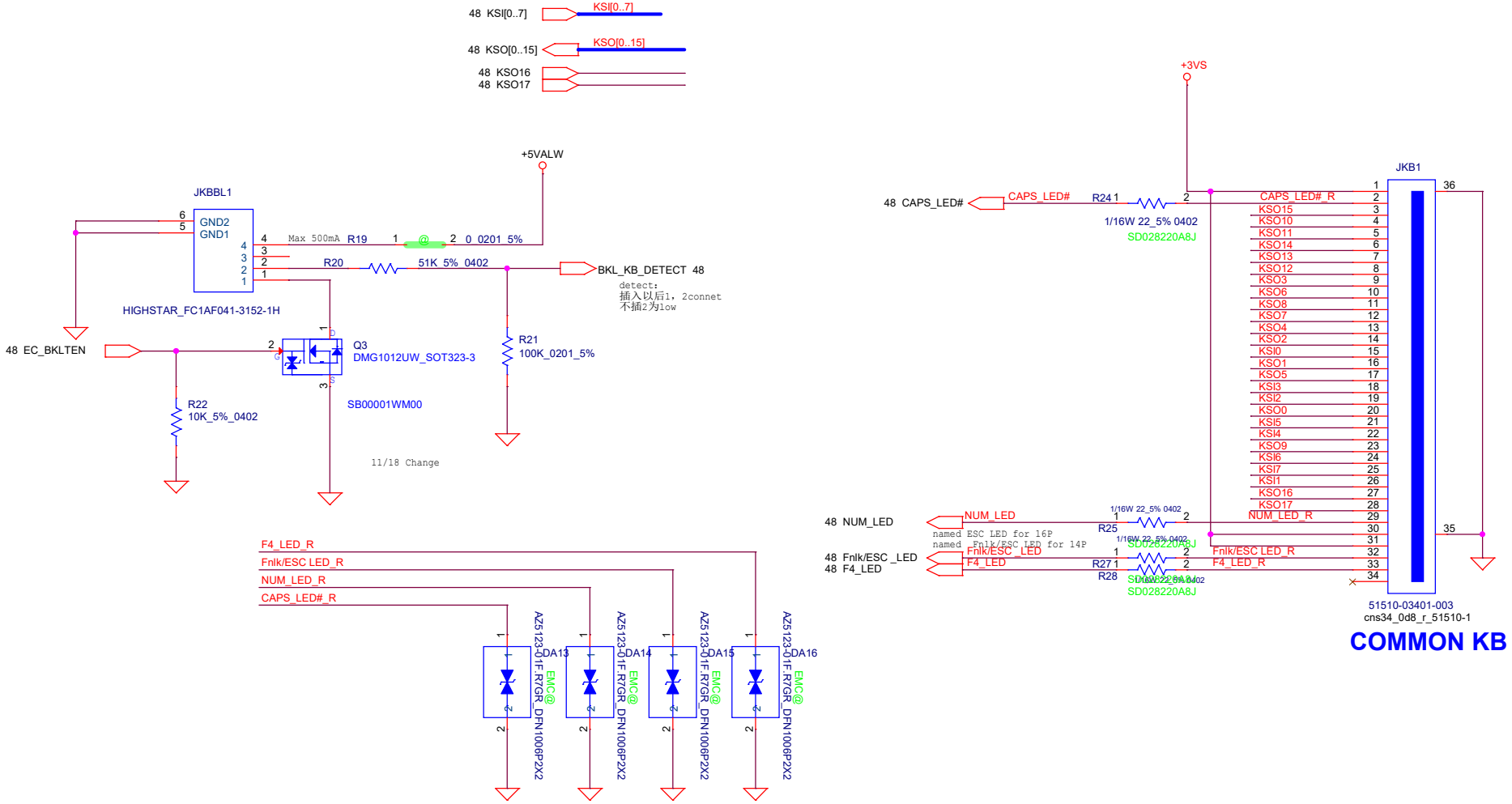
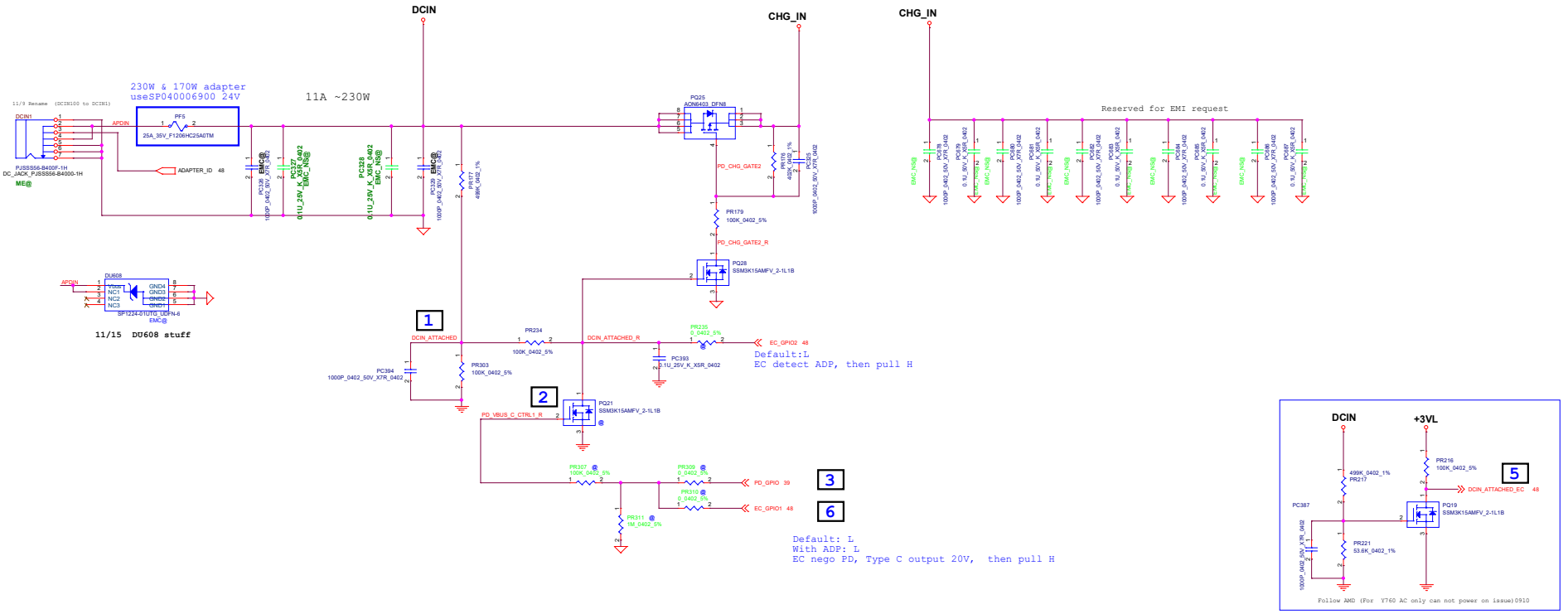


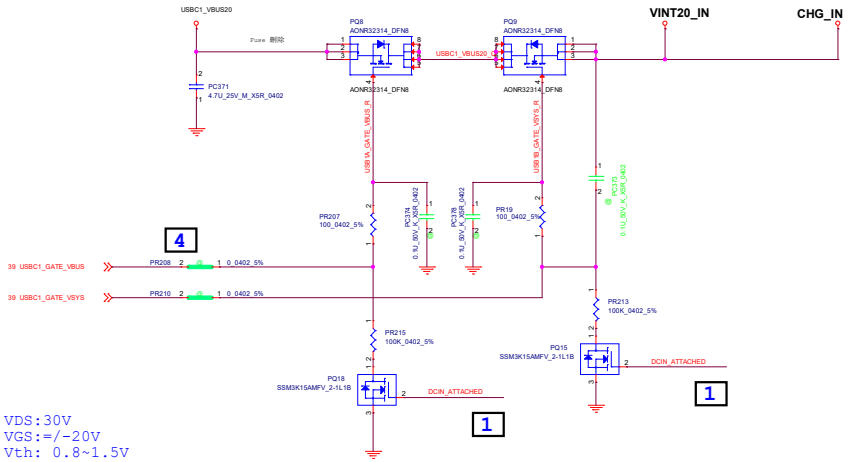
Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title	KB/KBBL CONN		
Size	Document Number		Rev
B	ARN35 AMD Rembrandt-H		1
Date:	Friday, March 18, 2022	Sheet	67 of 93



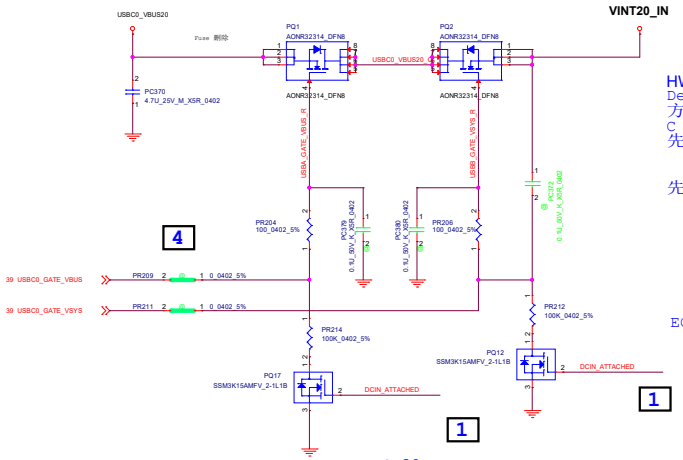
Type-C adapter 135W

Power loss about 0.68W, T rise 41C, need good thermal dispation



VDS:30V
VGS:=/-20V
Vth: 0.8~1.5V
ID:100mA
RDson: 3.5~6ohm, Vgs=2.5V

Power loss about 0.68W, T rise 41C, need good thermal dispation



VDS:30V
VGS:=/-20V
Vth: 0.8~1.5V
ID:100mA
RDson: 3.5~6ohm, Vgs=2.5V

HW Logic:
Default: 2,3,4,6,7:L (3,4 PD同步控制)
方口: 1->H, 5->L; 7->H; 2,3,4,6: L
C 口: 4->H, 2,3,6->H, 1,7: L , 5:H
先方口后C口: 1->H,5->L;7->H; 2,3,4,6: L
(方口优先, Logic不变)

先C口后方口: 1:L->H, 5:L->H;
EC控制PD控制4 H->L;2,3,6:H->L,C口先关,2变L后,7->H,方口再开
期间EC 拉L prochot#

EC control PD to achieve "Break before Make"

AC in&Type-C PD 参考Y770S
PD change to discrete MOS as thermal consideration

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: PWR_BATCON/RTC
Size: Custom
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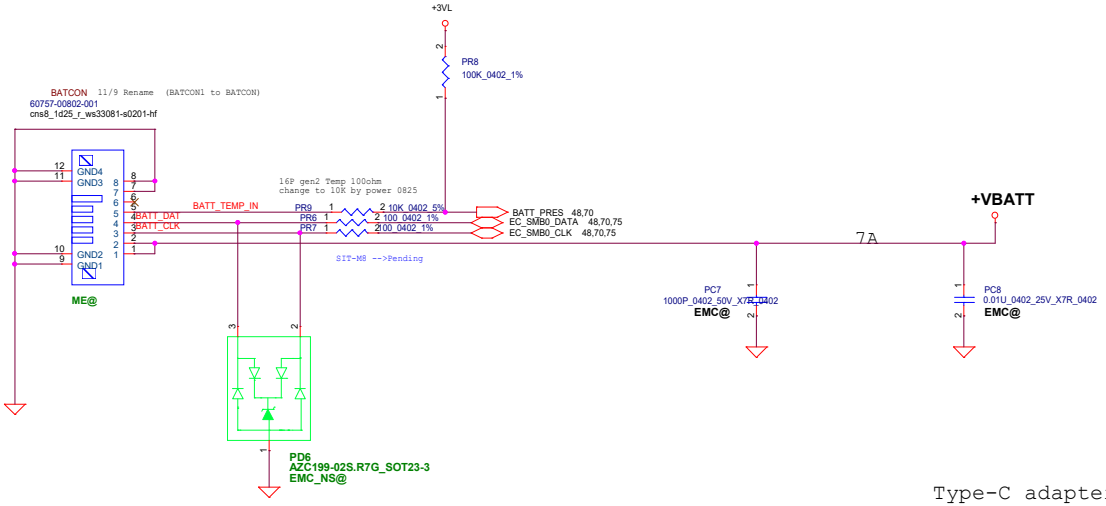
DCIN/BATTERY CONNECTOR



Type-C adapter 135W

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title	PWR_ACIN		LCFC
Size C	Document Number ARN35 AMD Rembrandt-H		Rev 1
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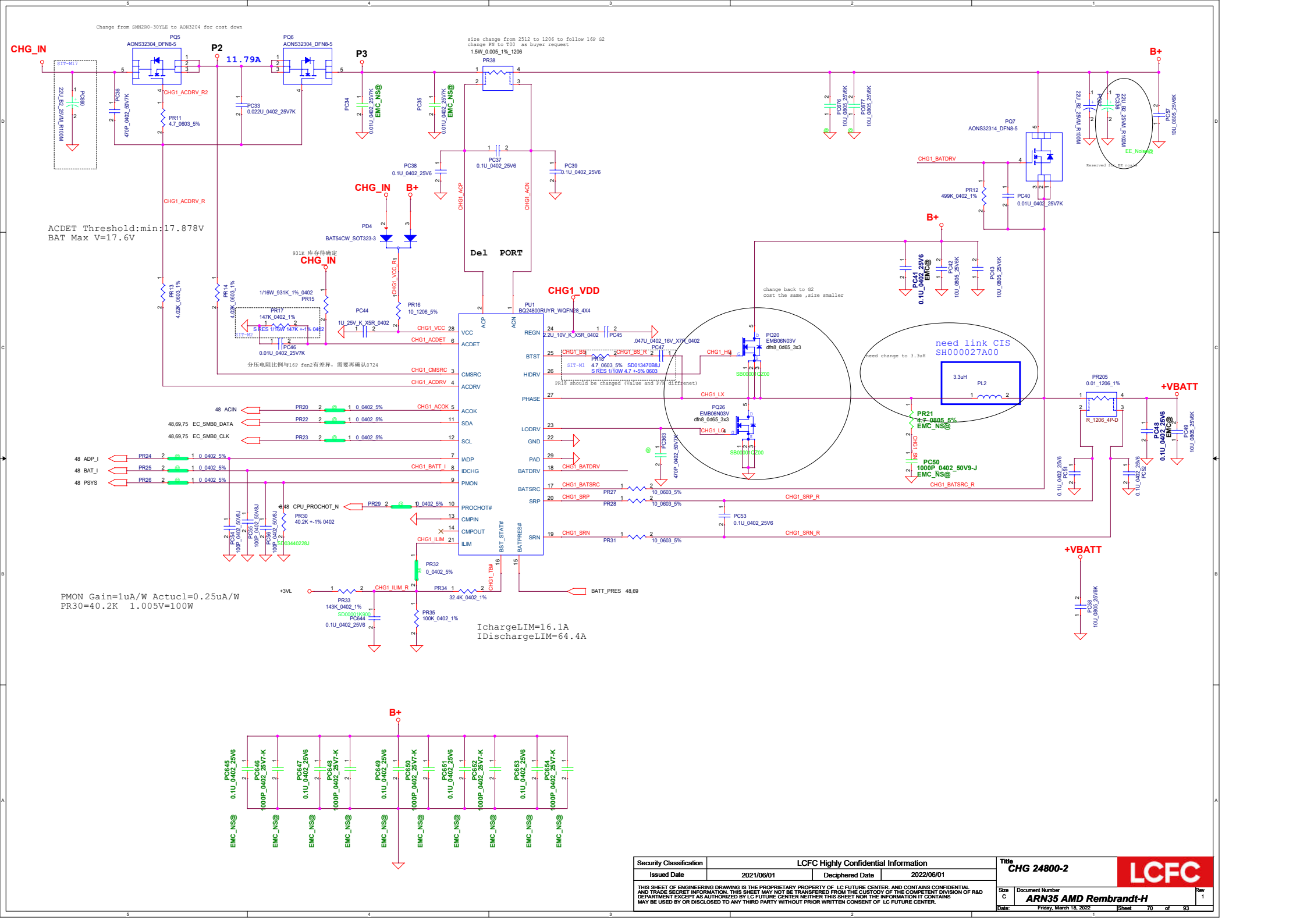

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: CHG 24800-2

LCFC

Size	Document Number	Rev
C	ARN35 AMD Rembrandt-H	1

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Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title
CHG 24800-2

LCFC

Size	Document Number	Rev
C	***ARN35 AMD Rembrandt-H***	1

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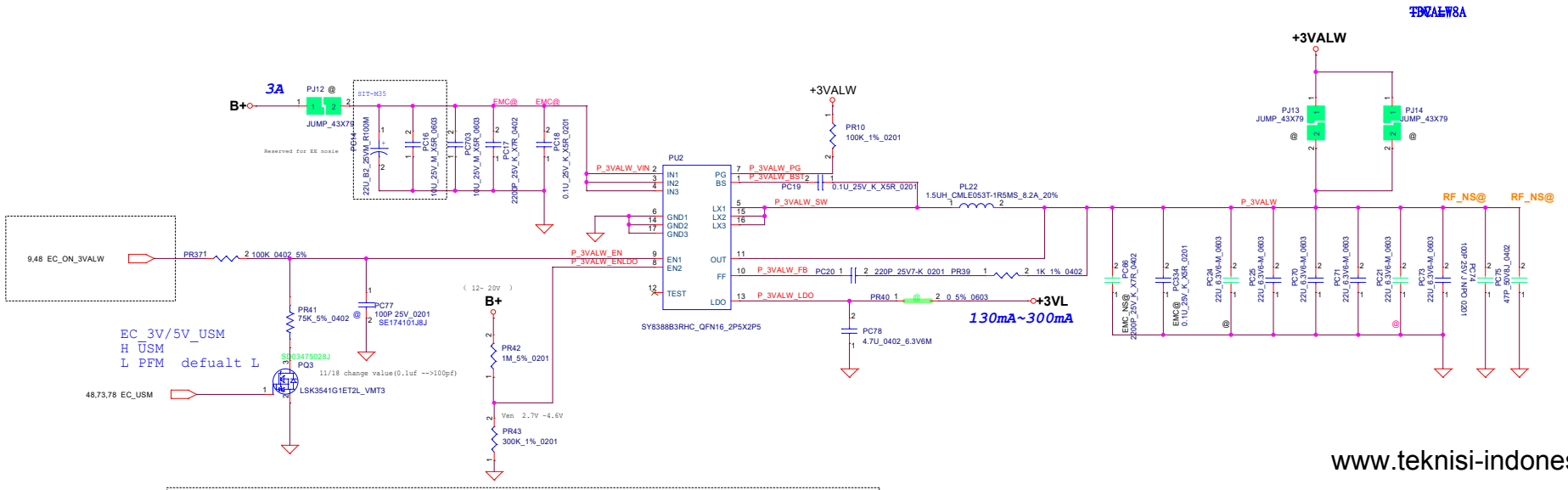

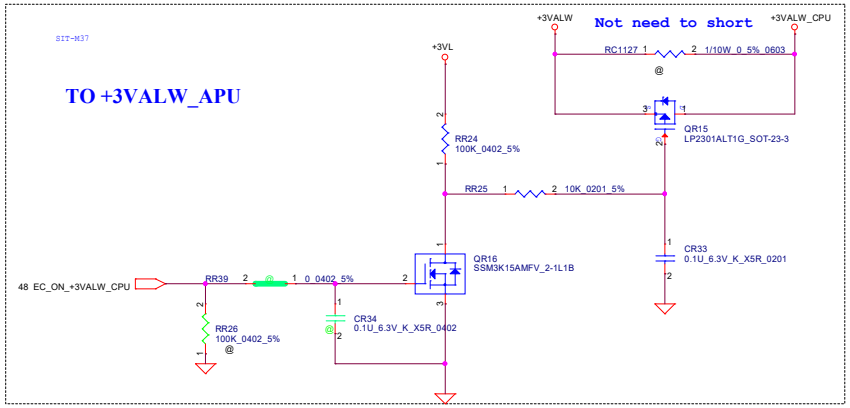

Vout=1.8V±5%
Vset=1.8V±2.3%
Vref=0.6V(+-1%)
TDC=8A
OCP=16A
OVP=(1.15~1.25)*Vout
UVP=(0.6~0.7)*Vout
Fsw=500Khz min=425K max=575K

Vout=3.3V±5%
Vset=3.3V±1%
FB=0.6V±1%
TDP=8A
FSW=600K
OCP=12A
OVP=Vout*(115%~125%)
UVP=Vout*60% typ

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: +3VALW

LCFC

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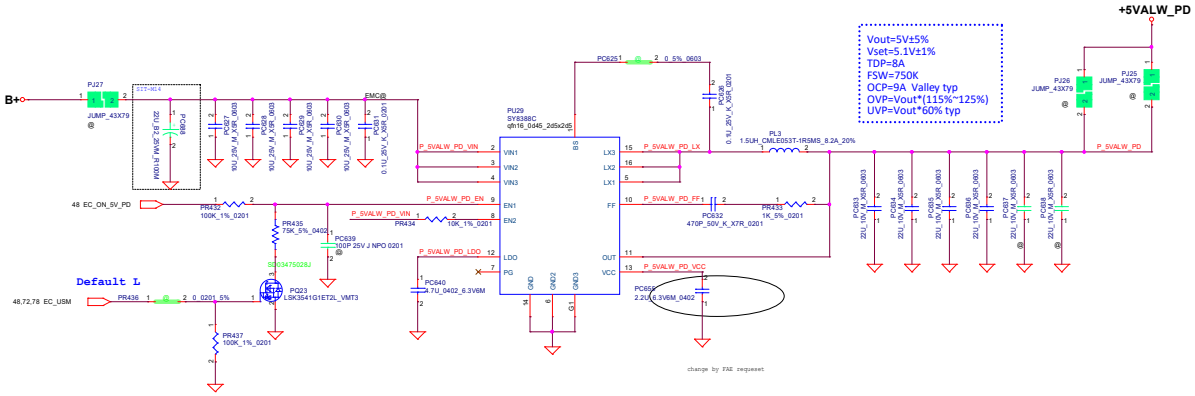
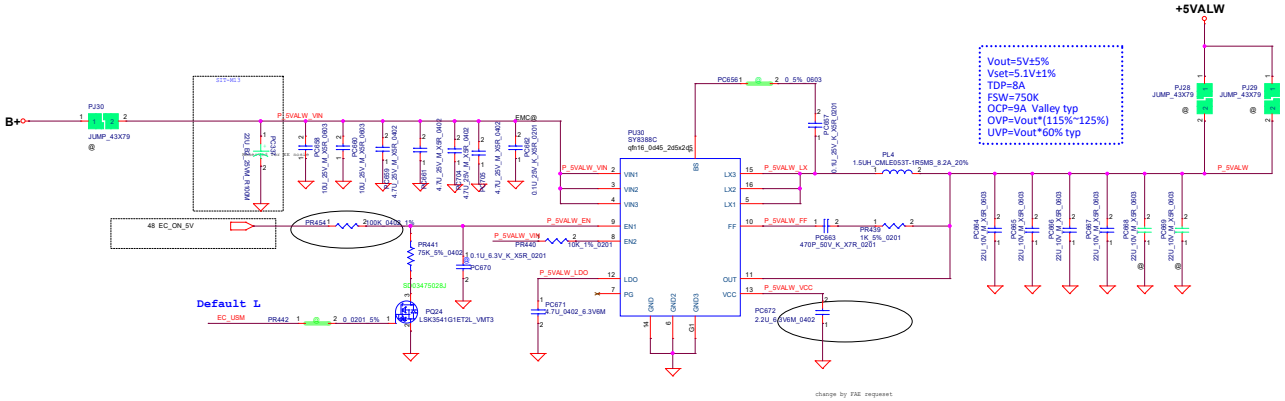
follow Y760 0728





Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title	5VALW&+5VALW_PD	LCFC	
Size	Document Number		Rev
Custom	ARN33 AMD Rembrandt-H		1
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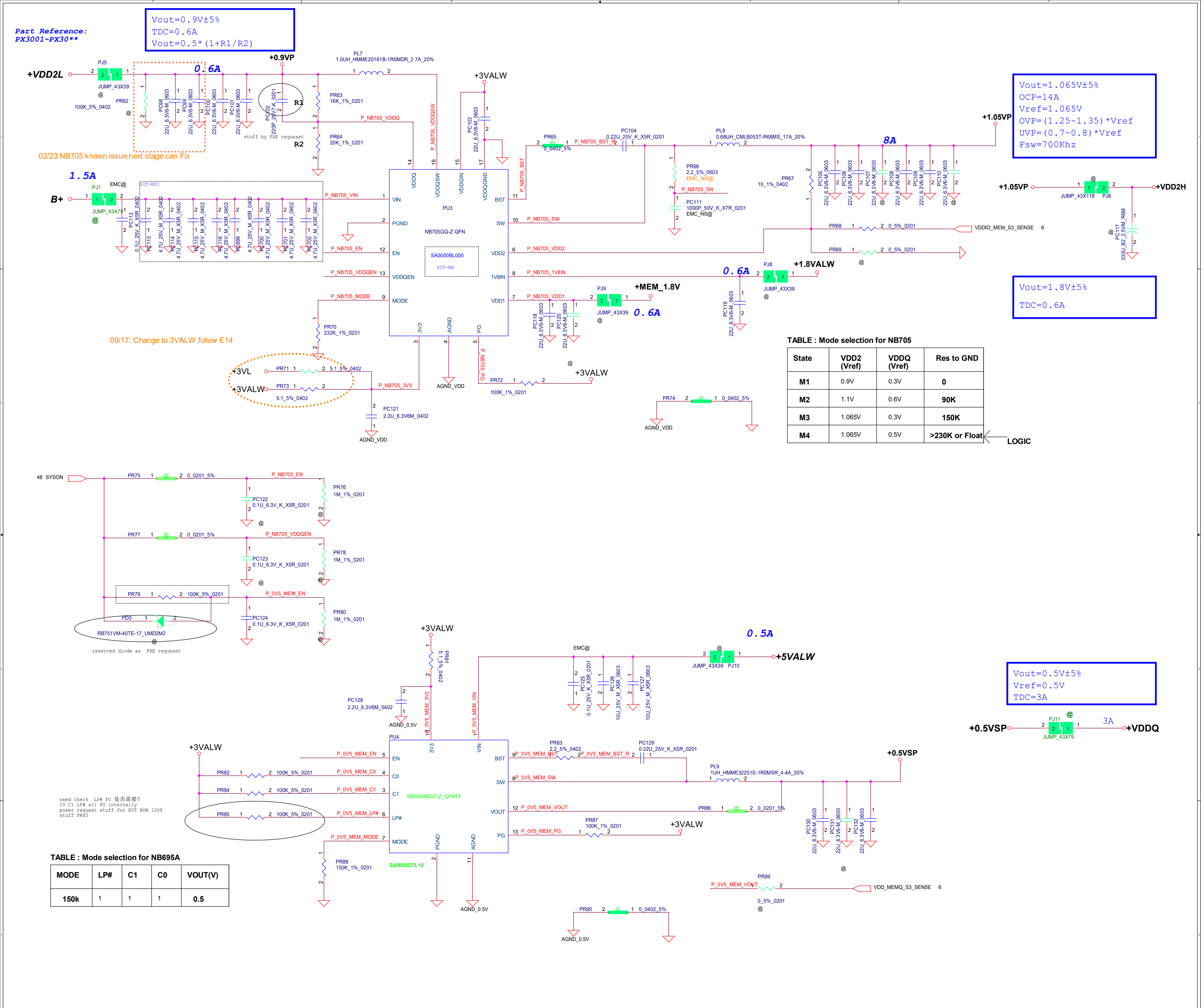

Part Reference:
PX3001~PX30**
Vout=0.9V±5%
TDC=0.6A
Vout=0.5*(1+R1/R2)
+VDD2L
+0.9VP
0.6A
PL7
1.0UH_HMME20161B-1R0MDR_2.7A_20%
R1
R2
PR63
16K_1%_0201
PR64
20K_1%_0201
stuff by FAE requeset
02/23:NB705 known issue,next stage can Fix
+3VALW
Vout=1.065V±5%
OCP=14A
Vref=1.065V
OVP=(1.25~1.35)*Vref
UVP=(0.7~0.8)*Vref
Fsw=700Khz
+1.05VP
PL8
0.68UH_CMLB053T-R68MS_17A_20%
8A
PC104
0.22U_25V_K_X5R_0201
PR65
0_0402_5%
PR66
2.2_5%_0603
EMC_NS@
PC111
1000P_50V_K_X7R_0201
EMC_NS@
PR67
10_1%_0402
+1.05VP
JUMP_43X118
PJ6
+VDD2H
PC117
330U_B2_2.5VM_R9M
1.5A
B+
PJ7
JUMP_43X79
EMC@
PU3
NB705GQ-Z QFN
SA0000BL000
VIN
PGND
EN
VDDQEN
MODE
VDDQ
VDDQSW
VDDQIN
VDDQGND
BST
SW
VDD2
1V8IN
VDD1
3V3
AGND
PG
P_NB705_VIN
P_NB705_EN
P_NB705_VDDQEN
P_NB705_MODE
P_NB705_VDDQ
P_NB705_VDDQSW
P_NB705_BST
P_NB705_SW
P_NB705_VDD2
P_NB705_1V8IN
P_NB705_VDD1
P_NB705_SN
P_NB705_3V3
P_NB705_PG
PR68
0_5%_0201
VDDIO_MEM_S3_SENSE
PR69
0_5%_0201
0.6A
PJ8
+1.8VALW
JUMP_43X39
PJ9
+MEM_1.8V
0.6A
Vout=1.8V±5%
TDC=0.6A
PR70
232K_1%_0201
09/17: Change to 3VALW,follow E14
+3VL
PR71
5.1_5%_0402
+3VALW
PR73
5.1_5%_0402
PC121
2.2U_6.3V6M_0402
AGND_VDD
PR72
100K_1%_0201
PR74
0_0402_5%
LOGIC
SYSON
PR75
0_0201_5%
PR76
1M_1%_0201
PC122
0.1U_6.3V_K_X5R_0201
PR77
0_0201_5%
PR78
1M_1%_0201
PC123
0.1U_6.3V_K_X5R_0201
PR79
100K_5%_0201
P_0V5_MEM_EN
PR80
1M_1%_0201
PC124
0.1U_6.3V_K_X5R_0201
PD3
RB751VM-40TE-17_UMD2M2
reserved diode as FAE requeset
+3VALW
PR81
5.1_5%_0402
PC128
2.2U_6.3V6M_0402
AGND_0.5V
0.5A
+5VALW
JUMP_43X39
PJ10
Vout=0.5V±5%
Vref=0.5V
TDC=3A
+0.5VSP
PJ11
JUMP_43X79
3A
+VDDQ
PU4
NB695ABGD-Z_QFN13
SA0000D7L10
PR82
100K_5%_0201
PR84
100K_5%_0201
PR85
100K_5%_0201
need check LP# PU 是否需要?
C0 C1 LP# all PU internally
power request stuff for EVT BOM 1008
stuff PR85
PR88
150K_1%_0201
PR83
2.2_5%_0402
PC129
0.22U_25V_K_X5R_0201
PL9
1UH_HMME32251E-1R0MSR_4.4A_20%
+0.5VSP
PR86
0_0201_5%
PR87
100K_1%_0201
PR89
0_5%_0201
VDD_MEMQ_S3_SENSE
PR90
0_0402_5%

TABLE : Mode selection for NB705

State	VDD2 (Vref)	VDDQ (Vref)	Res to GND
M1	0.9V	0.3V	0
M2	1.1V	0.6V	90K
M3	1.065V	0.3V	150K
M4	1.065V	0.5V	>230K or Float

TABLE : Mode selection for NB695A

MODE	LP#	C1	C0	VOUT(V)
150k	1	1	1	0.5

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: PWR_Memory PWR

LCFC

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Part Reference:
PX1001-PX1099

Controller---MP2845AGQK-0709-Z
D.r Mos---MP86941GQVT-Z*4
D.r Mos---MP86901-CGLT-Z*1
D.r Mos---MP86901-AGQT-Z*1
Chock---CMME063T-R15MI0R887

PN FW 16P 已更新 0730

+1.8VALW

+3VALW

+1.8VS

VCC1R8

VDD18

2/20

VDDCR_VDD
65A TDC
140A EDC

VDDCR_SOC
15A TDC
20A EDC

VDDCR_SR
2A TDC
3A EDC

+VDDCR_VDD

+VDDCR_SOC

+VDDCR_SR

Remote Sense

TDC 65A
EDC 140A
OCP 160A

TDC 15A
EDC 20A
OCP 30A

TDC 2A
EDC 3A
OCP 6A

B+

2.5A

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: CPU PWR Controller
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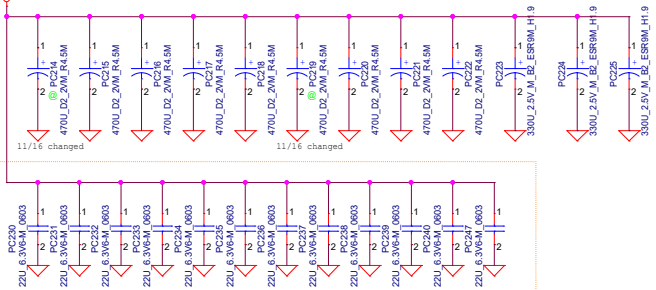
Part Reference:
PX1100~PX11**

Note--Rembrandt
470uF/4.5mohm*9pcs D2+330uF/9mohm 3pcs D2
22uF/0603*12pcss
10uF/0402*40pcs

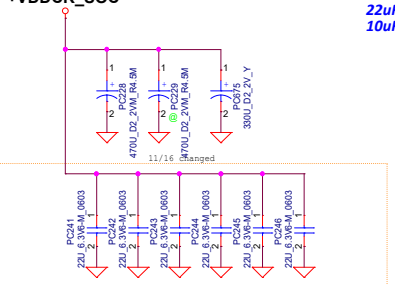
+VDDCR_VDD



All BU(on bot side beside CPU)

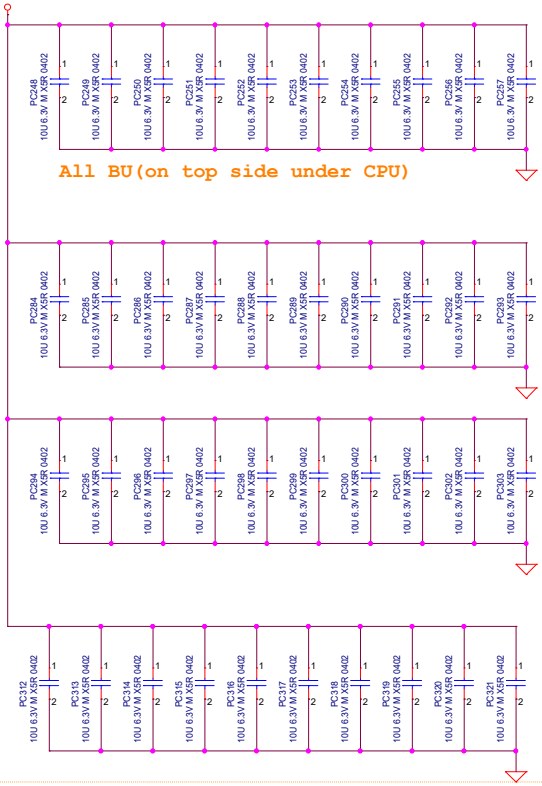
+VDDCR_SOC

Rembrandt
470uF/4.5mohm*2pcs D2
22uF/0603*6pcs
10uF/0402*26 pcs



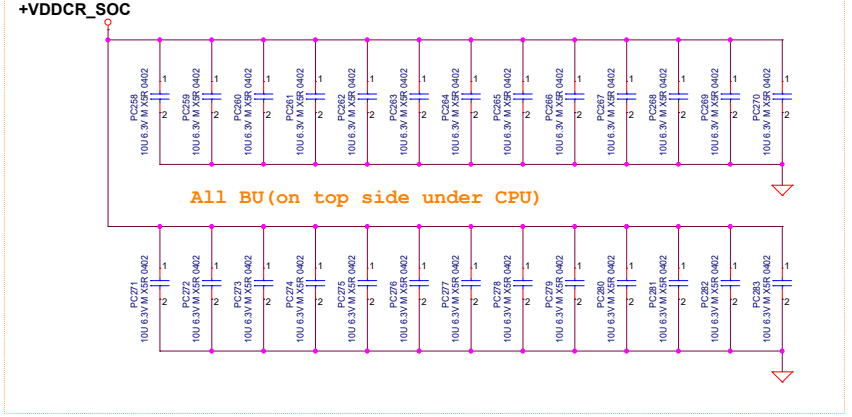
All BU(on bot side beside CPU)

+VDDCR_VDD



All BU(on top side under CPU)

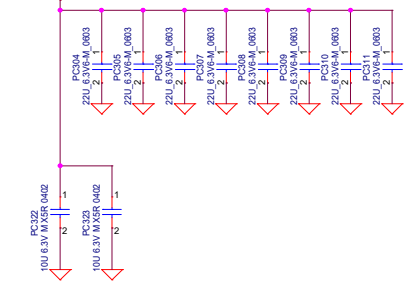
+VDDCR_SOC



All BU(on top side under CPU)

+VDDCR_SR

Rembrandt
22uF/0603*8pcs
10uF/0402*2pcs



Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: PWR Decoupling

LCFC

Size	Document Number	Rev
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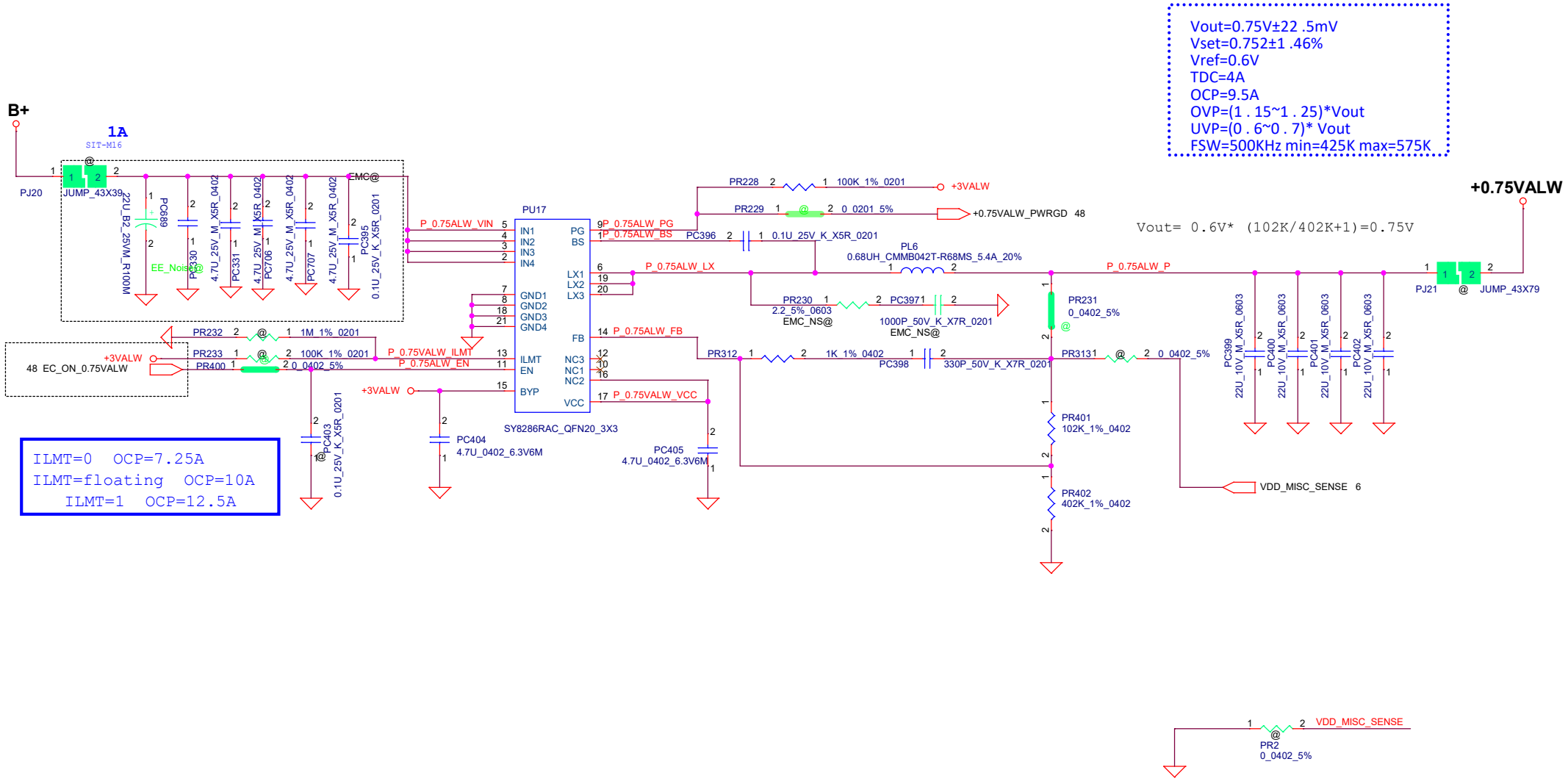

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title	PWR1_+0.75VALW		
Size	B	Document Number	ARN35 AMD Rembrandt-H
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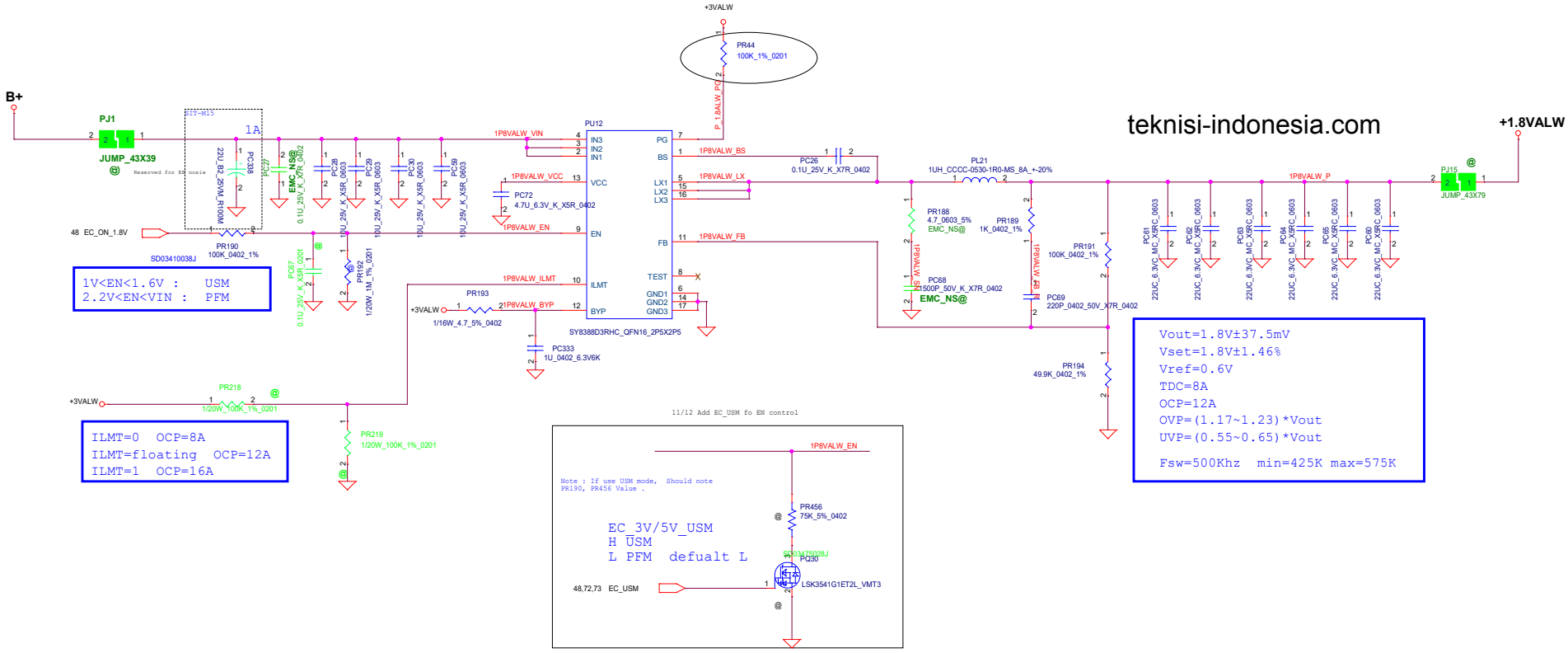

follow YX0 0729

Security Classification	LCFC Highly Confidential Information		
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Title	PWR2_+1.8VALW	LCFC	
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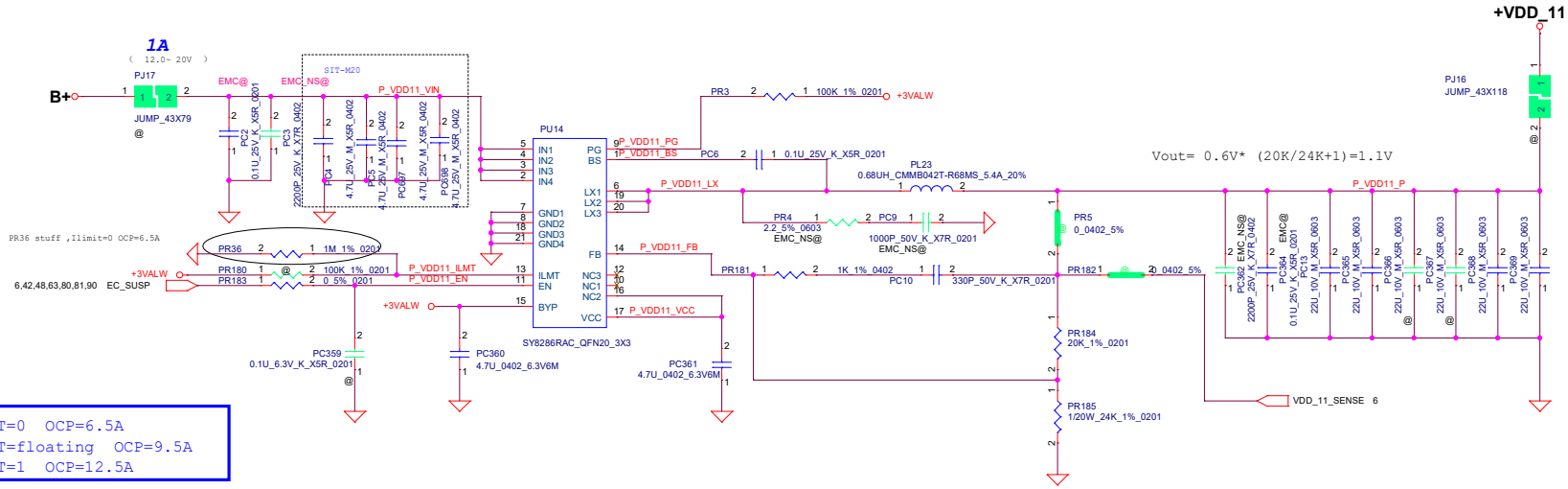
Vout=1.1V±22 .5mV
Vset=1.1±1 .46%
Vref=0.6V
TDC=5A
FSW=500KHz min=425K max=575K
OCP=9.5A
OVP=(1 . 15~1 . 25)*Vout
UVP=(0 . 6~0 . 7)* Vout



ILMT=0 OCP=6.5A
ILMT=floating OCP=9.5A
ILMT=1 OCP=12.5A

Security Classification	LCFC Highly Confidential Information		
Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title: PWR3_+VDD_11

LCFC

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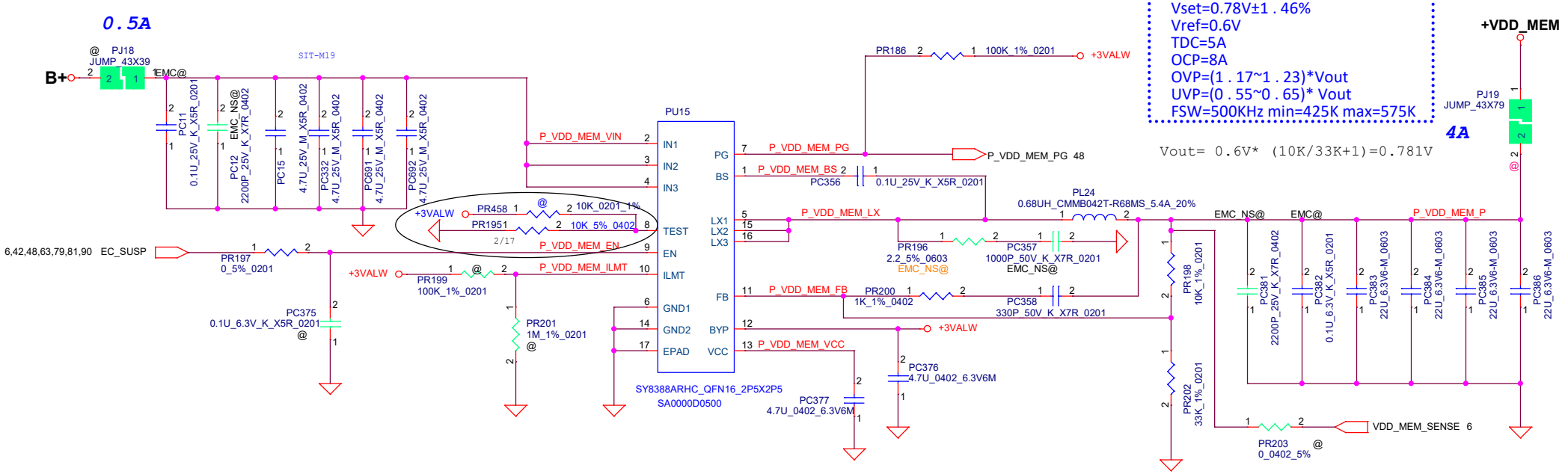
+VDD_MEM
TDC = 4A
Vout =0.78V

0.5A

Vout=0.78V±37.5mV
Vset=0.78V±1.46%
Vref=0.6V
TDC=5A
OCP=8A
OVP=(1.17~1.23)*Vout
UVP=(0.55~0.65)* Vout
FSW=500KHz min=425K max=575K

Vout= 0.6V* (10K/33K+1)=0.781V

4A



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Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title	PWR4_+VDD_MEM		
Size	Document Number		Rev
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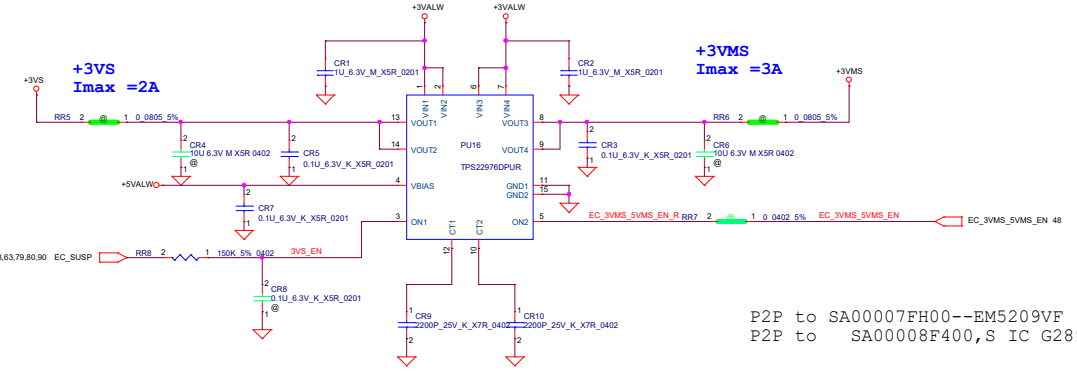
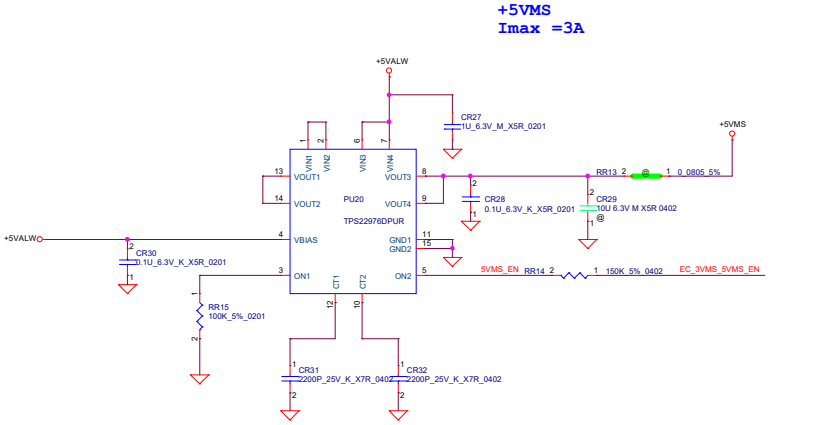
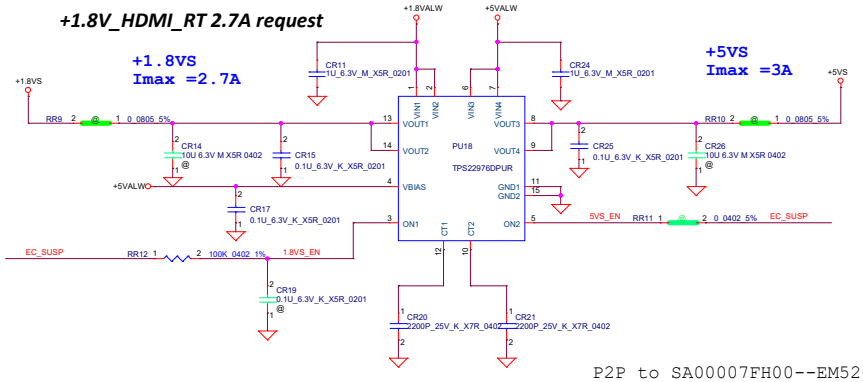


P2P to SA00007FH00--EM5209VF
P2P to SA00008F400,S IC G2898KD1U

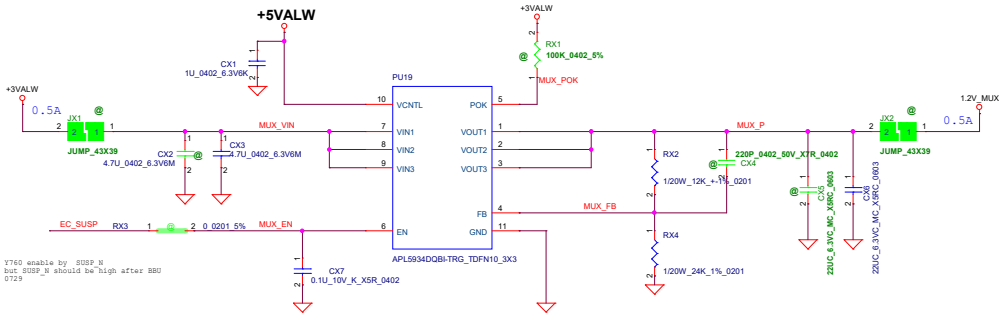


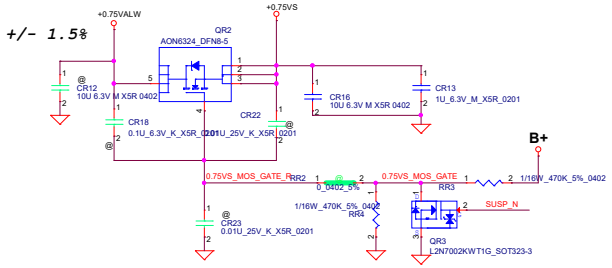
P2P to SA00007FH00--EM5209VF
P2P to SA00008F400,S IC G2898KD1U

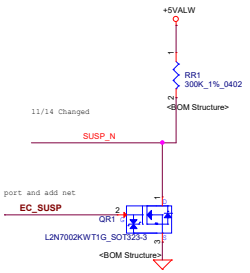


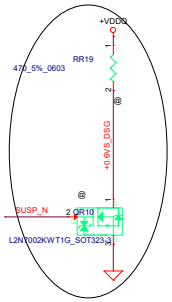
P2P to SA00007FH00--EM5209VF
P2P to SA00008F400,S IC G2898KD1U

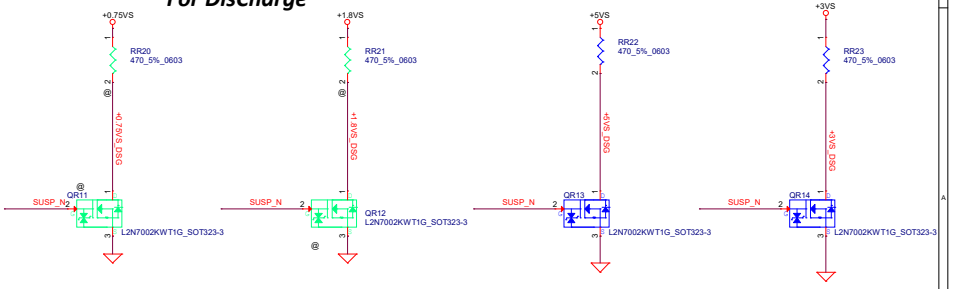
for Parade PS8461E 1.2V











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Title	DCDC_SYSTEM PWR	LCFC	
Size: Custom	Document Number: ARN35 AMD Rembrandt-H		Rev: 1
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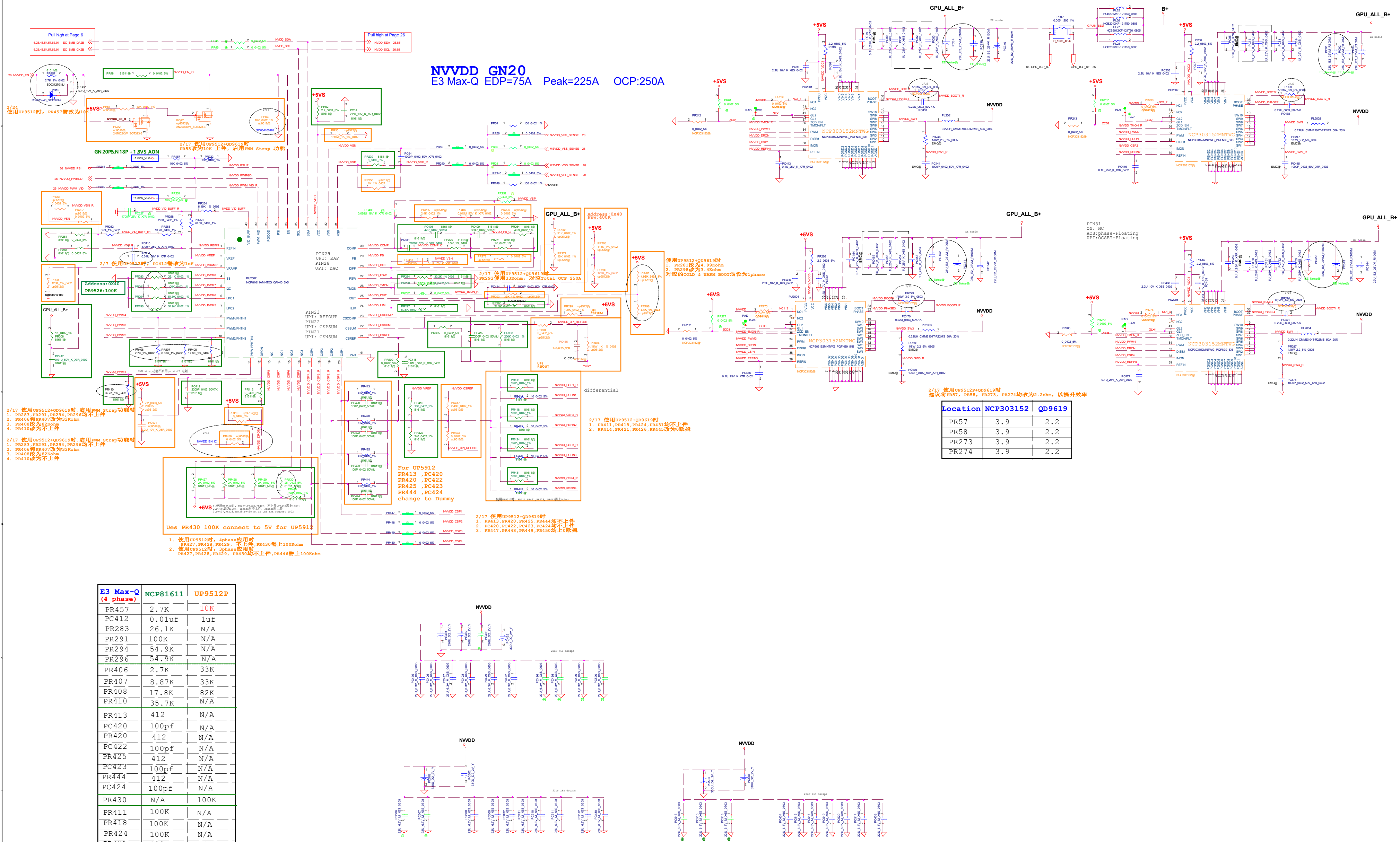

E3 Max-Q (4 phase)	NCP81611	UP9512P
PR457	2.7K	10K
PC412	0.01uf	1uf
PR283	26.1K	N/A
PR291	100K	N/A
PR294	54.9K	N/A
PR296	54.9K	N/A
PR406	2.7K	33K
PR407	8.87K	33K
PR408	17.8K	82K
PR410	35.7K	N/A
PR413	412	N/A
PC420	100pf	N/A
PR420	412	N/A
PC422	100pf	N/A
PR425	412	N/A
PC423	100pf	N/A
PR444	412	N/A
PC424	100pf	N/A
PR430	N/A	100K
PR411	100K	N/A
PR418	100K	N/A
PR424	100K	N/A
PR431	100K	N/A
PR414	10	0
PR421	10	0
PR426	10	0
PR445	10	0

2/17 使用UP9512P+QD9619时
建议将PR57，PR58，PR273，PR274均改为2.2ohm，以提升效率

Location	NCP303152	QD9619
PR57	3.9	2.2
PR58	3.9	2.2
PR273	3.9	2.2
PR274	3.9	2.2

Title: PWR-NVVDD
Document Number: ARN35 AMD Rembrandt-H
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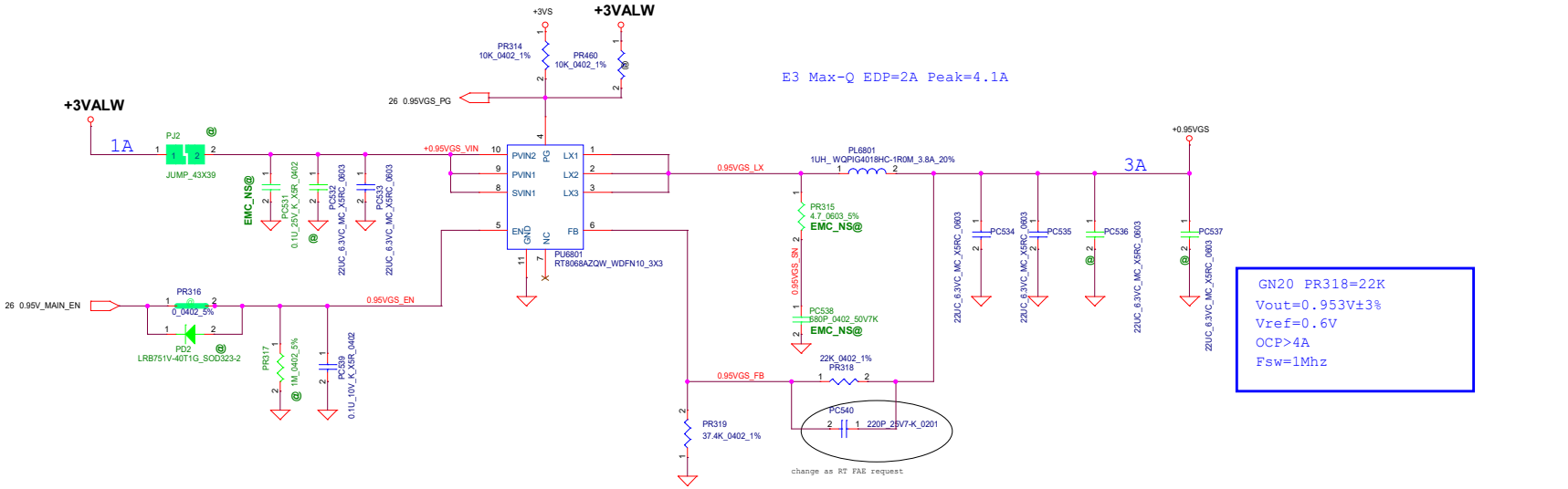
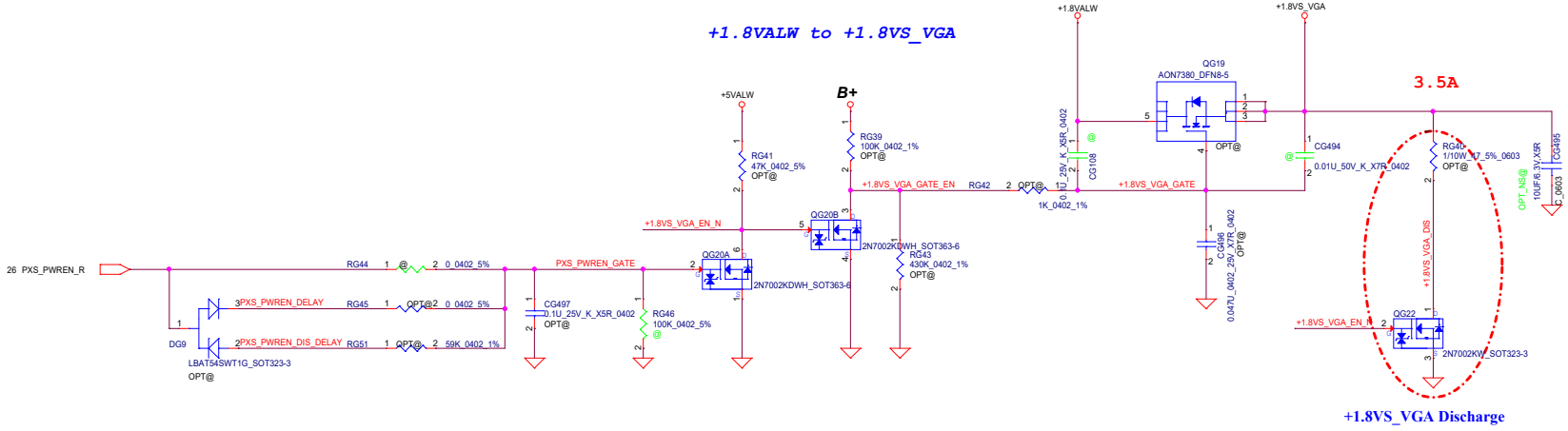
Date: Friday, March 18, 2022





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Issued Date	2021/06/01	Deciphered Date	2022/06/01

Title	PWR_GPU PWR		LCFC
Size C	Document Number ARN35 AMD Rembrandt-H		Rev 1
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Title ***PWR_GPU PWR2***

LCFC

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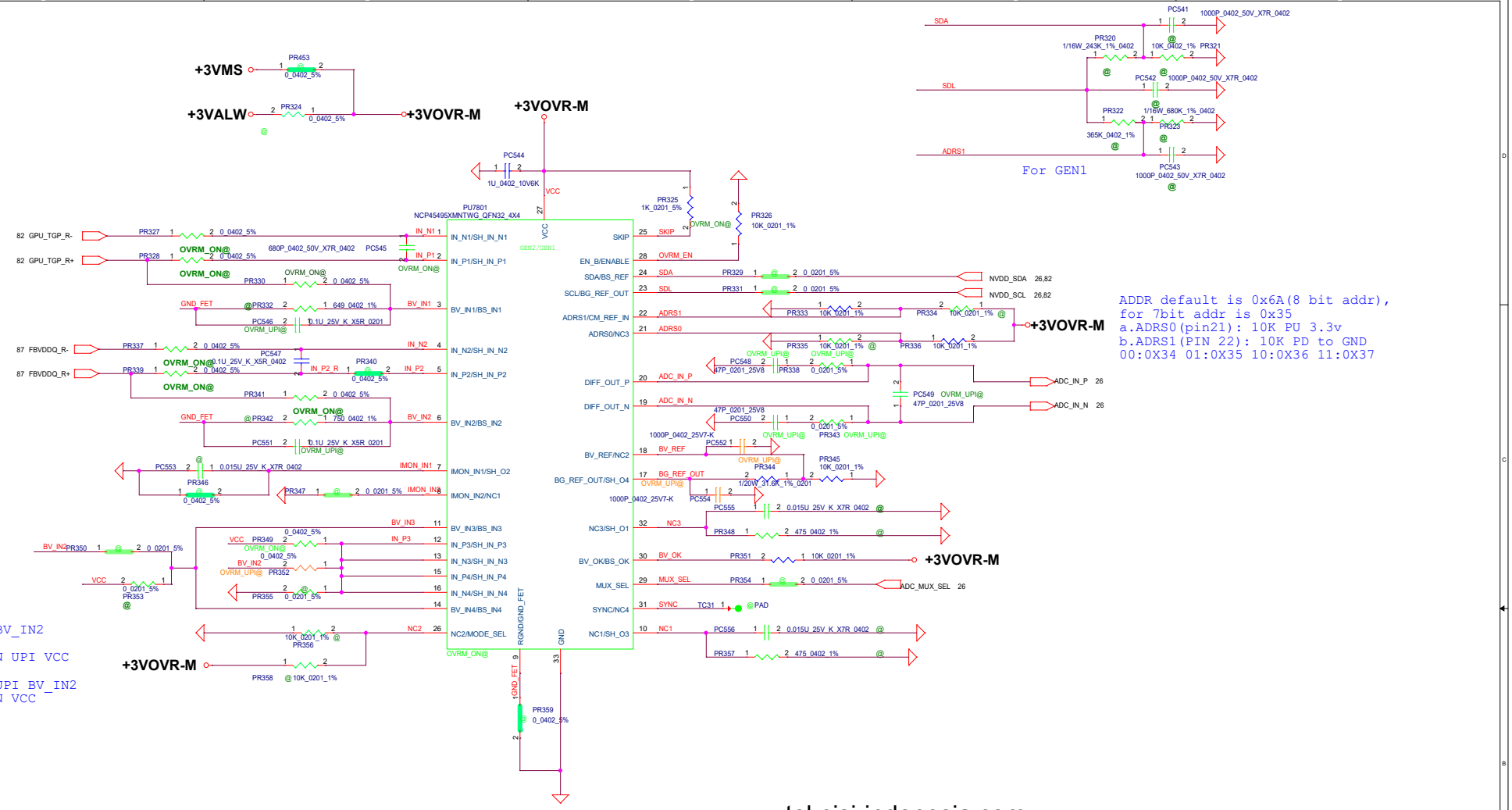

ADDR default is 0x6A(8 bit addr),
for 7bit addr is 0x35
a.ADRS0(pin21): 10K PU 3.3v
b.ADRS1(PIN 22): 10K PD to GND
00:0X34 01:0X35 10:0X36 11:0X37

GEN2:
BV_INX ON BV_IN2
UPI VCC
IN_NX PX ON UPI VCC
GEN1:
BV_INX ON UPI BV_IN2
IN_NX PX ON VCC
UPI GND

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Title	P105-PWR_GPU PWR Monitor		
Size	C	Document Number	ARN35 AMD Rembrandt-H
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Title

GPU PWR Decoupling

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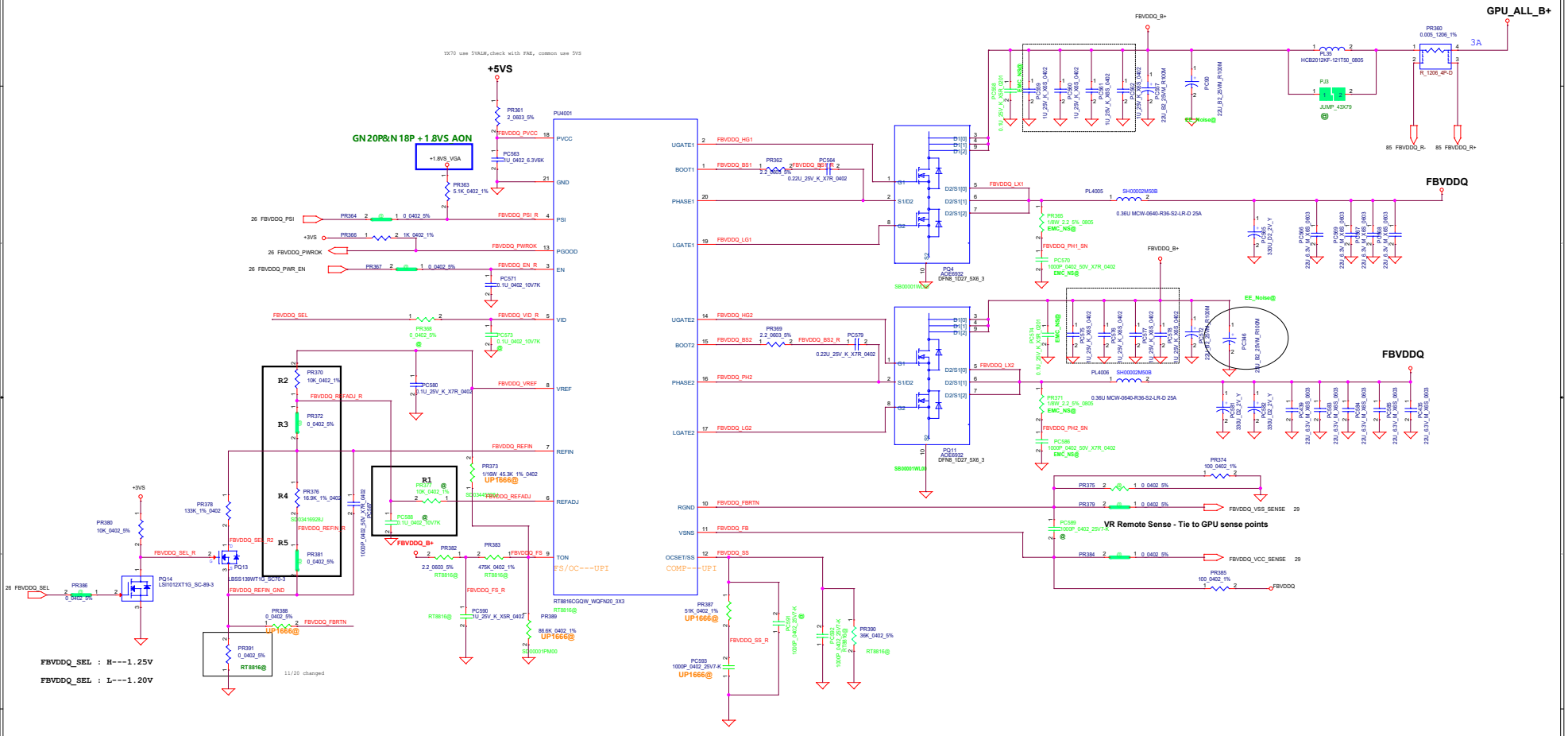
RT8816 PSI	UP1666 PSI	Phase Configuration
1.6V~5.5V	1.6~5.5V	2Phase CCM
1.08~1.35V	1~1.4V	2Phase DEM
0.7~0.88V	0.4V~0.8V	1Phase CCM
0~0.4V	0~0.2V	1Phase DEM

E3 Max-Q EDP=20A Peak=26A



Follow YX60/Y770S

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Title: PWR-FBVDDQ

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Title

PWR_Memory PWR Decoupling

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SIT-M21

Del

Current Sensor

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Title ***Blank***

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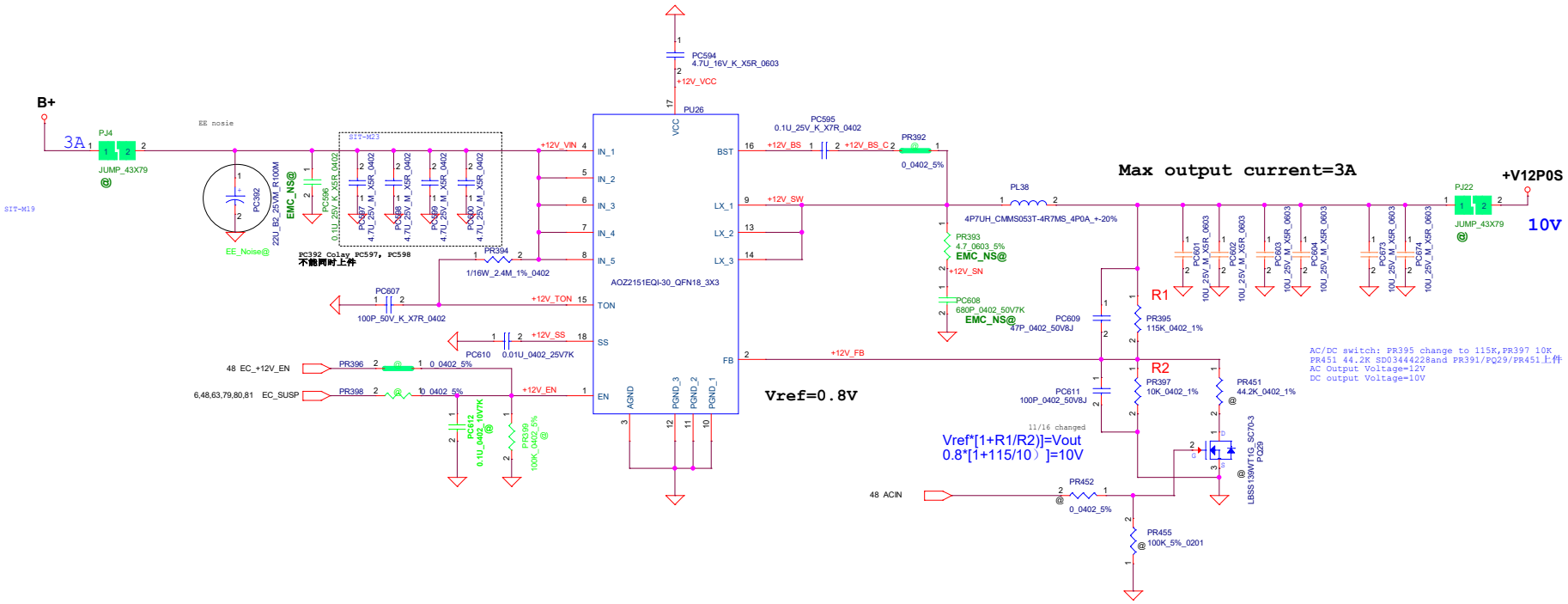

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Title: PWR_Memory PWR Decoupling

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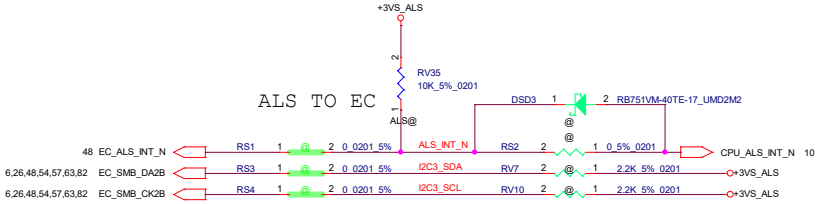
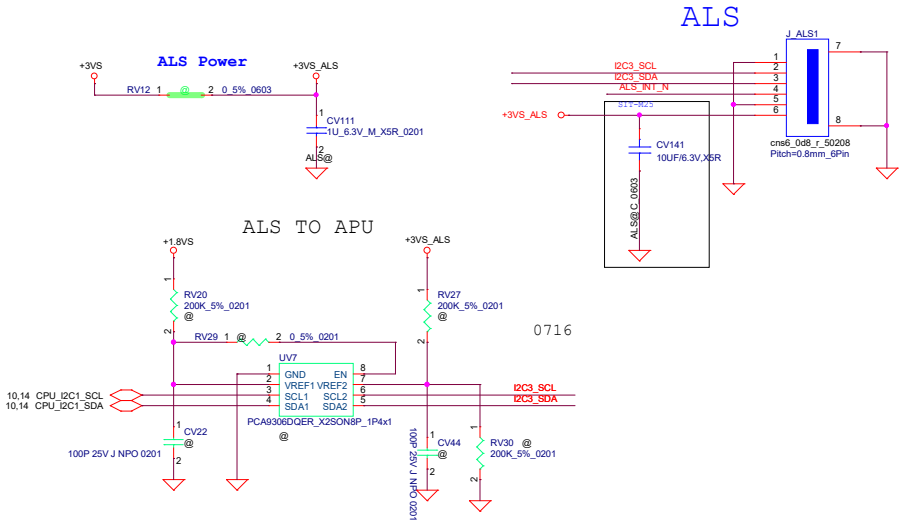
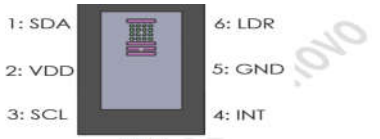




ALS pin definition



4. PIN DESCRIPTION

Pin No.	Pin Name	Dir.	Pin Function
1	SDA	B	I²C serial data line. (Open Drain)
2	VDD	PWR	Power supply: 1.7V to 3.3V.
3	SCL	I	I²C serial clock line.
4	/INT	O	Interrupt pin, LO for interrupt alarming. (Open Drain)
5	GND	GND	Ground. The thermal pad is also connected to the GND pin.
6	LDR	I	IR LED driver pin connecting to the cathode of the external IR LED. The sink current of the IR LED driver can be programmed through I²C or the external resistor.

Direction description:

O	Output	GND	Ground
I	Input	B	Bi-direction
PWR	Power	NC	Not Connect

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Title: ALS&TOF

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1. Changed some Part Reference Name (length>6)

BATCON1-->BATCON; USBLED1-->USBLED; HDMILED1-->HDMLED; BATLED1-->BATLED;
CHRLED1-->CHRLED; DCIN100-->DCIN1; JDEBUG1-->JDEBU1; JDEBUG2-->JDEBU2;
JNOVOSW1-->JNOVSW; RTC_BATT1 -->RTCBAT

2. Changed EC SMBUS (SMBus Address conflict on GPU and EC) --Page26

VGA_SMB_CK2/VGA_SMB_DA2-->From EC_SMB_CK2B/EC_SMB_DA2B To EC_SMB0_CLK/EC_SMB0_DATA

3. Changed ADCIN pin design --Page39

RU4 200K to 100K (SD00001LV00-> SD04110038J), RU3 12.1K to 22K (SD00001470J->SD00001R300)

4. Changed EC_LCDBLK_ON pull up --Page48

RE68 From stuff to unstuff

5. Changed board ID for 14P &16P differentiate --Page48

RE36 (unstuff -->SD000010U00)

6. Changed JKBBL1 pin define --Page67

JKBBL1 (exchanged pin 1->4, 2->3)

7. Changed Library --Page40&63

UU4 and UV9 ---Changed symbol (APL5934CQBI-TRG_TDFN10_3X3 to APL5934DQBI-TRG_TDFN10_3X3)

8. Changed PCB footprint --Page40&63

Capacitor and Resistor unify pcb foorprint

9. Changed Expander SMBUS --Page48

Changed net name (From EC_SMB_CK5A/EC_SMB_DA5A To EC_SMB_CK2B/EC_SMB_DA2B)

10. Changed EC GPIO for EC requirment --Page48

Exchanged EC_LCD_SELF_TEST and DCIN_ATTACHED_EC

11. Follow LCFC YX70 adjust CPU GPIO --Page9&10

GPIO

12. Changed Resistor to Fuse ---Page63

Del RV23 and Add RVF1

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Title: Change List_EE

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Title: ***Change List_PWR***

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