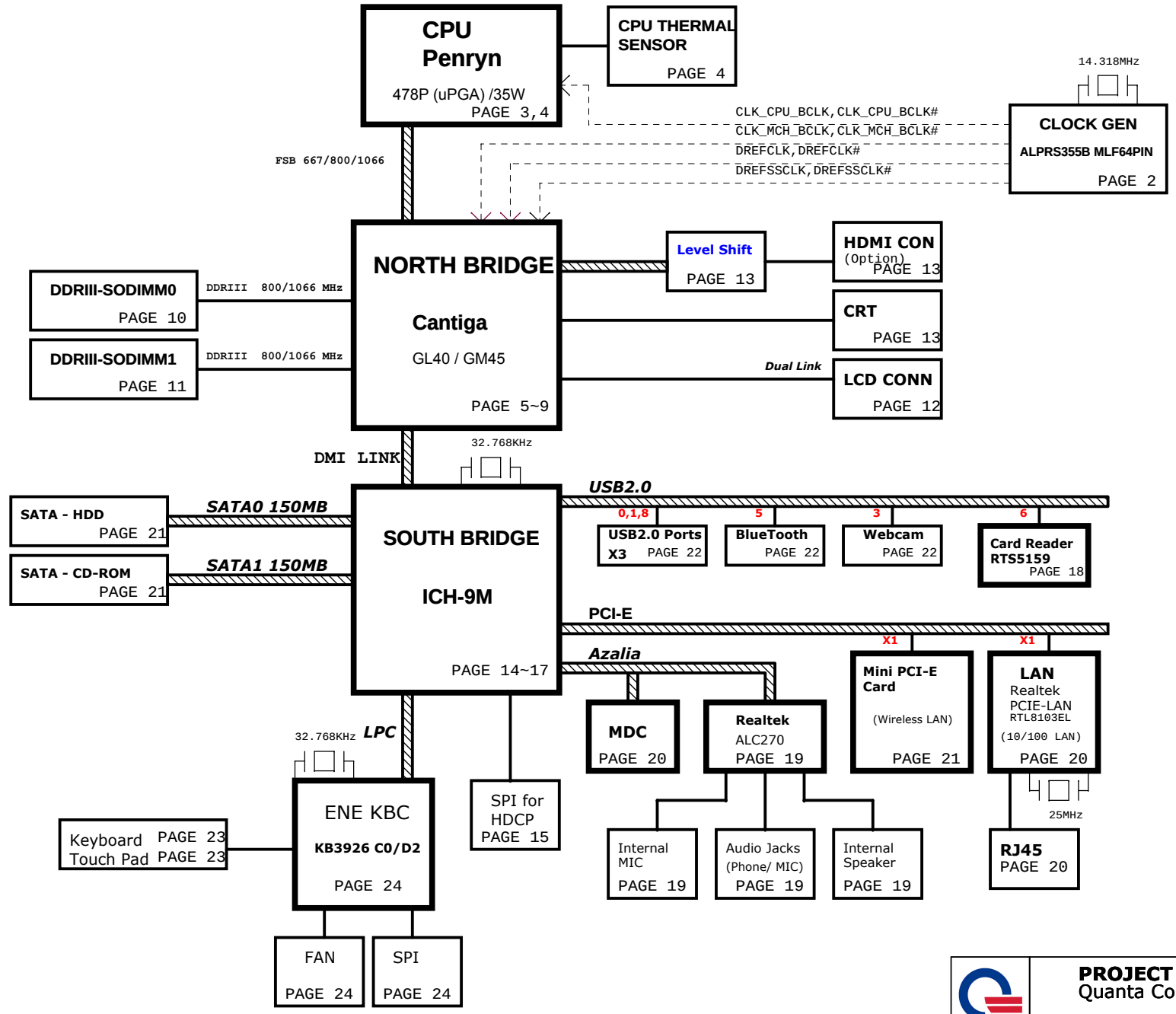
Wimbledon AX3/5 BLOCK DIAGRAM

01

PCB STACK UP

6L UMA CO-LAY DIS

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT



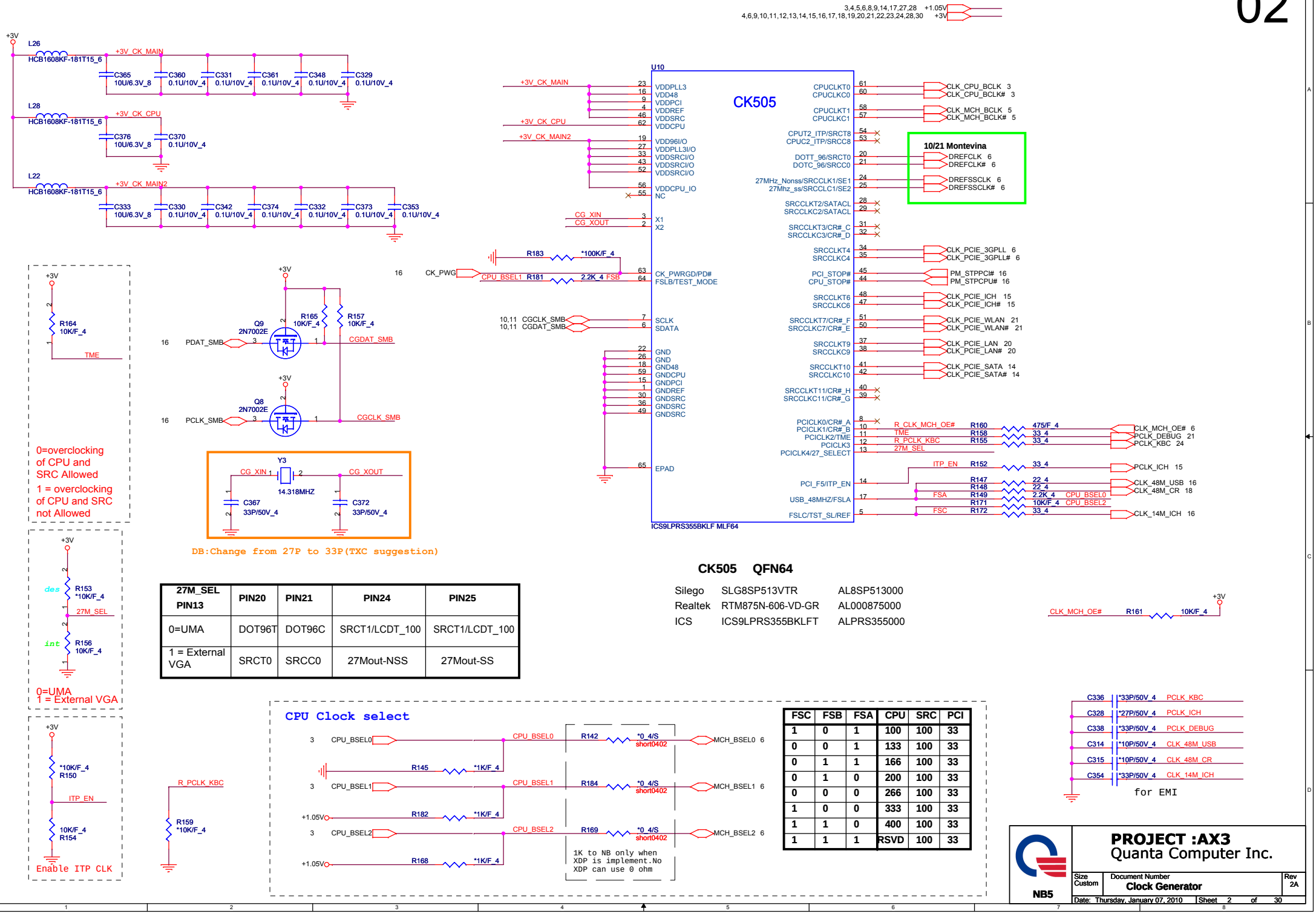
SYSTEM CHARGER (ISL6251AHAZ-T) PAGE 25
SYSTEM POWER (RT8206BGQW) PAGE 26
VCCP +1.05V (RT8209AGQW) & +1.8VSUS (RT9043GB) PAGE 27
CPU CORE (ISL6262ACRZ-T) PAGE 28
DDR III SMDDR +1.5VSUS (RT8207AGQW) PAGE 29
SYSTEM DISCHARGER PAGE 30

NB5

PROJECT :AX3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	2A

Date: Thursday, January 07, 2010 | Sheet 1 of 30



27M_SEL PIN13	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	SRCT1/LCDT_100	SRCT1/LCDT_100
1 = External VGA	SRCT0	SRCC0	27Mout-NSS	27Mout-SS

CK505 QFN64

Silego	SLG8SP513VTR	AL8SP513000
Realtek	RTM875N-606-VD-GR	AL000875000
ICS	ICS9LPRS355BKLFT	ALPRS355000

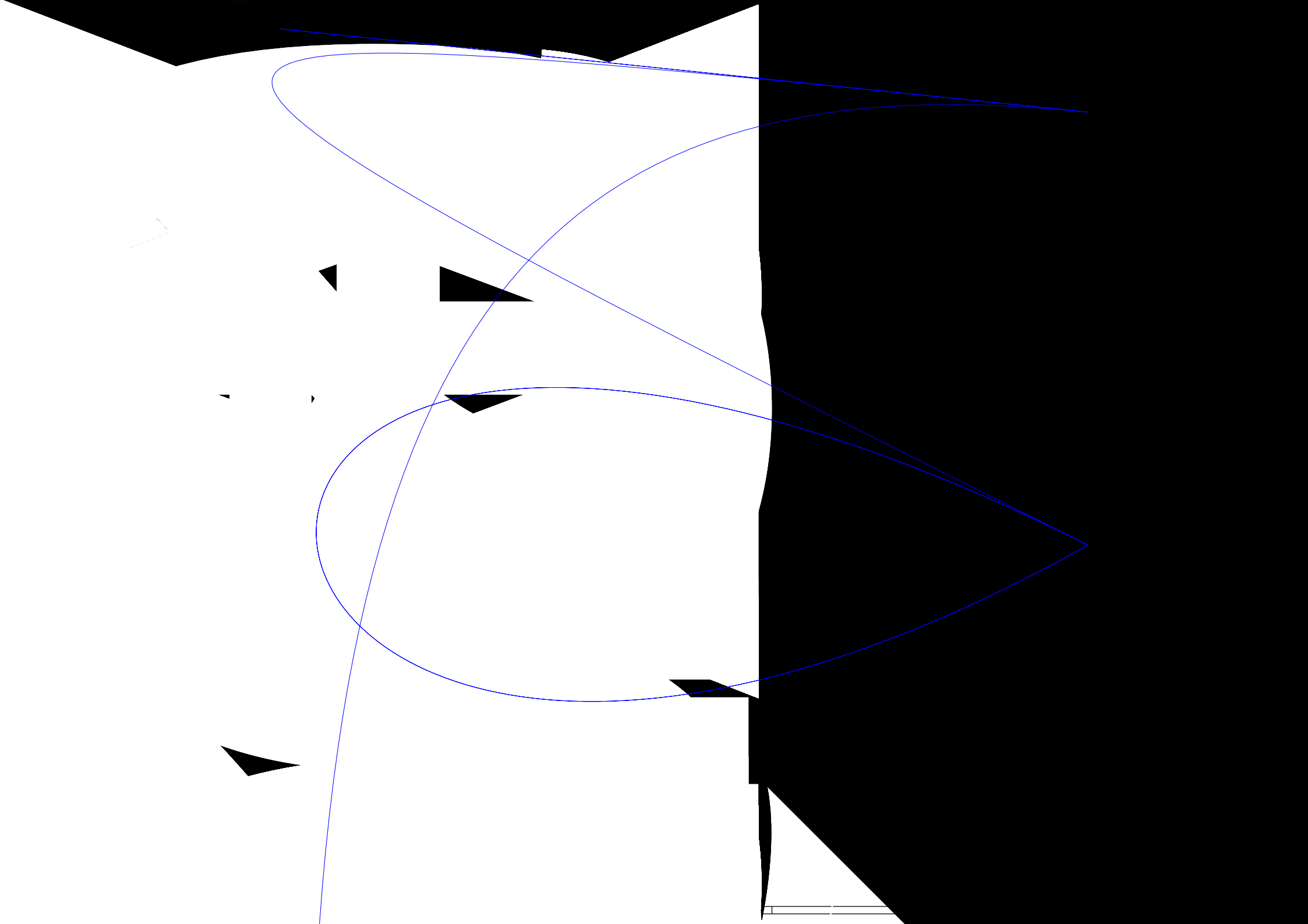
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

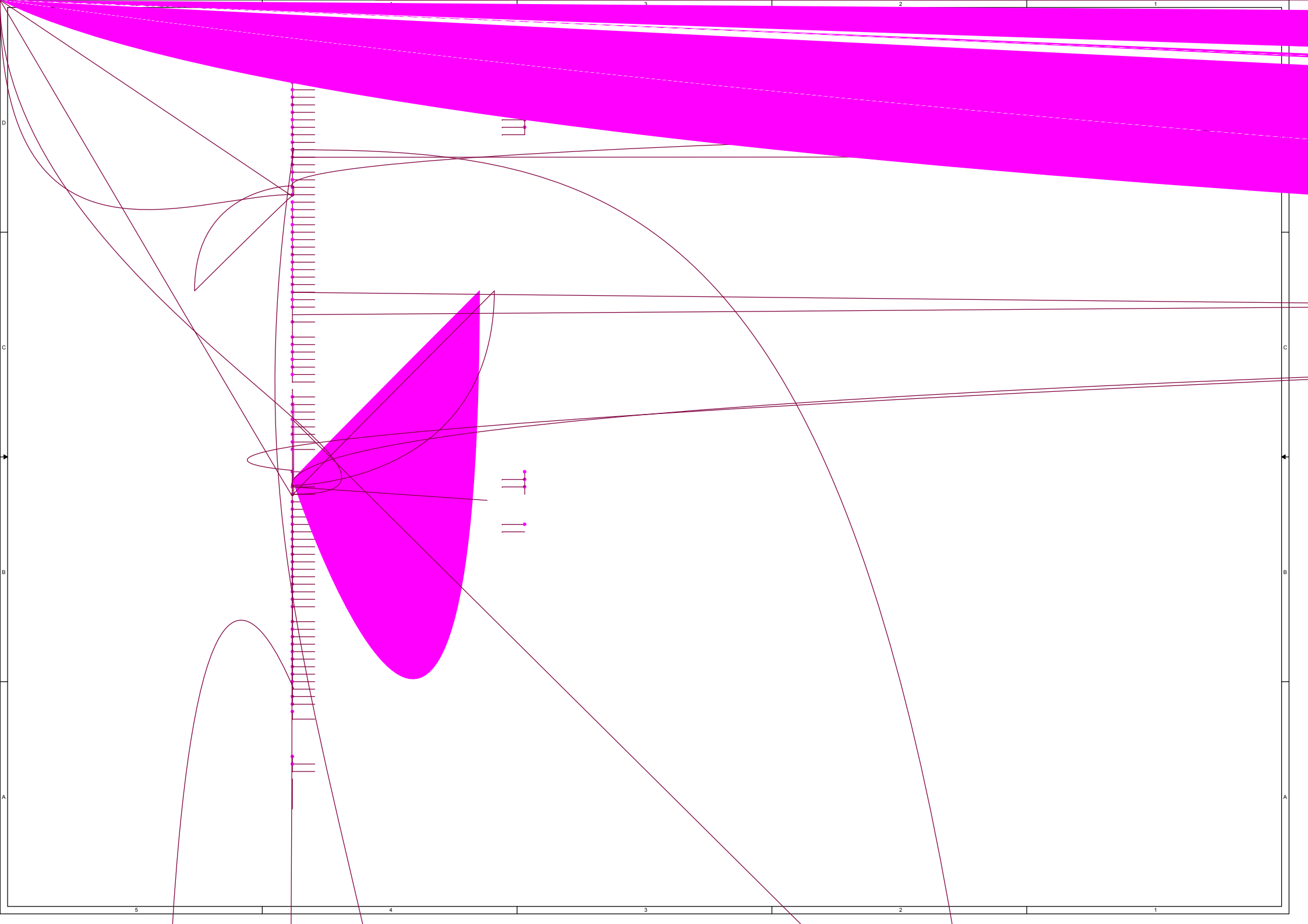
PROJECT :AX3
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	Clock Generator	2A

Date: Thursday, January 07, 2010 Sheet 2 of 30





MCH_CFG_5 DMIx2 selection

Low: DMIx2
High: DMIx4 (Default)

MCH_CFG_16 FSB Dynamic ODT

Low: Dynamic ODT disabled
High: Dynamic ODT enabled (Default)

MCH_CFG_9 PCI Express Graphic Lane

Low: Reverse Lane
High: Normal operation(Default)

MCH_CFG_19 DMI Lane Reversal

Low: Normal (Default)
High: Lane Reserved

MCH_CFG_6 iTPM Host Interface

Low: iTPM Host Interface enabled
High: iTPM Host Interface disabled (Default)

MCH_CFG_7 Intel (R) Management Engine Crypto

Low: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality
High: Intel (R) Management Engine Crypto
TLS cipher suite with no confidentiality (Default)

MCH_CFG_10 PCIe Lookback Enable

Low: Enabled
High: Disabled (Default)

MCH_CFG_12/13 XOR/ALLZ/CLOCK Un-gating

MCH_CFG_13	MCH_CFG_12	Configuration
0	0	Reserved
1	0	XOR Mode enabled
0	1	All-Z Mode enabled
1	1	Normal operation (Default)

U16B

RSVD: M36 RSVD1, N36 RSVD2, R33 RSVD3, T33 RSVD4, AH9 RSVD5, AH10 RSVD6, AH12 RSVD7, AH13 RSVD8, K12 RSVD9, T24, AY21 RSVD20, BG23 RSVD22, BF23 RSVD23, BH18 RSVD24, BF18 RSVD25

DDR CLK/ CONTROL/COMPENSATION: SA_CK_0 AP24 M_A_CLK0 10; SA_CK_1 AT21 M_A_CLK1 10; SB_CK_0 AV24 M_B_CLK0 11; SB_CK_1 AU20 M_B_CLK1 11; SA_CK#_0 AR24 M_A_CLK0# 10; SA_CK#_1 AR21 M_A_CLK1# 10; SB_CK#_0 AU24 M_B_CLK0# 11; SB_CK#_1 AV20 M_B_CLK1# 11; SA_CKE_0 BC28 M_A_CKE0 10; SA_CKE_1 AY28 M_A_CKE1 10; SB_CKE_0 AY36 M_B_CKE0 11; SB_CKE_1 BB36 M_B_CKE1 11; SA_CS#_0 BA17 M_A_CS#0 10; SA_CS#_1 AY16 M_A_CS#1 10; SB_CS#_0 AV16 M_B_CS#0 11; SB_CS#_1 AR13 M_B_CS#1 11; SA_ODT_0 BD17 M_A_ODT0 10; SA_ODT_1 AY17 M_A_ODT1 10; SB_ODT_0 BF15 M_B_ODT0 11; SB_ODT_1 AY13 M_B_ODT1 11; SM_RCOMP BG22 SM_RCOMP; SM_RCOMP# BH21 SM_RCOMP#; SM_RCOMP_VOH BF28 SM_RCOMP_VOH; SM_RCOMP_VOL BH28 SM_RCOMP_VOL; SM_DRAMRST# BC36 DDR3_DRAMRST# 10,11

+1.5VSUS

10/21 Montevina: R80 12K/F_4 +3VSUS; R60 499/F_4; +0.75VSMVREF_MCH; SW_PWROK_NB; SM_REXT

CLK: DPLL_REF_CLK B38 DREFCLK 2; DPLL_REF_CLK# A38 DREFCLK# 2; DPLL_REF_SSCLK E41 DREFSSCLK 2; DPLL_REF_SSCLK# F41 DREFSSCLK# 2; PEG_CLK F43 CLK_PCIE_3GPLL 2; E43 CLK_PCIE_3GPLL# 2

ME JTAG

CFG: MCH_BSEL0 T25 CFG_0; MCH_BSEL1 R25 CFG_1; MCH_BSEL2 P25 CFG_2; MCH_CFG_3 P20 CFG_3; MCH_CFG_4 P24 CFG_4; MCH_CFG_5 C25 CFG_5; MCH_CFG_6 N24 CFG_6; MCH_CFG_7 M24 CFG_7; MCH_CFG_8 E21 CFG_8; MCH_CFG_9 C23 CFG_9; MCH_CFG_10 C24 CFG_10; MCH_CFG_11 N21 CFG_11; MCH_CFG_12 P21 CFG_12; MCH_CFG_13 T21 CFG_13; MCH_CFG_14 R20 CFG_14; MCH_CFG_15 M20 CFG_15; MCH_CFG_16 L21 CFG_16; MCH_CFG_17 H21 CFG_17; MCH_CFG_18 P29 CFG_18; MCH_CFG_19 R28 CFG_19; MCH_CFG_20 T28 CFG_20; TP28; TP8; TP9; TP5

DMI: DMI_RXN_0 AE41 DMI_TXN0; DMI_RXN_1 AE37 DMI_TXN1; DMI_RXN_2 AE47 DMI_TXN2; DMI_RXN_3 AH39 DMI_TXN3 — DMI_TXN[3:0] 15; DMI_RXP_0 AE40 DMI_TXP0; DMI_RXP_1 AE38 DMI_TXP1; DMI_RXP_2 AE48 DMI_TXP2; DMI_RXP_3 AH40 DMI_TXP3 — DMI_TXP[3:0] 15; DMI_TXN_0 AE35 DMI_RXN0; DMI_TXN_1 AE43 DMI_RXN1; DMI_TXN_2 AE46 DMI_RXN2; DMI_TXN_3 AH42 DMI_RXN3 — DMI_RXN[3:0] 15; DMI_TXP_0 AD35 DMI_RXP0; DMI_TXP_1 AE44 DMI_RXP1; DMI_TXP_2 AF46 DMI_RXP2; DMI_TXP_3 AH43 DMI_RXP3 — DMI_RXP[3:0] 15

GRAPHICS VID: GFX_VID_0 B33 GFXVR_VID_0; GFX_VID_1 B32 GFXVR_VID_1; GFX_VID_2 G33 GFXVR_VID_2; GFX_VID_3 F33 GFXVR_VID_3; GFXVR_VID_4 TP34; GFX_VR_EN C34 GFXVR_EN TP67

PM: 16 PM_SYNC# R29; 3,14,28 H_DPRSTP# B7; 10,11 PM_EXTTS#0 N33; 11 PM_EXTTS#1 P32; 16,28 DELAY_VR_PWRGOOD AT40; 15 PLT_RST-R# RST_IN# MCH AT11; 3,14 PM_THRMTRIP# T20; 16,28 DPRSLPVR R32 — PM_SYNC# PM_DPRSTP# PM_EXT_TS#_0 PM_EXT_TS#_1 PWROK RSTIN# THERMTRIP# DPRSLPVR

ME: CL_CLK AH37 CL_CLK0 16; CL_DATA AH36 CL_DATA0 16; CL_PWROK AN36 ECPWROK 4,16,24; CL_RST# AJ35 CL_RST#0 16; CL_VREF AH34 MCH_CLVREF — 0.35 V; R79 1K/F_4; R76 499/F_4; +1.05V

MISC: SDVO_CTRLCLK G36 SDVO_CLK 13; SDVO_CTRLDATA E36 SDVO_DATA 13; CLKREQ# K36 CLK_MCH_OE# 2; ICH_SYNC# H36 MCH_ICH_SYNC# 16; DDPC_CTRLCLK; DDPPC_CTRLDATA; TSATN# B12 MCH_TSATN; +1.05V

HDA: ACZ_SDIN3_MCH — ACZ_BITCLK_MCH 14; ACZ_RST#_MCH 14; ACZ_SDIN3 14; ACZ_SDOUT_MCH 14; ACZ_SYNC_MCH 14

12/7 PV for PE request.

01/06 MV modify

NC: BG48 NC_1, BF48 NC_2, BD48 NC_3, BC48 NC_4, BH47 NC_5, BG47 NC_6, BE47 NC_7, BH46 NC_8, BF46 NC_9, BG45 NC_10, BH44 NC_11, BH43 NC_12, BH6 NC_13, BH5 NC_14, BG4 NC_15, A47 NC_26

CANTIGA_GM

+3V — R121 10K/F_4 — PM_EXTTS#0 — PM_EXTTS#1

ACZ_BITCLK_MCH

C488 *33P/50V_4

12 DPST_PWM; 12 LVDS_BLON; R119 10K/F_4 L_CTRL_CLK; +3V; L_CTRL_DATA

12 EDIDCLK; 12 EDIDDATA

12 DISP_ON — LVDS_IBG; LVDS_VBG; TP35

12 LA_CLK#; 12 LA_CLK; 12 LB_CLK#; 12 LB_CLK

12 LA_DATAN0; 12 LA_DATAN1; 12 LA_DATAN2; LA_DATAN3

12 LA_DATAP0; 12 LA_DATAP1; 12 LA_DATAP2; LA_DATAP3

12 LB_DATAN0; 12 LB_DATAN1; 12 LB_DATAN2; LB_DATAN3

12 LB_DATAP0; 12 LB_DATAP1; 12 LB_DATAP2; LB_DATAP3; TP29

TV_DCONSEL0; TV_DCONSEL1

13 CRT_B; 13 CRT_G; 13 CRT_R

13 DDCCLK; 13 DDCDATA; 13 HSYNC_COM; 13 VSYNC_COM — DDCCLK_INT; DDCDATA_INT; HSYNC_INT; CRTIREF; VSYNC_INT

10/21 Montevina +1.5VSUS

SM_RCOMP_VOH — C462 0.01U/25V_4 — R257 3.01K/F_4

SM_RCOMP_VOL — C460 0.01U/25V_4

+1.5VSUS 10/21 Montevina — R75 *1K/F_4; +0.75VSMVREF_MCH; R77 *0_4/S short0402; DDR_VTTREF 10,29; C213 0.1U/10V_4

HP SVTP TEST

PEG_COMP — +1.05V_PEG

HDMI_HPD#

C_PEG_TX#0 C_PEG_TX#1 C_PEG_TX#2 C_PEG_TX#3 — IN_D2# 13; IN_D1# 13; IN_D0# 13; IN_CLK# 13

C_PEG_TX0 C_PEG_TX1 C_PEG_TX2 C_PEG_TX3 — C253 0.1U/10V_4 — IN_D2 13; IN_D1 13; IN_D0 13; IN_CLK 13

For UMA HDMI Function

+3V — Ro R106 *20K/F_4 — HDMI_HPD# — Level: 0.9V

Rq

13 HDMI_HPD_CON — Rp R104 *7.5K/F_4

HPD# Inverting Level Shifting Circuit

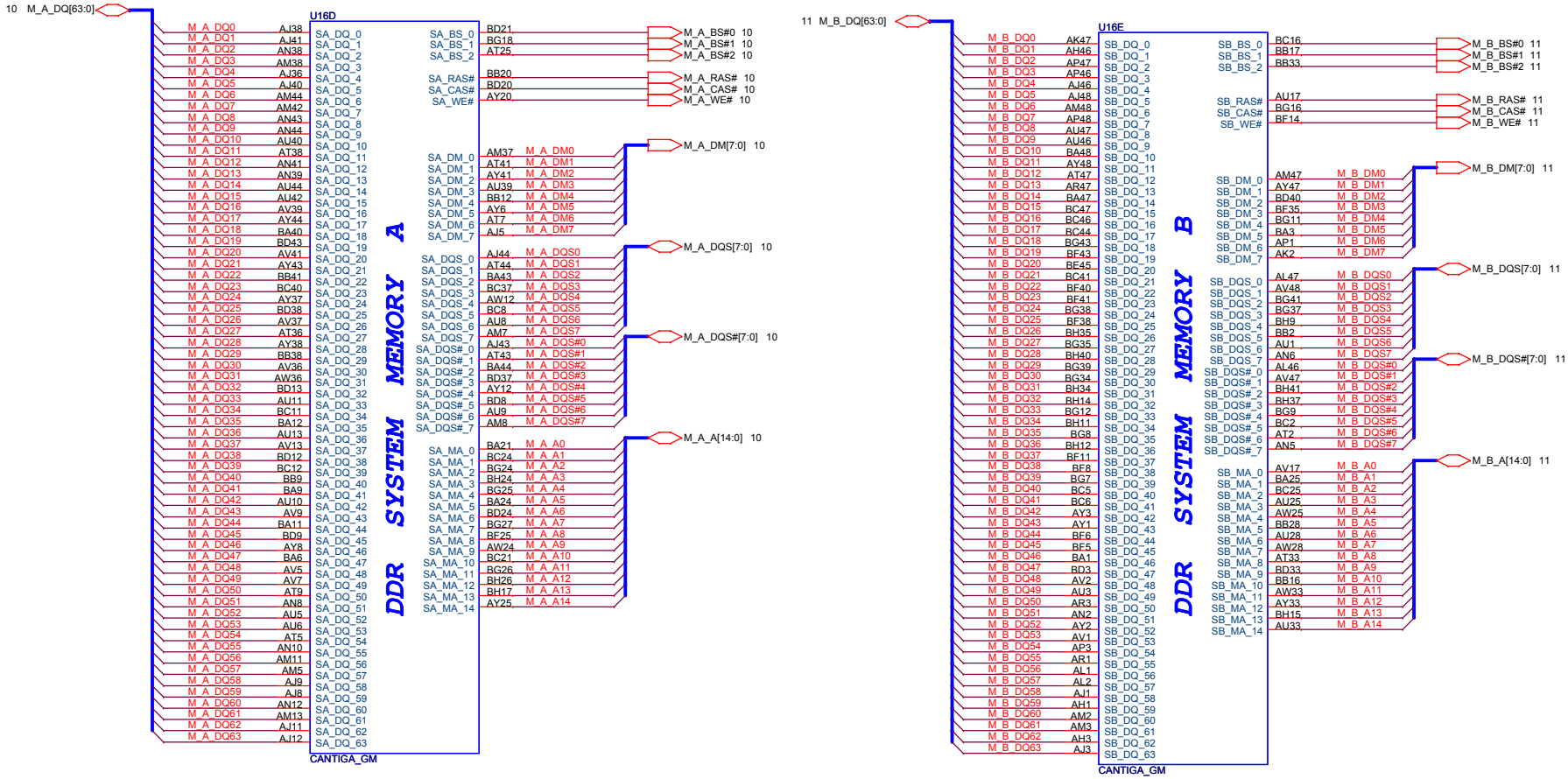
2,3,4,5,8,9,14,17,27,28 +1.05V
2,3,4,5,8,9,14,17,27,28 +1.05V_PEG
8,9,10,11,29,30 +1.5VSUS
2,4,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,24,28,30 +3V

NB5

PROJECT :AX3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga DMI/Display 2/5	2A

Date: Thursday, January 07, 2010 Sheet 6 of 30



NB5

PROJECT :AX3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga DDR3 3/5	2A

Date: Thursday, January 07, 2010 | Sheet 7 of 30

10/21 Montevina +1.5VSUS

2600mA

Ivcc_axg=6326.84mA

Ivcc=1930.4+508.12=2438.52mA

U16G

U16F

VCC_SM_36 through VCC_SM_42 can be left as NC for DDR2 desgins.

VCC_SM_36 VCC_SM_37 VCC_SM_38 VCC_SM_40 VCC_SM_42

VCC SM POWER

VCC GFX NCTF

VCC GFX

VCC SM LF

VCC CORE POWER

VCC NCTF

CANTIGA_GM

R65 10_4

R64 10_4

VCC_AXG_SENSE VSS_AXG_SENSE

+VCCSM_LF1 +VCCSM_LF2 +VCCSM_LF3 +VCCSM_LF4 +VCCSM_LF5 +VCCSM_LF6 +VCCSM_LF7

C464 *330u_2.5V_7343 C86 10U/6.3V_8 C240 10U/6.3V_8 C202 0.33U/6.3V_4 C171 0.33U/6.3V_4 C176 0.1U/10V_4

C126 0.1U/10V_4 C133 10U/6.3V_8 C141 10U/6.3V_8 C467 10U/6.3V_8 C465 10U/6.3V_8

C169 *0.1U/10V_4 C148 *0.1U/10V_4 C103 *0.1U/10V_4 C125 *0.1U/10V_4 C127 *0.1U/10V_4

C445 *390U/2.5V_6X5.8ESR10 C184 0.47U/6.3V_4 C200 1U/6.3V_4 C206 10U/6.3V_8 C153 10U/6.3V_8 C246 10U/6.3V_8 C185 0.1U/10V_4 C180 0.1U/10V_4

C117 0.1U/10V_4 C137 0.1U/10V_4 C93 0.33U/6.3V_4 C147 0.33U/6.3V_4 C222 0.47U/6.3V_4 C172 1U/6.3V_4 C217 1U/6.3V_4

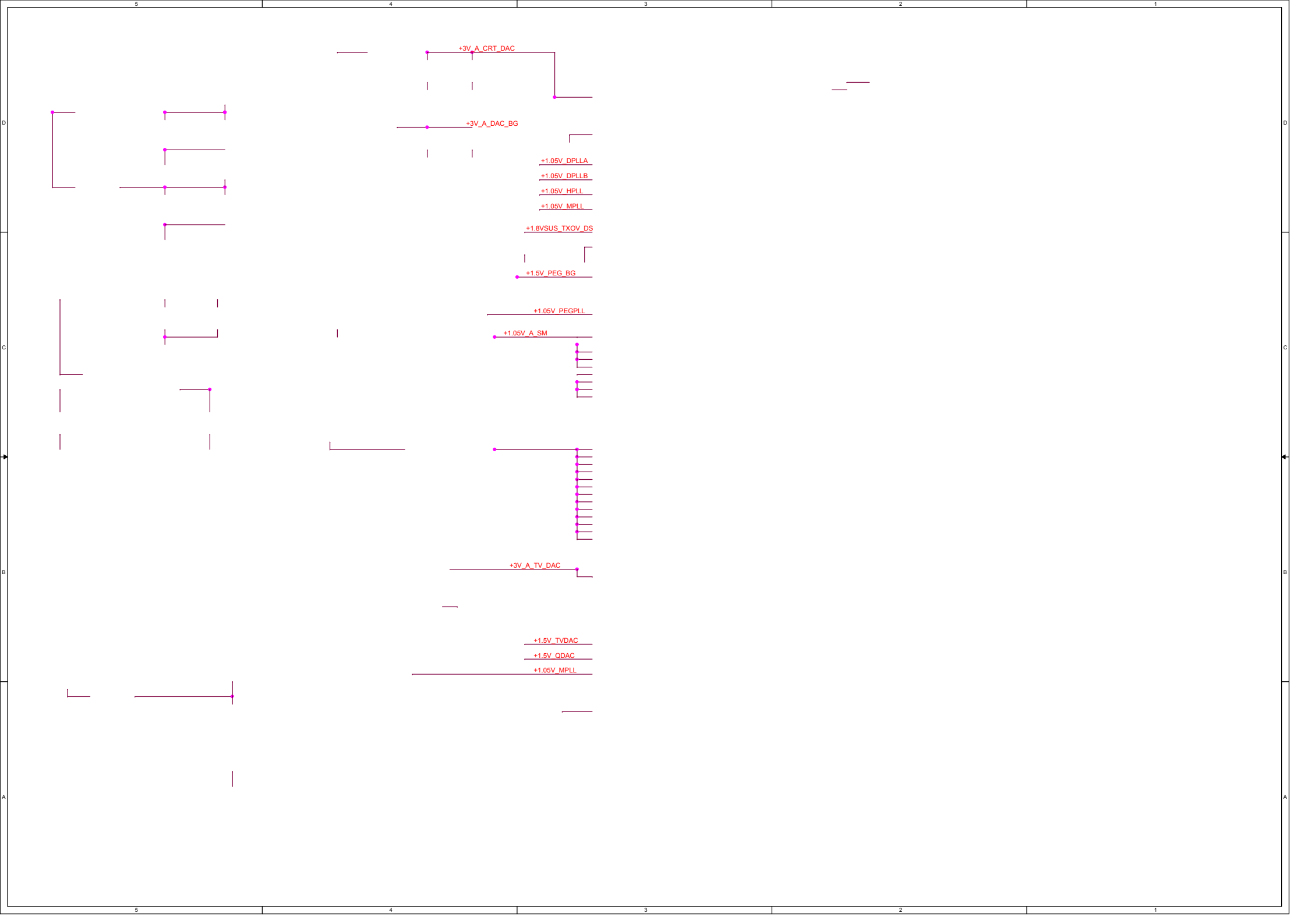
2,3,4,5,6,9,14,17,27,28 +1.05V
6,9,10,11,29,30 +1.5VSUS

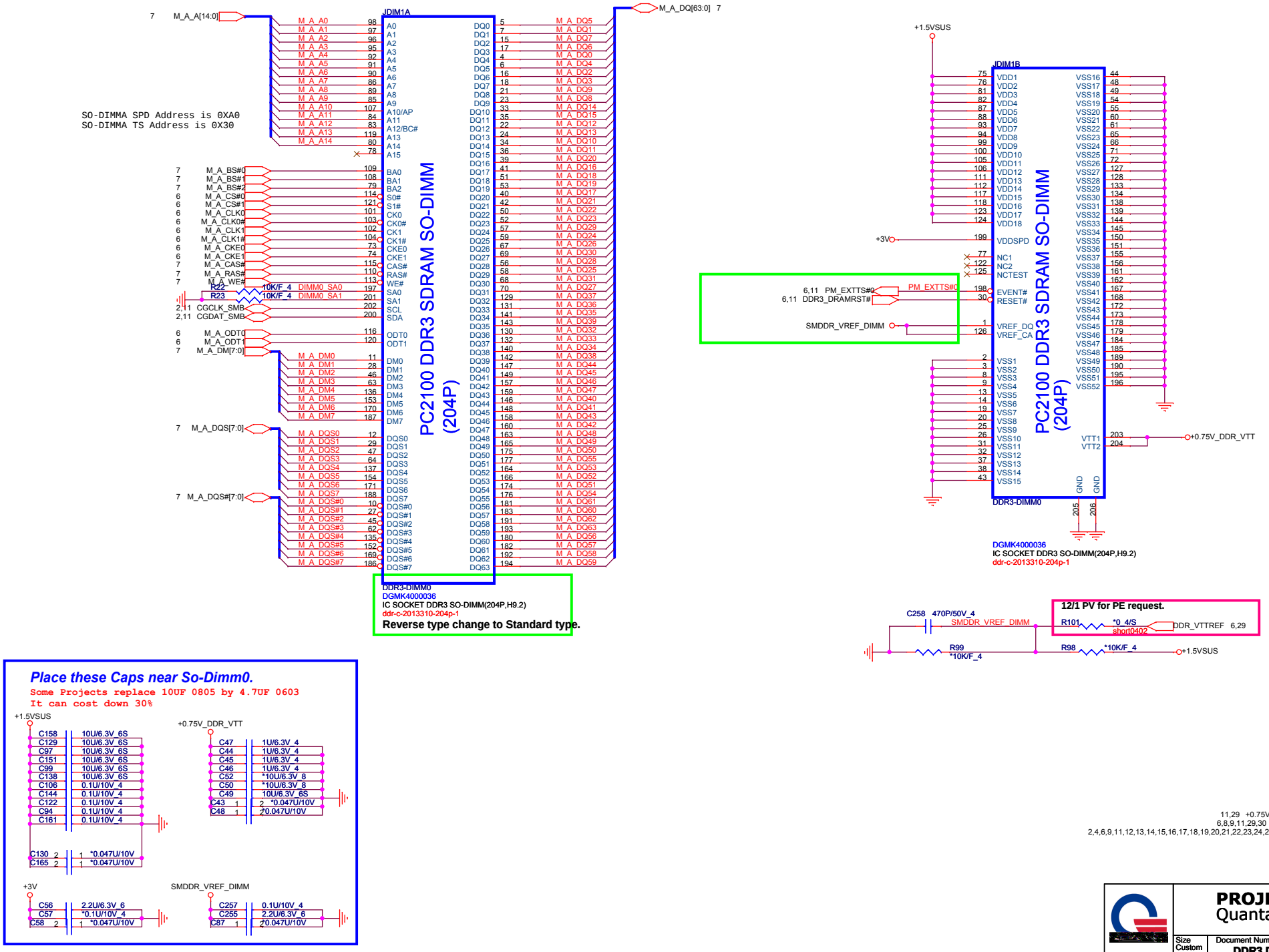
PROJECT :AX3
Quanta Computer Inc.

NB5

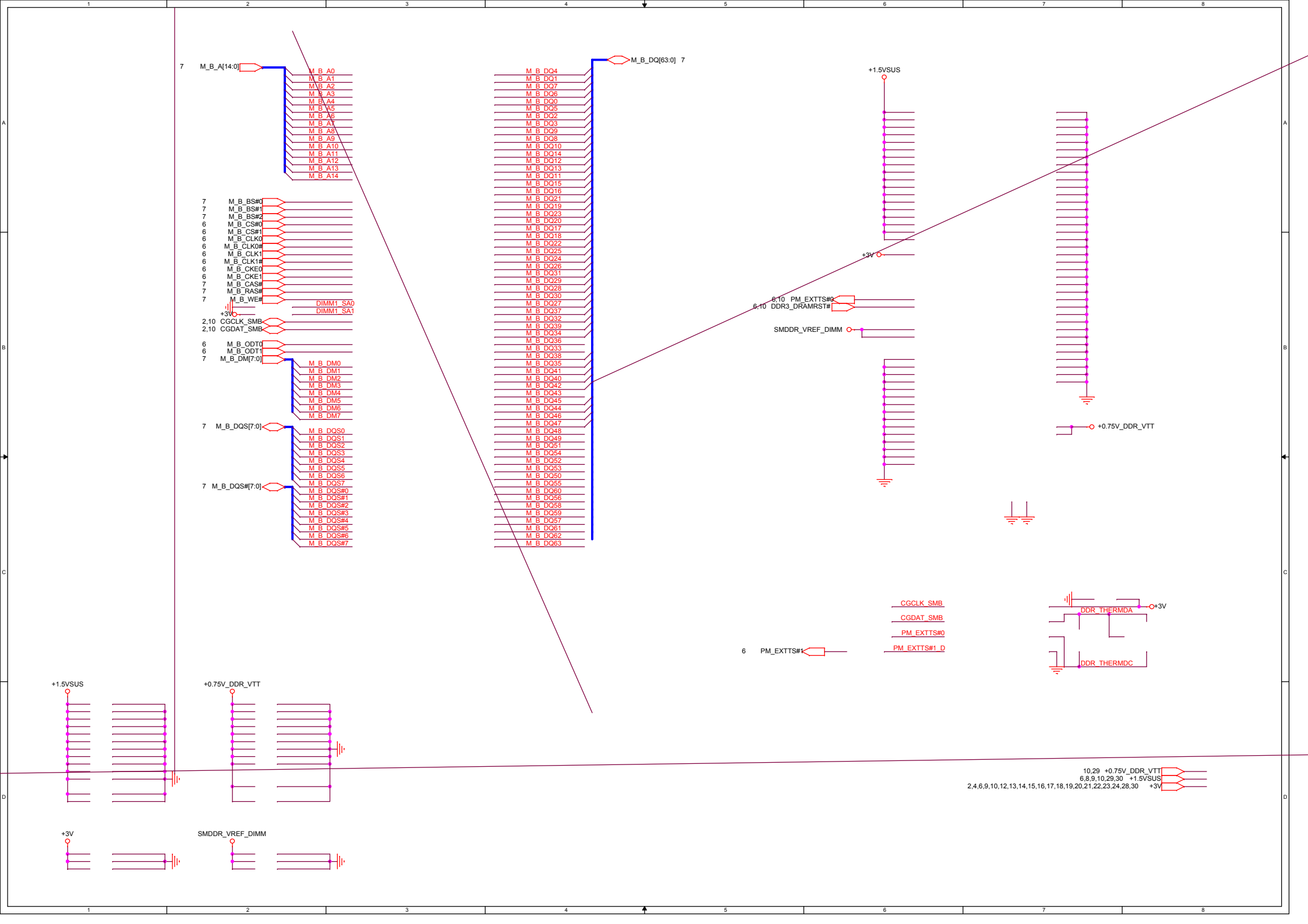
Size	Document Number	Rev
Custom	Cantiga VCC 4/5	2A

Date: Thursday, January 07, 2010 Sheet 8 of 30

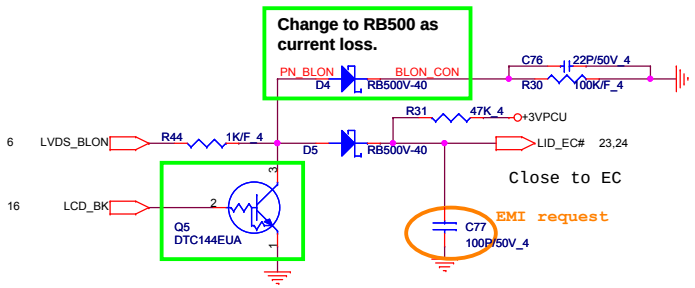

+3V_A_CRT_DAC
+3V_A_DAC_BG
+1.05V_DPLLA
+1.05V_DPLLB
+1.05V_HPLL
+1.05V_MPLL
+1.8VSUS_TXOV_DS
+1.5V_PEG_BG
+1.05V_PEGPLL
+1.05V_A_SM
+3V_A_TV_DAC
+1.5V_TVDAC
+1.5V_QDAC
+1.05V_MPLL

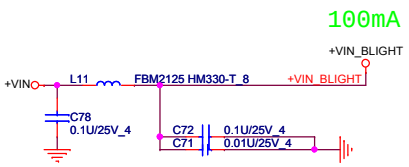


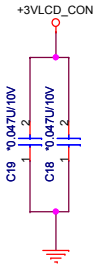
Project	PROJECT :AX3 Quanta Computer Inc.
Size	Custom
Document Number	DDR3 DIMM-0
Rev	2A
Date	Thursday, January 07, 2010
Sheet	10 of 30
NB5	

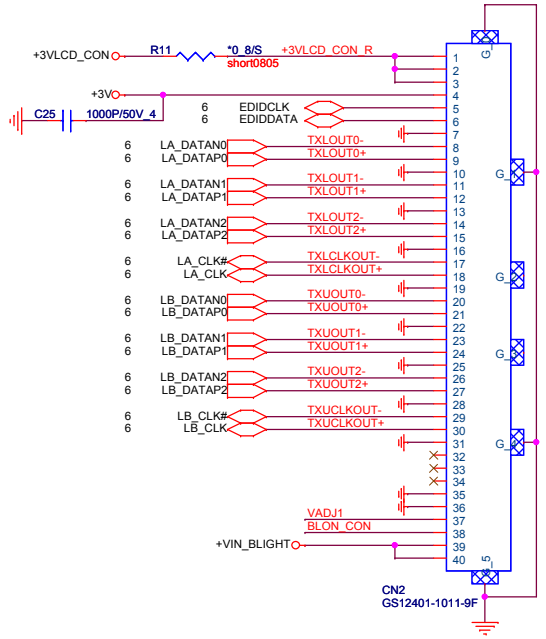

7 M_B_A[14:0]
M_B_A0
M_B_A1
M_B_A2
M_B_A3
M_B_A4
M_B_A5
M_B_A6
M_B_A7
M_B_A8
M_B_A9
M_B_A10
M_B_A11
M_B_A12
M_B_A13
M_B_A14
7 M_B_BS#0
7 M_B_BS#1
7 M_B_BS#2
6 M_B_CS#0
6 M_B_CS#1
6 M_B_CLK0
6 M_B_CLK0#
6 M_B_CLK1
6 M_B_CLK1#
6 M_B_CKE0
6 M_B_CKE1
7 M_B_CAS#
7 M_B_RAS#
7 M_B_WE#
DIMM1_SA0
DIMM1_SA1
+3V
2,10 CGCLK_SMB
2,10 CGDAT_SMB
6 M_B_ODT0
6 M_B_ODT1
7 M_B_DM[7:0]
M_B_DM0
M_B_DM1
M_B_DM2
M_B_DM3
M_B_DM4
M_B_DM5
M_B_DM6
M_B_DM7
7 M_B_DQS[7:0]
M_B_DQS0
M_B_DQS1
M_B_DQS2
M_B_DQS3
M_B_DQS4
M_B_DQS5
M_B_DQS6
M_B_DQS7
7 M_B_DQS#[7:0]
M_B_DQS#0
M_B_DQS#1
M_B_DQS#2
M_B_DQS#3
M_B_DQS#4
M_B_DQS#5
M_B_DQS#6
M_B_DQS#7
M_B_DQ[63:0] 7
M_B_DQ4
M_B_DQ1
M_B_DQ7
M_B_DQ6
M_B_DQ0
M_B_DQ5
M_B_DQ2
M_B_DQ3
M_B_DQ9
M_B_DQ8
M_B_DQ10
M_B_DQ14
M_B_DQ12
M_B_DQ13
M_B_DQ11
M_B_DQ15
M_B_DQ16
M_B_DQ21
M_B_DQ19
M_B_DQ23
M_B_DQ20
M_B_DQ17
M_B_DQ18
M_B_DQ22
M_B_DQ25
M_B_DQ24
M_B_DQ26
M_B_DQ31
M_B_DQ29
M_B_DQ28
M_B_DQ30
M_B_DQ27
M_B_DQ37
M_B_DQ32
M_B_DQ39
M_B_DQ34
M_B_DQ36
M_B_DQ33
M_B_DQ38
M_B_DQ35
M_B_DQ41
M_B_DQ40
M_B_DQ42
M_B_DQ43
M_B_DQ45
M_B_DQ44
M_B_DQ46
M_B_DQ47
M_B_DQ48
M_B_DQ49
M_B_DQ51
M_B_DQ54
M_B_DQ52
M_B_DQ53
M_B_DQ50
M_B_DQ55
M_B_DQ60
M_B_DQ56
M_B_DQ58
M_B_DQ59
M_B_DQ57
M_B_DQ61
M_B_DQ62
M_B_DQ63
+1.5VSUS
+3V
6,10 PM_EXTTS#0
6,10 DDR3_DRAMRST#
SMDDR_VREF_DIMM
+0.75V_DDR_VTT
CGCLK_SMB
CGDAT_SMB
PM_EXTTS#0
PM_EXTTS#1_D
6 PM_EXTTS#1
DDR_THERMDA
DDR_THERMDC
+3V
+1.5VSUS
+0.75V_DDR_VTT
+3V
SMDDR_VREF_DIMM
10,29 +0.75V_DDR_VTT
6,8,9,10,29,30 +1.5VSUS
2,4,6,9,10,12,13,14,15,16,17,18,19,20,21,22,23,24,28,30 +3V

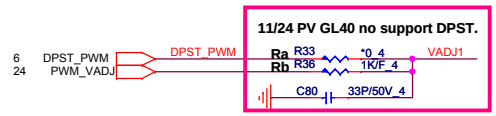
LID Switch

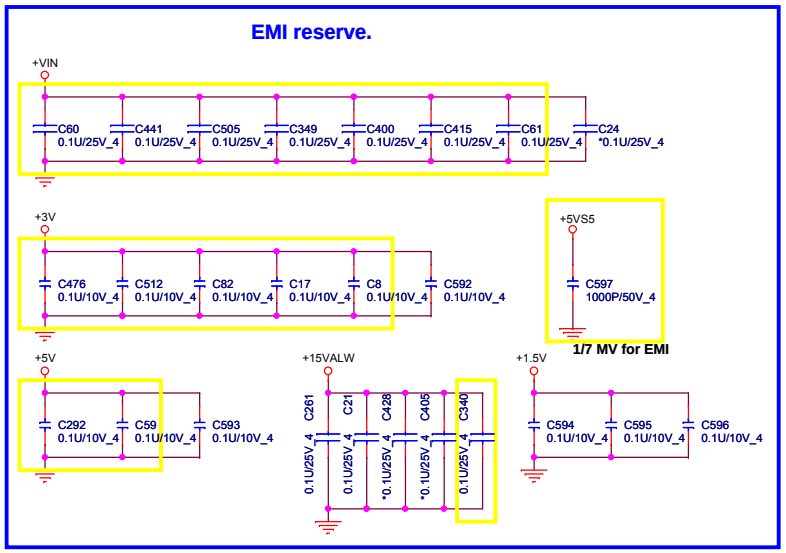


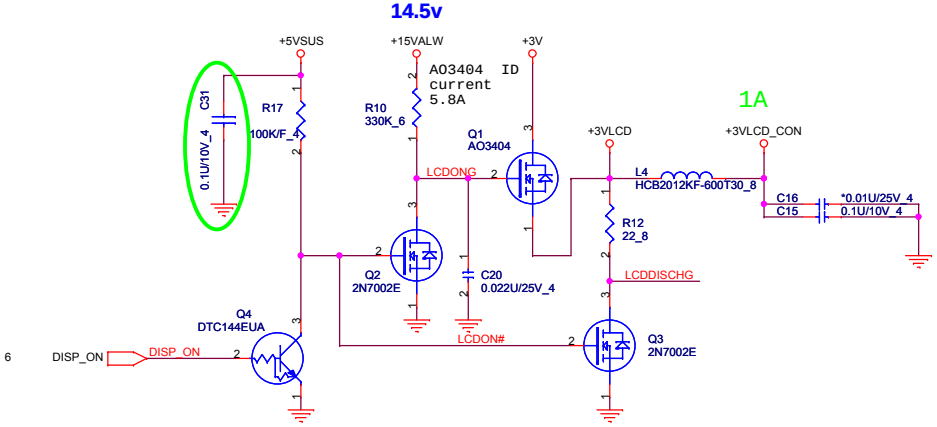












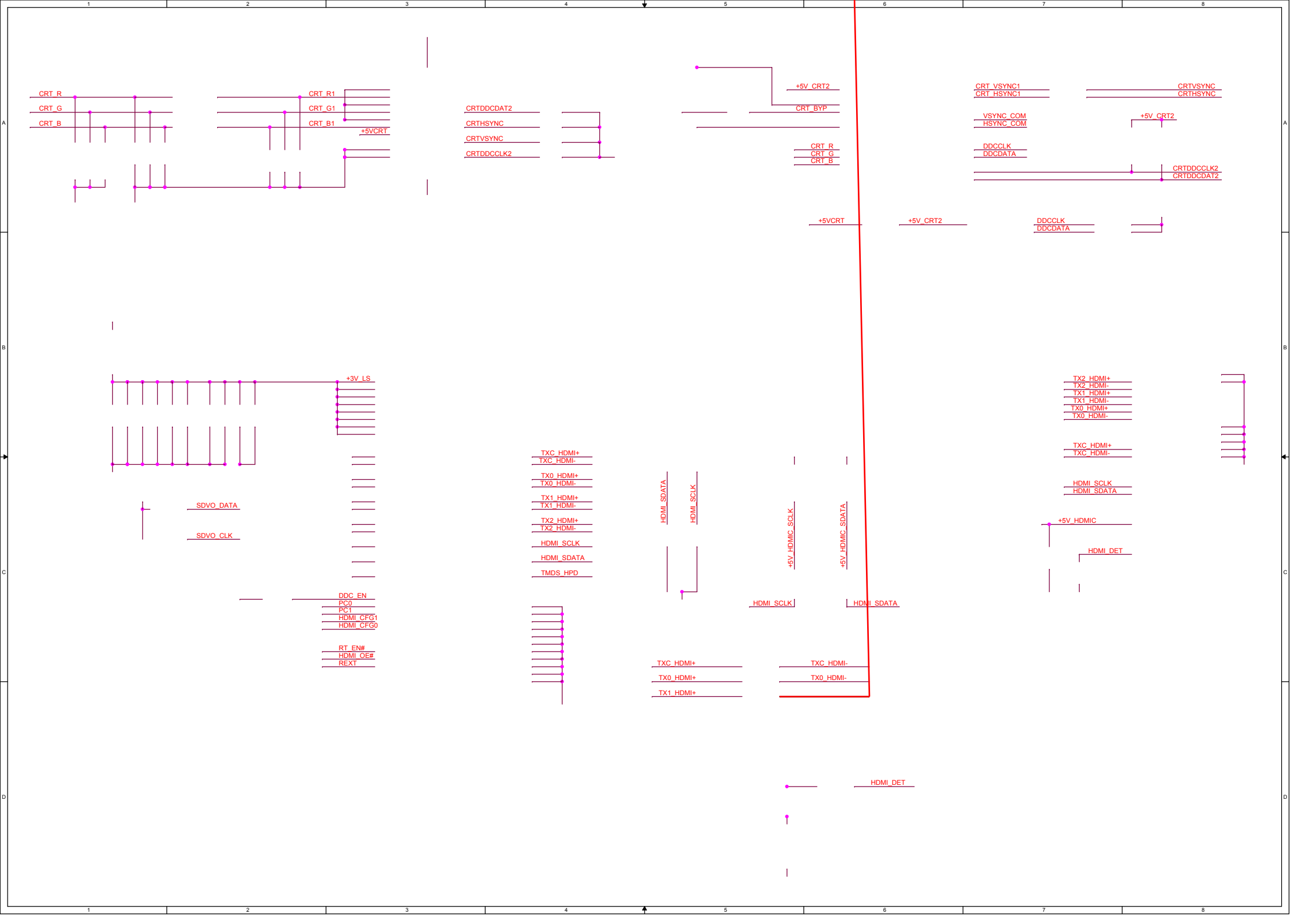
4,9,14,15,17,19,21,22,30 +1.5V
2,4,6,9,10,11,13,14,15,16,17,18,19,20,21,22,23,24,28,30 +3V
14,21,22,23,24,25,26,27,30 +3VPCU
13,17,19,21,22,23,24,30 +5V
23,30 +5VSUS
21,26,30 +15VALW
25,26,27,28,29,30 +VIN

PROJECT :AX3
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	LCD CONN/LID	2A

Date: Monday, January 11, 2010 Sheet 12 of 30


CRT_R
CRT_G
CRT_B
CRT_R1
CRT_G1
CRT_B1
+5VCRT
CRTDDCDAT2
CRTHSYNC
CRTVSYNC
CRTDDCCLK2
+5V_CRT2
CRT_BYP
CRT_R
CRT_G
CRT_B
CRT_VSYNC1
CRT_HSYNC1
CRTVSYNC
CRTHSYNC
VSYNC_COM
HSYNC_COM
+5V_CRT2
DDCCLK
DDCDATA
CRTDDCCLK2
CRTDDCDAT2
+5VCRT
+5V_CRT2
DDCCLK
DDCDATA
+3V_LS
SDVO_DATA
SDVO_CLK
DDC_EN
PC0
PC1
HDMI_CFG1
HDMI_CFG0
RT_EN#
HDMI_OE#
REXT
TXC_HDMI+
TXC_HDMI-
TX0_HDMI+
TX0_HDMI-
TX1_HDMI+
TX1_HDMI-
TX2_HDMI+
TX2_HDMI-
HDMI_SCLK
HDMI_SDATA
TMDS_HPD
HDMI_SDATA
HDMI_SCLK
+5V_HDMIC_SCLK
+5V_HDMIC_SDATA
HDMI_SCLK
HDMI_SDATA
TXC_HDMI+
TX0_HDMI+
TX1_HDMI+
TXC_HDMI-
TX0_HDMI-
HDMI_DET
TX2_HDMI+
TX2_HDMI-
TX1_HDMI+
TX1_HDMI-
TX0_HDMI+
TX0_HDMI-
TXC_HDMI+
TXC_HDMI-
HDMI_SCLK
HDMI_SDATA
+5V_HDMIC
HDMI_DET

DB: change from 18P to 15P(TXC suggestion)

Delete Pin AG7 for Lan_DISABLE#

Notice: GPIO33 is also a strap pin. Don't pull it to high.

HP Request

SB Strap

ICH9-M Internal VR Enable strap (Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

ICH9-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

XOR Chain Entrance Strap

ICH_TP3	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

ICH9 Boot BIOS select

STRAP	PCI_GNT0#	SPI_CS#1	
SPI	0	1	
PCI	1	0	
LPC	1	1	(default)

A16 swap override strap

PCI_GNT#3	Low = A16 swap override enabled Hi = Default

No Reboot Strap	
ACZ_SPKR	Low: Default Hi: No reboot

TPM physical presence	
ICH_GPIO57	Low: Default

PROJECT :AX3
Quanta Computer Inc.

NB5

Size	Document Number	Rev
Custom	ICH9-M SATA/HDA/RTC 1/4	2A

Date: Thursday, January 07, 2010 Sheet 14 of 30

PCIE_RXN0
PCIE_RXP0
PCIE_TXN0_C
PCIE_TXP0_C

PCIE_TXN1_C
PCIE_TXP1_C

DMI_RXN0 6
DMI_RXP0 6
DMI_TXP0 6
DMI_RXN1 6
DMI_RXP1 6
DMI_RXN2 6
DMI_RXP2 6
DMI_RXN3 6
DMI_RXP3 6

CLK_PCIE_ICH# 2
CLK_PCIE_ICH 2

DMI_IRCOMP_R

INTF#
LOCK#
IRDY#
PERR#

REQ0#
INTG#
INTE#
INTB#

REQ2#
REQ3#
FRAME#
TRDY#

REQ1#
DEVSEL#
INTD#
STOP#

SPI_CLK_R
SPI_CS#0_R

SPI_MOSI
SPI_MISO

USB_OC#0
USB_OC#1
USB_OC#2
USB_OC#3
USB_OC#4
USB_OC#5
USB_OC#6
USB_OC#7
USB_OC#8
USB_OC#9
USB_OC#10
USB_OC#11

USBRBIAS_PN

INTH#
INTA#
SERR#
INTC#

USB_OC#7
USB_OC#4
USB_OC#5
USB_OC#6

USB_OC#10
USB_OC#1
USB_OC#0
USB_OC#11

SPI_HOLD#

SPI_CS#0_R
SPI_CLK_R
SPI_MOSI
SPI_MISO

SPI_WP#

SPI_CLK_R

USB_OC#2
USB_OC#3
USB_OC#8
USB_OC#9

PCI_PME#

REQ0#
GNT0#
REQ1#
GNT1#
REQ2#
GNT2#
REQ3#
GNT3#

GNT0# 14

PCLK_ICH

IRDY#

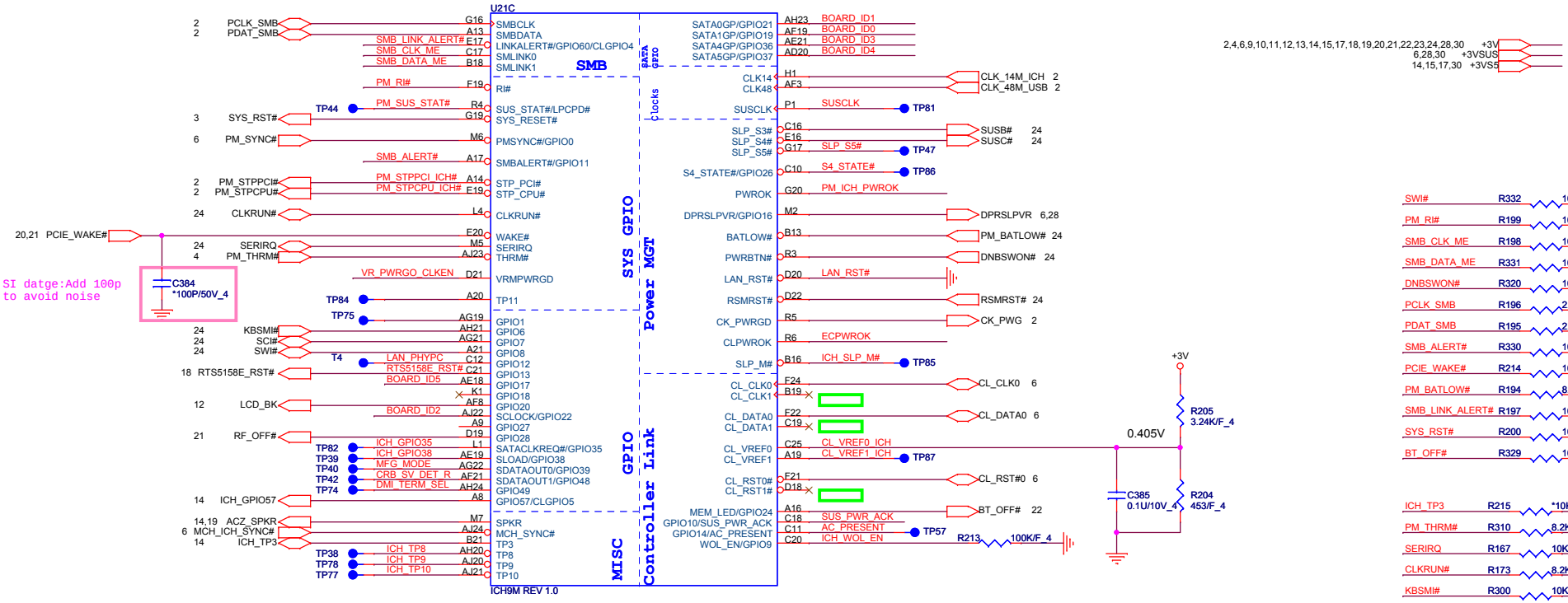
DEVSEL#
PERR#
LOCK#
SERR#
STOP#
TRDY#
FRAME#

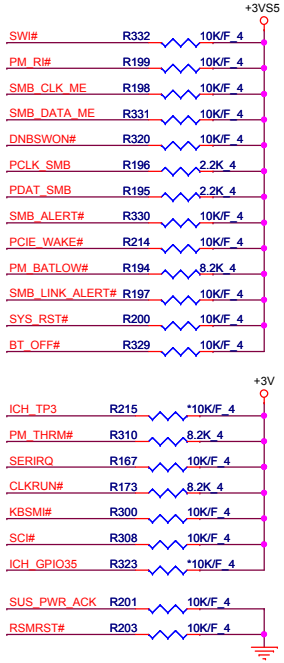
PLT_RST-R#

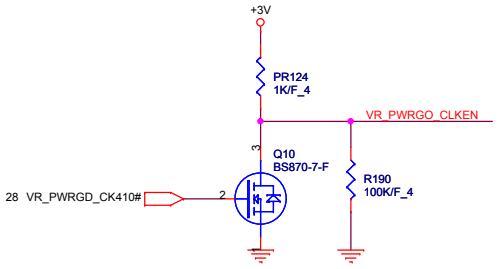
PLT_RST-R# 6
PCLK_ICH 2
PCI_PME#

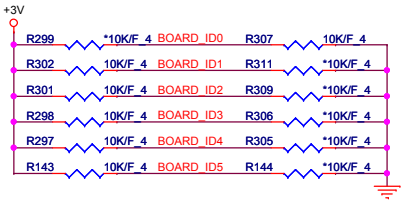
INTA#
INTB#
INTC#
INTD#

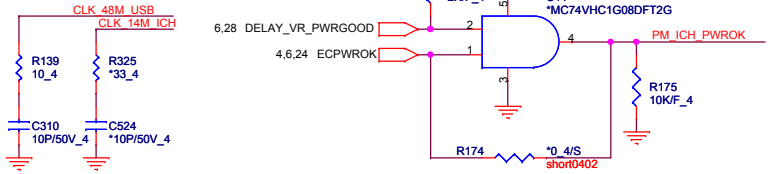
INTE#
INTF#
INTG#
INTH#











Board ID	ID0 GPIO19	ID1 GPIO21	ID2 GPIO22	ID3 GPIO36	ID4 GPIO37	ID5 GPIO17
UMA/DIS	0=UMA 1=Dis.					
CR/HDMI		0=No 1=Yes				
Reserve			0=No 1=Yes			
Reserve				0=No 1=Yes		
Reserve					0=No 1=Yes	
Reserve						0=No 1=Yes

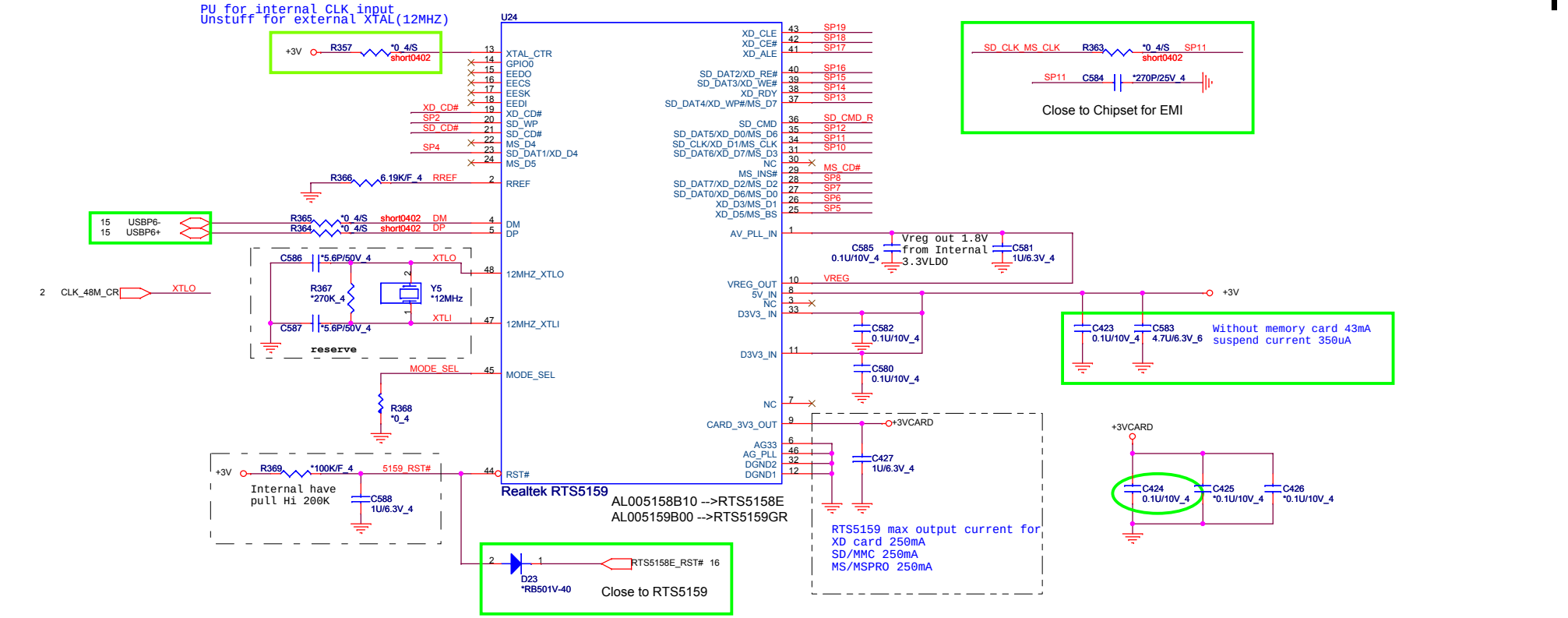
AX3 MB P/N	ID0	ID1	ID2	ID3	ID4	ID5
31AX6MB0000 (CHR)	0	1	1	1	1	1
31AX6MB0010 (PDT)	0	1	1	1	1	1
31AX6MB0020 (PIM)	0	1	1	1	1	1
31AX6MB0030	0	0	1	1	1	1

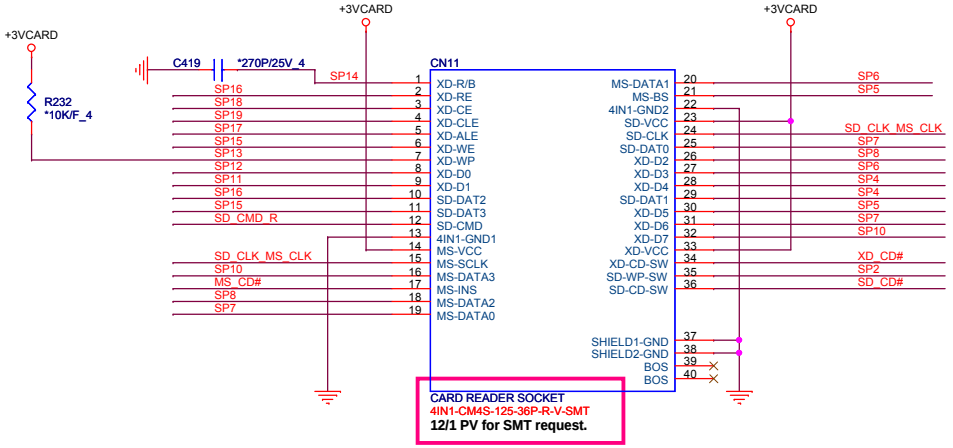
PROJECT :AX3
Quanta Computer Inc.

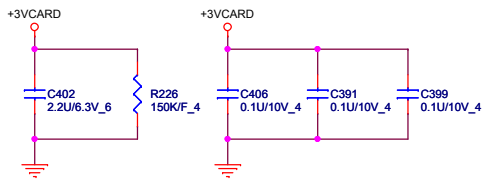
Size	Document Number	Rev
Custom	ICH9-M GPIO/Board ID 3/4	2A
Date: Thursday, January 07, 2010	Sheet 16 of 30	

NB5

+5VREF
+5VREF_SUS
+1.5V_APLL_ICH
+3V_VCCPAUX
+1.05V_LAN_ICH
+1.5V_ICH_GLANPLL
+1.5V_ICH_VCCDMIPLL
+1.05V_CPU_IO
+3V_DMI_ICH
+3V_SATA_ICH
+3V_VCCPCORE_ICH
+3V_PCI_ICH
TP_VCCSUS1_05_ICH_2
TP_VCCSUS1_5_ICH_1
+1.5VSUS_INT_ICH
+3VS5_SB_2
+1.05V_CL_INT_ICH
+3V_CL_ICH







Note:

	SD/MMC	MS	XD
SP0			
SP1			XD_CD#
SP2	SD_WP		
SP3	SD_CD#		
SP4	SD_DAT1		XD_D4
SP5		MS_BS	XD_D5
SP6		MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

5 IN1 CARD-READER (PUSH-PUSH)

Support SD/SD PRO/MMC/MS/MS PRO/xD Cards

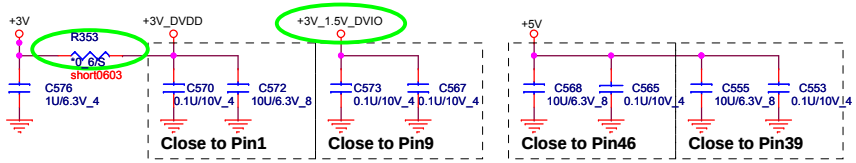
2,4,6,9,10,11,12,13,14,15,16,17,19,20,21,22,23,24,28,30 +3V

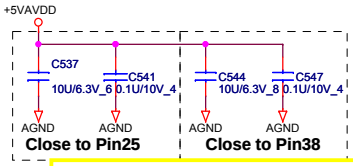
NB5

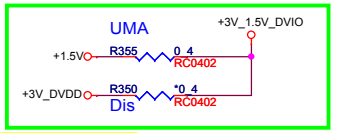
PROJECT :AX3
Quanta Computer Inc.

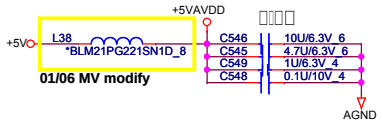
Size	Document Number	Rev
Custom	RTS5159/CR Socket	2A

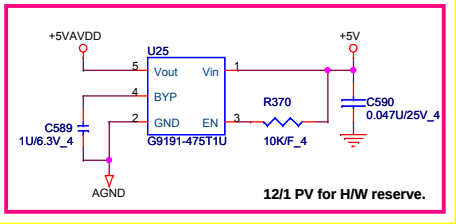
Date: Thursday, January 07, 2010 | Sheet 18 of 30

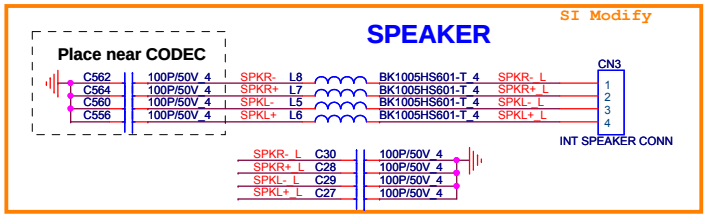


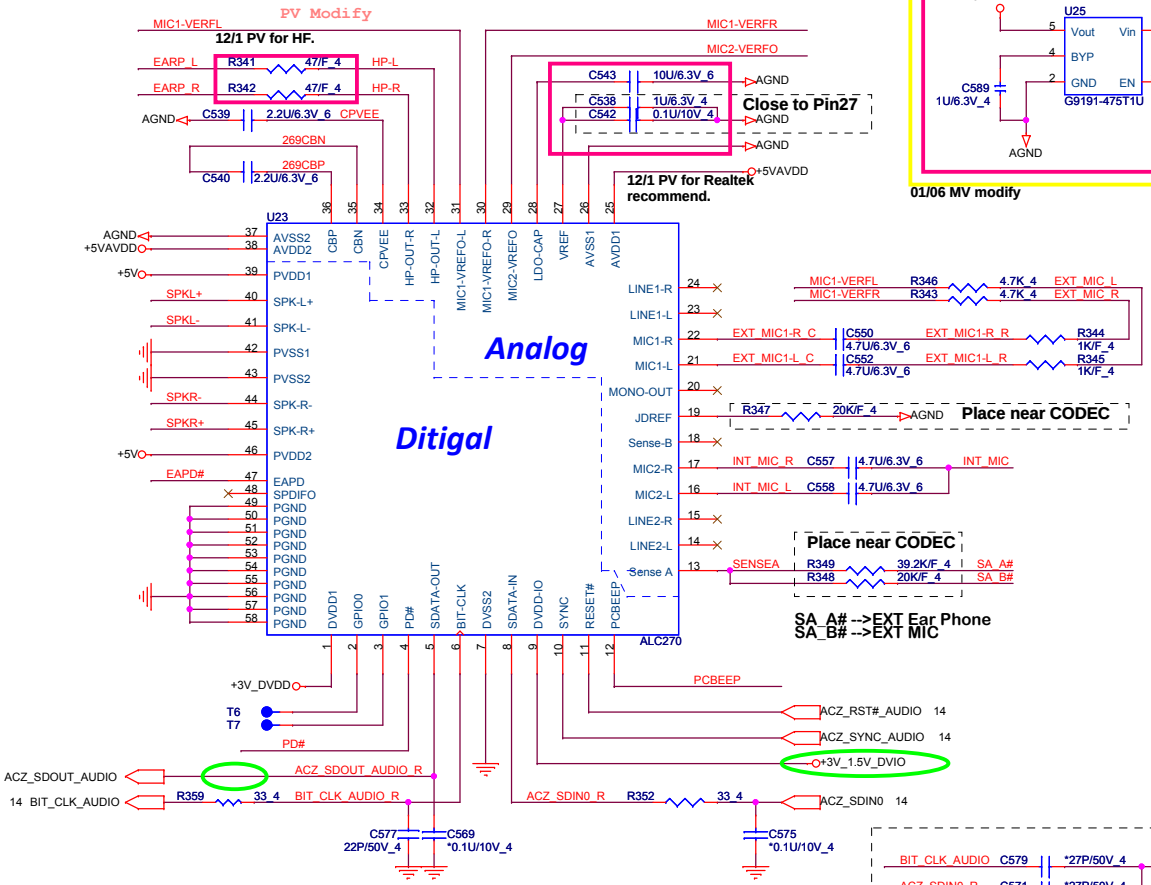


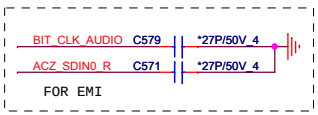


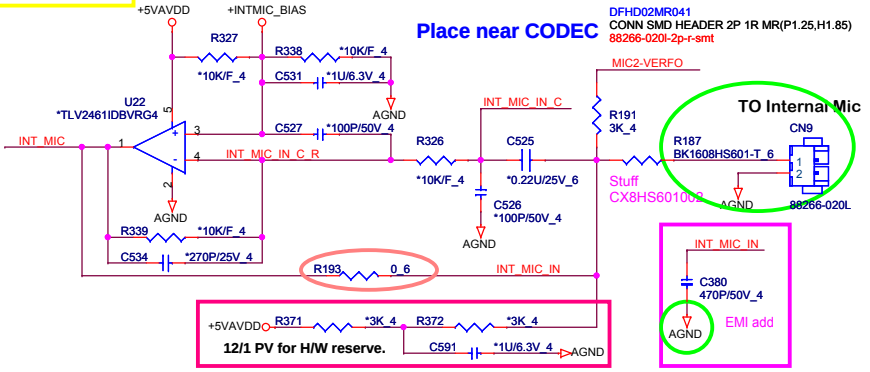


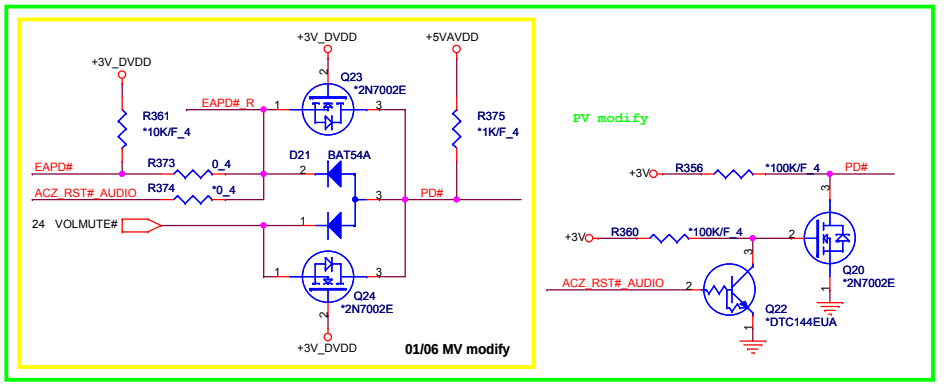


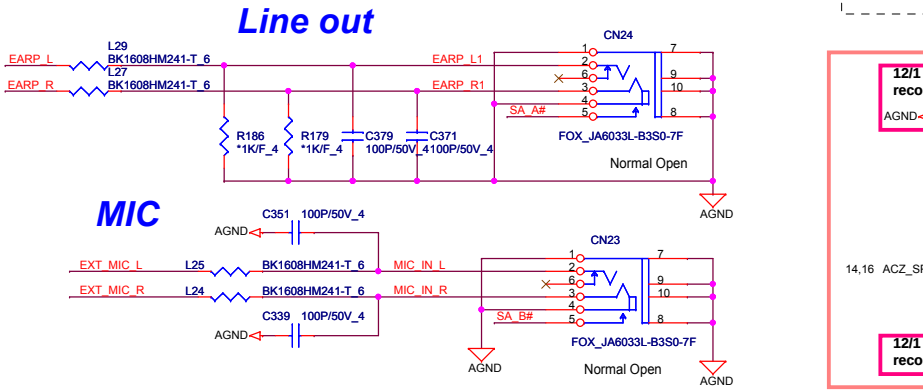


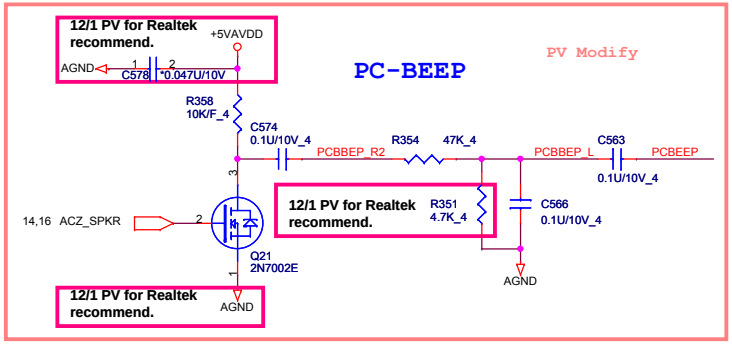


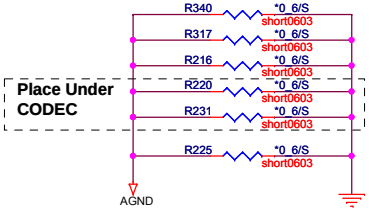










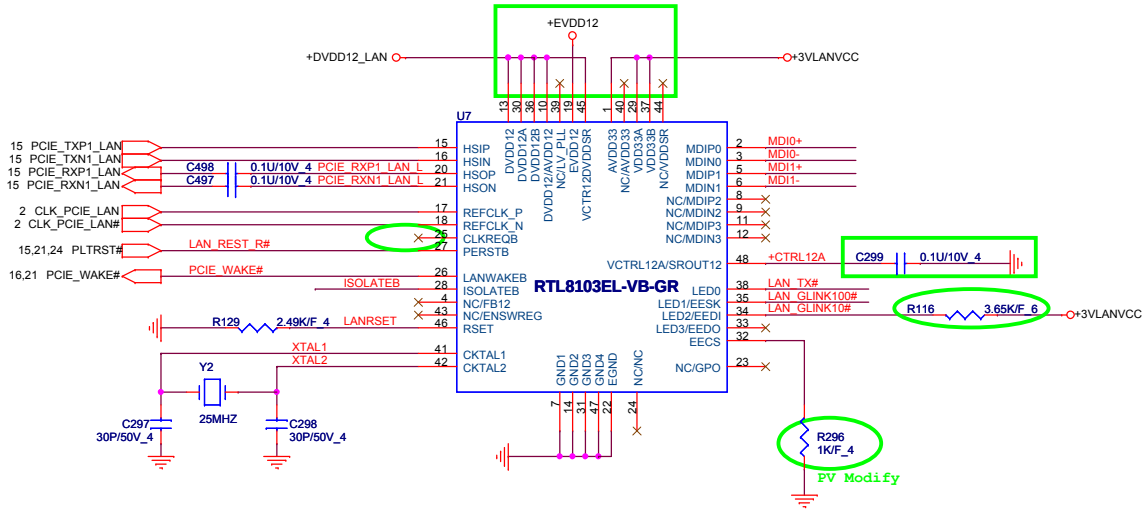


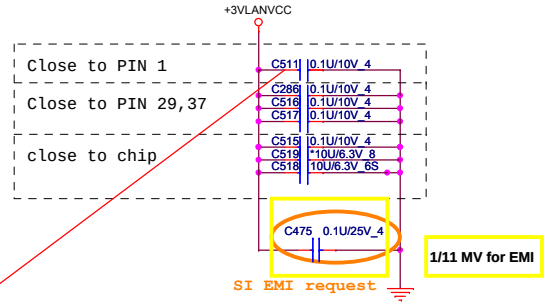
NB5

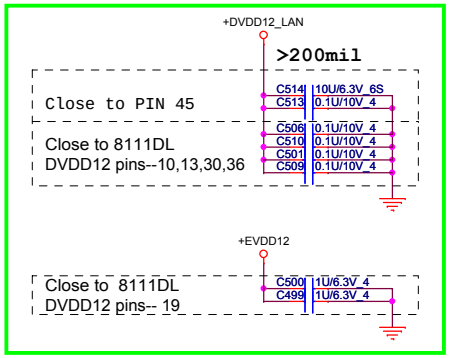
PROJECT :AX3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia ALC270/Audio Jack	1A

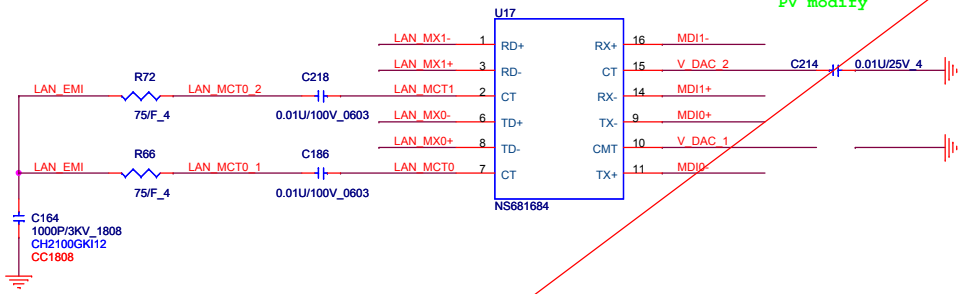
Date: Thursday, January 07, 2010 | Sheet 19 of 30

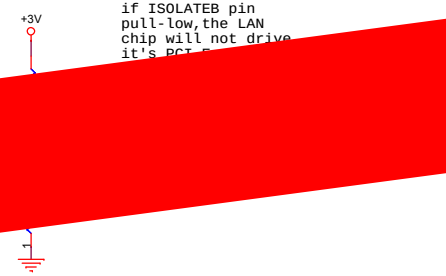




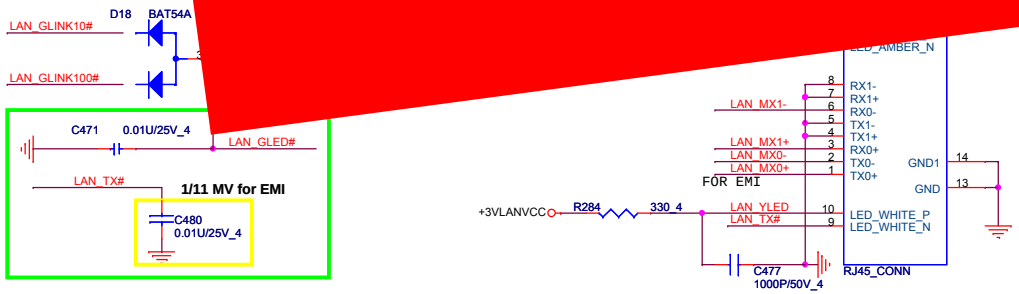


Transformer for 10/100





Lan Con.



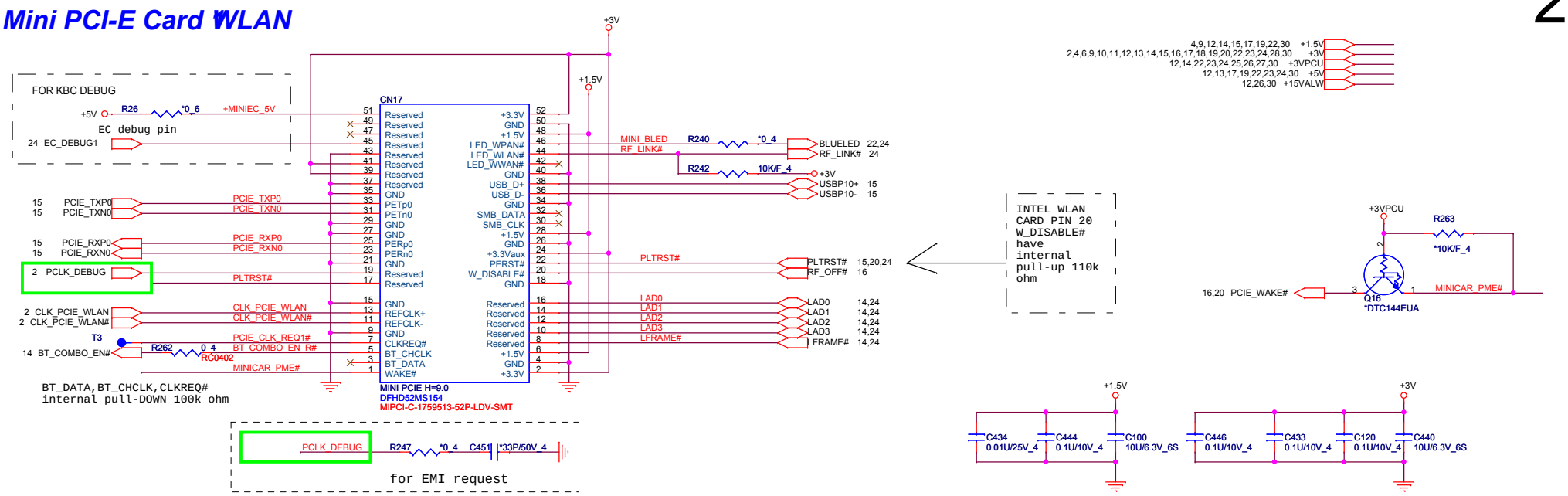
PROJECT :AX3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL8103EL/RJ45	2A

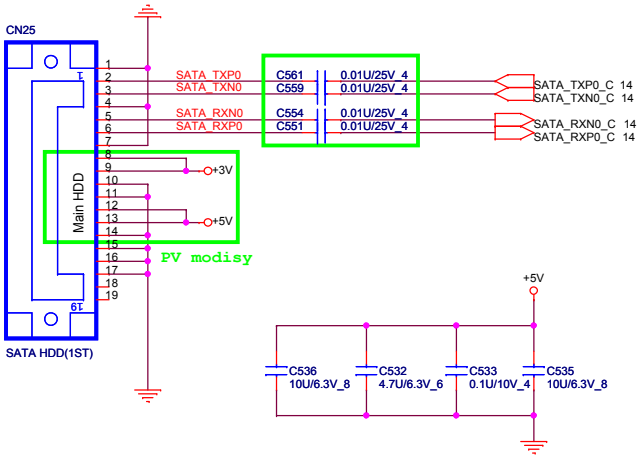
NB5

Date: Monday, January 11, 2010 | Sheet 20 of 30

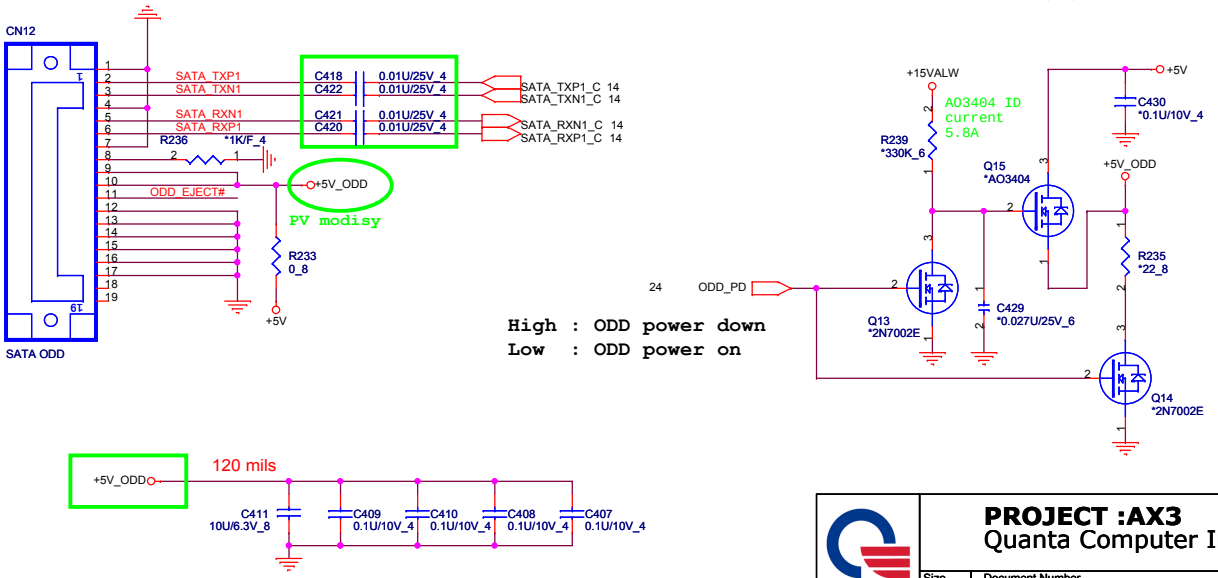
Mini PCI-E Card WLAN



SATA HDD CONNECTOR

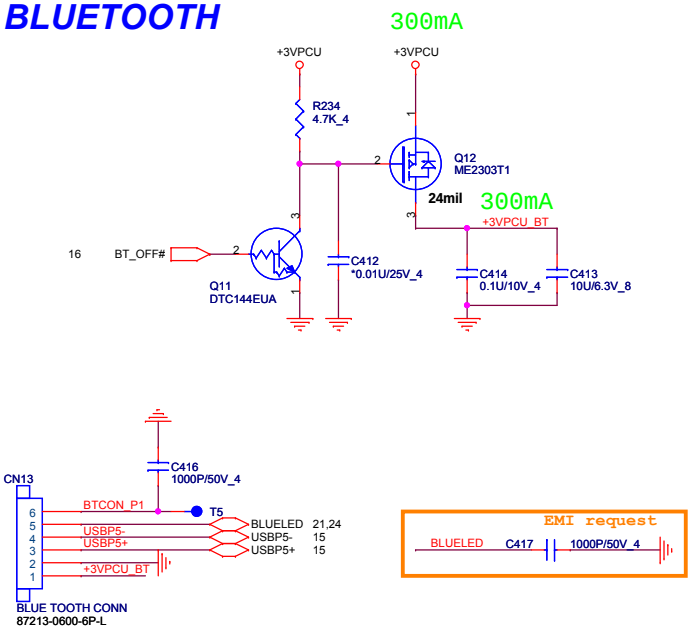


SATA ODD CONNECTOR

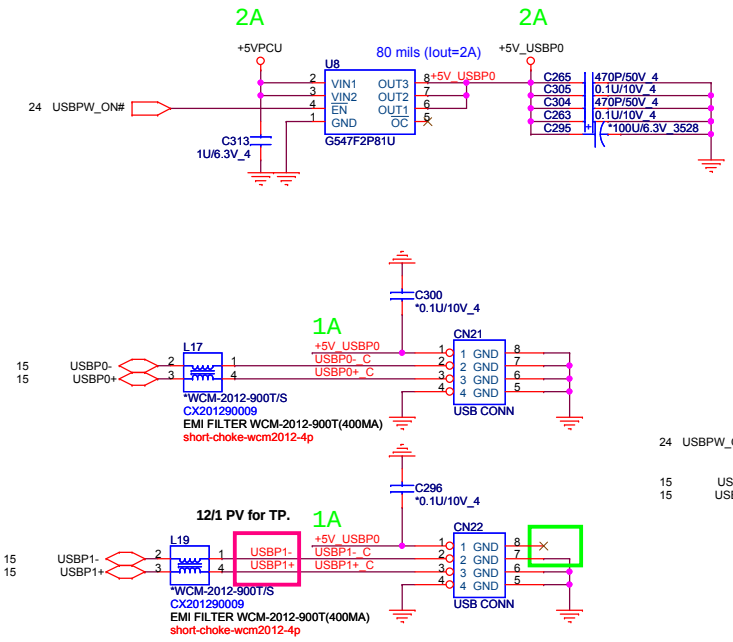


NB5	PROJECT :AX3 Quanta Computer Inc.		
	Size: Custom	Document Number: HDD/ODD/FAN	Rev: 2A
	Date: Thursday, January 07, 2010	Sheet 21 of 30	

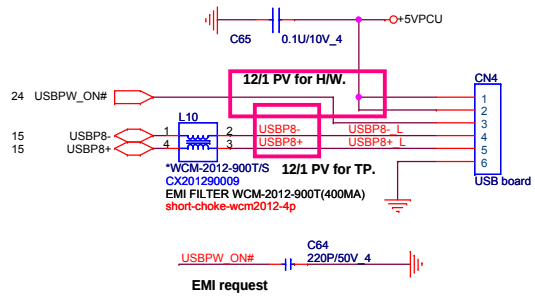
BLUETOOTH



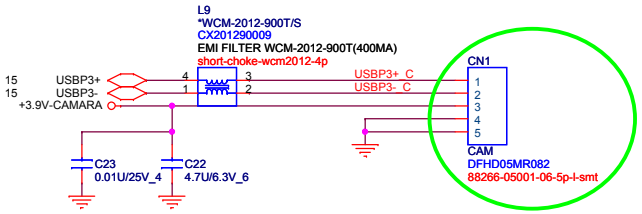
LEFT SIDE USBX1

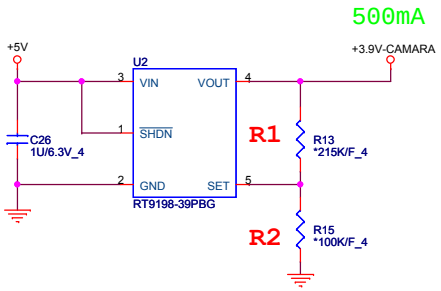


Right SIDE USBX1



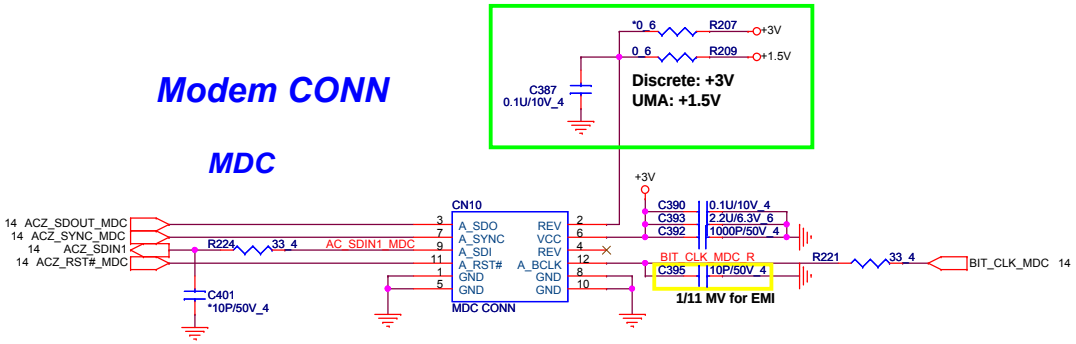
CAMERA

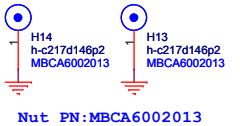




Modem CONN

MDC





4,9,12,14,15,17,19,21,30 +1.5V
2,4,6,9,10,11,12,13,14,15,16,17,18,19,20,21,23,24,28,30 +3V
12,14,21,23,24,25,26,27,30 +3VPCU
12,13,17,19,21,23,24,30 +5V
23,24,25,26,27,28,29,30 +5VPCU

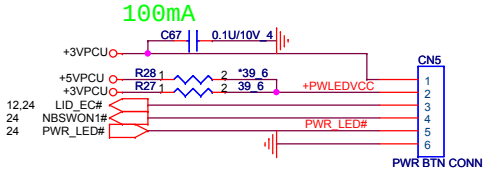
NB5

PROJECT :AX3
Quanta Computer Inc.

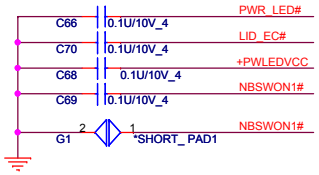
Size	Document Number	Rev
Custom	USB/BT/CAMERA/Modem	2A

Date: Monday, January 11, 2010 Sheet 22 of 30

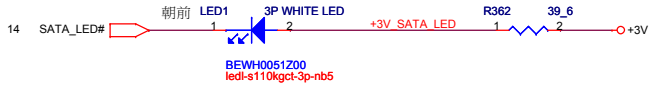
POWER BOTTON CONNECT



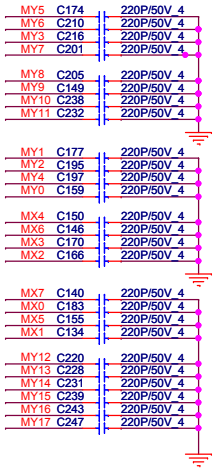
1. +3VPCU(LIDSWITCH PWR)
2. LEDVCC(+3VPCU)
3. LIDSWITCH
4. POWERON#
5. PWRLED#
6. GND

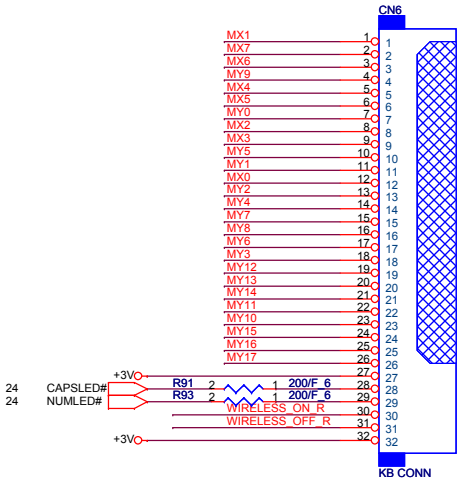


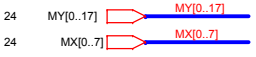
SATA LED



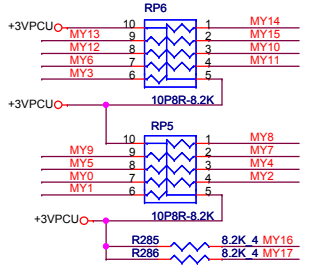
KEYBOARD Con.



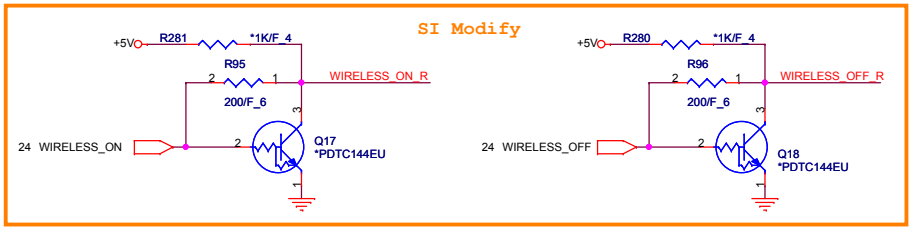




KEYBOARD PULL-UP

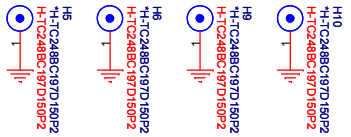


SI Modify



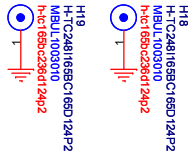
HOLE & PAD

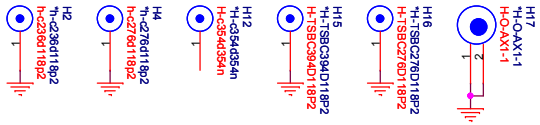
CPU

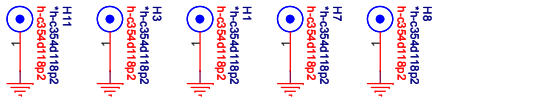


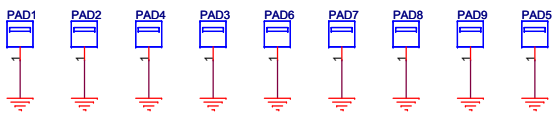
12/10 PV for DXF update.

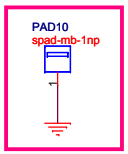
MCH



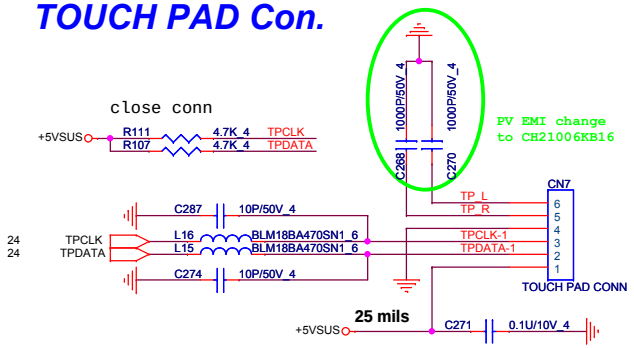




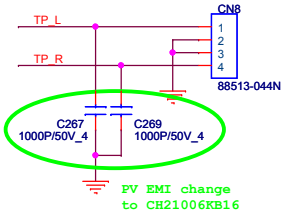




TOUCH PAD Con.



To TOUCH PAD SW board



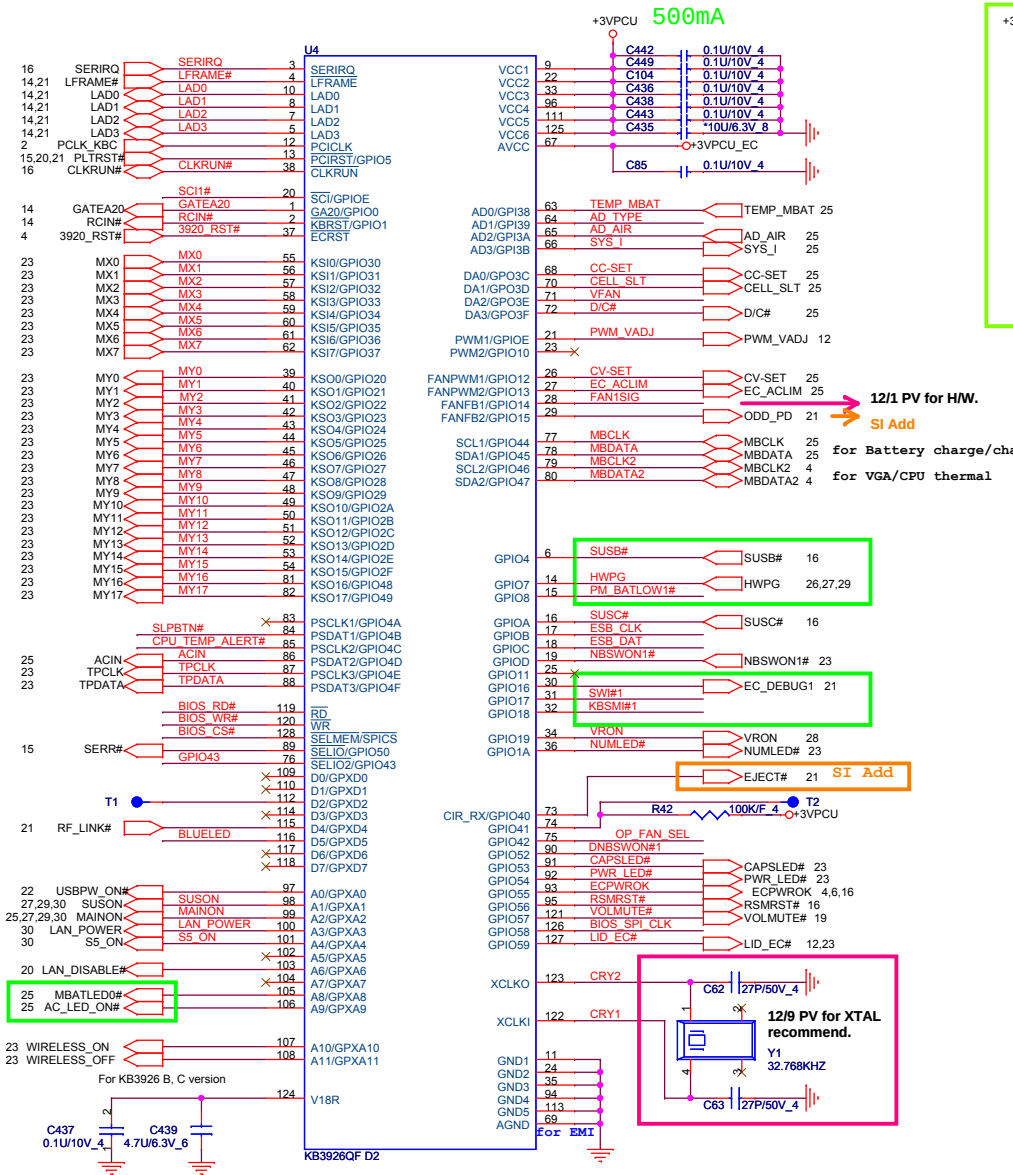
2,4,6,9,10,11,12,13,14,15,16,17,18,19,20,21,22,24,28,30 +3V
12,14,21,22,24,25,26,27,30 +3VPCU
12,13,17,19,21,22,24,30 +5V
12,30 +5VSUS
22,24,25,26,27,28,29,30 +5VPCU

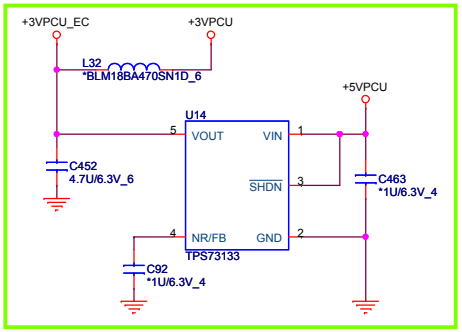
NB5

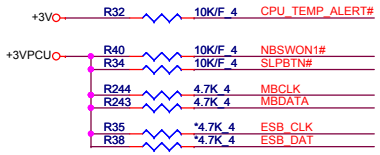
PROJECT :AX3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB/TP/SW/LED/Hole	2A

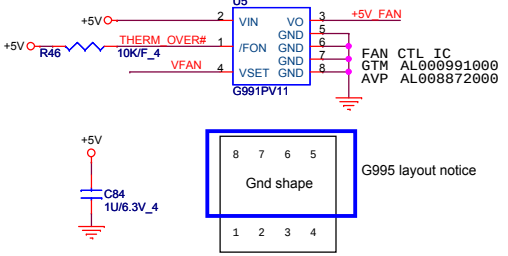
Date: Thursday, January 07, 2010 Sheet 23 of 30

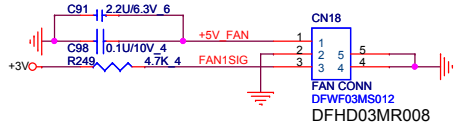






CPU FAN

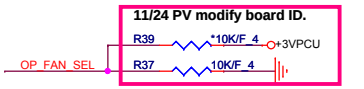




Adapter select for EC

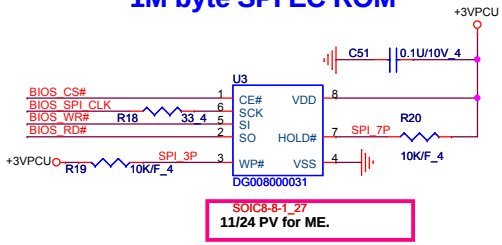
Hi ==> 120W
Low ==> 65W/90W

GPIO42 control fan table

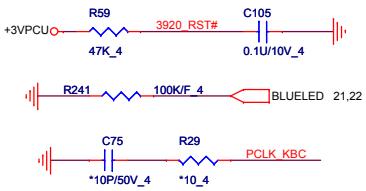


Project Model	GPIO42
AX 14"	High
AX 15.6"	Low
AX 17.3"	Middle (1.5V)

1M byte SPI EC ROM

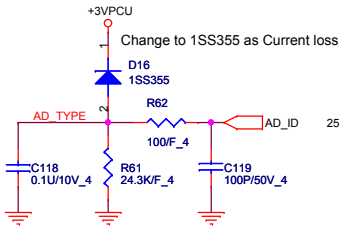


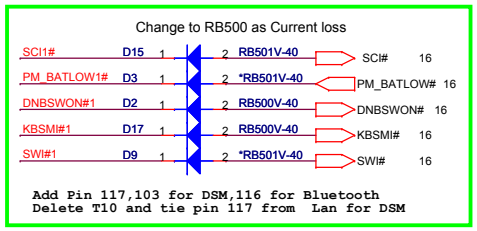
Socket: DG008000031
WINBOND AKE3GZN0N00
EON AKE3GZP0Q00
AIT AKE3GZP0801
MAX AKE5GFK0Z09



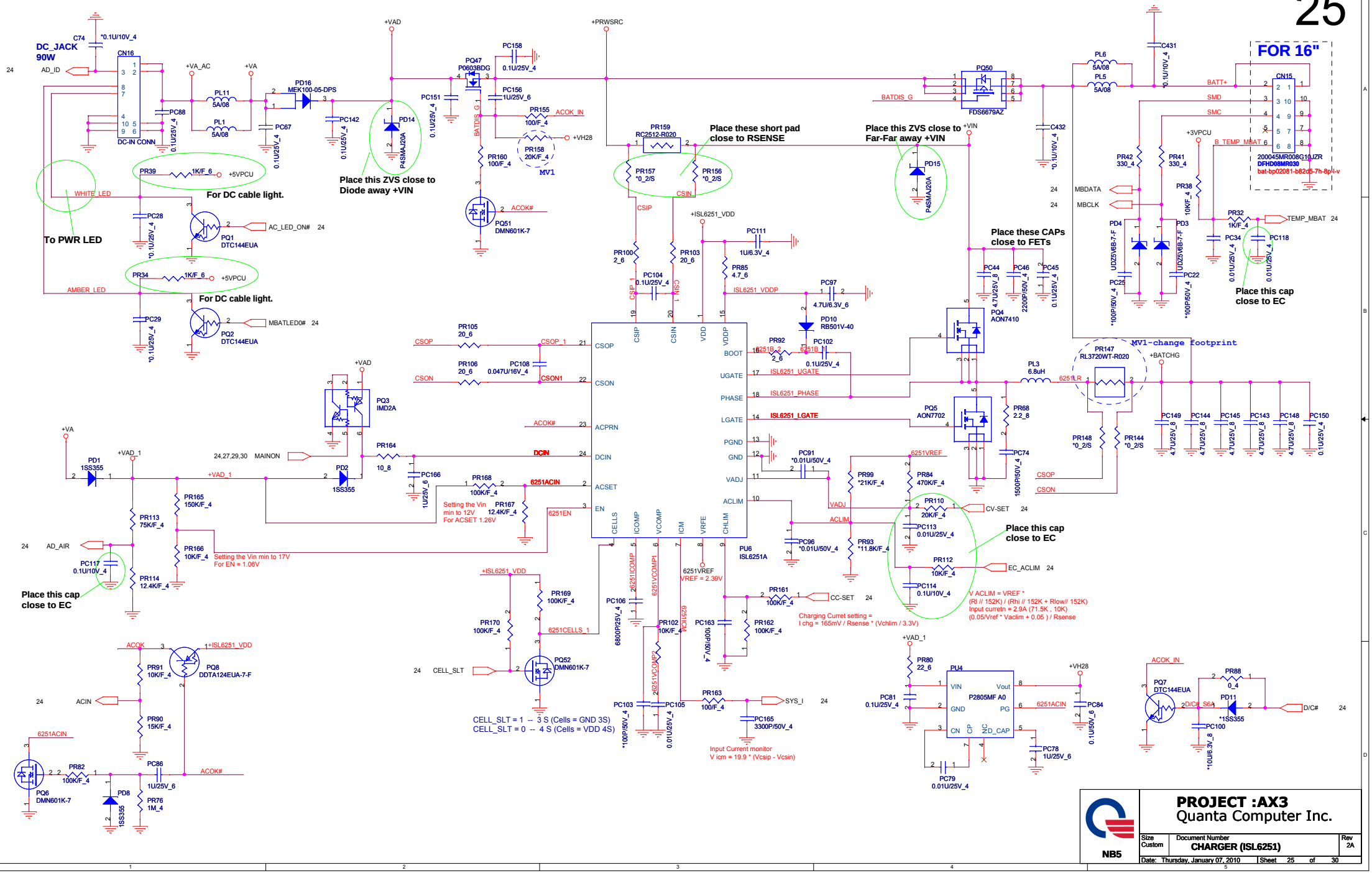
2,4,6,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23,28,30 +3V
12,14,21,22,23,25,26,27,30 +3VPCU
12,13,17,19,21,22,23,30 +5V
22,23,25,26,27,28,29,30 +5VPCU

adapter Type check





PROJECT : AX3			
Quanta Computer Inc.			
NB5	Size: Custom	Document Number: EC (KB3926)/ROM	Rev: 2A
	Date: Thursday, January 07, 2010	Sheet 24 of 30	


DC_JACK 90W
CN16
DC-IN CONN
AD_ID
+VA_AC
+VA
PD16 MEK100-05-DPS
PL11 5A/08
PL1 5A/08
PC88
PC67
+VAD
PD14 P4SMAJ20A
Place this ZVS close to Diode away +VIN
PC151
PQ47 P0603BDG
PC158 0.1U/25V_4
PC156 1U/25V_6
PR155 100/F_4
ACOK_IN
+VH28
PR158 20K/F_4 MV1
PR160 100/F_4
BATDIS_G
PQ51 DMN601K-7
ACOK#
+PRWSRC
PR159 RC2512-R020
Place these short pad close to RSENSE
PR157 *0_2/S
PR156 *0_2/S
CSIP
CSIN
PQ50 FDS6679AZ
Place this ZVS close to Far-Far away +VIN
PD15 P4SMAJ20A
+VIN
PL6 5A/08
PL5 5A/08
C431 *0.1U/10V_4
C432 *0.1U/10V_4
FOR 16"
CN15
BATT+
SMD
SMC
B_TEMP_MBAT
200045MR008G10JZR
DFHD08MR030
bat-bp02081-b82d5-7h-8p1-v
+3VPCU
PR42 330_4
PR41 330_4
PR38 10K/F_4
MBDATA
MBCLK
PD4 UDZSV6B-7-F
PD3 UDZSV6B-7-F
PR32 1K/F_4
TEMP_MBAT
PC34 0.01U/25V_4
PC118 0.01U/25V_4
Place this cap close to EC
PR39 1K/F_6
+5VPCU
For DC cable light.
WHITE_LED
To PWR LED
PC28 *0.1U/25V_4
PQ1 DTC144EUA
AC_LED_ON#
PR34 1K/F_6
AMBER_LED
PC29 *0.1U/25V_4
PQ2 DTC144EUA
MBATLED0#
Place these CAPs close to FETs
PC44 4.7U/25V_8
PC46 2200P/50V_4
PC45 0.1U/25V_4
PQ4 AON7410
PC25 *100P/50V_4
PC22 *100P/50V_4
PR105 20_6
PR106 20_6
PC108 0.047U/16V_4
CSOP
CSON
CSOP_1
CSON1
PQ3 IMD2A
PR164 10_8
PC166 1U/25V_6
ACOK#
DCIN
6251ACIN
6251EN
PR168 100K/F_4
PR167 12.4K/F_4
Setting the Vin min to 12V
For ACSET 1.26V
24,27,29,30 MAINON
+VA
+VAD_1
PD1 1SS355
PD2 1SS355
PR165 150K/F_4
PR113 75K/F_4
PR166 10K/F_4
Setting the Vin min to 17V
For EN = 1.06V
PR114 12.4K/F_4
AD_AIR
PC117 0.1U/10V_4
Place this cap close to EC
CSIP_1
CSIN_1
PC104 0.1U/25V_4
PR100 2_6
PR103 20_6
PR85 4.7_6
+ISL6251_VDD
PC111 1U/6.3V_4
ISL6251_VDDP
PC97 4.7U/6.3V_6
PD10 RB501V-40
PR92 2_6
PC102 0.1U/25V_4
ISL6251_UGATE
ISL6251_PHASE
ISL6251_LGATE
PL3 6.8uH
6251LR
PR147 RL3720WT-R020
MV1-change footprint
+BATCHG
PC149
PC144
PC145
PC143
PC148
PC150
PR148 *0_2/S
PR144 *0_2/S
PQ5 AON7702
PR68 2.2_8
PC74 1500P/50V_4
PC91 *0.01U/50V_4
PC96 *0.01U/50V_4
6251VREF
PR84 470K/F_4
PR99 *21K/F_4
PR93 *11.8K/F_4
VADJ
ACLIM
PR110 20K/F_4
PC113 0.01U/25V_4
PR112 10K/F_4
PC114 0.1U/10V_4
CV-SET
EC_ACLIM
Place this cap close to EC
V ACLIM = VREF * (RI // 152K) / (Rhi // 152K + Rlow// 152K)
Input curretn = 2.9A (71.5K , 10K)
(0.05/Vref * Vaclim + 0.05) / Rsense
PR161 100K/F_4
CC-SET
Charging Curret setting = I chg = 165mV / Rsense * (Vchlim / 3.3V)
PU6 ISL6251A
CELLS
ICOMP
VCOMP
ICM
VRFE
CHLIM
6251VREF
VREF = 2.39V
6251ICOMP
6251VCOMP1
6251VCOMP2
PC106 6800P/25V_4
PR102 10K/F_4
PC163 100P/50V_4
PR162 100K/F_4
PC103 *100P/50V_4
PC105 0.01U/25V_4
PR163 100/F_4
SYS_I
PC165 3300P/50V_4
Input Current monitor
V icm = 19.9 * (Vcsip - Vcsin)
+ISL6251_VDD
PR169 100K/F_4
PR170 100K/F_4
6251CELLS_1
CELL_SLT
PQ52 DMN601K-7
CELL_SLT = 1 -- 3 S (Cells = GND 3S)
CELL_SLT = 0 -- 4 S (Cells = VDD 4S)
ACOK
PR91 10K/F_4
PQ8 DDTA124EUA-7-F
ACIN
PR90 15K/F_4
6251ACIN
PQ6 DMN601K-7
PR82 100K/F_4
PC86 1U/25V_6
PD8 1SS355
PR76 1M_4
+VAD_1
PR80 22_6
PU4 P2805MF A0
VIN
Vout
GND
PG
CN
CP
NCD_CAP
PC81 0.1U/25V_4
PC84 0.1U/50V_6
PC78 1U/25V_6
PC79 0.01U/25V_4
+VH28
ACOK_IN
PR88 0_4
PQ7 DTC144EUA
D/C#
PD11 *1SS355
PC100
*10U/6.3V_8
PROJECT :AX3
Quanta Computer Inc.
NB5
Size Custom
Document Number CHARGER (ISL6251)
Rev 2A
Date: Thursday, January 07, 2010
Sheet 25 of 30

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

+5V +/- 5%
Countinue current:6A
Peak current :8A
OCP minimum :10A

+3.3V +/- 5%
Countinue current:5A
Peak current:6A
OCP minimum 7.5A

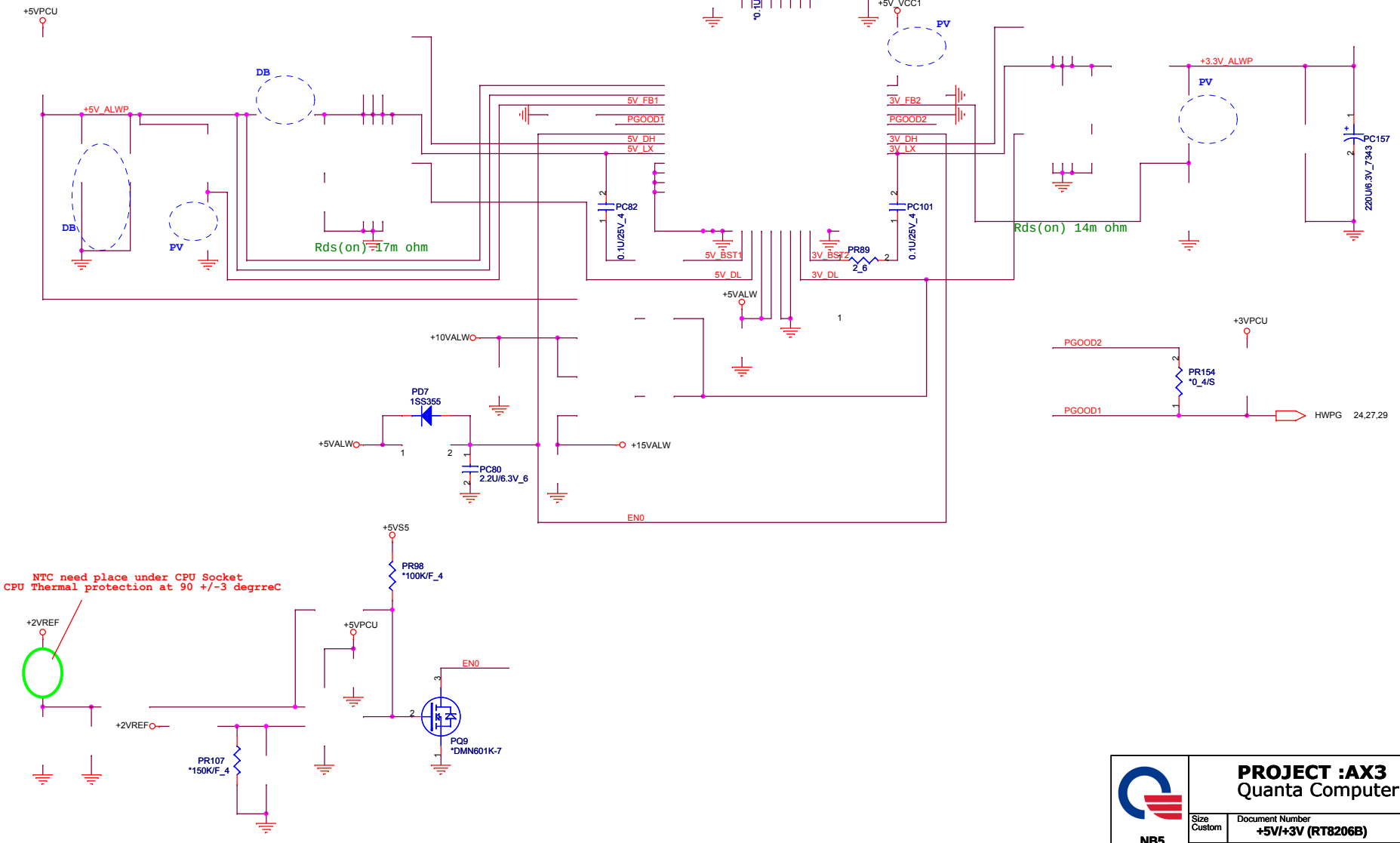
Place these CAPs close to FETs

Place these CAPs close to FETs

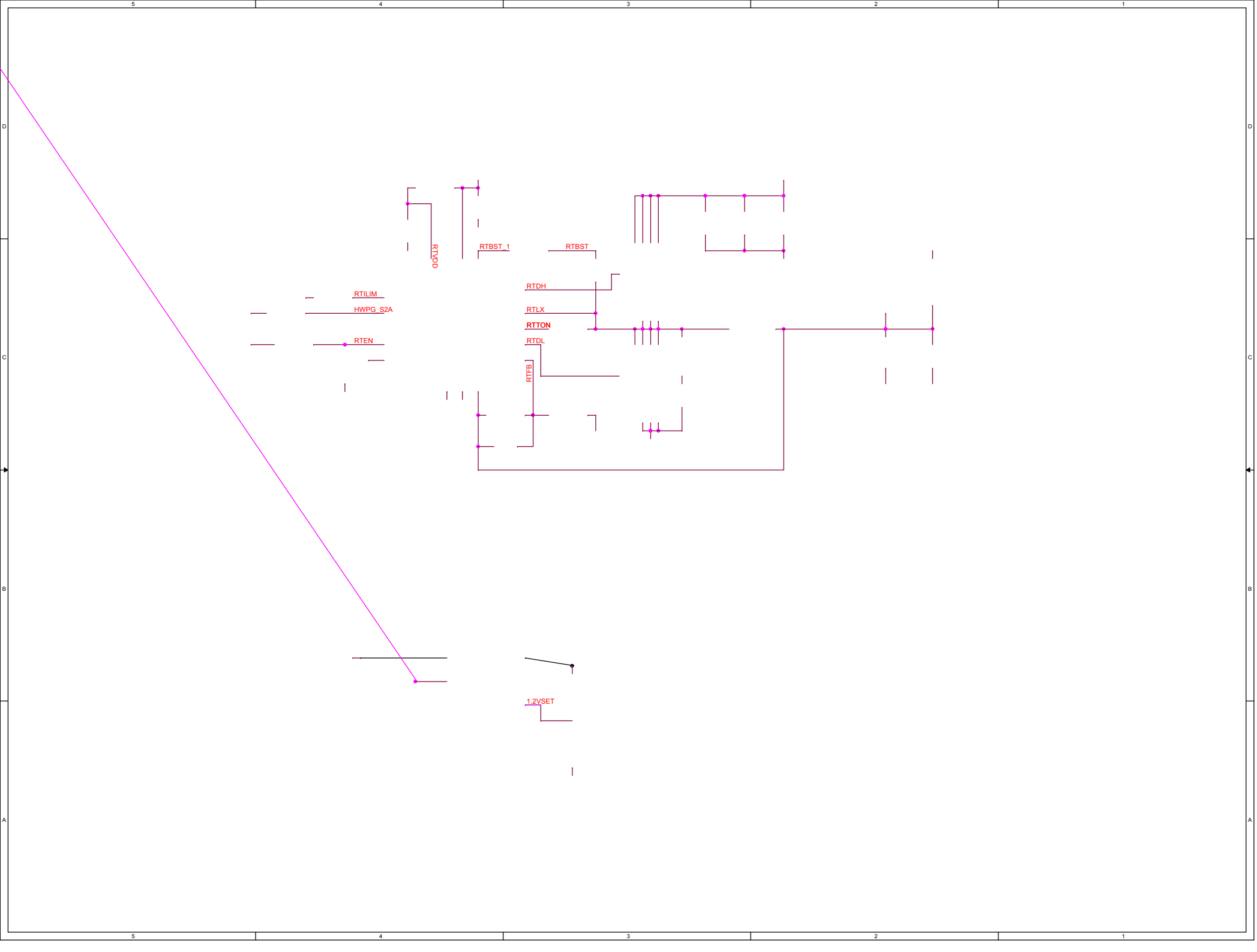
Rds(on) 17m ohm

Rds(on) 14m ohm

NTC need place under CPU Socket
CPU Thermal protection at 90 +/-3 degrreC



NB5	PROJECT :AX3 Quanta Computer Inc.	
Size: Custom	Document Number: +5V/+3V (RT8206B)	Rev: 2A
Date: Thursday, January 07, 2010	Sheet 26 of 30	


RTVDD
RTBST_1
RTBST
RTDH
RTILIM
HWPG_S2A
RTLX
RTTON
RTEN
RTDL
RTFB
1.2VSET

Merom: VCC_CORE/ 44A
Yonah: VCC_CORE/ 36A

+1.05V
PR1 *0_4 CPU_VID6
PR2 *0_4 CPU_VID5
PR3 *0_4 CPU_VID4
PR4 *0_4 CPU_VID3
PR5 *0_4 CPU_VID2
PR6 *0_4 CPU_VID1
PR7 *0_4 CPU_VID0
DELAY_VR_PWRGOOD 6,16

PWR_MON
PR15 4.99K/F_4 PGD_IN
PC1 0.1U/10V_4
for ISL6262A

3 PM_PSI# PSI#

+5VPCU
PR49 10_6
PC55 0.1U/25V_4
PR62 *0_6/S
PC50 1U/6.3V_4

+VIN
PR61 1/F_6
PR10 10_4
PC2 0.1U/10V_4
+3V
PR9 1.91K/F_4

PR123 Close to Phase 1 Inductor
Throttling temp.
105 degree C

+3VSUS
PR8 *68_4
3 H_PROCHOT#
PR150 *470K_4 NTC
PR23 *4.02K/F_4
ED8-B -0623-add
PC12 *0.01U/25V_4
Panasonic
ERT-J0EV474J

PSI# PR16 *0_4/S PSI#_1
PR22 147K/F_4 PGD_IN
PC21 0.015U/16V_4

PU1 ISL6262A

22	VCC		
20	VIN		
48	3V3		
1	PGOOD		
21	GND		
49	GND_T		
2	PSI#		
3	PGD_IN		
4	RBIAS		
5	VR_TT#		
6	NTC		
7	SOFT		
37	VID0	CPU_VID0	4
38	VID1	CPU_VID1	4
39	VID2	CPU_VID2	4
40	VID3	CPU_VID3	4
41	VID4	CPU_VID4	4
42	VID5	CPU_VID5	4
43	VID6	CPU_VID6	4
44	VR_ON	VR_ON	
45	DPRSLPVR	DPRSLPVR_R	6,16
46	DPRSTP#	H_DPRSTP#_R	3,6,14
47	CLK_EN#	CLKEN#	16 VR_PWRGD_CK410#
13	VDIFF		
12	FB2		
11	FB		
10	COMP		
9	VW		
15	RTN		
14	VSEN		
16	DROOP		
17	DFB		
35	UGATE1		
36	BOOT1		
34	PHASE1		
32	LGATE1		
33	PGND1		
24	ISEN1		
31	PVCC		
27	UGATE2		
26	BOOT2		
28	PHASE2		
30	LGATE2		
29	PGND2		
23	ISEN2		
25	NC		
8	OCSET		
19	VSUM		
18	VO		

VRON
PR14 *0_4/S VR_ON
PR12 100K/F_4
PR83 499/F_4 DPRSLPVR_R
PR11 *0_4/S H_DPRSTP#_R
PR13 *0_4/S CLKEN#

PR46 1K/F_4
PR48 255/F_4
PC57 1000P/50V_4
PR54 1K/F_4
PR45 97.6K/F_4
PC39 470P/50V_4
PC35 150P/50V_4
PR36 6.81K/F_4
PC30 1000P/50V_4

PR30 12.7K/F_4
PC58 0.1U/25V_4
PR56 11K/F_4
PR65 2.7K/F_4
PC51 0.22U/6.3V_4
PR145 10K_6 NTC
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
PR53 1K/F_4
PC66 0.33U/6.3V_4
PC52 0.01U/25V_4
PR52 3.16K/F_4 1%
PC53 180P/50V_4
ISL6262_VO
PC60 0.01U/25V_4
PC59 0.01U/25V_4

Parallel
PR63 0_4 VCCSENSE 4
PR64 0_4 VSSSENSE 4

PC31 4.7U/25V_8
PC23 4.7U/25V_8
PC42 *4.7U/25V_8
PC9 2200P/50V_4
PC11 0.1U/25V_4
PC162 100U/25V_L-F
PC161 100U/25V_L-F

PQ37 RJK03B9D
6262_UG1
6262_PH1
6262_LG1
PQ42 RJK03D3D
PR146 2.2_8
PC146 2200P/50V_4

+VCORE
PL10 0.36uH
PC168 330u_2.5V_7343
PC167 330u_2.5V_7343
PC75 0.1U/10V_4
PR72 *0_6/S
PR71 *0_6/S

PR74 3.65K/F_4
PR58 10K/F_4
PR59 1/F_6
PR55 10K/F_4
ISEN2
PC49 0.22U/6.3V_4
PC19 4.7U/6.3V_6
+5VPCU
PC26 4.7U/25V_8
PC43 4.7U/25V_8
PC38 4.7U/25V_8
PC16 2200P/50V_4
PC14 0.1U/25V_4

PQ38 RJK03B9D
6262_UG2
PR40 2_6
PC33 0.22U/25V_6
6262_PH2
6262_LG2
PQ41 RJK03D3D
PR67 2.2_8
PC77 2200P/50V_4
PC56 0.22U/6.3V_4

PL9 0.36uH
PC72 330u_2.5V_7343
PC73 330u_2.5V_7343
PC76 0.1U/10V_4
PR69 *0_6/S
PR70 *0_6/S
Parallel

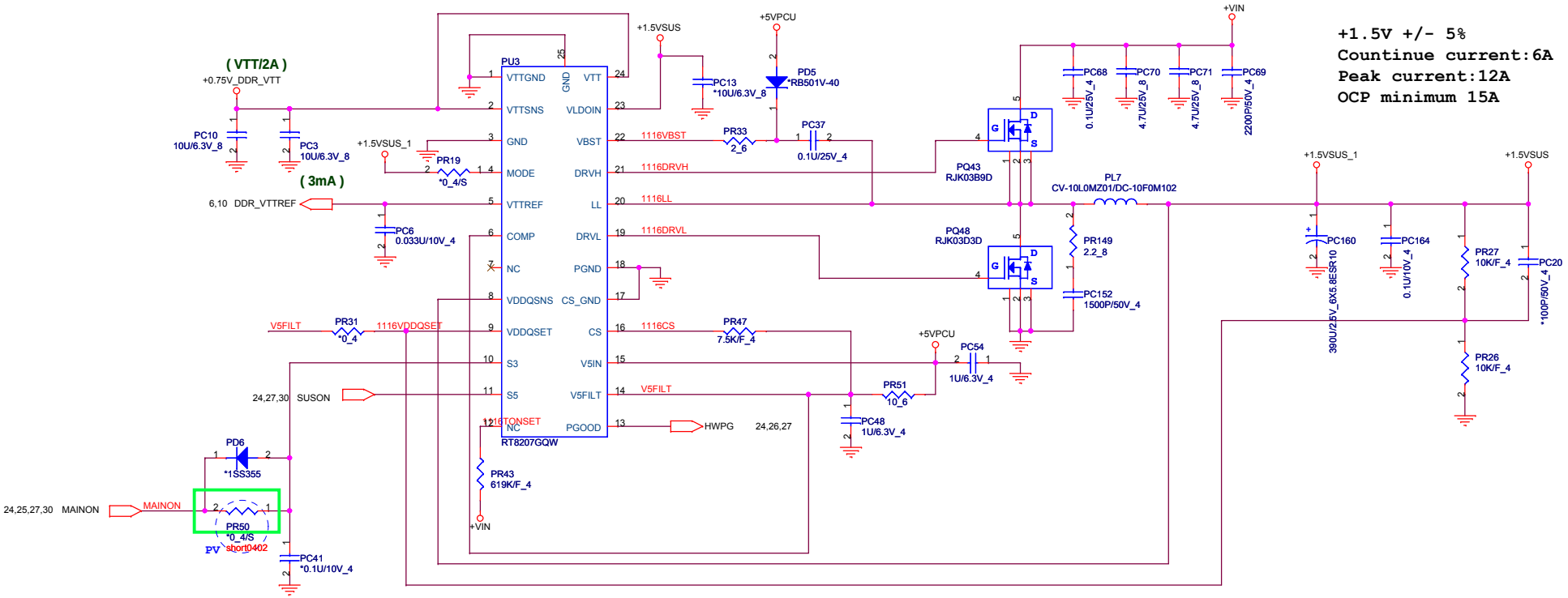
PR73 3.65K/F_4
PR66 10K/F_4
PR60 1/F_6
PR57 10K/F_4

PR17 2_6
PC5 0.22U/25V_6

NB5

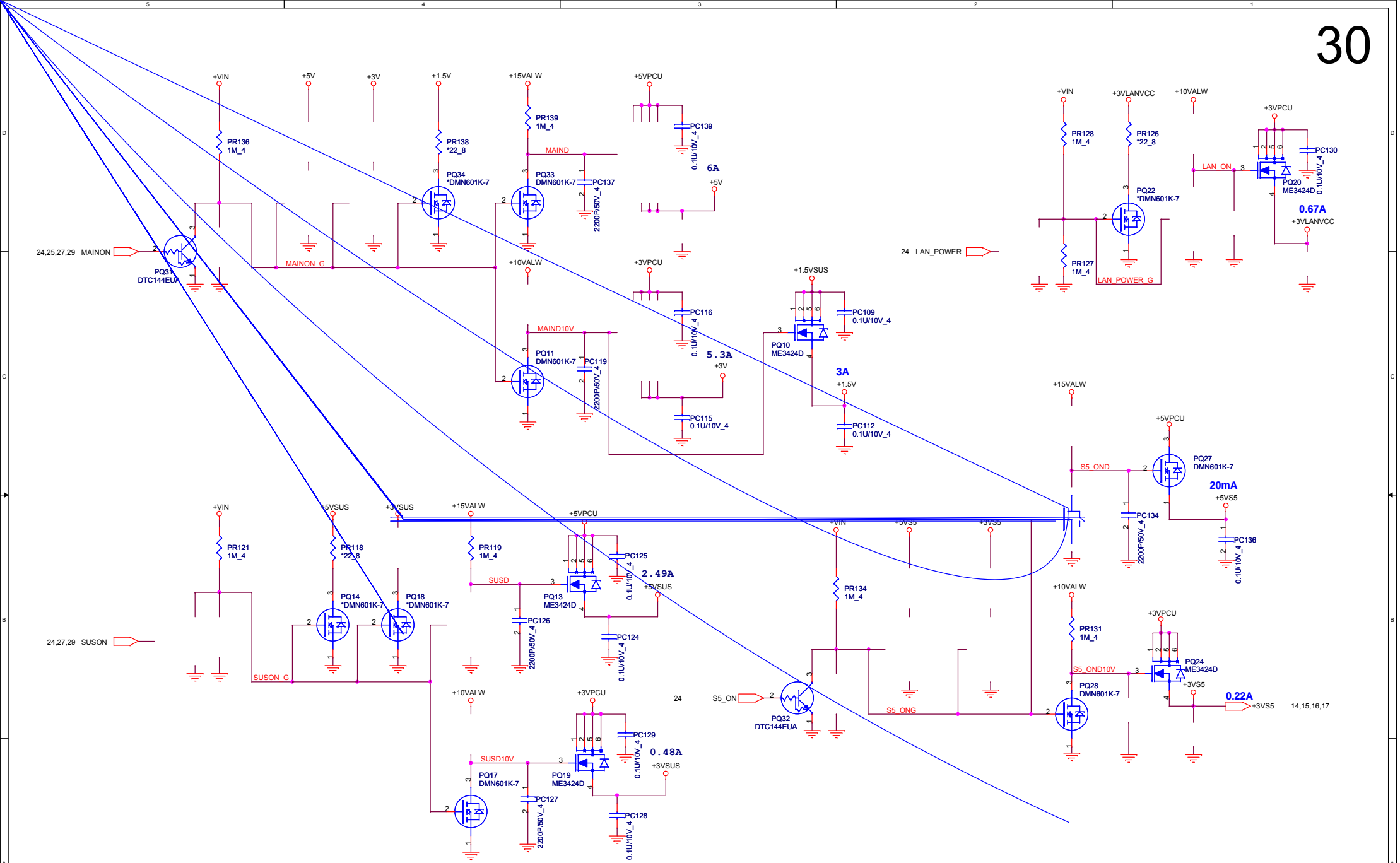
PROJECT :AX3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core (ISL6266A)	2A
Date: Thursday, January 07, 2010	Sheet 28 of 30	



+1.5V +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

NB5	PROJECT :AX3 Quanta Computer Inc.	
	Size: Custom Document Number: DDR3 (RT8207)	Rev: 2A
	Date: Thursday, January 07, 2010 | Sheet 29 of 30	



PROJECT :AX3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE/3VS5/5VS5/LAN	2A

NB5

Date: Thursday, January 07, 2010 | Sheet 30 of 30