Project
Code:NVX00
MB Serial Number:
LA-6111P
BOM:
46184736L01/L02
PCB
PN:DAA00001R00

NVX00----LA-6111P

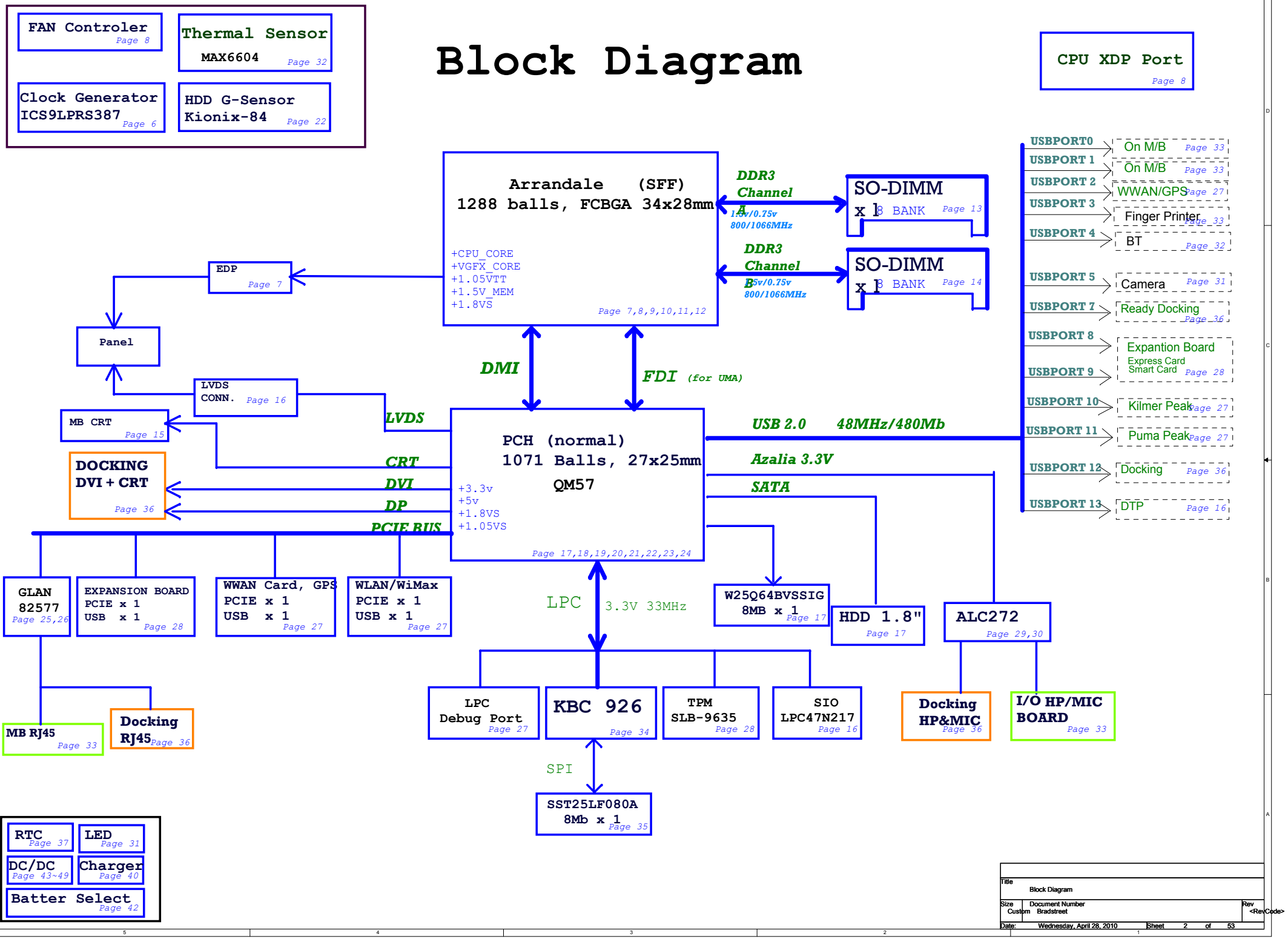
Callepla Platform, DDR3
BGA Arrandale+PCH

2010-04-28

REV: 1.0

Title: Cover Sheet			
Size: Custom	Document Number: Bradstreet1.5		Rev: 0.3
Date: Wednesday, April 28, 2010	Sheet 1 of 53		

Block Diagram



Title	Block Diagram		
Size: Custom	Document Number: Bradstreet		Rev: <RevCode>
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Voltage Rails

O MEANS ON X MEANS OFF

power plane / State	B+	+5VALW +3VALW +3V_LAN [1]	+1.5V_MEM V_DDR_REF	+5VS +3VS +1.8VS +1.5VS +0.75VTT +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4 AC Pluged	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC+Battery removed	X	X	X	X

NOTE:
1. S3 state, if without AC ON, +3V_LAN will be switched off.

SMBUS Control Table

	SOURCE	CLK GEN	PCH	Expansion Board	SODIMM A & B	G-SENSOR	WLAN/WWAN EXPRESS CARD	Giga Lan	THERMAL SENSOR PCH, Arrandale SO-DIMM A&B	THERMAL SENSOR Charger	BATT-1	BATT-2	XDP	Light sensor (LS4653)
SMB_EC_CK1_3A SMB_EC_DA1_3A	KB926	X	X	X	X	Y	X	X	X	X	Y	X	X	Y
SMB_EC_CK2_3A SMB_EC_DA2_3A	KB926	X	Y	X	X	X	X	X	Y	Y	X	Y	X	X
PCH_SMBCLK PCH_SMBDATA	PCH	Y	X	Y	Y	X	Y	X	X	X	X	X	Y	X
LAN_SMBCLK LAN_SMBDATA	PCH	X	X	X	X	X	X	Y	X	X	X	X	X	X

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
CLK GEN	D2	1101 0010
SODIMM A	C0	1100 0000
SODIMM B	C4	1100 0100
G-SENSOR	30	0011 0000
THERMAL SENSOR (PCH)	30	0011 0000
THERMAL SENSOR (Charger)	30	0011 0000
THERMAL SENSOR (Arrandale)	32	0011 0010
THERMAL SENSOR (So-DIMMs)	34	0011 0100
THERMAL SENSOR (Battery-1)	30	0011 0000
THERMAL SENSOR (Battery-2)	TBD	TBD
WLAN	TBD	TBD
WWAN	TBD	TBD
Expansion Board	TBD	TBD
XDP	TBD	TBD
Light sensor	72	0111 0010

Symbol Note :

: means Digital Ground

: means Analog Ground

@ : means just reserve , no build

Debug@ : for LPC debug card, 80 port.

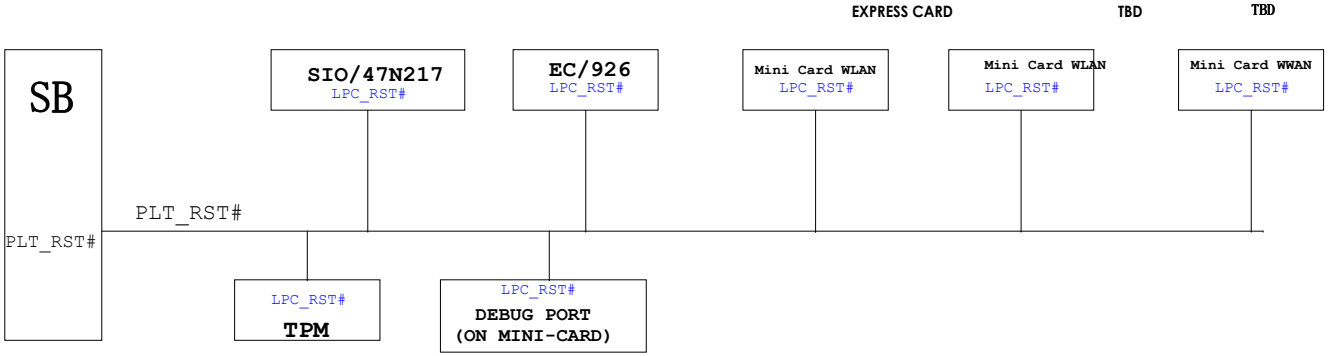
XDP@ : Reserve for CPU XTP debug.

MP@ : Should been staffed while in MP phase.

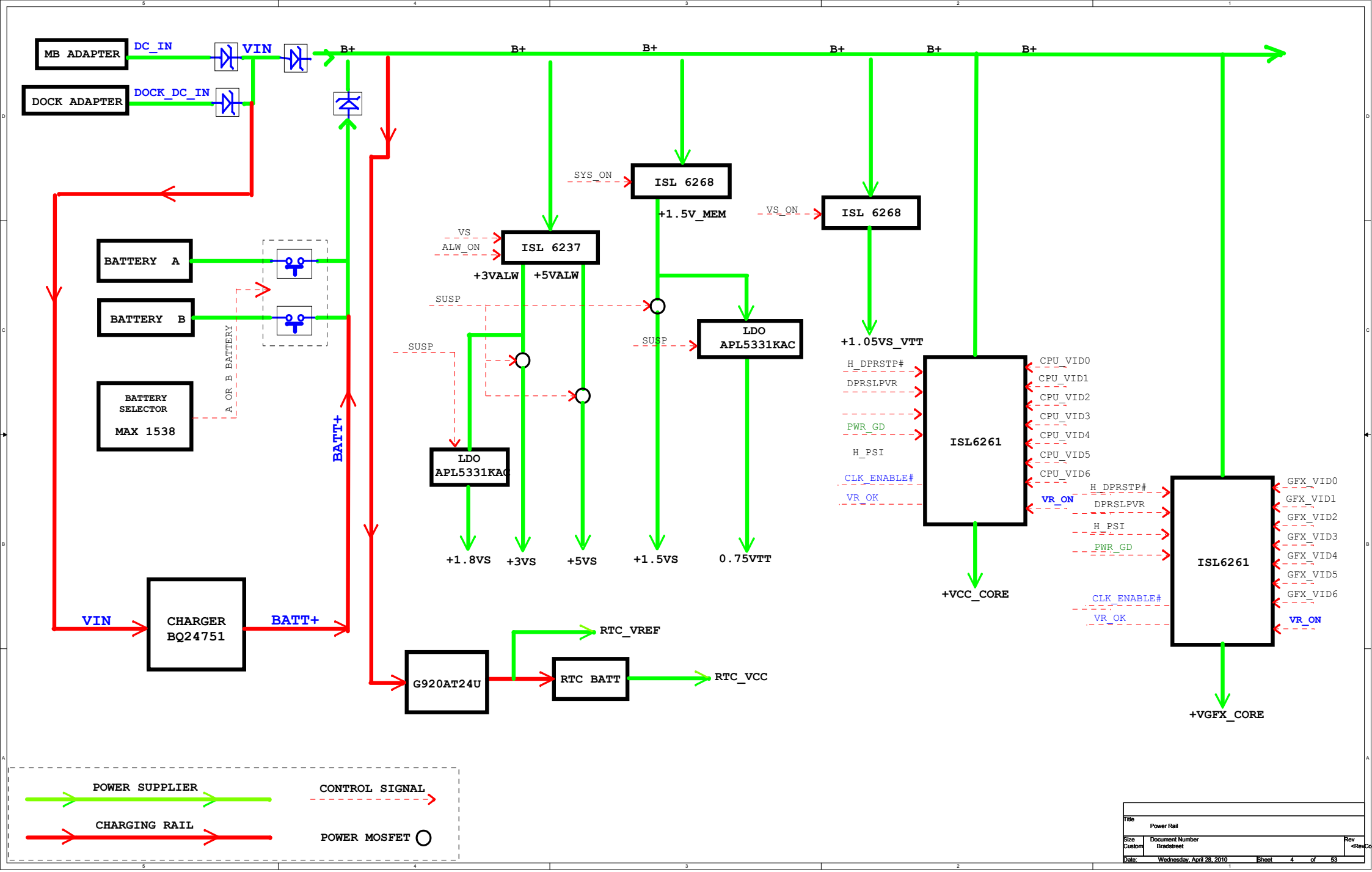
PCB 0D1 LA-6111P REV0 M/B
PCB

LPC BUS ADDRESSING/TOPOLOGY

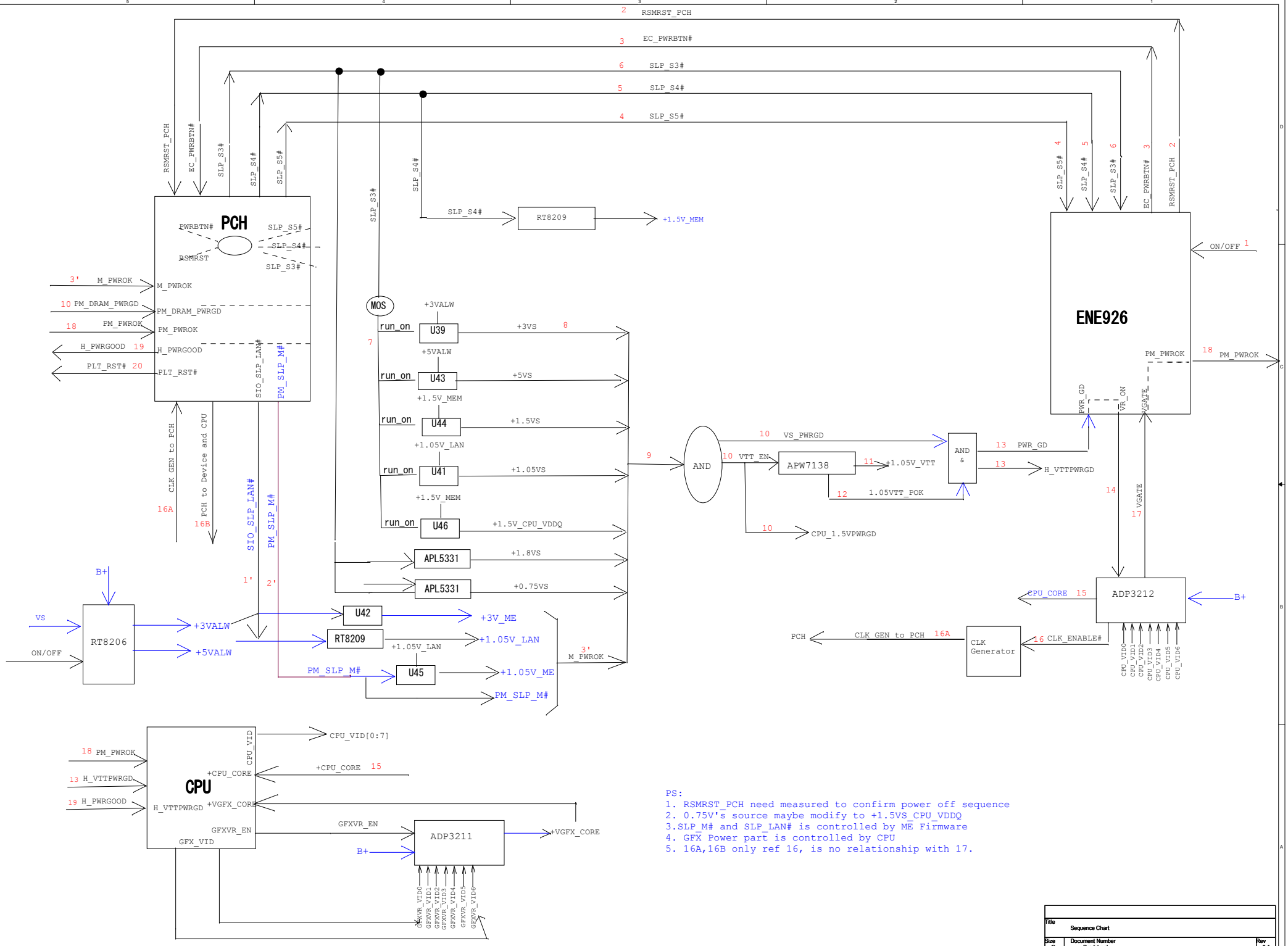
DEVICE	HEX	ADDRESS
SIO LPC47N217	2EH	0010 1110
TPM SLB9635TT1.2	4EH	0100 1110
Mini debug port	80	1000 0000



Title	Schematic Infomation		
Size: Custom	Document Number: Bradstreet		Rev: 0.01
Date: Wednesday, April 28, 2010	Sheet 3	of 53	



Title	Power Rail	
Size: Custom	Document Number: Bradstreet	Rev: <RevCo
Date: Wednesday, April 28, 2010	Sheet 4 of 53	



PS:
1. RSMRST_PCH need measured to confirm power off sequence
2. 0.75V's source maybe modify to +1.5VS_CPU_VDDQ
3.SLP_M# and SLP_LAN# is controlled by ME Firmware
4. GFX Power part is controlled by CPU
5. 16A,16B only ref 16, is no relationship with 17.

Title	Sequence Chart	
Size C	Document Number Bradstreet	Rev 0.1
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Update Footprint to R0805 because of DFX issue.
02/01/2010 Joyce

+1.05VS
L1 FBMA-L11-201209-221LMA30T_0805
C1 10U_0805_10V4Z
+CLK_VDDSRC
C2 10U_0805_10V4Z
C3
C4 0.1U_0402_16V4Z
0.1U_0402_16V4Z

+3VS
L2 FBMA-L11-201209-221LMA30T_0805
C5 10U_0805_10V4Z
+CLK_VDD
C6 10U_0805_10V4Z
C7 0.1U_0402_16V4Z
C8
C9 0.1U_0402_16V4Z
C10
C11 0.1U_0402_16V4Z

Clock Generator

Integrated 33ohm Resistor

18 CLK_BUF_DREF_96M
18 CLK_BUF_DREF_96M#
RP1 0_0404_4P2R_5%
PAD T23
18 CLK_BUF_PCIE_SATA
18 CLK_BUF_PCIE_SATA#
RP2 0_0404_4P2R_5%
18 CLK_BUF_CPU_DMI
18 CLK_BUF_CPU_DMI#
RP4 0_0404_4P2R_5%
H_STP_CPU#

Integrated 33ohm Resistor

U1
ICS9LRS3199AKLFT_MLF32_5X5
IDT SA000030P00

VDD_USB_48
VSS_48M
DOT_96
DOT_96#
VDD_27
27MHZ
27MHZ_SS
USB_48
VSS_27M
SATA
SATA#
VSS_SRC
SRC_1
SRC_1#
VDD_SRC_IO
CPU_STOP#
TGND
SCL
SDA
REF_0/CPU_SEL
VDD_REF
XTAL_IN
XTAL_OUT
VSS_REF
CKPWRGD/PD#
VDD_CPU
CPU_0
CPU_0#
VSS_CPU
CPU_1
CPU_1#
VDD_CPU_IO
VDD_SRC

Read Address:D3H;
Write Address:D2H

D_CK_SCLK
D_CK_SDATA
REF_0/CPU_SEL
R1 33_0402_5%
CLK_BUF_PCH_14M 18
CLK_XTAL_IN
CLK_XTAL_OUT
CK505_PWRGD
CLK_BUF_CPU_BCLK_R
CLK_BUF_CPU_BCLK#_R
RP3 0_0404_4P2R_5%
CLK_BUF_CPU_BCLK 18
CLK_BUF_CPU_BCLK# 18

Integrated 33ohm Resistor

IDT: 9LRS3199AKLFT, SA000030P00
SILEGO: SLG8SP587, SA00002XY00

Now, we are used IDT CLK G. 11/13 Joyce

D_CK_SCLK @ C12 100P_0402_50V8J
D_CK_SDATA @ C13 100P_0402_50V8J

+3VS
Silego Have Internal Pull-Up
R6 10K_0402_5% H_STP_CPU#

R8 place close to U1(CLK G) within 100mil.

IDT Have Internal Pull-Down
@ R8 10K_0402_5% REF_0/CPU_SEL

PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

+3VS
R7 4.7K_0402_5%
18,27,28 PCH_SMBDATA
Q2 2N7002_SOT23
D_CK_SDATA

+3VS
R9 4.7K_0402_5%
18,27,28 PCH_SMBCLK
Q3 2N7002_SOT23
D_CK_SCLK

+3VS
R4 10K_0402_5%
R5 0_0402_5%
CK505_PWRGD
VGATE 19,34,50
Q50 2N7002_SOT23
CLK_ENABLE# 50
CLK_ENABLE# @ C14 100P_0402_50V8J

CLK_XTAL_IN
C15 27P_0402_50V8J
Y1 14.31818MHz_20P_FSX8L14.318181M20FDB
C16 27P_0402_50V8J
CLK_XTAL_OUT

Title	CLK GENERATOR		
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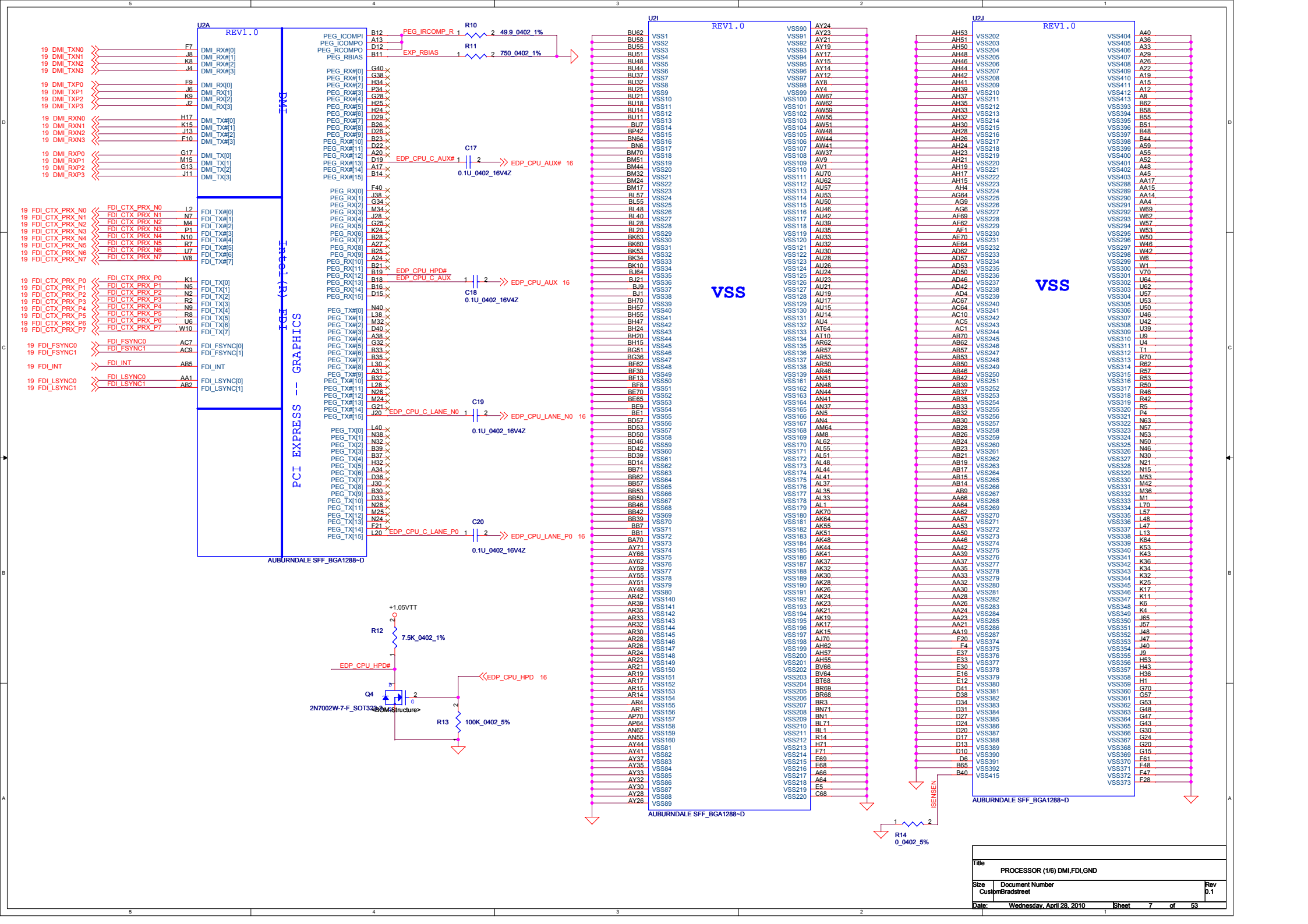
U2A
REV1.0
DMI
PCI EXPRESS -- GRAPHICS
FDI (R) FDI
AUBURNDALE SFF_BGA1288~D
U2I
REV1.0
VSS
AUBURNDALE SFF_BGA1288~D
U2J
REV1.0
VSS
AUBURNDALE SFF_BGA1288~D
R10 49.9_0402_1%
R11 750_0402_1%
C17 0.1U_0402_16V4Z
C18 0.1U_0402_16V4Z
C19 0.1U_0402_16V4Z
C20 0.1U_0402_16V4Z
+1.05VTT
R12 7.5K_0402_1%
Q4 2N7002W-7-F_SOT323-3
<BOMStructure>
R13 100K_0402_5%
R14 0_0402_5%
ISENSEN
Title
PROCESSOR (1/6) DMI,FDI,GND
Size Custom
Document Number Bradstreet
Rev 0.1
Date: Wednesday, April 28, 2010
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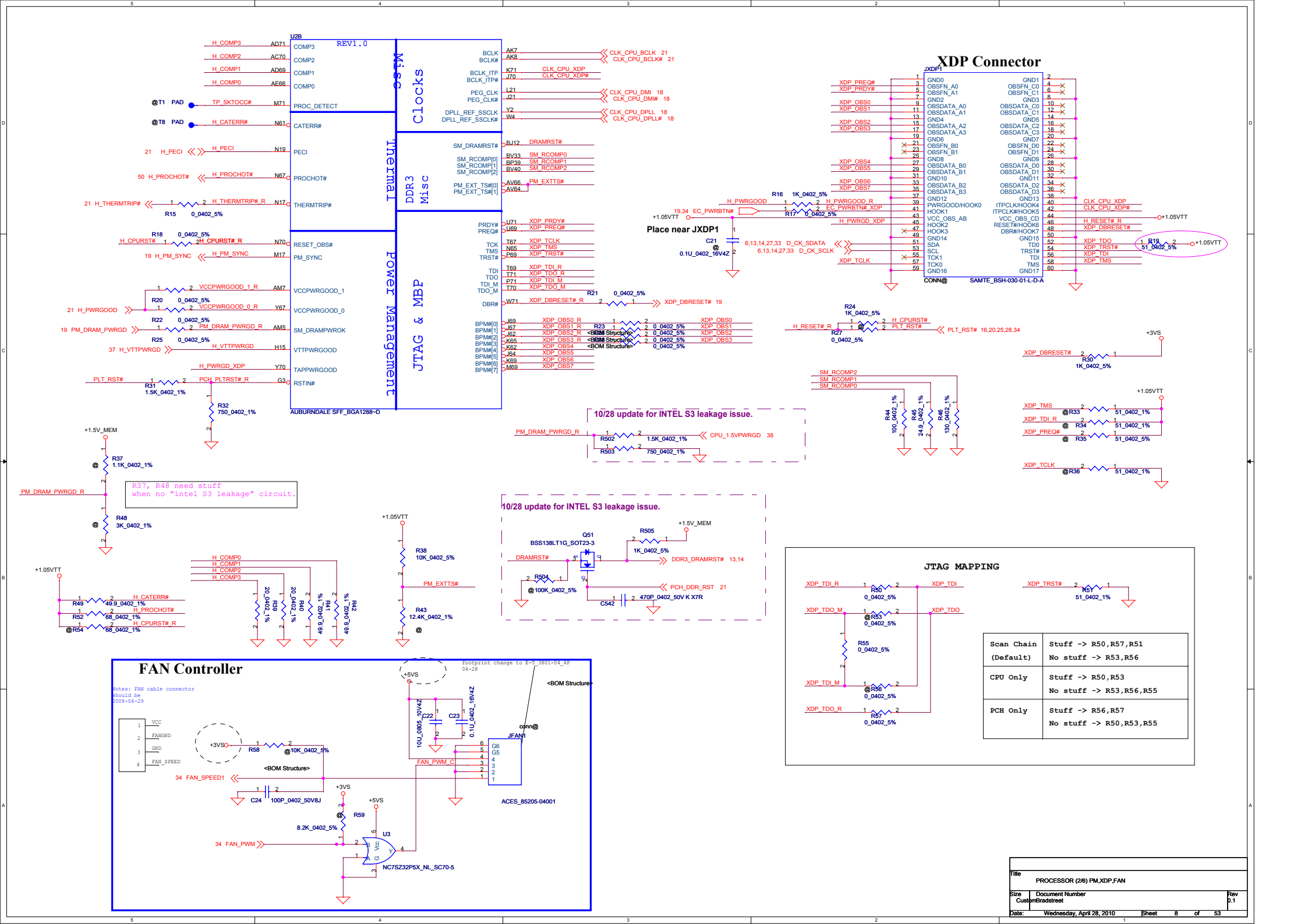
U2B
REV1.0
Misc Thermal Power Management
Clocks
DDR3 Misc
JTAG & MBP
AUBURNDALE SFF_BGA1288~D
XDP Connector
JXDP1
Place near JXDP1
10/28 update for INTEL S3 leakage issue.
10/28 update for INTEL S3 leakage issue.
R37, R48 need stuff
when no "intel S3 leakage" circuit.
JTAG MAPPING
FAN Controller
footprint change to E-T 3801-04_4P 04-28
Notes: FAN cable connector should be 2008-04-29
JFAN1
ACES_85205-04001
NC7SZ32P5X_NL_SC70-5
CONN@
SAMTE_BSH-030-01-L-D-A
Scan Chain (Default) | Stuff -> R50,R57,R51 / No stuff -> R53,R56
CPU Only | Stuff -> R50,R53 / No stuff -> R53,R56,R55
PCH Only | Stuff -> R56,R57 / No stuff -> R50,R53,R55
Title
PROCESSOR (2/6) PM,XDP,FAN
Size Custom
Document Number Bradstreet
Rev 0.1
Date: Wednesday, April 28, 2010
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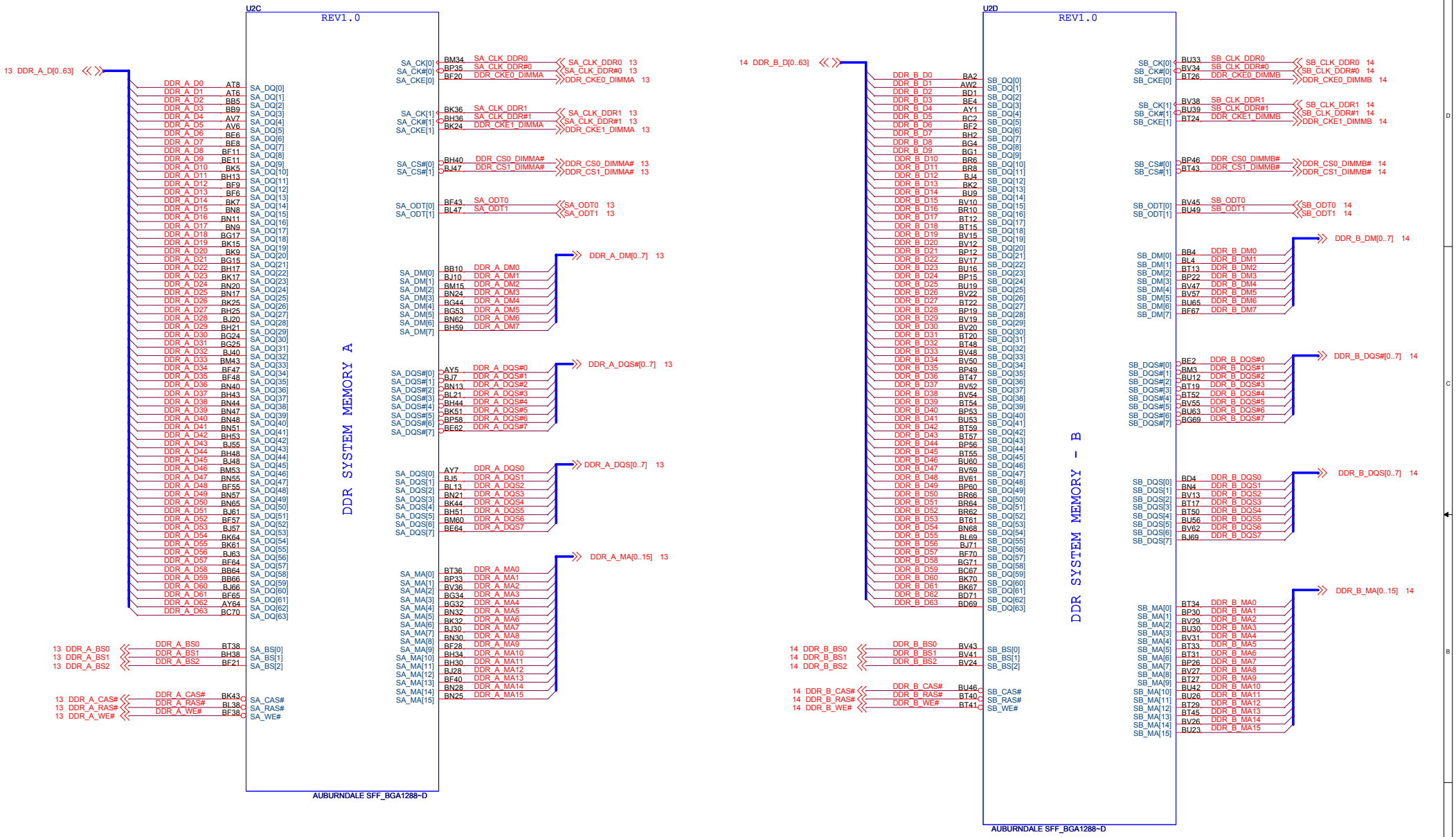
U2C
REV1.0
DDR SYSTEM MEMORY A
AUBURNDALE SFF_BGA1288~D
U2D
REV1.0
DDR SYSTEM MEMORY - B
AUBURNDALE SFF_BGA1288~D
13 DDR_A_D[0..63]
14 DDR_B_D[0..63]
DDR_A_DM[0..7] 13
DDR_A_DQS#[0..7] 13
DDR_A_DQS[0..7] 13
DDR_A_MA[0..15] 13
DDR_B_DM[0..7] 14
DDR_B_DQS#[0..7] 14
DDR_B_DQS[0..7] 14
DDR_B_MA[0..15] 14
Title
PROCESSOR (3/6) DDRIII
Size Custom
Document Number Bradstreet
Rev 0.1
Date: Wednesday, April 28, 2010
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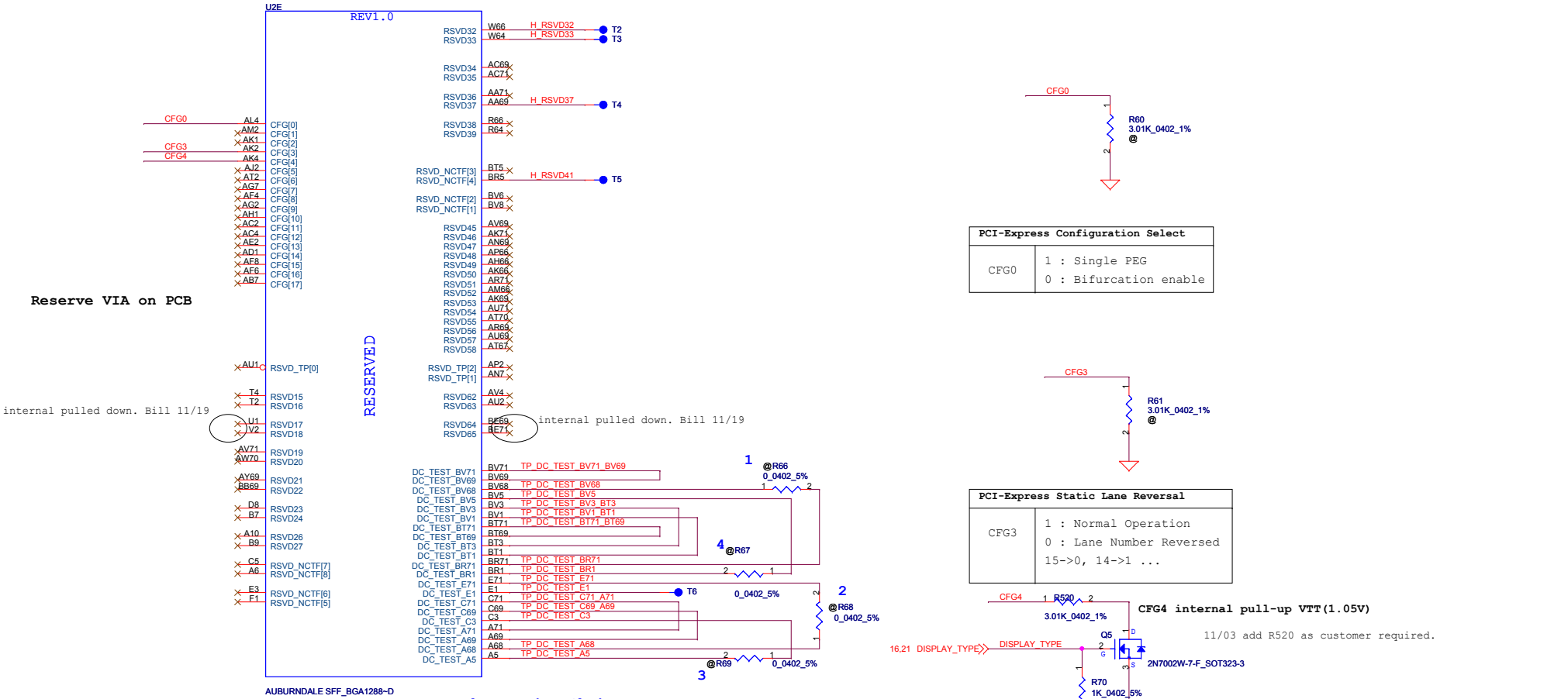

Package Daisy Chain:

1: BR71 - pkg - BT71- board - BT69 - pkg - BV71 - board - BV69 - pkg - BV68

2: A68 - pkg - A69 - board - C69 - pkg - A71 - board - C71 - pkg - E71

3: A5 - pkg - C3

4: BR1 - pkg - BT1 - board - BV1 - pkg - BT3 - board - BV3 - pkg - BV5

Title	PROCESSOR (4/6) RSVD,CF
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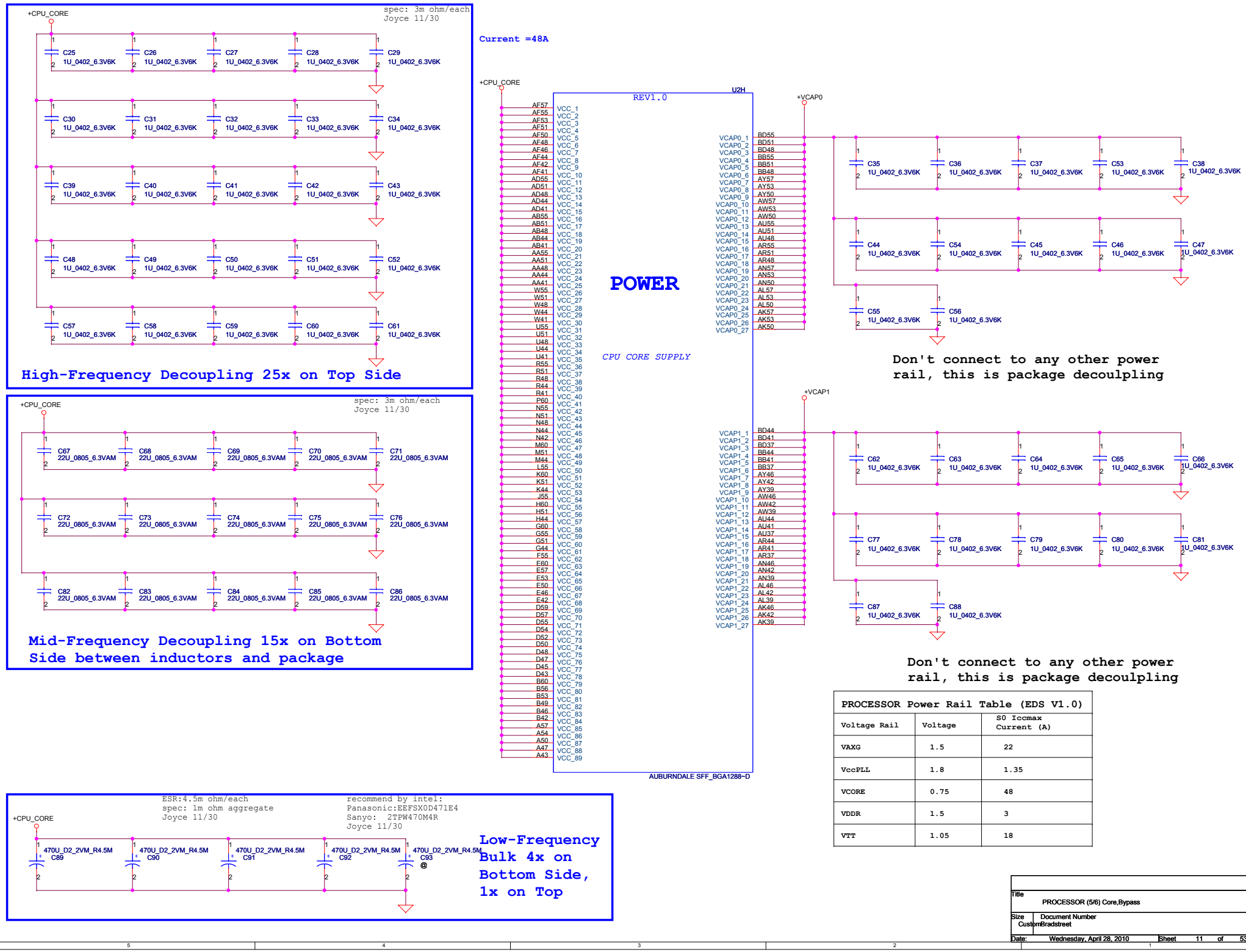

PROCESSOR Power Rail Table (EDS V1.0)

Voltage Rail	Voltage	S0 Iccmax Current (A)
VAXG	1.5	22
VccPLL	1.8	1.35
VCORE	0.75	48
VDDR	1.5	3
VTT	1.05	18

Title	PROCESSOR (5/6) Core,Bypass	
Size: Custom	Document Number: Bradstreet	Rev: 0.1
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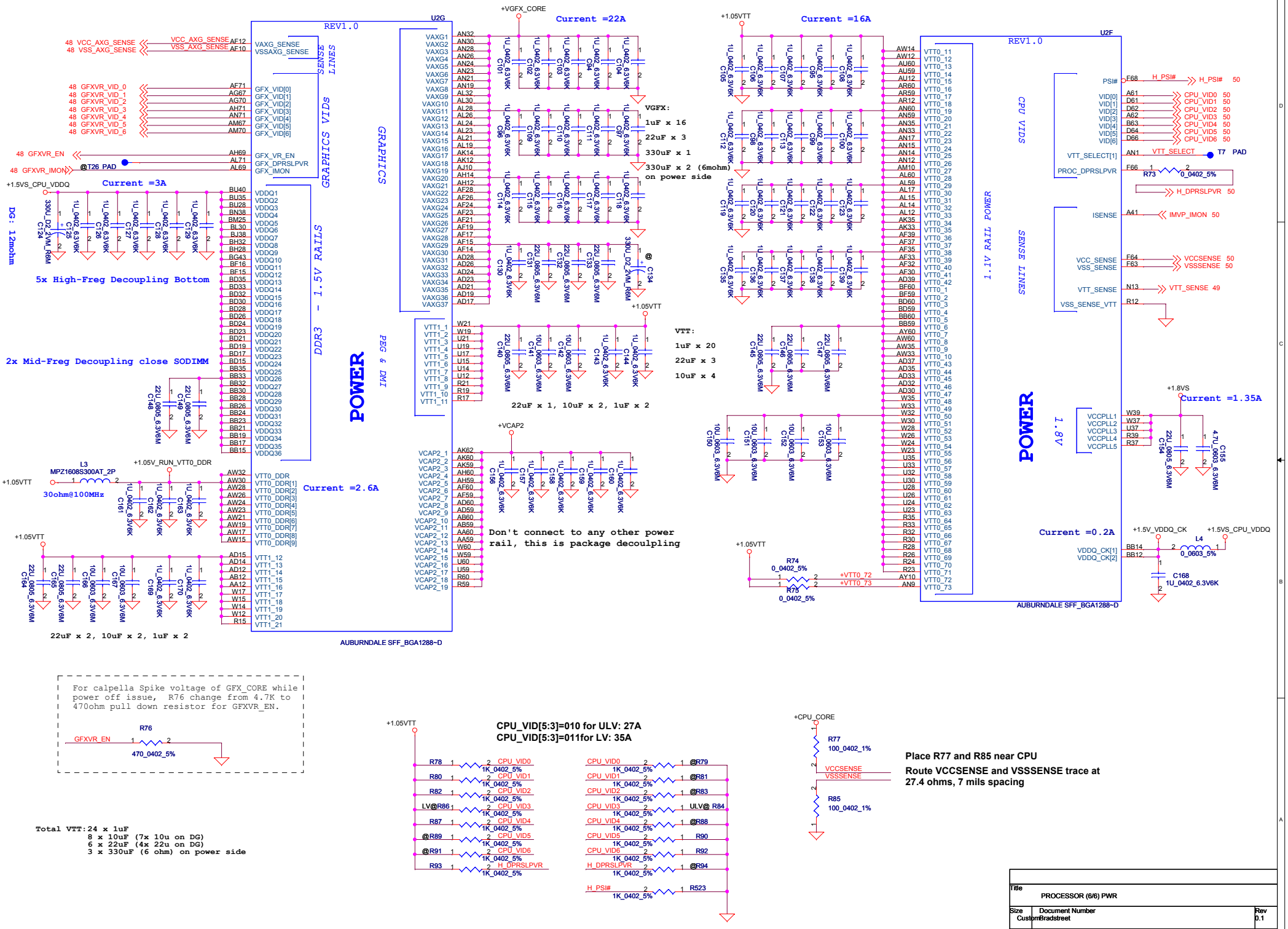
U2G
REV1.0
POWER
DDR3 - 1.5V RAILS
GRAPHICS VIDS
SENSE LINES
PEG & DMI
AUBURNDALE SFF_BGA1288~D
+VGFX_CORE
Current =22A
VGFX:
1uF x 16
22uF x 3
330uF x 1
330uF x 2 (6mohm)
on power side
+1.05VTT
Current =16A
VTT:
1uF x 20
22uF x 3
10uF x 4
22uF x 1, 10uF x 2, 1uF x 2
+VCAP2
Don't connect to any other power
rail, this is package decoulpling
+1.05VS_CPU_VDDQ
Current =3A
DG: 12mohm
5x High-Freg Decoupling Bottom
2x Mid-Freg Decoupling close SODIMM
L3
MPZ1608S300AT_2P
30ohm@100MHz
+1.05V_RUN_VTT0_DDR
Current =2.6A
22uF x 2, 10uF x 2, 1uF x 2
U2F
1.1V RAIL POWER
CPU VIDS
SENSE LINES
1.8V
Current =1.35A
Current =0.2A
+1.8VS
+1.5V_VDDQ_CK
+1.5VS_CPU_VDDQ
For calpella Spike voltage of GFX_CORE while
power off issue, R76 change from 4.7K to
470ohm pull down resistor for GFXVR_EN.
Total VTT: 24 x 1uF
8 x 10uF (7x 10u on DG)
6 x 22uF (4x 22u on DG)
3 x 330uF (6 ohm) on power side
CPU_VID[5:3]=010 for ULV: 27A
CPU_VID[5:3]=011for LV: 35A
Place R77 and R85 near CPU
Route VCCSENSE and VSSSENSE trace at
27.4 ohms, 7 mils spacing
Title
PROCESSOR (6/6) PWR
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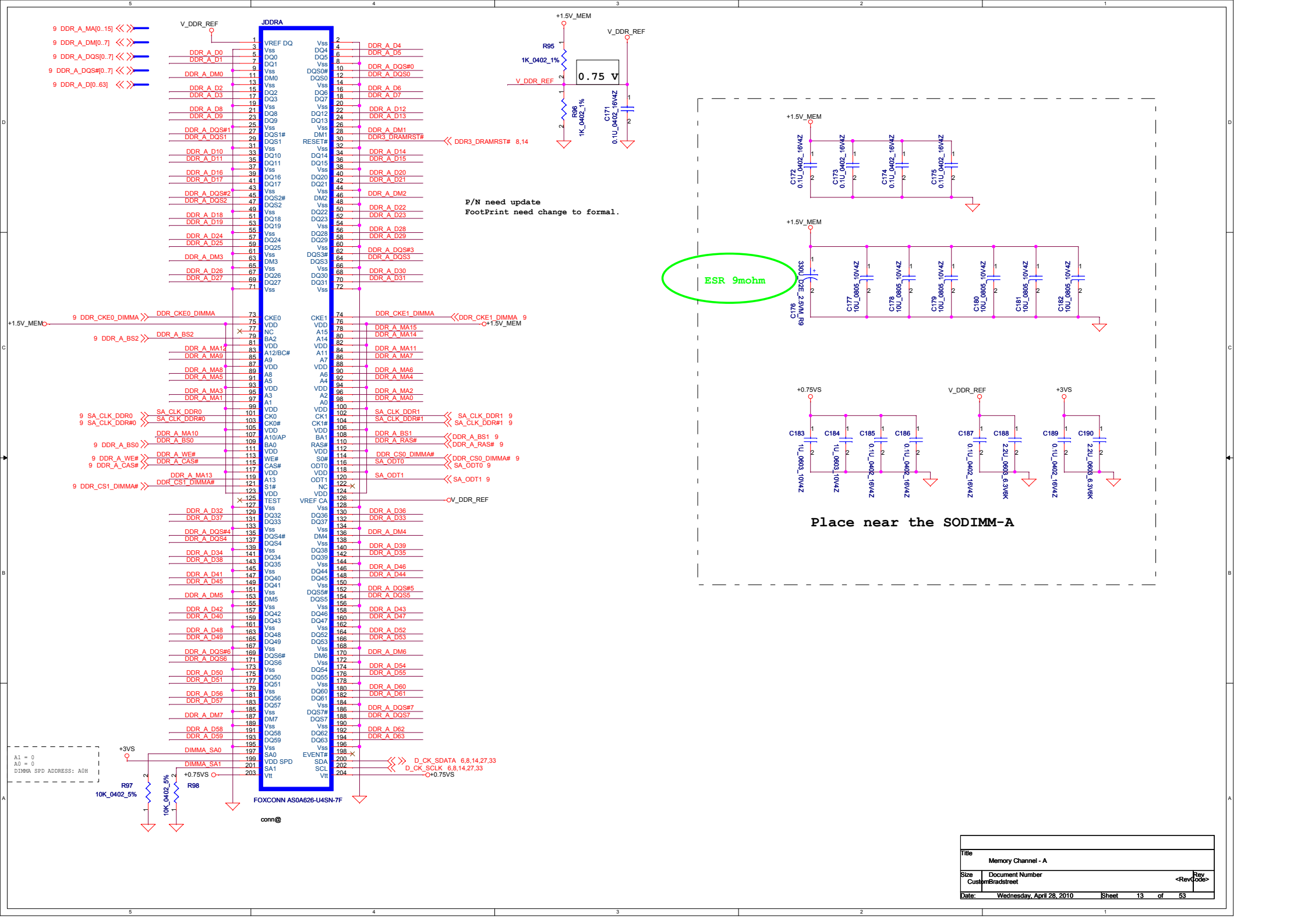
9 DDR_A_MA[0..15]
9 DDR_A_DM[0..7]
9 DDR_A_DQS[0..7]
9 DDR_A_DQS#[0..7]
9 DDR_A_D[0..63]
V_DDR_REF
JDDRA
DDR3_DRAMRST# 8,14
+1.5V_MEM
V_DDR_REF
R95
1K_0402_1%
0.75 V
R96
1K_0402_1%
C171
0.1U_0402_16V4Z
P/N need update
FootPrint need change to formal.
ESR 9mohm
+1.5V_MEM
C172 0.1U_0402_16V4Z
C173 0.1U_0402_16V4Z
C174 0.1U_0402_16V4Z
C175 0.1U_0402_16V4Z
+1.5V_MEM
330U_D2E_2.5VM_R9
C176
C177 10U_0805_10V4Z
C178 10U_0805_10V4Z
C179 10U_0805_10V4Z
C180 10U_0805_10V4Z
C181 10U_0805_10V4Z
C182 10U_0805_10V4Z
+0.75VS
V_DDR_REF
+3VS
C183 1U_0603_10V4Z
C184 1U_0603_10V4Z
C185 0.1U_0402_16V4Z
C186 0.1U_0402_16V4Z
C187 0.1U_0402_16V4Z
C188 2.2U_0603_6.3V6K
C189 0.1U_0402_16V4Z
C190 2.2U_0603_6.3V6K
Place near the SODIMM-A
A1 = 0
A0 = 0
DIMMA SPD ADDRESS: A0H
+3VS
R97
10K_0402_5%
R98
10K_0402_5%
+0.75VS
FOXCONN AS0A626-U4SN-7F
conn@
Title
Memory Channel - A
Size
Custom
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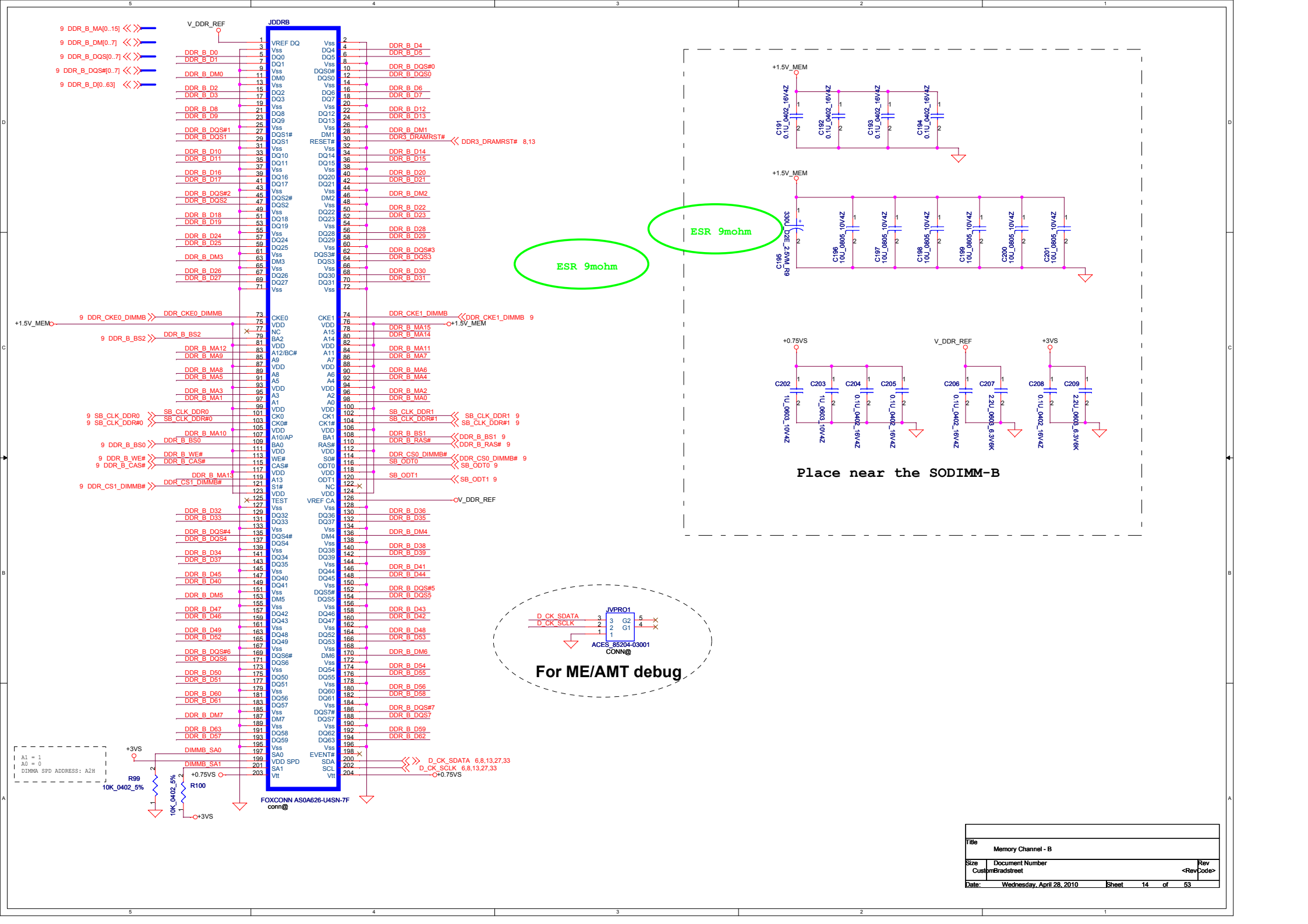

Title	Memory Channel - B	
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CRT

+3vs, Decoupling Capacitors for PI3512.

C210 0.1U_0402_16V4Z, C211 0.1U_0402_16V4Z, C212 0.1U_0402_16V4Z, C213 0.1U_0402_16V4Z

Need change to same net with LAN switch/USB switch

defult 0, need add pull down R? 04/25

U4 PI3V512QE_QSOP24

34 DOCKEN_VGA	DOCKEN_VGA	SEL	
19 D_RED	D_RED	YA	CRT_R_MB
19 D_GREEN	D_GREEN	YB	CRT_G_MB
19 D_BLUE	D_BLUE	YC	CRT_B_MB
19 CRT_HSYNC	CRT_HSYNC	YD	CRT_HSYNC_MB
19 CRT_VSYNC	CRT_VSYNC	YE	CRT_VSYNC_MB
		GND	CRT_R_DOCK → CRT_R_DOCK 36
		GND	CRT_G_DOCK → CRT_G_DOCK 36
		GND	CRT_B_DOCK → CRT_B_DOCK 36
		GND	CRT_HSYNC_DOCK → CRT_HSYNC_DOCK 36
		GND	CRT_VSYNC_DOCK → CRT_VSYNC_DOCK 36

DOCKEN_VGA	
0: TO MB ★	L YN to IN0
1: TO DOCK	H YN to IN1

R101 10K_0402_5%, DOCKEN_VGA# / DOCKEN_VGA, Q6 2N7002W-7-F_SOT323-3

C214 0.1U_0402_16V4Z @

add BS"@" to C214 since CRT DDC signals EA test Rising time and Falling time fail.

R102 2.2K_0402_5%, R103 2.2K_0402_5%, CRT_DDC_CLK, CRT_DDC_DATA

U5 SN74CBTD3306CPWR_TSSOP8

19 CRT_DDC_DATA	CRT_DDC_DATA	1A
	DOCKEN_VGA	1OE#
	DOCKEN_VGA#	2OE#
	3VDDCDA	VCC
	3VDDCDA_DOCK → 3VDDCDA_DOCK 36	2B
		GND

C215 0.1U_0402_16V4Z

U6 SN74CBTD3306CPWR_TSSOP8

19 CRT_DDC_CLK	CRT_DDC_CLK	1A
	DOCKEN_VGA	1OE#
	DOCKEN_VGA#	2OE#
	3VDDCCL	VCC
	3VDDCCL_DOCK → 3VDDCCL_DOCK 36	2B
		GND

C216 0.1U_0402_16V4Z

need 47onh25%/0.3ohm/100mA Bead SM01000C600

FBMA-L11-201209-170LMT L5, L6, L7

CRT_R_MB → CRT_R_MB_MID, CRT_G_MB → CRT_G_MB_MID, CRT_B_MB → CRT_B_MB_MID

R106 0_0603_5%, R107 0_0603_5%, R108 0_0603_5%

CRT_R_MB_MID → CRTR, CRT_G_MB_MID → CRTG, CRT_B_MB_MID → CRTB

D2 DAN217_SC59-3, D3 DAN217_SC59-3, D4 DAN217_SC59-3

C218 0.1U_0402_16V4Z

R109 150_0402_1%, R110 150_0402_1%, R111 150_0402_1%

C222 10P_0402_50V8K, C223 10P_0402_50V8K, C224 10P_0402_50V8K, C225 10P_0402_50V8K, C226 10P_0402_50V8K, C227 10P_0402_50V8K, C228 10P_0402_50V8K @, C229 10P_0402_50V8K @, C230 10P_0402_50V8K @

will update to 47ohm/100MHz bead.

P6-GND, P11-NC, P7-GND, P12-3VDDCDA, P8-GND, P13-HSYNC, P9-CRTVCC, P14-VSYNC, P10-GND, P15-3VDDCCL

P1-R, P2-G, P3-B

CRT Footprint

F1 1.1A 6V UL/CSA/TUV, D1 PMEG2010ET

D1: changed main source from ROHM "SC1B491D000" to NXP "SCS00003H00". 01/19 DVT

+CRTVCC, C217 0.1U_0402_16V4Z, R104 2.2K_0402_5%, R105 2.2K_0402_5%

JCRT1 SUYIN_070112FR015S222XU

CRTR, CRTG, CRTB, CRT_HSYNC_MB_C, CRT_VSYNC_MB_C, 3VDDCDA, 3VDDCCL

C219 47P_0402_50V8J @, C220 47P_0402_50V8J @, C221 conn@ 100P_0402_50V8J

Follow ME advice change PN to DC060001300 2008-04-01, change PCB FT to SUYIN_070546FR015S2307R_15P, same with JAL70(A58) DVT, 0619

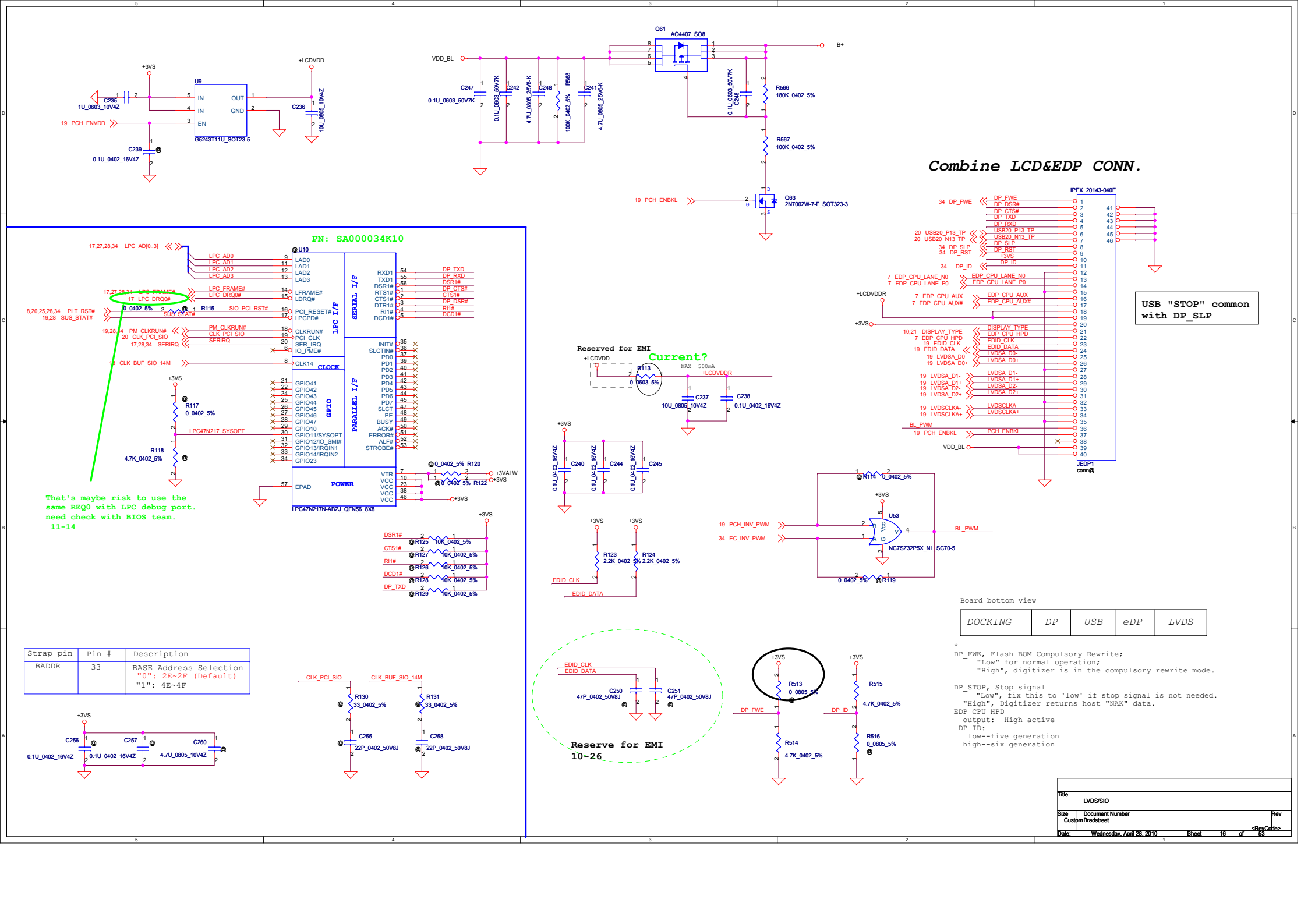
U7 74AHCT1G125GW_SOT353-5, U8 74AHCT1G125GW_SOT353-5

CRT_HSYNC_MB → CRT_HSYNC_MB_C, CRT_VSYNC_MB → CRT_VSYNC_MB_C

C233 0.1U_0402_16V4Z, C234 0.1U_0402_16V4Z, R112 1K_0402_5%

C231 0.1U_0402_16V4Z, C232 0.1U_0402_16V4Z, D5 DAN217_SC59-3, D6 DAN217_SC59-3

Title	CRT/BlueTooth/Camera
Size	Custom
Document Number	Bradstreet
Rev	<RevCode>
Date:	Wednesday, April 28, 2010
Sheet	15 of 53


Combine LCD&EDP CONN.
PN: SA000034K10
LPC47N217N-ABZJ_QFN56_8X8
That's maybe risk to use the same REQ0 with LPC debug port. need check with BIOS team. 11-14
Reserved for EMI
Current?
Reserve for EMI 10-26
USB "STOP" common with DP_SLP
Board bottom view
DOCKING
DP
USB
eDP
LVDS
DP_FWE, Flash BOM Compulsory Rewrite;
"Low" for normal operation;
"High", digitizer is in the compulsory rewrite mode.
DP_STOP, Stop signal
"Low", fix this to 'low' if stop signal is not needed.
"High", Digitizer returns host "NAK" data.
EDP_CPU_HPD
output: High active
DP_ID:
low--five generation
high--six generation
Strap pin | Pin # | Description
BADDR | 33 | BASE Address Selection "0": 2E~2F (Default) "1": 4E~4F
Title: LVDS/SIO
Size: Custom
Document Number: Bradstreet
Rev: <RevCode>
Date: Wednesday, April 28, 2010
Sheet 16 of 53

CMOS_CLR	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers

		PCH JTAG Enable		PCH JTAG Disable		Production
PCH Pin	Ref.	ES1	ES2	ES1	ES2	All
TDO	R152	No Stuff	200 ohm	No Stuff	No Stuff	51 ohm
	R156	No Stuff	100 ohm	No Stuff	No Stuff	No Stuff
TMS	R150	200 ohm	200 ohm	No Stuff	No Stuff	51 ohm
	R154	100 ohm	100 ohm	No Stuff	No Stuff	No Stuff
TDI	R151	200 ohm	200 ohm	20K ohm	No Stuff	51 ohm
	R155	100 ohm	100 ohm	10K ohm	No Stuff	No Stuff
TCK	R148	51 ohm	51 ohm	51 ohm	51 ohm	51 ohm

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

internal pull-up 20k

PCH_SPI_MOSI
High-internal TPM Enable
Low- internal TPM Disable

Place near HDD SATA connector.

Those decoupling capacitors need place near the SATA connector

No Reboot Strap	
SPKR	Low = Default
	High = No Reboot

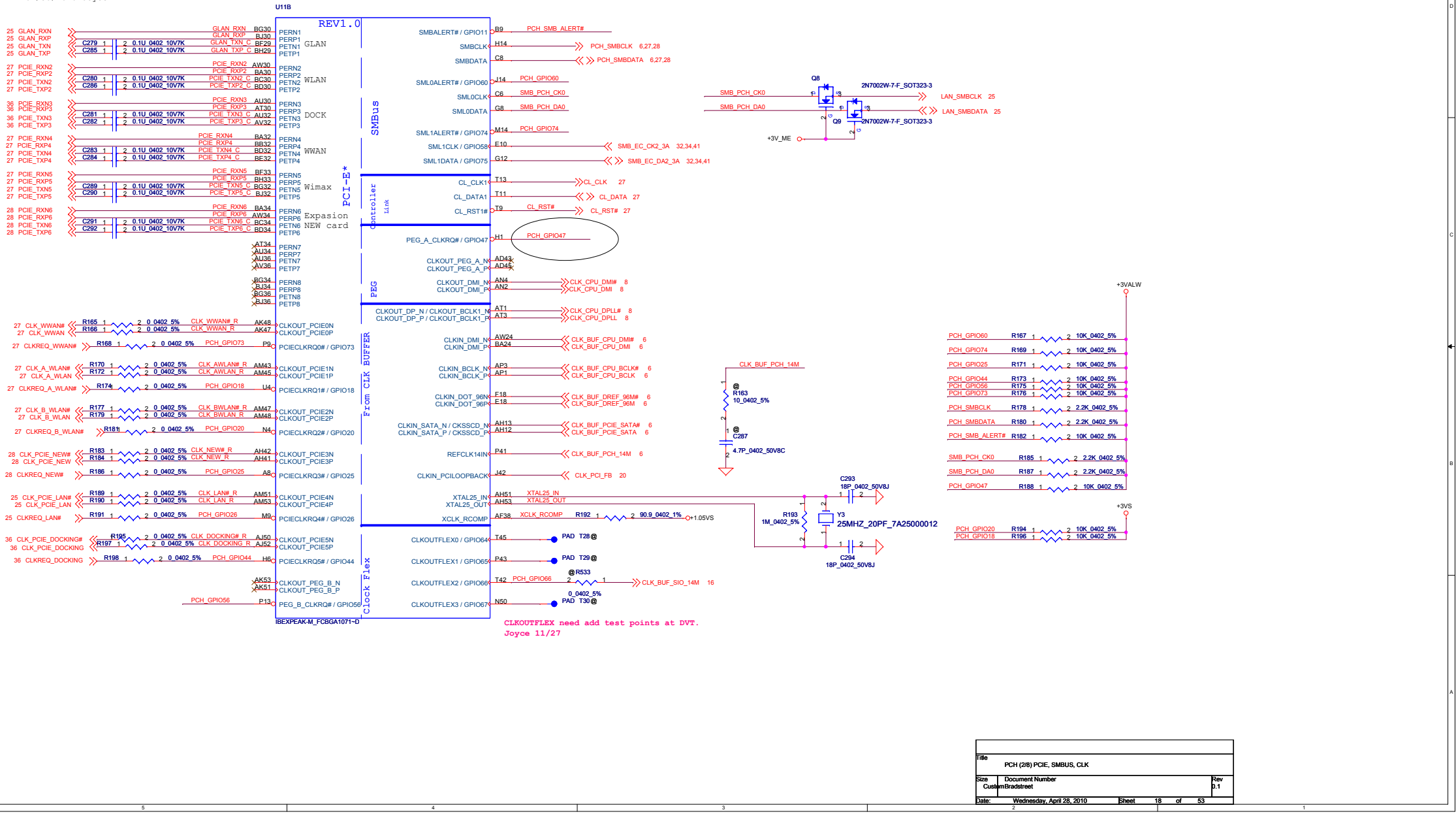
G-Sensor

SM BUS Addr: 0011 0000

Title	PCH(1/8)SATA,HDA,SPI,		
Size: Custom	Document Number: Bradstreet		Rev: 0.1
Date: Wednesday, April 28, 2010	Sheet 17 of 53		

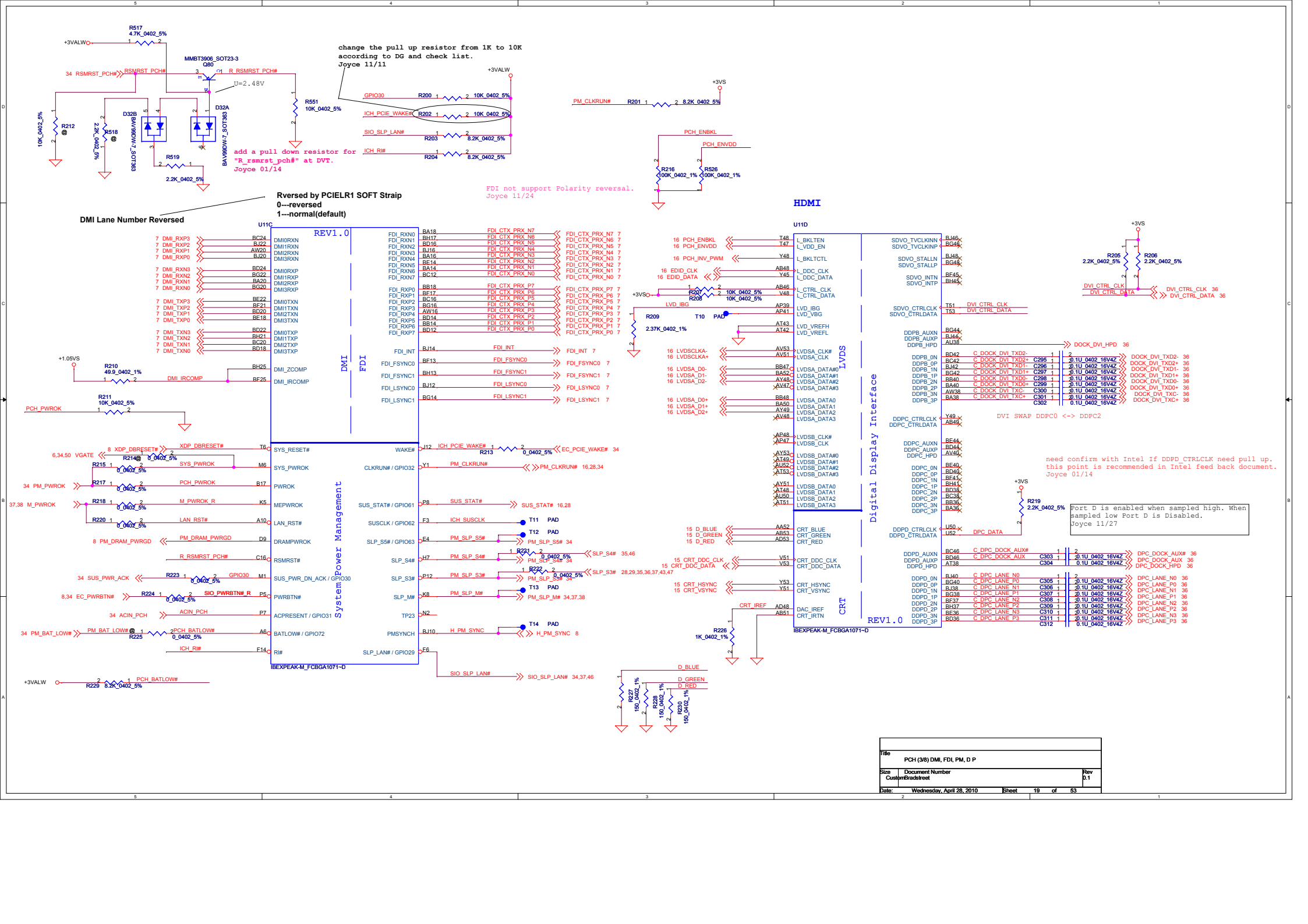
Swapped PCIE port1 & port 3 connection to PCH
01/27/2010 Joyce

changed PCH PCIE connection back same as original
via discussion with Jeff on con-call today.
01/30/2010 Joyce



CLKOUTFLEX need add test points at DVT.
Joyce 11/27

Title	PCH (2/8) PCIE, SMBUS, CLK		
Size: Custom	Document Number: Bradstreet		Rev: 0.1
Date: Wednesday, April 28, 2010	Sheet 18 of 53		


change the pull up resistor from 1K to 10K
according to DG and check list.
Joyce 11/11
add a pull down resistor for
"R_rsmrst_pch#" at DVT.
Joyce 01/14
Rversed by PCIELR1 SOFT Straip
0---reversed
1---normal(default)
DMI Lane Number Reversed
FDI not support Polarity reversal.
Joyce 11/24
HDMI
U11C
REV1.0
DMI
FDI
System Power Management
iBEXPEAK-M_FCBGA1071-D
U11D
LVDS
Digital Display Interface
CRT
REV1.0
iBEXPEAK-M_FCBGA1071-D
DVI SWAP DDPC0 <-> DDPC2
need confirm with Intel If DDPD_CTRLCLK need pull up.
this point is recommended in Intel feed back document.
Joyce 01/14
Port D is enabled when sampled high. When
sampled low Port D is Disabled.
Joyce 11/27
Title
PCH (3/8) DMI, FDI, PM, D P
Size
Custom
Document Number
Bradstreet
Rev
0.1
Date:
Wednesday, April 28, 2010
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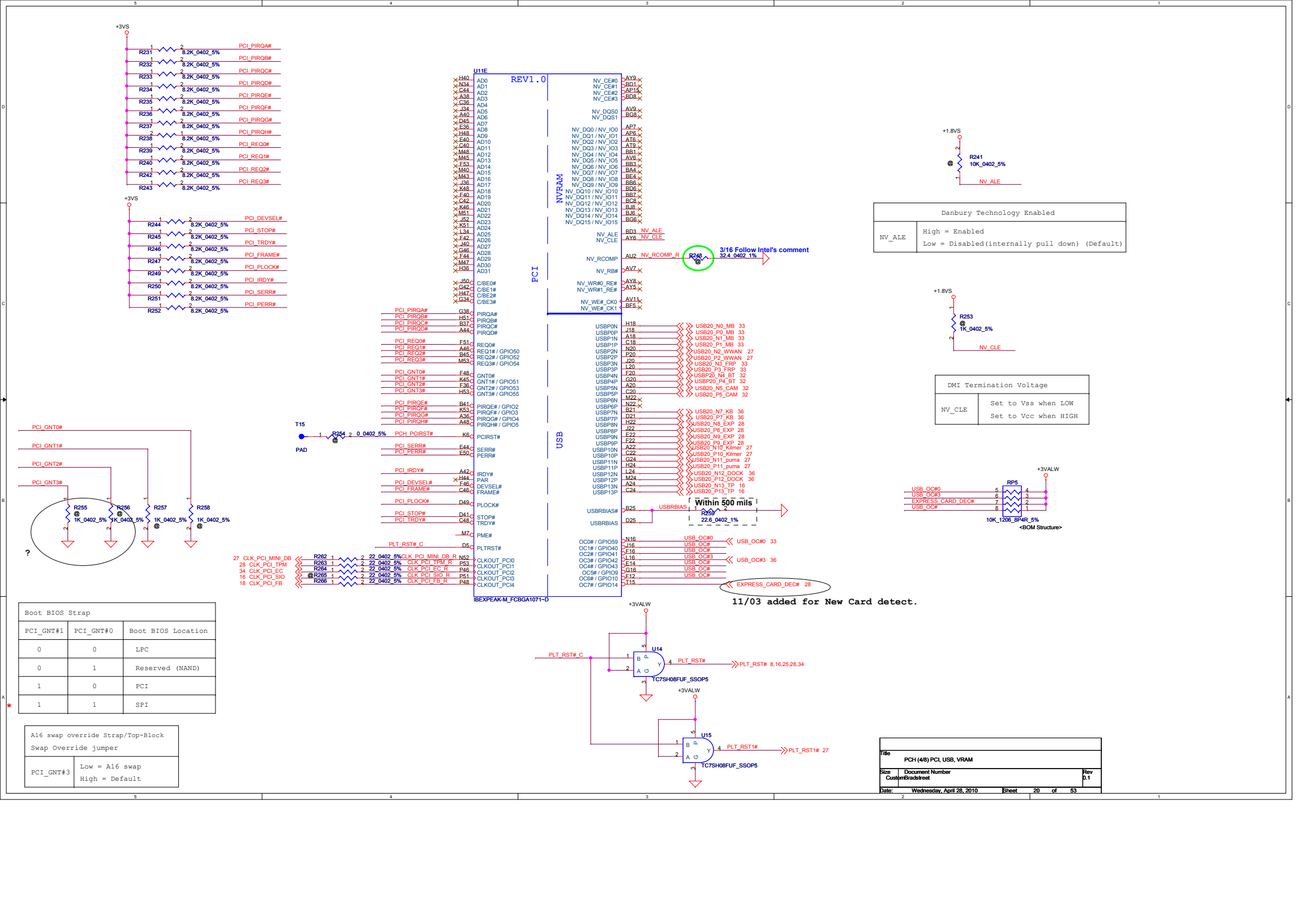
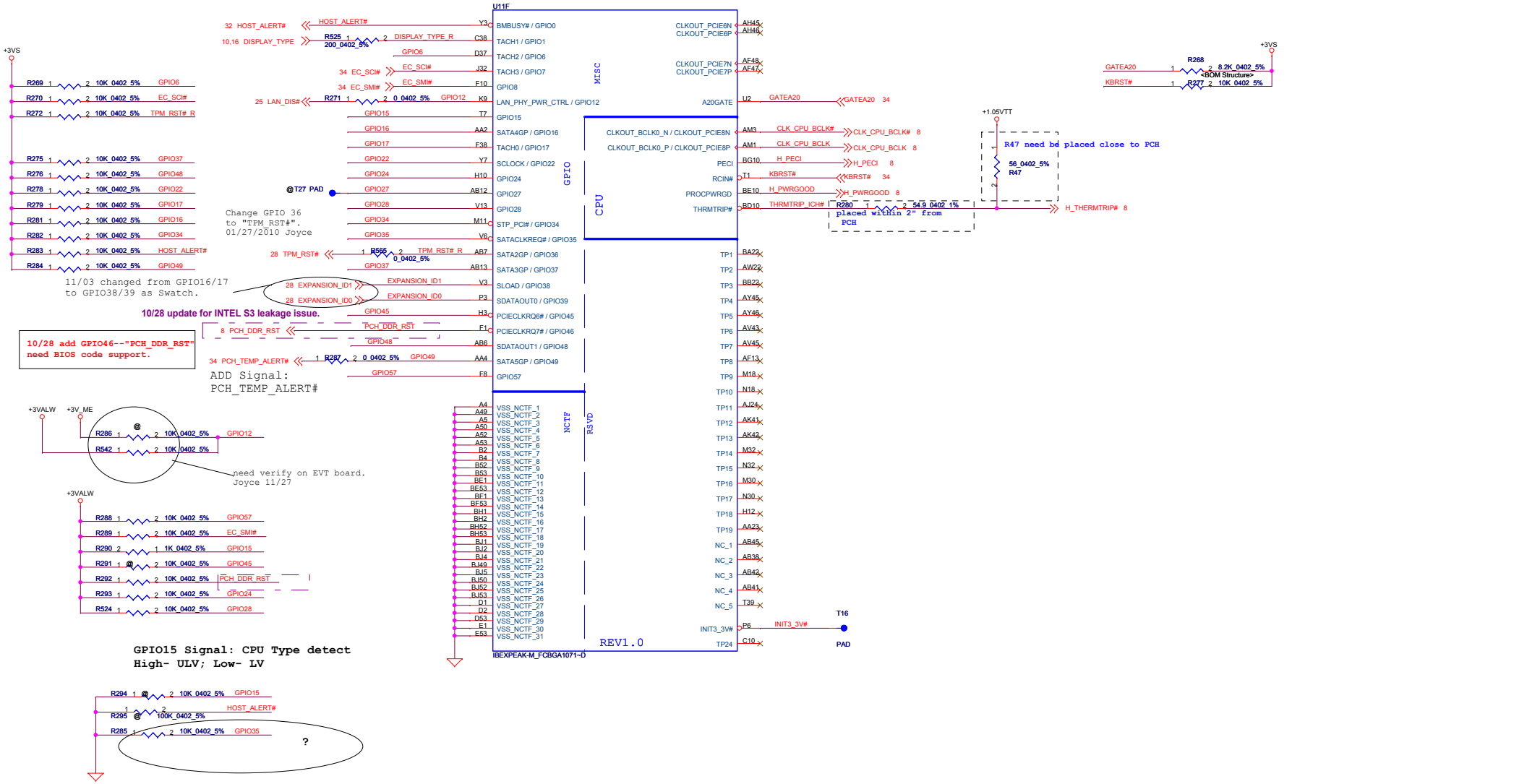
53


+3VS
R231 8.2K_0402_5% PCI_PIRQA#
R232 8.2K_0402_5% PCI_PIRQB#
R233 8.2K_0402_5% PCI_PIRQC#
R234 8.2K_0402_5% PCI_PIRQD#
R235 8.2K_0402_5% PCI_PIRQE#
R236 8.2K_0402_5% PCI_PIRQF#
R237 8.2K_0402_5% PCI_PIRQG#
R238 8.2K_0402_5% PCI_PIRQH#
R239 8.2K_0402_5% PCI_REQ0#
R240 8.2K_0402_5% PCI_REQ1#
R242 8.2K_0402_5% PCI_REQ2#
R243 8.2K_0402_5% PCI_REQ3#
+3VS
R244 8.2K_0402_5% PCI_DEVSEL#
R245 8.2K_0402_5% PCI_STOP#
R246 8.2K_0402_5% PCI_TRDY#
R247 8.2K_0402_5% PCI_FRAME#
R249 8.2K_0402_5% PCI_PLOCK#
R250 8.2K_0402_5% PCI_IRDY#
R251 8.2K_0402_5% PCI_SERR#
R252 8.2K_0402_5% PCI_PERR#
U11E
REV1.0
PCI
NVRAM
USB
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31
C/BE0# C/BE1# C/BE2# C/BE3#
PIRQA# PIRQB# PIRQC# PIRQD#
REQ0# REQ1# / GPIO50 REQ2# / GPIO52 REQ3# / GPIO54
GNT0# GNT1# / GPIO51 GNT2# / GPIO53 GNT3# / GPIO55
PIRQE# / GPIO2 PIRQF# / GPIO3 PIRQG# / GPIO4 PIRQH# / GPIO5
PCIRST#
SERR# PERR#
IRDY# PAR DEVSEL# FRAME#
PLOCK#
STOP# TRDY#
PME#
PLTRST#
CLKOUT_PCI0 CLKOUT_PCI1 CLKOUT_PCI2 CLKOUT_PCI3 CLKOUT_PCI4
NV_CE#0 NV_CE#1 NV_CE#2 NV_CE#3
NV_DQS0 NV_DQS1
NV_DQ0 / NV_IO0 NV_DQ1 / NV_IO1 NV_DQ2 / NV_IO2 NV_DQ3 / NV_IO3 NV_DQ4 / NV_IO4 NV_DQ5 / NV_IO5 NV_DQ6 / NV_IO6 NV_DQ7 / NV_IO7 NV_DQ8 / NV_IO8 NV_DQ9 / NV_IO9 NV_DQ10 / NV_IO10 NV_DQ11 / NV_IO11 NV_DQ12 / NV_IO12 NV_DQ13 / NV_IO13 NV_DQ14 / NV_IO14 NV_DQ15 / NV_IO15
NV_ALE NV_CLE
NV_RCOMP
NV_RB#
NV_WR#0_RE# NV_WR#1_RE#
NV_WE#_CK0 NV_WE#_CK1
USBP0N USBP0P USBP1N USBP1P USBP2N USBP2P USBP3N USBP3P USBP4N USBP4P USBP5N USBP5P USBP6N USBP6P USBP7N USBP7P USBP8N USBP8P USBP9N USBP9P USBP10N USBP10P USBP11N USBP11P USBP12N USBP12P USBP13N USBP13P
USBRBIAS# USBRBIAS
OC0# / GPIO59 OC1# / GPIO40 OC2# / GPIO41 OC3# / GPIO42 OC4# / GPIO43 OC5# / GPIO9 OC6# / GPIO10 OC7# / GPIO14
IBEXPEAK-M_FCBGA1071-D
R248 @ 32.4_0402_1% 3/16 Follow Intel's comment
R249 22.6_0402_1% Within 500 mils
USB_OC#0 USB_OC#3 USB_OC# EXPRESS_CARD_DEC# 28
11/03 added for New Card detect.
+1.8VS
R241 @ 10K_0402_5% NV_ALE
Danbury Technology Enabled
NV_ALE: High = Enabled; Low = Disabled(internally pull down) (Default)
+1.8VS
R253 @ 1K_0402_5% NV_CLE
DMI Termination Voltage
NV_CLE: Set to Vss when LOW; Set to Vcc when HIGH
+3VALW
RP5 10K_1206_8P4R_5%
<BOM Structure>
T15 PAD
R254 @ 0_0402_5% PCH_PCIRST#
PCI_GNT0# PCI_GNT1# PCI_GNT2# PCI_GNT3#
R255 @ 1K_0402_5% R256 @ 1K_0402_5% R257 @ 1K_0402_5% R258 @ 1K_0402_5%
?
27 CLK_PCI_MINI_DB R262 22_0402_5% CLK_PCI_MINI_DB_R
28 CLK_PCI_TPM R263 22_0402_5% CLK_PCI_TPM_R
34 CLK_PCI_EC R264 22_0402_5% CLK_PCI_EC_R
16 CLK_PCI_SIO @R265 22_0402_5% CLK_PCI_SIO_R
18 CLK_PCI_FB R266 22_0402_5% CLK_PCI_FB_R
PLT_RST# C
U14 TC7SH08FUF_SSOP5 PLT_RST# PLT_RST# 8,16,25,28,34
U15 TC7SH08FUF_SSOP5 PLT_RST1# PLT_RST1# 27
Boot BIOS Strap
PCI_GNT#1 | PCI_GNT#0 | Boot BIOS Location
0 | 0 | LPC
0 | 1 | Reserved (NAND)
1 | 0 | PCI
1 | 1 | SPI
A16 swap override Strap/Top-Block Swap Override jumper
PCI_GNT#3: Low = A16 swap; High = Default
Title: PCH (4/8) PCI, USB, VRAM
Size: Custom Document Number: BradStreet Rev: 0.1
Date: Wednesday, April 28, 2010 Sheet 20 of 53



Title	PCH (5/8) GPIO, CPU, MISC
Size	Custom
Document Number	Bradstreet
Rev	0.1
Date:	Wednesday, April 28, 2010
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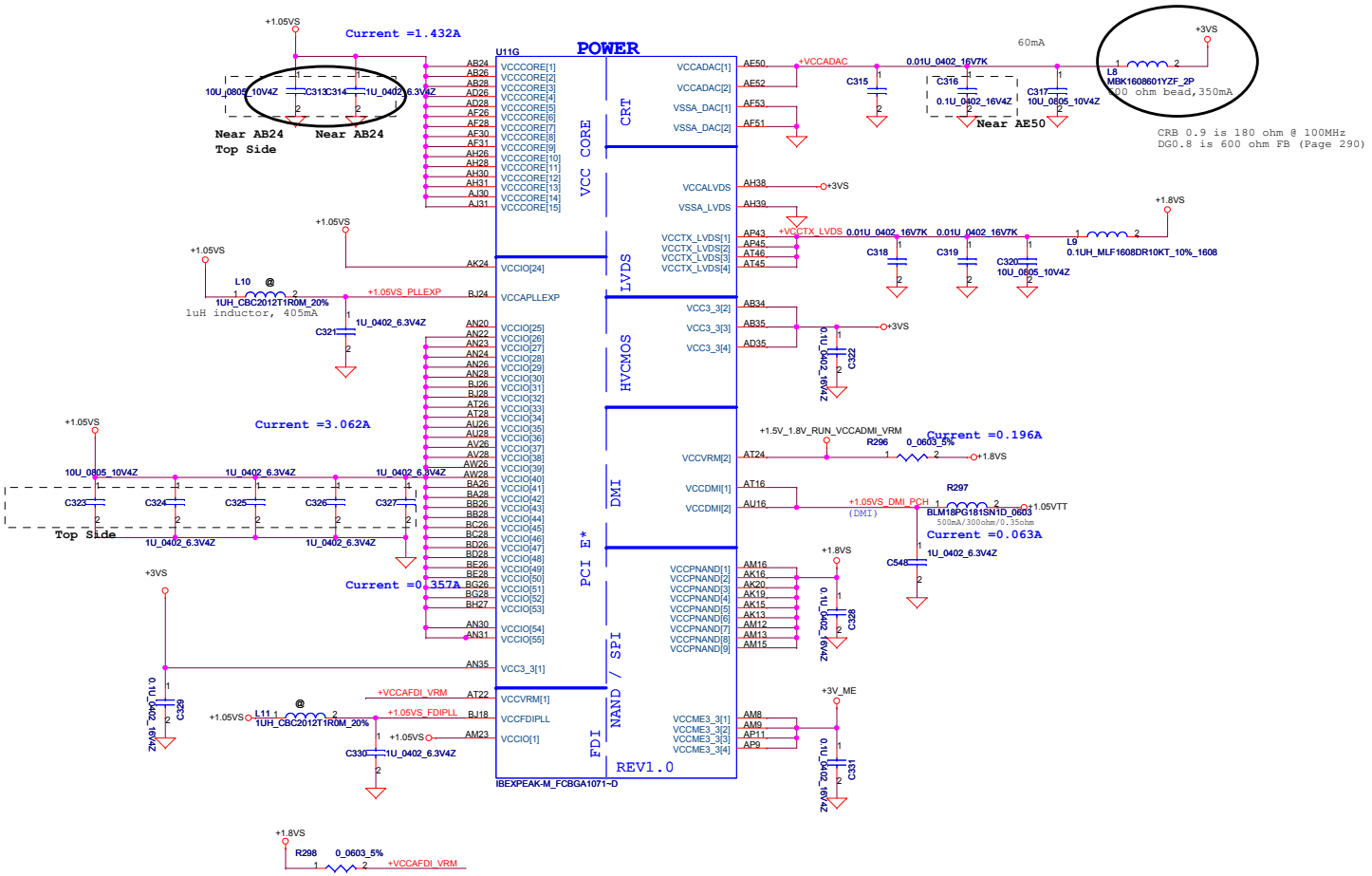
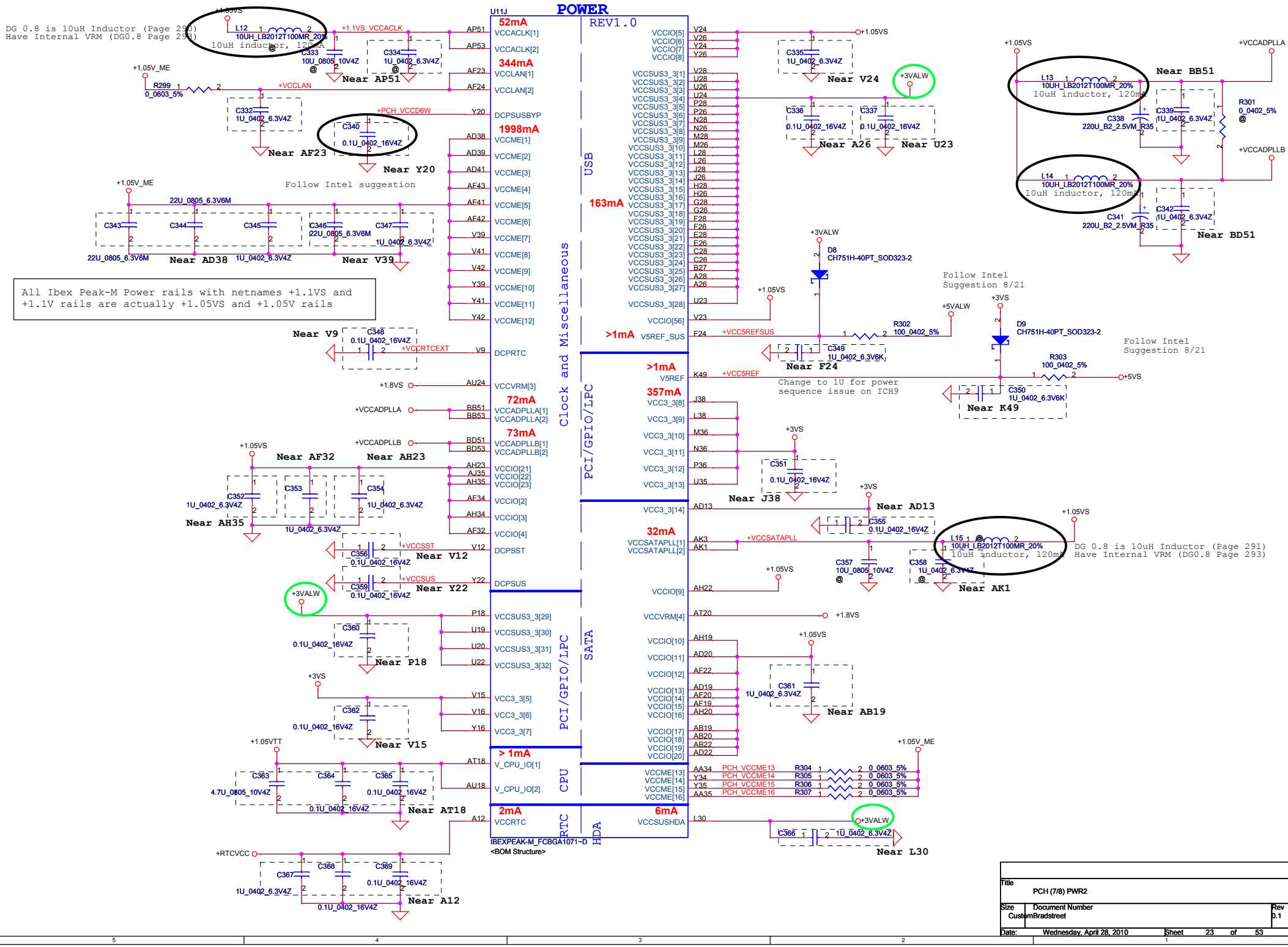


Title	PCH (6/8) PWR		
Size: Custom	Document Number: Bradstreet		Rev: 0.1
Date: Wednesday, April 28, 2010	Sheet 22 of 53		


POWER
REV1.0
U11J
IBEXPEAK-M_FCBGA1071~D
<BOM Structure>
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
DG 0.8 is 10uH Inductor (Page 290)
Have Internal VRM (DG0.8 Page 293)
10uH inductor, 120mA
Follow Intel suggestion
All Ibex Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails
Follow Intel Suggestion 8/21
Change to 1U for power sequence issue on ICH9
Title
PCH (7/8) PWR2
Size
Custom
Document Number
Bradstreet
Rev
0.1
Date:
Wednesday, April 28, 2010
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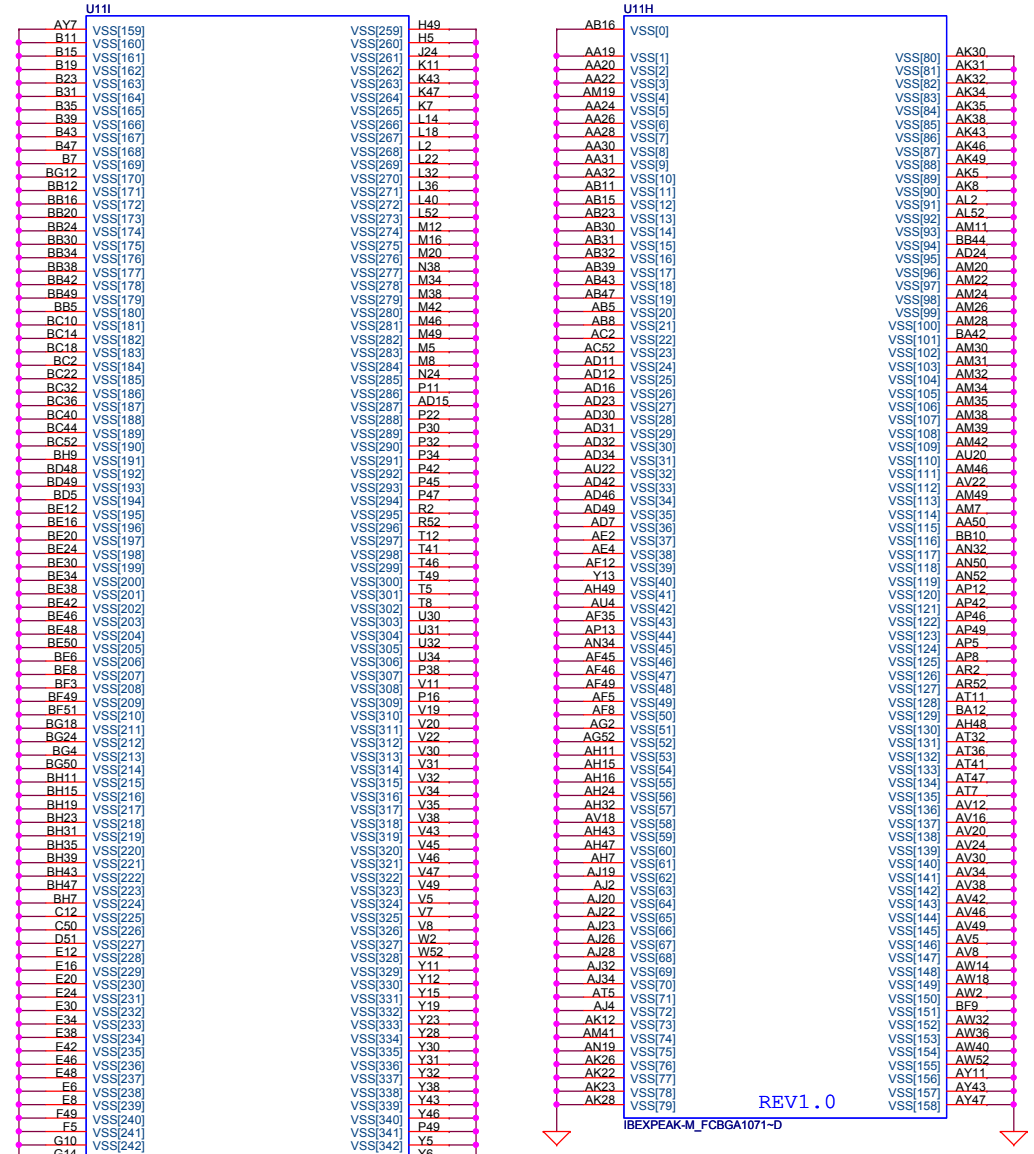
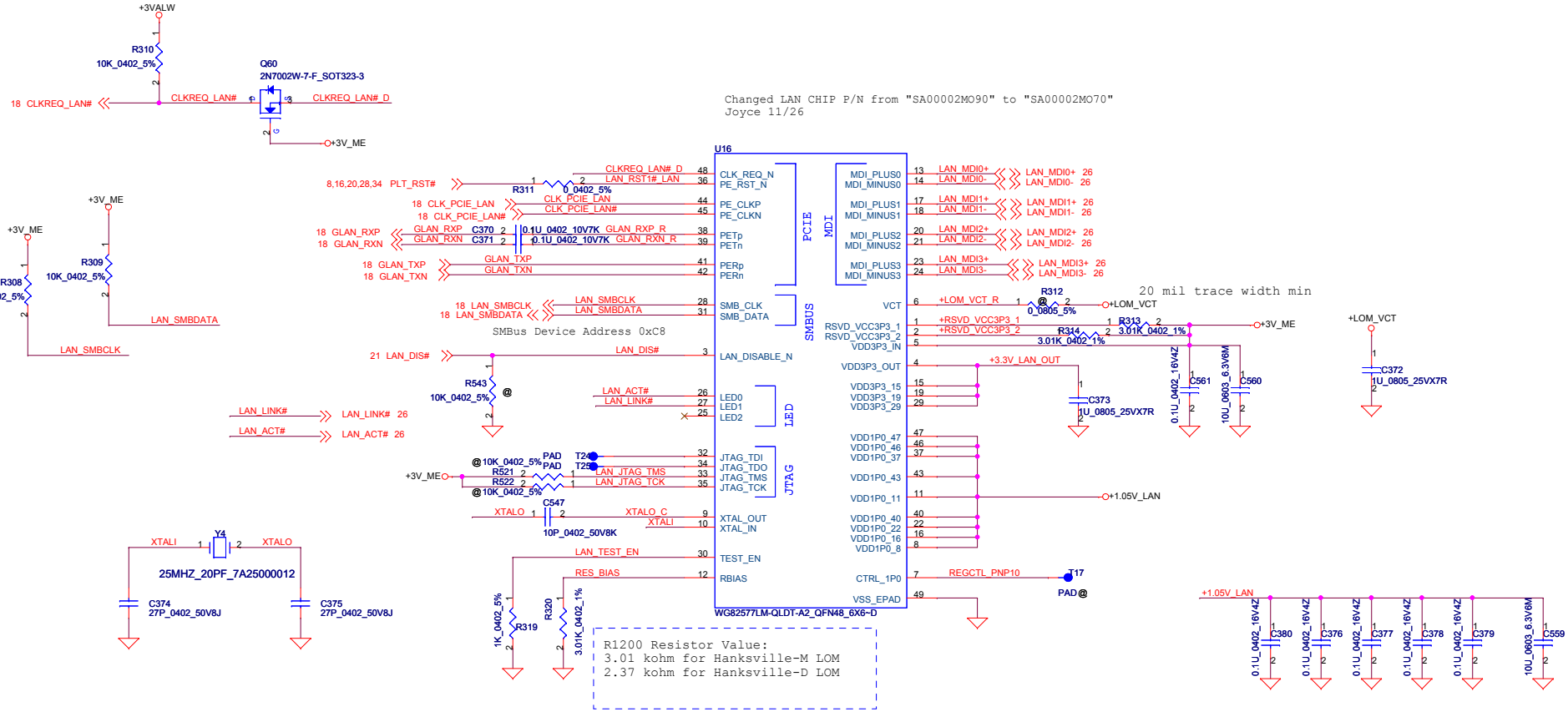
53



Title	PCH (8/8) VSS	
Size: Custom	Document Number: Bradstreet	Rev: 0.1
Date: Wednesday, April 28, 2010	Sheet 24 of 53	


Changed LAN CHIP P/N from "SA00002MO90" to "SA00002MO70"
Joyce 11/26
U16
WG82577LM-QLDT-A2_QFN48_6X6-D
PCIE
MDI
SMBUS
LED
JTAG
SMBus Device Address 0xC8
20 mil trace width min
R1200 Resistor Value:
3.01 kohm for Hanksville-M LOM
2.37 kohm for Hanksville-D LOM
25MHZ_20PF_7A25000012
Title
GiGa LAN 1/2
Size
Custom
Document Number
Bradstreet
Rev
0.2
Date:
Wednesday, April 28, 2010
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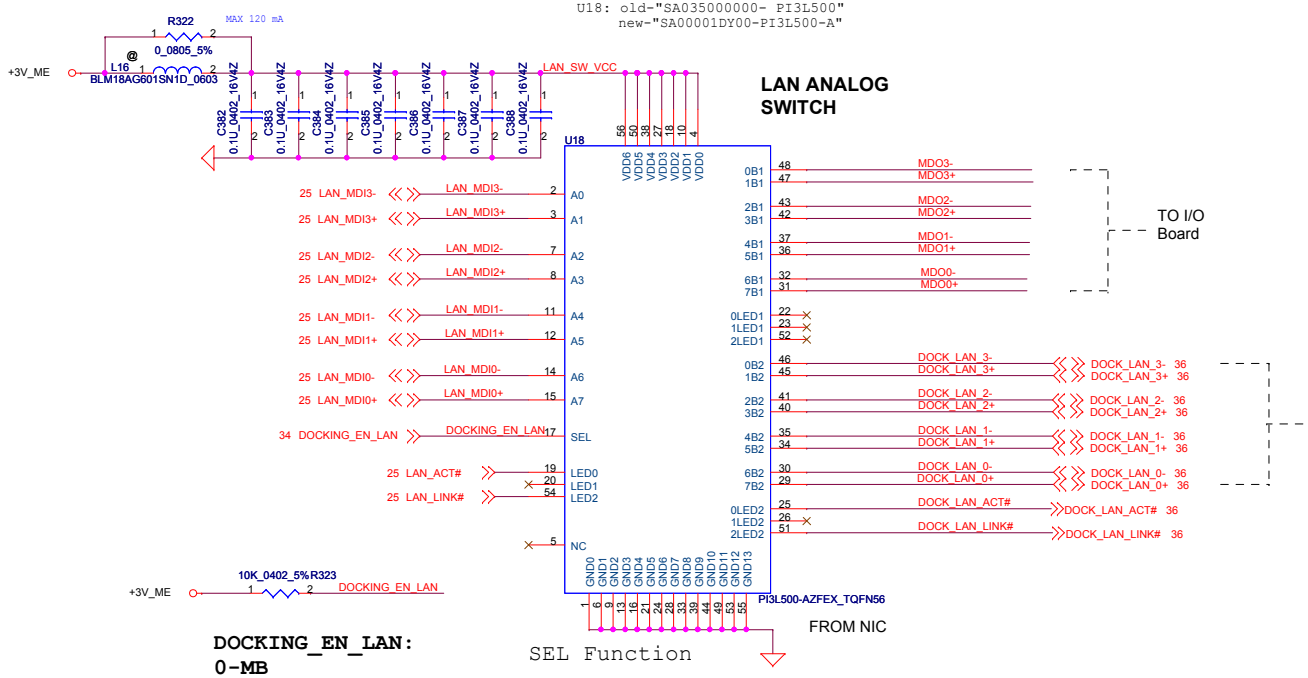
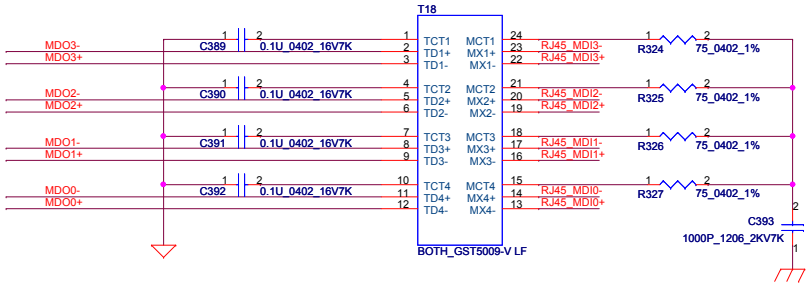
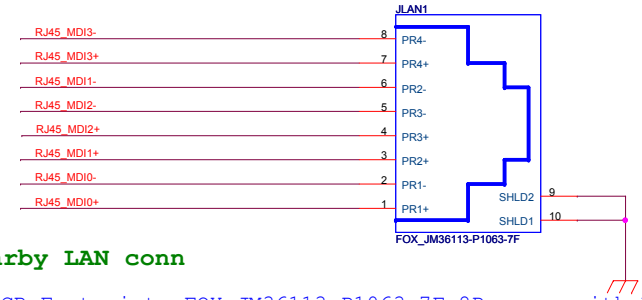
of
53



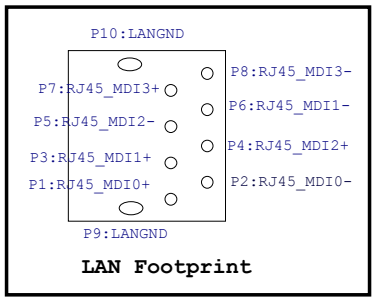
DOCKING_EN_LAN:
0-MB
1-DOCKING

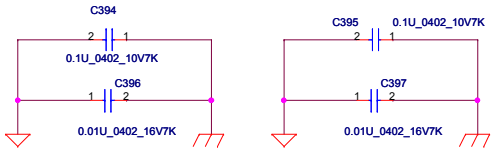




Please nearby LAN conn

USE DC234000B00 PCB Footprint, FOX_JM36113-P1063-7F_8P, same with EFL31
2008-03-18



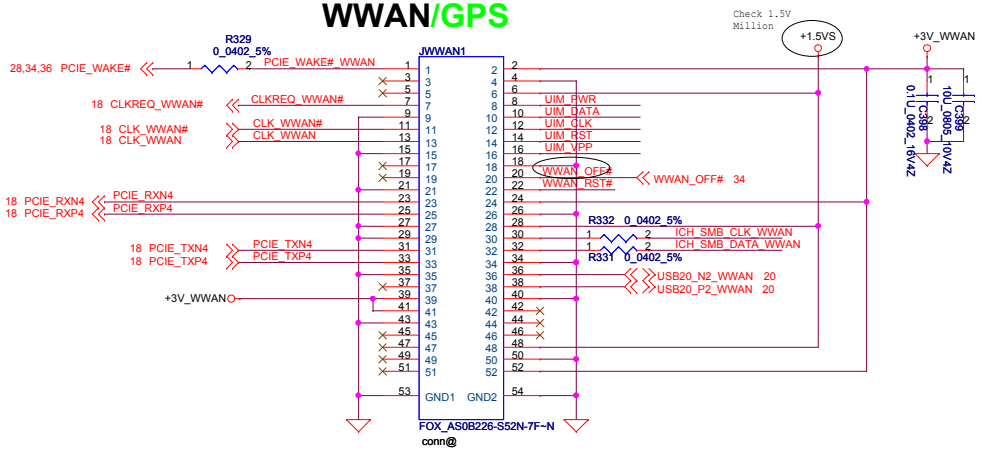


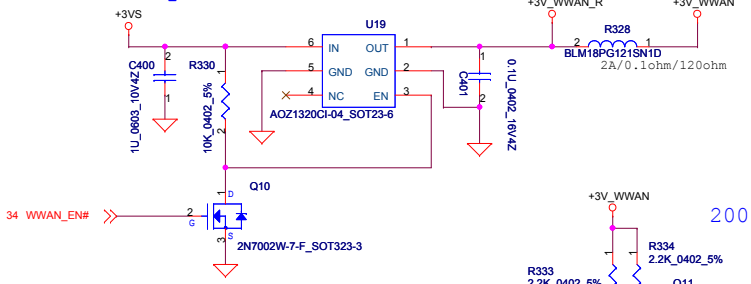
Realtek reference circuit for EMI!

Title	GiGa LAN 2/2	
Size: Custom	Document Number: Bradstreet	Rev: <RevCode>
Date: Wednesday, April 28, 2010	Sheet 26 of 53	

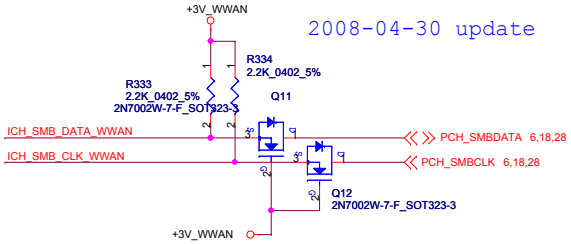
DVT, need study,0619

WWAN/GPS



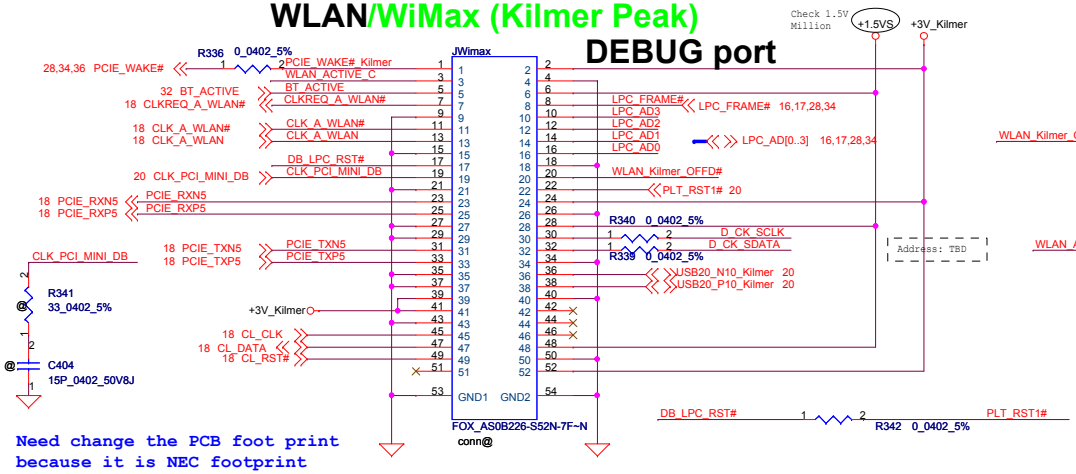


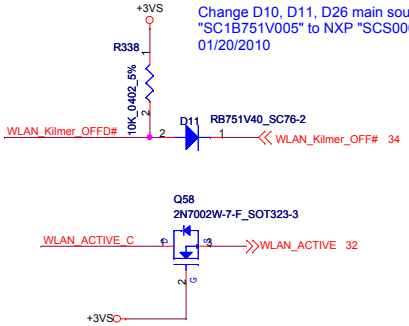
2008-04-30 update



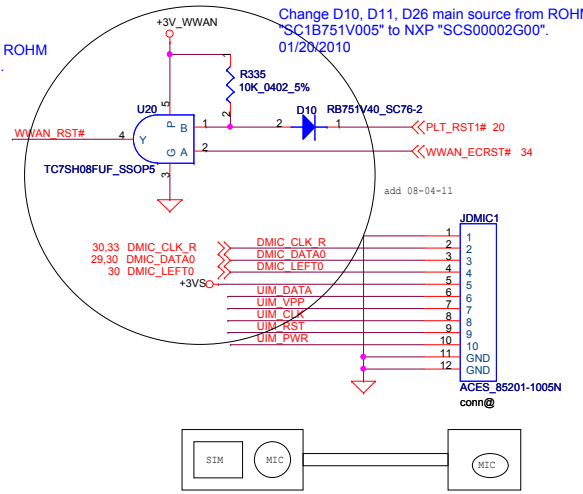
WLAN/WiMax (Kilmer Peak)

DEBUG port





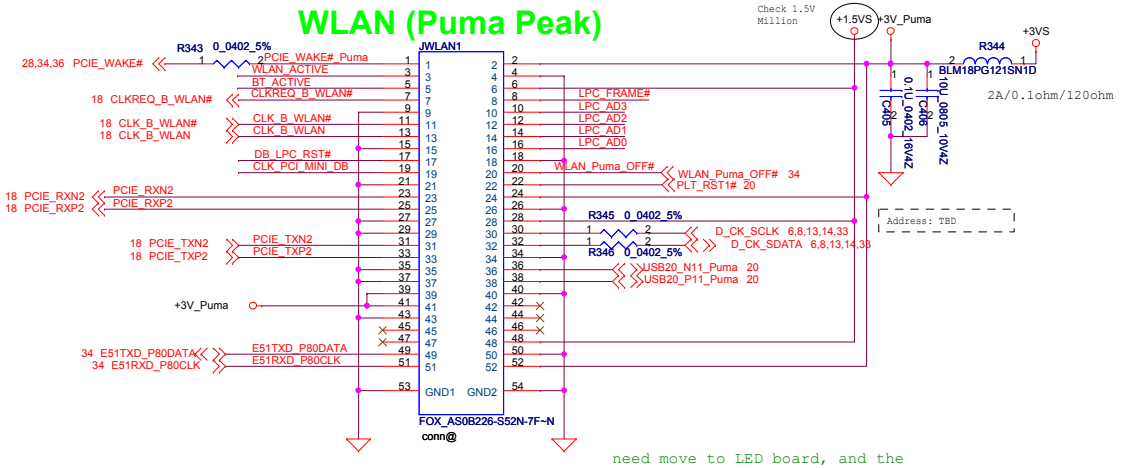
Change D10, D11, D26 main source from ROHM "SC1B751V005" to NXP "SCS00002G00".
01/20/2010

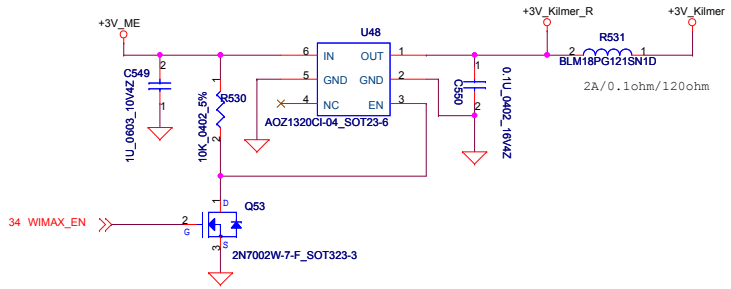


Change D10, D11, D26 main source from ROHM "SC1B751V005" to NXP "SCS00002G00".
01/20/2010

Need change the PCB foot print because it is NEC footprint

WLAN (Puma Peak)





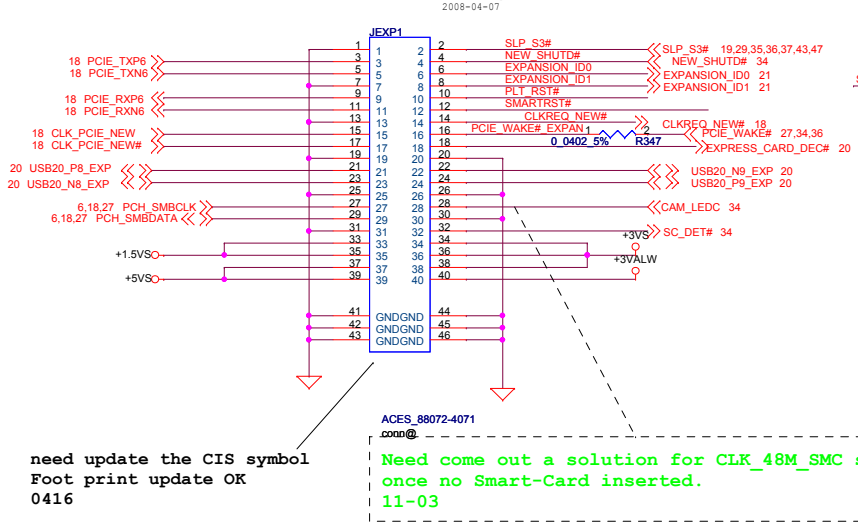
need move to LED board, and the corlor of LED need modify, also the dim adjustment circuit need been added.
11-12

Title	MINI-Card, Debug		
Size	Document Number		Rev
Custom	Bradstreet		<RevCode>
Date:	Wednesday, April 28, 2010	Sheet 27 of 53	

Expansion Board Conn

del 48MHZ termination R&C
2008-03-21

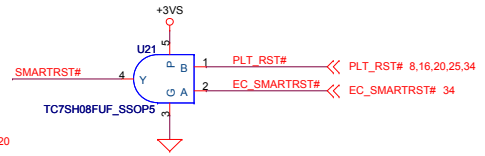
0.4A each pin
2008-04-07



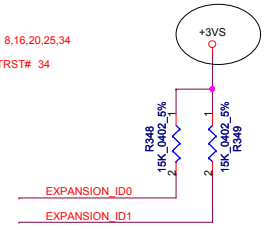
ACES_88072-4071
conn@

need update the CIS symbol
Foot print update OK
0416

Need come out a solution for CLK_48M_SMC signal
once no Smart-Card inserted.
11-03

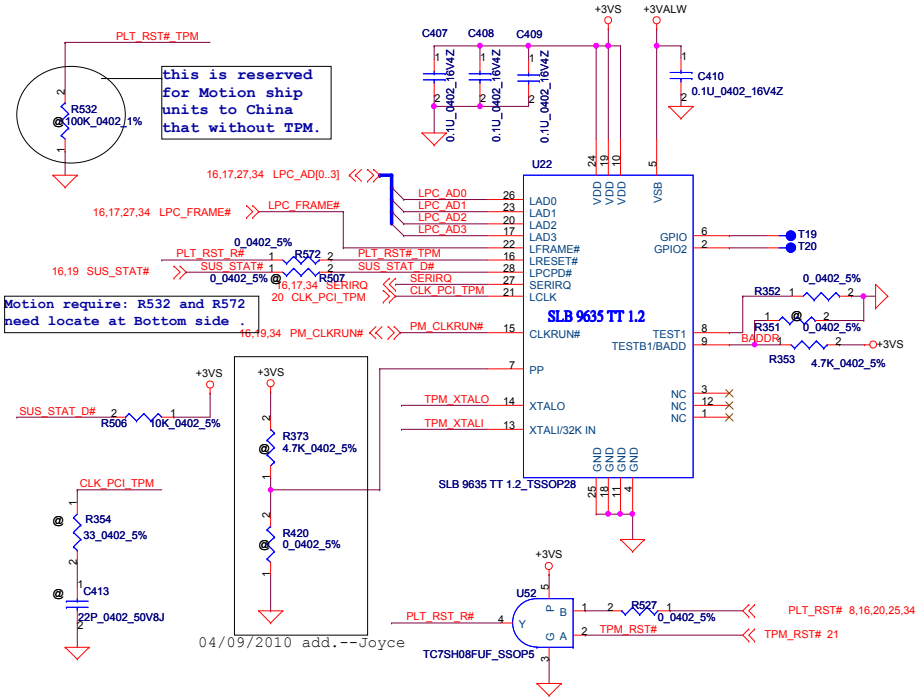


Changed from +3valw to +3vs
according to PCH EDS. 01/20



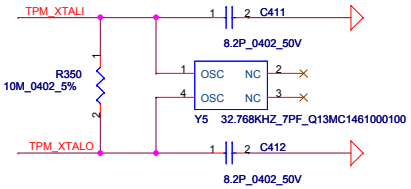
EXPANSION_ID0	EXPANSION_ID1	IO Expansion Type
1	1	No any card
1	0	Smart Card + Express Card
0	1	Reserver
0	0	Reserver

TPM



04/09/2010 add.--Joyce

Base I/O Address
0 = 02Eh
*1 = 04Eh(Default)



Title	Expansion, TPM		
Size	Custom	Document Number Bradstreet	Rev <RevCode>
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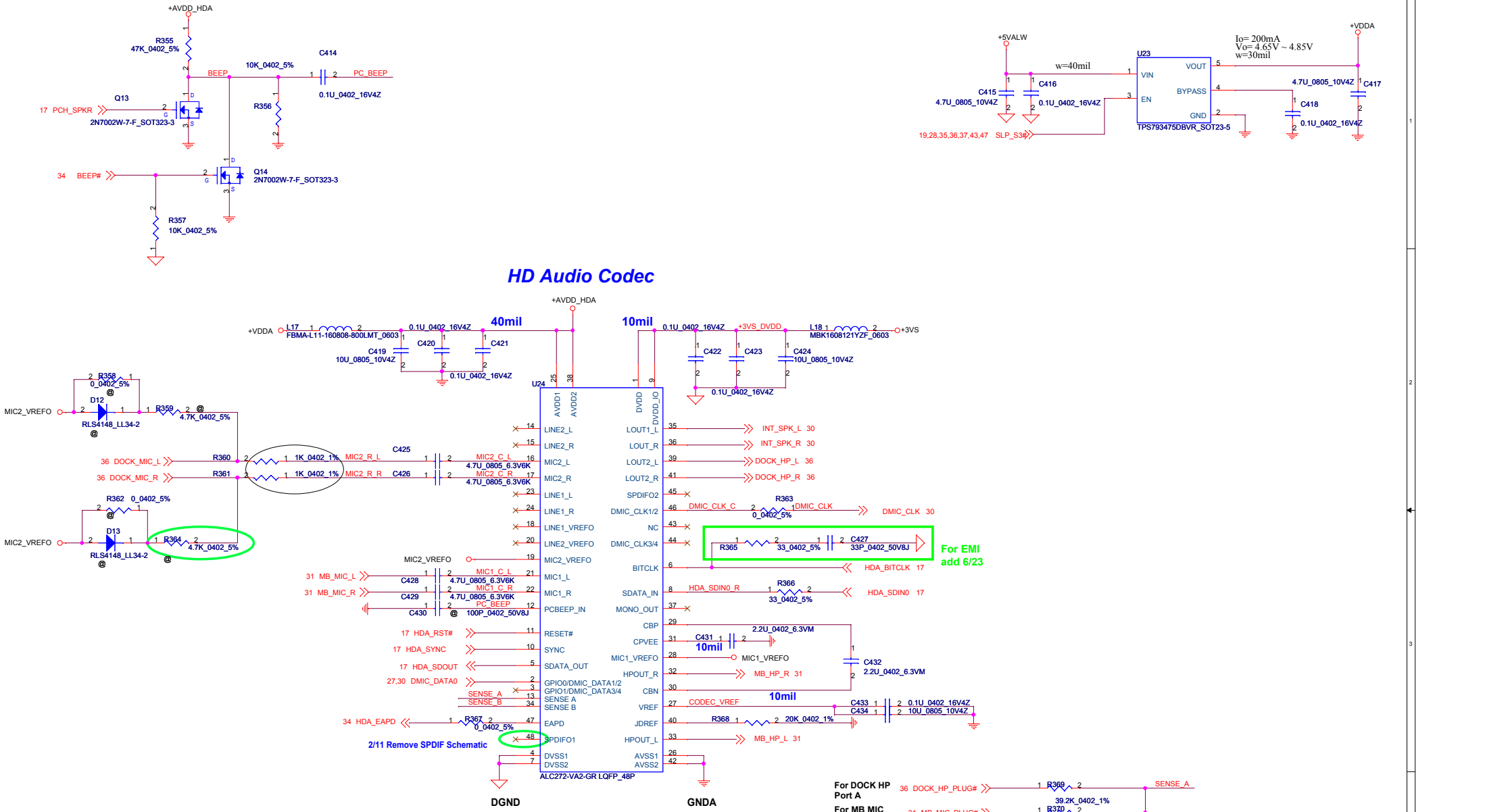
HD Audio Codec



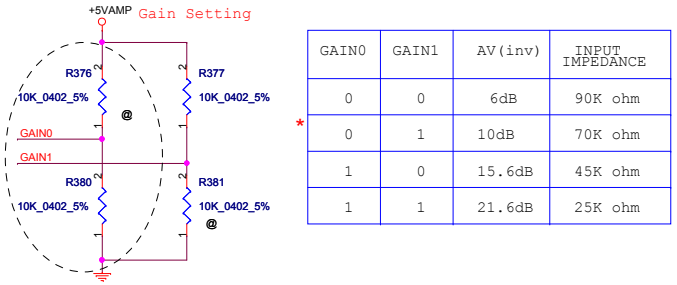
SENSE PIN	Inpedance	Codec Signals	Function
SENSE A	39.2K	PORT A (PIN 41,39)	DOCK HP
	20k	PORT B (PIN 21,22)	MB MIC
	5.1K	PORT D (PIN 35,36)	Speaker
SENSE B	20k	PORT F (PIN 16,17)	DOCK MIC
	5.1K	PORT I (PIN 32,33)	MB HP

Compal Electronics, Inc.(KunShan)

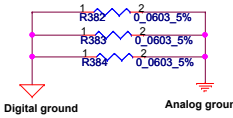
Title: Realtek ALC272 Codec

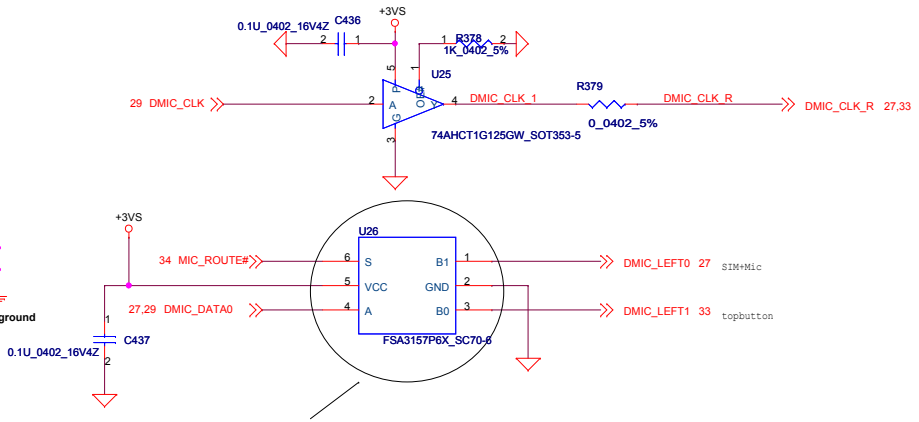
Size: Custom | Document Number: NVX00 LA-6111P | Rev: 0.1

Date: Wednesday, April 28, 2010 | Sheet 29 of 53



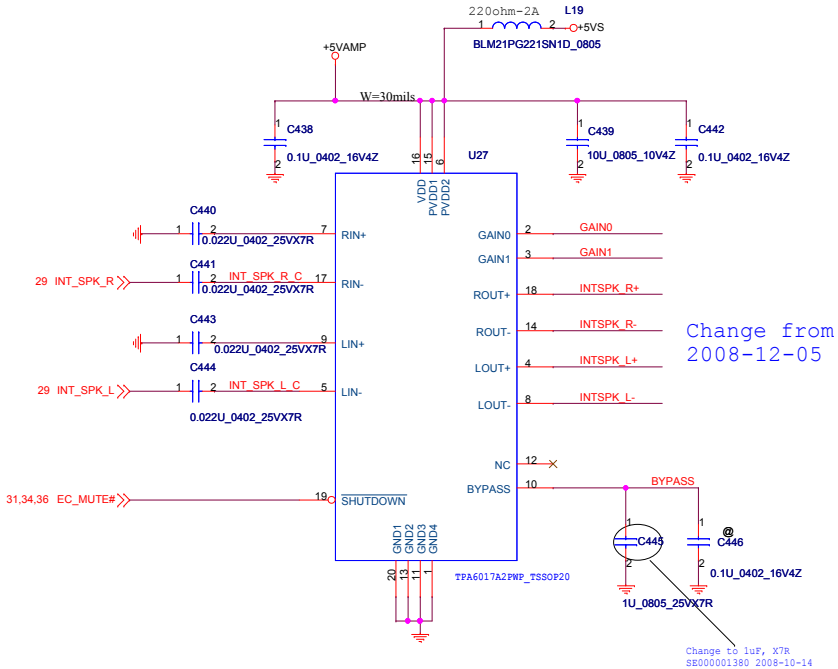
GAIN0	GAIN1	AV(inv)	INPUT IMPEDANCE
0	0	6dB	90K ohm
0	1	10dB	70K ohm
1	0	15.6dB	45K ohm
1	1	21.6dB	25K ohm





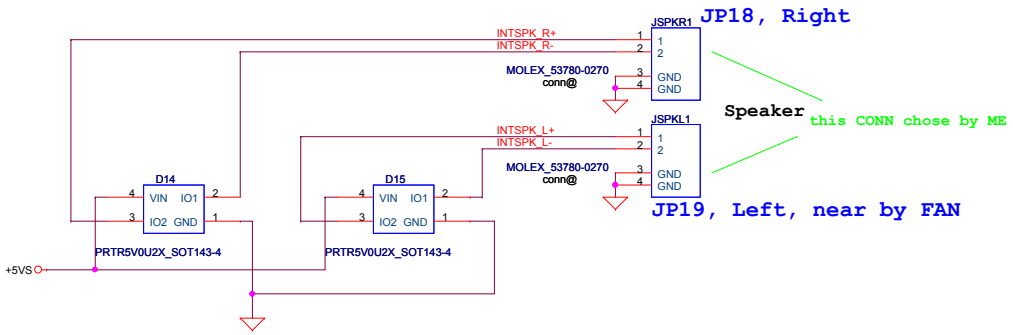
Change to SA731157010
2008-05-26

SEL	
0	B0
1	B1 *



Change from SA601720010 to SA000016Y10
2008-12-05

this CONN chose by ME



Compal Electronics, Inc.(KunShan)
Title: IDT 92HD71B7 Amp&Jack
Size: Custom
Document Number: Bradstreet-
Rev: 0.01
Date: Wednesday, April 28, 2010
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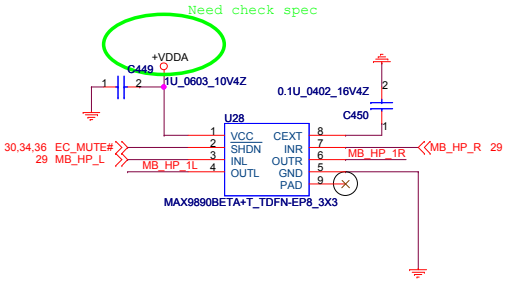
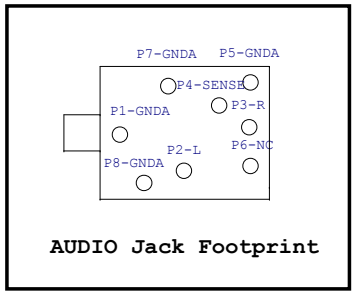
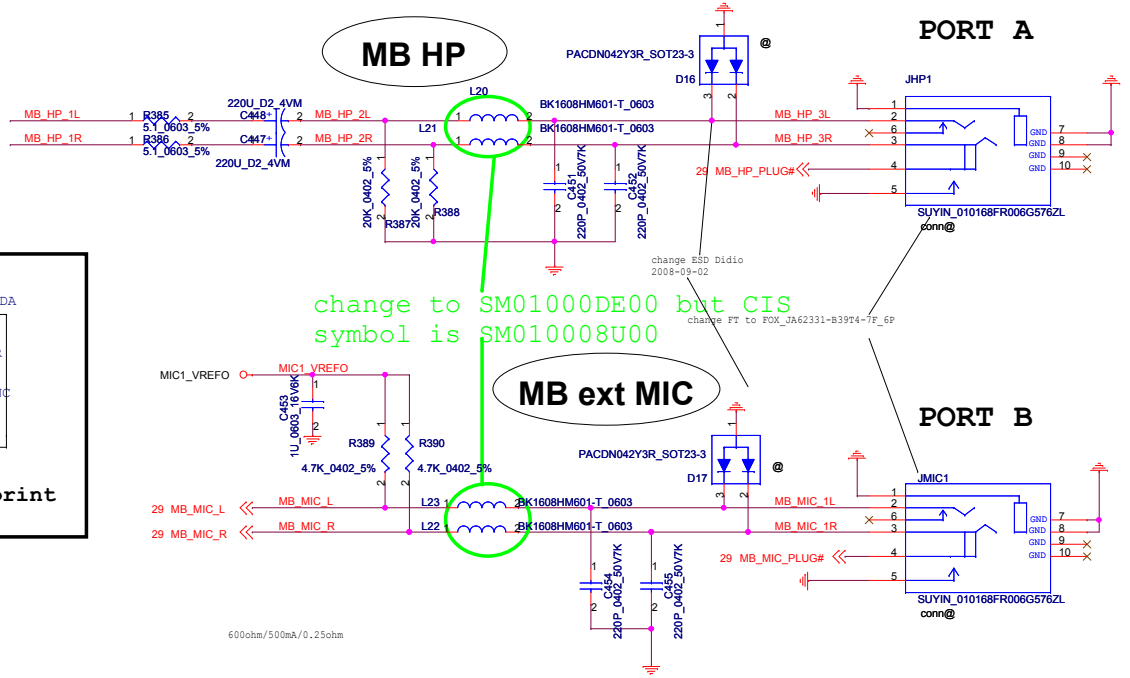
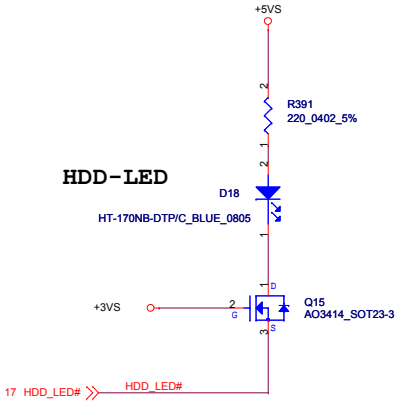
AUDIO JACK







LED



Follow Bill command to delete the LED brightless controller circuit.
1-19

Need double check the signal type.

Title: LED		
Size: Custom	Document Number: Bradstreet	Rev: <RevCode>
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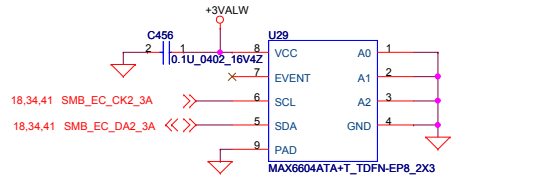
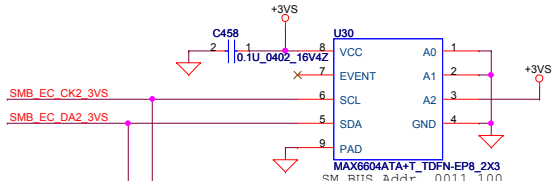
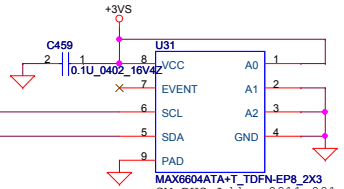
Thermal Sensor



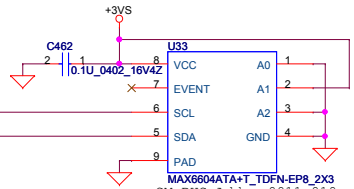
SM BUS Addr. 0011 000
Thermal Sensor for charger



SM BUS Addr. 0011 100
Thermal Sensor for PCH

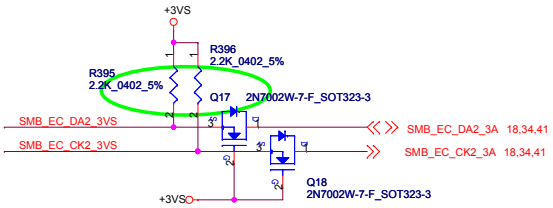


SM BUS Addr. 0011 001
Thermal Sensor for CPU



SM BUS Addr. 0011 010
Thermal Sensor for SO-DIMMs

DVT

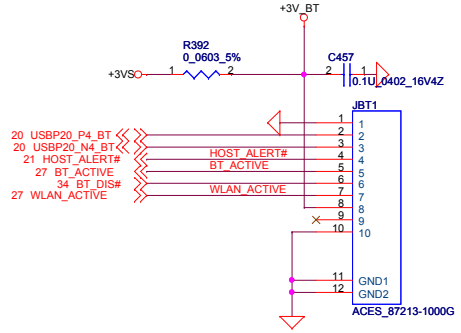


Blue Tooth

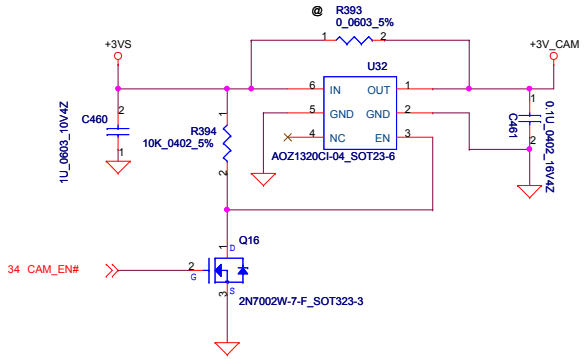
USI BT solution

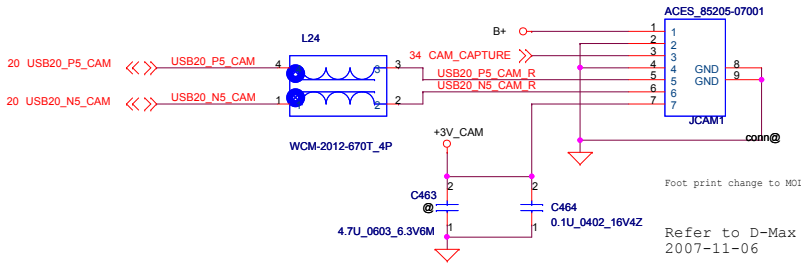
Delete +3V_BT power switch.
2007-11-15

	MB signal		new BT signal
1	GND	1	GND
2	USB+	2	USB+
3	USB-	3	USB-
4	HOST_ALERT#	4	BT_ACTIVE(PIO5)
5	BT_ACTIVE	5	BT_Priority/Ch_Clk(PIO4)
6	HW_RADIO_DIS#	6	HW_RADIO_DIS#(PIO3)
7	WLAN_ACTIVE	7	WLAN_ACTIVE/Ch_Data(PIO6)
8	+3.3V	8	+3.3V
9	NC	9	LED(PIO7)
10	GND	10	GND



Camera





Foot print change to MOLEX_53398-0571_5P

Refer to D-Max GD-5253 SPEC.
2007-11-06

Title	Thermal Sensor		
Size	Document Number		Rev
Custom	Bradstreet		<RevCode>
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Finger Printer

change to LCD MOS?

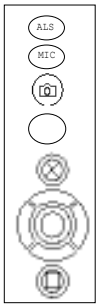
1:D
2:G
3:S

Side button

JSBTN1
ACES_87213-1400G

20 USB20_N3_FRP
20 USB20_P3_FRP
34 PWR_LED
35 ON/OFFBTN#
+5VALW
+3V_FPR
34 SASBTN#
34 LED_PWM
34 CHARGE_LED
34 BATT_LED
PWR_LED
ON/OFFBTN#
SASBTN#
LED_PWM
CHARGE_LED
BATT_LED

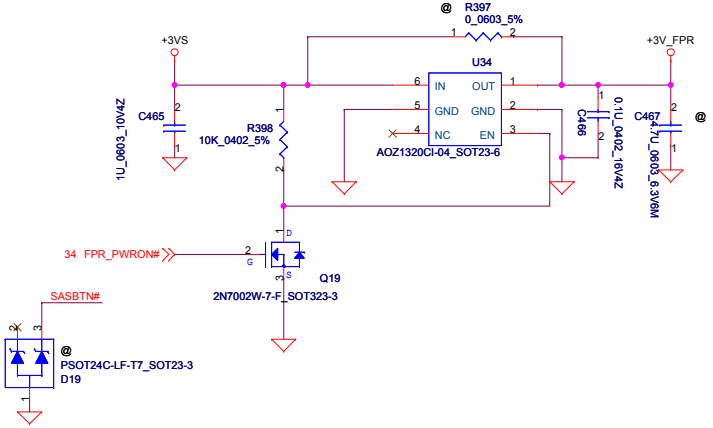
Top side Board Connect to M/B



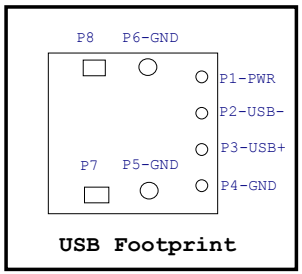
J5WAY1
ACES_88512-1641
conn@

+3VALW
+3VS
34 DASH#
34 ESCAPE#
34 RIGHT#
34 UP#
34 ENTER#
34 DOWN#
34 LEFT#
34 USER1#
34 CAMERA#
ALS_SMBDATA
ALS_SMBCLK
27,30 DMIC_CLK_R
30 DMIC_LEFT1
DMIC_CLK_R
DMIC_LEFT1

ALS SM BUS address: 0111 001
01/27/2010 Joyce

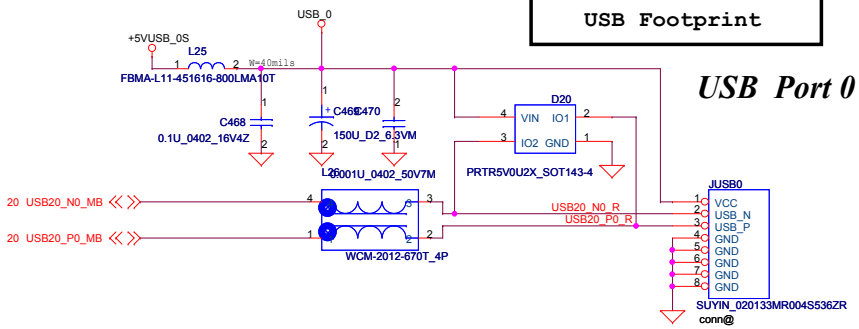


17,34 SMB_EC_DA1_3VS
17,34 SMB_EC_CK1_3VS
6,8,13,14,27 D_CK_SDATA
6,8,13,14,27 D_CK_SCLK
R557 0_0402_5%
R558 0_0402_5%
@R559 0_0402_5%
@R560 0_0402_5%
ALS_SMBDATA
ALS_SMBCLK



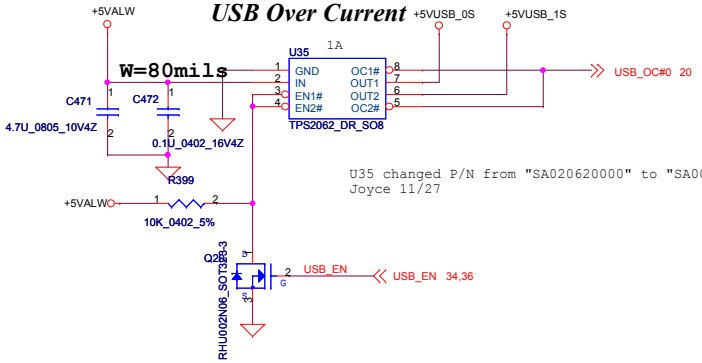
USB Footprint

USB Port 0

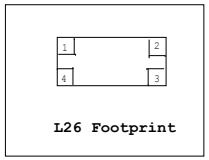


USB ON MB

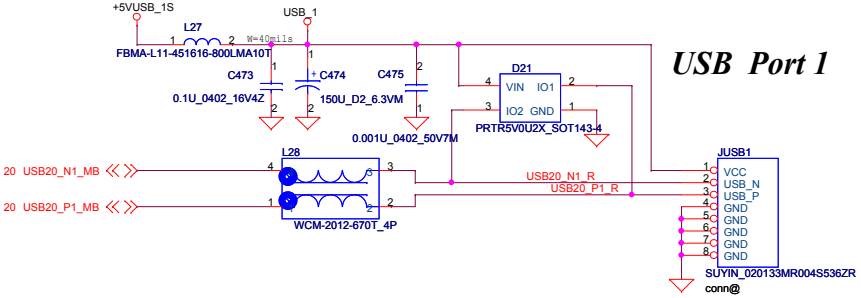
USB Over Current



U35 changed P/N from "SA020620000" to "SA00002AS00".
Joyce 11/27

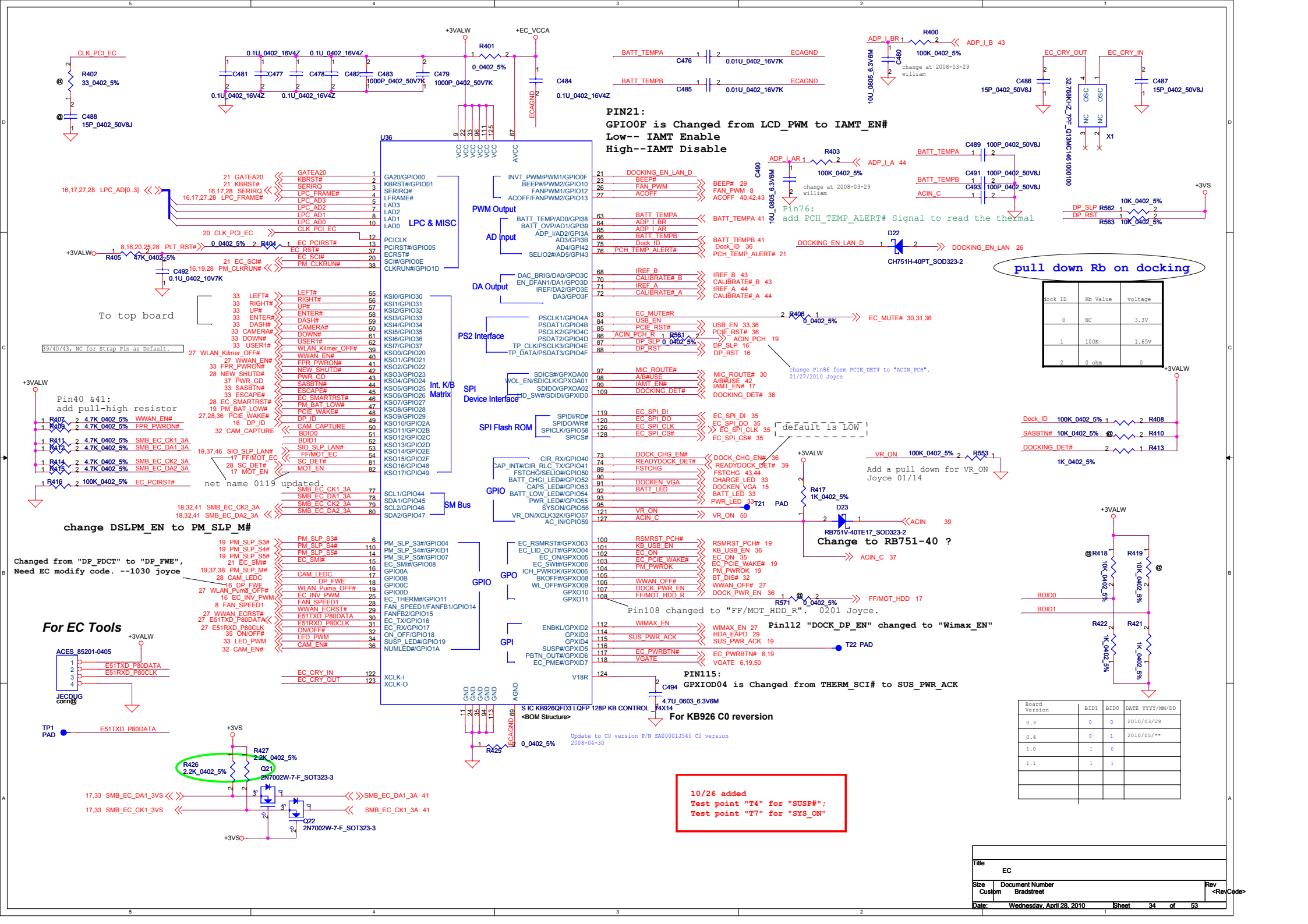


L26 Footprint



USB Port 1

Title	FRP/IO/BTN/Wireless-SW	
Size: Custom	Document Number: Bradstreet	Rev: <RevCode>
Date: Wednesday, April 28, 2010	Sheet 33 of 53	


U36
PIN21:
GPIO0F is Changed from LCD_PWM to IAMT_EN#
Low-- IAMT Enable
High--IAMT Disable
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
GPIO
GPI
LPC & MISC
Int. K/B Matrix
SM Bus
Pin76:
add PCH_TEMP_ALERT# Signal to read the thermal
pull down Rb on docking
Dock ID | Rb Value | voltage
0 | NC | 3.3V
1 | 100K | 1.65V
2 | 0 ohm | 0
To top board
Pin40 &41:
add pull-high resistor
change DSLPM_EN to PM_SLP_M#
Changed from "DP_PDCT" to "DP_FWE",
Need EC modify code. --1030 joyce
net name 0119 updated.
default is LOW
Add a pull down for VR_ON
Joyce 01/14
Change to RB751-40 ?
Pin108 changed to "FF/MOT_HDD_R". 0201 Joyce.
Pin112 "DOCK_DP_EN" changed to "Wimax_EN"
PIN115:
GPXIOD04 is Changed from THERM_SCI# to SUS_PWR_ACK
For KB926 C0 reversion
For EC Tools
10/26 added
Test point "T4" for "SUSP#";
Test point "T7" for "SYS_ON"
Title
EC
Size Custom
Document Number Bradstreet
Rev
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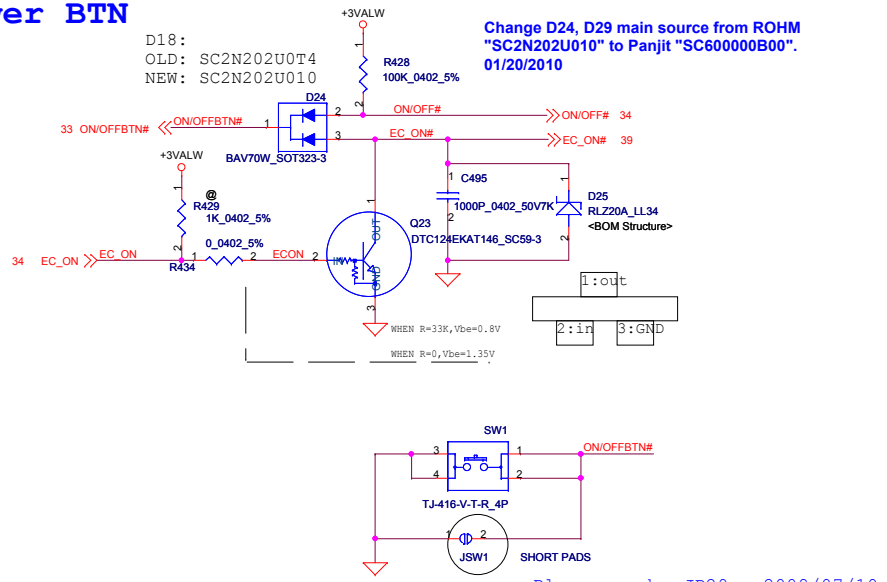
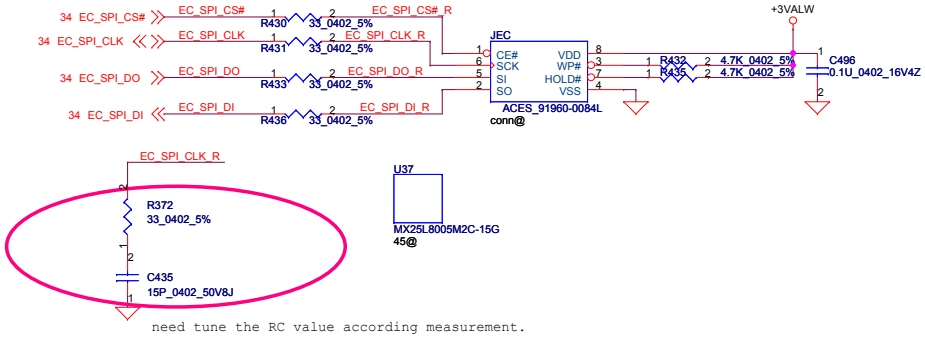
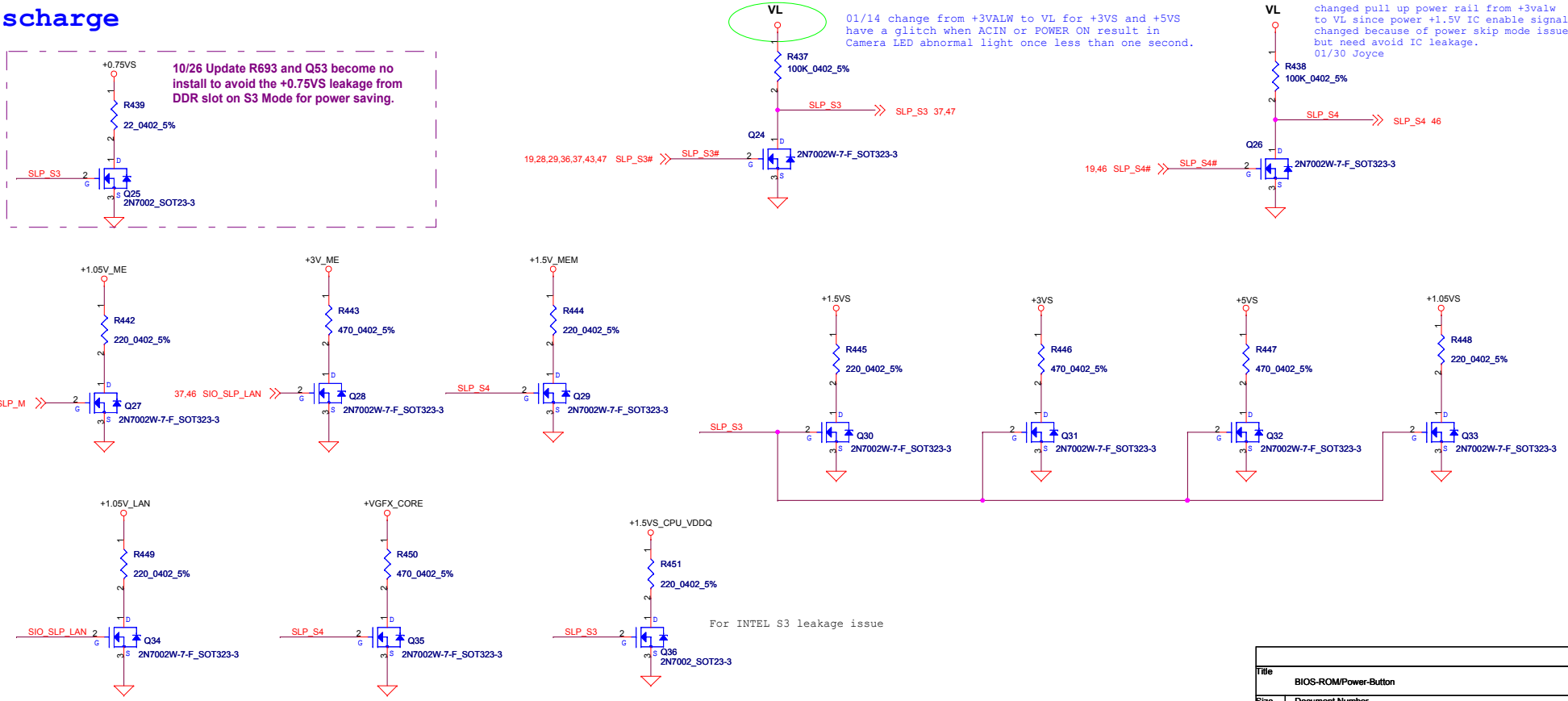
Power BTN



BIOS-ROM/SPI



Discharge



Title	BIOS-ROM/Power-Button	
Size: Custom	Document Number: Bradstreet	Rev: <RevCode>
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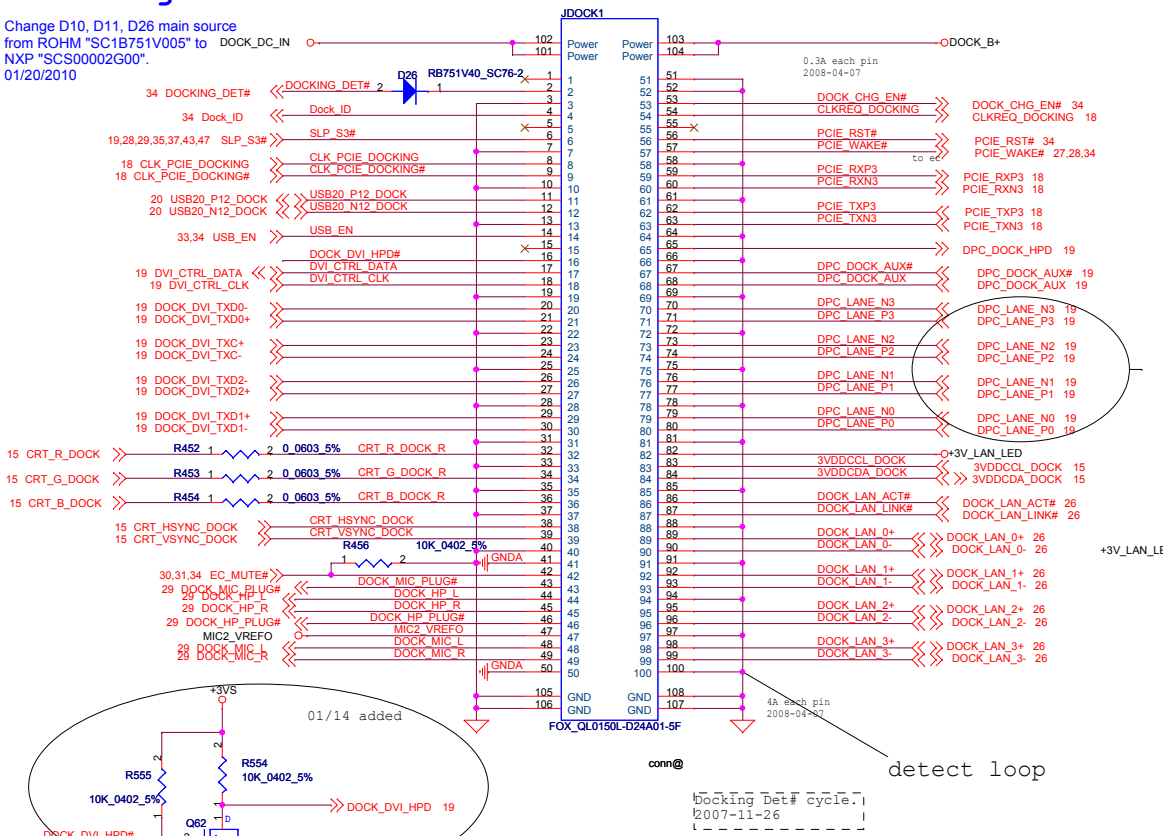
Docking Connecter

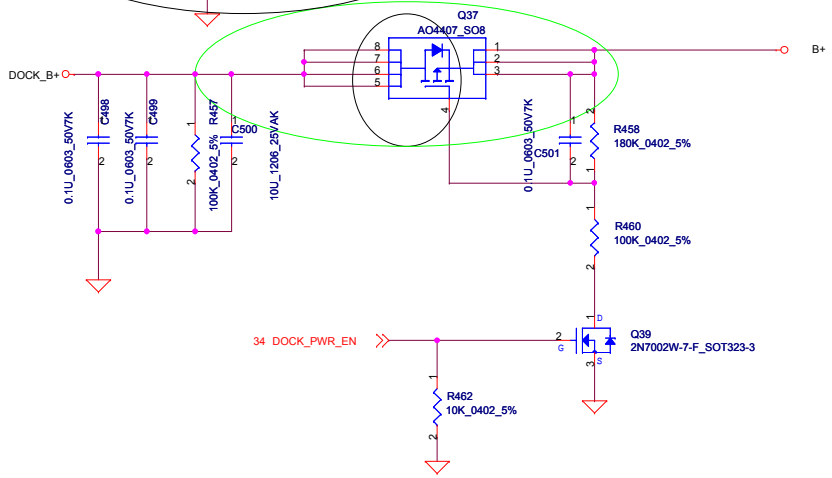
KeyBoard Connecter

Change D10, D11, D26 main source from ROHM "SC1B751V005" to NXP "SCS00002G00". 01/20/2010

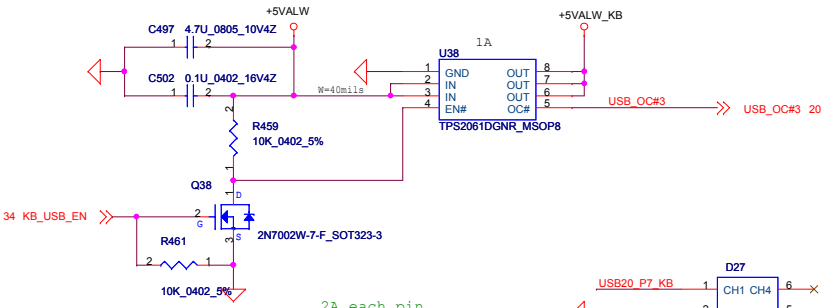
Dock ON, ---------"0"
UN-PLUG,--------"1"
Pull high on Docking

ESD DIODE will add on the Docking bridge board.



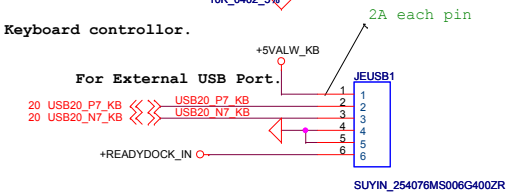


need change follow power's suggestion
2007/12/19

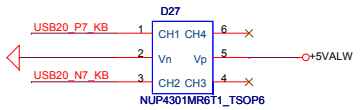


For Keyboard controllor.

For External USB Port.



Pogo Connector



Title	Dock Conn/Keyboard Conn	
Size: CustomBradstreet	Document Number	Rev: <RevCode>
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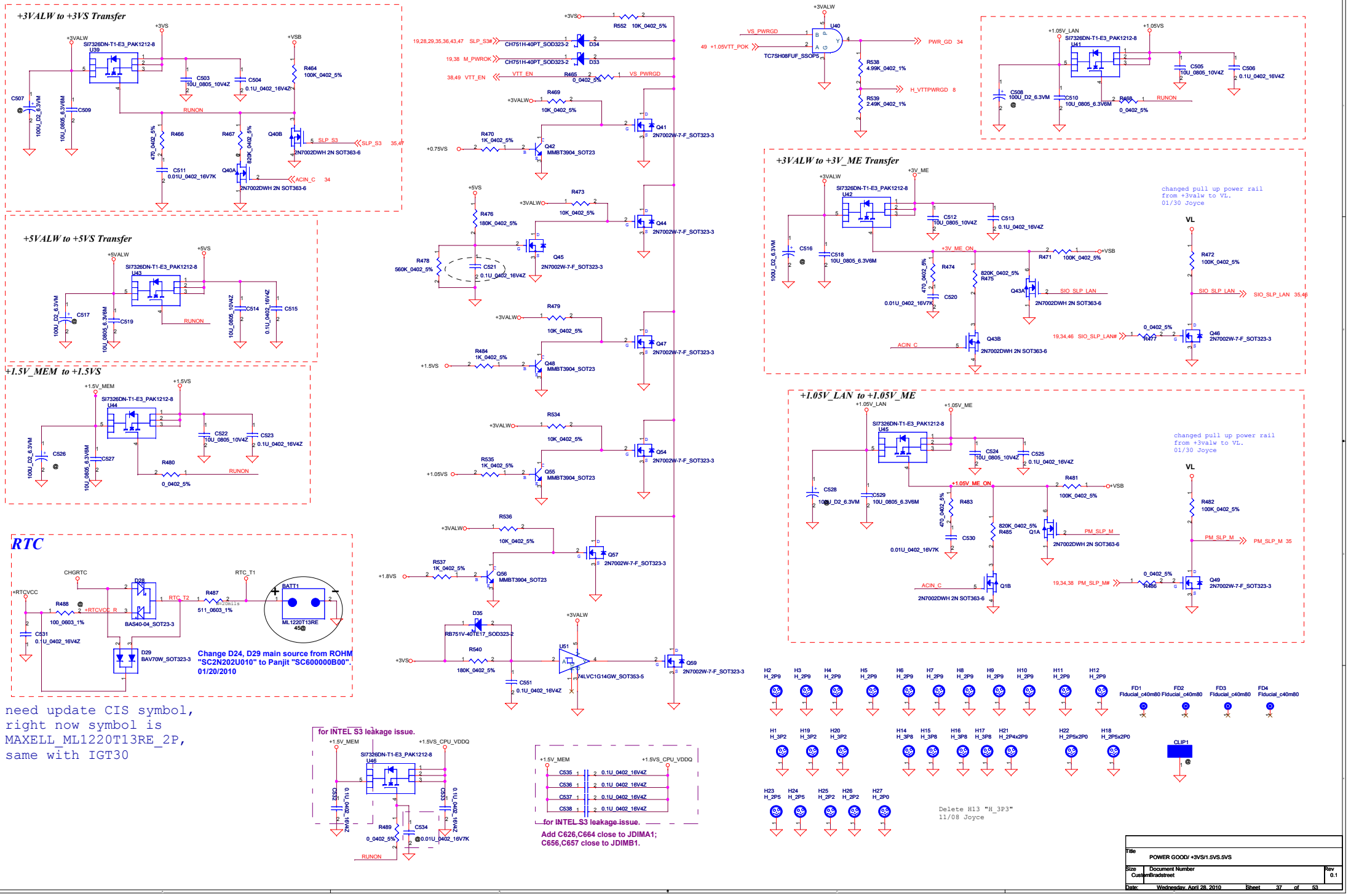
+3VALW to +3VS Transfer
+5VALW to +5VS Transfer
+1.5V_MEM to +1.5VS
RTC
Change D24, D29 main source from ROHM "SC2N202U010" to Panjit "SC600000B00". 01/20/2010
need update CIS symbol, right now symbol is MAXELL_ML1220T13RE_2P, same with IGT30
for INTEL S3 leakage issue.
Add C626,C664 close to JDIMA1; C656,C657 close to JDIMB1.
+3VALW to +3V_ME Transfer
changed pull up power rail from +3valw to VL. 01/30 Joyce
+1.05V_LAN to +1.05V_ME
changed pull up power rail from +3valw to VL. 01/30 Joyce
Delete H13 "H_3P3" 11/08 Joyce
Title
POWER GOOD/ +3VS/1.5VS.5VS
Size
Custom
Document Number
Bradstreet
Rev
0.1
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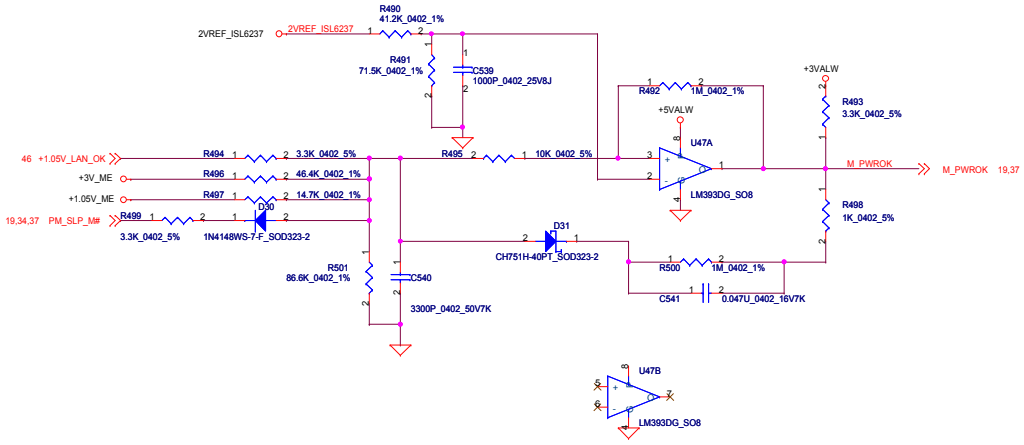
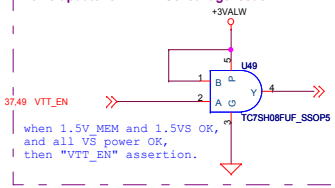
53



10/28 update for INTEL S3 leakage issue.



Title	CPU_CORE	
Size C	Document Number Bradstreet 1.5	Rev <RevCode>
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DC301005580

PJPDC1
SINGA_2DW-0005-B03
conn@

DC_IN_S1
PL1
FBMA-L11-322513-151LMA50T_1210
DC_IN_S2
PC1 1000P_0402_50V7K
PC2 100P_0402_50V8J
PC3 1000P_0402_50V7K
PC4 100P_0402_50V8J

DOCK_DC_IN
PD1 B540C_SMC
PD2 B540C_SMC
DC_IN
VIN

+READYDOCK_IN
PD3 SBR3A40SA-13_SMA2
PR3 340K_0402_1%
PR4 100K_0402_5%
+3VALW
PR2 100K_0402_5%
READYDOCK_DET#
PQ2 2N7002W-T/R7_SOT323-3
PQ1 2N7002W-T/R7_SOT323-3
PR1 100K_0402_5%
38W/50W# 43,44

BATT_A
BATT_B
PD4 LL4148_LL34-2
PD6 LL4148_LL34-2
PD5 LL4148_LL34-2
1538VCC
PQ3 TP0610K-T1-E3_SOT23-3
PR5 68_1206_5%
PR6 68_1206_5%
PR7 200_0603_5%
CHGRTCP
PR8 100K_0402_1%
PC5 0.22U_0603_25V7K
PC6 0.1U_0603_25V7K
35 EC_ON#
PR9 22K_0402_1%
VS

RTCVREF
PR10 200_0603_5%
PR11 560_0603_5%
PR12 560_0603_5%
3.3V
CHGRTC
PU1 G920AT24U_SOT89-3
OUT
IN
GND
PC7 10U_0805_10V4Z
PC8 1U_0805_25V4Z

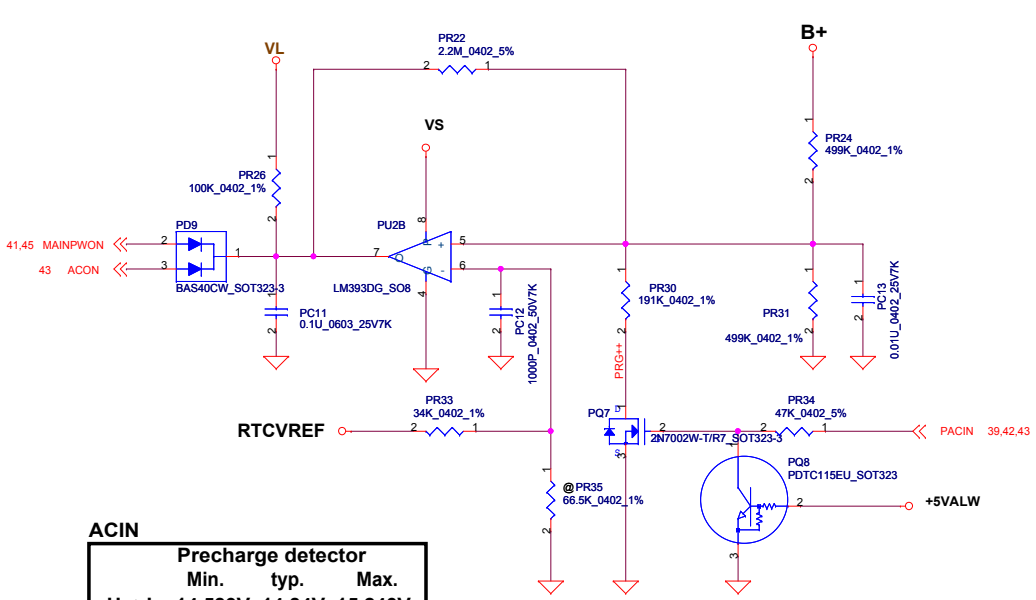
PJ1 JUMP_43X118 +3VALWP +3VALW (4.1A,180mils ,Via NO.= 9)
PJ3 JUMP_43X118 +5VALWP +5VALW (4.6A,220mils ,Via NO.= 10)
PJ4 JUMP_43X39 +VSBP +VSB (120mA,20mils ,Via NO.= 1)
PJ7 JUMP_43X118 +1.05V_LANP +1.05V_LAN (6A,280mils ,Via NO.= 12)
PJ9 JUMP_43X118 +1.05VTTP
PJ11 JUMP_43X118 +1.05VTT (12A,640mils ,Via NO.=28)
PJ2 JUMP_43X79 +1.8VSP +1.8VS (1.3A,60mils ,Via NO.= 3)
PJ5 JUMP_43X79 +0.75VSP +0.75VS (1A,40mils ,Via NO.= 3)
PJ6 JUMP_43X118
PJ8 JUMP_43X118 +1.5VP +1.5V_MEM (8.5A,380mils ,Via NO.=19)
PJ10 JUMP_43X118
PJ12 JUMP_43X118 +VGFX_COREP +VGFX_CORE (11A,600mils ,Via NO.=28)

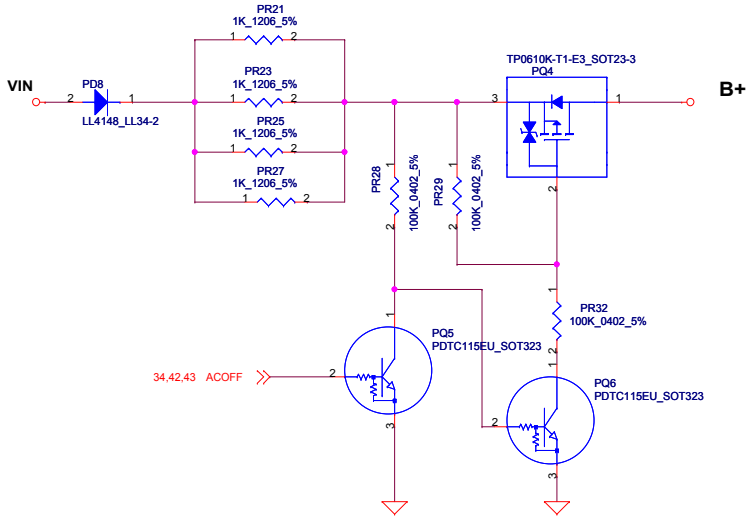
VIN
PR13 1M_0402_1%
PR14 84.5K_0402_1%
PR17 22K_0402_1%
PR18 20K_0402_1%
PC9 1000P_0402_50V7K
PC10 0.1U_0402_16V7K
PU2A LM393DG_SO8
PR20 10K_0402_5%
RTCVREF
3.3V
PR15 10K_0402_5%
PR16 0_0402_5%
ACIN 34
PACIN 40,42,43
GLZ4.3B_LL34-2 PD7
PR19 10K_0402_1%

Vin Detector(080704)

	Min	Tyb	Max
H-L	16.61	17.234	17.713
L-H	17.430	17.901	18.384

Title	DC-IN	
Size	Document Number Bradstreet 1.5	Rev <RevCode>
Date: Wednesday, April 28, 2010	Sheet 39 of 52	





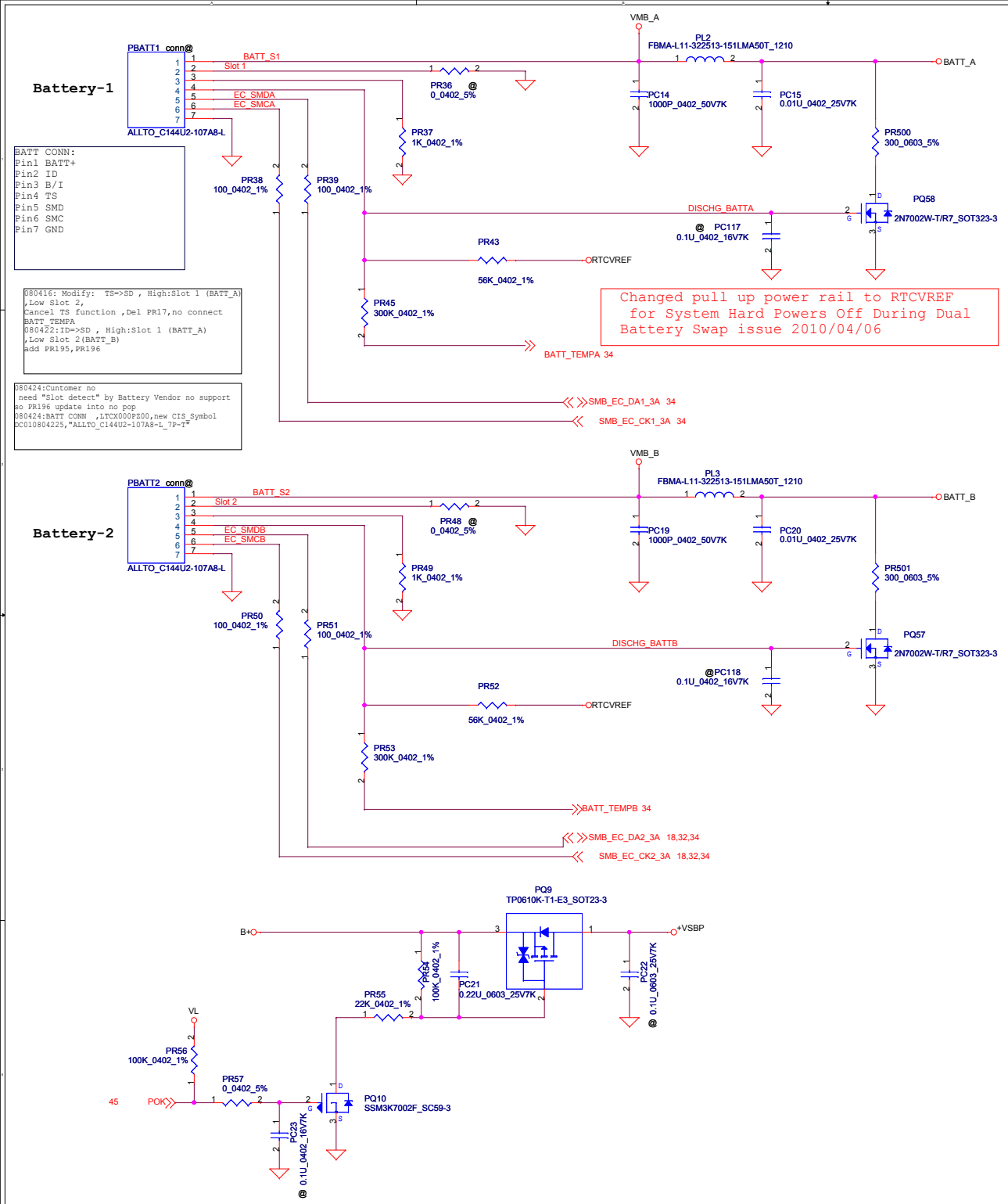
ACIN

Precharge detector			
	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector			
	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

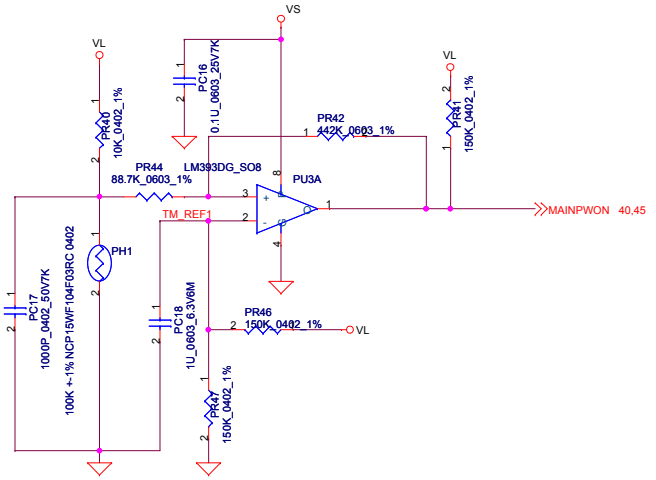
Title	PRECHARGE	
Size	Document Number Bradstreet 1.5	Rev <RevCode>
Date:	Wednesday, April 28, 2010	Sheet 40 of 52



PH1 under CPU botten side :

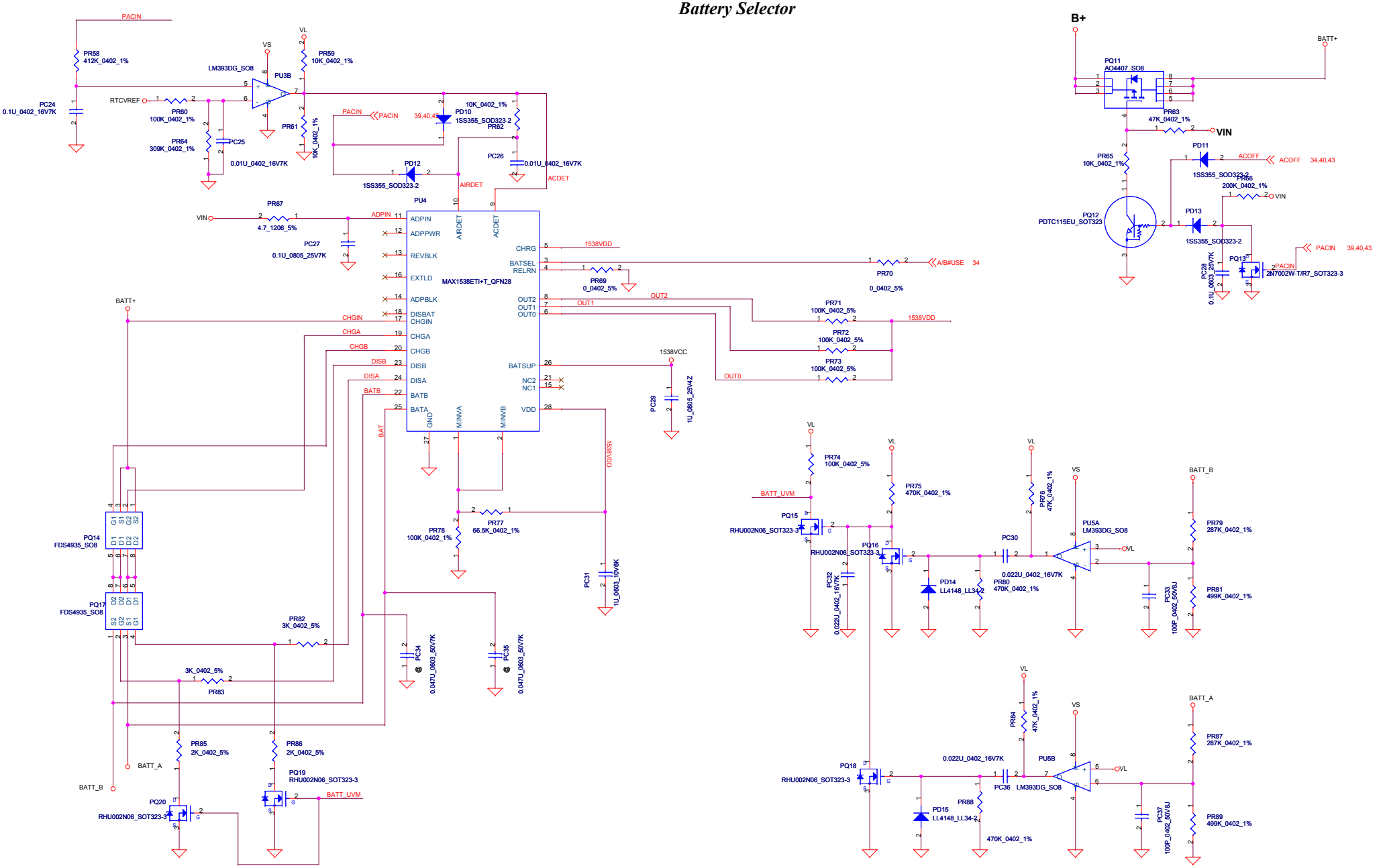
CPU thermal protection at 92 degree C

Recovery at 70 degree C



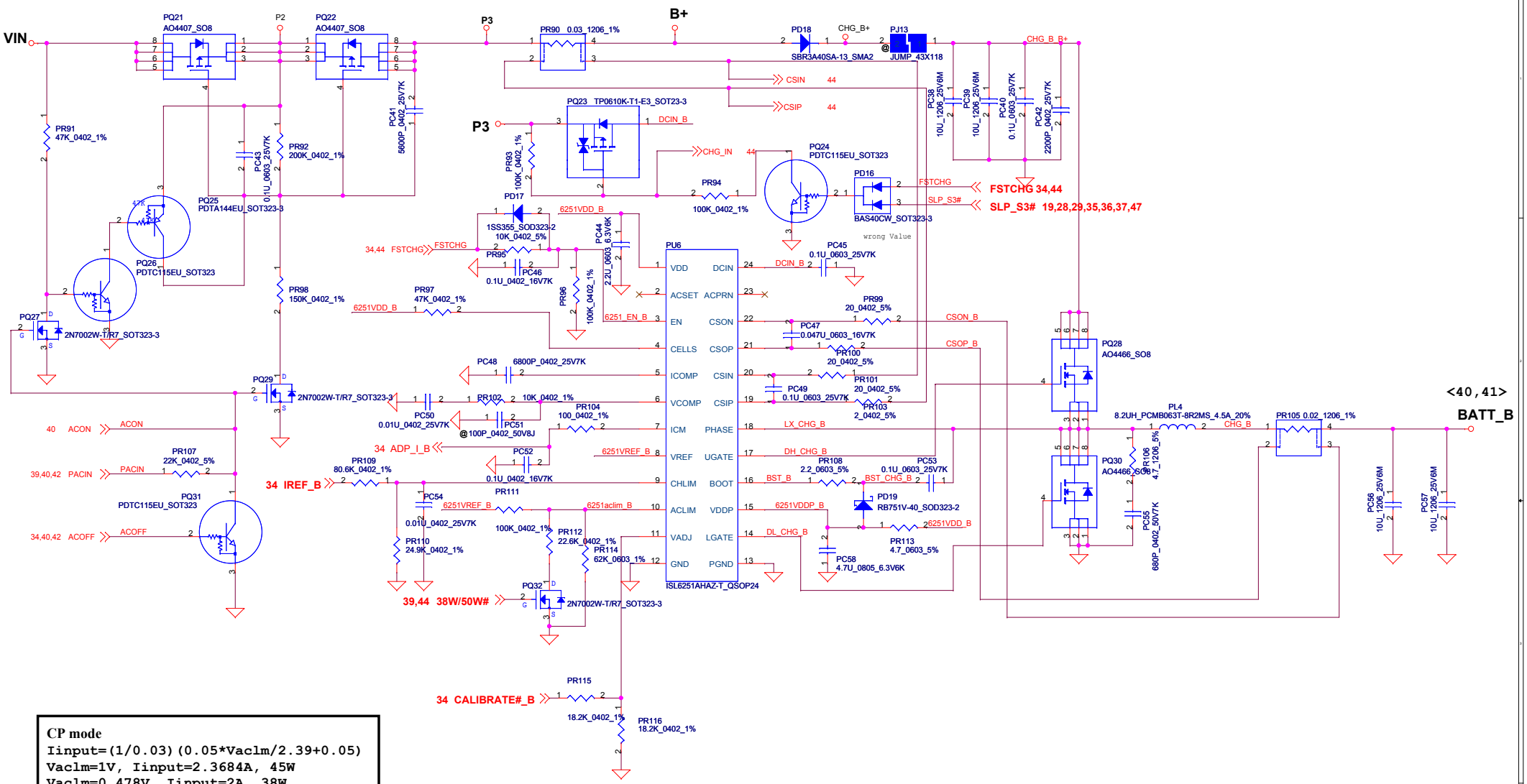
Title	BATT-CONN/OTP/DC-DETECT	
Size	Document Number Bradstreet 1.5	Rev <RevCode>
Date: Wednesday, April 28, 2010	Sheet 41 of 52	

Battery Selector



Iada=0~3.42A(65W/19V=3.42A)

CP = 45W ; CP point= 2.3684A



CP mode

Iinput=(1/0.03)(0.05*Vaclm/2.39+0.05)

Vaclm=1V, Iinput=2.3684A, 45W

Vaclm=0.478V, Iinput=2A, 38W

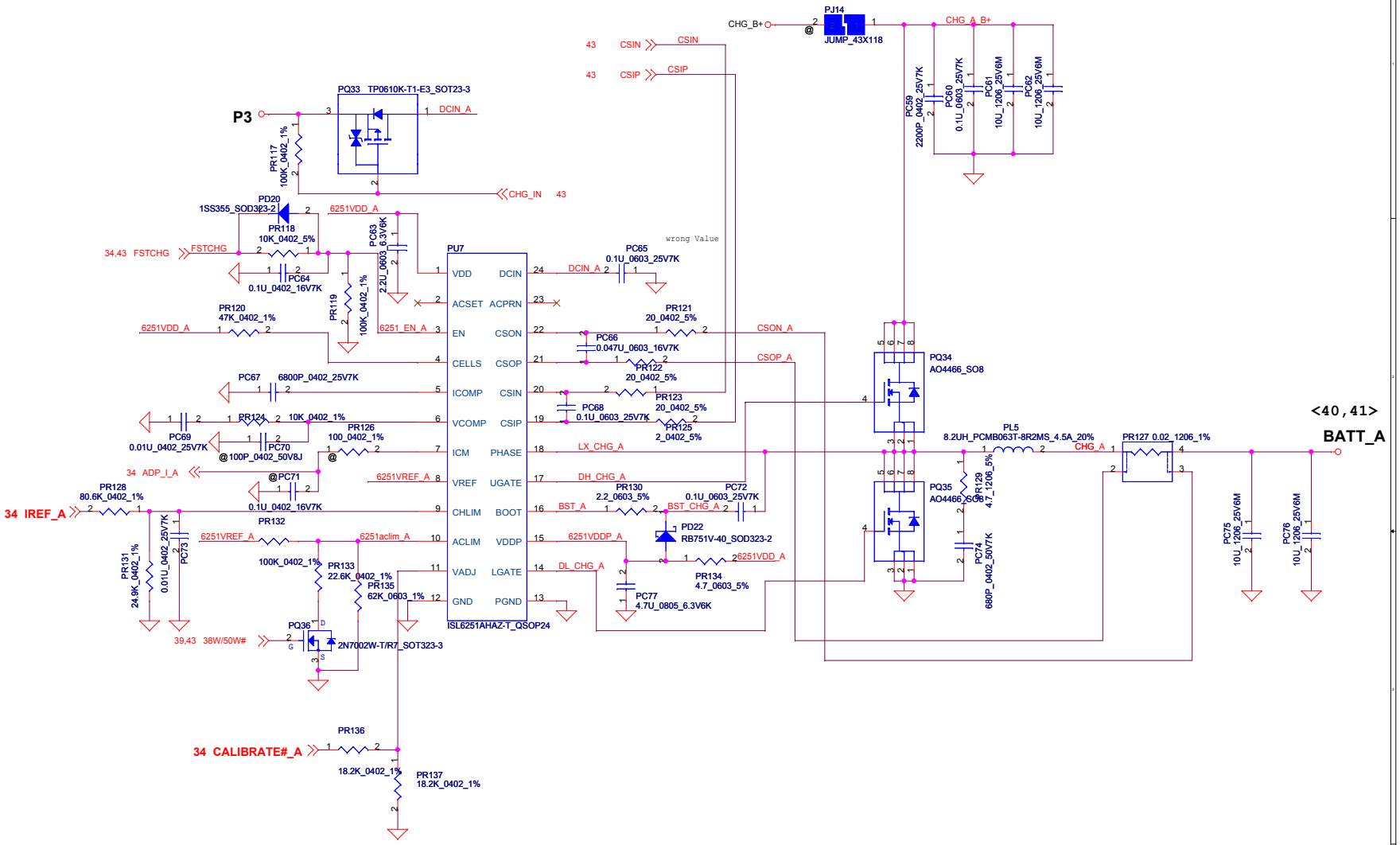
CC=0.5~1.3A(0.65C)

IREF=1.695*Icharge

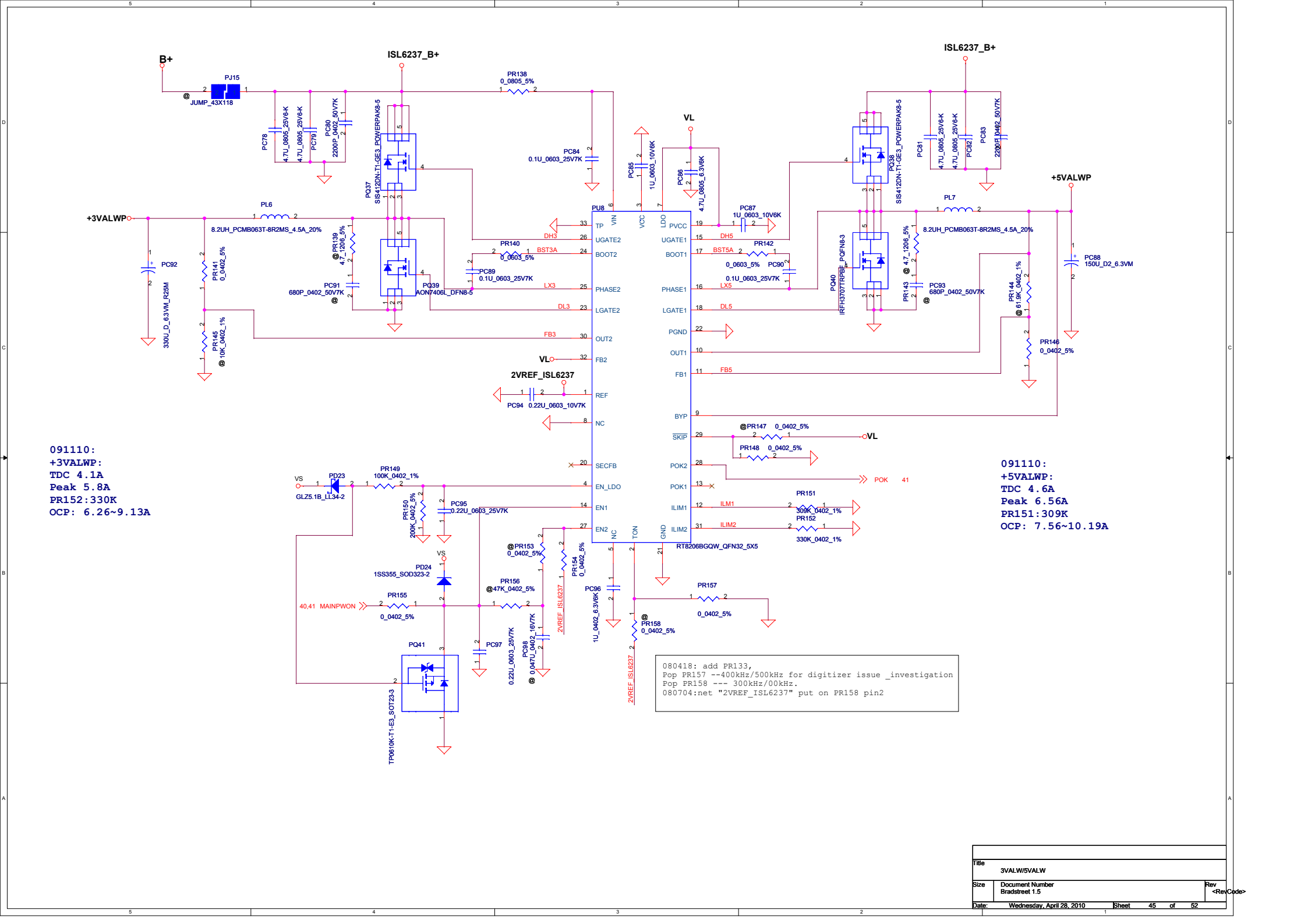
IREF=0.847V~2.2V

Li-ion battery, 103450 size, 4S LI-ON cells, 2000mAH/3.7V

Title	CHARGE B	
Size	Document Number Bradstreet 1.5	Rev <RevCode>
Date: Wednesday, April 28, 2010	Sheet 43 of 52	



Title	CHARGE A	
Size	Document Number Bradstreet 1.5	Rev <RevCode>
Date:	Wednesday, April 28, 2010	Sheet 44 of 52



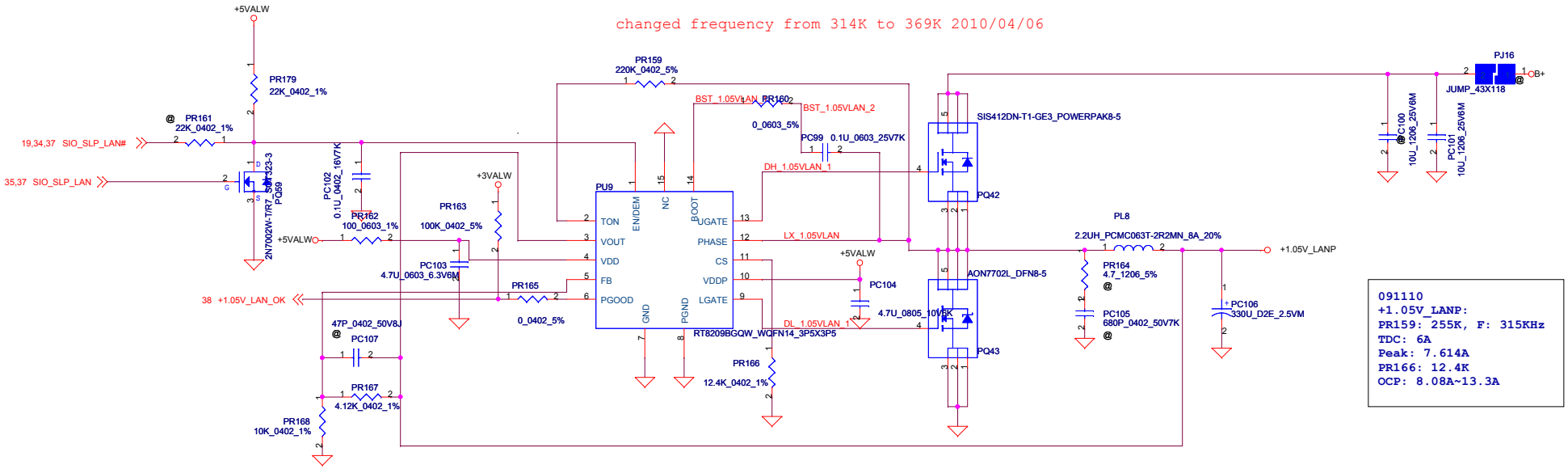
091110:
+3VALWP:
TDC 4.1A
Peak 5.8A
PR152:330K
OCP: 6.26~9.13A

091110:
+5VALWP:
TDC 4.6A
Peak 6.56A
PR151:309K
OCP: 7.56~10.19A

080418: add PR133,
Pop PR157 --400kHz/500kHz for digitizer issue _investigation
Pop PR158 --- 300kHz/00kHz.
080704:net "2VREF_ISL6237" put on PR158 pin2

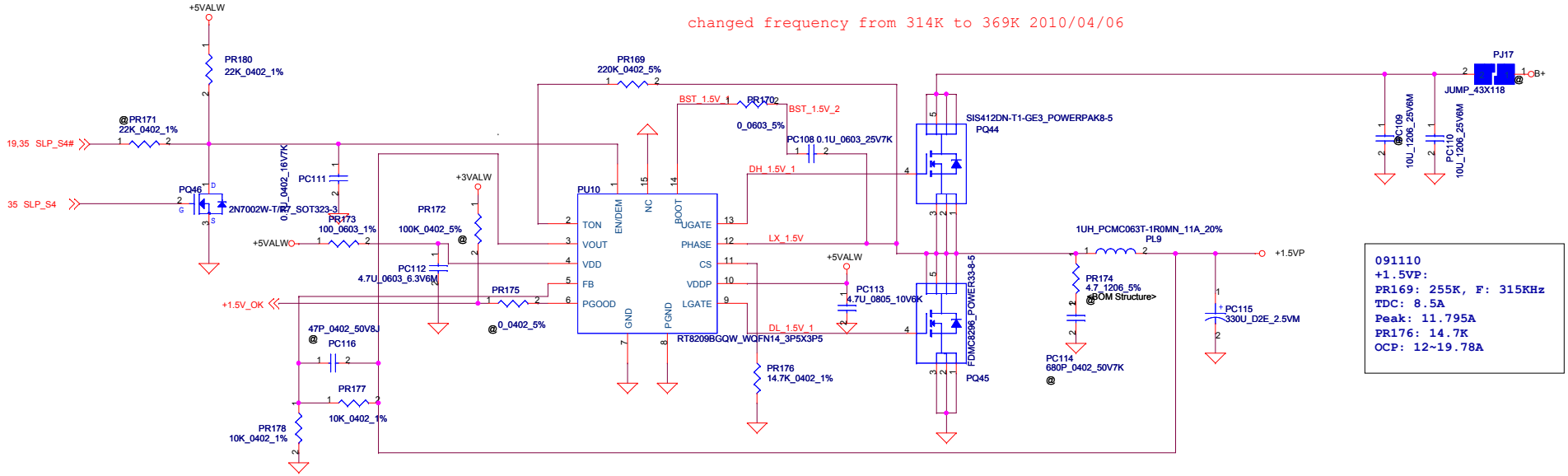
Title	3VALW/5VALW	
Size	Document Number Bradstreet 1.5	Rev <RevCode>
Date: Wednesday, April 28, 2010	Sheet 45 of 52	

changed frequency from 314K to 369K 2010/04/06



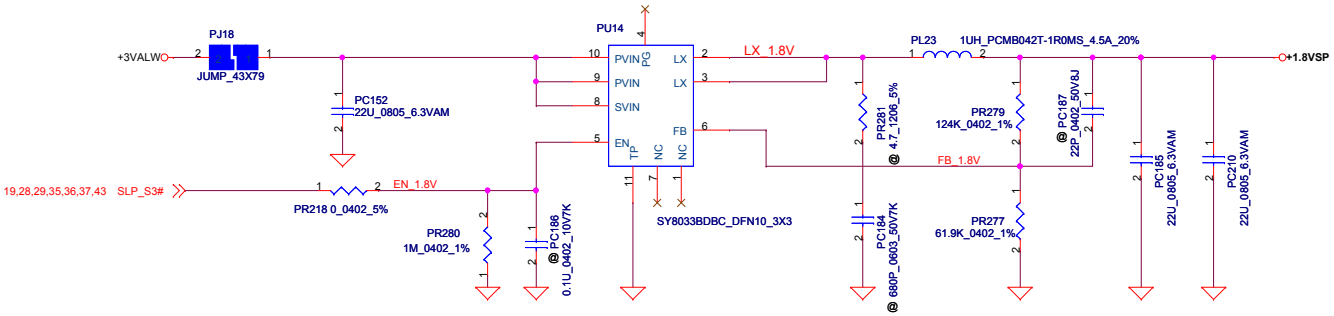
091110
+1.05V_LANP:
PR159: 255K, F: 315KHz
TDC: 6A
Peak: 7.614A
PR166: 12.4K
OCP: 8.08A~13.3A

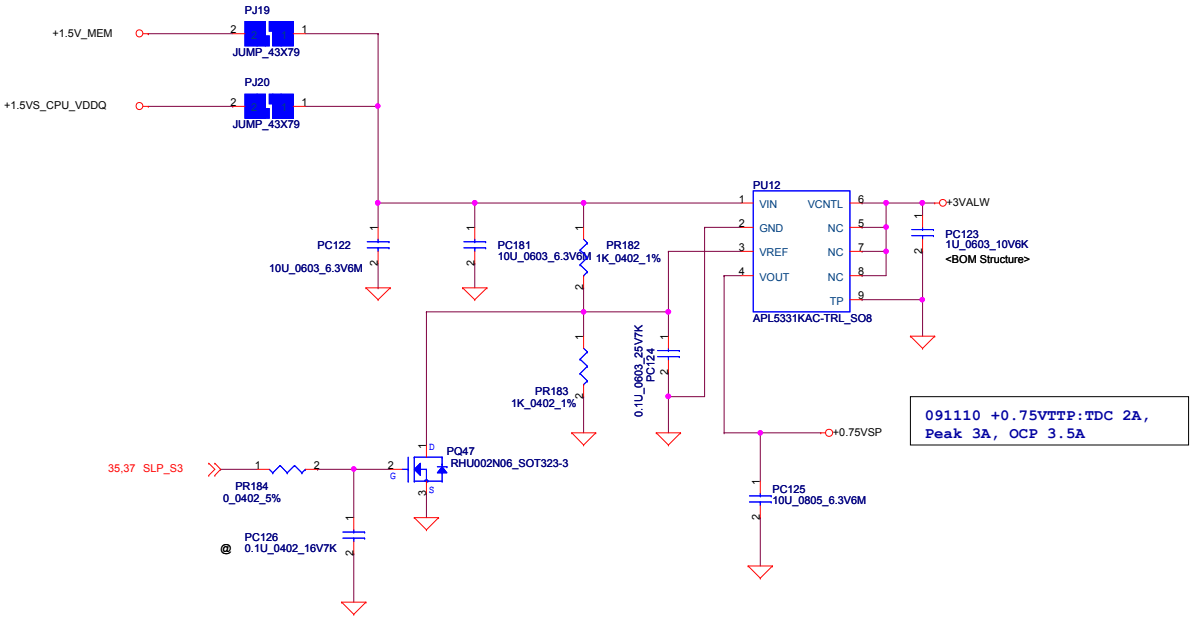
changed frequency from 314K to 369K 2010/04/06



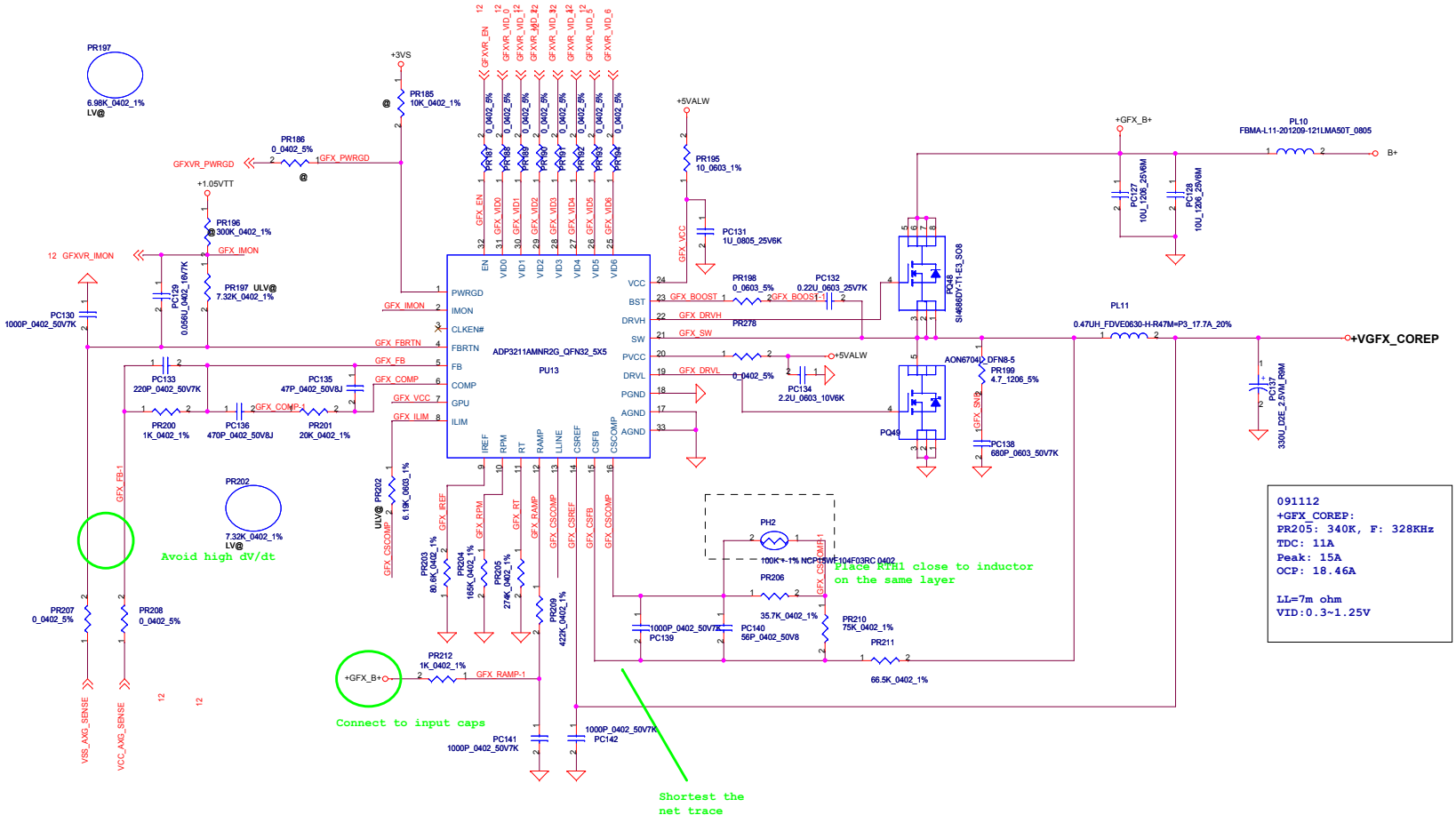
091110
+1.5VP:
PR169: 255K, F: 315KHz
TDC: 8.5A
Peak: 11.795A
PR176: 14.7K
OCP: 12~19.78A

Title	1.05VS&1.5V		
Size: Custom	Document Number: Bradstreet		Rev: <RevCode>
Date: Wednesday, April 28, 2010	Sheet 46 of 52		

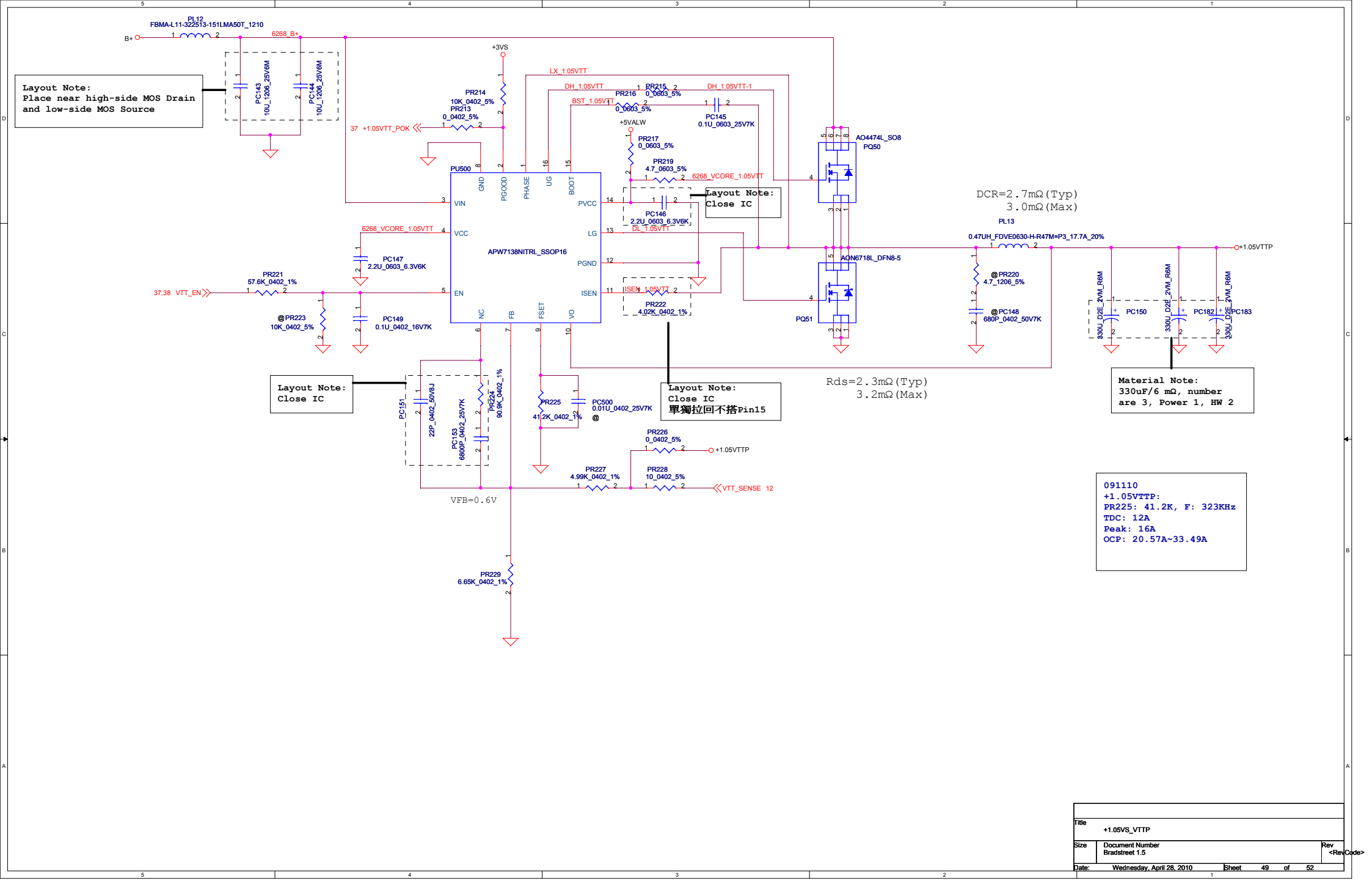




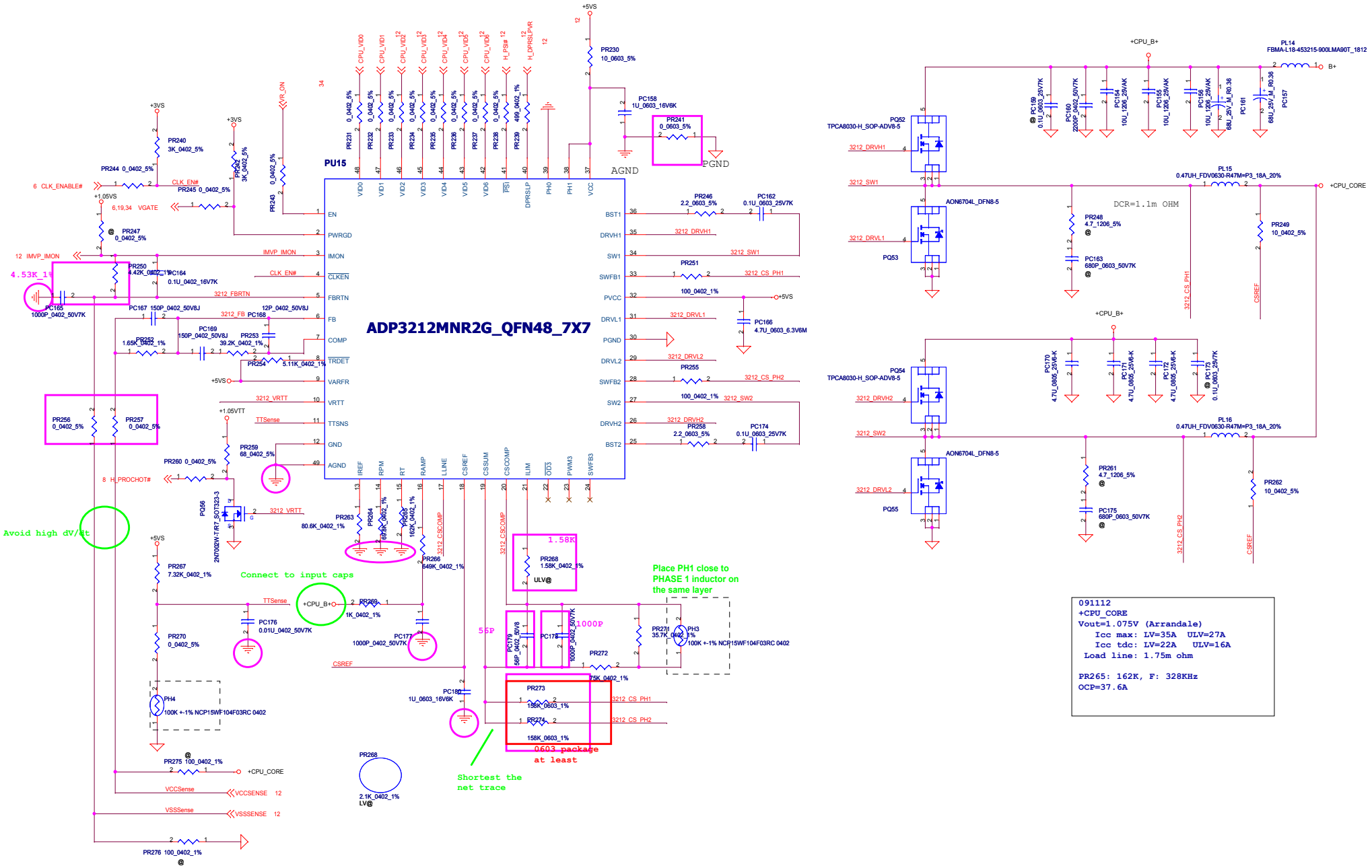
Title	1.8VS&0.75VTT	
Size	Document Number Bradstreet 1.5	Rev <RevCode>
Date: Wednesday, April 28, 2010	Sheet 47 of 52	



Title	VGFX_CORE	
Size	Document Number Bradstreet 1.5	Rev <RevCode>
Date: Wednesday, April 28, 2010	Sheet 48 of 52	



Title	+1.05VS_VTTP	
Size	Document Number Bradstreet 1.5	Rev <RevCode>
Date:	Wednesday, April 28, 2010	Sheet 49 of 52


ADP3212MNR2G_QFN48_7X7
PU15
Avoid high dV/dt
Connect to input caps
Place PH1 close to PHASE 1 inductor on the same layer
Shortest the net trace
0603 package at least
DCR=1.1m OHM
091112
+CPU_CORE
Vout=1.075V (Arrandale)
Icc max: LV=35A ULV=27A
Icc tdc: LV=22A ULV=16A
Load line: 1.75m ohm
PR265: 162K, F: 328KHz
OCP=37.6A
Title
CPU_CORE
Size C
Document Number Bradstreet 1.5
Rev <RevCode>
Date: Wednesday, April 28, 2010
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NVX00 from EVT to DVT LA-6111P REV:0.1 -> 0.2 Modify <2010.01.14.~2010.02.02. >

Rev	Item	Date	Impact	Page	Change Cause	Modify Description
0.2	1	01/14	Circuit,Layout	18	Debug purpose according to Intel suggestion.	Add T28, T29, T30 for CLKOUTFLEX*.
	2	01/14	Circuit, Layout, BOM	19	Design Guide Page320 for RSMRST connection, EVT made error that pull down resistor put to EC side not PCH side, so DVT add a pull down resisitor at PCH side and reserve at EC side.	Add a 10K pull down resistor R551 for "R_RSMRST_PCH#", and reserve R212 pull down resistor at EC side.
	3	01/14	Circuit, Layout, BOM	21	PCH EDS Page88 for PCH GPIO12 connection.	Add a 10K pull up to +3VALW resistor R542 for "LAN_DIS#", and reserve R286 10Kpull up to +3V_ME.
	4	01/14	Circuit, BOM	16	for material shortage, change C241, C248 from 10U to 4.7U_25V_0805.	Change C241, C248 from 10U to 4.7U_25V_0805 (P/N: SE000006R80).
	5	01/14	BOM	34	EVT released MEMO to changed EC from C0 version to D3 version and verified OK.	Changed EC from C0 version (P/N: SA00001J540) to D3 version (P/N: SA00001J580).
	6	01/14	Circuit, BOM	12	DVT add LV CPU configuration, need configure VID.	Changed R84 Bom Struction from "@" to "ULV@", R86 add Bom Struction "LV@"
	7	01/14	Circuit, BOM	34	EVT can't power on issue for ACIN_C only 0.7V.	Change R417 from 4.7K to 1K.
	8	01/14	Circuit, Layout, BOM	37	EVT schematic error, DVT add pull up for VS_PWRGD.	Add R552 10K pull up to +3VS for VS_PWRGD.
	9	01/14	Circuit, Layout, BOM	34	VR_ON floating result in CPU_CORE come out even before SYS power on when no EC ROM.	Add R553 100K pull down for VR_ON.
	10	01/14	Circuit,Layout	20	USB port7 for Motion K/B +/- signal reversed at EVT PCH side.	Modify USB port7 for Motion K/B +/- signal connection at PCH side.
	11	01/14	Circuit, Layout, BOM	36	DVI HPD signal active error at EVT.	Add Q62, R554, R555 for DVI HPD active modify.
	12	01/14	Circuit, Layout	35	+3VS and +5VS have a glitch result in Camera LED abnormal light once less than one second when ACIN or POWER ON .	SLP_S3 pull high power rail change from +3VALW to VL for +3VS and +5VS have a glitch result in Camera LED abnormal light once less than one second when ACIN or POWER ON .
	13	01/14	Circuit, BOM	34	CLK EA test rising time fail, but when remove the EMI RC, EMI could test PASS.	Add Bom Structure "@" to EMI R402 & C488 for CLK_PCI_EC.
	14	01/14	Circuit, BOM	16	CLK EA test rising time fail, but when remove the EMI RC, EMI could test PASS.	Add Bom Structure "@" to EMI R130 & C255 for CLK_PCI_SIO.
	15	01/14	Circuit, BOM	27	CLK EA test rising time fail, but when remove the EMI RC, EMI could test PASS.	Add Bom Structure "@" to EMI R341 & C404 for CLK_PCI_MINI_DB.
	17	01/14	Circuit, BOM	15	CRT DDC signals EA test Rising time and Falling time fail.	Add BS"@" to C214 since CRT DDC signals EA test Rising time and Falling time fail.
	18	01/14	Circuit, Layout, BOM	25	LAN circuit modify according to Intel recommendation.	Delete O ohm resistors R315, R316, R317, R318. Add one 0.1uF C561 & one 10uF C560 for 3.3V, one 10uF C559 for 1.05V. Add 10K R543 pull down reserving for LAN_DIS# (@R543).
	19	01/19	Circuit, Layout, BOM	17 34	G-sensor IC change to new part of Koinix according to customer's recommendation.	Change U13 part from "SA00000RM00" to "SA00003U100 ". Change net "MOTION" to "MOT_EN", change net "F_FALL" to "FF/MOT". delete C267, C270, R162; Add R556.
	20	01/19	Circuit, BOM	34	Board ID configure change from EVT to DVT (EVT not used).	Delete "@" for R421; Add "@" for R419.
	21	01/20	Circuit, Layout	34	Exchange EC Pin21 and Pin 99 for EC common design from EC require.	Exchange EC Pin21 and Pin 99 connection.
	22	01/20	Circuit, Layout	28	GPIO38 & GPIO39 pull high power rail error at EVT(should be +3vs) that result in +3vs Back drive.	Change EXPANSION_ID1 & EXPANSION_ID0 pull high power rail from +3VALW to +3VS.
	23	01/20	Circuit, Layout, BOM	26	Sourcer require change GLAN switch U18 from "SA035000000- PI3L500" to "SA00001DY00-PI3L500-A"	GLAN switch U18 from "SA035000000- PI3L500" to "SA00001DY00-PI3L500-A"
	24	01/20	Circuit, BOM	15 27 36 35 37	Cost issue from PIR.	Change D1 main source from ROHM "SC1B491D000" to NXP "SCS00003H00". Change D10, D11, D26 main source from ROHM "SC1B751V005" to NXP "SCS00002G00". Change D24, D29 main source from ROHM "SC2N202U010" to Panjit "SC600000B00".
	25	01/22	Circuit, Layout, BOM	16	Sourcer require change SIO U10 from "SA472170050" to "SA000034K10".	Change SIO U10 from "SA472170050" to "SA000034K10".
	26	01/25	Circuit, Layout, BOM	17	Remove SATA repeater according to customer's request.	Delete U50, R508, R509, R510, C545, C546, C265, C266.
	28	01/27	BOM	16	Display PWM controll change default connection from PCH to EC for ALS function.	Add @ to R114, delete @ for R119.
	29	01/27	Circuit, Layout, BOM	33	Reserve ALS SM Bus connection to PCH.	Add R557, R558, @R559, @R560.
	30	01/27	Circuit,Layout	34 36 19	ACIN to PCH better is controlled by EC if have VPro.	Delete net PCIE_DET# which is just reserved, change EC pin86 to "ACIN_PCH", add 0 ohm resister R561.

Security Classification	Compal Secret Data		
Issued Date	2006/02/13	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: NVX00 PIR SHEET

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Custom	LA-6111P	0.2

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NVX00 from EVT to DVT LA-6111P REV:0.1 -> 0.2 Modify <2010.01.14.~2010.02.02. >

Rev	Item	Date	Impact	Page	Change Cause	Modify Description
0.2						
	31	01/27	Circuit, Layout, BOM	34	No need RP7 for just two pull high.	Delete RP7, add R562, R563 for DP_SLP and DP_RST pull high.
	32	01/27	Circuit, Layout, BOM	34 27 21 28	BIOS debug reuqest.	Add BIOS debug signals on JWLAN conn. Change PCH GPIO36 to "TPM_RST#" and add 0 ohm resistor R565. Add U52.
	33	01/28	Circuit, Layout, BOM	16	Add Pannel backlight control circuit according to customer require.	Delete R121, C243, Add Q61, Q63, R566, R567, R568.
	34	02/02	BOM	16	SIO parts need remove in BOM that customer required.	Add "@" to parts U10, R115, R117, R118, R120, R122, R125, R126, R127, R128, R129, C256, C257, C260, R130, R131, C255, C258.
	35	01/29	Circuit, Layout, BOM	17 34	From customer implementation, add G-sensor free fall and motion interrupt to HDD for configure 2 &3.	Add R569, @R570 at Page17, add @R571 at Page34.
	36	01/29	Circuit, Layout	35 37	Avoid leakage after power change +1.5V power enable signal control since power IC skip mode issue. Avoid leakage issue same as SLP_S3 signal pull up power rail.	Change SLP_S4, SIO_SLP_LAN, PM_SLP_M pull up power rail from +3valw to VL.
	37	02/01	Circuit,Layout	6	DFX issue.	Change L1&L2 footprint to R_0805.
	38	02/01	Circuit, Layout	34 17	Customer implementation.	change EC Pin108 to "FF/MOT_HDD_R"
	39	02/01	Circuit, Layout	11	DFX issue.	Change C89, C90, C91, C92, C93 footprint from "C_D2T" to "C_D2E".
	40	02/02	Circuit, Layout, BOM	28	Customer TPM RESET require before gerber.	Add R572, add @ to R532.
	41	02/02	Circuit, Layout, BOM	16	Customer ALS Display PWM control require before gerber.	Add U53, Add @ to R119.
	42	02/03	BOM	18 20	SIO parts will not mount in BOM.	Add @ to R533 at Page18, R265 at Page20.

NVX00 from DVT to PVT LA-6111P REV:0.2 -> 0.3 Modify <2010.03.26.~2010.04.13. >

Rev	Item	Date	Impact	Page	Change Cause	Modify Description
0.3						
	1	03/29	Circuit, BOM	34	Board ID configure.	Re-define board ID configure for EC.
	2	03/29	Circuit, Layout, BOM	17	G-sensor issue.	Add a capacitor C552 for G-sensor reset!
	3	03/29	Circuit, BOM	28	Require from BIOS.	Add "@" to R507 for TPM.
	4	03/29	Circuit, Layout, BOM	18	Controller link signal connected error at EVT.	Delete R529, Q52, R541.
	5	03/29	Circuit, BOM		update CPU, PCH, LAN P/N to MP P/N.	update CPU, PCH, LAN P/N to MP P/N.
	6	03/30	Circuit, BOM	28	DVT forgot to update TPM P/N to FW3.16 IC P/N.	Update TPM P/N to FW3.16 IC P/N.
	7	04/06	Circuit, Layout, BOM	35	Customer implementation for GPS performance issue.	add snubber to EC_SPI_CLK_R
	8	04/09	Circuit, Layout, BOM	28	TPM issue.	add @R373, @R420 for TPM PP pin required by BIOS.
	9	04/12	Circuit, Layout, BOM	17	Require from Motion to add more decoupling capacitors for G-sensor VDD.	Add R553 and R554.
	10	04/14	Circuit, BOM	17	DQA RTC time lag issue.	Change C261, C262 from "8.2pF" to "6.8pF"
	1	04/28	Circuit, BOM	17 35	Change SYS BIOS "JP10" to JBIOS, change EC ROM socket "JBIOS1" to "JEC"	Change SYS BIOS "JP10" to JBIOS, change EC ROM socket "JBIOS1" to "JEC"
	2					

Compal Electronics, Inc.

Title: NVX00 PIR SHEET

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Custom	LA-6111P	0.2

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Version change list (P.I.R. List)

Item	Category	Modify List	PG#	Date	Phase
1	add battery discharge function	add PR500,PR501,PQ57,PQ58		2010/01/29	DVT
2	modify AC&battery swap function	connect PR58 to PACIN,PU4.5 to PU4.28		2010/01/29	DVT
3	change 1.8V solution	add PC152,PC184,PC185,PC186,PC187,PC210,PJ18,PL23,PR218,PR277,PR279,PR280,PR281,PU14		2010/01/29	DVT
4	remove 1.05VTTP snubber	remove PR220,PC148		2010/01/29	DVT
5	changed 1.5VP&1.05V_LANP PWM frequency to 369k	changed PR159,PR169 to 220k		2010/04/14	PVT
6	added pull down resister on 1.8V EN pin	added PR280		2010/04/14	PVT
7	modify battery swap function	changed power rail to RTCVREF, changed PR45,PR53 to 300k		2010/04/14	PVT
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					
21					
22					
23					

Compal Electronics, Inc.
Title: PIR (PWR)
Size: Custom | Document Number: MB Schematic | Rev: 0.1
Date: Wednesday, April 28, 2010 | Sheet 59 of 60