MS-7788 Ver: 2.0 m-ATX : 243.84 X 228mm

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(H61)

OnBoard Chipset:

HD Audio Codec:RTL887 Co-lay 892
LAN:8105E 10/100, Co-lay RTL 8111E 10/100/1000
SIO:FIN71868AD
Flash ROM: 64Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 1
PCI Slot *1 by ASM1083

PWM:

Controller:VRD12 UT501 3Phase
CPU+GPU: UP6282 MOSFET Driver
CPU VTT: IP6103
CPU SA : OP+MOS
DDR: UP6103
PCH: OP+MOS

ACPI:

UPI

Other:

SATA2.0 x4 (PCH)
SATA3.0 x2 (ASM1061)
USB2.0 RearX4 Front x4
USB3.0 RearX2 FrontX2
D-SUB/DVI/*1
TPM Header *1(debug only)

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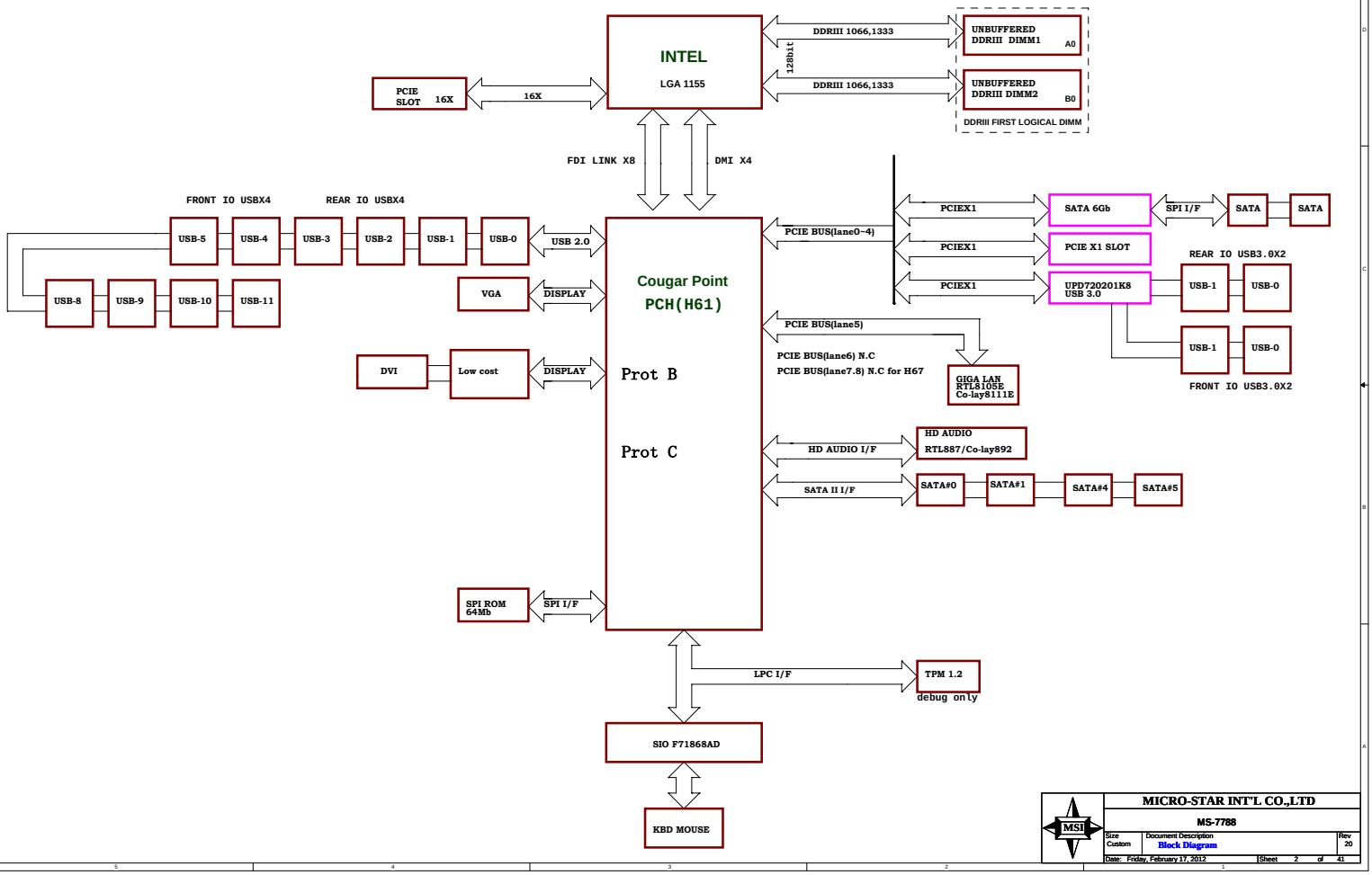
Manual & Option
Manual & Option
Manual & Option



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Size: Custom | Document Description: Block Diagram | Rev: 20

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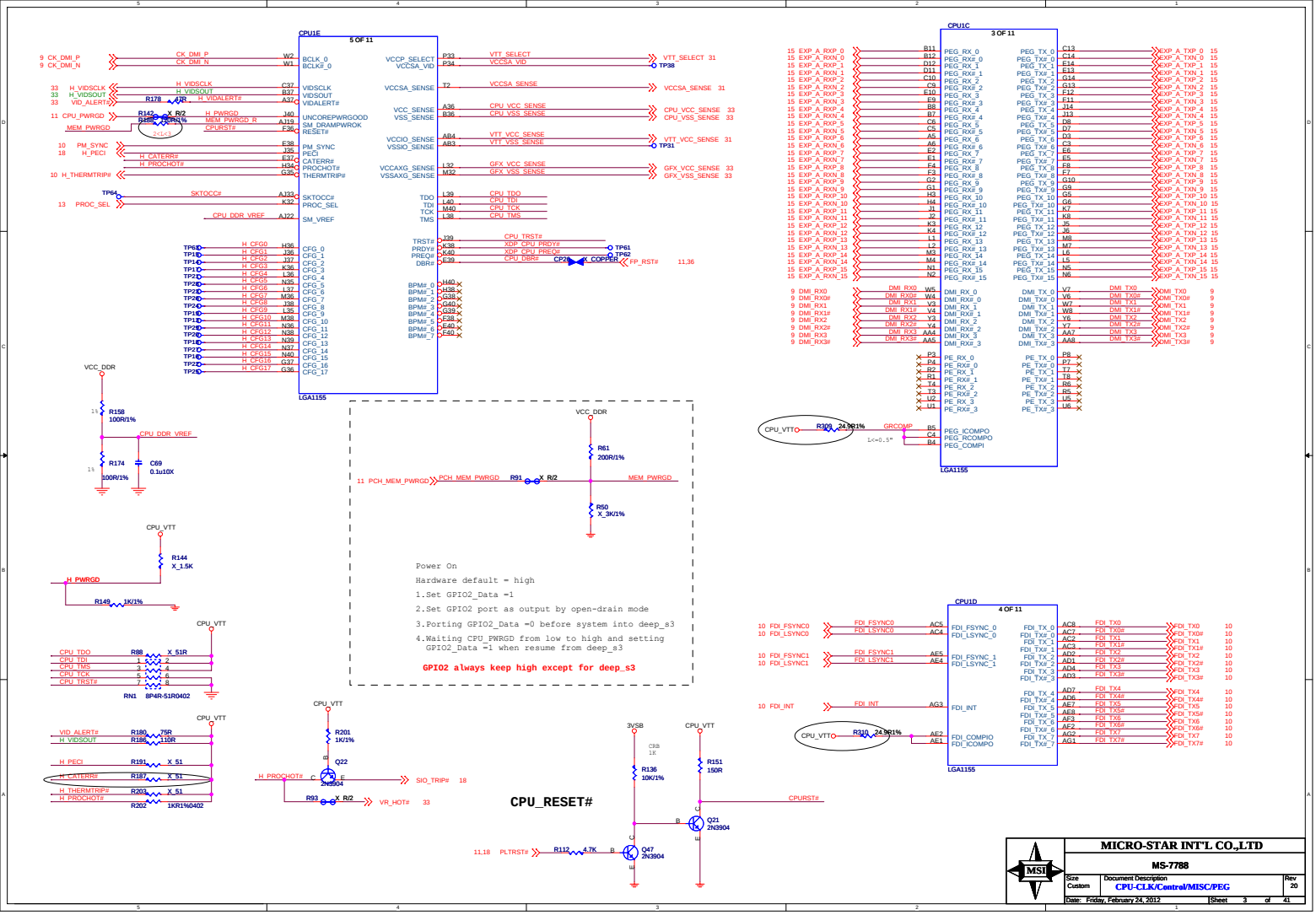

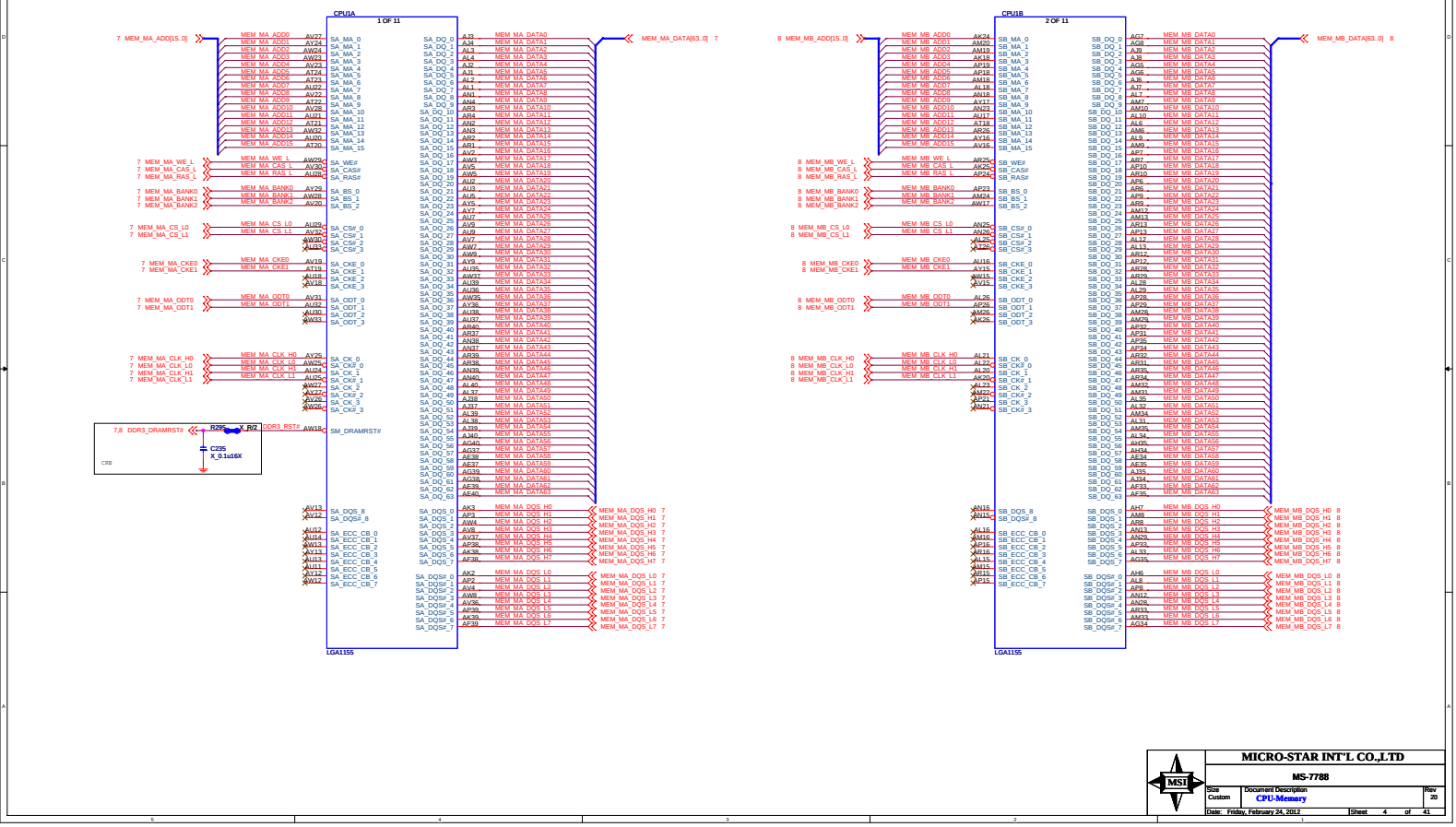

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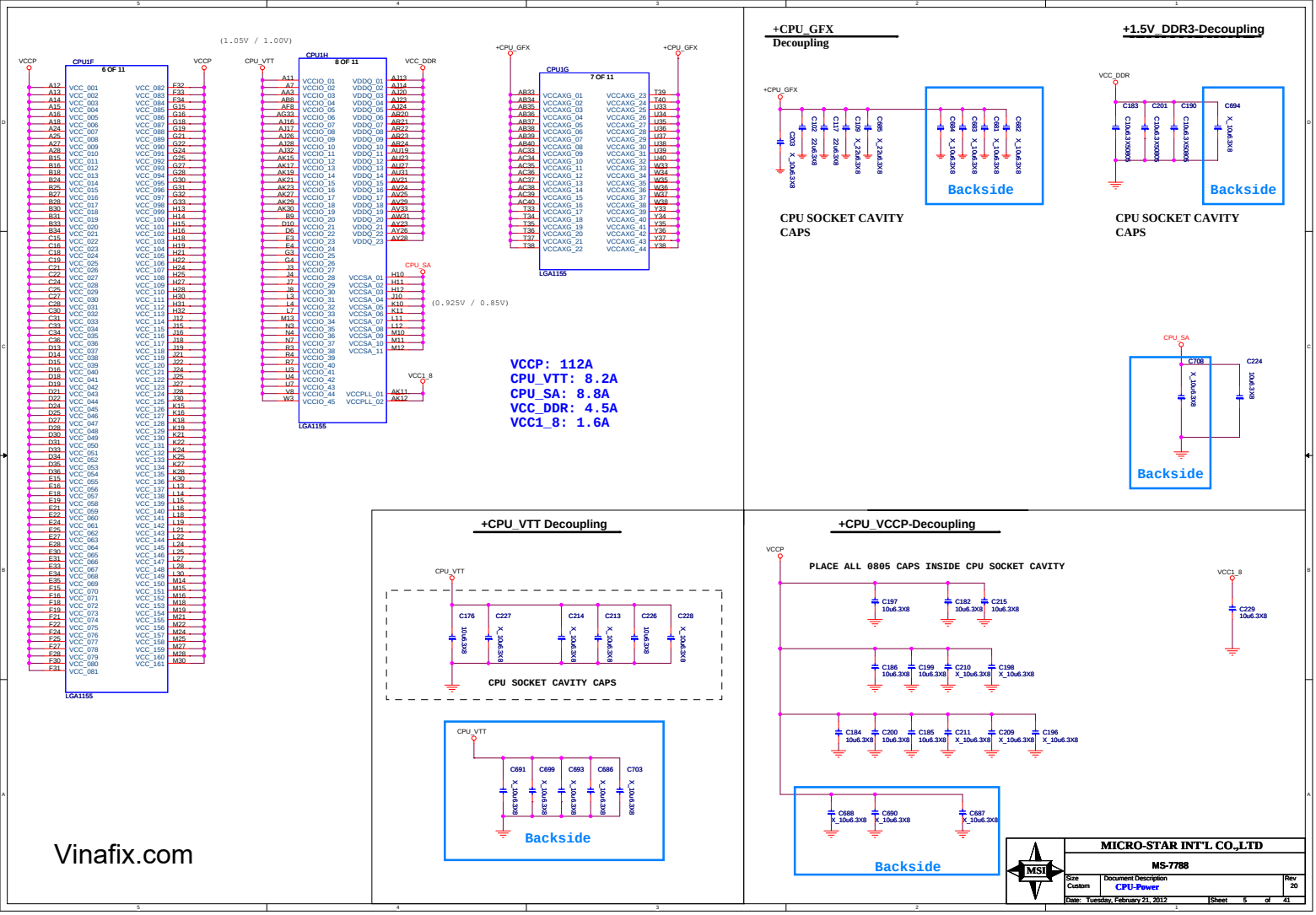
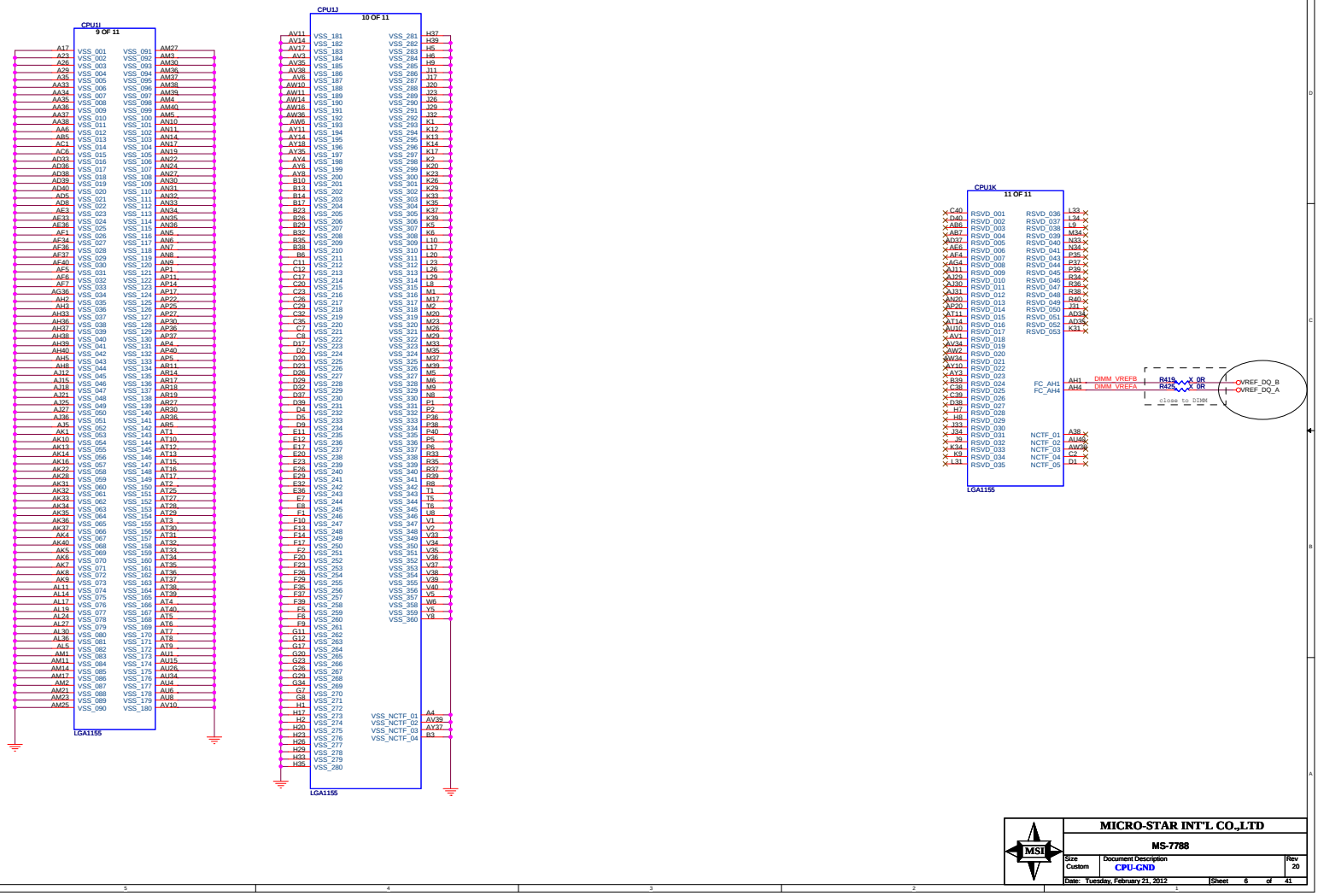
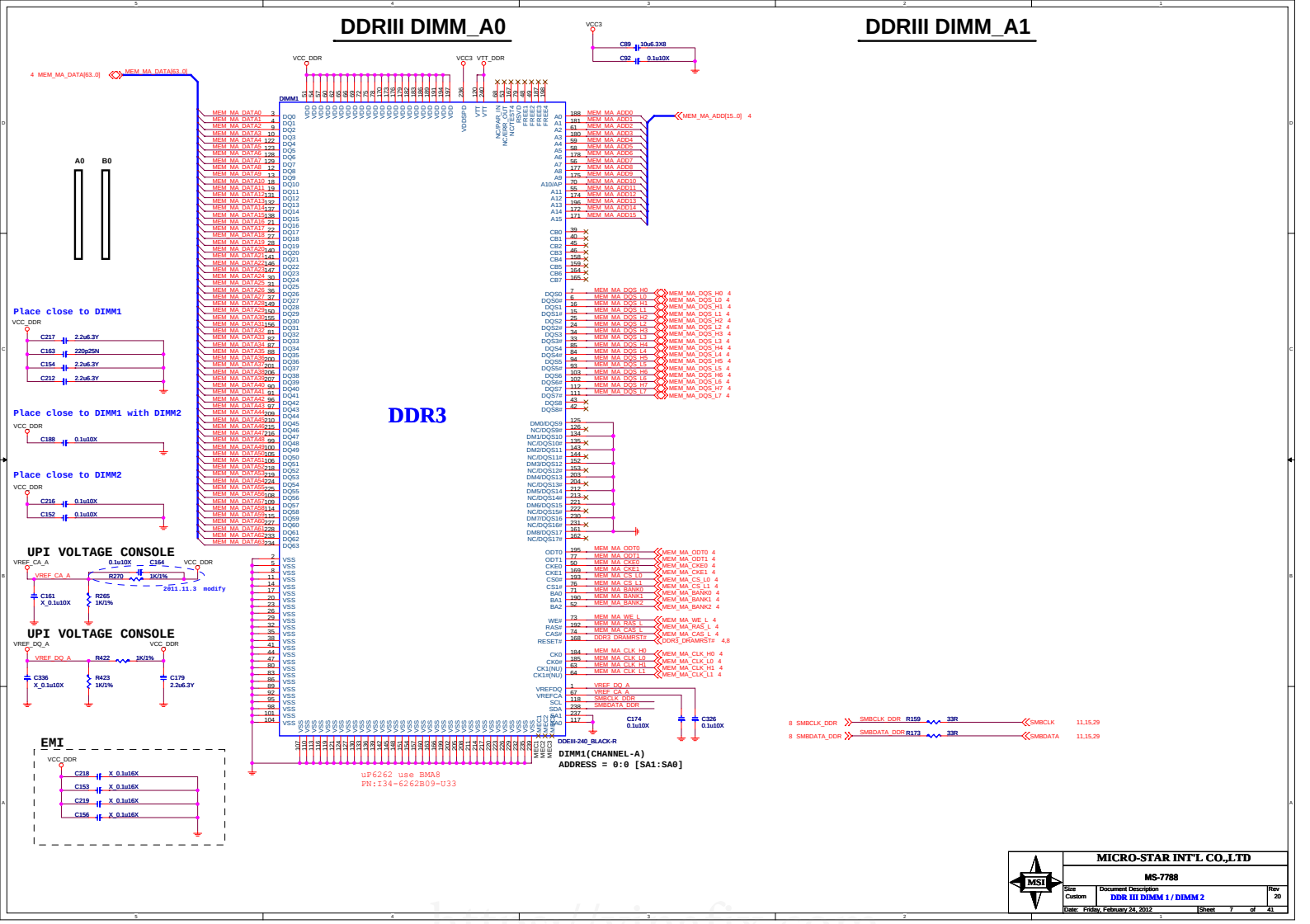
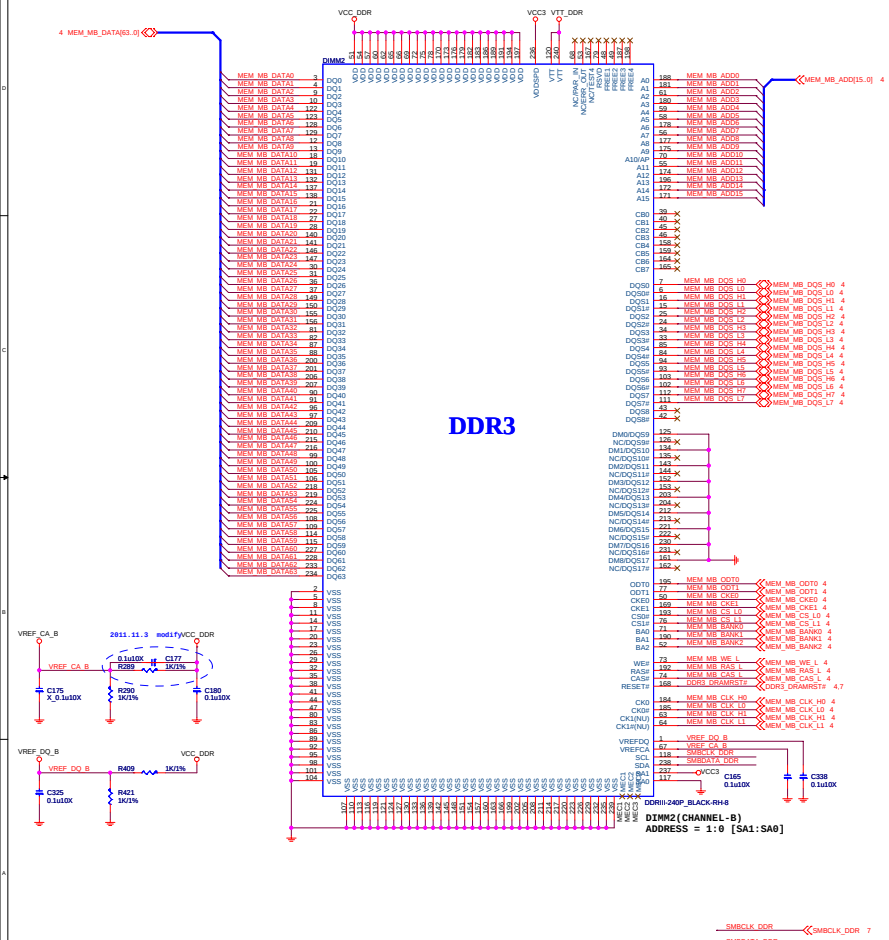




MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7788	
Size: Custom	Document Description: CPU-GND	Rev: 20
Date: Tuesday, February 21, 2012	Sheet 6 of 41	



DDRIII DIMM_B0



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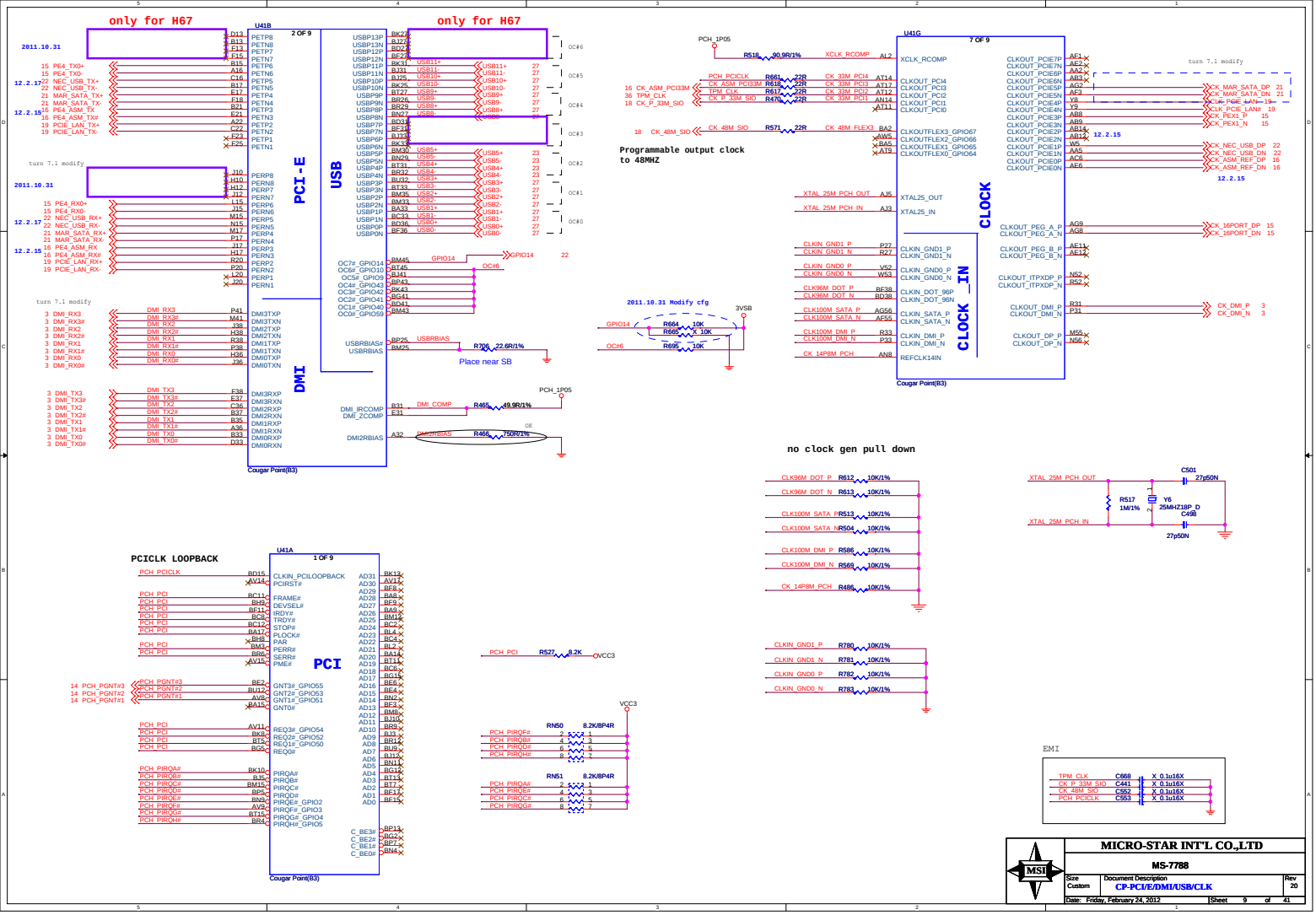
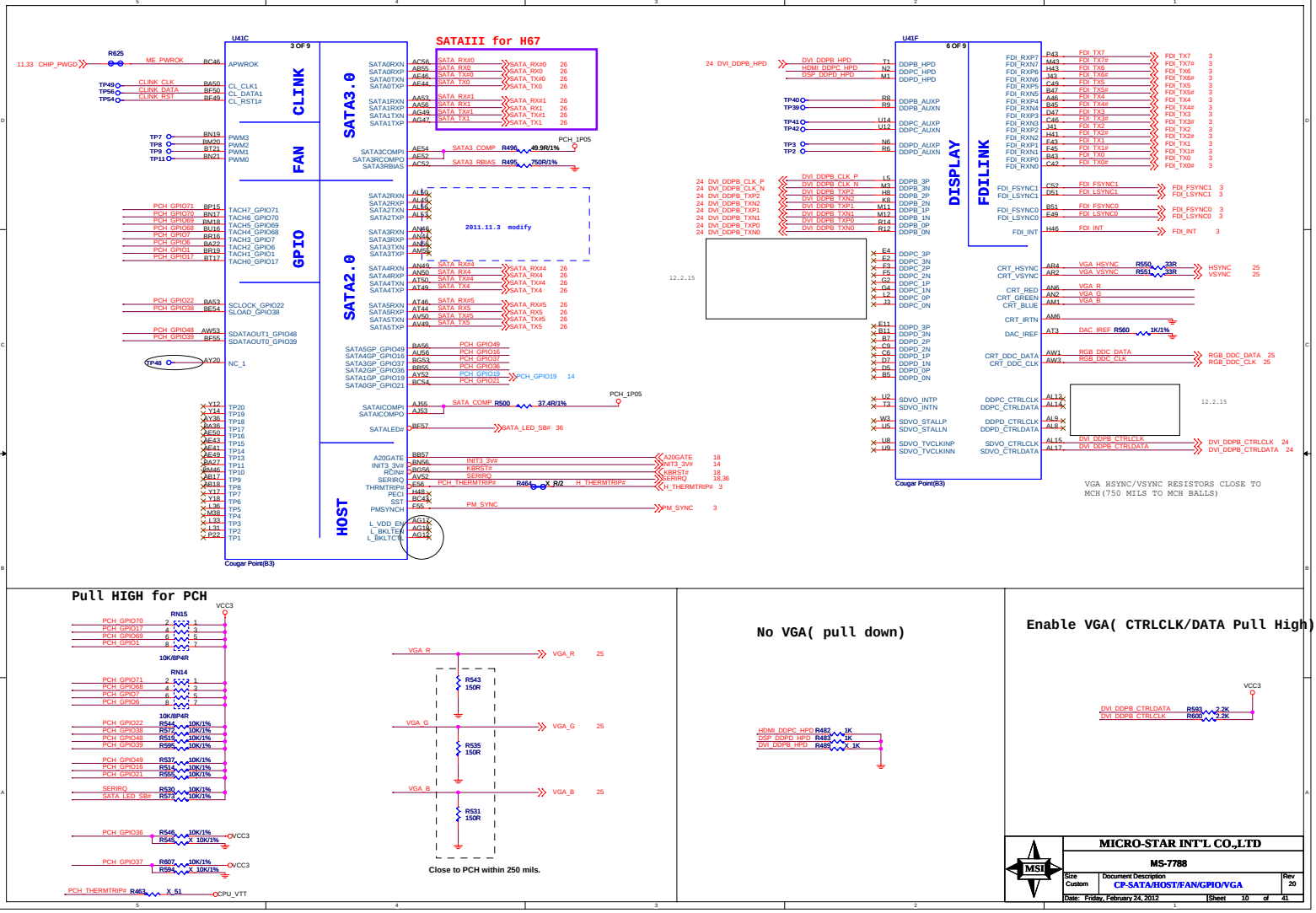
MS-7788		
Size: Custom	Document Description: DDR III DIMM 3 / DIMM 4	Rev: 20
Date: Friday, February 24, 2012	Sheet 8 of 41	





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MS-7788		
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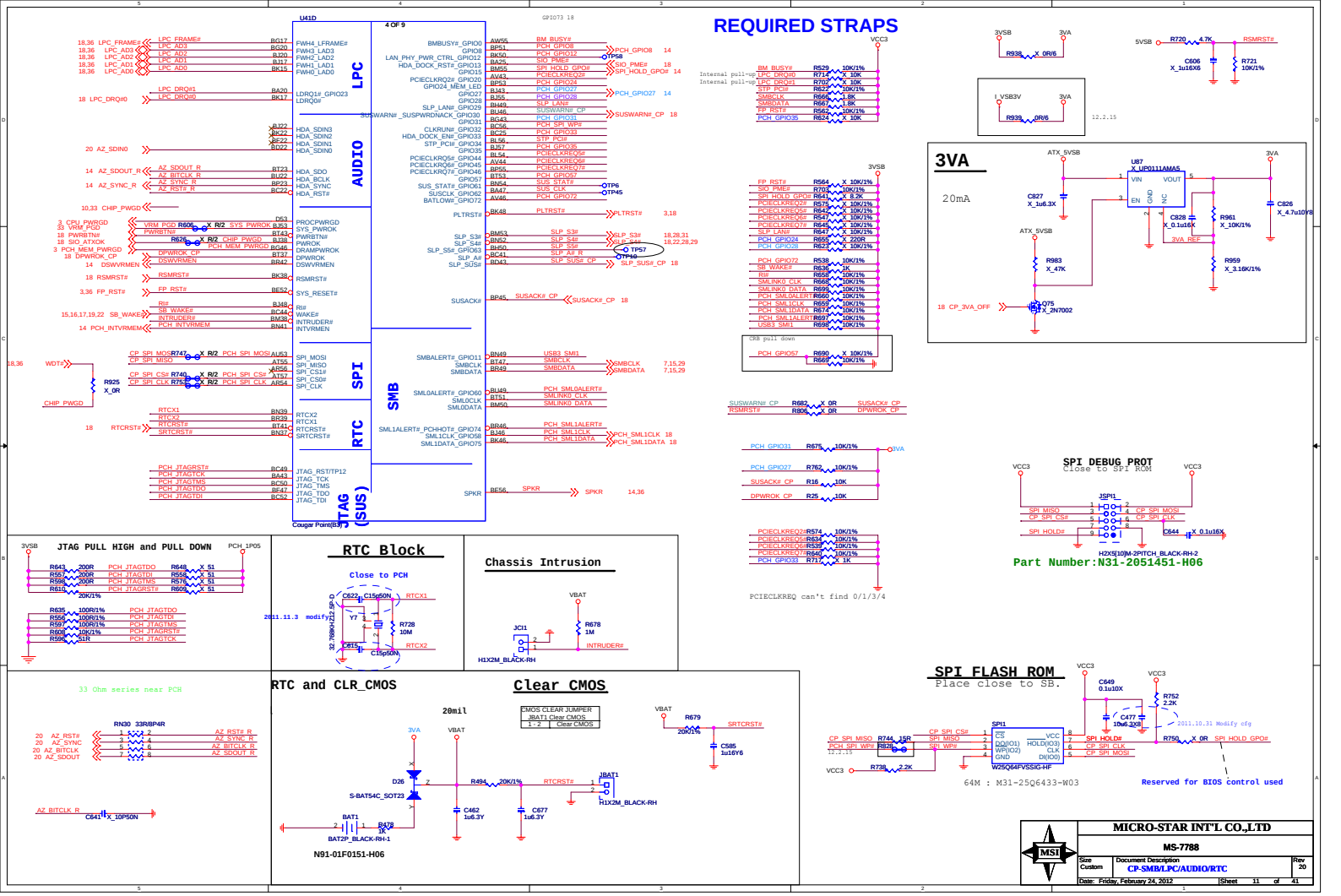

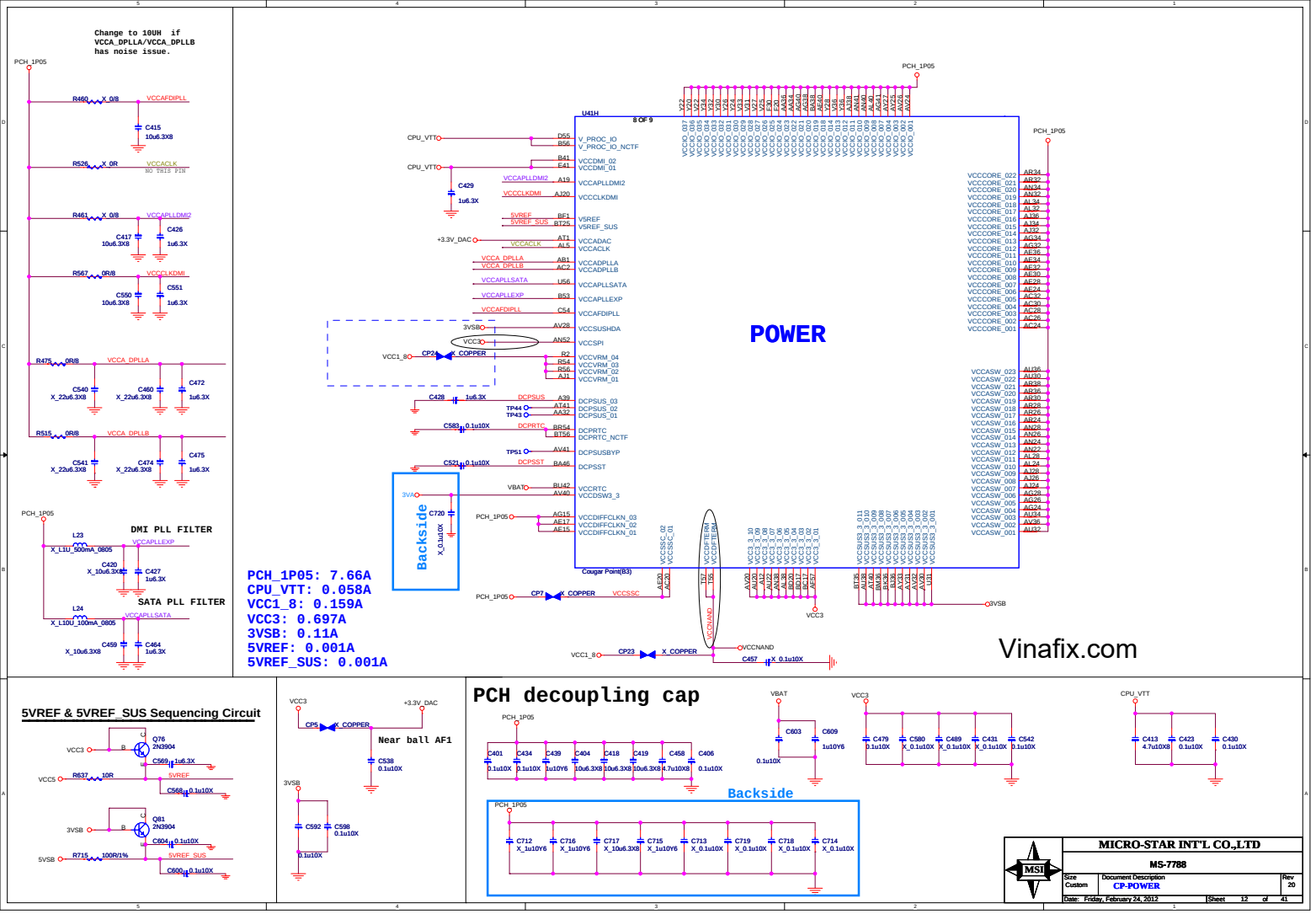

MICRO-STAR INT'L CO.,LTD		
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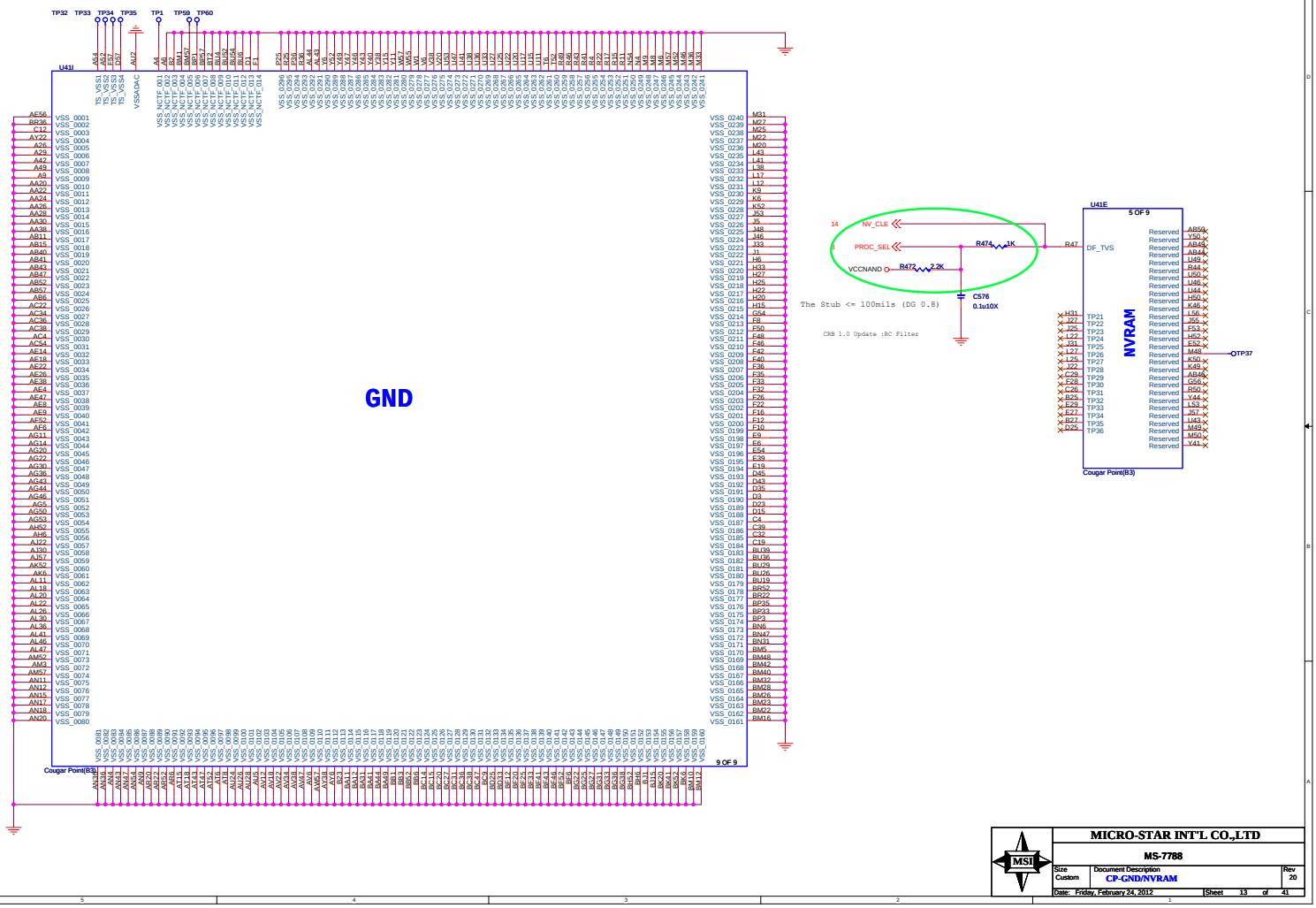
Size: Custom	Document Description: CP-POWER	Rev: 20
Date: Friday, February 24, 2012	Sheet 12 of 41	



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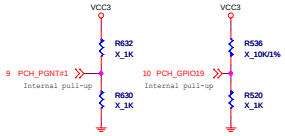
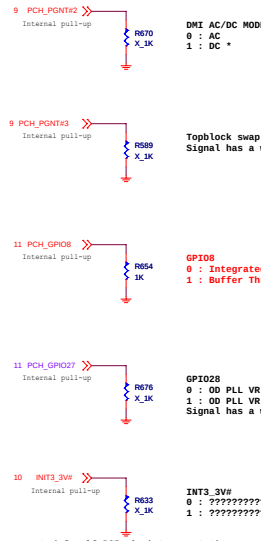
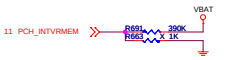
PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1





1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.

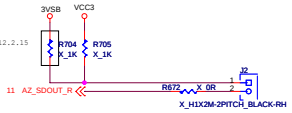


INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltageregulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

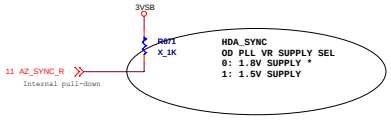
DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.



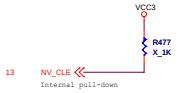
HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high

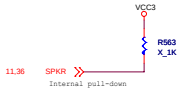


HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

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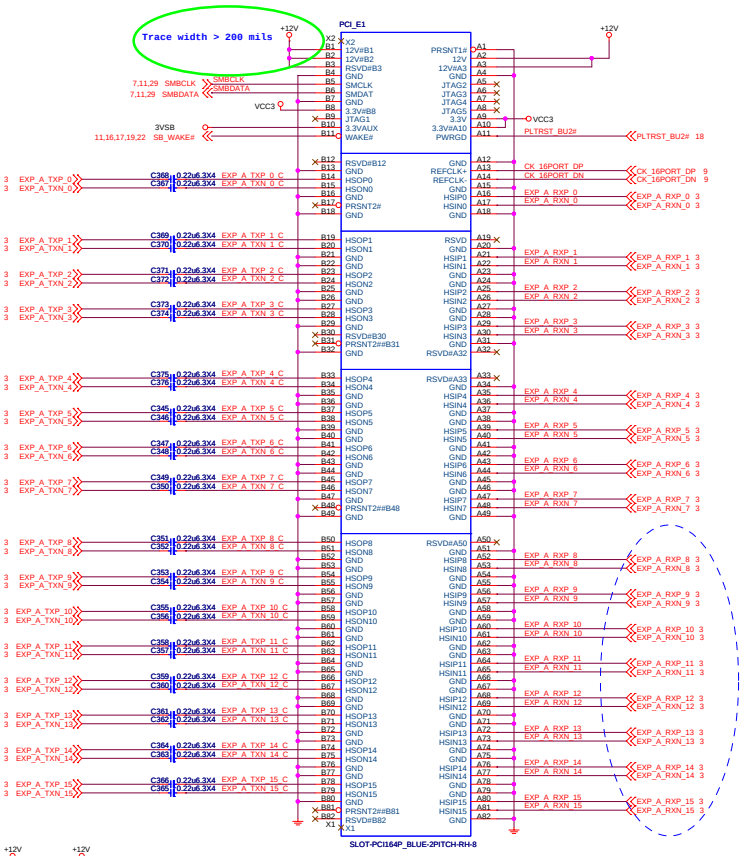
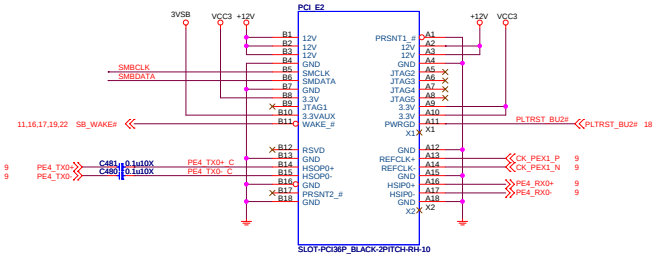
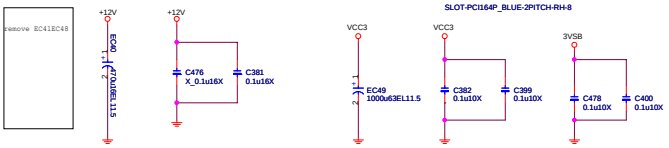
PCI_Express X16 Slot



PCI EXPRESS x1-PORT





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Size: Custom	Document Description: PCIE x16 /x1 teknisi indonesia
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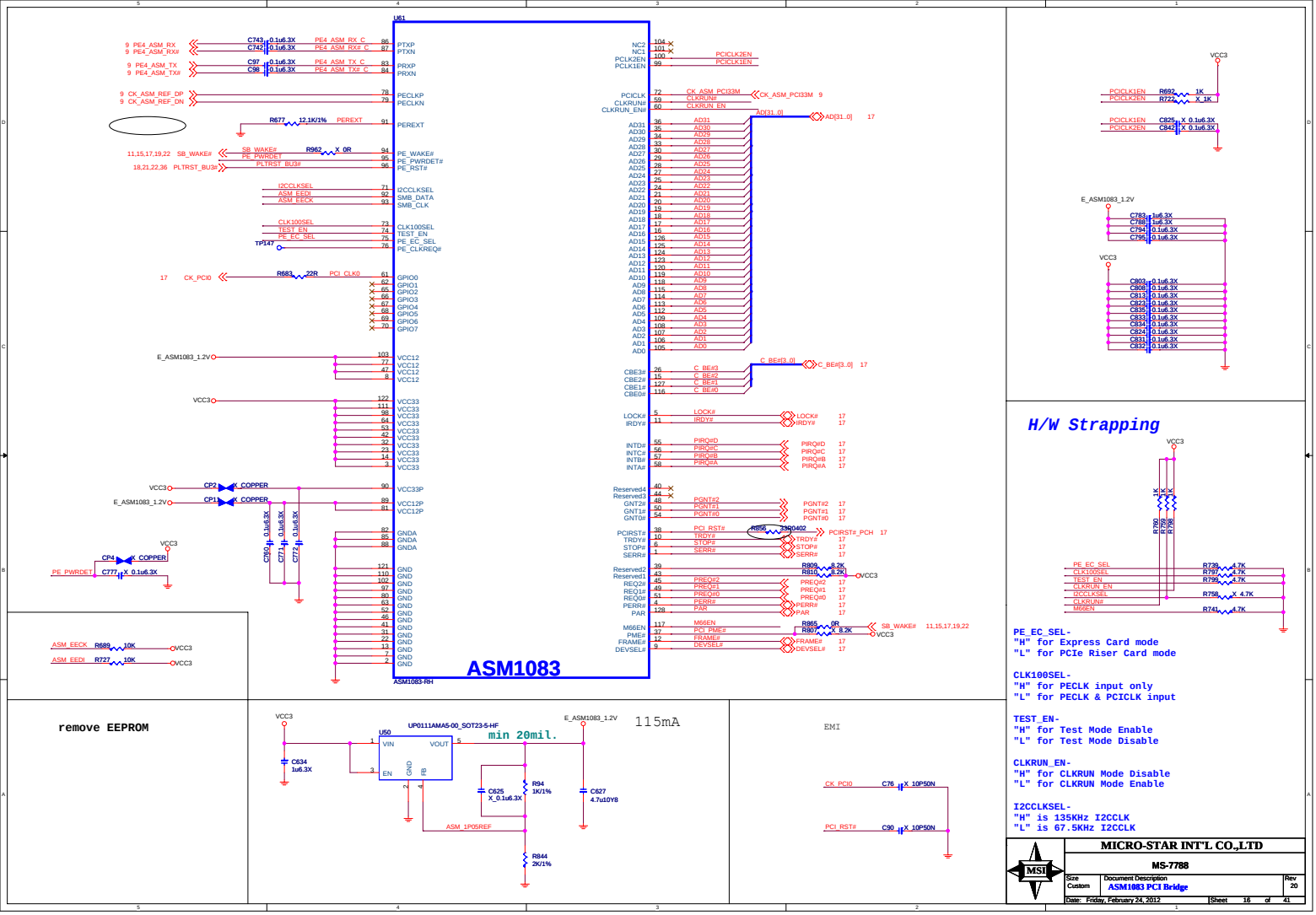

H/W Strapping

PE_EC_SEL-
"H" for Express Card mode
"L" for PCIe Riser Card mode

CLK100SEL-
"H" for PECLK input only
"L" for PECLK & PCICLK input

TEST_EN-
"H" for Test Mode Enable
"L" for Test Mode Disable

CLKRUN_EN-
"H" for CLKRUN Mode Disable
"L" for CLKRUN Mode Enable

I2CCLKSEL-
"H" is 135KHz I2CCLK
"L" is 67.5KHz I2CCLK

remove EEPROM

EMI

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: ASM1083 PCI Bridge	Rev: 20
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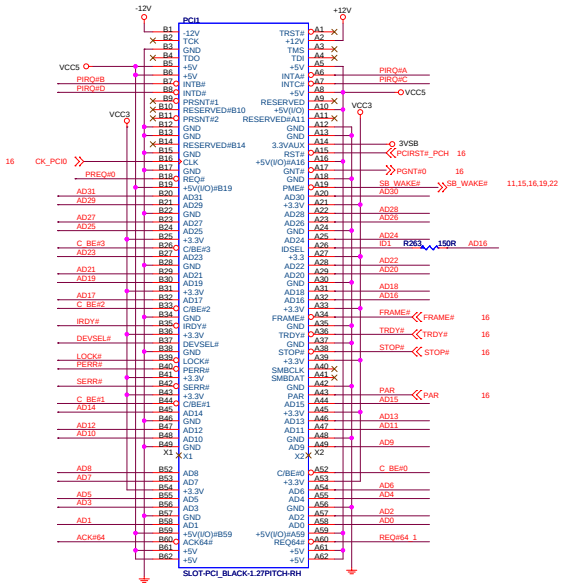
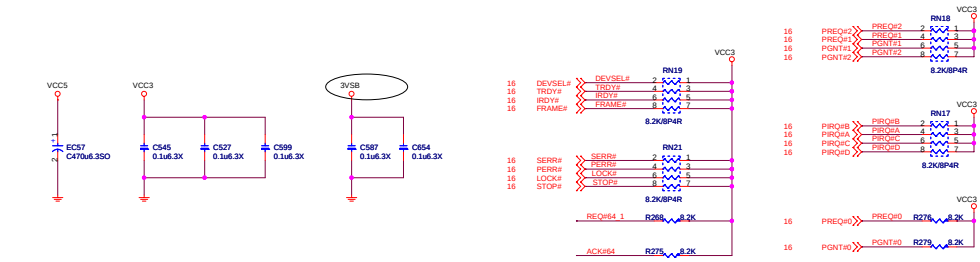


IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

PCI PULL-UP / DOWN RESISTORS



PCI slot (X1)	
+3.3Vaux (wake)	- 1125mA
+3.3Vaux (no wake)	- 60mA
+3.3V	- 7.6A
+5V	- 5A
+12V	- 0.5A

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: PCIx1 Slots	Rev: 20
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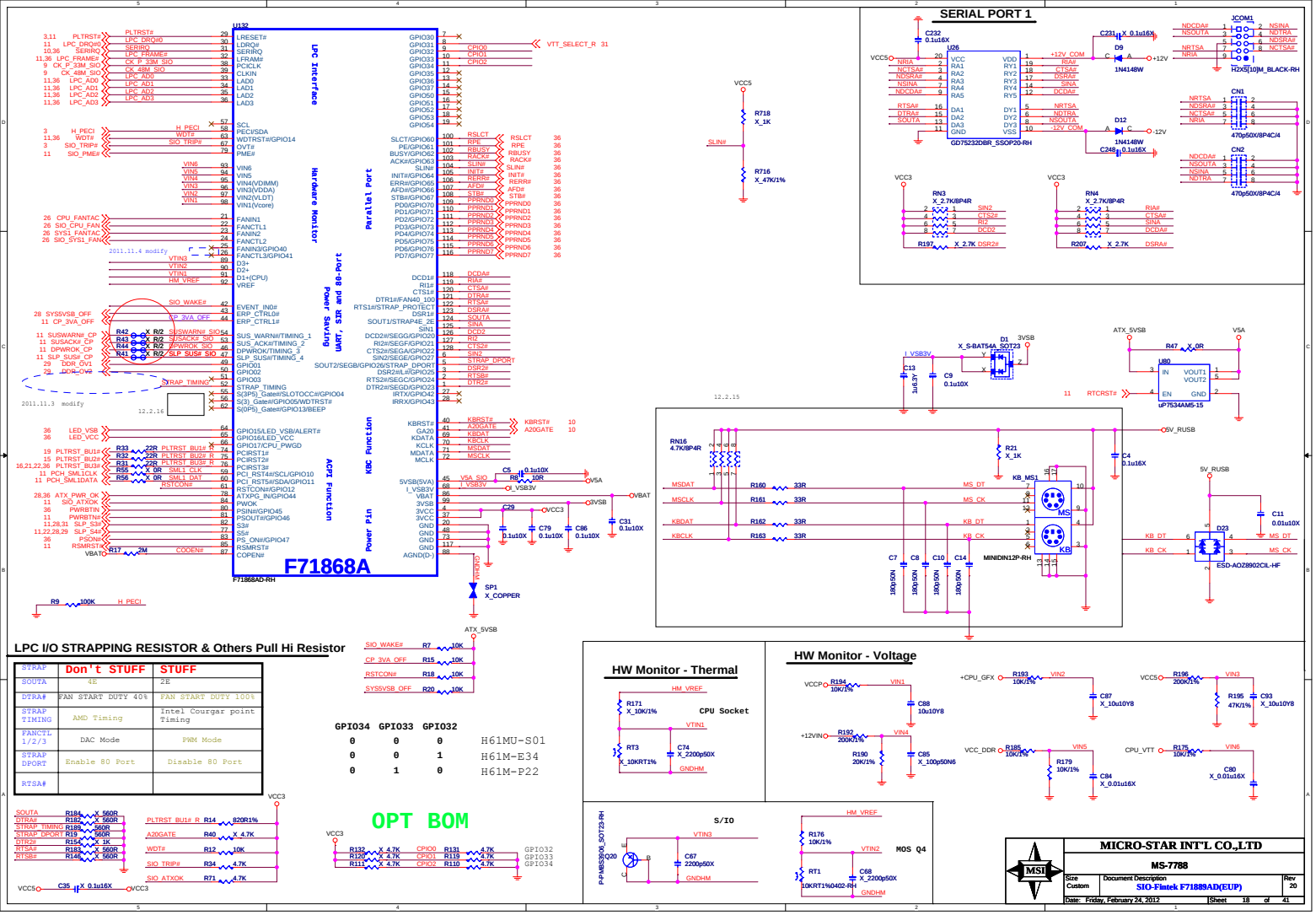

LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP TIMING	AMD Timing	Intel Courgar point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP DPORT	Enable 80 Port	Disable 80 Port
RTSA#		

GPIO34	GPIO33	GPIO32	
0	0	0	H61MU-S01
0	0	1	H61M-E34
0	1	0	H61M-P22

OPT BOM

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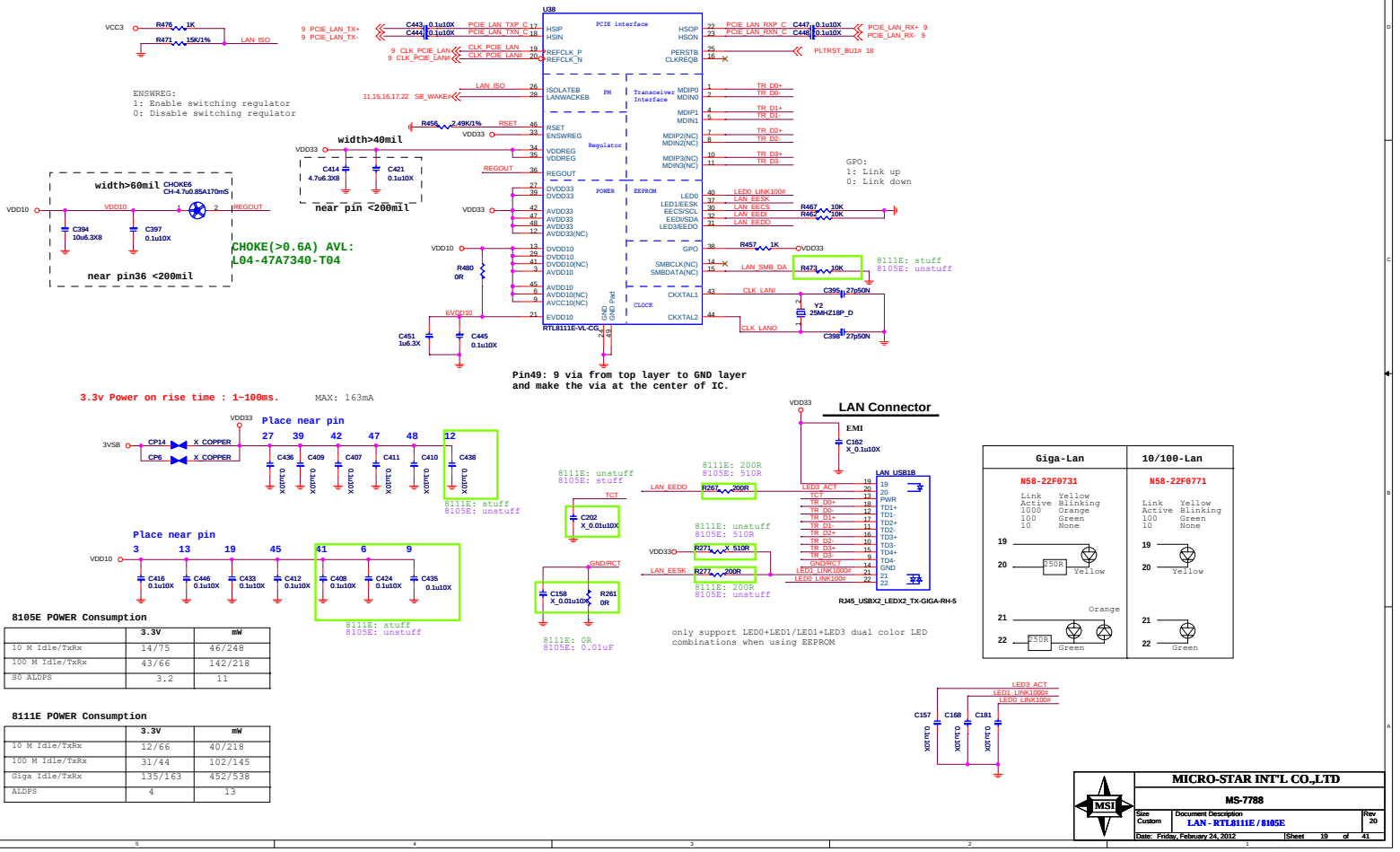
RTL8111E Giga LAN

RTL8105E 10/100M LAN



3.3v Power on rise time : 1~100ms. MAX: 163mA

8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

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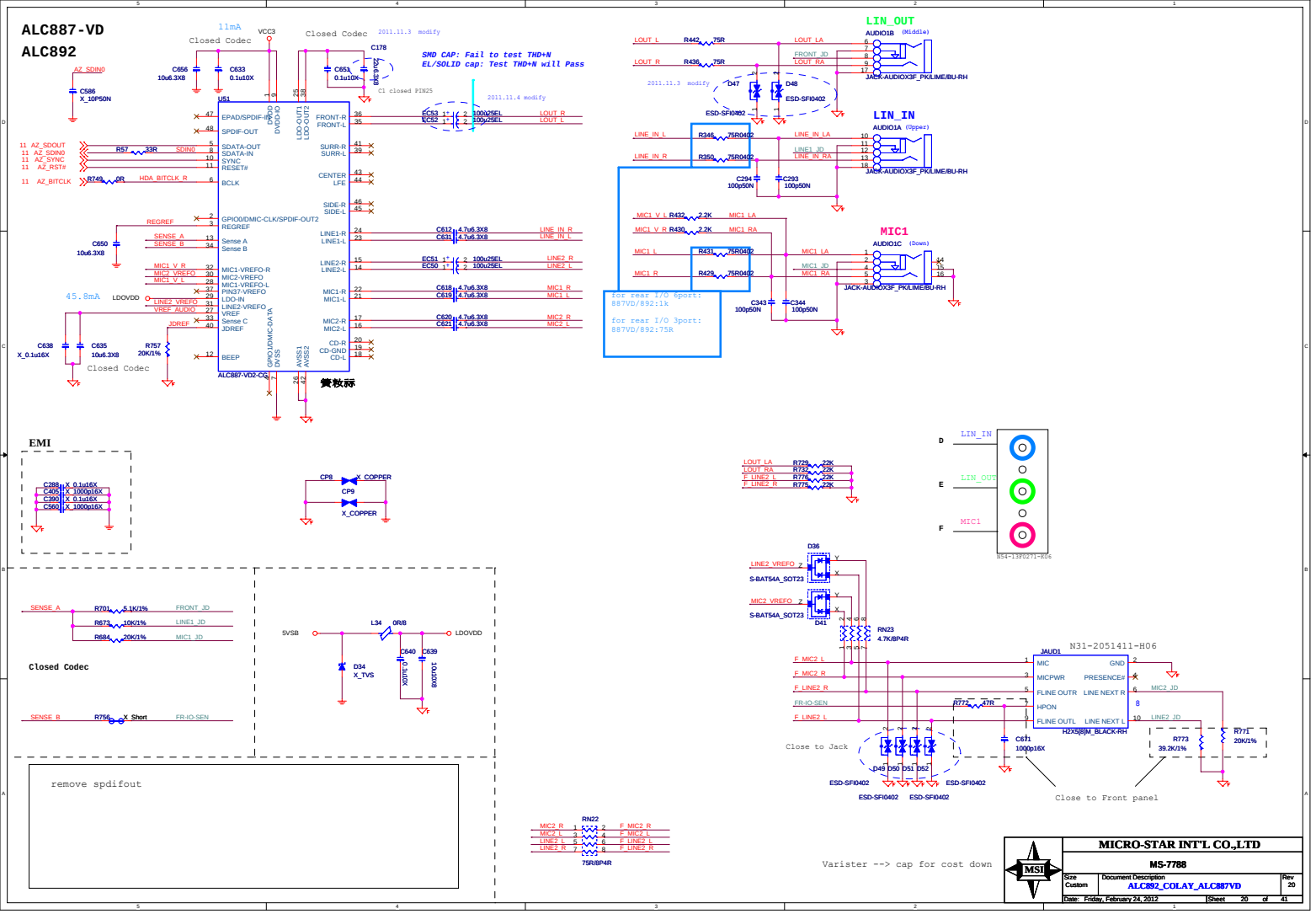
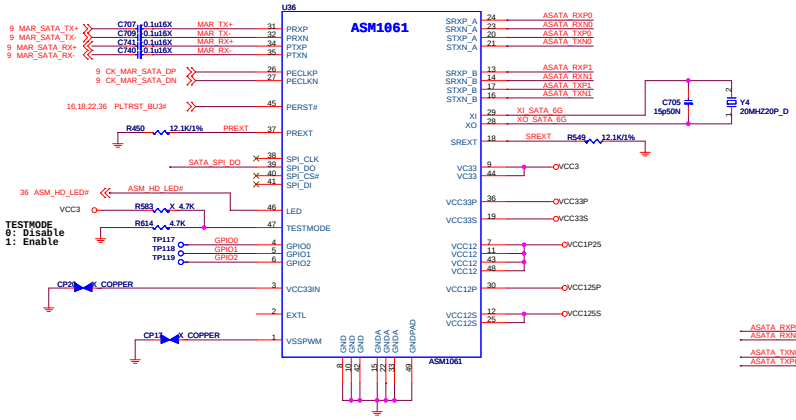
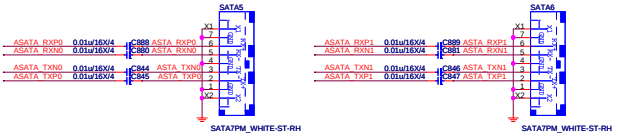


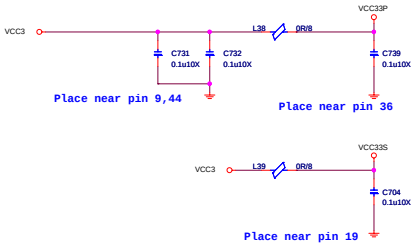
ASM1061 SATA6G

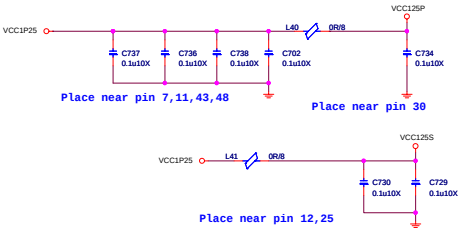


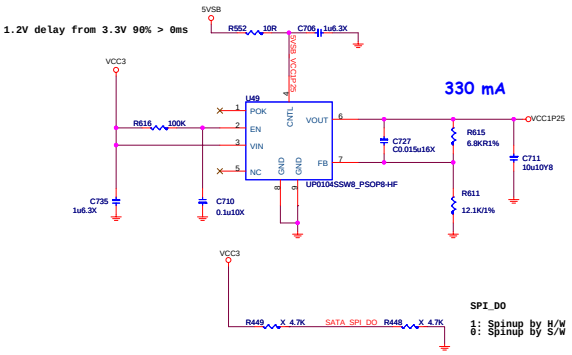


ASM1061 POWER Consumption

	3.3V	1.2V	Power (mW)
Idle (mA)	98.45	212.3	579.645
Busy (mA)	91.1	330.7	697.47







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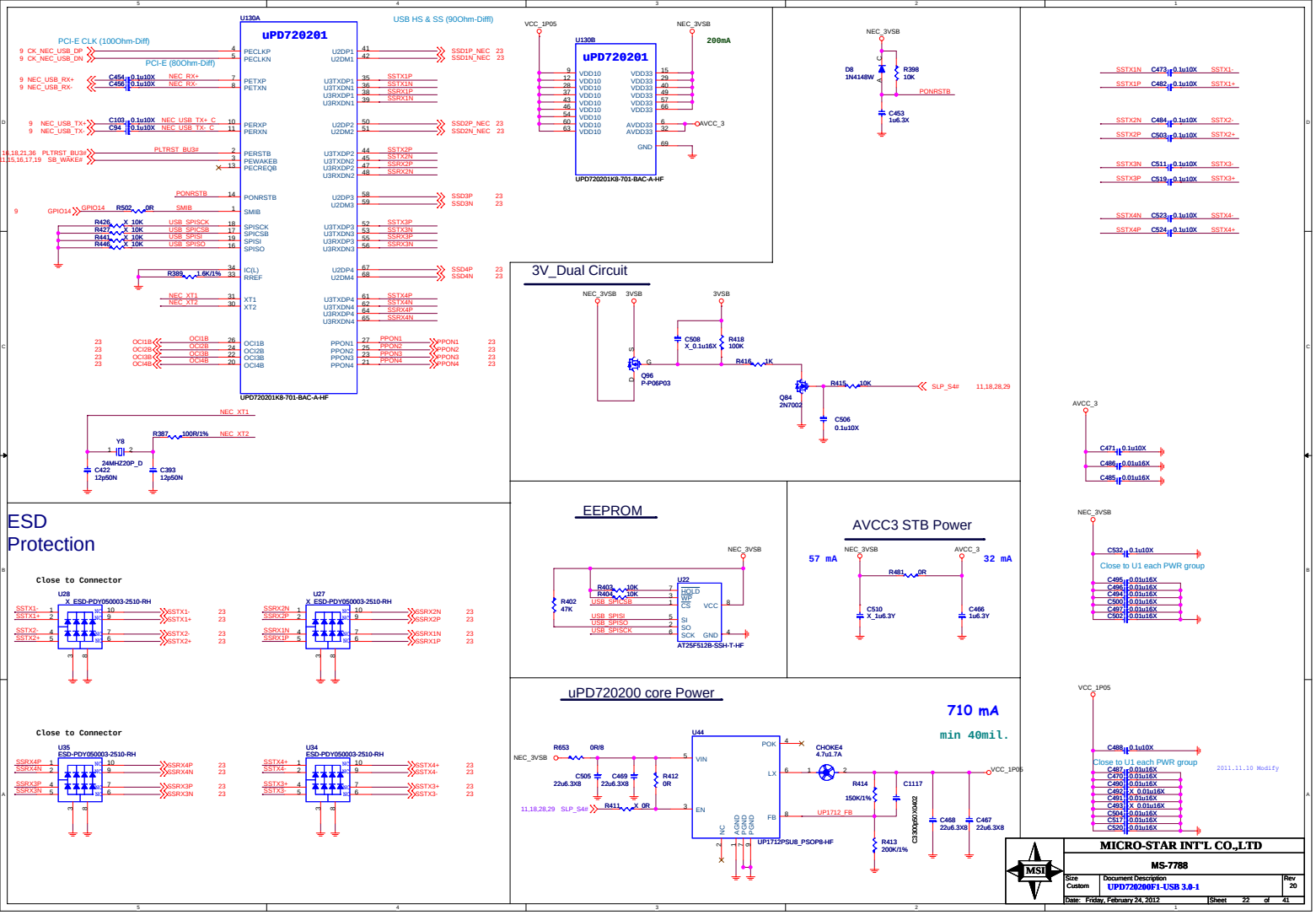
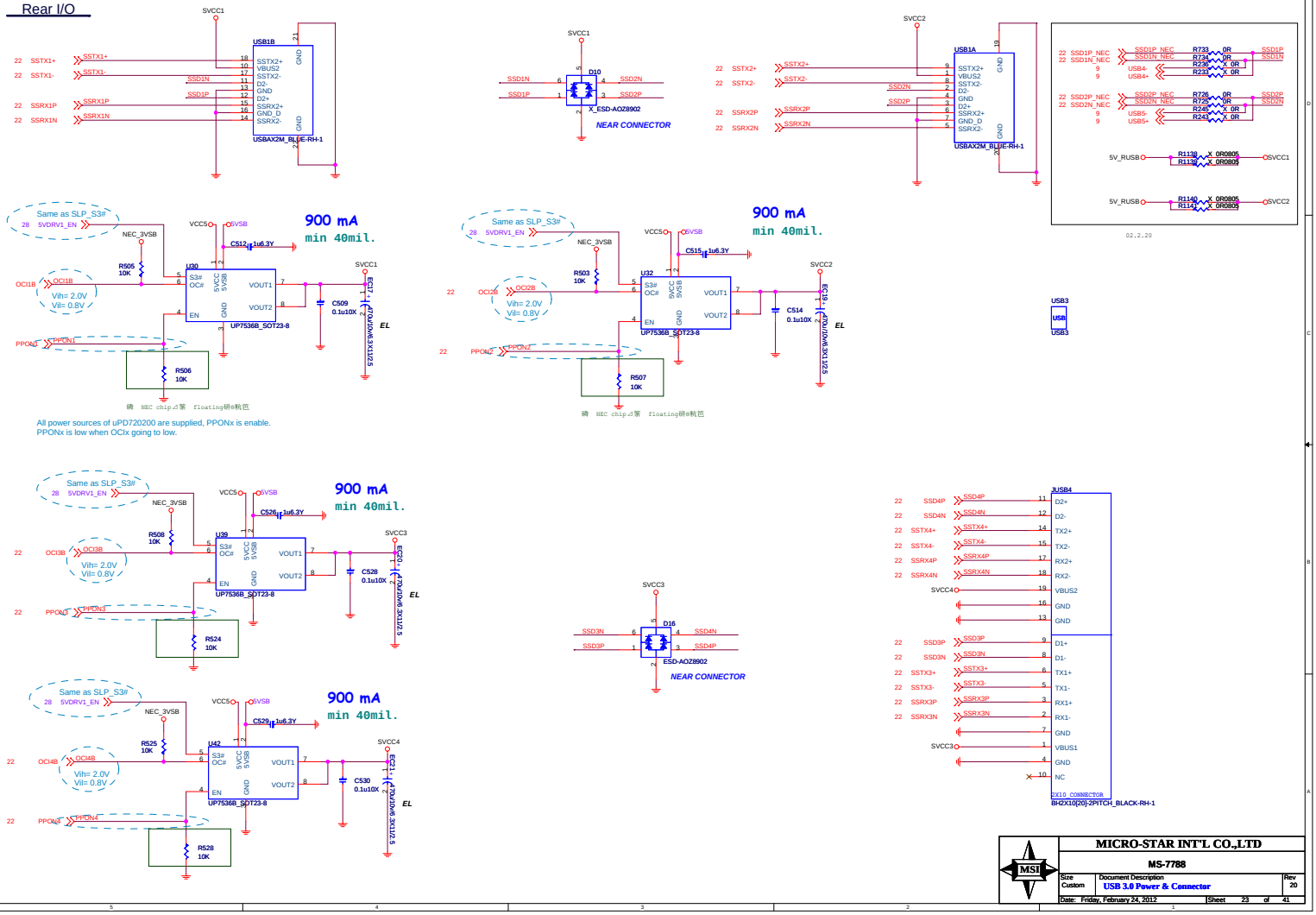
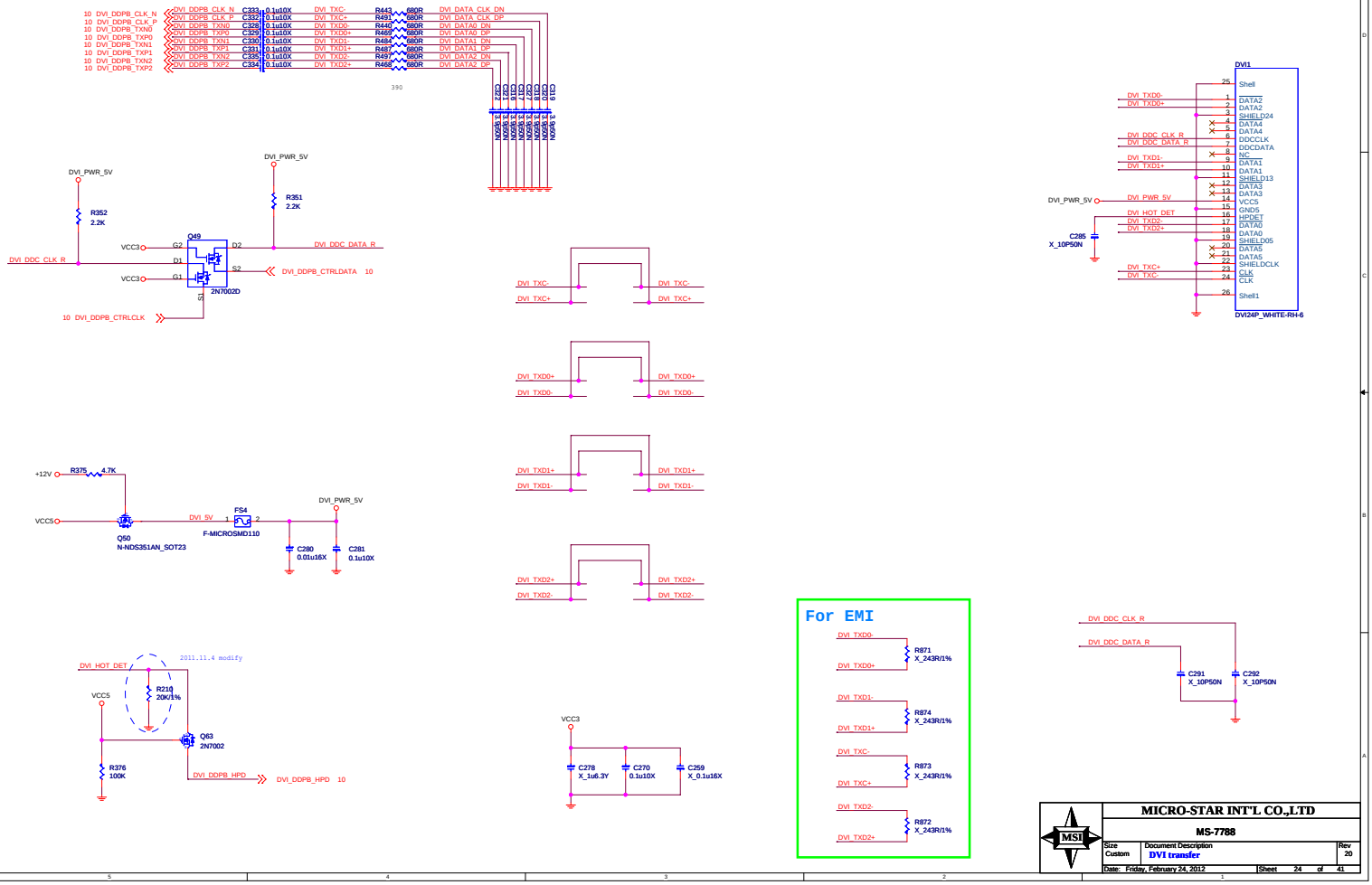
WW





DVI level shifter

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)



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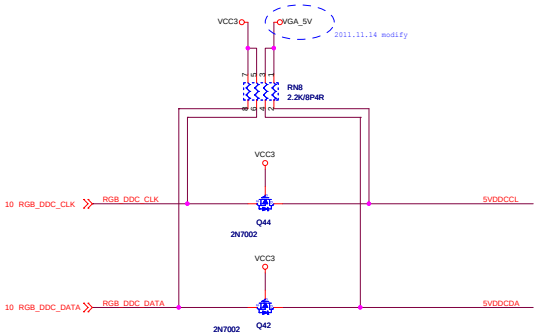
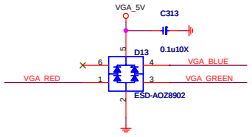
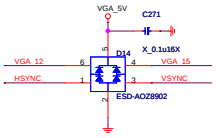
D-Sub

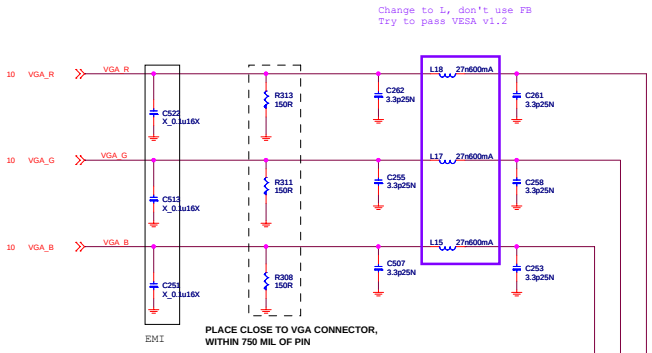
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

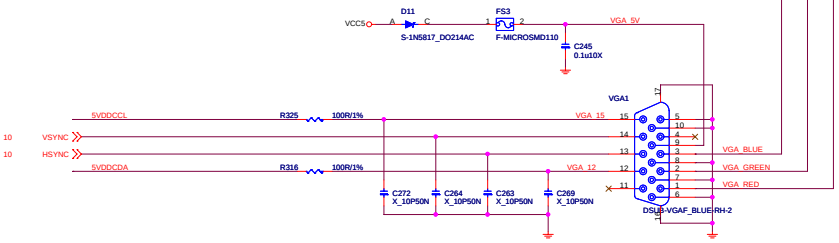
Level shift











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SATA 6G PORT 0,1 H61 PORT 0/1 Support 3G
H67 PORT 0/1 Support 6G

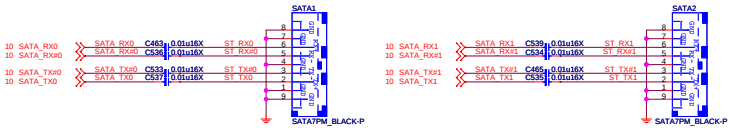
Table 1-3. Desktop Intel® 6 Series Chipset SKUs

Feature Set	SKU Name(s)					
	Q67	Q65	B65	H67	P67	H61
Total number of SATA ports	6	6	6	6	6	4
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)	2[4]	1[5]	1[5]	2[4]	2[4]	0
• SATA Ports (3 Gb/s and 1.5 Gb/s only)	4	5	5	4	4	4[8]

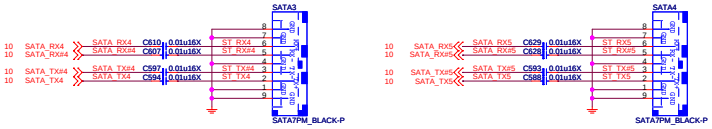
NOTES:

8. SATA ports 2 and 3 are disabled.

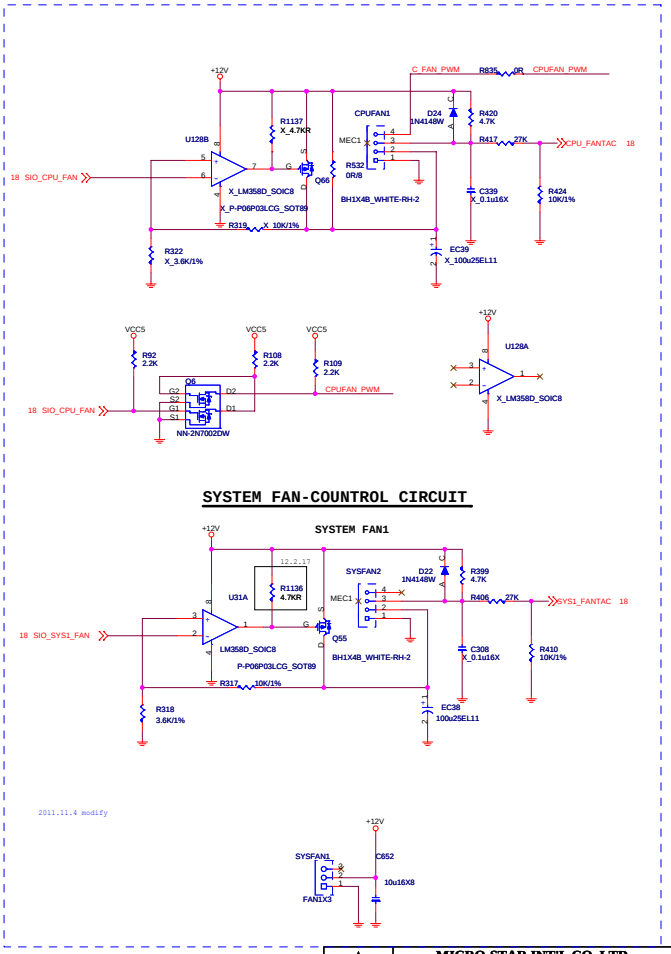
SATA 3G PORT 0,1



SATA 3G PORT 4,5



CPU FAN-COUNTROL CIRCUIT



SYSTEM FAN-COUNTROL CIRCUIT

2011.11.4 modify

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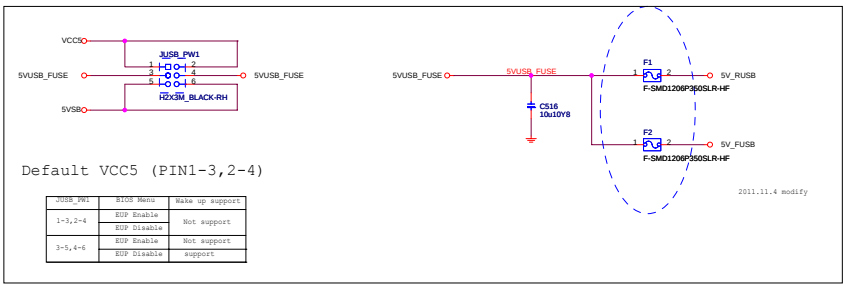
5V_RUSB Switch

5V_RUSB must 120mm



12.2.16

Default VCC5 (PIN1-3,2-4)

JUSB_PW1	BIOS Menu	Wake up support
1-3,2-4	EUP Enable	Not support
	EUP Disable	
3-5,4-6	EUP Enable	Not support
	EUP Disable	support

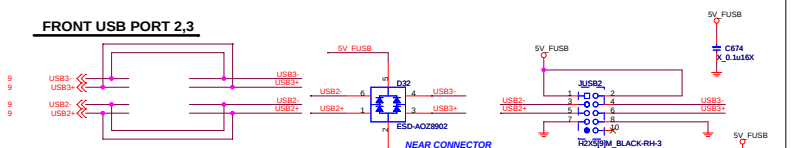
Front USB Connector

NEAR USB Front CONNECTOR

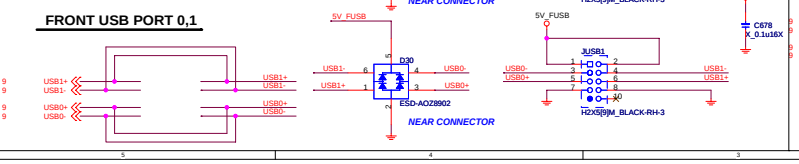
For H61 6,7,12,13 Port should be remove

12.2.15

FRONT USB PORT 2,3

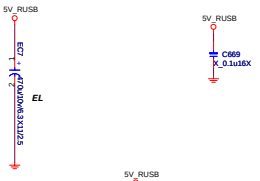


FRONT USB PORT 0,1

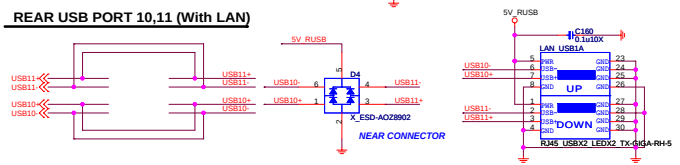


Rear USB Connector

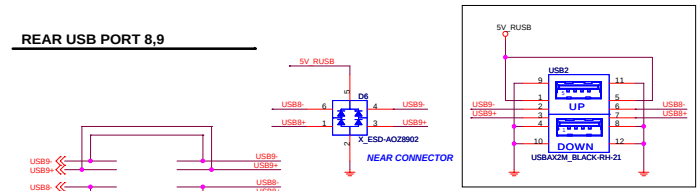
NEAR USB REAR CONNECTOR



REAR USB PORT 10,11 (With LAN)



REAR USB PORT 8,9



12.2.15

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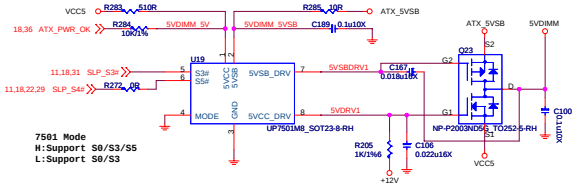
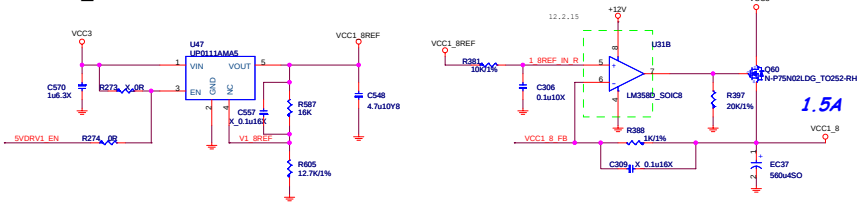
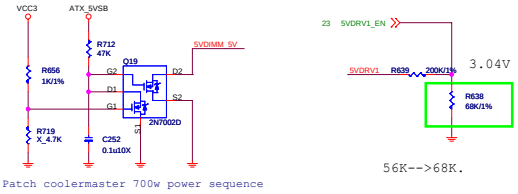
5VDIMM FOR DDR



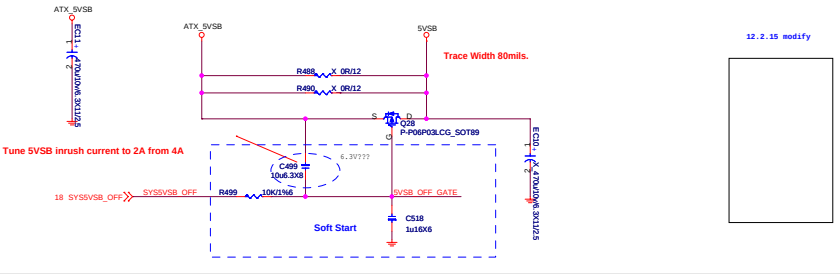
VCC1_8REF



USB MODE

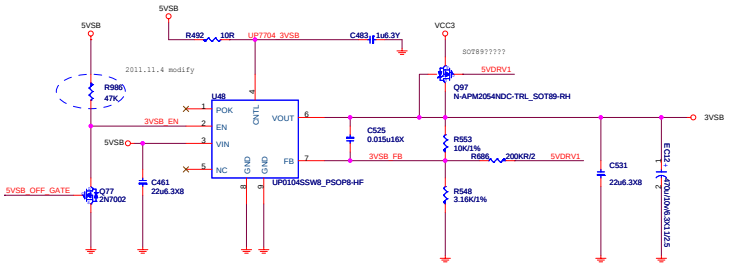


5VSB Power Switch



3VSB

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



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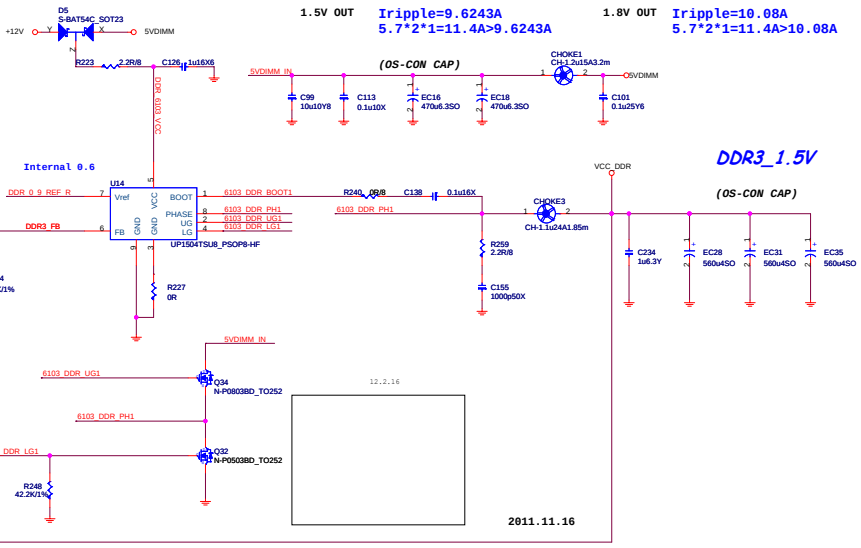
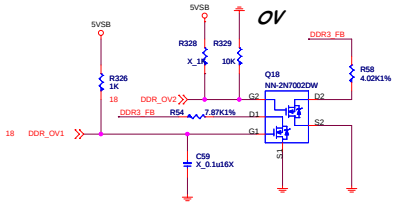
DDR3_1.5V 4.5A+7.5A+1A=21A

4.5A FOR CPU
7.5A FOR 2DIMM
1A FOR DDR VTT
8A FOR PCH Core Power

1.5V OUT Iripple=9.6243A
5.7*2*1=11.4A>9.6243A

1.8V OUT Iripple=10.08A
5.7*2*1=11.4A>10.08A

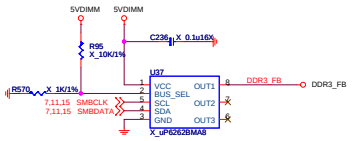




*Default 1.5V

DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01(S/IO)
DDR_OV2 = GPIO02(S/IO)

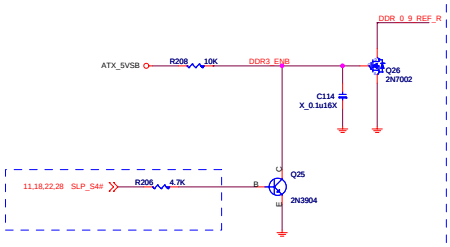


UPI VOLTAGE CONSOLE

0x20:RH=10K,RL=OPEN

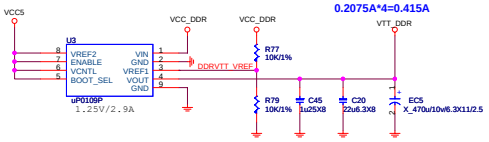
ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

P.S. Only for meet Intel power down sequence.



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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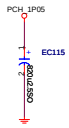
PCH Power:1.05V

PCH Core 6.2A+1.8A=8A



For PCH Core 12.2.21

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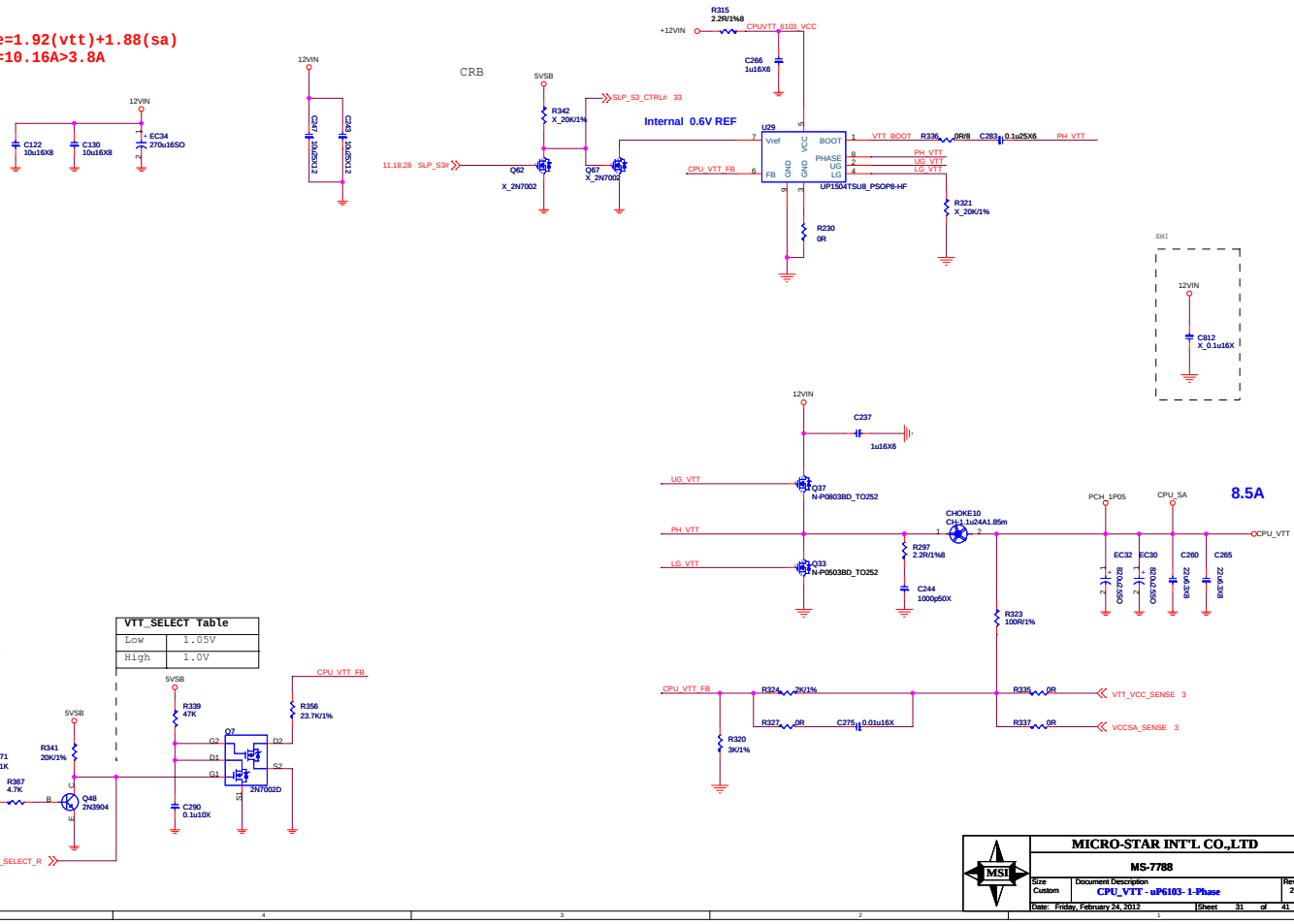
CPU_VTT:1.05/1.00

CPU VTT 8.5A + SA Core =8.8A =17.3A

Iripple=1.92(vtt)+1.88(sa)
5.08*2=10.16A>3.8A



VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V

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CPU_SA:0.925/0.85

SA Core =8.8A

Waitting CPU_VTT Ready

MSI	MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: CPU_SA - uP6103 1-Phase	Rev: 20
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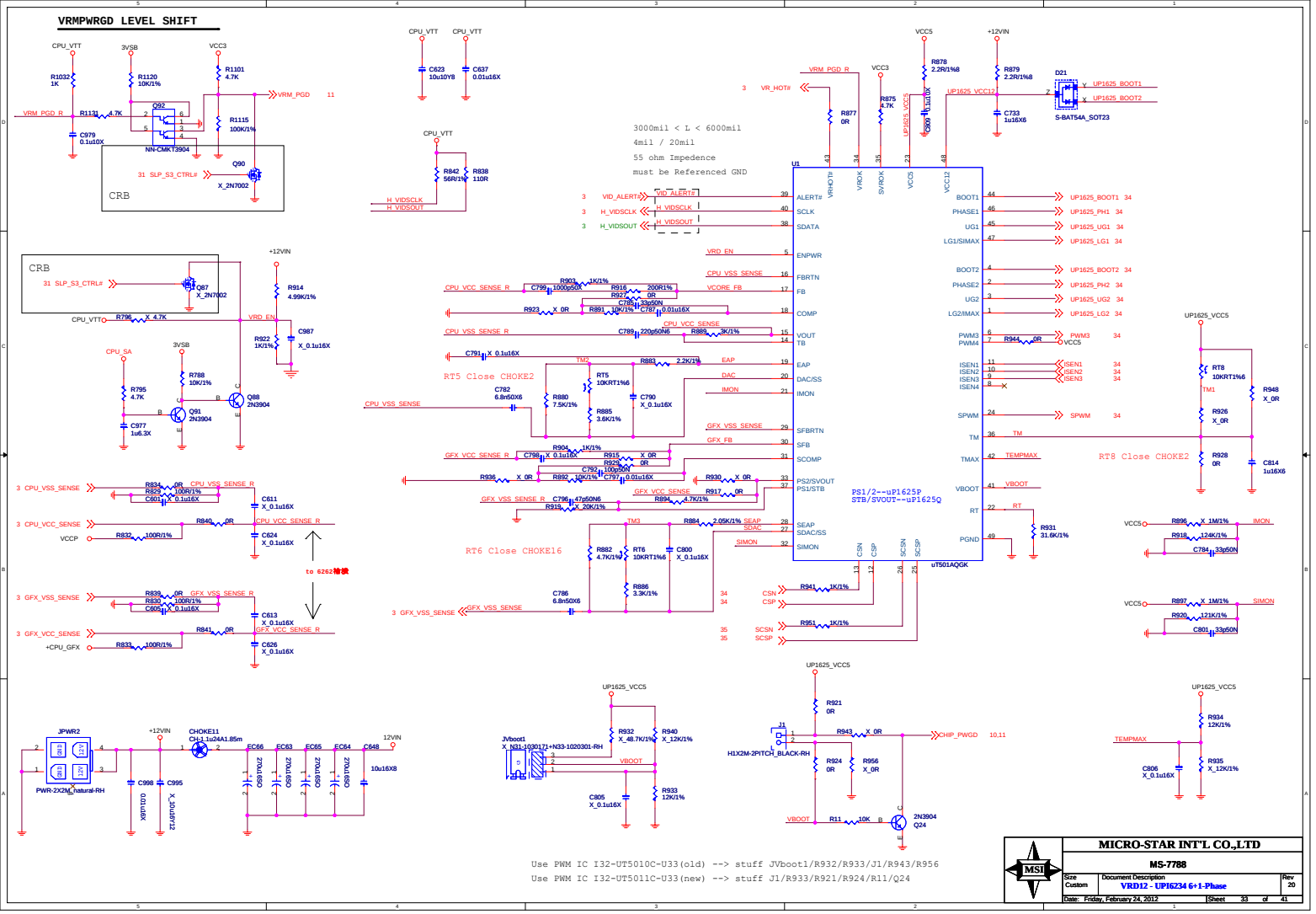

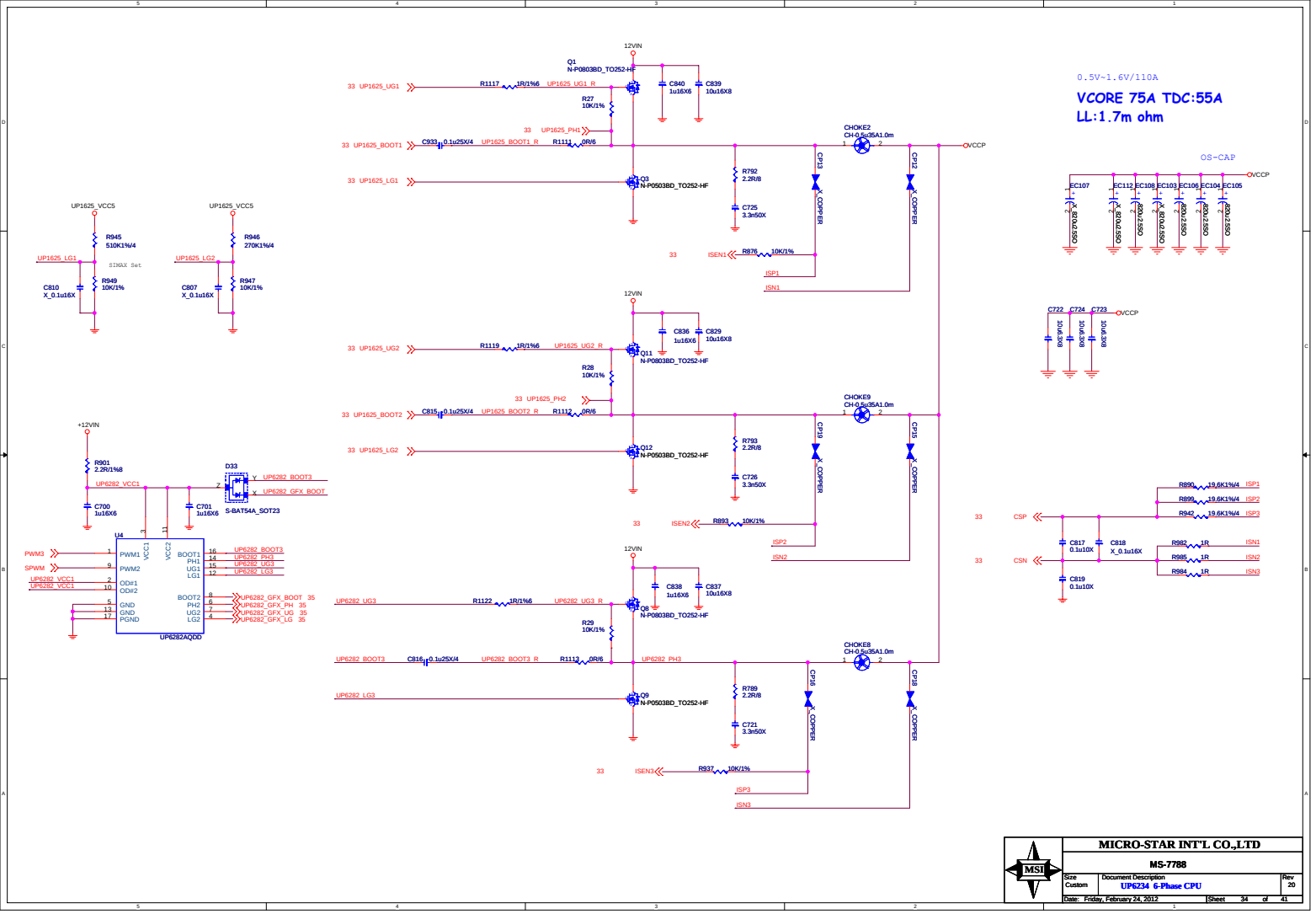

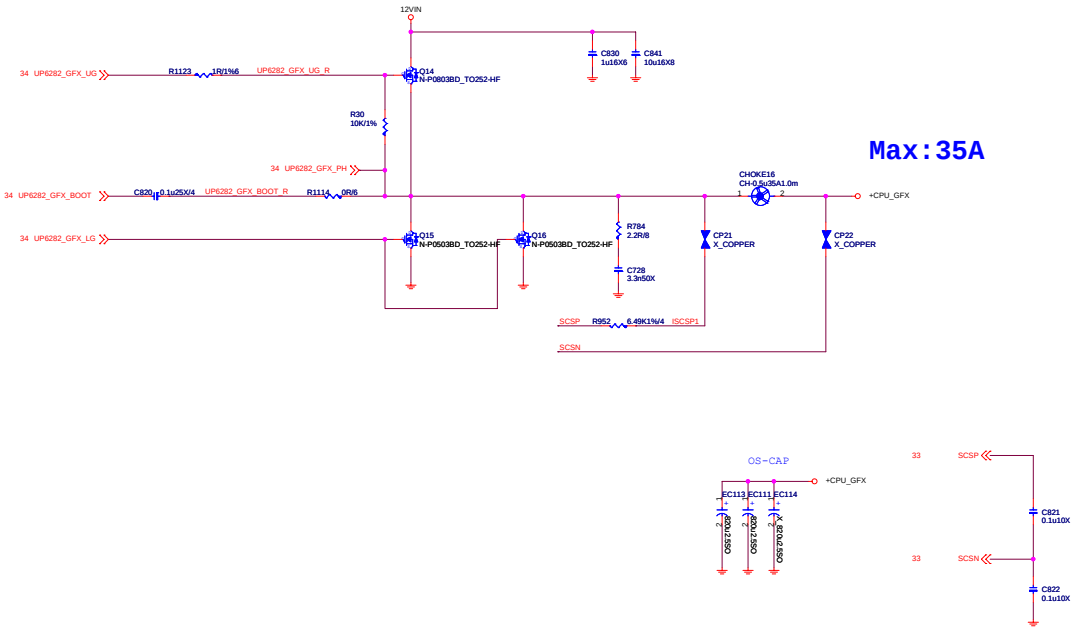

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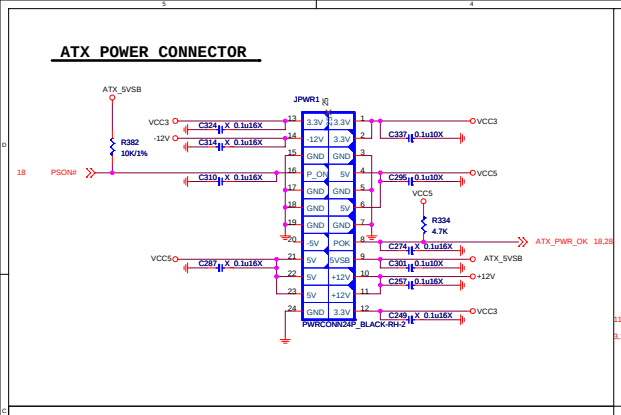

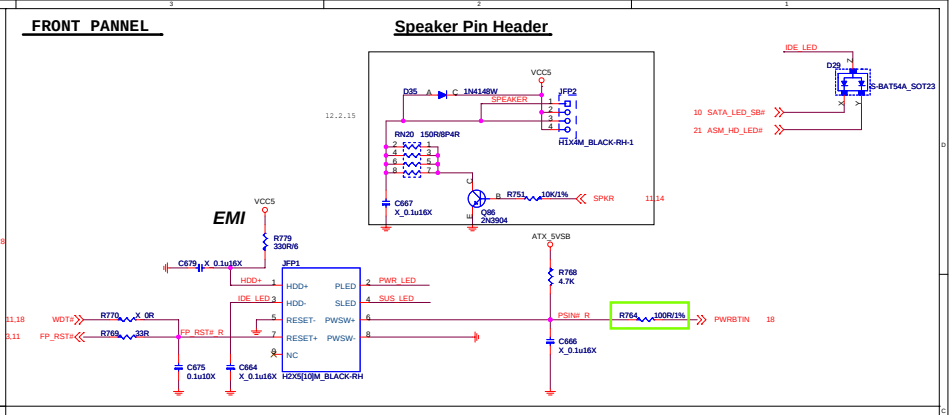

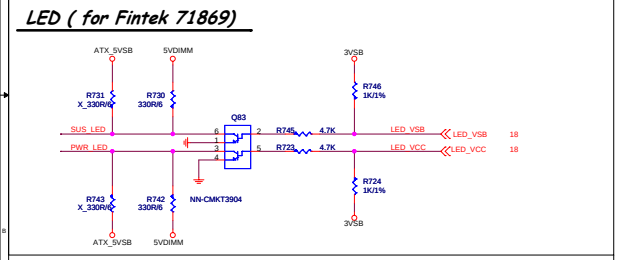

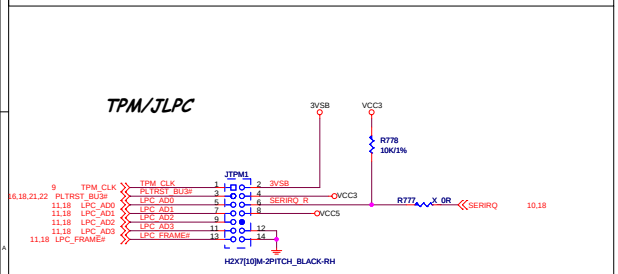

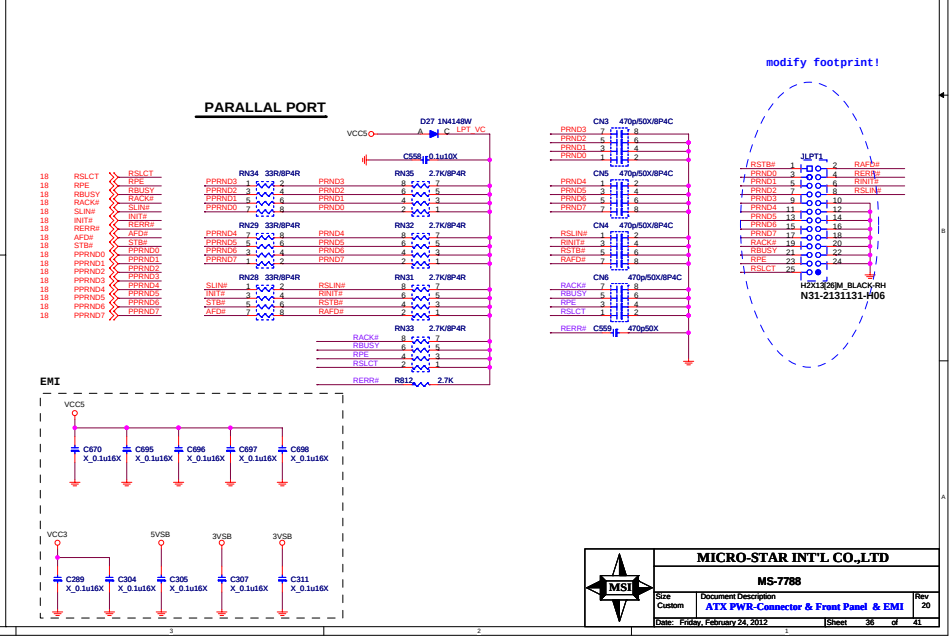

MS-7680-7.0

OPT	Configure	BOM	Function

TAIWAN OSC OPT

EC204 EC205 EC206 EC207

270uF16OS 470uF6.3OS 560uF4OS 820uF2.5OS

AUDIO CON OPT.

AUDIO10

AUDIO

PK/GR/BU/GY/OR/BL

EL/OS OPT.

EC200 EC201 EC202 EC203

270uF16OS 100u16SO 470u6.3SO 100u25EL

LABEL

LA10

Label

LABEL

HDMI_LA1

Label

HDMI LABEL

LA1

AMI_BIOS LABLE

BIOS_LABLE

PCB1

7788-20

BAT1_X1

BAT-BCR2032P-RH

RUB1 RUB2

USB

X_Rubber X_Rubber

CPU_H1

CPU

E21-7557050-L06

THX1

Label

THX

X_THX LABEL

PCH XDP PWRGD/RESET

HS_PCH1

MEC1 MEC2

HS-0403980-RH

Simulation

VCC5

SIM2 SIM1

X_PIN1*2

SIM1 SIM2

X_PIN1*2

Optical Fiducial Marks-120

FM5 FM8 FM2 FM4

FM6 FM7 FM1 FM3

X_FM

Mounting Holes

MH7 MH2 MH4

MH5 MH1

MH8

X_MH001

ASM

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Document Description: XDP / Manual Parts

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