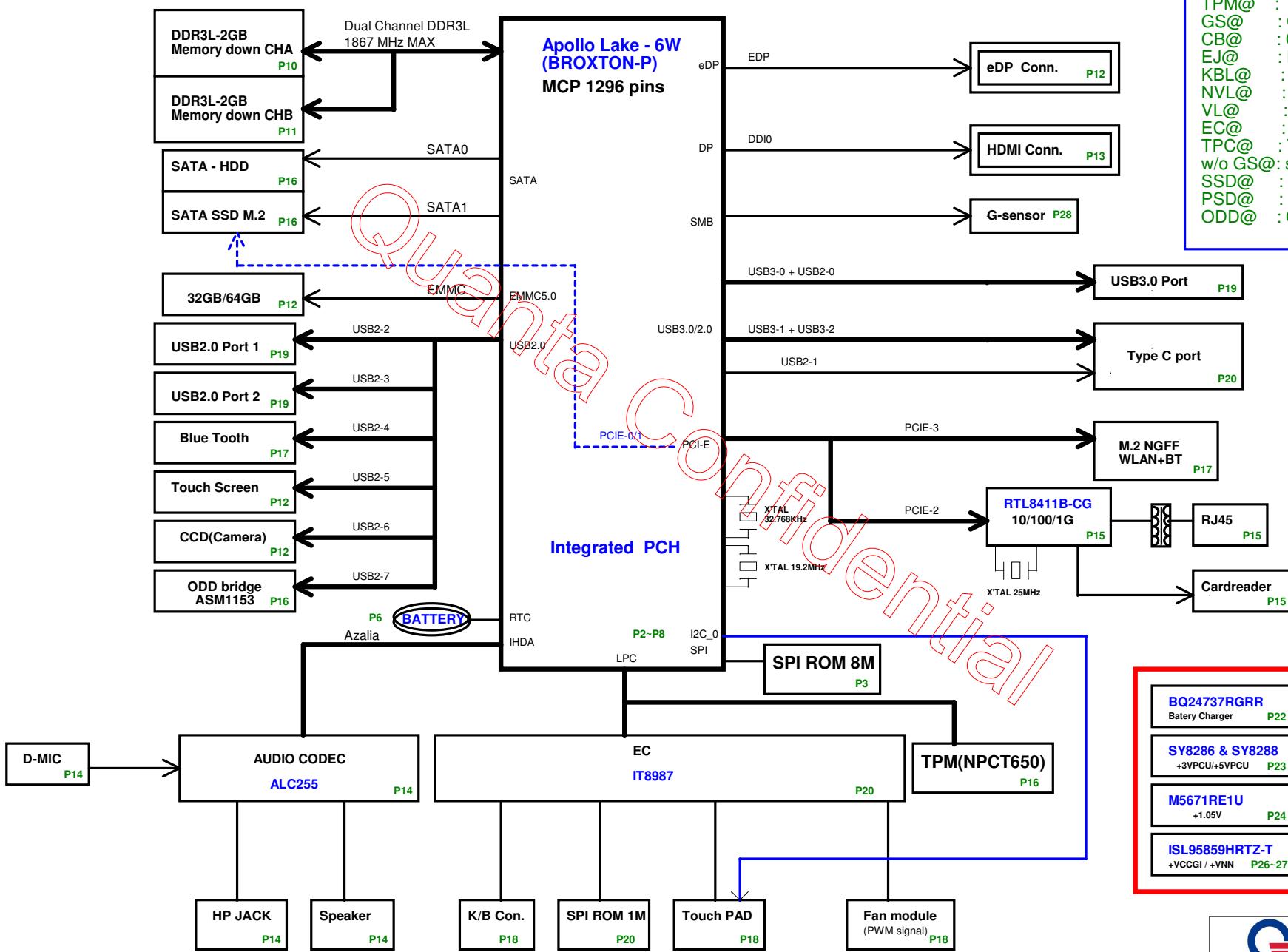


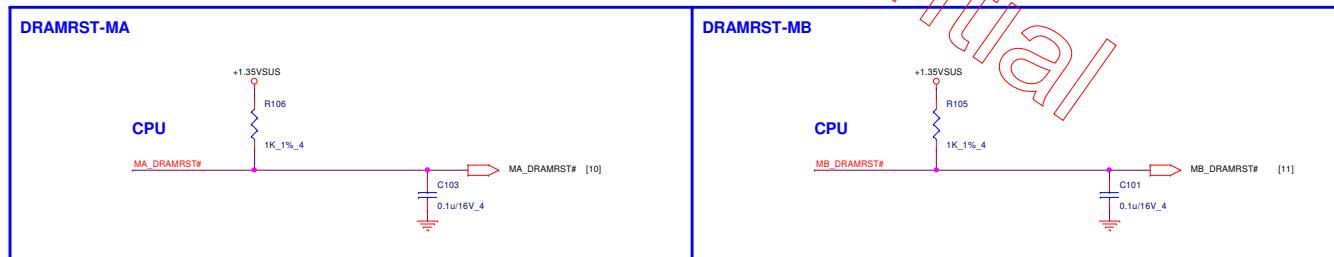
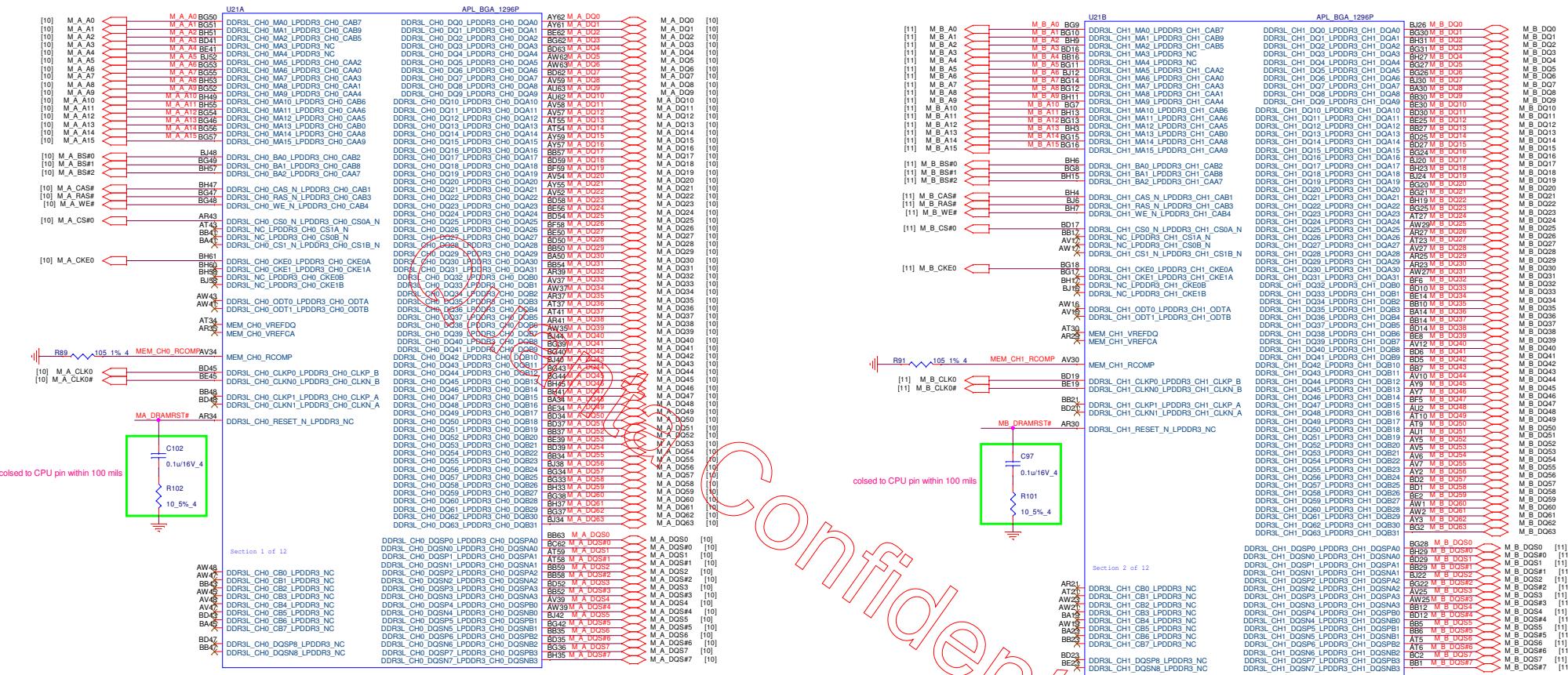
# ZAJ/Z8P/Z8PA SYSTEM BLOCK DIAGRAM

**BOM**

TPM@	: TPM
GS@	: G-SENSOR
CB@	: Cloud book SKU
EJ@	: EJ series SKU
KBL@	: keyboard backlight
NVL@	: none LED panel boost
VL@	: LED panel boost
EC@	: EMMC
TPC@	: Type C function
w/o GS@:	stuff with none GS sku
SSD@	: SATA interface SSD
PSD@	: PCIE interface SSD
ODD@	: ODD function

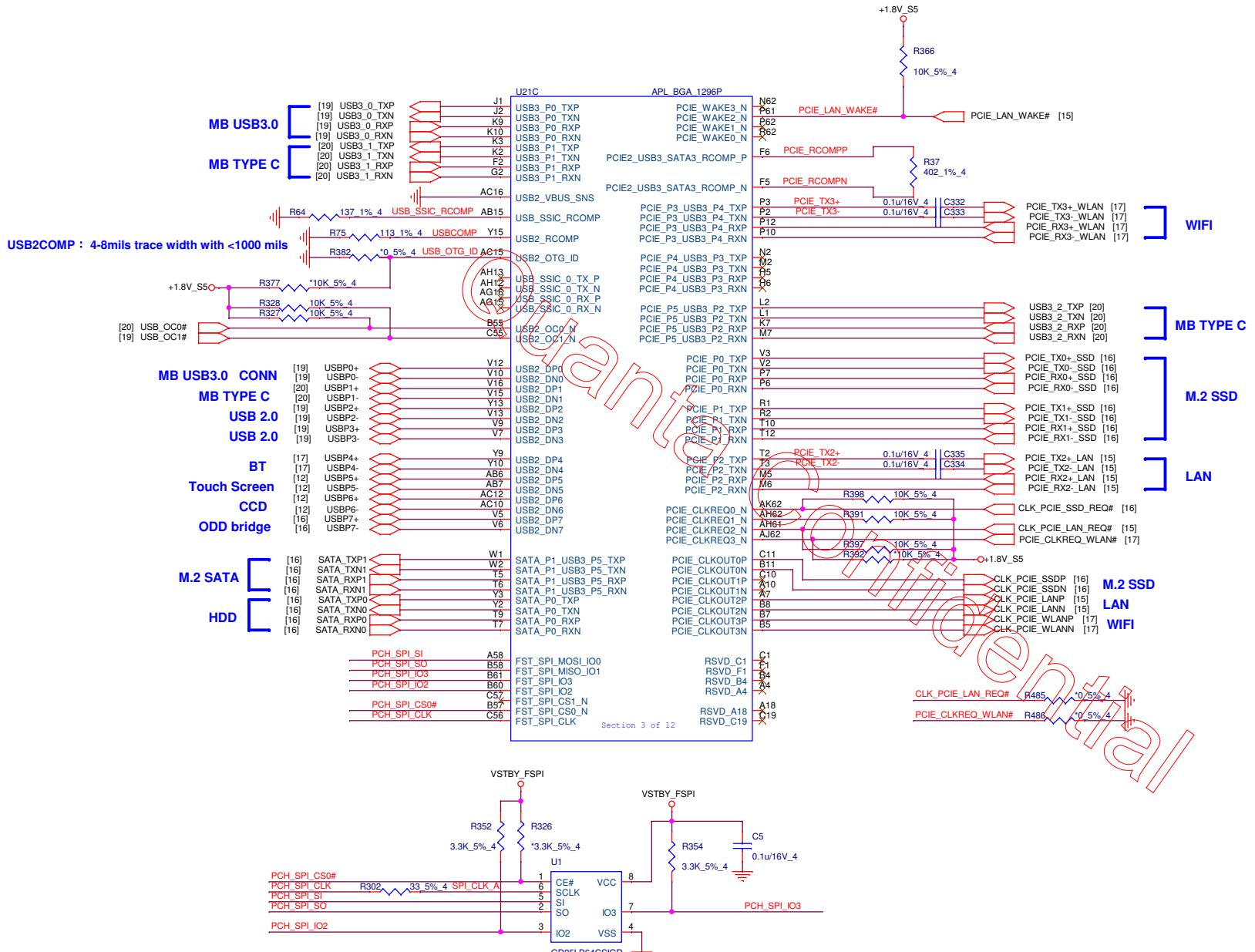
BQ24737RGRR Baty Charger	P22	RT8231BGQW +1.35VSUS	P25
SY8286 & SY8288 +3VPCU/+5VPCU	P23	G5719CTB1U G5719CTB1U G9661MF11U	+1.8V_S5 / +1.24VSUS/+1.5V
M5671RE1U +1.05V	P24		P28
ISL95859HRTZ-T +VCCGI / +VNN	P26~27	Thermal Protection Discharger	P29

## **APL ULT (DDR3L)**



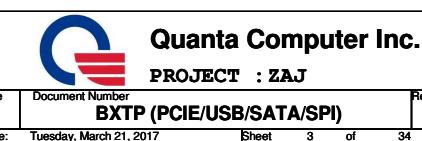
PROJECT : ZAJ		Rev 3A
Size	Document Number	
<b>BXTP (MEMORY)</b>		
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## Apollo lake (SATA , ODD, CLK ,USB,PCIE)

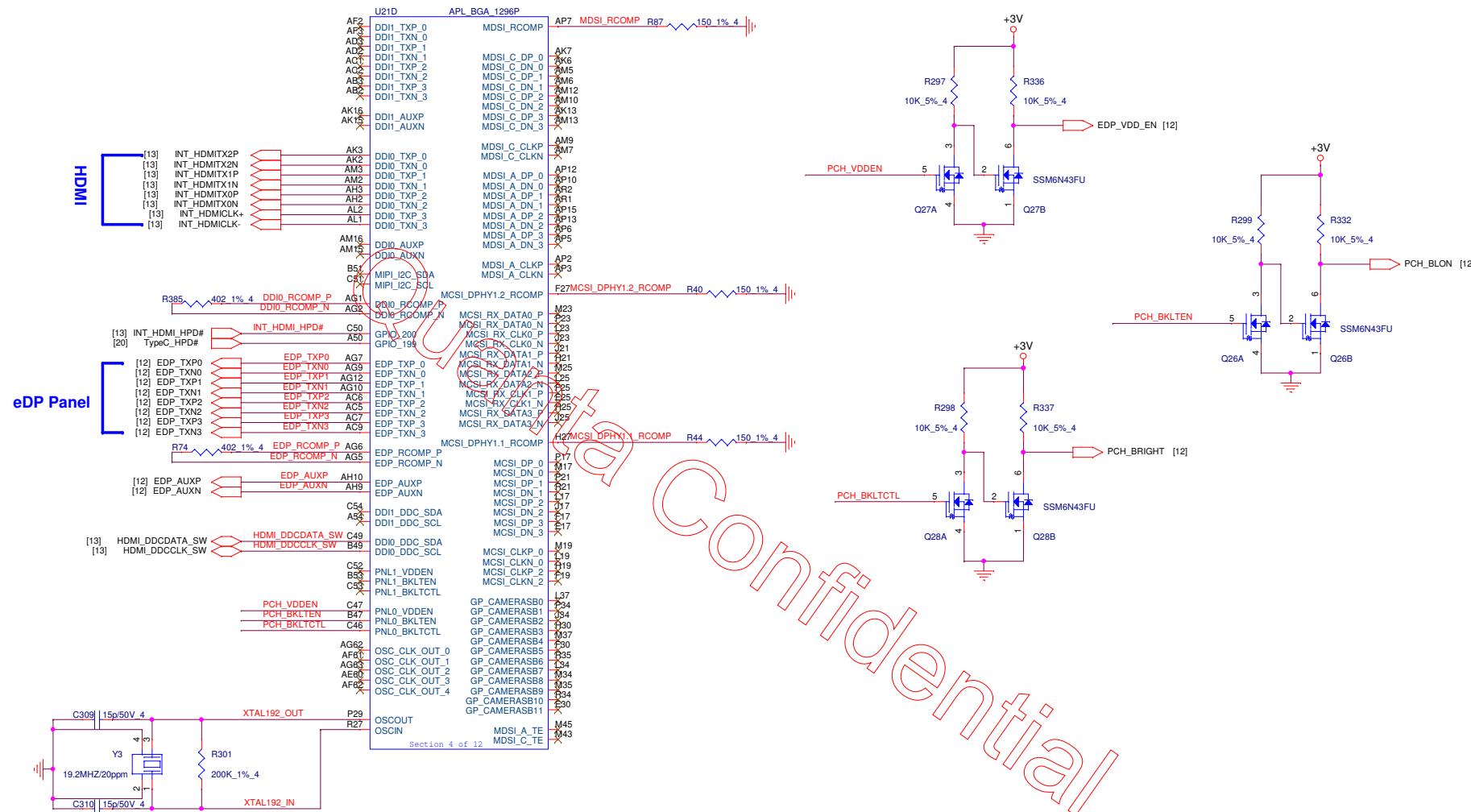


SP@ socket P/N: DFHS08FS023 only for A-TEST

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
1.8V	WND	8M	AKE5EZN0N01	W25Q64FWSSIQ
	GGD	8M	AKE5EG-0Q01	GD25LB64CISIGR

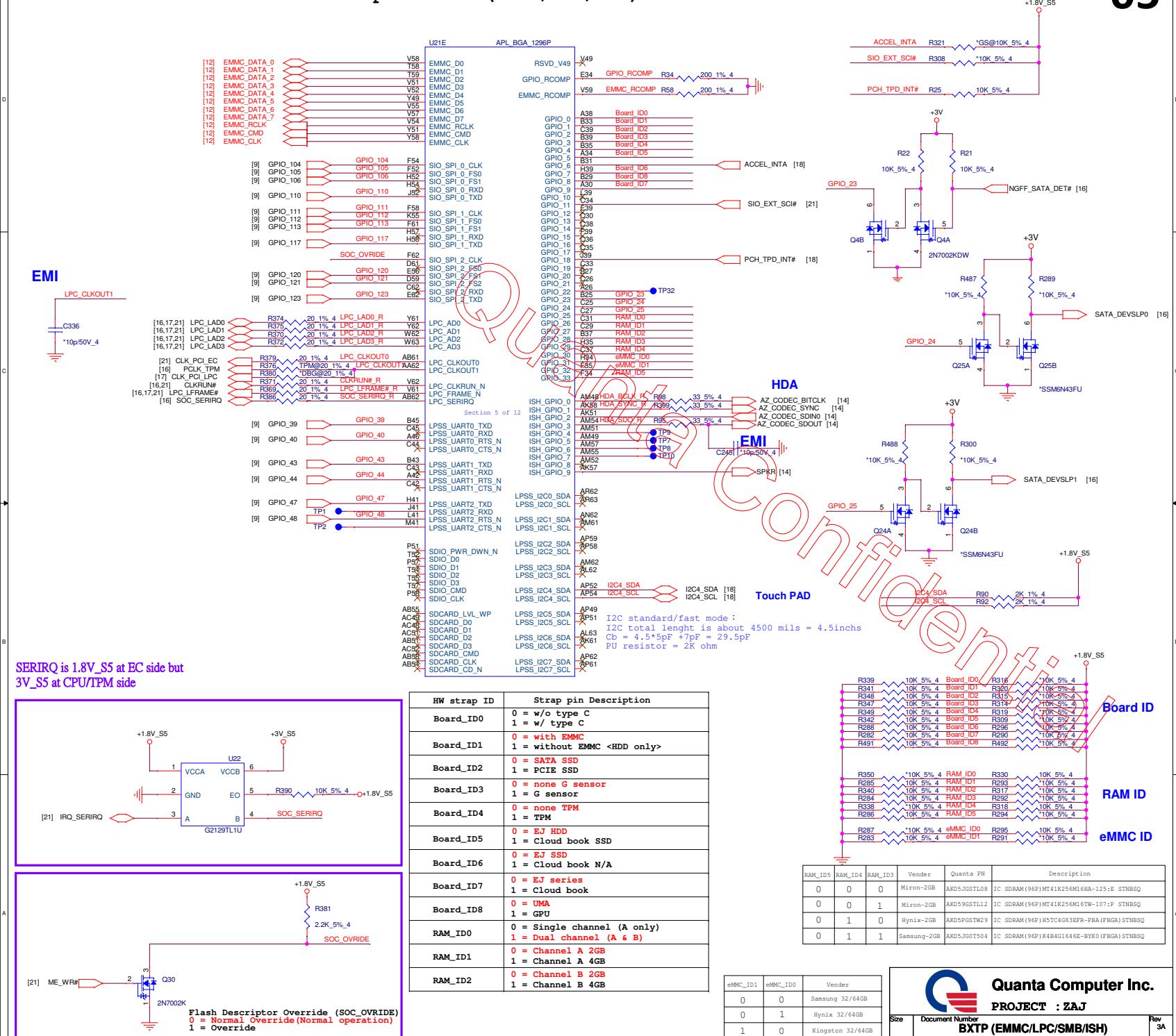


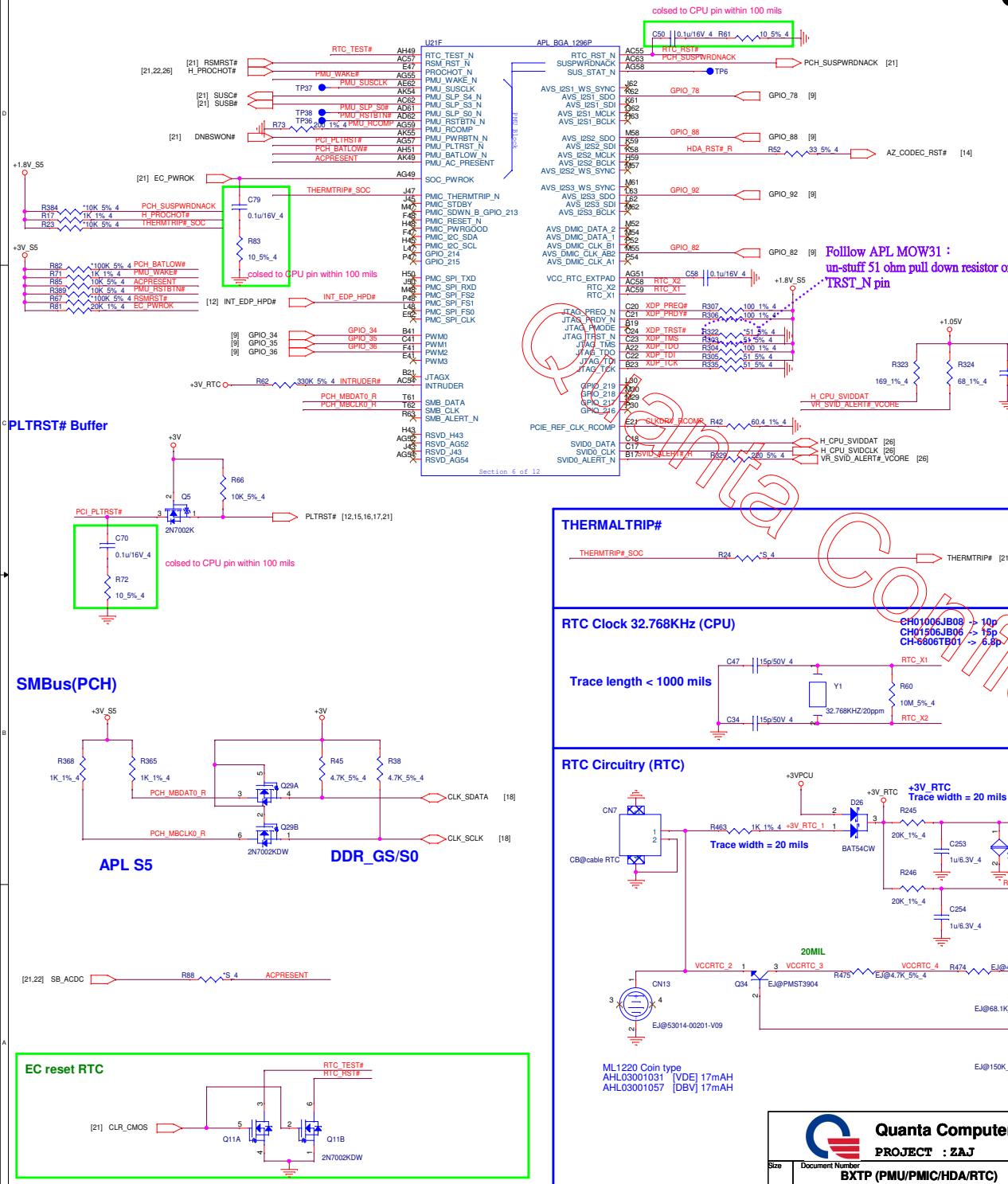
## **Apollolake (DISPLAY, eDP)**



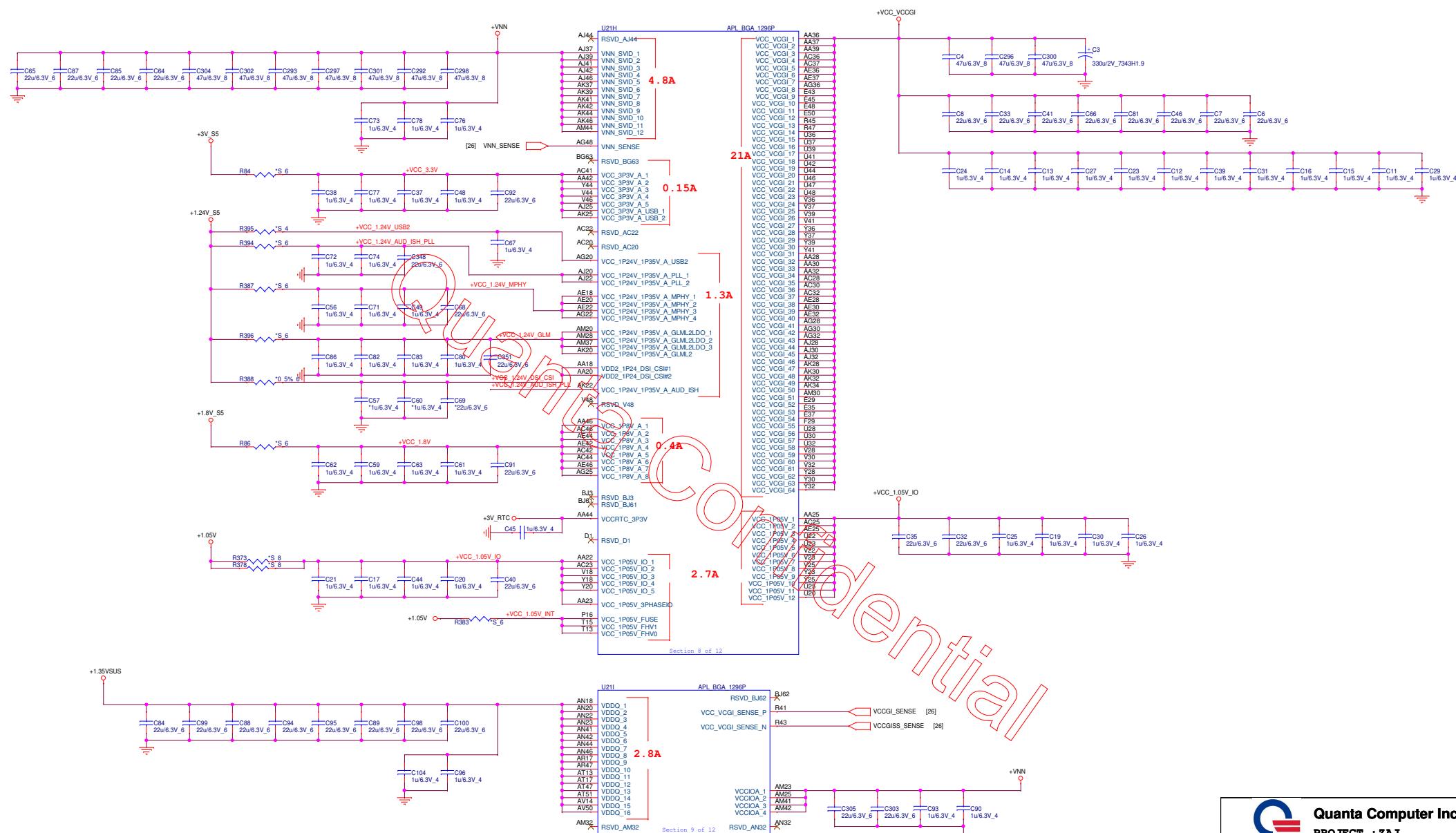
The diagram shows a logic circuit for the PCH\_BKLTCTL signal. It consists of two NMOS transistors, Q28A and Q28B, connected in series between the output node and ground. The drain of Q28A is connected to the source of Q28B. The gate of Q28A is controlled by the PCH\_BKLTCTL signal, while the gate of Q28B is controlled by the inverse of the PCH\_BKLTCTL signal. The source of Q28A is connected to the drain of Q28B. The output node is labeled SSM6N43FU.

## **Apollolake (EMMC/LPC/I2C)**

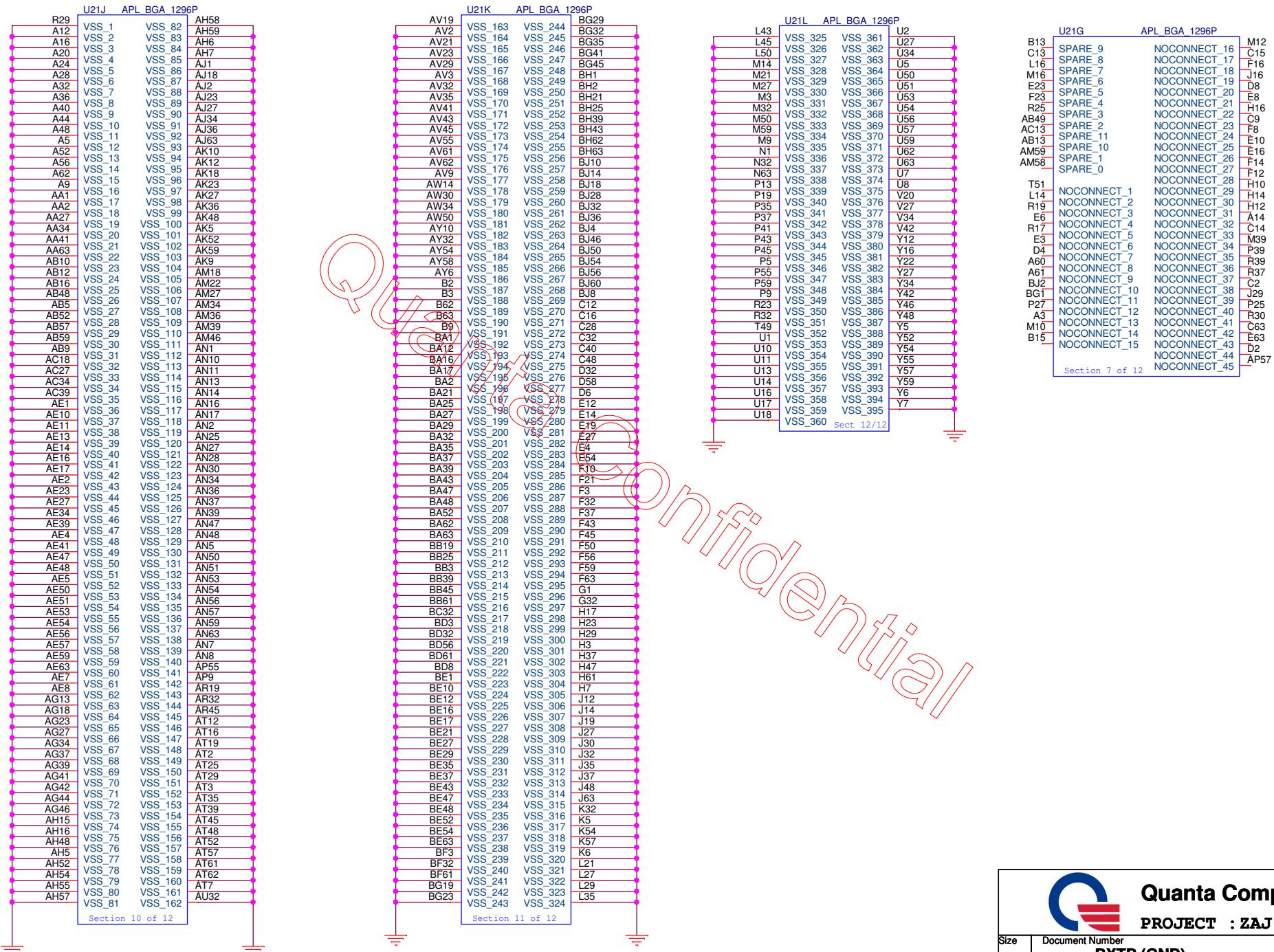




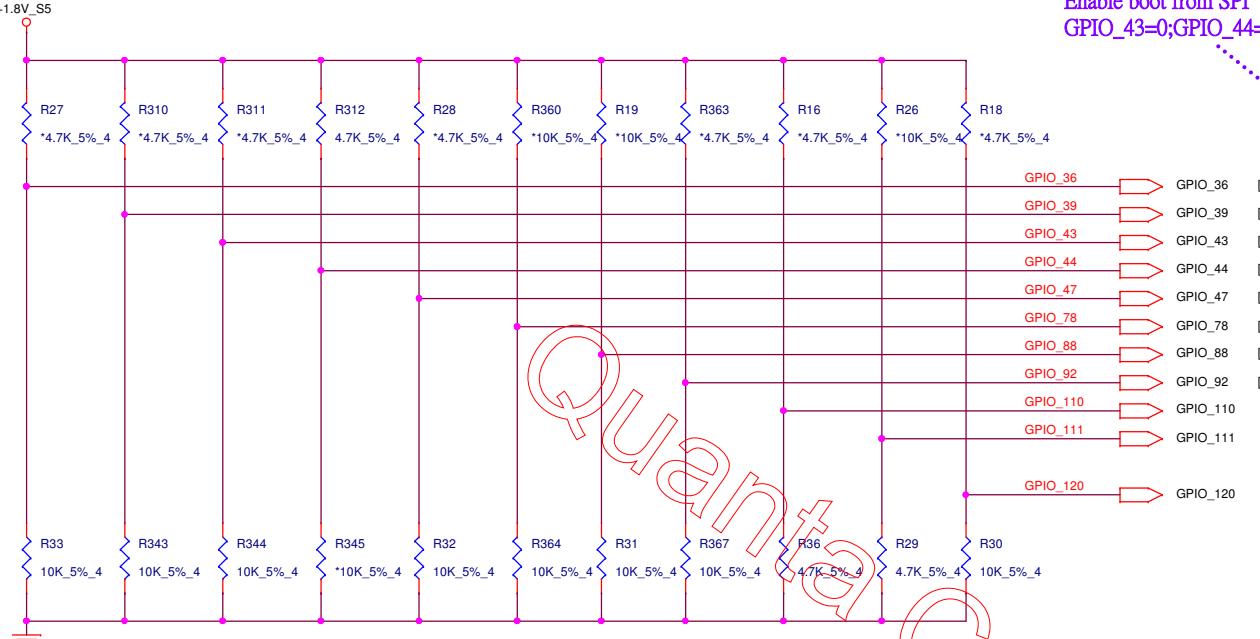
## Apollolake (POWER)



## Apollolake ULT (GND)

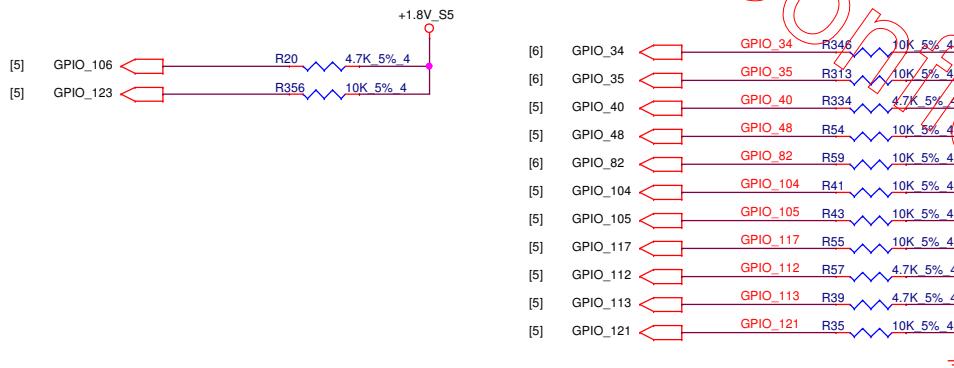


## HARDWARE STRAPS



Follow APL WoW36 :  
Enable boot from SPI  
GPIO\_43=0;GPIO\_44=1

Hardware Strap	Strap Description
GPIO_36	VCC_1P24V_1P35V_A voltage select 0 = 1.24V 1 = 1.35V
GPIO_39	Enable CSE (TXE3.0) ROM Bypass 0 = <b>Disable Bypass</b> 1 = Enable Bypass
GPIO_43	Allow eMMC as a boot source 0 = <b>Disable</b> 1 = Enable
GPIO_44	Allow SPI as a boot source 0 = Disable 1 = <b>Enable</b>
GPIO_47	Force DNX FW Load 0 = <b>Do not force</b> 1 = Force
GPIO_78	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V 1=buffers set to 1.8V
GPIO_88	PMU 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode
GPIO_92	SMBus No Re-Boot 0 = <b>Disable (default)</b> 1 = Enable
GPIO_110	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode
GPIO_111	Boot BIOS Strap 0 = <b>Boot from SPI</b> 1 = Do not boot from SPI
GPIO_120	Top swap override 0 = <b>Disable</b> 1 = Enable

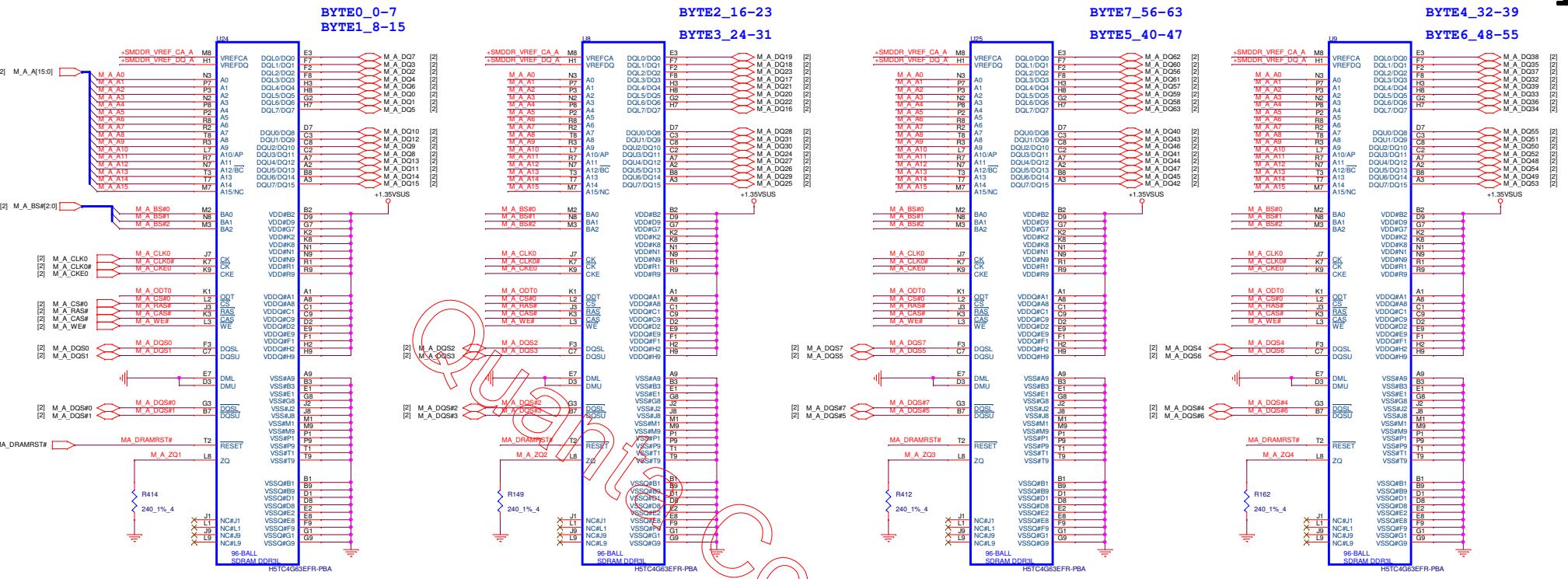


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BROJECT : ZAI

Size	Document Number	<b>HARDWARE STRAPS</b>			Rev 3A
Date:	Tuesday, March 21, 2017	Effect:	0	of	24

#### On board memory (OBM)



## **DE-CAPS FOR MEMORY CHANNEL A**

## ~~VTT TERMINATIONS~~

## **VREF\_CA-DQ CIRCUIT**

Distributed around all DRAM devices (CHA)

10u/6.3V\_4 10u/6.3V\_4 10u/6.3V\_4 10u/6.3V\_4 10u/6.3V\_4 10u/6.3V\_4

**Place these Caps near each X16 Memory Down**

1u/6.3V\_4 1u/6.3V\_4 1u/6.3V\_4 1u/6.3V\_4 1u/6.3V\_4 1u/6.3V\_4

C365 C361 C356 C357 C354 C369

Digitized by srujanika@gmail.com

A timing diagram illustrating four identical digital pulses. Each pulse consists of a high state followed by a low state. The labels above the pulses are: 1u/6.3V\_4, 1u/6.3V\_4, 1u/6.3V\_4, and 1u/6.3V\_4. The diagram shows the signal transitioning from high to low at the start of each pulse and returning to high at the end.

Follow APL WoW37 : Memory Down  
ODT single on DRAM side is pulled up to VDDQ

VREF CA trace at least 20mils wide and space

 +1.35VSUS VREF\_DQ trace at least 20mils wide and space

Figure 1. A schematic diagram of the experimental setup. The light source (labeled 1) is a pulsed laser diode (LD) operating at  $\lambda = 532$  nm. The beam splitter (BS) is a polarizing beam splitter cube. The lens (L) focuses the beam onto the sample stage. The sample stage is a motorized stage with a resolution of  $0.1 \mu\text{m}$ . The objective lens (O) has a magnification of  $\times 100$  and a numerical aperture (NA) of 1.4. The emission light is collected by the objective lens and focused onto the photomultiplier tube (PMT). The PMT is connected to a lock-in amplifier (LIA) and a computer for data processing.

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PROJECT : ZAJ

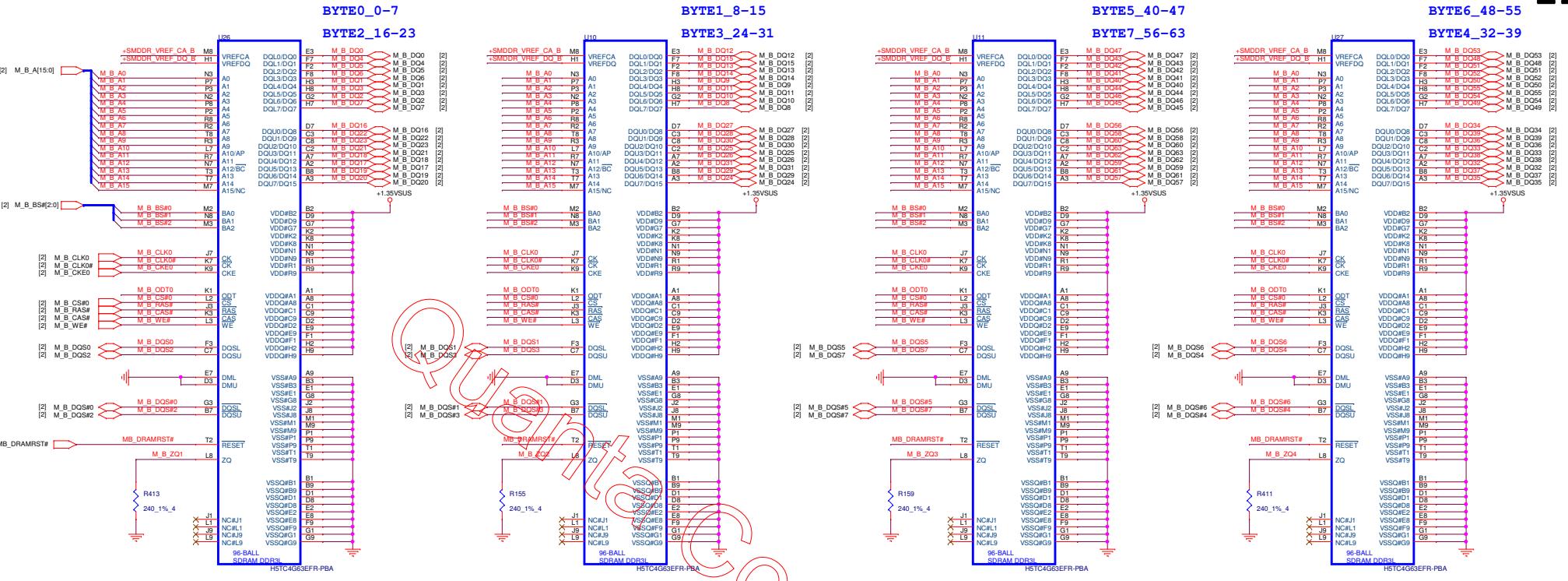
Size Document Number Rev  
DDR3L SODIMM-STD CHA 3A  
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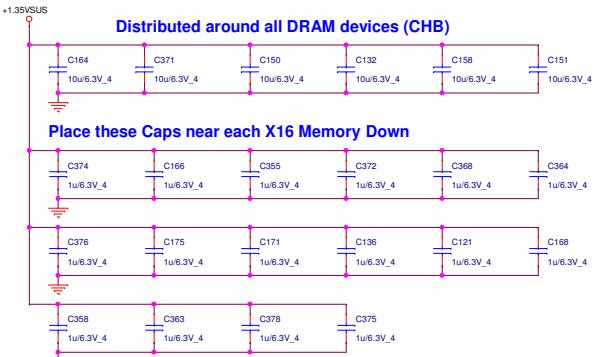
## On board memory (OBM)

## **DDR3L MEMORY CHANNEL B**

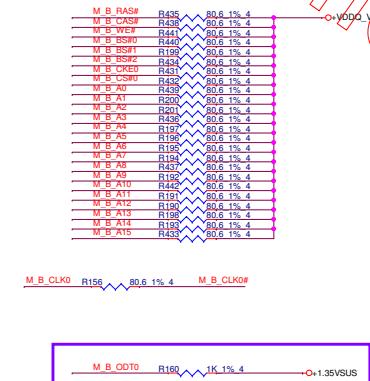
11



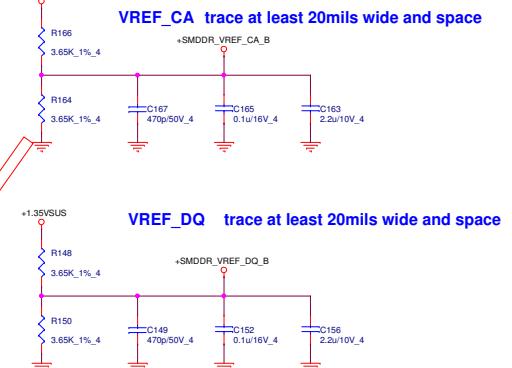
## DE-CAPS FOR MEMORY CHANNEL B

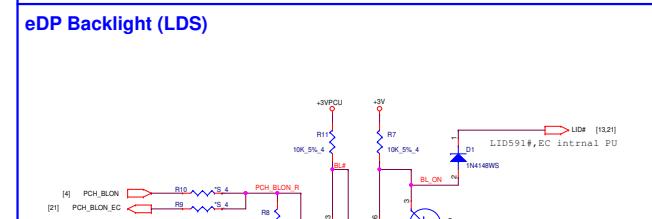
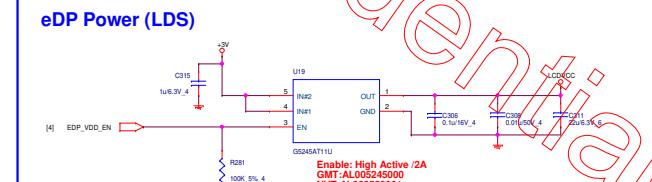
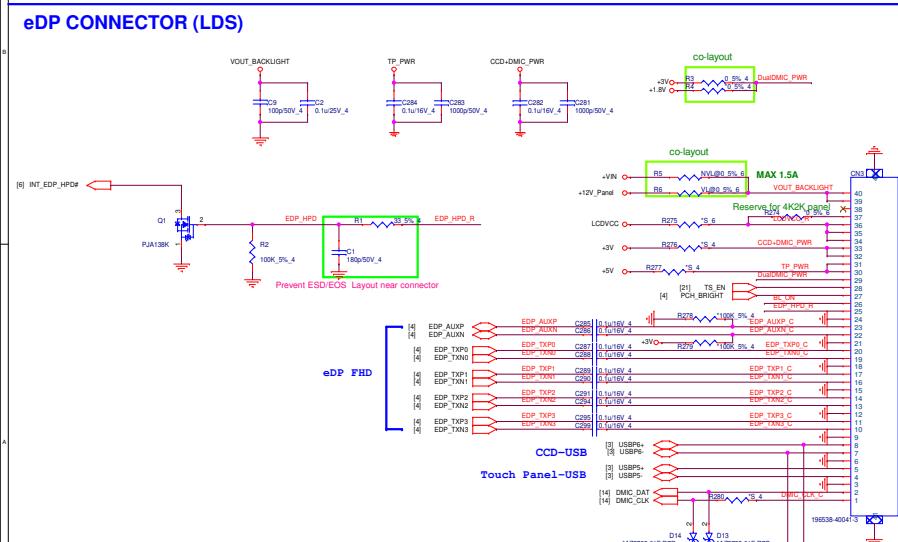
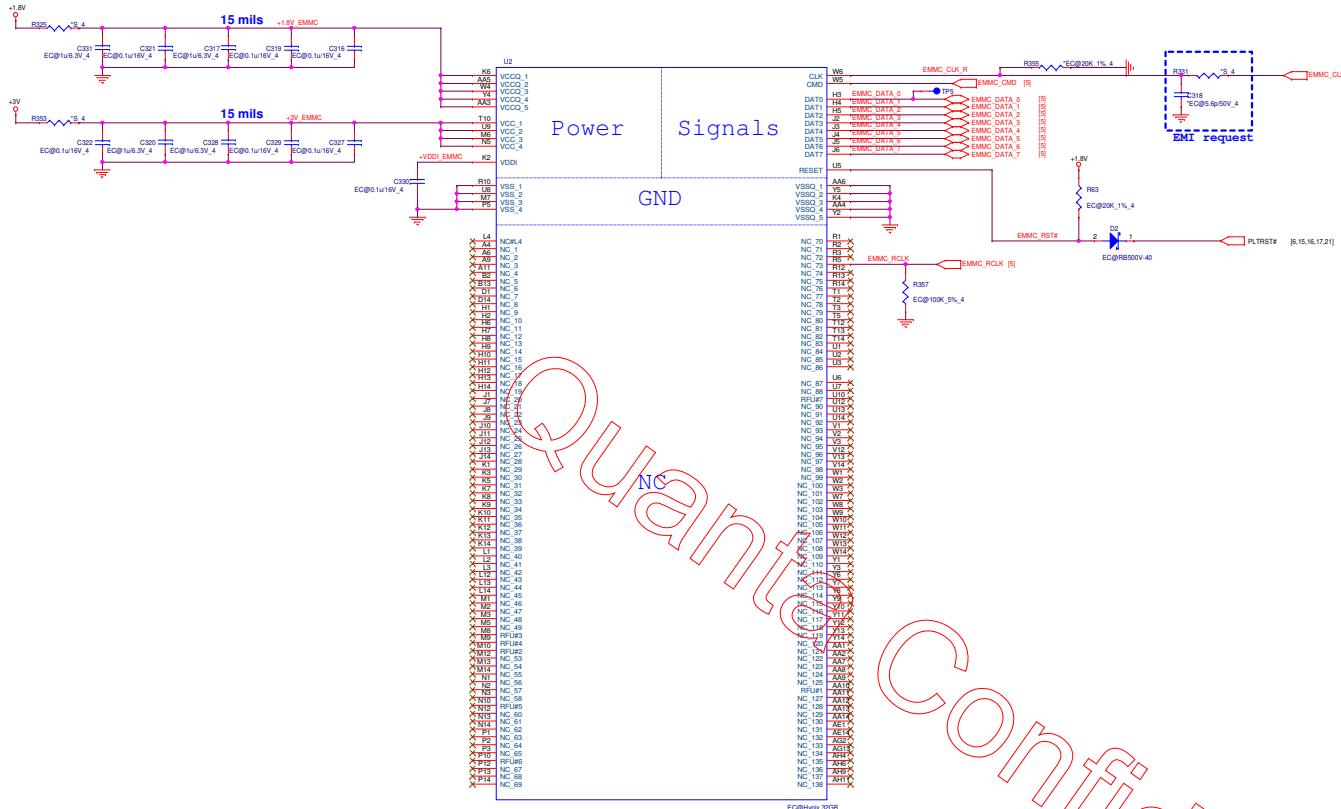


# ~~VTT TERMINATIONS~~



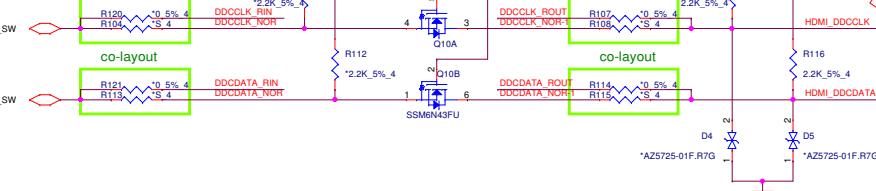
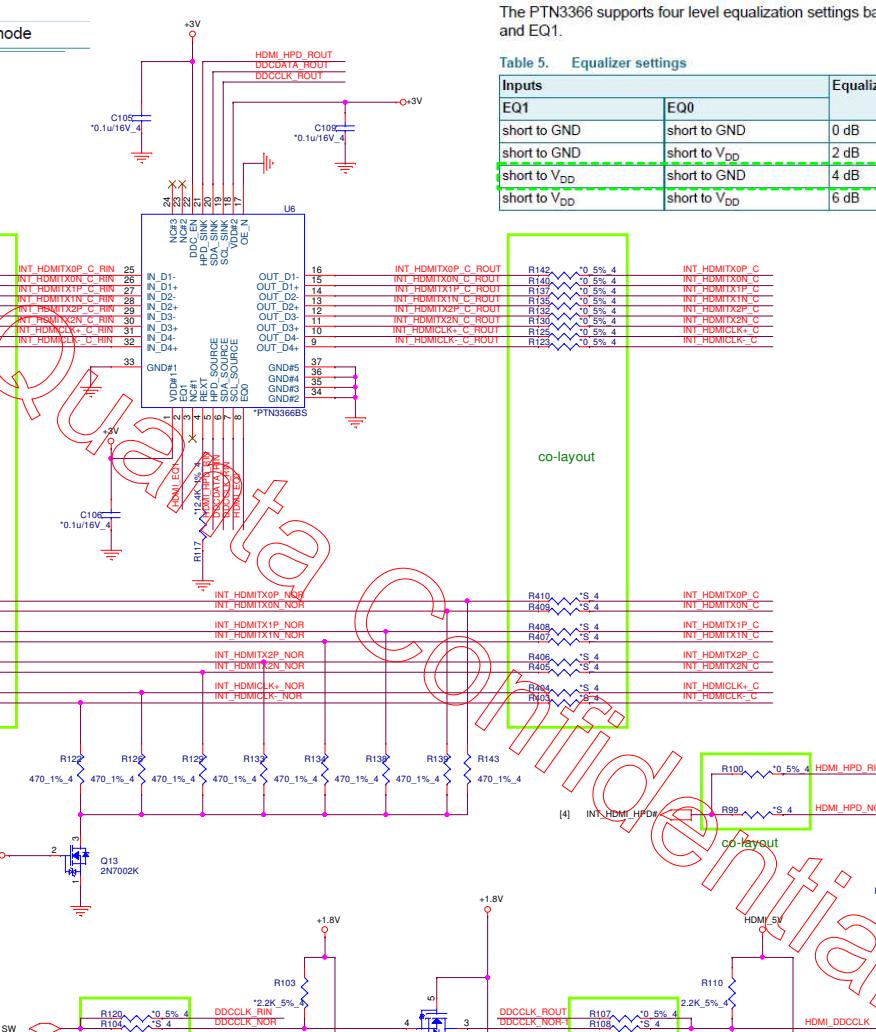
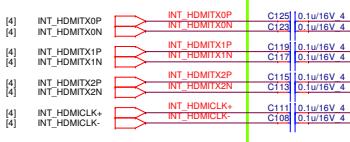
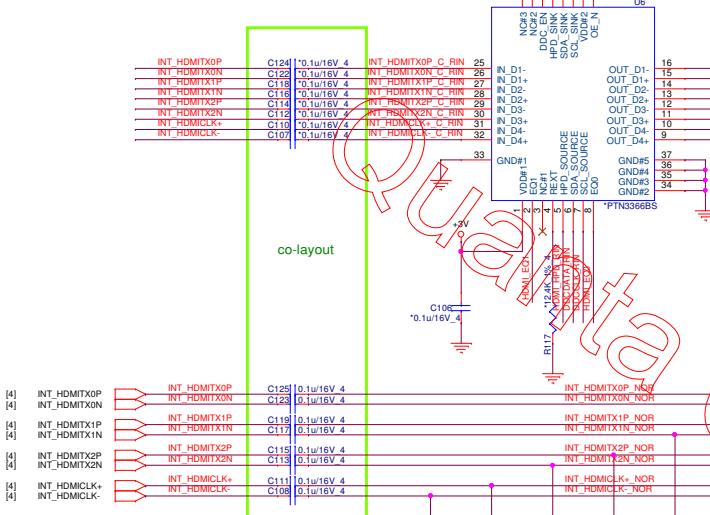
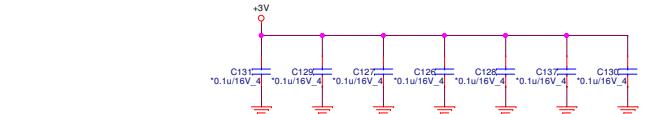
## VREF\_CA-DQ CIRCUIT





## HDMI (HDM)

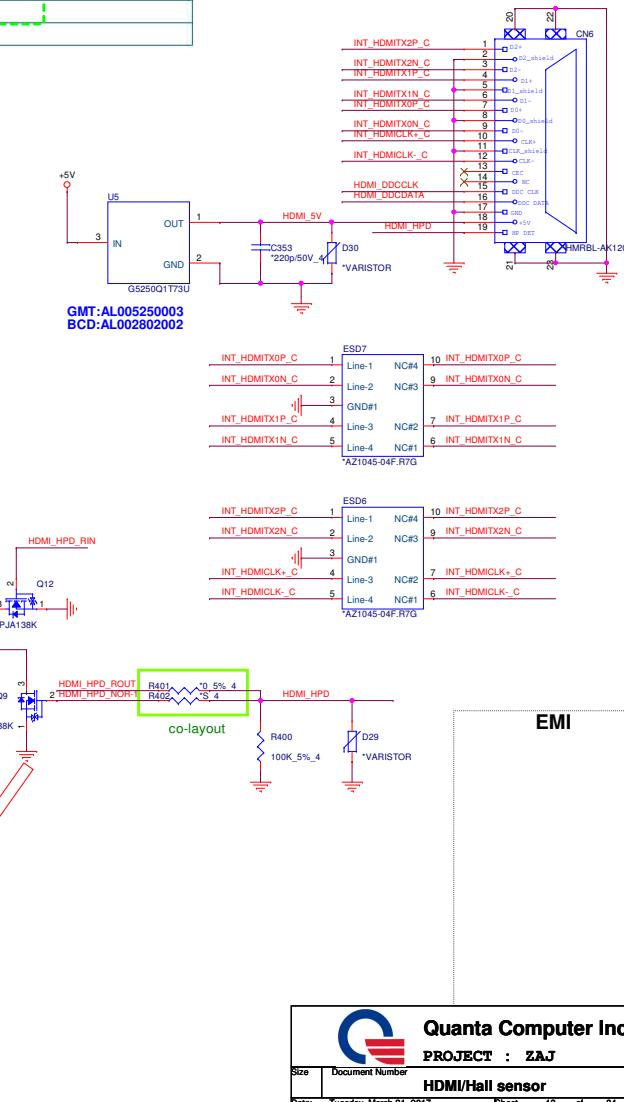
<b>OE_N</b>	<b>DDC_EN</b>	<b>HPD_SINK</b>	<b>Source output</b>	<b>PTN3366 power mode</b>
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode



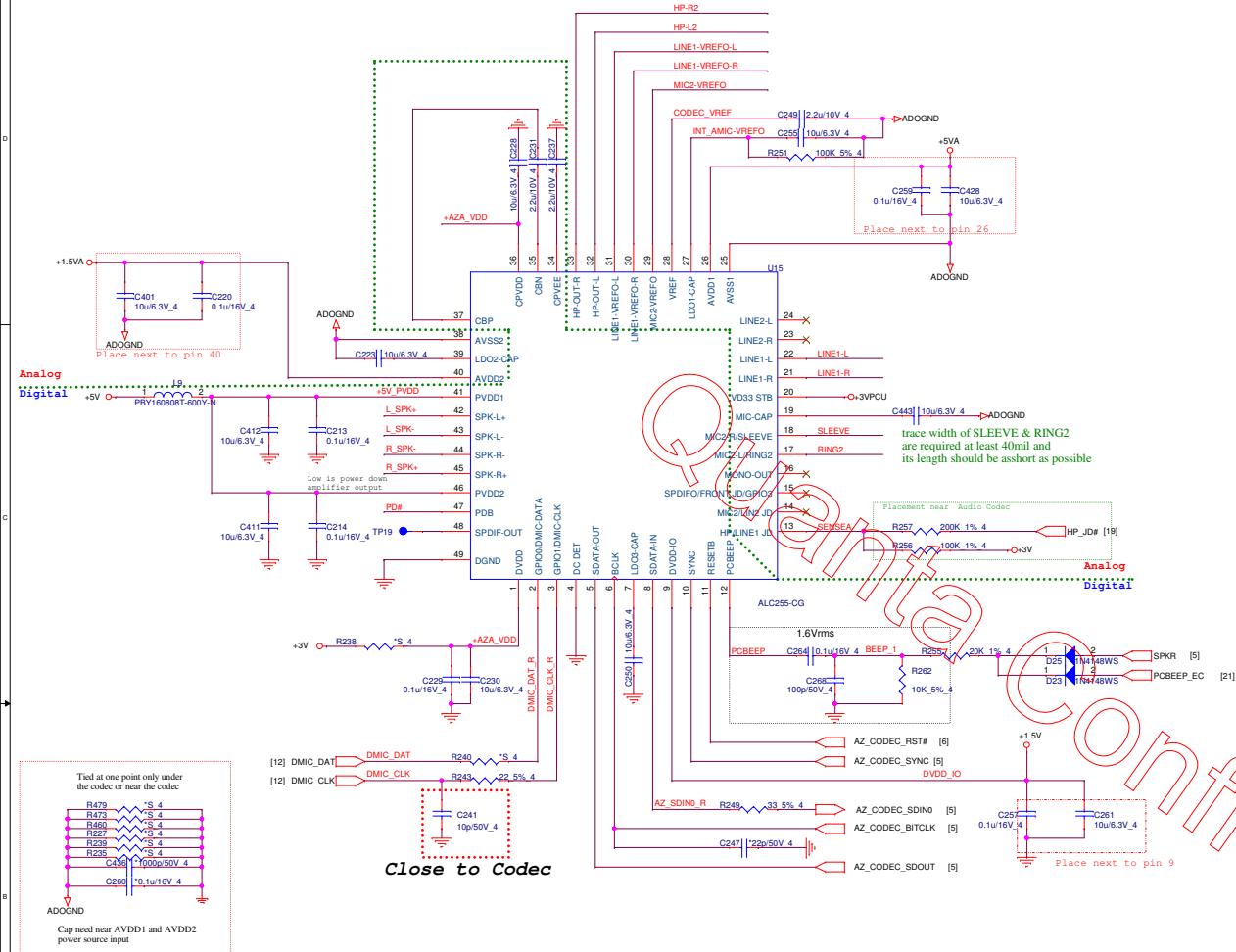
The PTN3366 supports four level equalization settings based on binary input pins EQ0 and EQ1.

**Table 5.** Equalizer settings

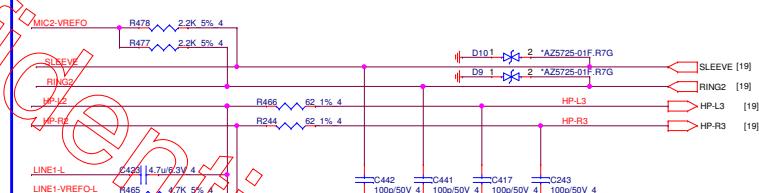
Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to $V_{DD}$	2 dB
short to $V_{DD}$	short to GND	4 dB
short to $V_{DD}$	short to $V_{DD}$	6 dB



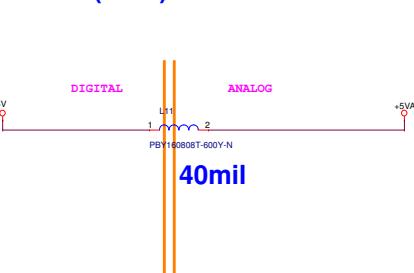
## Codec(ADO)



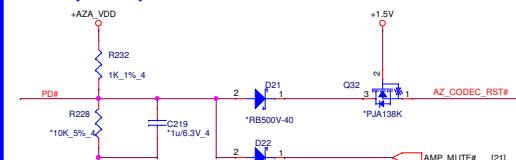
## Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)



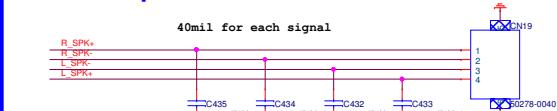
## Codec PWR 5V(ADO)



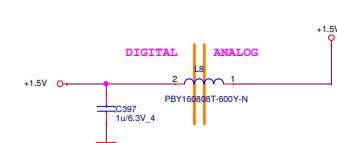
## Mute(ADO)



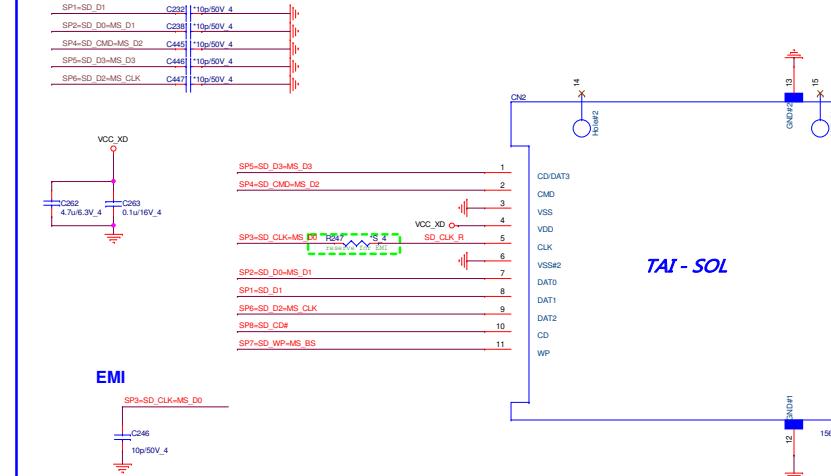
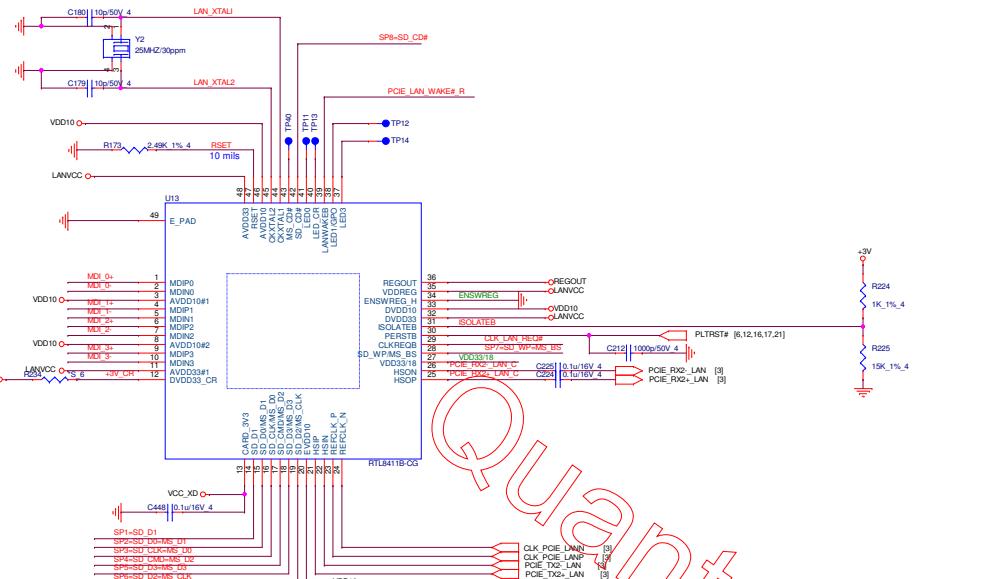
## Internal Speaker



Codec PWR 1.5V(ADO)

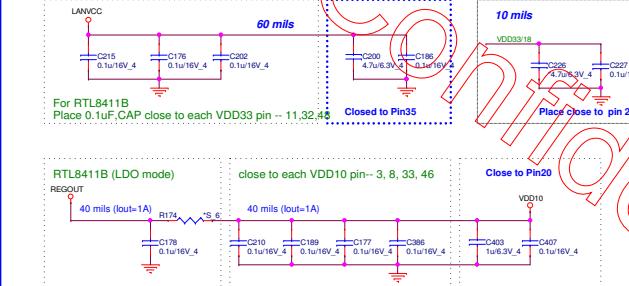
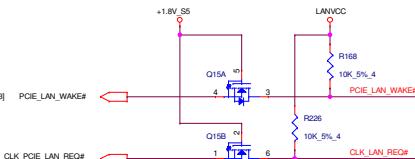


## Card Reader (CRD)

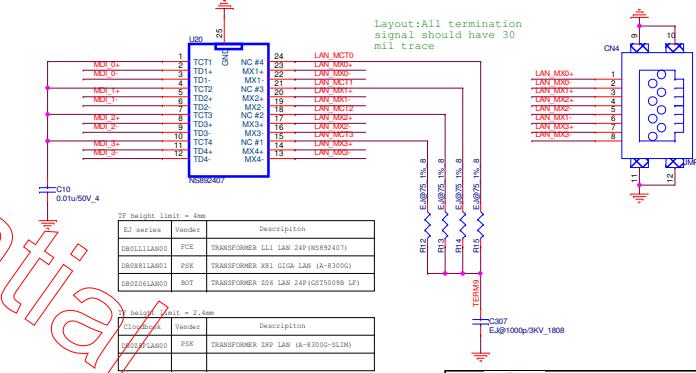


TAI - SO

## WAKE#/REQ# circuit(LAN)



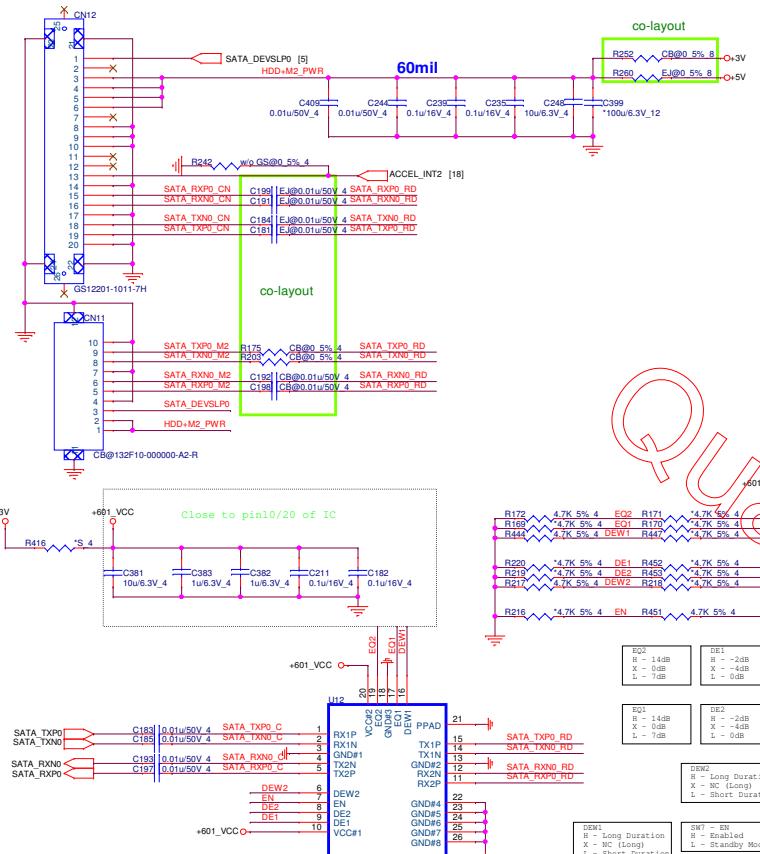
## Transforme



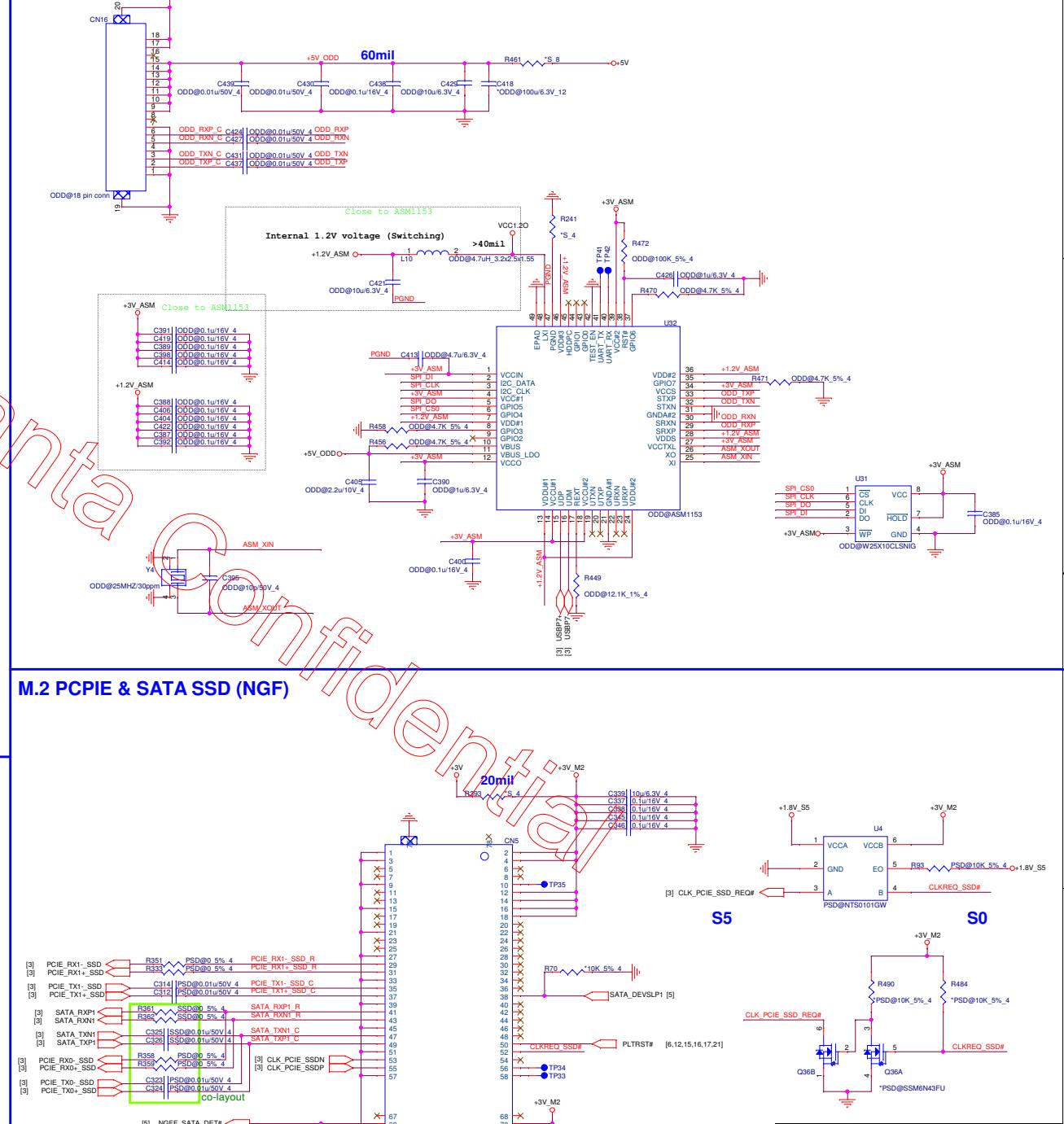
Layout:All termination  
signal should have 30  
mil trace

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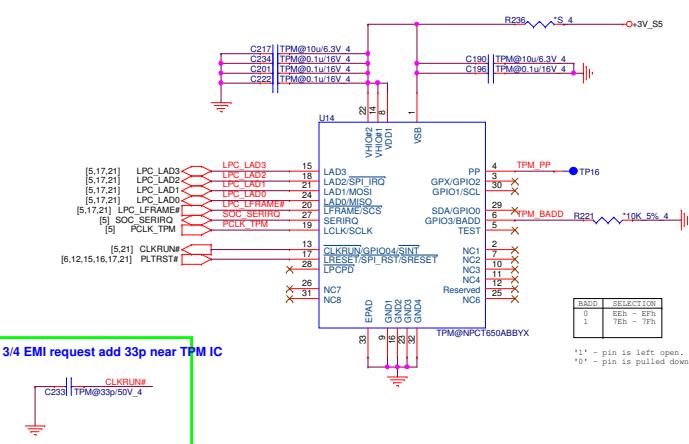
## 2.5" SATA HDD (HDD)



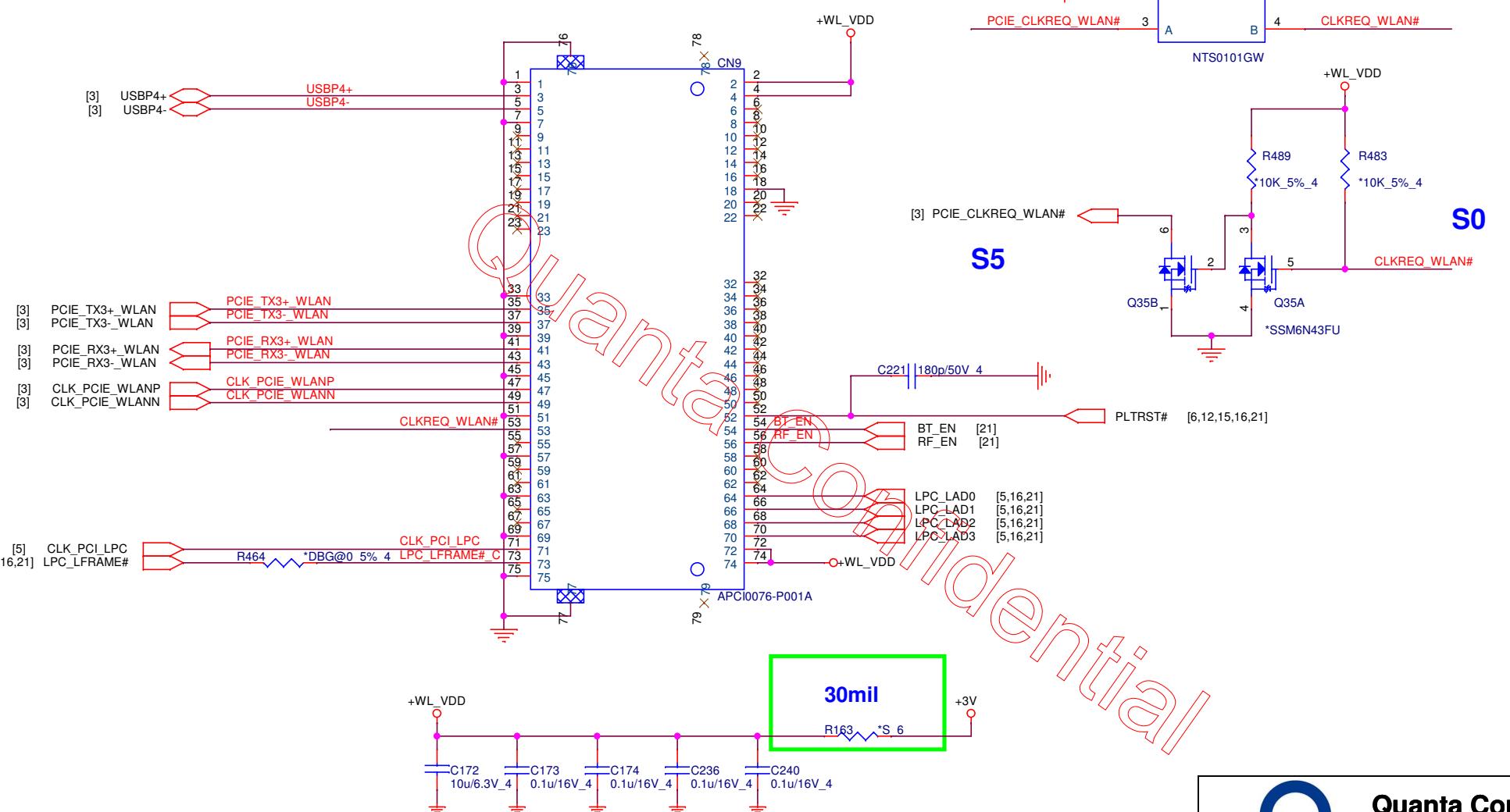
## USB ODD Bridge (ODD)



TPM NPCT650 (TPM)



# NGFF\_M.2 WiFi & BT (NGF)



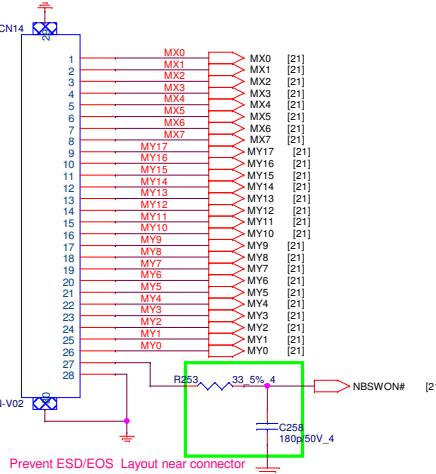
Quanta Computer Inc.

PROJECT : ZAJ

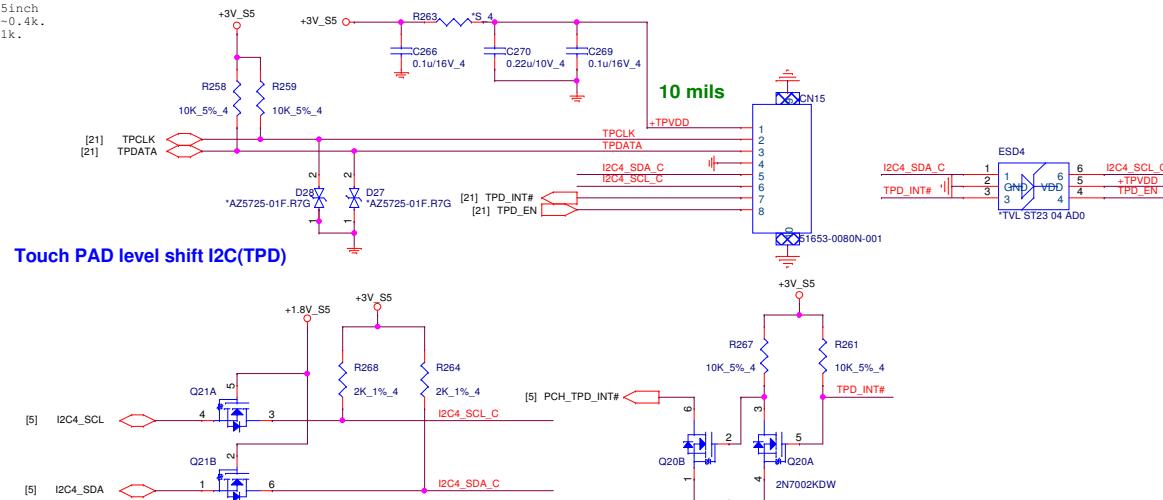
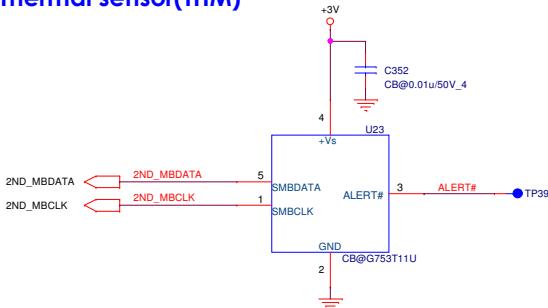
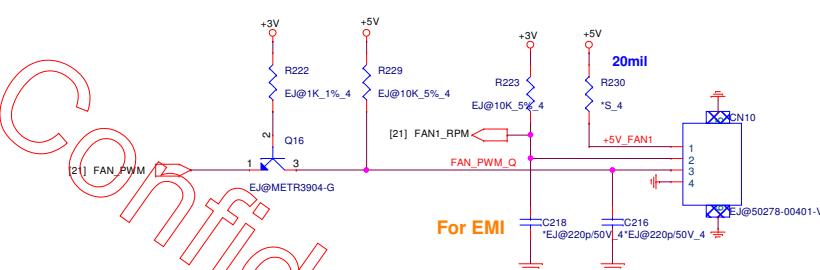
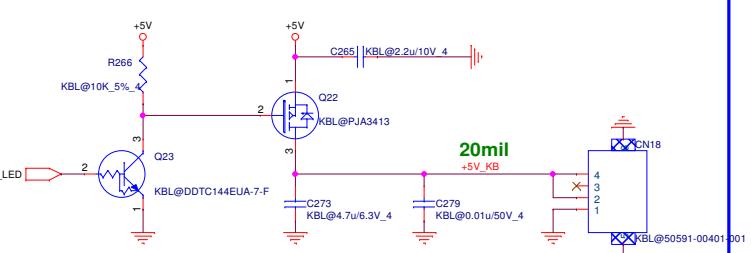
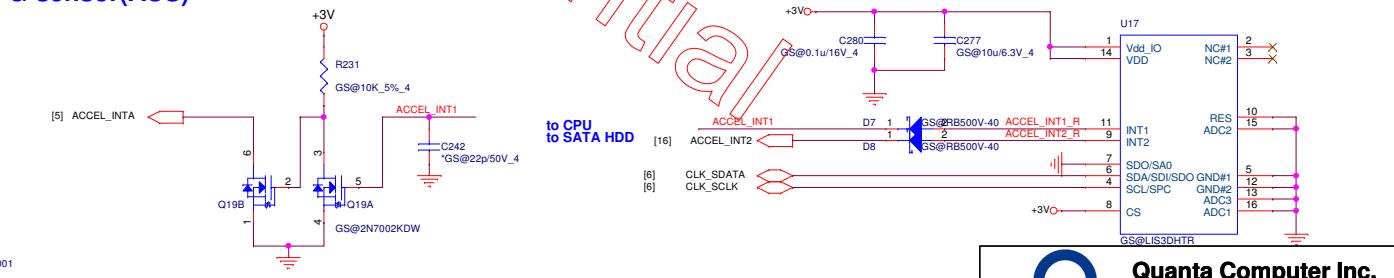
Size	Document Number	Rev
	NGFF WiFi & BT	3A

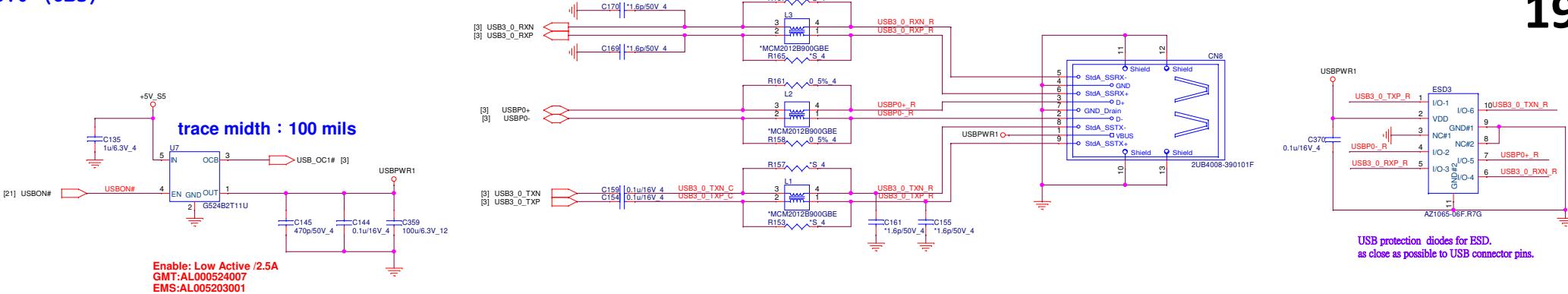
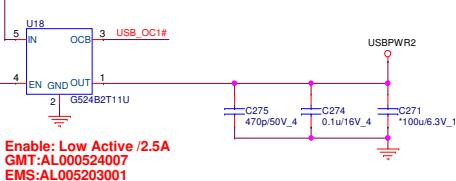
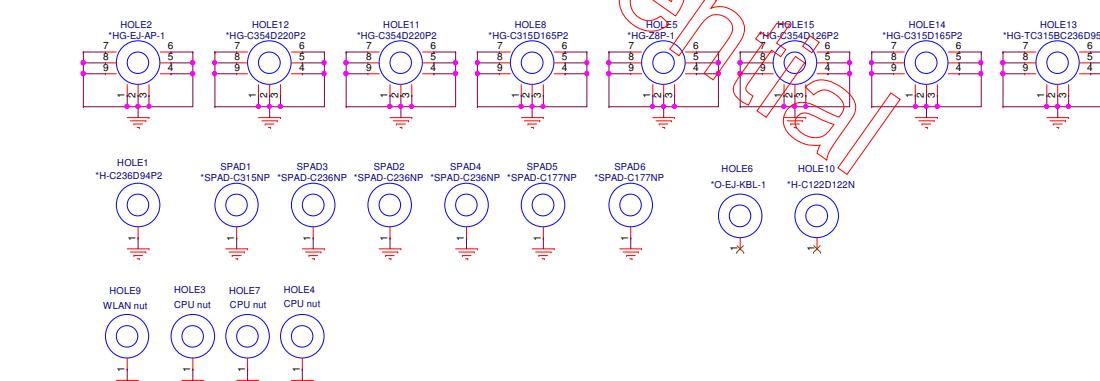
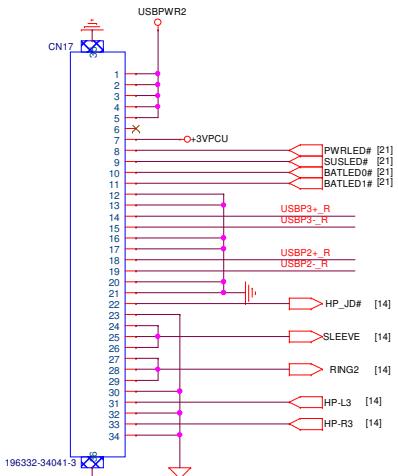
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**KEYBOARD (KBC)****TOUCHPAD (TPD I2C/PS2 co-lay)**

TPD->100kHz, TS=400Khz  
Intel design guide suggestion  
MCP PIN 10u.  
Per inch 3u TS=3x5inch  
400kHz 10-100u =2.4-0.4k.  
100Khz 10-100u=9k-1k.

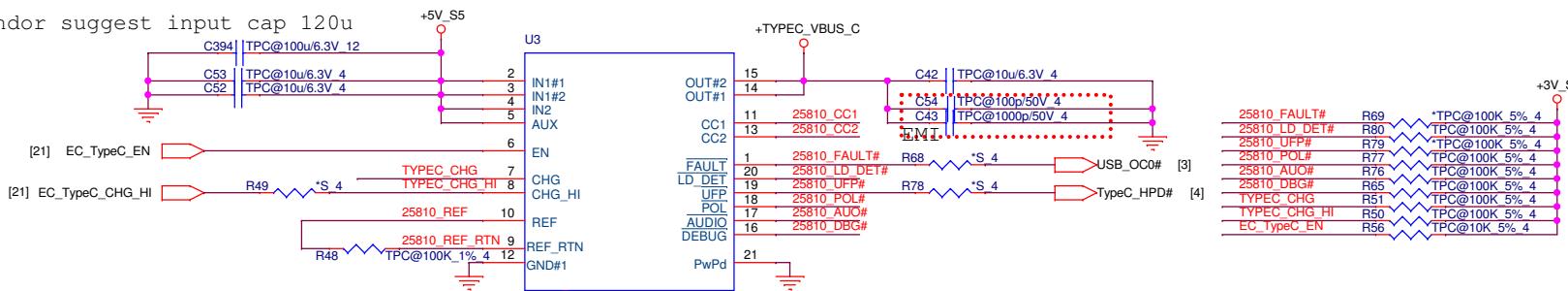
**CPU Thermal sensor(THM)****CPU FAN (THM)****Keyboard backlight (KBL)****G-sensor(ACS)**

**USB 3.0 (UB3)****USB 2.0 (UB2)****trace width : 100 mils****Stitch cap (EMC)****HOLE(OTH)****USB 2.0/LED/AUDIO JACK DB (UB2)**

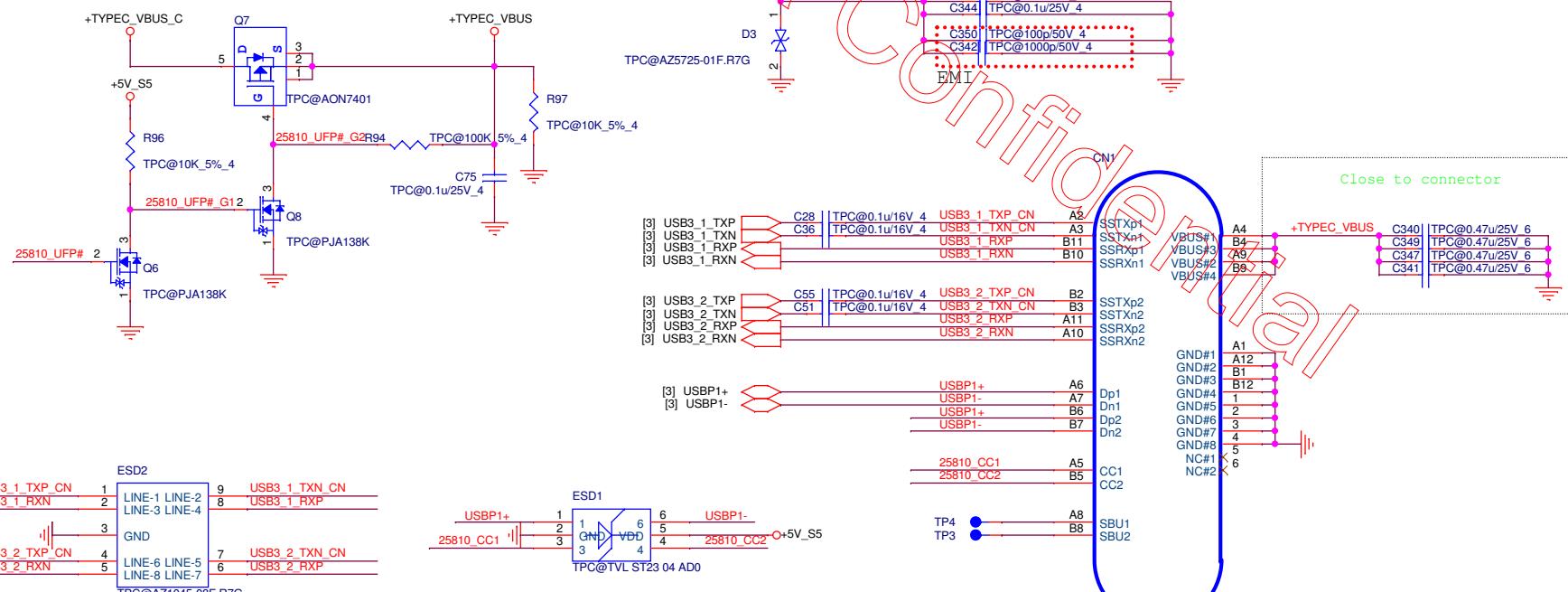
# USB TYPE-C (UB3)

trace midth : 150 mils

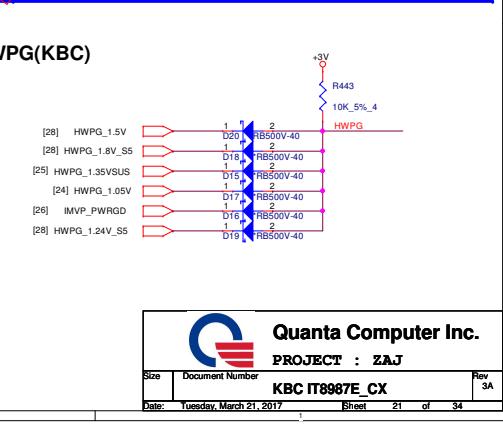
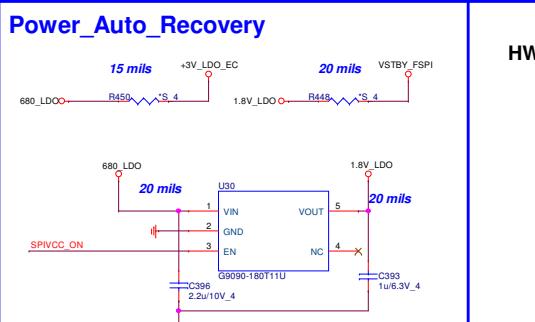
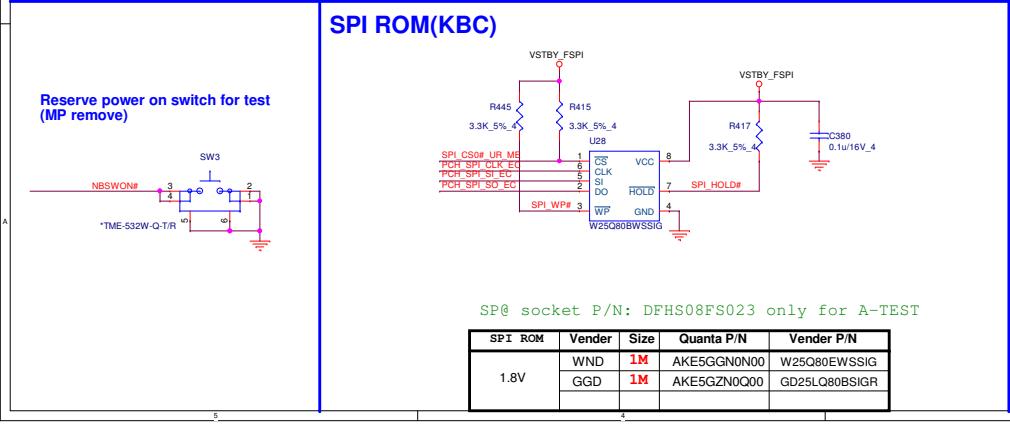
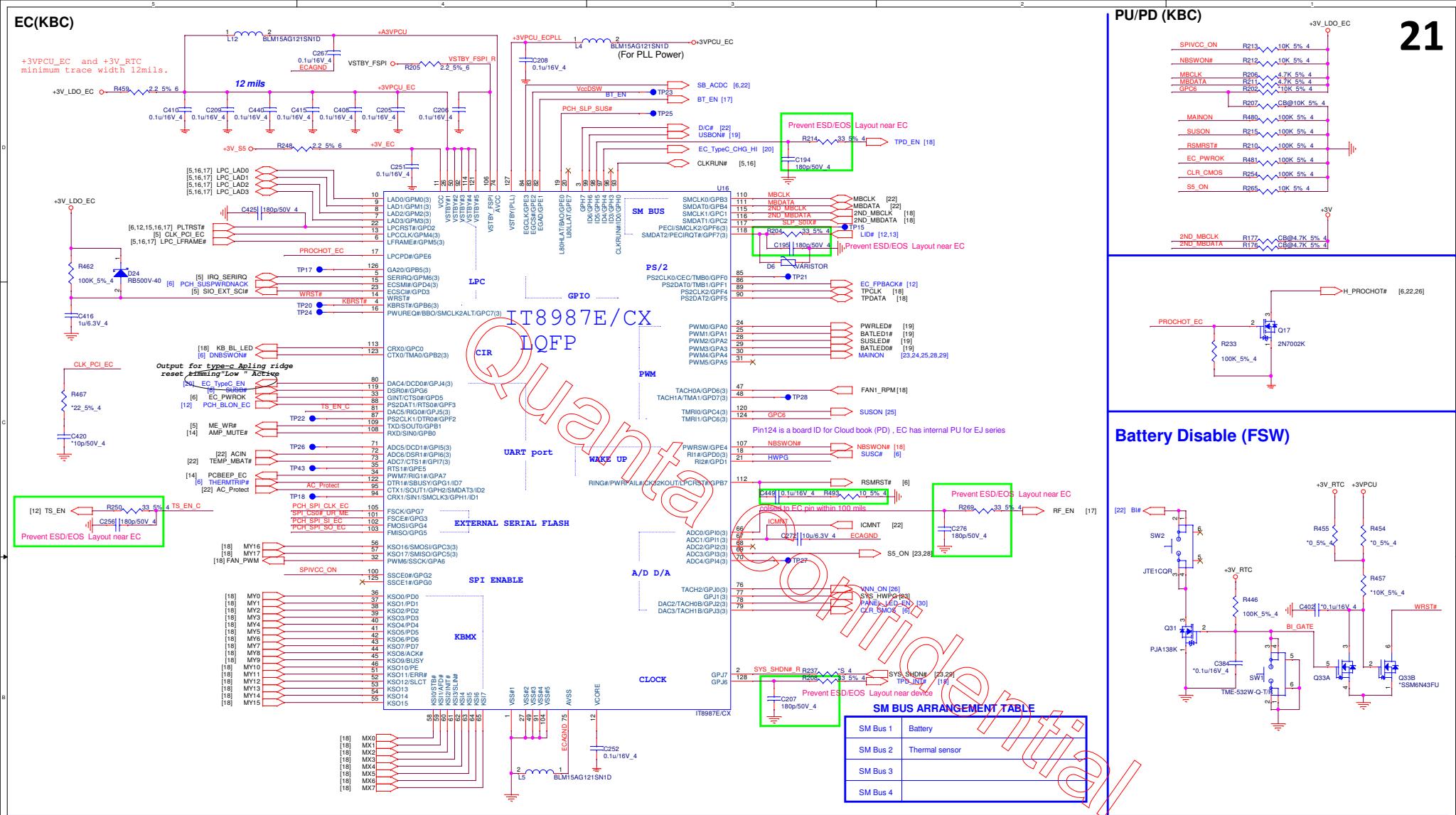
Vendor suggest input cap 120u



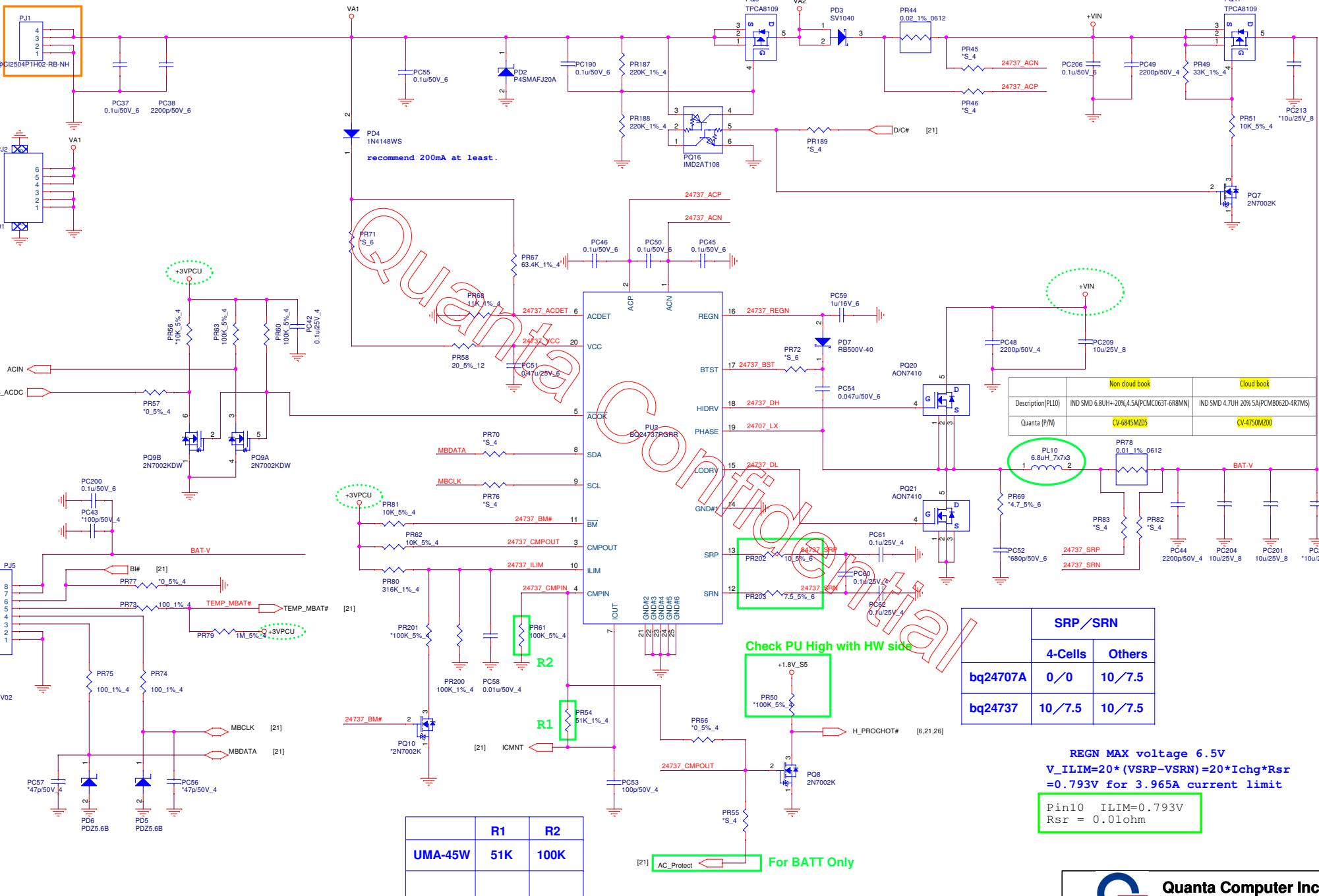
trace midth : 150 mils



Amazing : BC104508Z00  
PJT : BC605S8QZ00  
INPAQ : BC38109LZ00



## Double Check ADP-IN Connector with ME

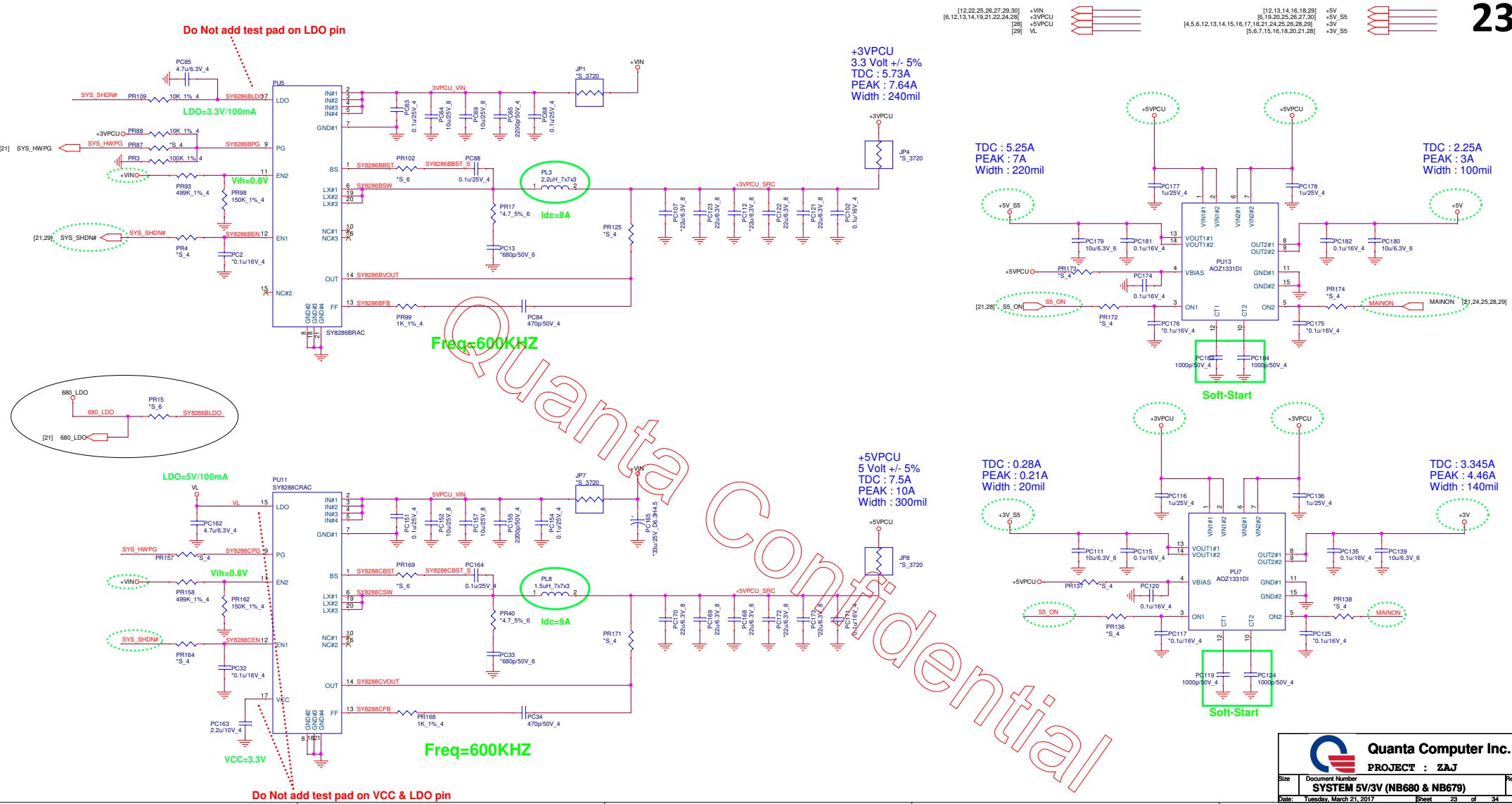


REGN MAX voltage 6.5V  
 $V_{ILIM}=20*(VSRP-VSRN)=20*I_{Chg}*R_{sr}$   
 $=0.793V$  for  $3.965A$  current limit

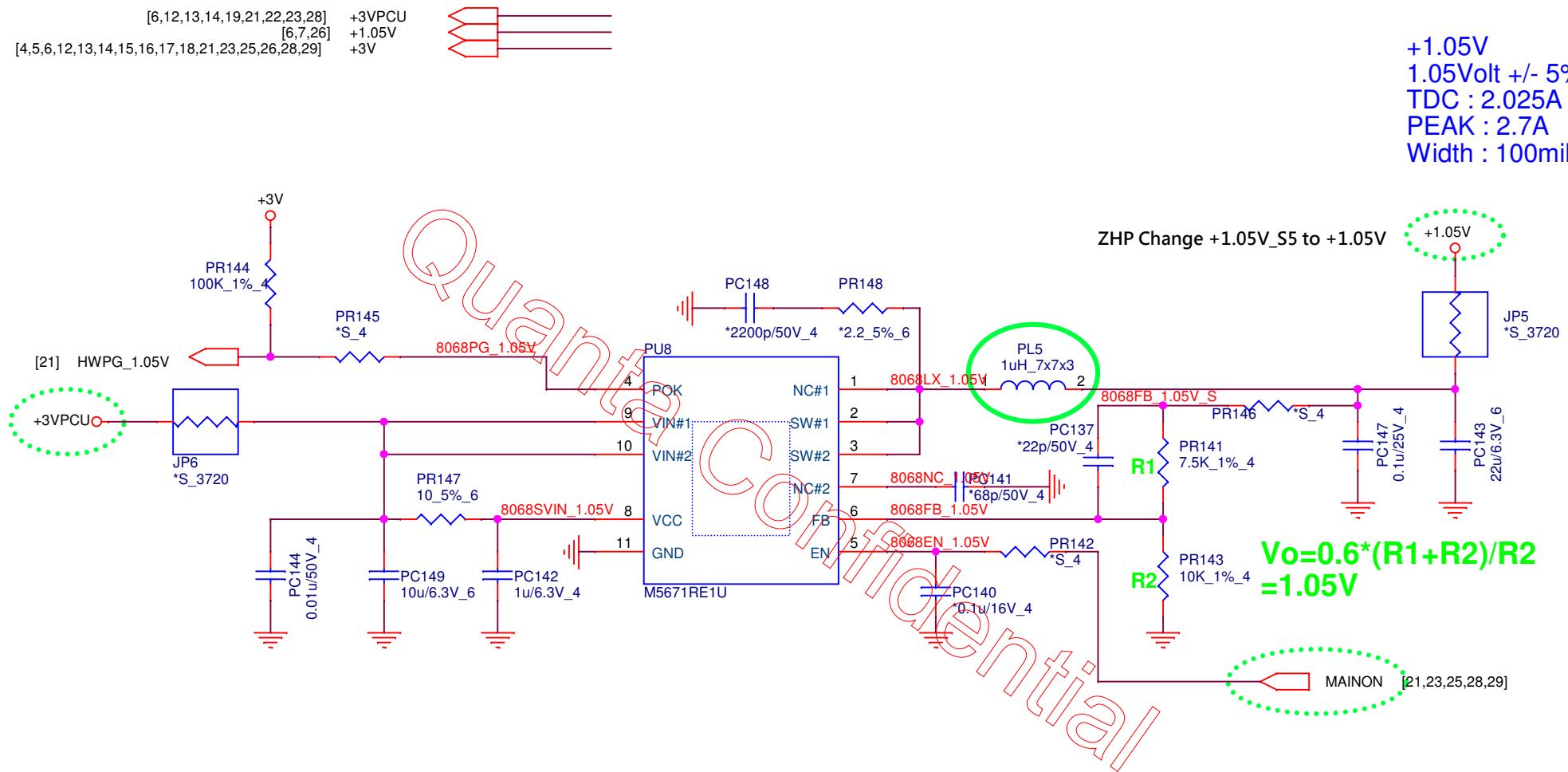
Pin10 ILIM=0.793V  
Rsr = 0.01ohm

	R1	R2
UMA-45W	51K	100K

For BATT Only

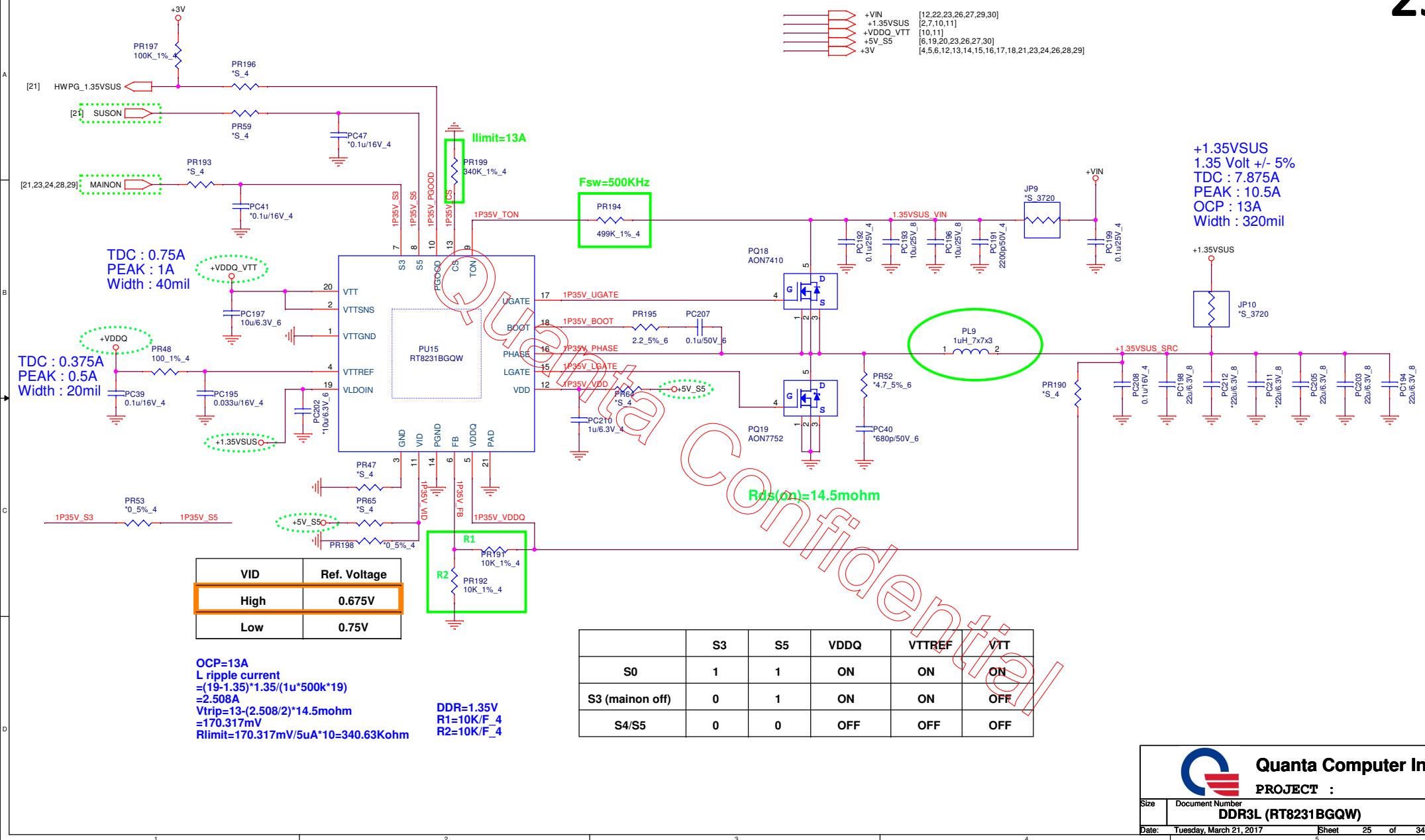


+1.05V  
1.05Volt +/- 5%  
TDC : 2.025A  
PEAK : 2.7A  
Width : 100mil



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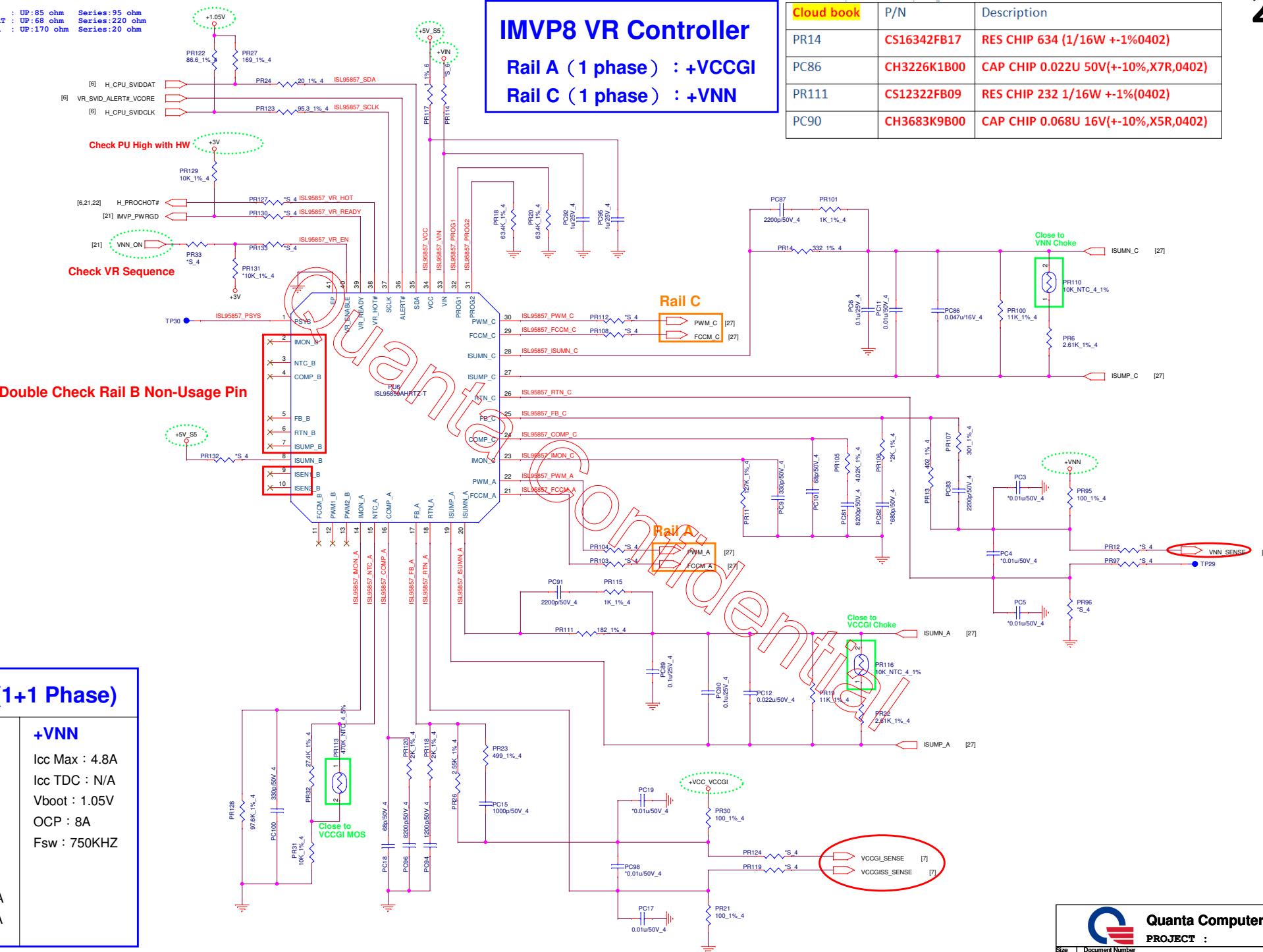
Size	Document Number <b>+1.05V (M5671RE1U)</b>	Rev 3A
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# IMVP8 VR Controller

Rail A (1 phase) : +VCCGI  
Rail C (1 phase) : +VNN

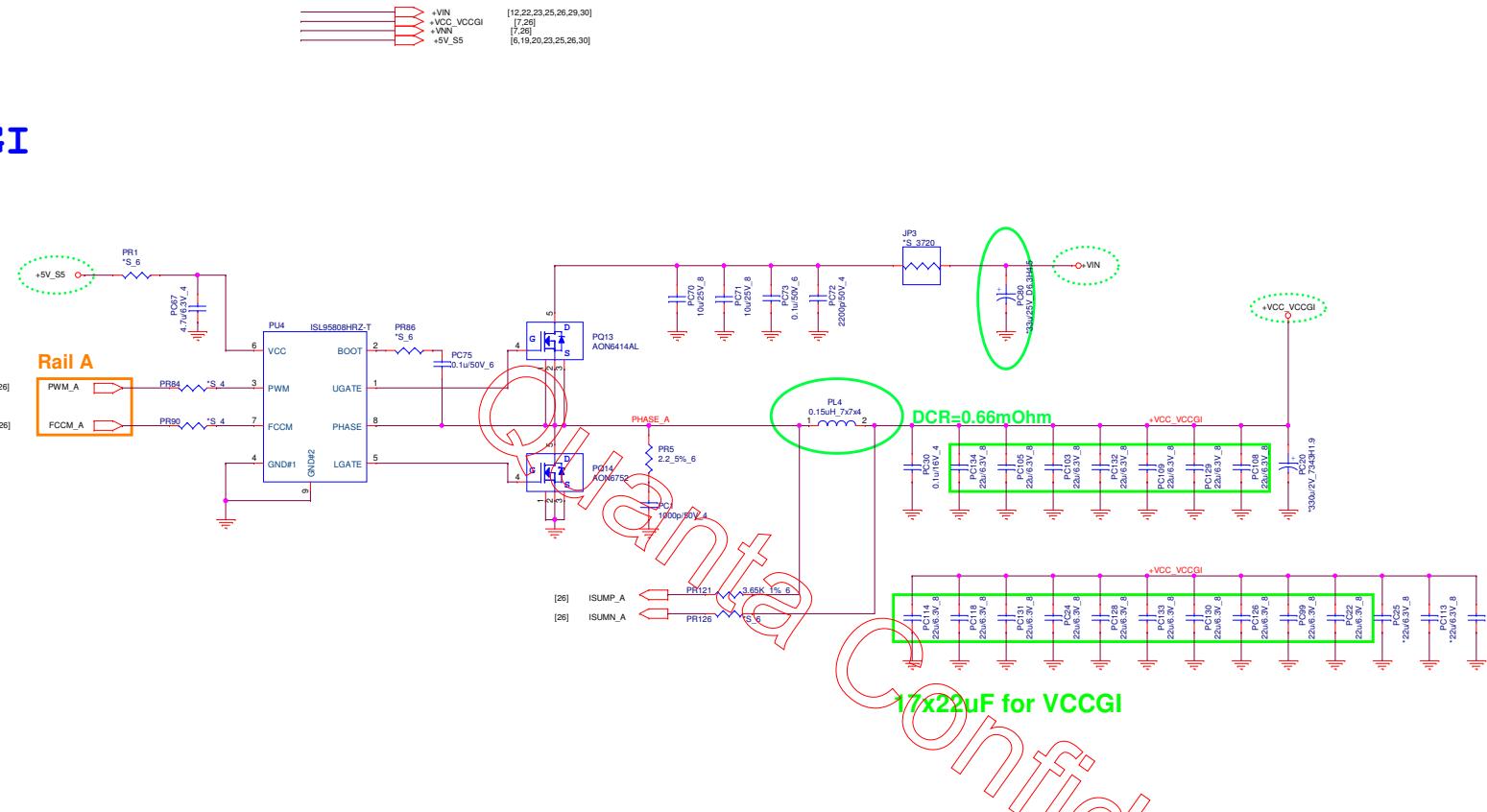
Cloud book	P/N	Description
PR14	<b>CS16342FB17</b>	<b>RES CHIP 634 (1/16W +-1%0402)</b>
PC86	<b>CH3226K1B00</b>	<b>CAP CHIP 0.022U 50V(+-10%,X7R,0402)</b>
PR111	<b>CS12322FB09</b>	<b>RES CHIP 232 1/16W +-1%(0402)</b>
PC90	<b>CH3683K9B00</b>	<b>CAP CHIP 0.068U 16V(+-10%,X5R,0402)</b>



APL VR (1+1 Phase)

<b>+VCCGI</b>	<b>+VNN</b>
Icc Max : 21A	Icc Max : 4.8A
Icc TDC : 18A	Icc TDC : N/A
Vboot : 0V	Vboot : 1.05V
OCP : 25A	OCP : 8A
Fsw : 750KHZ	Fsw : 750KHZ

VCCGI



17x22uF for VCCGI

JP2  
S 3720

P074  
220p/35V, 4

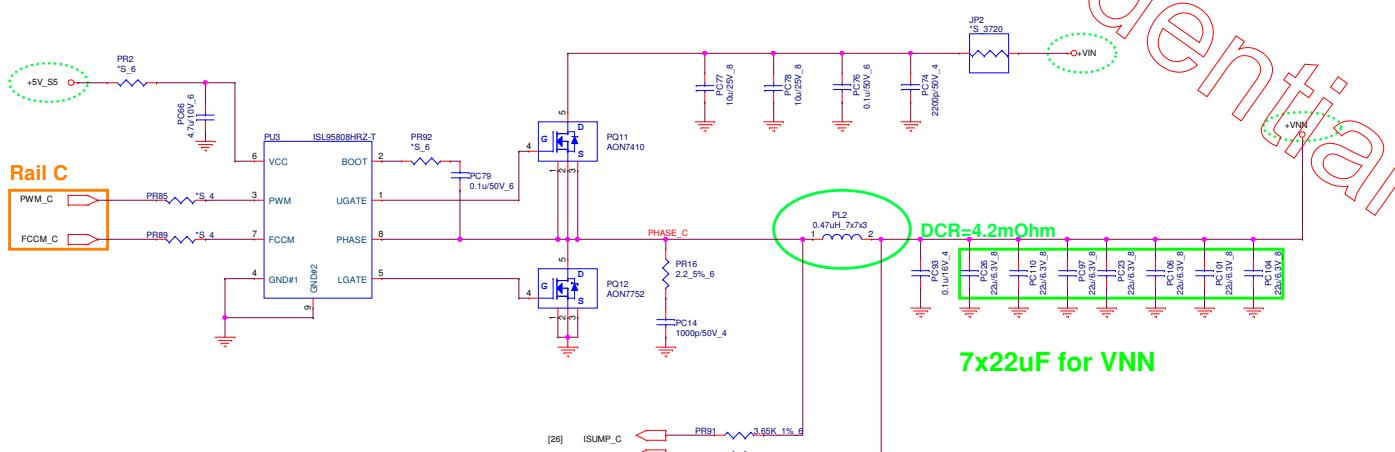
0.1uF/35V, 6

VIN

VNN

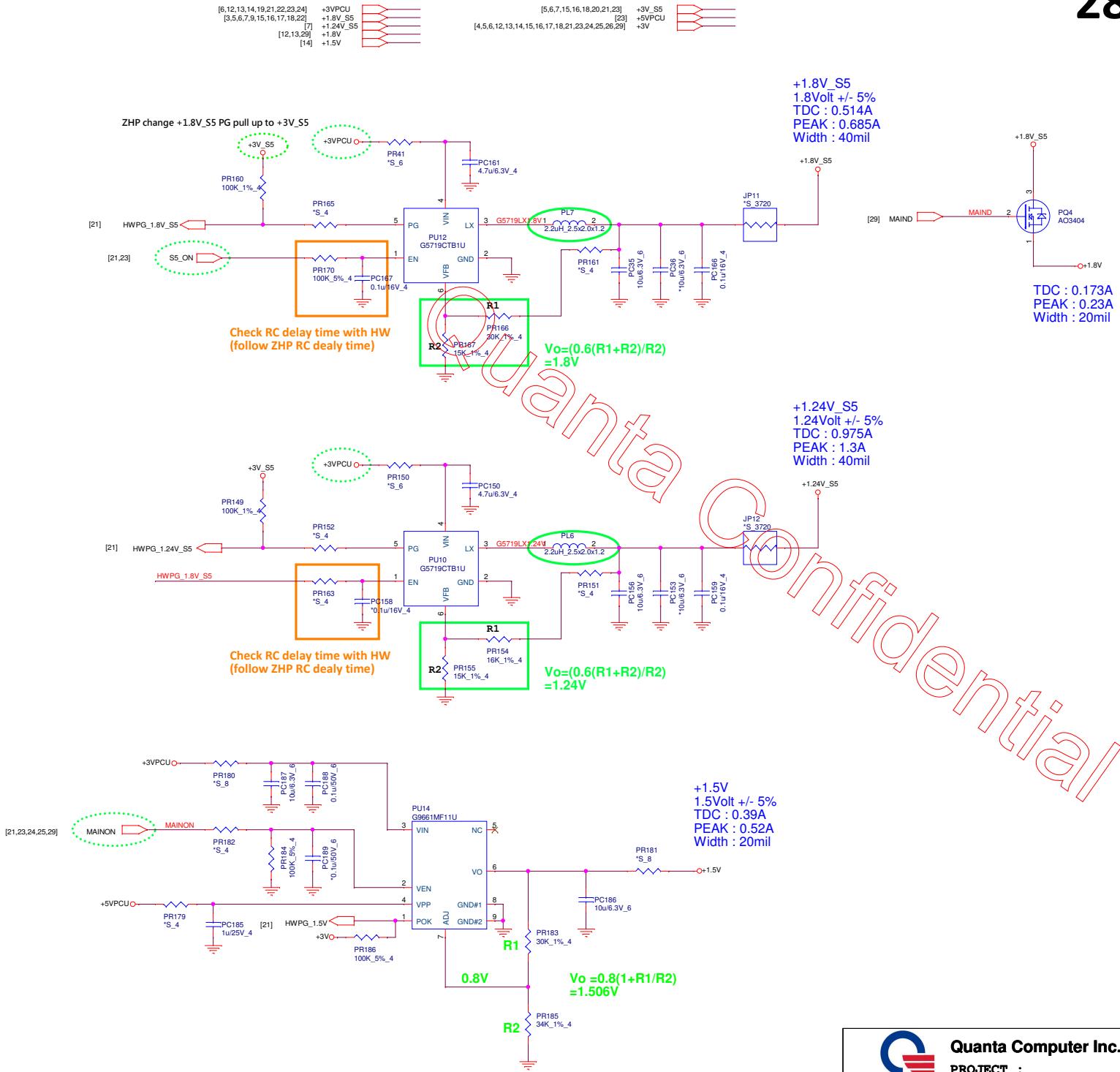
+VCCGI  
Icc Max : 21A  
Icc TDC : 18A  
Vboot : 0V  
OCP : 25A  
Fsw : 750KHZ  
  
**VCCGI L/L :**  
R\_DC\_LL : 6mV/  
R\_AC\_LL : 6mV/

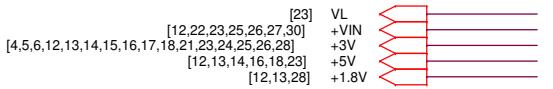
VNN



7x22uF for VNN

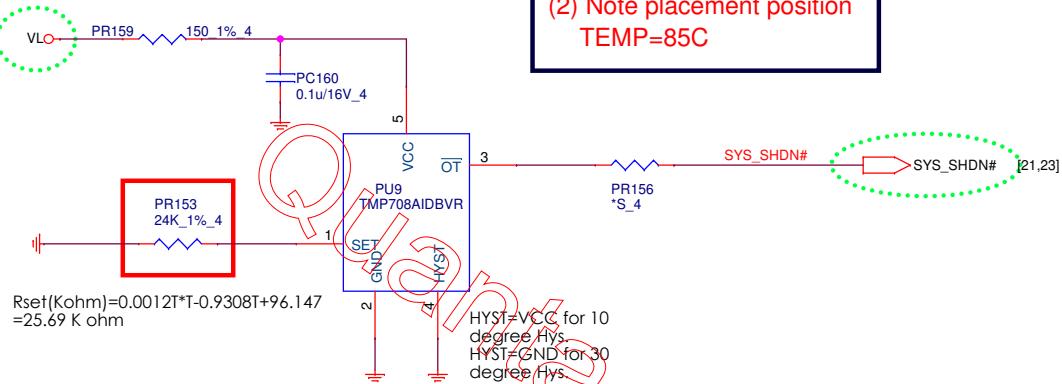
+VNN  
Icc Max : 4.8A  
Icc TDC : N/A  
Vboot : 1.05V  
OCP : 8A  
Fsw : 750KHZ



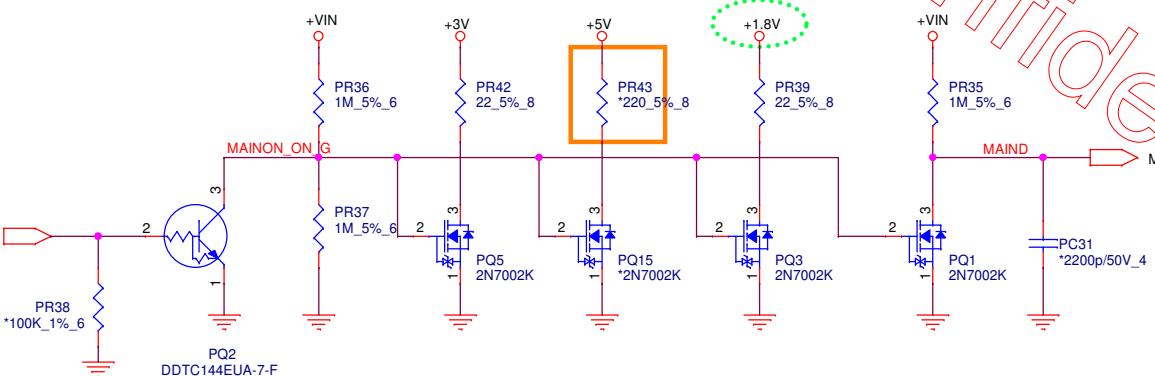


## Thermal Protection

- (1) Need fine tune for thermal protect point
- (2) Note placement position TEMP=85C

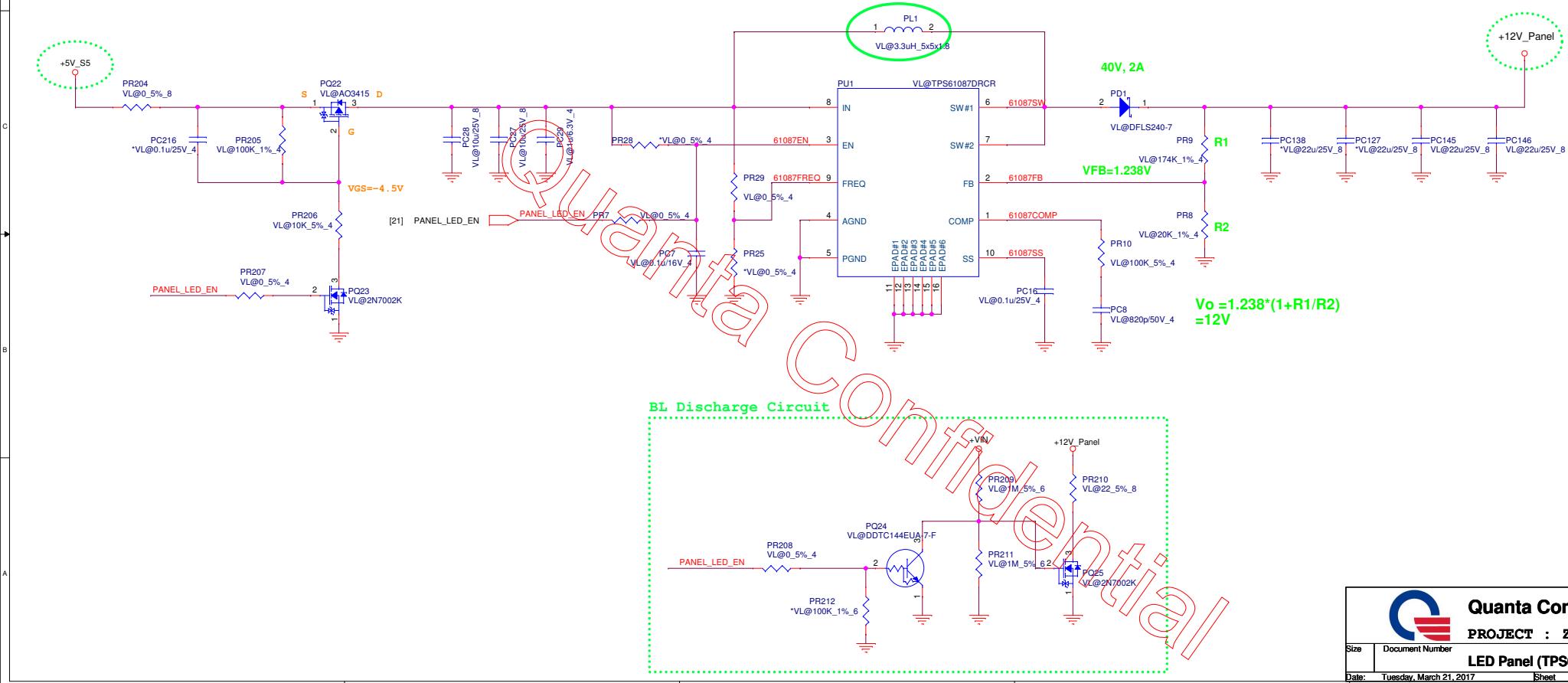


+5V PU High R= 220 ohm for Bo-Bo sound issue.

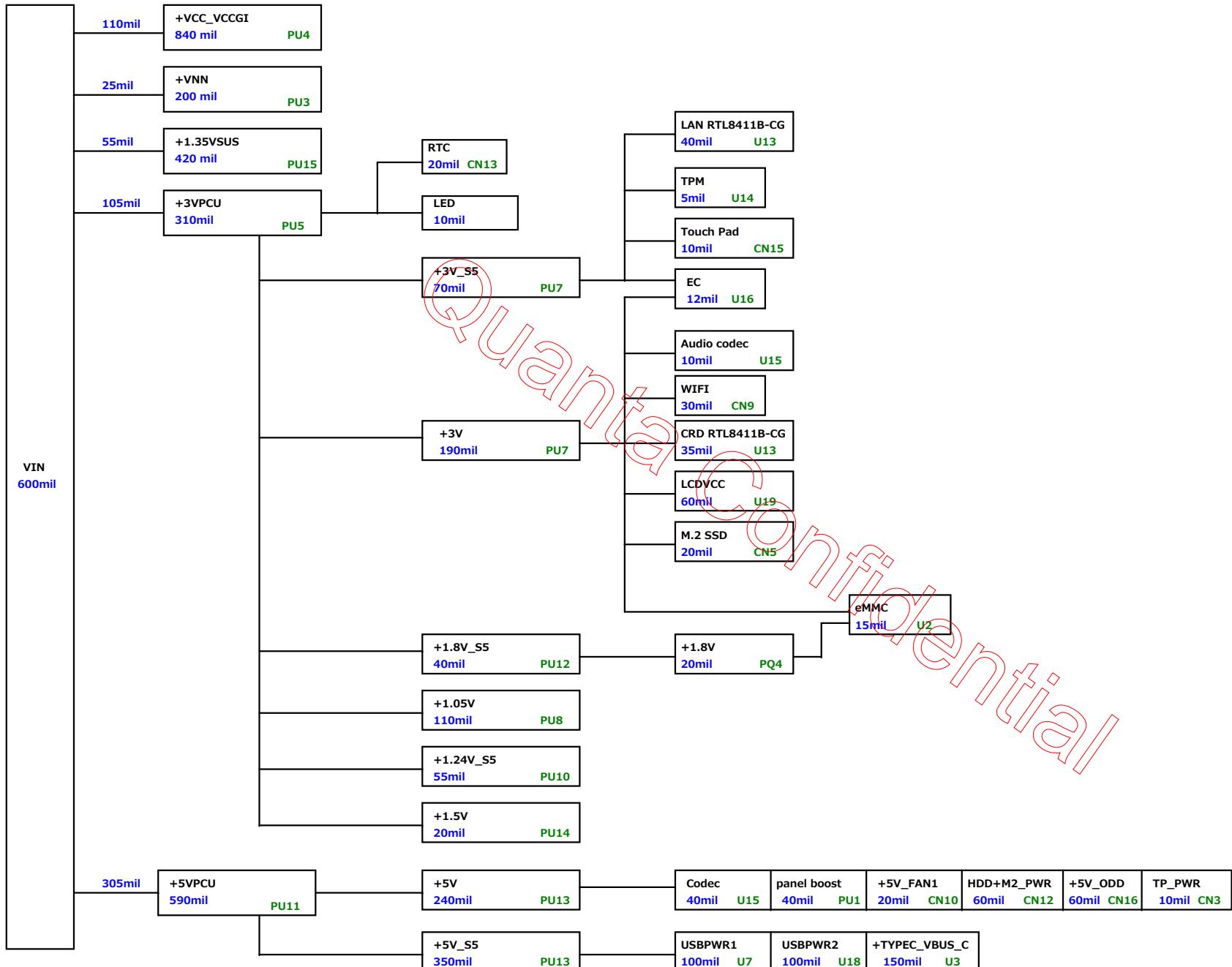


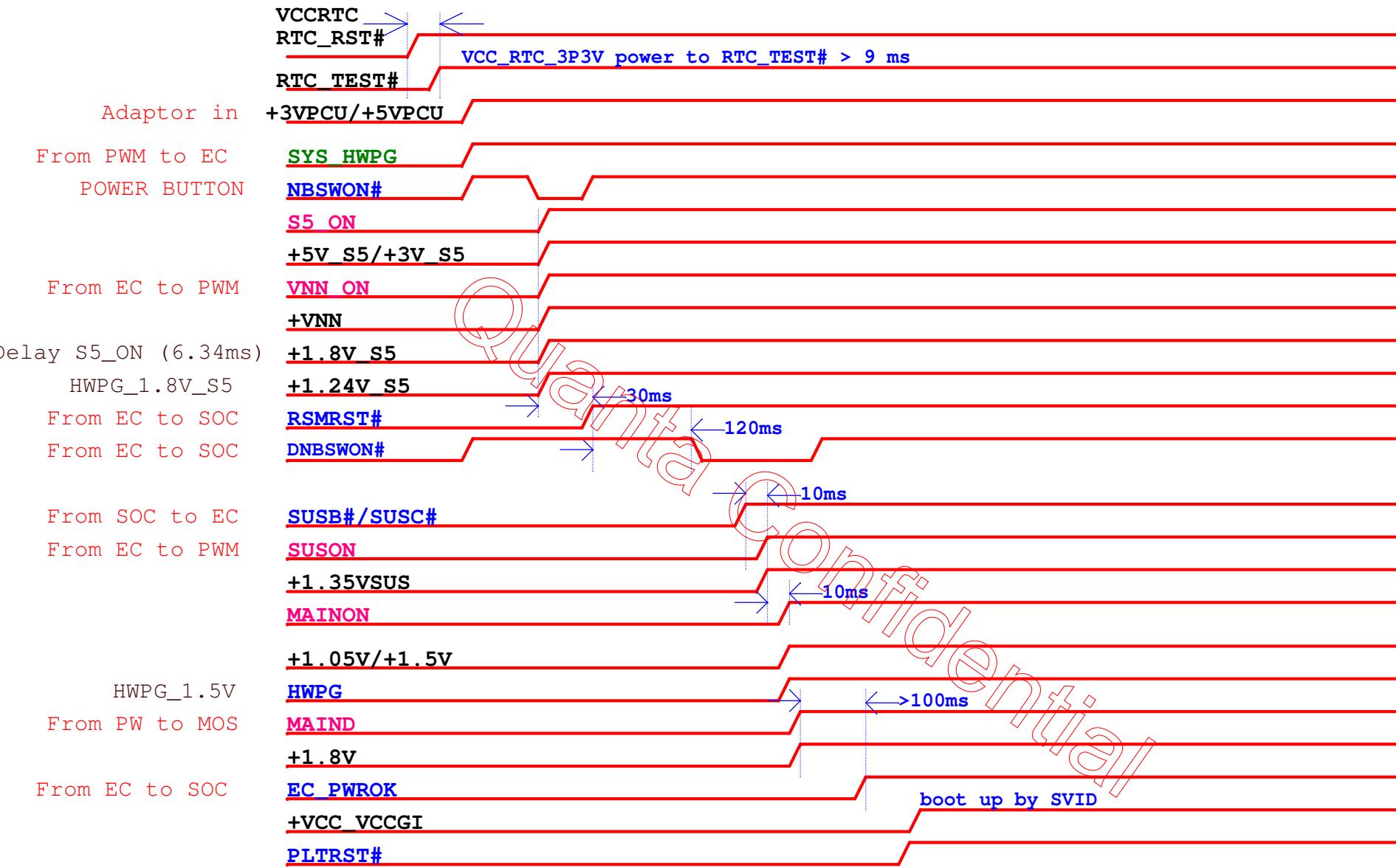
Panel Spec (TFT-LCD 14")  
VLED : 6V~21V (Typ:12V)  
Power Consumption : 3W (MAX)

+12V\_Panel  
12 Volt +/- 5%  
PEAK : 0.35A  
Width : 20mil

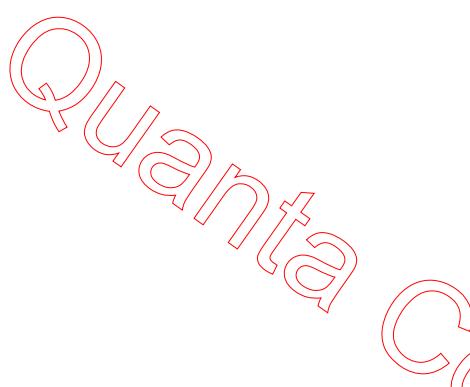


## Apollo Power Tree





Power plane	Description	S0	S3	S5
+VIN	Adaptor power supply	ON	ON	ON
+VCC_VCCGI	Variable voltage supply to CPU and Graphics Core and ISP logic	ON	OFF	OFF
+VNN	Variable voltage supply to other (non core) logic	ON	OFF	OFF
+1.05V	Fixed voltage rail for SRAM,I/O,internal Logic	ON	OFF	OFF
+1.24V_S5	Fixed voltage rail for SoC L2/ Audio & ISH I/O Logic and PLLs MIPI Logic/ USB2-I/O/MIPI I/Os	ON	ON	ON
+1.8V_S5	Fixed voltage rail for all GPIOs	ON	ON	ON
+1.35VSUS	Fixed voltage rail for DDR3L IO	ON	ON	OFF
+3V_RTC	Fixed Voltage rail for RTC (Real Time Clock)	ON	ON	ON
+1.8V	1.8V S0 power rail	ON	OFF	OFF
+1.5V	1.5V S0 power rail	ON	OFF	OFF
+5VPCU	5V always on power rail	ON	ON	ON
+5V_S5	5V S5 power rail	ON	ON	ON
+5V	5V S0 power rail	ON	OFF	OFF
+3VPCU	3V always on power rail	ON	ON	ON
+3V_S5	3V S5 power rail	ON	ON	ON
+3V	3V S0 power rail	ON	OFF	OFF

Model	Date	CHANGE LIST
ZAJ REV.D	02/10	1.Change 0 ohm to shortpad : R403,R404,R405,R406,R407,R408,R409,R410,R104,R113,R108,R115,R99,R402,R167,R165,R161,R158,R157,R153,R270,R271,R272,R273,R247 2.Un-stuff R380/R464 (debug card circuit)
	02/18	1.Unstuff SW3 2.Update SW2 FP to "sw-ds-a40e-4p-smt" by SMT request 3.Update CN2 FP to "sdcard-156-1001902602-11p-smt" by SMT request 4.Update CN9 FP to "ngff-apci0076-p001a-75p-ke-smt" by SMT request
		

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 Quanta Computer Inc. PROJECT : ZAJ	DOC NO.	PROJECT MODEL :	ZAJ	APPROVED BY:		DATE:
Change list		PART NUMBER:		DRAWING BY:		REVISION:
Today, March 21, 2017						