MS-7788 Ver: 3.0 u-ATX : 226 * 173 mm

CPU:

Intel - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH(H61)

OnBoard Chipset:

HD Audio Codec:ALC887VD / VT1708SCE
LAN:RTL 8105E 10/100 , Co-lay 8111E 10/100/1000
SIO:FIN71868AD
Flash ROM: 32Mb SPI (PCH)

Main Memory:

DDRIII (1066/1333MHz) * 2 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1
PCI Express (X1) Slot * 1

PWM:

Controller: UT501 3+1 Phase
CPU+GPU: UP6282 MOSFET Driver
CPU VTT: UP1504
CPU SA : OP+MOS
DDR: UP1504
PCH: OP+MOS

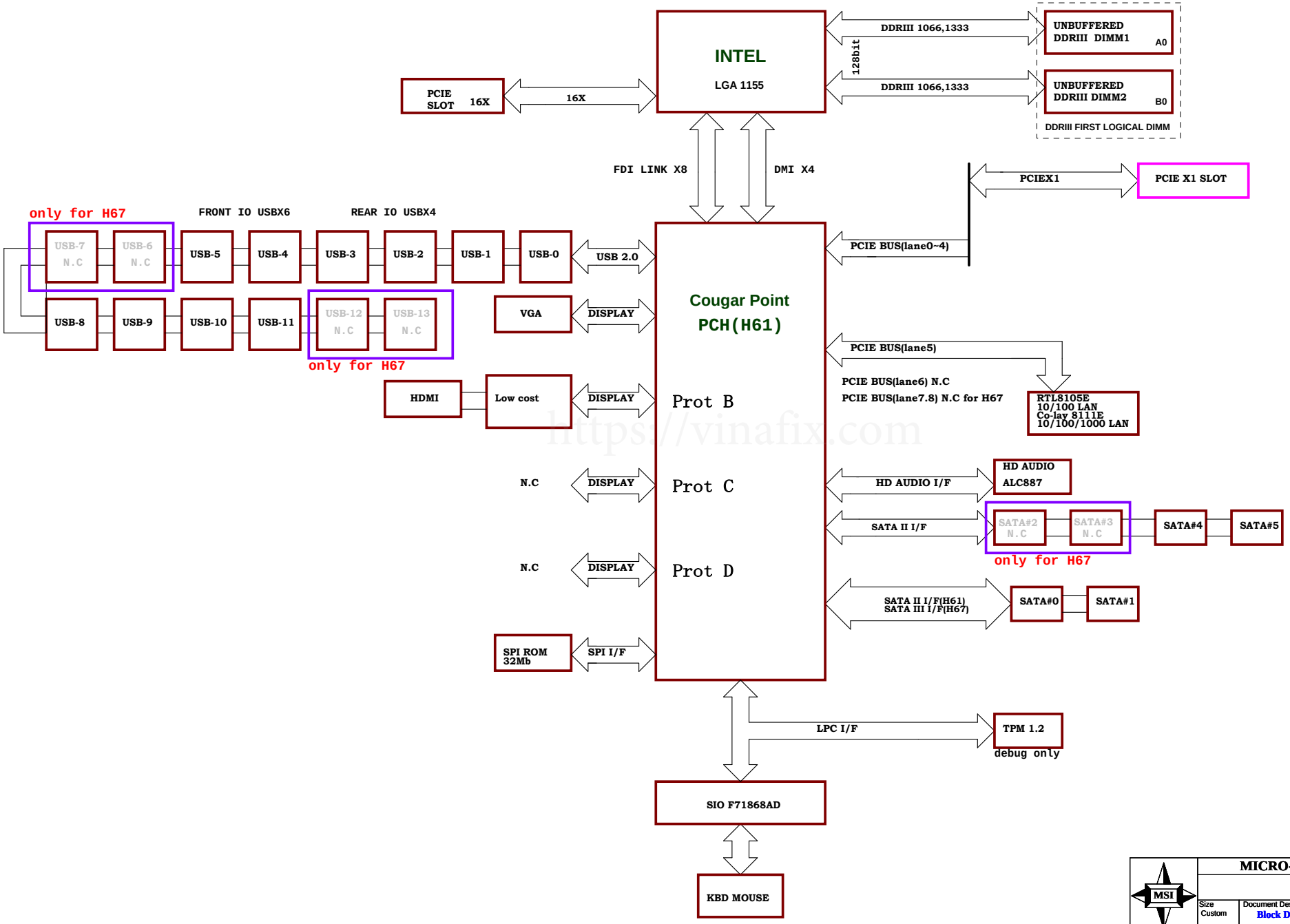
ACPI:

UPI

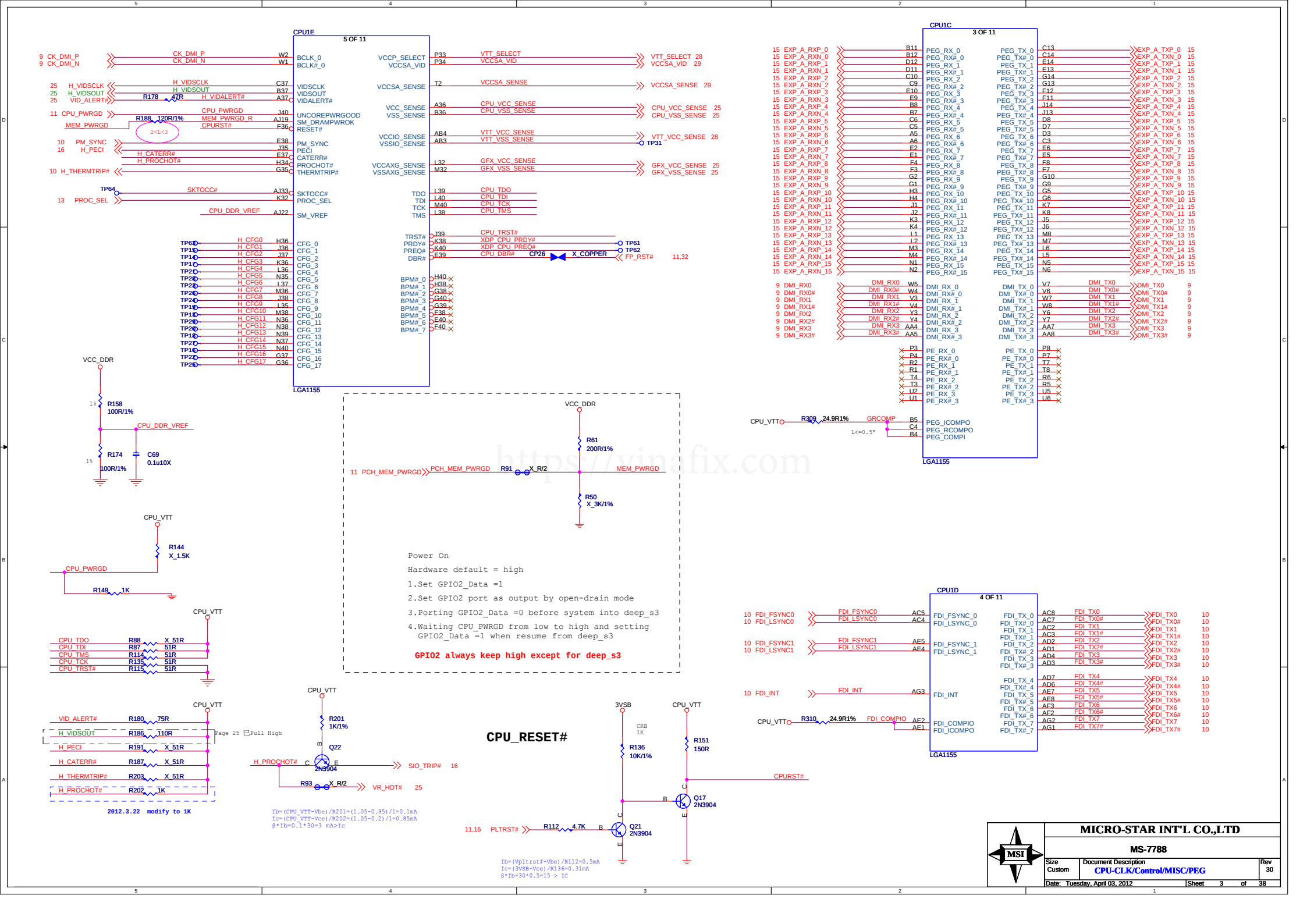
Other:

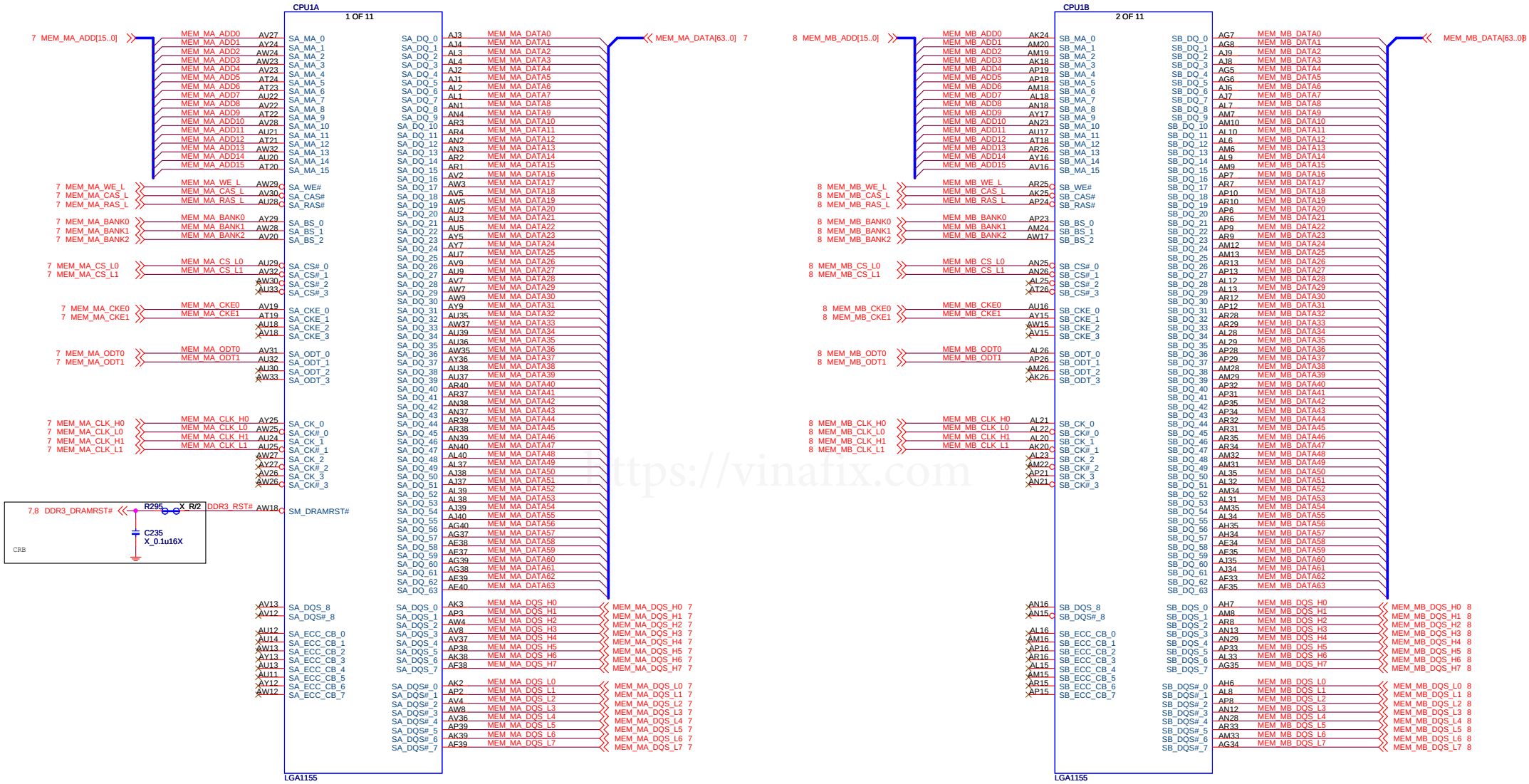
SATA2.0 x4 (PCH)
USB2.0 RearX6 Front x4
D-SUB/HDMI*1
TPM Header *1
Speaker Pin Header

MICRO-STAR INT'L CO.,LTD		
MS-7788		
Size: Custom	Document Description: Cover Sheet	Rev: 30
Date: Tuesday, April 03, 2012	Sheet 1 of 38	



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7788	
Size: Custom	Document Description: Block Diagram	Rev: 30
Date: Tuesday, April 03, 2012	Sheet 2 of 38	


CPU1E
5 OF 11
LGA1155
CPU1C
3 OF 11
LGA1155
CPU1D
4 OF 11
LGA1155
Power On
Hardware default = high
1.Set GPIO2_Data =1
2.Set GPIO2 port as output by open-drain mode
3.Porting GPIO2_Data =0 before system into deep_s3
4.Waiting CPU_PWRGD from low to high and setting GPIO2_Data =1 when resume from deep_s3
GPIO2 always keep high except for deep_s3
CPU_RESET#
2012.3.22 modify to 1K
MICRO-STAR INT'L CO.,LTD
MS-7788
CPU-CLK/Control/MISC/PEG
Date: Tuesday, April 03, 2012
Sheet 3 of 38



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7788	
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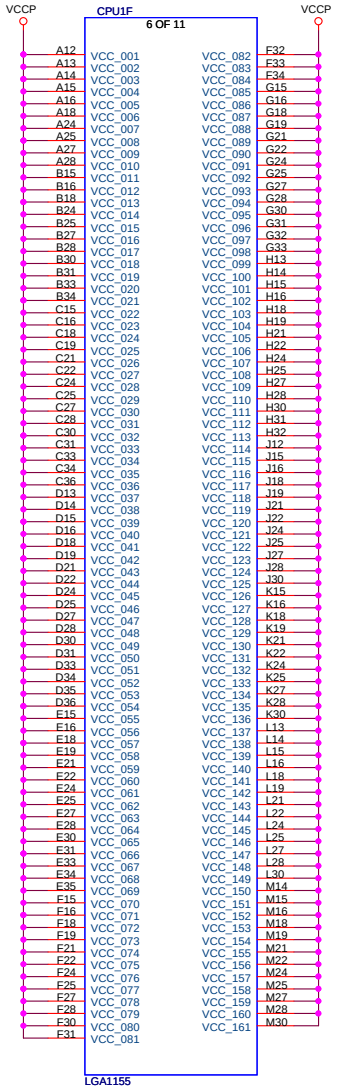
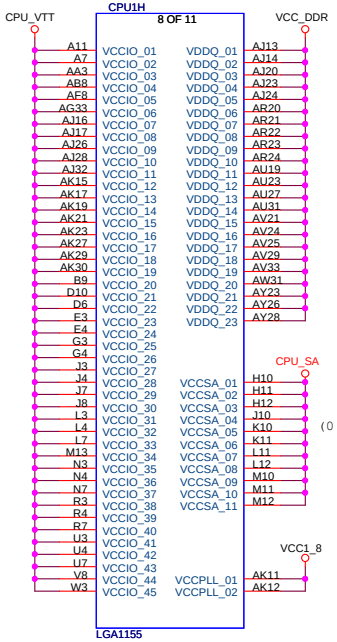
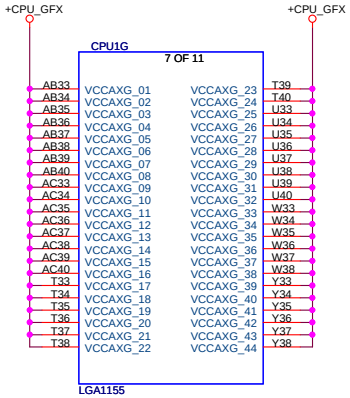
(1.05V / 1.00V)



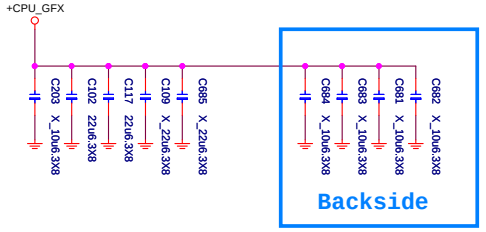




(0.925V / 0.85V)

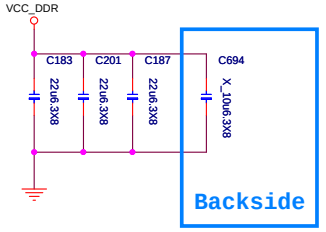
VCCP: 112A
CPU_VTT: 8.2A
CPU_SA: 8.8A
VCC_DDR: 4.5A
VCC1_8: 1.6A

+CPU_GFX Decoupling



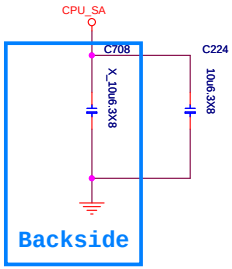
CPU SOCKET CAVITY CAPS

+1.5V_DDR3-Decoupling

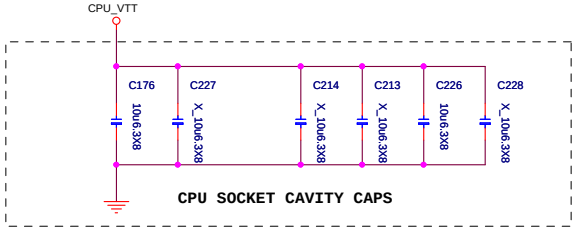


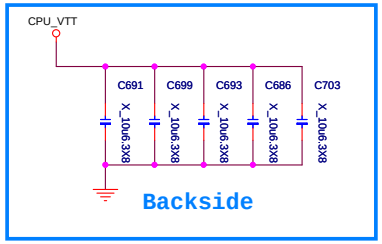
CPU SOCKET CAVITY CAPS

Vinafix.com

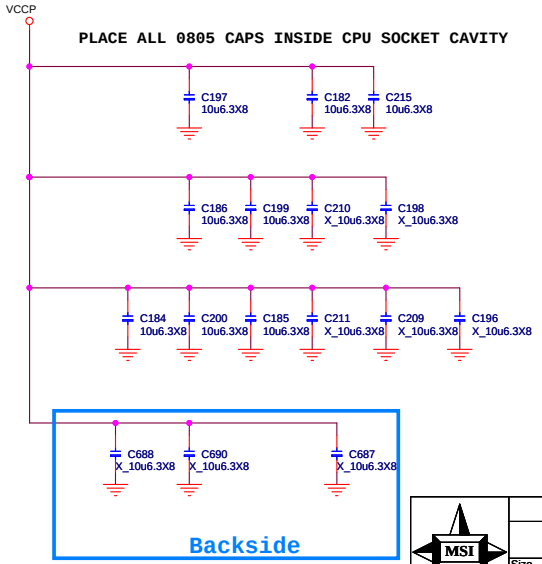


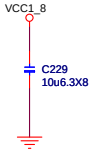
+CPU_VTT Decoupling





+CPU_VCCP-Decoupling





MICRO-STAR INT'L CO.,LTD		
MS-7788		
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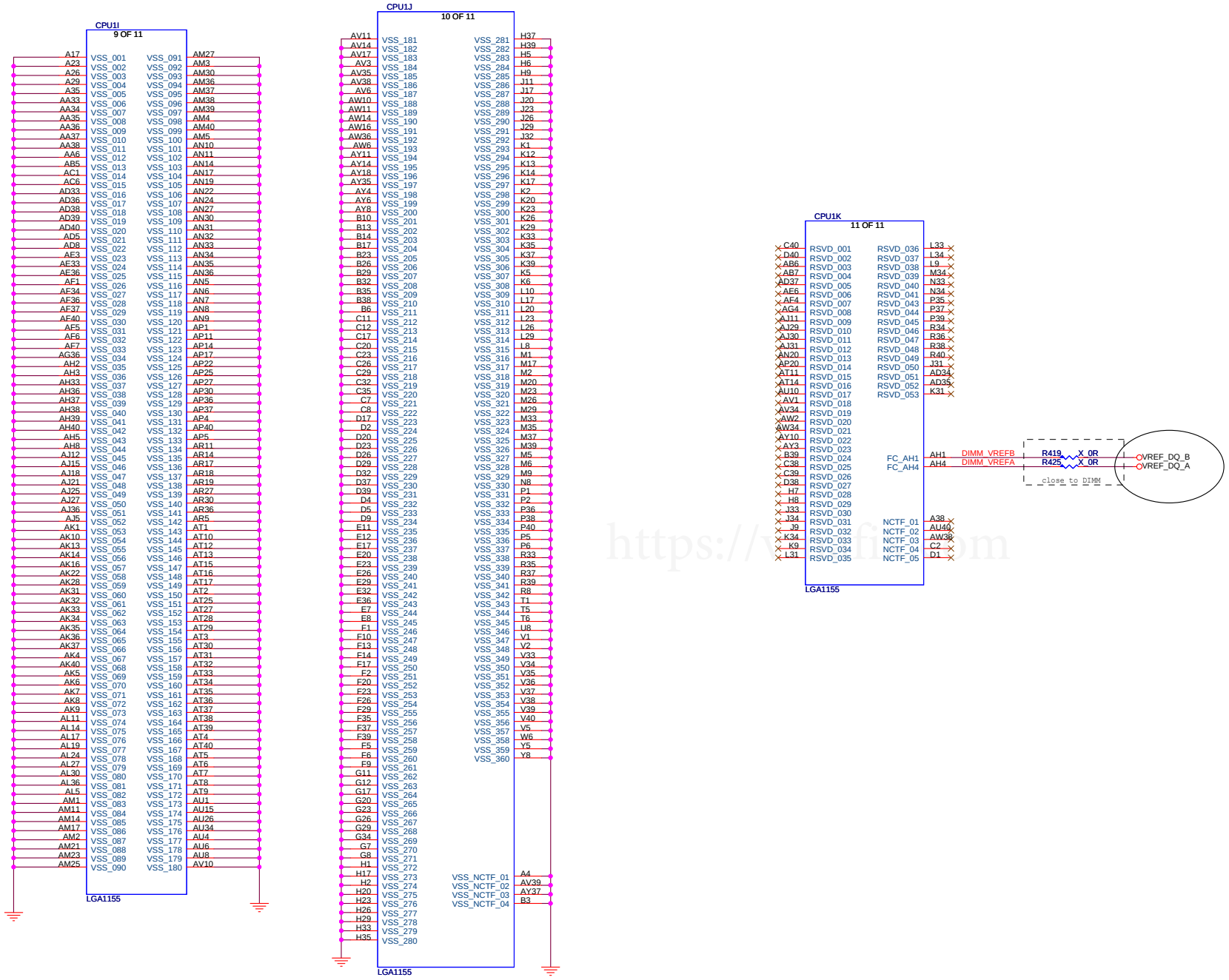

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-7788	
Size: Custom	Document Description: CPU-GND	Rev: 30
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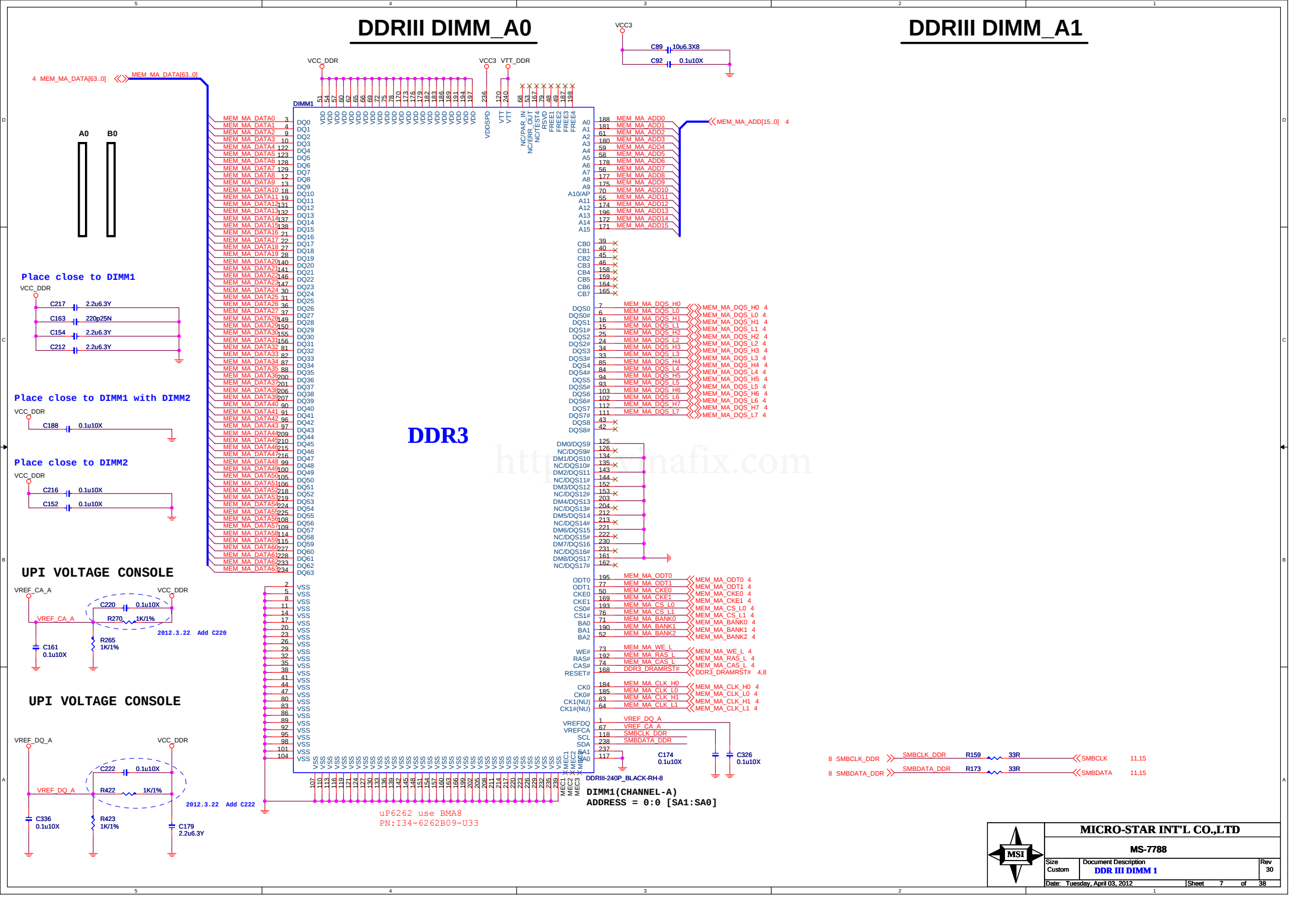
DDRIII DIMM_A0

DDRIII DIMM_A1



MICRO-STAR INT'L CO.,LTD	
MS-7788	
Size: Custom	Document Description: DDR III DIMM 1
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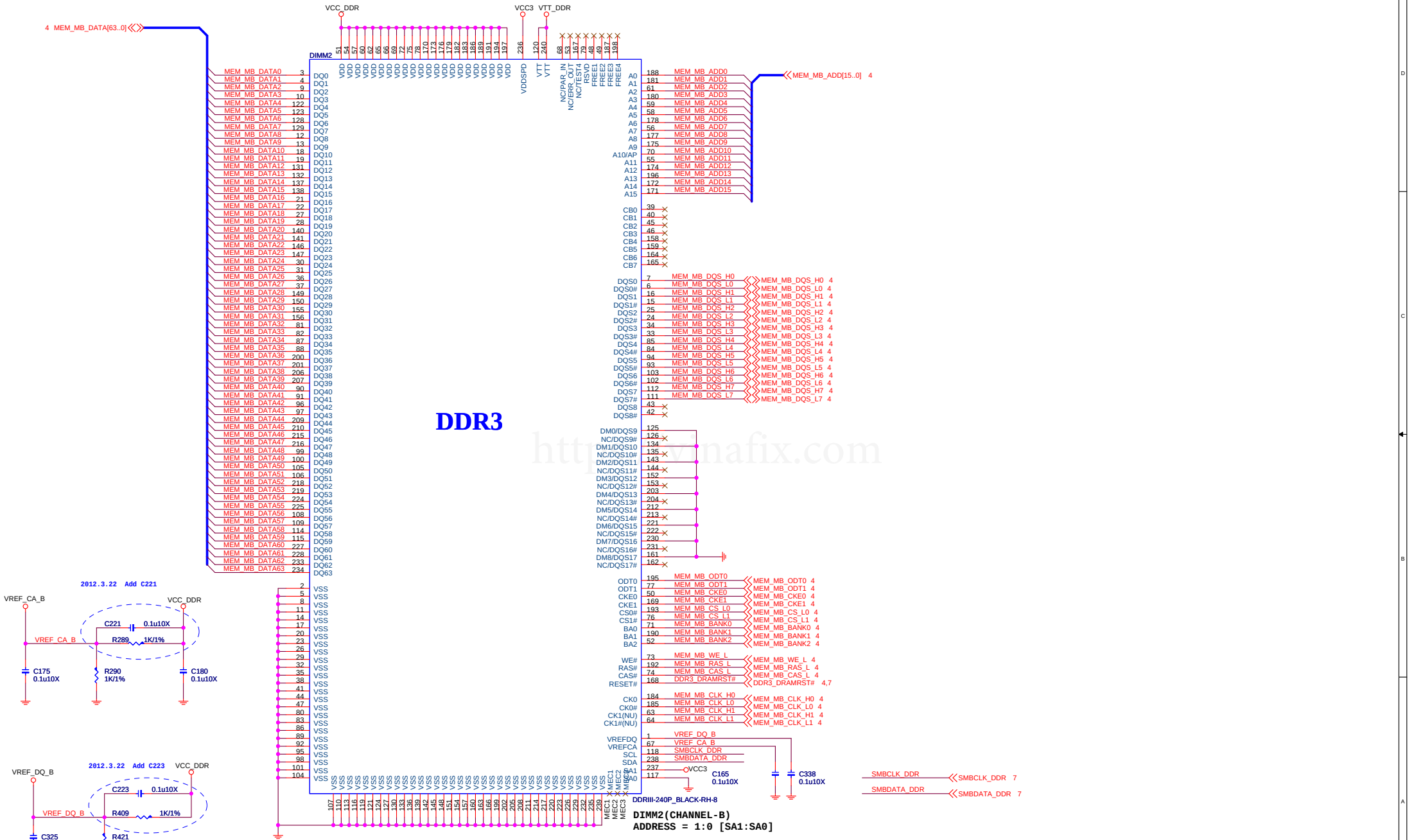
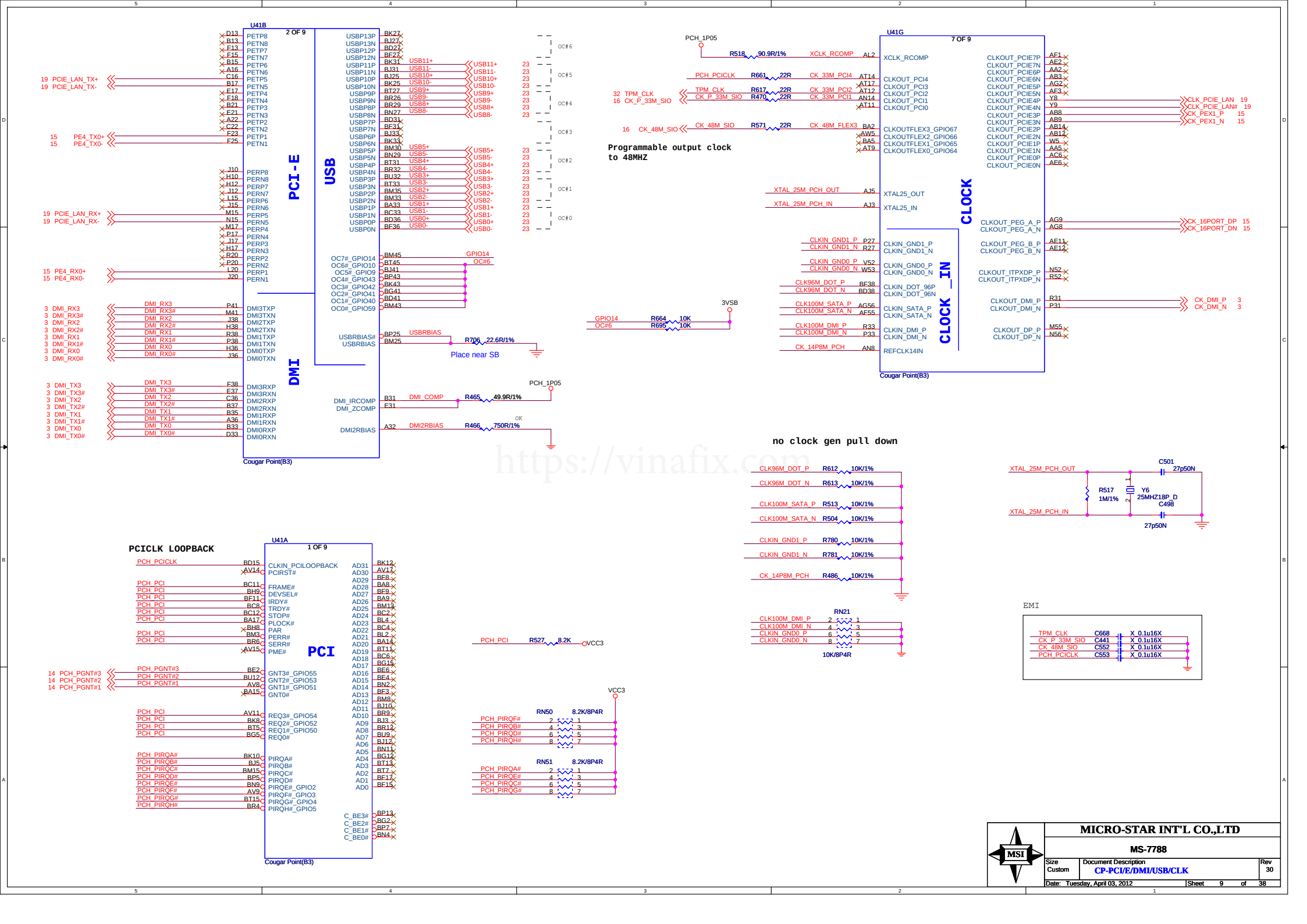
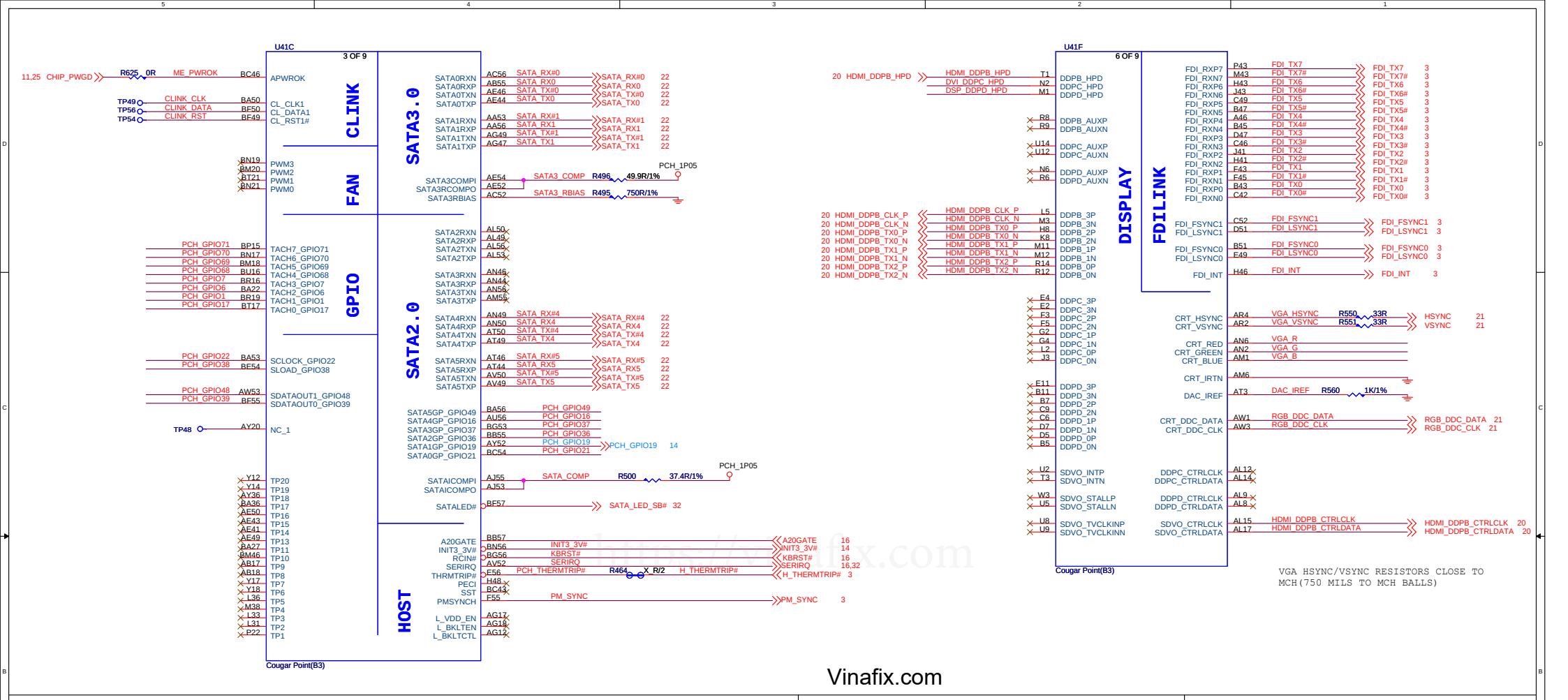
DDRIII DIMM_B0

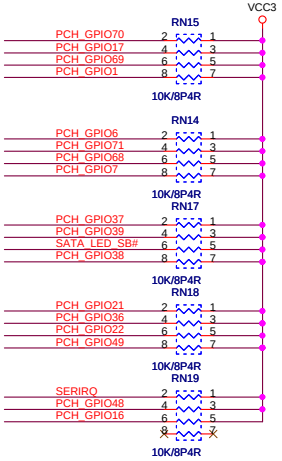


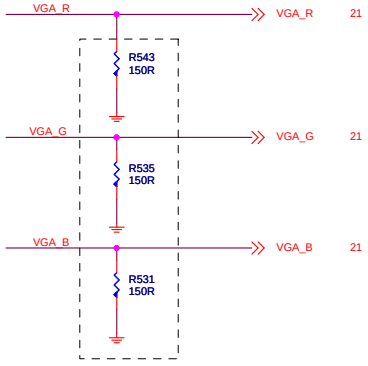
MICRO-STAR INT'L CO.,LTD	
MS-7788	
Size: Custom	Document Description: DDR III DIMM 2
Rev: 30	
Date: Tuesday, April 03, 2012	Sheet 8 of 38


U41B
2 OF 9
PCI-E
USB
DMI
Cougar Point(B3)
U41G
7 OF 9
CLOCK
CLOCK_IN
Cougar Point(B3)
Programmable output clock to 48MHZ
Place near SB
U41A
1 OF 9
PCI
PCICLK LOOPBACK
Cougar Point(B3)
no clock gen pull down
EMI
MICRO-STAR INT'L CO.,LTD
MS-7788
CP-PCI/E/DMI/USB/CLK
Size Custom
Rev 30
Date: Tuesday, April 03, 2012
Sheet 9 of 38



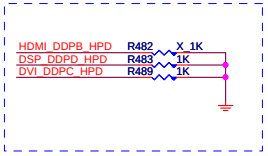
Pull HIGH for PCH



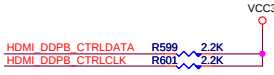


Close to PCH within 250 mils.

No VGA(pull down)



Enable VGA(CTRLCLK/DATA Pull High)



MICRO-STAR INT'L CO.,LTD		
MS-7788		
Size: Custom	Document Description: CP-SATA/HOST/FAN/GPIO/VGA	Rev: 30
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REQUIRED STRAPS

LPC

16,32 LPC_FRAME#	LPC_FRAME#	BG17	FWH4_LFRAME#
16,32 LPC_AD3	LPC_AD3	BG20	FWH3_LAD3
16,32 LPC_AD2	LPC_AD2	BJ20	FWH2_LAD2
16,32 LPC_AD1	LPC_AD1	BJ17	FWH1_LAD1
16,32 LPC_AD0	LPC_AD0	BK15	FWH0_LAD0
	LPC_DRQ#1	BA20	LDRQ1#_GPIO23
16 LPC_DRQ#0	LPC_DRQ#0	BK17	LDRQ0#

AUDIO

		BJ22	HDA_SDIN3
		BK22	HDA_SDIN2
		BE22	HDA_SDIN1
18 AZ_SDIN0		BD22	HDA_SDIN0
14 AZ_SDOUT_R	AZ_SDOUT_R	BT23	HDA_SDO
	AZ_BITCLK_R	BU22	HDA_BCLK
14 AZ_SYNC_R	AZ_SYNC_R	BP23	HDA_SYNC
	AZ_RST#_R	BC22	HDA_RST#

SPI

10,25 CHIP_PWGD		D53	PROCPWRGD
3 CPU_PWRGD	VRM_PGD R606 X_R/2 SYS_PWROK	BJ53	SYS_PWROK
25 VRM_PGD	PWRBTN#	BT43	PWRBTN#
16 PWRBTN#	R626 X_R/2 CHIP_PWGD	BJ38	PWROK
16 SIO_ATXOK	PCH_MEM_PWRGD	BG46	DRAMPWROK
3 PCH_MEM_PWRGD	DPWROK_CP	BT37	DPWROK
16 DPWROK_CP	DSWVRMEN	BR42	DSWVRMEN
14 DSWVRMEN	RSMRST#	BK38	RSMRST#
16 RSMRST#	FP_RST#	BE52	SYS_RESET#
3,32 FP_RST#	RI#	BJ48	RI#
	SB_WAKE#	BC44	WAKE#
15,19 SB_WAKE#	INTRUDER#	BM38	INTRUDER#
14 PCH_INTVRMEM	PCH_INTVRMEM	BN41	INTVRMEN
	CP_SPI_MOSI R747 X_R/2 PCH_SPI_MOSI	AU53	SPI_MOSI
	CP_SPI_MISO	AT55	SPI_MISO
	CP_SPI_CS# R740 X_R/2 PCH_SPI_CS#	AR56	SPI_CS1#
	CP_SPI_CLK R753 X_R/2 PCH_SPI_CLK	AT57	SPI_CS0#
		AR54	SPI_CLK

RTC

	RTCX1	BN39	RTCX2
	RTCX2	BR39	RTCX1
16 RTCRST#	RTCRST#	BT41	RTCRST#
	SRTCRST#	BN37	SRTCRST#

JTAG (SUS)

	PCH_JTAGRST#	BC49	JTAG_RST/TP12
	PCH_JTAGTCK	BA43	JTAG_TCK
	PCH_JTAGTMS	BC50	JTAG_TMS
	PCH_JTAGTDO	BF47	JTAG_TDO
	PCH_JTAGTDI	BC52	JTAG_TDI

U41D — 4 OF 9 — Cougar Point(B3)

SMB

	SMBALERT#_GPIO11	BN49	PCH_SMBALERT
	SMBCLK	BT47	SMBCLK
	SMBDATA	BR49	SMBDATA
	SML0ALERT#_GPIO60	BU49	PCH_SML0ALERT#
	SML0CLK	BT51	SMLINK0_CLK
	SML0DATA	BM50	SMLINK0_DATA
	SML1ALERT#_PCHHOT#_GPIO74	BR46	PCH_SML1ALERT#
	SML1CLK_GPIO58	BJ46	PCH_SML1CLK
	SML1DATA_GPIO75	BK46	PCH_SML1DATA

GPIO

	BMBUSY#_GPIO0	AW55	BM_BUSY#
	GPIO8	BP51	PCH_GPIO8
	LAN_PHY_PWR_CTRL_GPIO12	BK50	PCH_GPIO12
	HDA_DOCK_RST#_GPIO13	BA25	SIO_PME#
	GPIO15	BM55	SPI_HOLD_GPO#
	PCIECLKRQ2#_GPIO20	AV43	PCIECLKREQ2#
	GPIO24_MEM_LED	BP53	PCH_GPIO24
	GPIO27	BJ43	PCH_GPIO27
	GPIO28	BJ55	PCH_GPIO28
	SLP_LAN#_GPIO29	BH49	SLP_LAN#
	SUSWARN#_SUSPWRDNACK_GPIO30	BU46	SUSWARN#_CP
	GPIO31	BG43	PCH_GPIO31
	CLKRUN#_GPIO32	BC56	PCH_SPI_WP#
	HDA_DOCK_EN#_GPIO33	BC25	PCH_GPIO33
	STP_PCI#_GPIO34	BL56	STP_PCI#
	GPIO35	BJ57	PCH_GPIO35
	PCIECLKRQ5#_GPIO44	BL54	PCIECLKREQ5#
	PCIECLKRQ6#_GPIO45	AV44	PCIECLKREQ6#
	PCIECLKRQ7#_GPIO46	BP55	PCIECLKREQ7#
	GPIO57	BT53	PCH_GPIO57
	SUS_STAT#_GPIO61	BN54	SUS_STAT#
	SUSCLK_GPIO62	BA47	SUS_CLK
	BATLOW#_GPIO72	AV46	PCH_GPIO72
	PLTRST#	BK48	PLTRST#
	SLP_S3#	BM53	SLP_S3#
	SLP_S4#	BN52	SLP_S4#
	SLP_S5#_GPIO63	BH50	SLP_S5#
	SLP_A#	BC41	SLP_A#_R
	SLP_SUS#	BD43	SLP_SUS#_CP
	SUSACK#	BP45	SUSACK#_CP
	SPKR	BE56	SPKR

GPIO73 18

	BM_BUSY#	R529	10K/1%
Internal pull-up	LPC_DRQ#0	R714	X_10K
Internal pull-up	LPC_DRQ#1	R702	X_10K
	STP_PCI#	R622	10K/1%
	SMBCLK	R666	1.8K
	SMBDATA	R667	1.8K
	FP_RST#	R562	10K/1%
	PCH_GPIO35	R624	X_10K

VCC3

	FP_RST#	R564	X_10K/1%
	SIO_PME#	R703	10K/1%
	SPI_HOLD_GPO#	R641	X_8.2K
	PCIECLKREQ2#	R575	X_10K/1%
	PCIECLKREQ5#	R642	X_10K/1%
	PCIECLKREQ6#	R547	X_10K/1%
	PCIECLKREQ7#	R645	X_10K/1%
	SLP_LAN#	R647	X_10K/1%
	PCH_GPIO24	R655	X_220R
	PCH_GPIO28	R623	X_10K/1%
	PCH_SMBALERT	R627	10K/1%
	PCH_GPIO72	R538	10K/1%
	SB_WAKE#	R636	1K
	RI#	R658	10K/1%
	SMLINK0_CLK	R668	10K/1%
	SMLINK0_DATA	R699	10K/1%
	PCH_SML0ALERT#	R660	10K/1%
	PCH_SML1CLK	R659	10K/1%
	PCH_SML1DATA	R674	10K/1%
	PCH_SML1ALERT#	R697	10K/1%

3VSB

CRB pull down

	PCH_GPIO57	R690	X_10K/1%
		R669	10K/1%

	SUSWARN#_CP	R682	X_0R
	RSMRST#	R806	X_0R

SUSACK#_CP / DPWROK_CP

	PCH_GPIO31	R675	10K/1%
	PCH_GPIO27	R762	10K/1%
	SUSACK#_CP	R16	10K
	DPWROK_CP	R25	10K

3VA

	PCIECLKREQ2#	R574	10K/1%
	PCIECLKREQ5#	R634	10K/1%
	PCIECLKREQ6#	R539	10K/1%
	PCIECLKREQ7#	R640	10K/1%
	PCH_GPIO33	R717	X_1K

PCIECLKREQ can't find 0/1/3/4

I_VSB3V — R938 0R/6 — 3VA

5VSB — R720 4.7K — RSMRST# — C606 X_1u16Y6 — R721 10K/1%

3VA

20mA

ATX_5VSB — C827 X_1u6.3X

U87 X_UP7707M5-00_SOT23-5-RH (VIN, VOUT, EN, GND, NC) — 3VA

C828 X_0.1u16X — R961 X_10K/1% — C826 X_4.7u10Y8

3VA_REF — R959 X_3.16K/1%

ATX_5VSB — R983 X_47K

16 CP_3VA_OFF — Q75 X_2N7002

SPI DEBUG PROT

Close to SPI ROM

VCC3 — JSPI1 — SPI_MISO — CP_SPI_CS# — SPI_HOLD# — CP_SPI_MOSI — CP_SPI_CLK — C644 X_0.1u16X

H2X5[10]M-2PITCH_BLACK-RH-2

Part Number:N31-2051451-H06

JTAG PULL HIGH and PULL DOWN

3VSB — PCH_1P05

R643	200R	PCH_JTAGTDO	R648	X_51R	
R557	200R	PCH_JTAGTDI	R558	X_51R	
R598	200R	PCH_JTAGTMS	R576	X_51R	
R610	20K/1%	PCH_JTAGRST#	R609	X_51R	
R635	100R/1%	PCH_JTAGTDO			
R556	100R/1%	PCH_JTAGTDI			
R597	100R/1%	PCH_JTAGTMS			
R608	10K/1%	PCH_JTAGRST#			
R596	51R	PCH_JTAGTCK			

RTC Block

Close to PCH

C630 10p50N — RTCX1 — Y7 32.768KHZ12.5P-D — R728 10M — RTCX2 — C632 10p50N

Chassis Intrusion

VBAT — R678 1M — JCI1 — INTRUDER# — H1X2M_BLACK-RH

33 Ohm series near PCH

18 AZ_RST# — R59 33R — AZ_RST#_R

RN30 33R/8P4R

18 AZ_SYNC — AZ_SYNC_R

18 AZ_BITCLK — AZ_BITCLK_R

18 AZ_SDOUT — AZ_SDOUT_R

AZ_BITCLK — C641 X_10P50N

RTC and CLR_CMOS

20mil

Clear CMOS

CMOS CLEAR JUMPER JBAT1 Clear CMOS	
1 - 2	Clear CMOS

3VA — D26 S-BAT54C_SOT23 — VBAT — R494 20K/6 — RTCRST# — JBAT1 — H1X2M_BLACK-RH

C462 1u10Y6 — C677 1u10Y6

BAT1 — BAT2P_BLACK-RH-1 — R478 1K

VBAT — R679 20K/1% — SRTCRST# — C585 1u10Y6

N91-01F0151-H06

2012.3.22 modify to 0603 size

SPI FLASH ROM

Place close to SB.

VCC3 — C649 0.1u10X — C14 10u10Y8 — R752 2.2K

CP_SPI_MISO — R744 15R — CP_SPI_CS# — SPI1 — SPI_HOLD# — R750 X_0R — SPI_HOLD_GPO#

PCH_SPI_WP# — R828 0R — SPI_WP# — CP_SPI_CLK — CP_SPI_MOSI

VCC3 — R738 2.2K

W25Q32BVSSIG-HF

32M : M31-25L3203-M24

Reserved for BIOS control used

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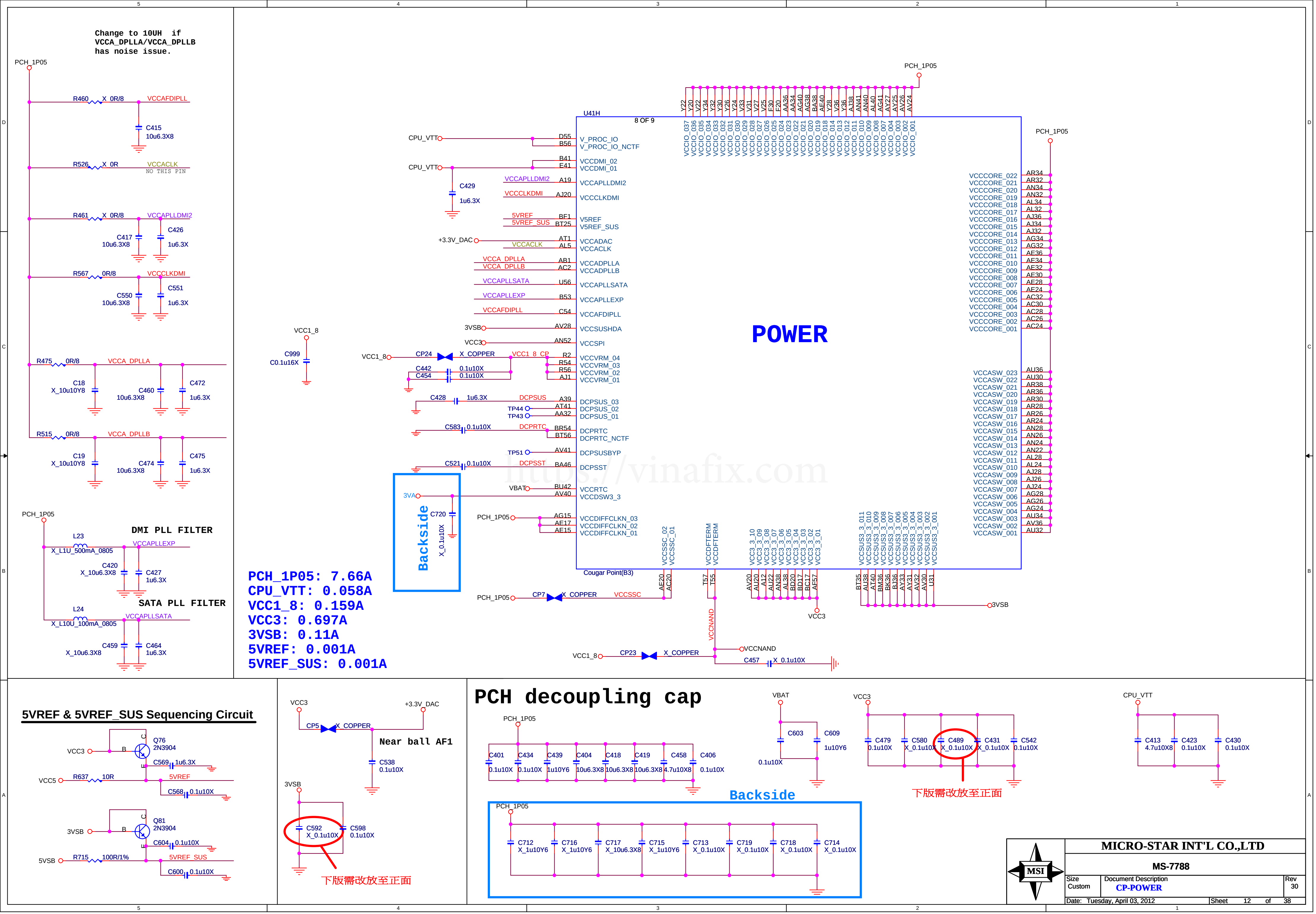
Reserved for BIOS control used



Change to 10UH if VCCA_DPLLA/VCCA_DPLLB has noise issue.
PCH_1P05
R460 X_0R/8 VCCAFDIPLL
C415 10u6.3X8
R526 X_0R VCCACLK NO THIS PIN
R461 X_0R/8 VCCAPLLDMI2
C417 10u6.3X8
C426 1u6.3X
R567 0R/8 VCCCLKDMI
C550 10u6.3X8
C551 1u6.3X
R475 0R/8 VCCA_DPLLA
C18 X_10u10Y8
C460 10u6.3X8
C472 1u6.3X
R515 0R/8 VCCA_DPLLB
C19 X_10u10Y8
C474 10u6.3X8
C475 1u6.3X
DMI PLL FILTER
L23 X_L1U_500mA_0805 VCCAPLLEXP
C420 X_10u6.3X8
C427 1u6.3X
SATA PLL FILTER
L24 X_L10U_100mA_0805 VCCAPLLSATA
C459 X_10u6.3X8
C464 1u6.3X
VCC1_8
C999 C0.1u16X
U41H 8 OF 9
POWER
Cougar Point(B3)
CPU_VTT
V_PROC_IO
V_PROC_IO_NCTF
VCCDMI_02
VCCDMI_01
C429 1u6.3X
VCCAPLLDMI2
VCCCLKDMI
V5REF
V5REF_SUS
+3.3V_DAC
VCCADAC
VCCACLK
VCCADPLLA
VCCADPLLB
VCCAPLLSATA
VCCAPLLEXP
VCCAFDIPLL
3VSB VCCSUSHDA
VCC3 VCCSPI
CP24 X_COPPER VCC1_8_CP
VCCVRM_04
VCCVRM_03
VCCVRM_02
VCCVRM_01
C442 0.1u10X
C454 0.1u10X
C428 1u6.3X DCPSUS
DCPSUS_03
DCPSUS_02
DCPSUS_01
TP44
TP43
C583 0.1u10X DCPRTC
DCPRTC
DCPRTC_NCTF
TP51 DCPSUSBYP
C521 0.1u10X DCPSST
DCPSST
VBAT VCCRTC
3VA VCCDSW3_3
Backside
C720 X_0.1u10X
PCH_1P05 VCCDIFFCLKN_03
VCCDIFFCLKN_02
VCCDIFFCLKN_01
VCCIO_037 … VCCIO_001
VCCCORE_022 … VCCCORE_001
VCCASW_023 … VCCASW_001
VCCSSC_02
VCCSSC_01
VCCDFTERM
VCC3_3_10 … VCC3_3_01
VCCSUS3_3_011 … VCCSUS3_3_001
CP7 X_COPPER VCCSSC
VCCNAND
CP23 X_COPPER
C457 X_0.1u10X
PCH_1P05: 7.66A
CPU_VTT: 0.058A
VCC1_8: 0.159A
VCC3: 0.697A
3VSB: 0.11A
5VREF: 0.001A
5VREF_SUS: 0.001A
5VREF & 5VREF_SUS Sequencing Circuit
Q76 2N3904
C569 1u6.3X
VCC5 R637 10R 5VREF
C568 0.1u10X
Q81 2N3904
C604 0.1u10X
5VSB R715 100R/1% 5VREF_SUS
C600 0.1u10X
CP5 X_COPPER
Near ball AF1
C538 0.1u10X
C592 X_0.1u10X
C598 0.1u10X
下版需改放至正面
PCH decoupling cap
C401 0.1u10X
C434 0.1u10X
C439 1u10Y6
C404 10u6.3X8
C418 10u6.3X8
C419 10u6.3X8
C458 4.7u10X8
C406 0.1u10X
VBAT
C603 0.1u10X
C609 1u10Y6
C479 0.1u10X
C580 X_0.1u10X
C489 X_0.1u10X
C431 X_0.1u10X
C542 0.1u10X
下版需改放至正面
C413 4.7u10X8
C423 0.1u10X
C430 0.1u10X
Backside
C712 X_1u10Y6
C716 X_1u10Y6
C717 X_10u6.3X8
C715 X_1u10Y6
C713 X_0.1u10X
C719 X_0.1u10X
C718 X_0.1u10X
C714 X_0.1u10X
MSI
MICRO-STAR INT'L CO.,LTD
MS-7788
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Document Description CP-POWER
Rev 30
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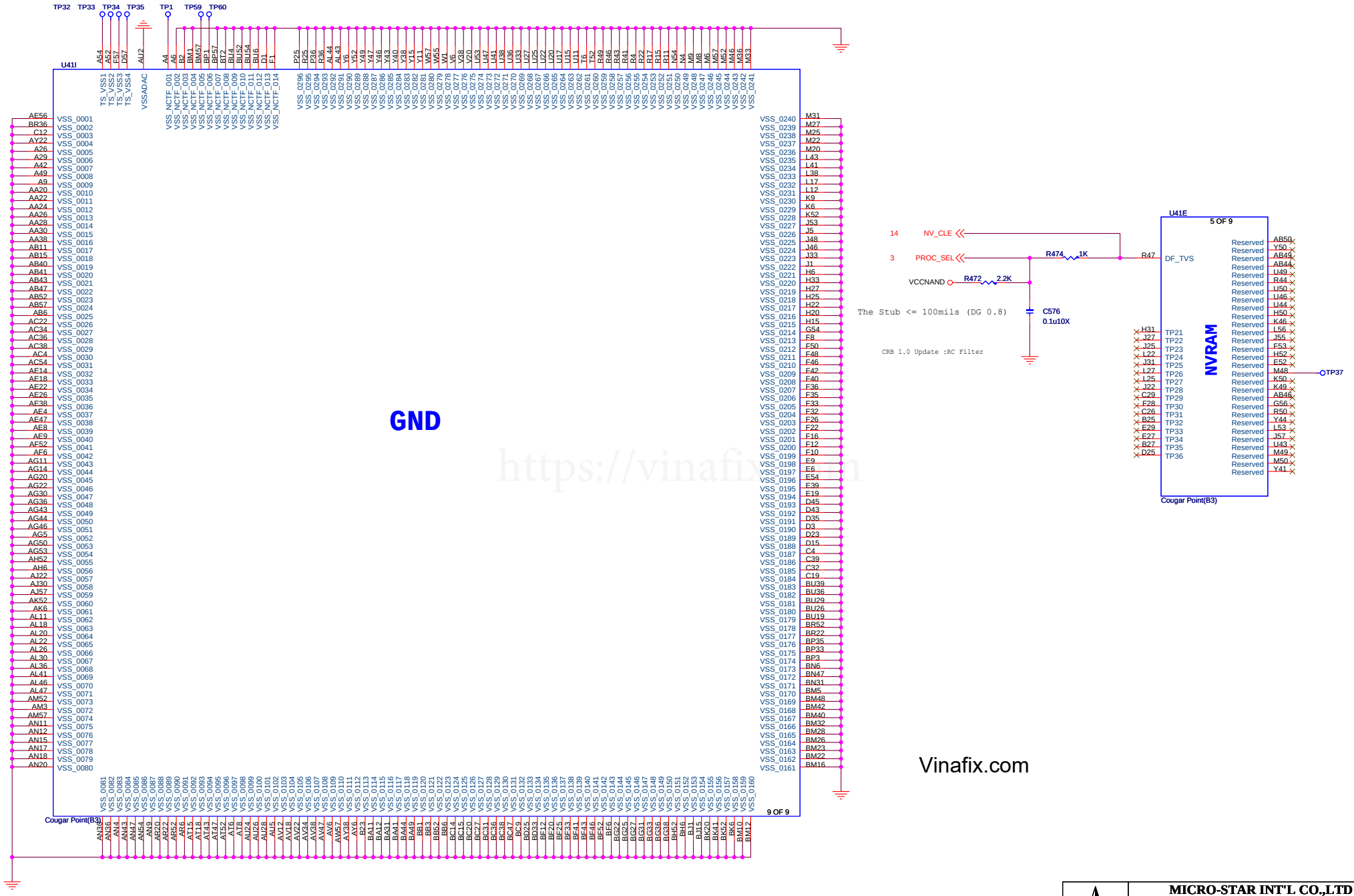

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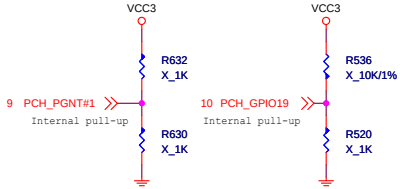
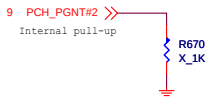
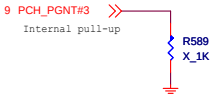
PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

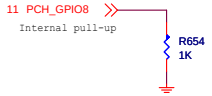




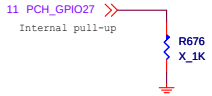
DMI AC/DC MODE
0 : AC
1 : DC *



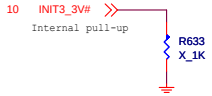
Topblock swap override when pull-low
Signal has a weak internal pull-up



GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)

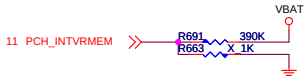


GPIO28
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INT3_3V#
0 : ??????????????
1 : ?????????????? *

1: INIT3_3V to asserted for 16 PCI clock to reset the processor by some evens occur.
0: Can not to reset the processor.

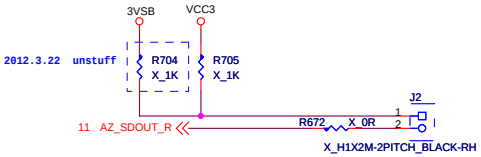


INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltageregulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.

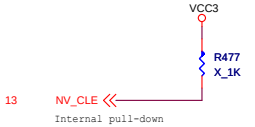


HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????

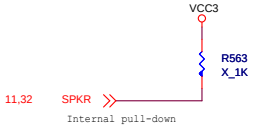
HDA_SDO has internal pull down.
Default should be connected to SDIN of codec, no pull up/down.
To Disable ME need to have a jumper to pull high

HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY

GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT

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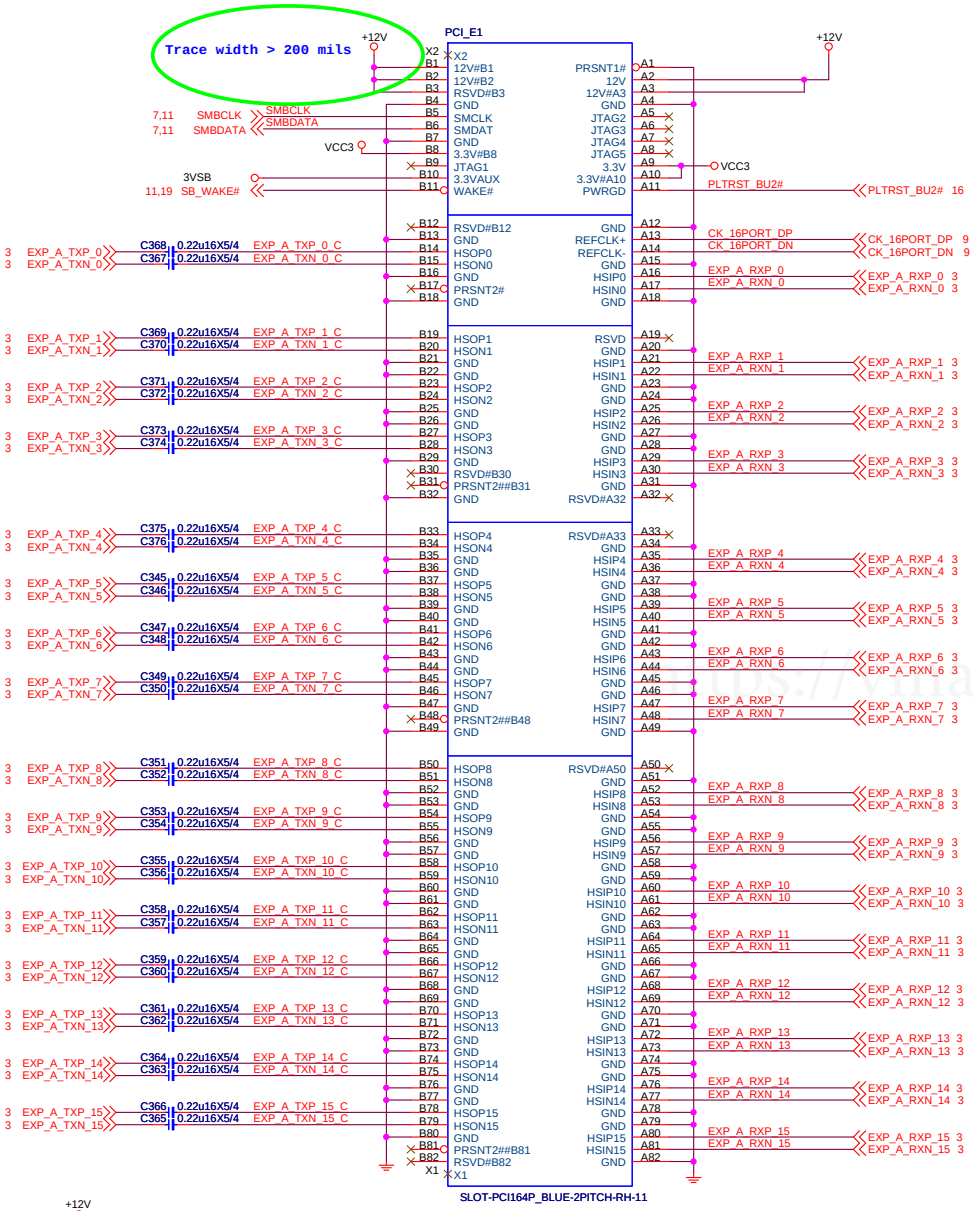
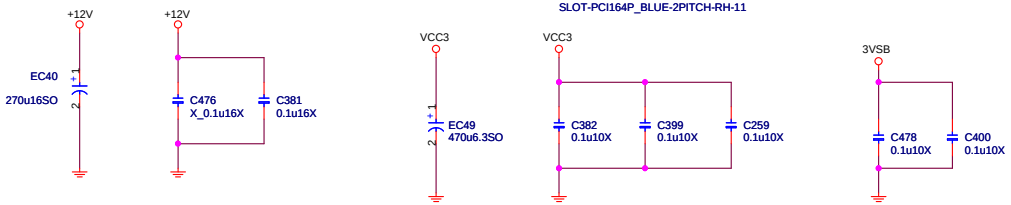
PCI_Express X16 Slot

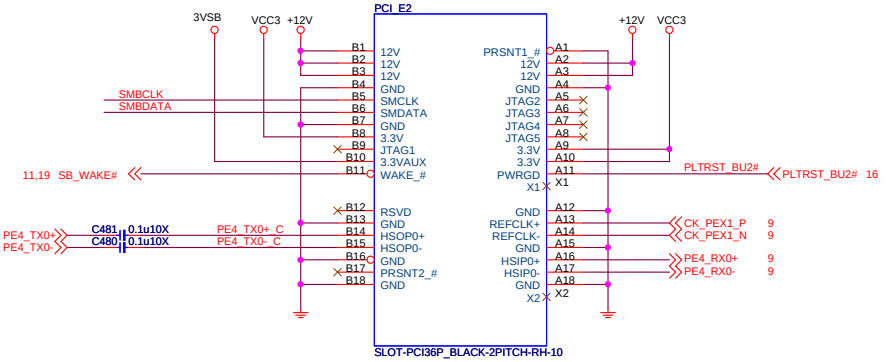
N11-1640971-K06

Trace width > 200 mils





PCI EXPRESS x1-PORT



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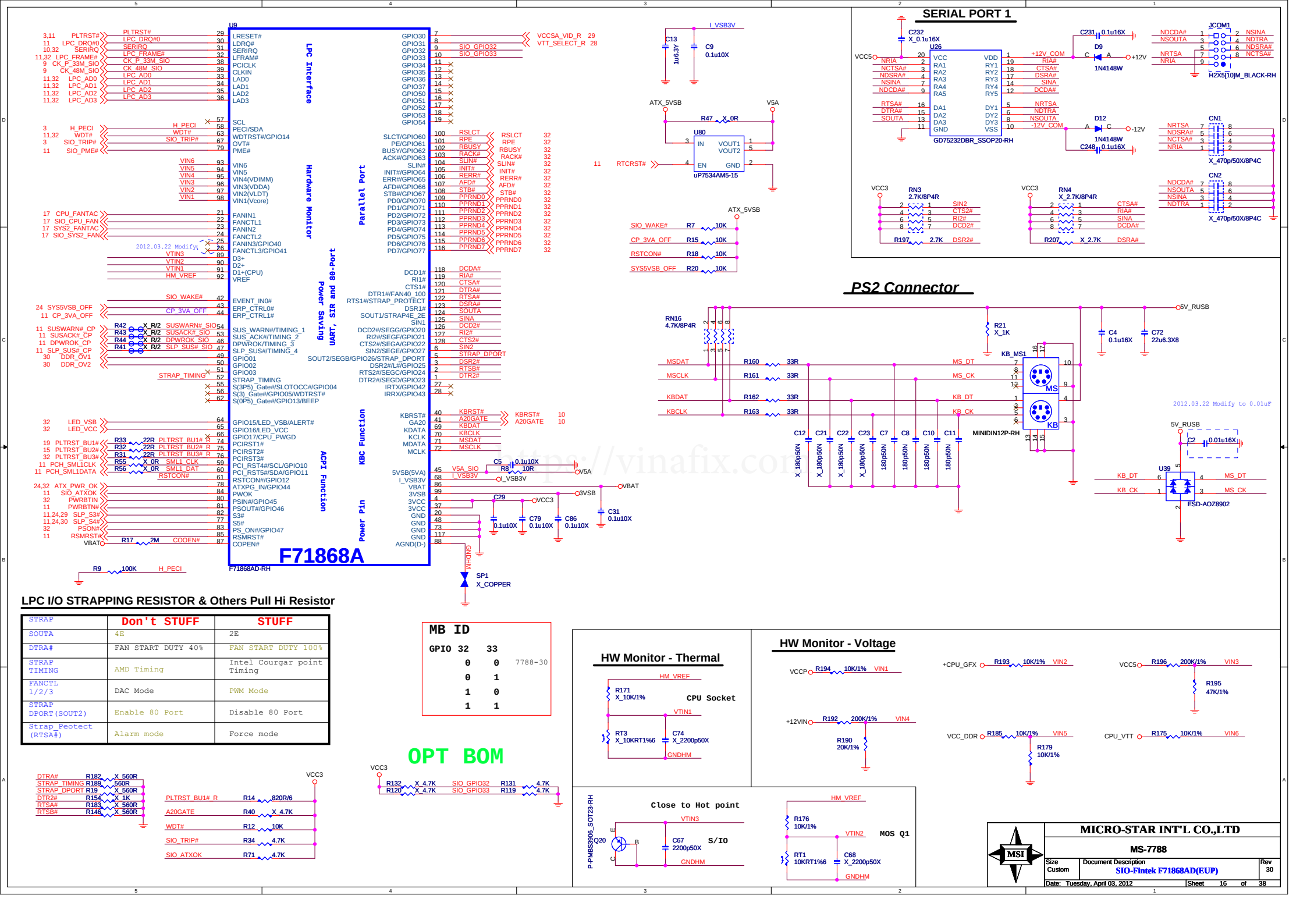

STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP TIMING	AMD Timing	Intel Courgar point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP DPORT(SOUT2)	Enable 80 Port	Disable 80 Port
Strap_Peotect (RTSA#)	Alarm mode	Force mode

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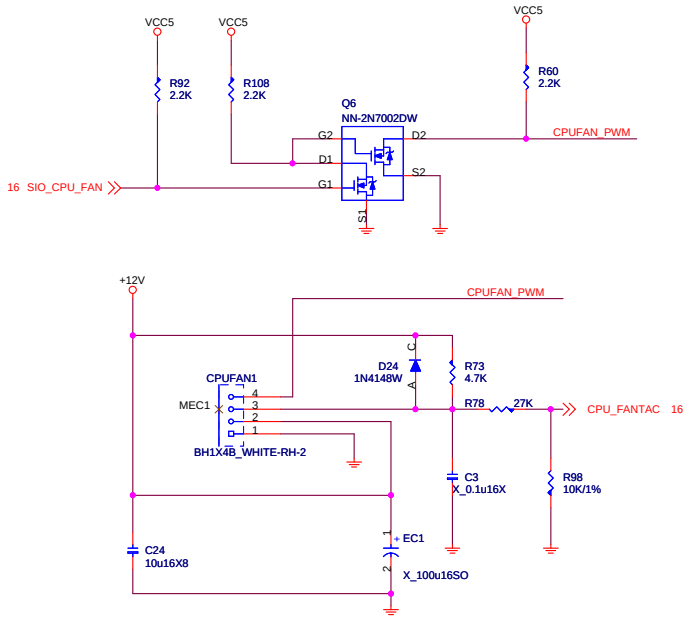
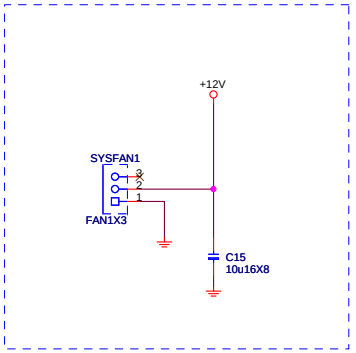
CPU FAN-COUNTROL CIRCUIT

From SIO SYSTEM FAN1



SYSTEM FAN3-COUNTROL CIRCUIT

From SIO SYSTEM FAN3

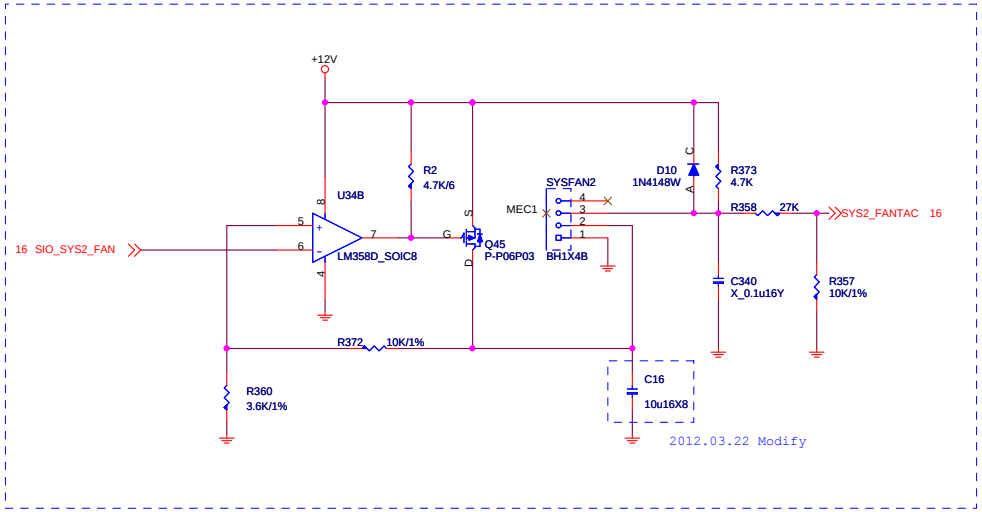


2012.03.22 Modify follow Module

CHASSIS FAN-COUNTROL CIRCUIT

From SIO SYSTEM FAN2

2012.03.22 Modify follow Module



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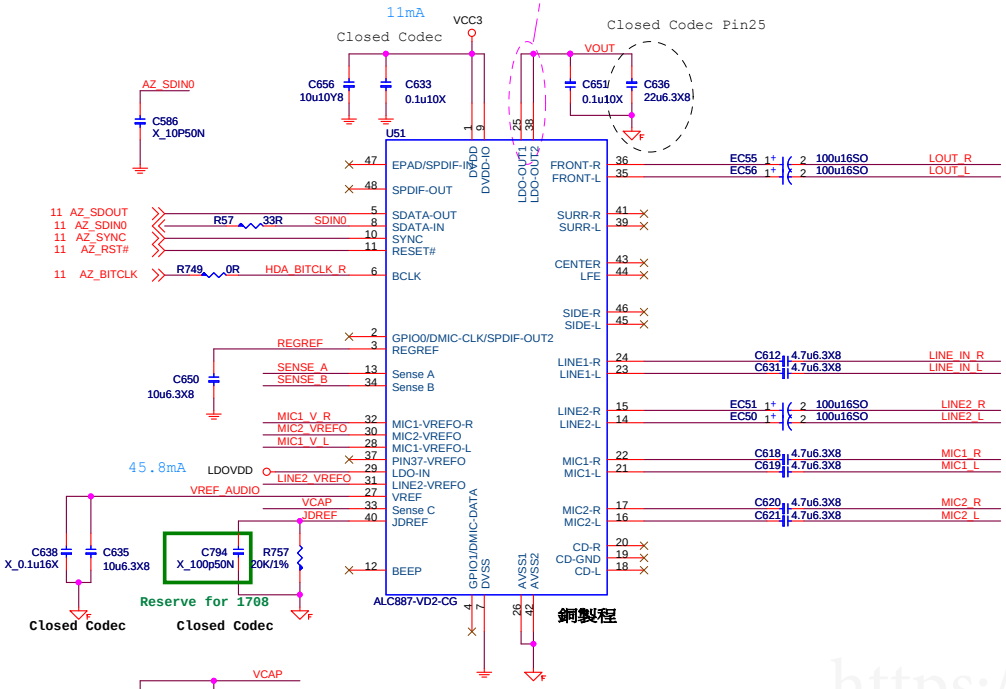
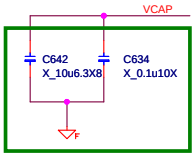
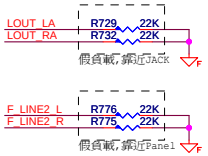
ALC887-VD
VT1708S CE

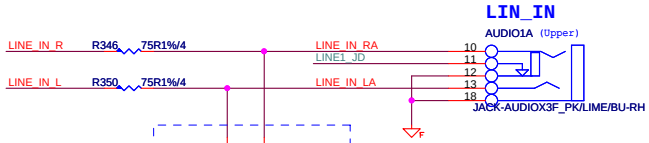
Codec Pin25 & 38連接的Layout，以最短路徑，至少40mils線寬連接。

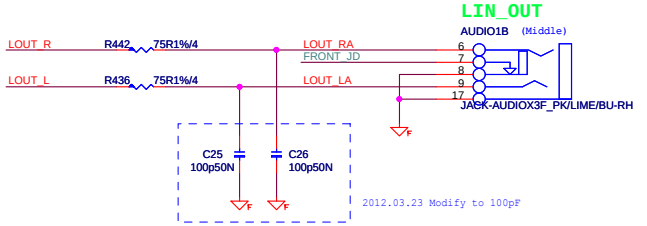


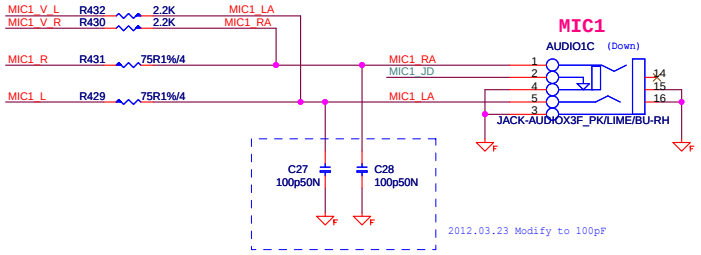


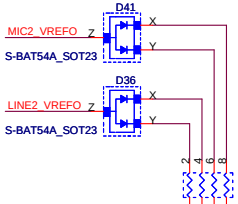
當串接電容有極性時，需上對地電阻

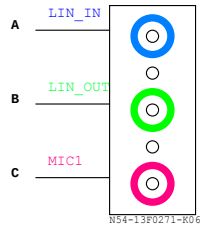




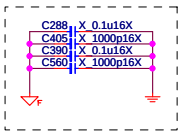


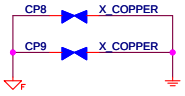


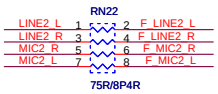


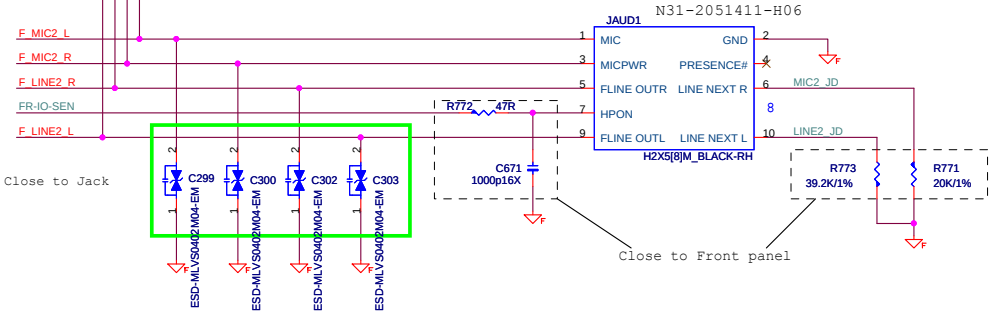


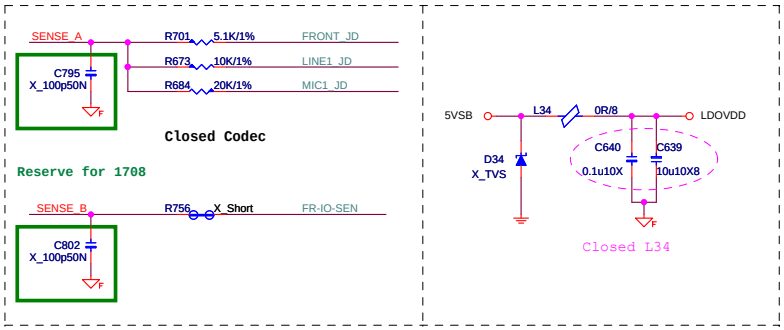
EMI











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	MS-7788	
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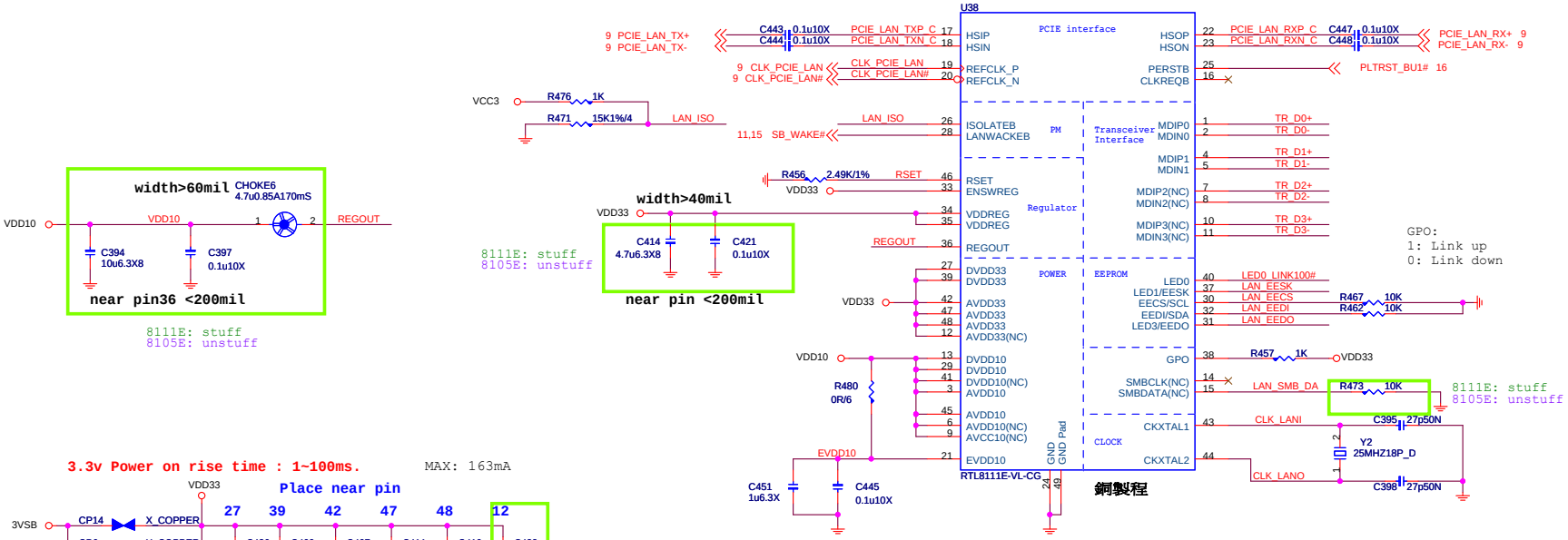
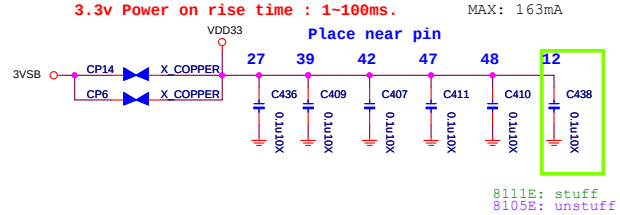
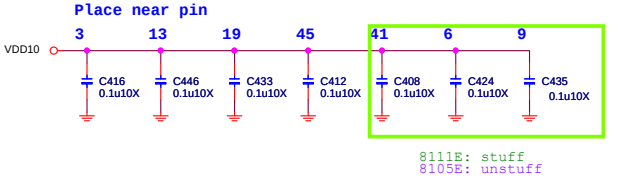
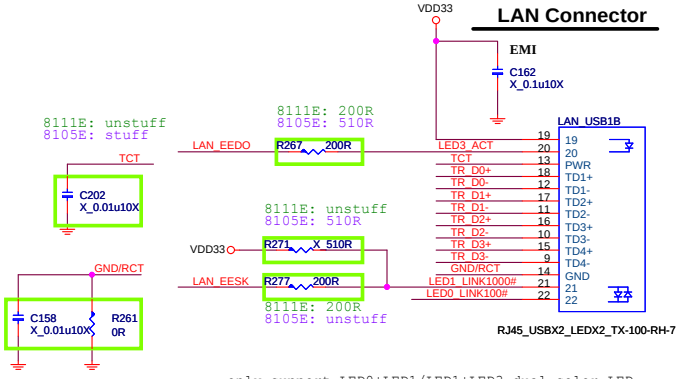
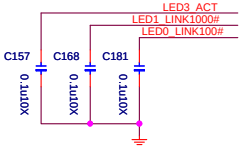
RTL8105E 10/100M LAN
co-lay RTL8111E Giga LAN











Giga-Lan	10/100-Lan
N58-22F0731	N58-22F0771
Link Yellow Active Blinking 1000 Orange 100 Green 10 None	Link Yellow Active Blinking 100 Green 10 None
19, 20 — 250R — Yellow 21, 22 — 250R — Green	19, 20 — Yellow 21, 22 — Green

8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
S0 ALDPS	3.2	11

8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

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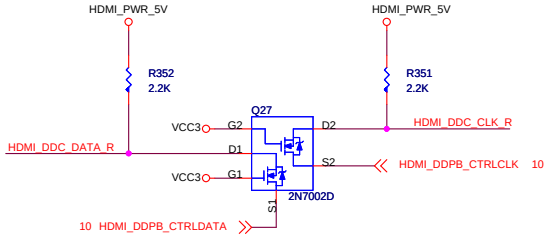
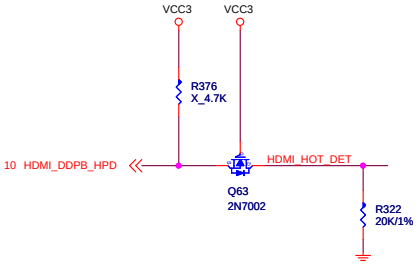
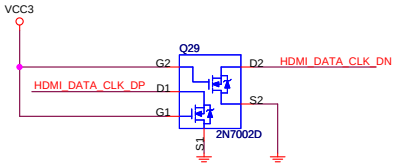
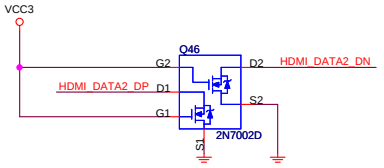
HDMI level shifter

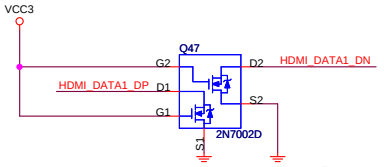
HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)

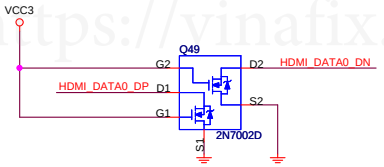


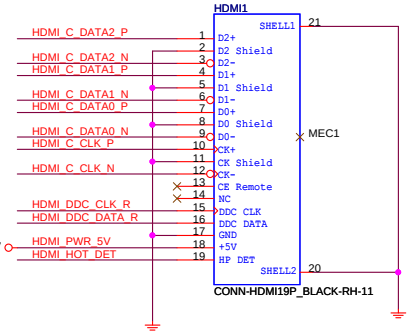


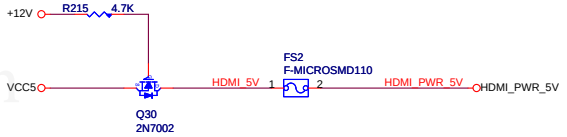


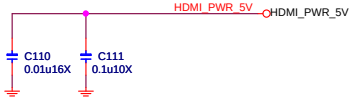


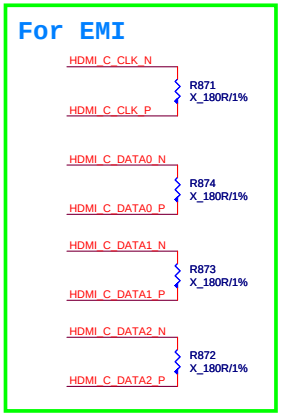


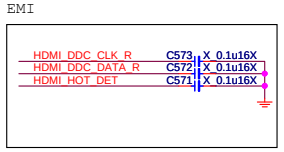












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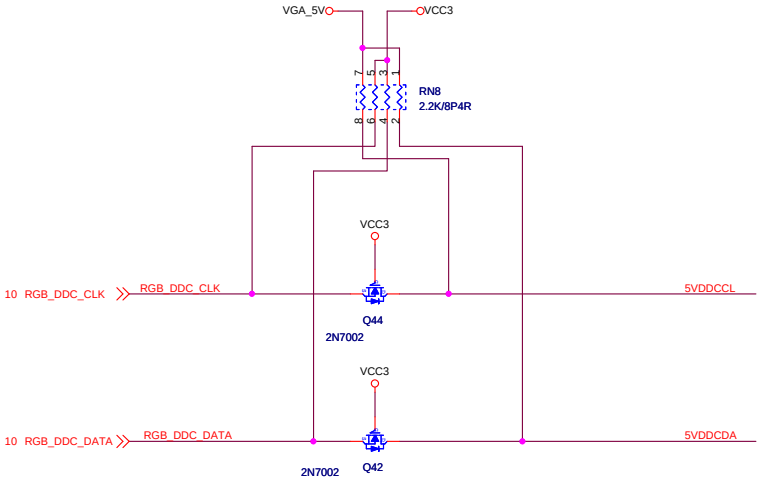
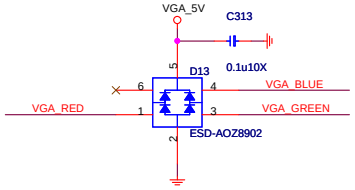
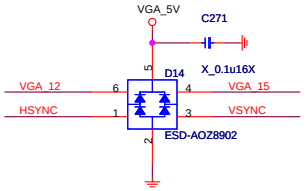
D-Sub

VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

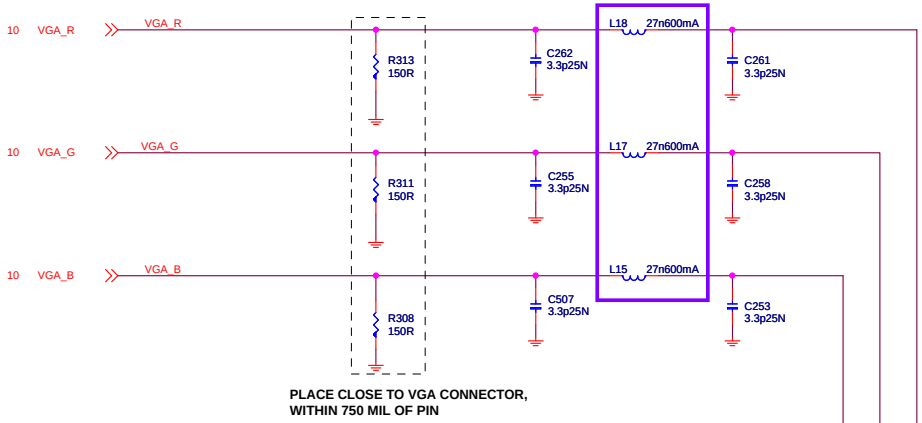
Level shift







Change to L, don't use FB
Try to pass VESA v1.2



PLACE CLOSE TO VGA CONNECTOR,
WITHIN 750 MIL OF PIN

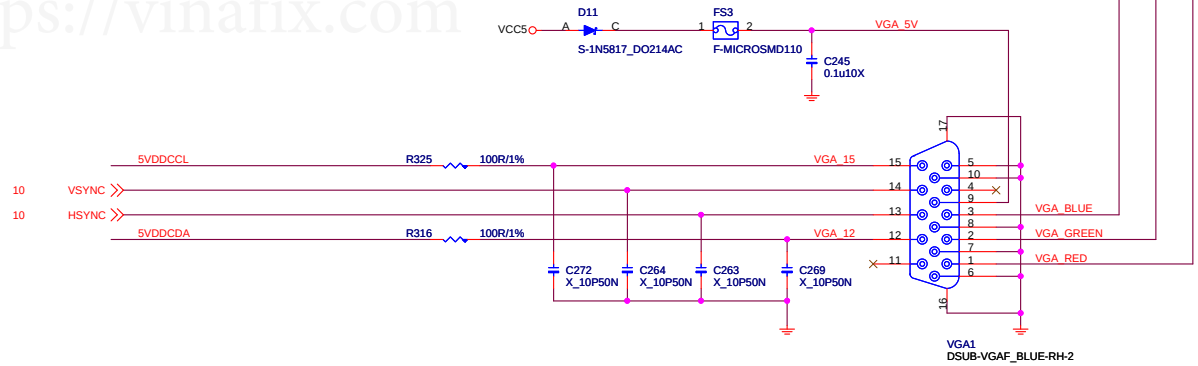


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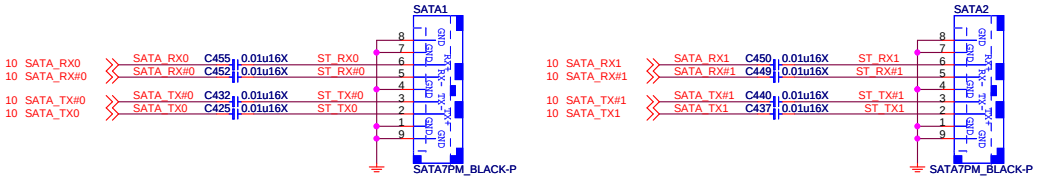
Table 1-3. Desktop Intel® 6 Series Chipset SKUs

Feature Set	SKU Name(s)					
	Q67	Q65	B65	H67	P67	H61
Total number of SATA ports	6	6	6	6	6	4
• SATA Ports (6 Gb/s, 3 Gb/s, and 1.5 Gb/s)	2[4]	1[5]	1[5]	2[4]	2[4]	0
• SATA Ports (3 Gb/s and 1.5 Gb/s only)	4	5	5	4	4	4[8]

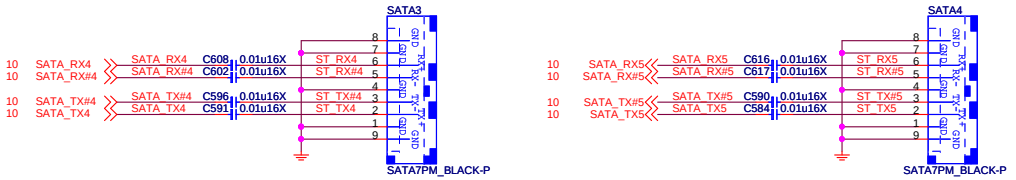
NOTES:

8. SATA ports 2 and 3 are disabled.

SATA 3G PORT 0,1



SATA 3G PORT 4,5



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MS-7788		
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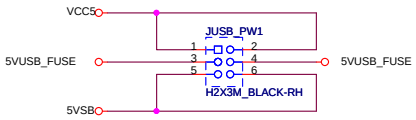
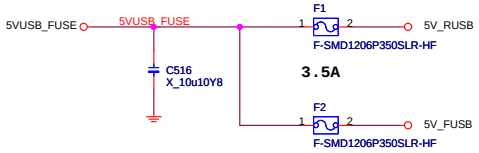
5V_RUSB Switch

5V_RUSB must 120mm





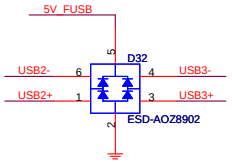
Default VCC5 (PIN1-3,2-4)

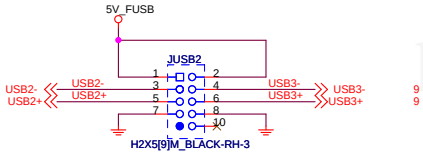
JUSB_PW1	BIOS Menu	Wake up support
1-3,2-4	EUP Enable	Not support
	EUP Disable	
3-5,4-6	EUP Enable	Not support
	EUP Disable	support

Front USB Connector

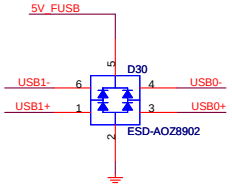
For H61 6,7,12,13 Port should be remove

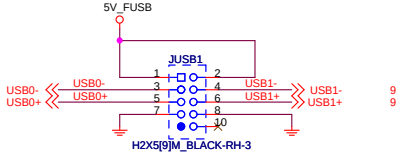
FRONT USB PORT 2,3

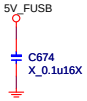


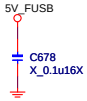


FRONT USB PORT 0,1



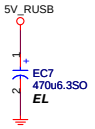


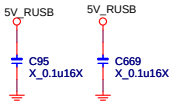




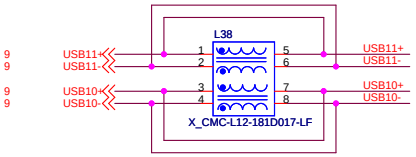
Rear USB Connector

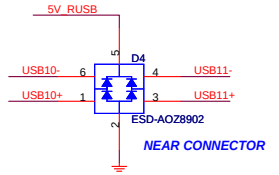
NEAR USB REAR CONNECTOR

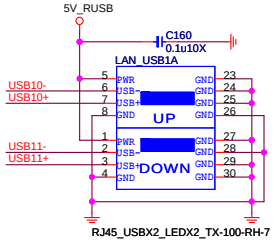




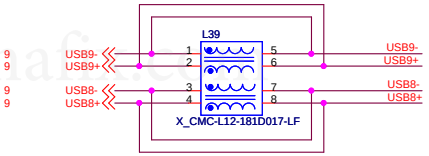
REAR USB PORT 10,11 (With LAN)

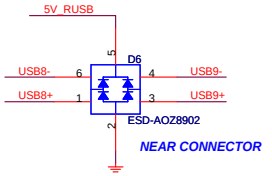


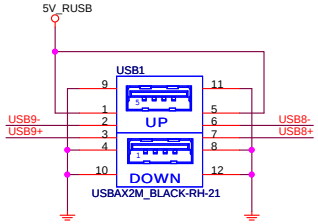




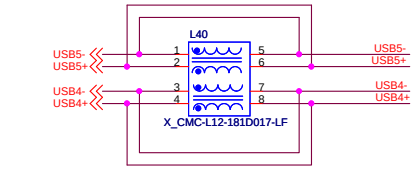
REAR USB PORT 8,9

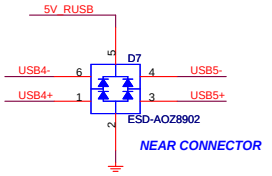


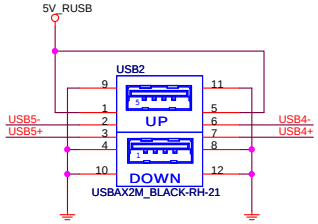




REAL USB PORT 4,5







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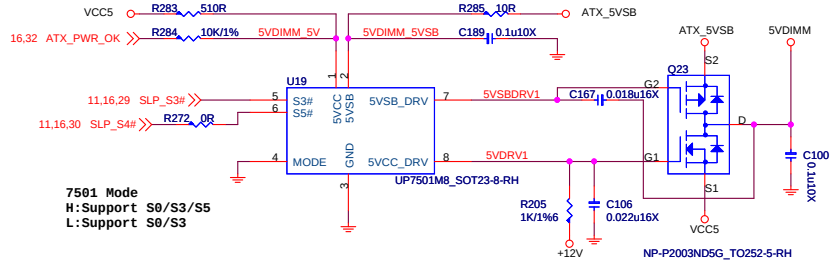
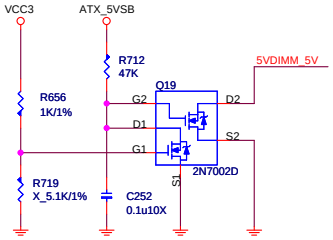
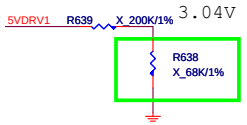
5VDIMM FOR DDR



7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

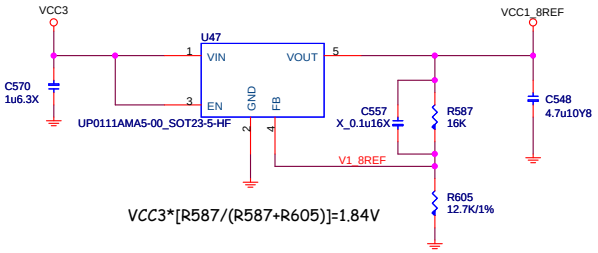


Patch coolermaster 700w power sequence

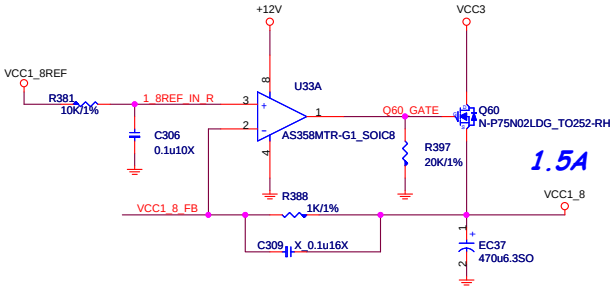


56K-->68K縮少料件

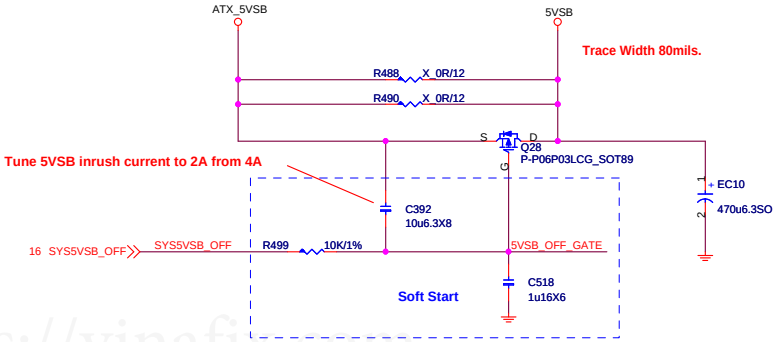
VCC1_8REF

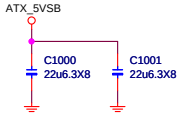


VCC3*[R587/(R587+R605)]=1.84V



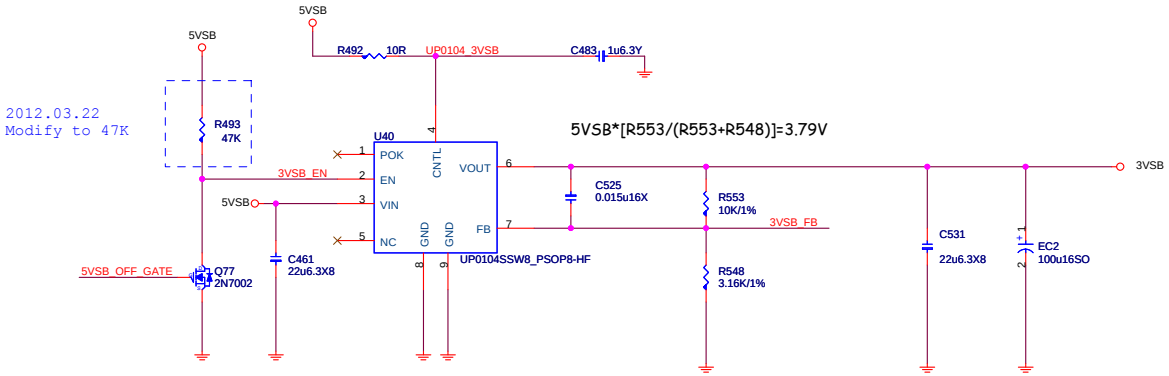
5VSB Power Switch





3VSB

3VSB supply to PCH and other device.
Turn off when Deep S3/S5 by 5VSB off.



5VSB*[R553/(R553+R548)]=3.79V

MICRO-STAR INT'L CO.,LTD			
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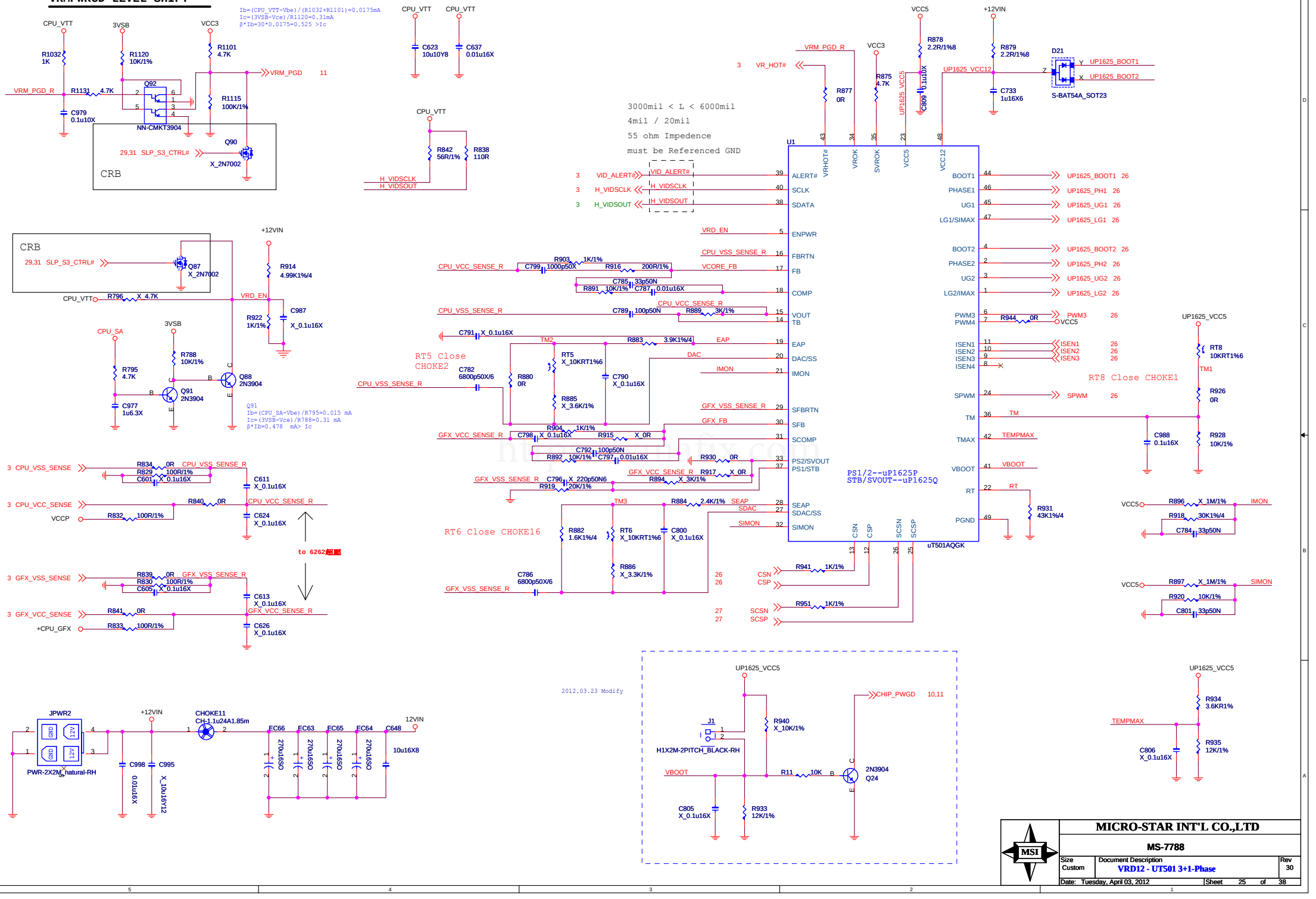
VRMPWRGD LEVEL SHIFT



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MS-7788	
Size: Custom	Document Description: VRD12 - UT501 3+1-Phase
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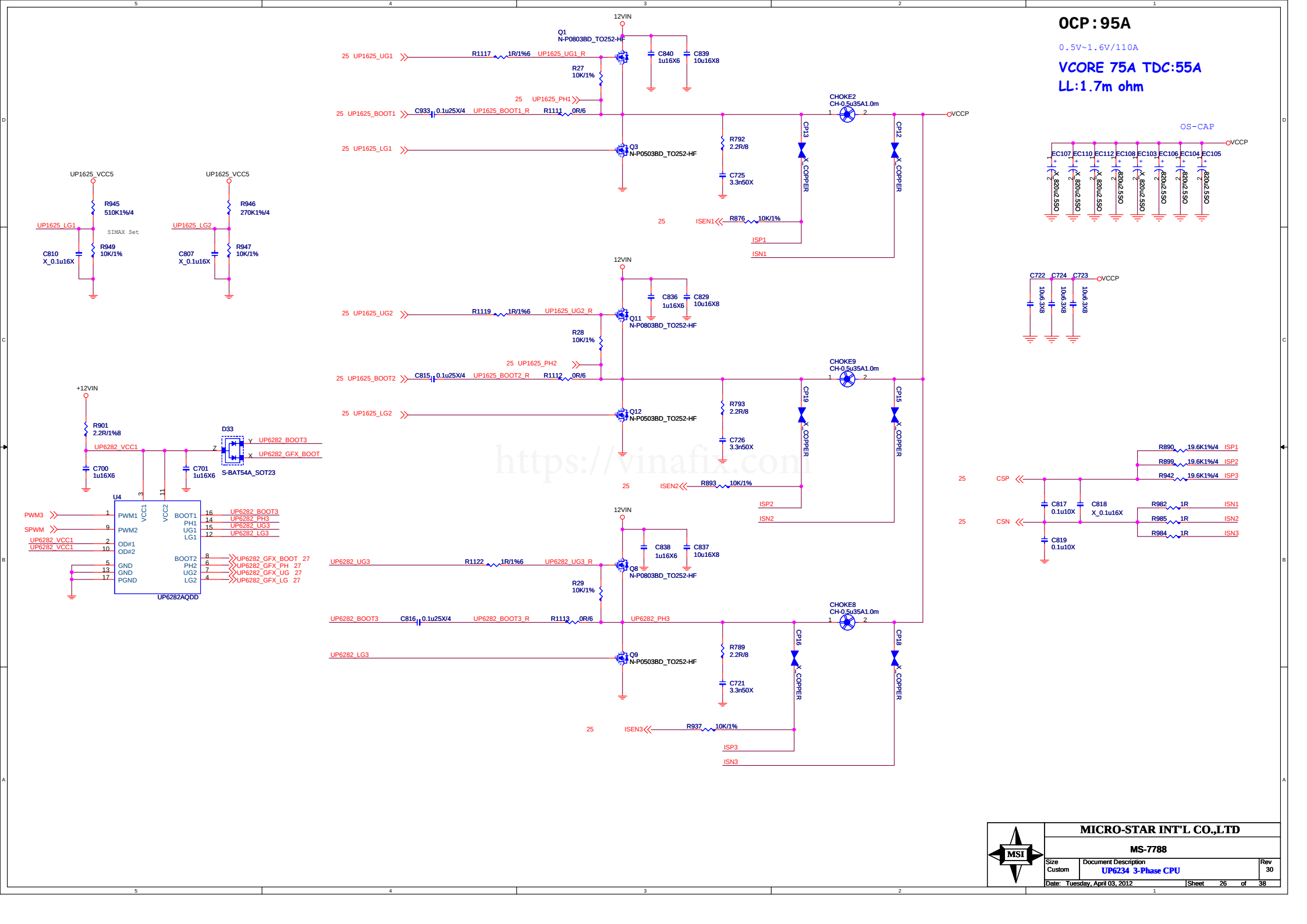
OCP : 95A
0.5V~1.6V/110A
VCORE 75A TDC:55A
LL:1.7m ohm
OS-CAP
12VIN
VCCP
UP1625_VCC5
+12VIN
Q1
N-P0803BD_TO252-HF
Q3
N-P0503BD_TO252-HF
Q11
N-P0803BD_TO252-HF
Q12
N-P0503BD_TO252-HF
Q8
N-P0803BD_TO252-HF
Q9
N-P0503BD_TO252-HF
CHOKE2
CH-0.5u35A1.0m
CHOKE9
CH-0.5u35A1.0m
CHOKE8
CH-0.5u35A1.0m
D33
S-BAT54A_SOT23
U4
UP6282AQDD
SIMAX Set
X_COPPER
https://vinafix.com
MICRO-STAR INT'L CO.,LTD
MS-7788
Size
Custom
Document Description
UP6234 3-Phase CPU
Rev
30
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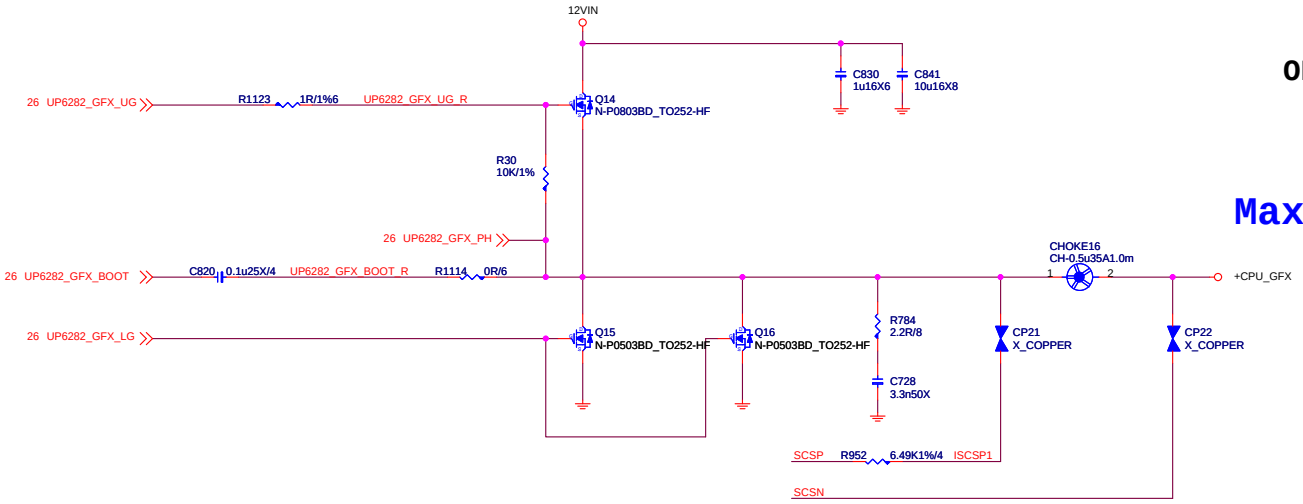
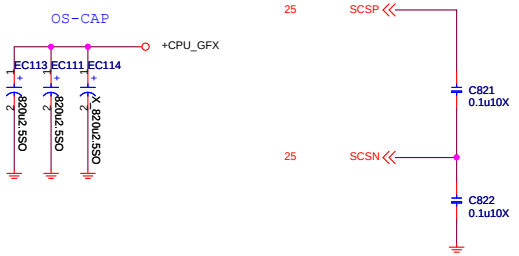


OPC:50A

Max:35A



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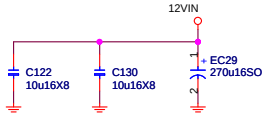
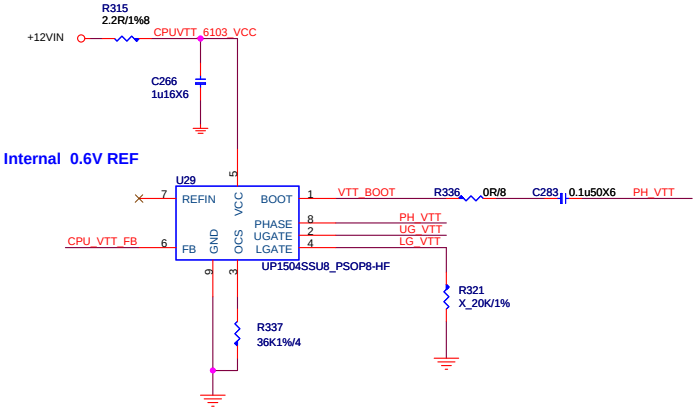
CPU_VTT:1.05/1.00

CPU VTT 8.5A + SA Core =8.8A =17.3A

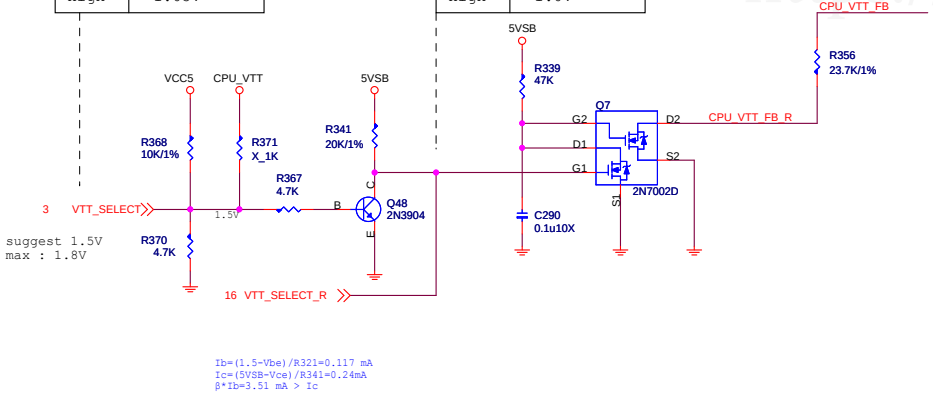
Iripple=1.92(vtt)+1.88(sa)
5*1=5A>3.8A

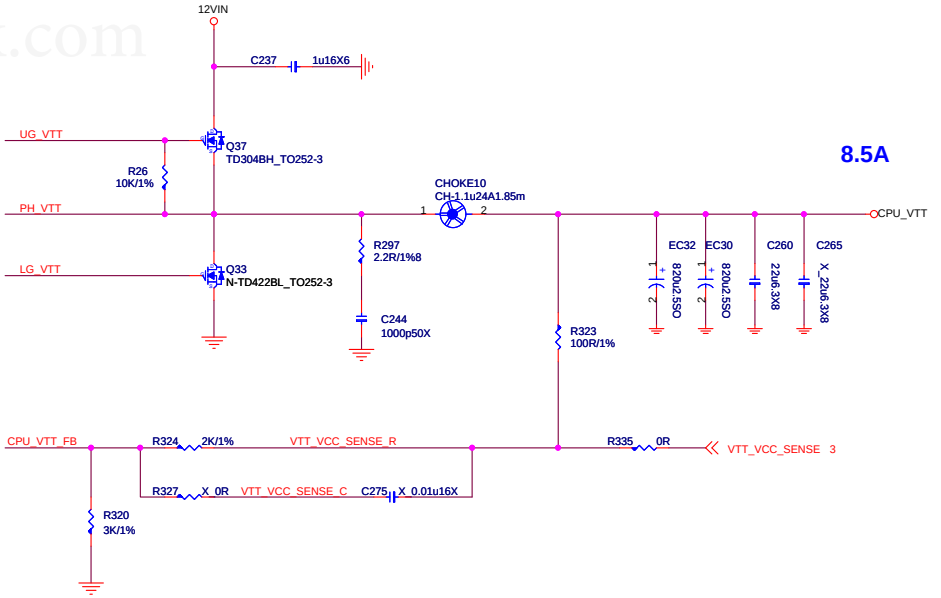




VTT_SELECT	
Low	1.0V
High	1.05V

VTT_SELECT Table	
Low	1.05V
High	1.0V





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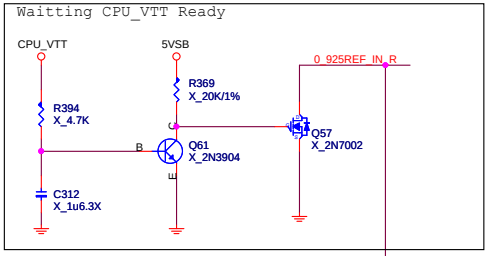
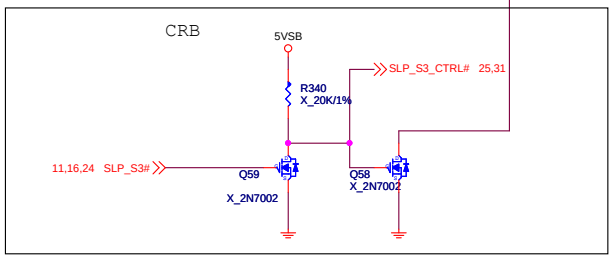
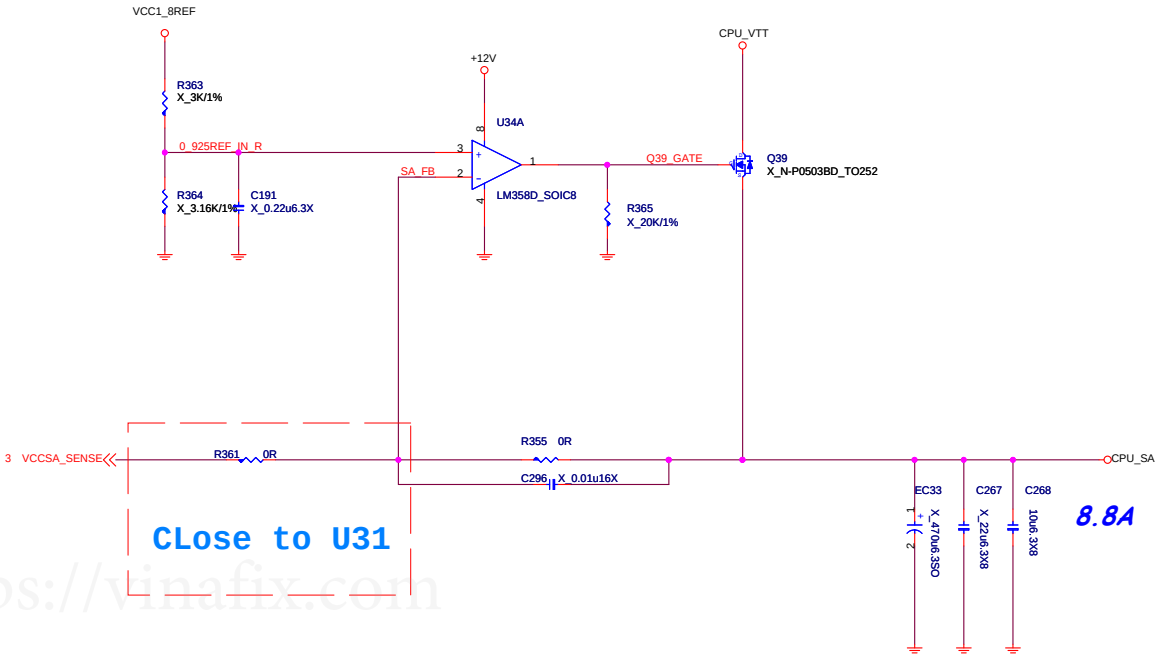
CPU_SA:0.925/0.85

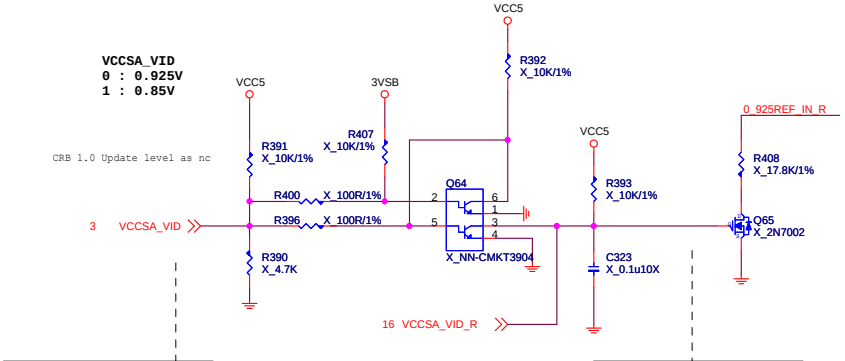
SA Core =8.8A



Ib=(CPU_VTT-Vbe)/R394 =0.021 mA
Ic=(5VSB-Vce)/R369=0.24 mA
β*Ib=0.638 mA > Ic



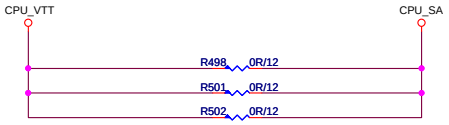




VCCSA_VID	
Low	0.925V
High	0.85V

Ib=(Vvccsa_vid-Vbe)/R396=1 mA
Ic=(VCC5-Vce)/R393= 0.48 mA
β*Ib =30 mA > Ic

VCCSA_VID_SIO Table	
Low	0.925V
High	0.85V



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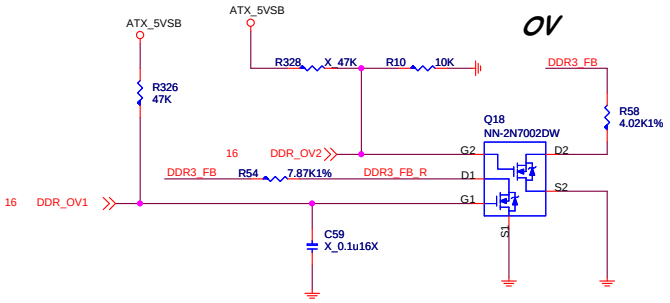
DDR3_1.5V 4.5A+7.5A+1A=13A

4.5A FOR CPU
7.5A FOR 2DIMM
1A FOR DDR VTT

2012.03.22 Modify Pull hi (47K)to ATX_5VSB

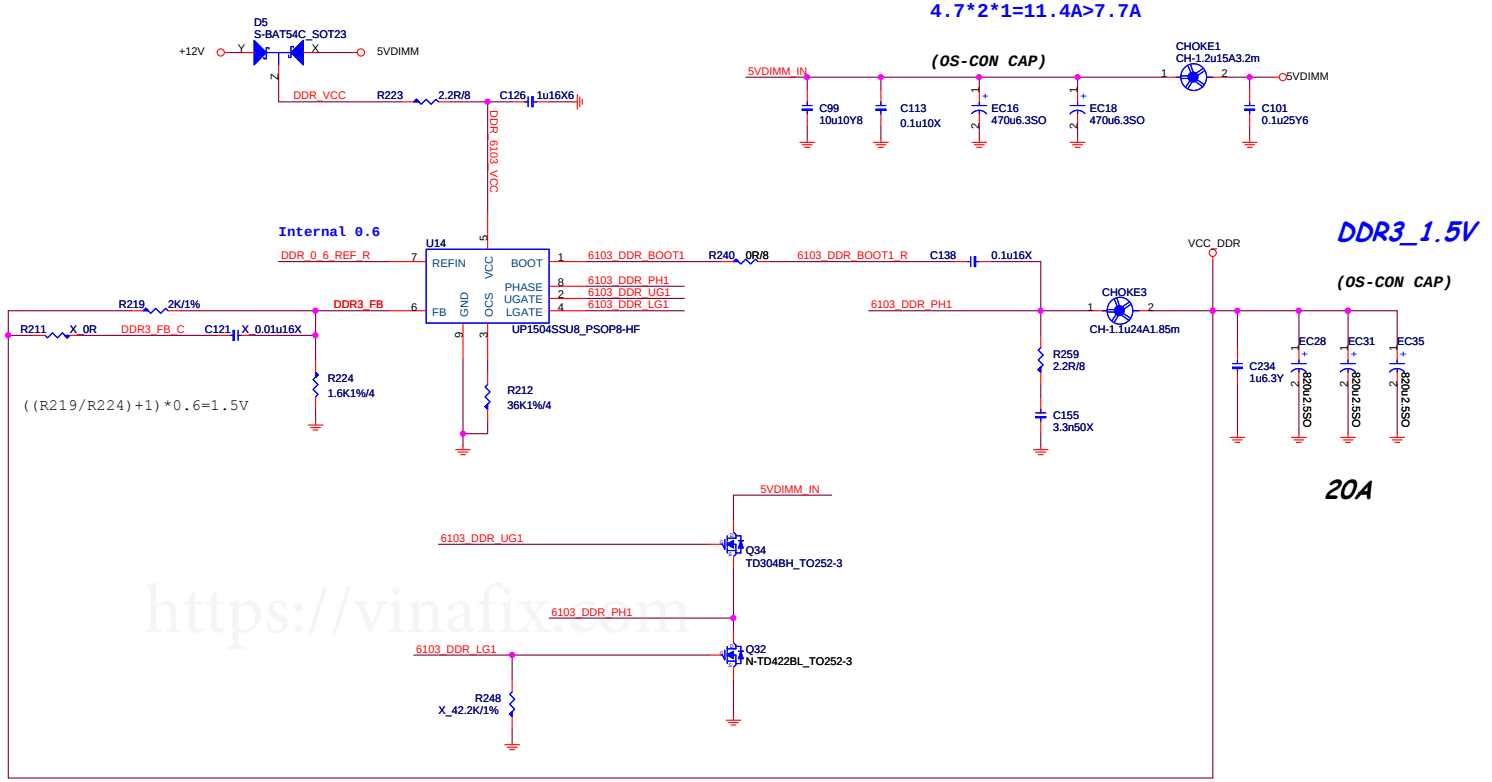


OV

*Default 1.5V

DDR_OV	1.35V	1.5V	1.65V	1.8V
DDR_OV1	Low	High	Low	High
DDR_OV2	Low	Low	High	High

DDR_OV1 = GPIO01(S/IO)
DDR_OV2 = GPIO02(S/IO)



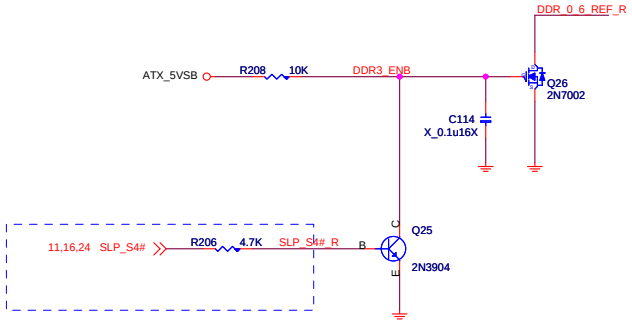
Iripple=7.7A
4.7*2*1=11.4A>7.7A

DDR3_1.5V

(OS-CON CAP)

20A

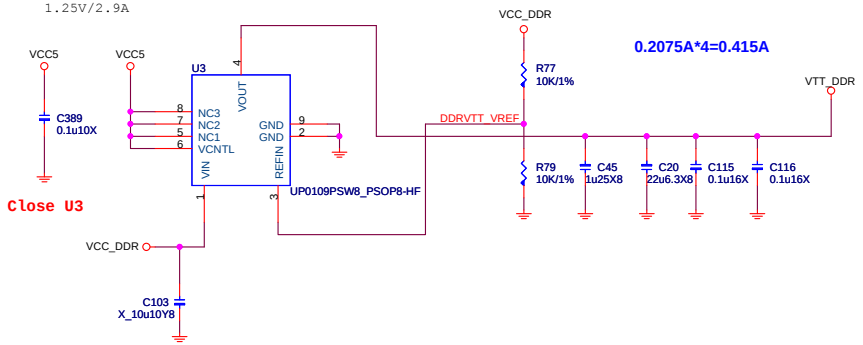
P.S. Only for meet Intel power down sequence.



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

1.25V/2.9A



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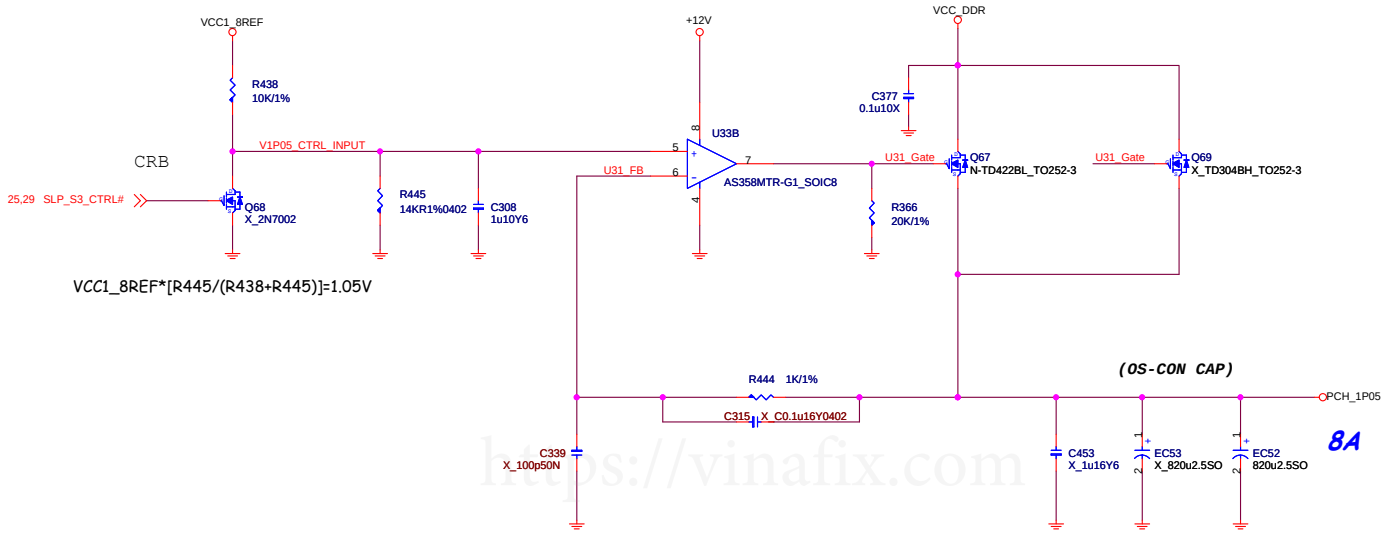
PCH Power:1.05V



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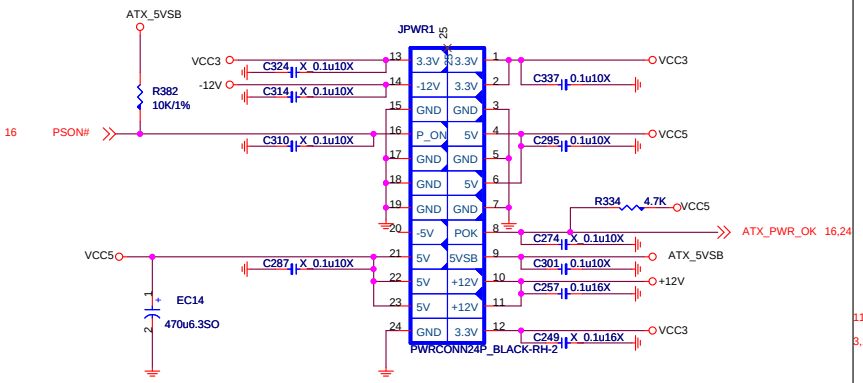
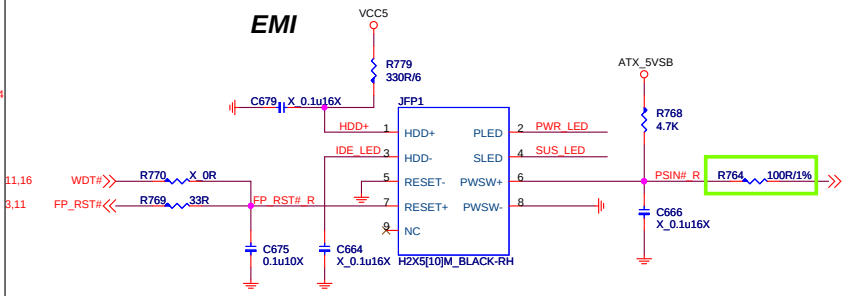
ATX POWER CONNECTOR

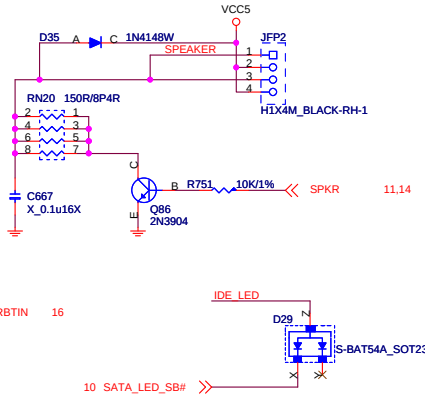


FRONT PANNEL

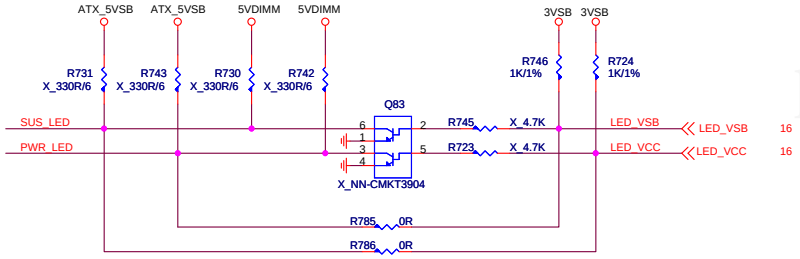
EMI



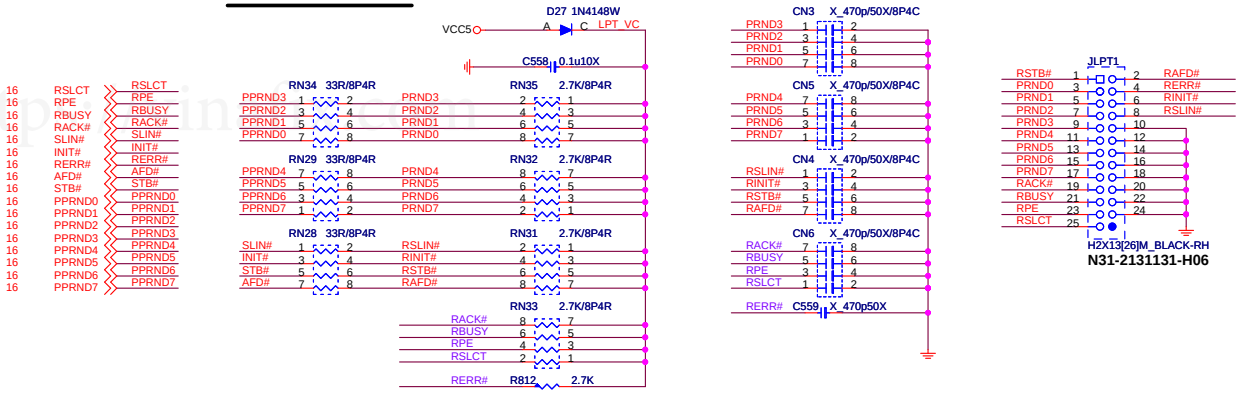
Speaker Pin Header



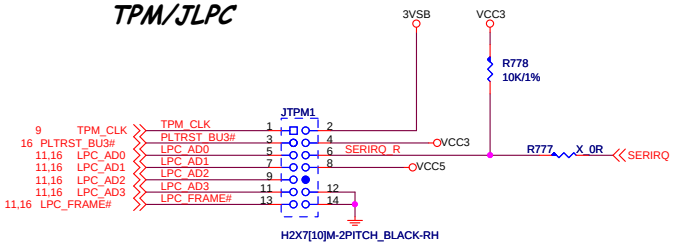
LED (for Fintek 71868)



PARALLAL PORT



TPM/JLPC



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Custom	ATX PWR-Connector & Front Panel & EMI	30

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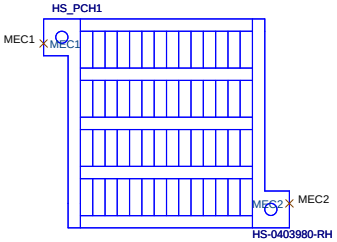
MS-7788-30

OPT	Configure	BOM	Function
			MS-7788 30 H61M-E33(G3) H61 B3+2*DDRIII+1*PCI-Ex16,1*PCI-Ex1+D- sub/HDMI+ 4*SATAII+10*USB2+H/D 8Ch Audio+Gb LAN,Lan,All Solid Cap,EuP,RoHS

PCH XDP PWRGD/RESET

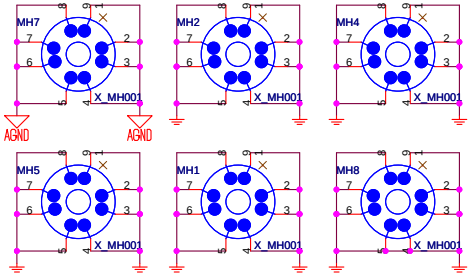
HS_PCH1



HS-0403980-RH

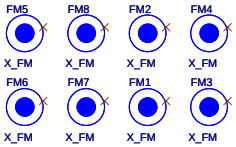
Simulation

Mounting Holes



HDMI_RLA1
Real Label
HDMI
HDMI_RLA
HDMI Label P/N

Optical Fiducial Marks-120



LA1
Label
601-7788-01S
LABEL

LA3
Label
601-7788-02S
LABEL

LA2
AMI_BIOS LABLE
BIOS_LABEL

HDMI_LA1
Label
HDMI
HDMI LABEL

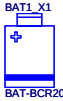
Virtual MSI P/N

PCB1

7788-30

PK0-0778830-G37,精成,17,寶安恩斯邁廠(MSIS),4,Coffee
PK0-0778830-E48,競華,17,寶安恩斯邁廠(MSIS),4,Coffee
PK0-0778830-E55,依頓,16,寶安恩斯邁廠(MSIS),4,Coffee

BAT1_X1



BAT-BCR2032P-RH

RUB1
USB
X_Rubber

RUB2
USB
X_Rubber

CPU_H1
CPU
鐵座
E21-7557050-L06

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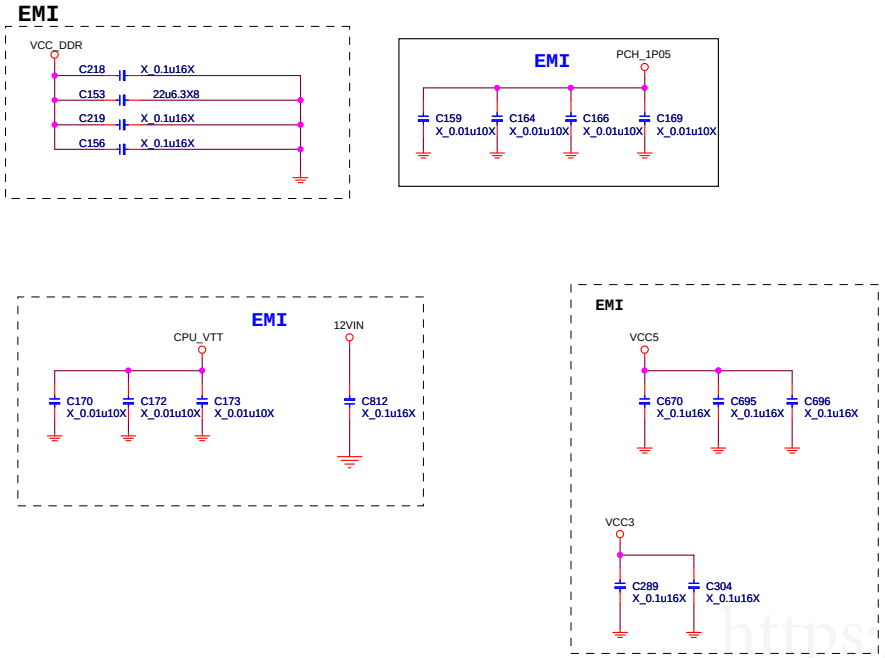

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