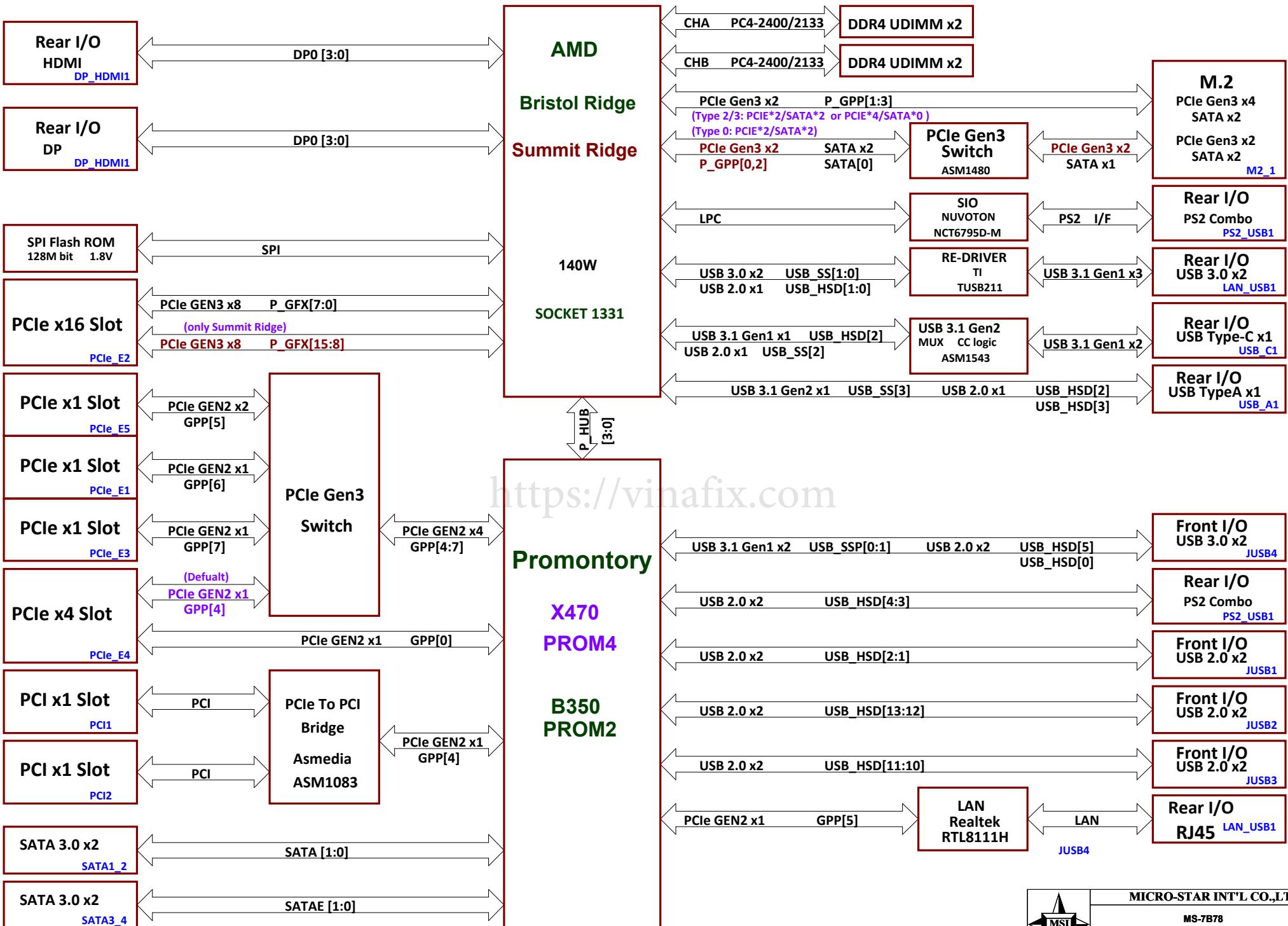
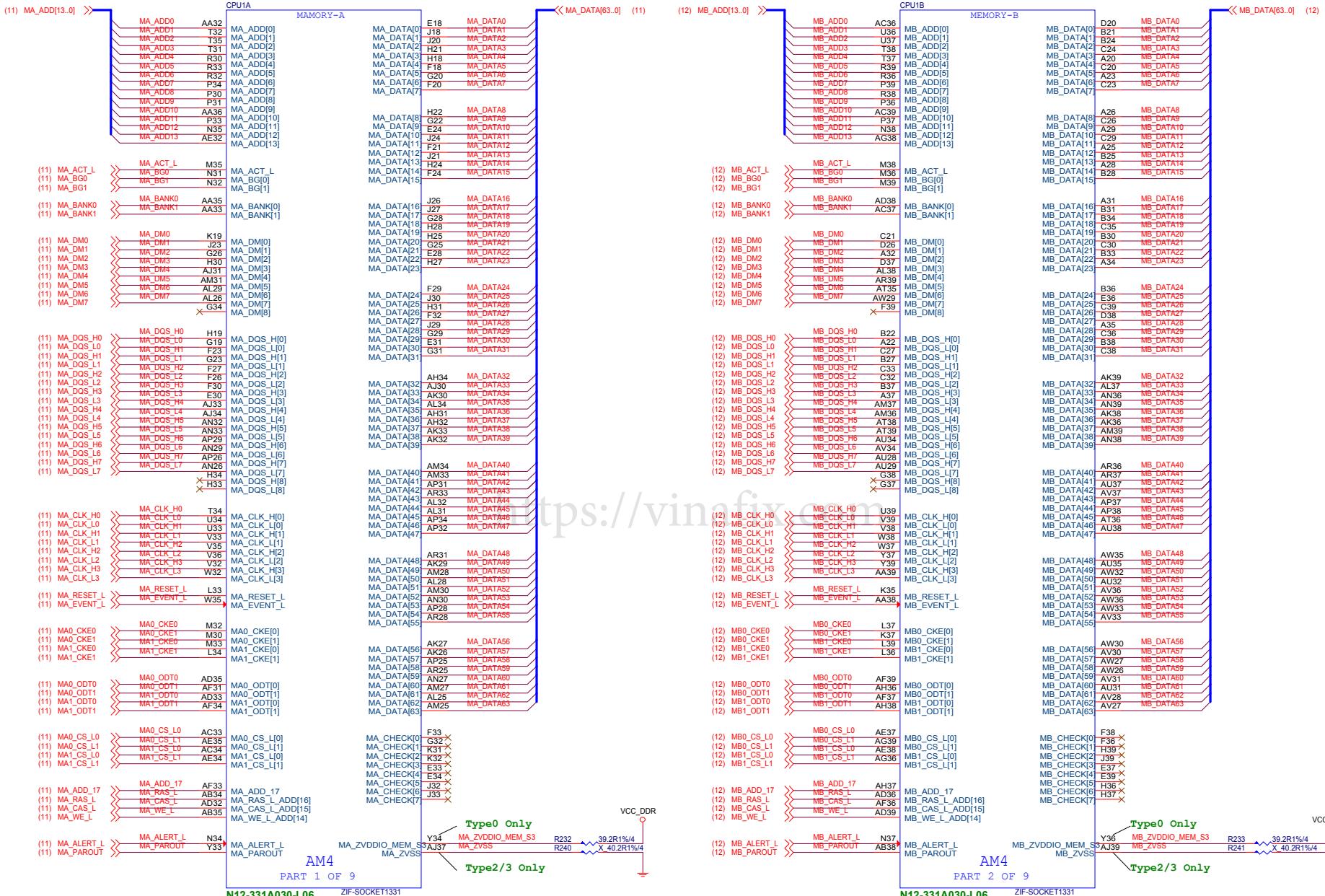
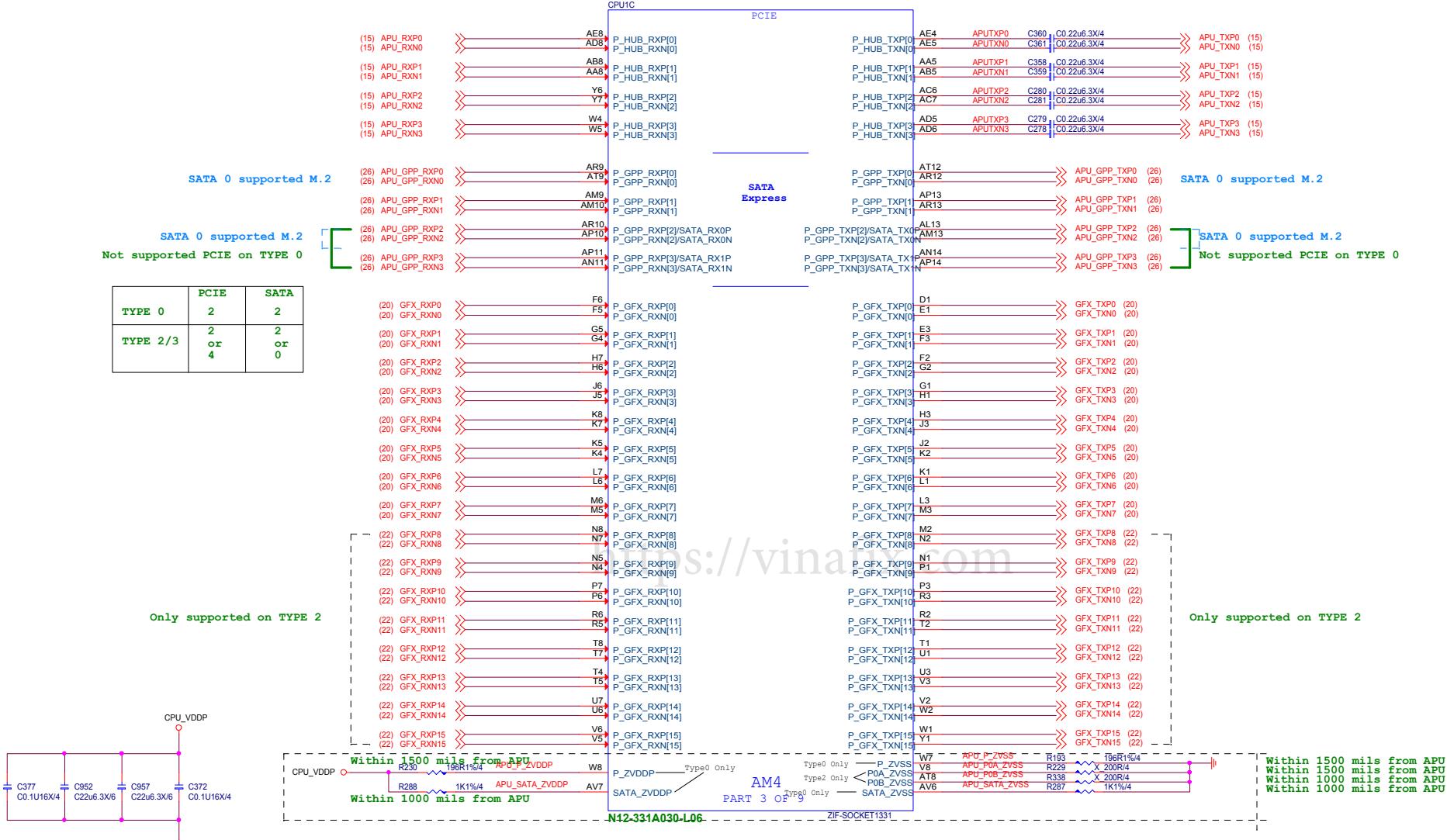


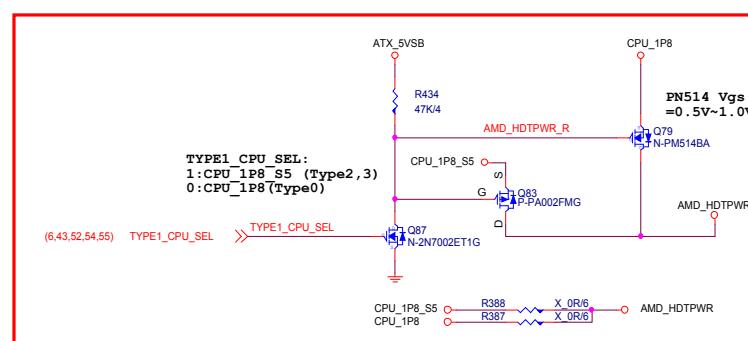
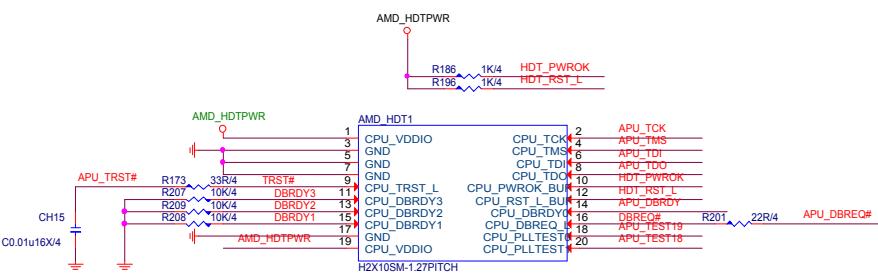
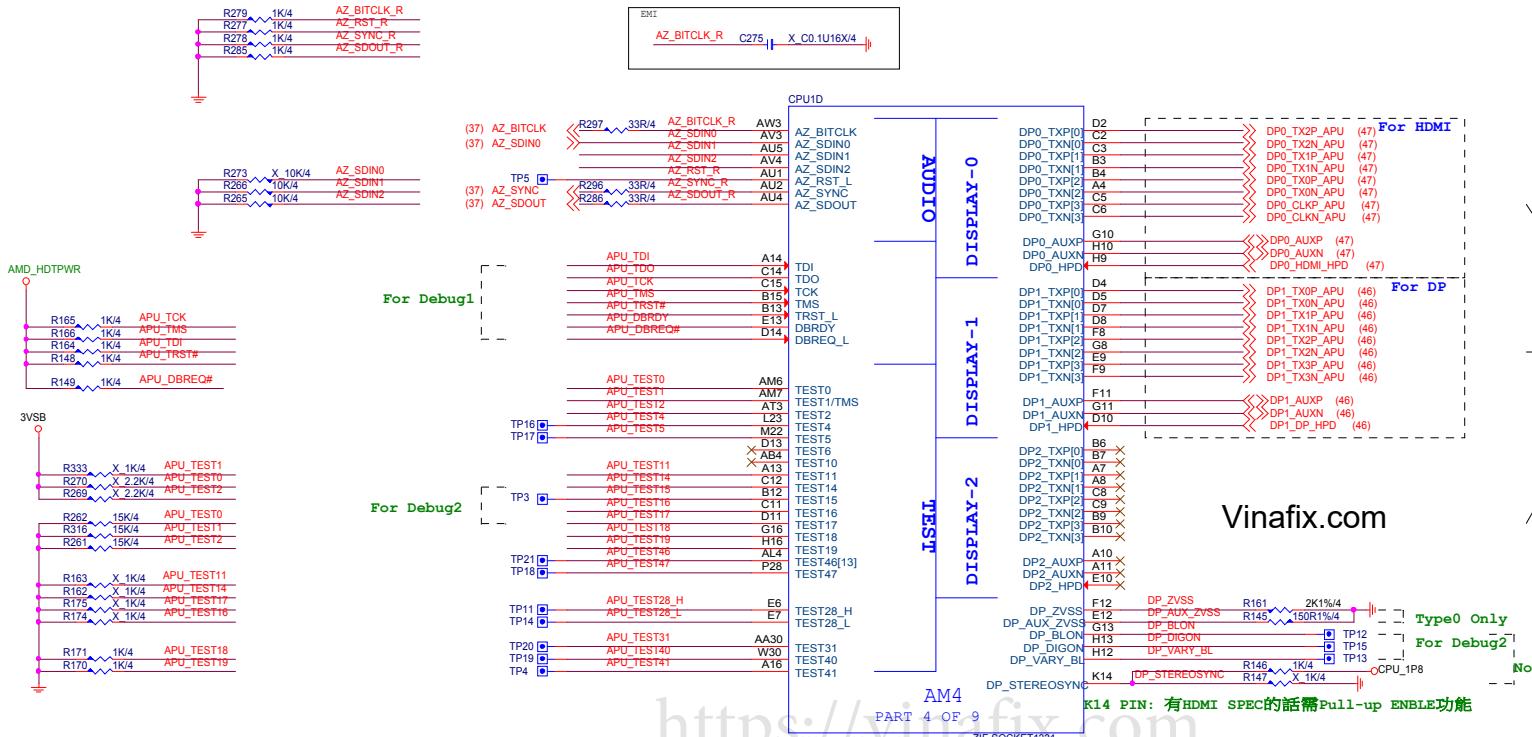
AMD AM4

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05	AM4 Display / Audio	40	Front USB2.0 Header	70	LED - Mystic Light - 2
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23	PCI_E1_E3_E5 (X1)	53	CPU power 1.8_S0 / S5		
24	PCI_E6 (X4)	54	CPU power VDDP - TPS56C215		
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27	M.2_2	57	DDR Power - VPP25 / VTT		
28	M.2_3 (WIFI+BT)	58	PROM - SY8288RAC / 1.05V		
29	SIO NCT6797D-M	59	PROM - GS7133 / 2.5V		
30	SIO HW Monitor / NCT7718W	60	OV Control - NCT3933		
31	FAN TYPE-J CPUFAN1	61	OV 12VIN - RT9553B		
32	FAN TYPE-J PUMPFAN1	62	ACPI - 3VSB / 5VDIMM		
33	FAN TYPE-K SYSFAN1/2	63	ATX Power - FrptnPanel / EMI		
34	FAN TYPE-K SYSFAN3/4	64	LED - EZDEBUG / AMP		
35	FAN GPIO NCT5605	65	LED - DIMM / PCIE SLOT		









$$\begin{aligned} IB &= (\text{AMD_HDTPWR-Vbe}) / 4.7k \\ &= (1.8 - 0.95) / 4.7k = 0.181mA \end{aligned}$$

$$\begin{aligned} IC &= (Vc - Vce) / 10k \\ &= (1.8 - 0.2) / 10k = 0.16mA \end{aligned}$$

$$B * Ib > Ic = 10 * 0.181 = 1.81 > 0.16$$

$$\begin{aligned} IB &= (Vb - Vbe) / 10k \\ &= (1.75 - 0.95) / 10k = 0.08mA \end{aligned}$$

$$B * Ib > Ic = 10 * 0.08 = 0.8 > 0.16$$

$$\begin{aligned} IC &= (Vc - Vce) / 10k \\ &= (3.3 - 0.2) / 10k = 0.16mA \end{aligned}$$

$$B * Ib > Ic = 10 * 0.16 = 1.6 > 0.16$$

$$\begin{aligned} IB &= (\text{AMD_HDTPWR-Vbe}) / 4.7k \\ &= (1.8 - 0.95) / 4.7k = 0.181mA \end{aligned}$$

$$\begin{aligned} IC &= (Vc - Vce) / 10k \\ &= (1.8 - 0.2) / 10k = 0.16mA \end{aligned}$$

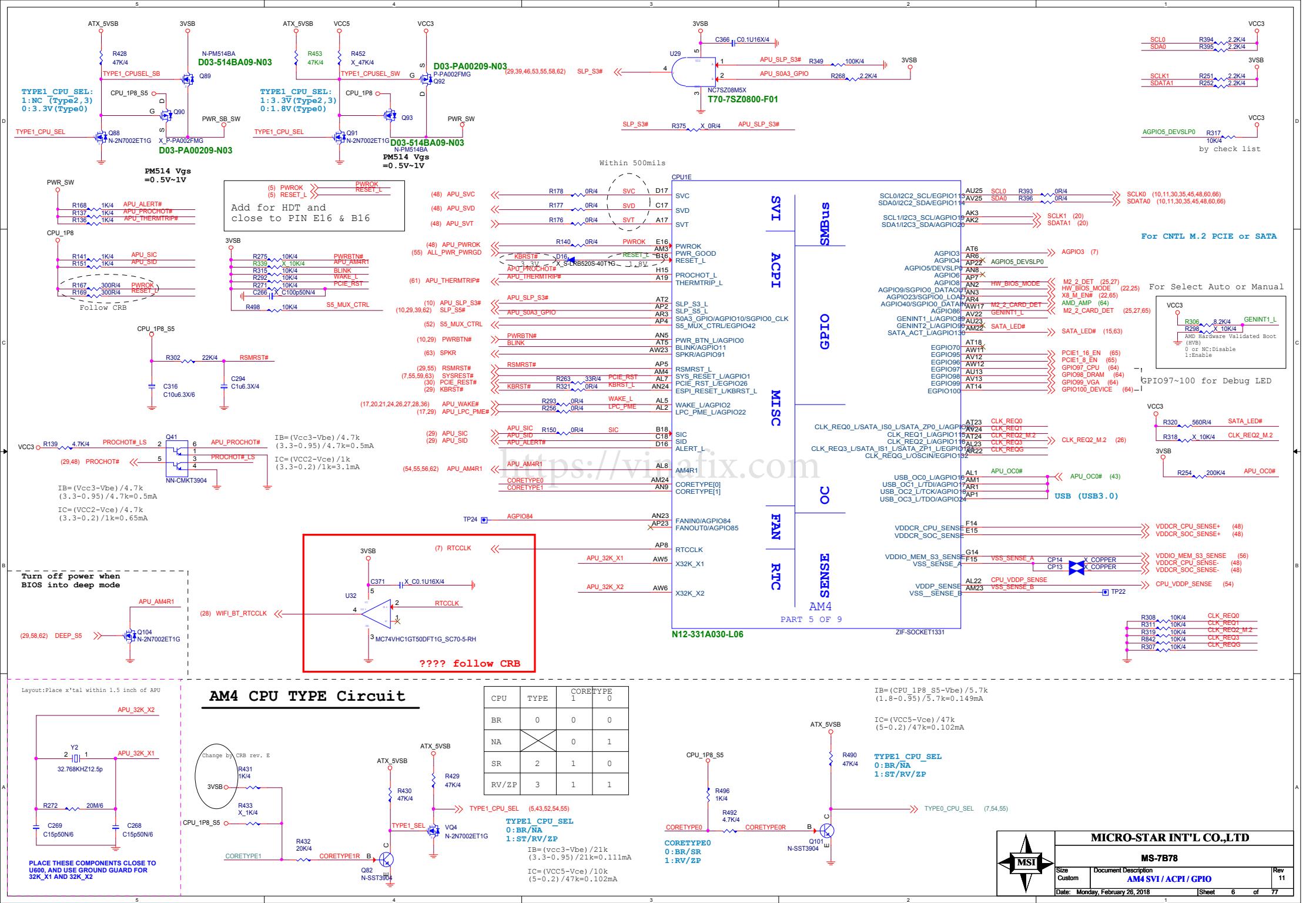
$$B * Ib > Ic = 10 * 0.181 = 1.81 > 0.16$$

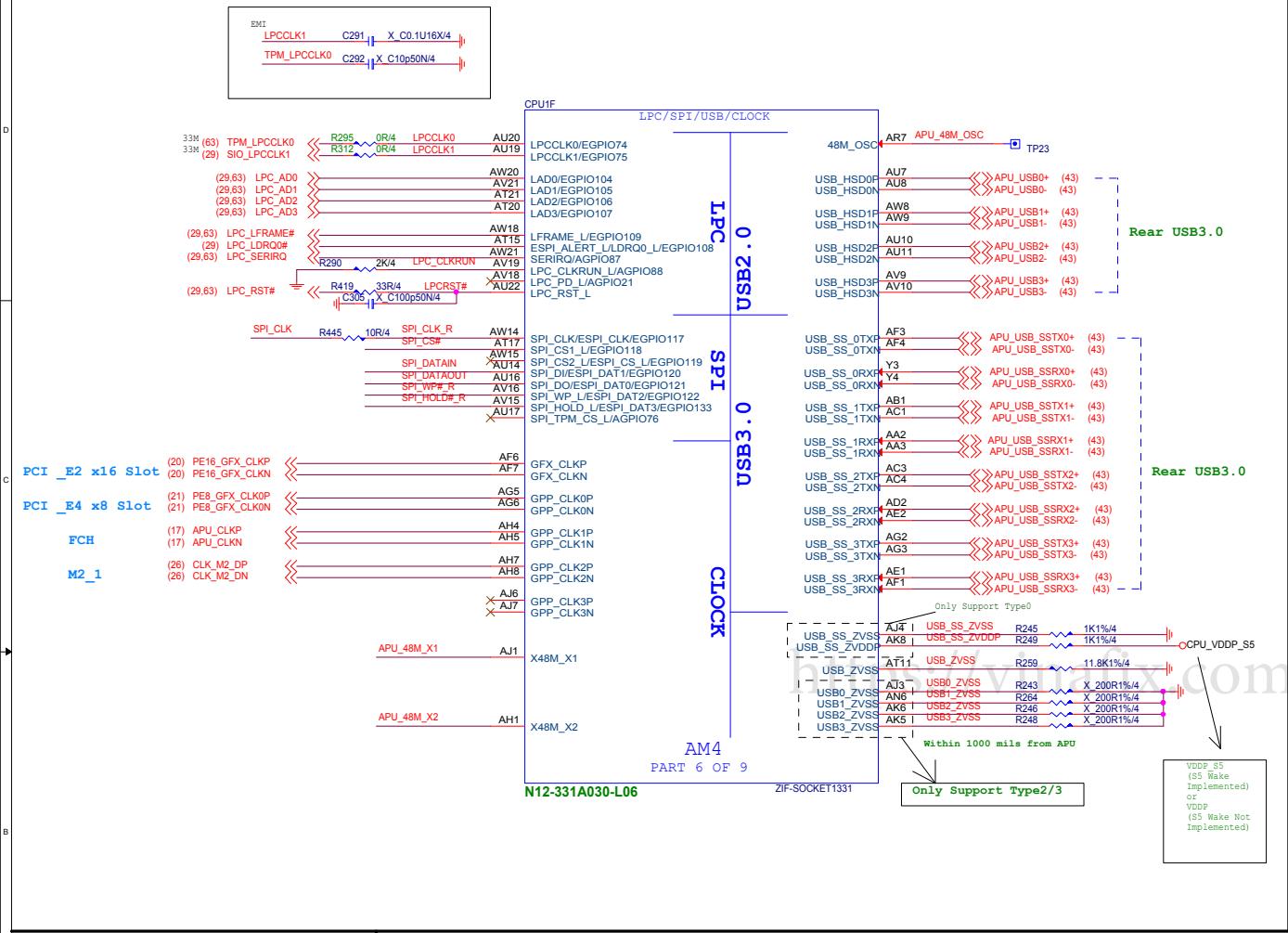
$$\begin{aligned} IB &= (Vb - Vbe) / 10k \\ &= (1.75 - 0.95) / 10k = 0.08mA \end{aligned}$$

$$B * Ib > Ic = 10 * 0.08 = 0.8 > 0.16$$

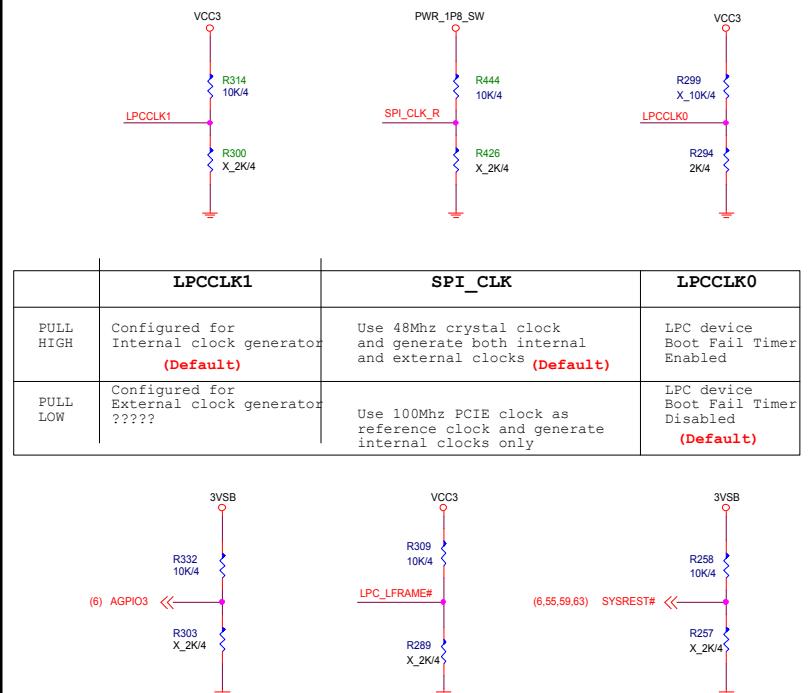
$$\begin{aligned} IC &= (Vc - Vce) / 10k \\ &= (3.3 - 0.2) / 10k = 0.16mA \end{aligned}$$

$$B * Ib > Ic = 10 * 0.16 = 1.6 > 0.16$$



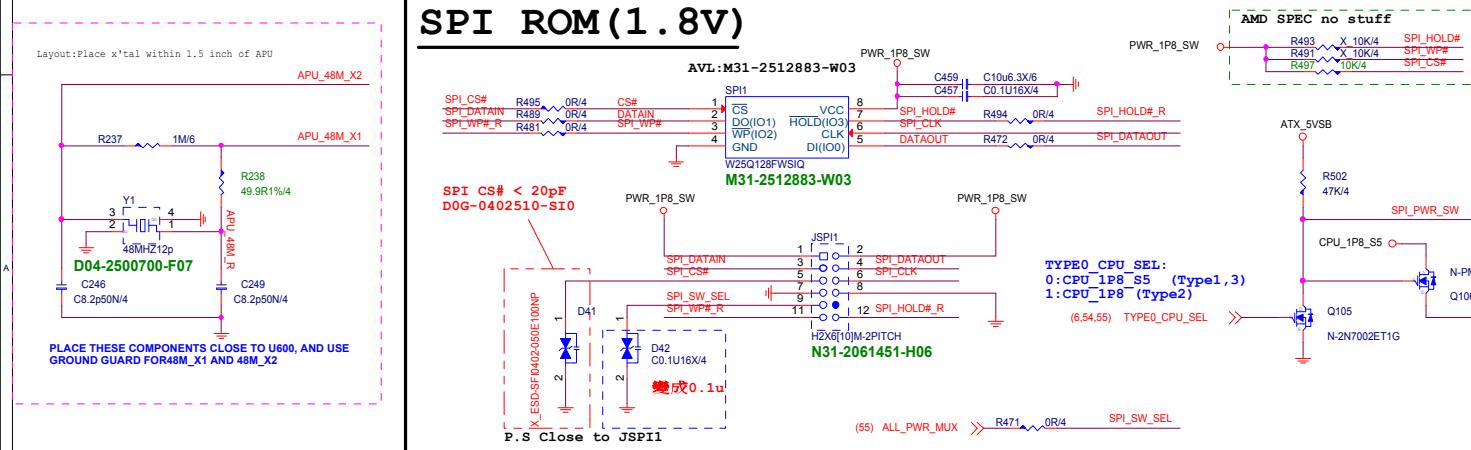


Strapping Options



	AGPIO3	SIO_LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

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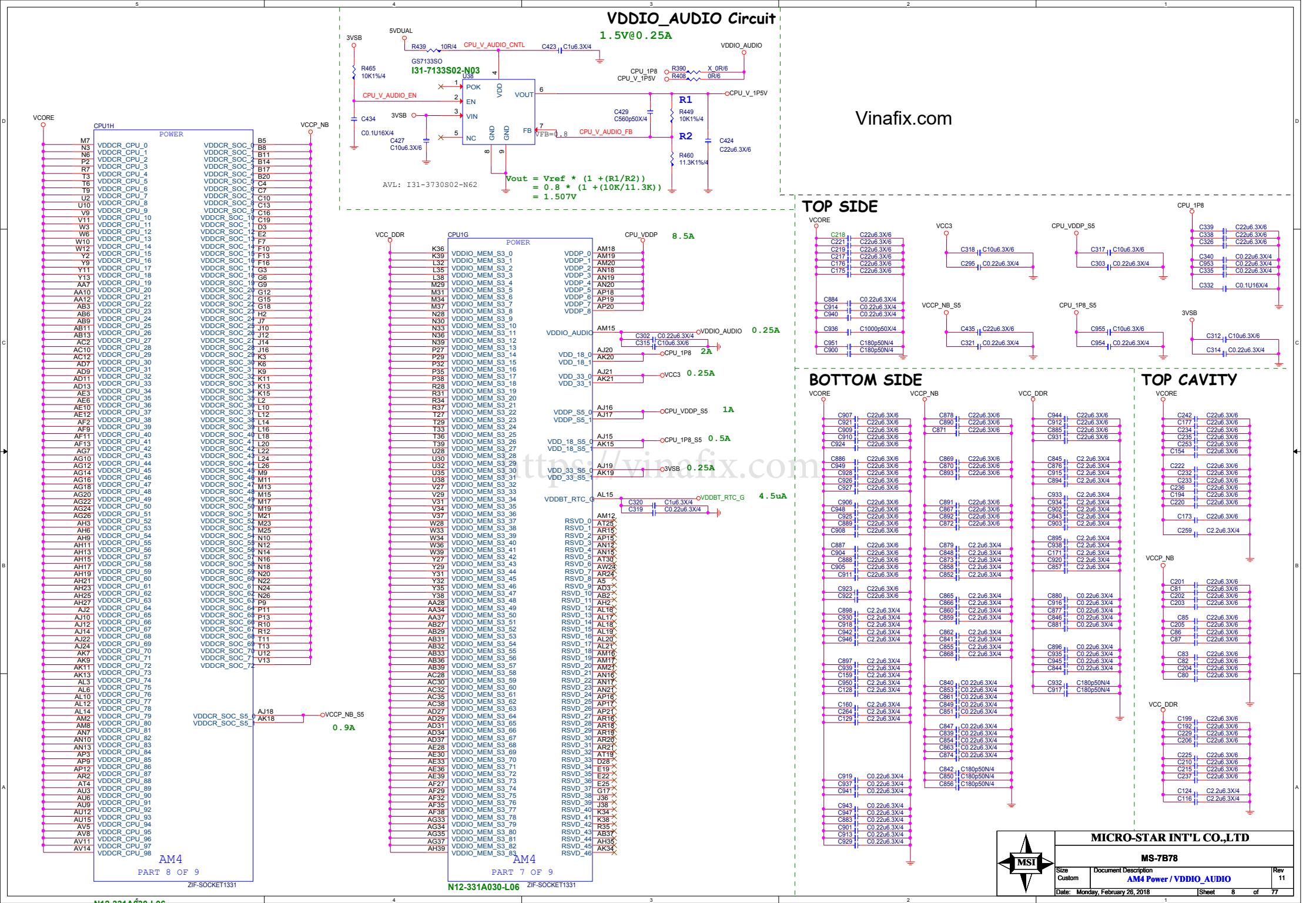
RTCCLK	
PULL HIGH	RTC Coin Battery is on board (Default)
PULL LOW	RTC Coin Battery is not on board

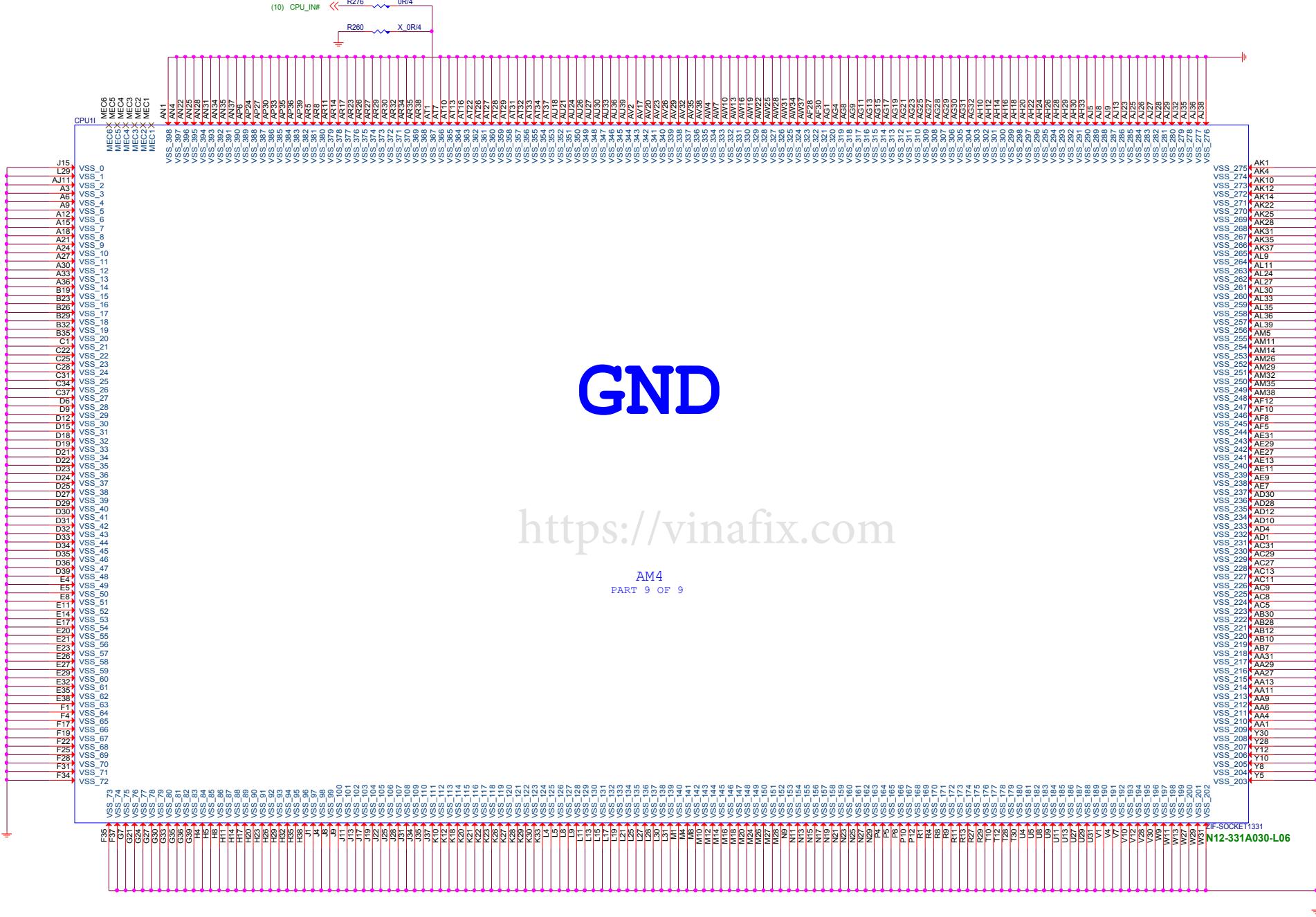


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AM4
PART 9 OF 9

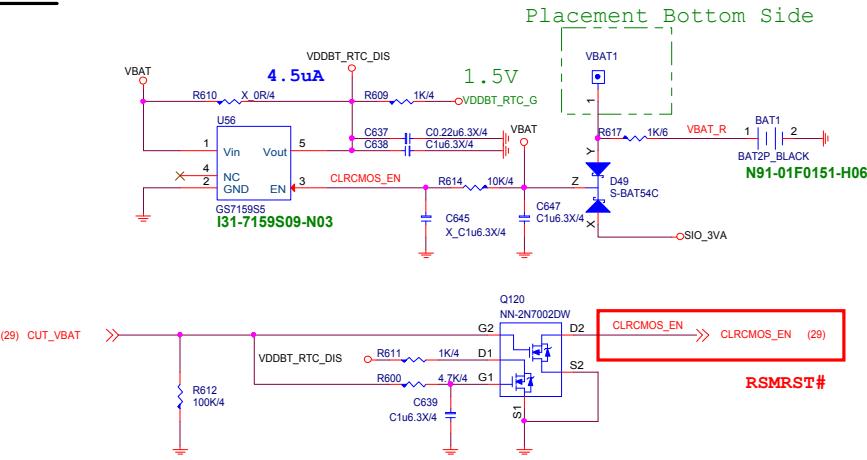


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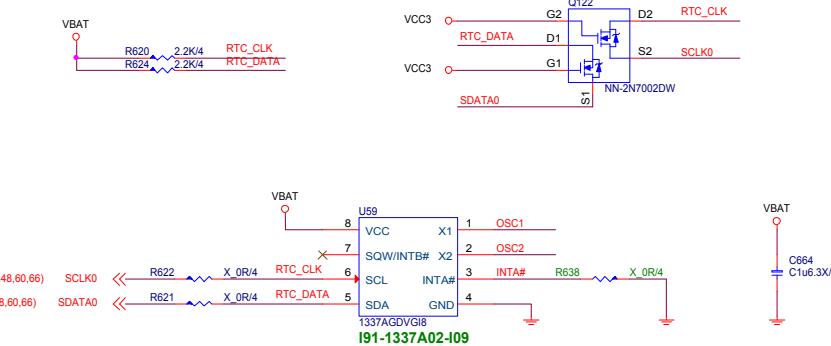
MS-7B'

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RTC & Clear CMOS Circuit



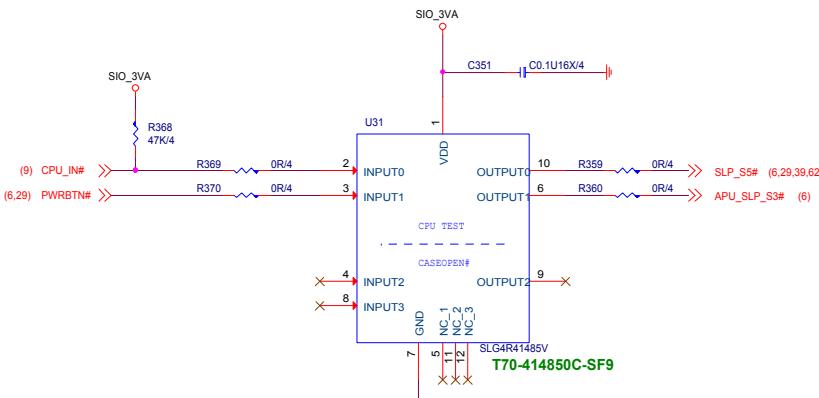
RTC Backup



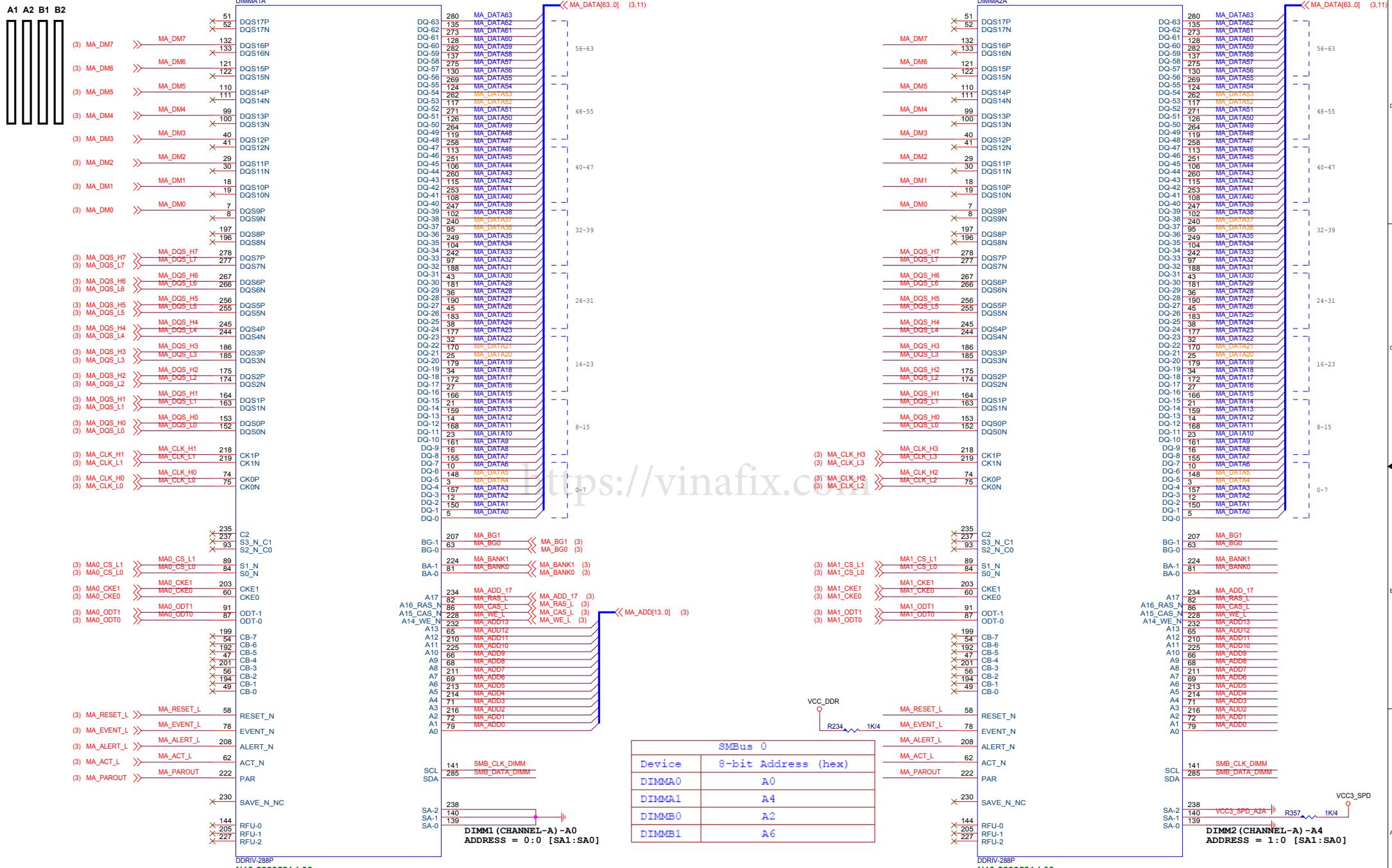
Clear CMOS button



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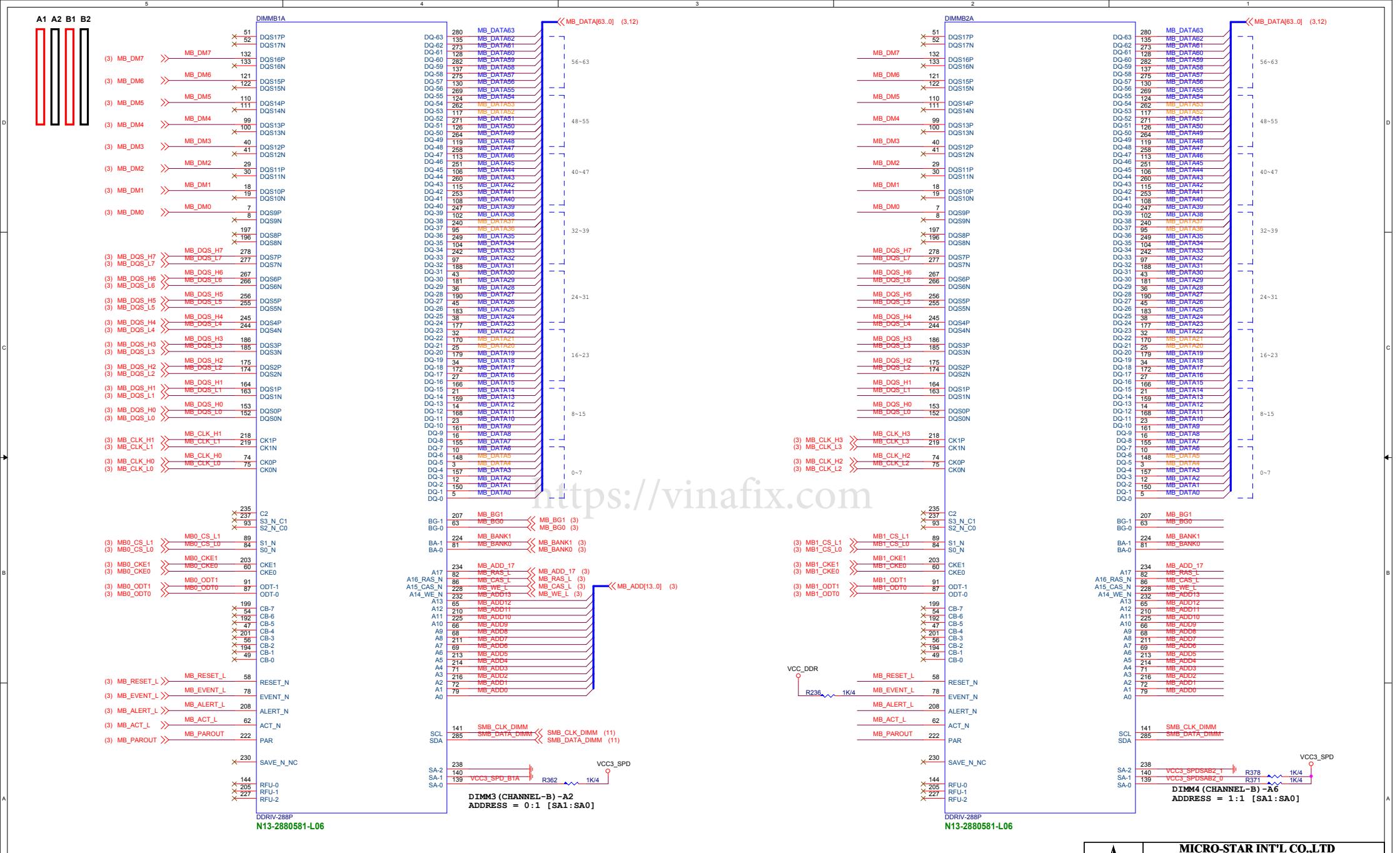


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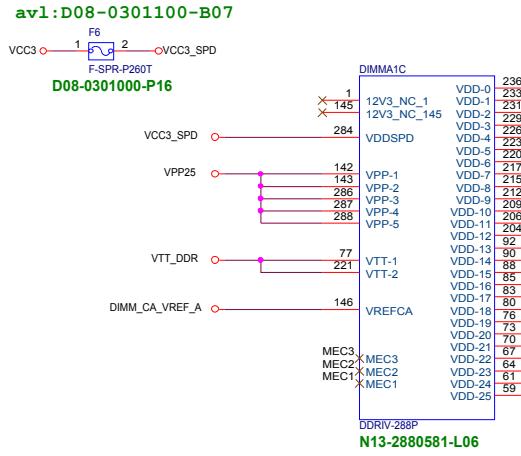


Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

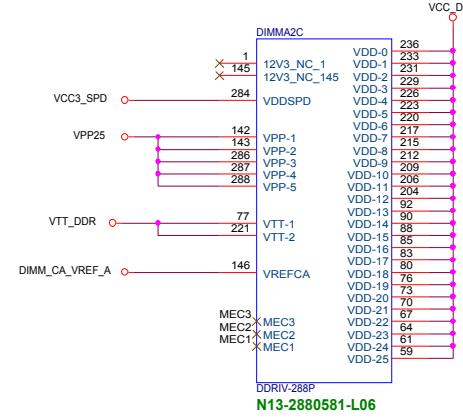
(6,10,30,35,45,48,60,66) SCLK0 R407 0R/4 SMB_CLK_DIMM
(6,10,30,35,45,48,60,66) SDATA0 R399 0R/4 SMB_DATA_DIMM (12) SMB_CLK_DIMM (12)
(6,10,30,35,45,48,60,66) SCLK0 R407 0R/4 SMB_CLK_DIMM
(6,10,30,35,45,48,60,66) SDATA0 R399 0R/4 SMB_DATA_DIMM (12) SMB_CLK_DIMM (12)



MICRO-STAR INT'L CO., LTD		
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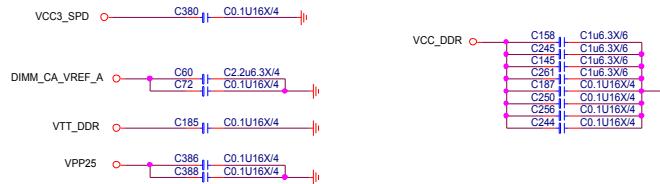
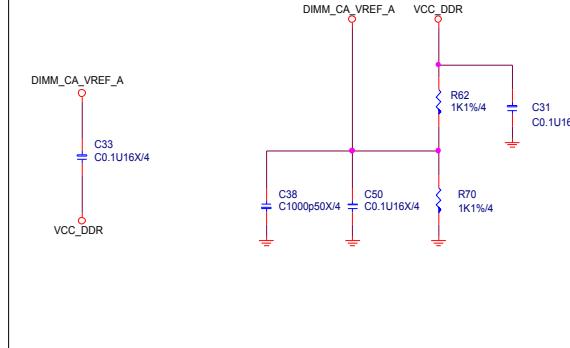


DIMM SLOT PN BY SPEC

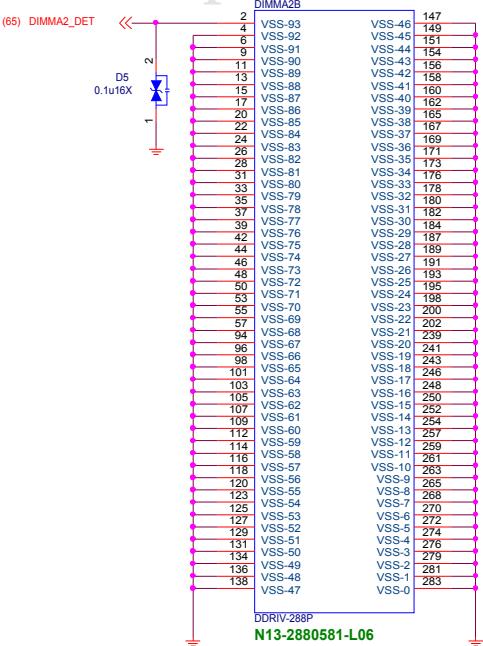
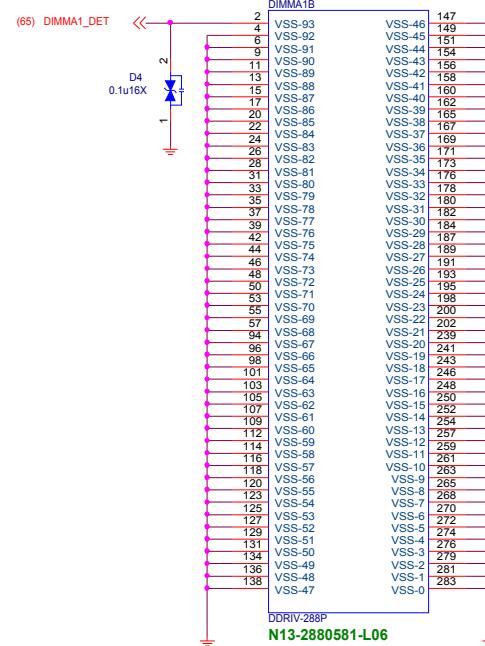


DDR VREF

(place resistors close to DIMMs)



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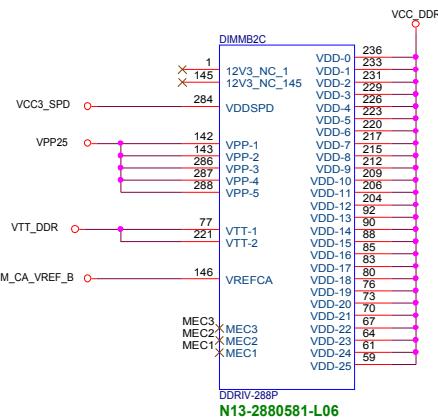
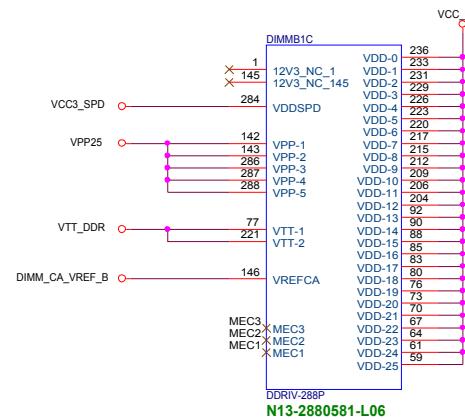
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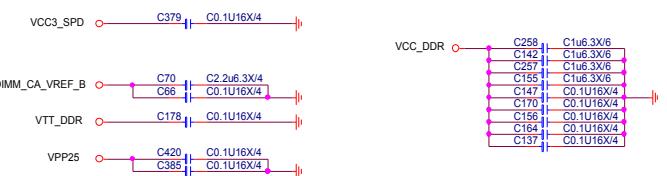
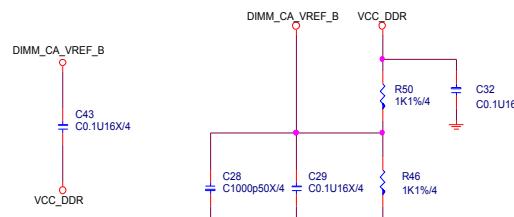
MICRO-STAR INT'L CO., LTD.

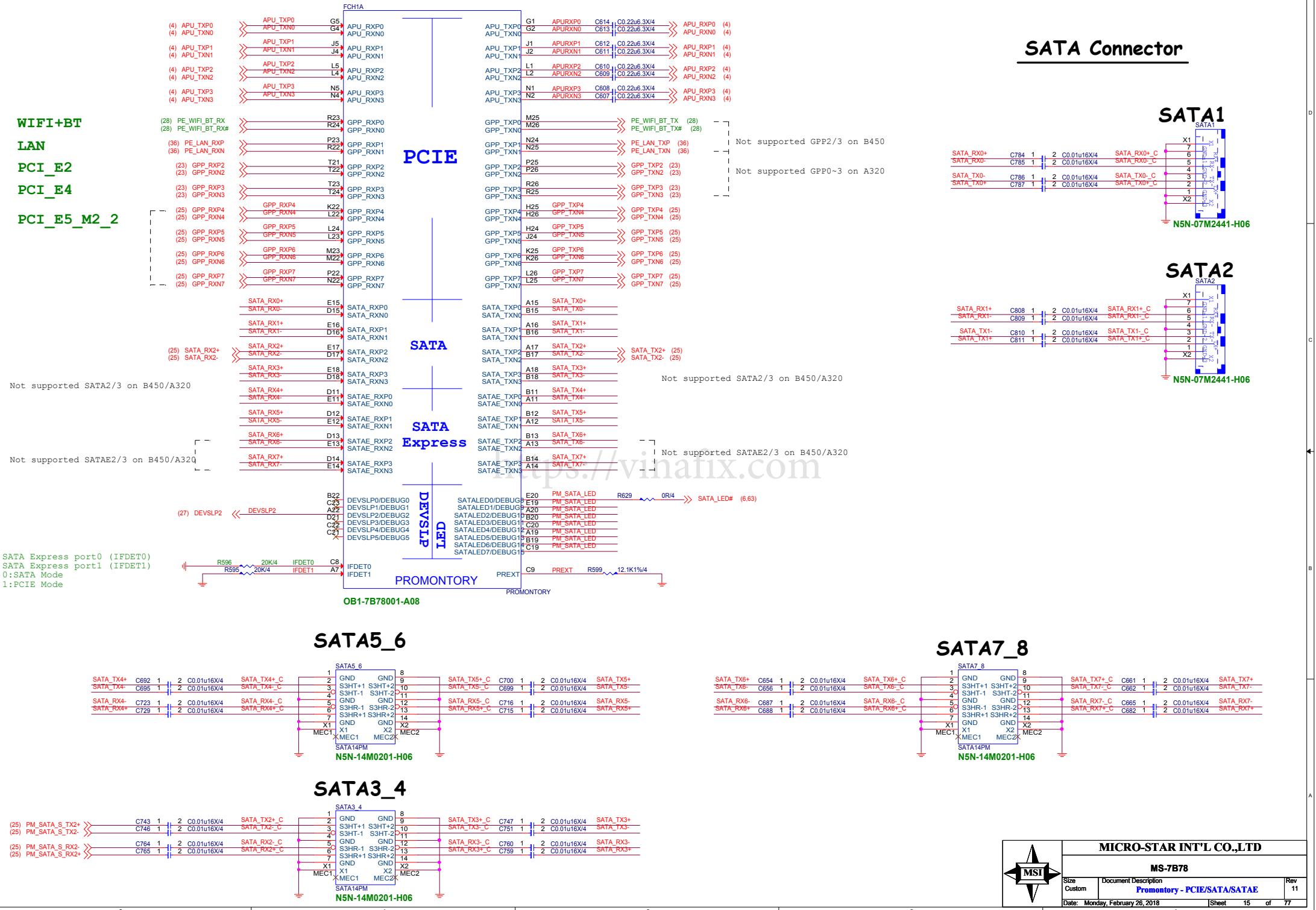
MS-7B78

Size Custom	Document Description DDR4 - POWER/GND-1	Rev 11
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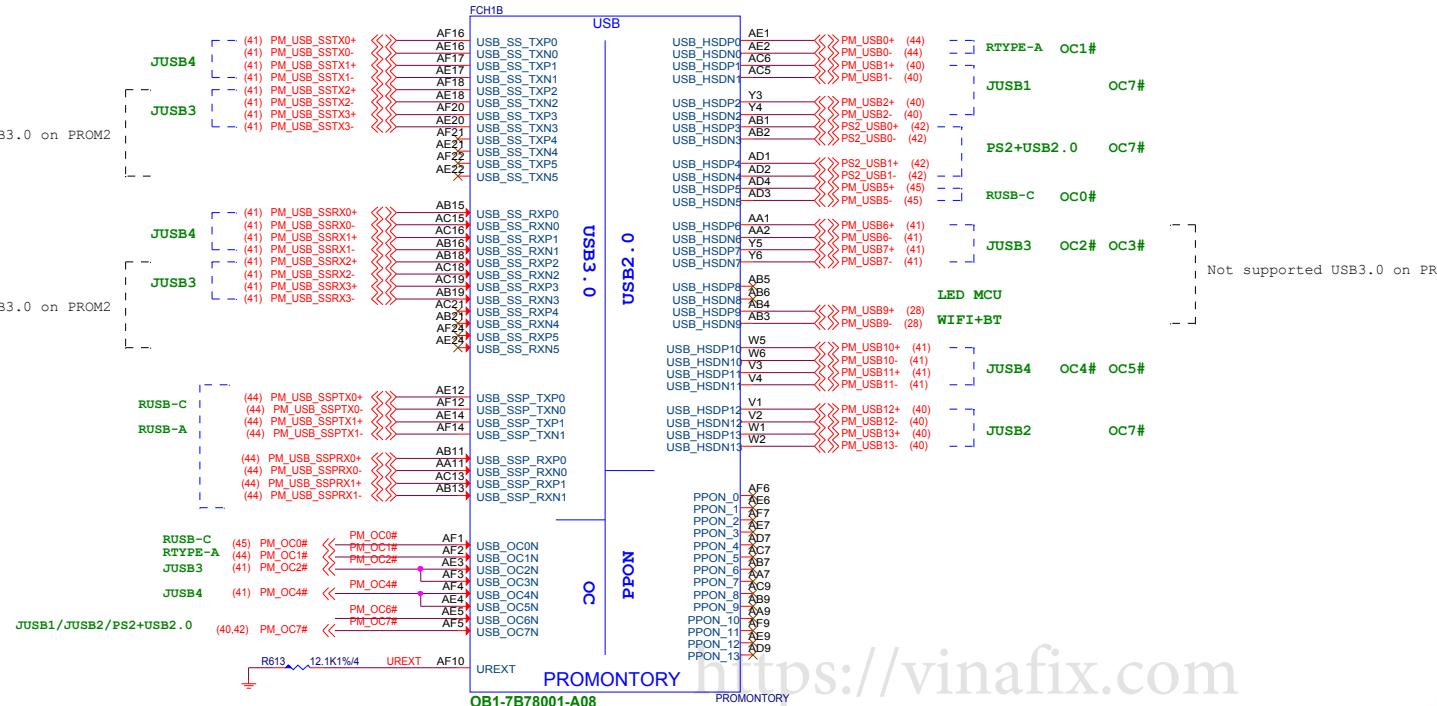
DDR VREF (place resistors close to DIMMs)





Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
USB_HSDP/N[1]	USB_OC7N	
USB_HSDP/N[2]	USB_OC7N	
USB_HSDP/N[3]	USB_OC7N	
USB_HSDP/N[4]	USB_OC7N	
USB_HSDP/N[12]	USB_OC7N	
USB_HSDP/N[13]	USB_OC7N	



Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port0~3	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

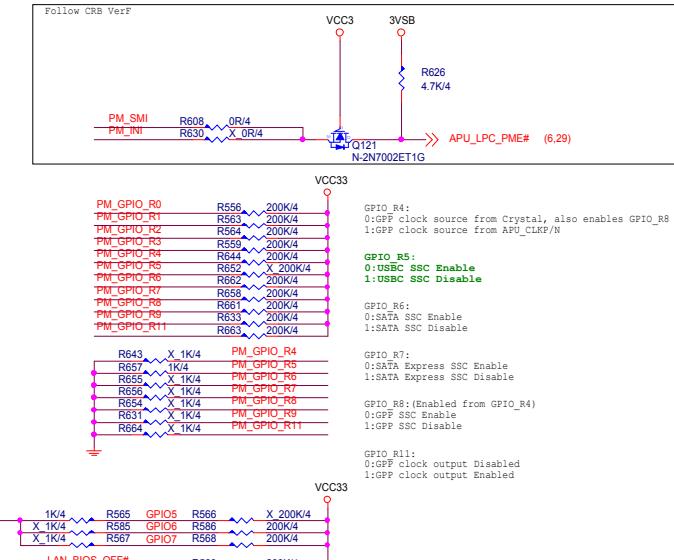
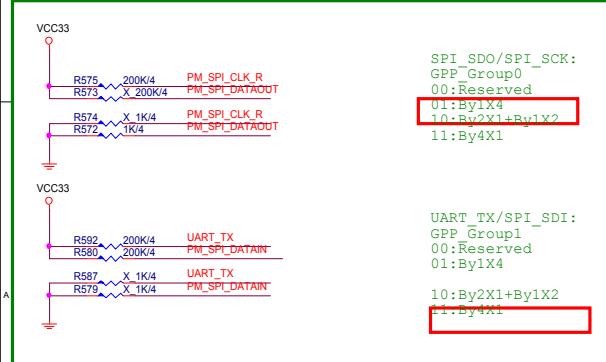
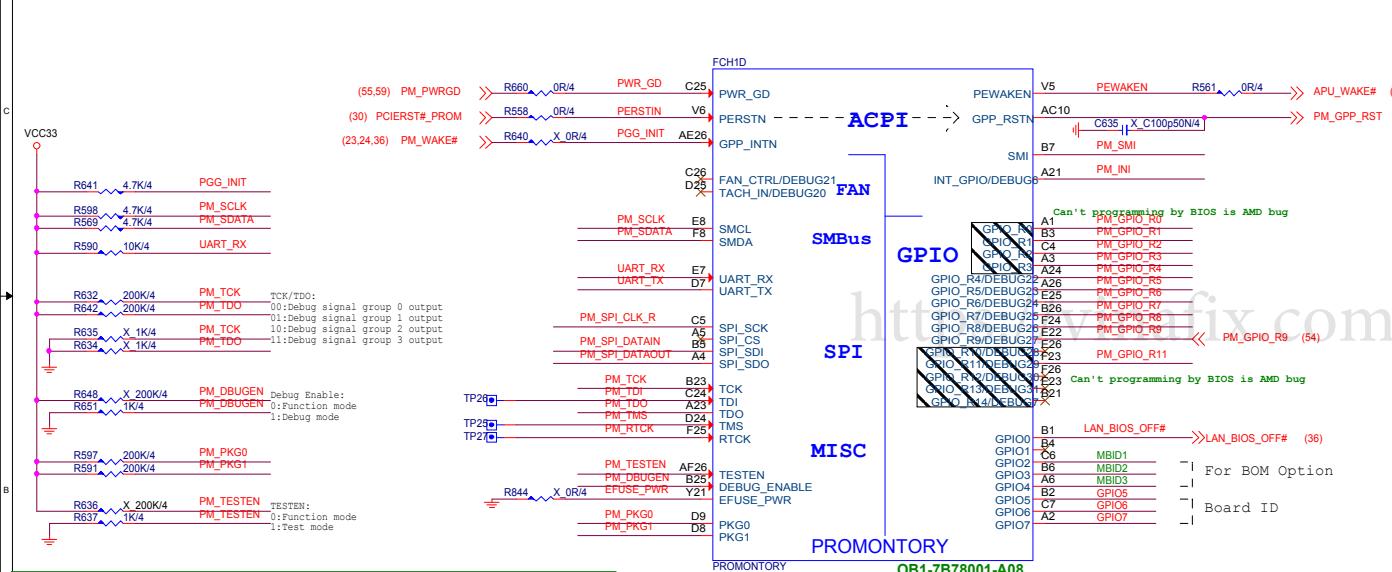
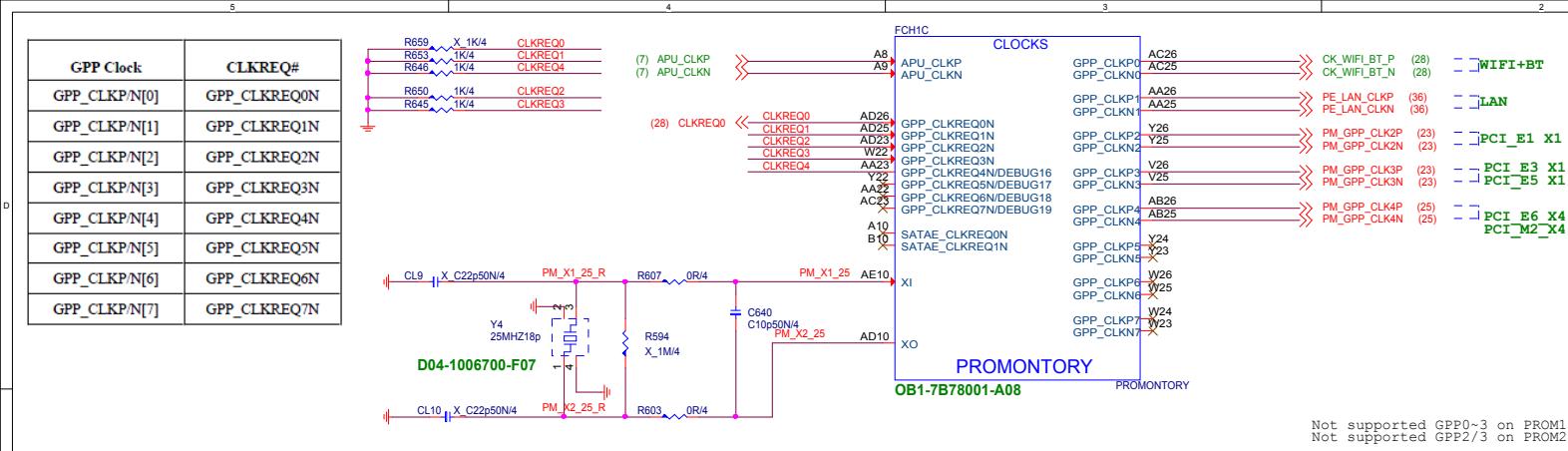
CLK2.3不能用
CLK1~3不能用

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen1 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0-1	USB_SS Port 0-5	USB_HSD Port0-13	USB_SSP Port0
PROM2	USB_SSP Port0-1	USB_SS Port 0-1	USB_HSD Port0-5	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port1	USB_HSD Port10, 12-13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0-3	SATAE port0-3	GPP lane0-7	CLK0-7
PROM2	SATA port0-1	SATAE port0-1	GPP lane0-1	CLK0-1
PROM1	SATA port0-1	SATAE port0-1	GPP lane4-7	CLK4-7

CLK2.3不能用
CLK1-3不能用

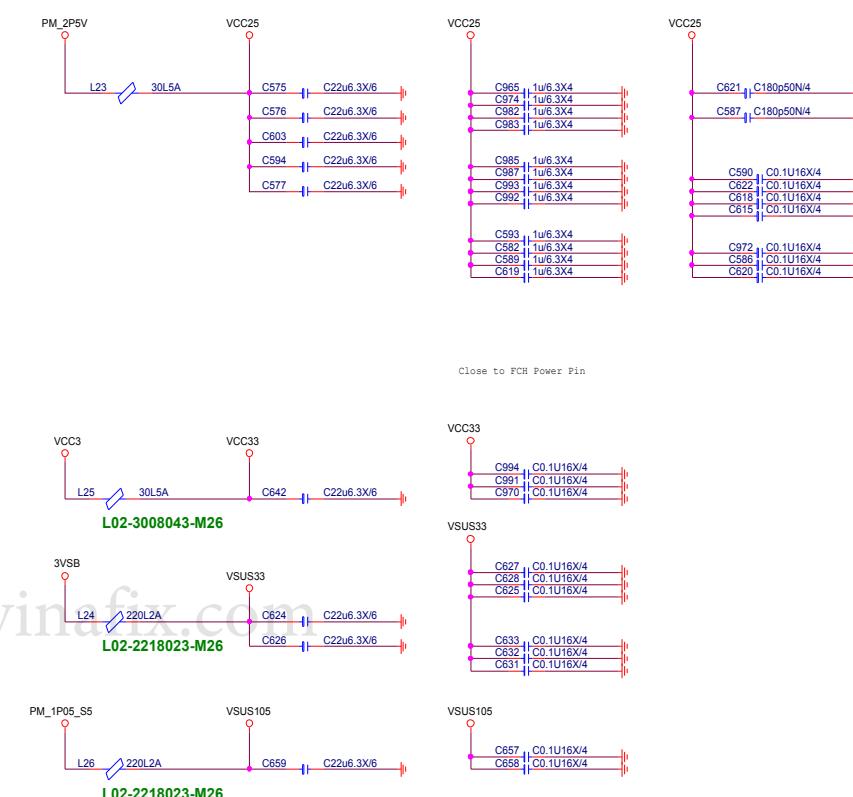
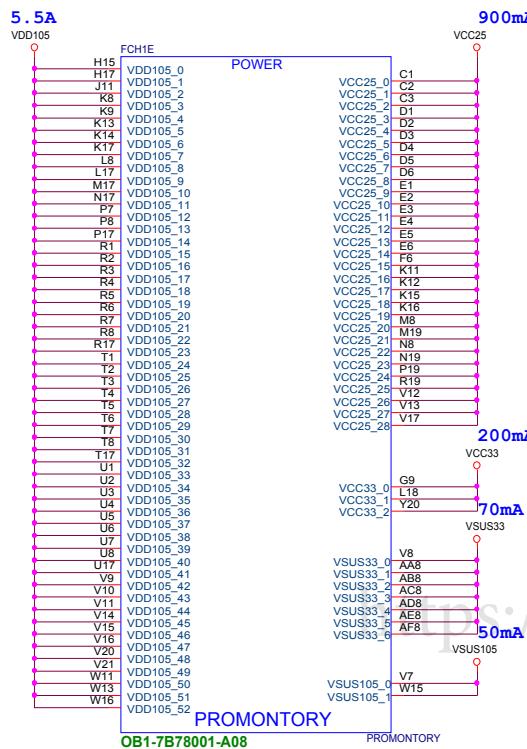
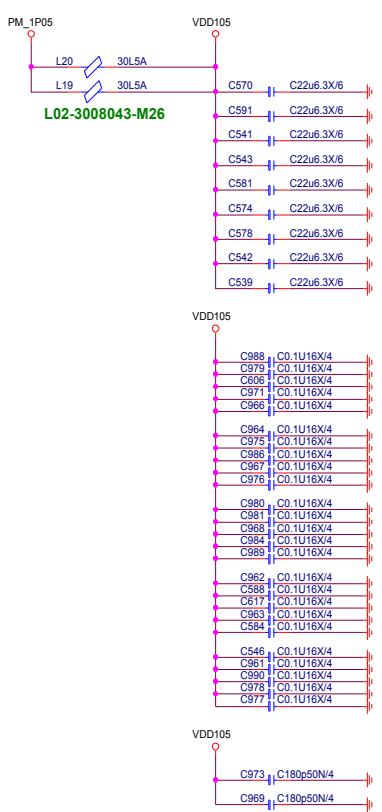


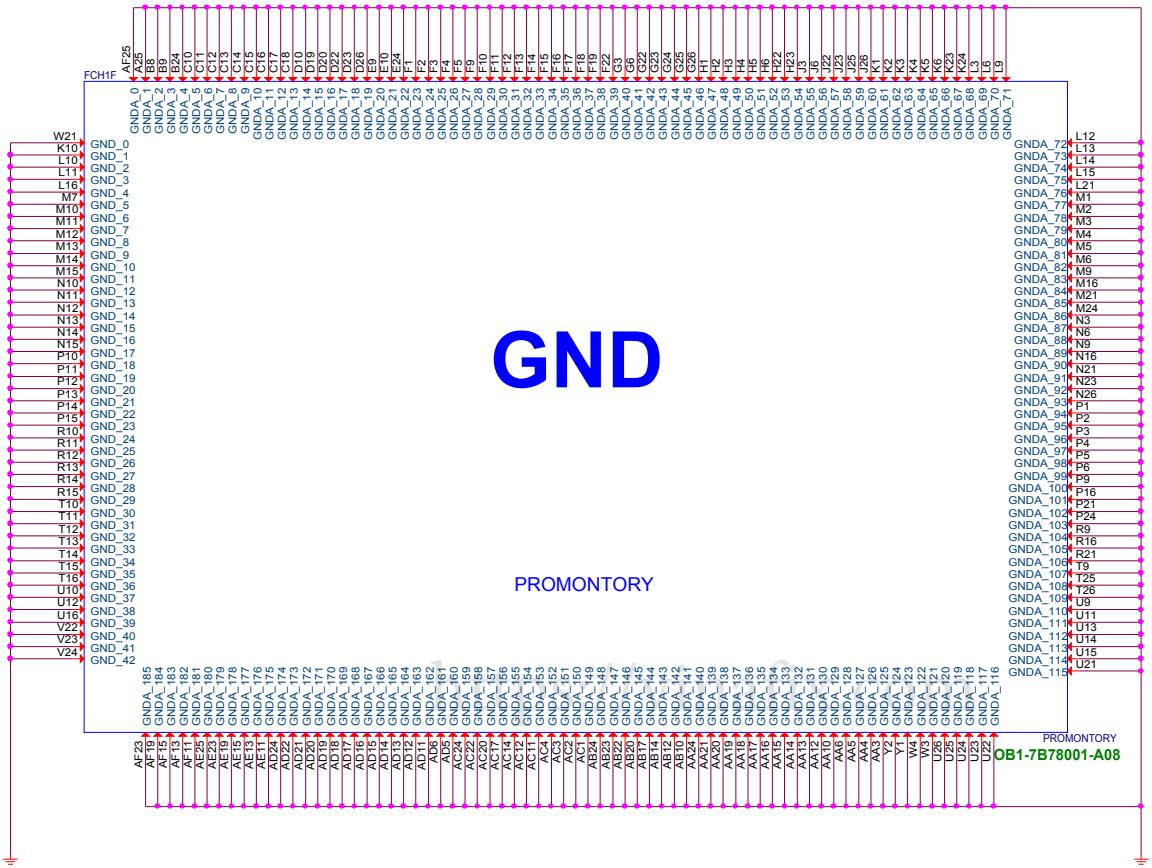
	MBID3	MBID2	MBID1
Z470	0	0	0

BOM OPTION

VCC3	R582 X 10K4 <MSI-BOM>	MBID1	R581 10K4 <MSI-BOM>
	R584 X 10K4 <MSI-BOM>	MBID2	R583 10K4 <MSI-BOM>
	R586 X 10K4 <MSI-BOM>	MBID3	R588 10K4 <MSI-BOM>

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	Promontory - CLK/ACPI/GPIO	Date: Monday, February 26, 2018	Sheet 17 of 77



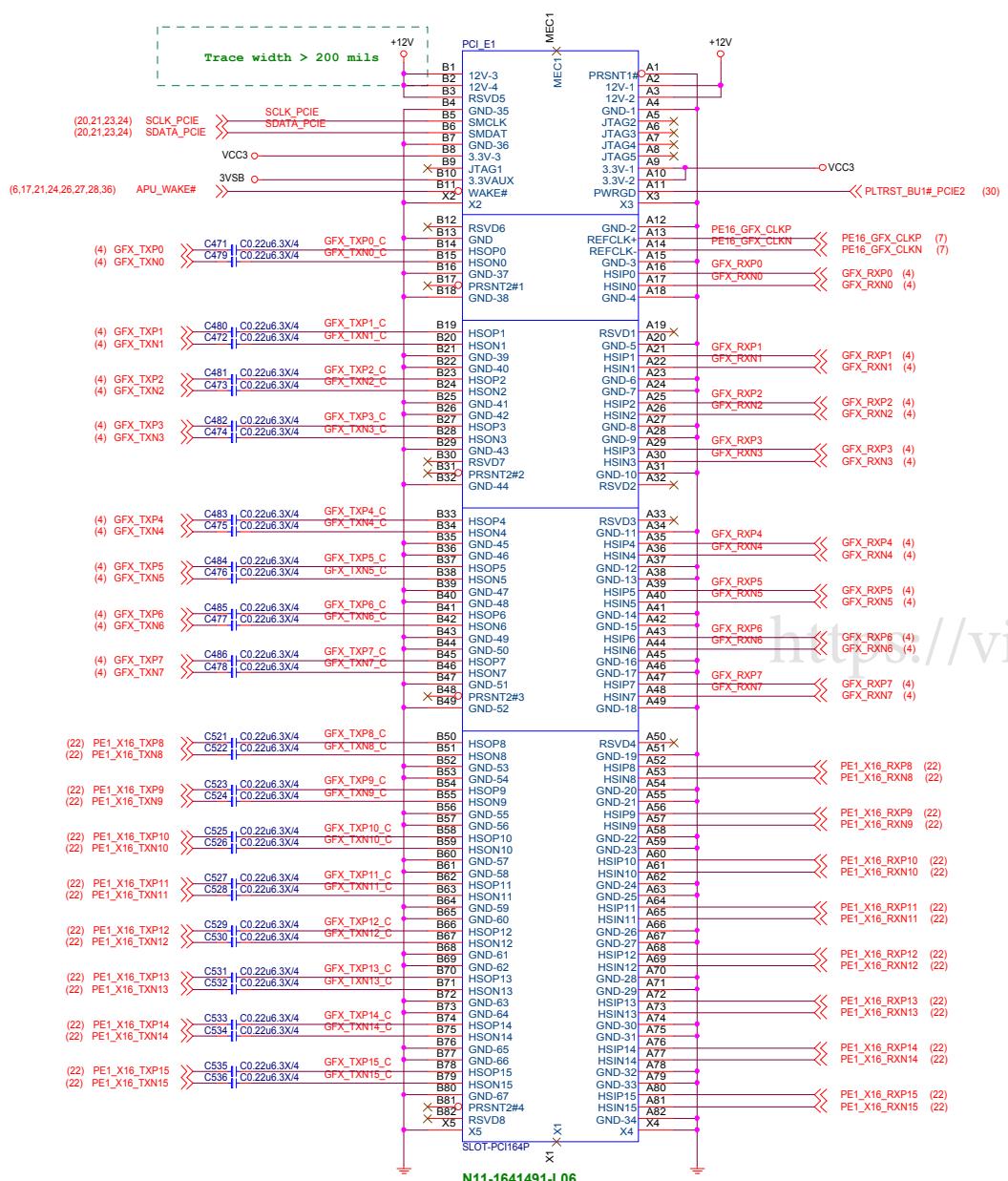


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PCI EXPRESS x16 Slot

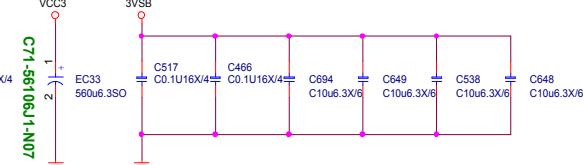
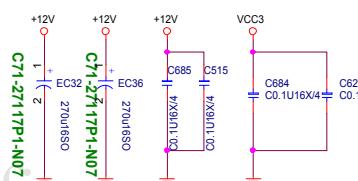
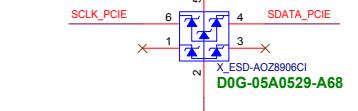
PCI E1



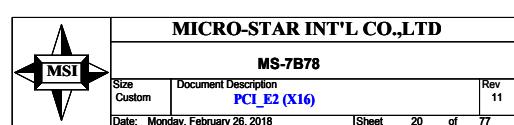
SMB_SEL
GPIO Default High



X_ESD-AO8906CI
D0G-05A0529-A68

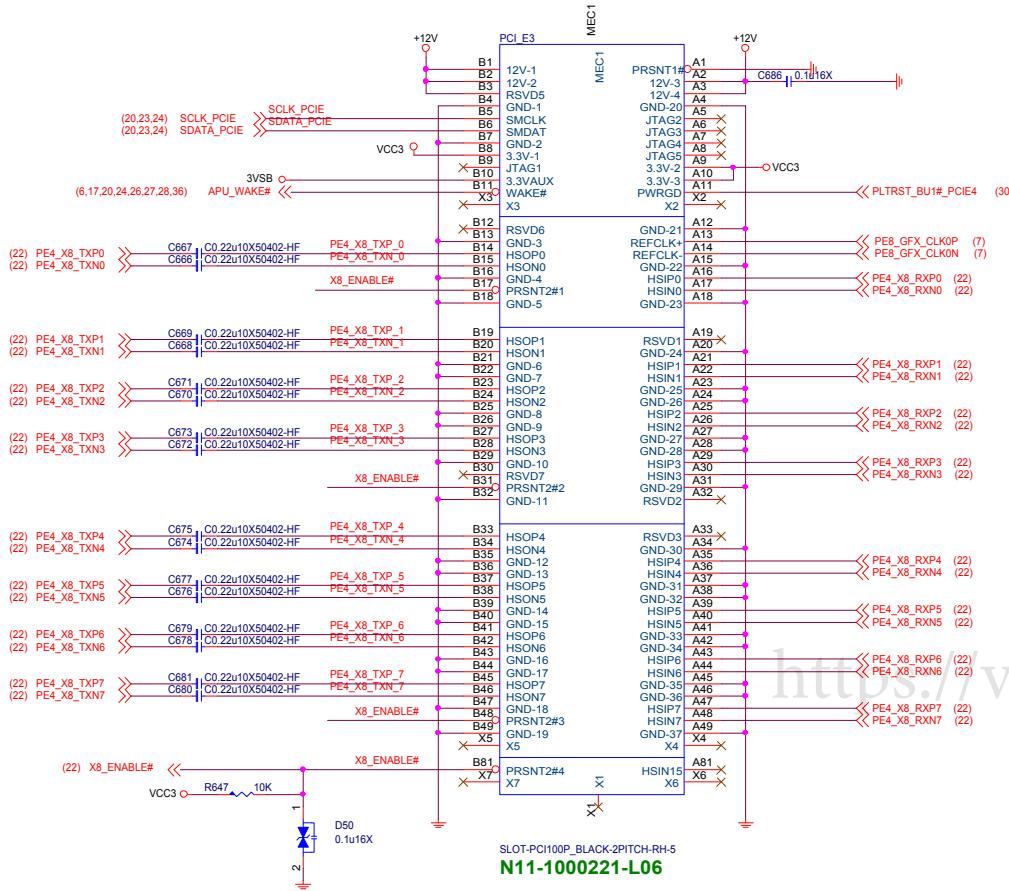


PCI Express x16 Slot		
+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA



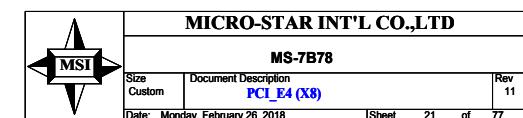
PCI EXPRESS x8 SLOT

PCI_E3



SLOT-PCI100P_BLACK-2PITCH-RH-5
N11-1000221-L06

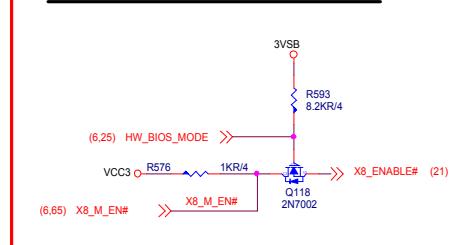
PCI Express x8 Slot		
+12V	-	A
+VCC3	-	3A
+3V3_S5 (wake)	-	375mA
+3V3_S5 (no wake)	-	20mA



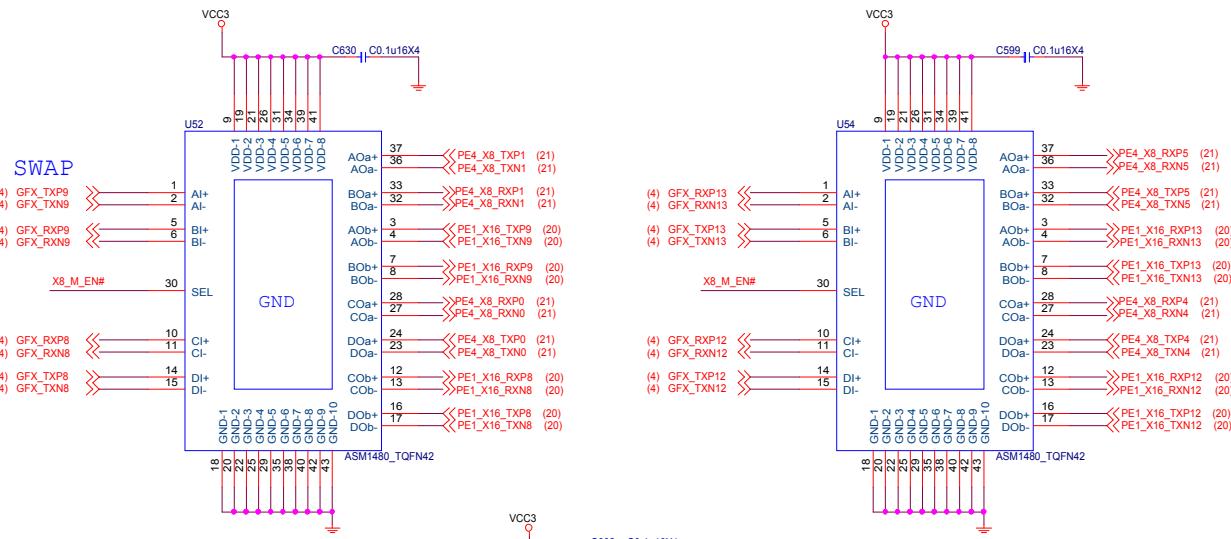
PCI EXPRESS Switch

For PCIE1 & PCIE3

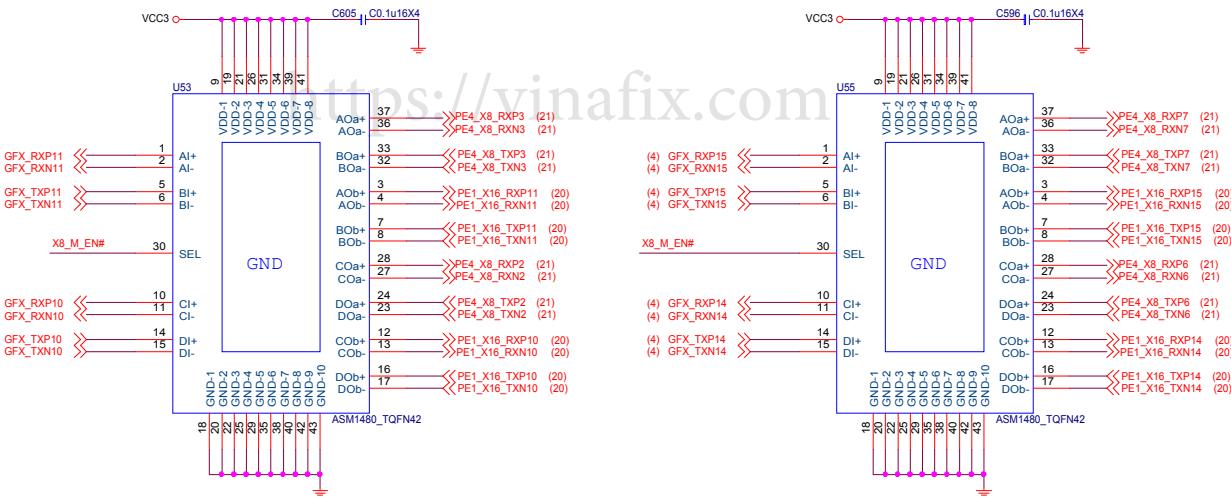
PCIE Lanes control circuit



	HW_BIOS_MODE	X8_M_EN#
Auto	1	1
Manual x16	0	1
Manual x8, x8	0	0



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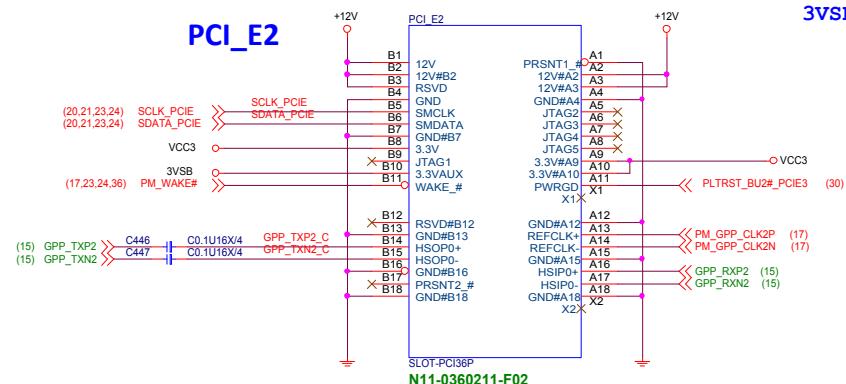


PCI EXPRESS X1 SLOT

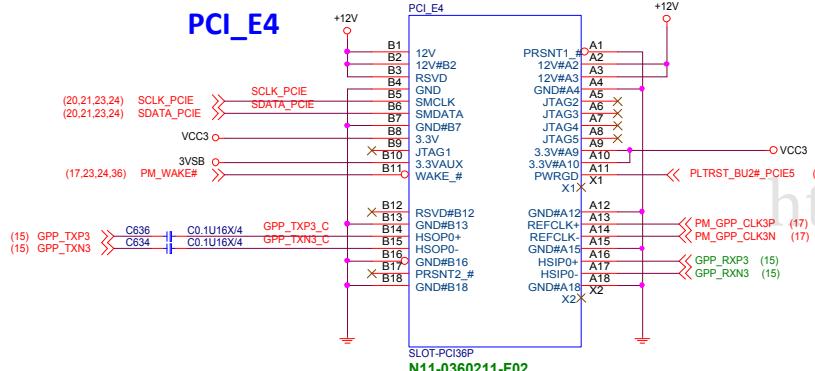
12V - 0.5A

VCC3 - 3A

3VSBV - 375mA



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PCI Express x1 Slot *3	
+12V	- 1.5 A
+VCC3	- 9A
+3V3_S5 (wake)	- 1125mA
+3V3_S5 (no wake)	- 60mA



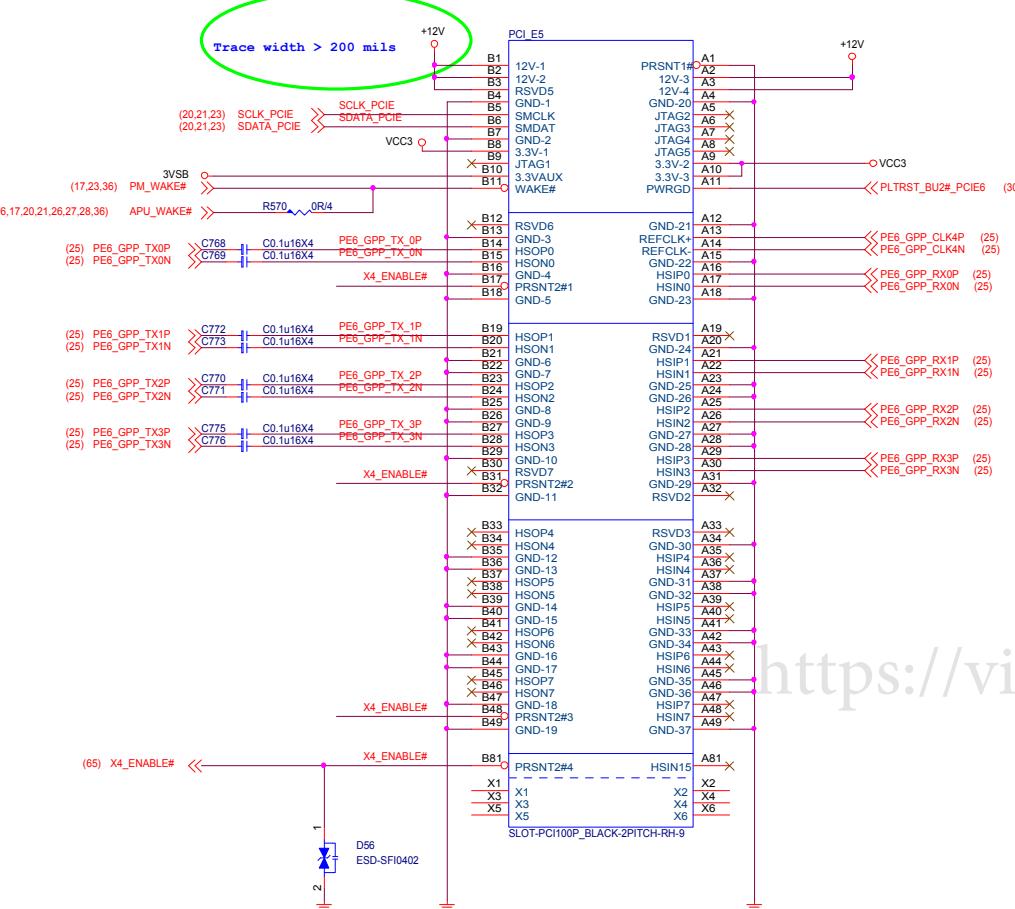
MICRO STAR INT'L CO., LTD.

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 Custom PCI_E1_E3_E5 (X1) 11
 Date: Monday, February 26, 2018 Sheet 23 of 77

PCI EXPRESS X4 SLOT

PCI_E6



PCI Express x4 Slot *1		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA



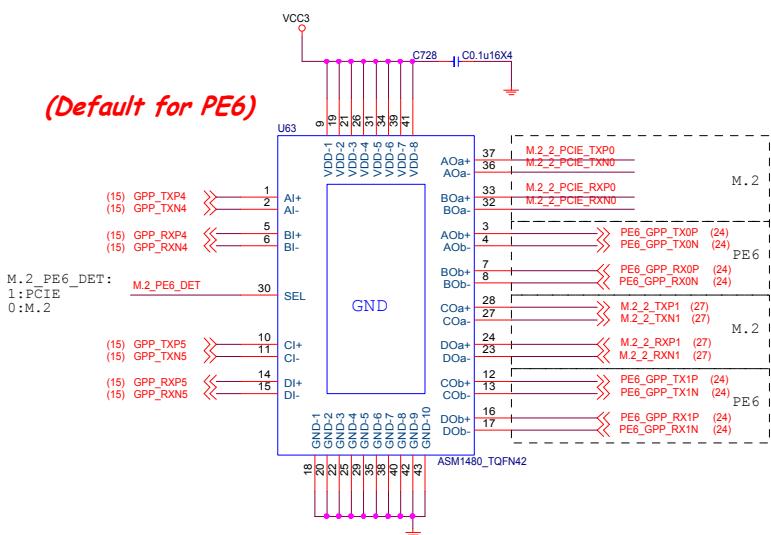
MICRO-STAR INT'L CO LTD

MS-7B78

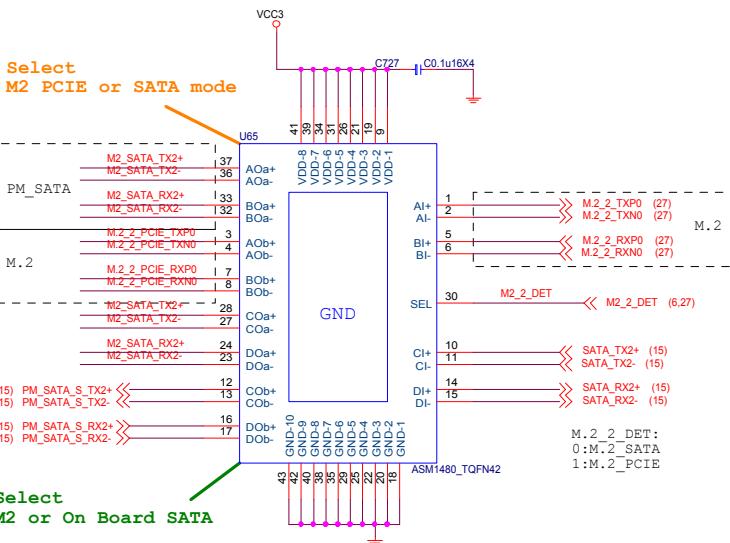
MS-7B7c
Date: Monday, February 26, 2018 Sheet 24 of 77
Size Custom Document Description Rev
PCI_E6 (X4) 11

PCI_E6 and M2_2 and SATA1 Switch

(Default for PE6)

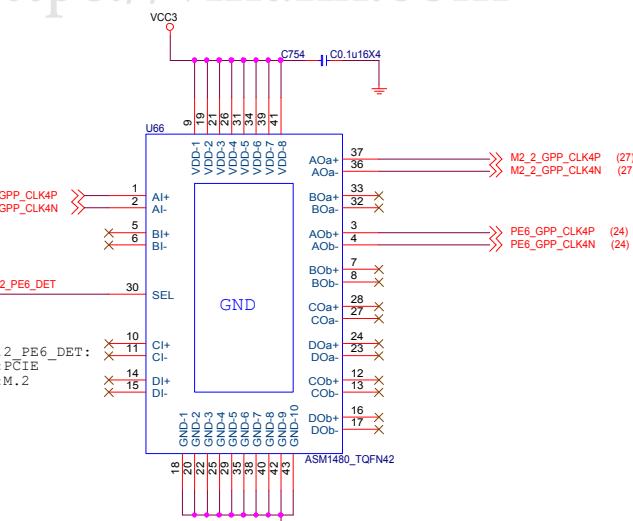
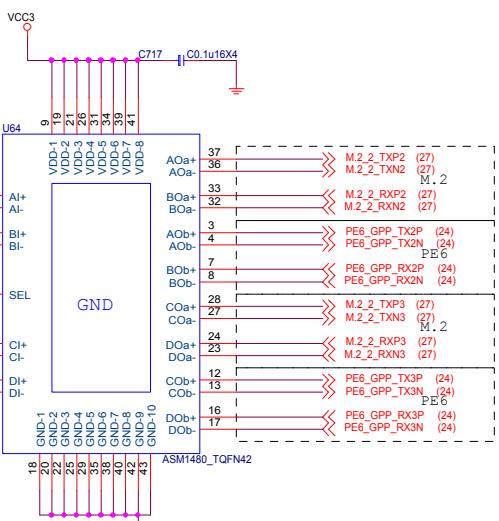


Select
M2 PCIE or SATA mode



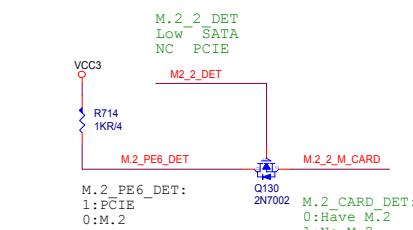
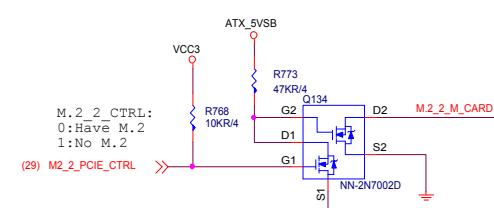
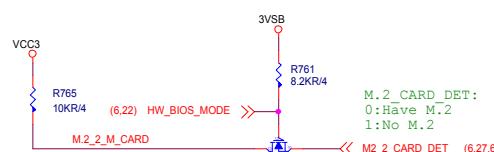
Select
M2 or On Board SATA

(Default for PE6)



Manufacture Control					
	AUTO Mode	PCIE X4	M.2 X4	M.2 SATA	SATA5
HW_BIOS_MODE	1	0	0	1	/
M2_2_PCIE_CTRL	0	1	0	0	/

紅色數字為判抓到PCIE或SATA device時所要判斷的訊號



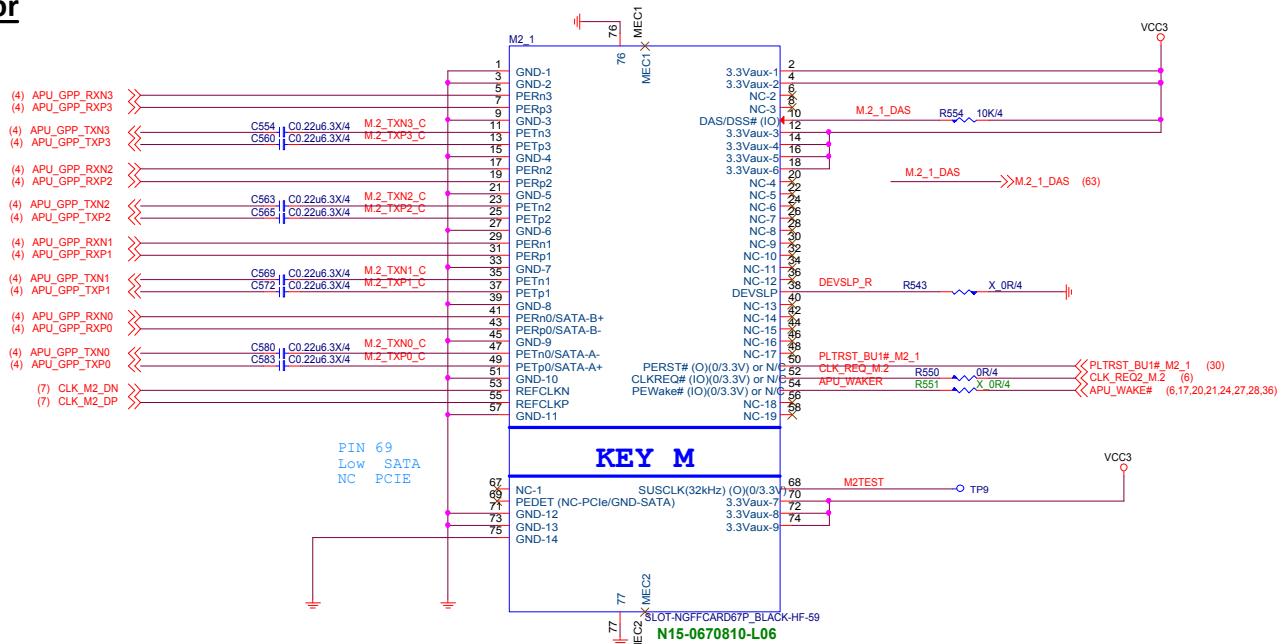
MICRO-STAR INT'L CO., LTD.

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Size Custom	Document Description PCIE Switch PE6 / M2_2	Rev 11
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M.2 1 Connector

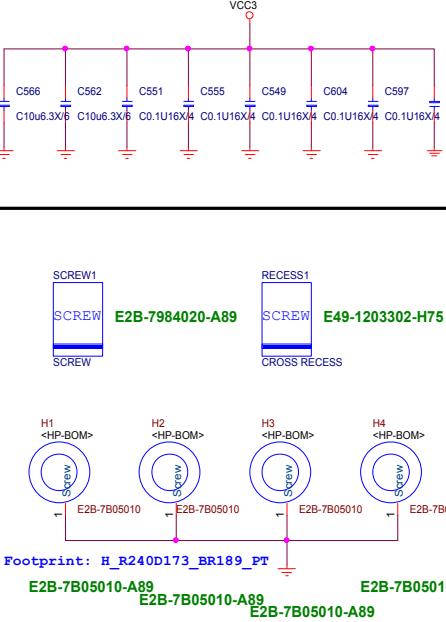
3.3V@2.5A



KEY M

SLOT-NGFFCARDS7P_BLACK-HF-59
N15-0670810-L06

3.3V@2.5A



SCREW1

E2B-7984020-A89

RECESS1

E49-1203302-H75

SCREW

CROSS RECESS

H1

<HP-BOM>

E2B-7B05010-A89

H2

<HP-BOM>

E2B-7B05010-A89

H3

<HP-BOM>

E2B-7B05010-A89

H4

<HP-BOM>

E2B-7B05010-A89

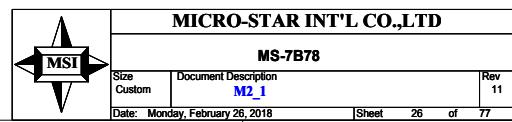
RECESS3

SCREW

SHIELD

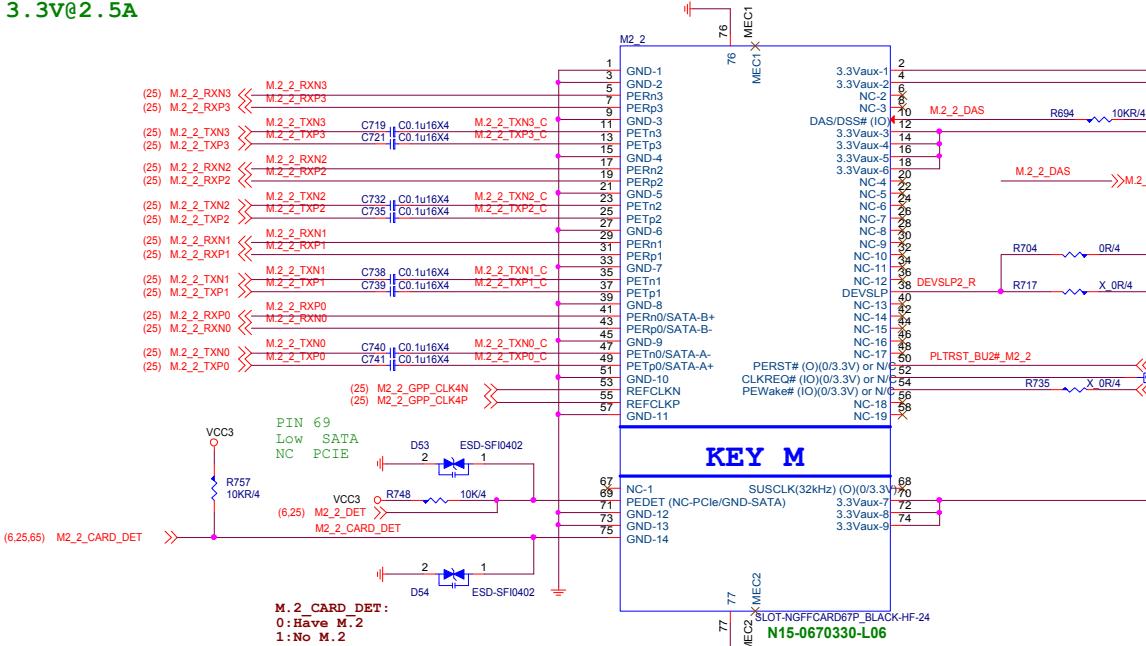
https://vinafix.com

Vinafix.com

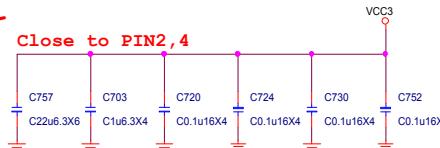


M.2 2 Connector

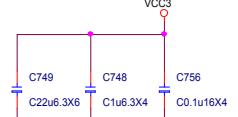
3.3V@2.5A



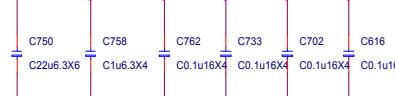
VCC3 2.5A



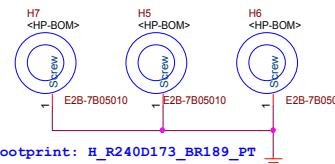
Close to PIN12, 14, 16, 18



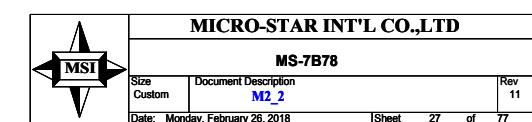
- Close to PIN70, 72, 74

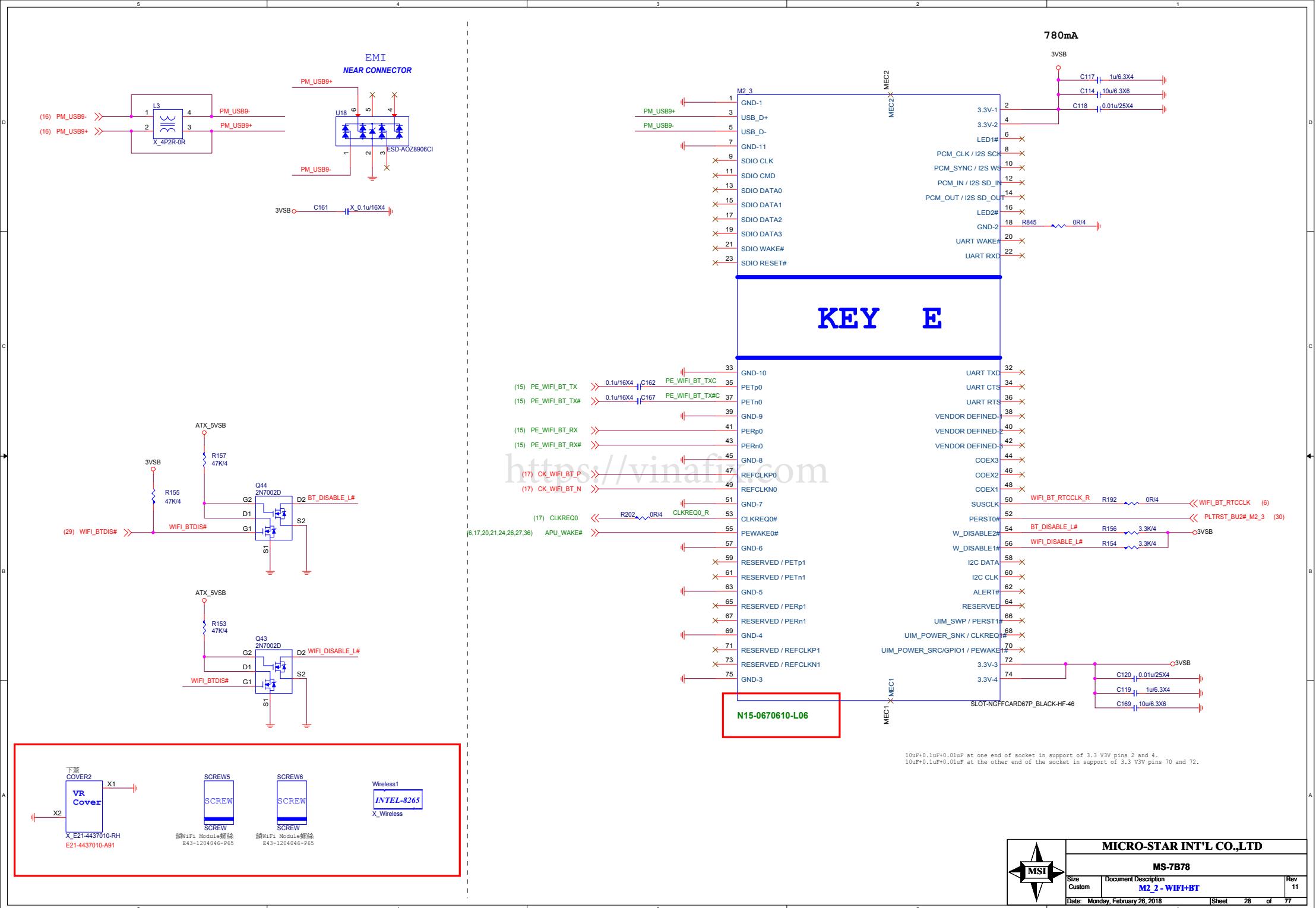


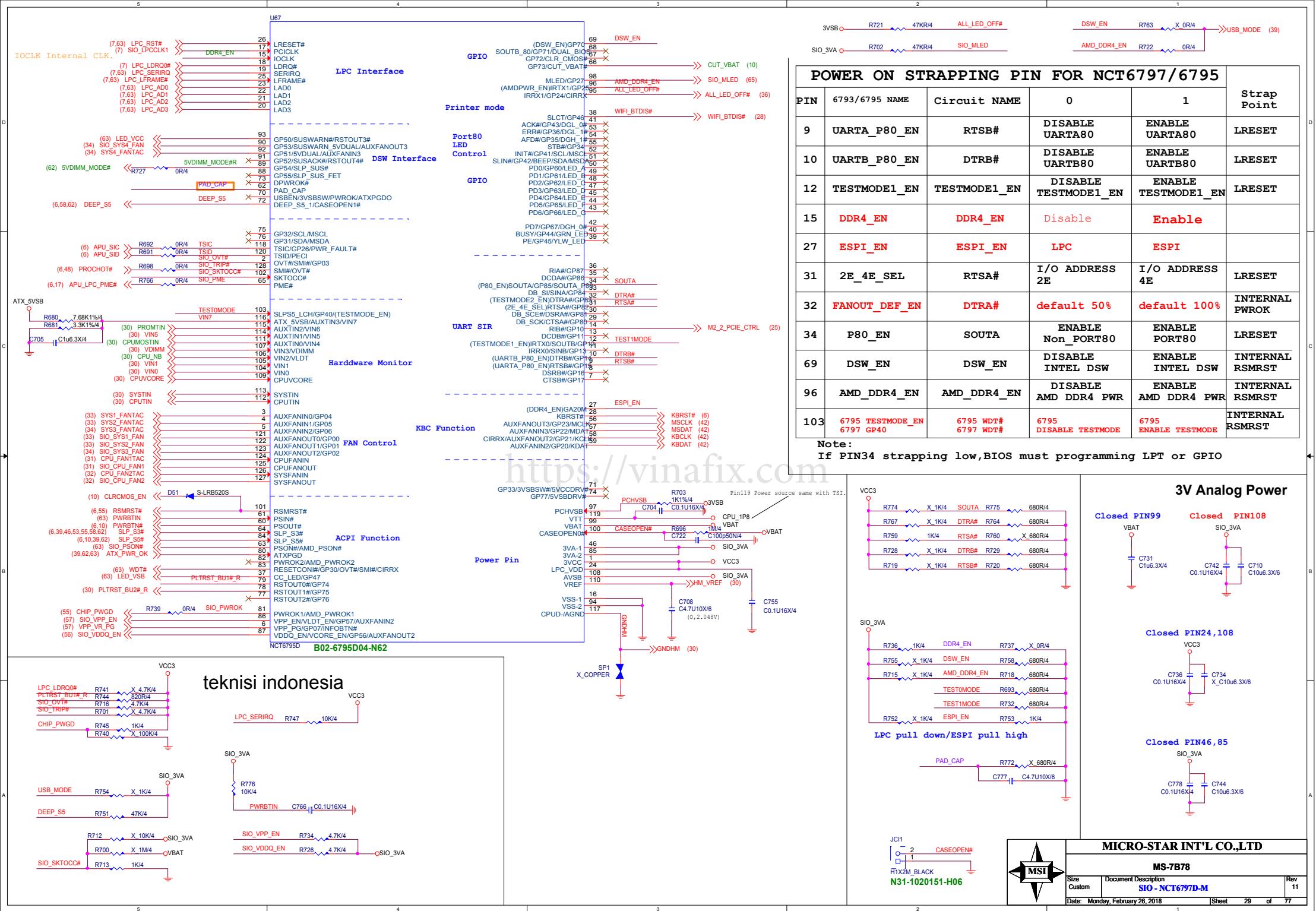
<https://vinafix.com>



Footprint: H_R240D173_BR189_PT 
E2B-7B05010-A89  **E2B-7B05010-A89**  **E2B-7B05010-A89**

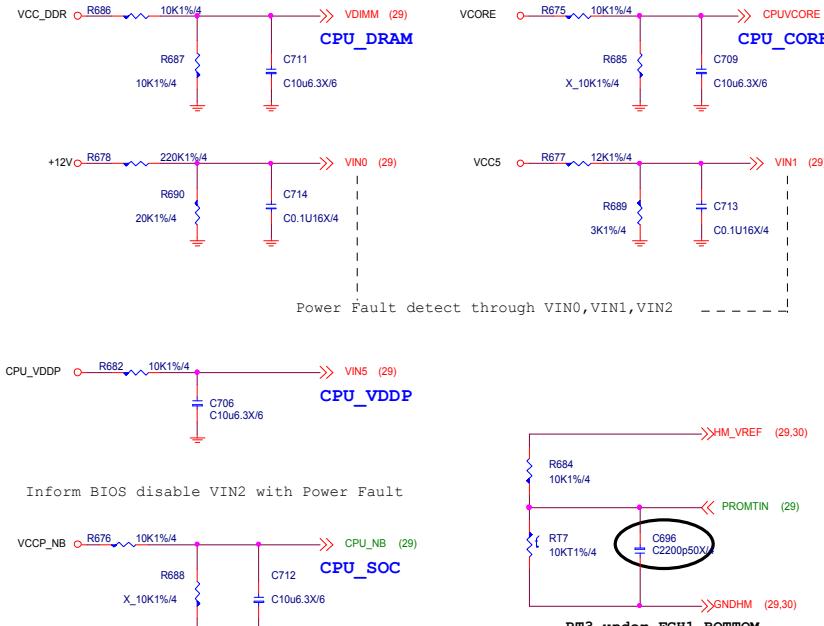




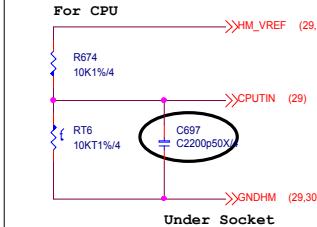


HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect

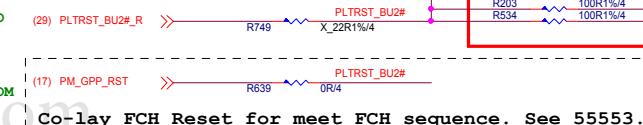


TEMP SENSOR

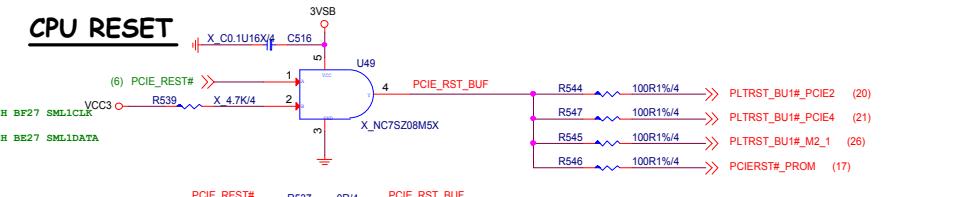


COM PORT

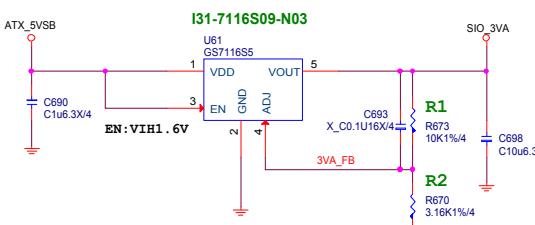
PROM RESET



CPU RESET



SIO_3VA



$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (10K/3.16K)) \\ &= 3.33V \end{aligned}$$

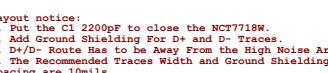
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MS-7B78

Size	Document Description	Rev
Custom	SIO - HW Monitor / NCT7718W	11

NCT7718W SM Bus address is 98h (1001100xb)

Default: ALERT# Output Comparator Mode



Layout notice:

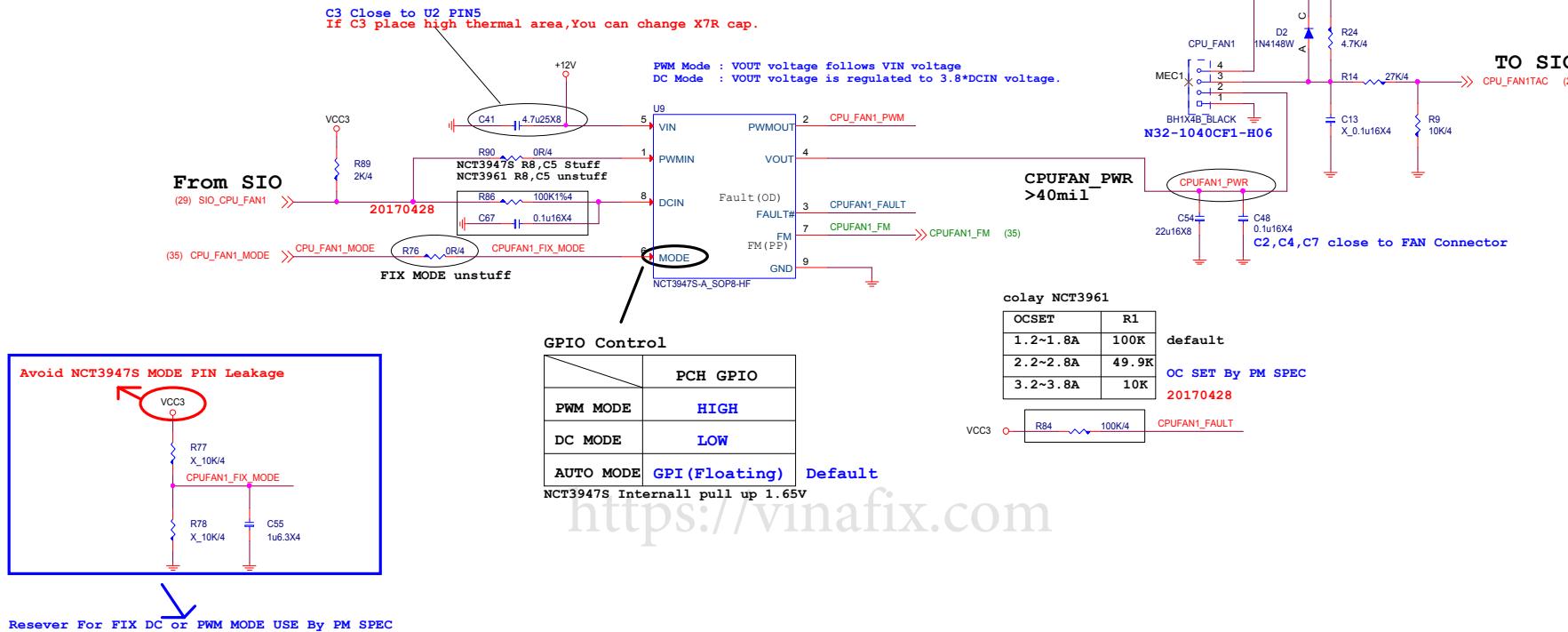
- Put the C1 2200pF to close the NCT7718W.
- Add Ground Shielding For D+ and D- Traces.
- D+/D- Route Has to be Away From the High Noise Area.
- The Recommended Traces Width and Ground Shielding Spacing are 10mils.

TEMPERATURE (°C)	T_CRT#				
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	77	87	97	107	117
2KΩ	79	89	99	109	119
7.5KΩ	81	91	101	111	121
10.5KΩ	83	93	103	113	123
14KΩ	85	95	105	115	125
18.7KΩ					

TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

1. PWM/DC/OCP LED
2. Mode GPIO BIOS can switch PWM/DC MODE
3. OCP connect GPIO for BIOS Use
4. FM:BIOS can read FAN PWM/DC MODE
5. CPUFAN1_LED_OFF_BLINK Use LED On/OFF

CPUFAN1



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TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

1. PWM/DC/OCP LED

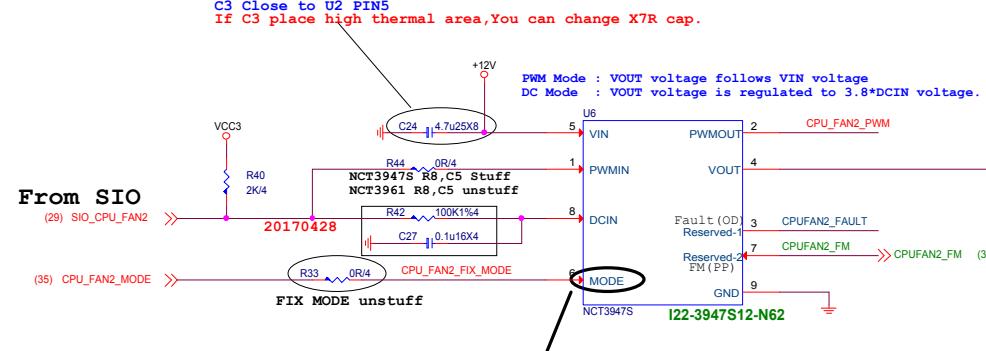
PUMPFAN1 2.Mode GPIO BIOS can switch PWM/DC MODE

3.OCP connect GPIO for BIOS Use

4.FM:BIOS can read FAN PWM/DC MODE

5.CPUFAN1_LED_OFF_BLINK Use LED On/OFF

C3 Close to U2 PIN5
If C3 place high thermal area, You can change X7R cap.



GPIO Control

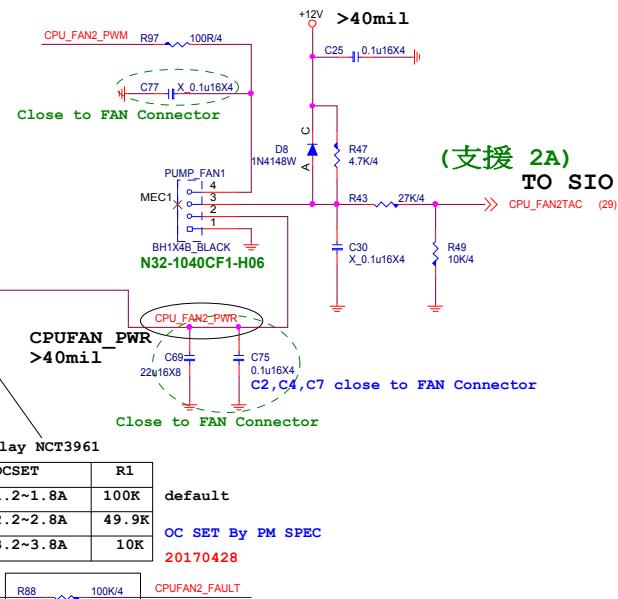
	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

NCT3947S Internal pull up 1.65V

Avoid NCT3947S MODE PIN Leakage

VCC3
R34 X_10K/4
CPU_FAN2_FIX_MODE
R41 X_10K/4
C26 1u6.3X4

Reserve For FIX DC or PWM MODE USE By PM SPEC



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MS-7B78

Size Custom	Document Description	Rev 11
	FAN TYPE-J PUMPFANI	

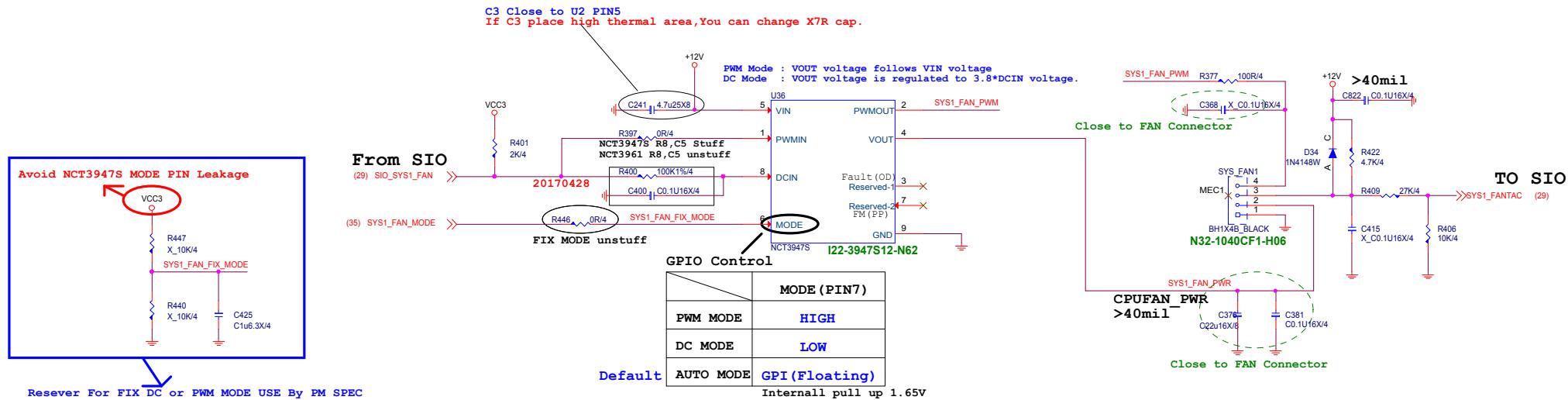
Date: Monday, February 26, 2018

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SYSFAN1

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1. Mode GPIO BIOS can switch PWM/DC MODE

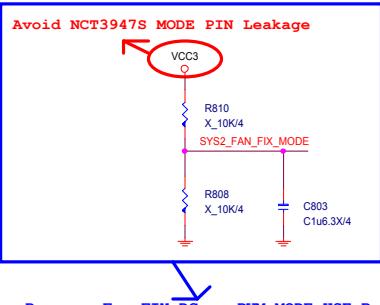


SYSFAN2

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1. Mode GPIO BIOS can switch PWM/DC MODE

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MS-7B78

Size	Document Description	Rev
Custom	FAN TYPE-K SYSFAN1/2	11

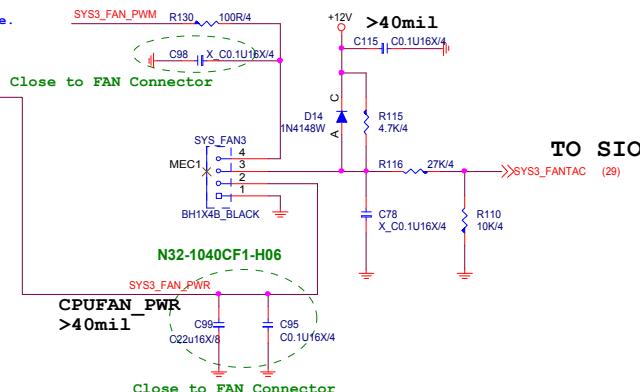
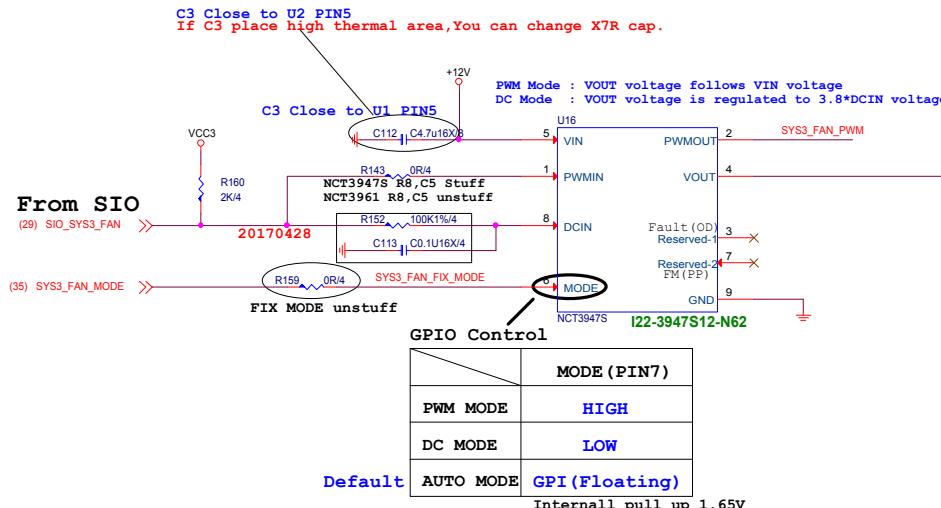
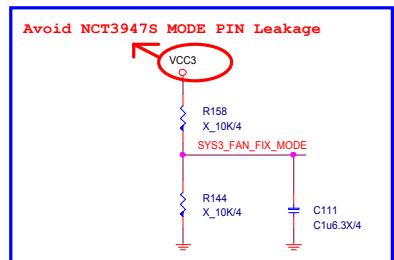
Date: Monday, February 26, 2018

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SYSFAN3

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

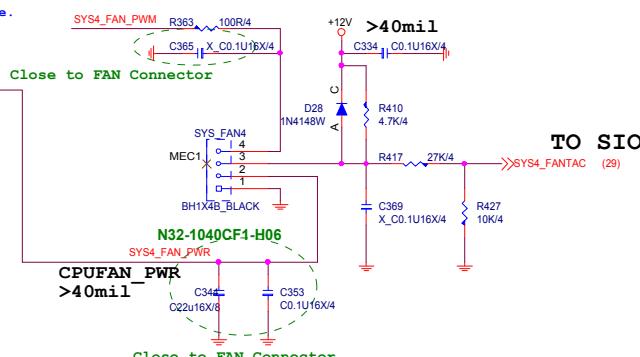
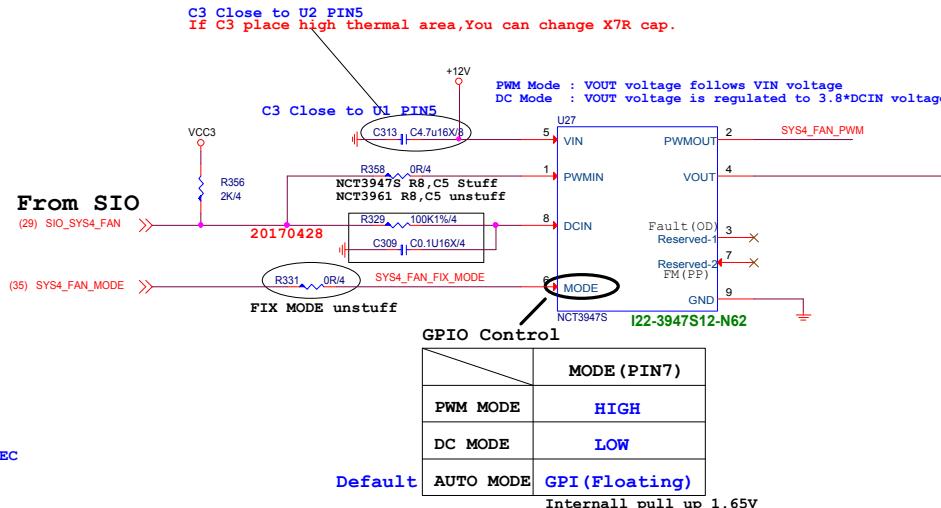
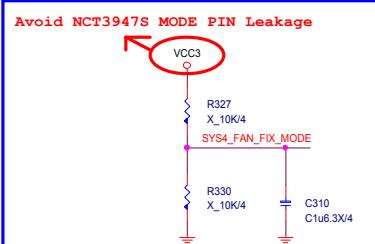
1. Mode GPIO BIOS can switch PWM/DC MODE

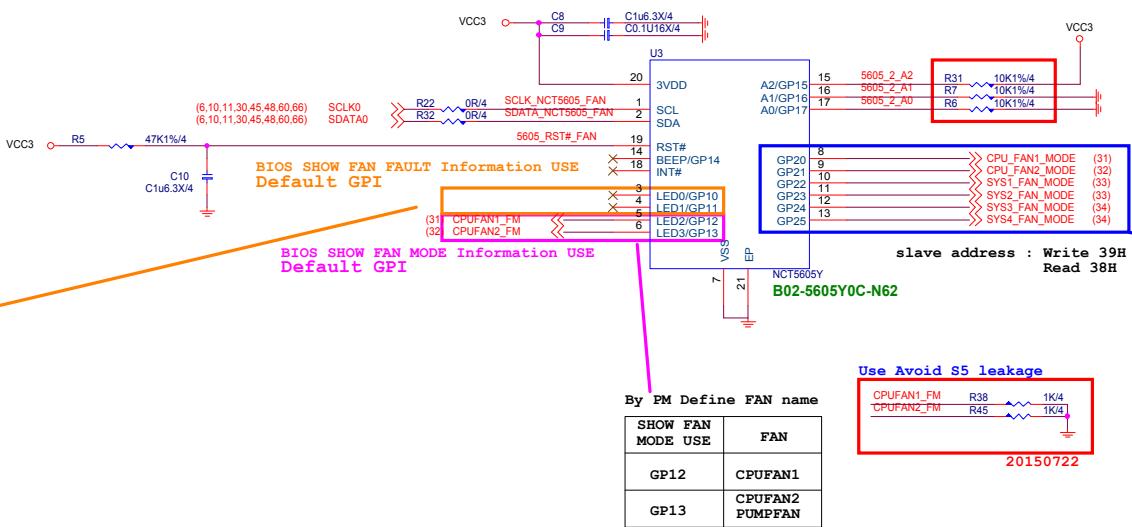


SYSFAN4

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1. Mode GPIO BIOS can switch PWM/DC MODE





By PM Define FAN name

LED OFF BLINK	FAN
GP16	CPUFAN1
GP17	CPUFAN2 PUMPFAN

USE LED OFF & LED BLINK

Default GPI

By PM Define FAN name

SHOW FAN FAULT USE	FAN
GP10	CPUFAN1
GP11	CPUFAN2 PUMPFAN

BIOS SHOW FAN FAULT Information USE
Default GPIBIOS SHOW FAN MODE Information USE
Default GPI

By PM Define FAN name

SHOW FAN MODE USE	FAN
GP12	CPUFAN1
GP13	CPUFAN2 PUMPFAN

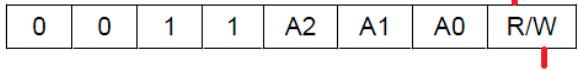
By PM Define FAN name

FAN MODE USE	FAN
GP20	CPUFAN1
GP21	CPUFAN2 PUMPFAN
GP22	SYSFAN1
GP23	SYSFAN2
GP24	SYSFAN3
GP25	SYSFAN4

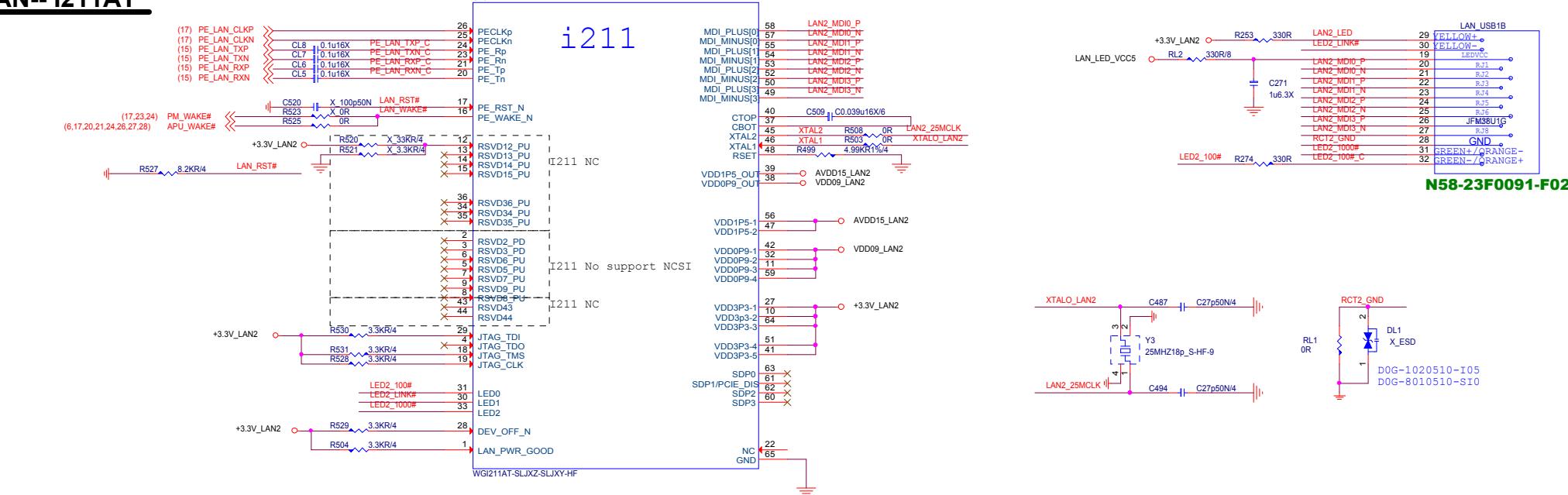
1. GENERAL DESCRIPTION

The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPIO pins. It also can provide SMBus™ address setting pins to set the address during power-on reset or from external reset.

NCT5605Y SMBus™ Address is:

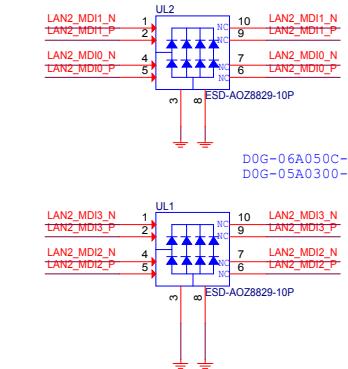
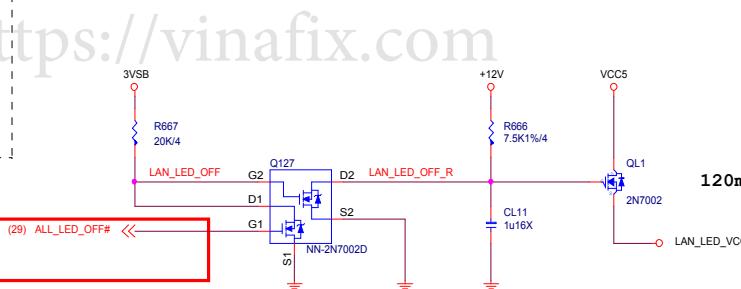
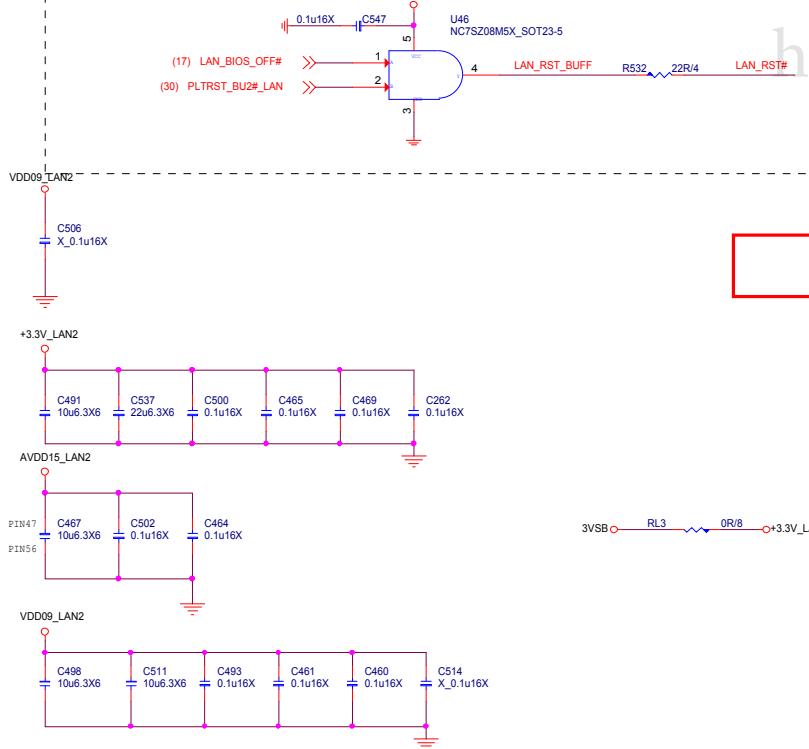
0
1

LAN-- I211AT



2016.07.21 Add

Disable LAN Function



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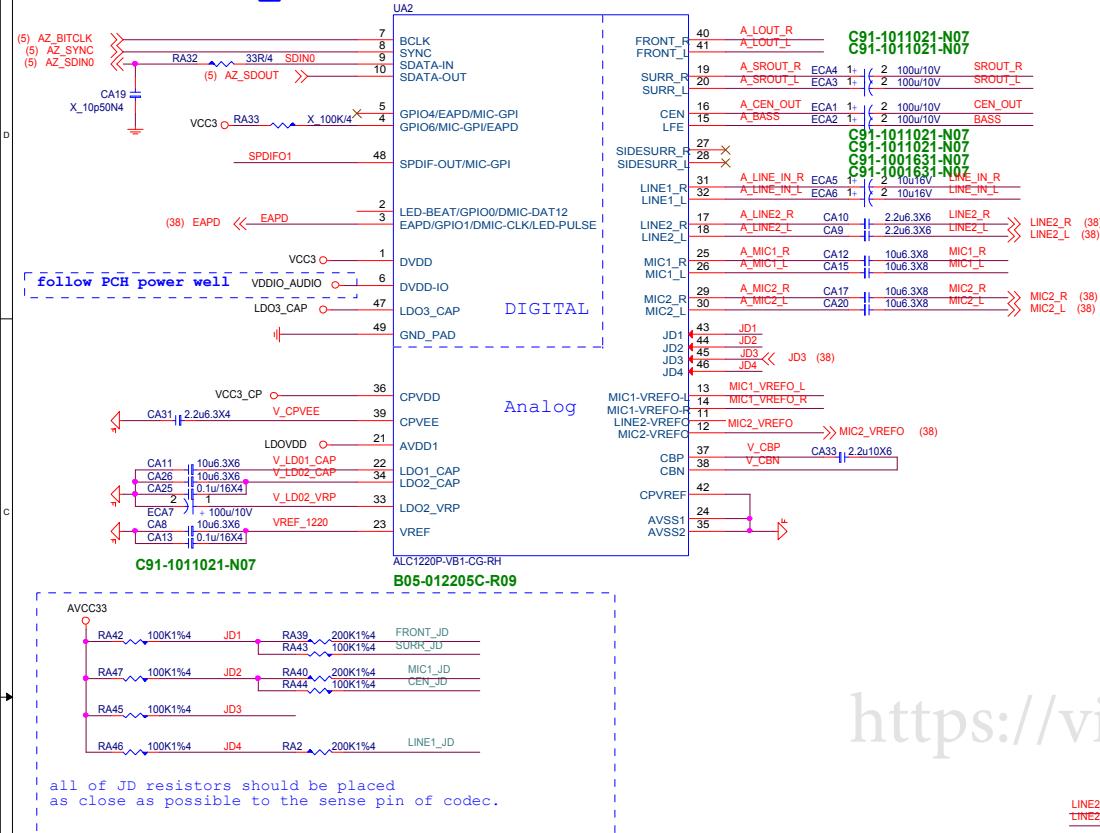


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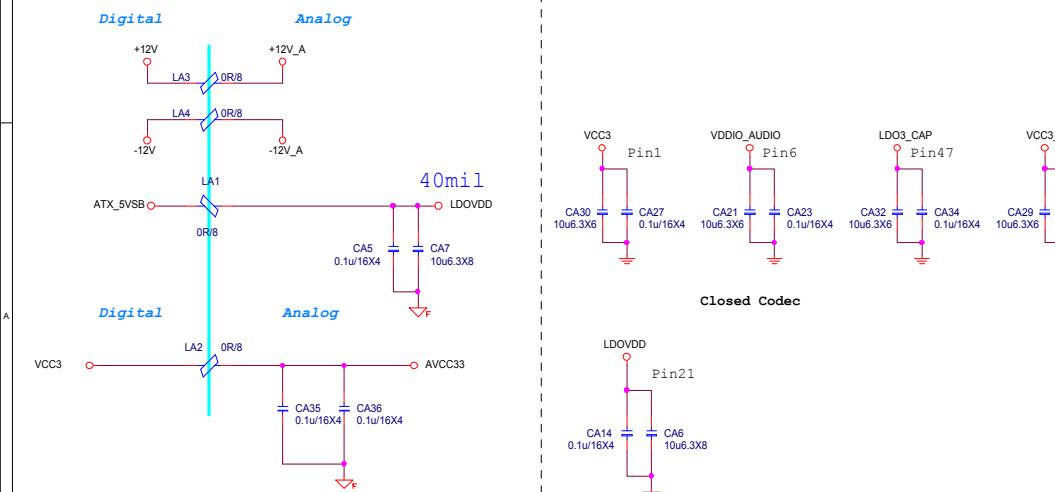
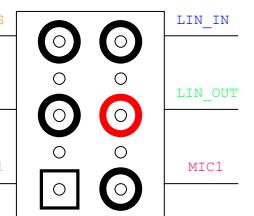
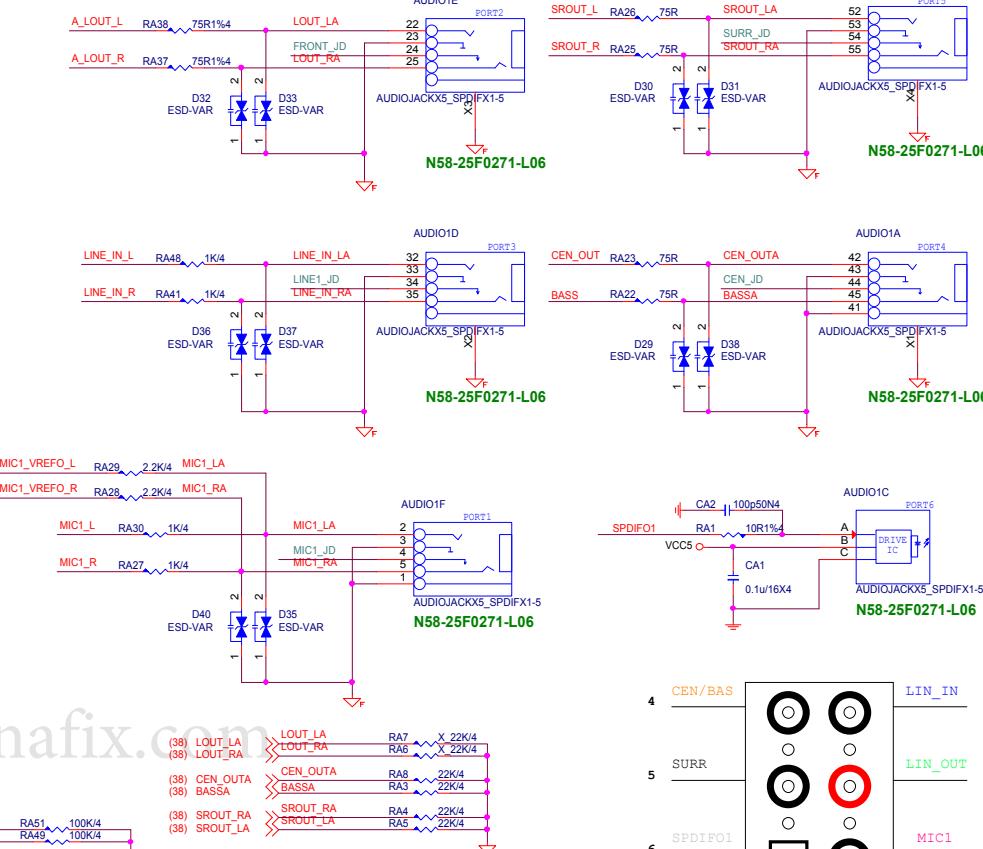
MS-7B

Size Document Description Rev
 Custom **LAN - I211AT** 11
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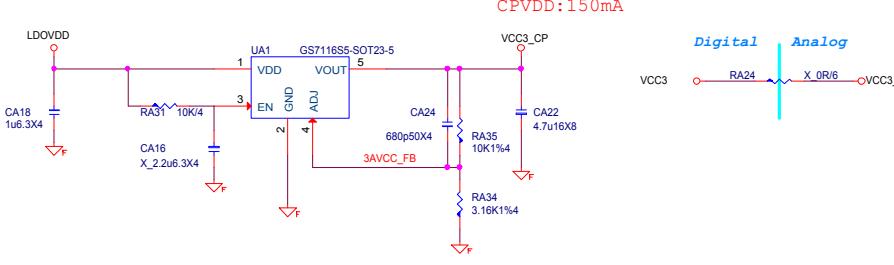
ALC1220P-VB1_48PIN



<https://vinafix.com>



CPVDD POWER: ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V

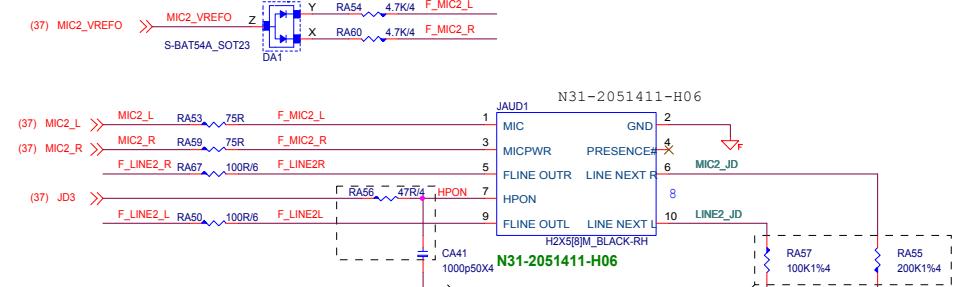
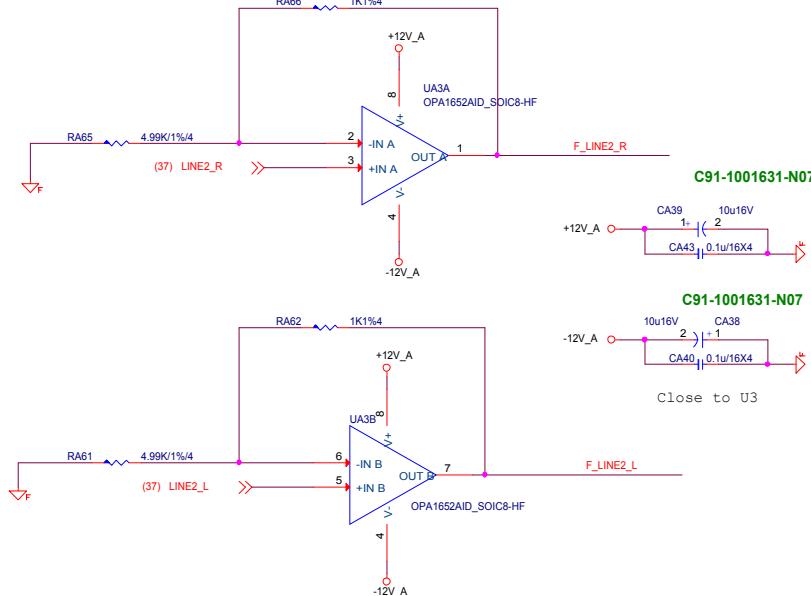


MICRO-STAR INT'L CO., LTD.

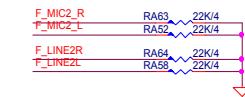
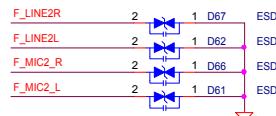
MS-7B78

Event Description

22-2010

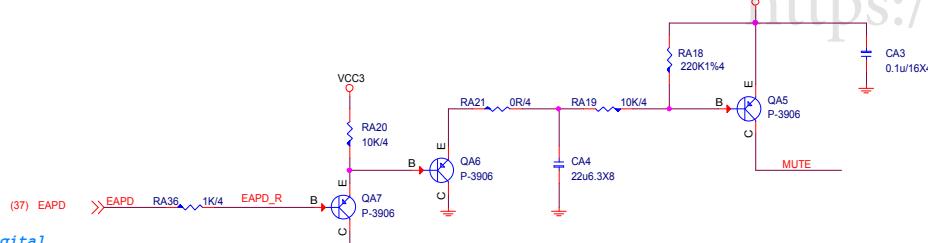


Close to Jack
ESD protect

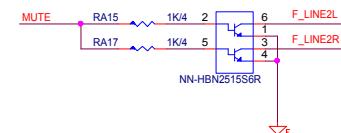
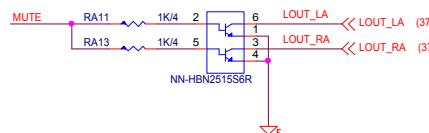


Rear Line OUT De-POP circuit (De-pop circuit for Rear Line out & Front Headphone out)

<https://vinafix.com>

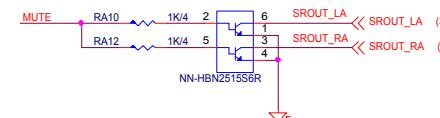
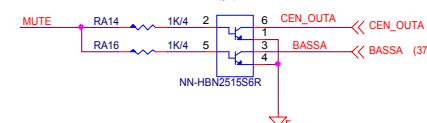


Analog

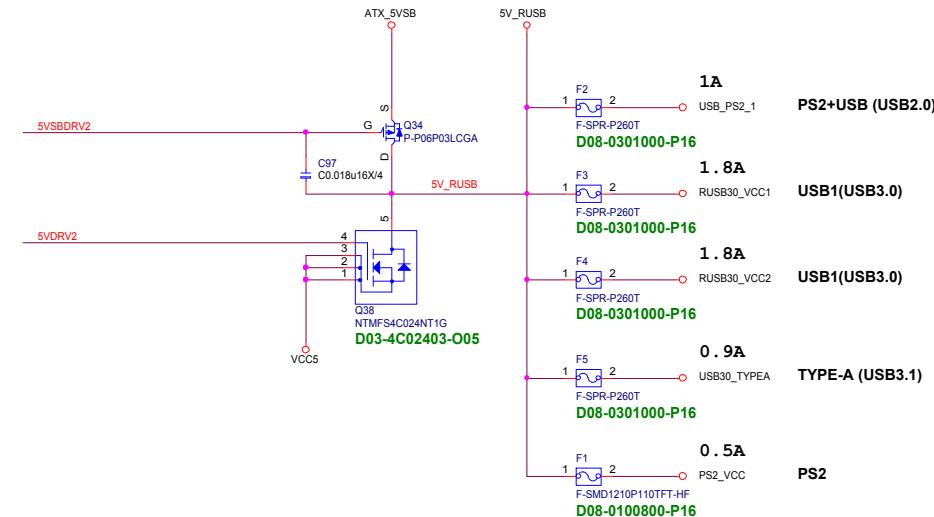
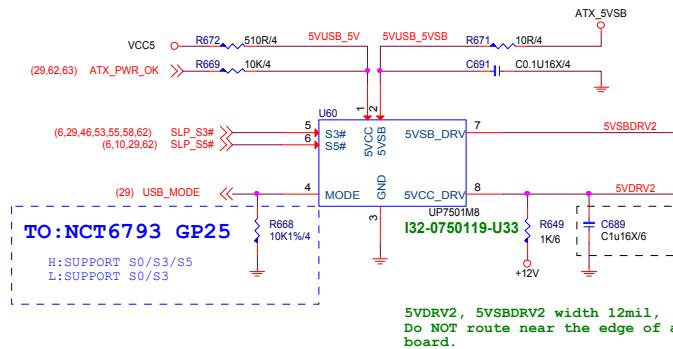


Audio moat is transparent and width 40mil

(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change SRROUT_LA, SRROUT_RA, CEN_OUTA, BASSA to TVS)



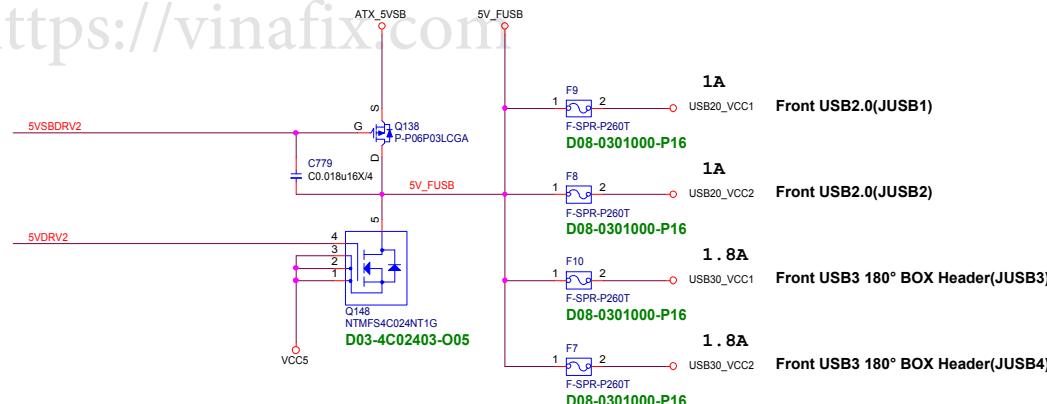
USB Power



Rear (5.1A)

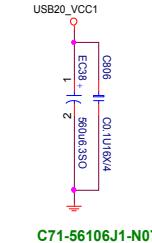
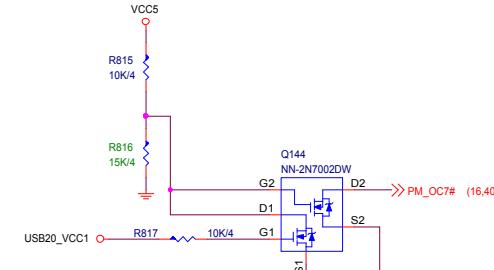
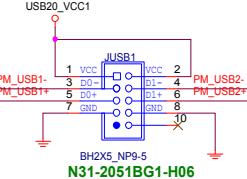
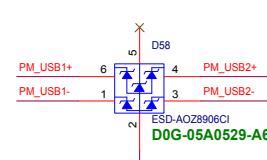
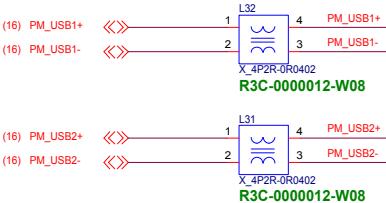
Front (5.6A)

<https://vinafix.com>



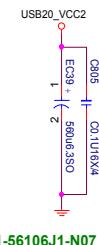
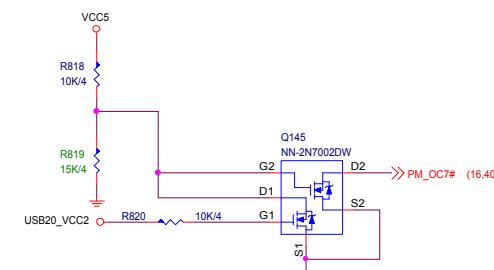
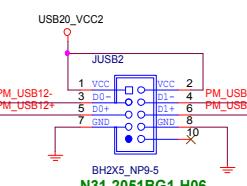
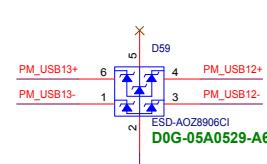
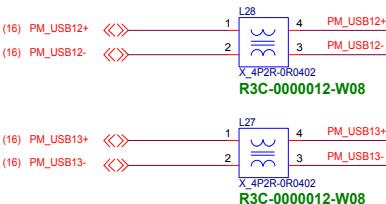
Front USB2.0 (JUSB1)

5V@1A



Front USB2.0 (JUSB2)

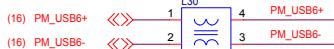
5V@1A



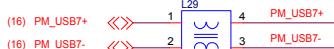
<https://vinafix.com>

Front USB3 180° BOX Header(JUSB3)

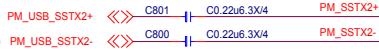
5V@1.8A



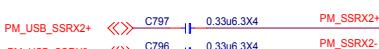
R3C-0000012-W08



R3C-0000012-W08



PM_SSTX2+



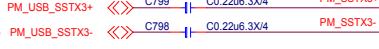
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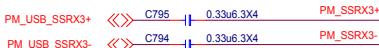
PM_SS RX2+



PM_SS RX2-



PM_SSTX3+



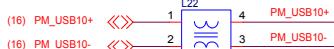
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PM_SS RX3+



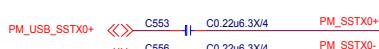
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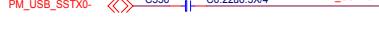
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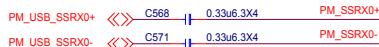
R3C-0000012-W08



PM_SSTX0+



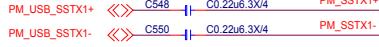
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PM_SS RX0+



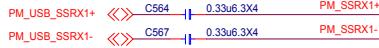
PM_SS RX0-



PM_SSTX1+



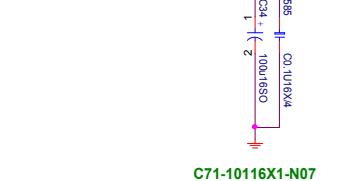
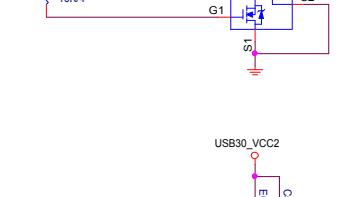
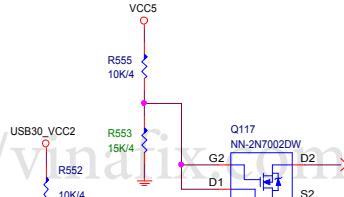
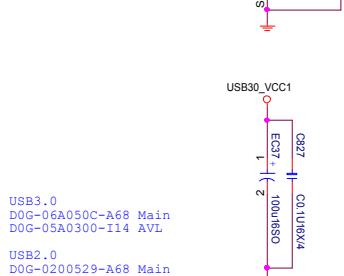
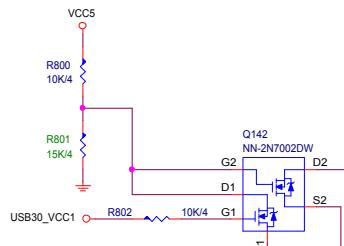
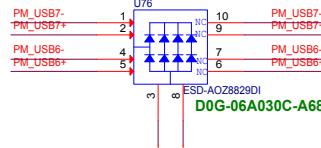
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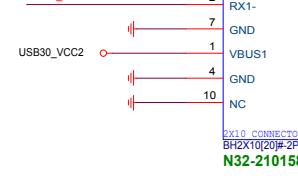
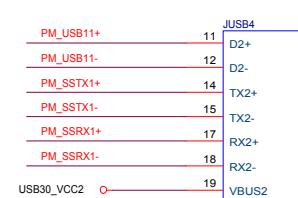
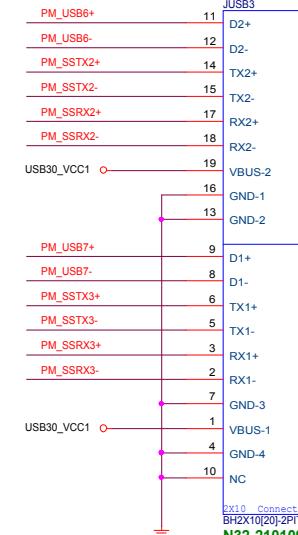
PM_SS RX1+



PM_SS RX1-



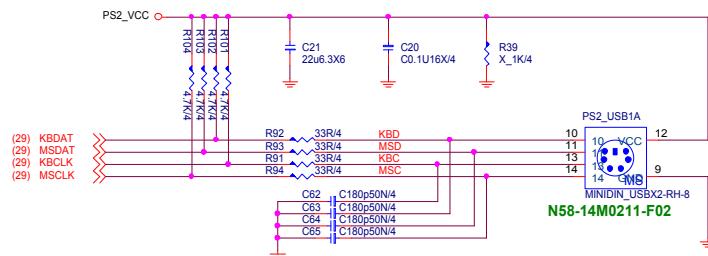
C71-10116X1-N07



C71-10116X1-N07

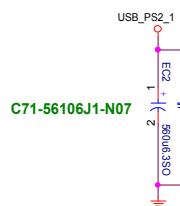
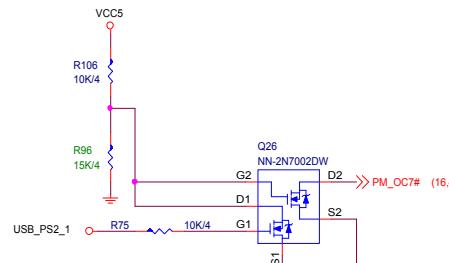
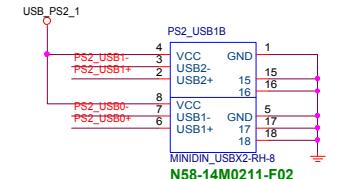
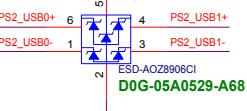
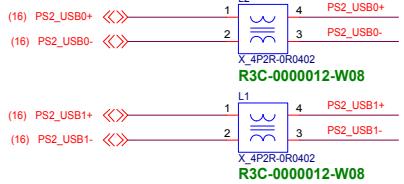
PS2+USB (USB2.0)

5V@1A

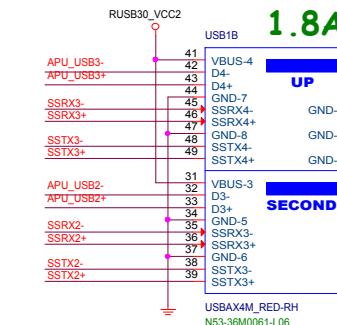
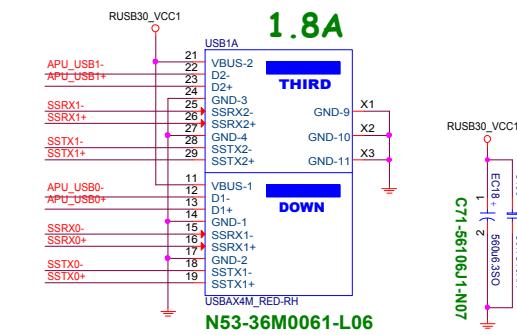
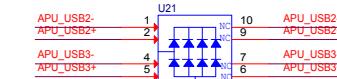
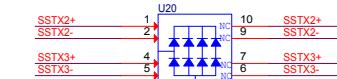
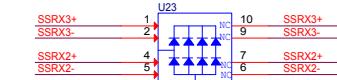
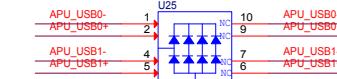
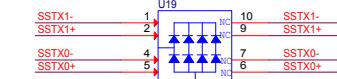
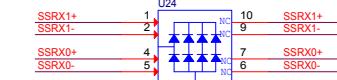
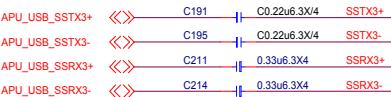
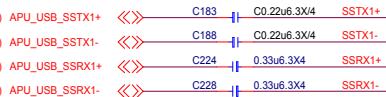
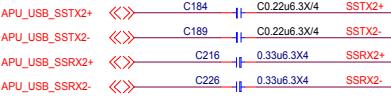
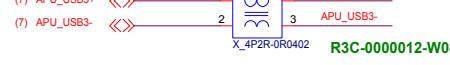
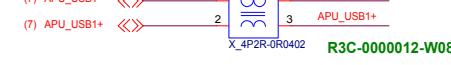
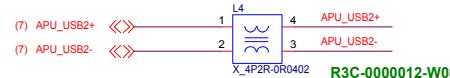
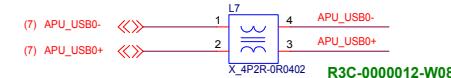


layout note:
C21 must close to TVS pin5
TVS must near KB MSI connector and route without branch
Varistor must close to TVS and route without branch

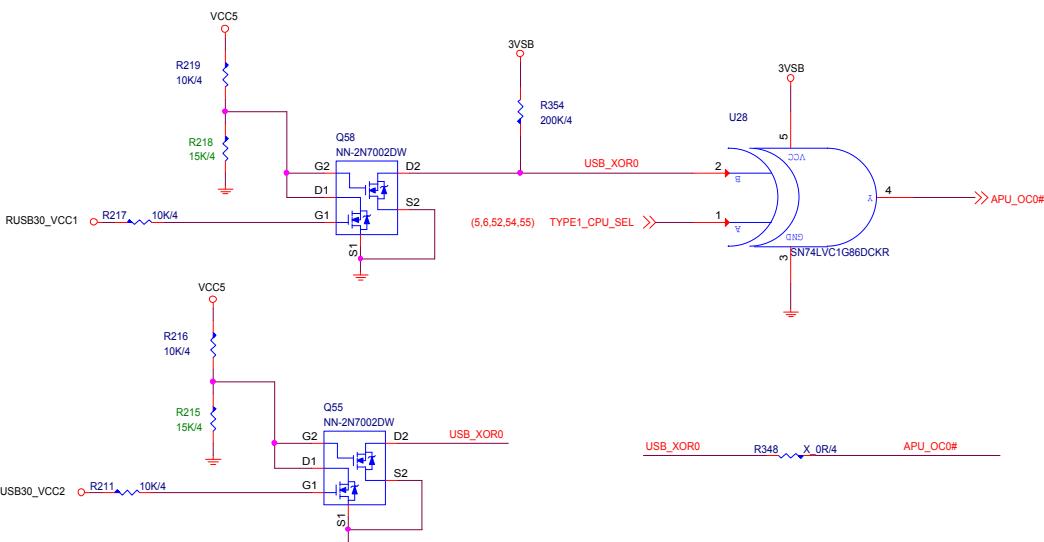
av1:D0G-45B0510-I14



Rear USB3.0 GEN1



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	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0



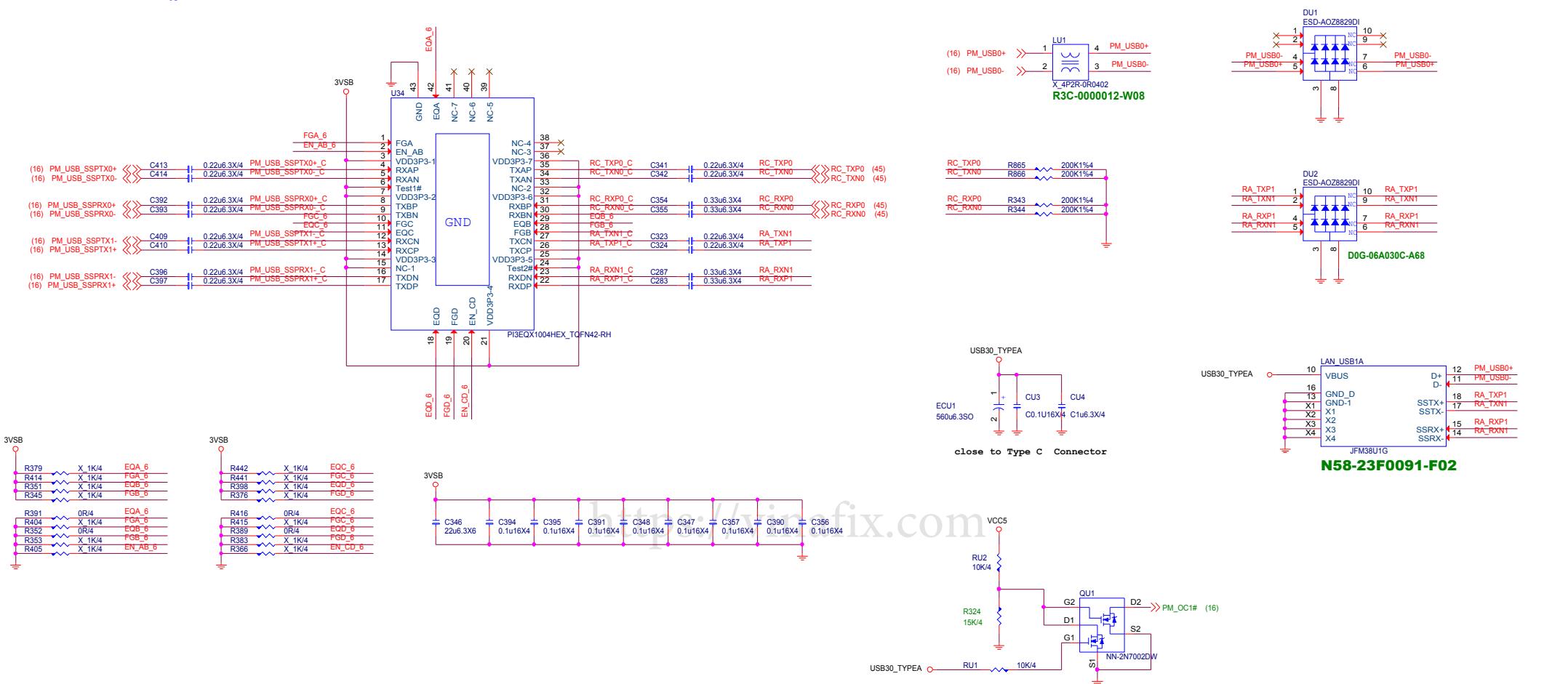
MICRO-STAR INT'L CO., LTD.

MS-7

Document Description

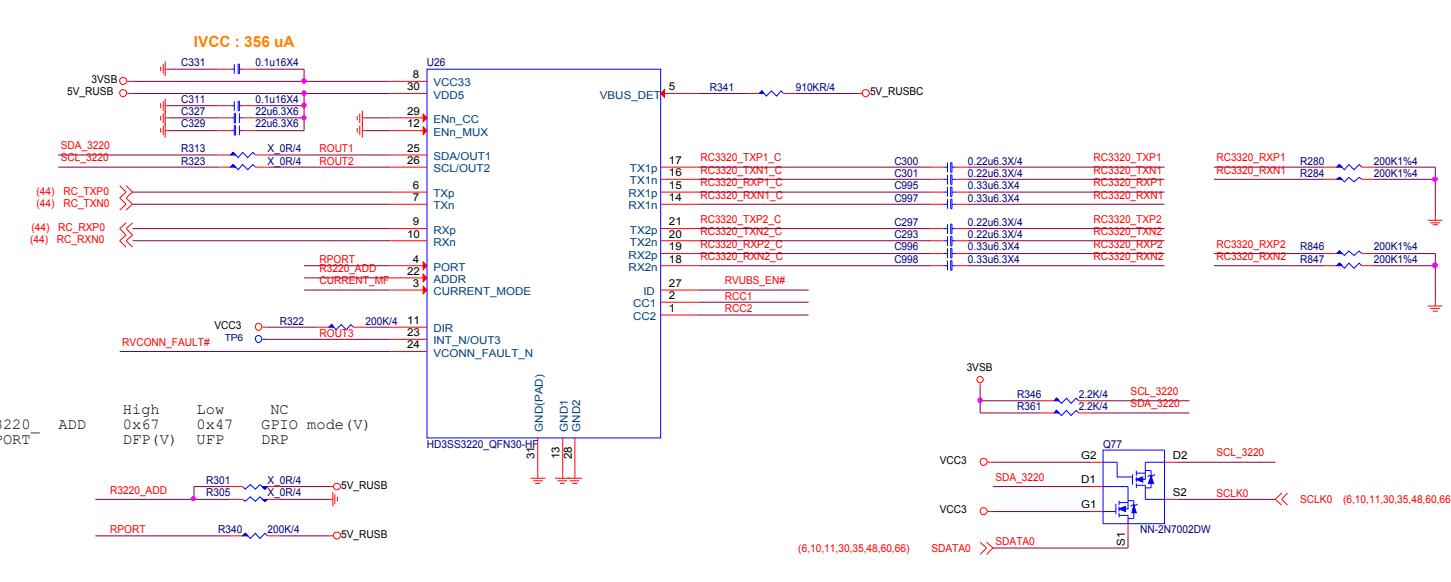
Rear_USB3.0 * 4

TYPE-A PI3EQX1004 Redriver

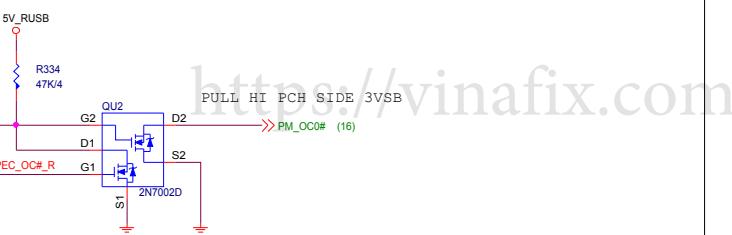


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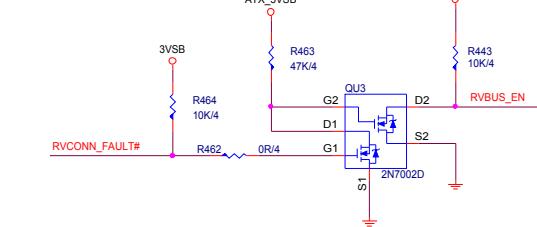
USB 3.1-Type-C USB Type-C MUX with Configuration Channel (CC)



VBUS OC# LEVEL SHIFT

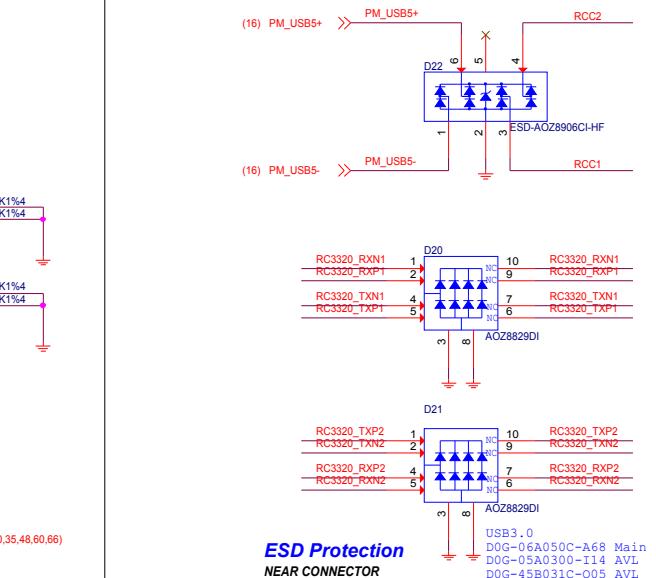
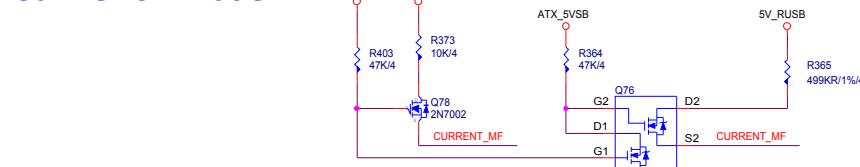


VCOM OC#

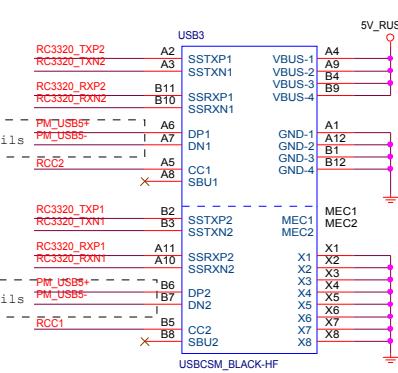


The circuit diagram illustrates the logic level conversion and enable signal generation for the VBUS_EN pin. The 3VSB input is converted to 5V_RUSB through a resistor (R418) and a diode (D06). This signal, along with the microcontroller's EN# output, is fed into the CTP1 optoisolator. The optoisolator's output is connected to the VIN pin of the RT9742AGJ5F driver IC. The IC also receives the RVBUS_EN signal from the microcontroller's FLG pin. The driver's EN pin is connected to the X_0.01u16X4 signal. The driver's output (OUT) is connected to the RU3 10k4 pull-up resistor, which connects to the 5V_RUSB line. The driver's GND pin is connected to the microcontroller's GND pin. The microcontroller's GND pin is also connected to the 5V_RUSBC pin. The microcontroller's OUT pin is connected to the EC24 560u6.3SO relay driver. The relay driver's coil is connected to the 3VSB line through a diode (D06) and a 2N7002 MOSFET. The relay driver's output is connected to the 5V_RUSBC pin. The microcontroller's GND pin is also connected to the 5V_RUSBC pin.

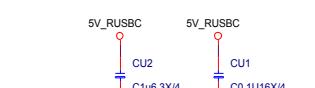
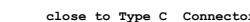
Current Mode



ESD Protection
NEAR CONNECTOR



N53-24M0040-L06



0180.0X4 00.1



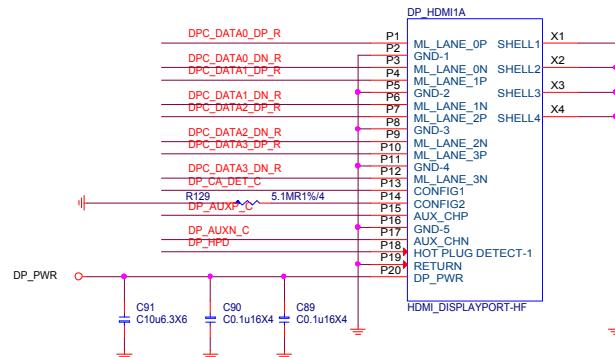
MICRO-STAR INT'L CO., LTD.

MS-7B7

Document Description
Rear USB3.1 Type C / mux

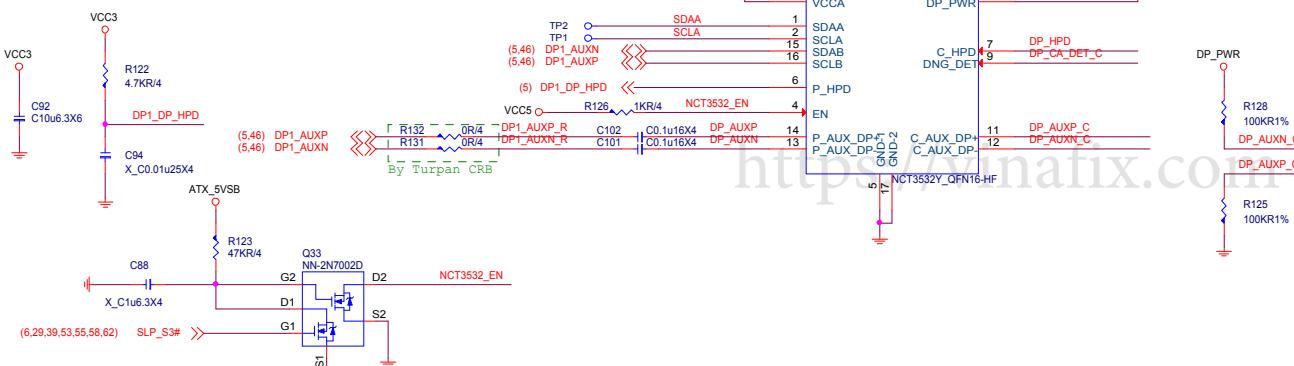
DP CONNECTOR

(5) DP1_TX0P_APU C104 C0.1u16X4 DPC_DATA0_DP_R
 (5) DP1_TX0N_APU C103 C0.1u16X4 DPC_DATA0_DN_R
 (5) DP1_TX1N_APU C106 C0.1u16X4 DPC_DATA1_DN_R
 (5) DP1_TX1P_APU C105 C0.1u16X4 DPC_DATA1_DP_R
 (5) DP1_TX2N_APU C96 C0.1u16X4 DPC_DATA2_DN_R
 (5) DP1_TX2P_APU C100 C0.1u16X4 DPC_DATA2_DP_R
 (5) DP1_TX3N_APU C109 C0.1u16X4 DPC_DATA3_DN_R
 (5) DP1_TX3P_APU C107 C0.1u16X4 DPC_DATA3_DP_R

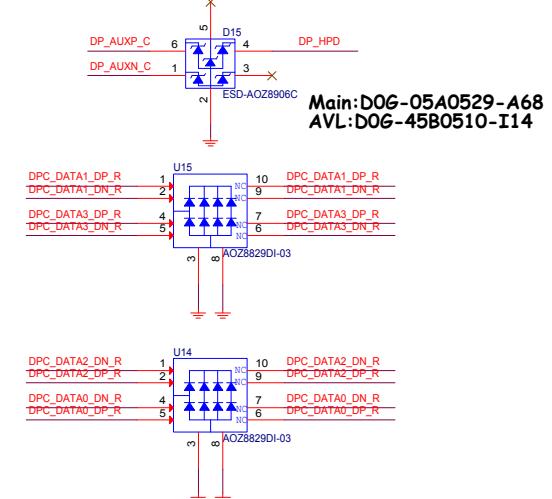


DP AUX & HPD Circuit

Support HDMI Dongle



ESD



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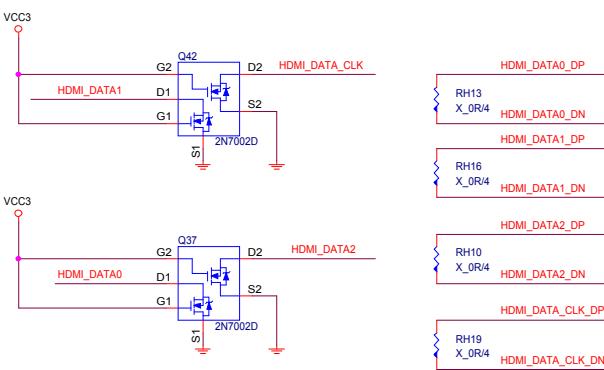
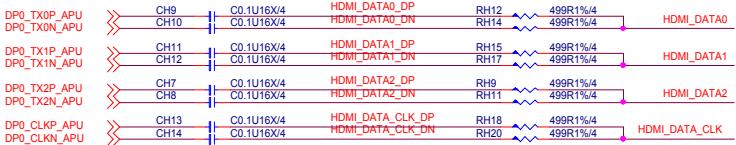
MS-7B78

Size	Document Description	Rev
Custom	DP	11

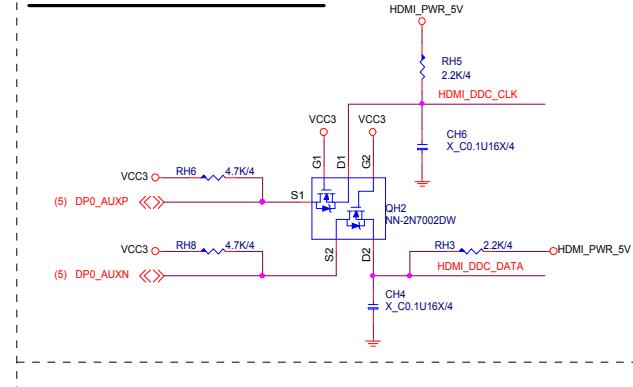
Date: Monday, February 26, 2018

HDMI CONNECTOR

For HDMI 1.4

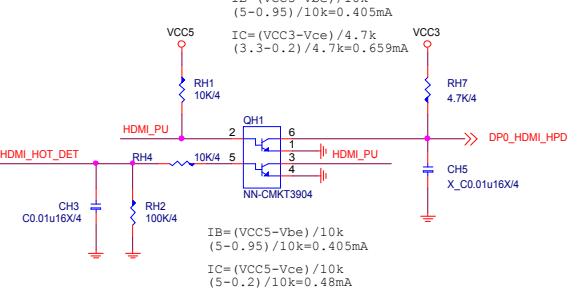


AUX Level Shifter



Connector

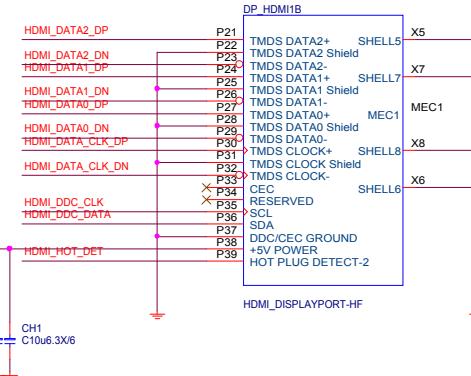
HPD Circuit



Connector Power

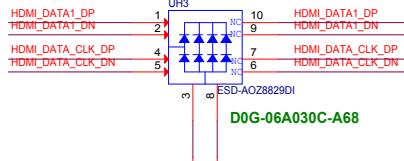
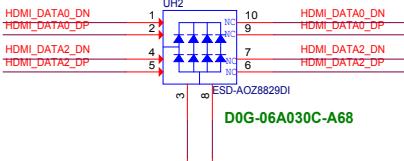


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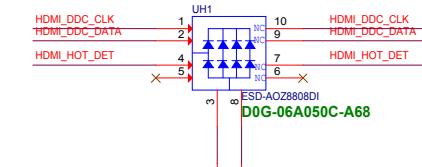


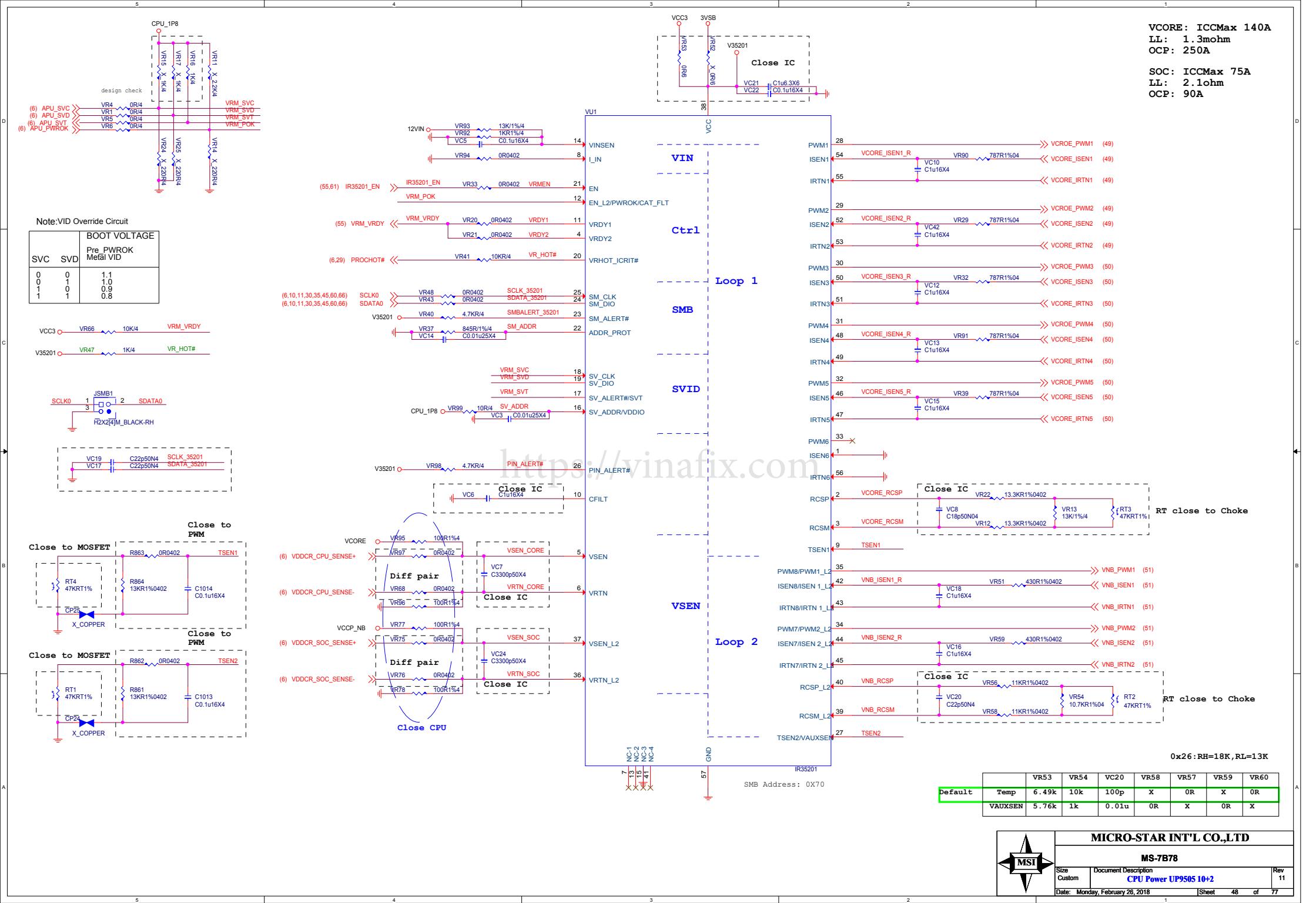
teknisi indonesia

For EMI

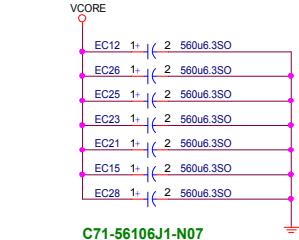
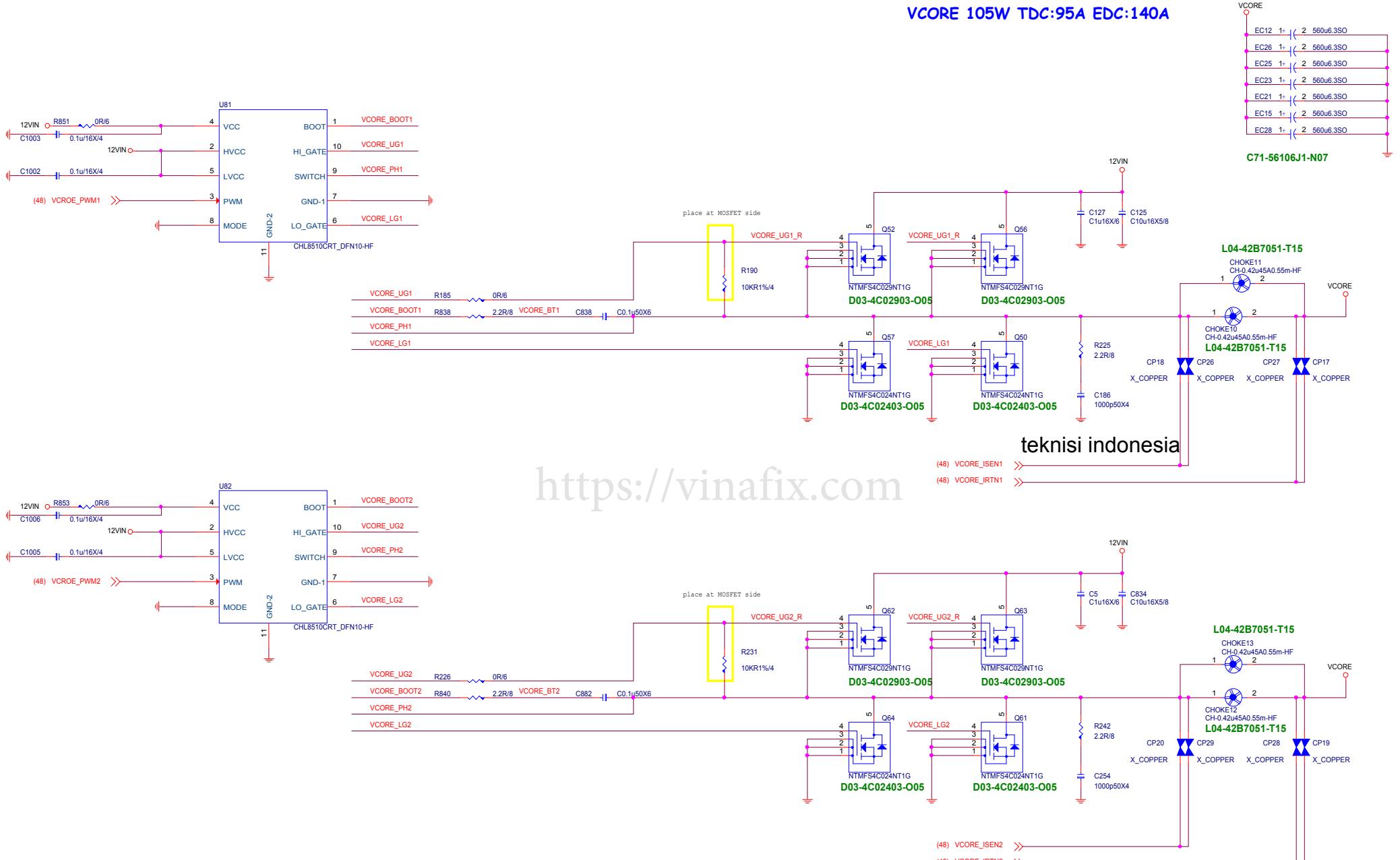


注意:耐壓5v零件



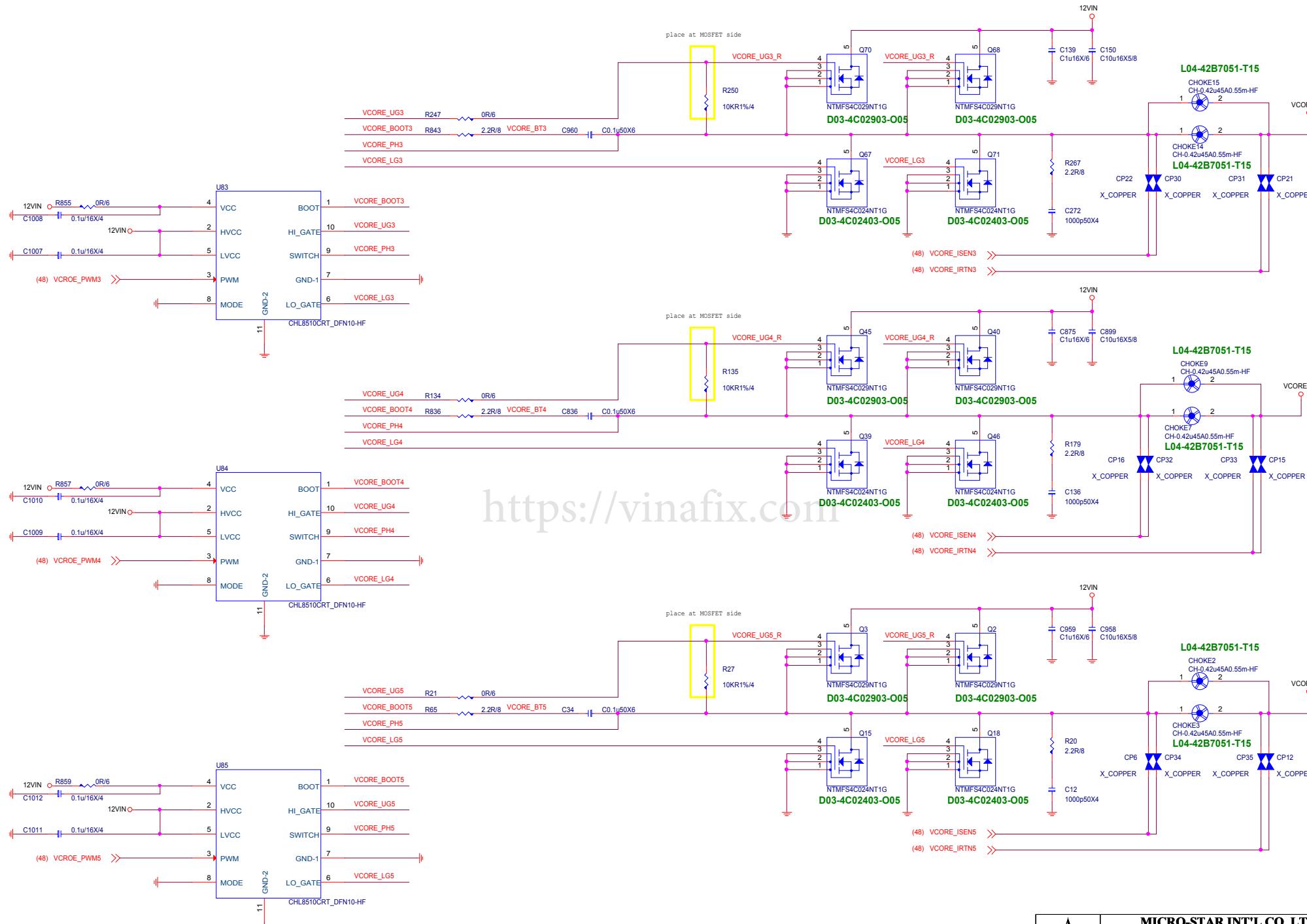


VCORE 105W TDC:95A EDC:140A



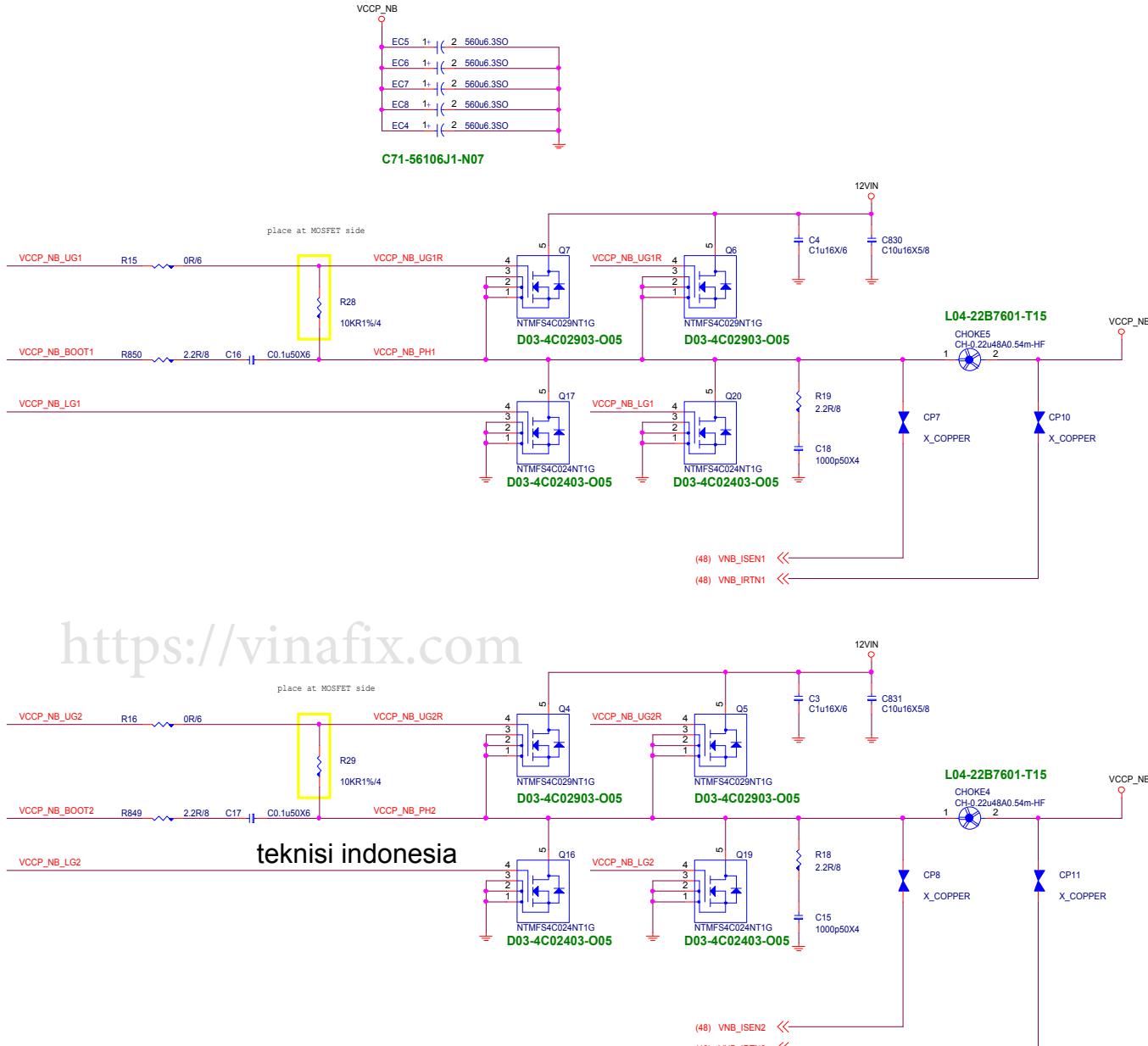
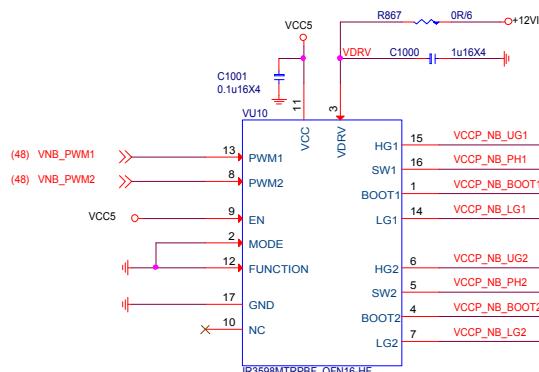
MICRO-STAR INT'L CO., LTD	
MS-7B78	
Size Custom	Document Description CPU Power Phase 1 - 4
Date: Monday, February 26, 2018	Rev 11

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VCCP_NB 105W TDC:50A EDC:75A

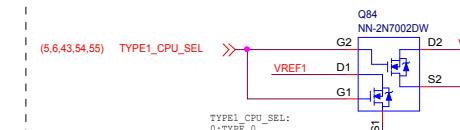
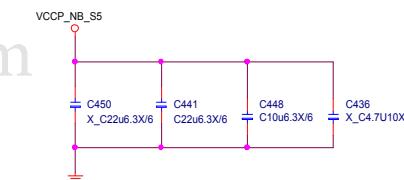
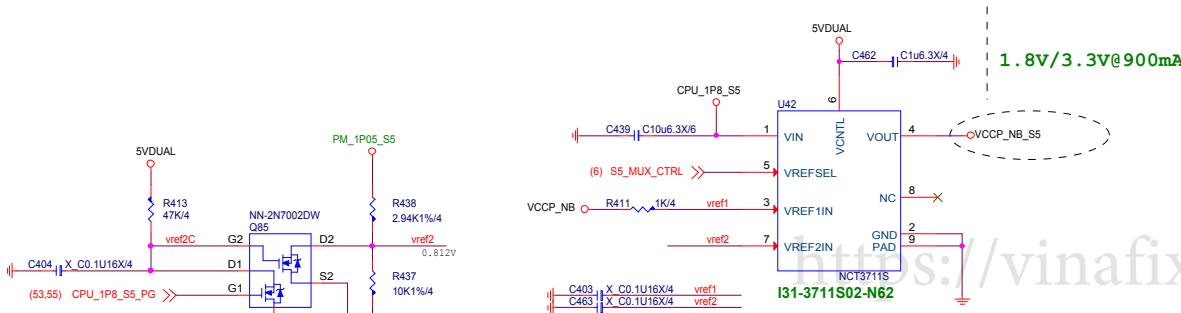
Table for IR3598			
Function	Mode	PWM Mode	Phase Mode
0	1	IR ATL	Dual
1	1	IR ATL	Doubler
0	0	Tri-State	Dual
1	0	Tri-State	Doubler



S5_MUX_CTRL
HIGH: S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V), VDDCR_SOC_S5 = 0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)



CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	X	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0



MICRO-STAR INT'L CO., LTD

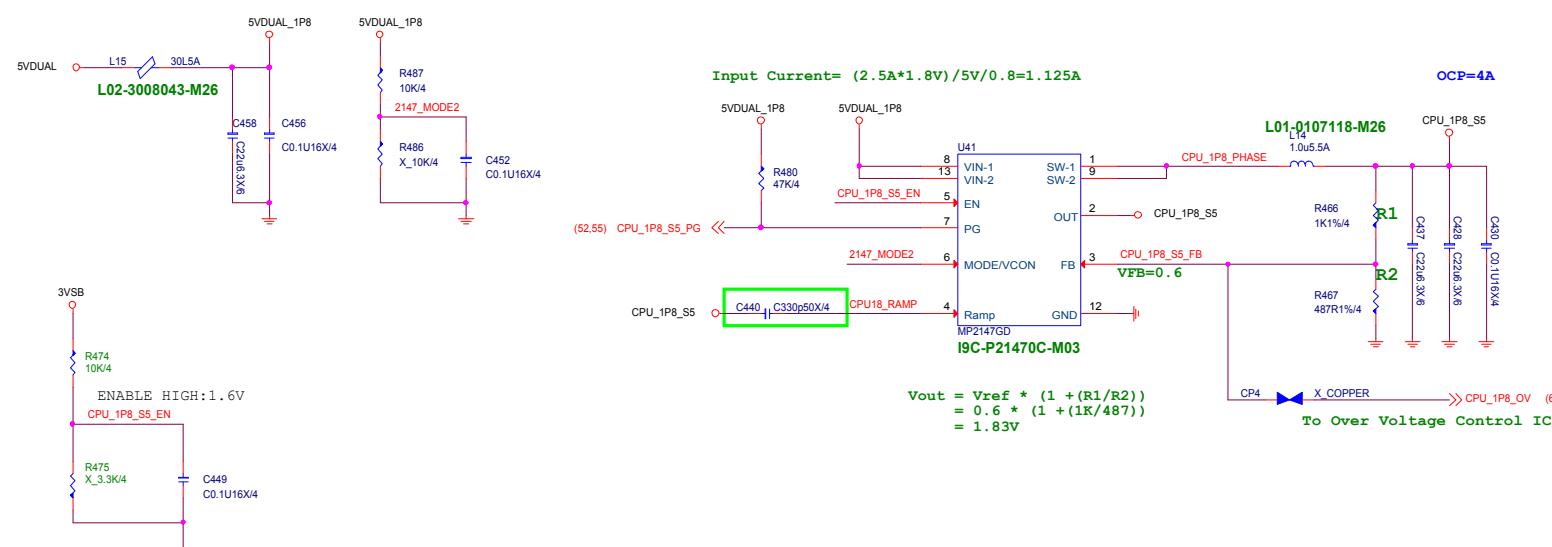
MS-7B78

Size	Document Description	Rev
Custom	CPU Power NB_S5	11

Date: Monday, February 26, 2018 | Sheet 52 of 77

CPU 1.8V S5 @0.5A

1.8V S5@0.5A

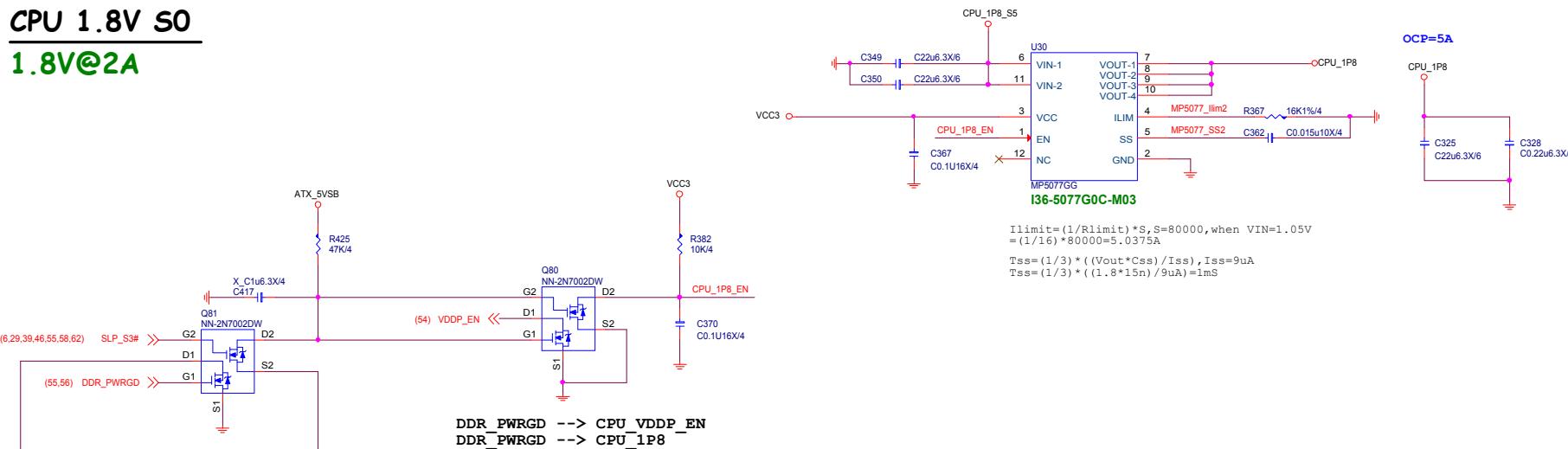


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CPU 1.8V S0

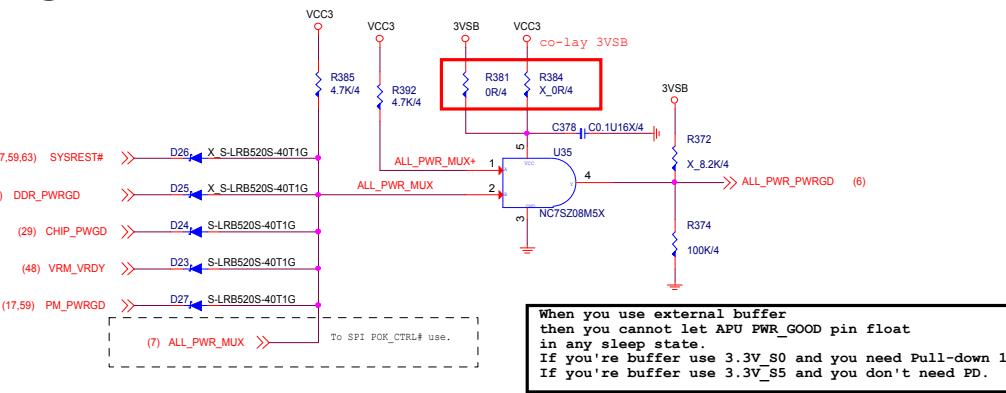
1.8V@2A



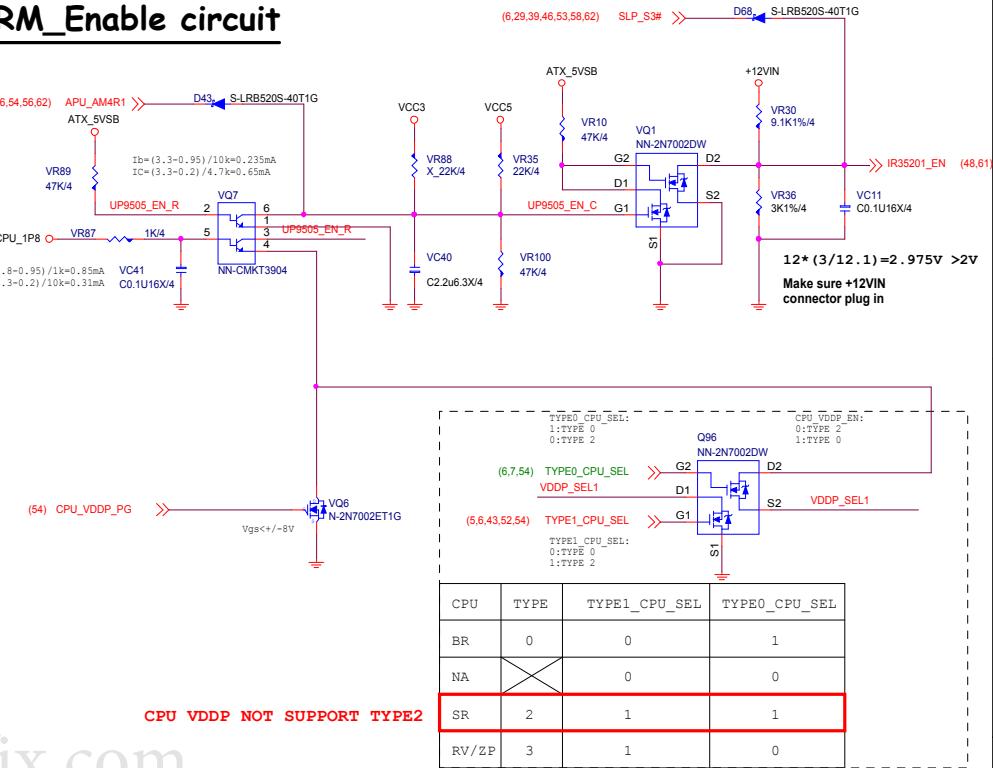
MICRO-STAR INT'L CO., LTD		
MS-7B78		
Size Custom	Document Description CPU Power 1.8_S0 / S5	Rev 11
Date: Monday, February 26, 2018		

ALL POWER GOOD MUX

S0 PG

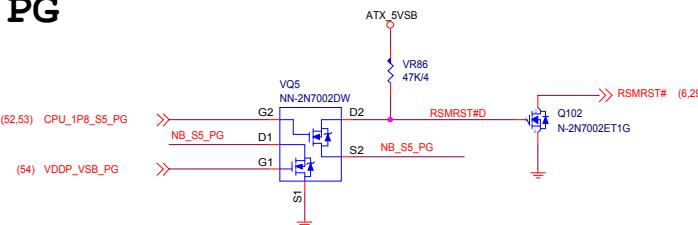


VRM_Enable circuit



<https://vinafix.com>

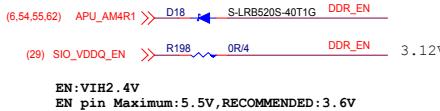
S5 PG



DDR4_1.2V@26.2A

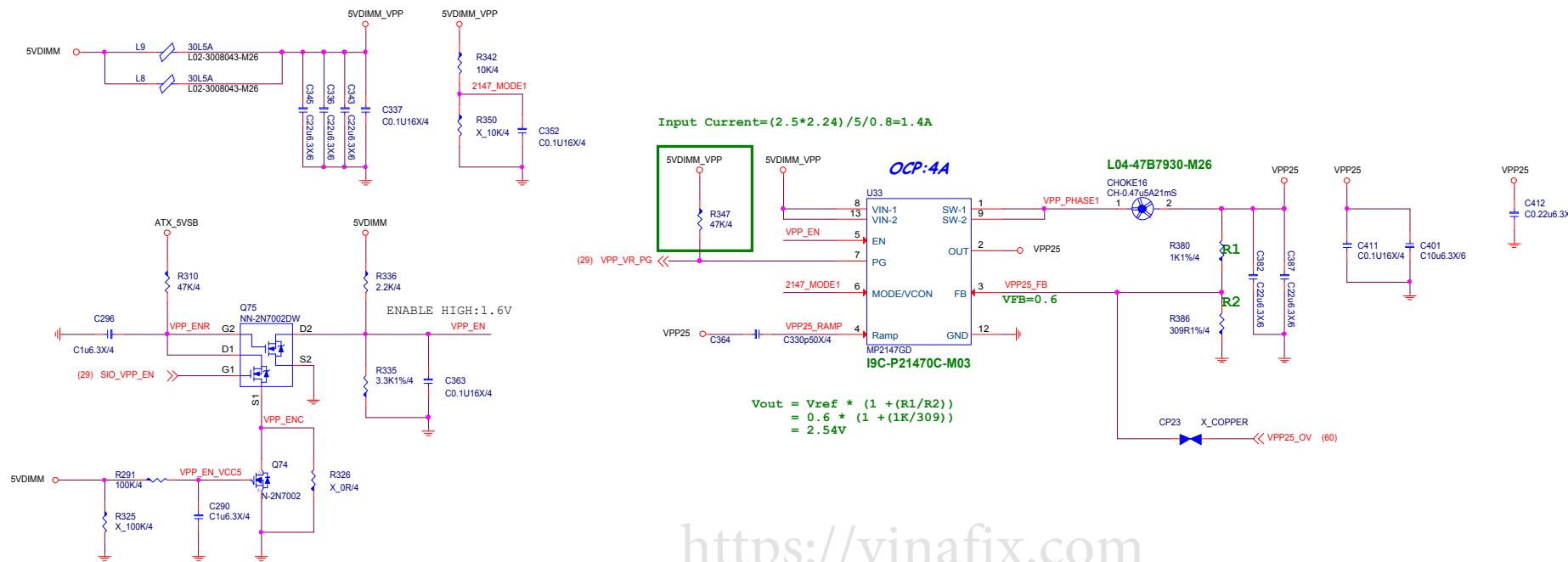
**15.5A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT**

**Rocset:4.32K
OCP=Rocset*Rdson (Low side) /10uA
=8.2K*10uA/4mohm
=20.5A**



4DIMM : VPP25

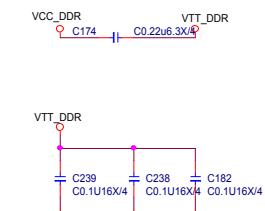
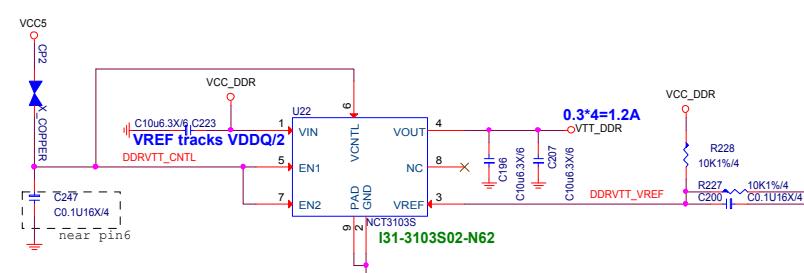
2.5V@2.24A



<https://vinafix.com>

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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	DDR VPP25 / VTT	

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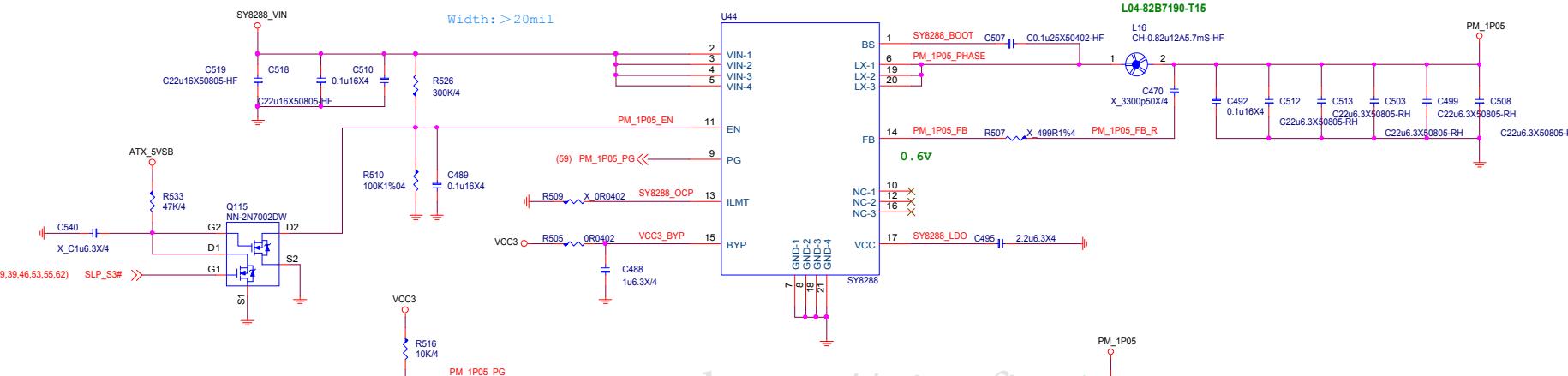
FOR Promontory 1.05V_S0

1.05V
S0: 5.5A
S5: 0.05A



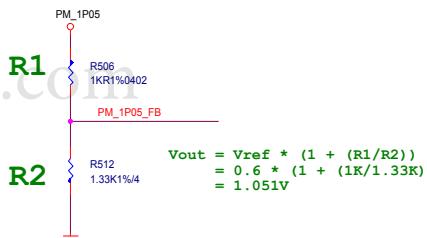
$$\text{Input Current} = (5.5\text{A} \times 1.05\text{V}) / 12\text{V} / 0.8 = 0.6\text{A}$$

OCP=12A
1.05V@5.5A



SY8288_OCP	OCP
0	8A
floating	12A
1	16A

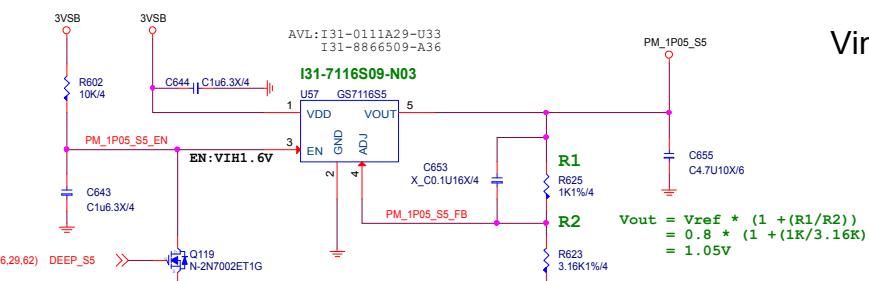
https://vinafix.com



$$\text{Vout} = \text{Vref} * (1 + (\text{R1}/\text{R2})) \\ = 0.6 * (1 + (1\text{K}/1.33\text{K})) \\ = 1.051\text{V}$$

FOR Promontory 1.05V_S5

1.05V@0.05A

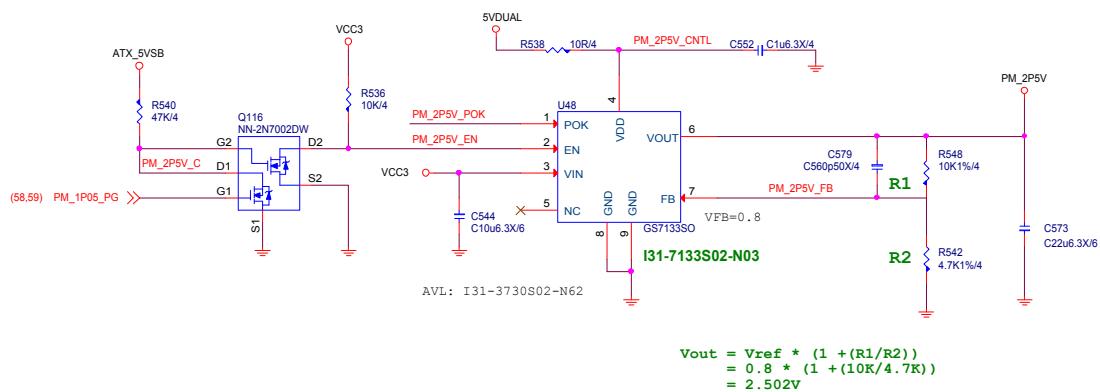


$$\text{Vout} = \text{Vref} * (1 + (\text{R1}/\text{R2})) \\ = 0.8 * (1 + (1\text{K}/3.16\text{K})) \\ = 1.05\text{V}$$

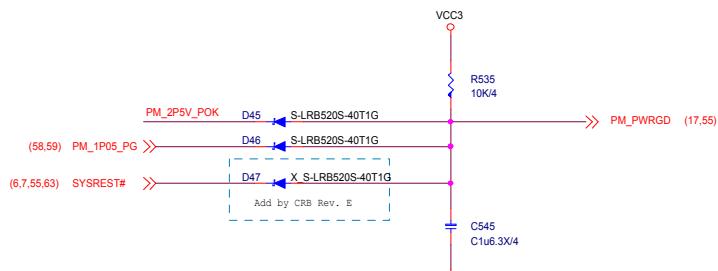
Vinfix.com

Promontory-2.5V

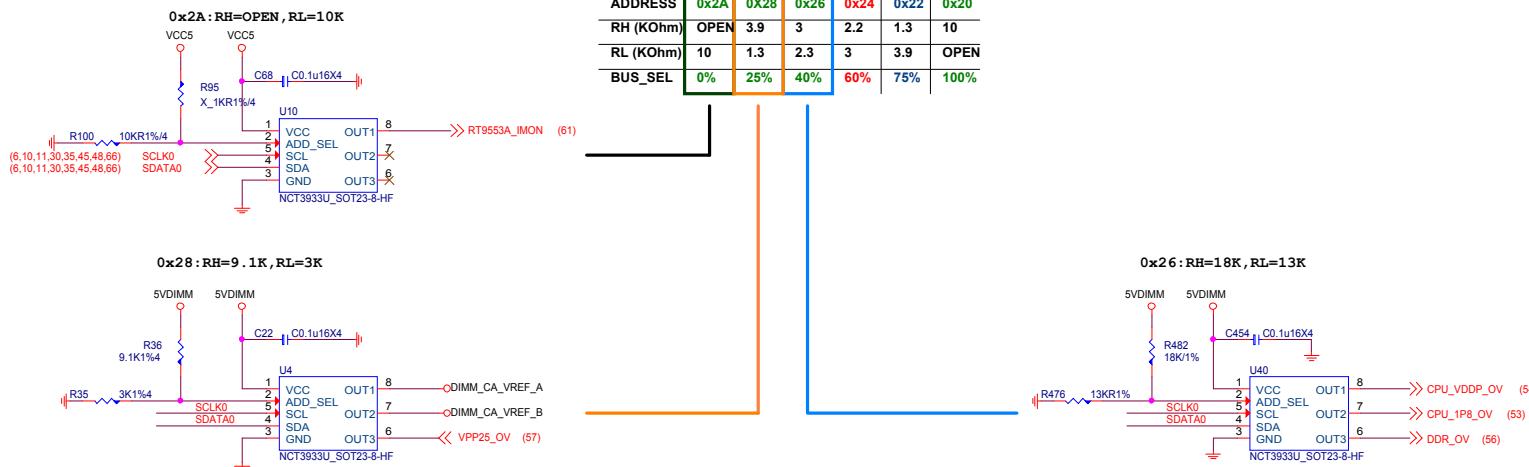
2.5V@900mA



<https://vinafix.com>



Over Voltage Control IC

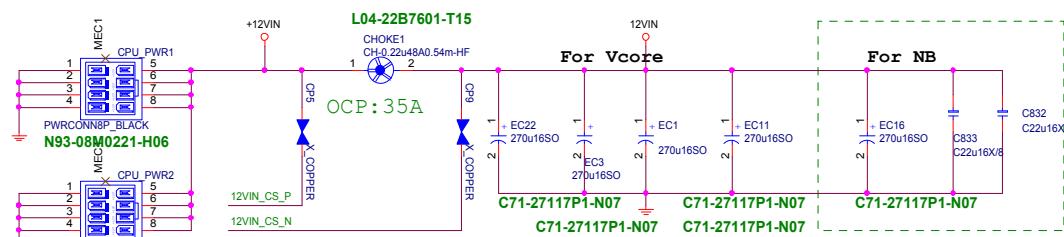


<https://vinafix.com>

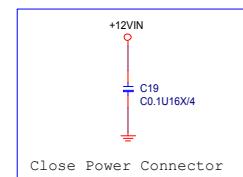
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

CPU POWER CONNECTOR

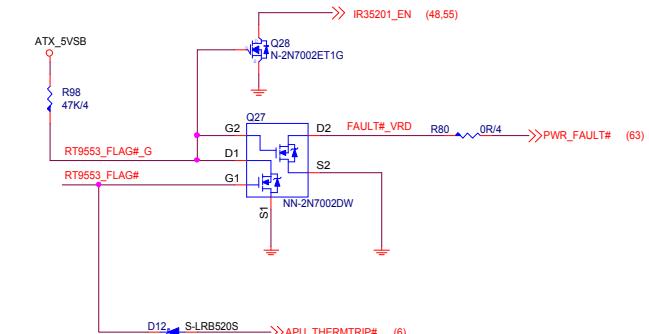
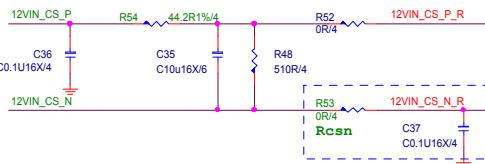
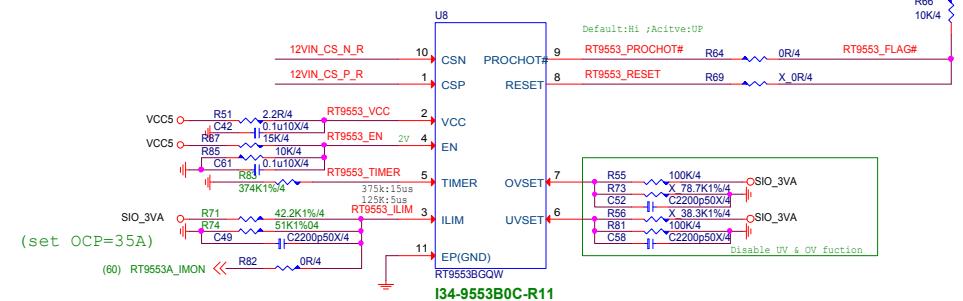


NB	D=Vout/Vin	VCCP	D=Vout/Vin
	Vin = 12 > input voltage		Vin = 12 > input voltage
	Vout = 1.4 > output Vcore		Vout = 1.4 > output Vcore
	D = 0.116667		D = 0.116667
	Io = Icore(max)*0.8		Io = Icore(max)*0.8
	I core(max) = 75 > Vcore current		I core(max) = 125 > Vcore current
	I avg. = 75 A		I avg. = 125 A
	I ripple = {Io*sqrt(D*(1-D))} / Phase		I ripple = {Io*sqrt(D*(1-D))} / Phase
	Phase = 2 phases		Phase = 4 phases
	I ripple = 12.03835 A		I ripple = 10.03196 A
How many pcs. Of Cap.			
1 ripple/cap	= 5000 m A	1 ripple/cap	= 5000 m A
COE _{cap}	= 1	COE _{cap}	= 1
Input Cap.	= 3 pcs.	Input Cap.	= 3 pcs.



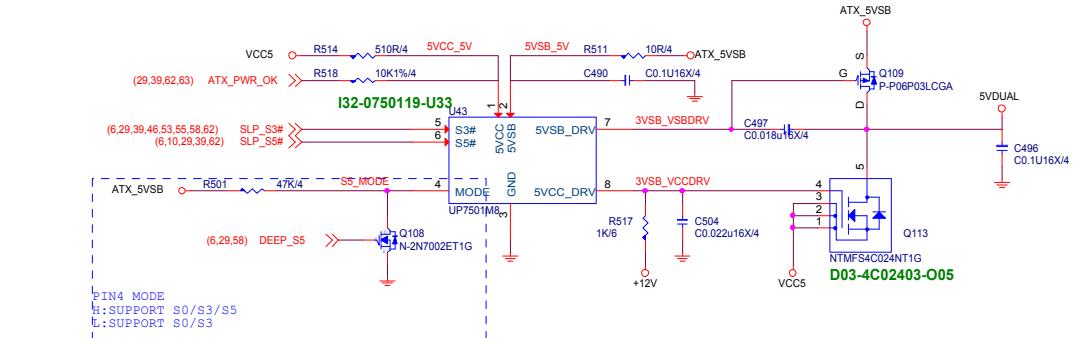
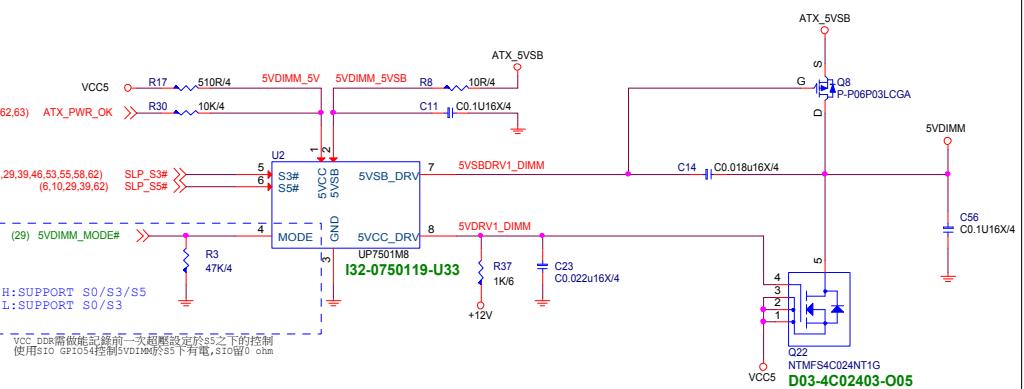
RT9553B CURRENT SENSE

RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.

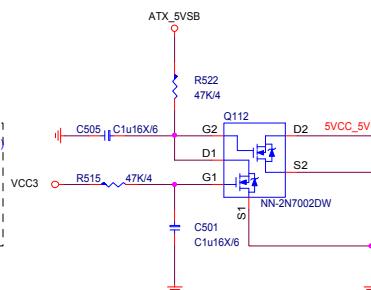


5VDUAL For 3VSB、CPU 1.8V 、 VDDP

5VDIMM FOR DDR



| For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
| The power supply VCC3 delay 12ms after VCC5 assert.
| The chip U7501 5VDRV1 work when the VCC5 ready
| (When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
| VCC3 not ready and let the 3VSB sequence fail.



3VSB cost down

3.3V@2.63A

1.05V@0.05A
VDBBT_RTC_G@4.5uA

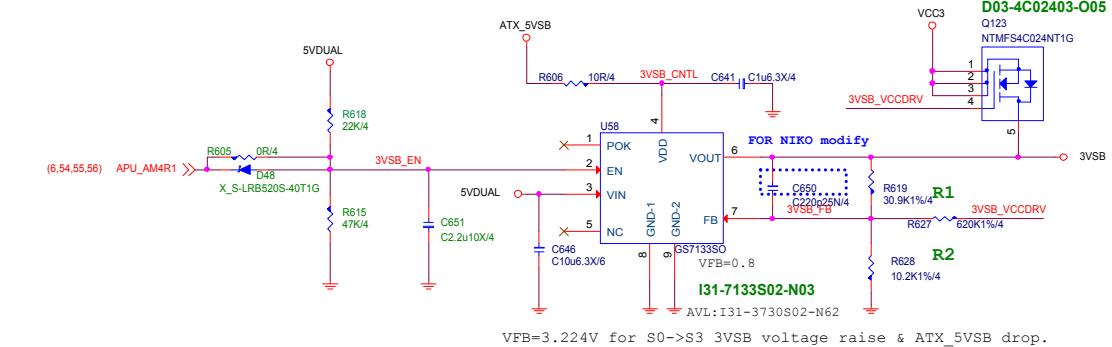
FCH@0.07A

CPU@0.25A

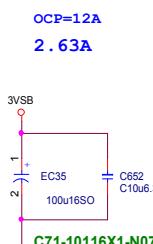
PCI @0.75A

PCIE*4 @1.5A

USB TYPE-C @0.9mA

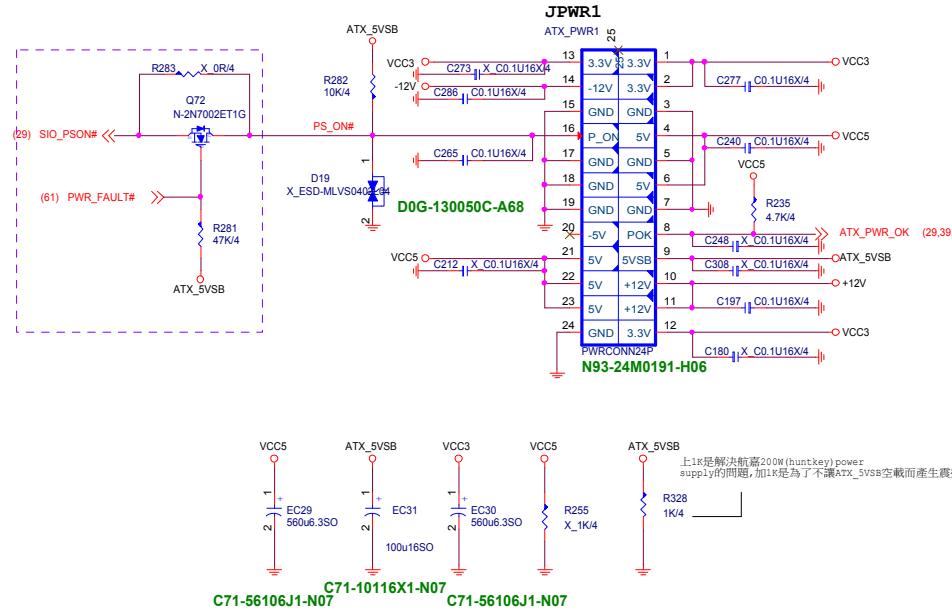


$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (30.9K/10.2K)) \\ &= 3.22V \end{aligned}$$

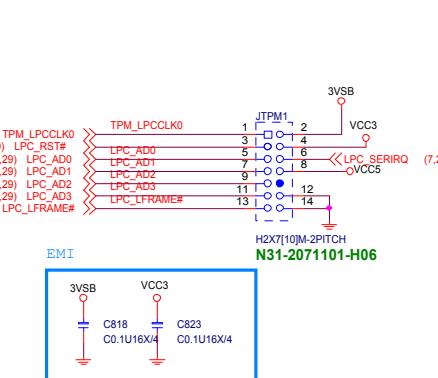


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Size Custom	Document Description ACPI - 5VDIMM / 3VSB	Rev 11	
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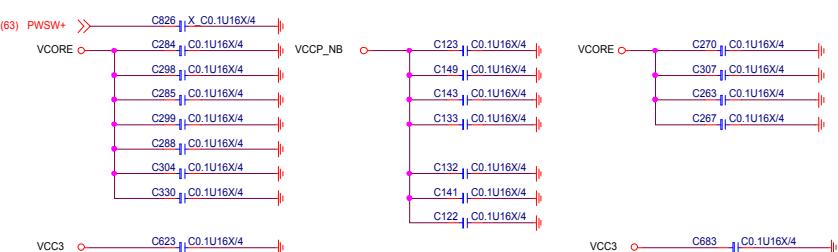
ATX POWER CONNECTOR



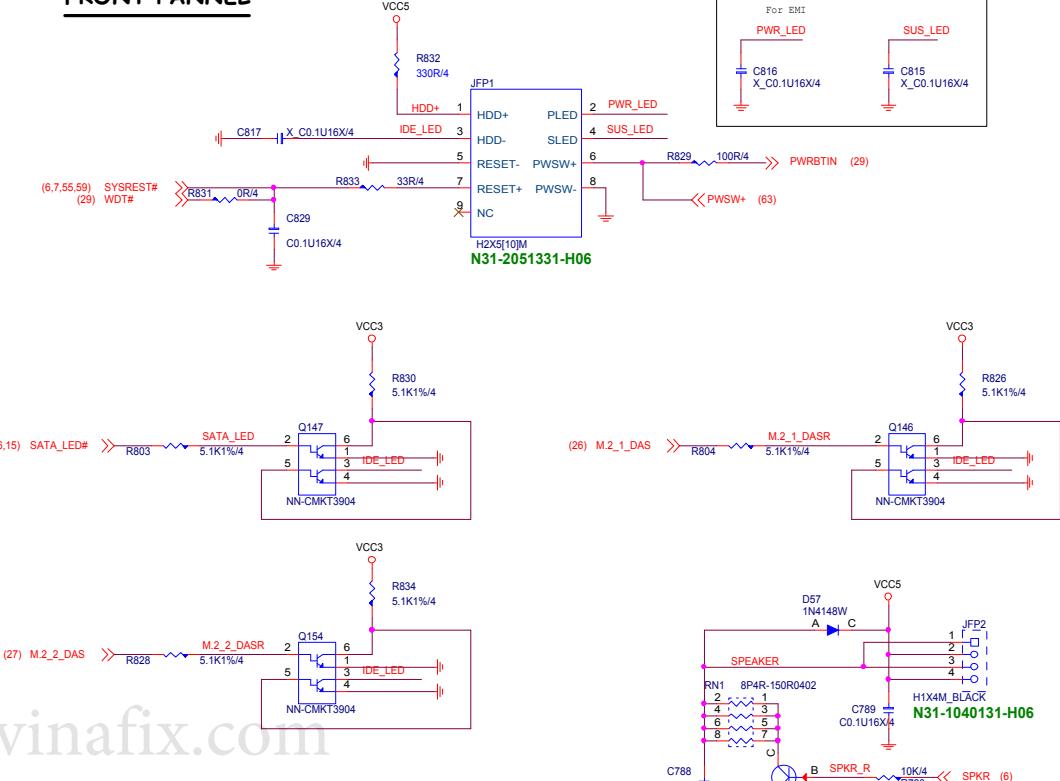
TPM



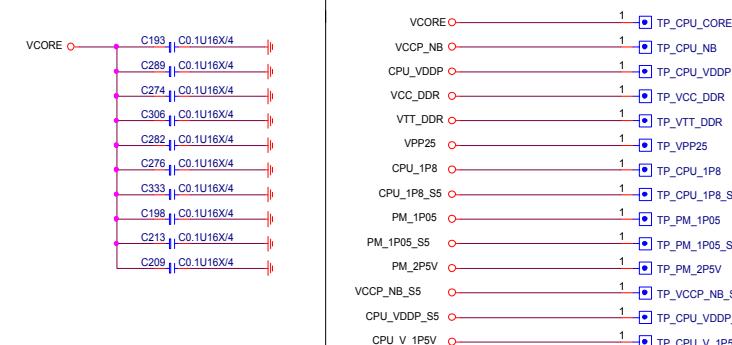
Add for EMI



FRONT PANNEL



Voltage Measure Point

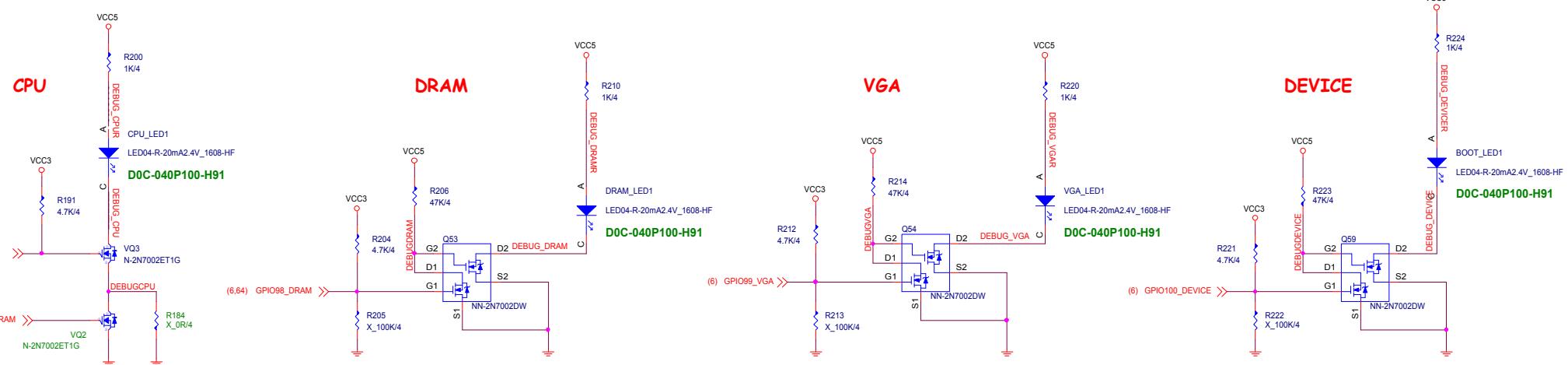


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MS-7B7

Document Description	Rev
ATX power - FrontPanel / EMI	11

EZ Debug LED

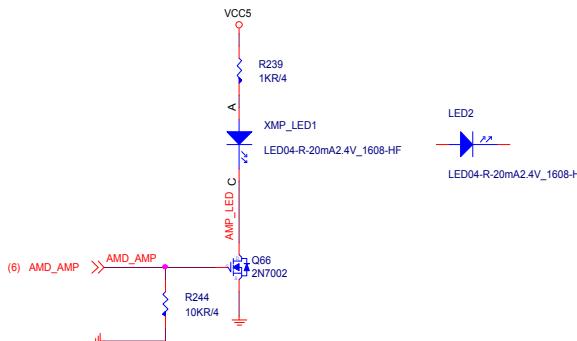


LED亮燈時同時將CPU LED關掉

LEDGPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	(GPO HIGH (default HIGH))	(GPO HIGH (default HIGH))	(GPO HIGH (default HIGH))

Vinifix.com

AMD AMP Detect LED



<https://vinifix.com>

DIMM_SLOT

FORM SIO

D0C-040P100-H91/D0C-040S500-E07

DIMMA1
DIMM_LED1
LED04-R-20mA2.4V_1608-HF
D0C-040P100-H91

SIO_PIN98

(29.65) SIO_MLED >> SIO_MLED
(13) DIMMA1_DET >> DIMMA1_DET

DIMMA1_PIN2

DIMMA2
DIMM_LED2
LED04-R-20mA2.4V_1608-HF
D0C-040P100-H91

(13) DIMMA2_DET >> DIMMA2_DET

DIMMA2_PIN2

DIMMB1
DIMM_LED3
LED04-R-20mA2.4V_1608-HF
D0C-040P100-H91

(14) DIMMB1_DET >> DIMMB1_DET

DIMMB1_PIN2

DIMMB2
DIMM_LED4
LED04-R-20mA2.4V_1608-HF
D0C-040P100-H91

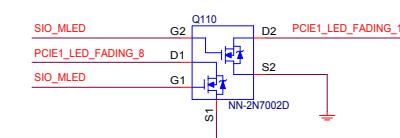
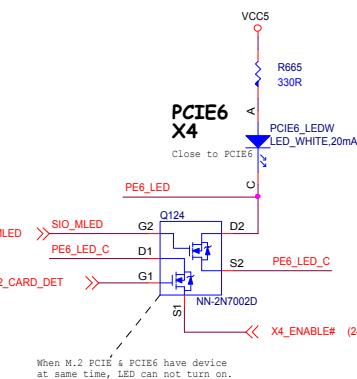
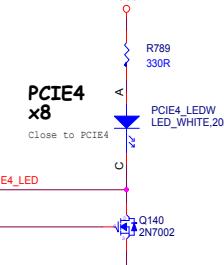
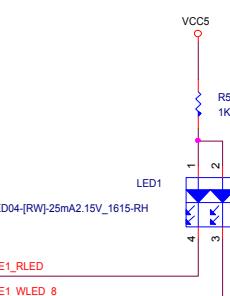
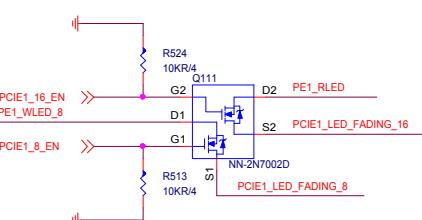
(14) DIMMB2_DET >> DIMMB2_DET

DIMMB2_PIN2

PCIE_SLOT LED

FORM SIO

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1

Sheet

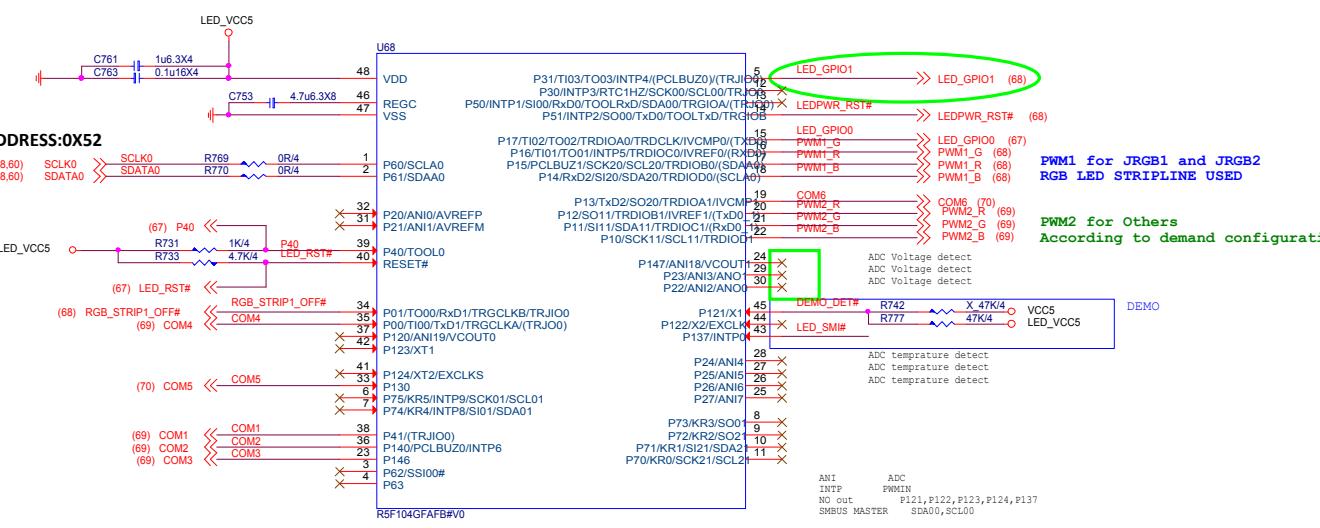
65

of

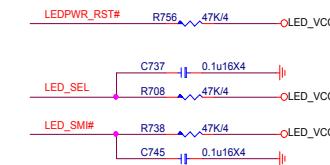
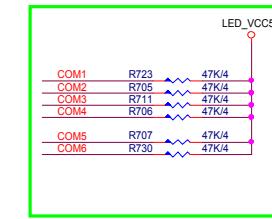
77

48 PIN LED MCU

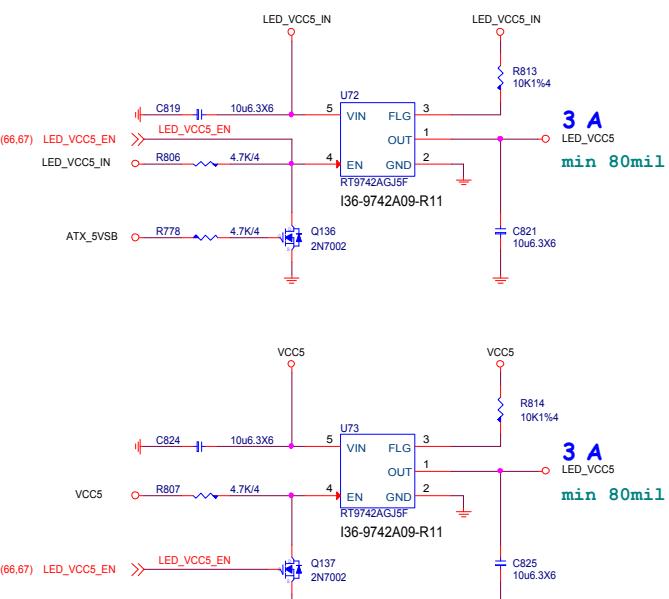
C345 & C359 near VDD Pin.



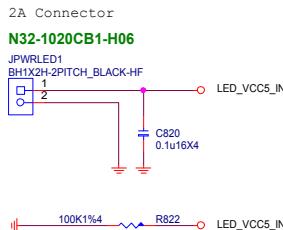
Control	Net Name	PWM USE	Connector
PCH	LED_GPIO1	No Use	JPIPE_LED2
Audio	COM1~4	PWM2	RGB LED
Board Side LED	COM5~8	PWM2	RGB LED
LED STRIPLINE	RGB_STRIP1_OFF#	PWM1	JLED1
LED STRIPLINE	RGB_STRIP1_ON#	PWM1	JLED2
IO Cover	LED_GPIO0	No Use	JPIPE_LED1



EXTERNAL POWER INPUT



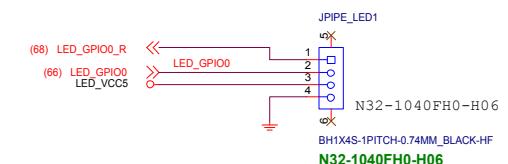
External Power



LED Demo Button

1 PCH HEATSINK LED
PCS LED*0.16W=W

2 AUDIO/IO Cover LED
PCS LED*0.16W=W



JT1 for FW update

For FW update.
JT1
1 LED_VCC5
2 LED_RST#
3 P40
4 P40 (66)
Hx14M_BLACK-RH-1
1027 Remove JT1

Color Demo Jumper

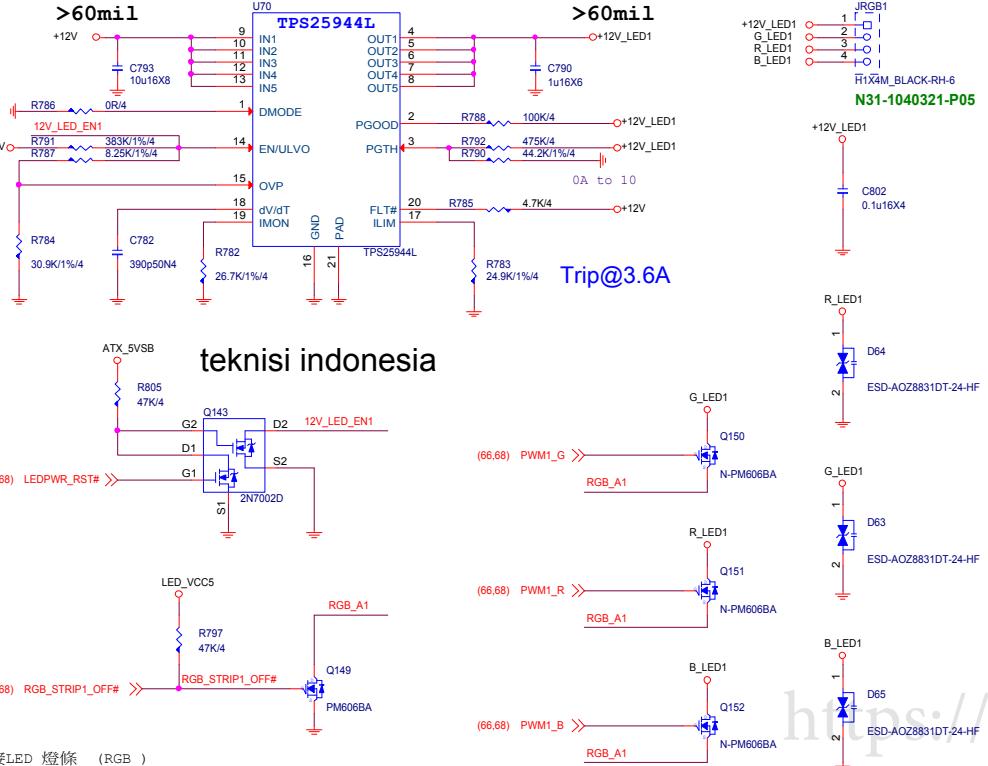
3 MOS HEATSINK LED
PCS LED*0.16W=W

JPIPE_LED3 no SPEC

JPIPE:PIN1:output ,PIN2:input

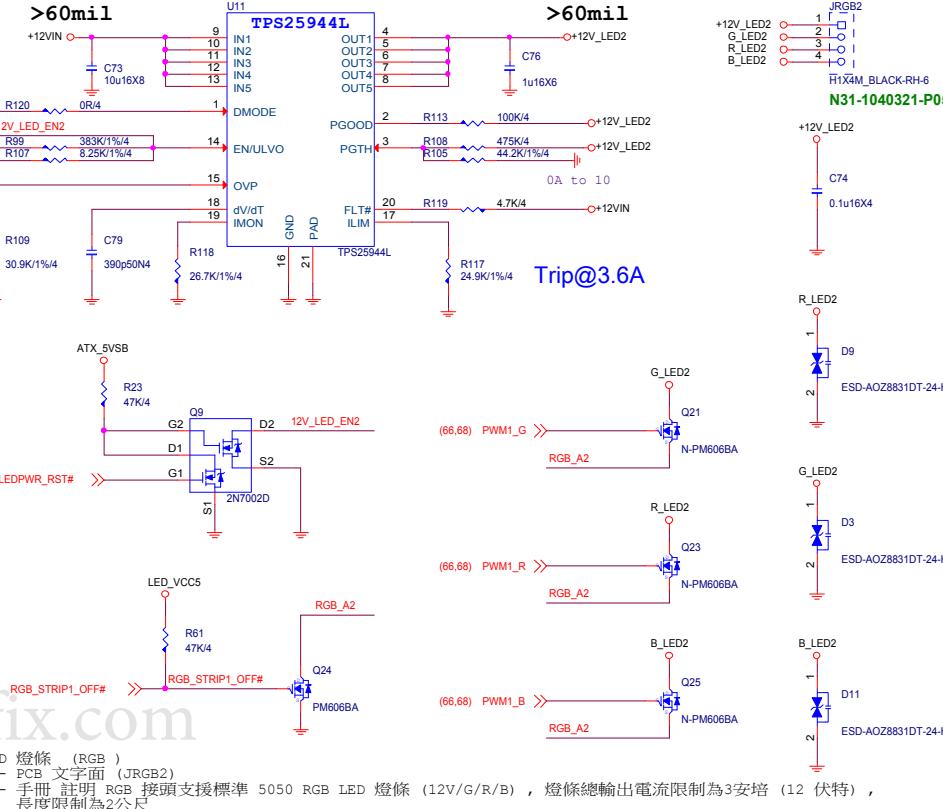
<https://vinafix.com>

JRGB1

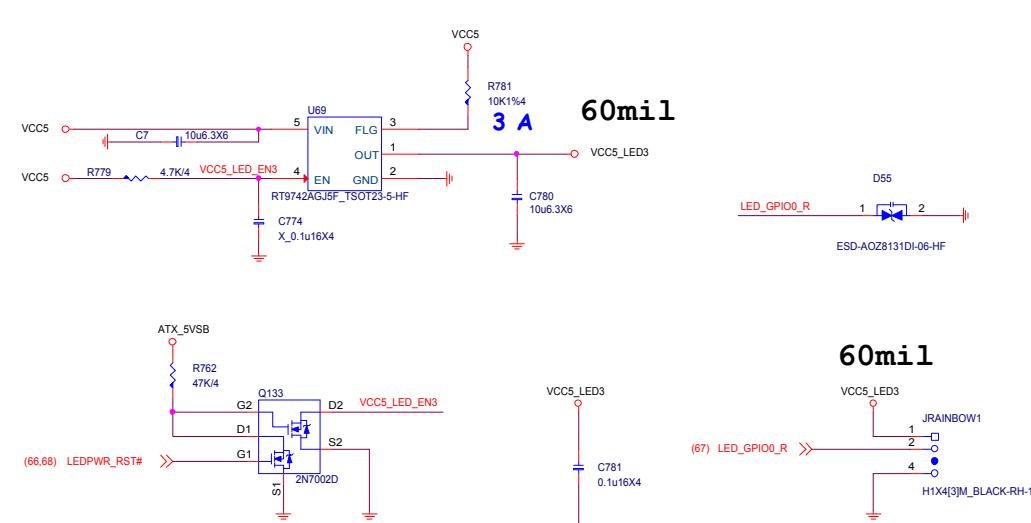


外接LED 燈條 (RGB)
---- PCB 文字面 (JRGB1)
---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

JRGB2

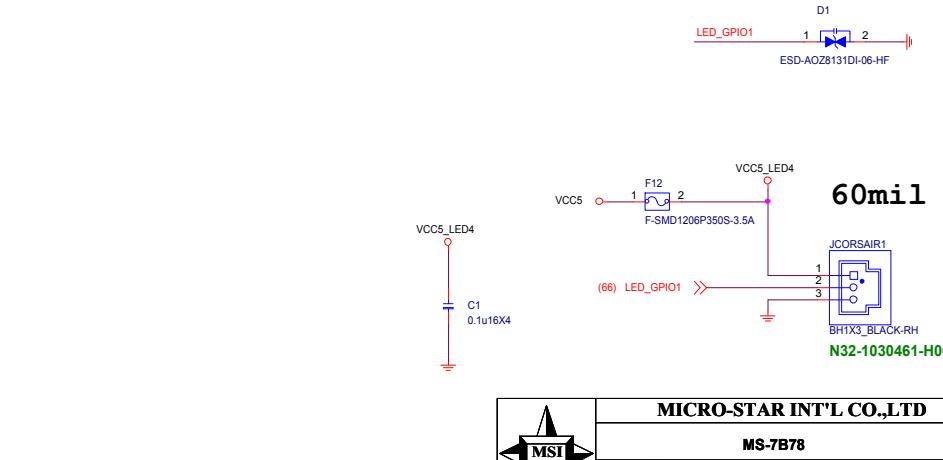


JRAINBOW1



JCORSAIR1

60mil



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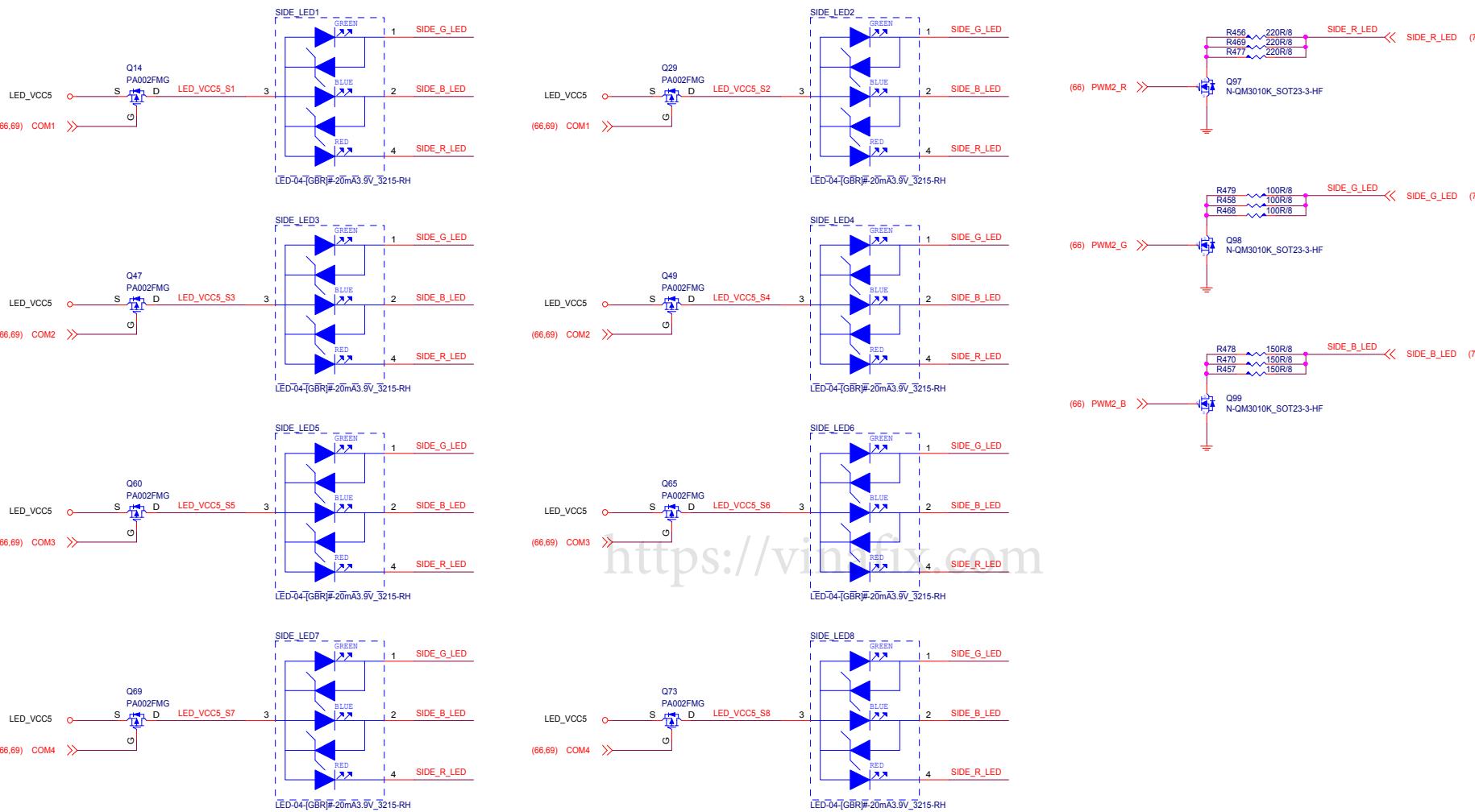
Size Custom Document Description

LED-JLED1/2/3/4

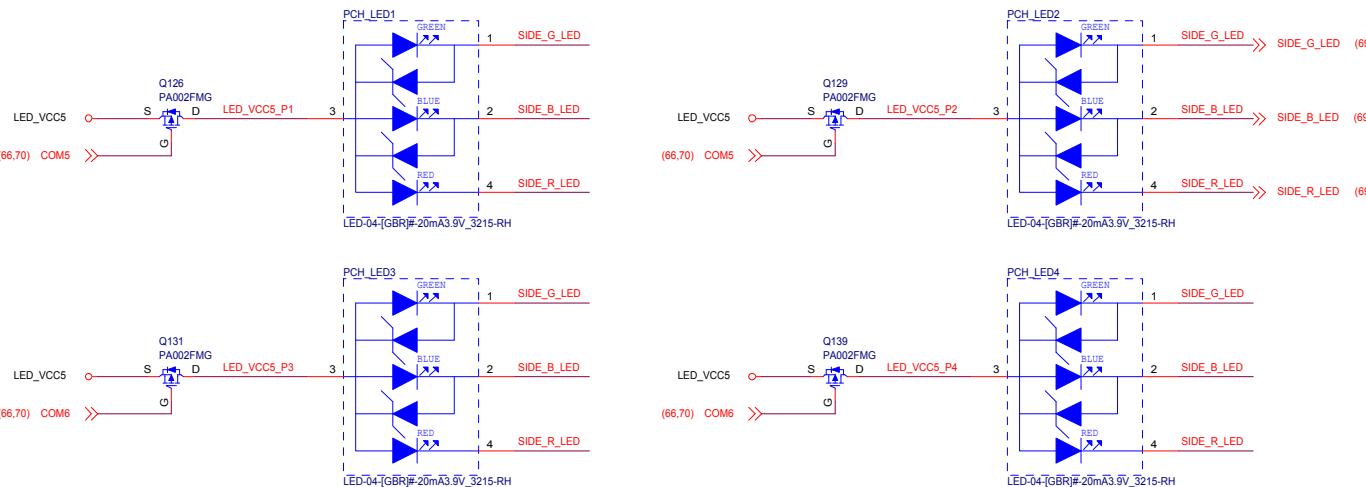
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Right Track LED *8



PCH LED *4



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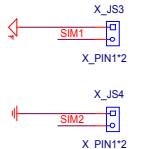
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CPU Socket



E95-0000022-C22

Simulation



PCB

PCB

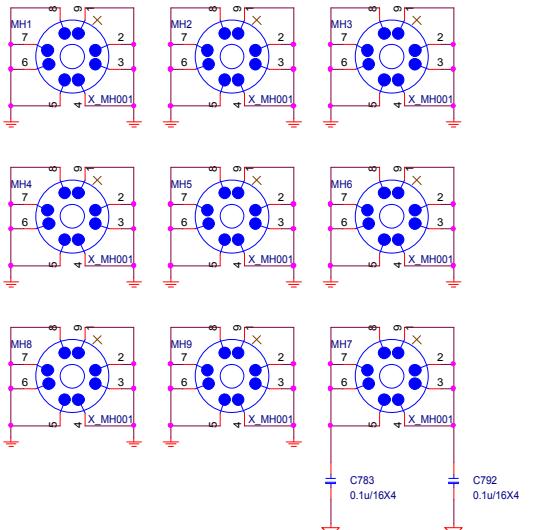


7B78_11

PCB1

X_FM120

Optics Orientation Holes

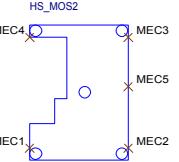
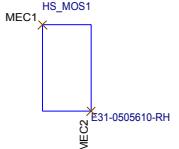


MANUAL PART

UEFI1
G51-M1SPXXA-A09
G51-M1SPXXA-A09CFOS
Y02-MU00170-CFO
Y02-MU00170-CFOHDMI_LAI
Label
HDMI LABEL
Y01-RHDMI03-000NAHIMIC
Y02-MU00100-NAH
Y02-MU00100-NAHSLI
Y01-RNVIDIL-000
Y01-RNVIDIL-000WIFI_MUDUAL
WiFi
604-4442-020BAT1_X1
C783 0.1u/16X4
C792 0.1u/16X4LA6
MKT
X470XSPLIT
X_Y02-MA00401-XSP
Y02-MA00401-XSP

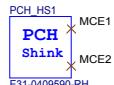
SSE
X_Y02-MA00101-SSE
Y02-MA00101-SSE

MOS HEATSINK



IO COVER+MOSA

PCH HEATSINK

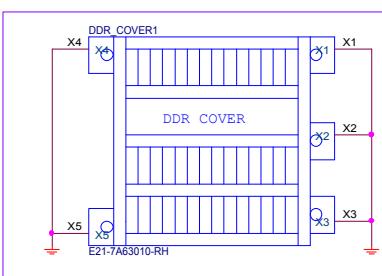


PCH Heatsink

Audio COVER

<https://vinafix.com>

DDR COVER



0901 Modify DDR_COVER1 PIN X1.X2.X3.X4.X5 Connect to GND

mos heatsink