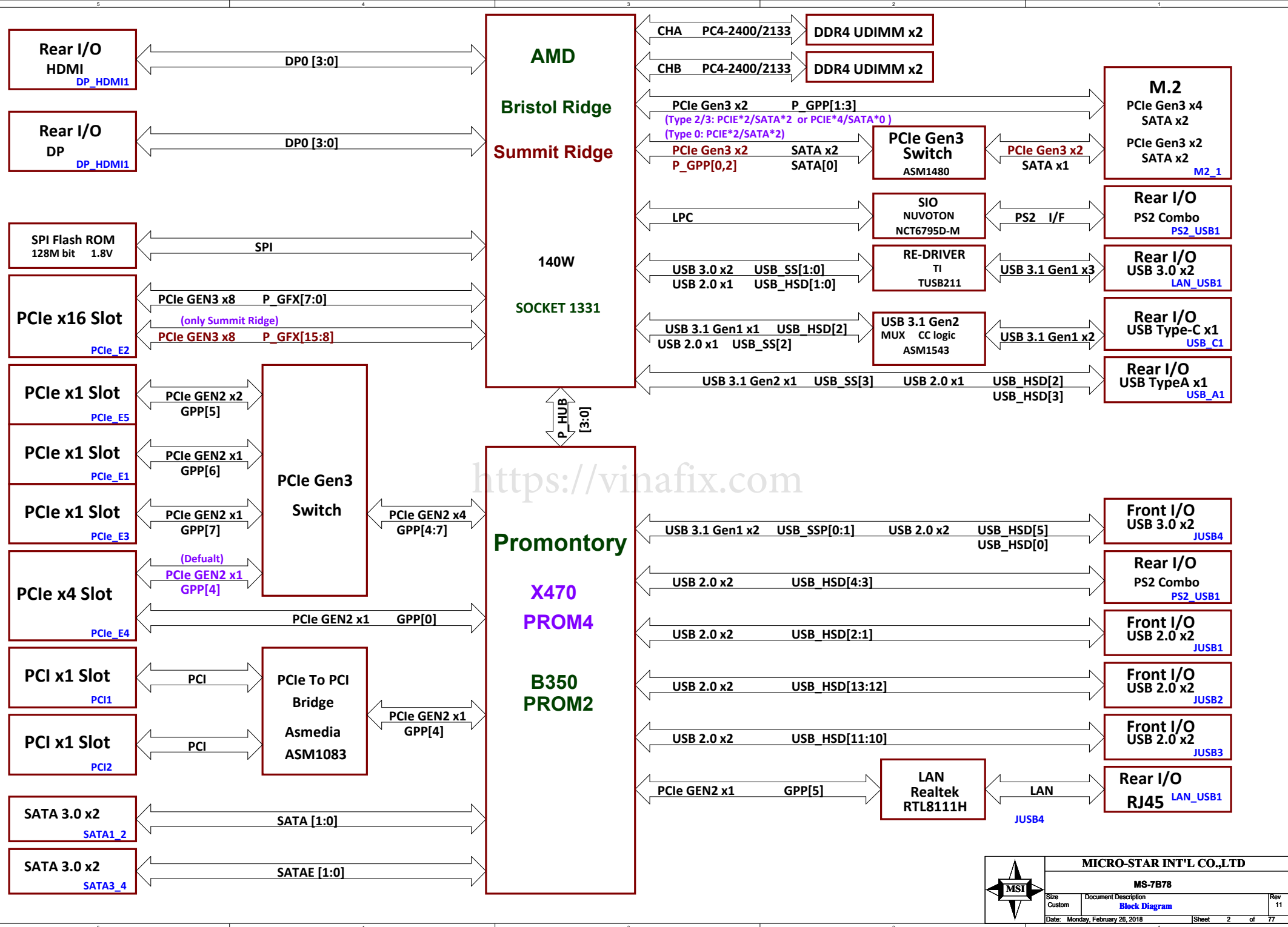
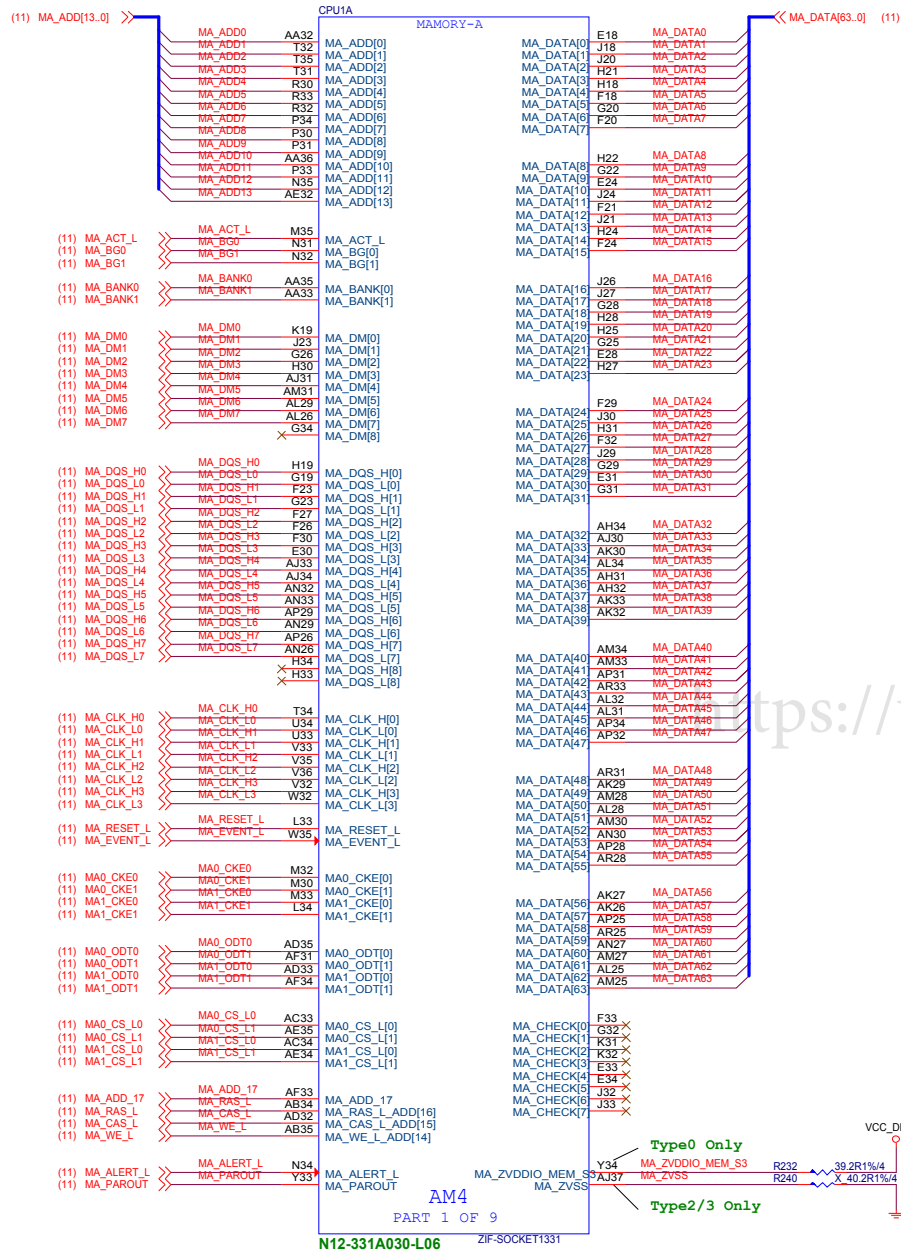
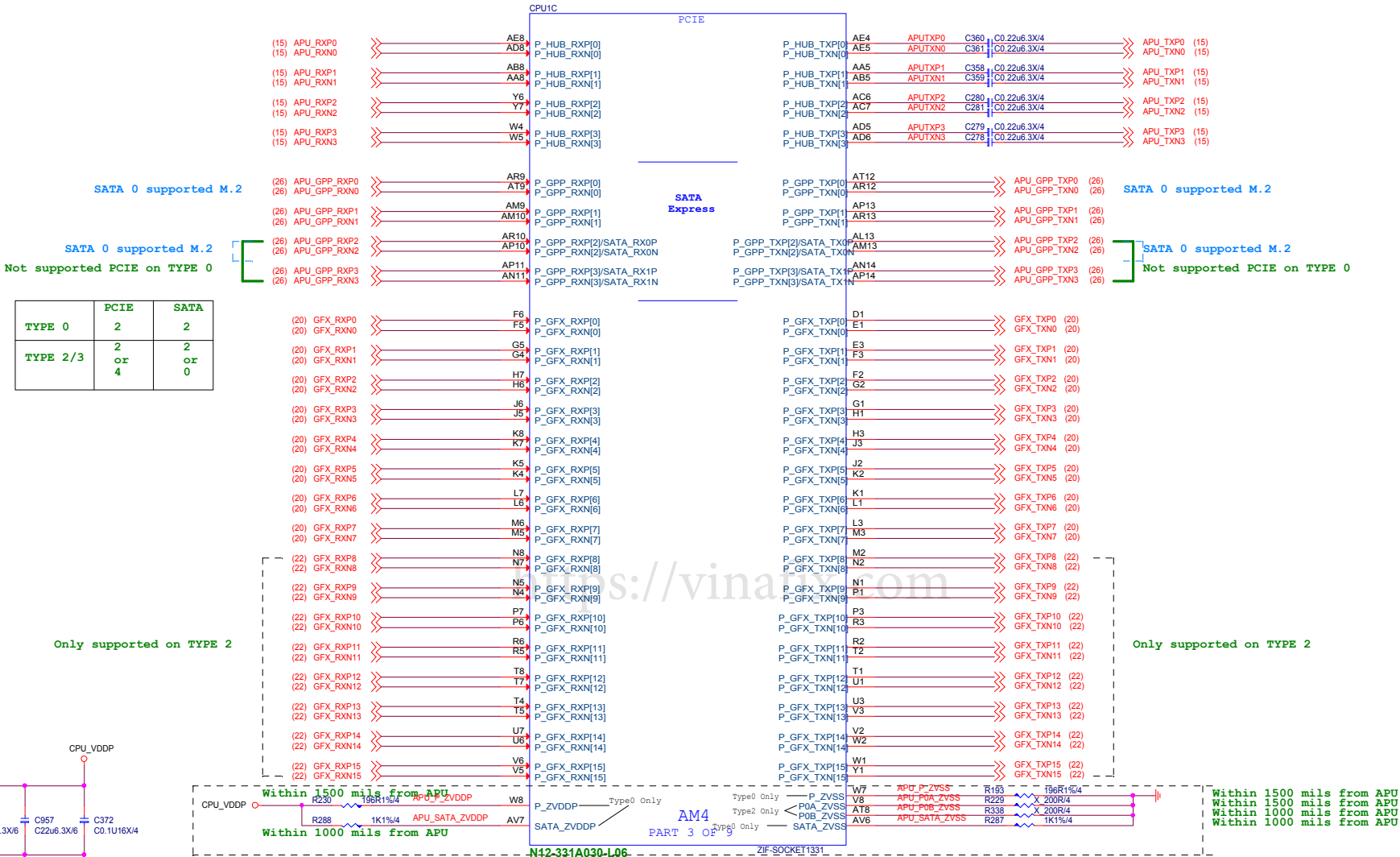


AMD AM4

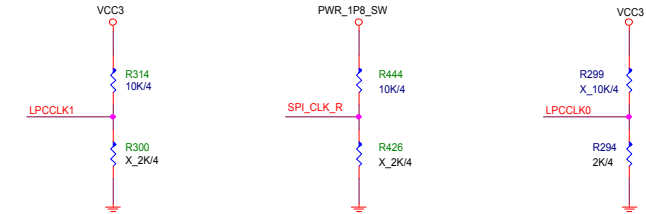
01	Cover Sheet	36	LAN - I211AT	66	MCU - LED Control
02	Block Diagram	37	Audio ALC1220P-VB	67	LED - Power / JPIPE
03	FM4 DDR4 I / F	38	Audio DePop	68	LED - JLED1 / 2 / 3 / 4
04	AM4 PCIE / SATAE	39	USB Power - UP7501	69	LED - Mystic Light - 1
05	AM4 Display / Audio	40	Front USB2.0 Header	70	LED - Mystic Light - 2
06	AM4 SVI / ACPI / GPIO	41	Front USB3.0 Header	71	BOM Option
07	AM4 LPC / SPI / USB / CLK / STRAP	42	Rear USB3.0 + PS2	72	Manual Parts
08-09	AM4 Power / VDDIO_AUDIO Power / GND	43	Rear USB3.0	73	PG MAP
10	RTC / CMOS	44	Rear USB3.1 Type A / redrive	74	GPIO MAP
11-14	DDR4 - POWER / GND	45	Rear USB3.1 Type A / mux	75	Power Sequence
15	Promontory - PCIE / SATA / SATAE	46	DP	76	Power Delivery
16	Promontory - USB / OC	47	HDMI	77	History
17	Promontory - CLK / ACPI / GPIO	48	CPU power UP9505 10+2		
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21	PCI_E4 (X8)	51	CPU power NB 1-2		
22	PCIE Switch X16 / X8	52	CPU power NB_S5		
23	PCI_E1_E3_E5 (X1)	53	CPU power 1.8_S0 / S5		
24	PCI_E6 (X4)	54	CPU power VDDP - TPS56C215		
25	PCIE Switch X4 / M2_2	55	VRM PWRGD		
26	M.2_1	56	DDR Power - RT8125E		
27	M.2_2	57	DDR Power - VPP25 / VTT		
28	M.2_3 (WIFI+BT)	58	PROM - SY8288RAC / 1.05V		
29	SIO NCT6797D-M	59	PROM - GS7133 / 2.5V		
30	SIO HW Monitor / NCT7718W	60	OV Control - NCT3933		
31	FAN TYPE-J CPUFAN1	61	OV 12VIN - RT9553B		
32	FAN TYPE-J PUMPFAN1	62	ACPI - 3VSB / 5VDIMM		
33	FAN TYPE-K SYSFAN1/2	63	ATX Power - FrpntPanel / EMI		
34	FAN TYPE-K SYSFAN3/4	64	LED - EZDEBUG / AMP		
35	FAN GPIO NCT5605	65	LED - DIMM / PCIE SLOT		



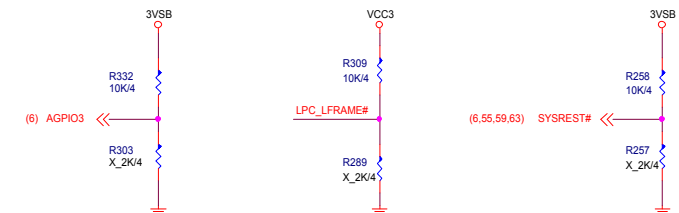




Strapping Options



	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	LPC device Boot Fail Timer Enabled
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIe clock as reference clock and generate internal clocks only	LPC device Boot Fail Timer Disabled (Default)



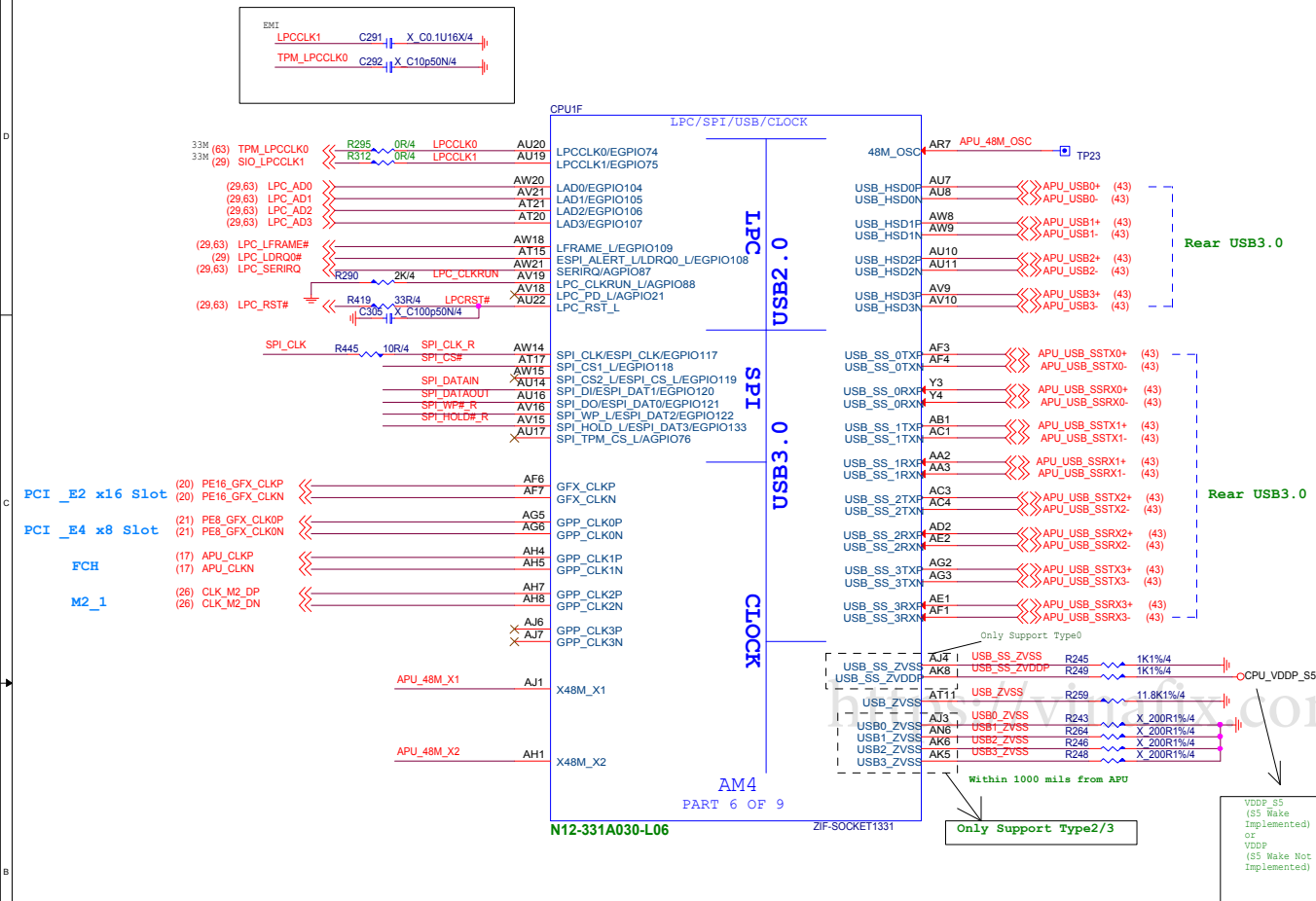
	AGPIO3	SIO_LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

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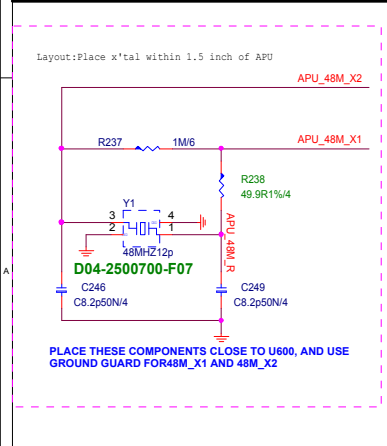
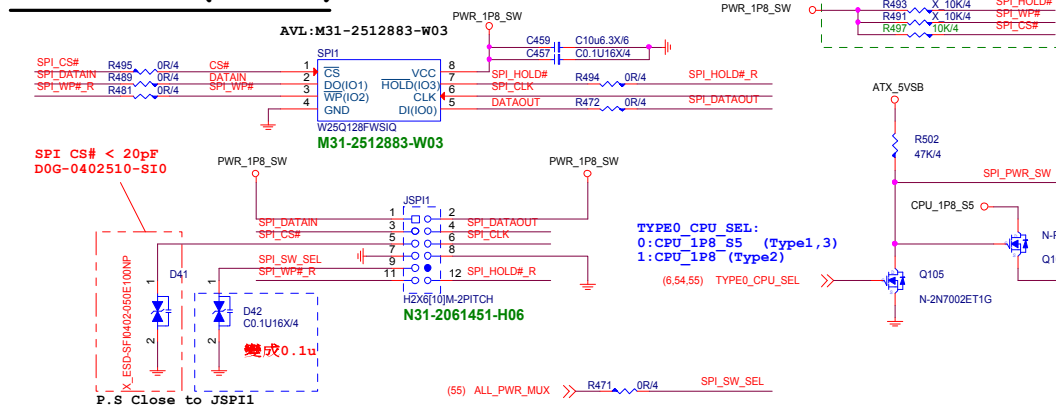
	RTCCCLK
PULL HIGH	RTC Coin Battery is on board (Default)
PULL LOW	RTC Coin Battery is not on board

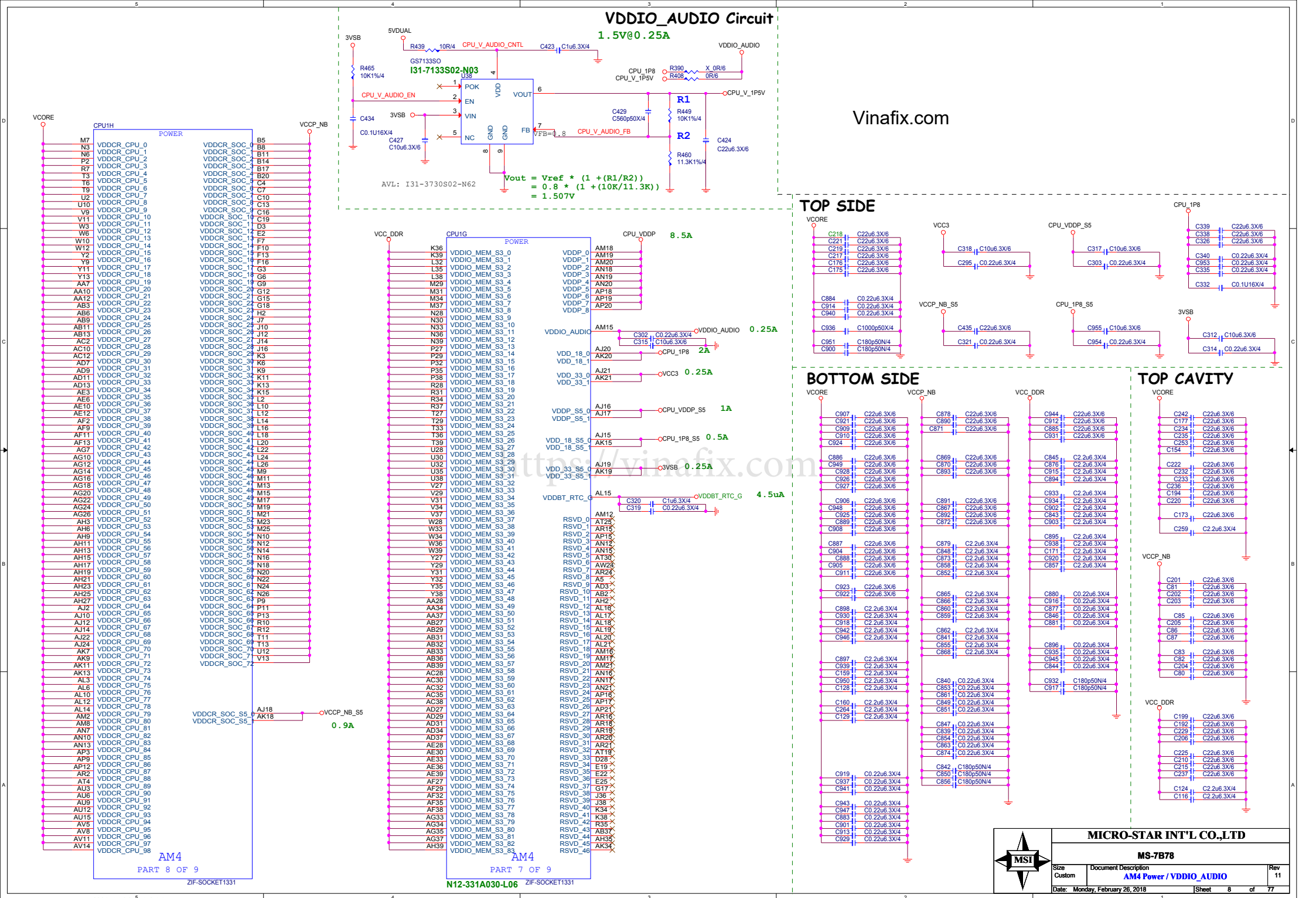


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Custom	AM4 LPC / SPI / USB / CLK / STRAP	11
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SPI ROM (1.8V)



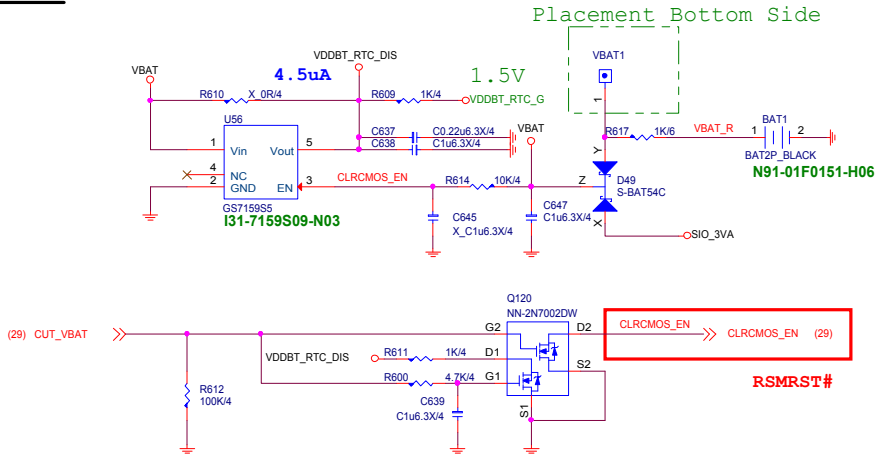


GND

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AM4
PART 9 OF 9

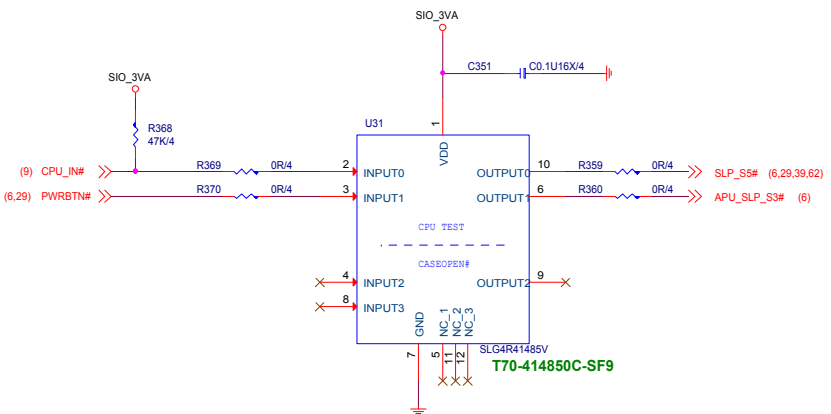
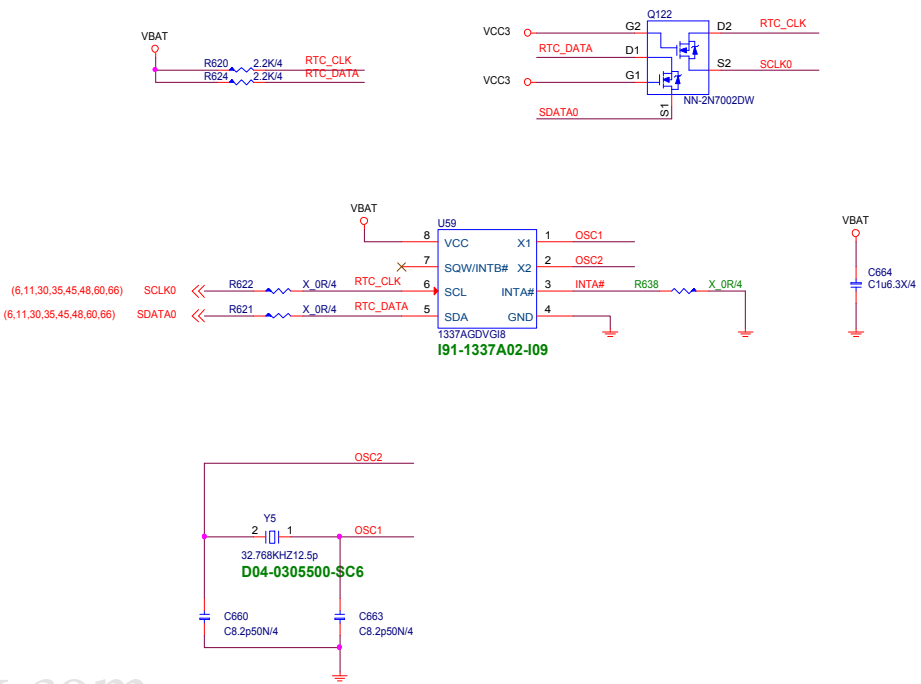
RTC & Clear CMOS Circuit



Clear CMOS button



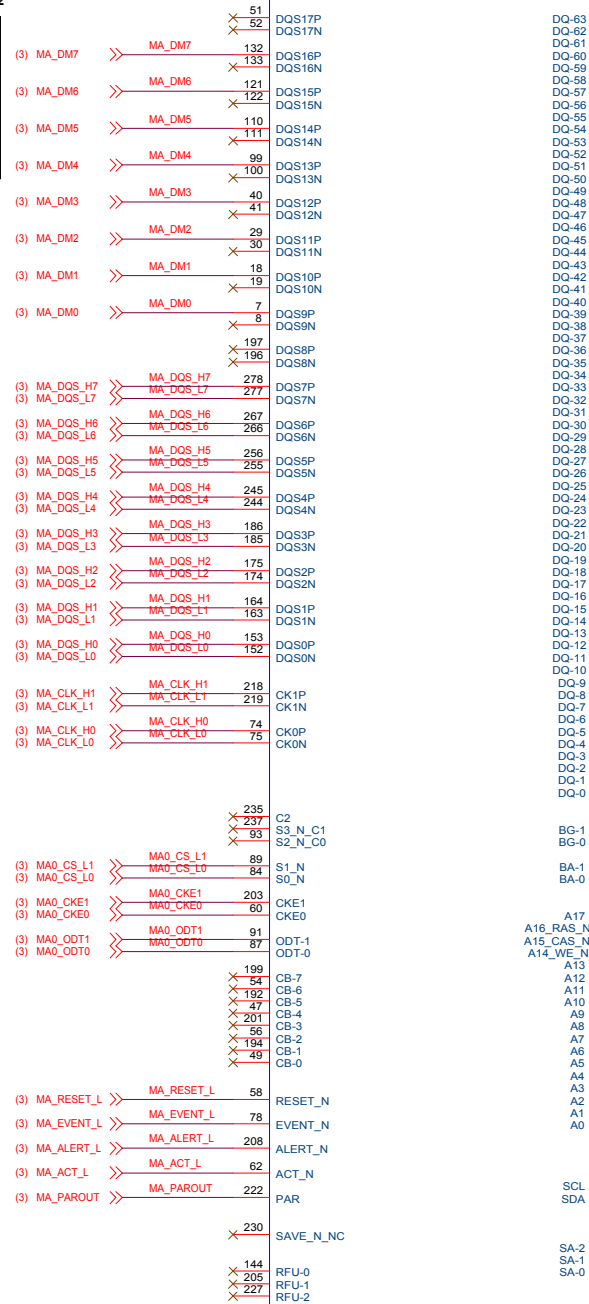
RTC Backup



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A1 A2 B1 B2

DIMMA1A

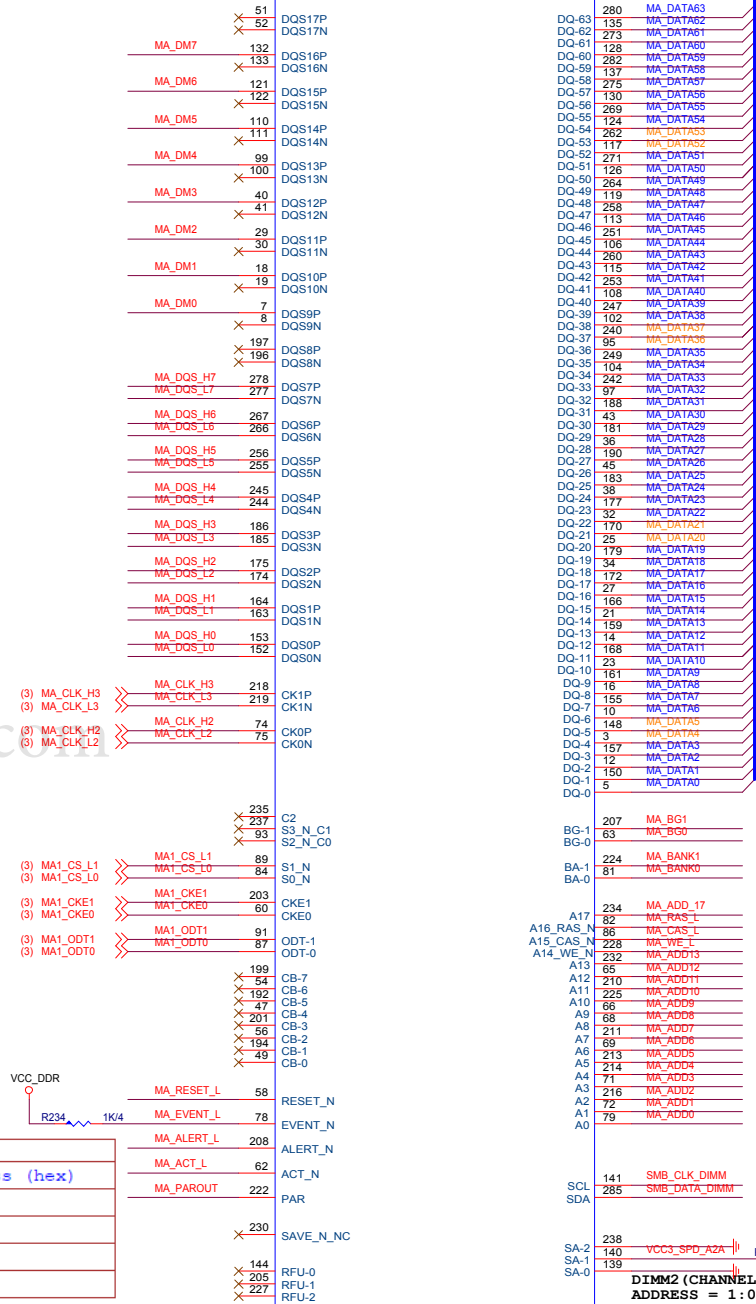
DDR4V-288P
N13-2880581-L06

(6,10,30,35,45,48,60,66)

SCLK0
SDATA0SCLK0
SDATA0R407
R399OR4
OR4SMB_CLK_DIMM
SMB_DATA_DIMMSMB_CLK_DIMM
SMB_DATA_DIMM(12)
(12)

SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMA1	A4
DIMMB0	A2
DIMMB1	A6

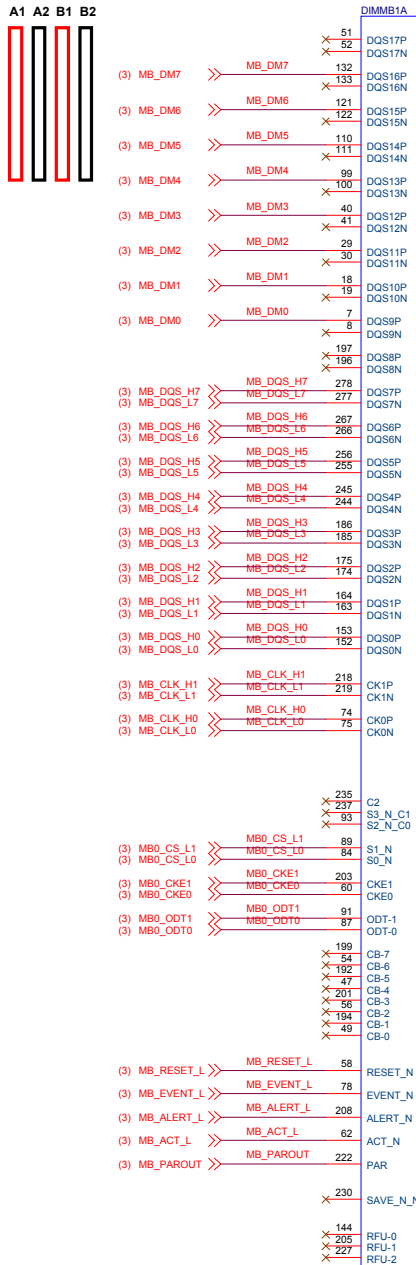
DIMMA2A

DDR4V-288P
N13-2880581-L06

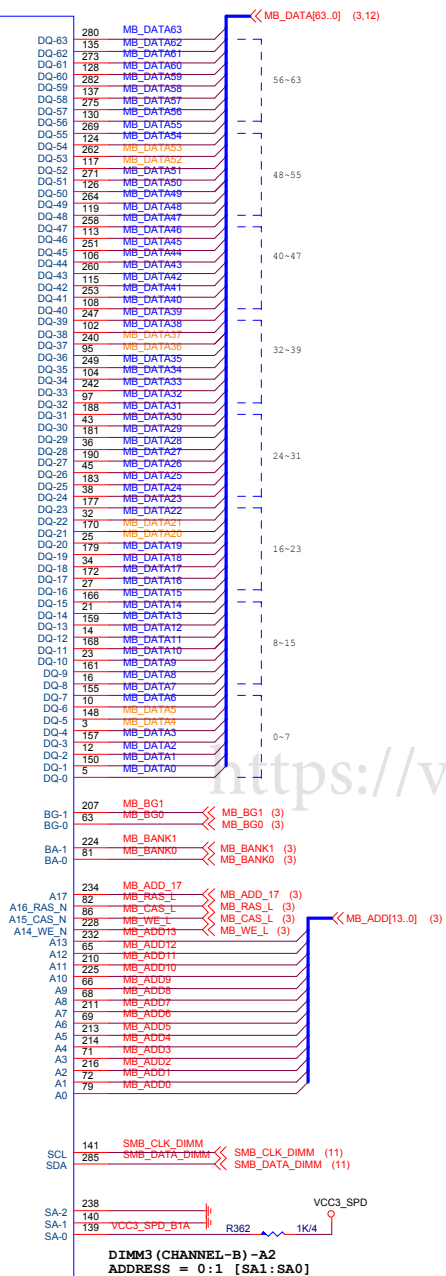
MICRO-STAR INT'L CO.,LTD

MS-7B78

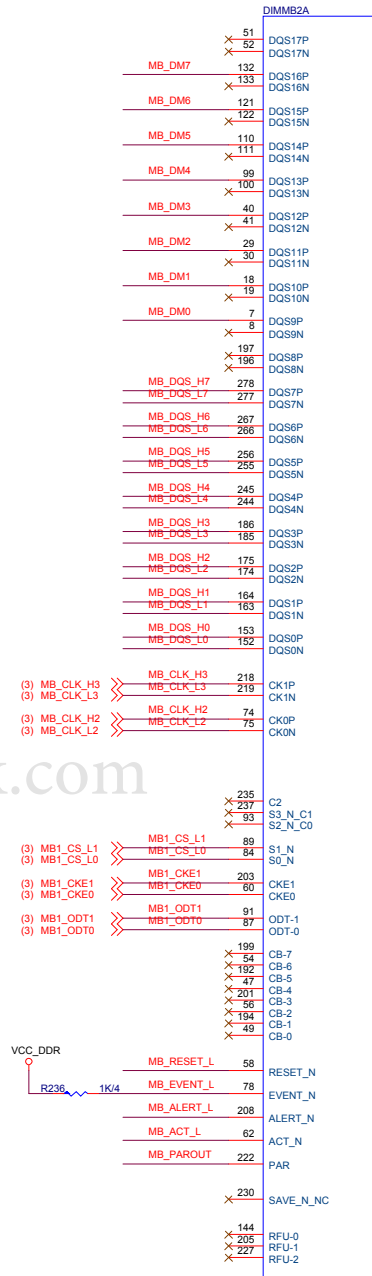
Size	Document Description	Rev
Custom	DDR4 - DIMM CH-A	11
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N13-2880581-L06



DIMM3 (CHANNEL-B) - A2
ADDRESS = 0:1 [SA1:SA0]

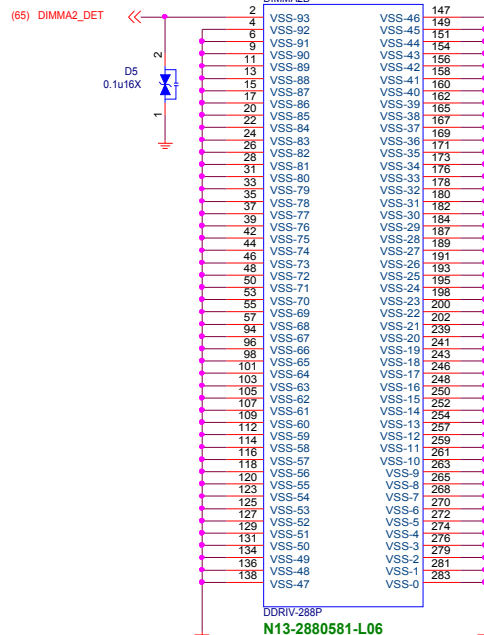
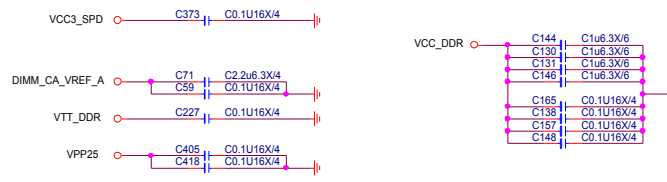
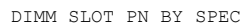


N13-2880581-L06

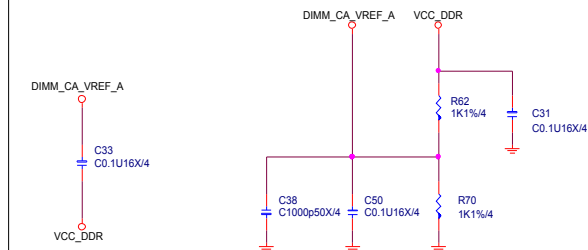


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Custom	DDR4 - DIMM CH-B	11
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D08-0301000-P16



(place resistors close to DIMMs)



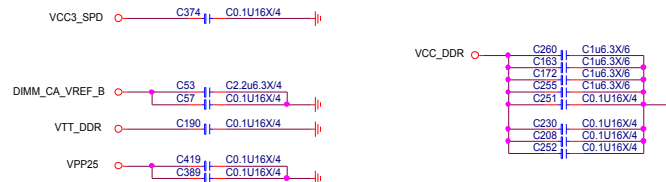
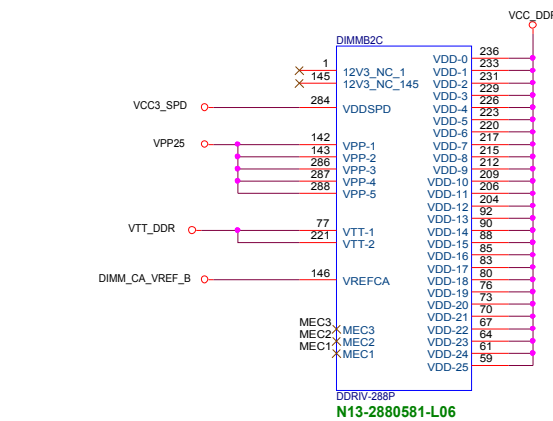
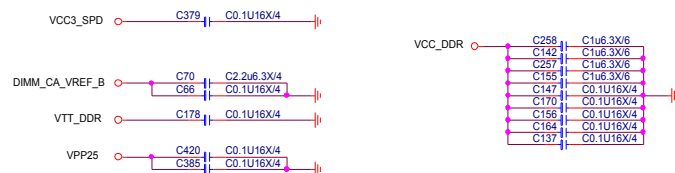
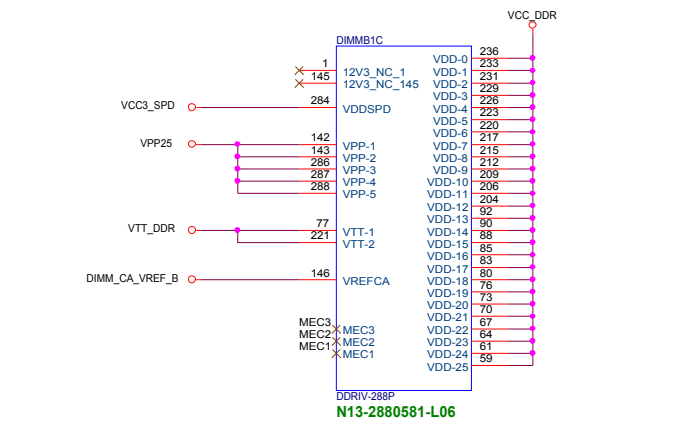
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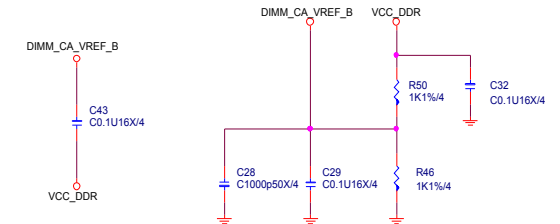
MS-7B78

Size Custom	Document Description DDR4 - POWER/GND-1	Rev 11
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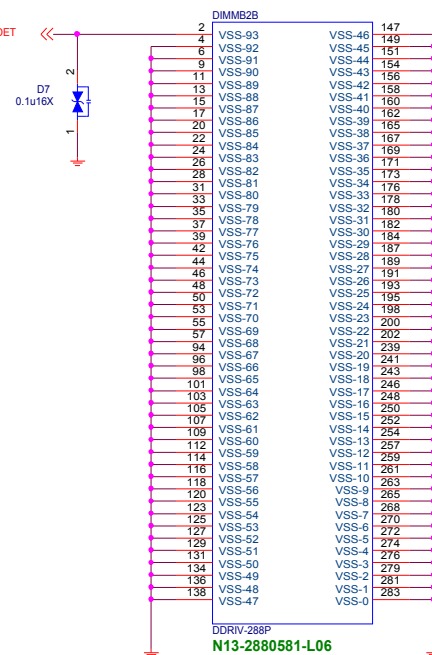
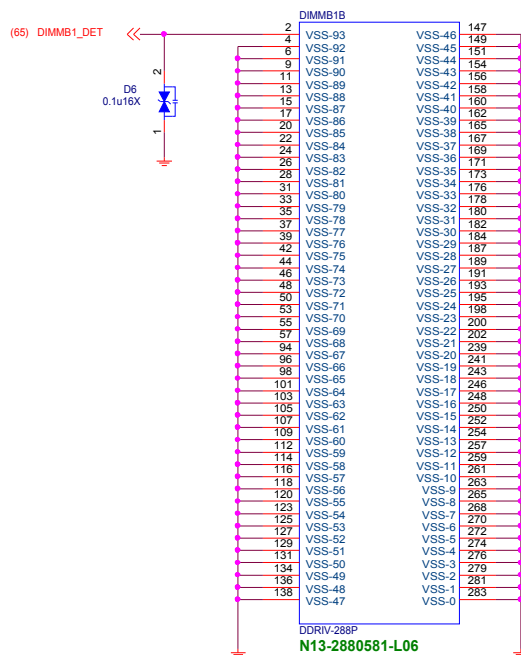


DDR VREF

(place resistors close to DIMMs)



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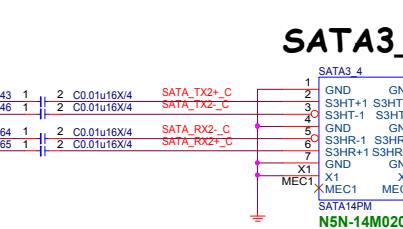
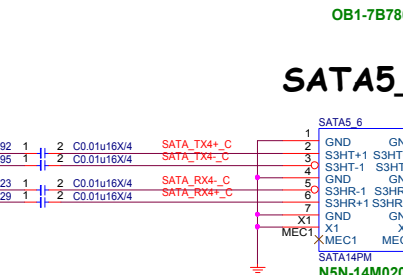
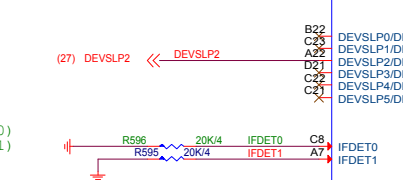
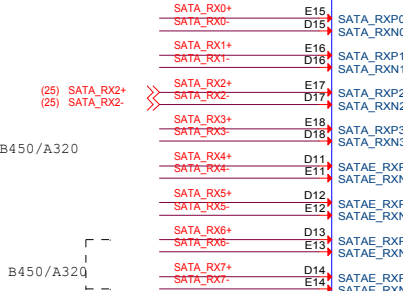
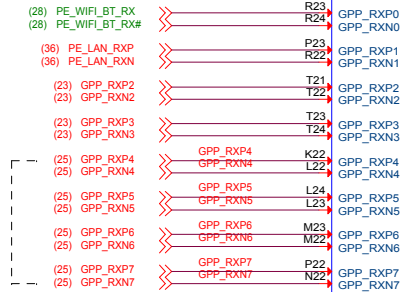
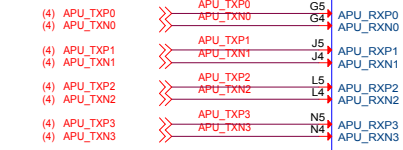
WIFI+BT

LAN

PCI_E2

PCI_E4

PCI_E5_M2_2



PCIE

SATA

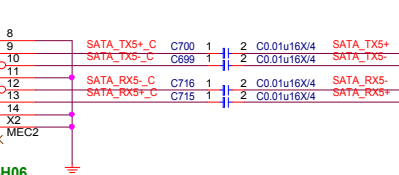
SATA Express

DEVSLP LED

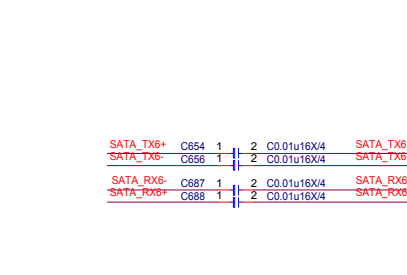
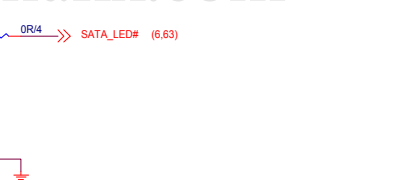
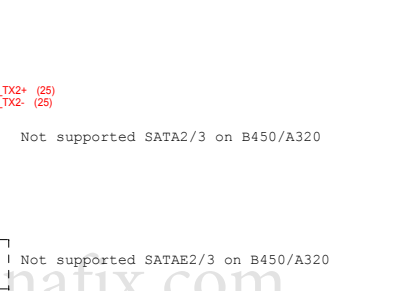
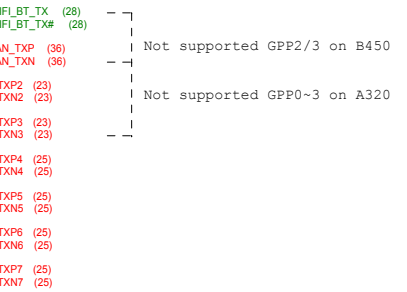
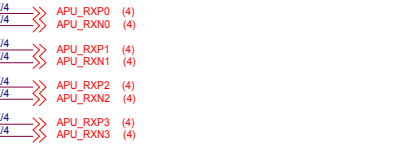
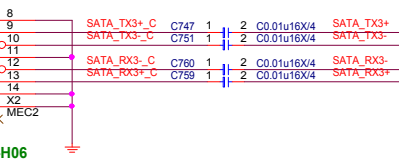
PROMONTORY

OB1-7B78001-A08

SATA5_6

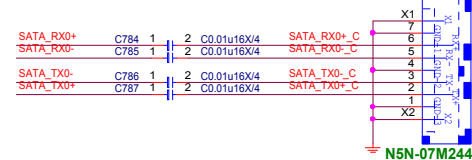


SATA3_4

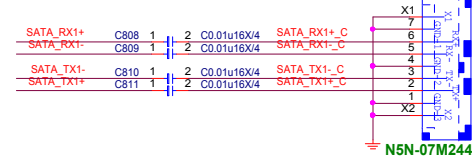


SATA Connector

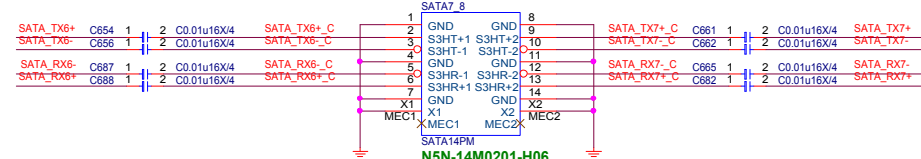
SATA1



SATA2



SATA7_8

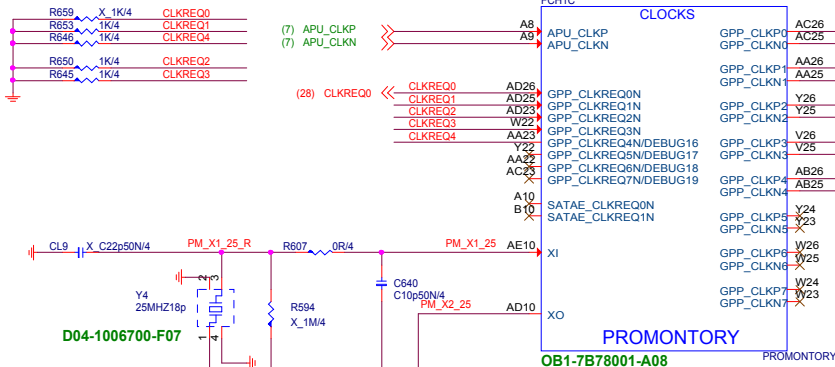


MICRO-STAR INT'L CO.,LTD

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GPP Clock	CLKREQ#
GPP_CLKP[N][0]	GPP_CLKREQ0N
GPP_CLKP[N][1]	GPP_CLKREQ1N
GPP_CLKP[N][2]	GPP_CLKREQ2N
GPP_CLKP[N][3]	GPP_CLKREQ3N
GPP_CLKP[N][4]	GPP_CLKREQ4N
GPP_CLKP[N][5]	GPP_CLKREQ5N
GPP_CLKP[N][6]	GPP_CLKREQ6N
GPP_CLKP[N][7]	GPP_CLKREQ7N



Not supported GPP0~3 on PROM1
Not supported GPP2/3 on PROM2

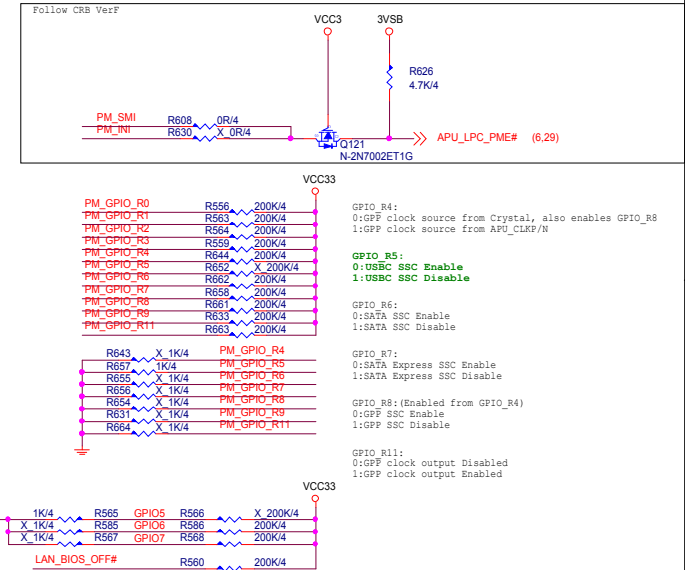
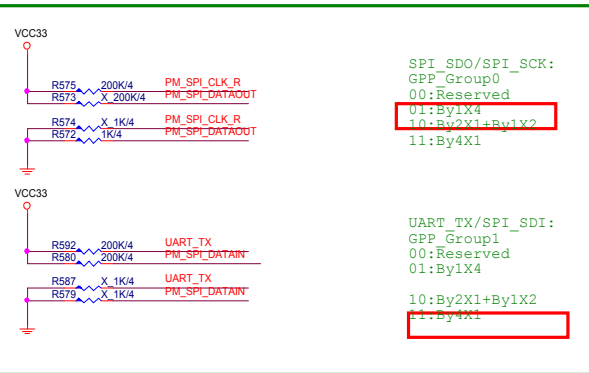
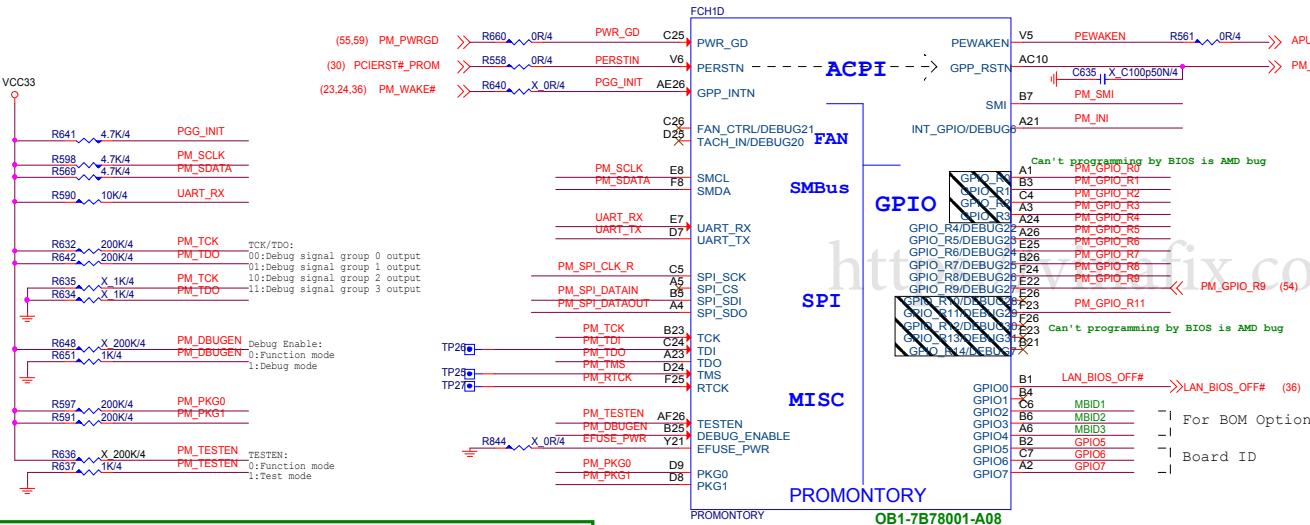
Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~3	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

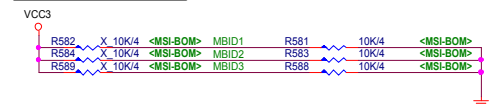
CLK2.3-不能用

CLK1.3-不能用



	MBID3	MBID2	MBID1
Z470	0	0	0

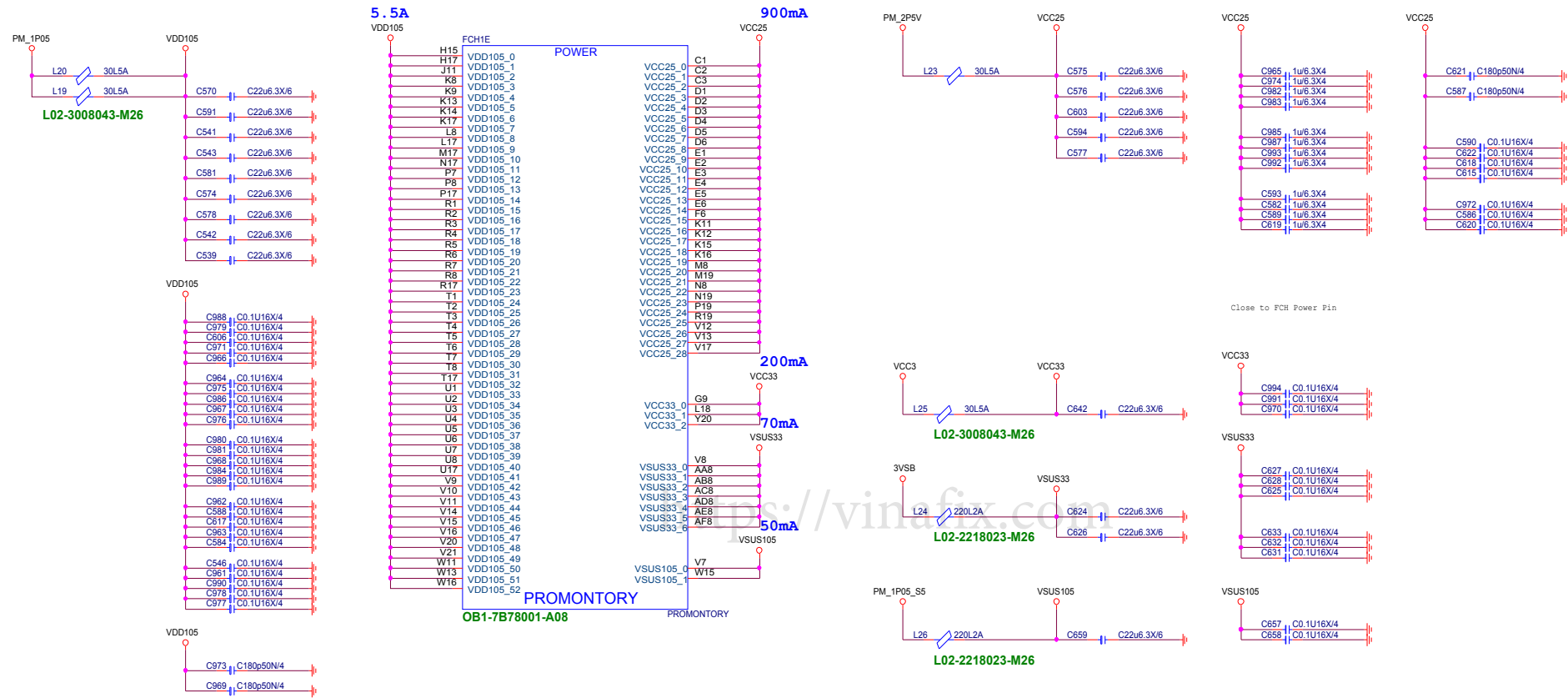
BOM OPTION



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GND

PROMONTORY

PROMONTORY

OB1-7B78001-A08

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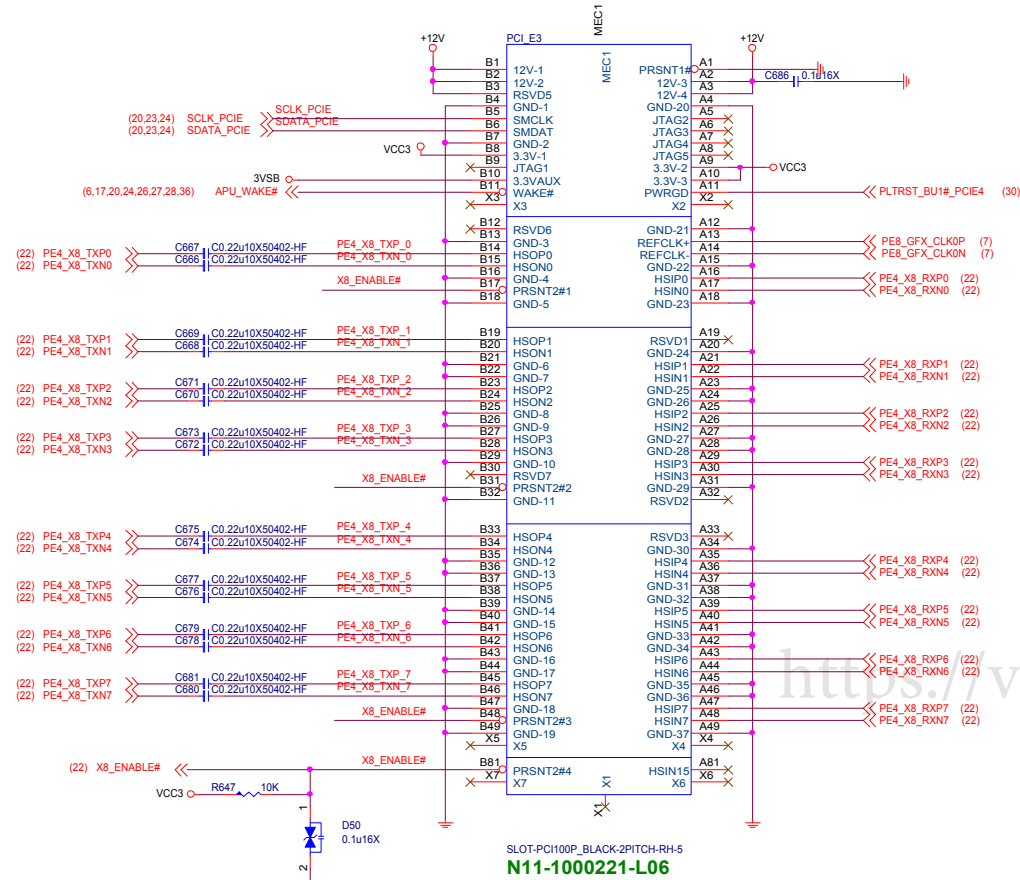
MICRO-STAR INT'L CO.,LTD

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Custom	Promontory - GND	11
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PCI EXPRESS x8 SLOT

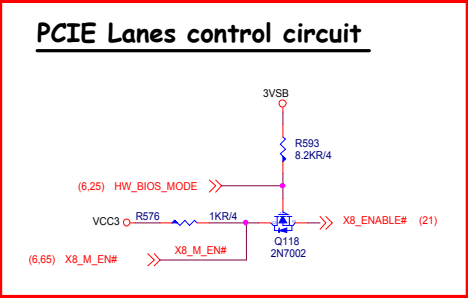
PCI_E3



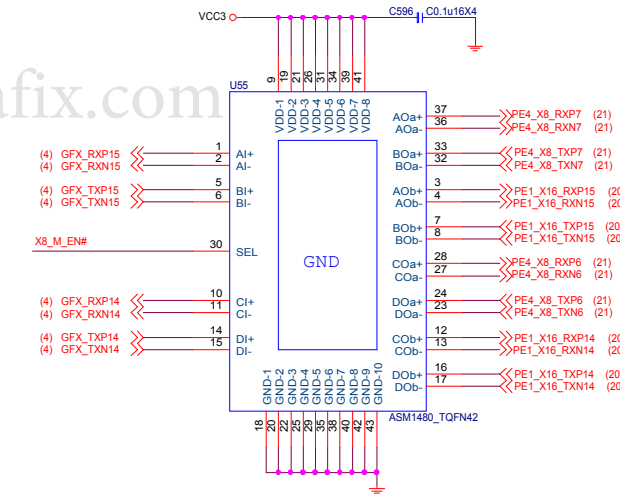
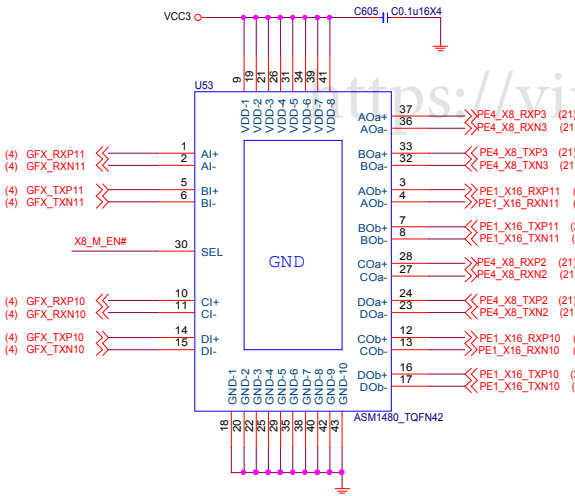
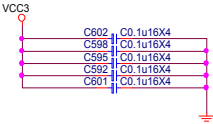
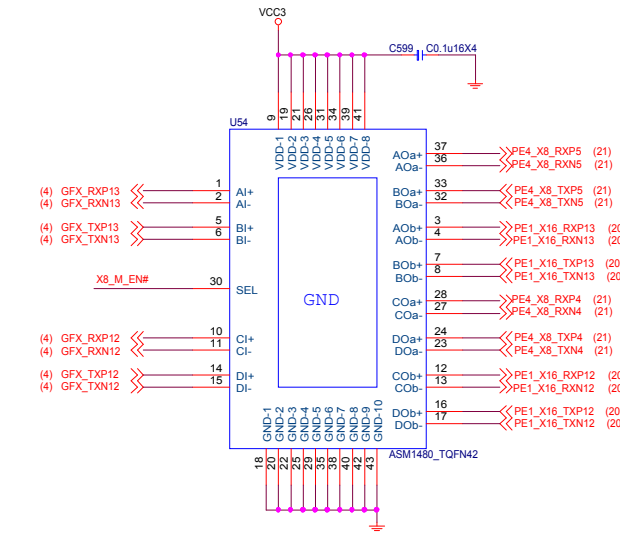
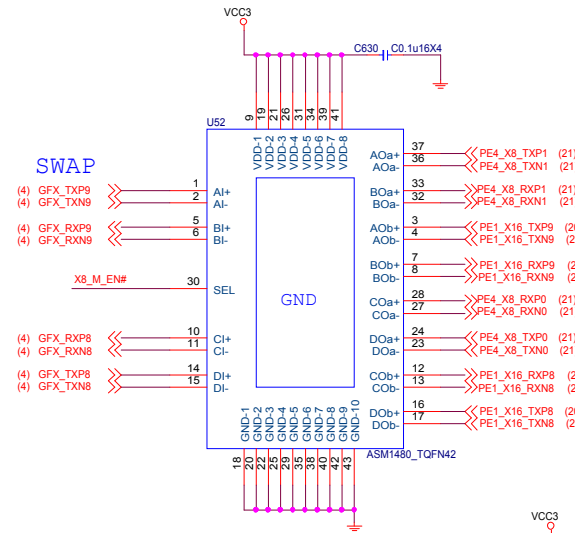
PCI Express x8 Slot		
+12V	-	A
+VCC3	-	3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

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PCI EXPRESS Switch
For PCIE1 & PCIE3



	HW_BIOS_MODE	X8_M_EN#
Auto	1	1
Manual x16	0	1
Manual x8, x8	0	0

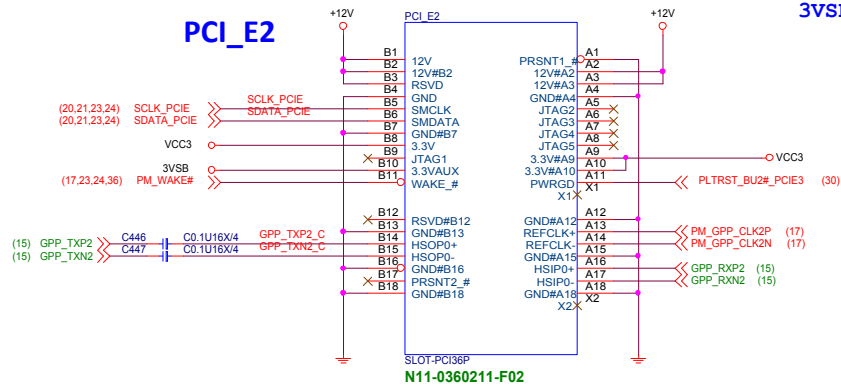


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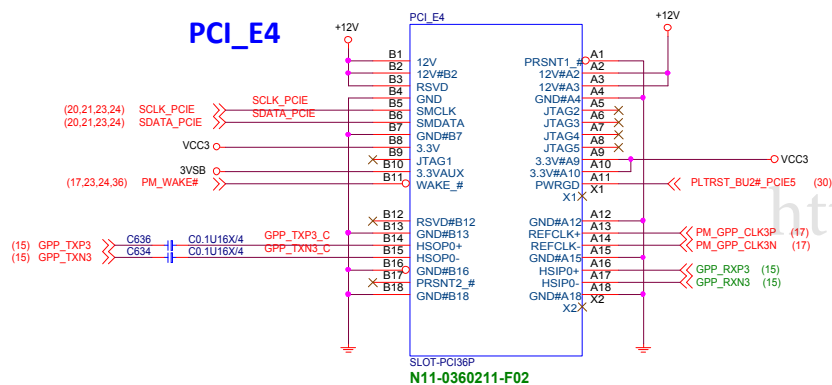
PCI EXPRESS X1 SLOT

12V - 0.5A
VCC3 - 3A
3VSBV - 375mA

PCI_E2



PCI_E4

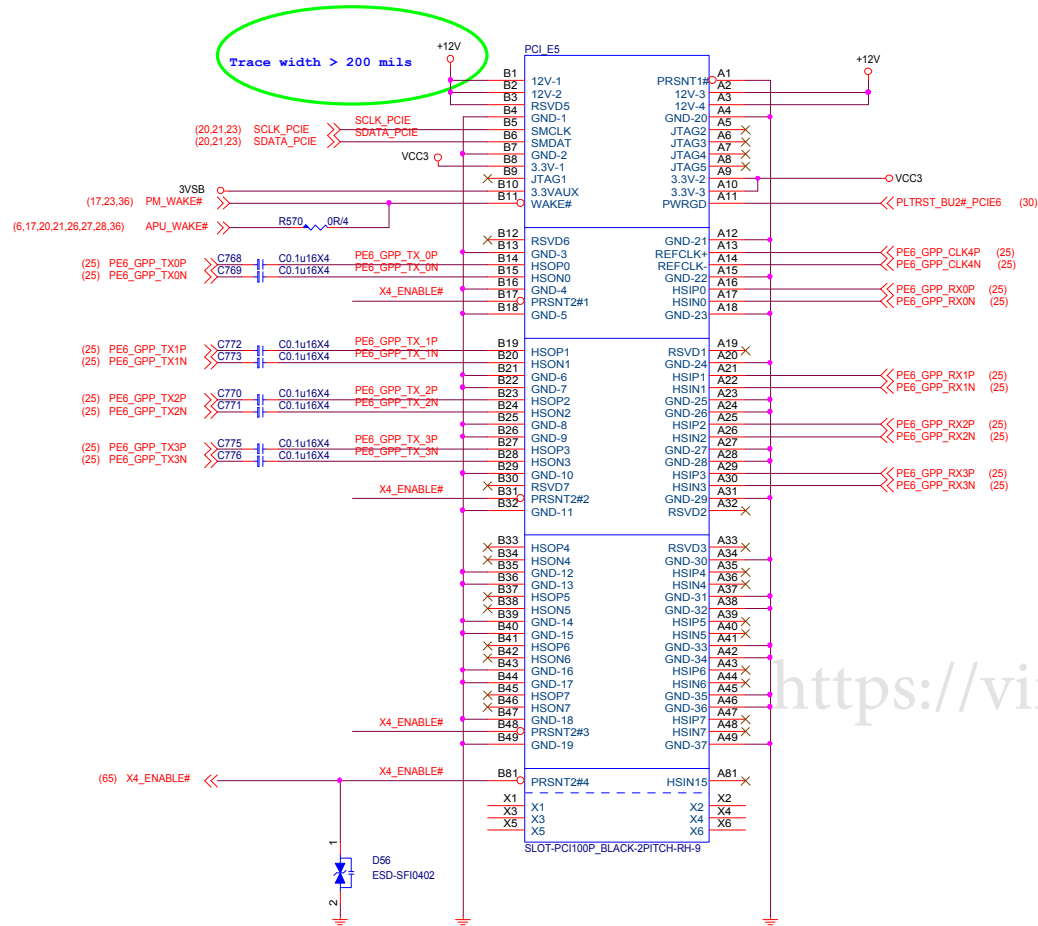


PCI Express x1 Slot *3	
+12V	- 1.5 A
+VCC3	- 9A
+3V3_S5 (wake)	- 1125mA
+3V3_S5 (no wake)	- 60mA

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Custom	PCI_E1_E3_E5(XI)	11	
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PCI EXPRESS X4 SLOT

PCI_E6

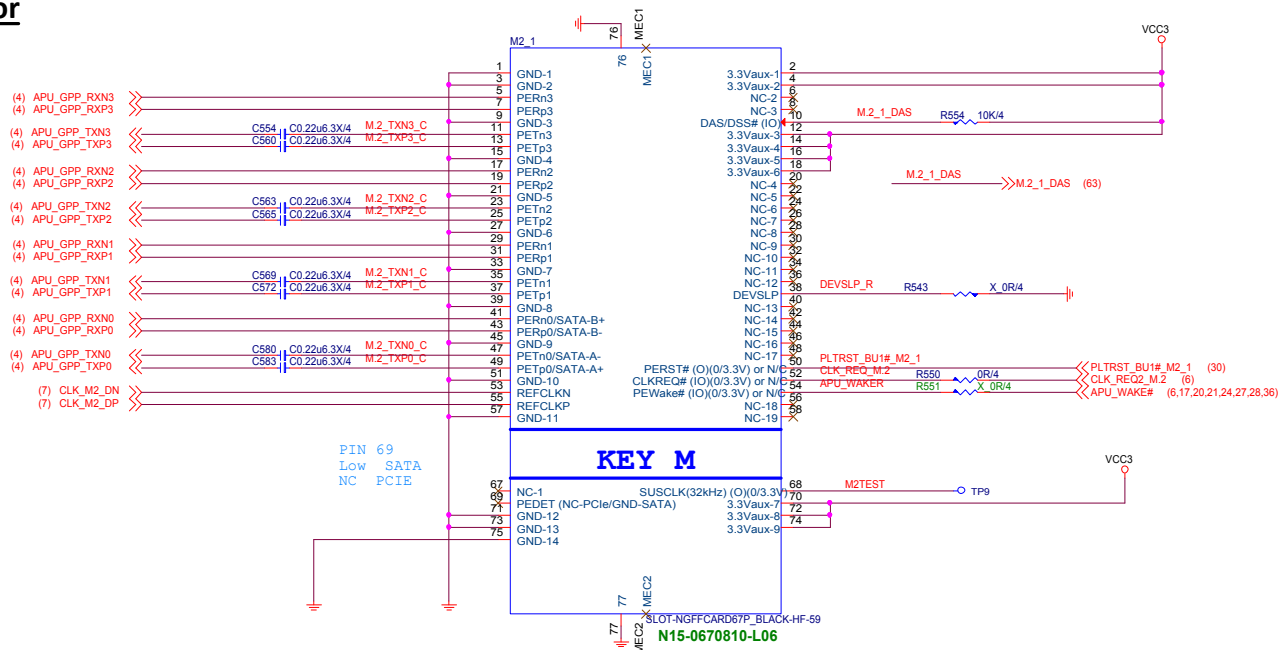


PCI Express x4 Slot *1	
+12V	- 2.1A
+VCC3	- 3A
+3V3_S5 (wake)	- 375mA
+3V3_S5 (no wake)	- 20mA

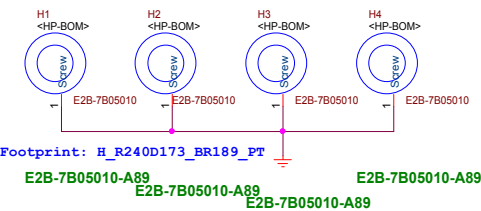
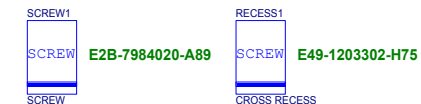
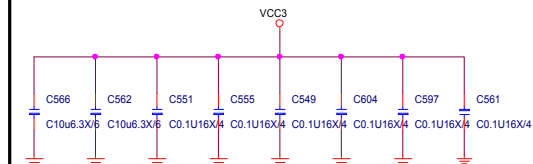
MICRO-STAR INT'L CO.,LTD		
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Size	Document Description	Rev
Custom	PCI_E6 (X4)	11
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M.2 1 Connector

3.3V@2.5A



3.3V@2.5A

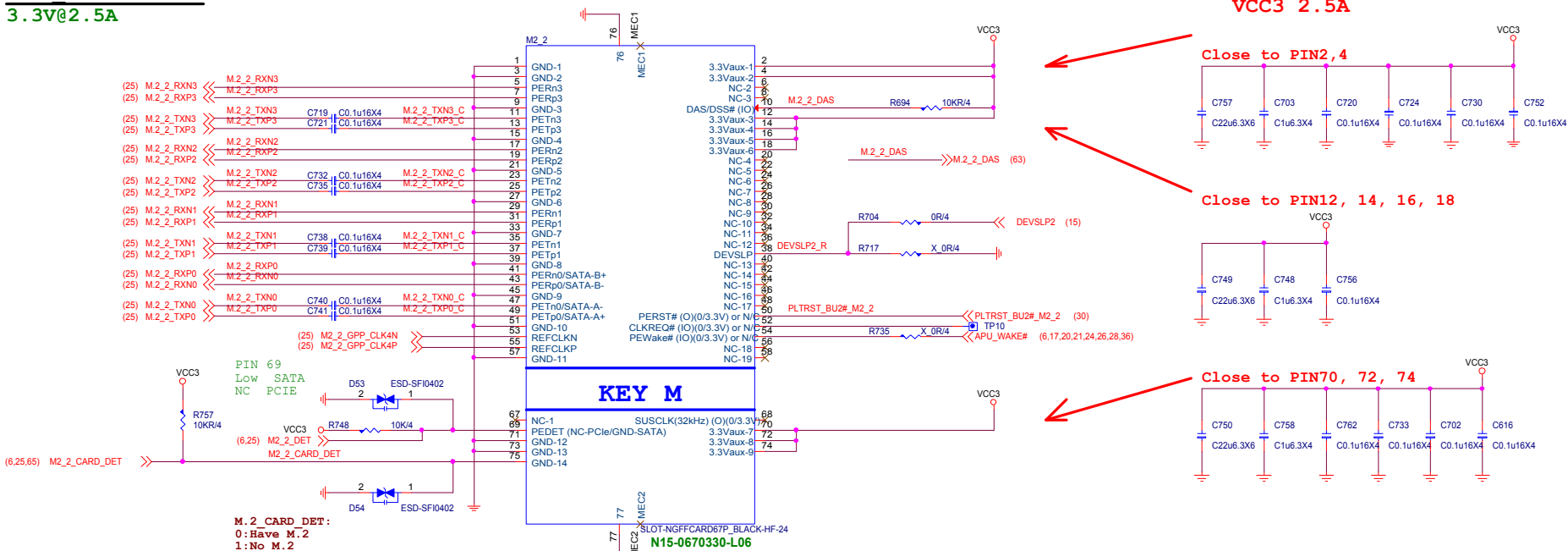


<https://vinafix.com>

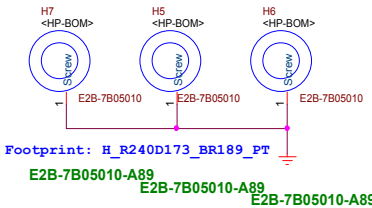
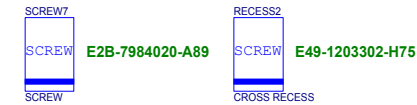
Vinafix.com

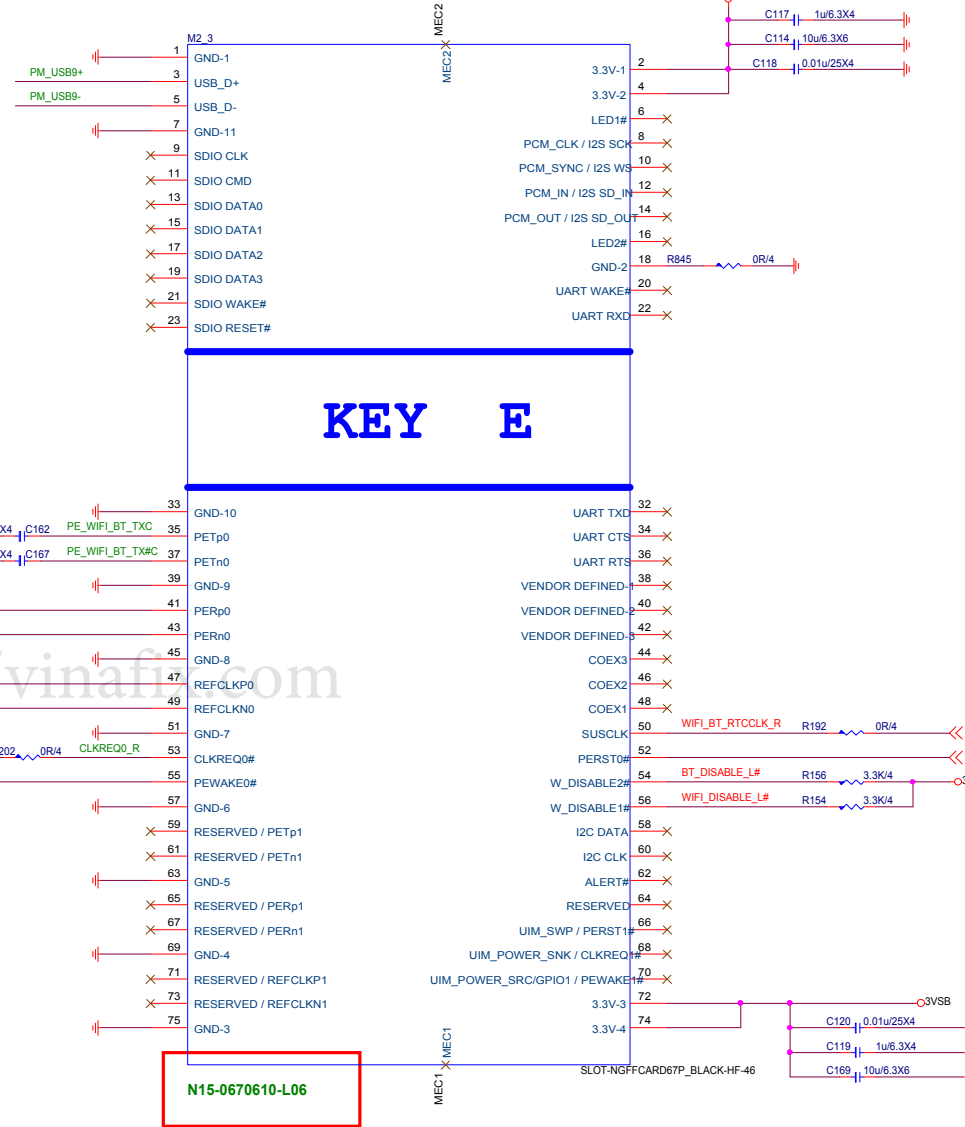
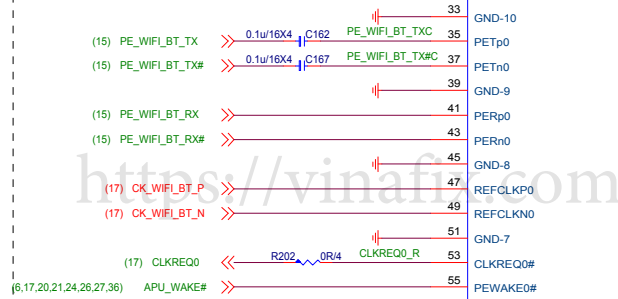
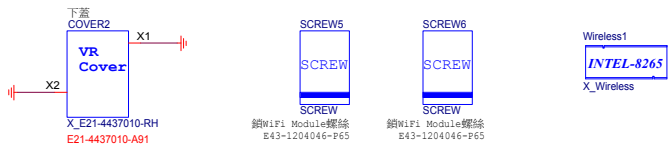
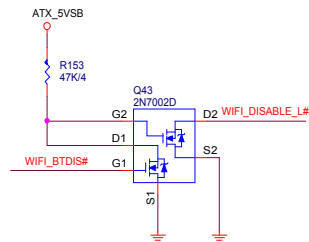
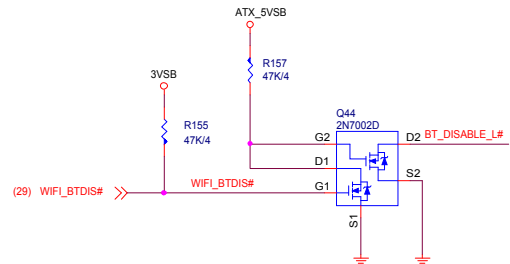
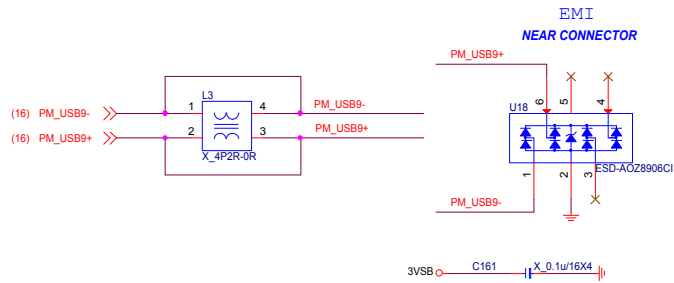
MICRO-STAR INT'L CO.,LTD			
MS-7B78			
Size	Document Description	Rev	
Custom	M2_1	11	
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M.2_2 Connector

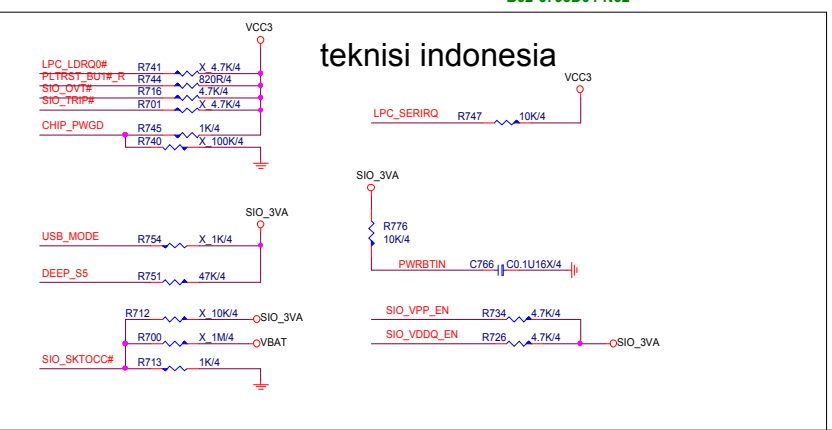
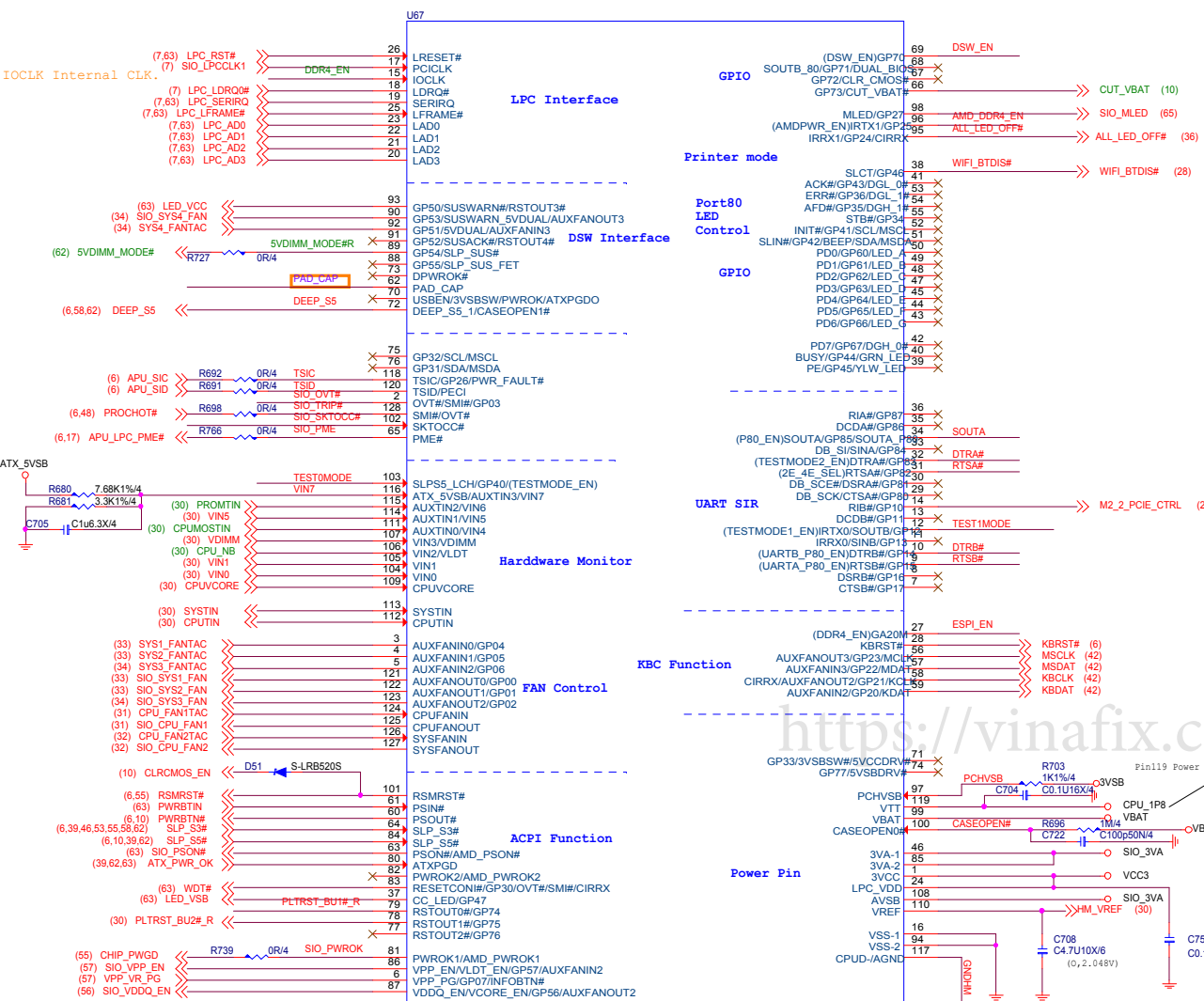


<https://vinafix.com>



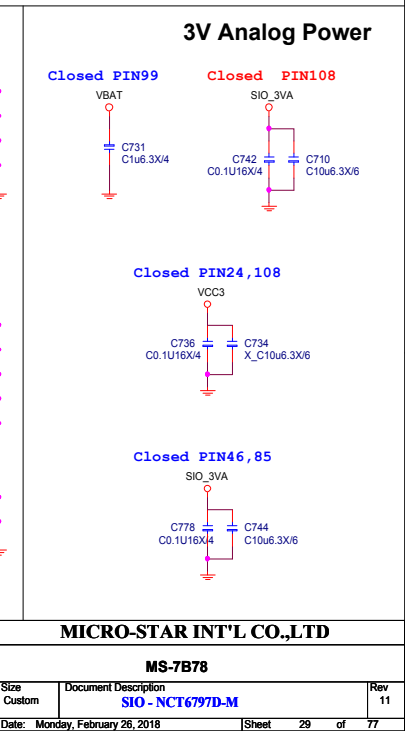
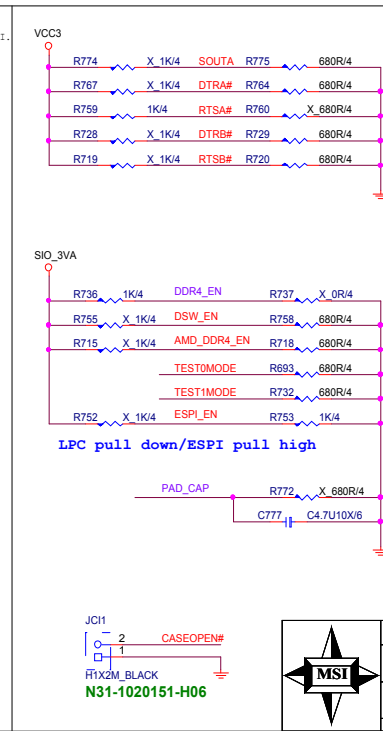



10uP+0.1uP+0.01uP at one end of socket in support of 3.3 V3V pins 2 and 4.
10uP+0.1uP+0.01uP at the other end of the socket in support of 3.3 V3V pins 70 and 72.



POWER ON STRAPPING PIN FOR NCT6797/6795					
PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE1_EN	TESTMODE1_EN	DISABLE TESTMODE1_EN	ENABLE TESTMODE1_EN	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	ESPI_EN	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMD_DDR4_EN	AMD_DDR4_EN	DISABLE AMD DDR4 PWR	ENABLE AMD DDR4 PWR	INTERNAL RSMRST
103	6795 TESTMODE_EN 6797 GP40	6795 WDT# 6797 WDT#	6795 DISABLE TESTMODE	6795 ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low, BIOS must programming LPT or GPIO





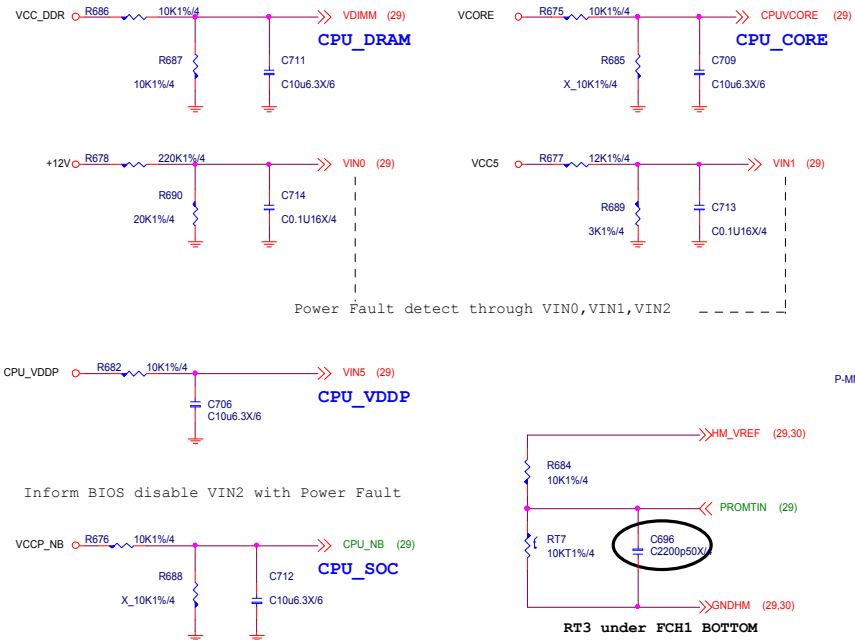
MICRO-STAR INT'L CO.,LTD

MS-7B78

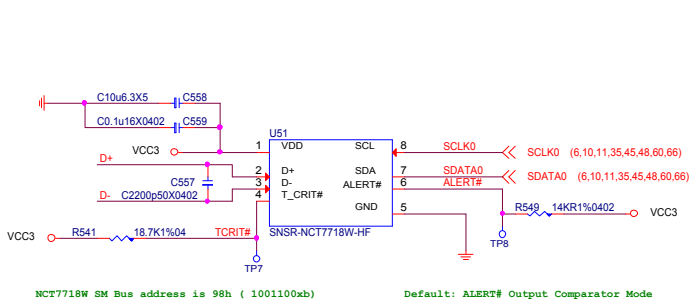
Size	Document Description	Rev
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HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect

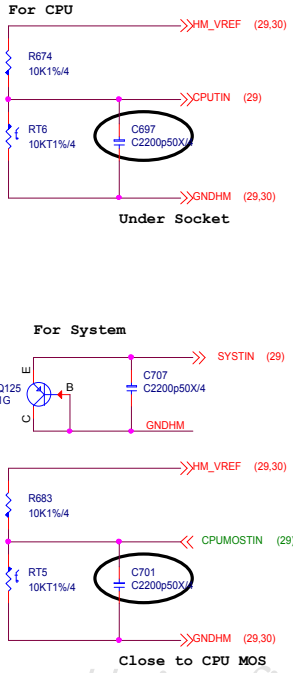


NCT7718W



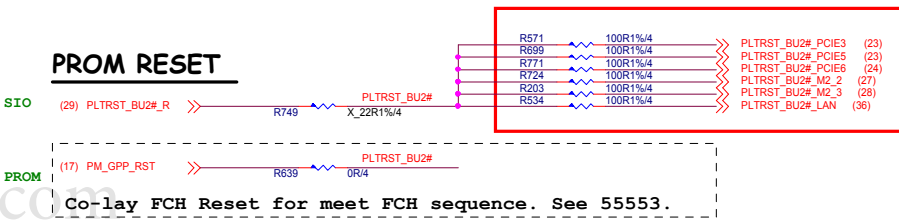
TEMPERATURE(℃)	T_CRIT#				
	2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107
	7.5KΩ	79	89	99	109
	10.5KΩ	81	91	101	111
	14KΩ	83	93	103	113
	18.7KΩ	85	95	105	115

TEMP SENSOR

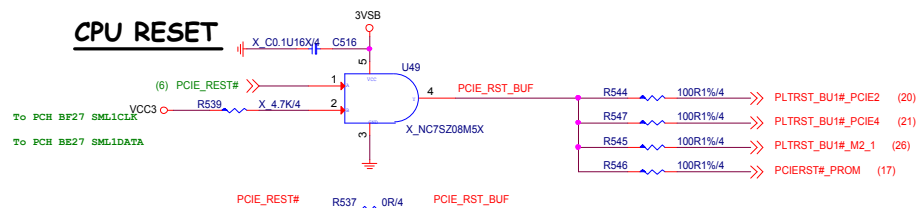


COM PORT

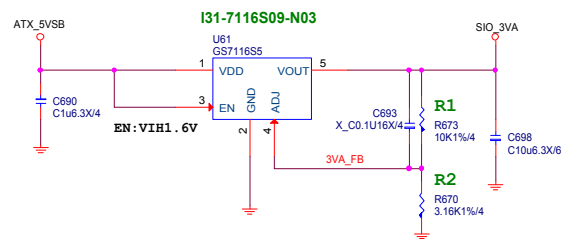
PROM RESET



CPU RESET



SIO_3VA



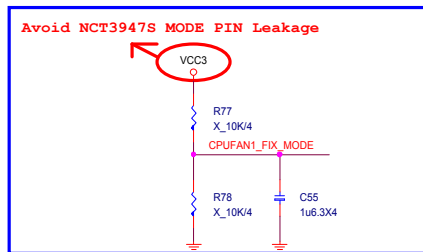
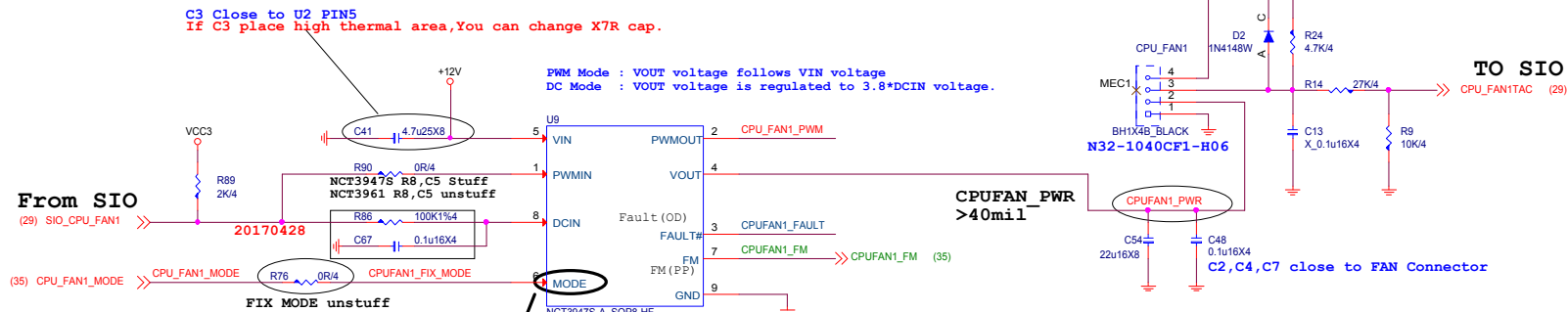
$$V_{out} = V_{ref} * (1 + (R1/R2)) = 0.8 * (1 + (10K/3.16K)) = 3.33V$$

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SIO - HW Monitor / NCT7718W		
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TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

- 1.PWM/DC/OCF LED
- 2.Mode GPIO BIOS can swtich PWM/DC MODE
- 3.OCP connect GPIO for BIOS Use
- 4.FM:BIOS can read FAN PWM/DC MODE
- 5.CPUFAN1_LED_OFF_BLINK Use LED On/OFF

CPUFAN1



Resever For FIX DC or PWM MODE USE By PM SPEC

GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI (Floating) Default

NCT3947S Internall pull up 1.65V

colay NCT3961

OCSET	R1
1.2~1.8A	100K
2.2~2.8A	49.9K
3.2~3.8A	10K

default
OC SET By PM SPEC
20170428



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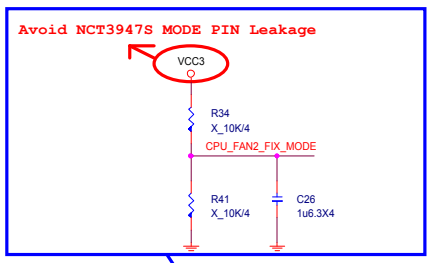
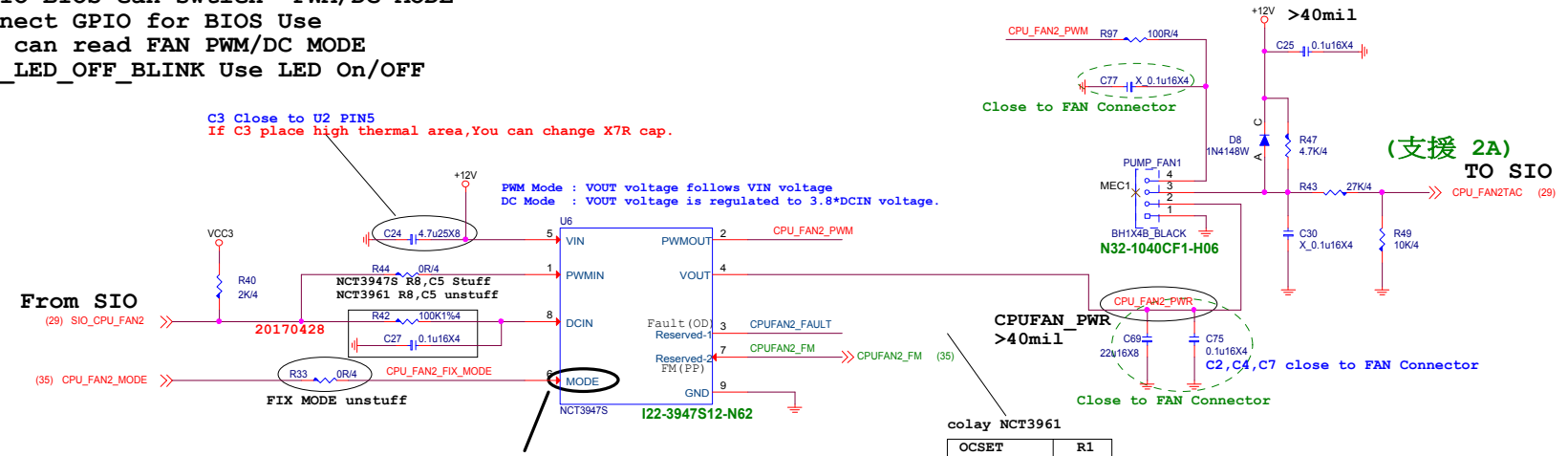
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Custom	FAN TYPE-J CPUDANI	11
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TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

- 1.PWM/DC/OCF LED
2.Mode GPIO BIOS can swtich PWM/DC MODE
3.OCF connect GPIO for BIOS Use
4.FM:BIOS can read FAN PWM/DC MODE
5.CPUFAN1_LED_OFF_BLINK Use LED On/OFF

PUMPFAN1



Resever For FIX DC or PWM MODE USE By FM SPEC

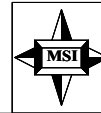
GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating)

NCT3947S Internall pull up 1.65V

colay NCT3961

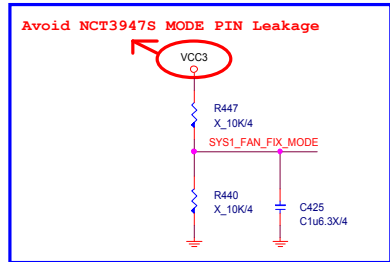
OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By FM SPEC
3.2~3.8A	10K	20170428



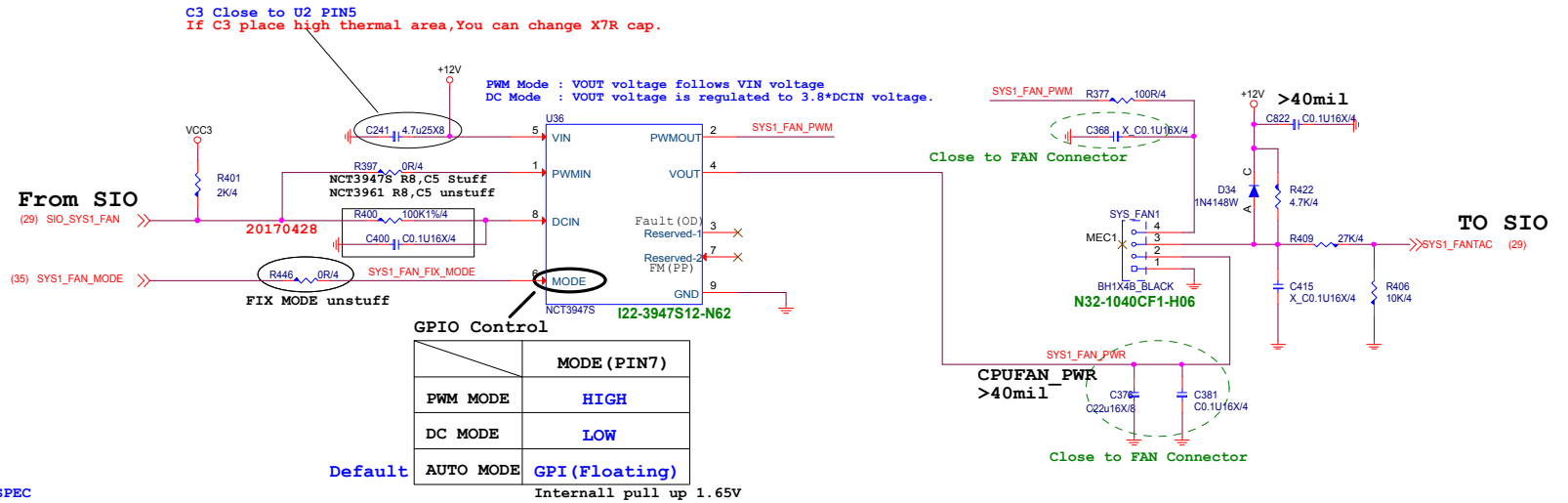
SYSFAN1

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



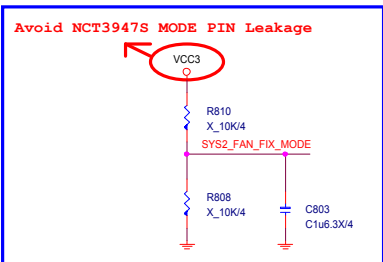
Resever For FIX DC or PWM MODE USE By FM SPEC



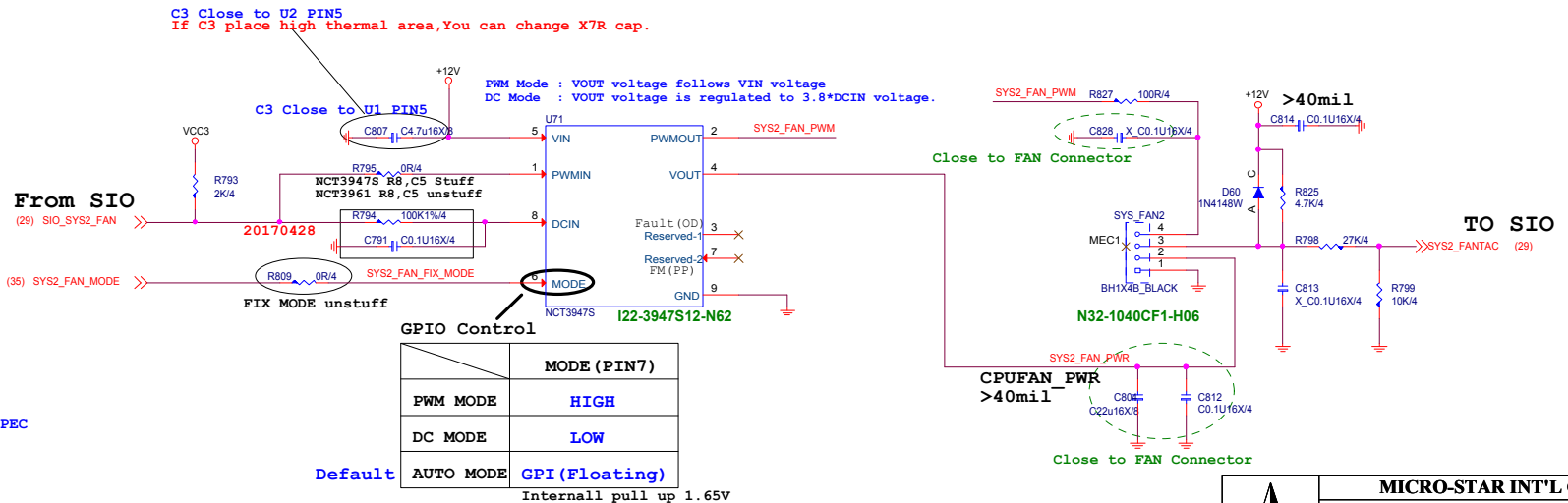
SYSFAN2

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



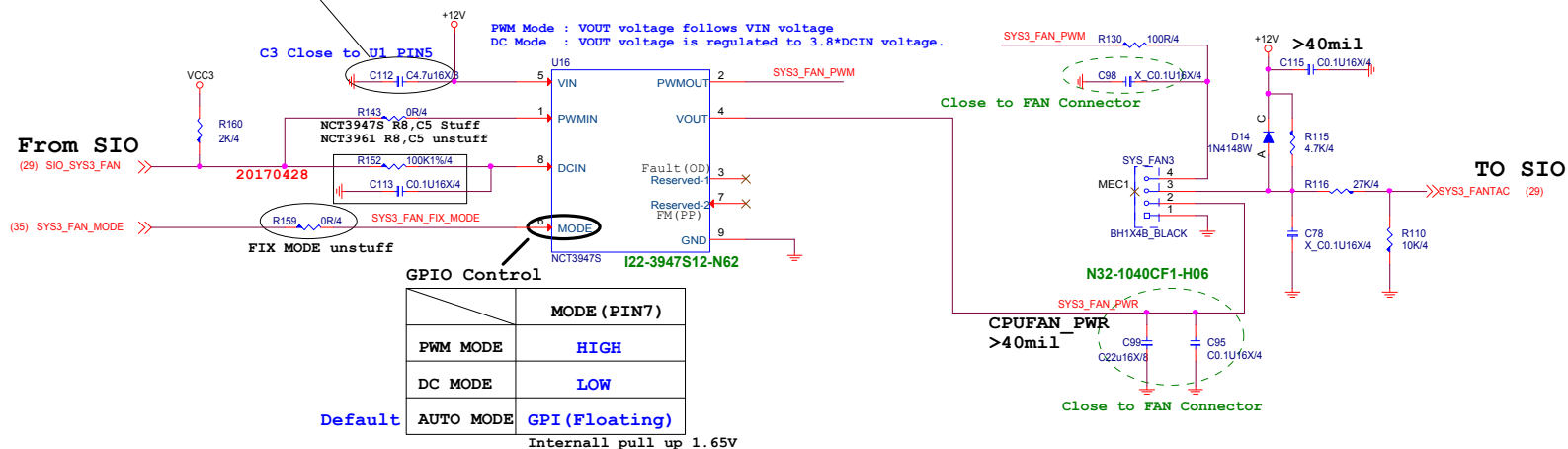
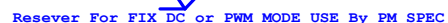
Resever For FIX DC or PWM MODE USE By FM SPEC



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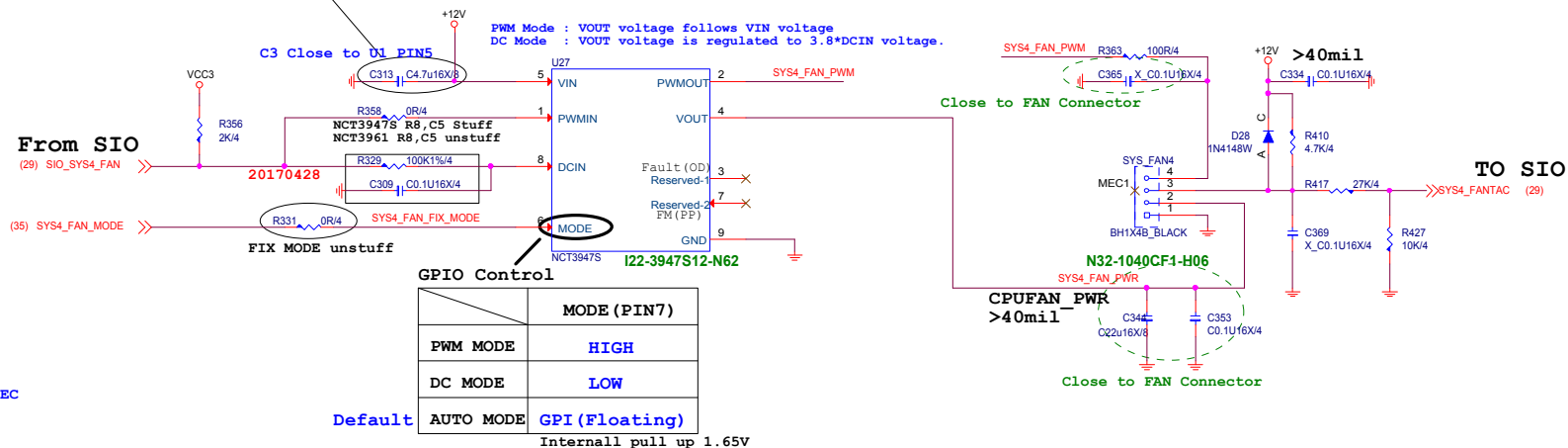
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

C3 Close to U2 PIN5
If C3 place high thermal area, You can change X7R cap.



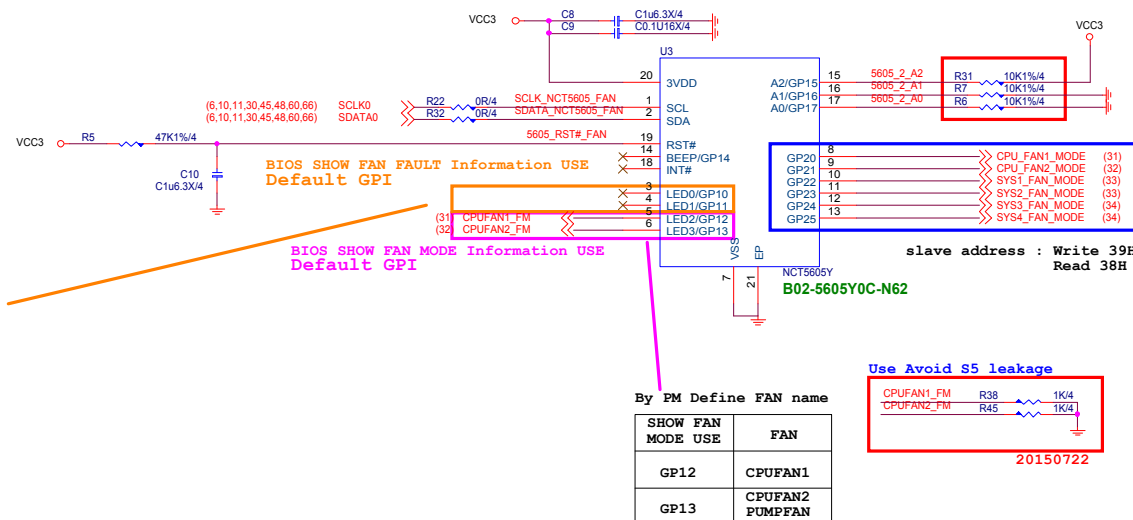
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

C3 Close to U2 PIN5
If C3 place high thermal area, You can change X7R cap.



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By PM Define FAN name

LED OFF BLINK	FAN
GP16	CPUFAN1
GP17	CPUFAN2 PUMPFAN

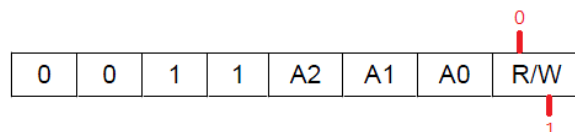
USE LED OFF & LED BLINK

Default GPI

1. GENERAL DESCRIPTION

The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPI/O pins. It also can provide SMBus™ address setting pins to set the address during power- on reset or from external reset.

NCT5605Y SMBus™ Address is:



<https://vinafix.com>

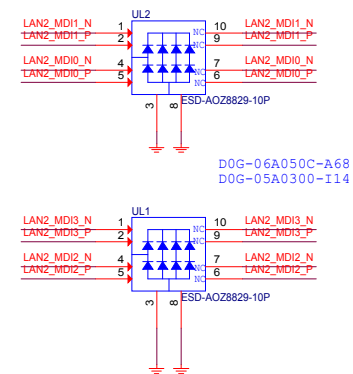
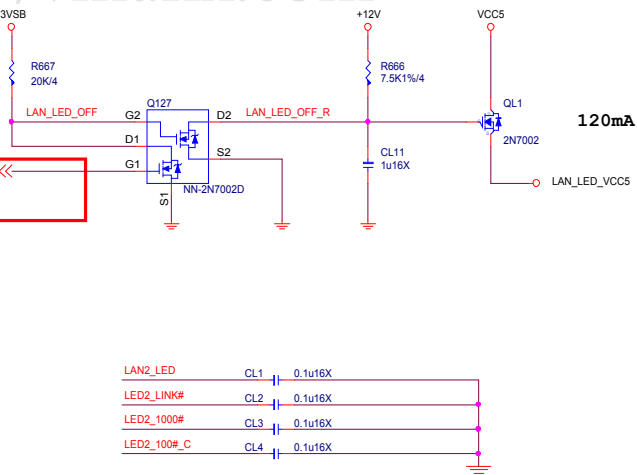
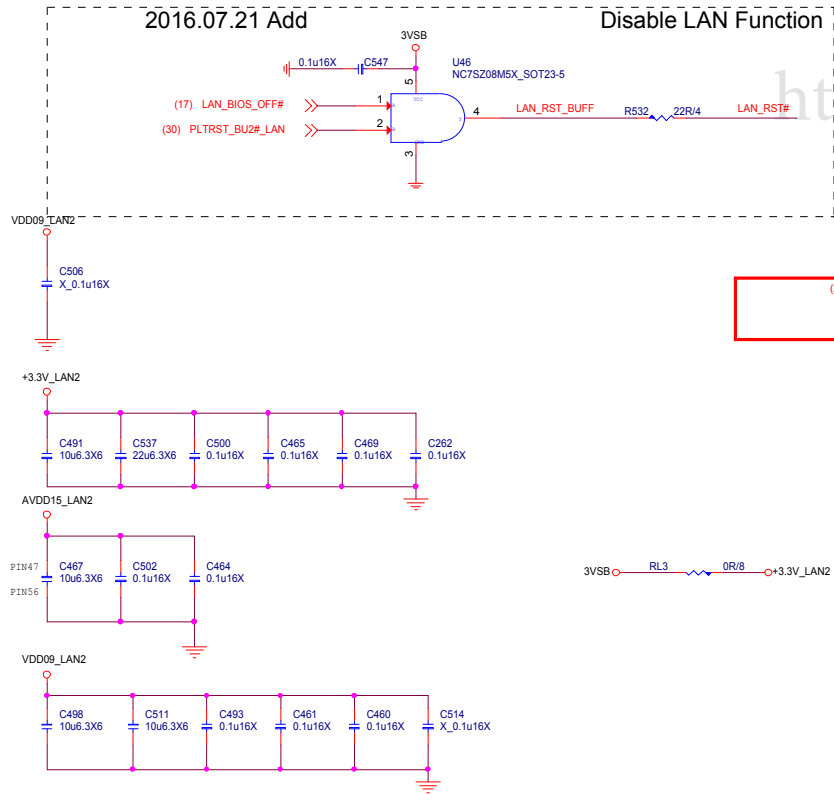
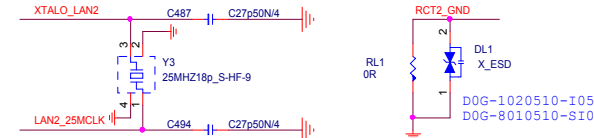
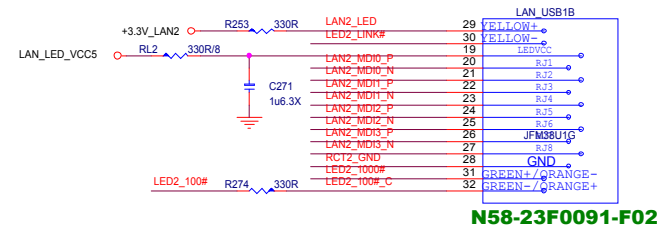
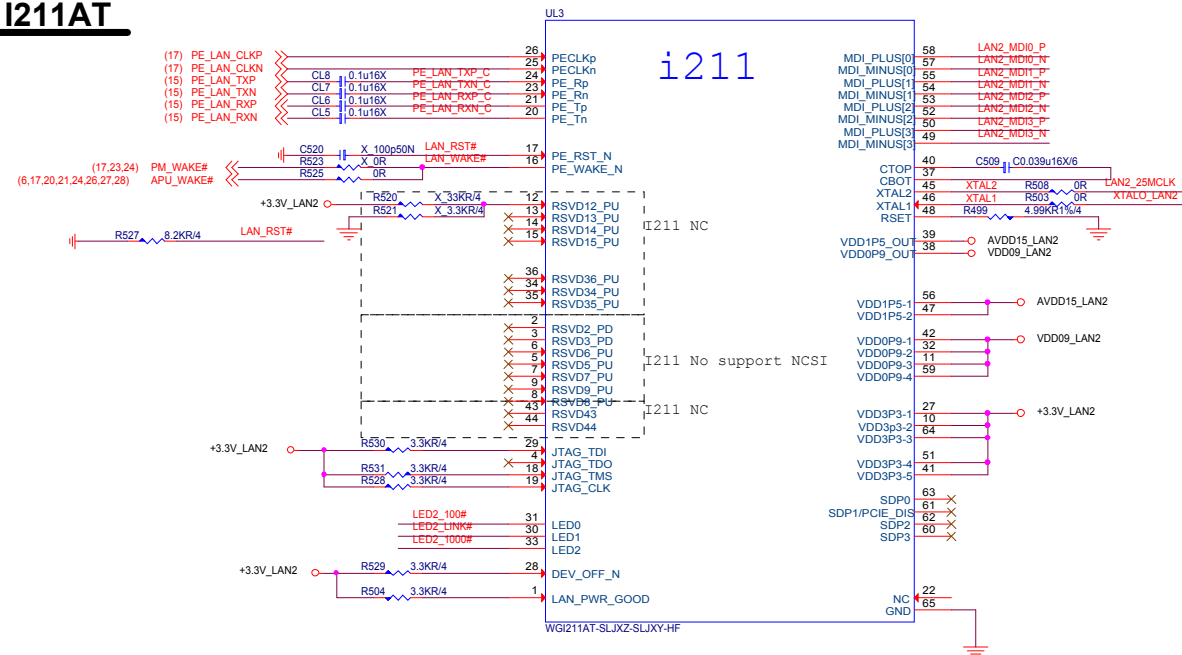


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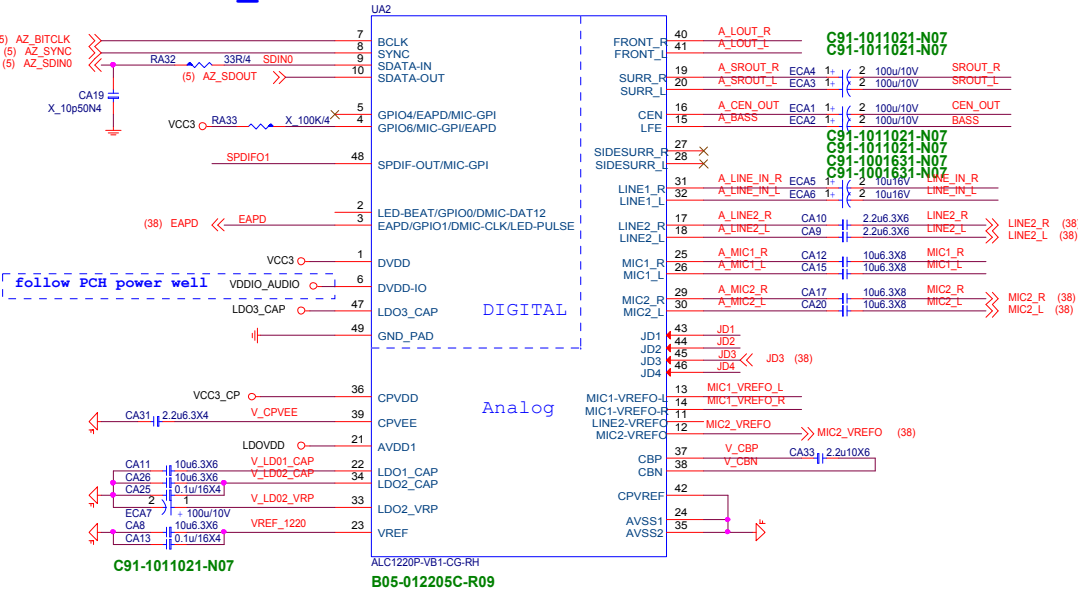
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	FAN GPIO NCT5605	
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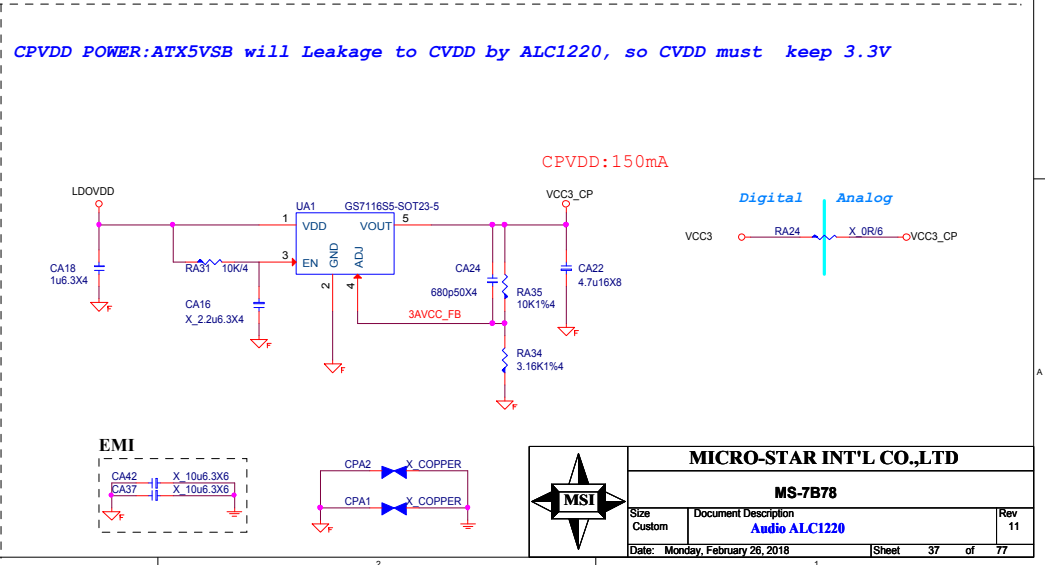
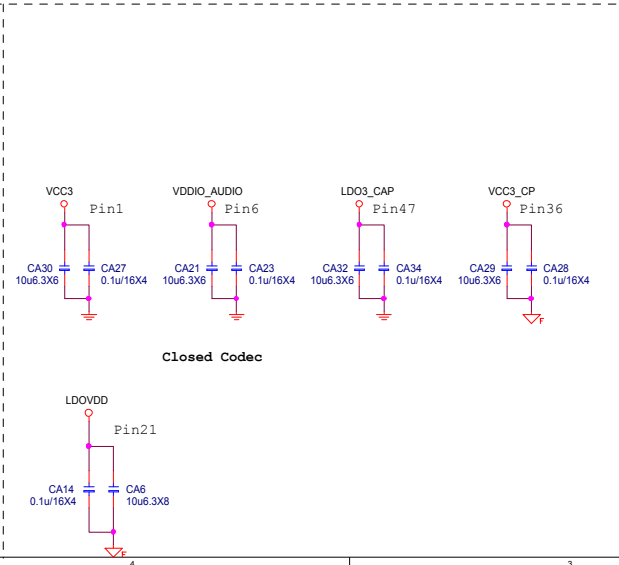
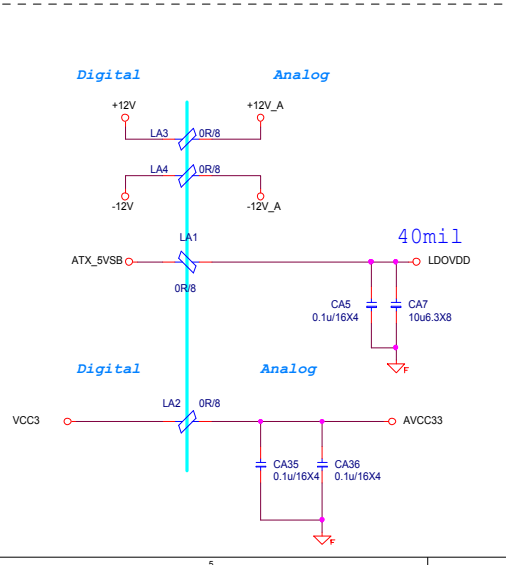
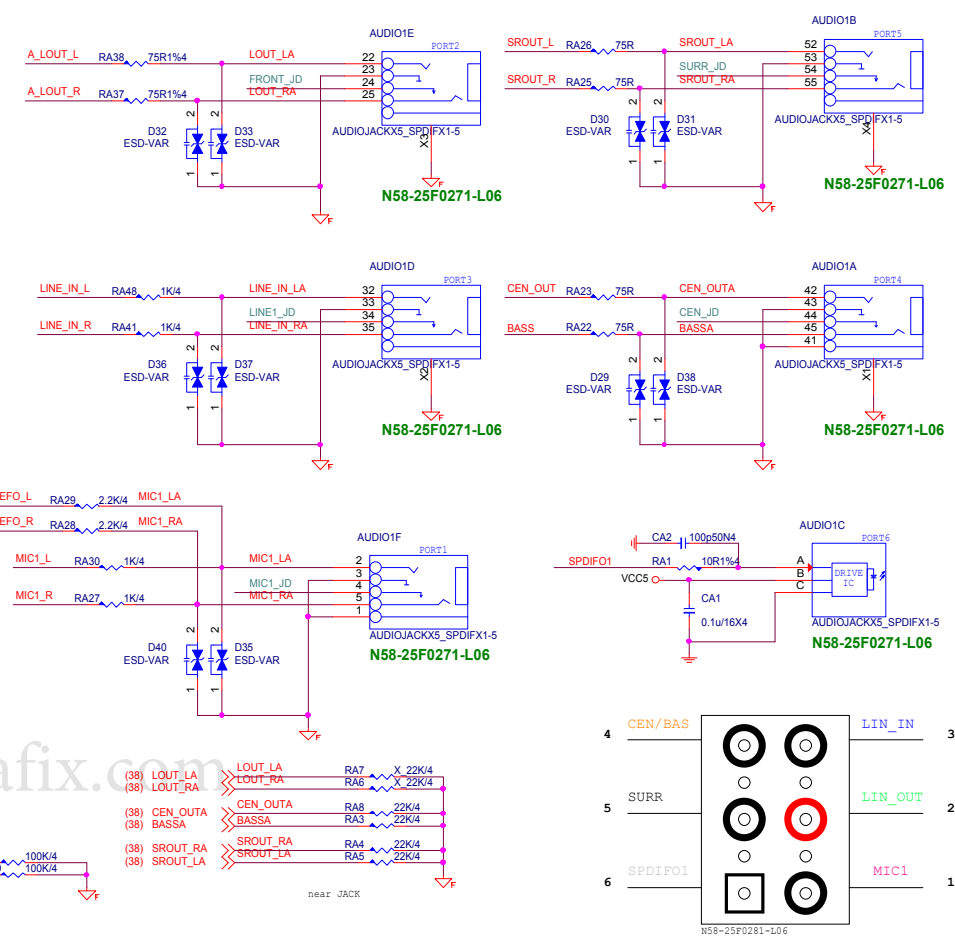
LAN-- I211AT

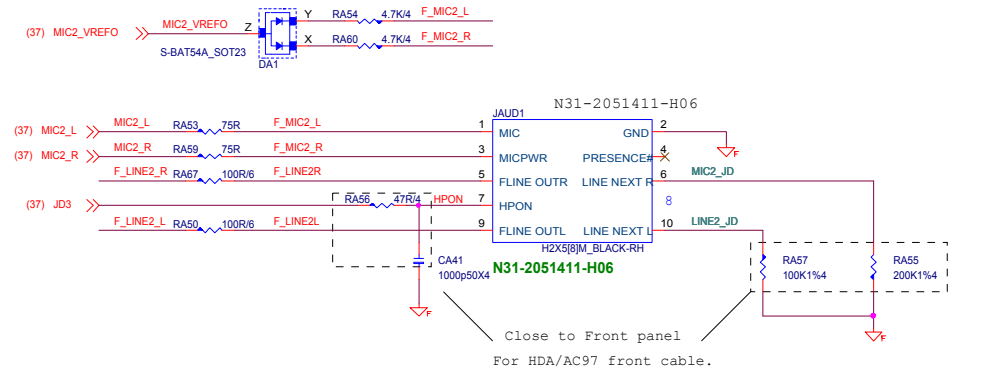
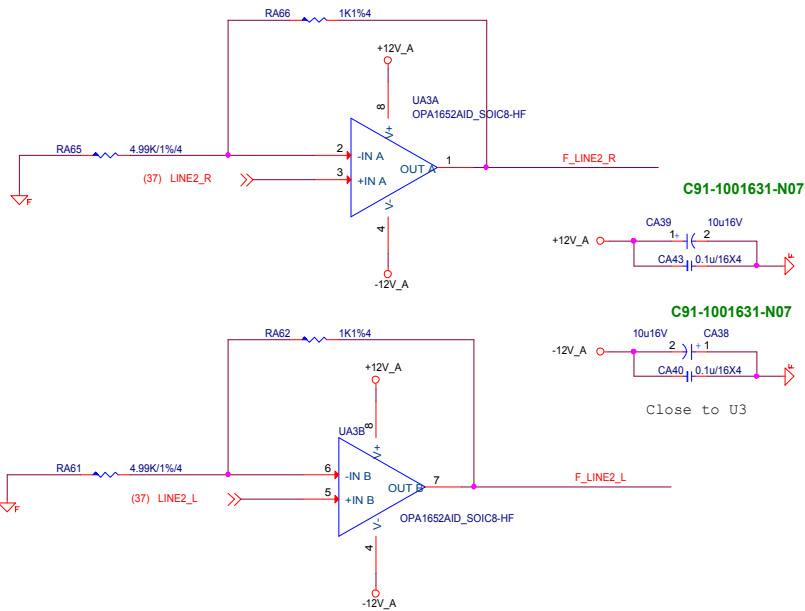


ALC1220P-VB1_48PIN

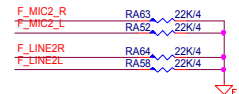
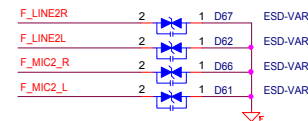


<https://vinafix.com>

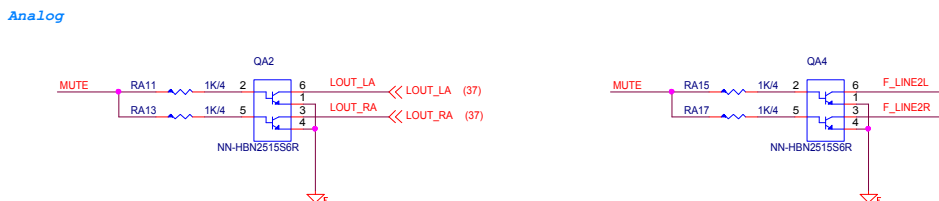
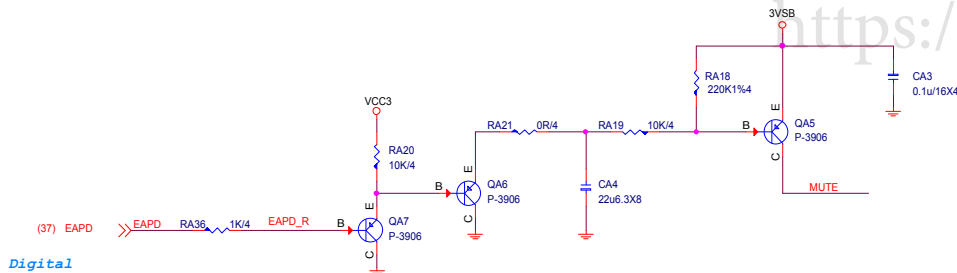




Close to Jack
ESD protect

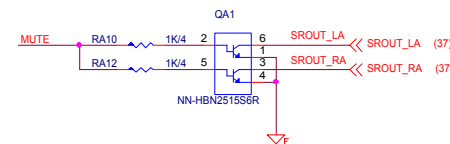
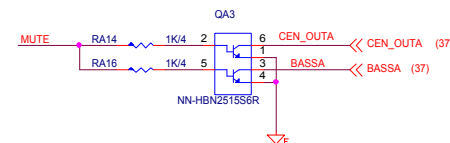


Rear Line OUT De-POP circuit (De-pop circuit for Rear Line out & Front Headphone out)



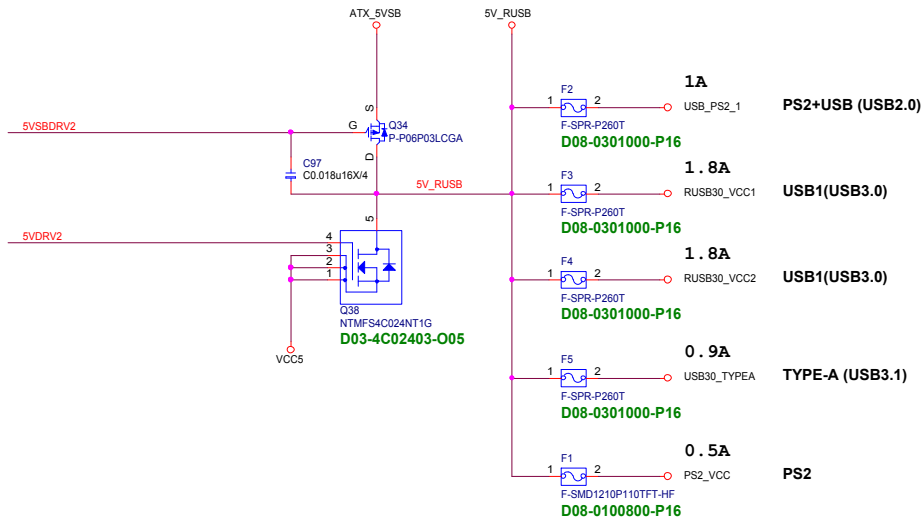
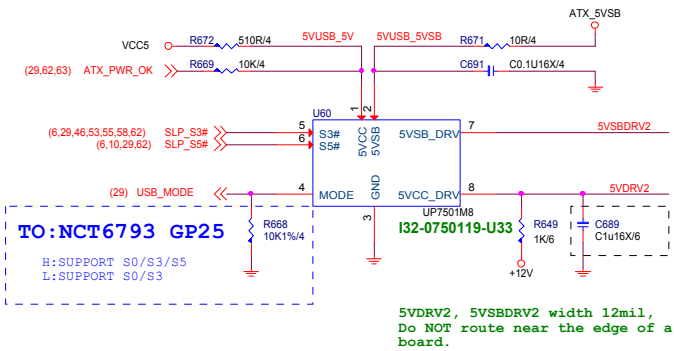
Audio moat is transparent and width 40mil

(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change SROUT_LA, SROUT_RA, CEN_OUTA, BASSA to TVS)



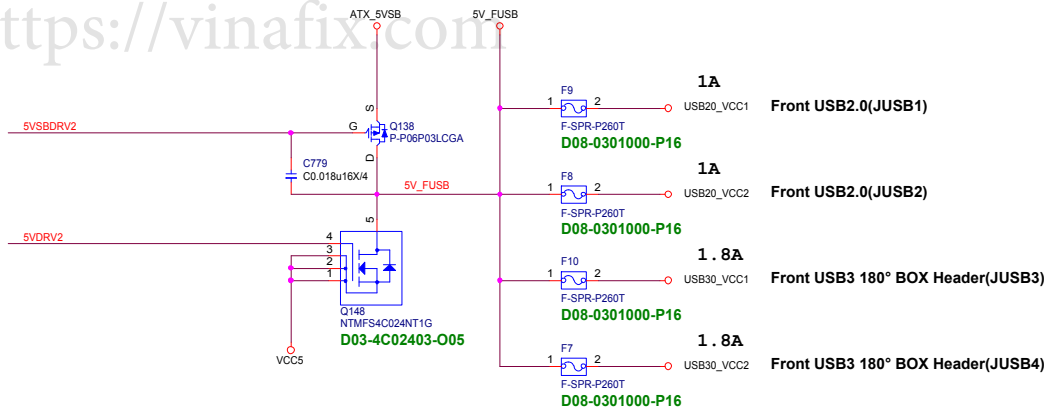
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USB Power



Rear (5.1A)

Front (5.6A)



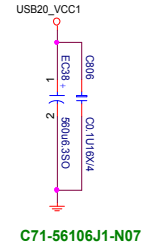
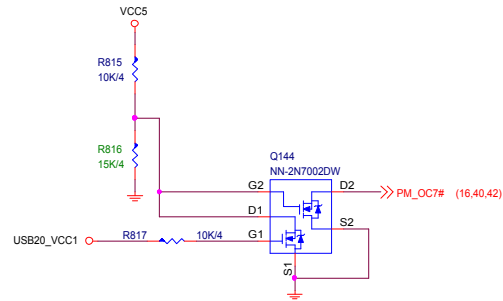
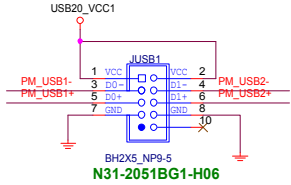
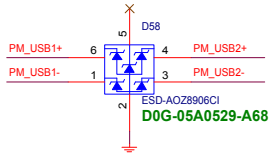
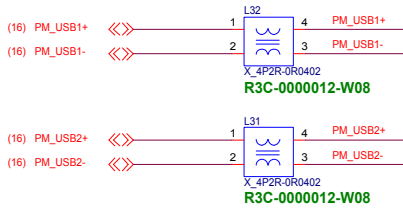
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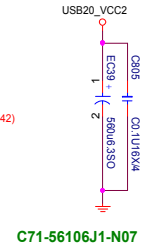
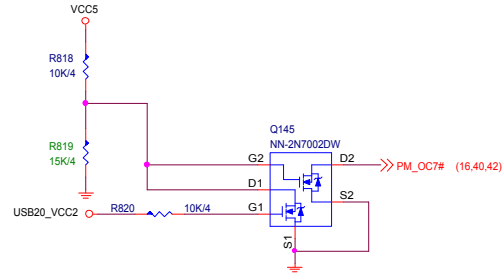
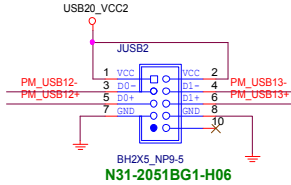
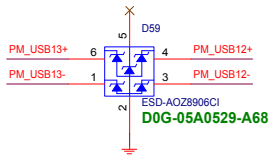
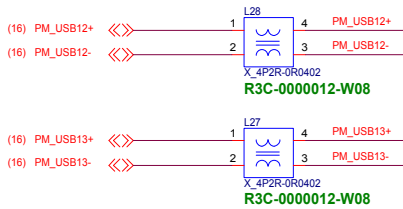
Front USB2.0 (JUSB1)

5V@1A



Front USB2.0 (JUSB2)

5V@1A

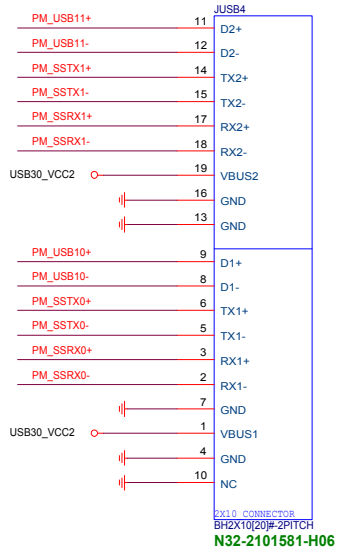
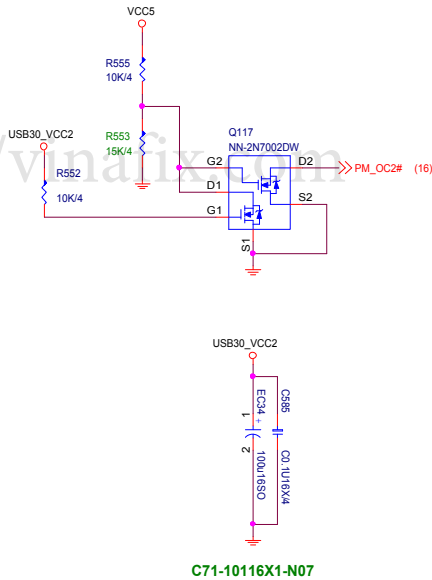
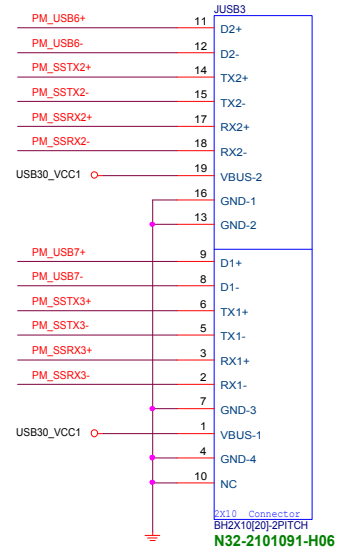
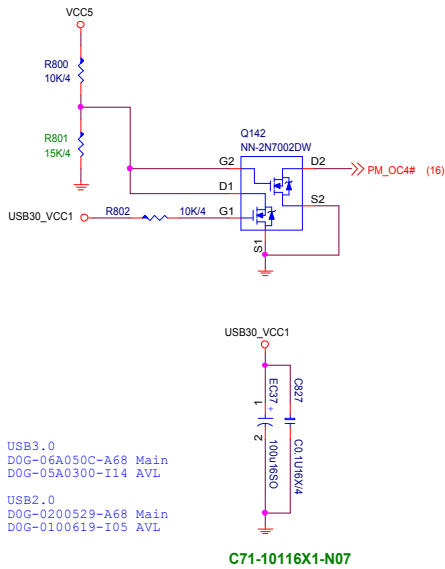
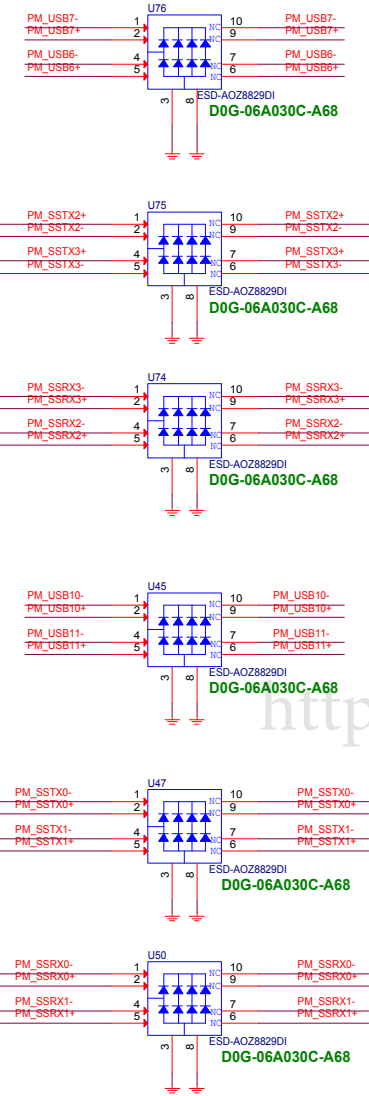
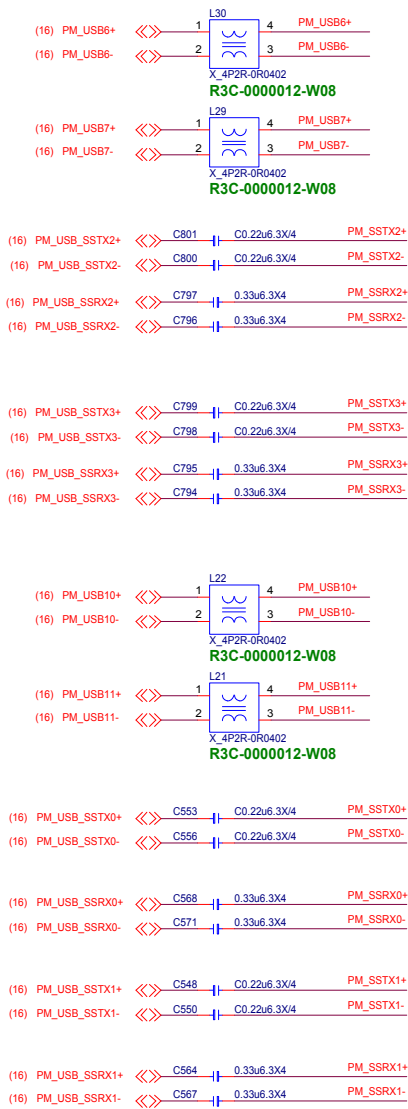


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Front USB3 180° BOX Header(JUSB3)
5V@1.8A

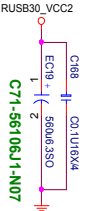
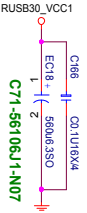
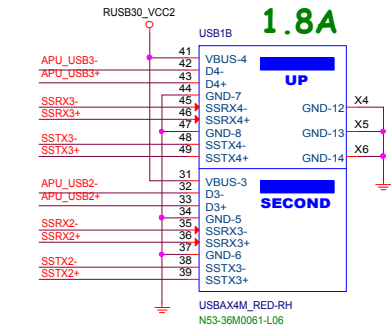
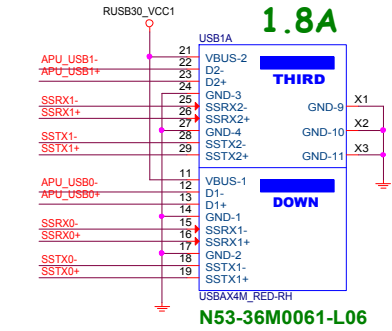
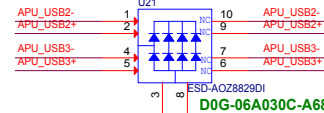
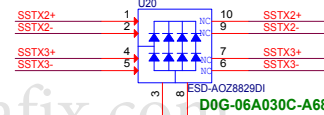
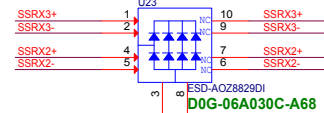
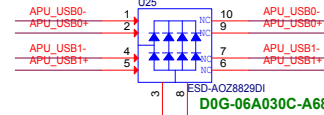
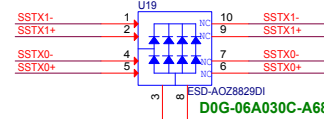
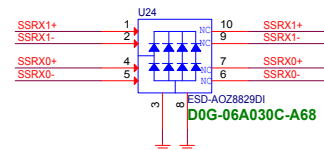
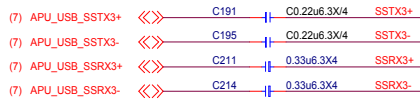
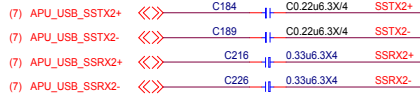
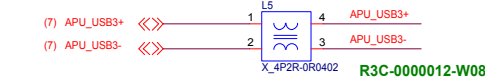
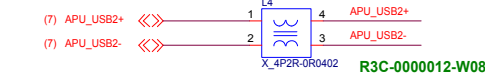
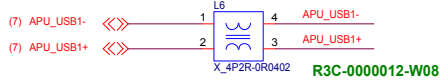
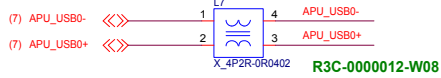


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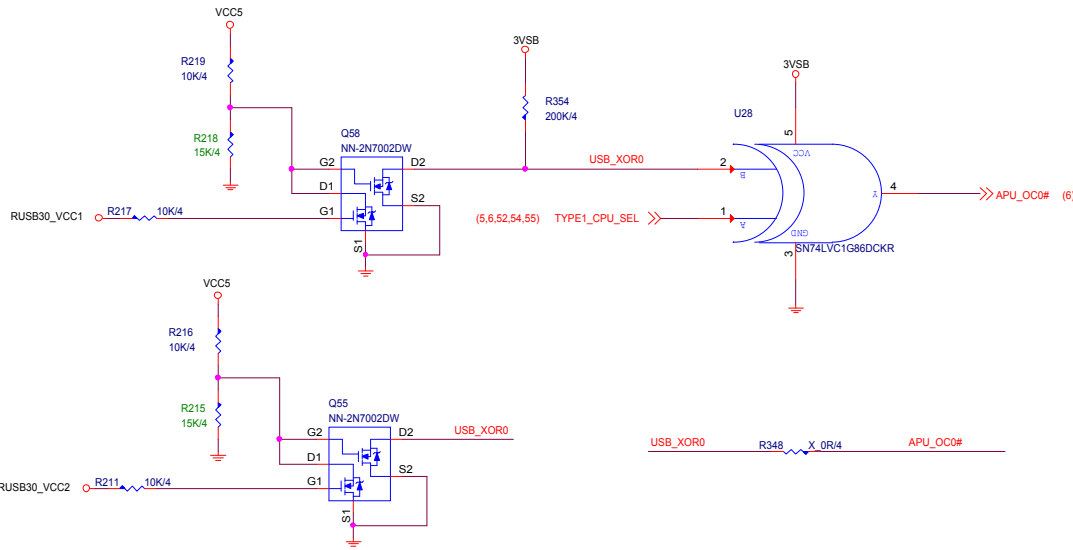
MS-7B78

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Rear USB3.0 GEN1 5V@1.8A



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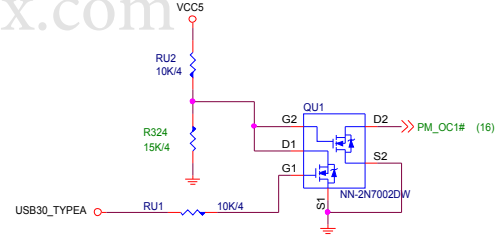
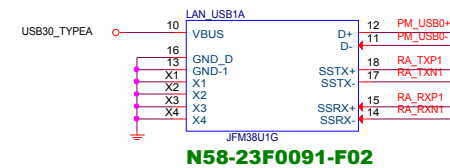
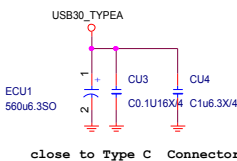
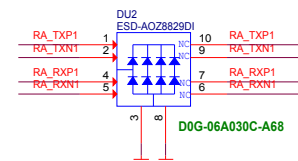
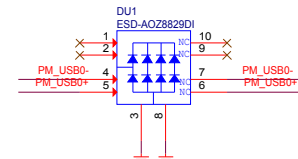
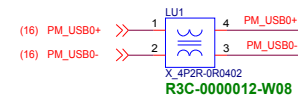
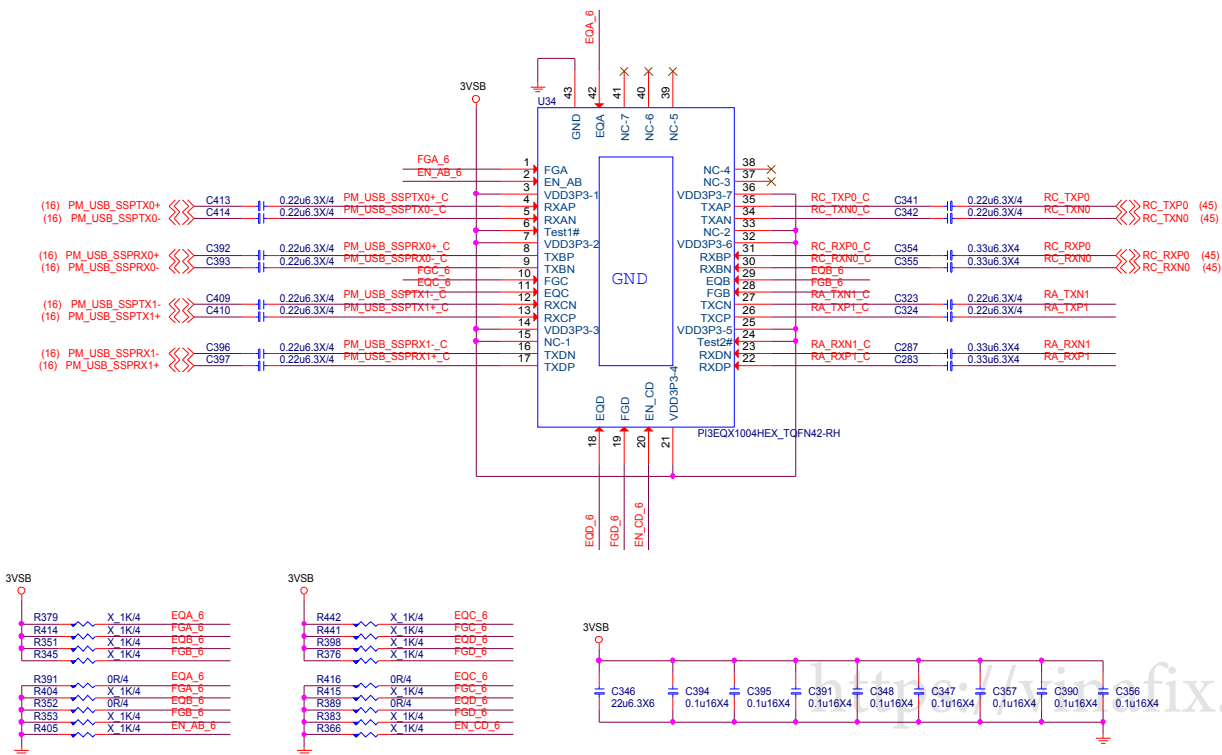


	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0



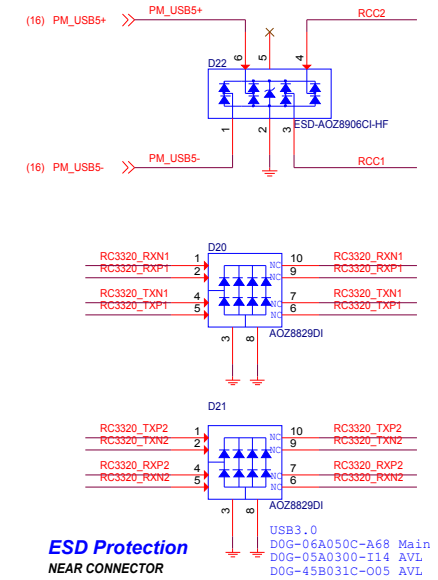
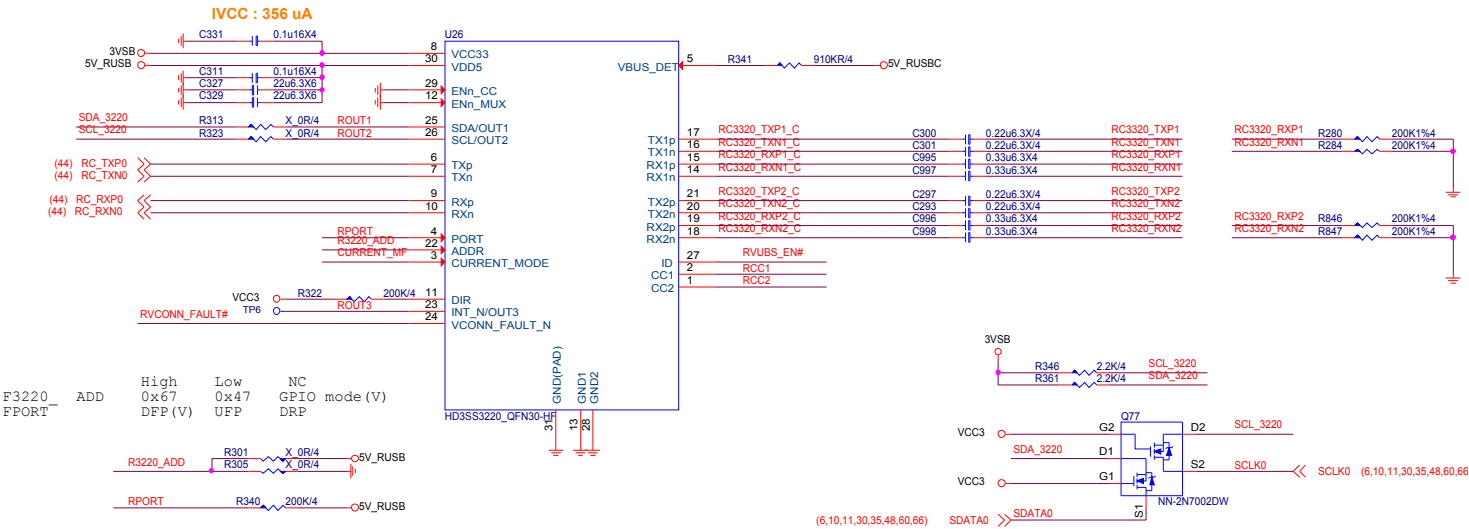
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TYPE-A PI3EQX1004 Redriver



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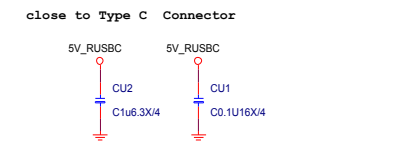
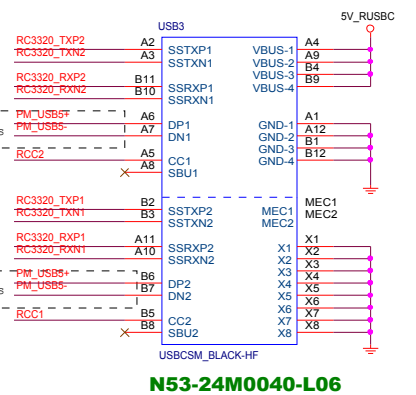
USB 3.1-Type-C USB Type-C MUX with Configuration Channel (CC)



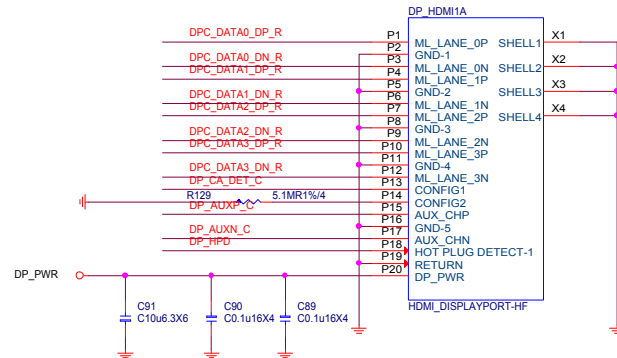
VBUS OC# LEVEL SHIFT

VCOM OC#

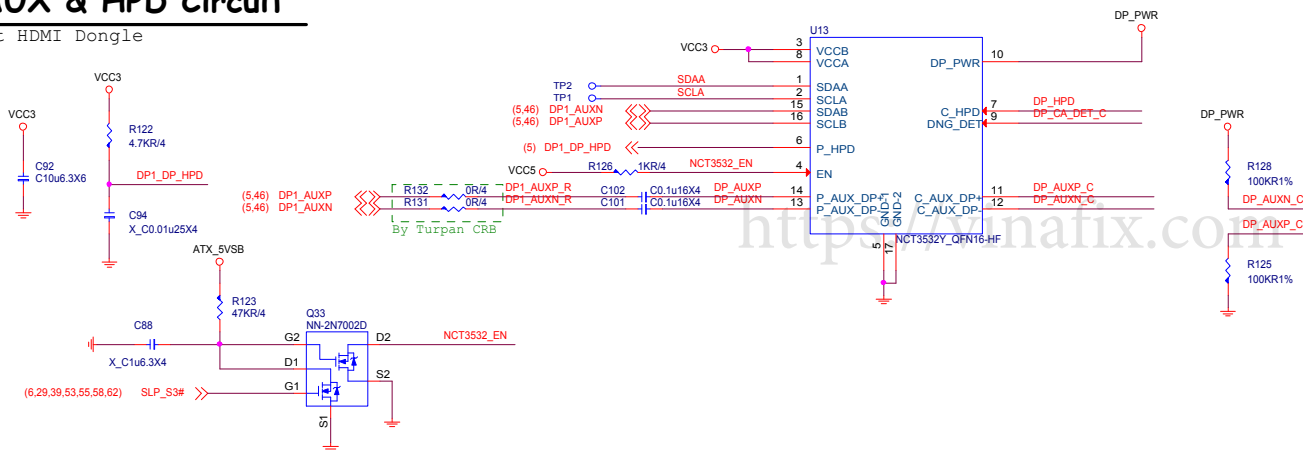
Current Mode



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[illegible]

Support HDMI Dongle



The diagrams illustrate the connection of DPC signals to the ESD-AOZ8906C, AOZ8829DI-03, and AOZ8829DI-03 components.

Top Diagram (ESD-AOZ8906C): Shows the connection of DPC_AUXP_C (pin 6) and DPC_AUXN_C (pin 1) to the ESD-AOZ8906C component. The component has pins 4 (D15), 3, and 5 (ESD-AOZ8906C). The signal lines are labeled DP_HPDI and DP_AVL. The component is connected to ground.

Middle Diagram (AOZ8829DI-03): Shows the connection of DPC_DATA1_DP_R (pin 1), DPC_DATA1_DN_R (pin 2), DPC_DATA3_DP_R (pin 4), and DPC_DATA3_DN_R (pin 5) to the AOZ8829DI-03 component. The component has pins 10, 9, 7, and 6. The signal lines are labeled DPC_DATA1_DP_R, DPC_DATA1_DN_R, DPC_DATA3_DP_R, and DPC_DATA3_DN_R. The component is connected to ground.

Bottom Diagram (AOZ8829DI-03): Shows the connection of DPC_DATA2_DN_R (pin 1), DPC_DATA2_DP_R (pin 2), DPC_DATA0_DP_R (pin 4), and DPC_DATA0_DN_R (pin 5) to the AOZ8829DI-03 component. The component has pins 10, 9, 7, and 6. The signal lines are labeled DPC_DATA2_DN_R, DPC_DATA2_DP_R, DPC_DATA0_DP_R, and DPC_DATA0_DN_R. The component is connected to ground.



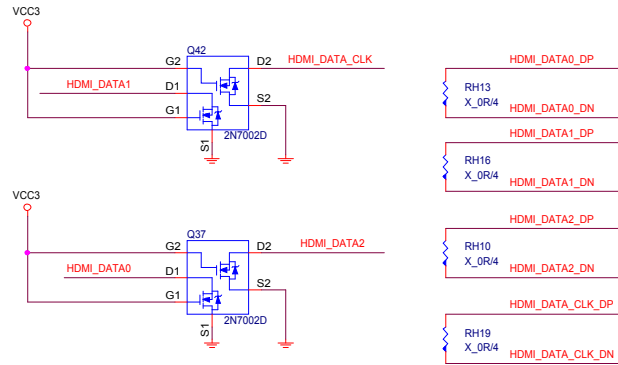
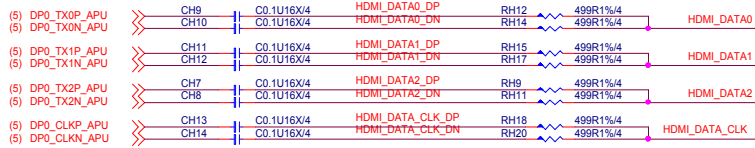
MICRO-STAR INT'L CO.,LTD

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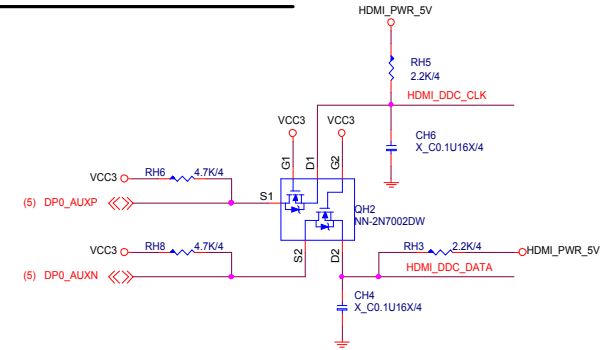
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HDMI CONNECTOR

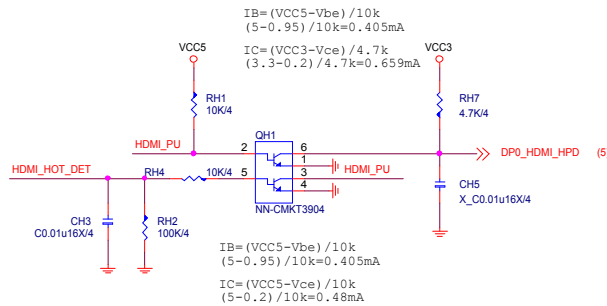
For HDMI 1.4



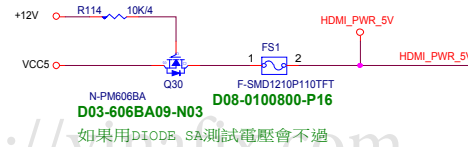
AUX Level Shifter



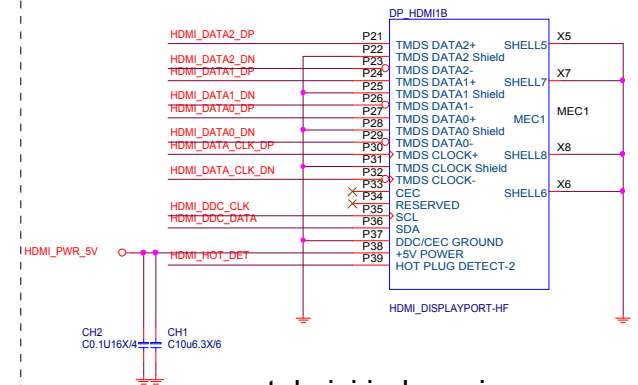
HPD Circuit



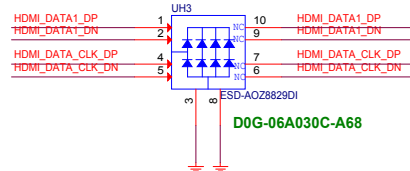
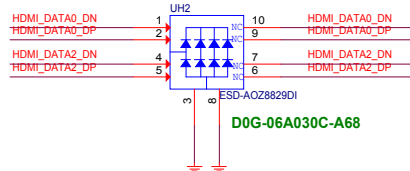
Connector Power



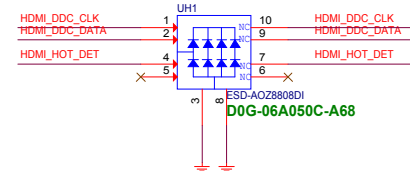
Connector



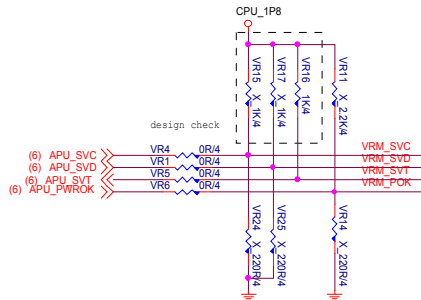
For EMI



注意:耐壓5v零件

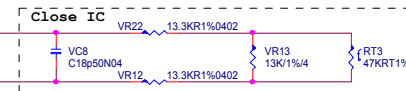
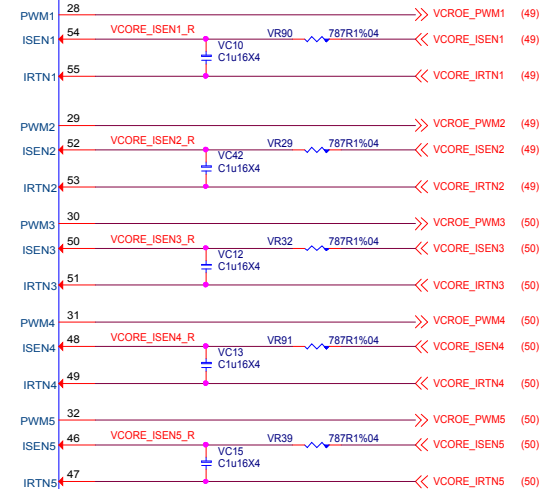
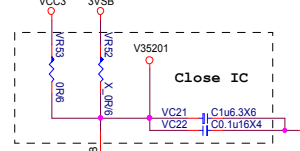
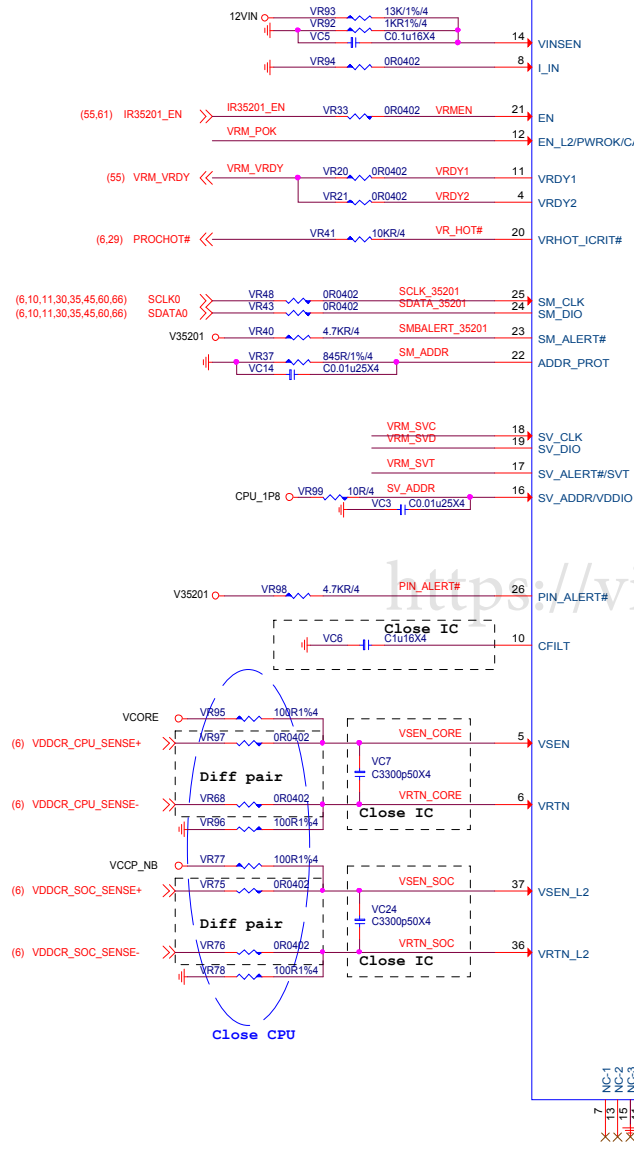
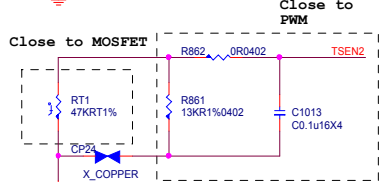
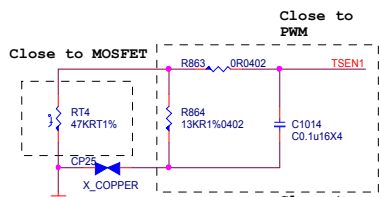
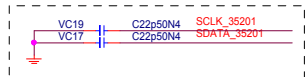
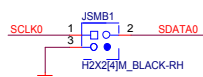
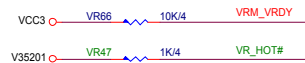


tekni indonesia

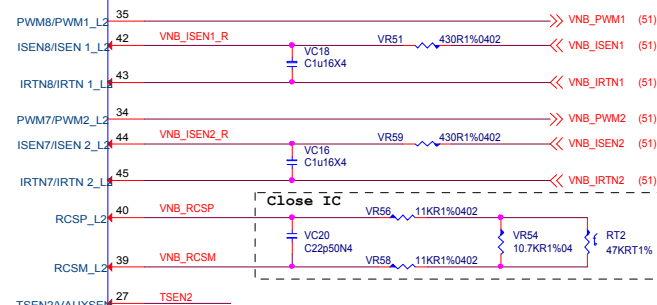


Note:VID Override Circuit

BOOT VOLTAGE		Pre_PWROK Metal VID
SVC	SVD	
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



RT close to Choke



RT close to Choke

0x26: RH=18K, RL=13K

	VR53	VR54	VC20	VR58	VR57	VR59	VR60
Default	Temp	6.49k	10k	100p	X	0R	X
	VAUXSEN	5.76k	1k	0.01u	0R	X	0R

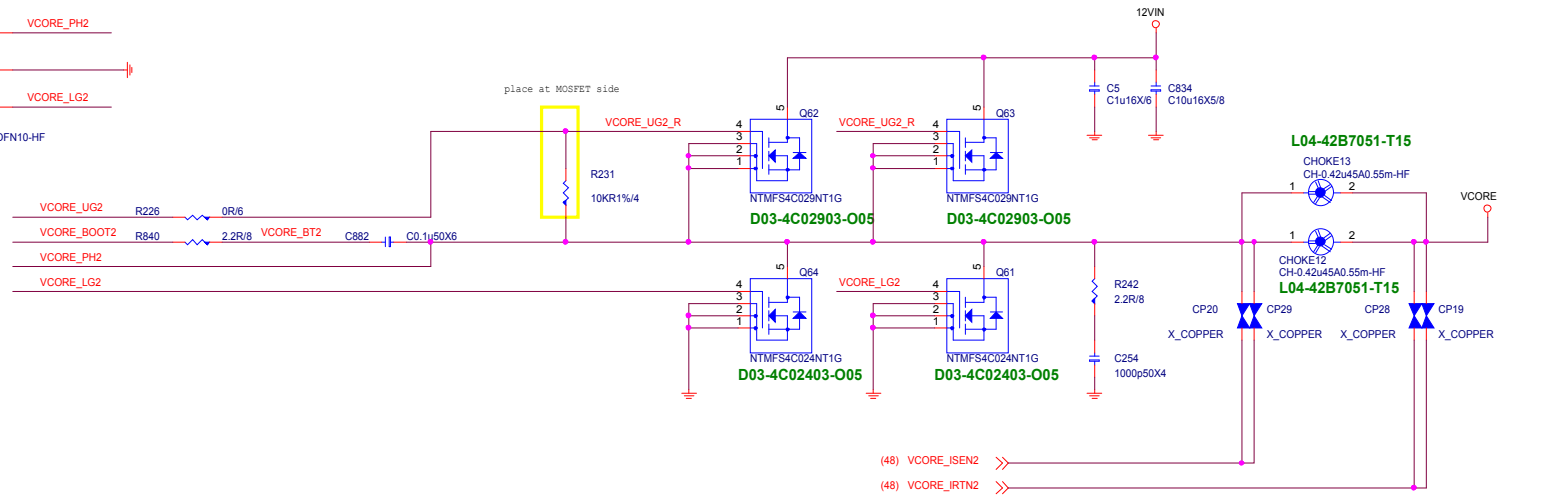
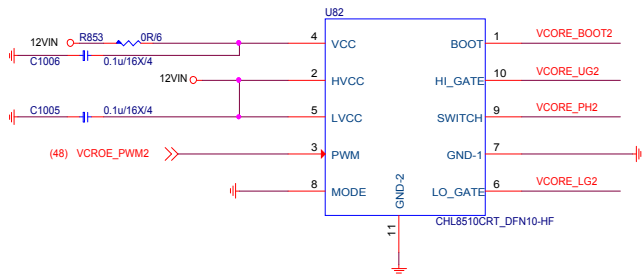
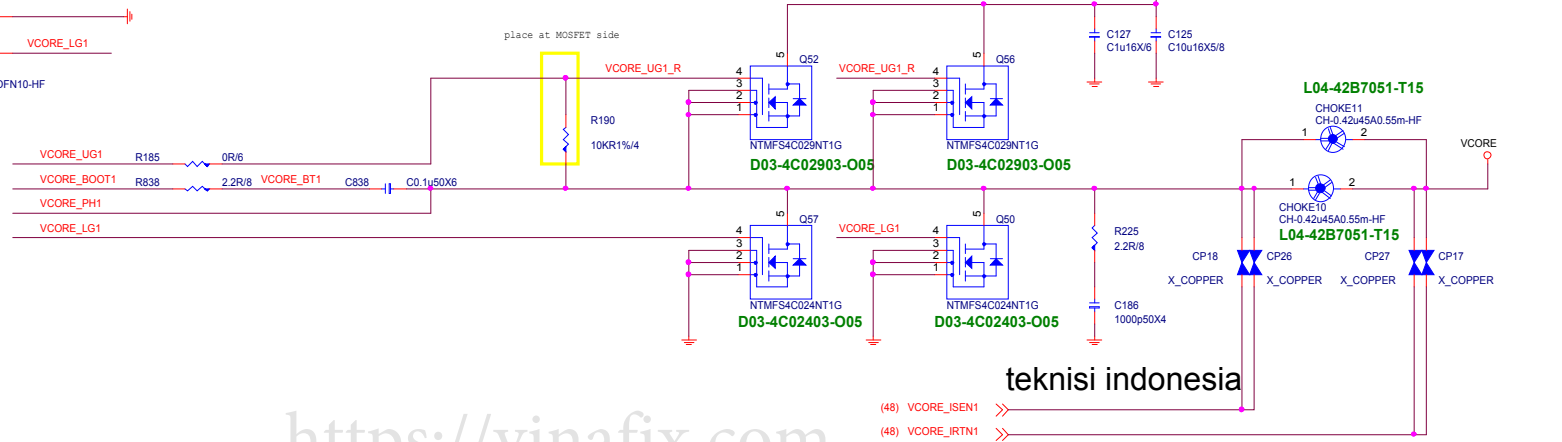
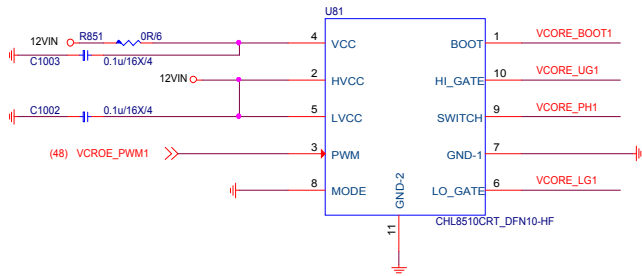


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VCORE 105W TDC:95A EDC:140A



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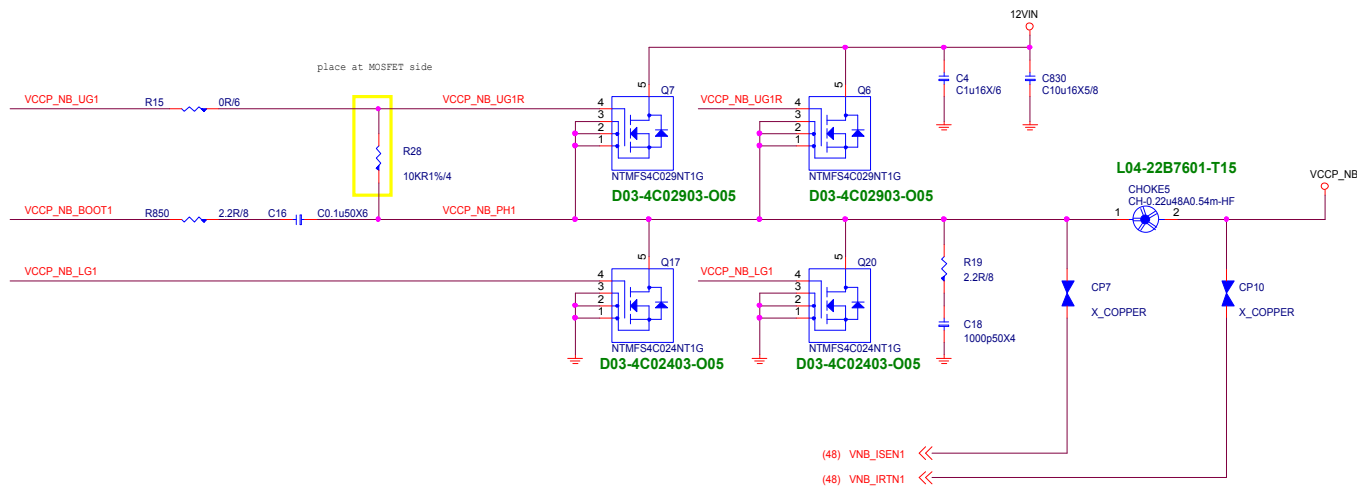
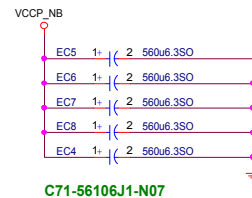
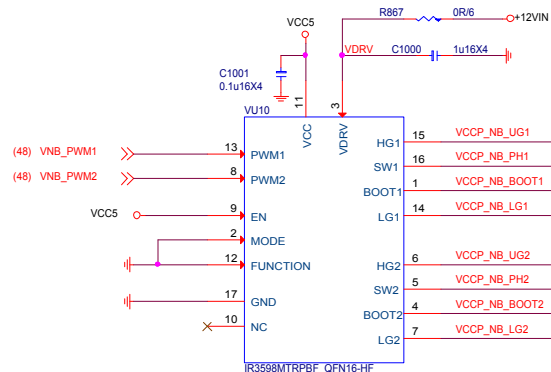
MS-7B78

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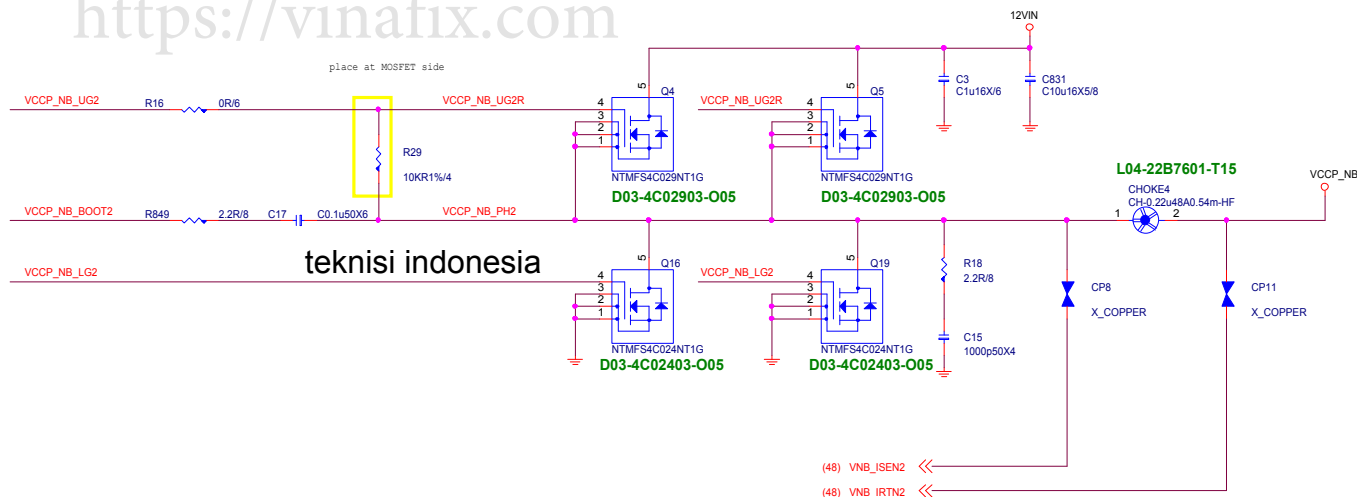
VCCP_NB 105W TDC:50A EDC:75A

Table for IR3598			
Function	Mode	PWM Mode	Phase Mode
0	1	IR ATL	Dual
1	1	IR ATL	Doubler
0	0	Tri-State	Dual
1	0	Tri-State	Doubler

SOC
Vcore



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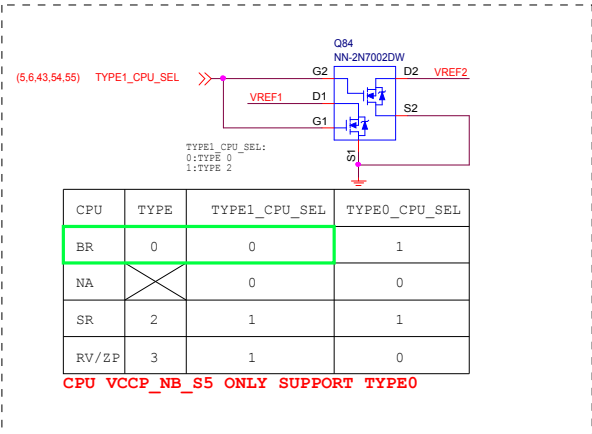
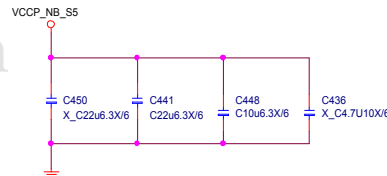
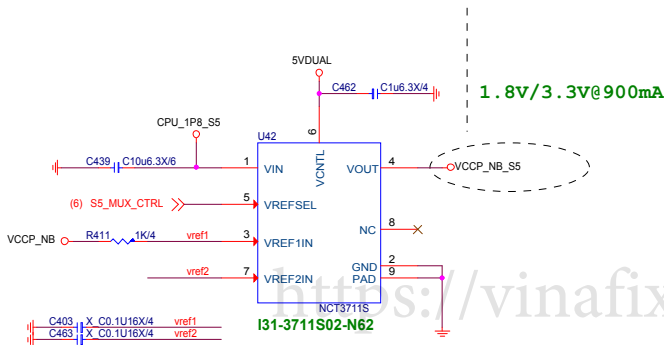
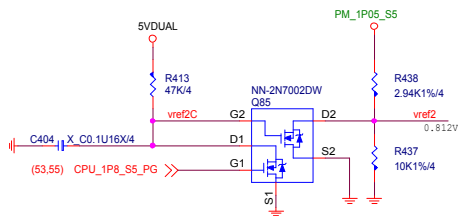


FOR
VCCP_SOC_S5

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V), VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)



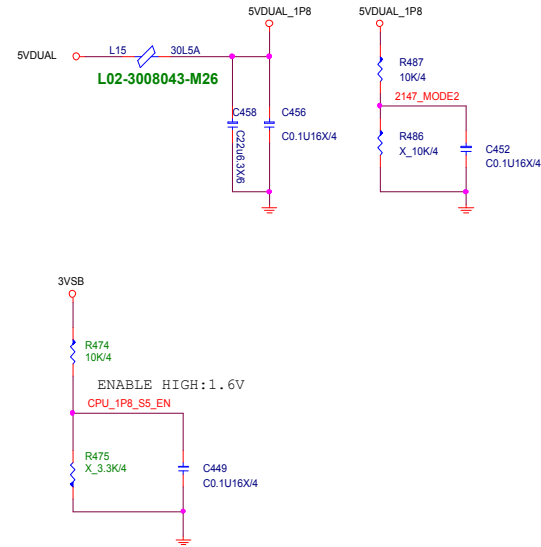
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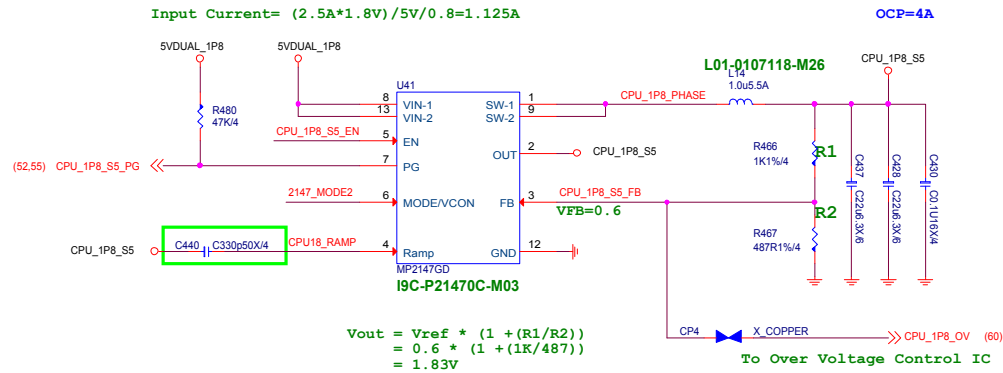
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CPU 1.8V S5 @0.5A

1.8V S5@0.5A

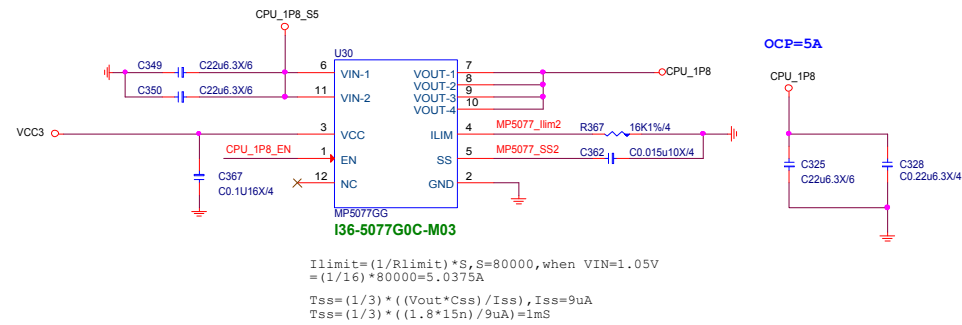
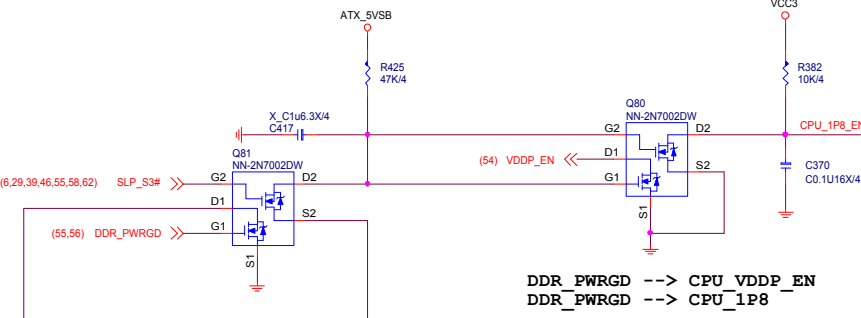


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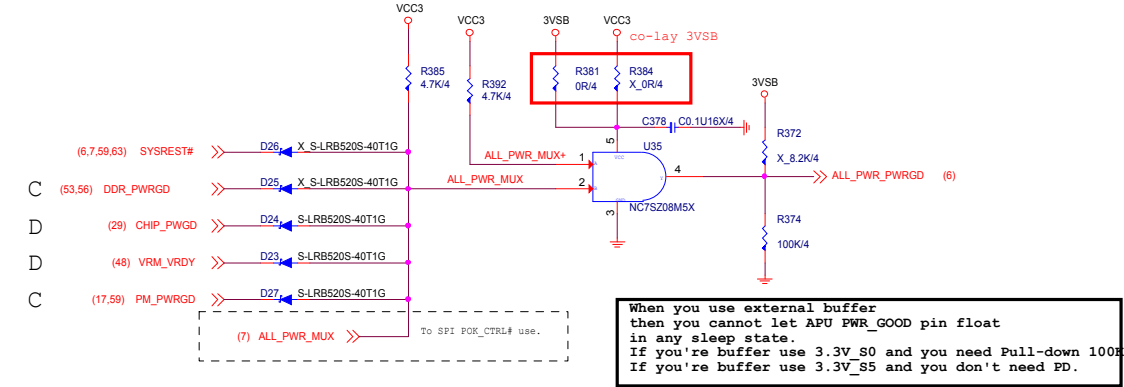
CPU 1.8V S0

1.8V@2A

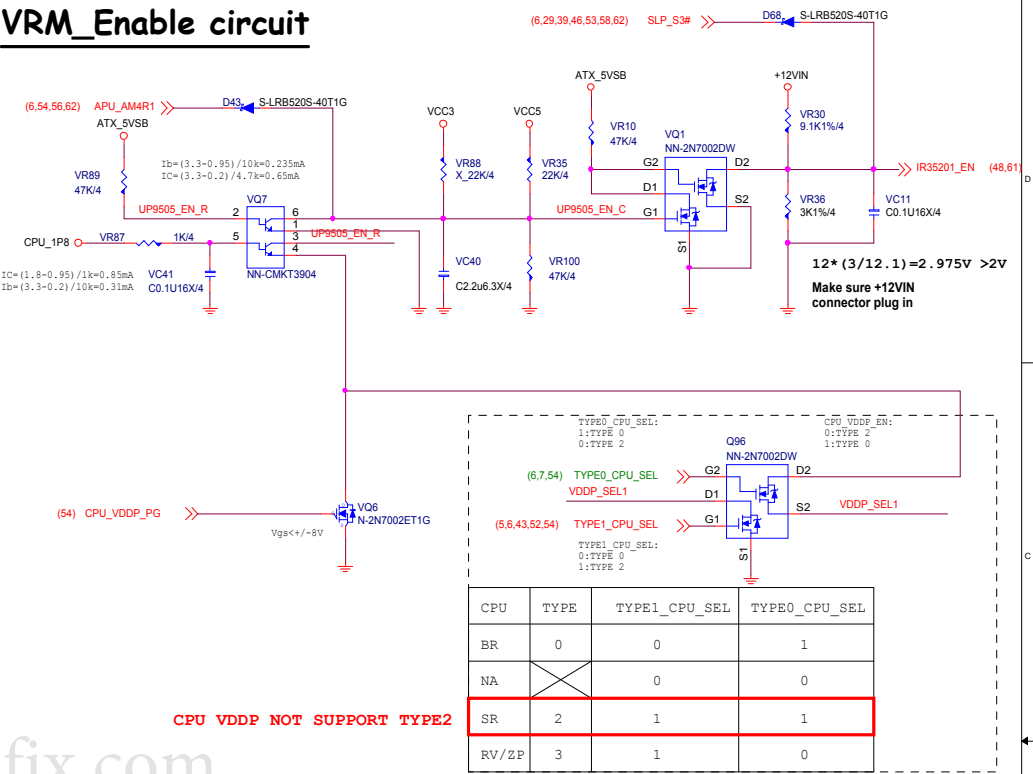


ALL POWER GOOD MUX

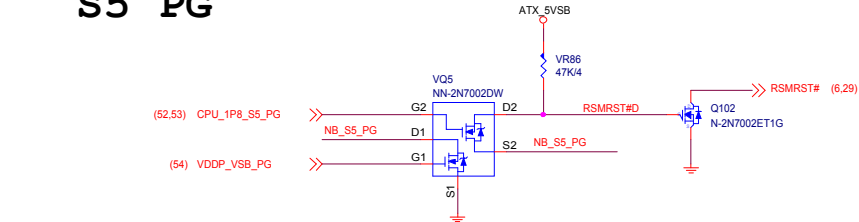
S0 PG



VRM_Enable circuit



S5 PG



DDR4_1.2V@26.2A

15.5A FOR CPU

9.5A FOR 4DIMM

1.2A FOR DDR VTT

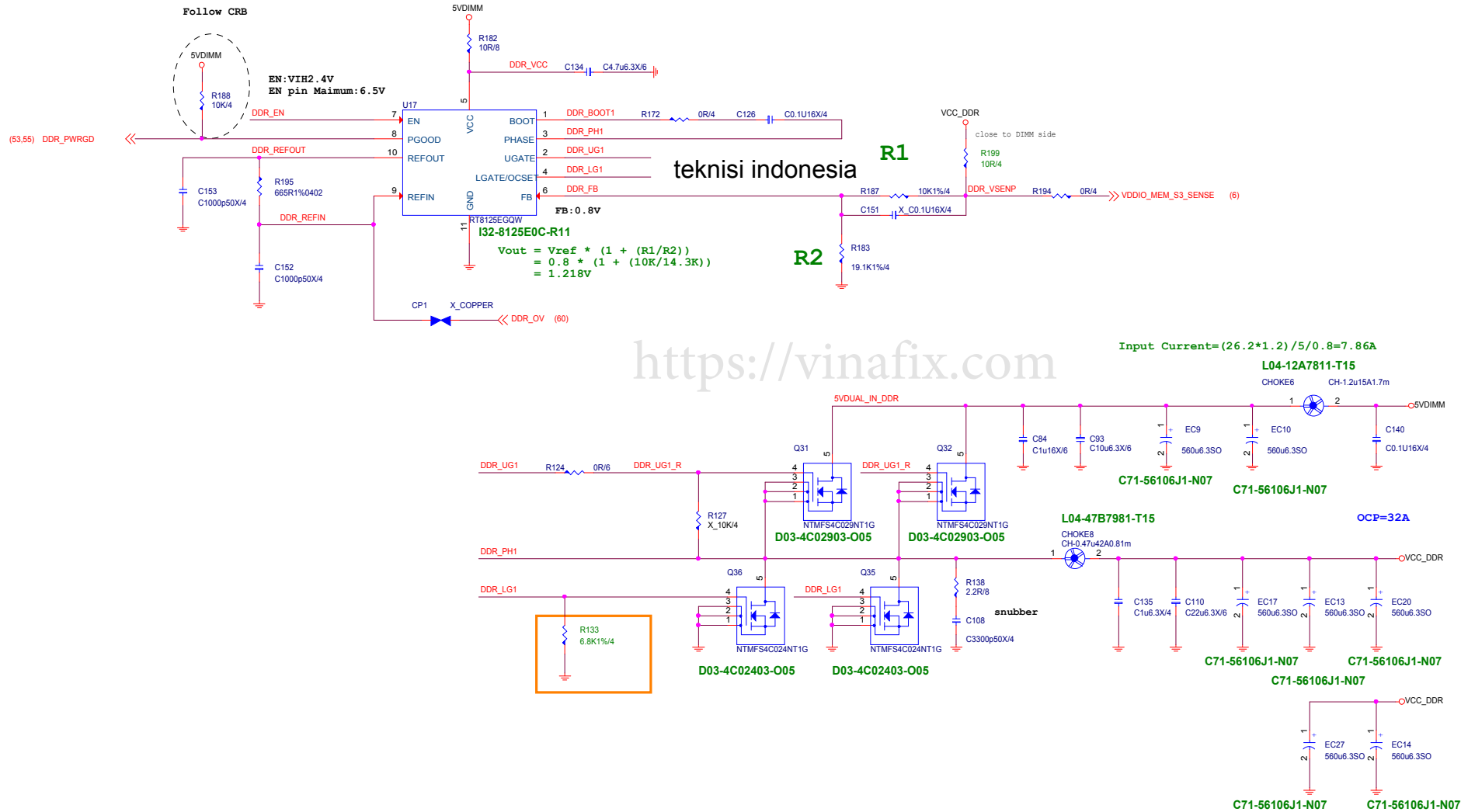
Rocpset:4.32K

OCP=Rocpset*Rdson (Low side) /10uA

=8.2K*10uA/4mohm

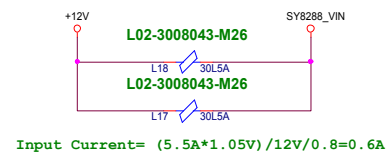
=20.5A

(6,54,55,62) APU_AMMR1 >> D18 >> S-LRB520S-40T1G DDR_EN
(29) SIO_VDDQ_EN >> R198 >> 0R/4 DDR_EN 3.12V
EN: VIH2.4V
EN pin Maximum: 5.5V, RECOMMENDED: 3.6V

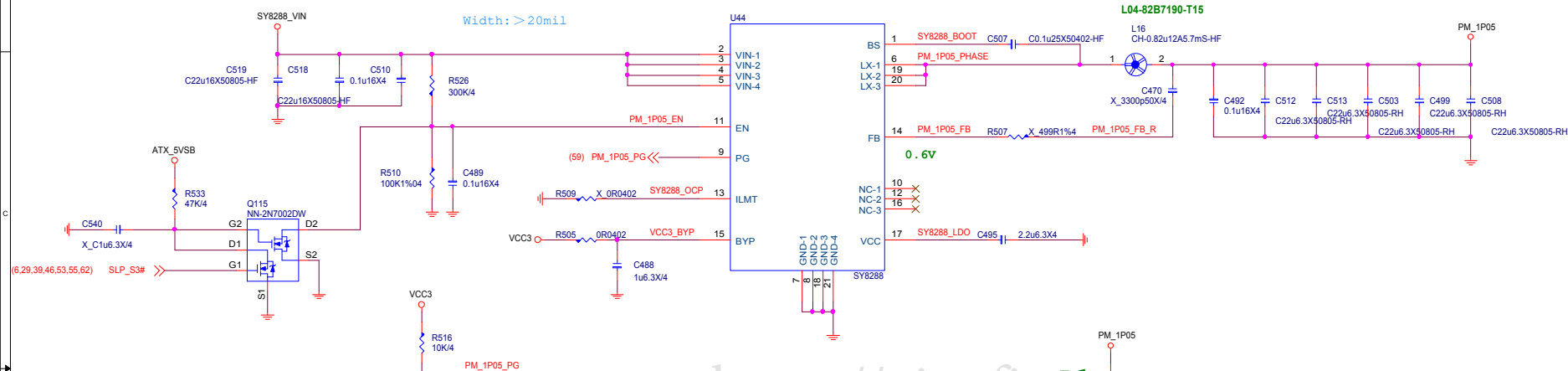


FOR Promontory 1.05V_S0

1.05V
S0: 5.5A
S5: 0.05A



OCP=12A
1.05V@5.5A



SY8288_OCP	OCP
0	8A
floating	12A
1	16A

<https://vinafix.com>

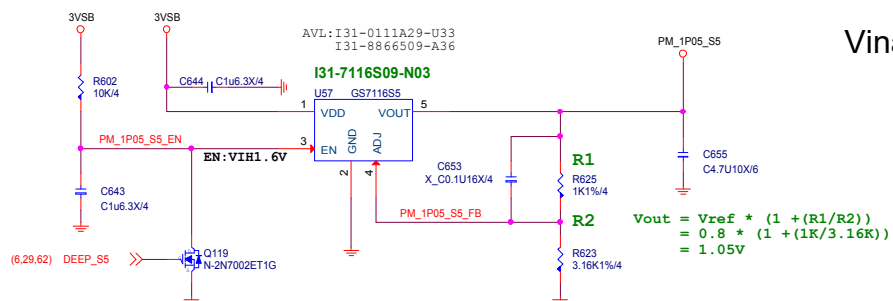
$$V_{out} = V_{ref} * (1 + (R1/R2))$$

$$= 0.6 * (1 + (1K/1.33K))$$

$$= 1.051V$$

FOR Promontory 1.05V_S5

1.05V@0.05A



$$V_{out} = V_{ref} * (1 + (R1/R2))$$

$$= 0.8 * (1 + (1K/3.16K))$$

$$= 1.05V$$

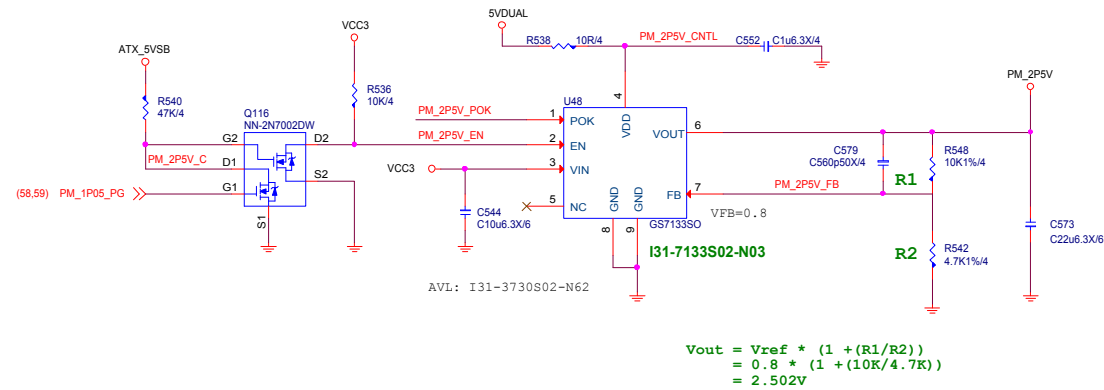
Vinafix.com



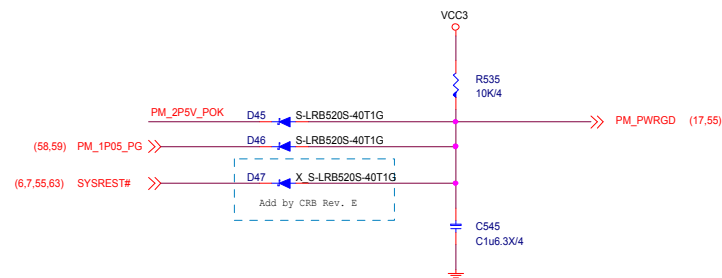
MICRO-STAR INT'L CO.,LTD		
MS-7B78		
Size	Document Description	Rev
Custom	PROM - SY8288RAC / 1.05V	11
Date:	Monday, February 26, 2018	Sheet 58 of 77

Promontory-2.5V

2.5V@900mA



<https://vinafix.com>

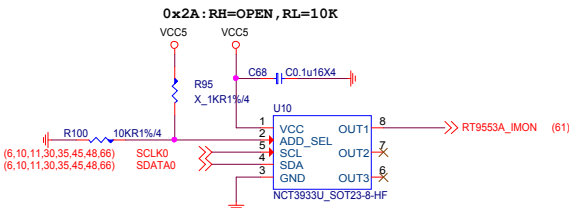


MICRO-STAR INT'L CO.,LTD

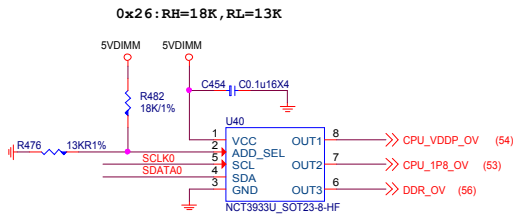
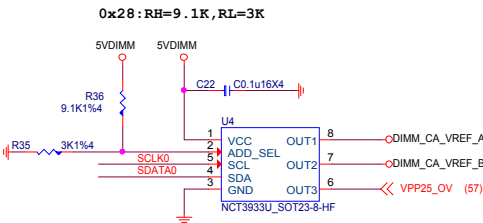
MS-7B78

Size Custom	Document Description PROM - GS7133 / 2.5V	Rev 11
Date: Monday, February 26, 2018	Sheet 59 of 77	

Over Voltage Control IC



UPI VOLTAGE CONSOLE						
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

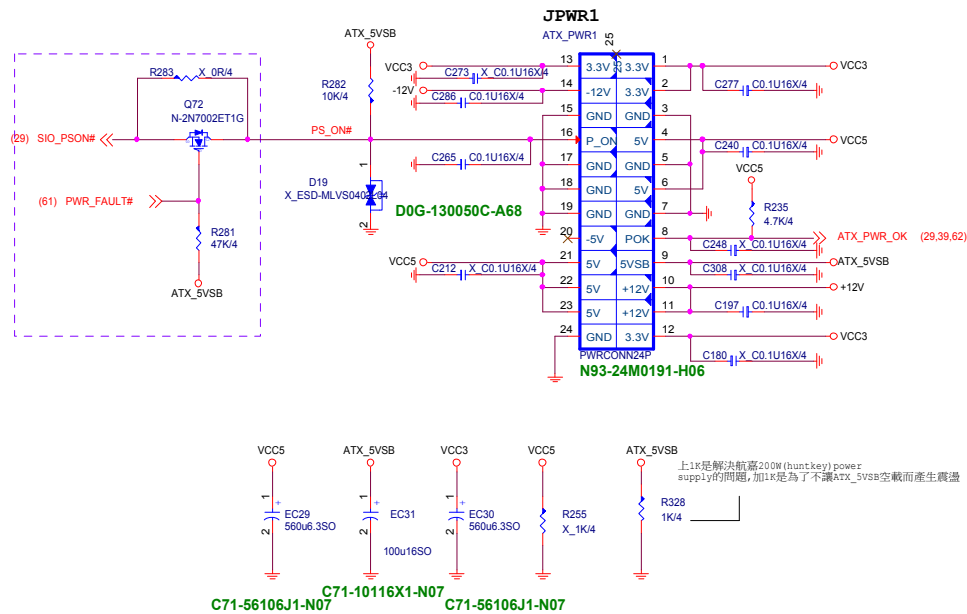


<https://vinafix.com>

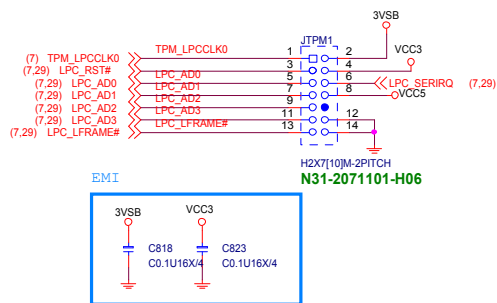
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

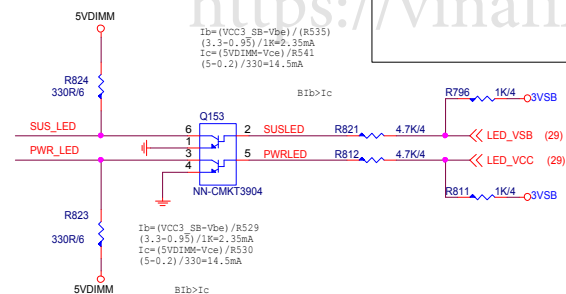
ATX POWER CONNECTOR



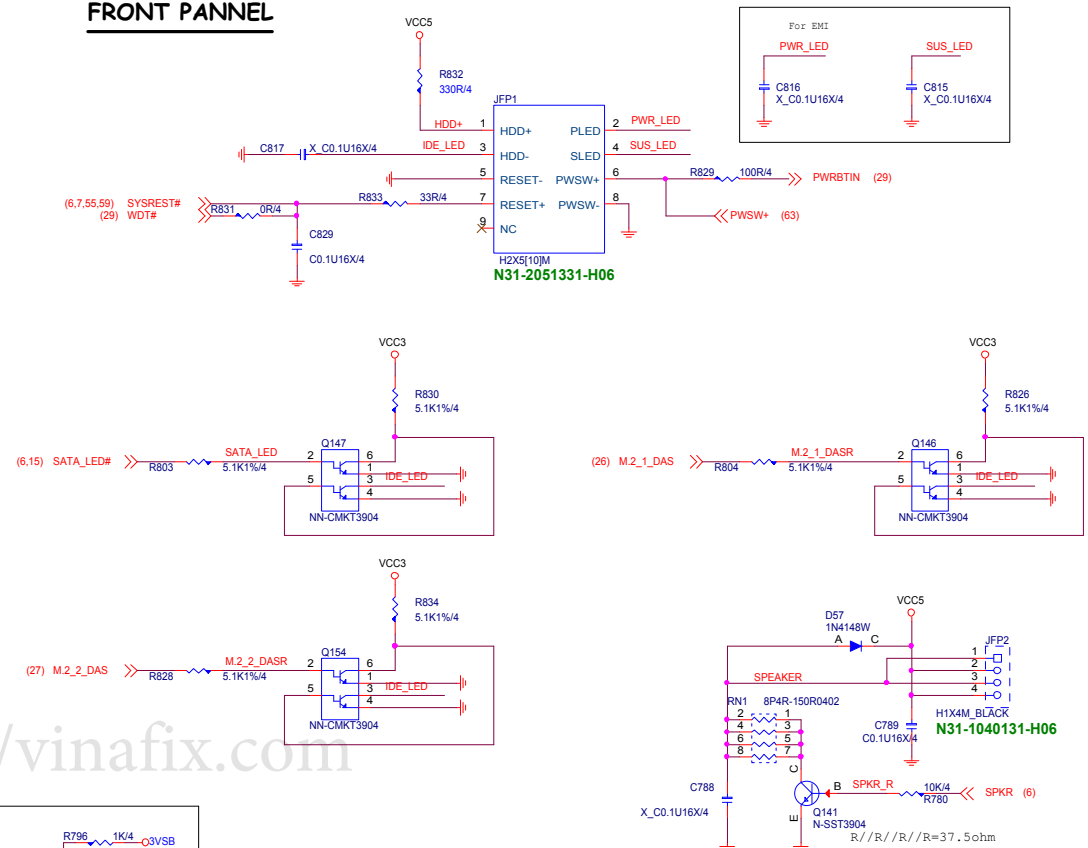
TPM



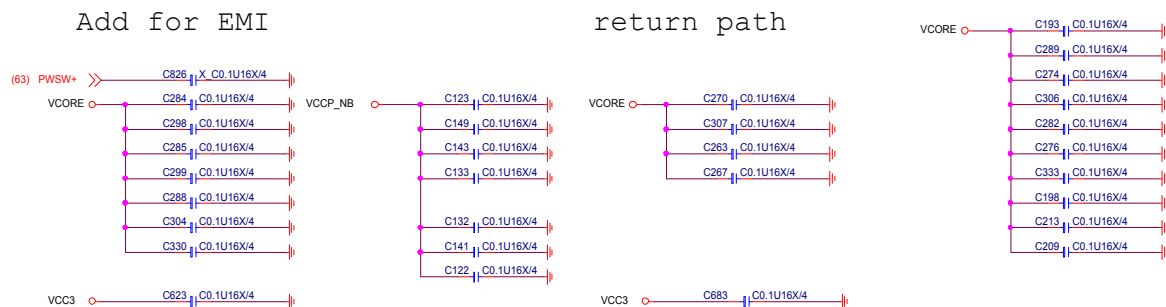
LED (for NCT6793D)



FRONT PANNEL



Voltage Measure Point

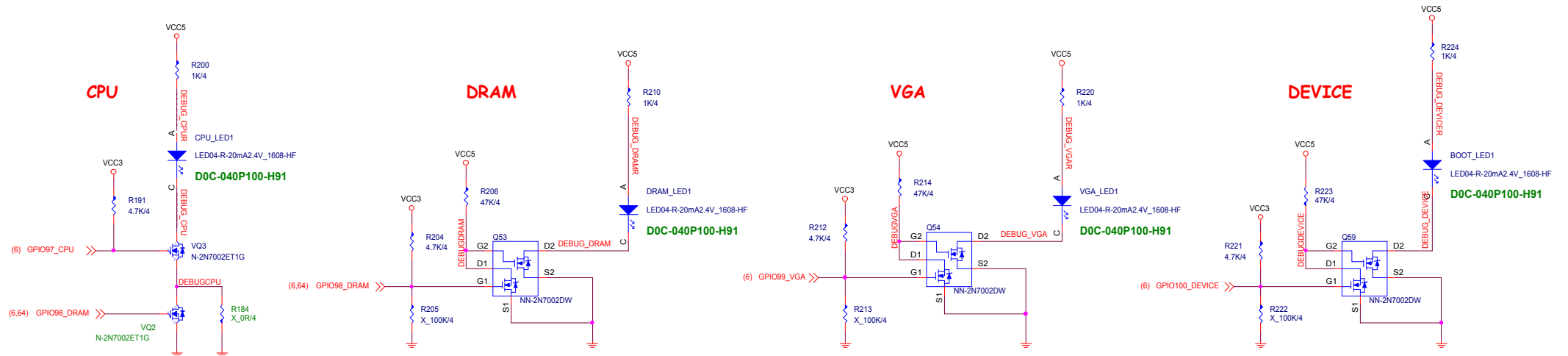


Signal	Value	Target
VCORE	1	TP_CPU_CORE
VCCP_NB	1	TP_CPU_NB
VCCP_VDDP	1	TP_CPU_VDDP
VCC_DDR	1	TP_VCC_DDR
VTT_DDR	1	TP_VTT_DDR
VPP25	1	TP_VPP25
CPU_1P8	1	TP_CPU_1P8
CPU_1P8_S5	1	TP_CPU_1P8_S5
PM_1P05	1	TP_PM_1P05
PM_1P05_S5	1	TP_PM_1P05_S5
PM_2P5V	1	TP_PM_2P5V
VCCP_NB_S5	1	TP_VCCP_NB_S5
CPU_VDDP_S5	1	TP_CPU_VDDP_S5
CPU_V_1P5V	1	TP_CPU_V_1P5V



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EZ Debug LED

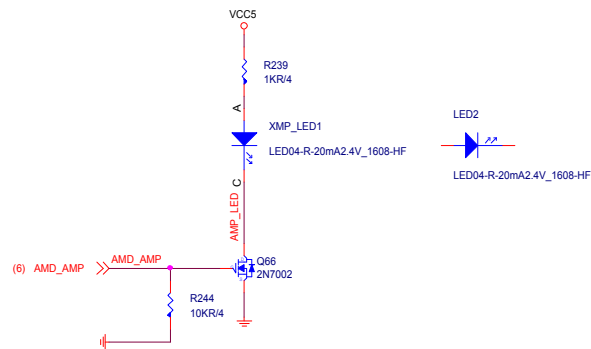


LED亮燈時同時將CPU LED關掉

LED GPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

Vinafix.com

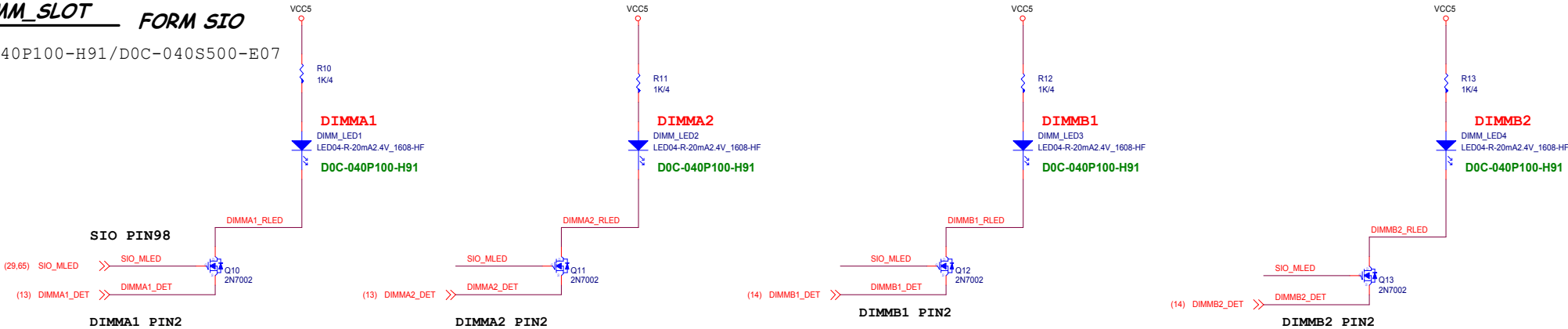
AMD AMP Detect LED



<https://vinafix.com>

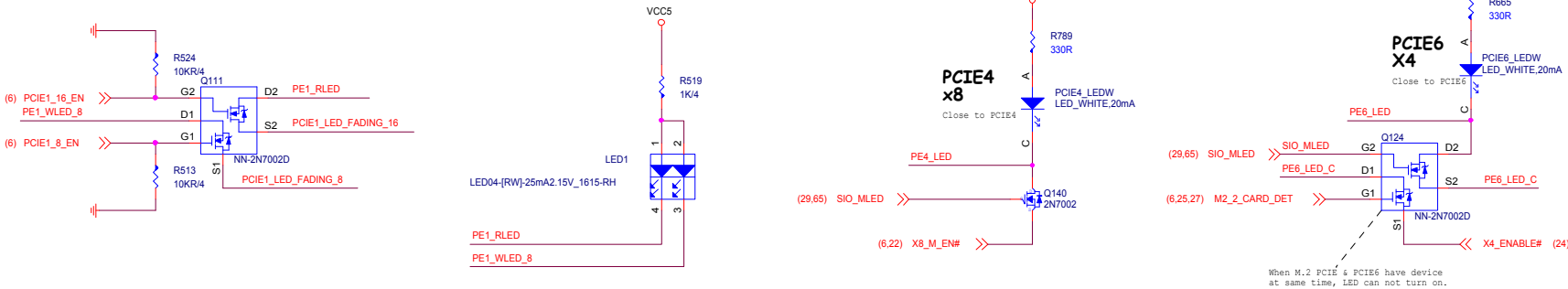
DIMM_SLOT FORM SIO

D0C-040P100-H91/D0C-040S500-E07

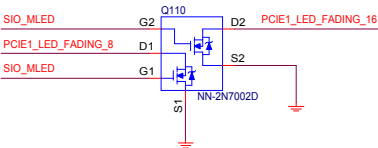


PCIE_SLOT LED FORM SIO

<https://vinafix.com>



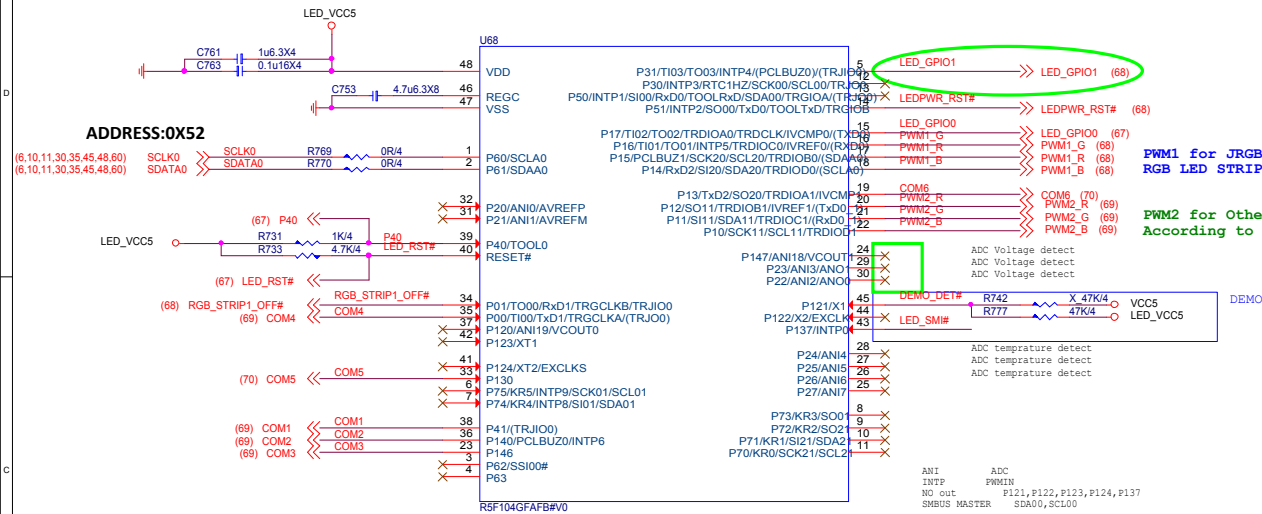
	x16	x8	x4
PCIE1	Red	X	X
PCIE1	X	White	X
PCIE4	X	White	X
PCIE6	X	X	White



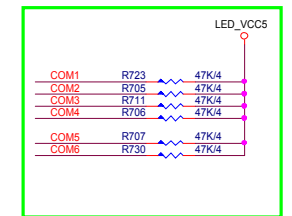
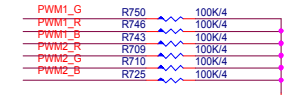
MICRO-STAR INT'L CO.,LTD		
MS-7B78		
Size Custom	Document Description LED - DIMM / PCIE SLOT	Rev 11
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48 PIN LED MCU

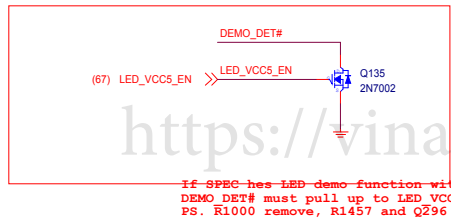
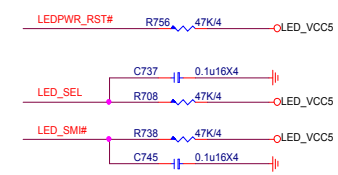
C345 & C359 near VDD Pin.



Control	Net Name	PWM USE	Connector
PCH	LED_GPIO1	No Use	JPIPE_LED2
Audio	COM1~4	PWM2	RGB LED
Board Side LED	COM5~8	PWM2	RGB LED
LED STRIPLINE	RGB_STRIP1_OFF#	PWM1	JLED1
LED STRIPLINE	RGB_STRIP1_OFF#	PWM1	JLED2
IO Cover	LED_GPIO0	No Use	JPIPE_LED1



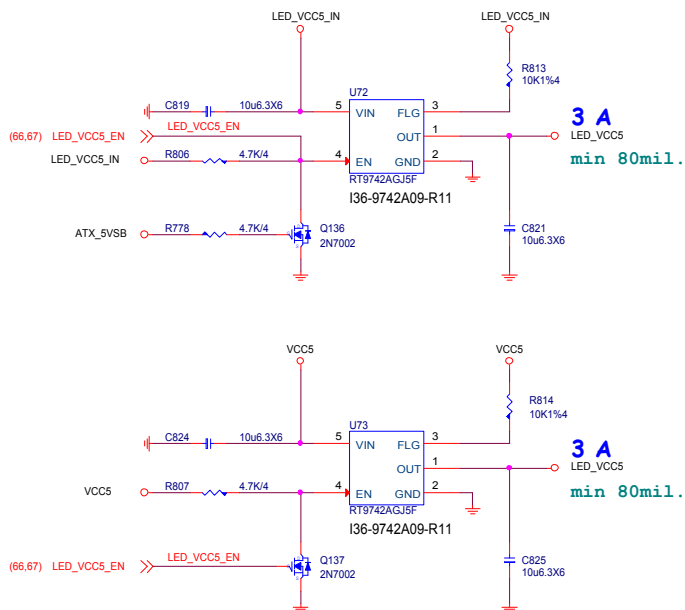
COM1~8 for PWM2
According to demand configuration.
Can configuration COM1~8,
To achieve 8 group Non-synchronized
onboard LED control.



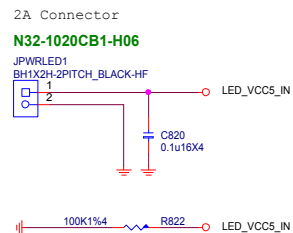
<https://vinafix.com>

If SPEC has LED demo function without demo button,
DEMO DET# must pull up to LED_VCC5 and control by LED_VCC5_EN.
PS. R1000 remove, R1457 and Q296 need to stuff

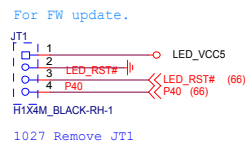
EXTERNAL POWER INPUT



External Power



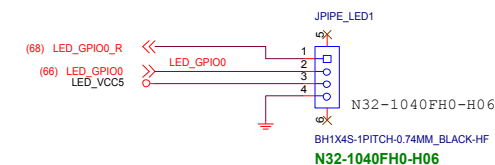
JT1 for FW update



LED Demo Button

1 **PCH HEATSINK LED**
PCS LED*0.16W=W

2 **AUDIO/IO Cover LED**
PCS LED*0.16W=W



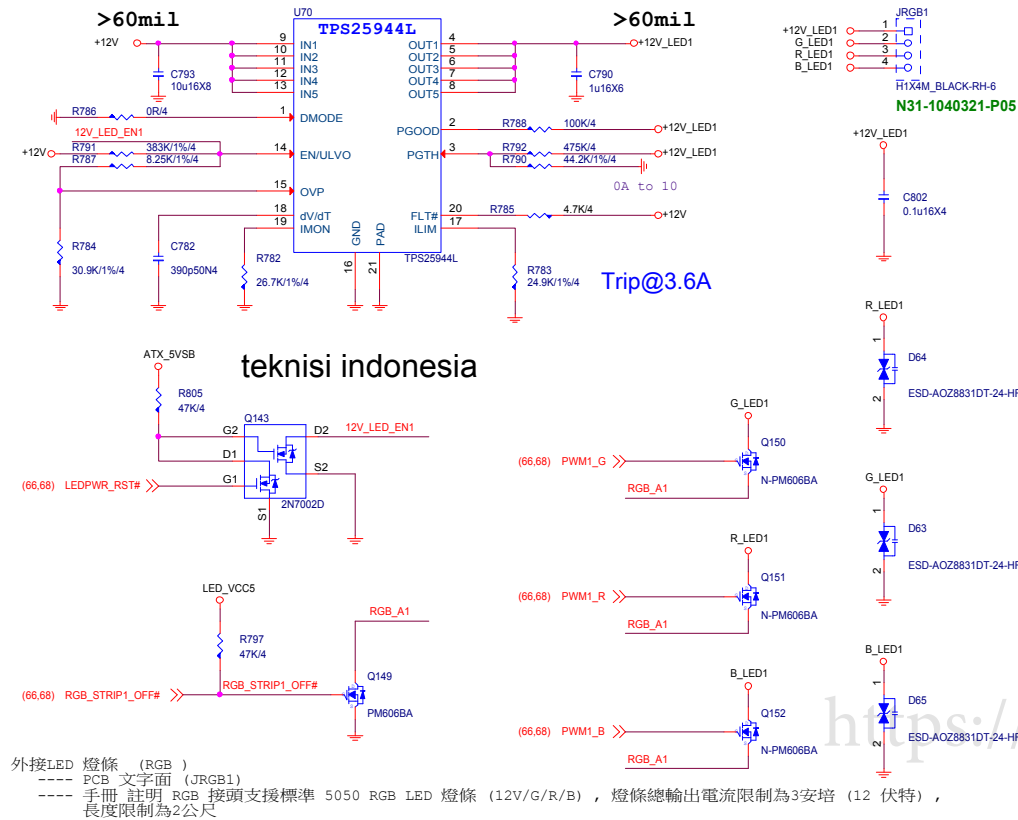
3 **MOS HEATSINK LED**
PCS LED*0.16W=W

JPIPE_LED3 no SPEC

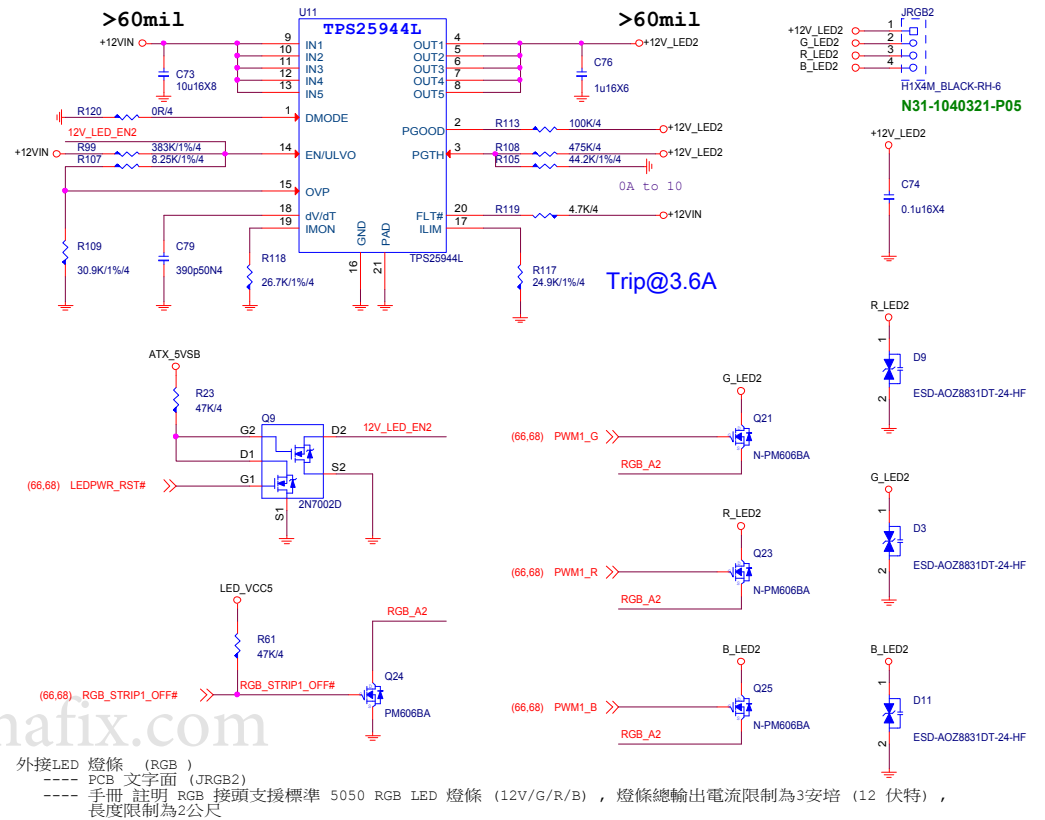
JPIPE:PIN1:output ,PIN2:input

<https://vinafix.com>

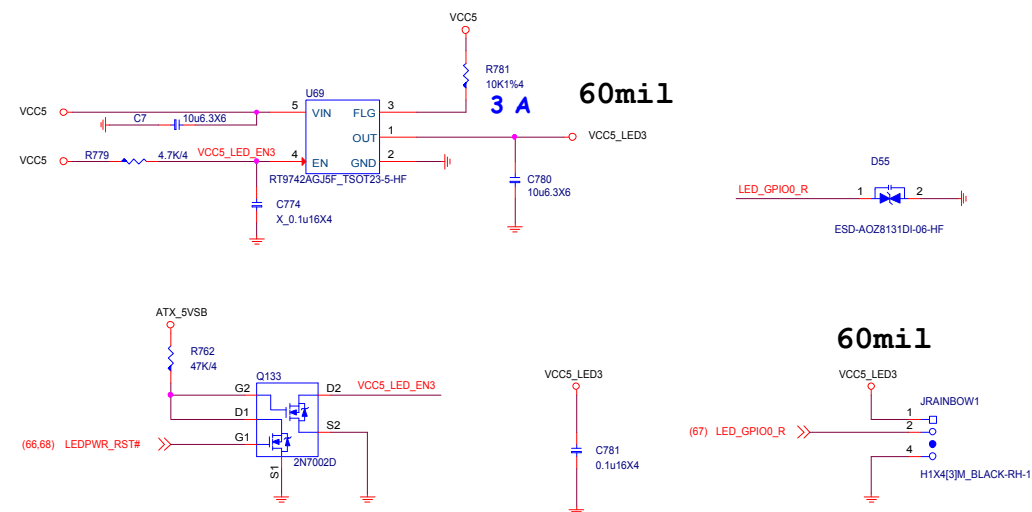
JRGB1



JRGB2

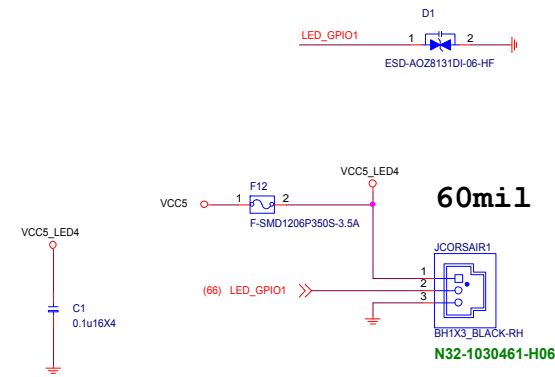


JRAINBOW1



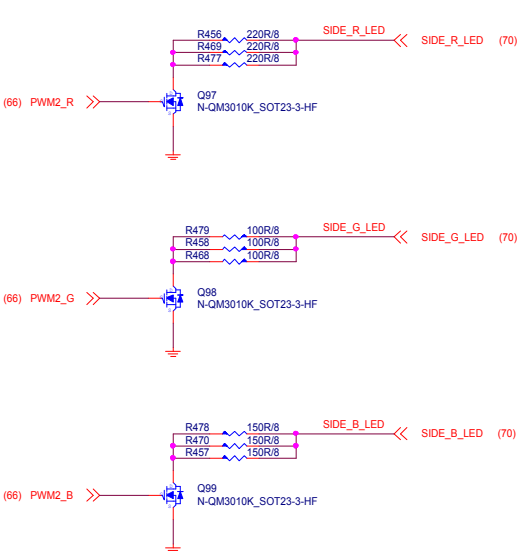
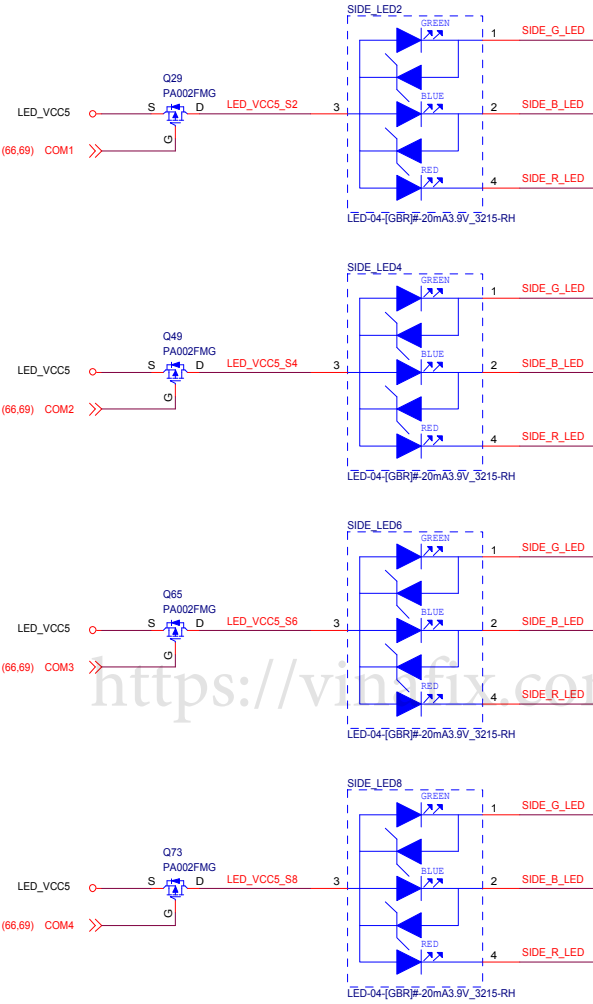
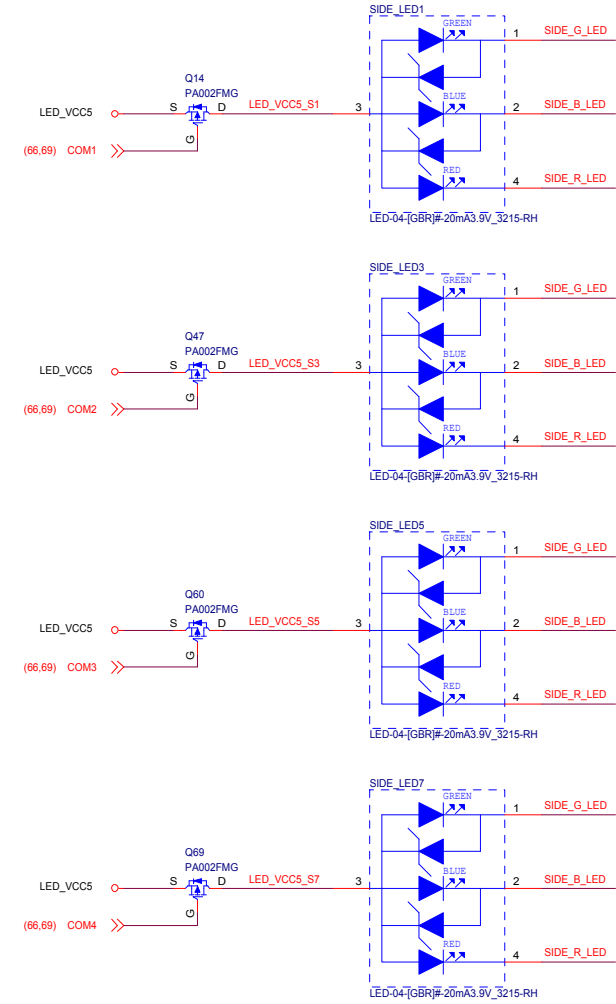
JCORSAIR1

60mil

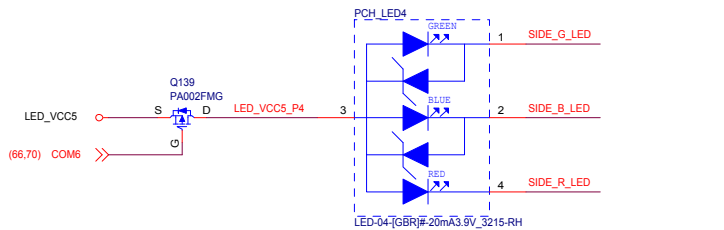
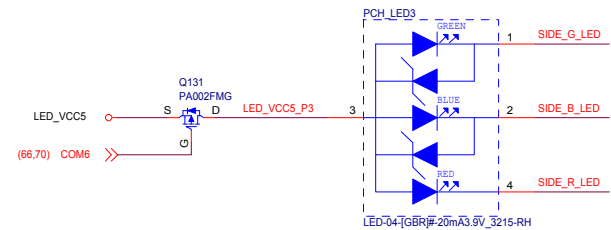
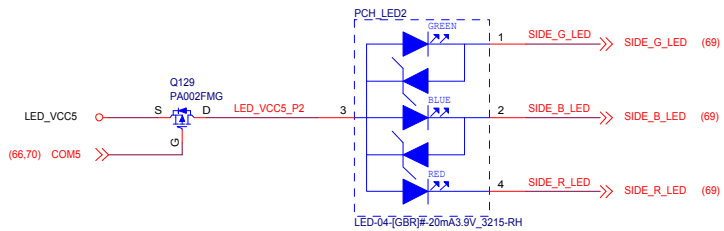
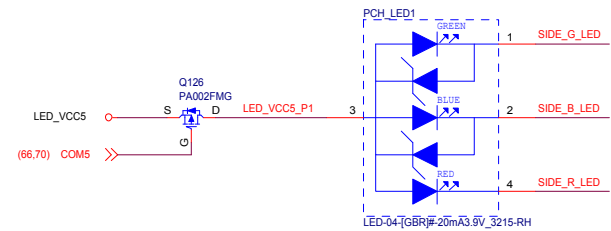


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Custom	LED - JLED1/2/3/4	11	
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Right Track LED *8




PCH LED *4

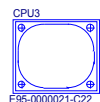


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<https://vinafix.com>

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			MS-7B78		
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CPU Socket



E95-0000022-C22

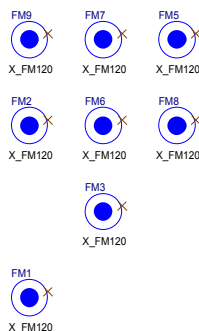
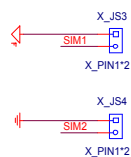
PCB

PCB

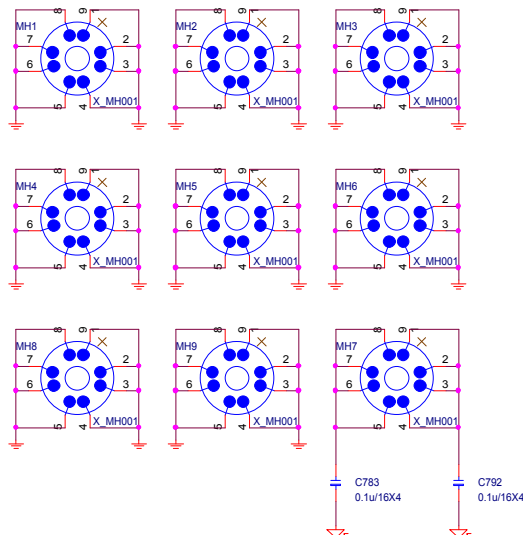


PD0-07B7811-G37

Simulation



Optics Orientation Holes



MANUAL PART

UEFI1
G51-MTSPXXA-A09
G51-M1SPXXA-A09

HDMI_LA1
Label
HDMI
HDMI LABEL
Y01-RHDMI03-000



AVL1:
D06-0100161-F52
D06-0100101-K26

CFOS <MSI-BOM>
Y02-MU00170-CFO
Y02-MU00170-CFO

NAHIMIC <MSI-BOM>
Y02-MU00100-NAH
Y02-MU00100-NAH

SLI <MSI-BOM>
Y01-RNVIDIL-000
Y01-RNVIDIL-000

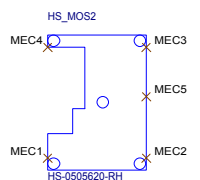
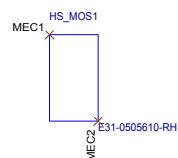
WIFI_MUDUAL <MSI-BOM>
WIFI
604-4442-020



XSPILT <MSI-BOM>
X_Y02-MA00401-XSP
Y02-MA00401-XSP

SSE <MSI-BOM>
X_Y02-MA00101-SSE
Y02-MA00101-SSE

MOS HEATSINK



IO COVER+MOSA

mos heatsink

PCH HEATSINK

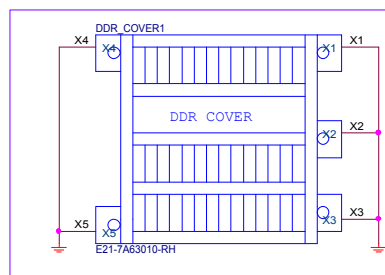


PCH Heatsink

Audio COVER



DDR COVER



0901 Modify DDR_COVER1 PIN X1.X2.X3.X4.X5 Connect to GND

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