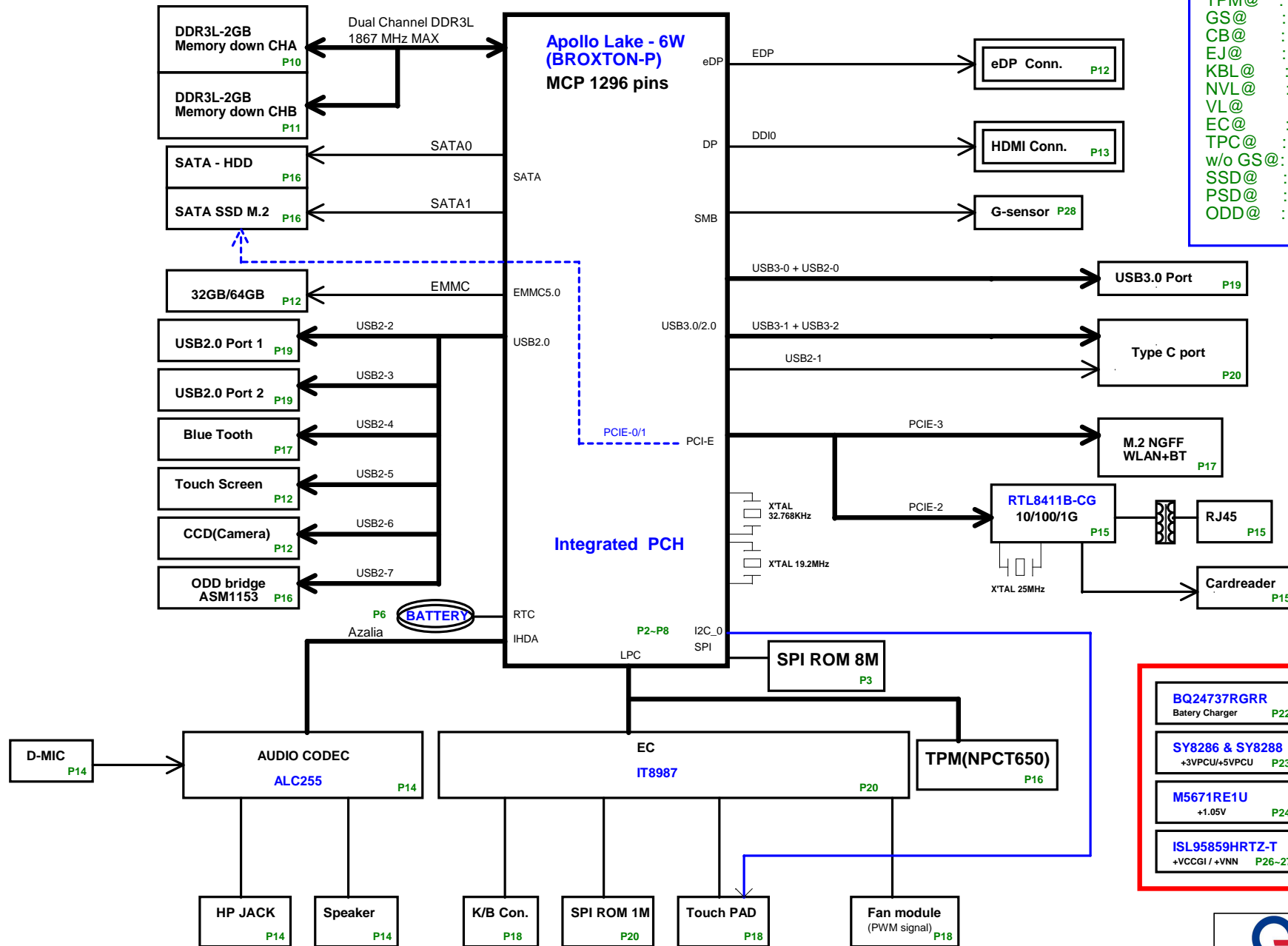


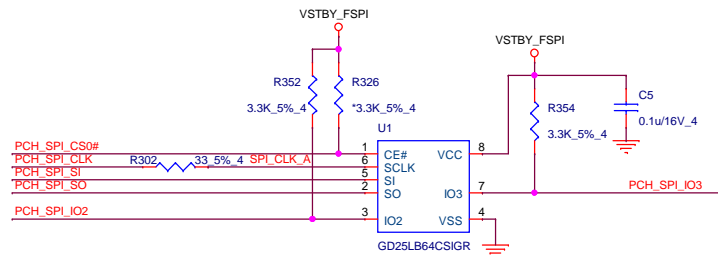
ZAJ/Z8P/Z8PA SYSTEM BLOCK DIAGRAM



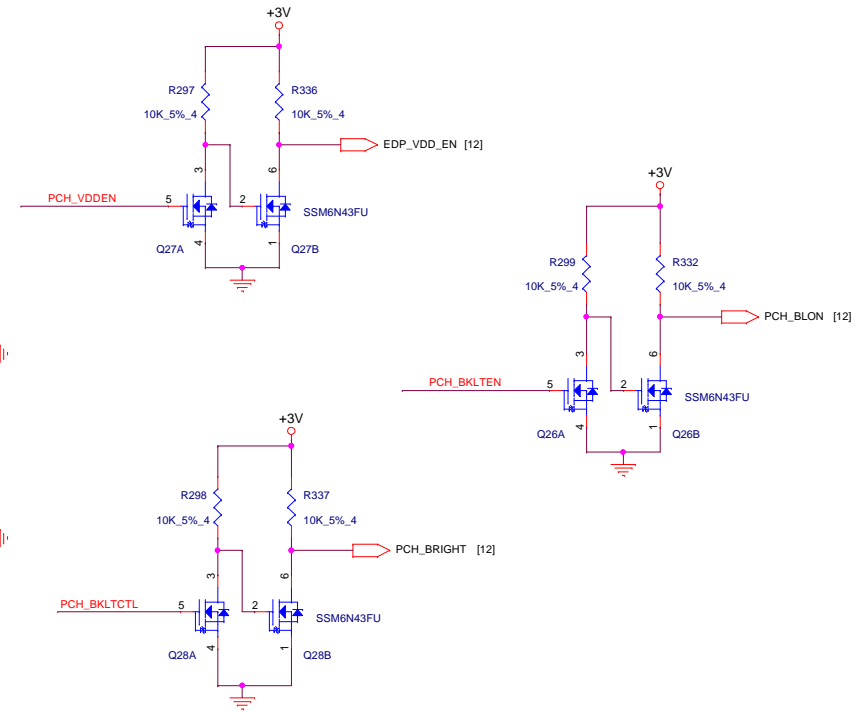
BOM

TPM@ : TPM
 GS@ : G-SENSOR
 CB@ : Cloud book SKU
 EJ@ : EJ sereies SKU
 KBL@ : keyboard backlight
 NVL@ : none LED panel boost
 VL@ : LED panel boost
 EC@ : EMMC
 TPC@ : Type C function
 w/o GS@ : stuff with none GS sku
 SSD@ : SATA interface SSD
 PSD@ : PCIE interface SSD
 ODD@ : ODD function

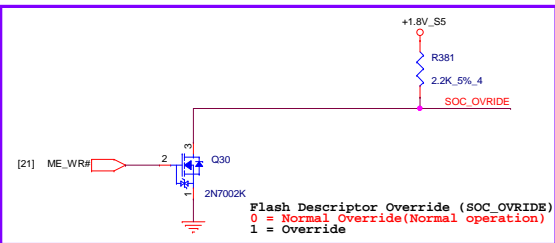
BQ24737RGR Battery Charger P22	RT8231BGQW +1.35VSUS P25
SY8286 & SY8288 +3VPCU/+5VPCU P23	G5719CTB1U G5719CTB1U G9661MF11U
M5671RE1U +1.05V P24	+1.8V_ S5 / +1.24VSUS/+1.5V P28
ISL95859HRTZ-T +VCCGI / +VNN P26-27	Thermal Protection Discharger P29




SPI ROM	Vender	Size	Quanta P/N	Vender P/N
1.8V	WND	8M	AKE5EZ0N0N01	W25Q64FWSSIQ
	GGD	8M	AKE5EG-0Q01	GD25LB64CSIGF

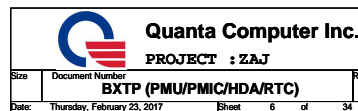


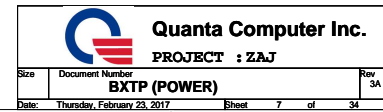
05

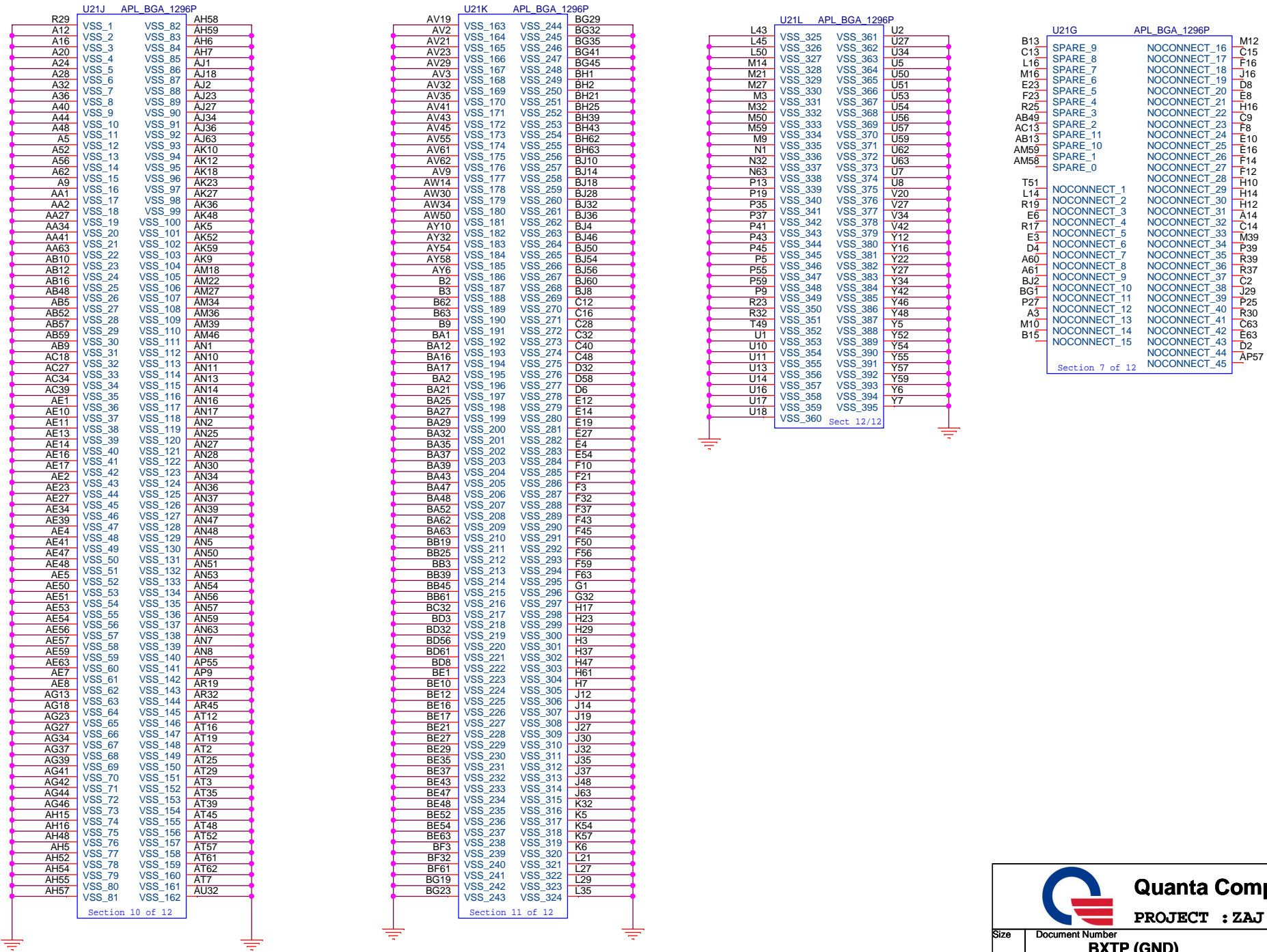


eMMC_ID1	eMMC_ID0	Vender
0	0	Samsung 32/64GB
0	1	Hynix 32/64GB
1	0	Kingston 32/64GB

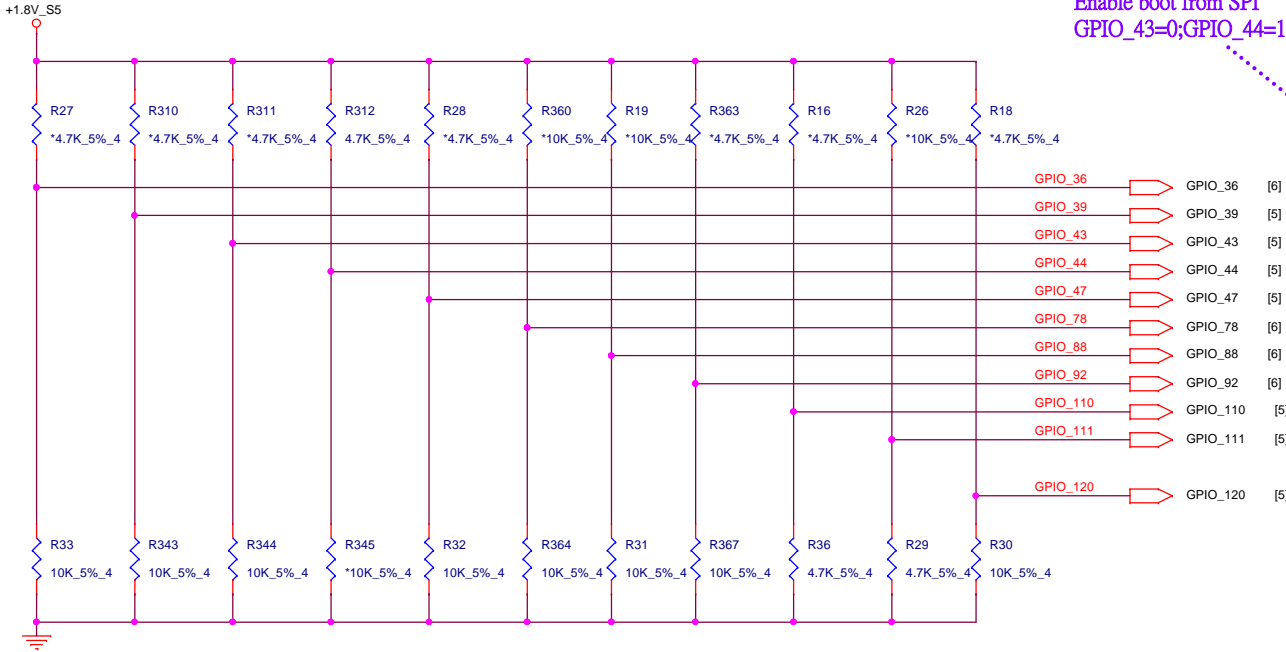
 Quanta Computer Inc. PROJECT : ZAJ		
Size	Document Number	Rev
	BXTP (EMMC/LPC/SMB/ISH)	



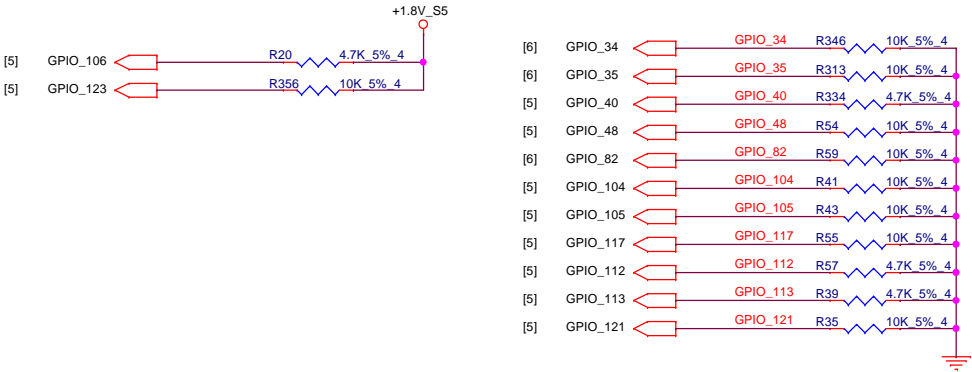





HARDWARE STRAPS



Hardware Strap	Strap Description
GPIO_36	VCC_1P24V_1P35V_A voltage select 0 = 1.24V 1 = 1.35V
GPIO_39	Enable CSE(TXE3.0) ROM Bypass 0 = Disable bypass 1 = Enable Bypass
GPIO_43	Allow eMMC as a boot source 0 = Disable 1 = Enable
GPIO_44	Allow SPI as a boot source 0 = Disable 1 = Enable
GPIO_47	Force DNX FW Load 0 = Do not force 1 = Force
GPIO_78	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V 1=buffers set to 1.8V
GPIO_88	PMU 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode
GPIO_92	SMBus No Re-Boot 0 = Disable (default) 1 = Enable
GPIO_110	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode
GPIO_111	Boot BIOS Strap 0 = Boot from SPI 1 = Do not boot from SPI
GPIO_120	Top swap override 0 = Disable 1 = Enable

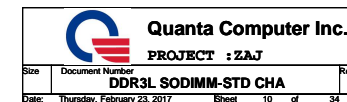


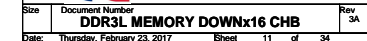


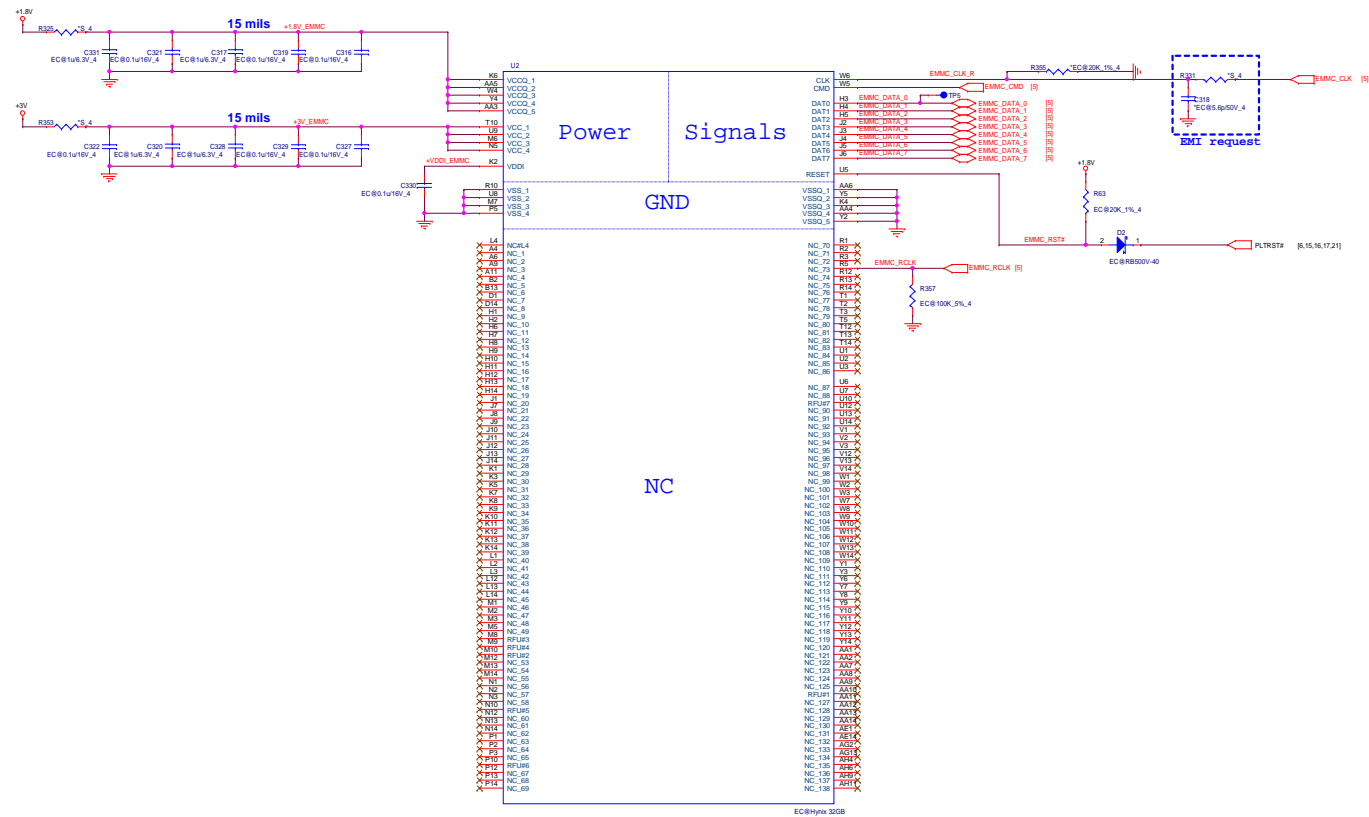
Quanta Computer Inc.

PROJECT : ZAJ

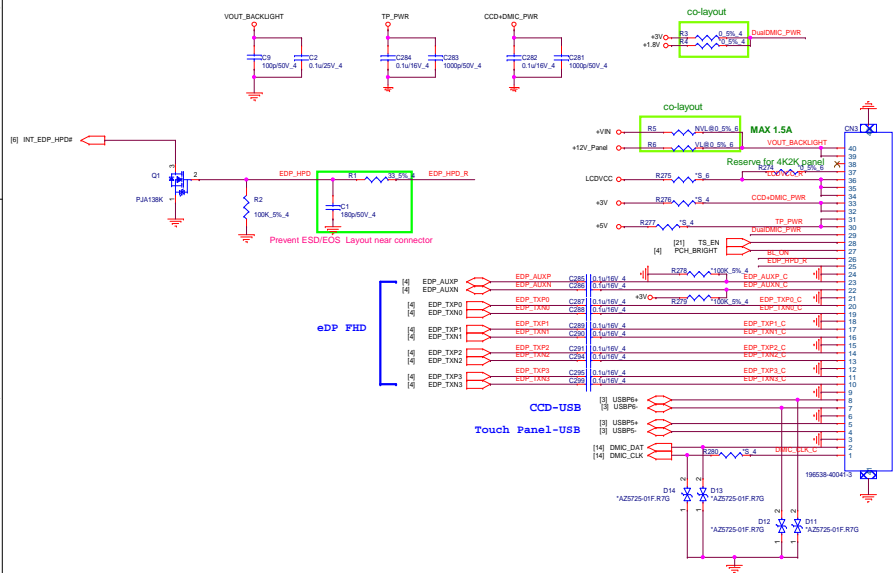
Size	Document Number	Rev
	HARDWARE STRAPS	3A
Date:	Thursday, February 23, 2017	Sheet 9 of 34



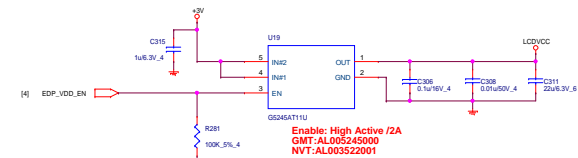




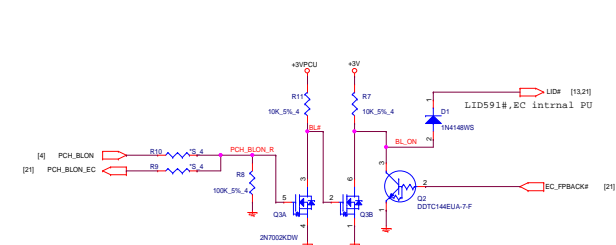
eDP CONNECTOR (LDS)



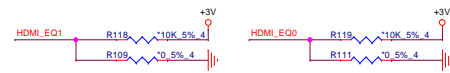
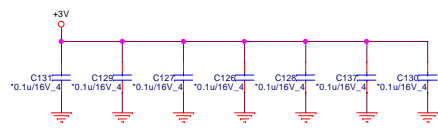
eDP Power (LDS)



eDP Backlight (LDS)



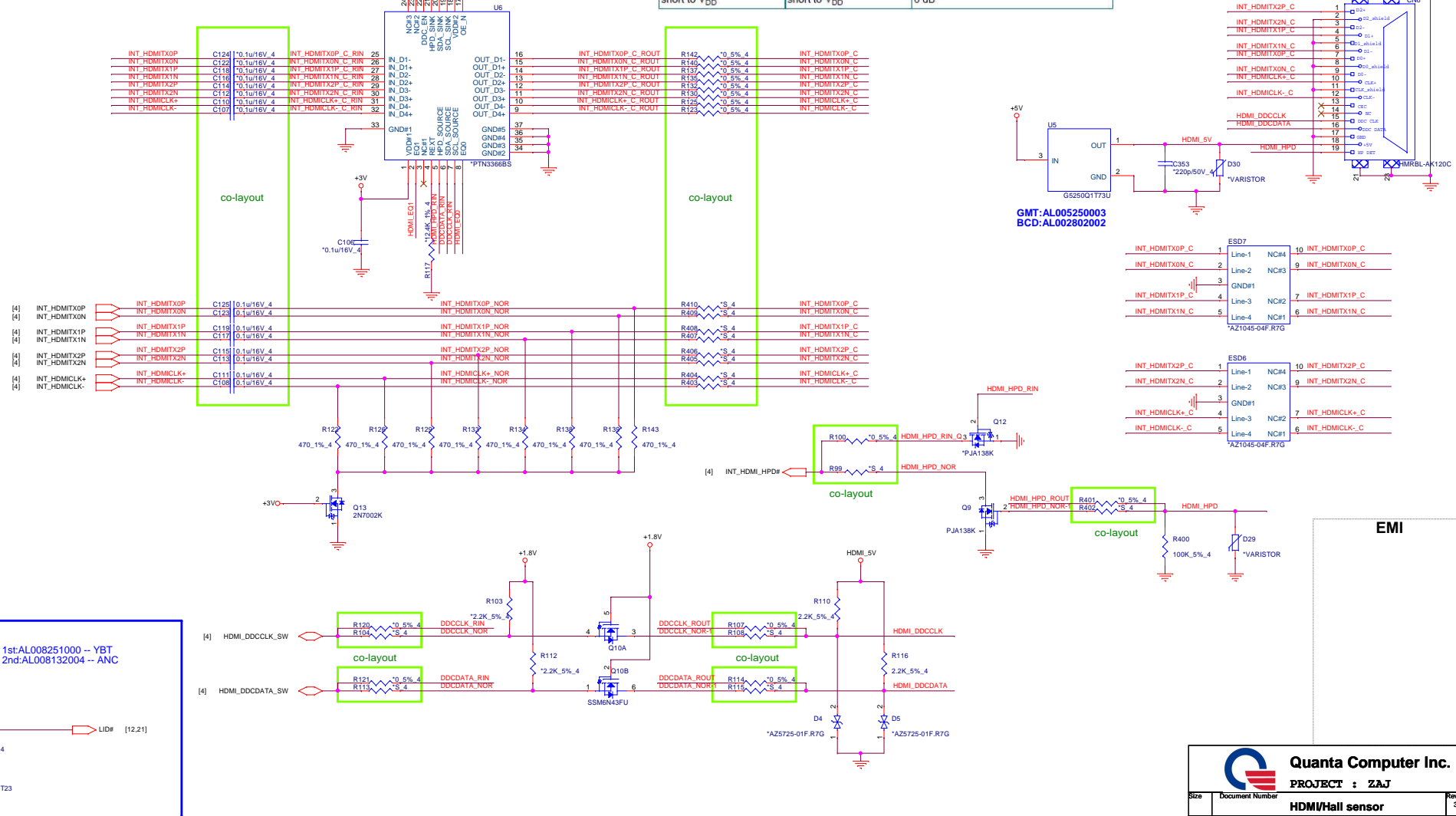
OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode



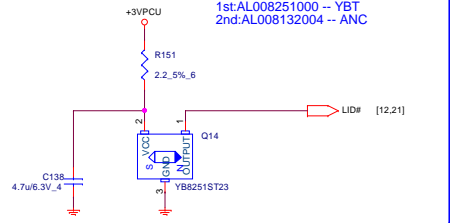
The PTN3366 supports four level equalization settings based on binary input pins EQ0 and EQ1.

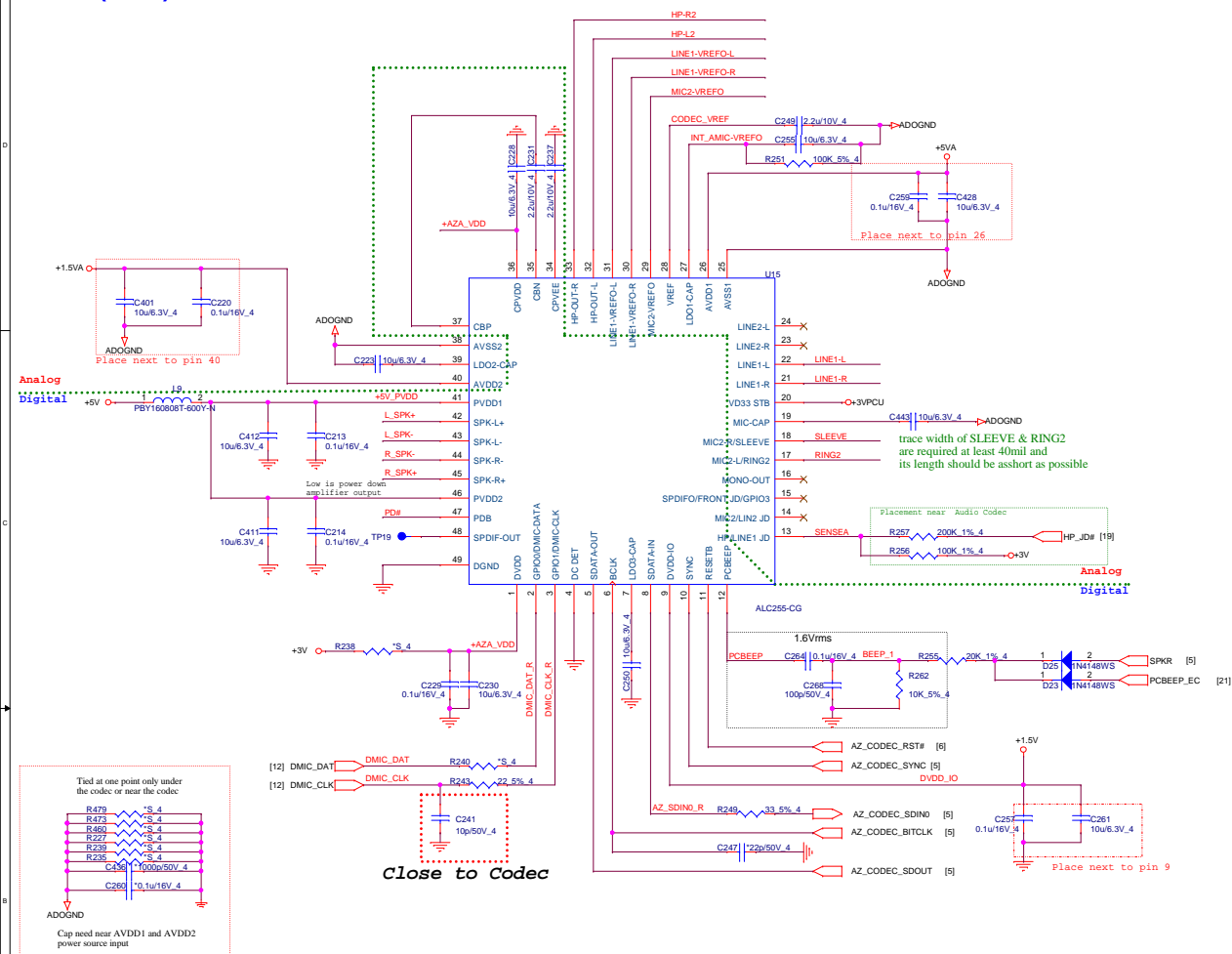
Table 5. Equalizer settings

Inputs		Equalization for 3 Gbit/s
EQ1	EQ0	
short to GND	short to GND	0 dB
short to GND	short to V_{DD}	2 dB
short to V_{DD}	short to GND	4 dB
short to V_{DD}	short to V_{DD}	6 dB

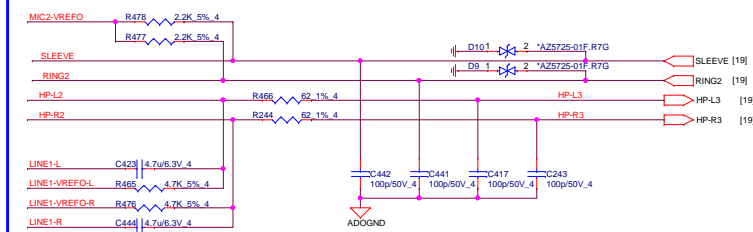


Hall Sensor (HSR)

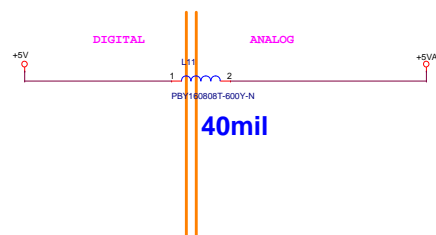




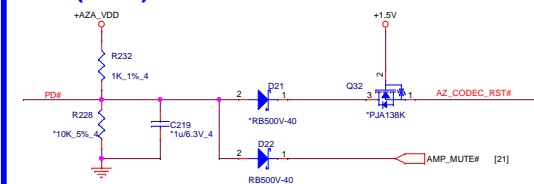
Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)



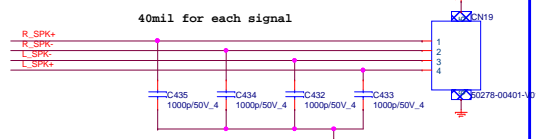
Codec PWR 5V(ADO)



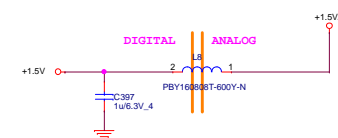
Mute(ADO)

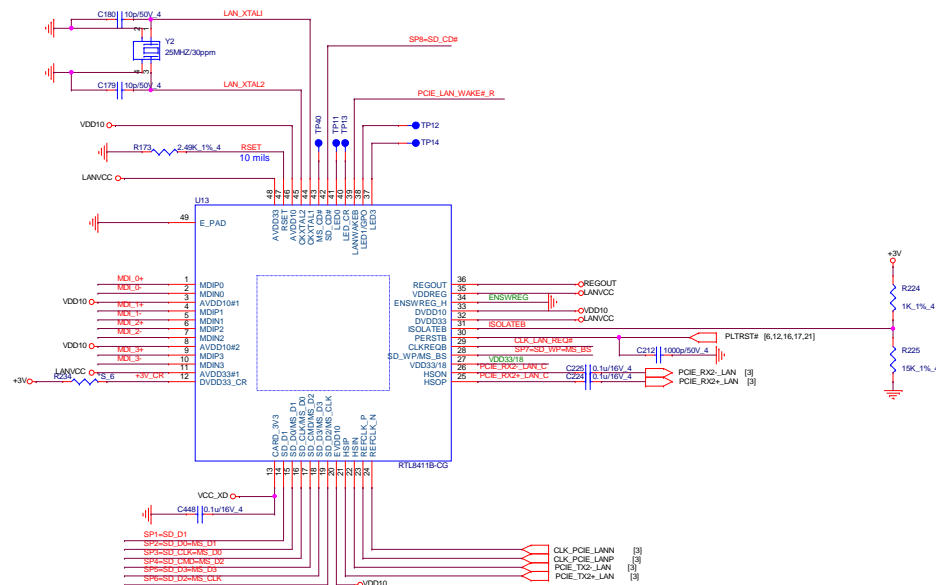


Internal Speaker

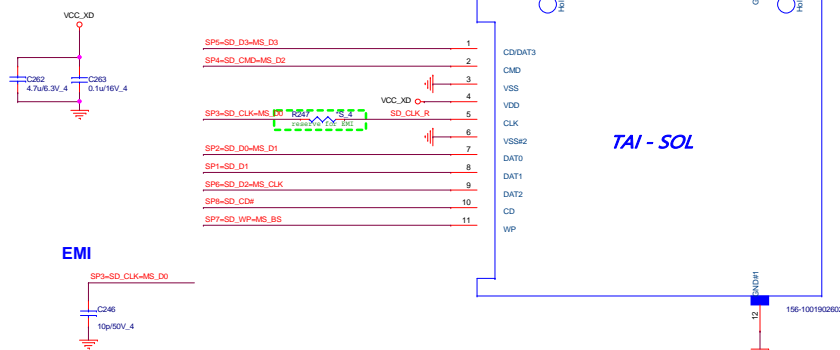


Codec PWR 1.5V(ADO)





SP1=SD_D1	C232	*10p/50V_4
SP2=SD_D0=MS_D1	C238	*10p/50V_4
SP4=SD_CMD=MS_D2	C445	*10p/50V_4
SP5=SD_D3=MS_D3	C446	*10p/50V_4
SP6=SD_D2=MS_CLK	C447	*10p/50V_4



[X] POE_LAN_WAKE#

[Y] CLK_POE_LAN_REQ#

+1.8V_S5

LANVCC

Q15A

Q15B

10K_5%_4

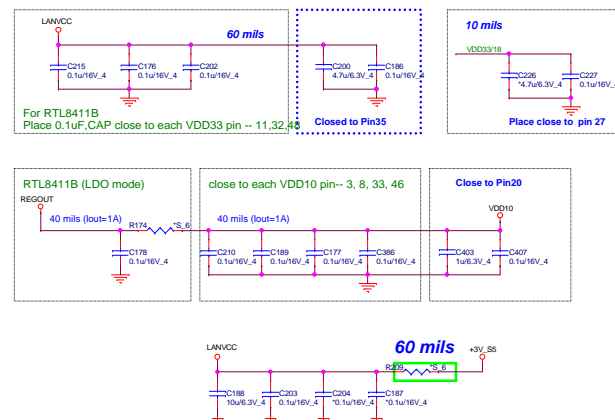
10K_5%_4

10K_5%_4

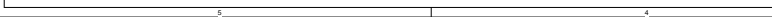
10K_5%_4

POE_LAN_WAKES_R

CLK_LAN_REQ#

[illegible]

16

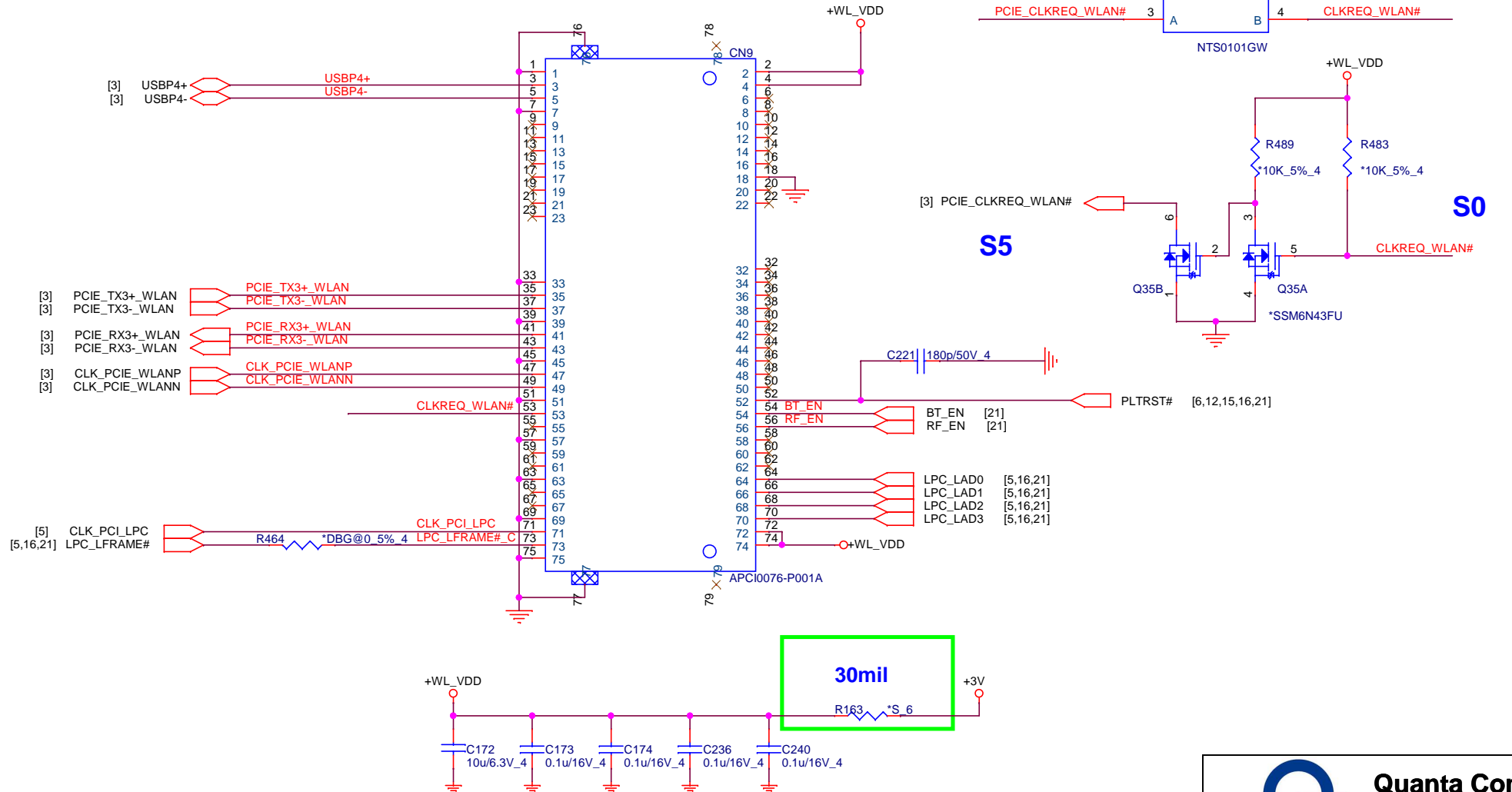


M.2 PCPIE & SATA SSD (NGF)

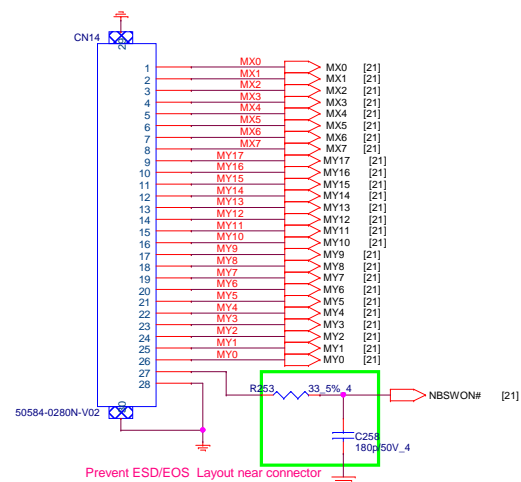


NGFF_M.2 WiFi & BT (NGF)

17

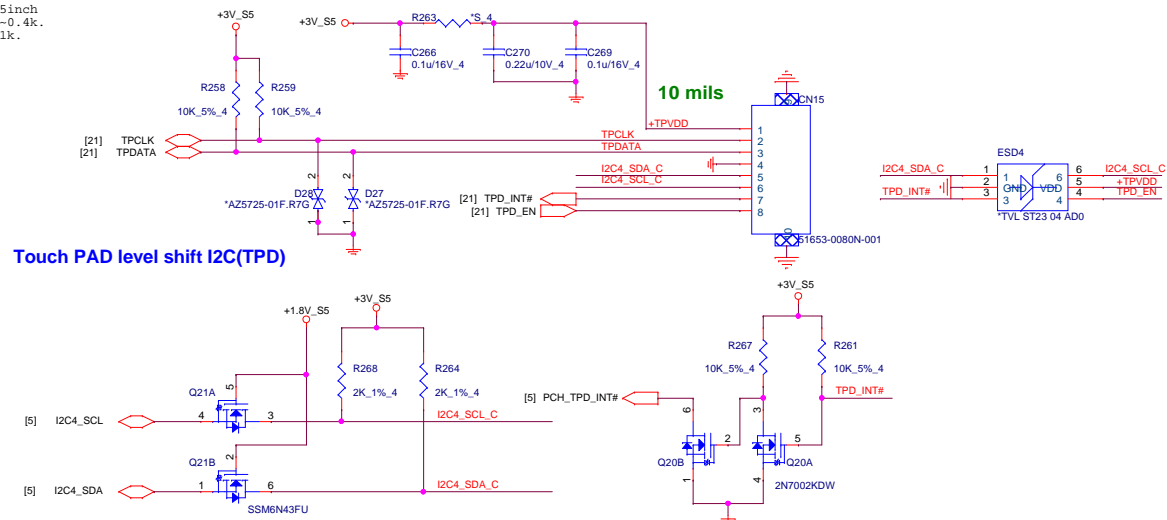


KEYBOARD (KBC)

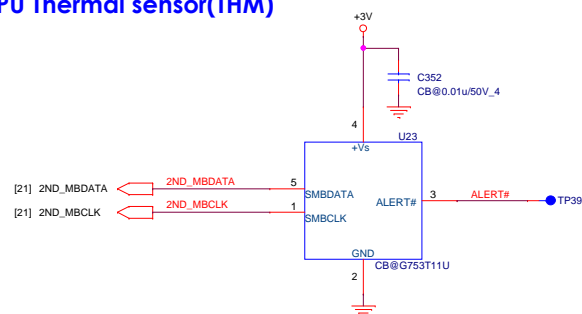


TOUCHPAD (TPD I2C/PS2 co-lay)

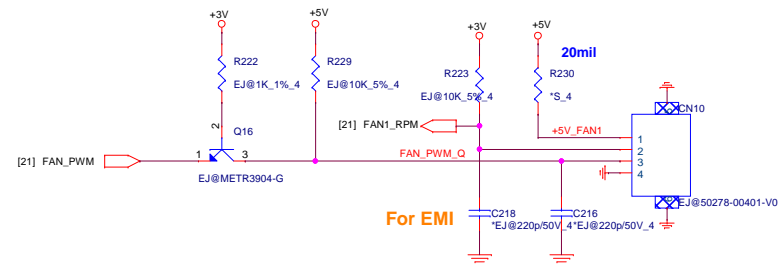
TPD->100kHz, TS=400KHz
Intel design guide suggestion
MCP PIN 10u.
Per inch 3u TS=3x5inch
400kHz10-100u =2.4-0.4k.
100KHz 10-100u=9k-1k.



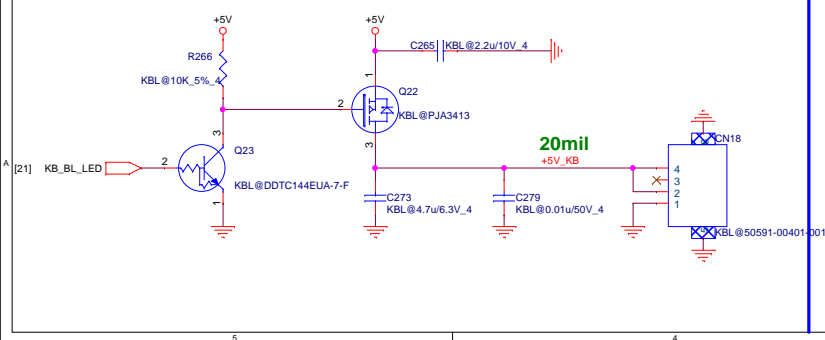
CPU Thermal sensor (THM)



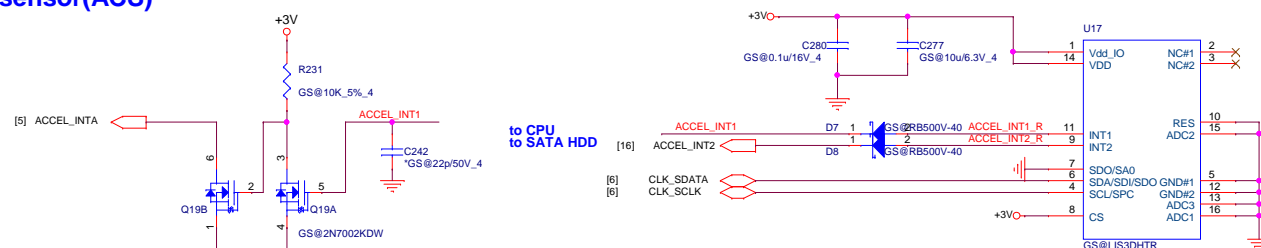
CPU FAN (THM)

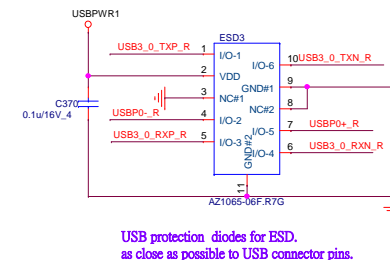
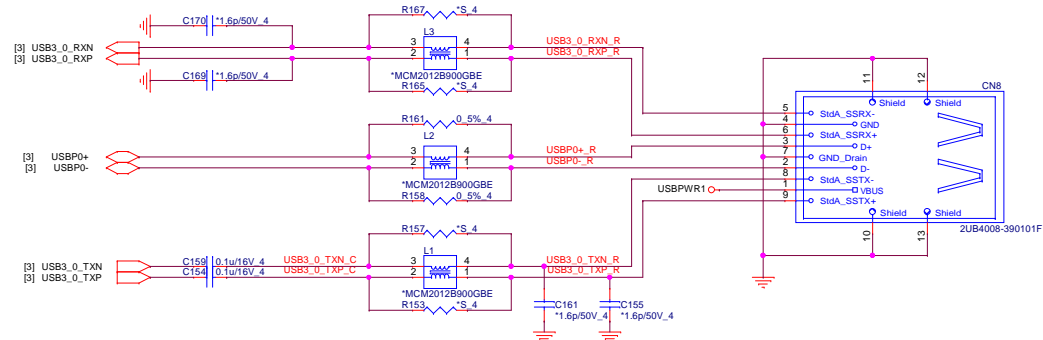
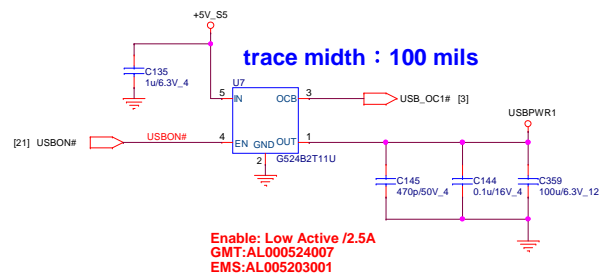


Keyboard backlight (KBL)

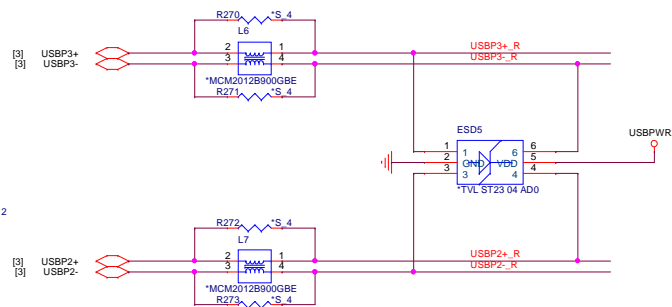
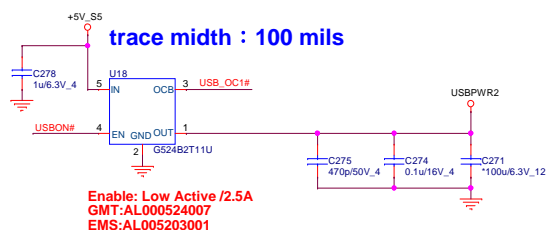


G-sensor (ACS)



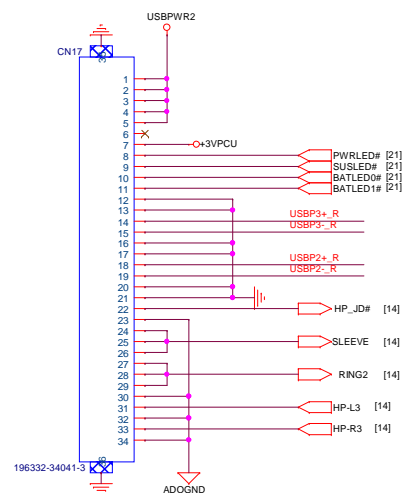


USB 2.0 (UB2)

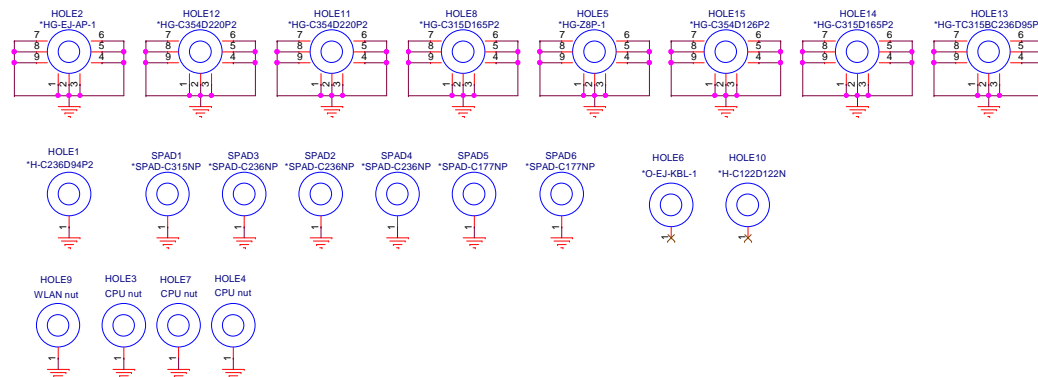


Stitch cap (EMC)

USB 2.0/LED/AUDIO JACK DB (UB2)



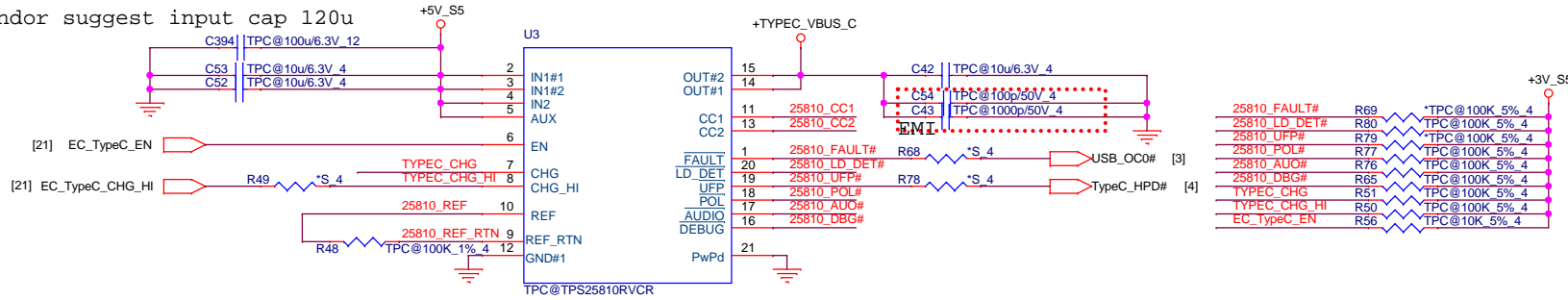
HOLE(OTH)



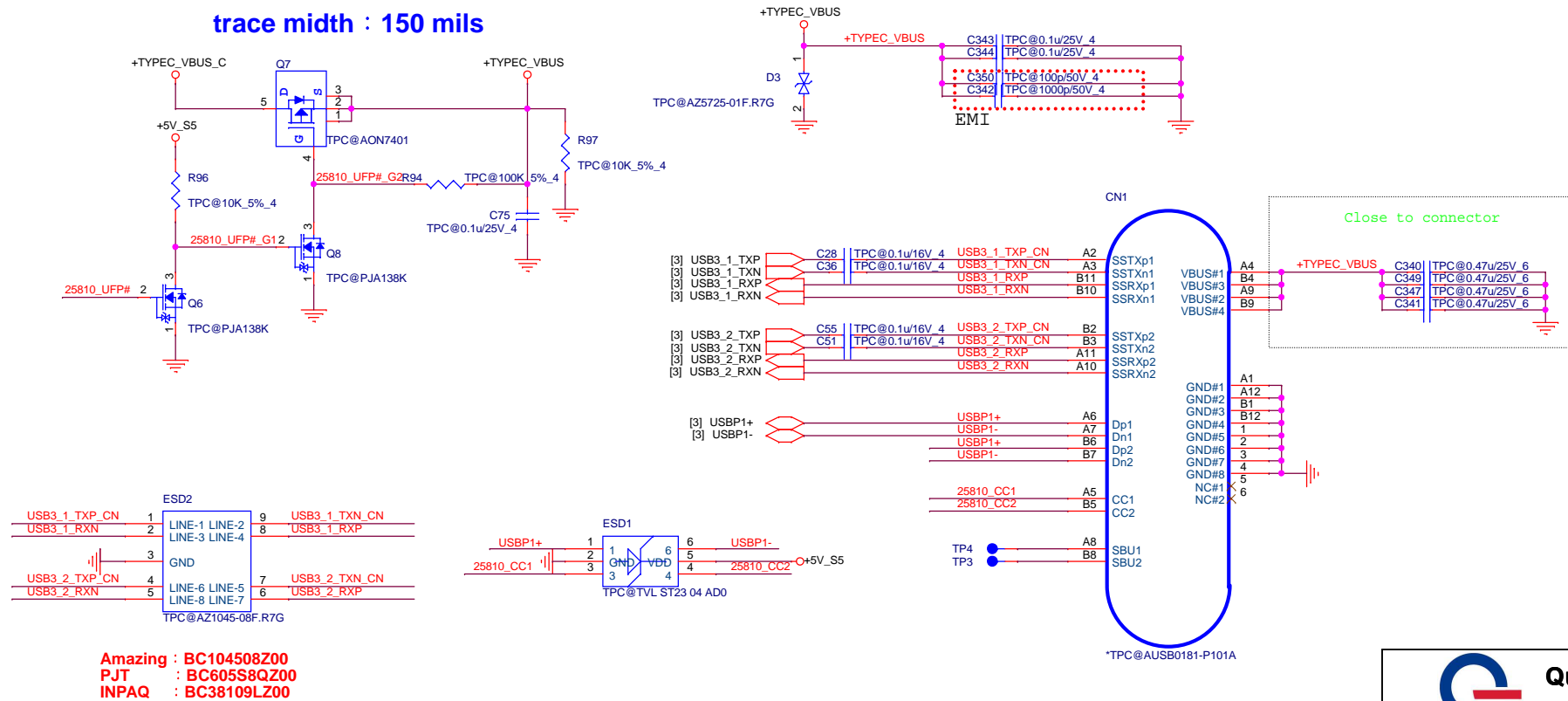
USB TYPE-C (UB3)

trace width : 150 mils

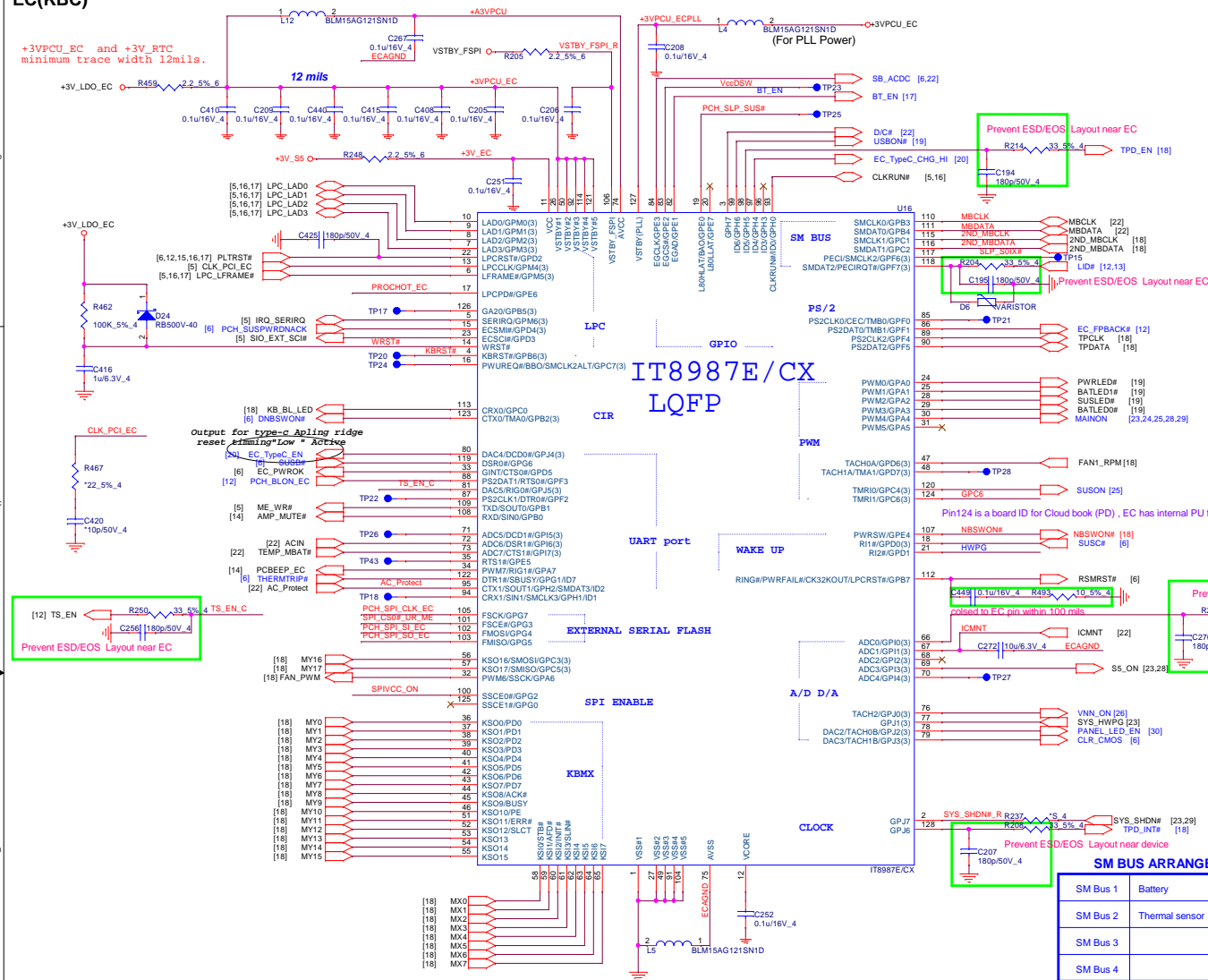
Vendor suggest input cap 120u



trace width : 150 mils

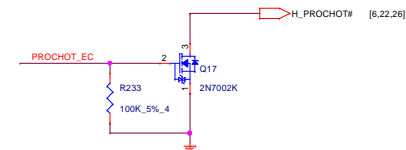
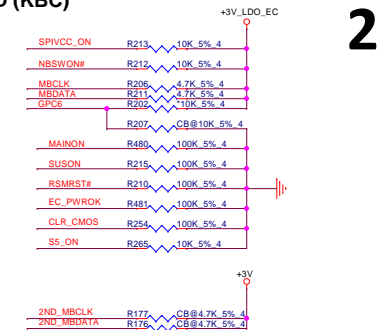


EC(KBC)

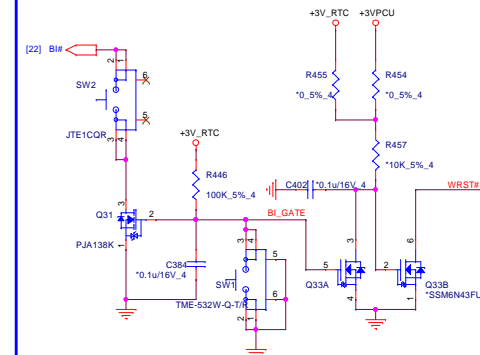


PU/PD (KBC)

21

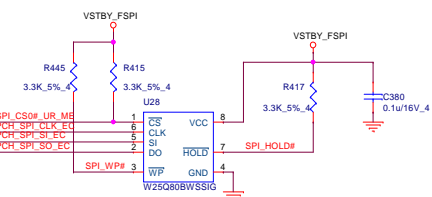
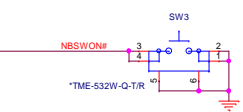


Battery Disable (FSW)



SPI ROM(KBC)

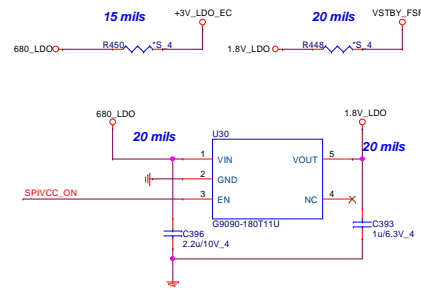
Reserve power on switch for test
(MP remove)



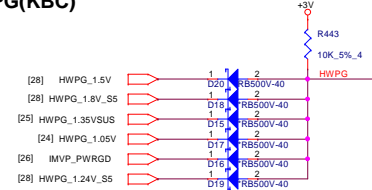
SP@ socket P/N: DFHS08FS023 only for A-TEST

SPI ROM	Vender	Size	Quanta P/N	Vender P/N
1.8V	WND	1M	AKE5GGN0N00	W25Q80EWSSIG
	GGD	1M	AKE5GZN0Q00	GD25LQ80BSIGR

Power_Auto_Recovery



HWPG(KBC)



Quanta Computer Inc.

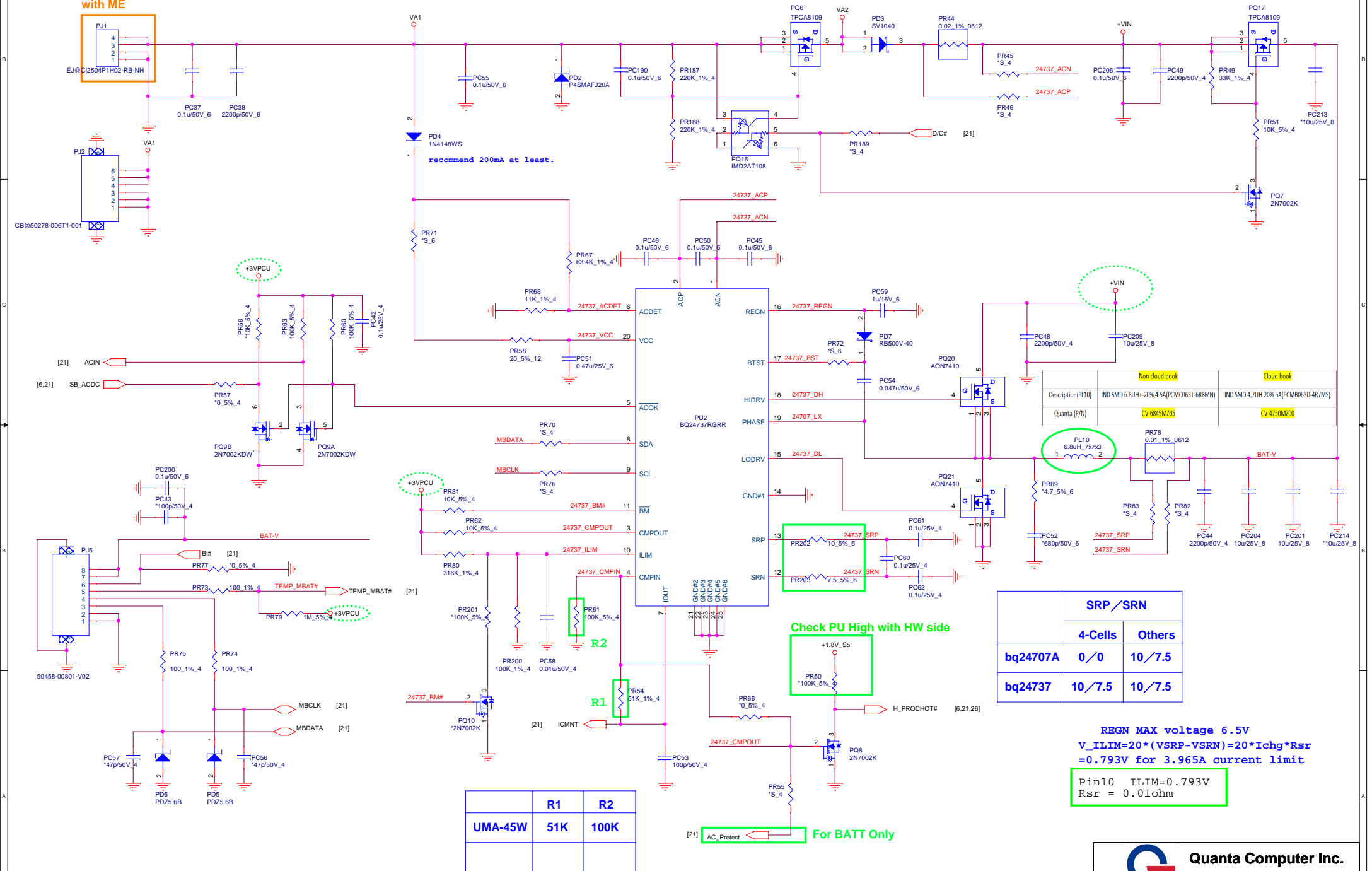
PROJECT : ZAJ

Size	Document Number
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		KBC IT8987E_CX
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Date: Thursday, February 23, 2017 Sheet 21 of 3

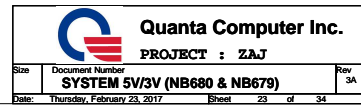
Double Check ADP-IN Connector with ME



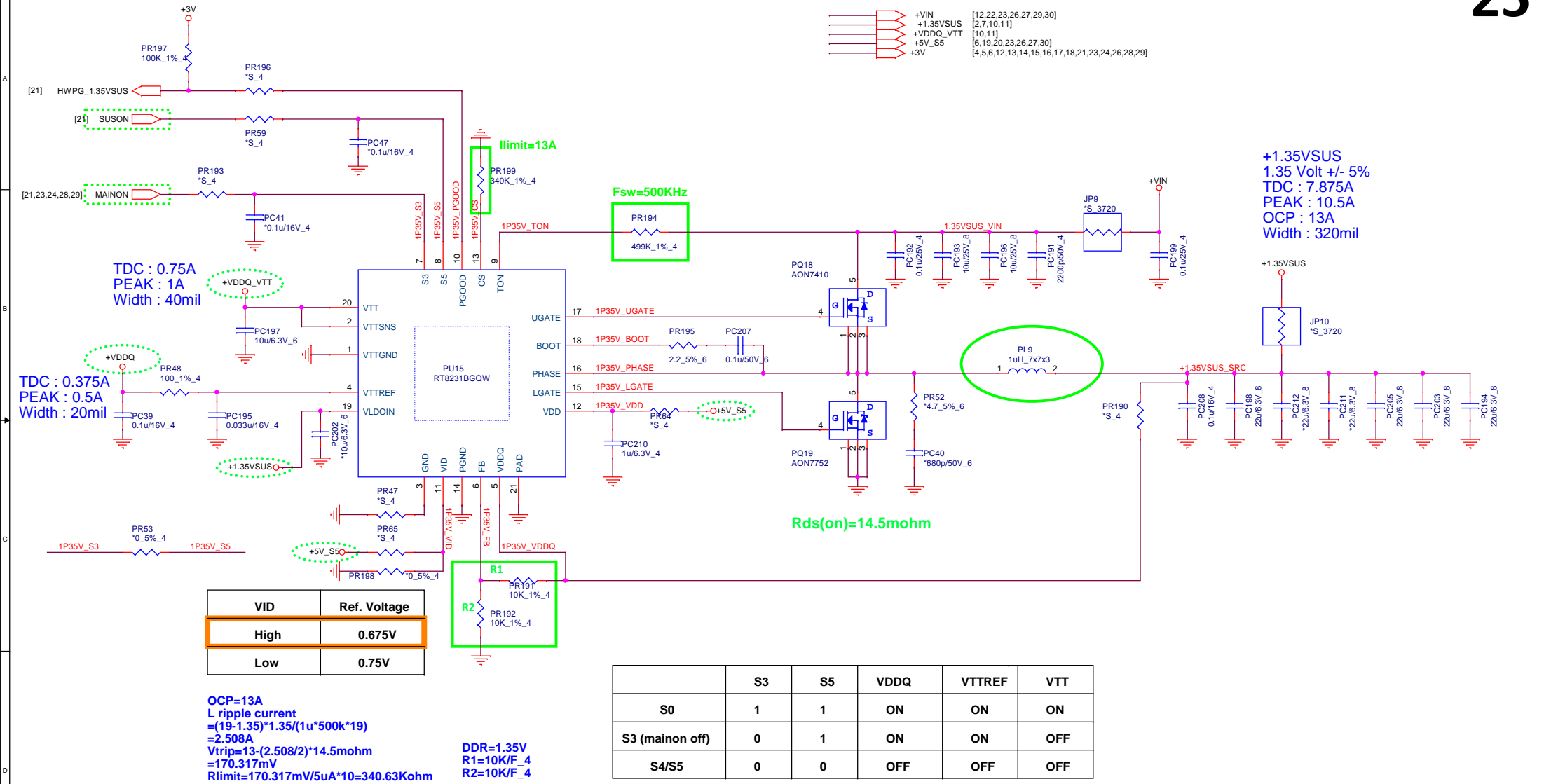
	SRP / SRN	
	4-Cells	Others
bq24707A	0 / 0	10 / 7.5
bq24737	10 / 7.5	10 / 7.5

REGN MAX voltage 6.5V
 $V_{ILIM} = 20 * (VSRP - VSRN) = 20 * I_{chg} * R_{sr}$
 = 0.793V for 3.965A current limit

Pin10 ILIM=0.793V
Rsr = 0.01ohm



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Quanta Computer Inc.

PROJECT :

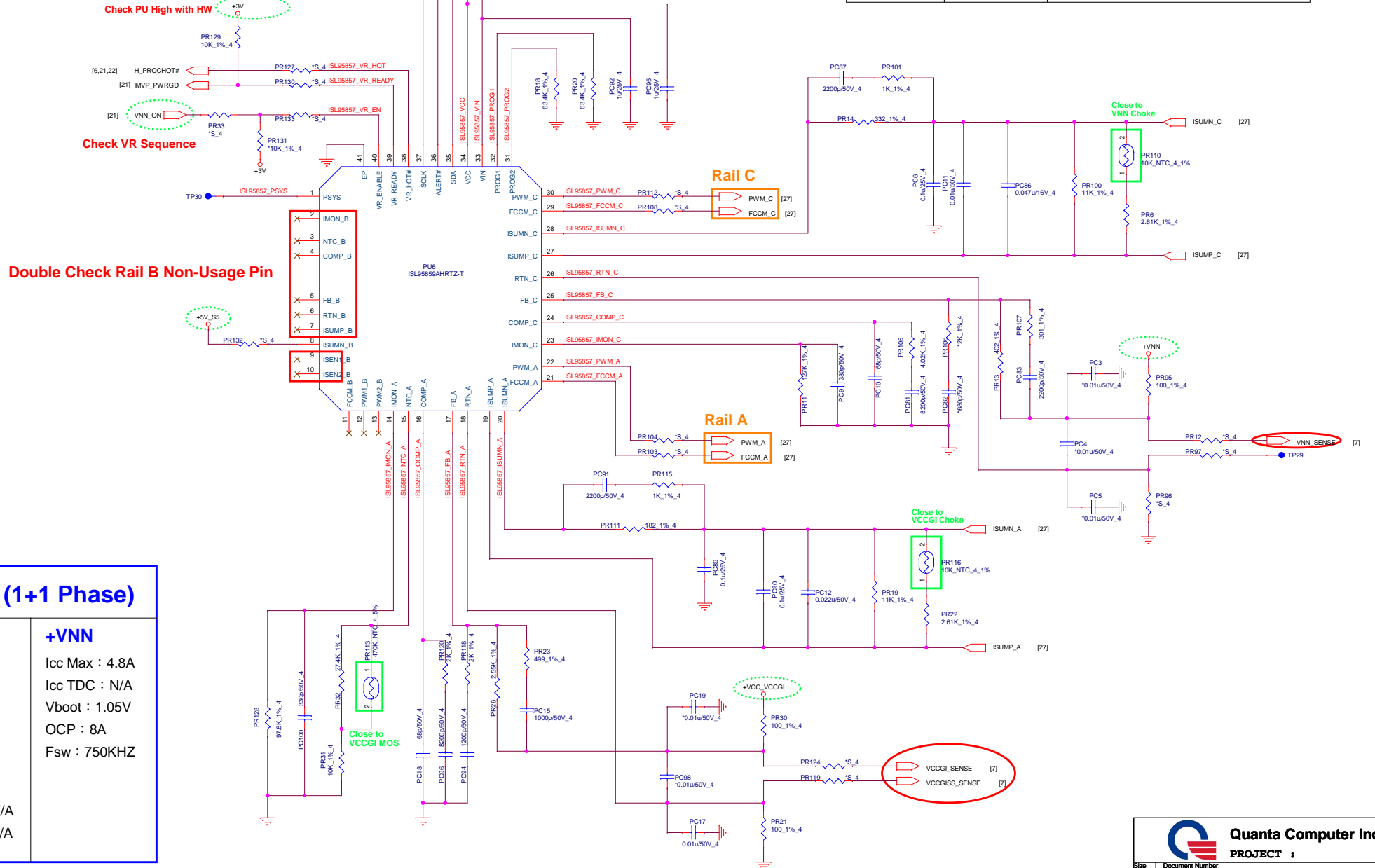
Size	Document Number	Rev
	DDR3L (RT8231BGQW)	3A
Date:	Thursday, February 23, 2017	Sheet 25 of 34

SVID_CLK : UP:85 ohm Series:95 ohm
 SVID_ALERT : UP:68 ohm Series:220 ohm
 SVID_DATA : UP:170 ohm Series:20 ohm

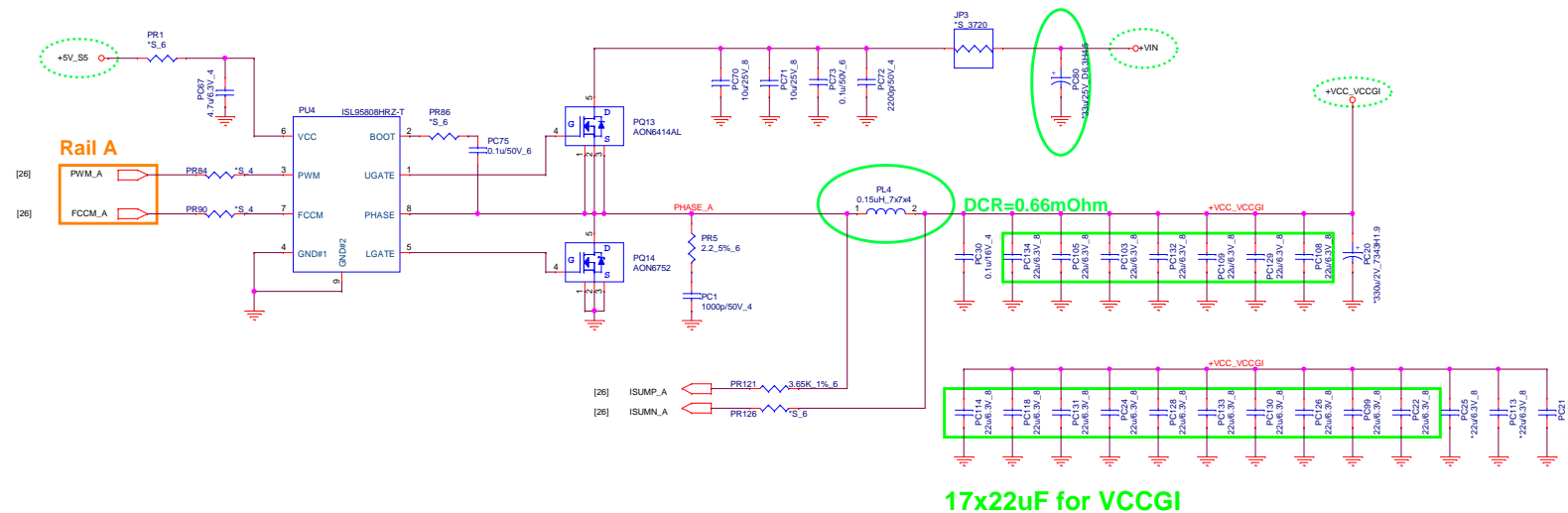
IMVP8 VR Controller

Rail A (1 phase) : +VCCGI
 Rail C (1 phase) : +VNN

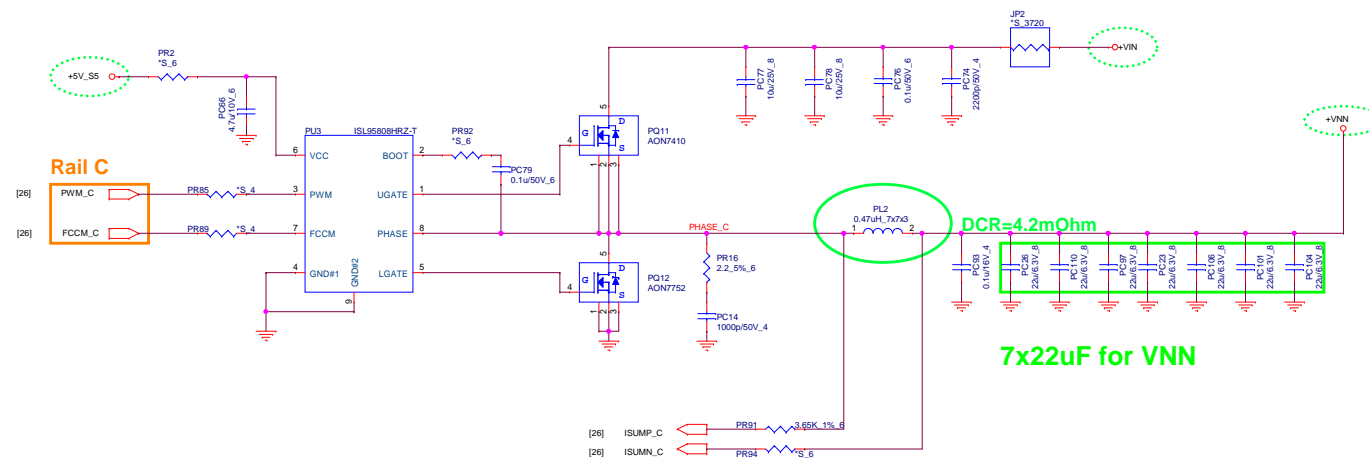
Cloud book	P/N	Description
PR14	CS16342FB17	RES CHIP 634 (1/16W +-1%0402)
PC86	CH3226K1B00	CAP CHIP 0.022U 50V(+/-10%,X7R,0402)
PR111	CS12322FB09	RES CHIP 232 1/16W +-1%(0402)
PC90	CH3683K9B00	CAP CHIP 0.068U 16V(+/-10%,X5R,0402)



VCCGI



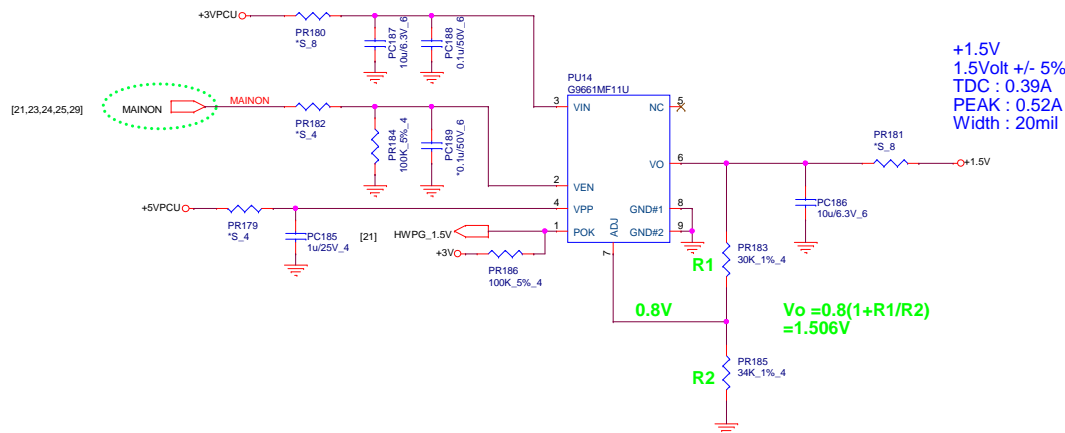
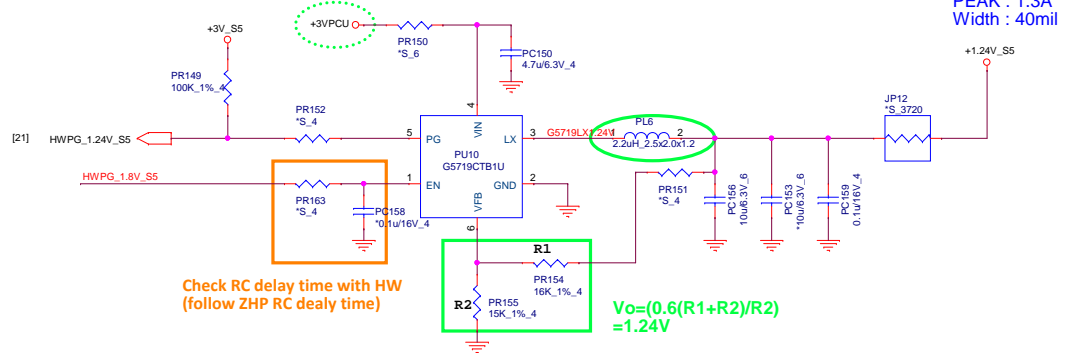
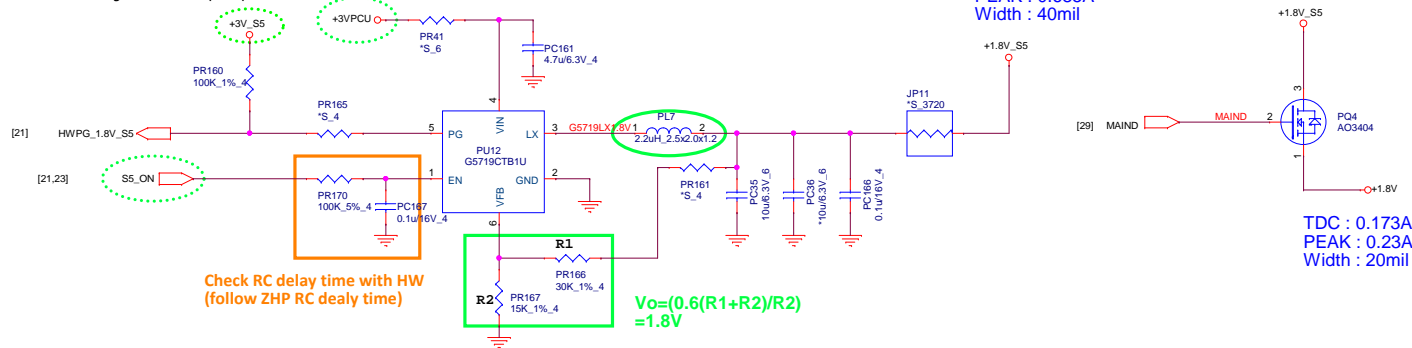
VNN



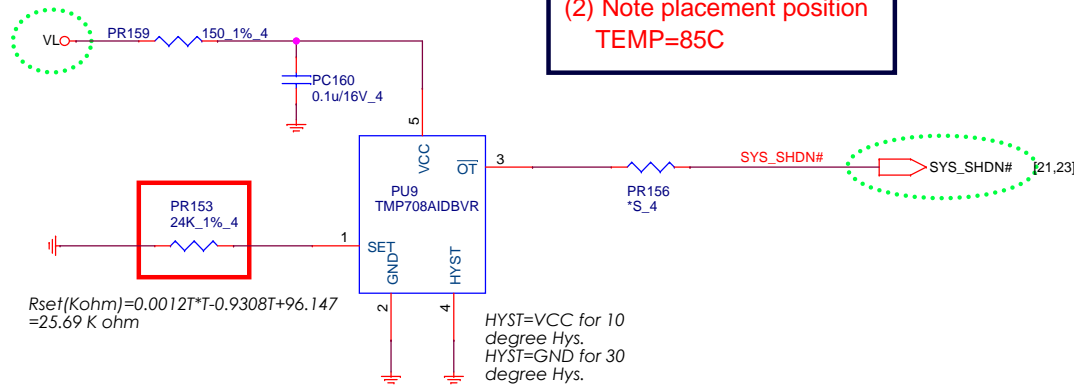
[6,12,13,14,19,21,22,23,24] +3VPCU
 [3,5,6,7,9,15,16,17,18,22] +1.8V_S5
 [7] +1.24V_S5
 [12,13,29] +1.8V
 [14] +1.5V

[5,6,7,15,16,18,20,21,23] +3V_S5
 [23] +5VPCU
 [4,5,6,12,13,14,15,16,17,18,21,23,24,25,26,29] +3V

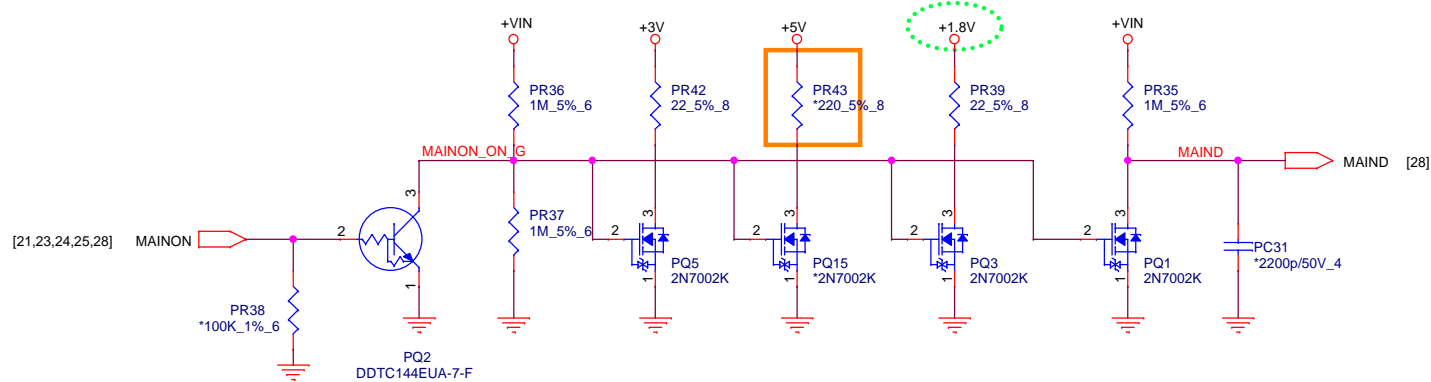
ZHP change +1.8V_S5 PG pull up to +3V_S5



- (1) Need fine tune for thermal protect point
- (2) Note placement position
TEMP=85C

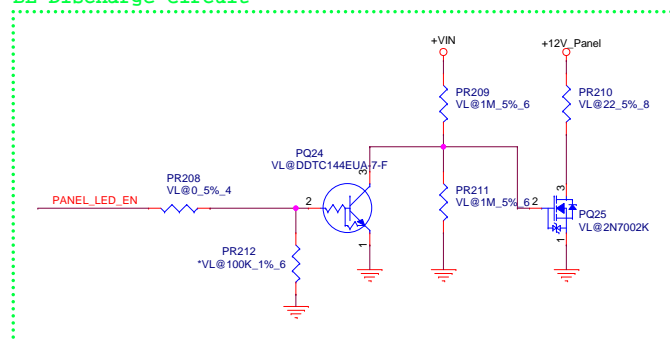
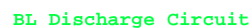


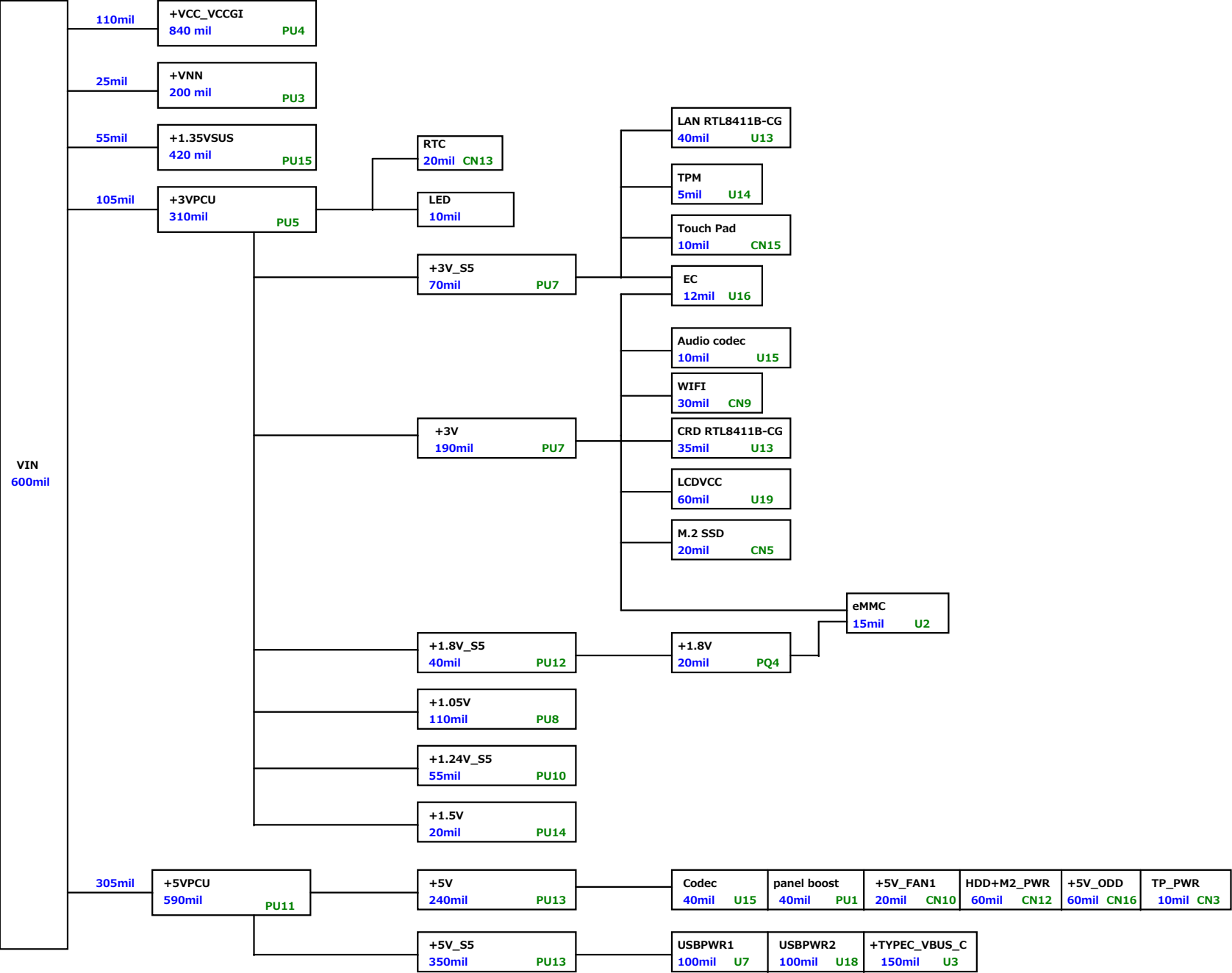
+5V PU High R= 220 ohm for Bo-Bo sound issue.

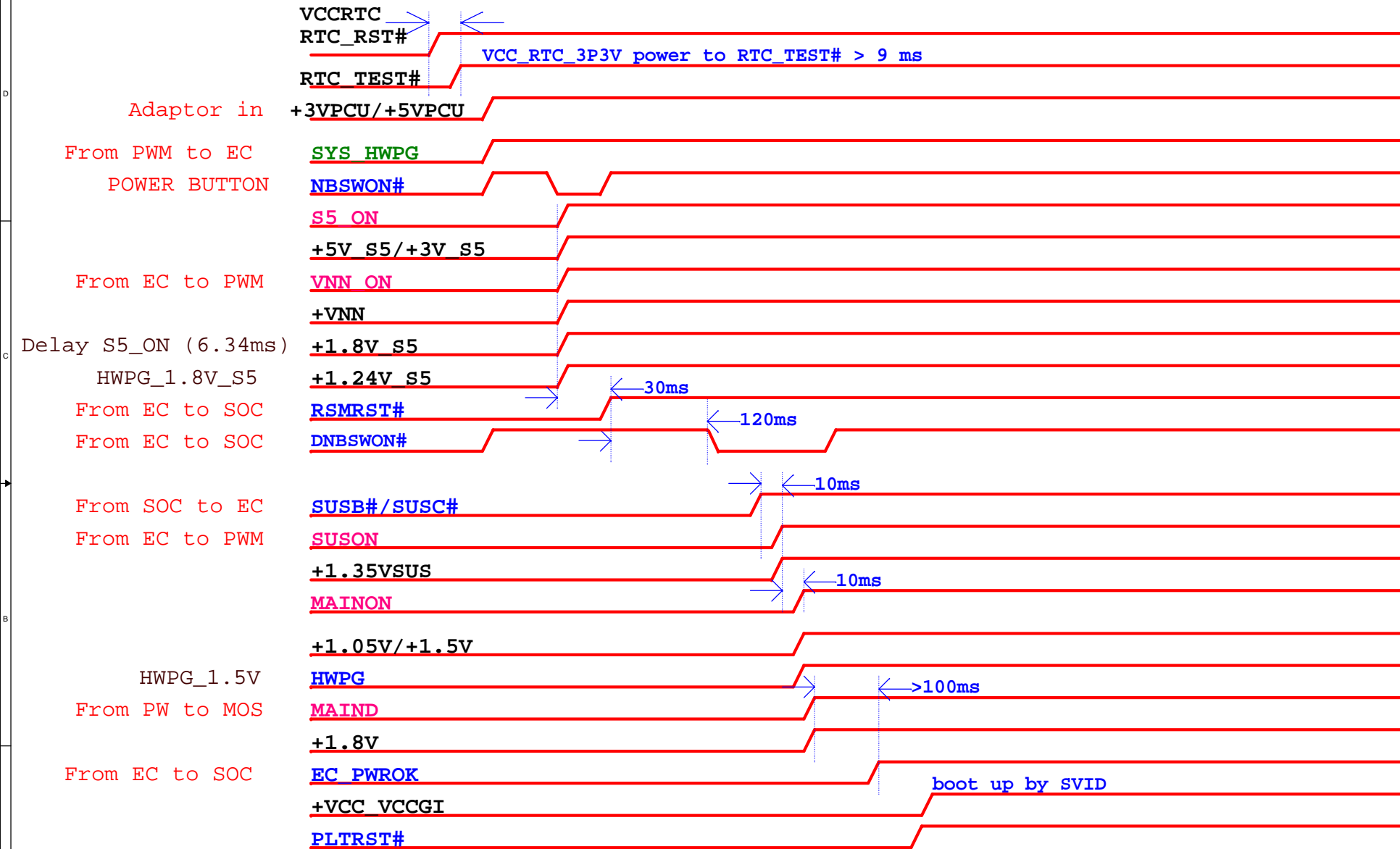


PROJECT :

Size	Document Number Thermal / Discharge	Rev 3A
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Quanta Computer Inc.

PROJECT : ZAJ

Size	Document Number	Rev
	Power on Sequence	3A

Date: Thursday, February 23, 2017 Sheet 32 of 34

Power plane	Description	S0	S3	S5
+VIN	Adaptor power supply	ON	ON	ON
+VCC_VCCGI	Variable voltage supply to CPU and Graphics Core and ISP logic	ON	OFF	OFF
+VNN	Variable voltage supply to other (non core) logic	ON	OFF	OFF
+1.05V	Fixed voltage rail for SRAM,I/O,internal Logic	ON	OFF	OFF
+1.24V_S5	Fixed voltage rail for SoC L2/ Audio & ISH I/O Logic and PLLs MPHY Logic/ USB2-I/O/MIPI I/Os	ON	ON	ON
+1.8V_S5	Fixed voltage rail for all GPIOs	ON	ON	ON
+1.35VSUS	Fixed voltage rail for DDR3L IO	ON	ON	OFF
+3V_RTC	Fixed Voltage rail for RTC (Real Time Clock)	ON	ON	ON
+1.8V	1.8V S0 power rail	ON	OFF	OFF
+1.5V	1.5V S0 power rail	ON	OFF	OFF
+5VPCU	5V always on power rail	ON	ON	ON
+5V_S5	5V S5 power rail	ON	ON	ON
+5V	5V S0 power rail	ON	OFF	OFF
+3VPCU	3V always on power rail	ON	ON	ON
+3V_S5	3V S5 power rail	ON	ON	ON
+3V	3V S0 power rail	ON	OFF	OFF

Model	Date	CHANGE LIST
ZAJ REV.D	02/10	1.Remove U33/R482 2.Change 0 ohm to shortpad : R403,R404,R405,R406,R407,R408,R409,R410,R104,R113,R108,R115,R99,R402,R167,R165,R161,R158,R157,R153,R270,R271,R272,R273 3.Change C34 from 18pF to 15pF 4.Un-stuff R380/R464 (debug card circuit) 5.Change PR5/PR16 from 1% to 5%
	02/16	1.Remove HDMI EMI resistor -R131/R136/R141/R124
	02/18	1.Unstuff SW3 2.Update SW2 FP to "sw-ds-a40e-4p-smt" by SMT request 3.Update CN2 FP to "sdcard-156-1001902602-11p-smt" by SMT request 4.Update CN9 FP to "nglfl-apci0076-p001a-75p-ke-smt" by SMT request
	02/20	1.Un stuff PC211&PC212 then stuff PC203&PC194 by power team request 2.Un stuff PC107&PC112 then stuff PC121&PC122 by power team request 3.Change R158/R161 from shortpad to 0 ohm 4.Add C449&R493 for RSMRST#
	02/23	1.Modify Q31/Q33 from 2N7002 (Vgs=2.5V) to PJA138K (Vgs=1.5V) 2.Change CN14 QPN and FP to DFFC28FR029 -- "50584-0280n-v02-28p-I" by PDC request 3.Change CN17 QPN and FP to DFFC34FR026 -- "196332-34041-3-34p-I" by PDC request