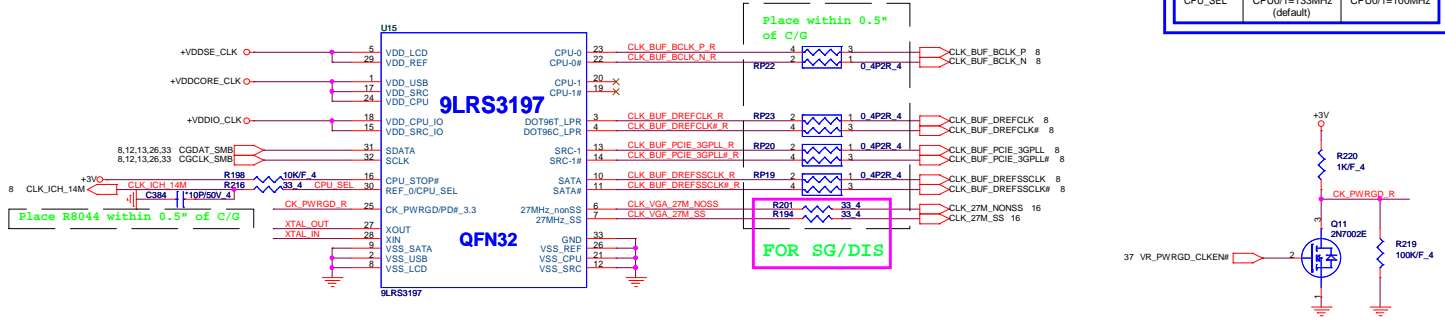
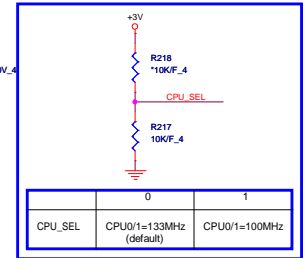
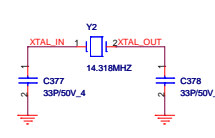
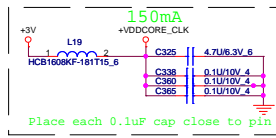
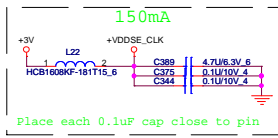
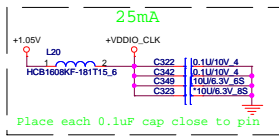
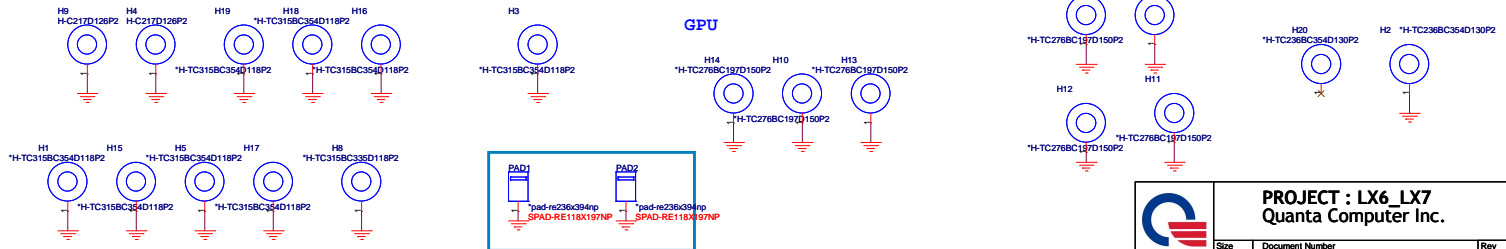
 <b>NB5</b>	<b>PROJECT : LX6_LX7</b> <b>Quanta Computer Inc.</b>	
	Size Custom	Document Number <b>BLOCK DIAGRAM</b>
Date: Tuesday, February 02, 2010    Sheet 1 of 44		

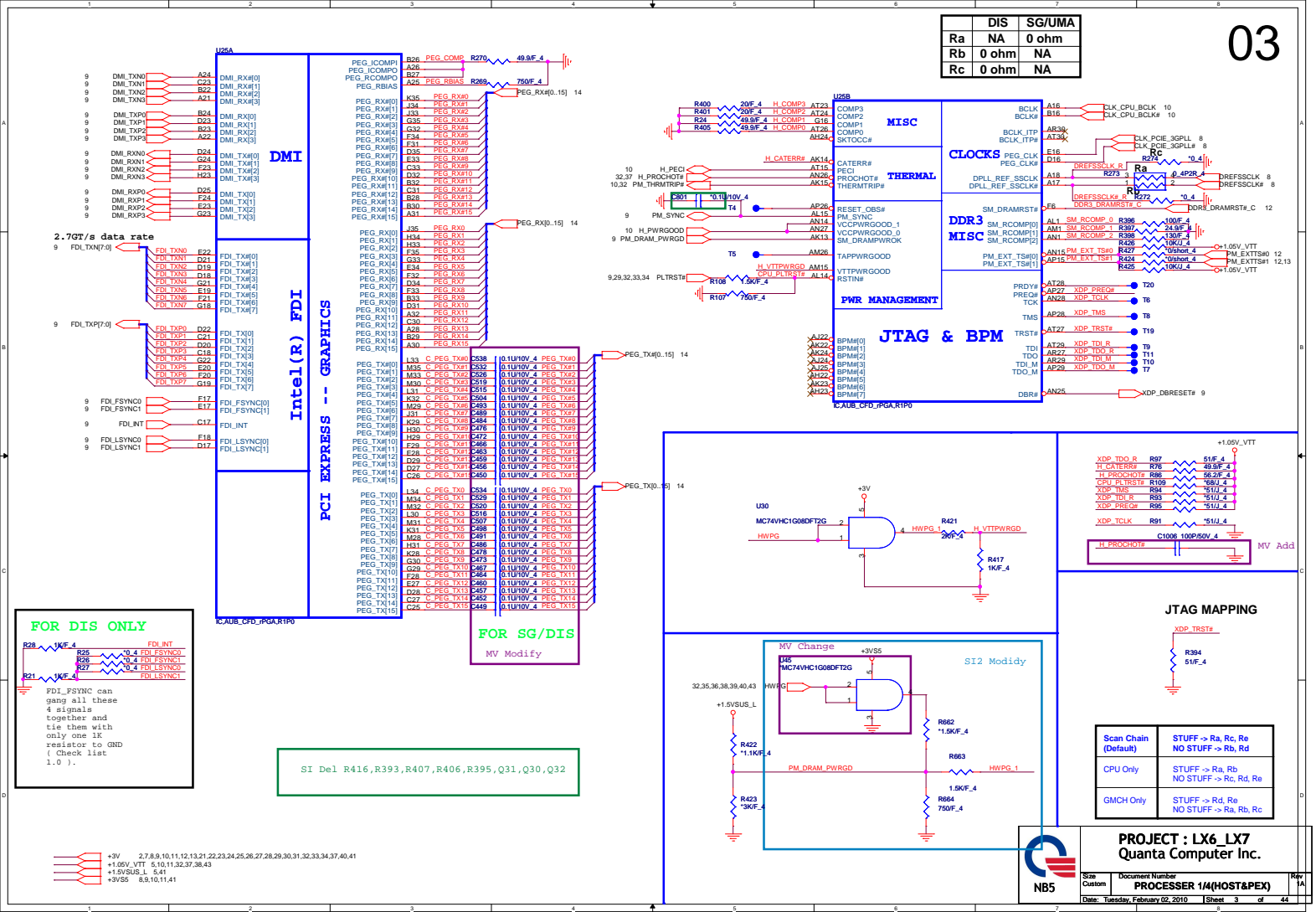


+1.05V 7,8,9,11,36,37,43  
 +1.5V 33,41  
 +3V 3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,40,41

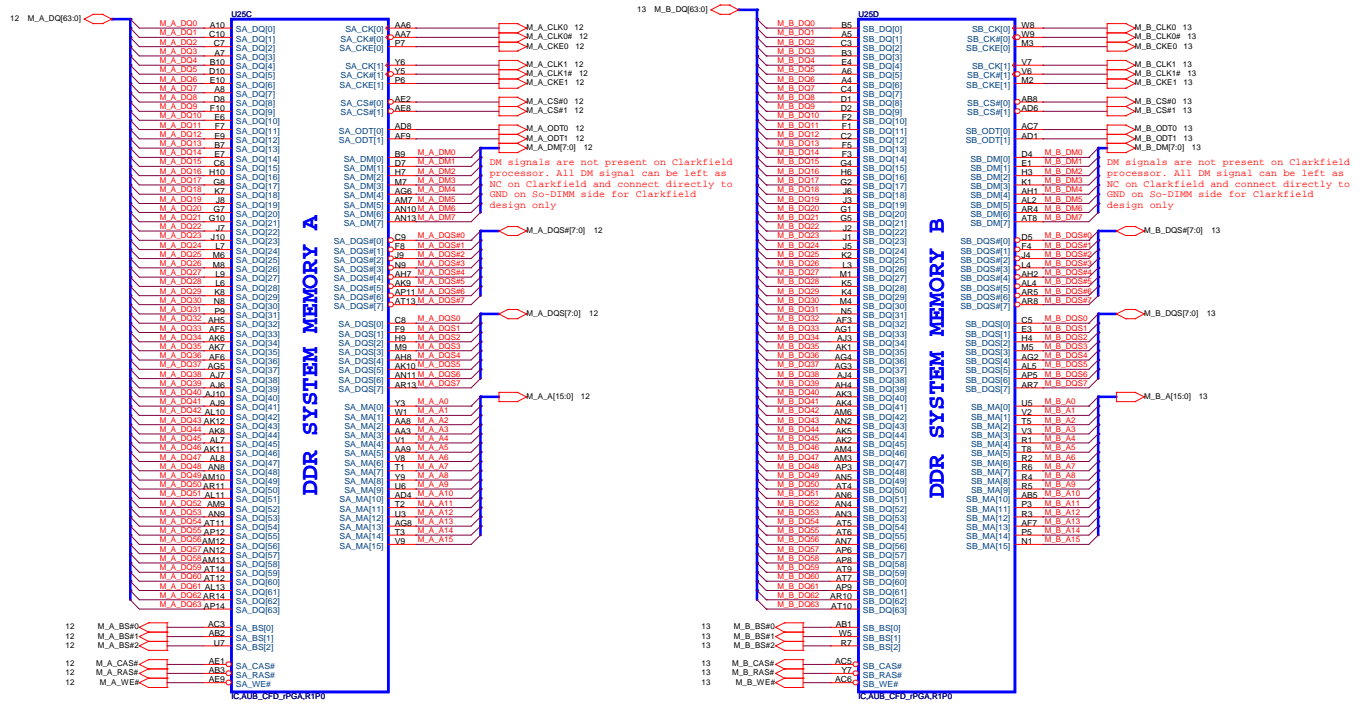
## HOLE

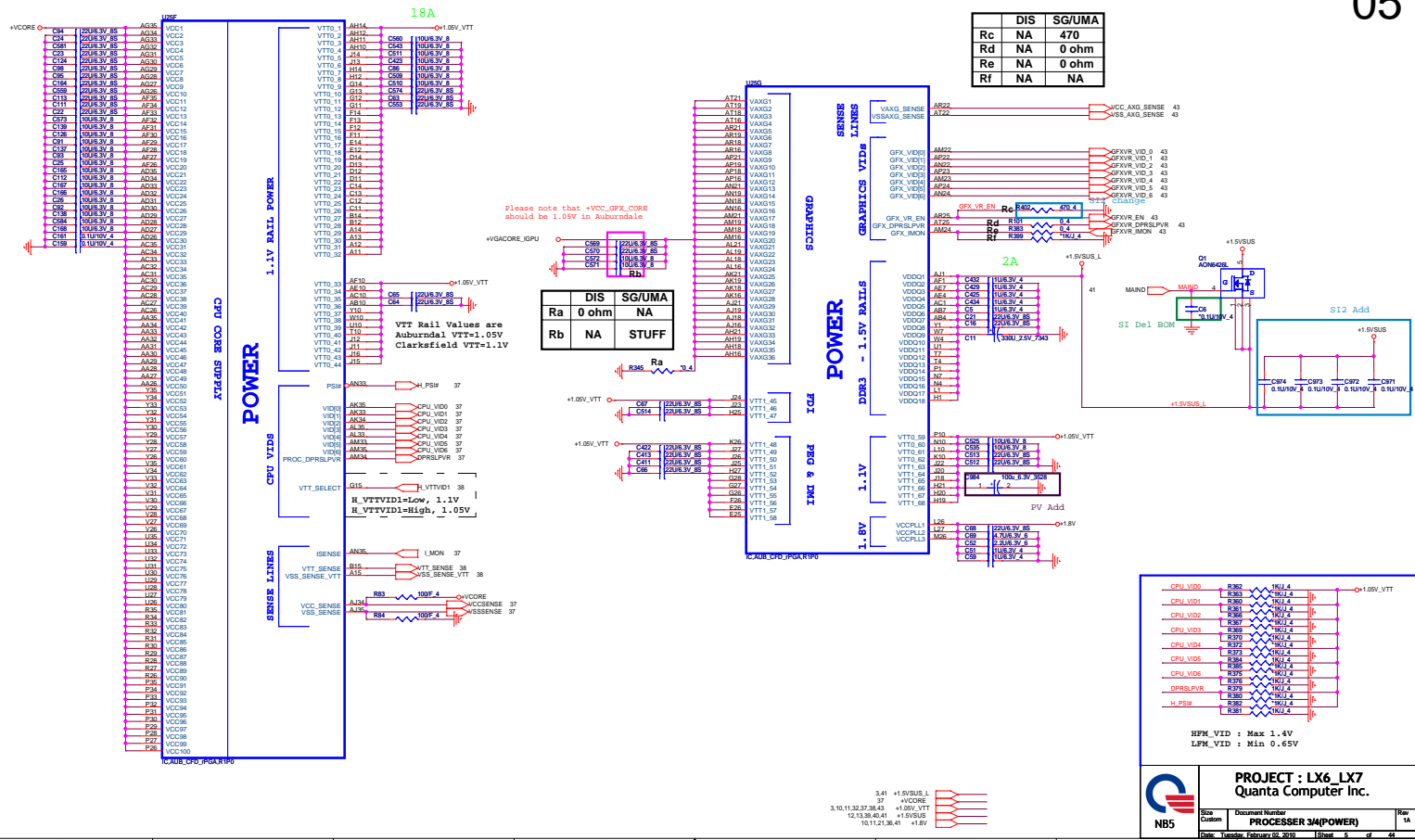


	DIS	SG/UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

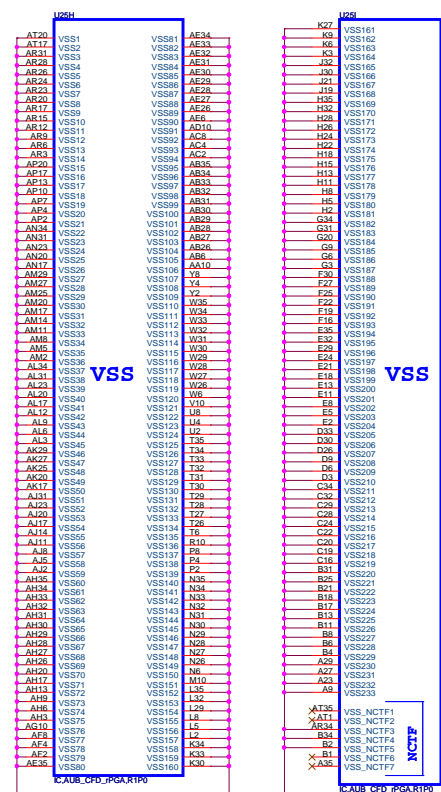


## AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)

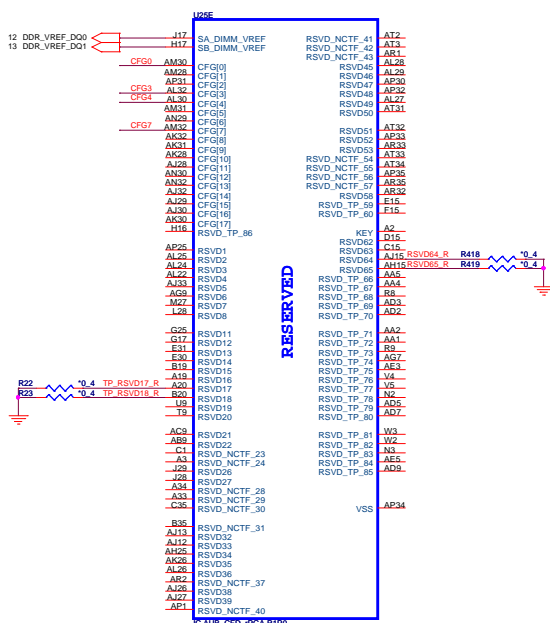




### AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



## AUBURNDALE/CLARKSFIELD PROCESSOR( RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.


	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

	UMA	SG/DIS
R90	NA	NA
R77	NA	3.01K
R79	NA	NA
R87	NA	NA

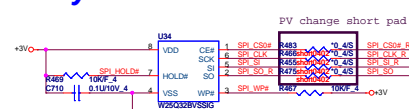
CFG[ 1:0 ] = PCI\_Express Configuration Select

- \* 11 = 1 x 16 PEG
- \* 10 = 2 x 8 PEG

**PROJECT : LX6\_LX7**  
**Qanta Computer Inc.**

	Size	Document Number	Rev
	Custom	<b>PROCESSOR 4/4 (GND)</b>	

NB5



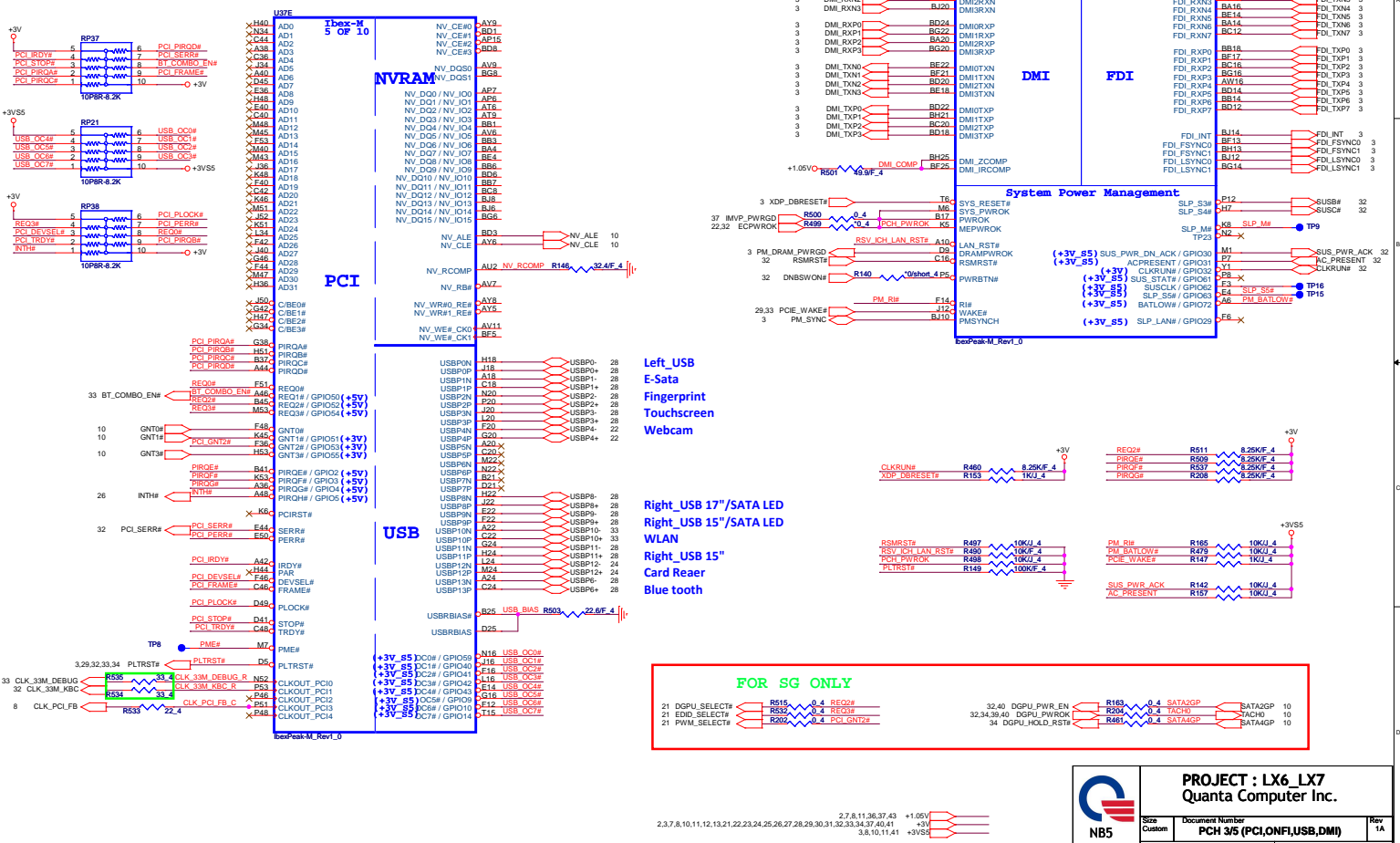
**PROJECT : LX6\_LX7**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>PCH 1/5 (SATA,HDA,LPC)</b>	Rev 1A
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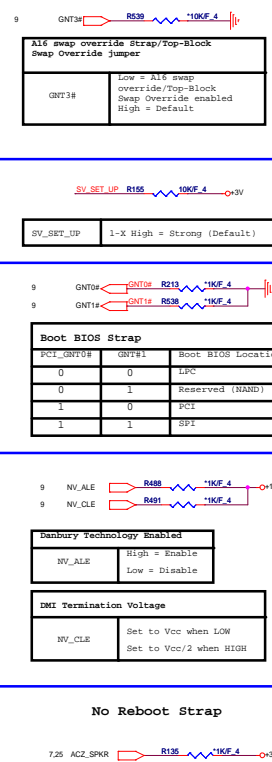




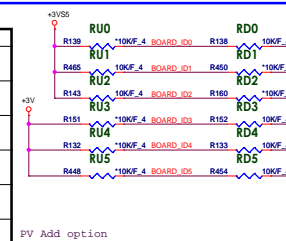
## IBEX PEAK-M (PCI, USB, NVRAM)



## IBEX PEAK-M (GND)



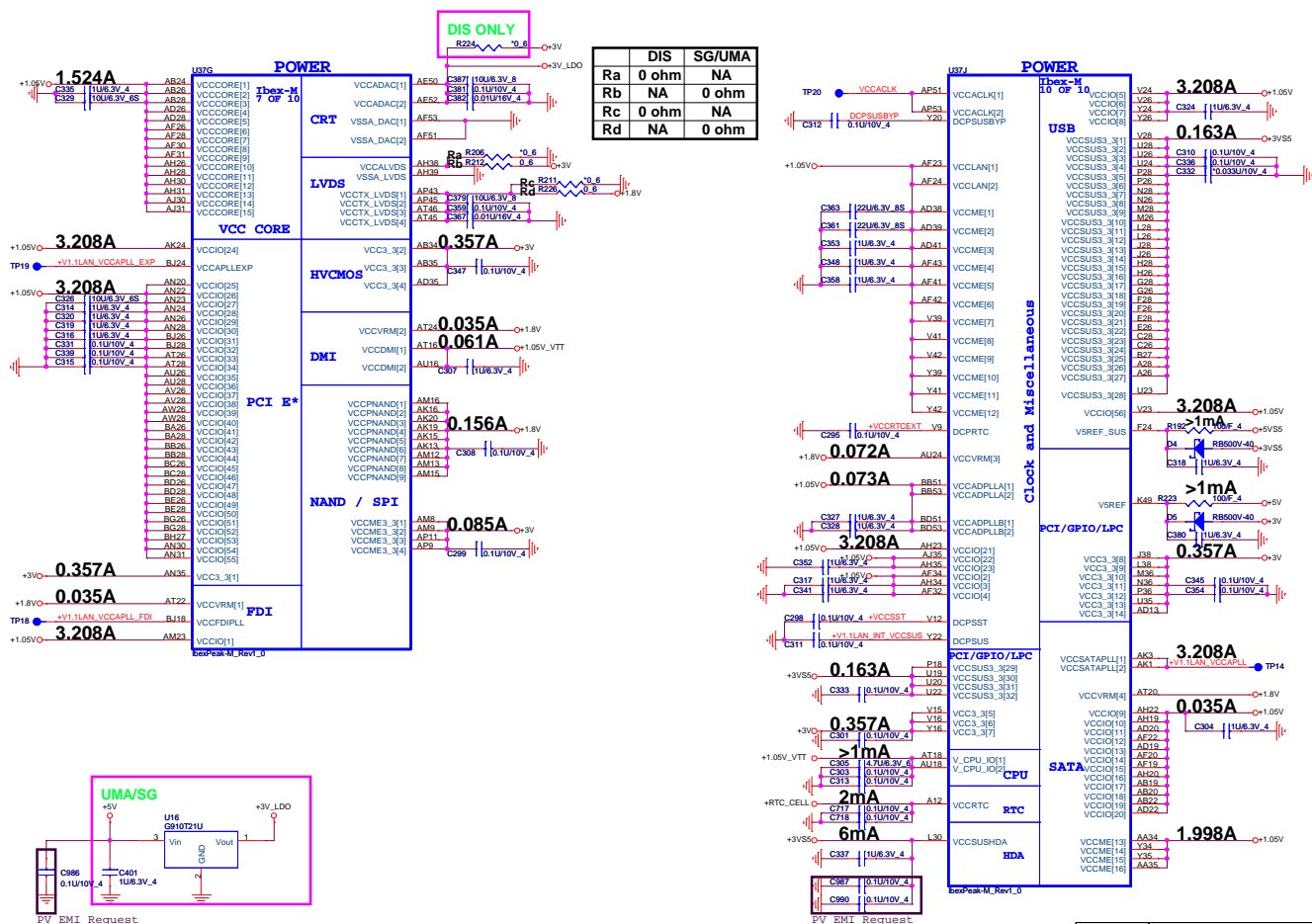
Board ID	ID0	ID1	ID2	ID3	ID4	ID5
LX6	0	1				
LX7	1	0				
Discrete			0	0		
UMA			0	1		
SG			1	0		
LX7 No Subwoofer	1	1				



	PROJECT : LX6_LX7 Quanta Computer Inc.
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PROJECT : LX6\_LX7  
Quanta Computer Inc.



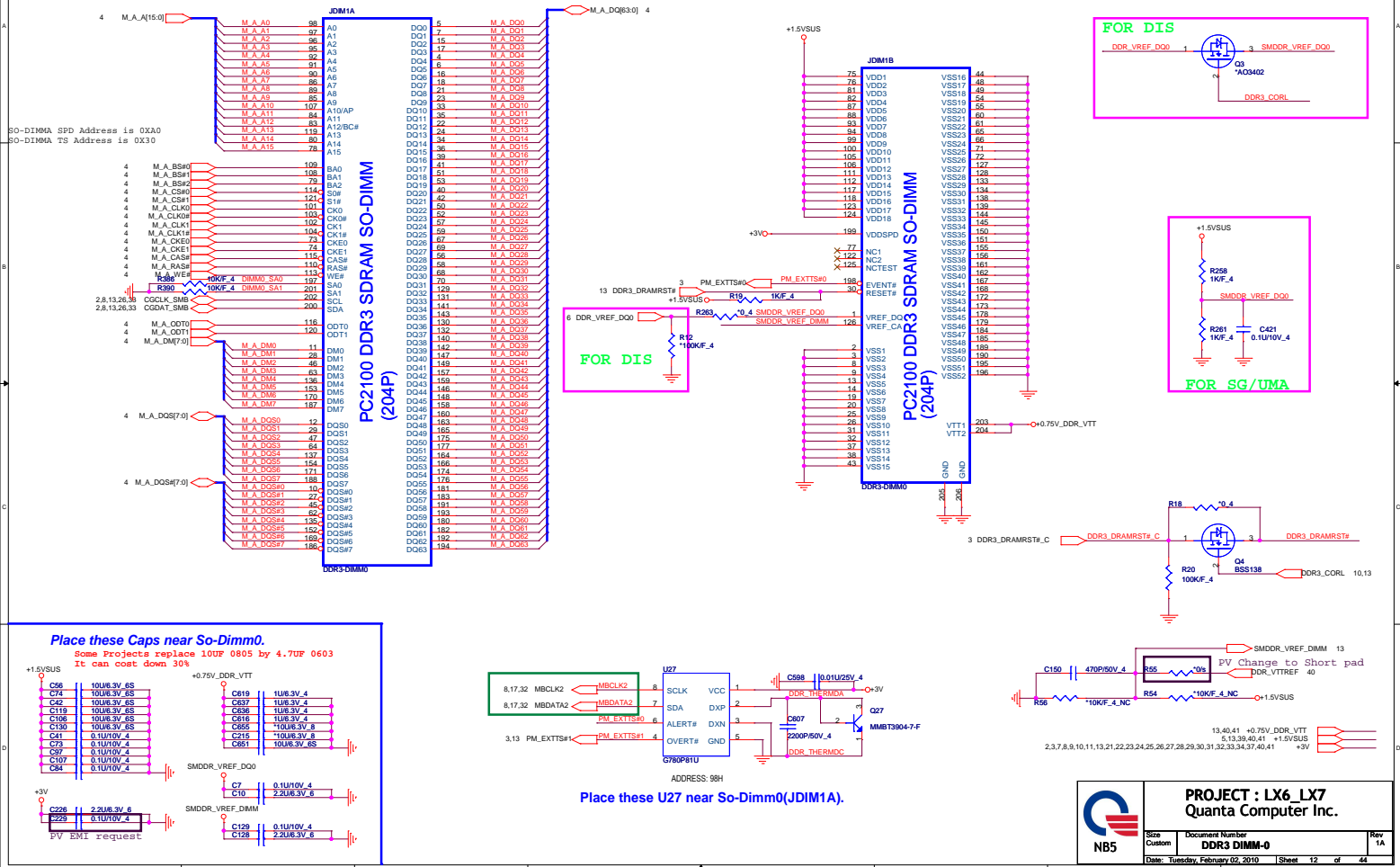
	DIS	SG/UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm

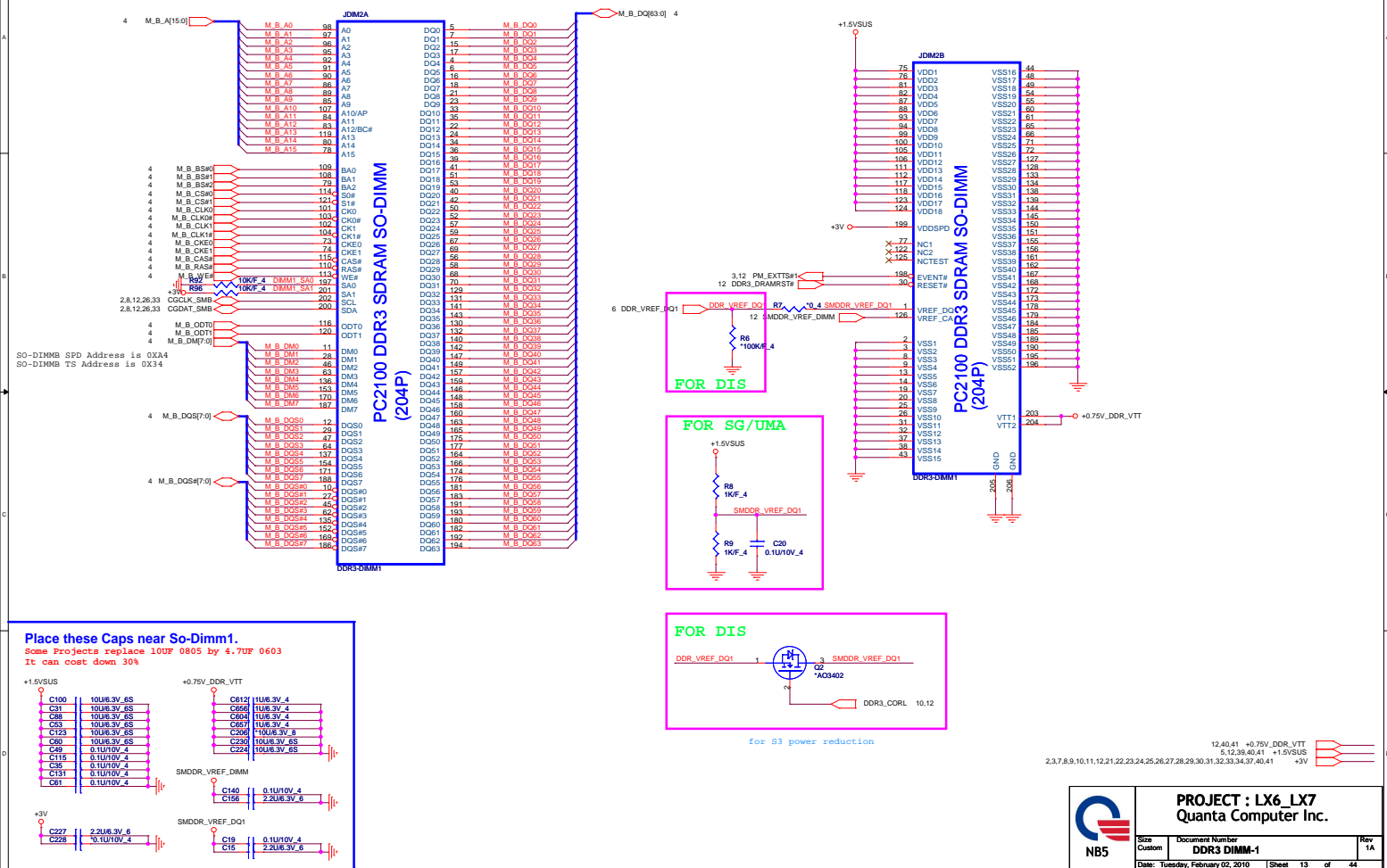
2,3,7,8,9,10,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,34,40,41 +3V  
3,5,10,32,37,38,43 +1.05V\_VTT  
5,10,21,36,41 +1.8V  
21,22,23,25,26,28,30,31,33,34,41 +5V  
41 +5VSS  
7 +RTC\_CELL

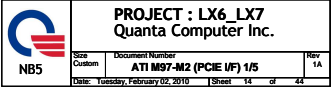


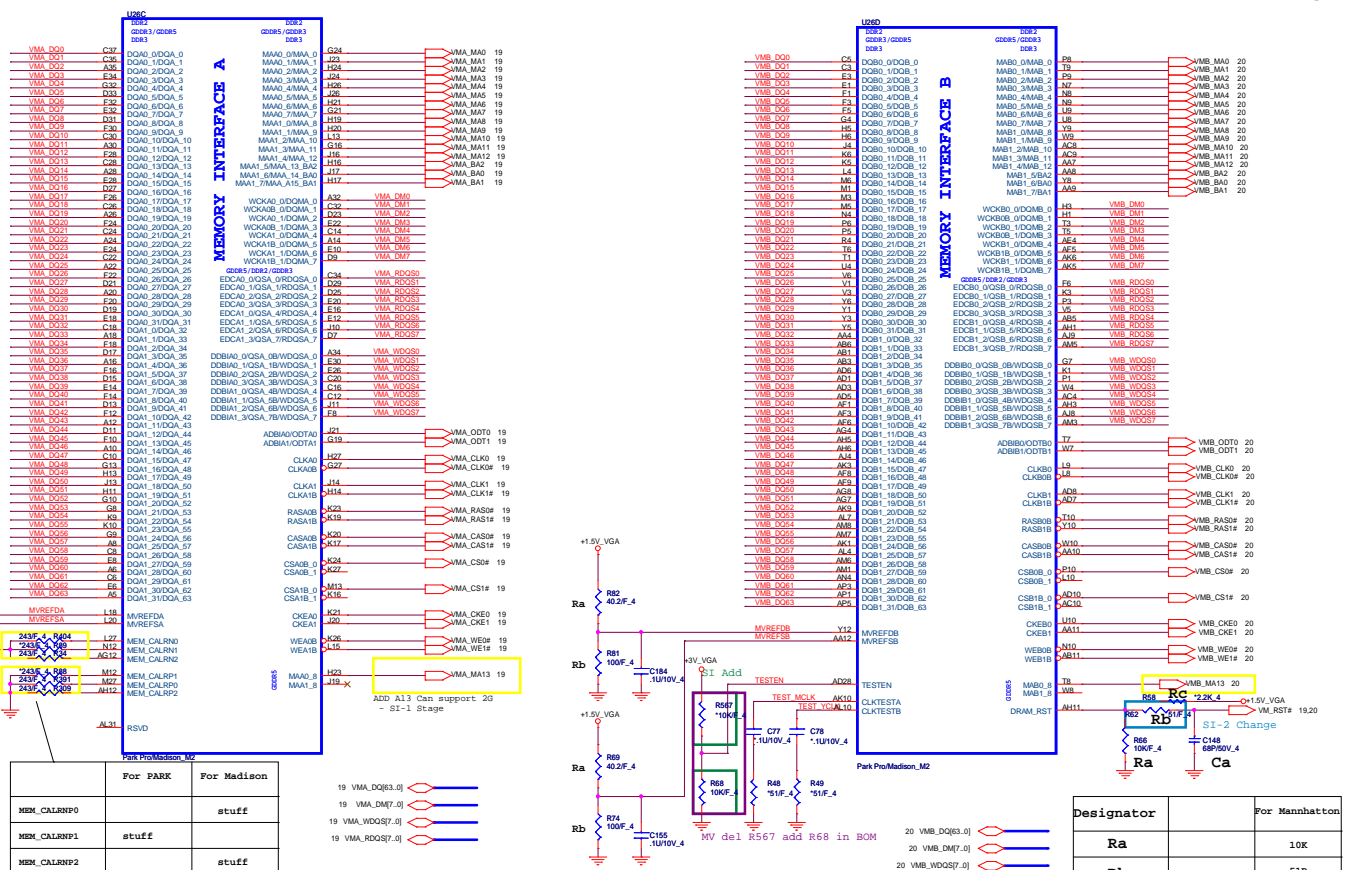
**PROJECT : LX6\_LX7**  
Quanta Computer Inc.

Size Custom	Document Number <b>PCH 5/5 (POWER)</b>	Rev 1A
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Memory Aperture size fix 256M

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

It is a shared pin strap with CONFIG[2:0] if BIOS\_ROM\_EN is set to 0.

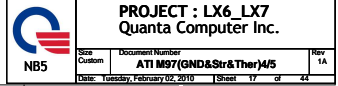


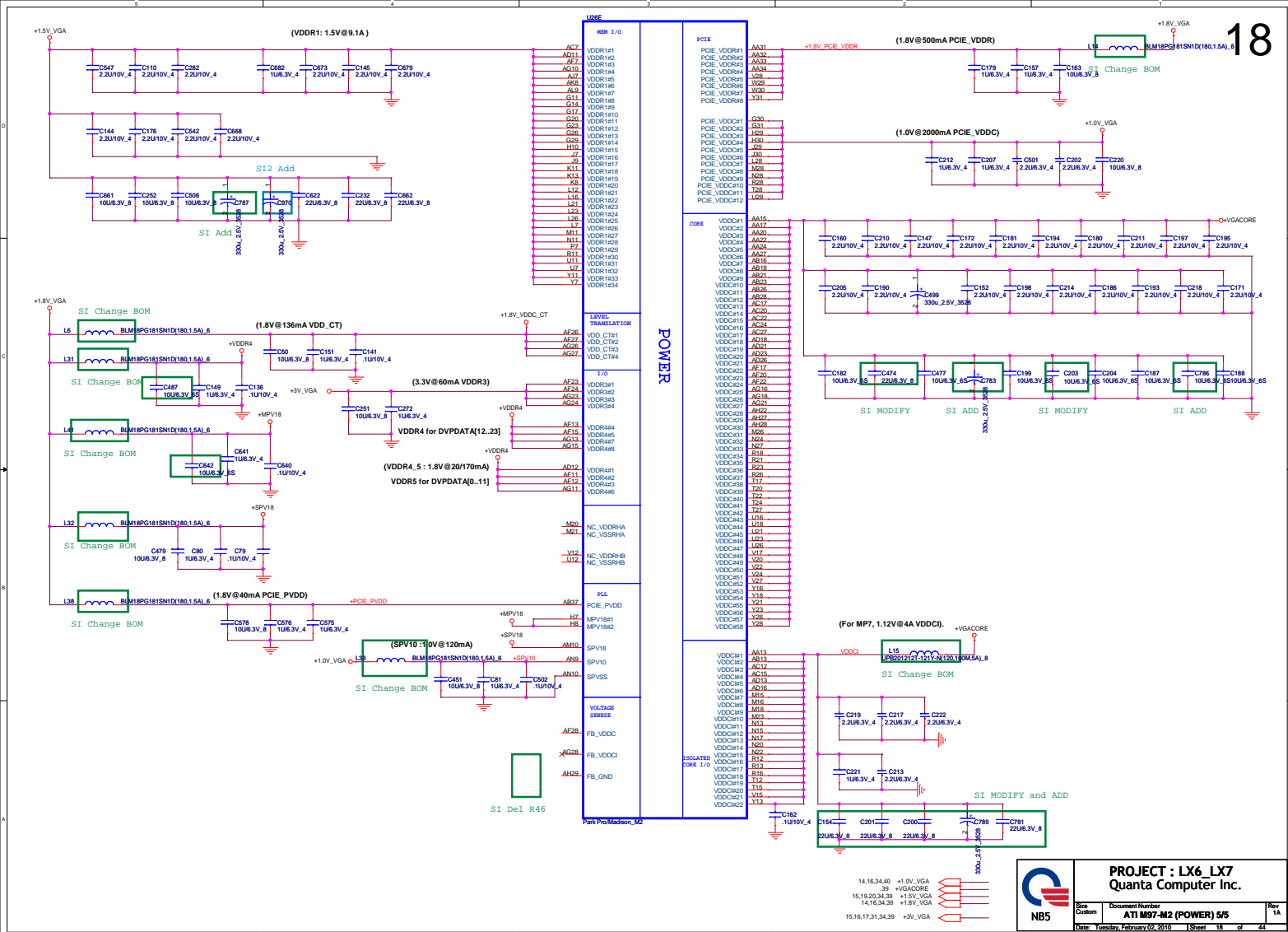
CONFIGURATION STRAPS			RECOMMENDED SETTINGS * DO NOT INSTALL RESISTOR † = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET			
STRAPS	PN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPI00	<b>Transmitter Power Savings Enable</b> 0 0Hz Tx output using for mobile mode 1 full Tx output using (Default setting for Desktop)	1
TX_DEEMPH_EN	GPI01	<b>PCI Express Transmitter De-emphasis Enable</b> 0 Tx de-emphasis disabled for mobile mode 1 Tx de-emphasis enabled (Default setting for Desktop)	1
BIF_GEN2_EN_A	GPI02	0 = Advise the PCI-E device as 2.5 GT/s capable at power-on. 1 = Advise the PCI-E device as 5.0 GT/s capable at power-on. 5.0 GT/s capability will be controlled by software.	0
RSVD BIF_VGA_DIS	GPI08 GPI09 GPI021	VGA ENABLED	0 0 0
BIOS_ROM_EN	GPI0_22_RMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2)	GPI0(13:11)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS	0
RSVD AUDI[1] AUDI[0]	GENERIC HSYNC VSYNC	AUDI[1] AUDI[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	0 0 11

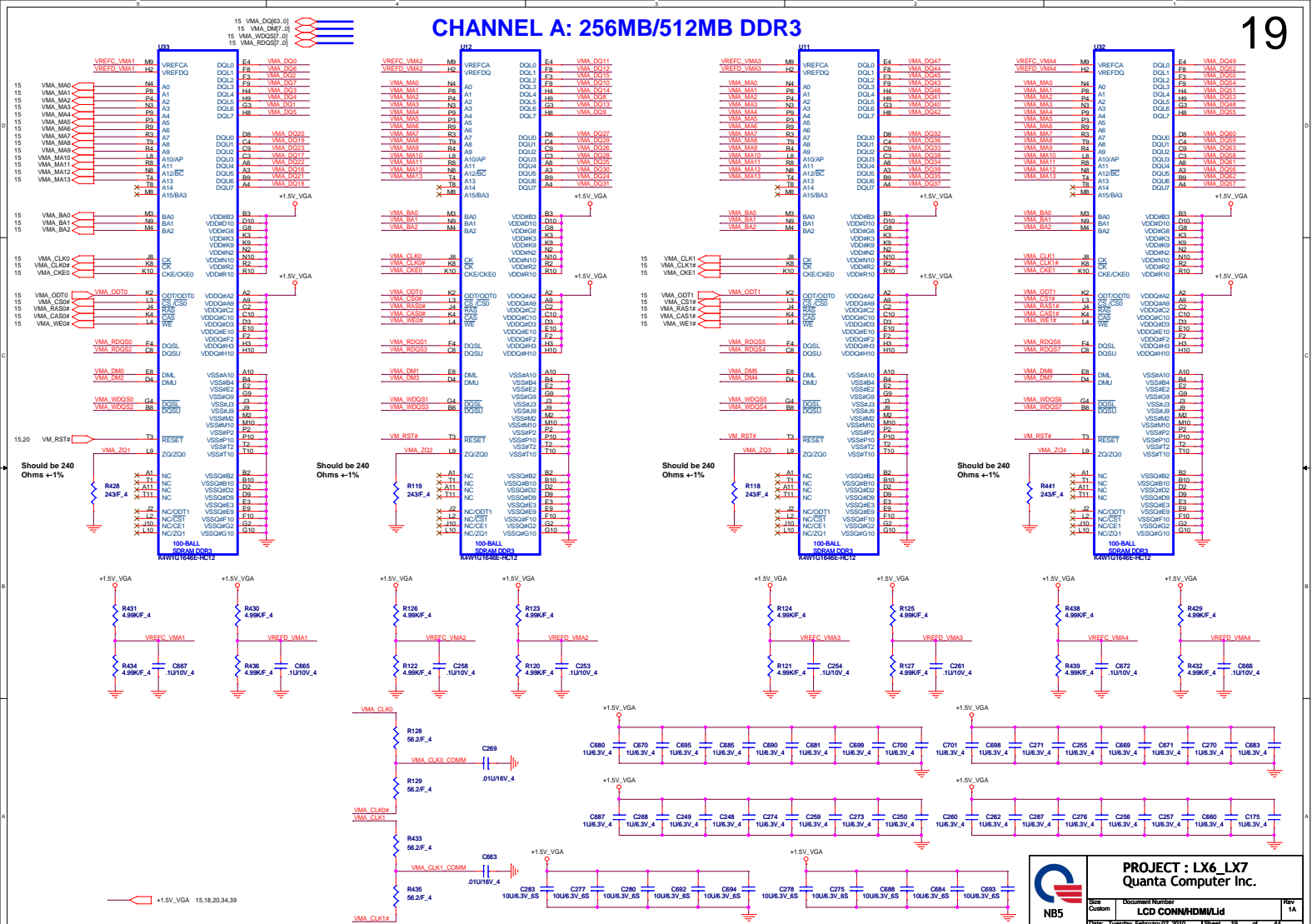
## AMD RESERVED CONFIGURATION STRAPS

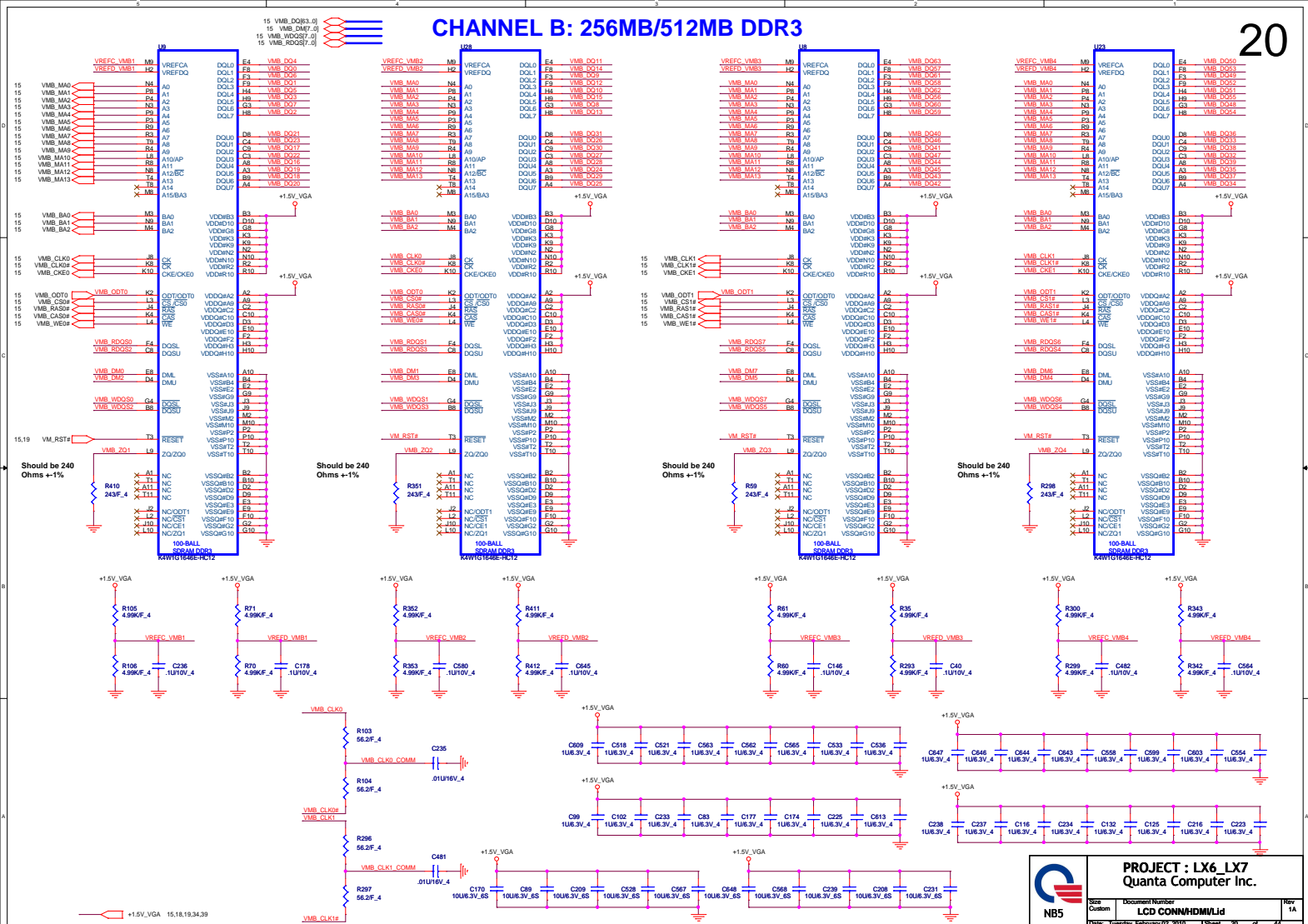
**ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET**

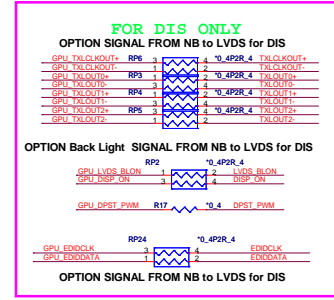
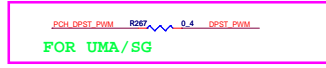
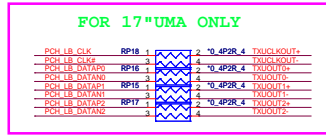
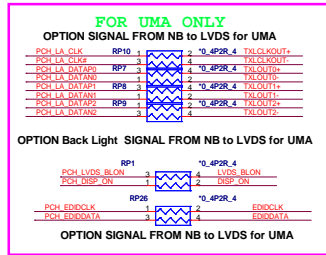
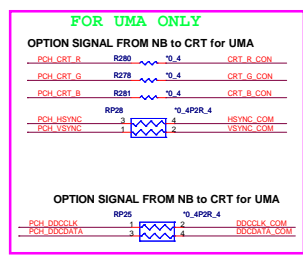
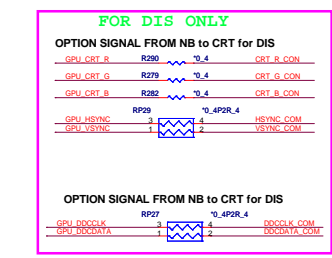
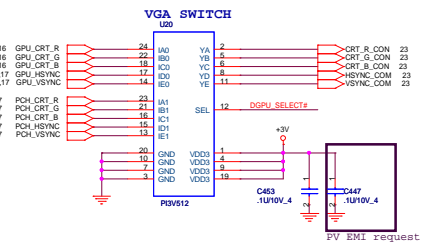
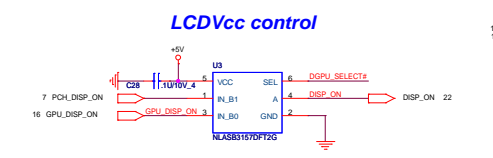
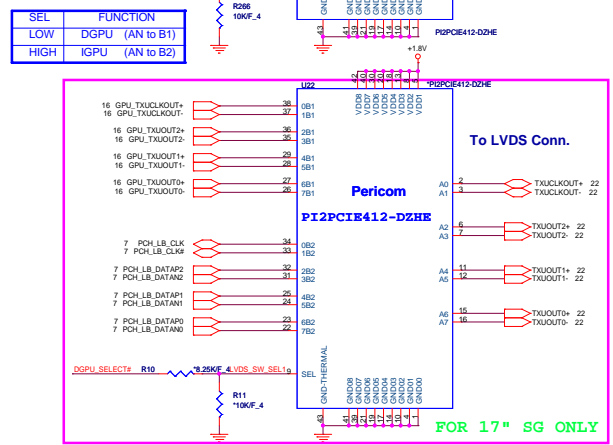
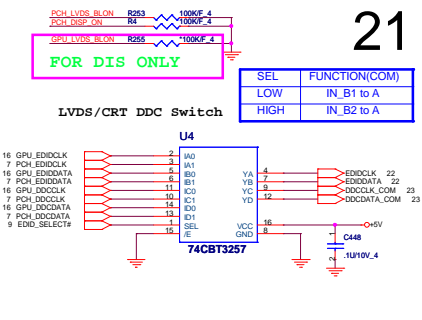
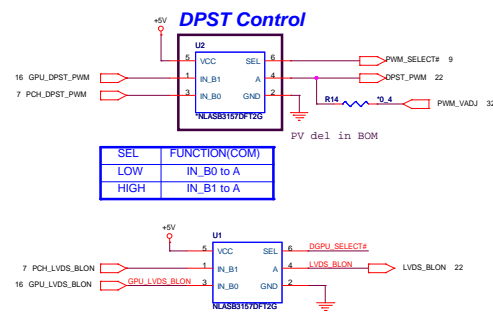
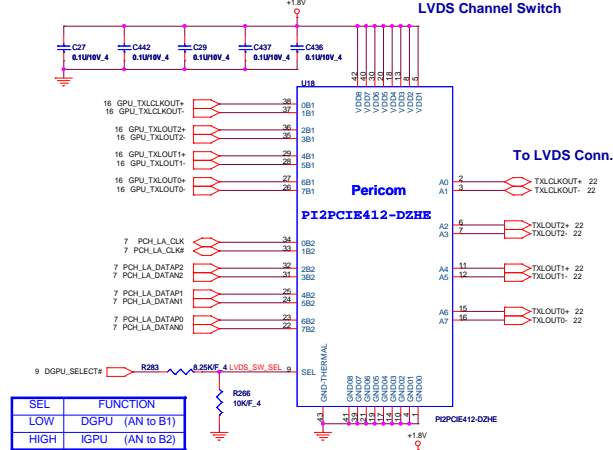
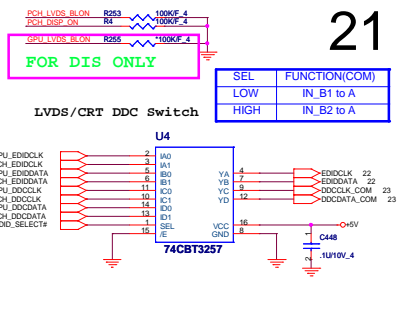
HQSYNCR	GENERICDC
<p><b>PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET</b></p>	
GPIOD21_BB_EN	

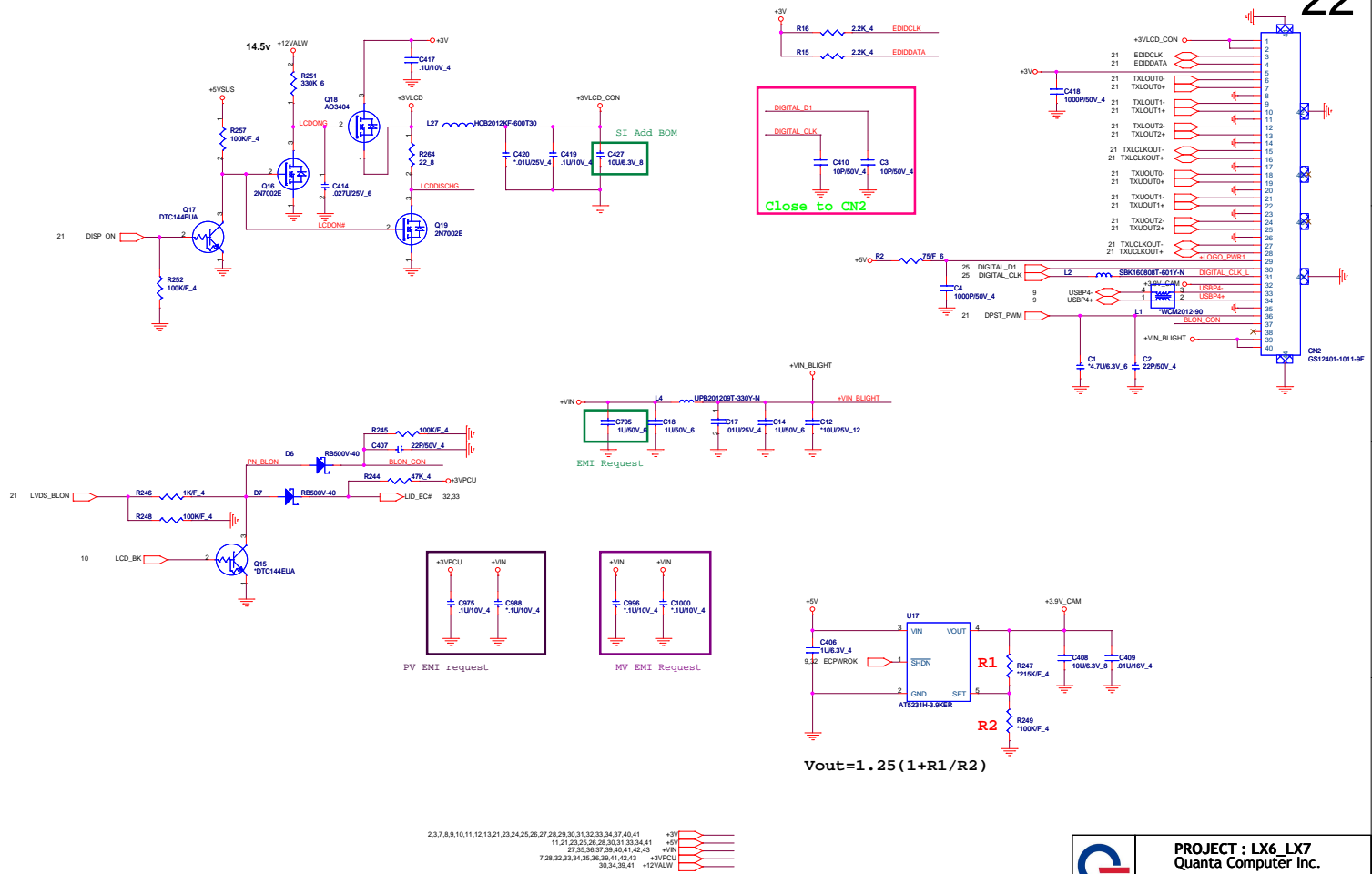


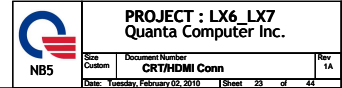
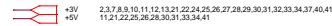








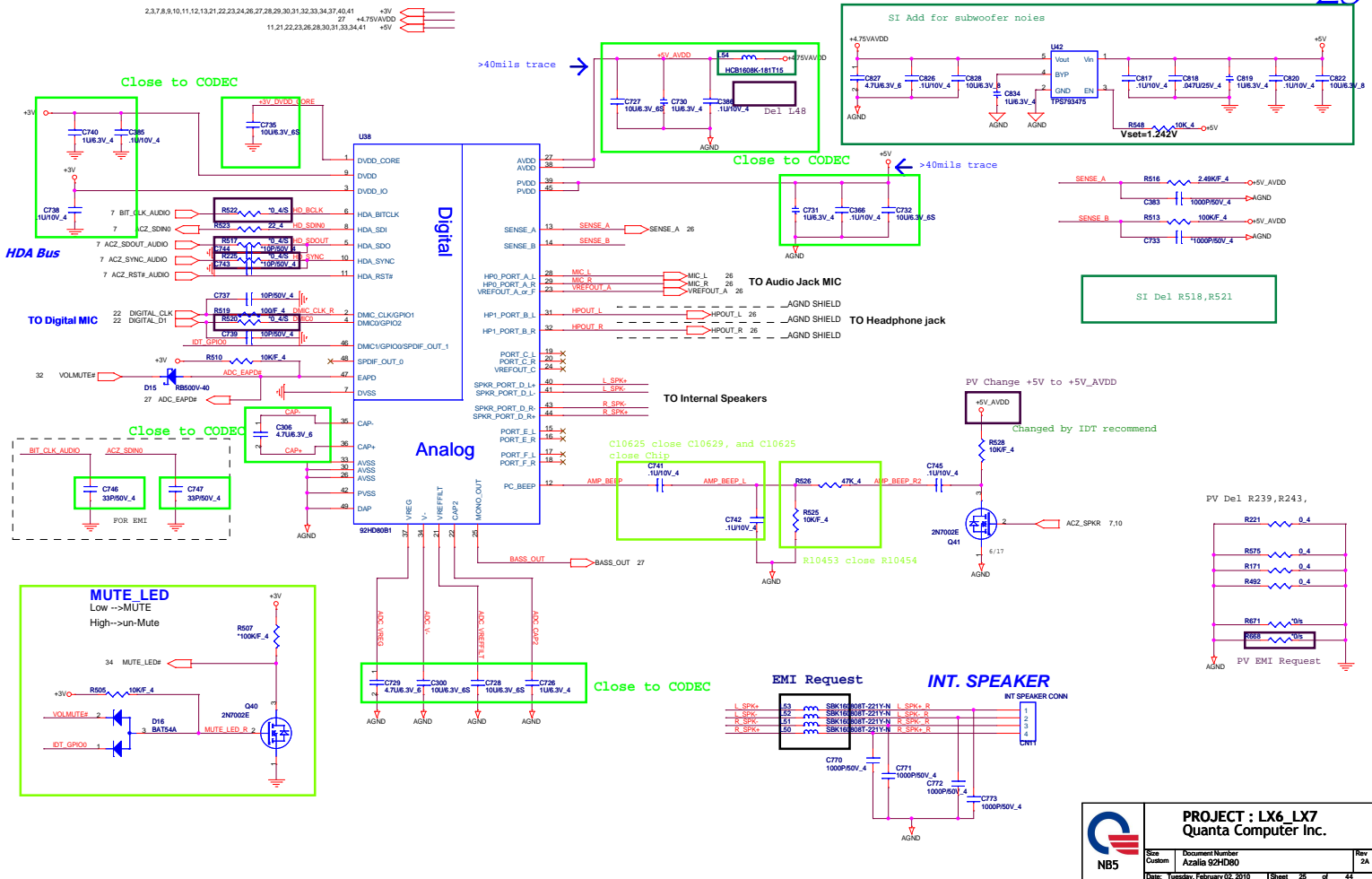


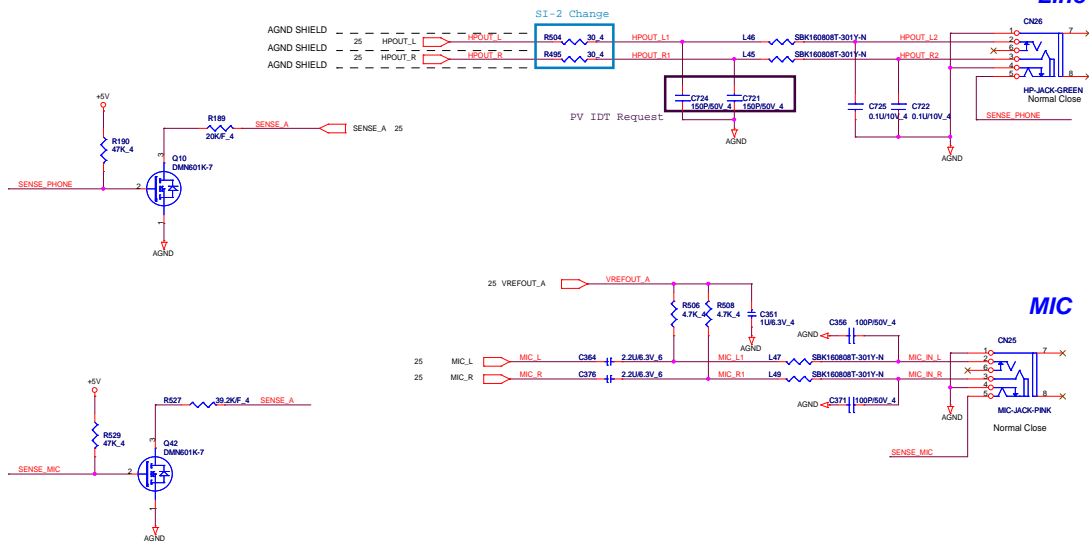






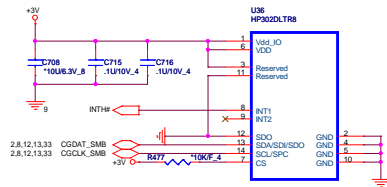
2,3,7,8,9,10,11,12,13,21,22,23,24,26,27,28,29,30,31,32,33,34,37,40,41 +3V  
27 +4.75VAVDD  
11,21,22,23,26,28,30,31,33,34,41 +5V






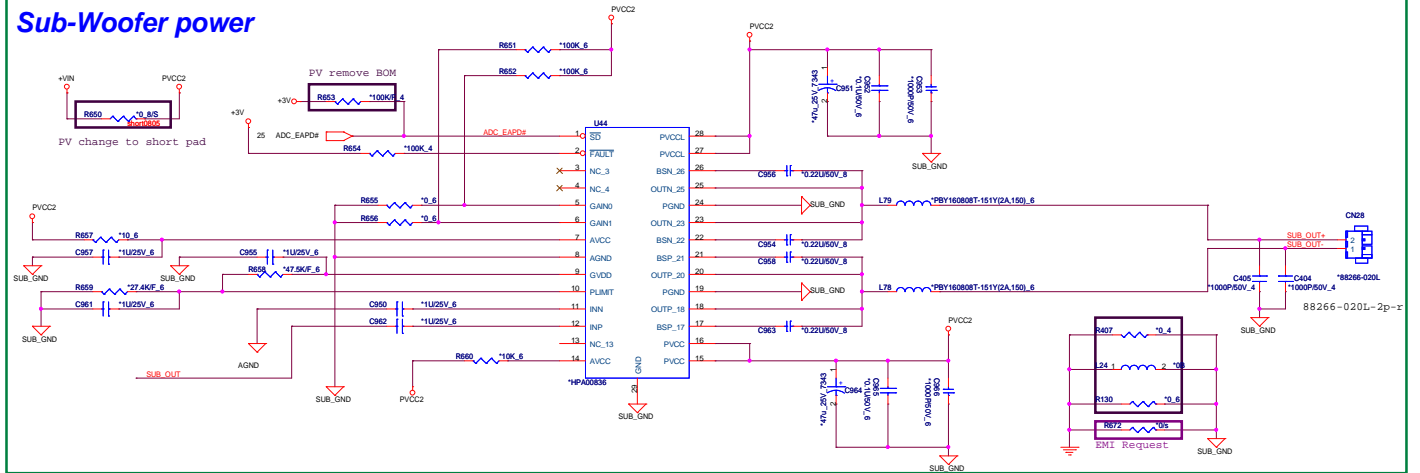
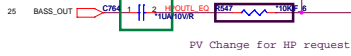
## Accelerometer Sensor

```
SGT-LIS302DLTR interrupt pin default
is low / active Hi , BIOS need to
programming 22h to change status
from active Hi to low
```

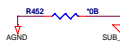


Pin 12: Low	38hex
Pin 12: unconnected/floating	3Ahex

 NB5	<b>PROJECT : LX6_LX7</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>Audio Jack/Accelerometer</b>	Rev 1A
Date: Tuesday, February 02, 2010   Sheet 26 of 44			



PV Del R574,R241,R240



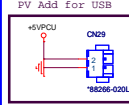
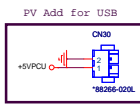
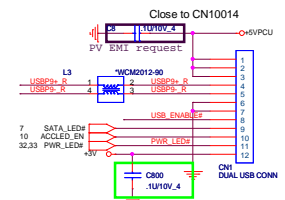
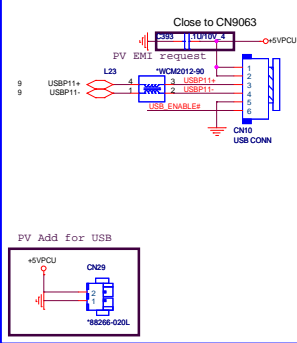
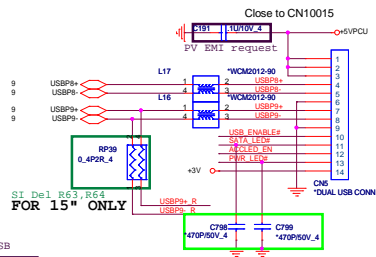
+3V	2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,28,29,30,31,32,33,34,37,40,41
+4.75VA	25
+VIN	22,35,36,37,39,40,41,42,43



Size Custom	Document Number <b>SUBWOOFER (EQ &amp; AMP.)</b>	Rev 1A
Date: Tuesday, February 02, 2010	Sheet 27 of 44	

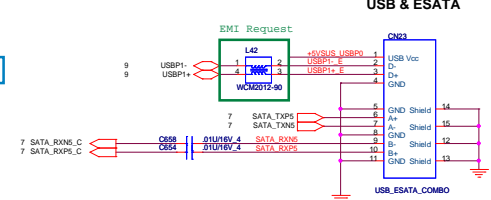
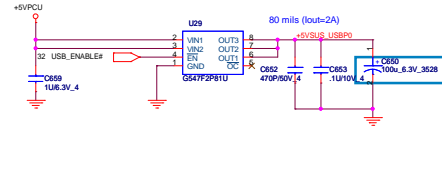
**RIGHT SIDE USBX2 for 17"**

## 28

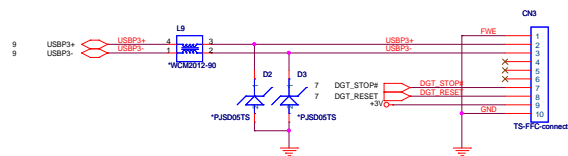
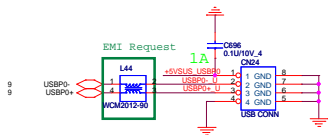


## E-SATA

- 



***Touch screen for 15"***



**PROJECT : LX6\_LX7**  
**Quanta Computer Inc.**

Size Custom	Document Number <b>BT/WC/FT/Touchscreen</b>	Rev 1A
Date: Tuesday, February 02, 2010	Sheet 28 of 44	

T : Stuffed for RTL8111DL(10/100/1000)

for RTL8111DL use close Pin 44,45

+CTRL12DVDD

+CTRL12DVDD

3V\_LAN

C703

C702

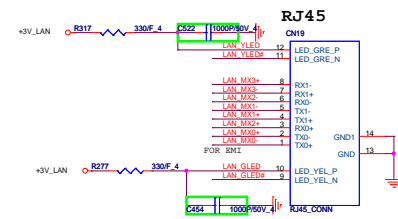
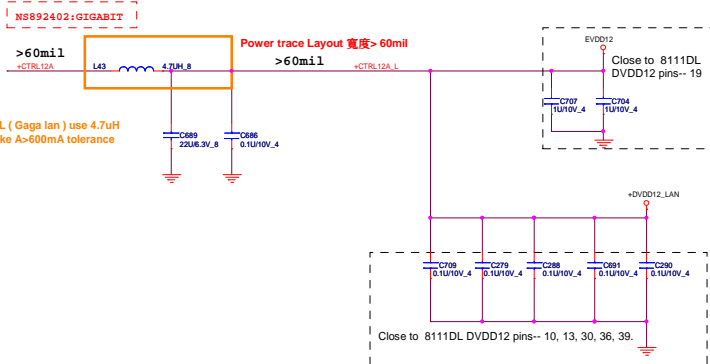
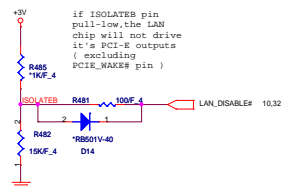
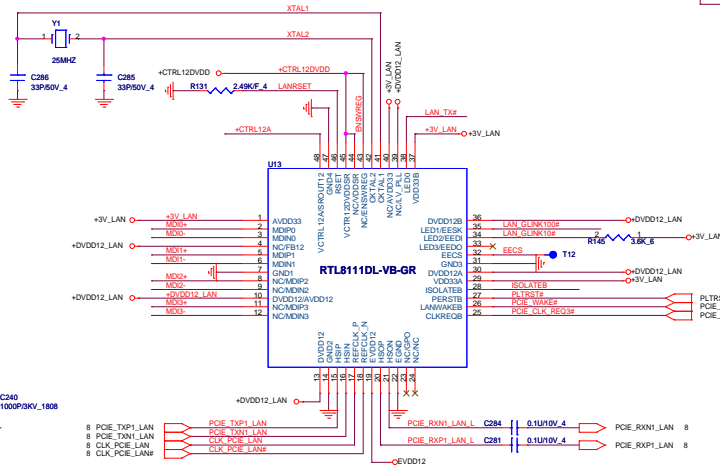
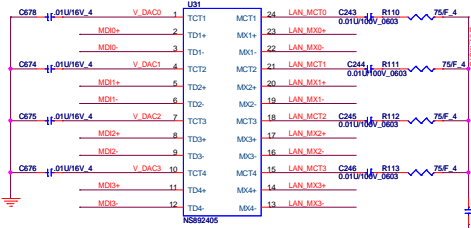
SI del R452


Remove R3571,R3573  
R3571 and R3573 are used in  
RTL8111DL , remove R3573 if  
switching regulator is enable  
, Remove R3571 external power  
is used.

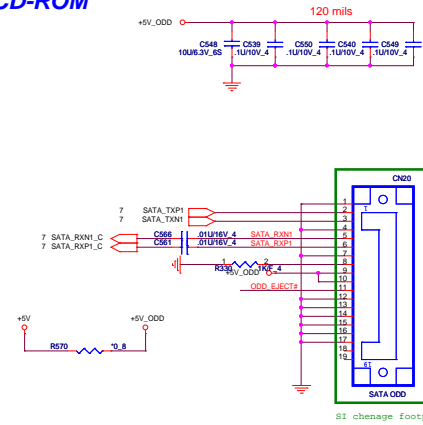
SI del R13

Close to PIN 1

AL08111DB00 RTL8111DL-GR



 NB5	<b>PROJECT : LX6_LX7</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>8103E/RJ45</b>	Rev 1A
Date: Tuesday, February 02, 2010		1 Sheet 29 of 44	



### SI Add

The diagram shows a circuit for a 'SI Add' function. It includes a 'PV modify' section with a 5V supply, a 10K resistor (R27), and a 4-pin connector (EJECT#). The main power supply section features a +12V (VALW) input, a 330K resistor (R78), an AO3404 ID current source (5.8A), and three AO3404 MOSFETs (Q43, Q44, Q45). A +5V (VALV) input is connected to a 10V (VALV\_4) supply and a 22.8K resistor (R79). The circuit is controlled by an ODD\_PD signal (pin 32) and an EJECT signal (pin 32).

PV modify

5V

R27  
10K $\Omega$ \_4

EJECT# 32

0.4 R18

High : ODD power down  
Low : ODD power on

32 ODD\_PD

+12V (VALW)

R78  
330K\_5

AO3404 ID  
current  
5.8A

Q43  
AO3404

+5V (VALV)

C803  
.1u10V\_4

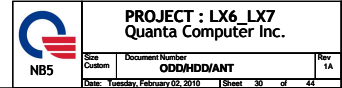
+5V ODD

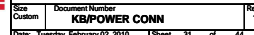
R79  
22.8

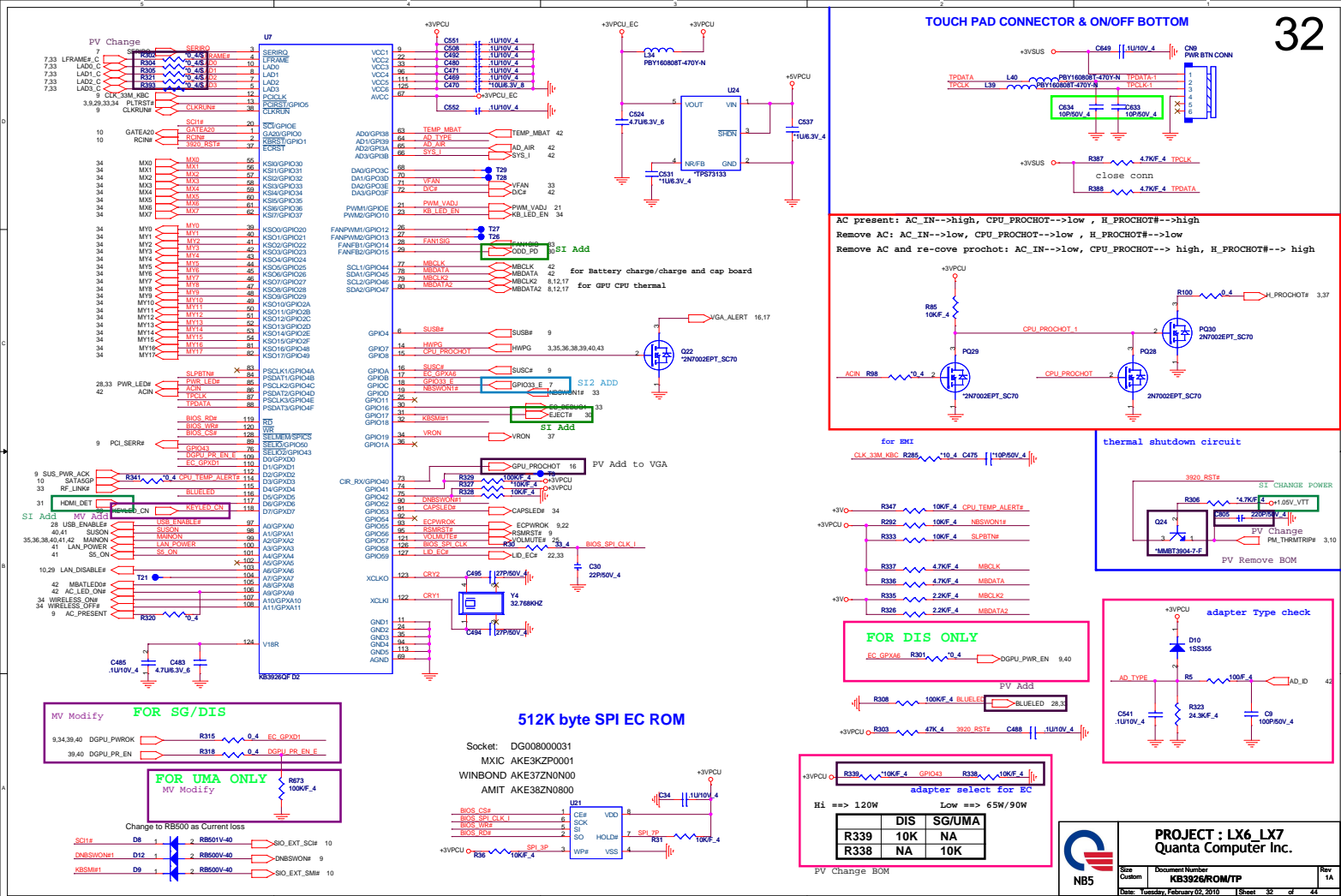
Q44  
2N7002E

Q45  
2N7002E

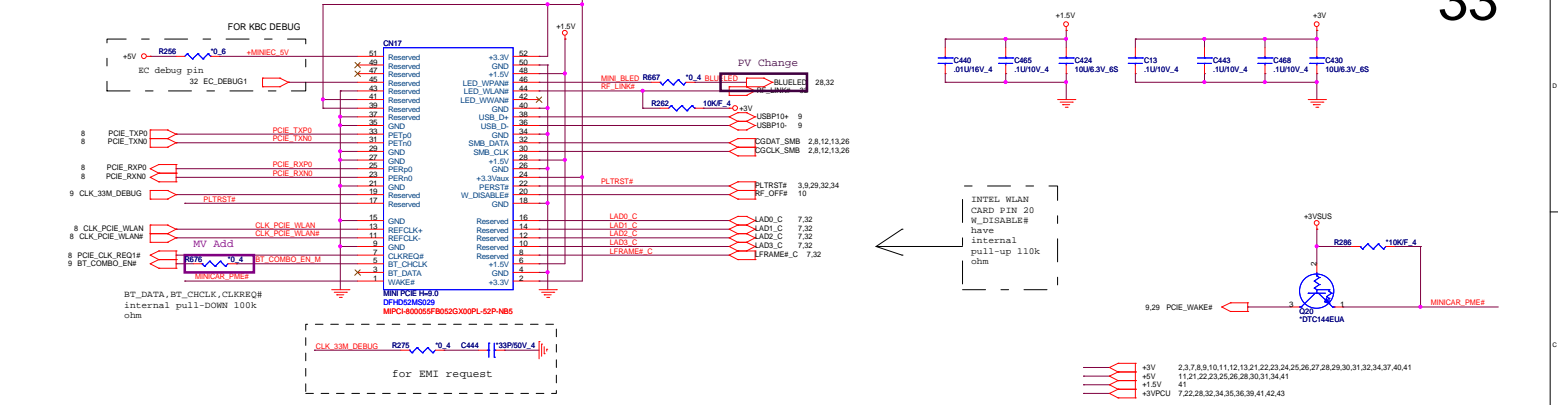
C804  
.001u25V\_6



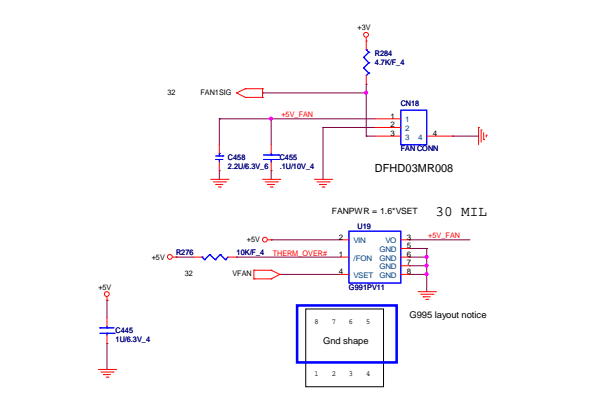




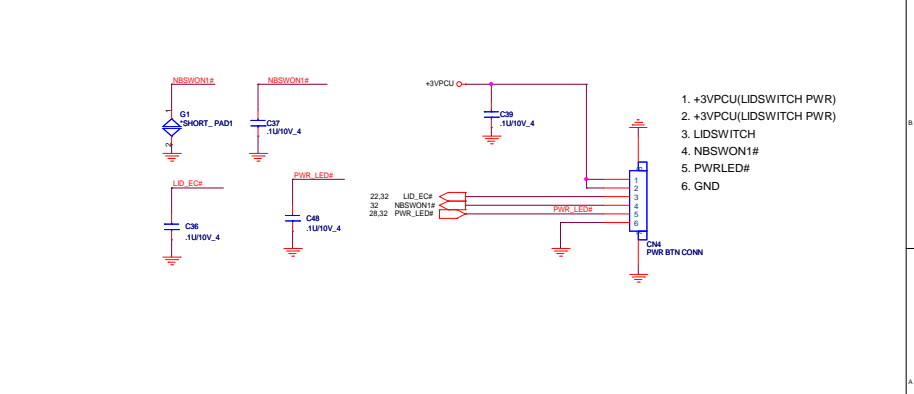




CPU FAN



POWER BUTTON CONNECT



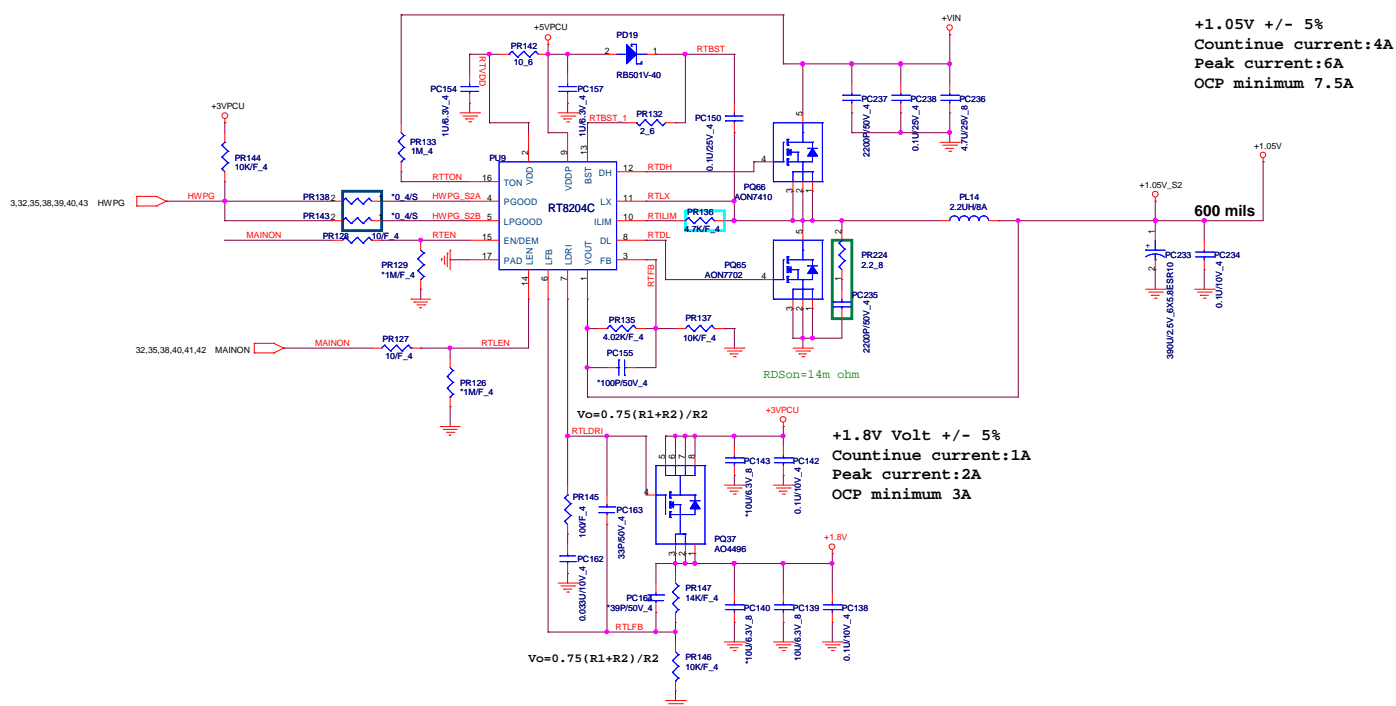
PROJECT : LX6\_LX7  
Quanta Computer Inc.

Rev	Document Number	Rev
1A	MINI PCI-E CONN/FAN	1A

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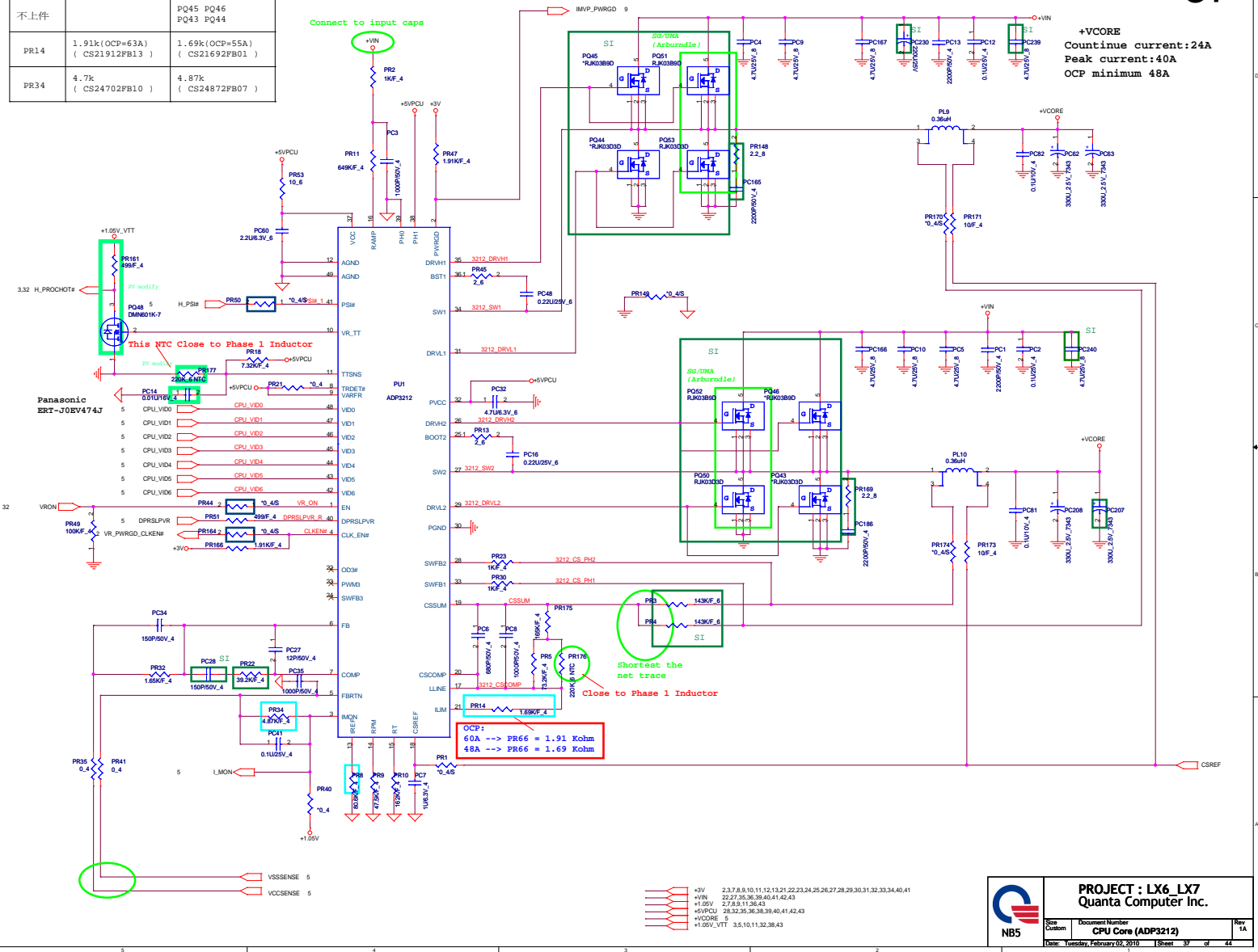


+1.8V	5,10,11,21,41
+VIN	22,27,35,37,39,40,41,42,43
+1.05V	2,7,8,9,11,37,43
+3VPCU	7,22,28,32,33,34,35,39,41,42,43
+5VPCU	28,32,35,37,38,39,40,41,42,43



**PROJECT : LX6\_LX7**  
**Quanta Computer Inc.**

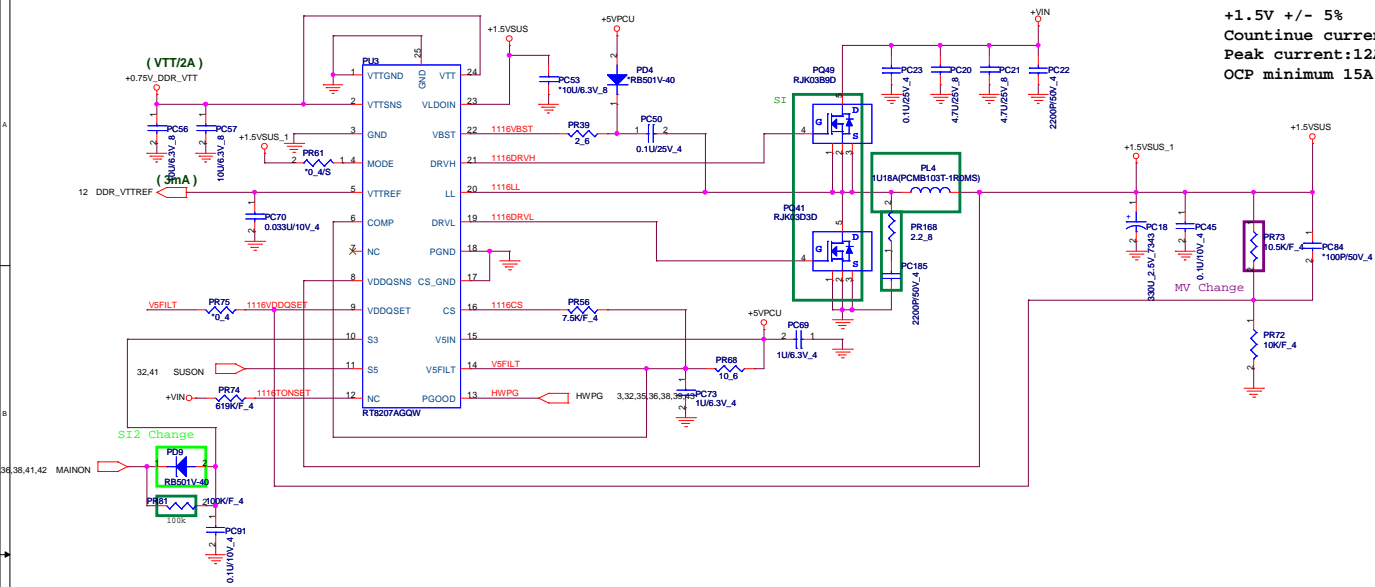
Size Custom	Document Number <b>+1.05V/+1.8V (RT8204C)</b>	Rev 1A
Date: Tuesday, February 02, 2010	Sheet 36 of 44	





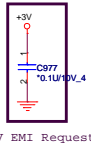
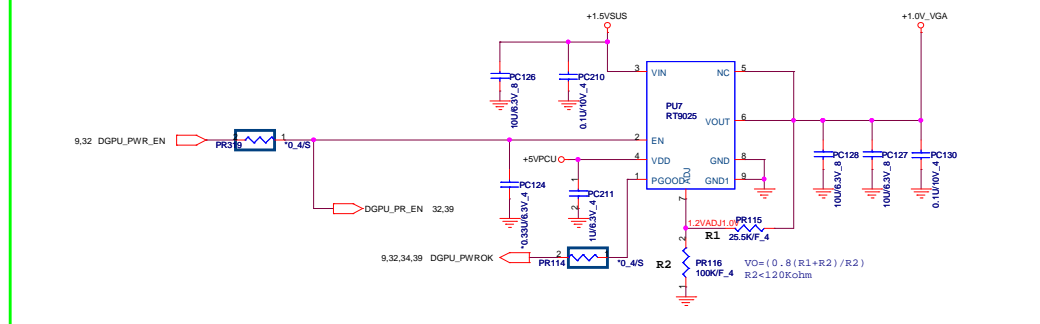


+1.5V +/- 5%  
 Countinue current:6A  
 Peak current:12A  
 OCP minimum 15A

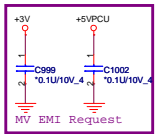


### SG & Discrete Only

+1.0V +/- 5%  
 Countinue current:1.7A  
 Peak current:3A



PV EMI Request



MV EMI Request

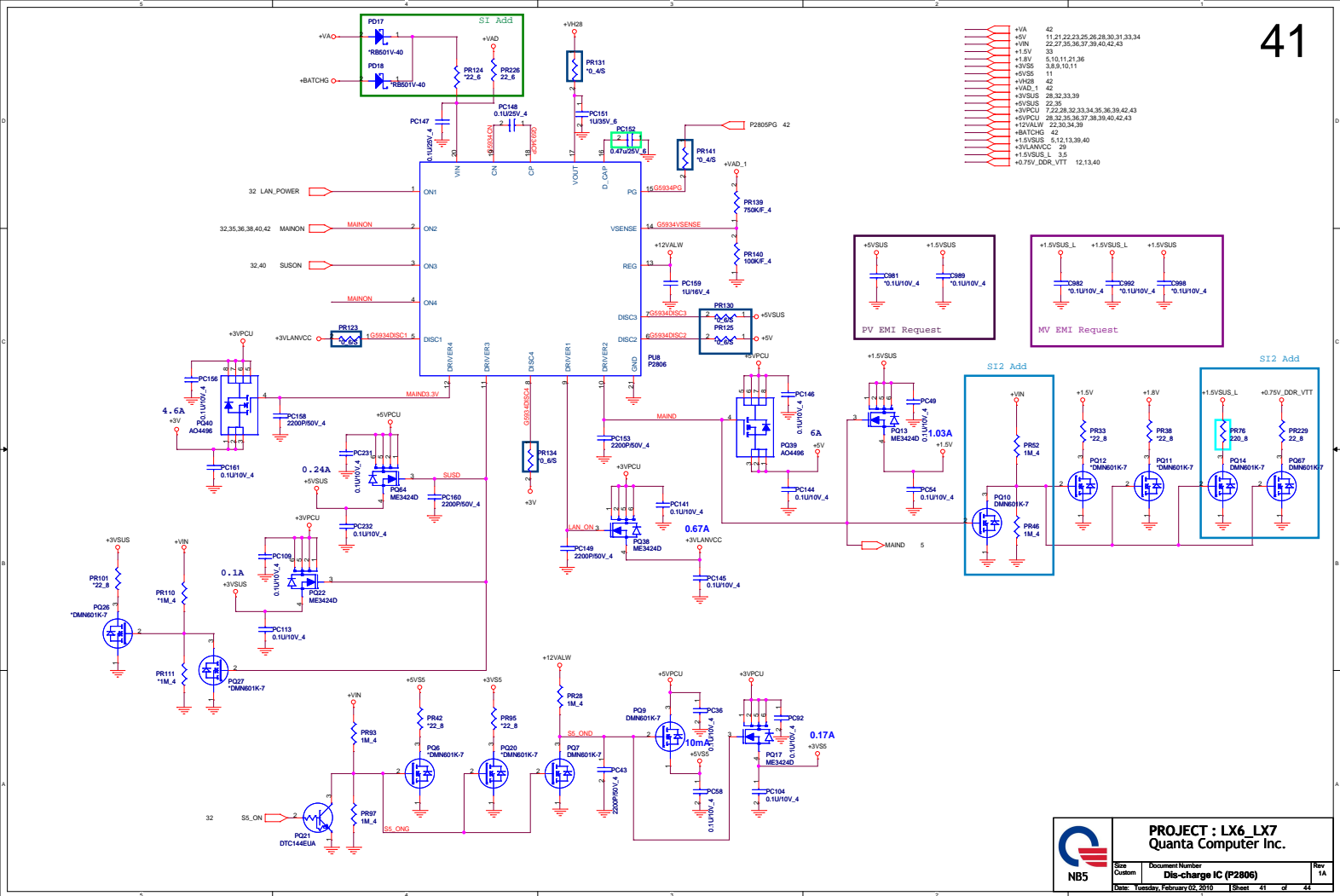
+3V	2,3,7,8,9,10,11,12,13,21,22,23,24,25,26,27,28,29,30,31,32,33,34,37,41
+VIN	22,27,35,36,37,39,41,42,43
+5VPCU	28,32,35,36,37,38,39,41,42,43
+1.5VSUS	5,12,13,39,41
+1.0V_VGA	14,16,18,34
+0.75V_DDR_VTT	12,13,41



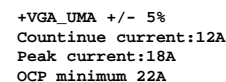
PROJECT : LX6\_LX7  
 Quanta Computer Inc.


Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A
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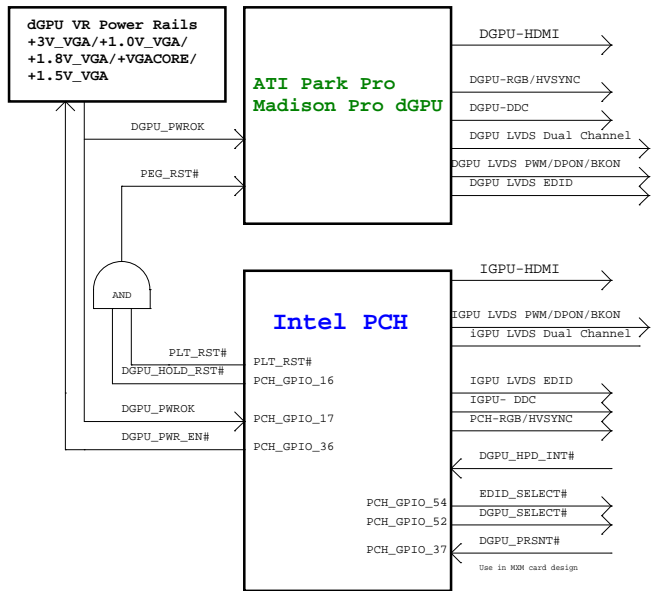




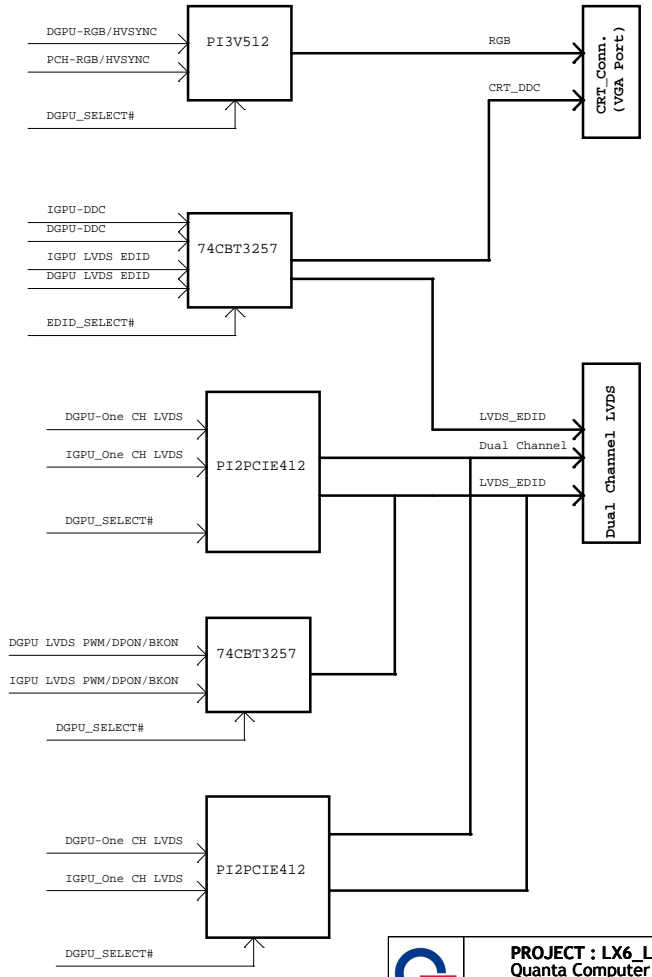





 NB5	<b>PROJECT : LX6_LX7</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number <b>UMA GPU CORE (RT8152C)</b>	Rev 1A
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Switchable GPIOs	Descriptions
PCH_GPIO52	DGPU_SELECT#
PCH_GPIO16	DGPU_HOLD_RST#
PCH_GPIO36	DGPU_PWR_EN#
PCH_GPIO17	DGPU_PWR_OK
PCH_GPIO54	EDID_ELECT#
PCH_GPIO37	DGPU_PRNT#





**PROJECT : LX6 LX7**  
Quanta Computer Inc.

Size Custom	Document Number <b>Switch Blockdiagram</b>	Rev 1A
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