

MODEL NAME : ZAVA1/ZAVC1  
PCB NO : DA80011D000 LA-B015P-R1.0

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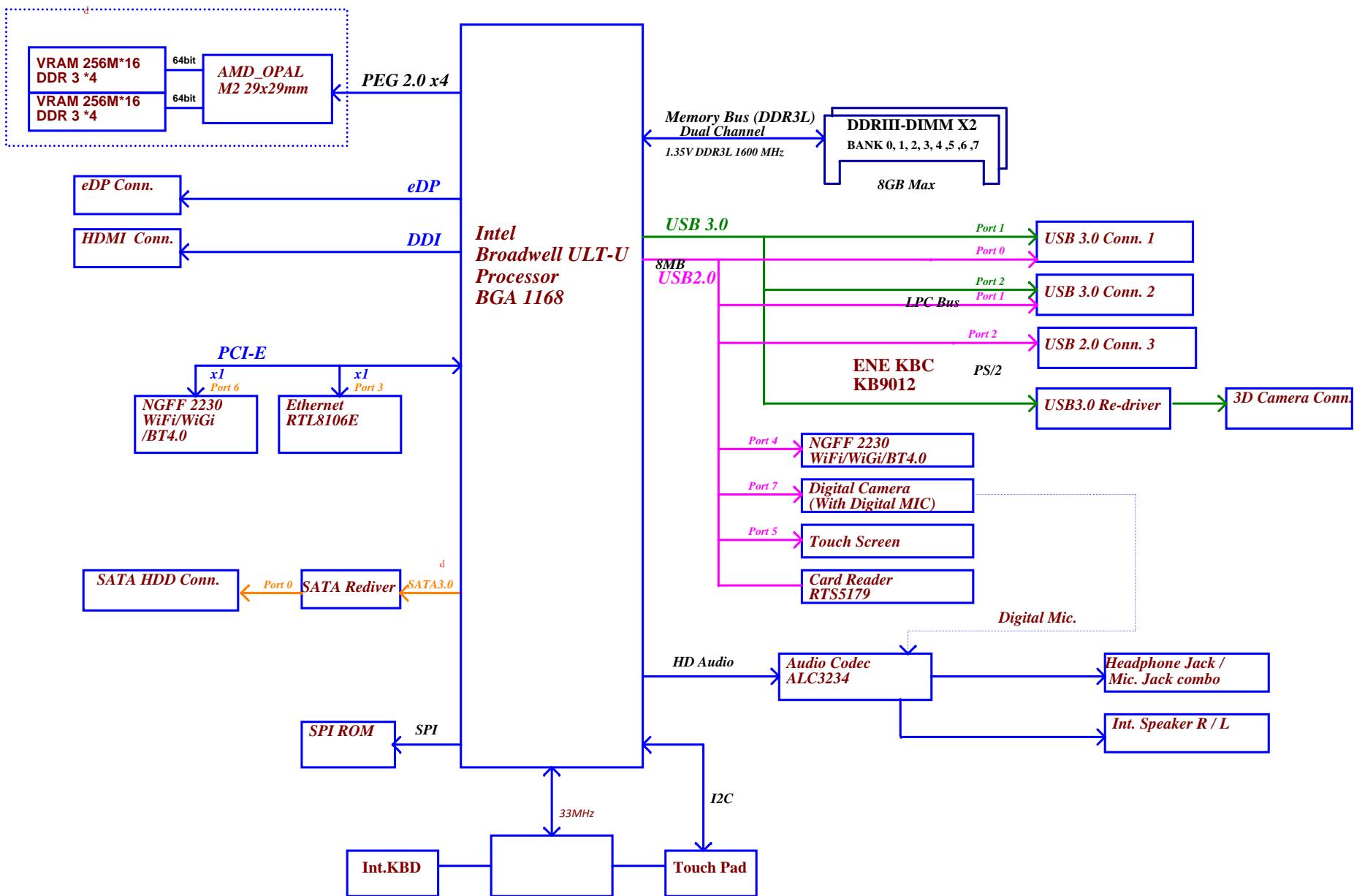
## Schematic Document

Intel BoardWell ULT  
ZAVA1/ZAVC1  
DIS AMD 25W/M2+DDR3x8

2014-10-17

Rev: 1.0

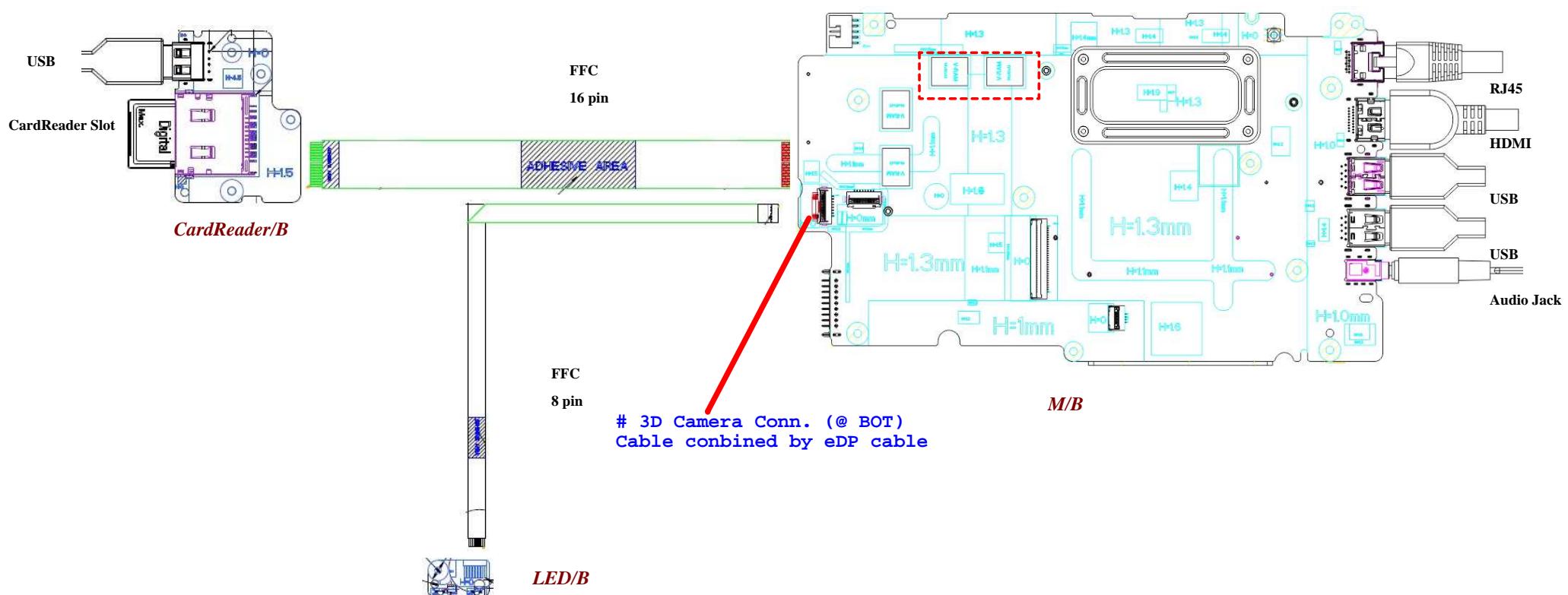
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Block Diagram	Document Number	Rev	Date	
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Board ID Table for AD channel									
Vcc	3.3V +/- 1%								
Ra	100K +/- 1%								
Board ID	Rb	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	EC	AD3			
0	0	0.000V	0.000V	0.300V	0x00	- 0x0B			
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C	- 0x1C			
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D	- 0x26			
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27	- 0x30			
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31	- 0x3B			
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C	- 0x46			
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47	- 0x54			
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55	- 0x64			
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65	- 0x76			
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77	- 0x87			
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88	- 0x96			
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97	- 0xA3			
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4	- 0xAD			
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE	- 0xB7			
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8	- 0xC0			
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1	- 0xC9			
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA	- 0xD3			
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4	- 0xDC			
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD	- 0xE6			
19	NC	3.000V	3.300V	3.300V	0xE7	- 0xFF			

SMBUS Control Table									
	SOURCE	BATT	Charger	VGA	DIMM	XDP	Thermal Sensor	FFS	
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V						
EC_SMB_CK2 EC_SMB_DA2	KB9012			V			V		
SMBCLK SMBDATA	ULT			V				V	
SML0CLK SML0DATA	ULT								
SML1CLK SML1DATA	ULT								

Symbol Note :


: means Digital Ground  

: means Analog Ground

HSW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)	DIS(OPAL)
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

BDW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)	DIS(OPAL)
0	1.0_3D CAM			
1		1.0_3D CAM		
2			1.0_3D CAM	
3	SSI(BDW)			
4		SSI(BDW)		
5			SSI(BDW)	
6	PT(BDW) SSI_3D CAM			
7		PT(BDW) SSI_3D CAM		
8			PT(BDW) SSI_3D CAM	
9	ST(BDW) PT_3D CAM			
10		ST(BDW) PT_3D CAM		
11			ST(BDW) PT_3D CAM	
12	1.0(BDW) ST_3D CAM			
13		1.0(BDW) ST_3D CAM		
14			1.0(BDW) ST_3D CAM	
15				SSI
16				PT
17				ST
18				1.0

CLOCK SIGNAL ( Diff. 100MHz )

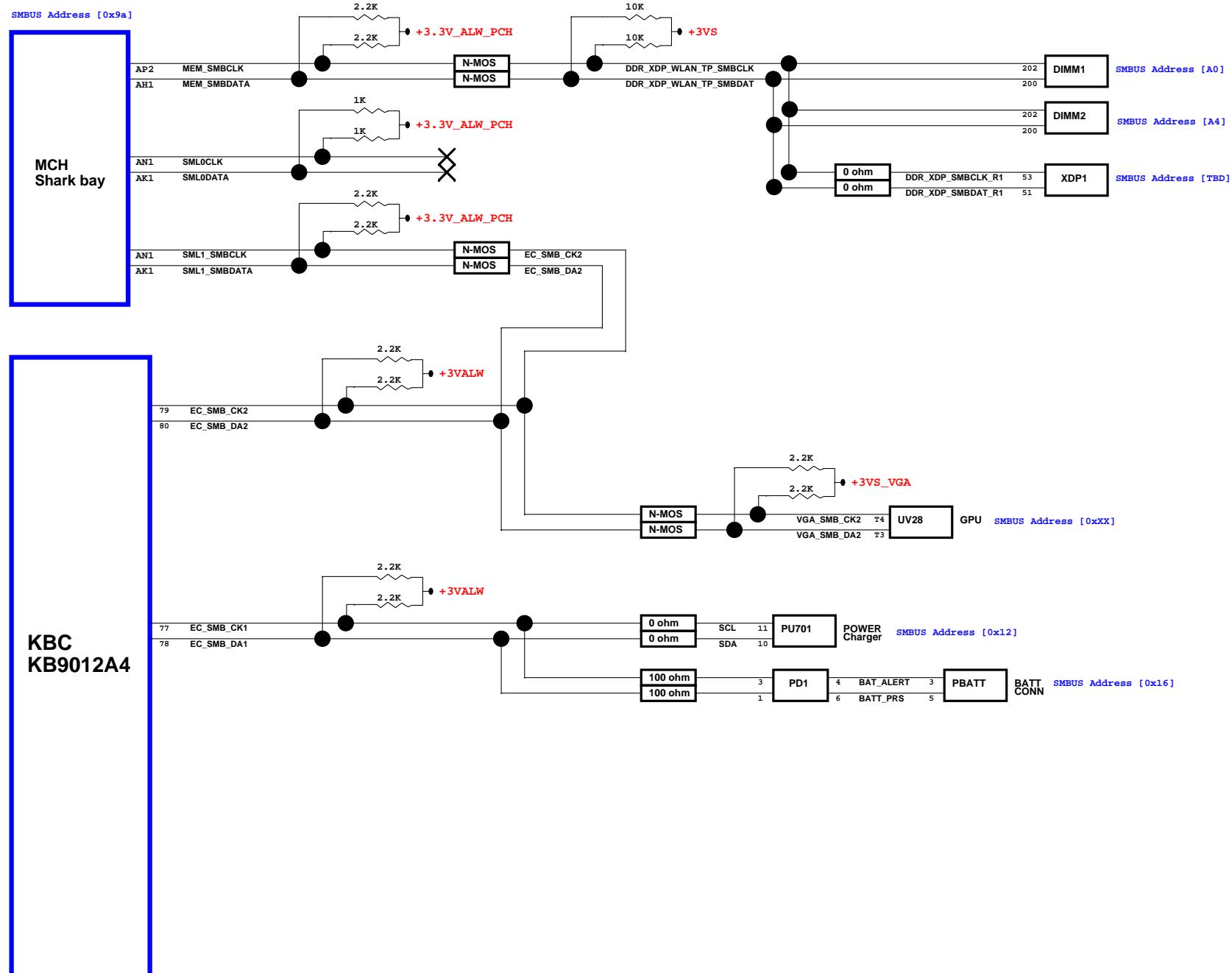
CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

USB3.0	
Port1	USB connector 1
Port2	USB connector 2
Port3	
Port4	3D Camera
USB2.0	
Port0	USB connector 1
Port1	USB connector 2
Port2	USB connector 3 (D/B)
Port3	
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera
PCI EXPRESS	
Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (AMD JET/TOBAZ)
Lane 6	
SATA	
SATA0	HDD
SATA1	
SATA2	
SATA3	

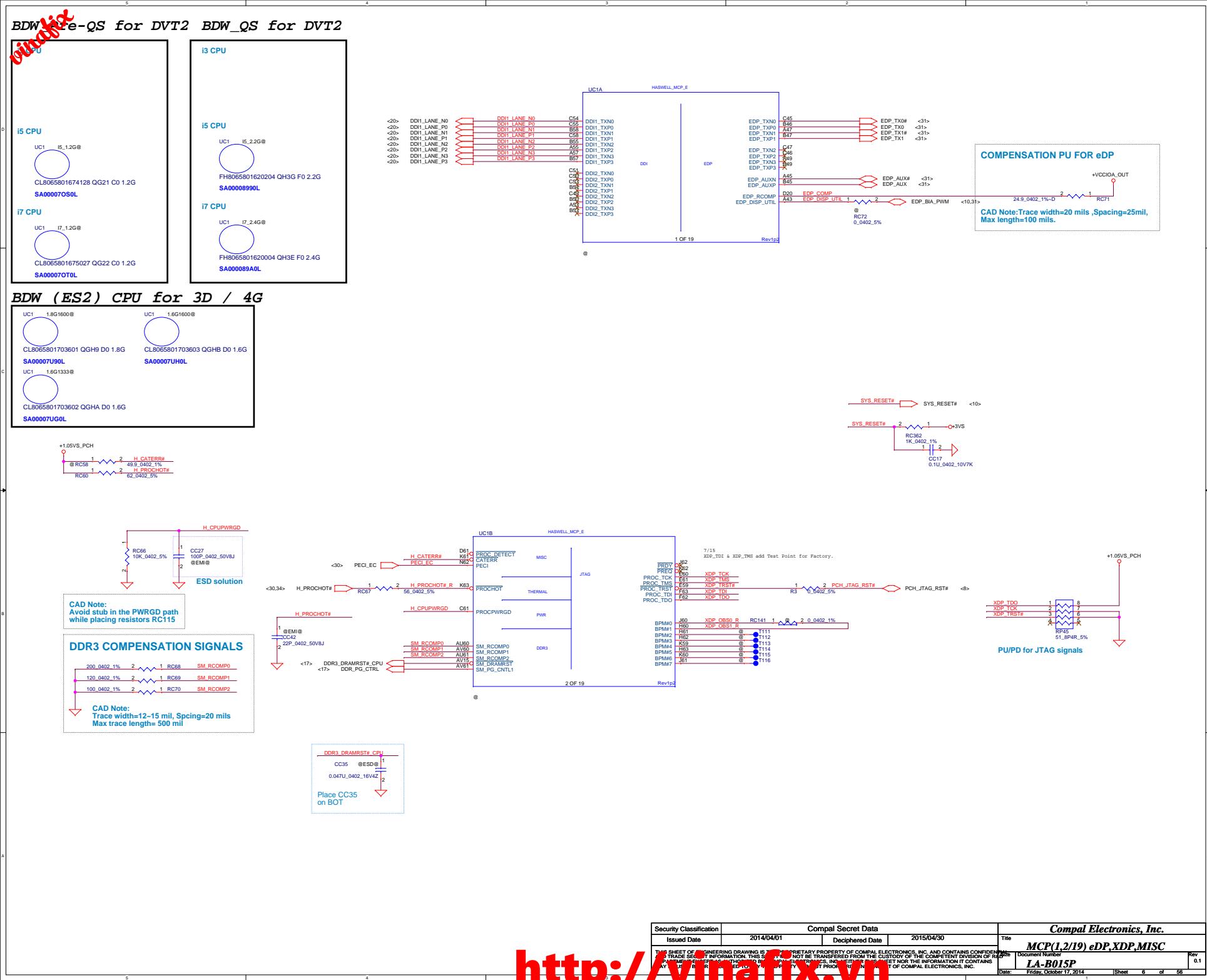
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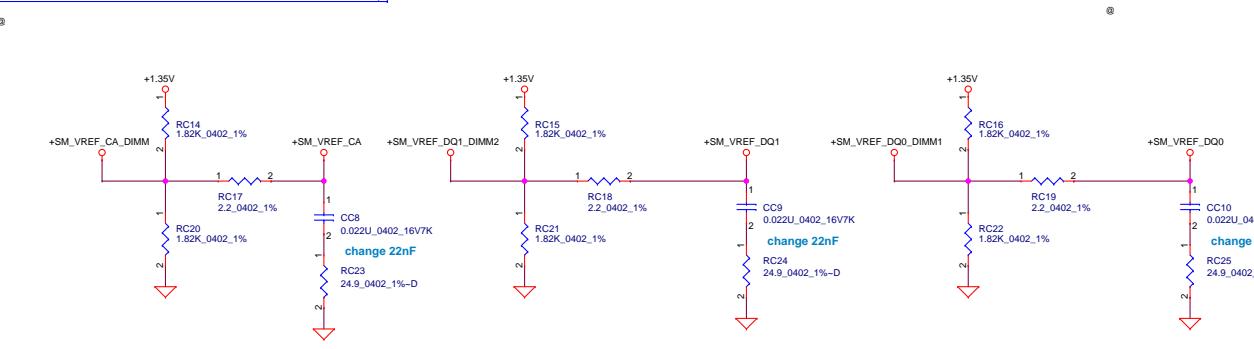
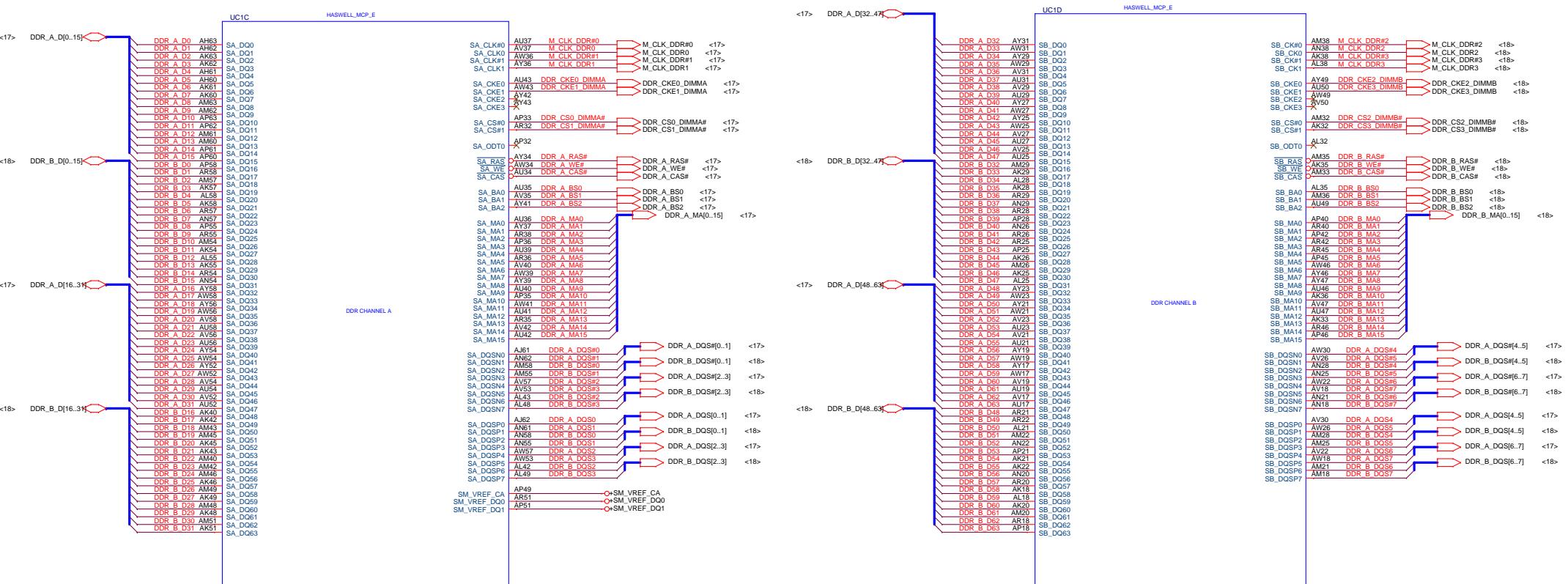


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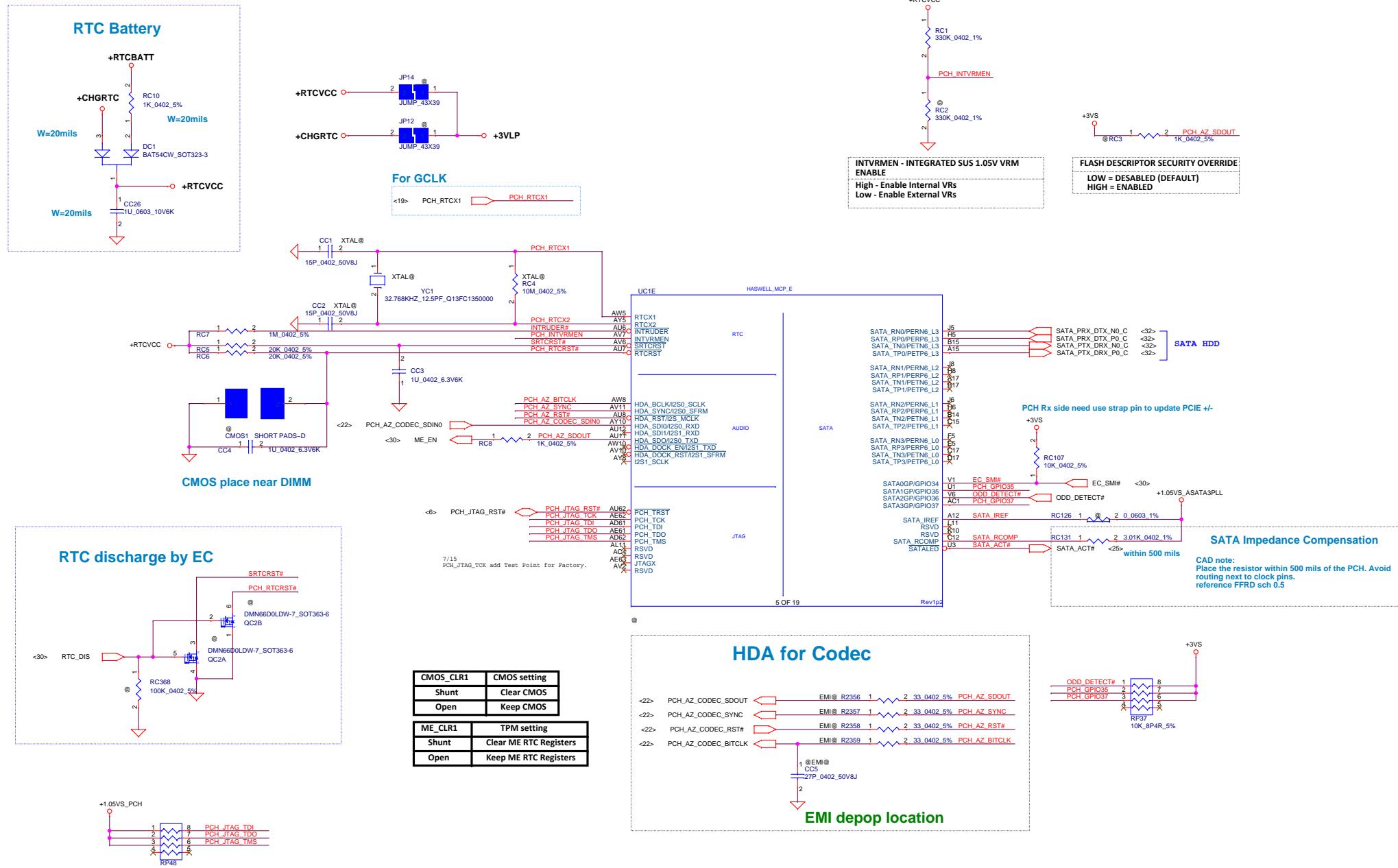
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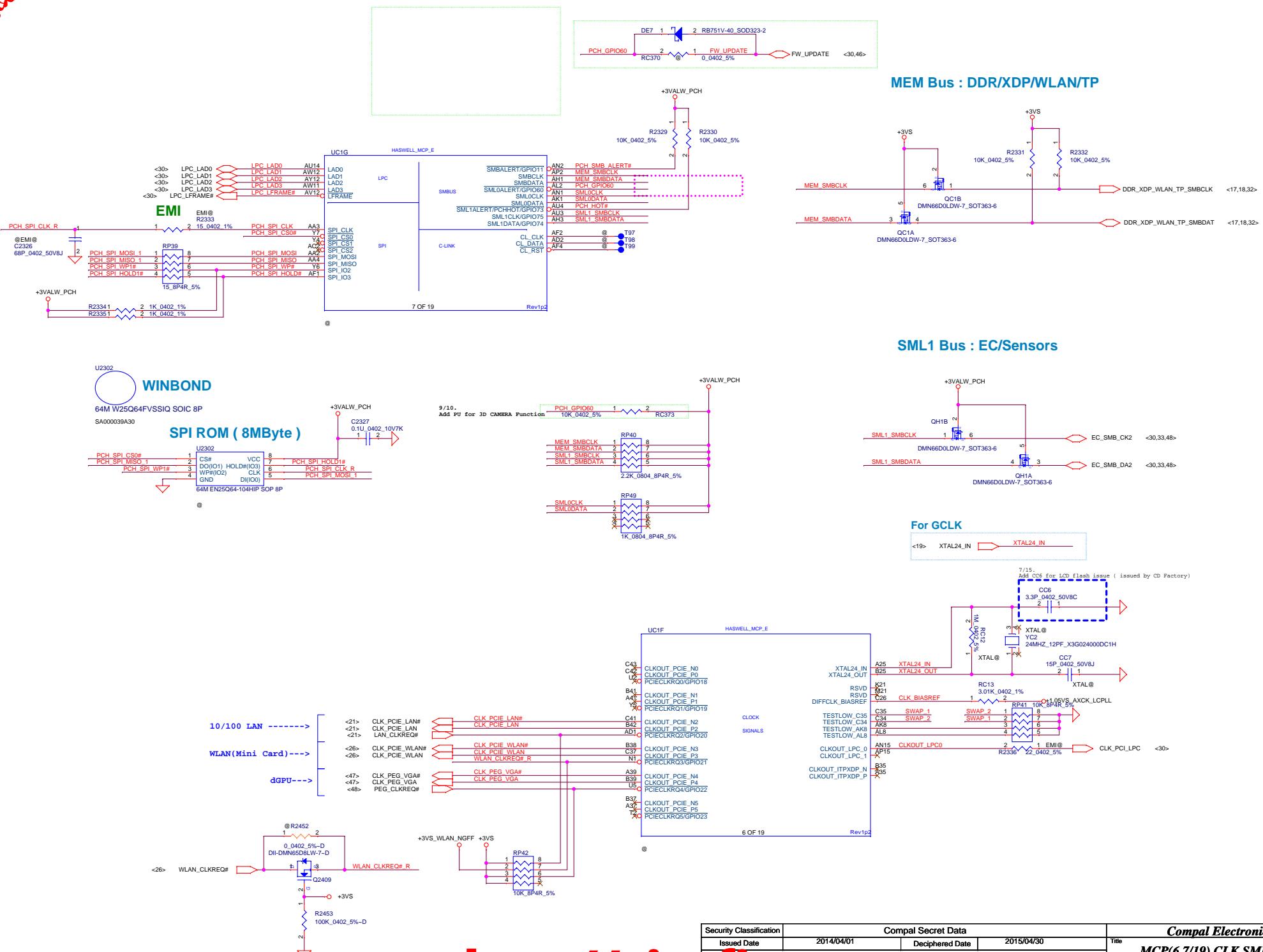
# Interleaved Memory



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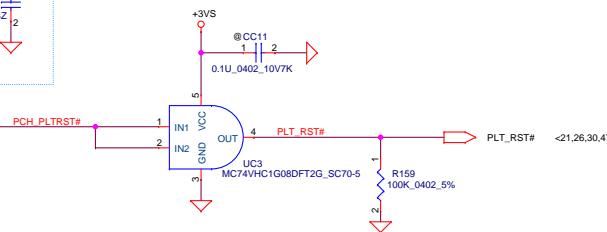
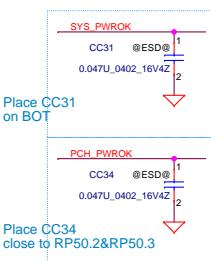
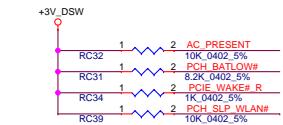
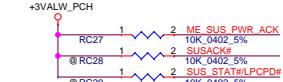
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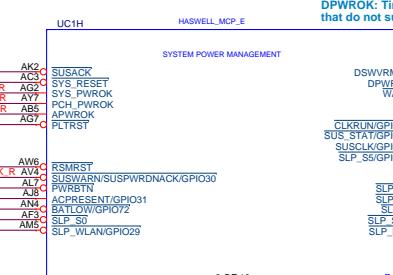


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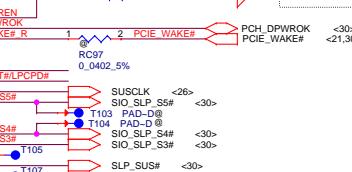


Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit CAN be NC, if not support Deep Sx



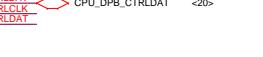
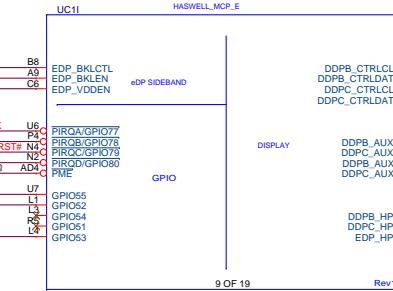
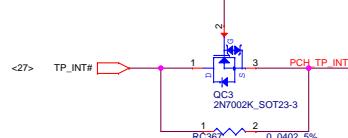
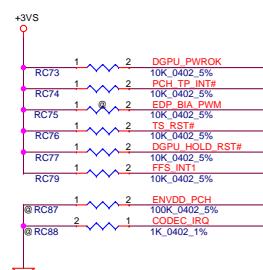
DSWODVREN - On Die DSW VR Enable  
★Enable(DEFAULT)  
Disable

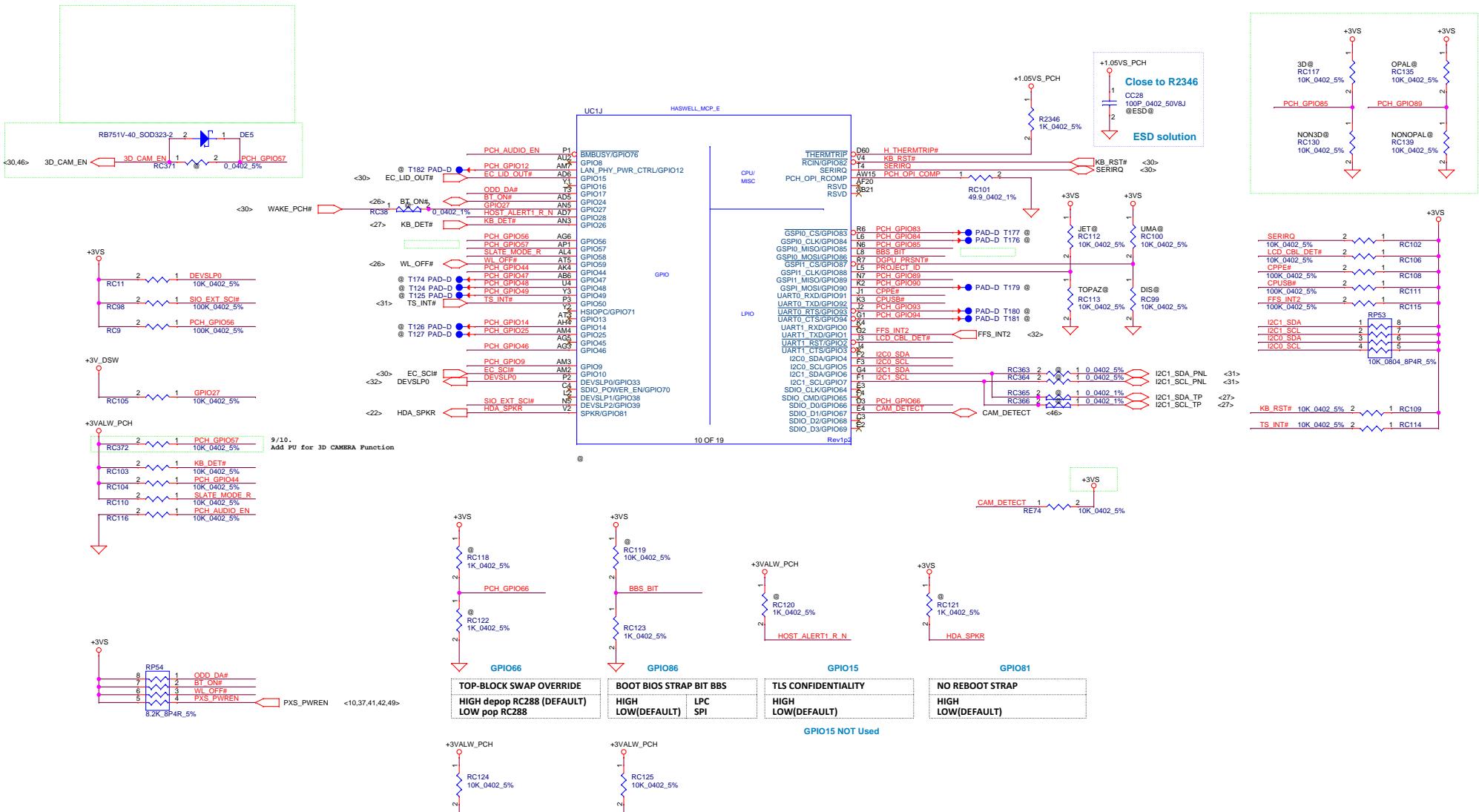
DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED



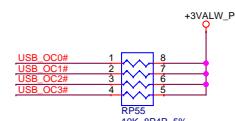
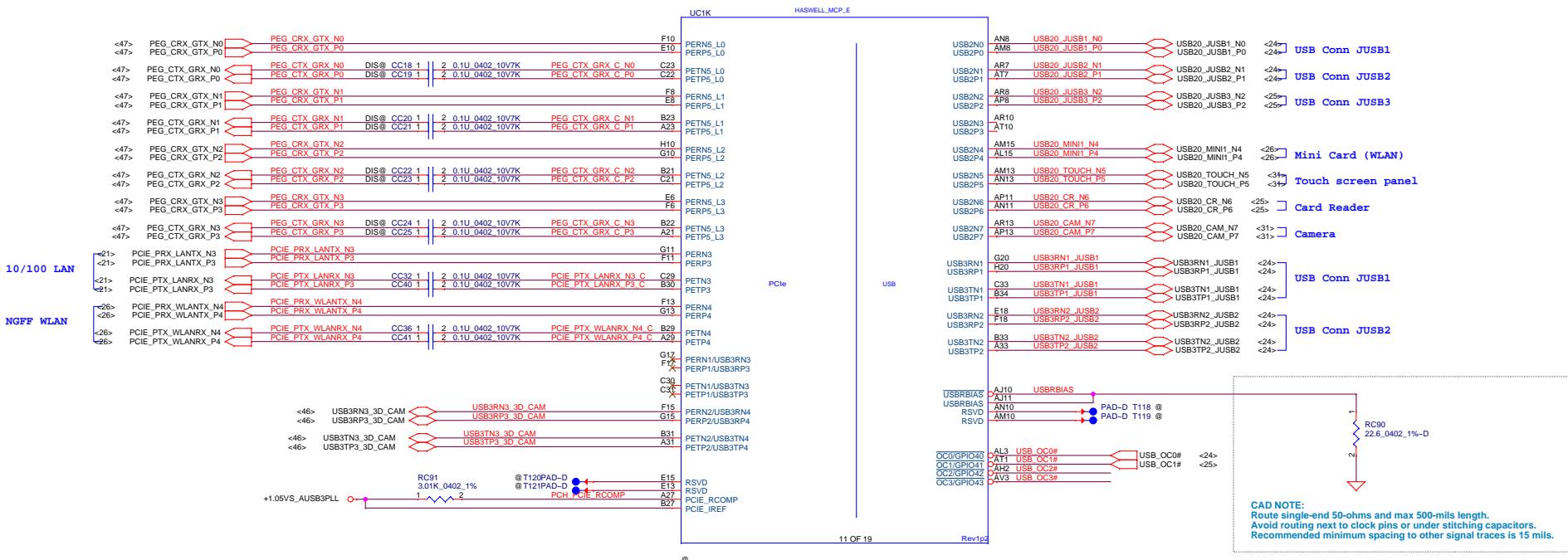
PCH\_BATLOW# Need pull high to VCCDSW3\_3  
(If no deep Sx, connect to VCCSUS3\_3)

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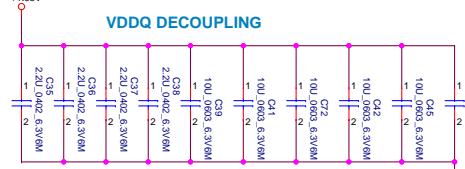
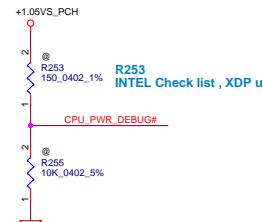
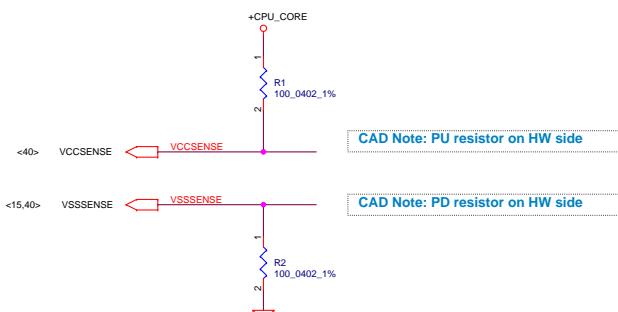
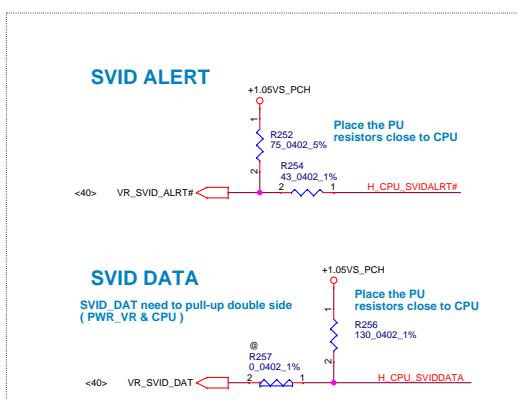
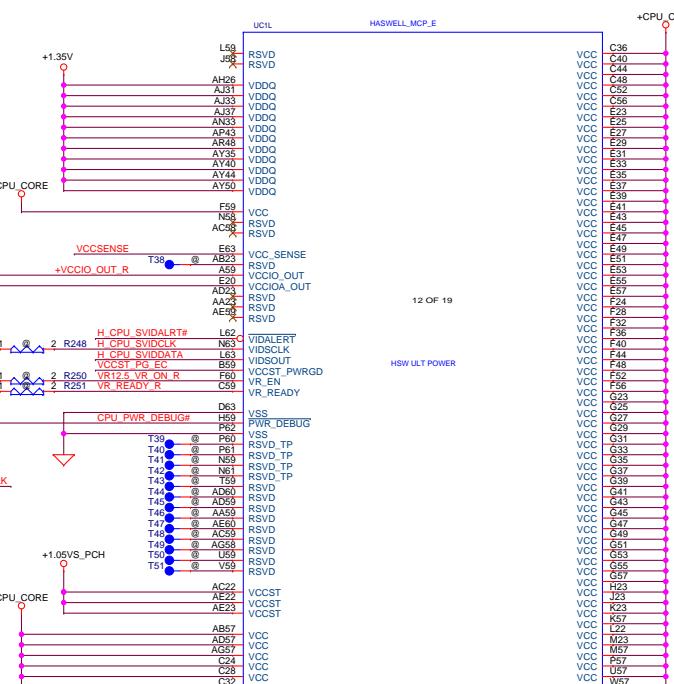
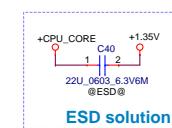
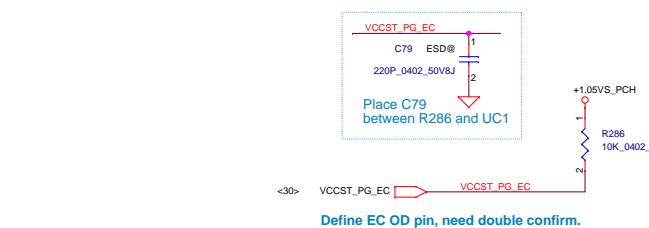
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**CAD NOTE:**  
Route single-end 50-ohms and max 500-mils length.  
Avoid routing next to clock pins or under stitching capacitors.  
Recommended minimum spacing to other signal traces is 15 mils.

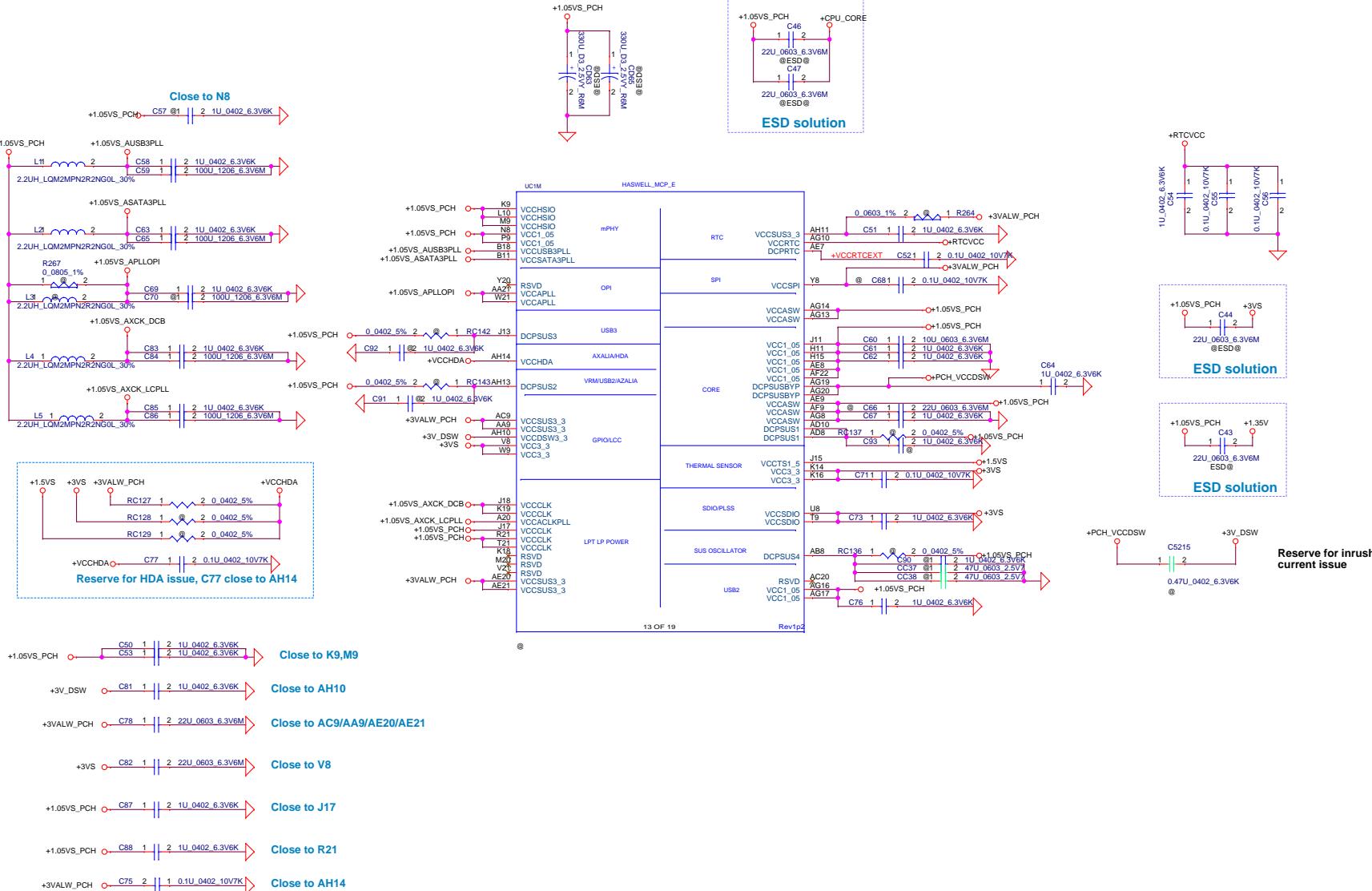
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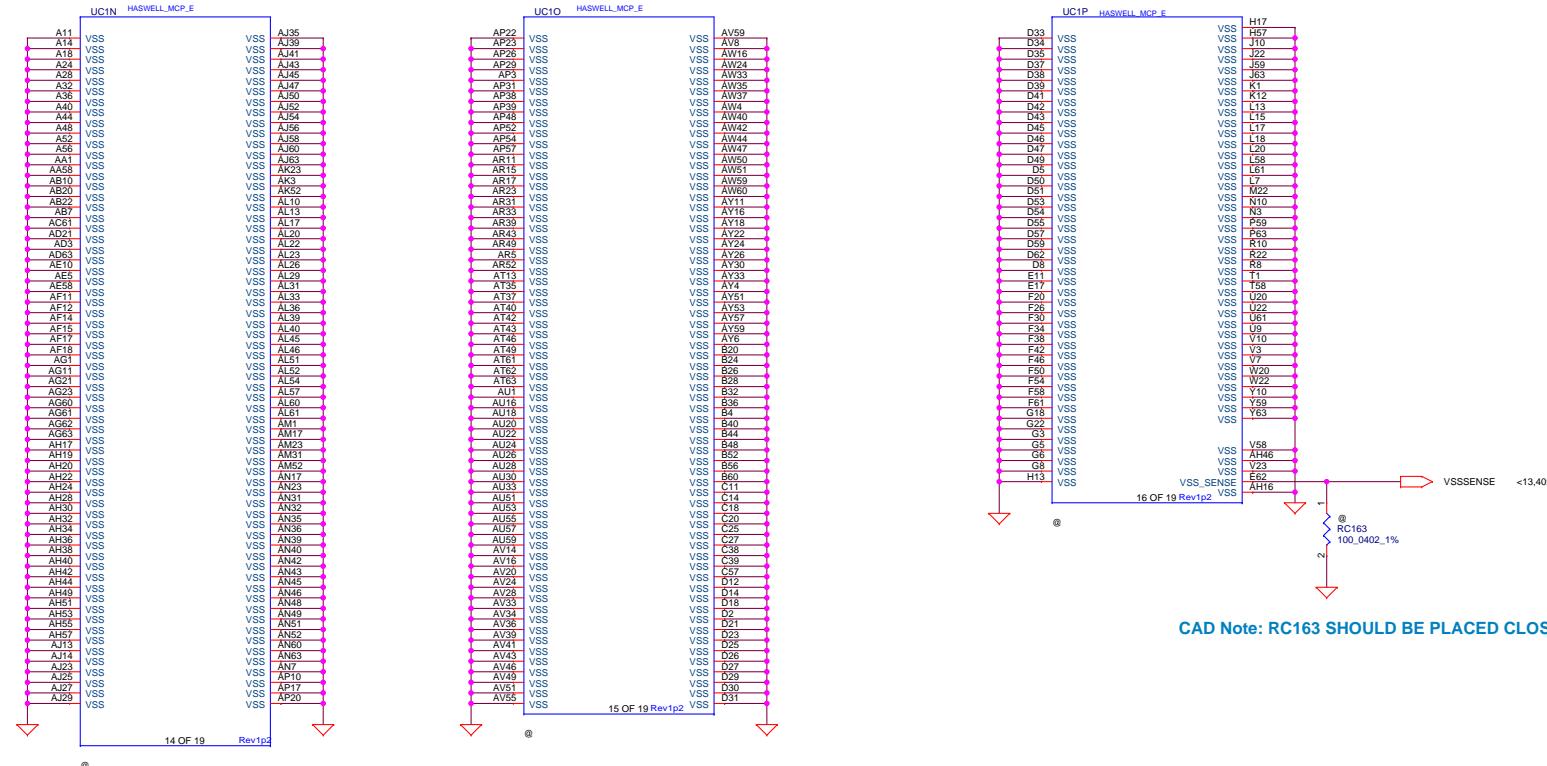
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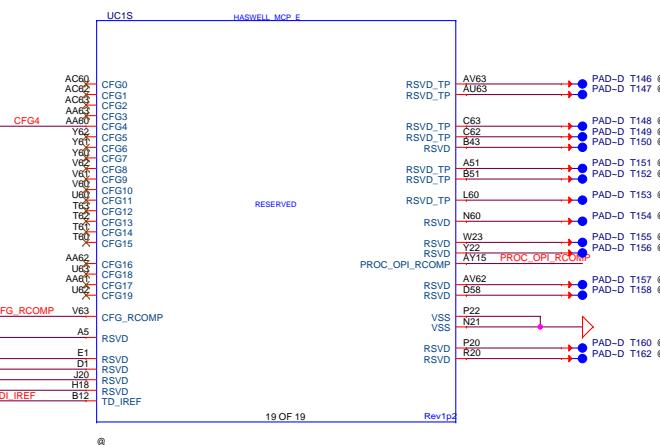
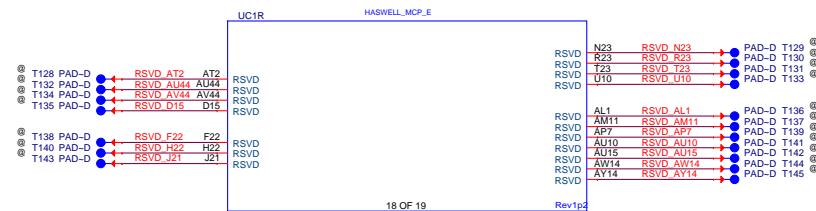
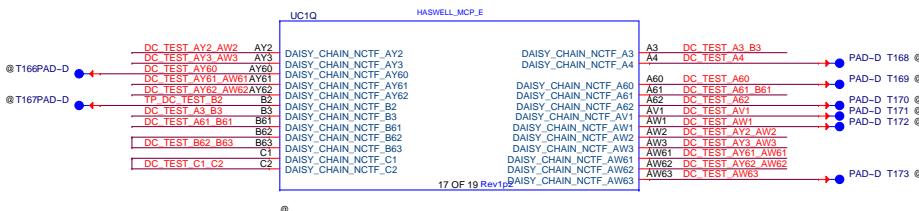
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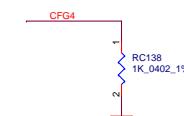


**CAD Note: RC163 SHOULD BE PLACED CLOSE TO CPU**

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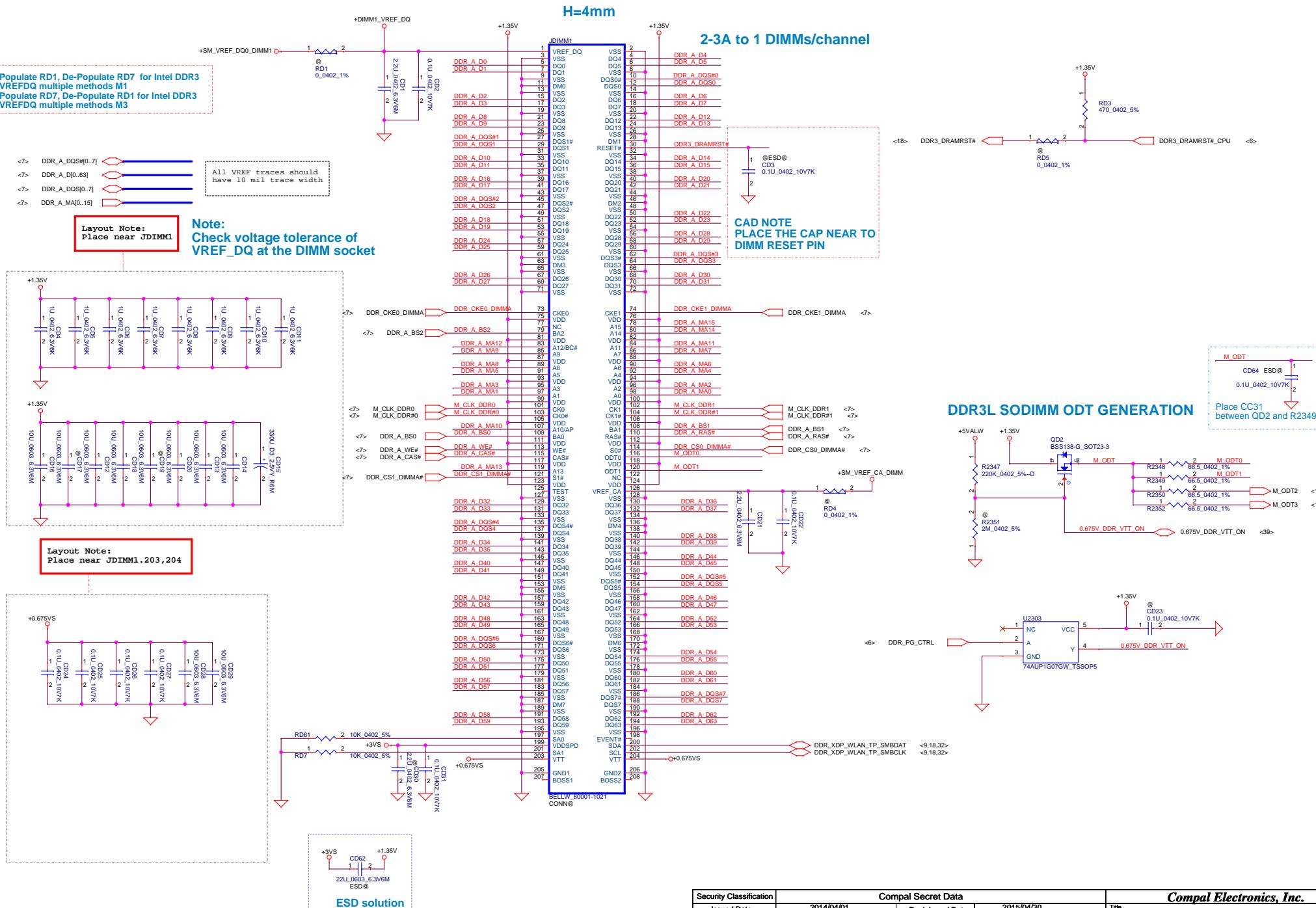


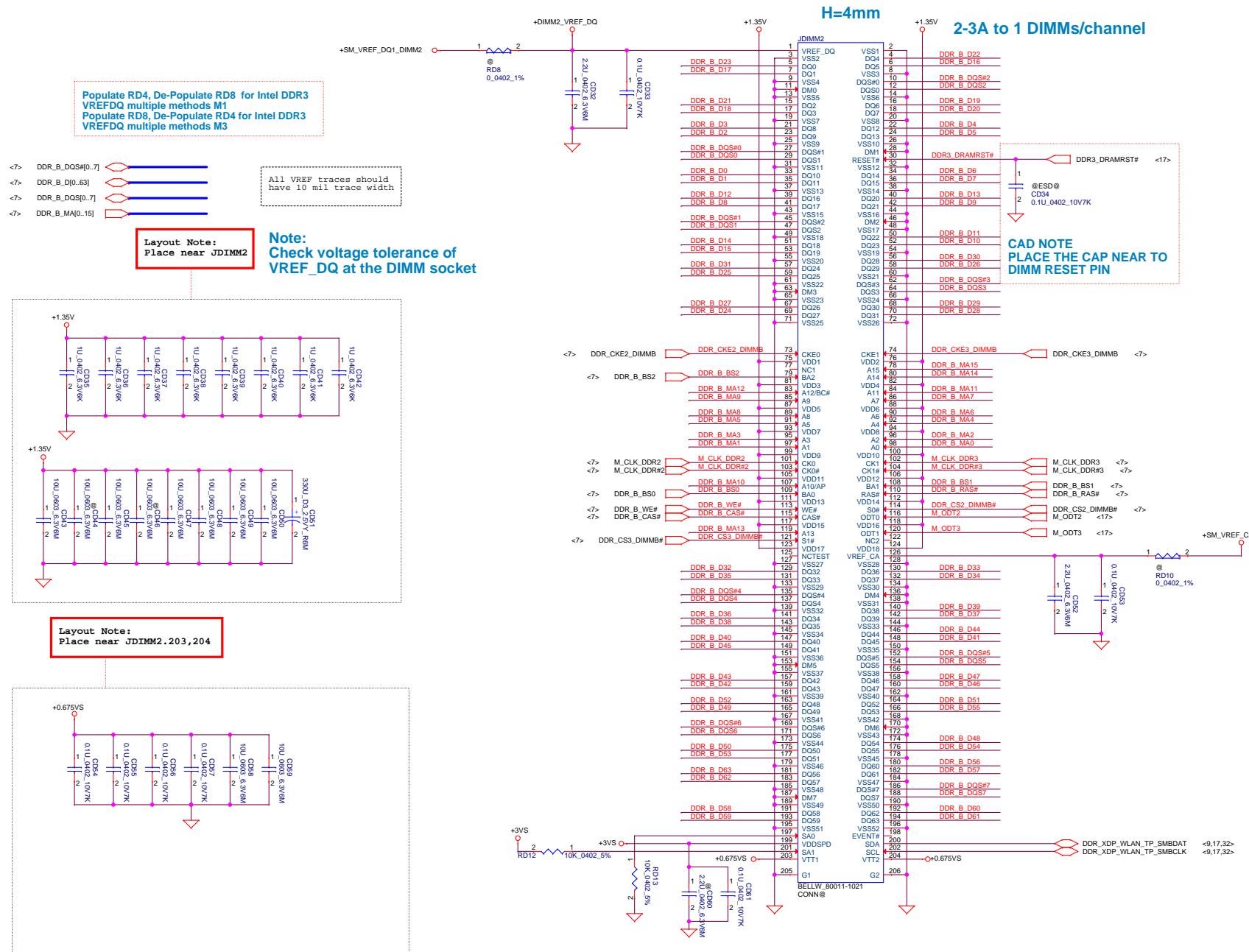
## **CFG STRAPS for CPU**



Display Port Presence Strap	
CFG4	<p>1: Disabled; No Physical Display Port attached to Embedded Display Port</p> <p>0: Enabled; An external Display Port device is connected to the Embedded Display Port.</p>

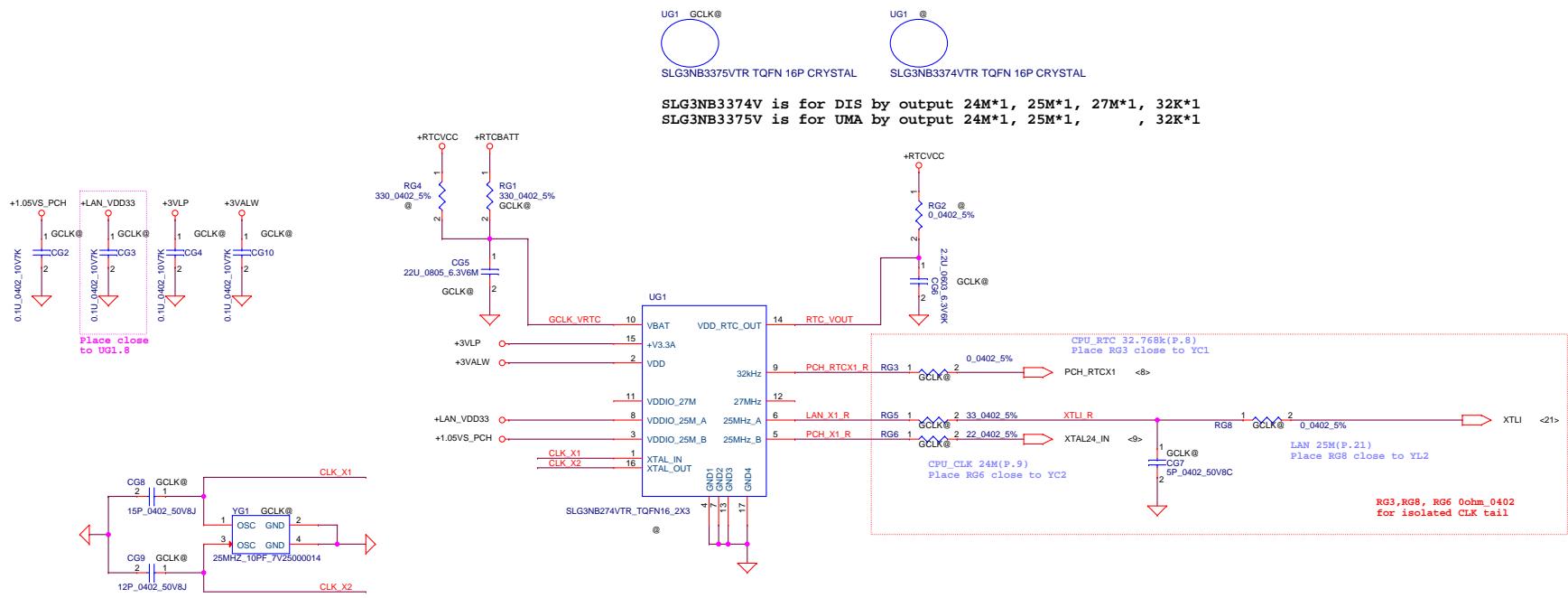






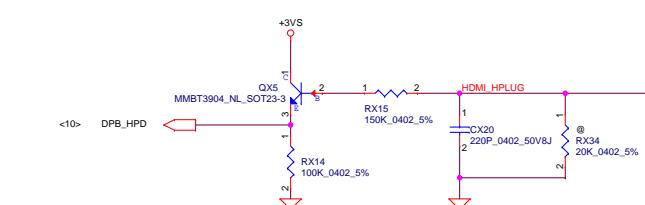
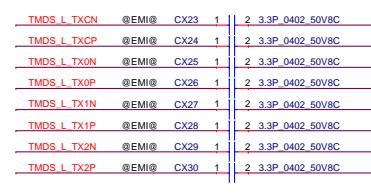
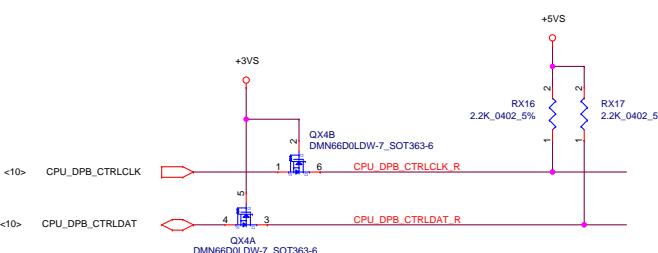
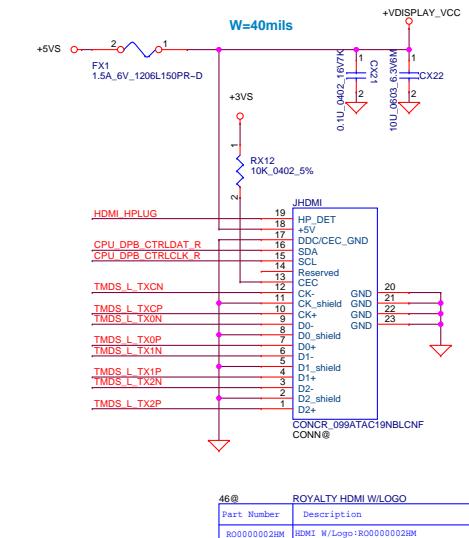
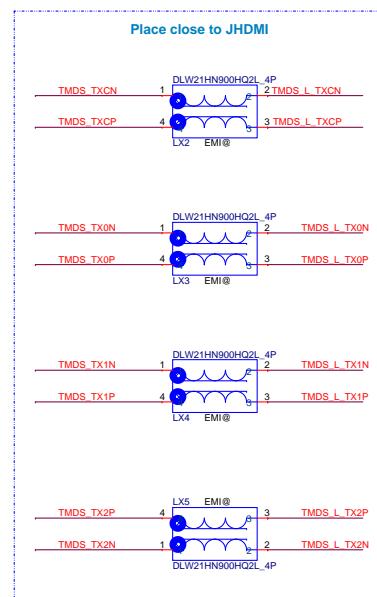
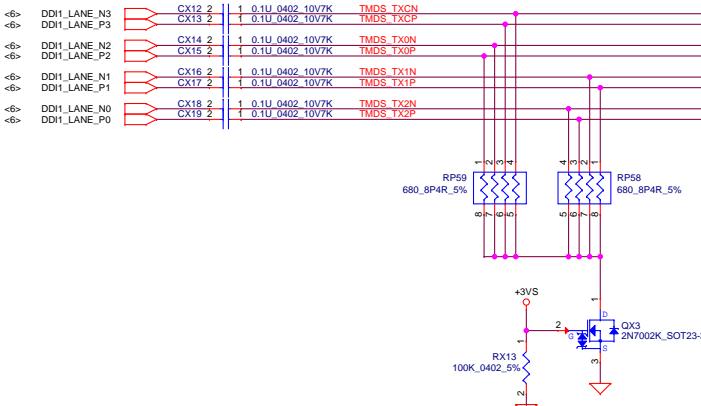
<b>Security Classification</b>	<b>Compal Secret Data</b>			<b>Compal Electronics, Inc.</b>		
<b>Issued Date</b>	2014/04/01	<b>Deciphered Date</b>	2015/04/30	<b>Title</b>	<b>DDR3L DIMMB</b>	
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Date:	Wednesday, September 10, 2014	Sheet	18	of	56	

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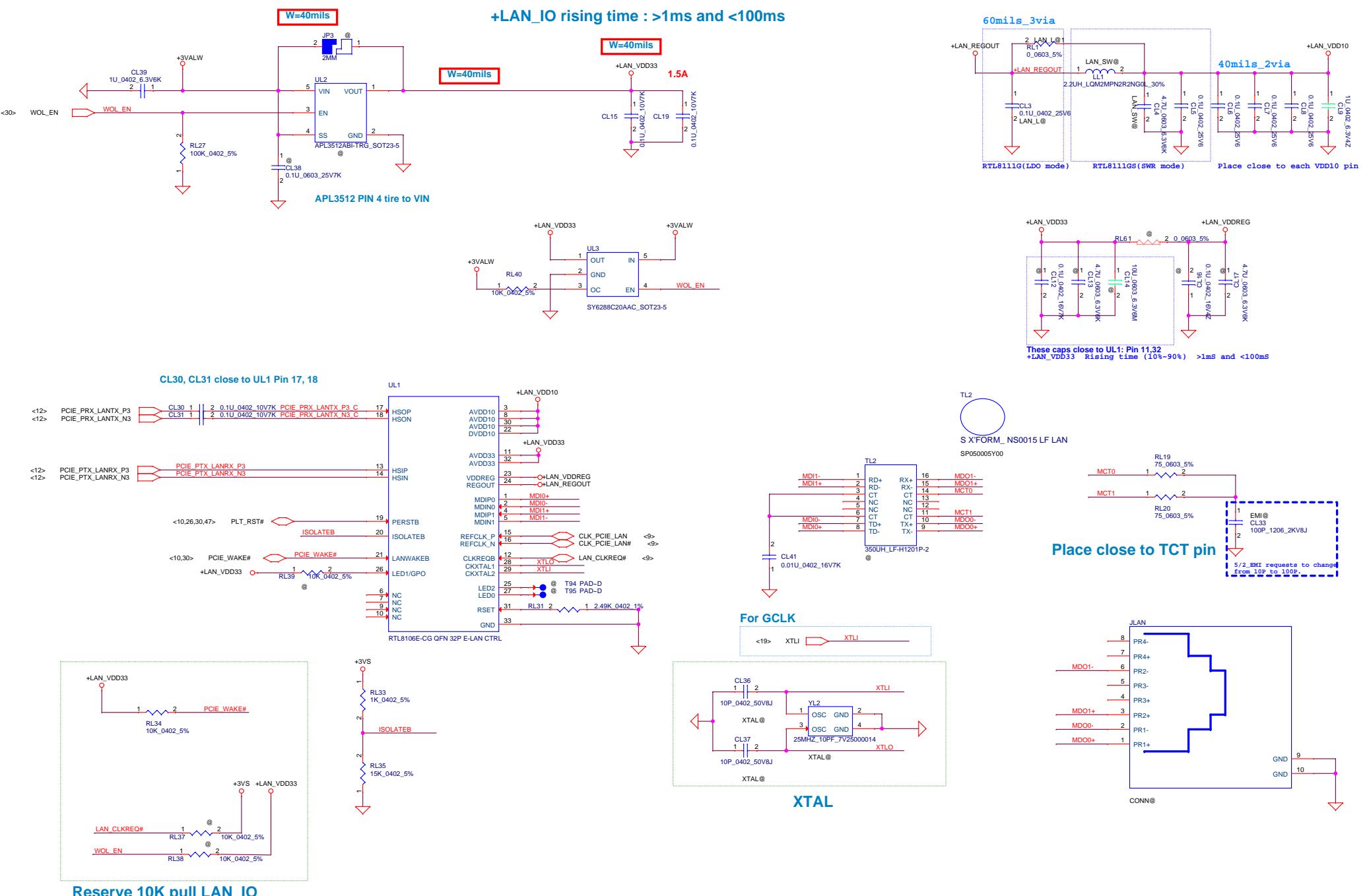
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title	Green CLK	
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					Sheet	19 of 56

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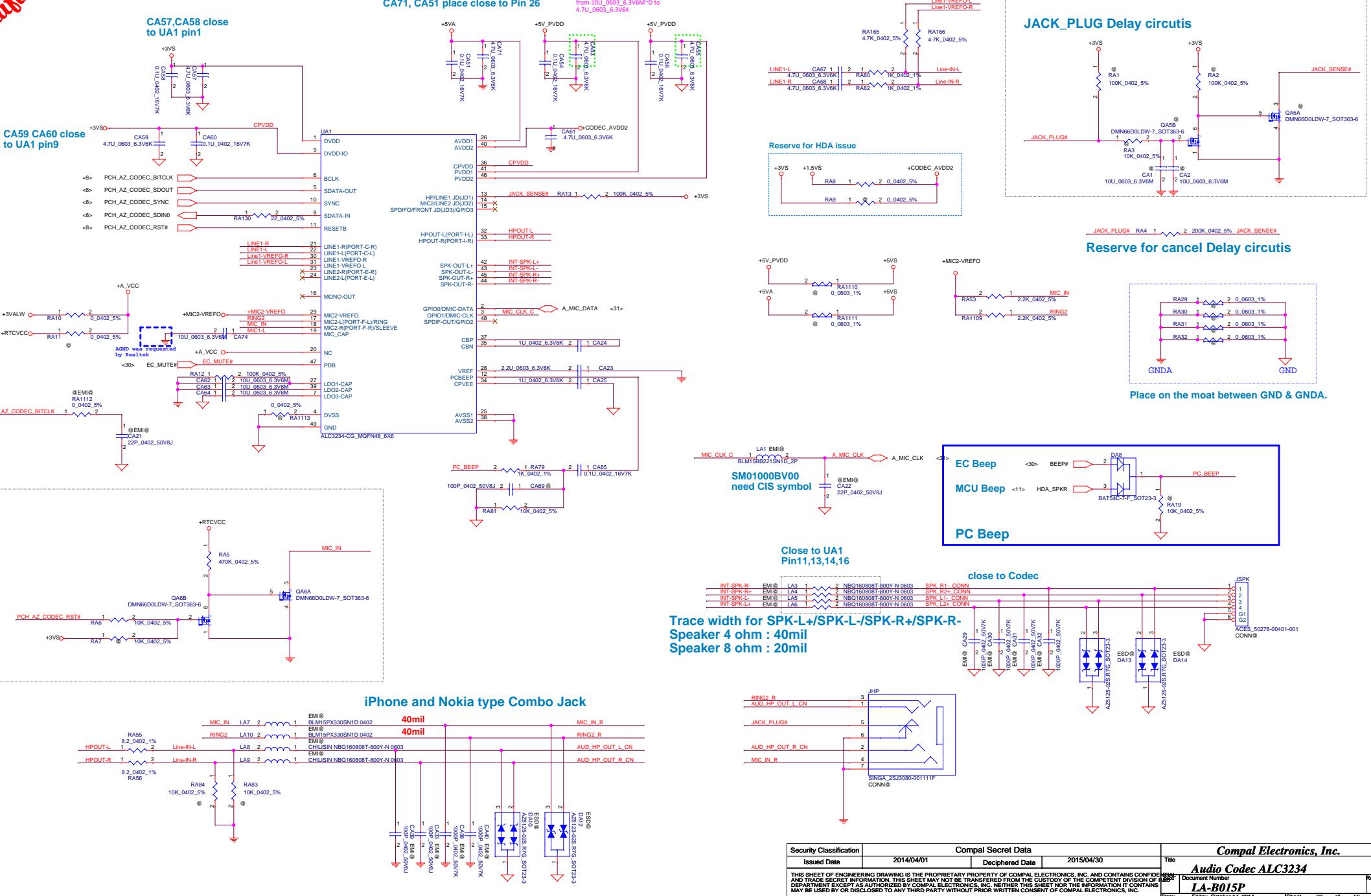
Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	Deciphered Date	2015/04/30	Title	LA-B015P
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2014/04/01			HDMI	Rev. 0.1
			Document Number	
			Date	Tuesday, September 16, 2014
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Document Number	LA-B015P	Rev.	0.1	10/100 LAN

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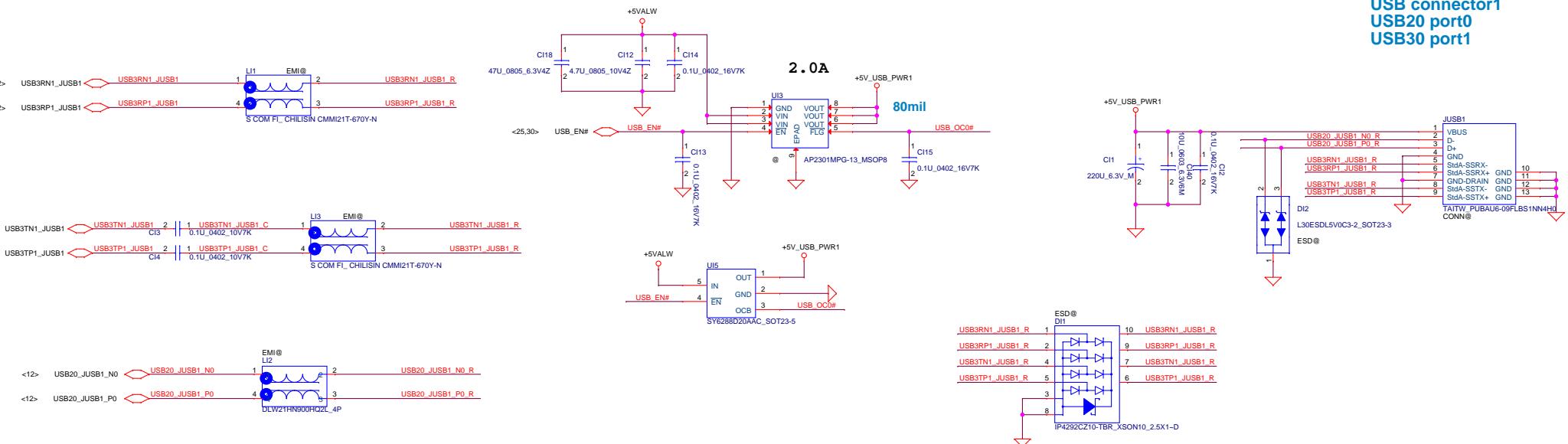


vinatix

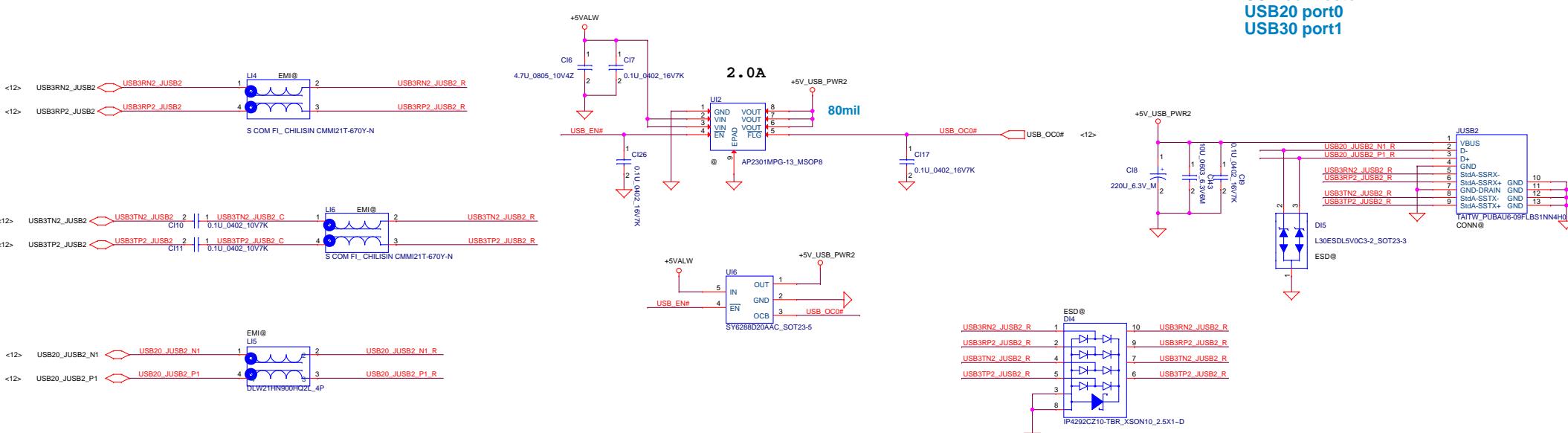
<http://vinafix.vn>

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**USB connector1**  
**USB20 port0**  
**USB30 port1**



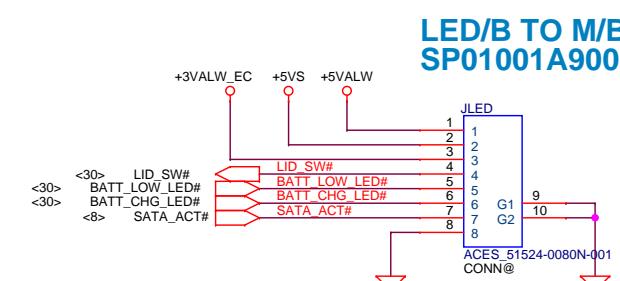
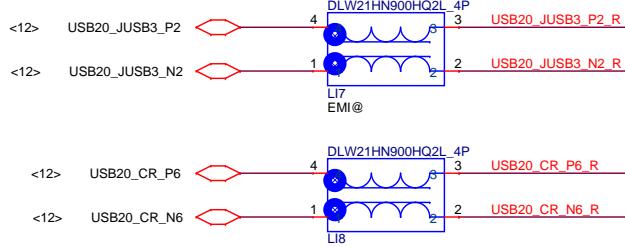
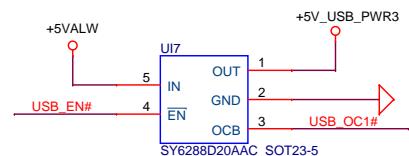
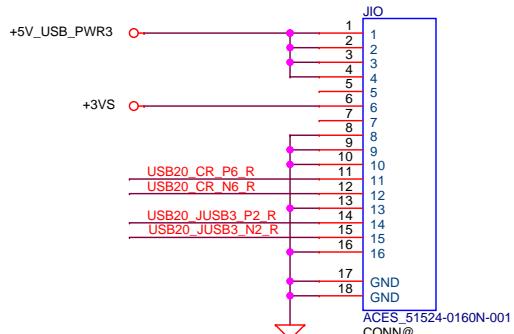
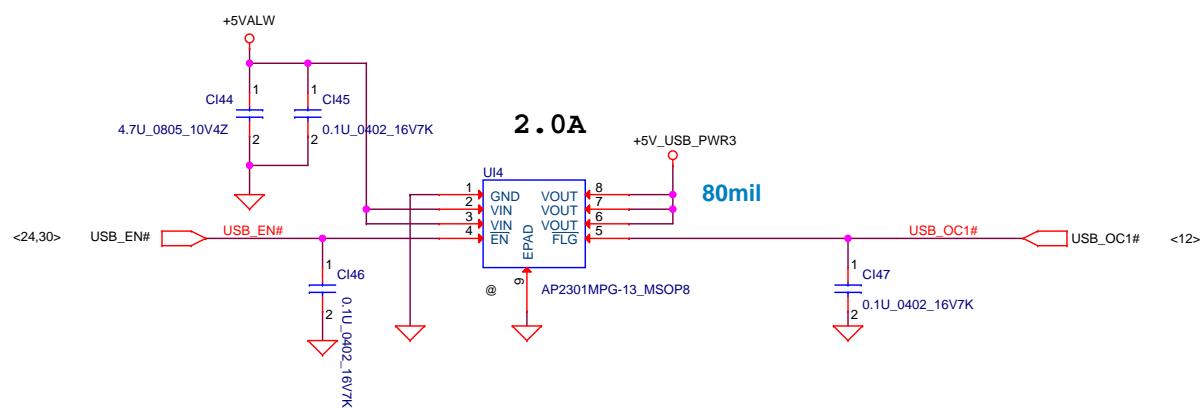
**USB connector2**  
**USB20 port0**  
**USB30 port1**



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Issued Date	Deciphered Date	2015/04/30	Compal Electronics, Inc.	USB3.0
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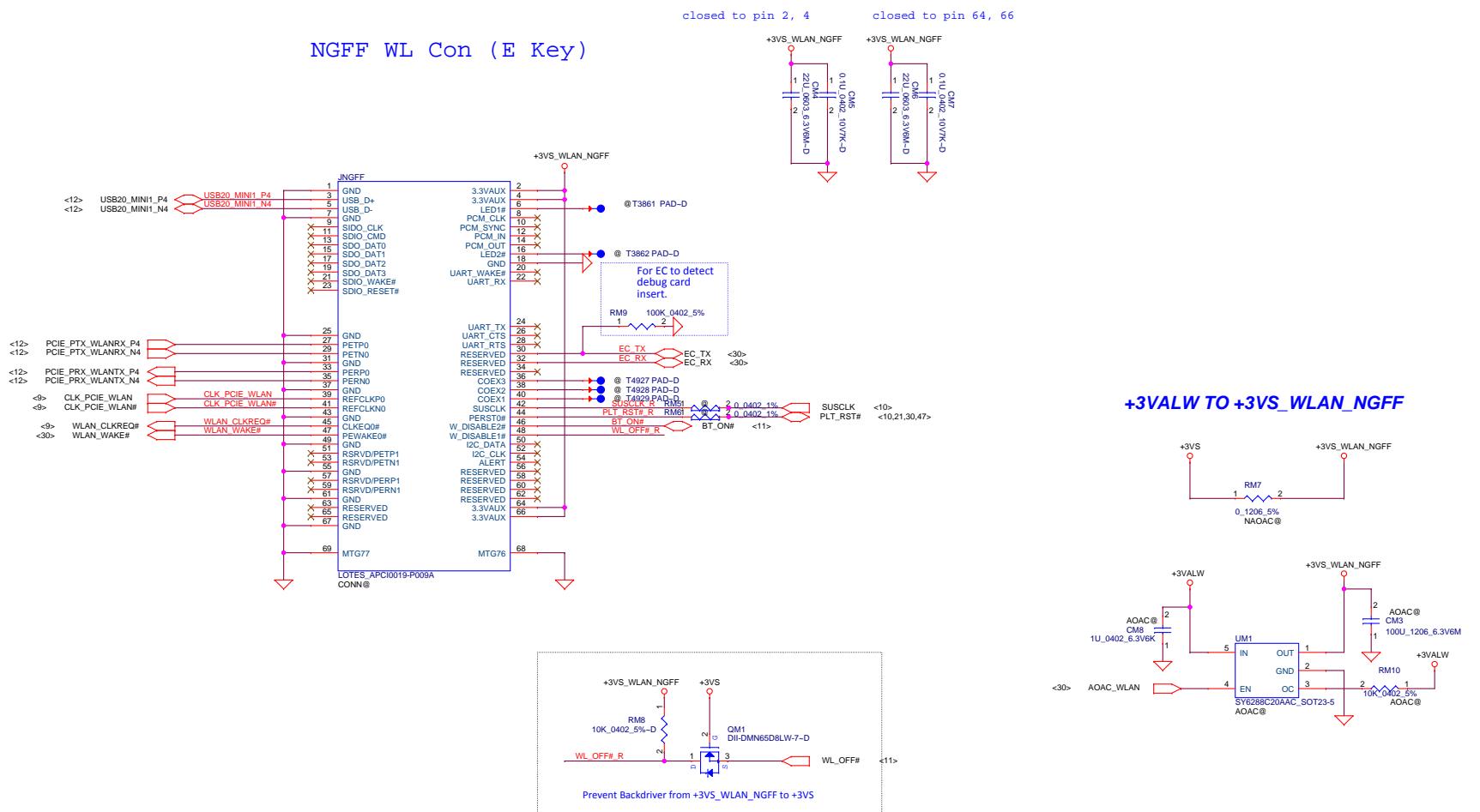
**IO to MB CONN**  
Substitute:SP01001FS00



**LED/B TO M/B**  
SP01001A900

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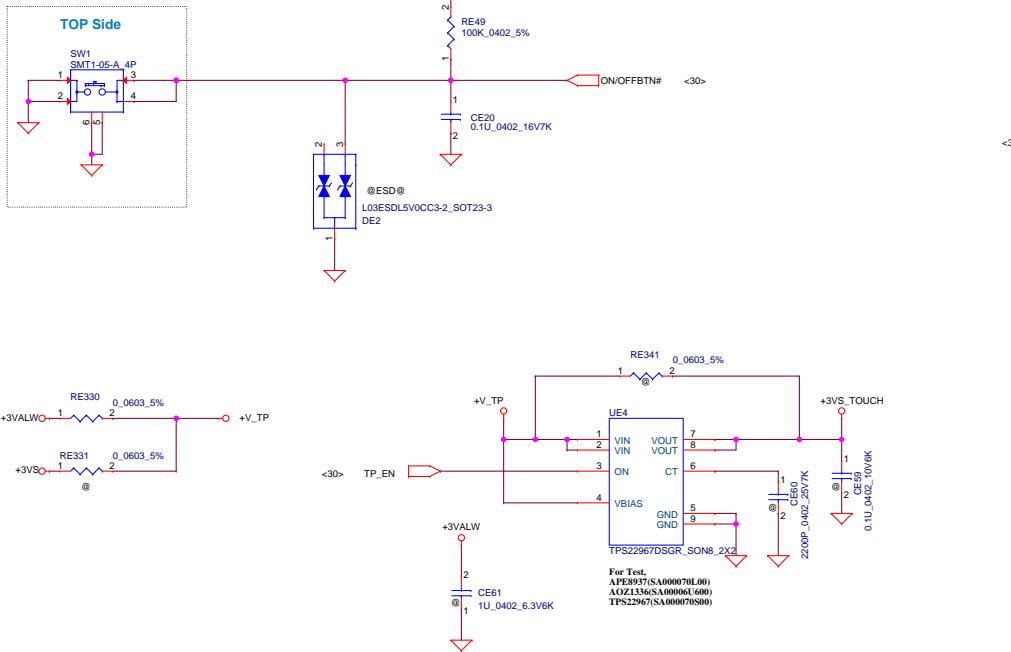


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2014/04/01	2015/04/30	NGFF WLAN		0.1		
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Date: Wednesday, September 10, 2014 Sheet 26 of 56						

## Power ON Circuit

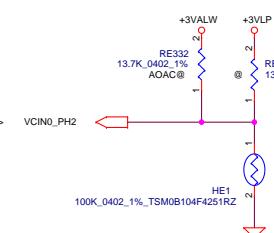
### ON/OFF switch



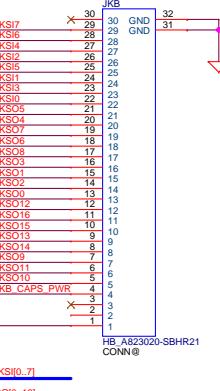
### FAN Control circuit



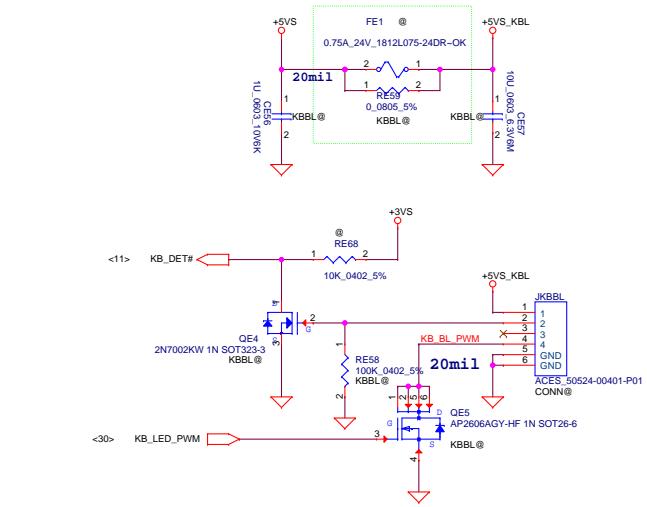
HE1 place around FAN area.



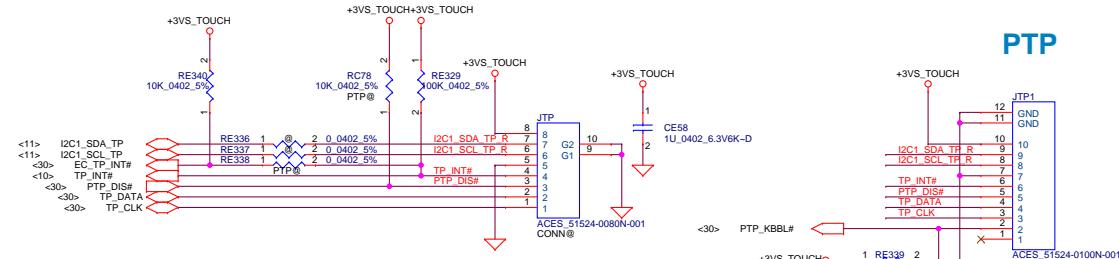
### INT\_KBD Connector



### \* Key Board Back Light

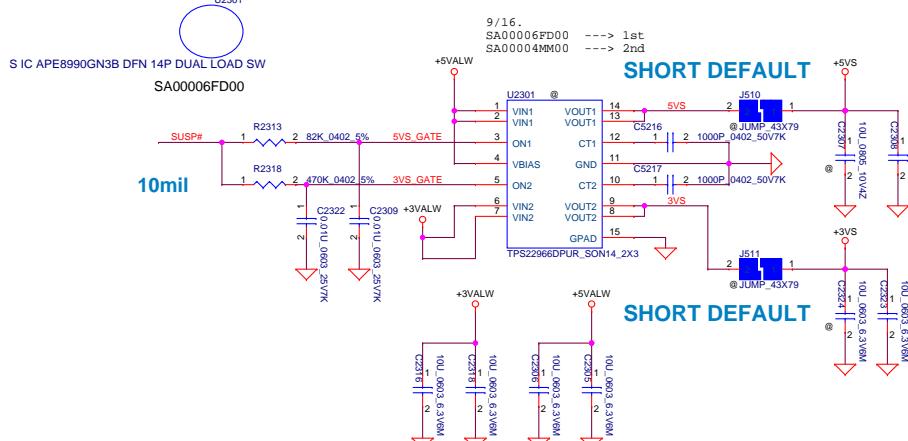


### Touch pad

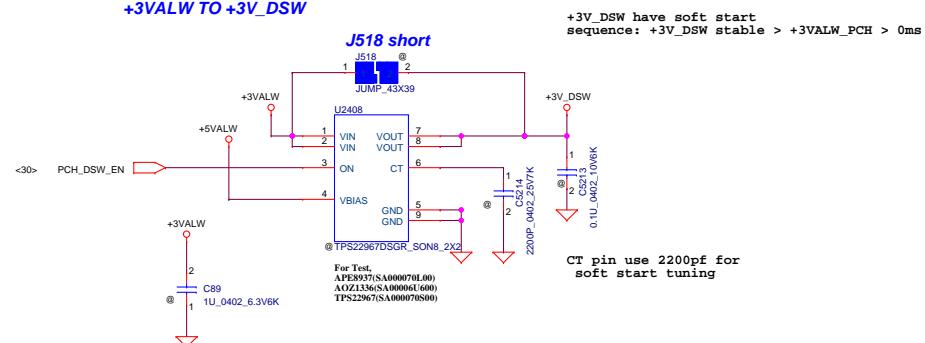


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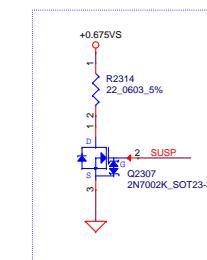
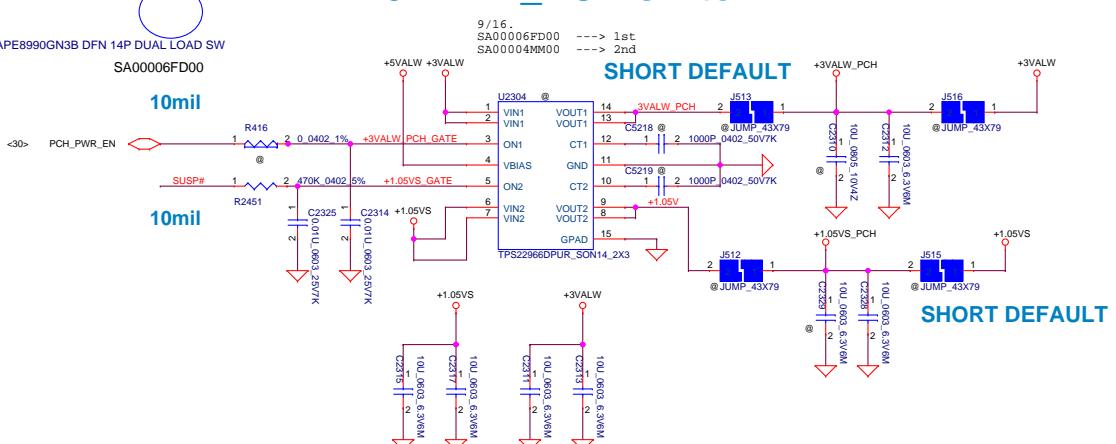
## +5VS and +3VS switch



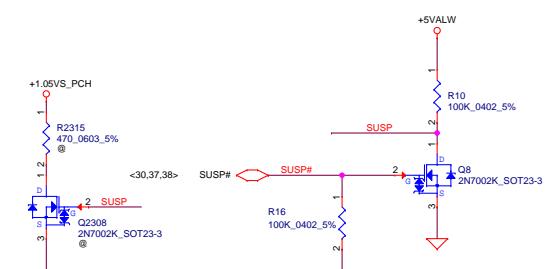
+3VALW TO +3V\_DSW



+3VALW PCH switch



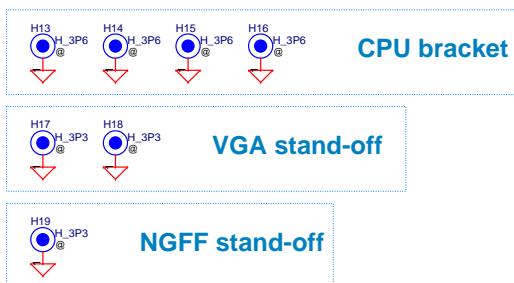
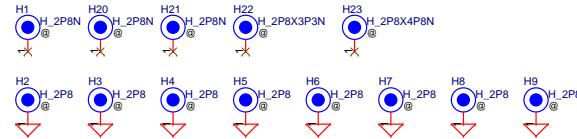
For Intel S3 Power Reduction



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Date:	Tuesday, September 16, 2014	Sheet	28	of	56	

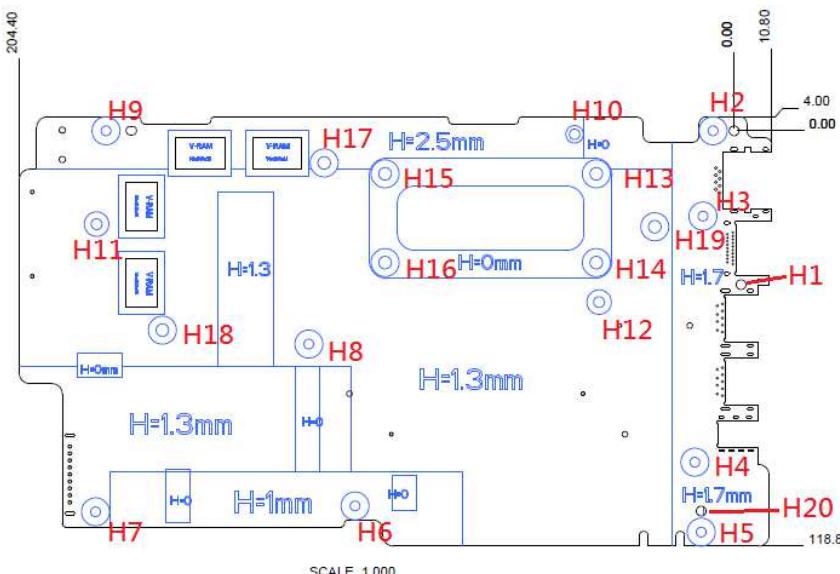
vinafix

## Screw Hole

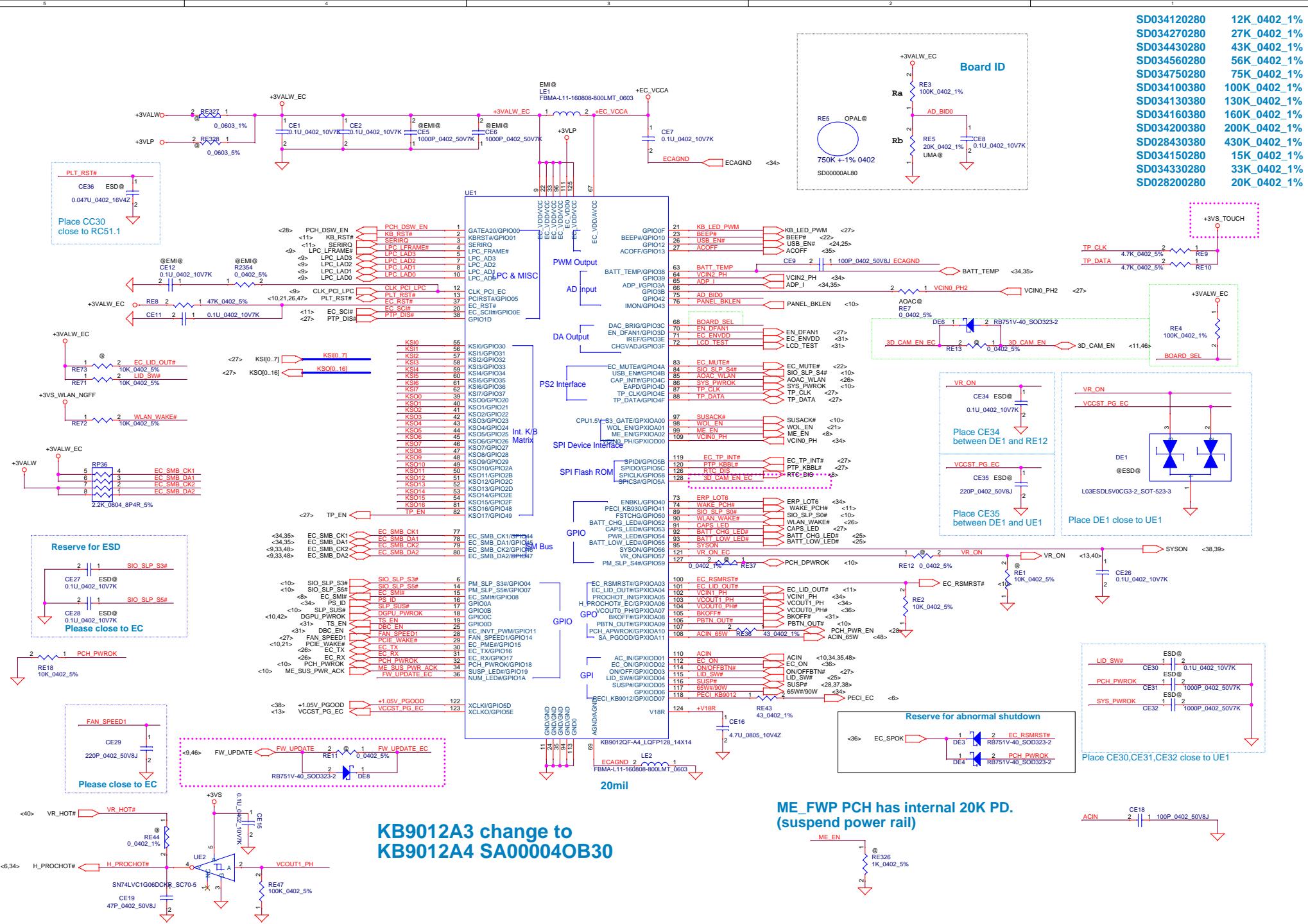


FD1 @ FIDUCIAL FD2 @ FIDUCIAL FD3 @ FIDUCIAL FD4 @ FIDUCIAL

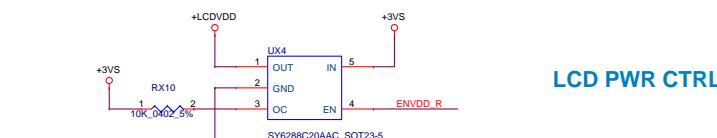
PCB 13G LA-B015P REV0 M/B  
DA80011D000



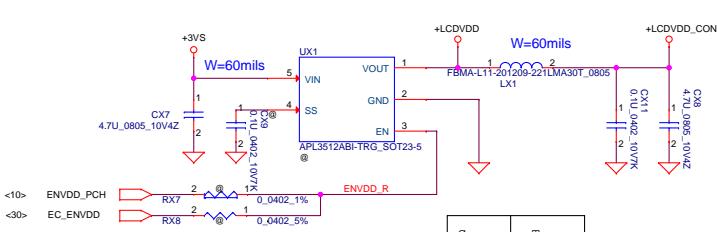
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Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title
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Screw Hole	Document Number	LA-B015P	Rev. 0.1	Date: Wednesday, September 10, 2014 Sheet 29 of 56



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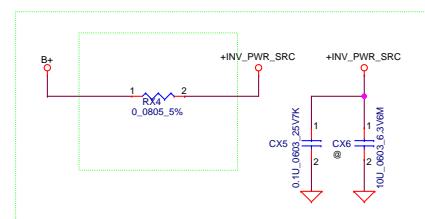


LCD PWR CTRL

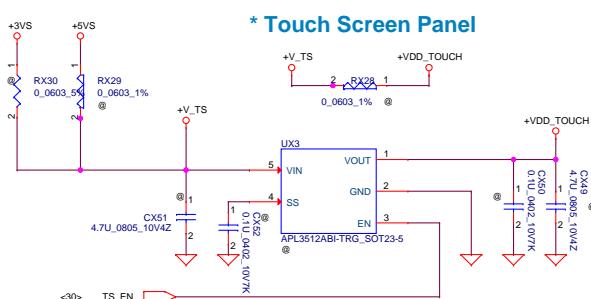


Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

SS table



Webcam PWR CTRL



Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

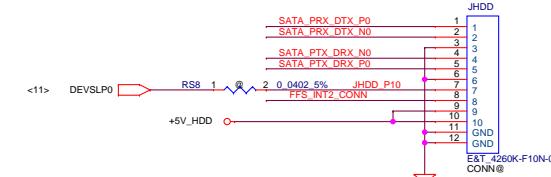
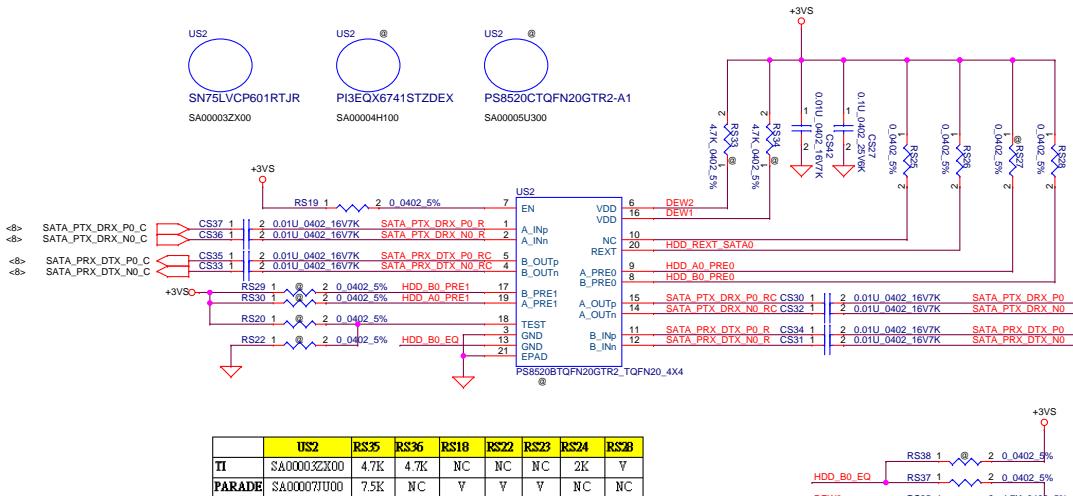
SS table

<http://vinafix.vn>

Security Classification	Compal Secret Data			Title
Issued Date	Deciphered Date	2015/04/30	Compal Electronics, Inc.	eDP / webcam / TouchScreen
2014/04/01				LA-B015P
Rev. 0.1	Date: Tuesday, September 16, 2014	Sheet 31 of 56	Document Number:	

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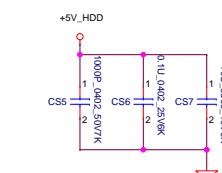
## SATA HDD Connector



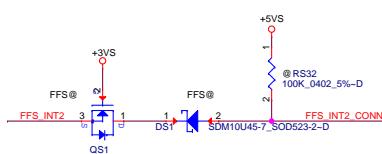
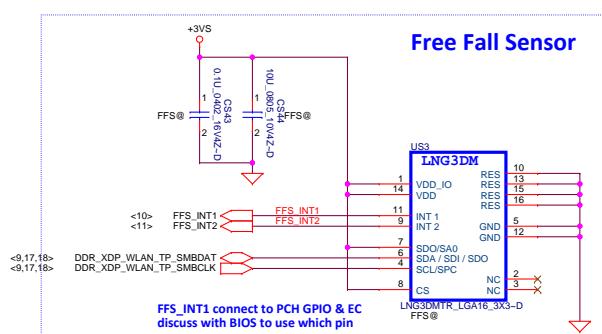
## +5V\_HDD Source



## SHORT DEFAULT



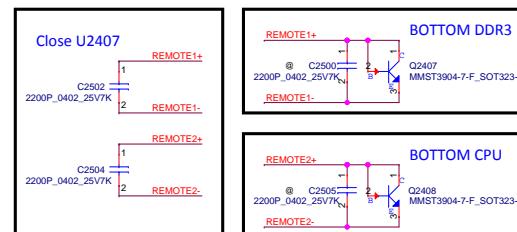
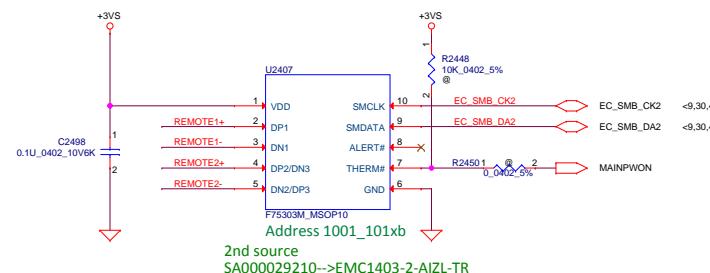
## Free Fall Sensor



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Document Number	LA-B015P	Rev	0.1	Date	Wednesday, September 10, 2014	Sheet 32 of 56		

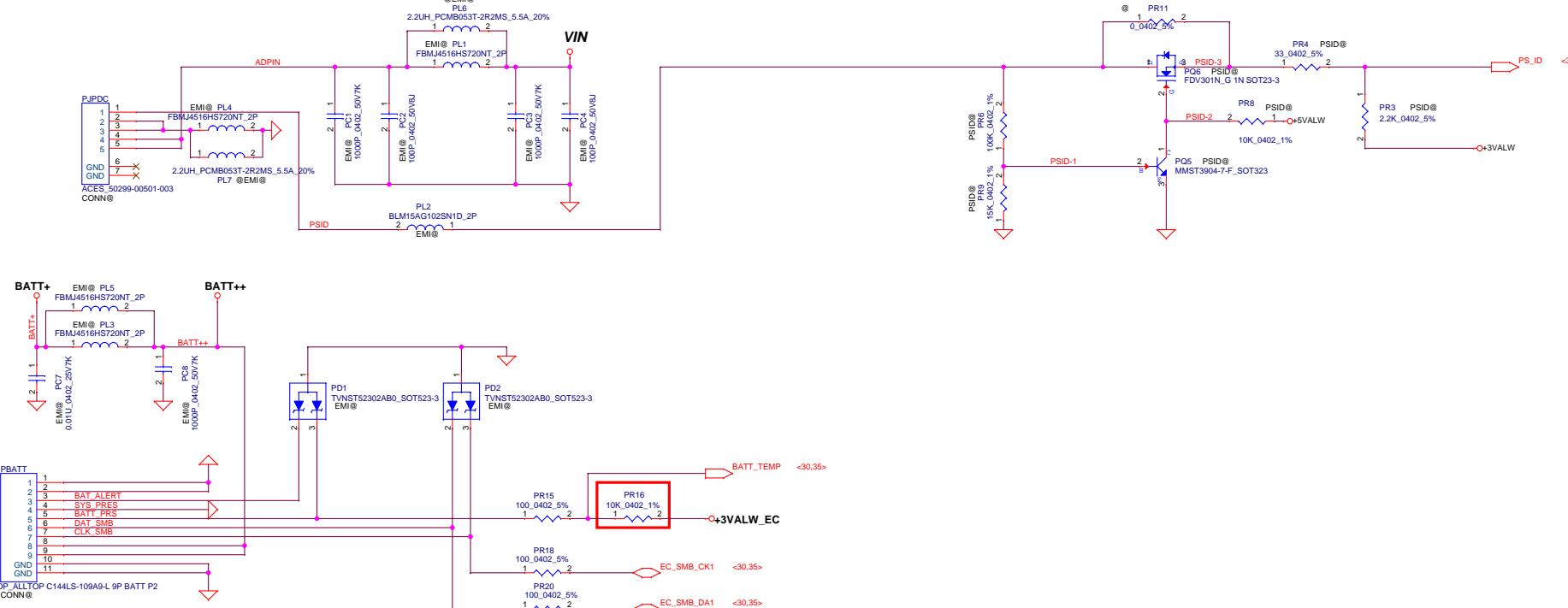
vinafix

Fintek thermal sensor  
placed near by TOP DDR3

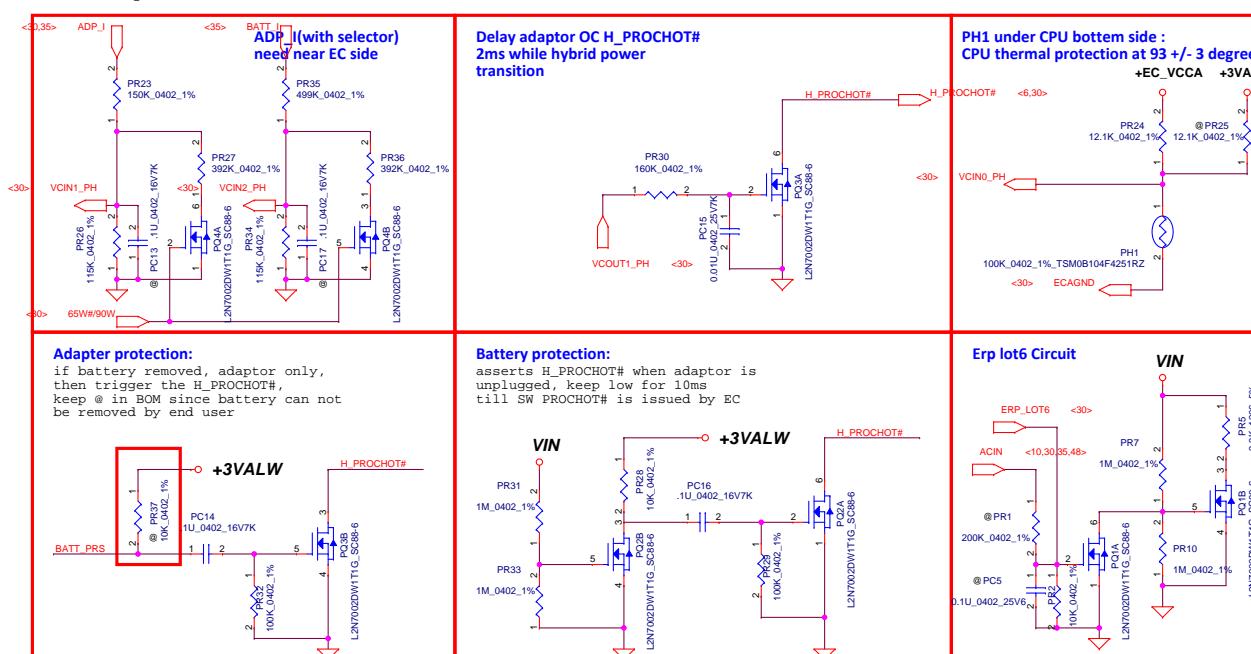


REMOTE1,2 (+/-):  
Trace width/space:10/10 mil  
Trace length:<8"

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Thermal Sensor	LA-B015P	Rev. 0.1	Date: Wednesday, September 10, 2014	Sheet 33 of 56

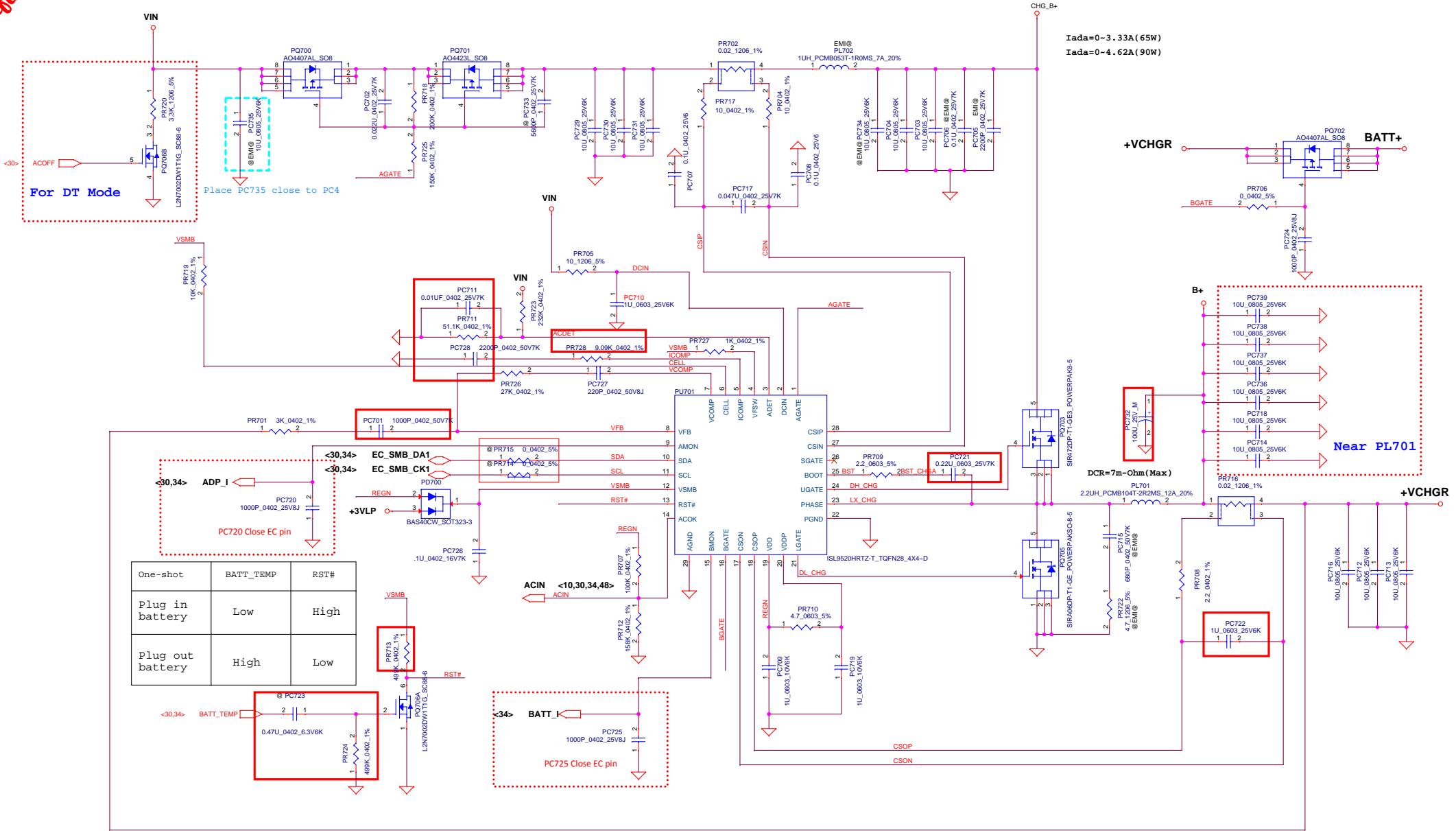


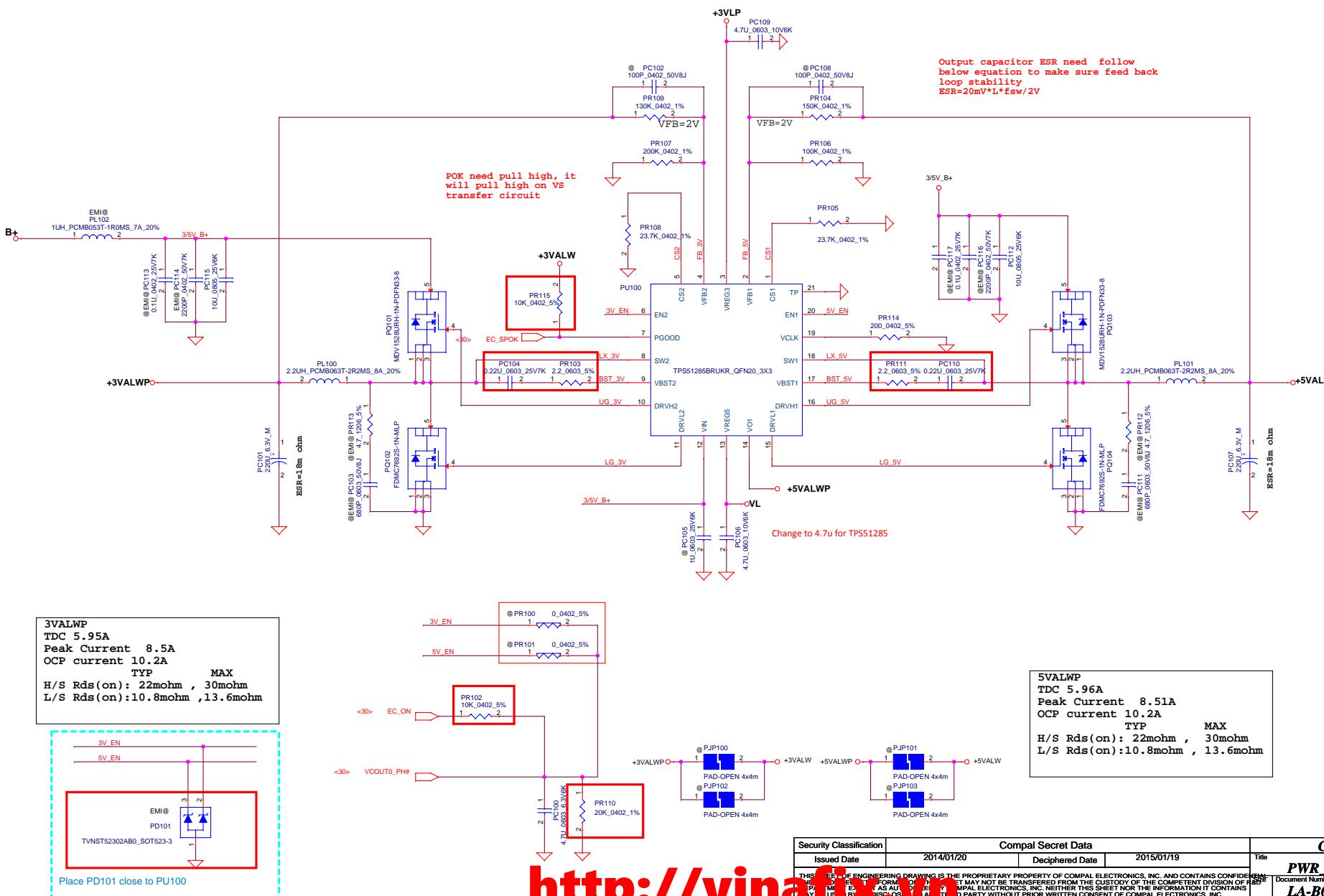
### Other component (37.1)

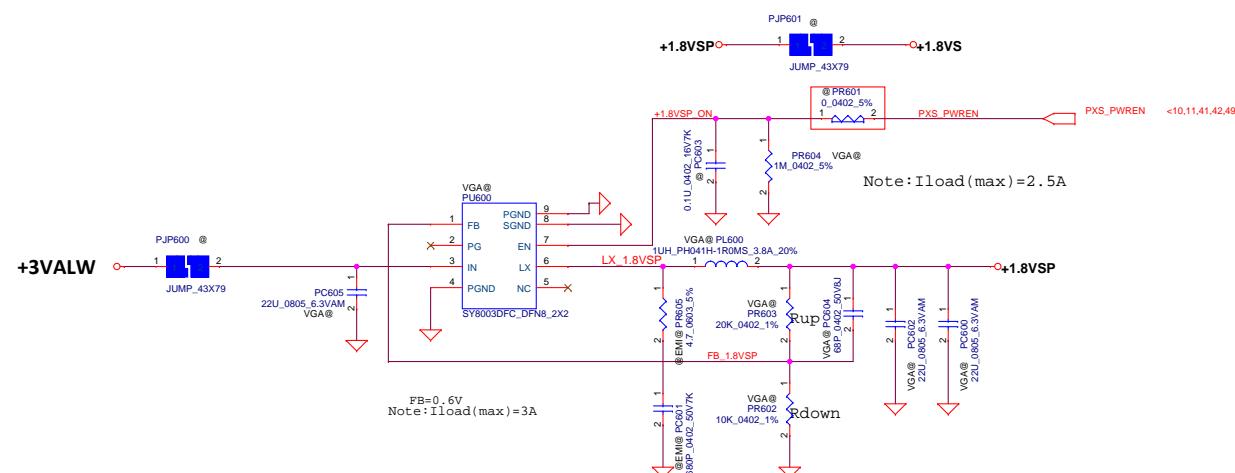
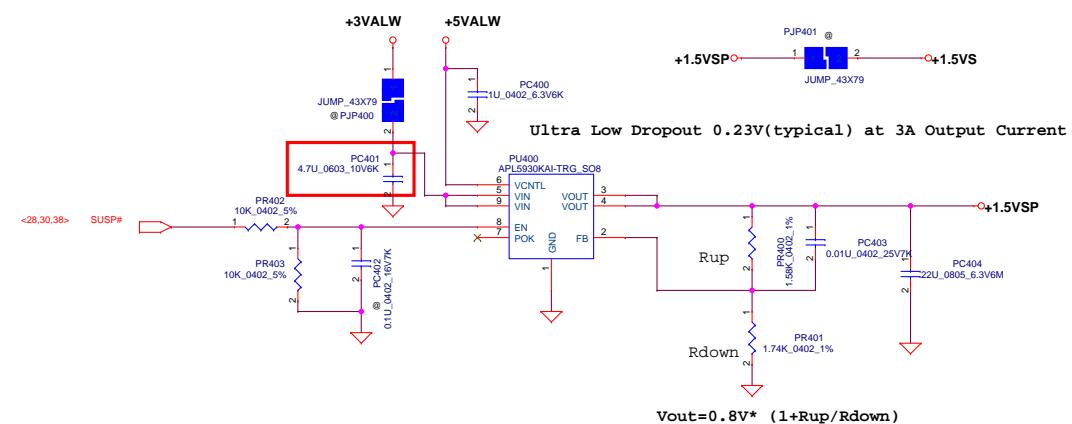


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CONFIDENTIAL	2014/01/20	2015/01/19	Document Number	LA-B012P	Rev 1.0
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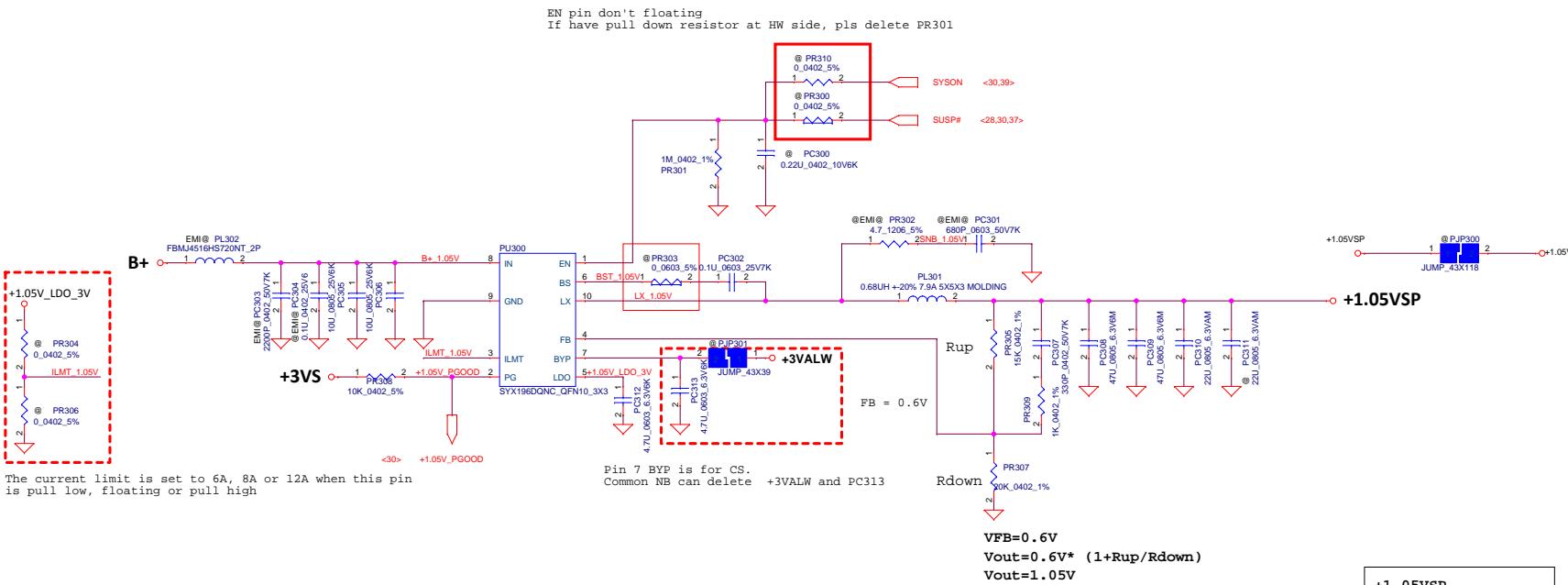
vinafix


<http://vinafix.vn>





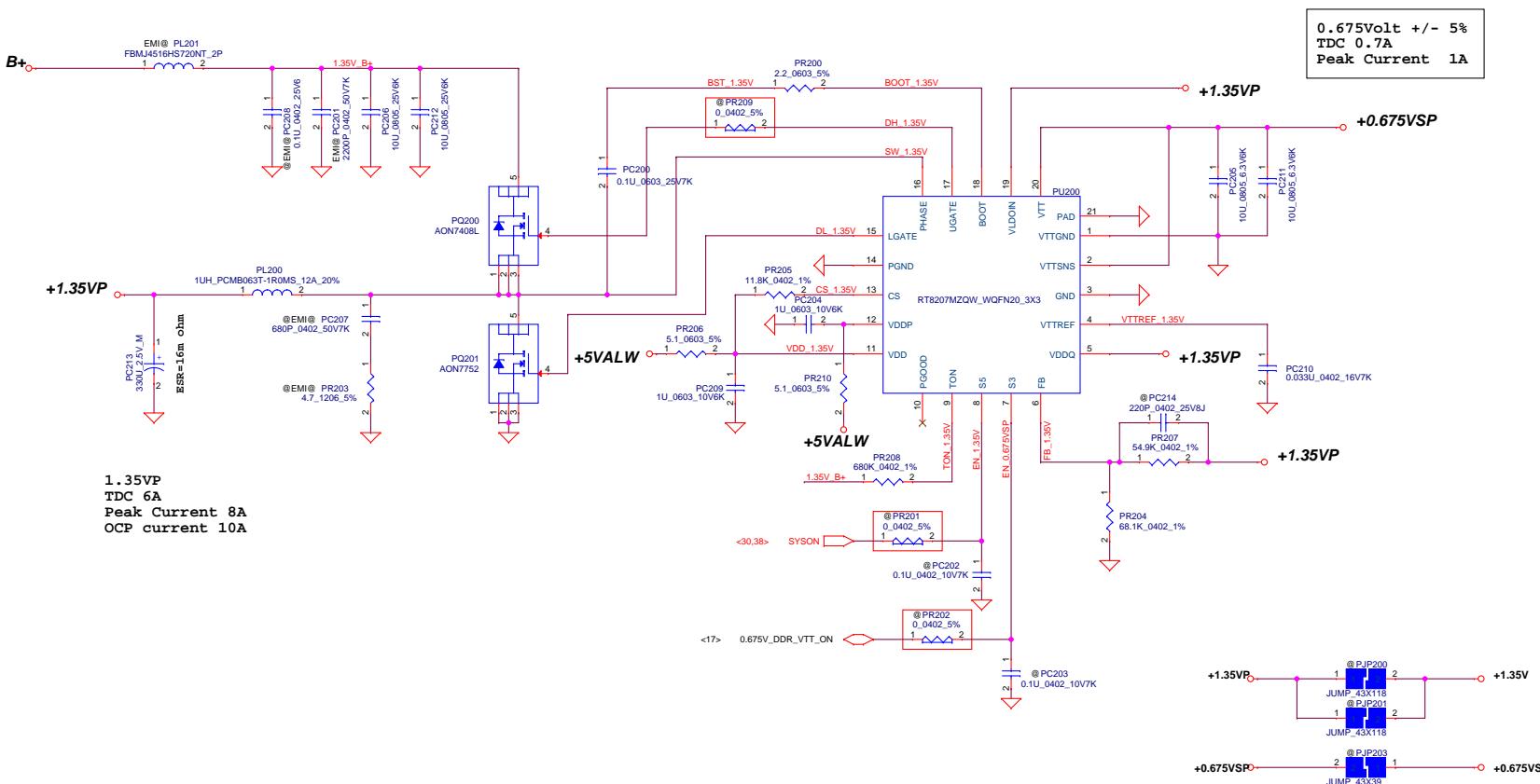
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Issued Date	Deciphered Date	2015/01/19	Title	PWR+_VCCIO	
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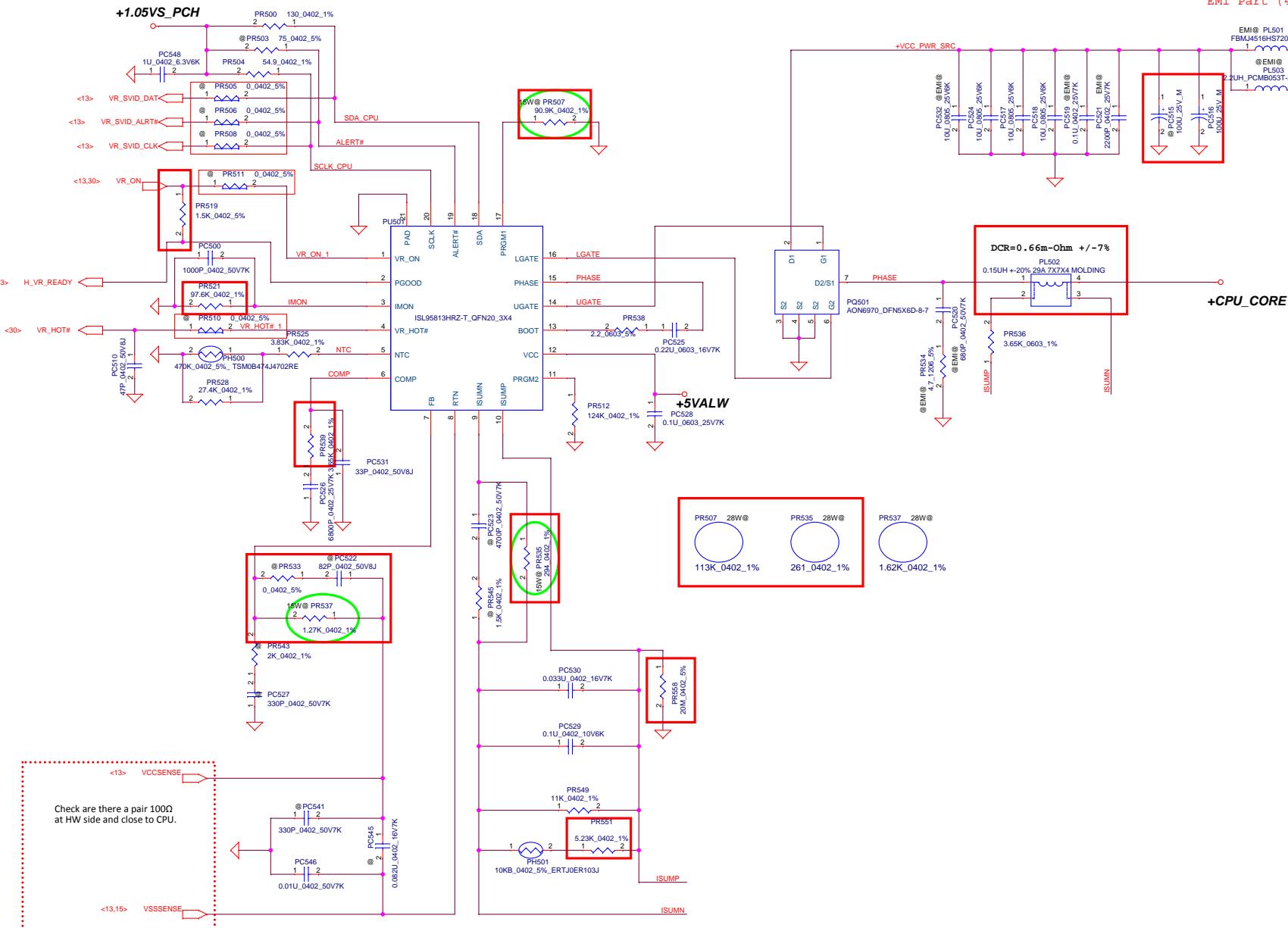
<http://vinafix.vn>

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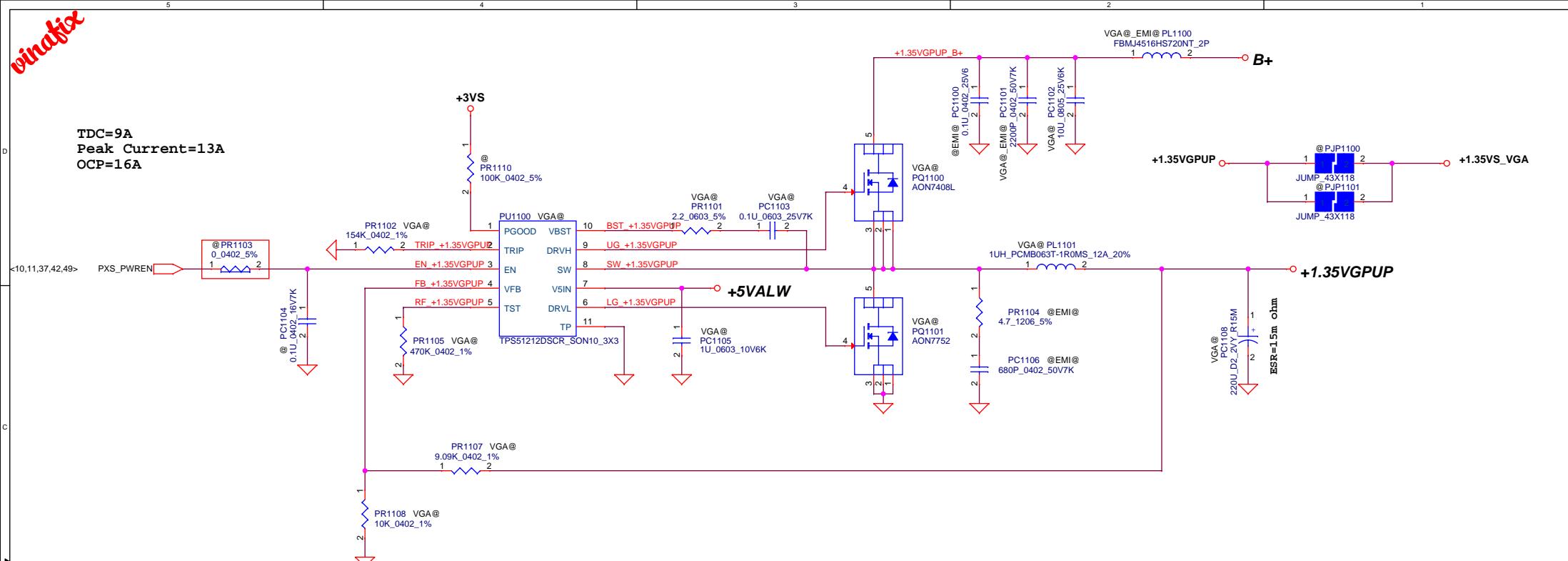
vinatix



CPU\_CORE  
TDC 10A/14A(PL2)@15W CPU  
Peak Current 32A@15W CPU  
OCP current 40A@15w  
Choke DCR 1.1m-Ohm(Max)  
Load line -2mV/A

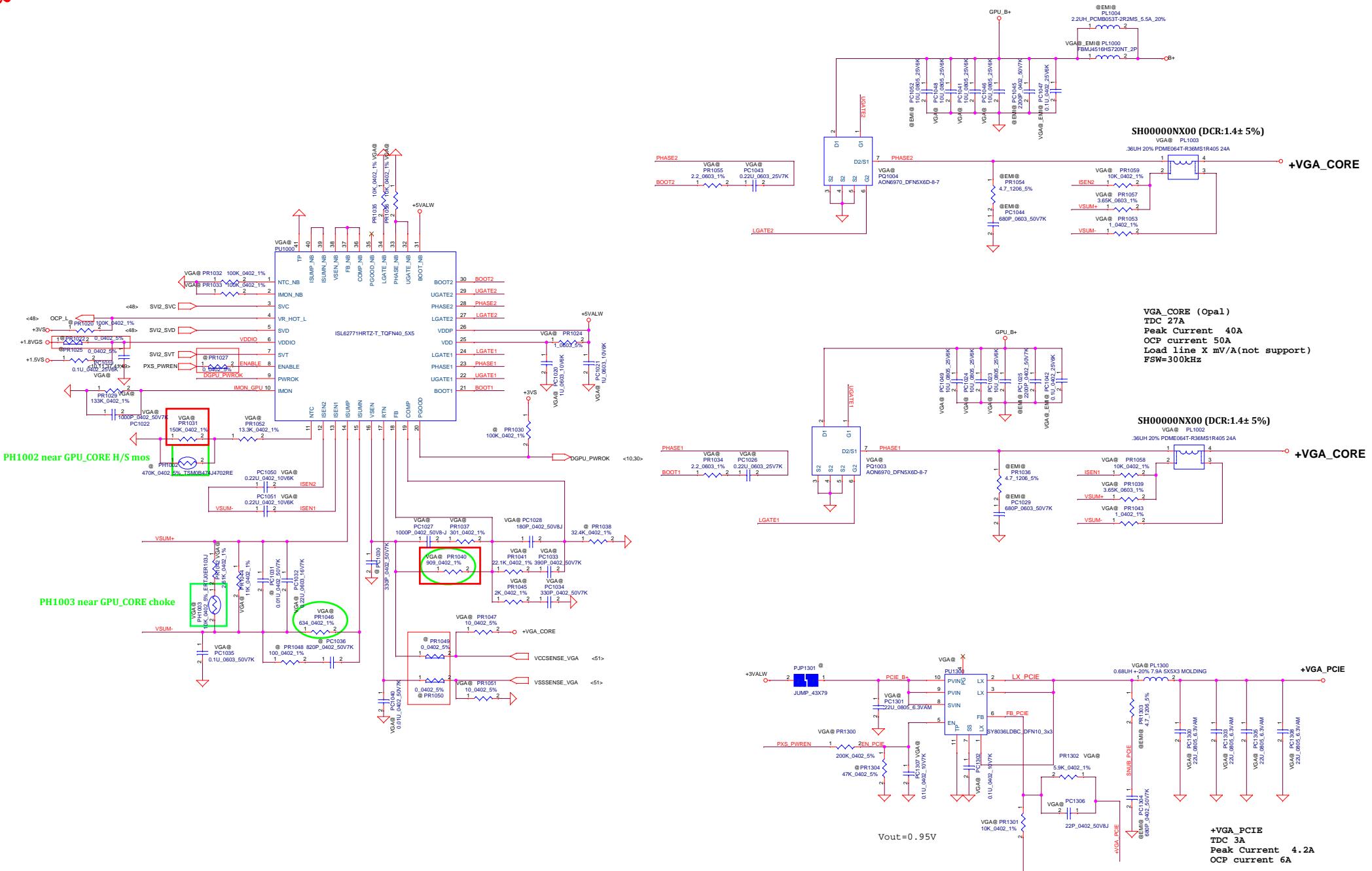
Security Classification	Compal Secret Data			<b><i>Compal Electronics, Inc.</i></b>		
Issued Date	2014/01/20	Deciphered Date	2015/01/19	Title	<b>PWR VCORE</b>	
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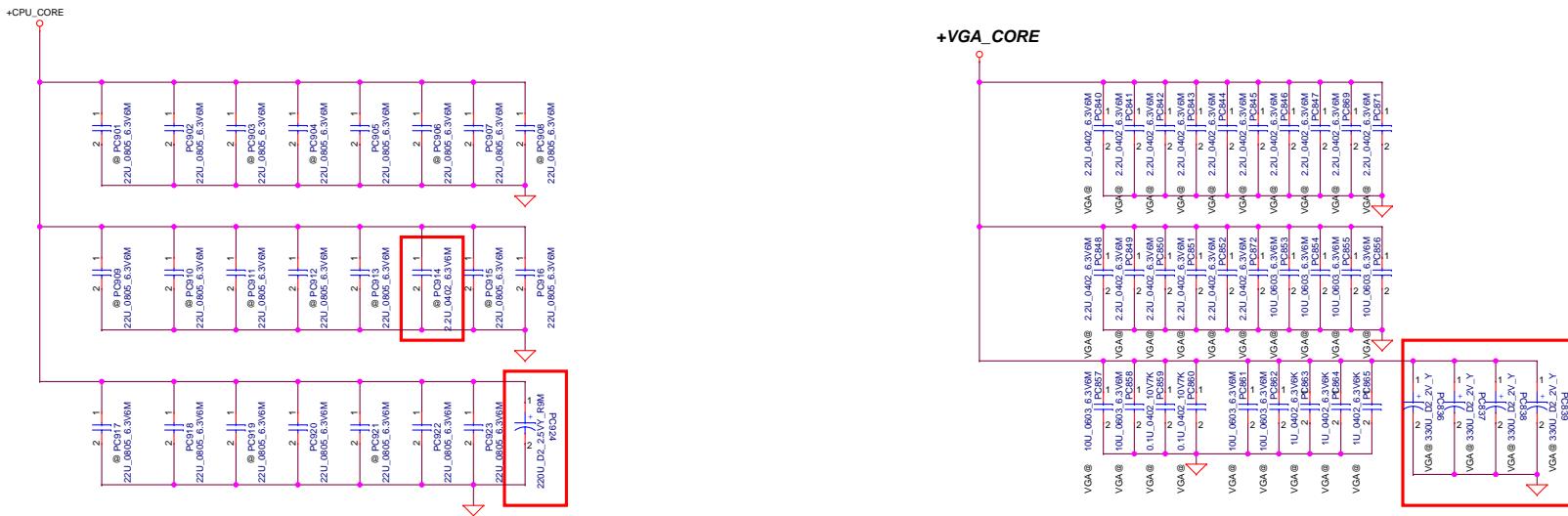
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Issued Date	Deciphered Date	Rev	Document Number	LA-B012P
2014/01/20	2015/01/19	1.0	Date: Wednesday, September 10, 2014	Sheet 41 of 56

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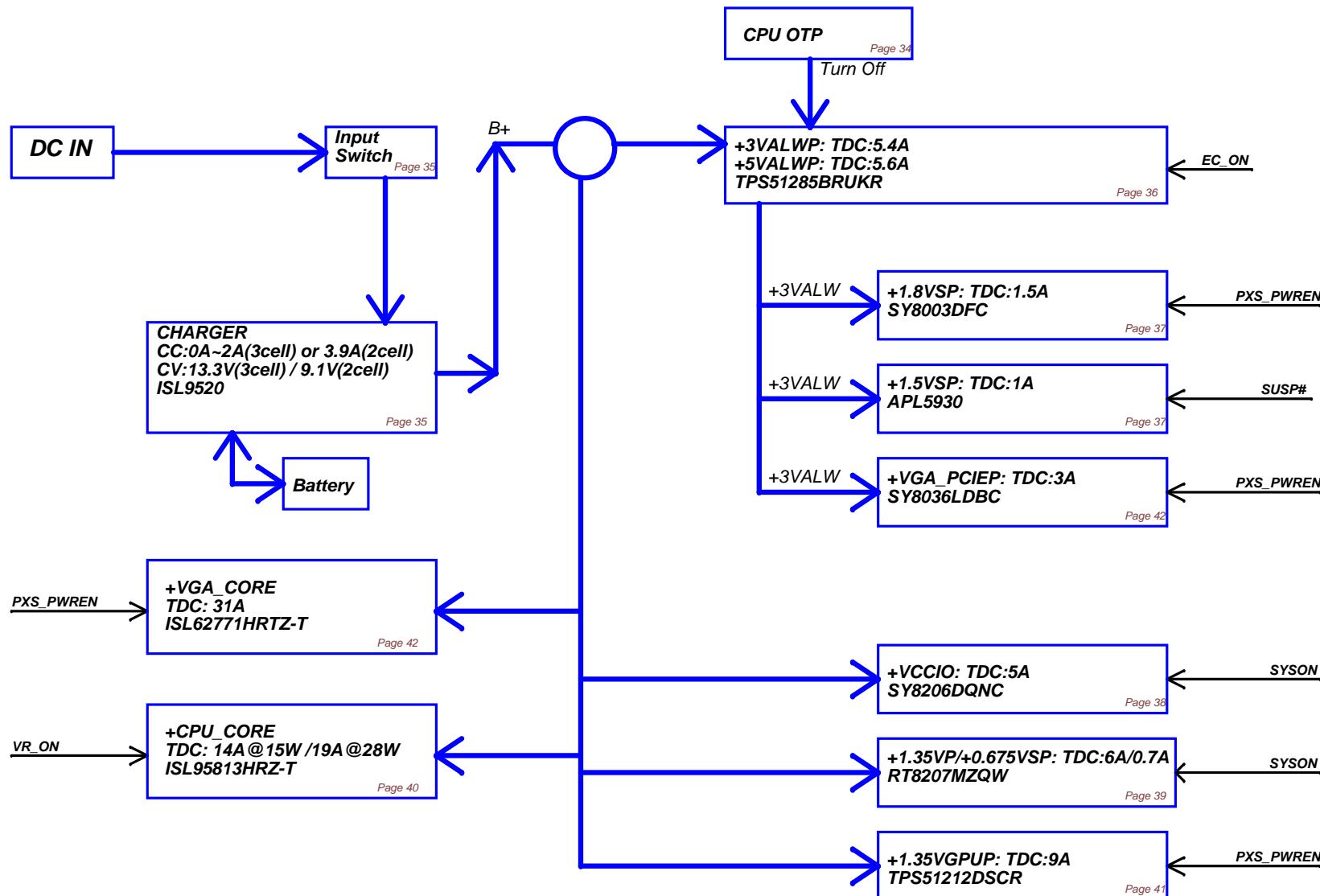


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## Power block



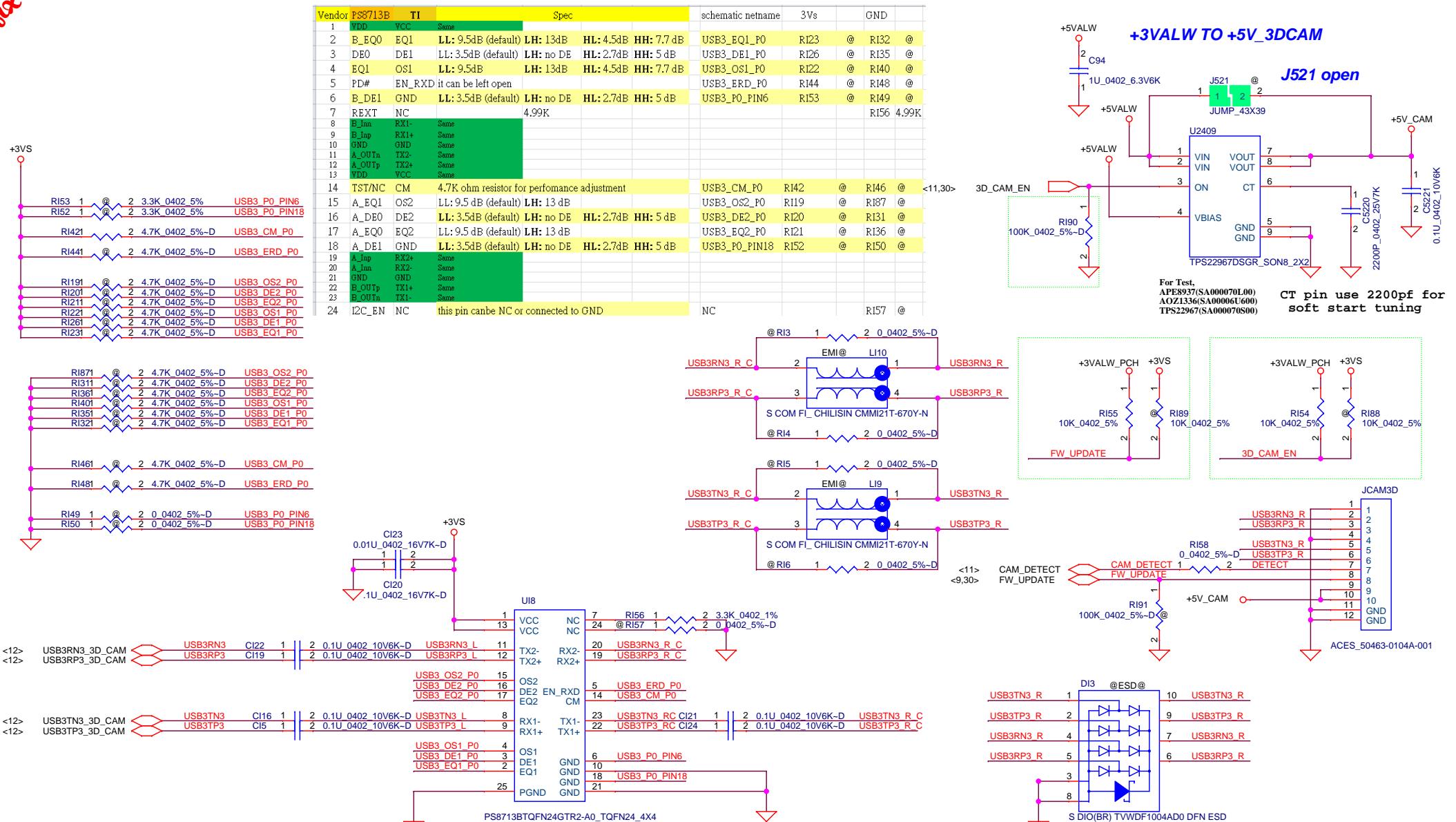
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1	44	DCIN/BATT CONN/OTP	13/10/24	Morris	design change	change PR16 from 100K to 10K add PR37 10K	0.2
2	45	CHARGER	13/10/24	Morris	design change	change PC711 from 1000pF to 0.01uF change PR711 from 49.9K to 51.1K change PR713 from 10K to 499K change PR724 from 100K to 499K change PC721 from 0.047u to 0.22u change PC722 from 0.1u to 1u add PC732 100u	0.2
3	46	3.3VALWP/5VALWP	13/10/24	Morris	design change for solve can't root issue	change PC104 from 0.1u to 0.22u change PC110 from 0.1u to 0.22u change PR102 from 2.2K to 10K add PR110 20K	0.2
4	50	VCORE	13/10/24	Morris	adjust CPU parameter	change PR507(15W@) from 90.9K to 169K change PR519 from 1.91K to 10K change PR521 from 95.3K to 97.6K change PR539 from 8.06K to 909 change PC515,PC516 from SF000005100 to SF000004M00 change PL502 from SH00000NM00 to SH00000PQ00 change PR535(15W@) from 340 to 210 change PR537 from 1.27K to 1.37K change PR535(28W@) from 432 to 261 change PR507(28W@) from 113K to 205K change PR551 from 2.61K to 5.23K add PC522 82pF add PR533 0-ohm	0.2
6	52	VGA_CORE/PCIE	13/10/24	Morris	design change from vendor change LL	change PR1040 from 1.24K to 825	0.2
7	53	PROCESSOR DECOUPLING	13/10/24	Morris	adjust CPU parameter	change PC924 from SGA20331E10 to SGA00009800 remove PC901,PC903,PC904,PC906,PC908,PC909,PC910,PC911,PC912,PC913,PC914,PC915,PC917,PC919,PC921	0.2
8	45	CHARGER	13/10/28	Morris	design change for plug out battery shut down issue	change PC723 from 0.01uF to 0.47uF change PR728 from 0 to 9.09K change PC728 from 4700pF to 2200pF change PC701 from 220pF to 1000pF	0.2
9	46	3.3VALWP/5VALWP	13/12/12	Morris	design change from EE request	add PR115 10K-ohm	0.3
10	50	VCORE	13/12/12	Morris	design change from Intel recommend	change PR519 from 10K to 1.5K	0.3
11	48	+VCCIO	13/12/13	Morris	design change from EE request	delete PR310 and add PR300 0-ohm	0.3
12	50	VCORE	14/01/20	Morris	adjust CPU parameter	change PR507(15W@) from 169K to 90.9K change PR507(28W@) from 205K to 113K	1.0
13	53	PROCESSOR DECOUPLING	14/02/13	Morris	design change from thermal request	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0
14	50	VCORE	14/03/03	Morris	design change for VGA thermal issue	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0

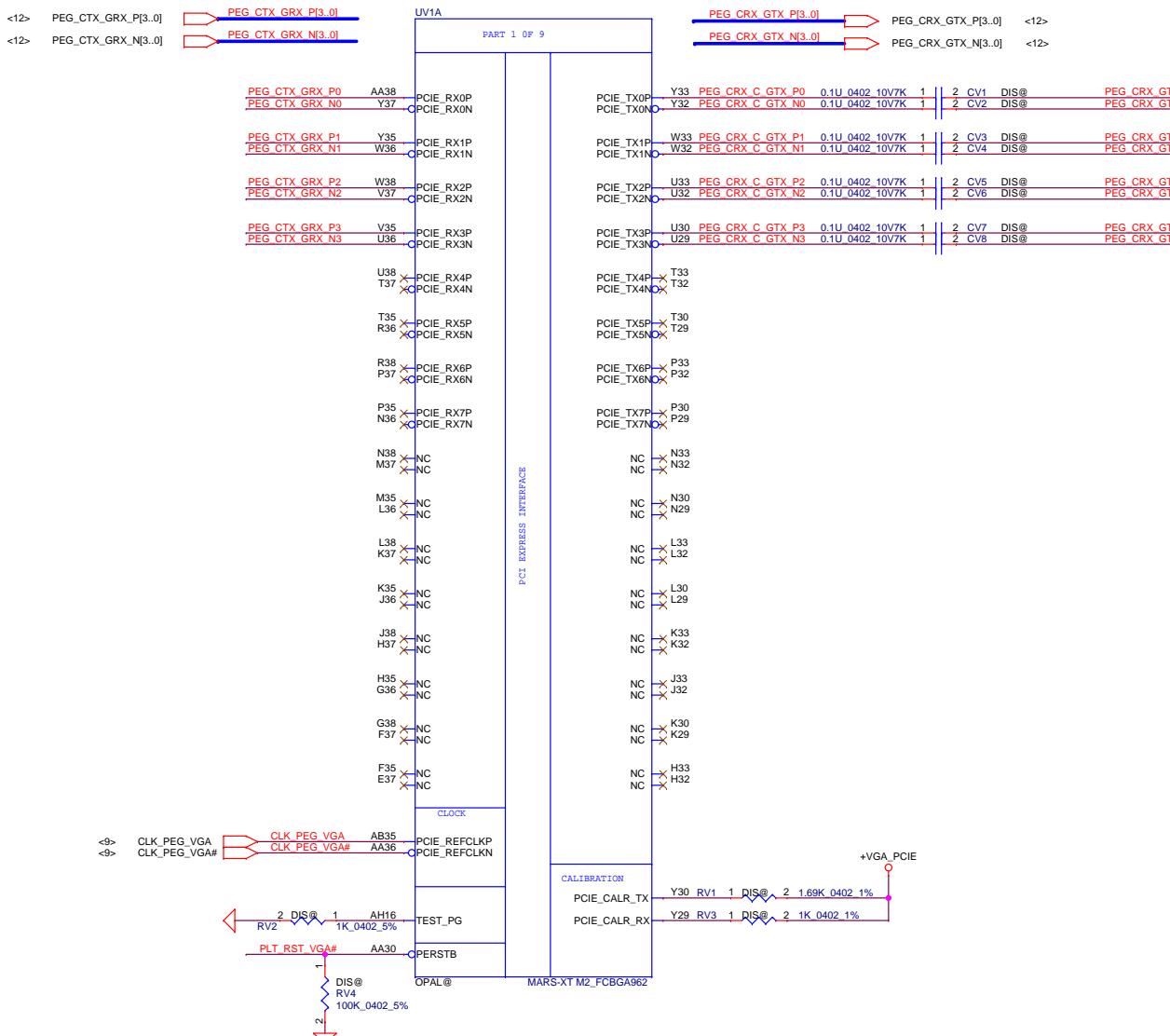
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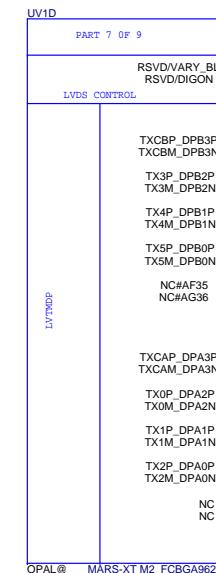


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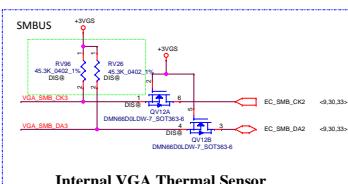
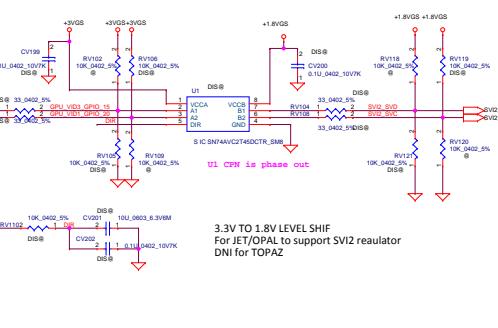
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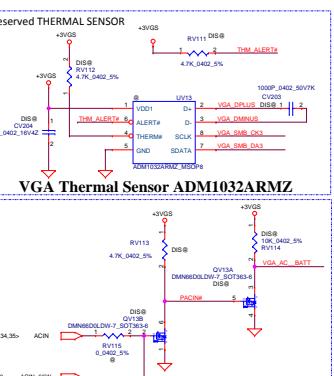
## LVDS Interface



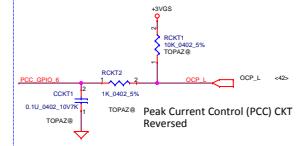
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2014/04/01	Deciphered Date	2015/04/30 <th>Title</th> <td>AMD_OPAL-XT_M2_PCIE/LVDS</td>	Title	AMD_OPAL-XT_M2_PCIE/LVDS
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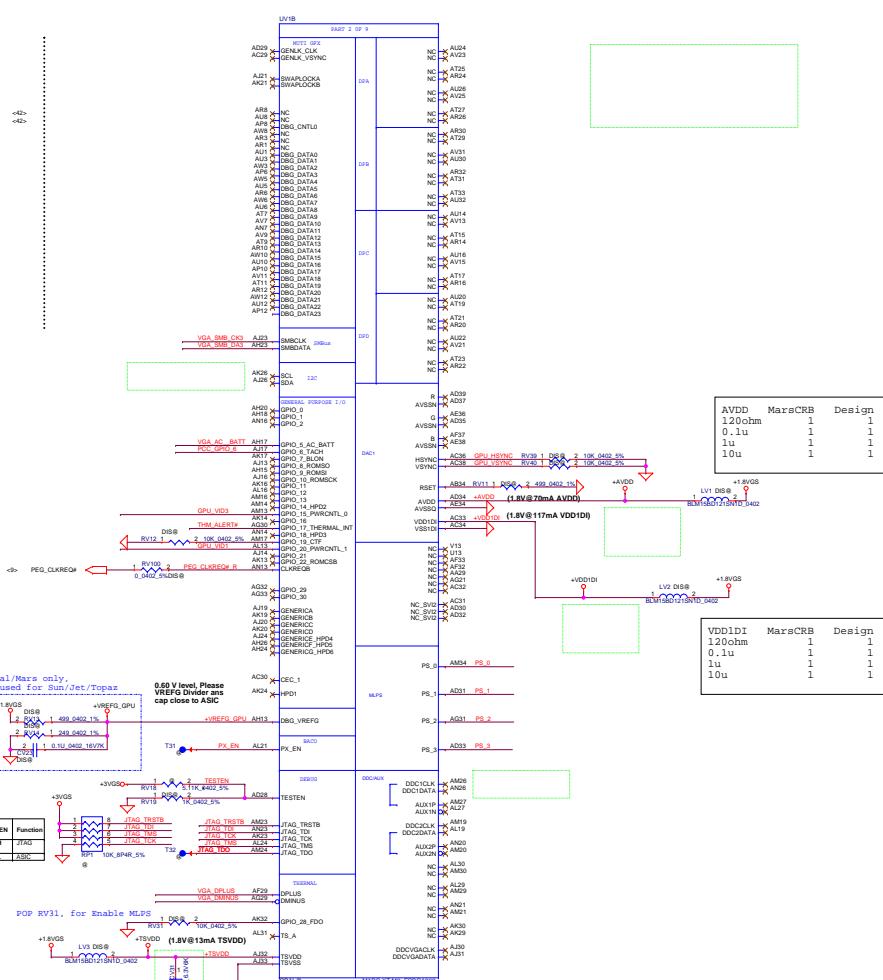
## Internal VGA Thermal Sensor



ADM1032ARMZ\_MSDP8



TSVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



Bits [3:1] Memory ID	P/N	Vendor	vendor part number	Size	RV20	RV21
(default)	111	SAMSUNG	K4W4G1646D-BC1A	4GB	4.75K	NC
	000	HYUNIX	H5TC4G63AFR-11C	4GB	NC	4.75
	001	Micron	MT41A16GM64A-992G-E	4GB	9.45K	NC

CONFIGURATION STRAPS		RECOMMENDED SETTINGS	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET		DO NOT INSTALL RESISTOR 1 = DO NOT INSTALL X = DESIGN DEPENDANT NA = NOT APPLICABLE	
STRAPS	MPLS	DESCRIPTION OF DEFAULT SETTINGS	Default Setting
TX_PWRs_ENB	P8,[14]	Transmitter Power Savings Enable Tx_PWRs output 1 = Tx power savings enabled 0 = Tx power savings disabled	1
TX_DEEMP_EN	P8,[15]	PCIe Transceiver De-emphasis Enable Tx_DEEMP output 1 = Tx de-emphasis enabled 0 = Tx de-emphasis disabled	0
BIF_GEN3_EN_A	P8,[11]	PCIe Gen3 Enable BIF_GEN3 output for Thamers/Seymour and should be strapped to 0 1 = GEN3 support or power-on 0 = GEN3 support or power-off	1
BIF_VGA_DIS	P8,[24]	VGA controller EVGA controller capability enabled 1 = EVGA controller 0 = VGA controller Note: ROM BIOS has a bug where it will always enable GPU	0
ROMIDFCG[2 0]	P8,[03..1]	Serial ROM type or Memory Address Block Select P8-[2 0]_0: Define memory parity size P8-[2 0]_1: Define memory parity type 100 = 512MB MCP30A (ST) 101 = 256MB MCP30A (ST) 101 = 256MB MCP30B (ST) 101 = 512MB MCP30B (ST) 101 = 1GB MCP30V01 (Cirrus) 101 = 1MB PLCC2LV01 (Cirrus)	000
BIOS_ROM_EN	P8,[23]	Enable external BIOS ROM device	0
AUD[0]	NA	00 - No audio function 01 - Audio for DP and HDMI if dangles are detected	XX
AUD[0 1]	NA	11 - Audio for DP and HDMI HDMI must only be enabled on systems that are designed to support it. It is the responsibility of the system designer to ensure that the system is enabled to support this feature.	
DAC_Dis	P8,[04]	Reserved for future ASIC	1
DO NOT INSTALL PULLUP PADS FOR THE RESERVED STRAPS BUT DO NOT INSTALL RESISTORS IF THESE GPIOS ARE USED, THEY MUST KEEP LOW AND NOT CONFLICT DURING RESET			
RESERVED	P8,[13]	Reserved	0
RESERVED	P8,[12]	Reserved	0
RESERVED	NA	Reserved	0
RESERVED	NA	Reserved (for Thamers/Whistler/Seymour only)	0
AUD_PORT_CONN_PINSTRAPS[0]	P8,[30]	STRAPS TO INDICATE THE NUMBER OF AUDIO PORTS SUPPORTED	XXX
AUD_PORT_CONN_PINSTRAPS[1]	P8,[34]	111 = 0 usable endpoints 110 = 1 usable endpoint 101 = 2 usable endpoints 100 = 3 usable endpoints 011 = 4 usable endpoints 010 = 5 usable endpoints 001 = 6 usable endpoints 000 = all endpoints are usable	
AUD_PORT_CONN_PINSTRAPS[2]	P8,[35]		

**MLPS Strap**

	Strap[4]	Strap[3:1]	Capacitor	R_pu	R_pd
PS_05[1]	1	1 1	NC	8.45K	2K
PS_15[1]	11	0 0 0	NC	NC	4.75K
PS_25[1]	11	0 0 0	NC	NC	4.75K
PS_36[1]	1 1	XXX	NC	X	X

Legend: NC = Not Connected, R = Resistor, C = Capacitor, GND = Ground, VDD = Power Supply, J = Jumper, SW = Switch, X = Open, +1.8VGS = +1.8V Ground Sense

Note: Memory RAM type conversion for the memory

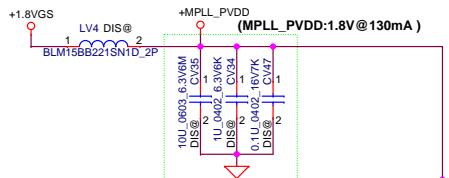
**Place CLOSE VGA CHIP**

**MLPS implementation:**  
Place MLPS circuit components as close to ASIC as possible  
Total DC resistance of trace between PS pin and C should be less than 2 ohm  
Total DC resistance of trace between C and ground should be less than 2 ohm  
Trace capacitance should be less than 10pF.

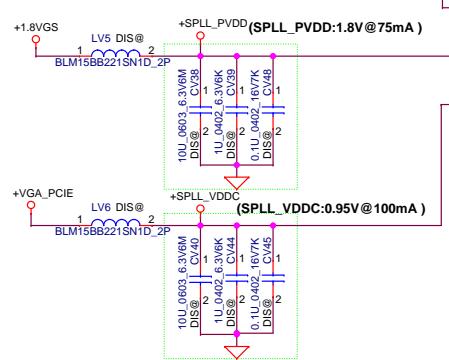
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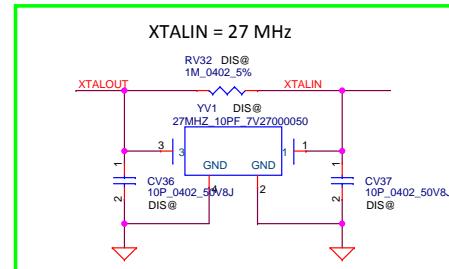
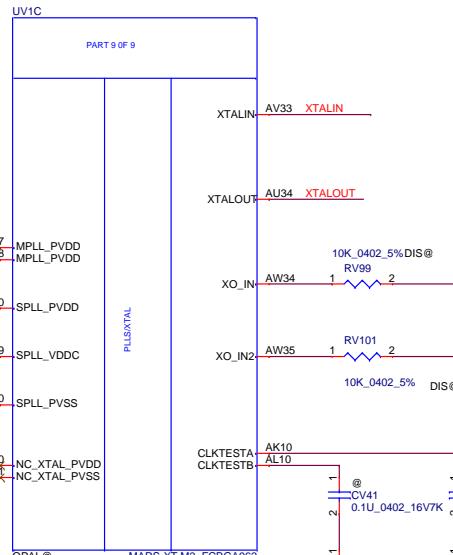
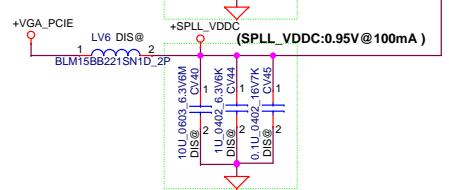
MPLL_PVDD	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



SPLL_PVDD	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1

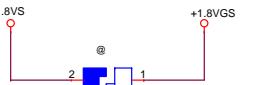


### +1.35VS\_VGA TO +1.35V\_MEM\_GFX



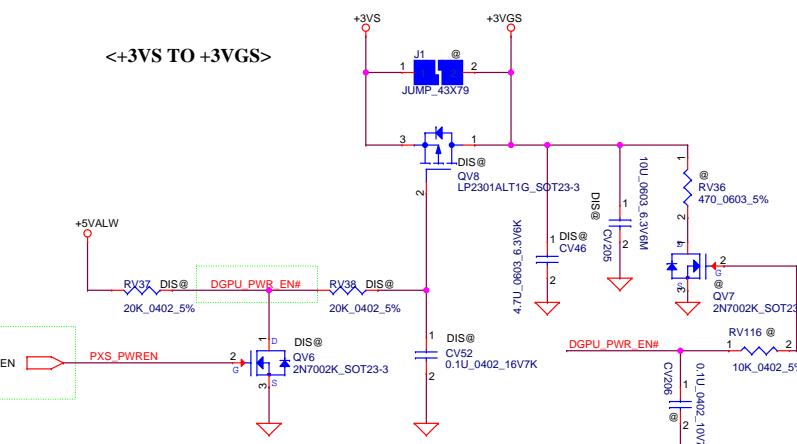
SHORT DEFAULT

### +1.8VS TO +1.8VGS

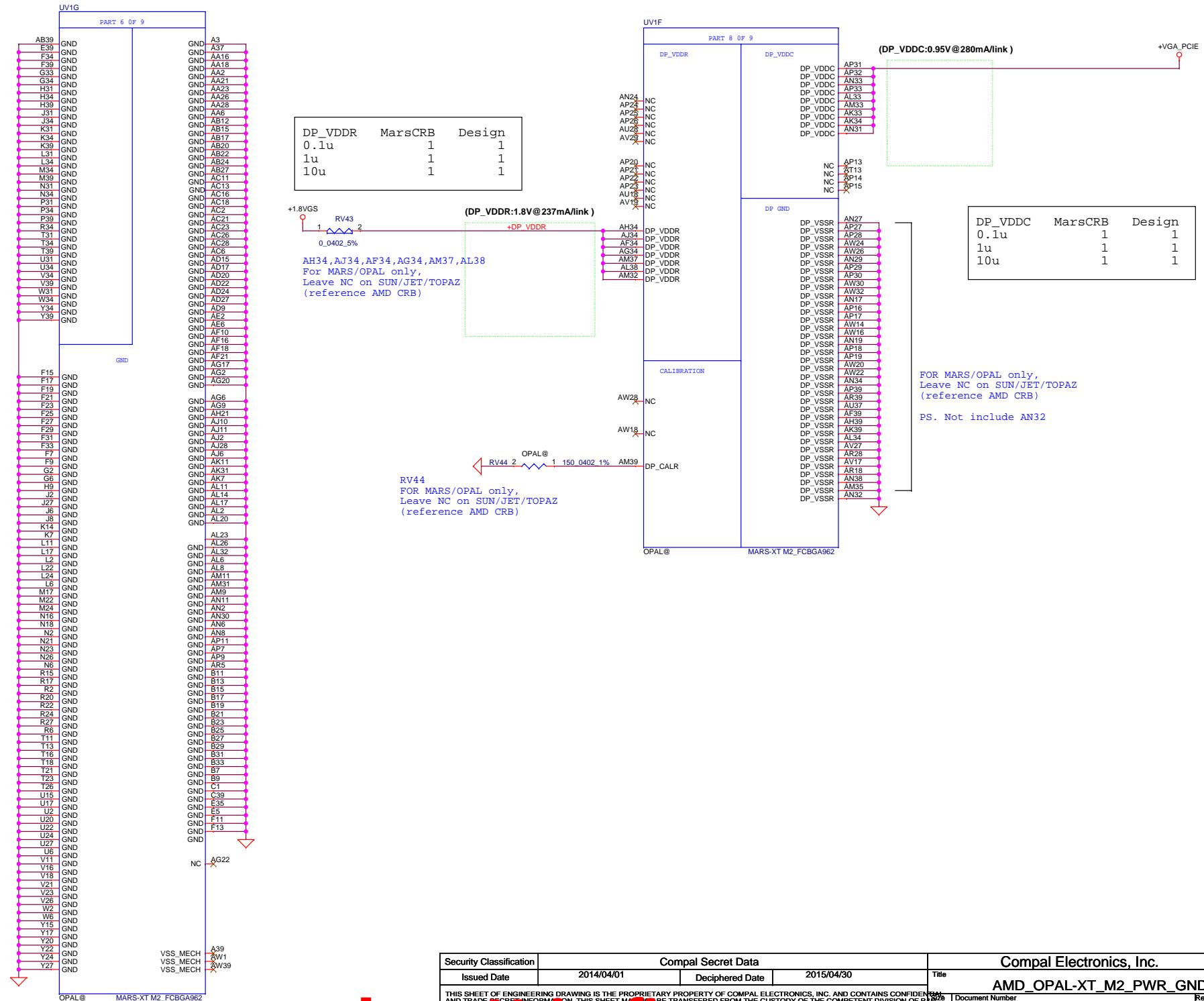


SHORT DEFAULT

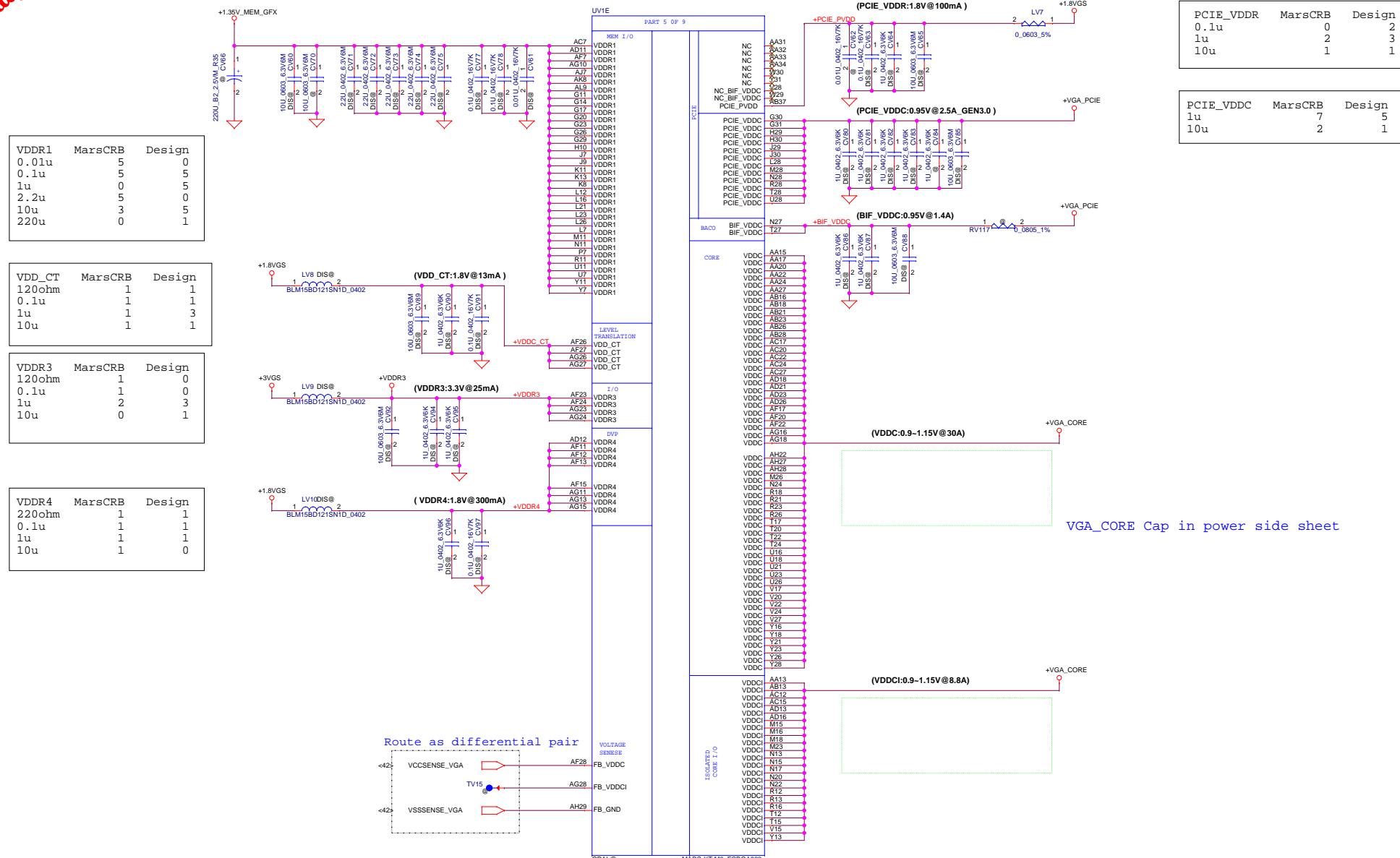
### <+3VS TO +3VGS>



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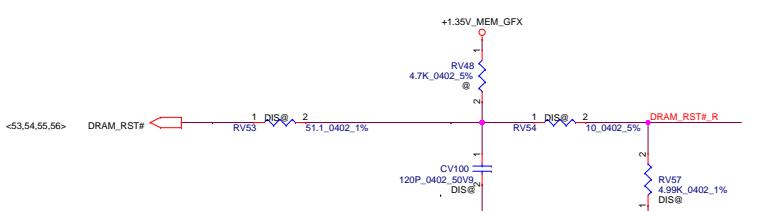
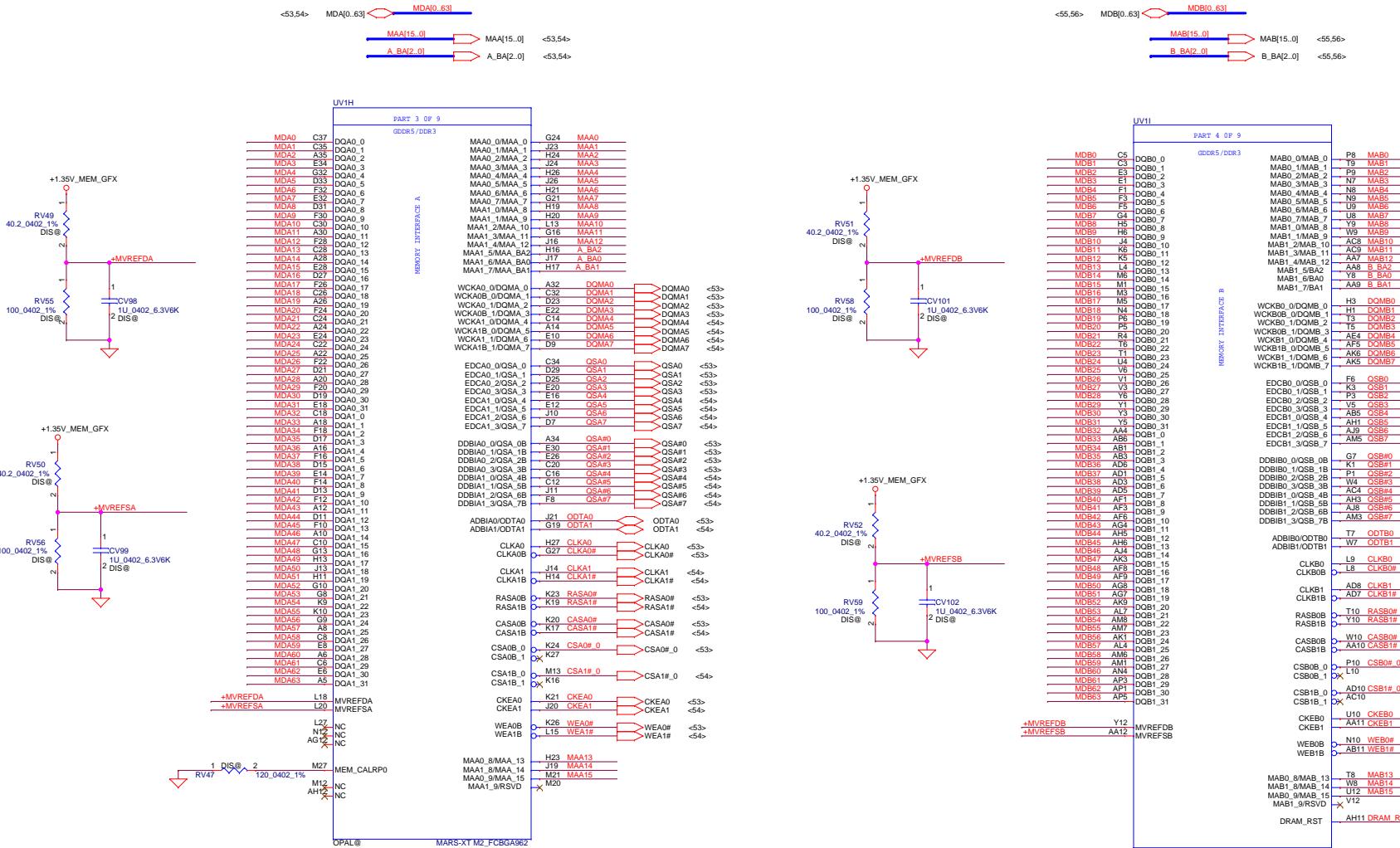


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Issued Date	Deciphered Date	2015/04/30	Title	AMD_OPAL-XT_M2_Power
2014/04/01			Document Number	LA-B015P
			Date	Wednesday, September 10, 2014
			Rev	0.1

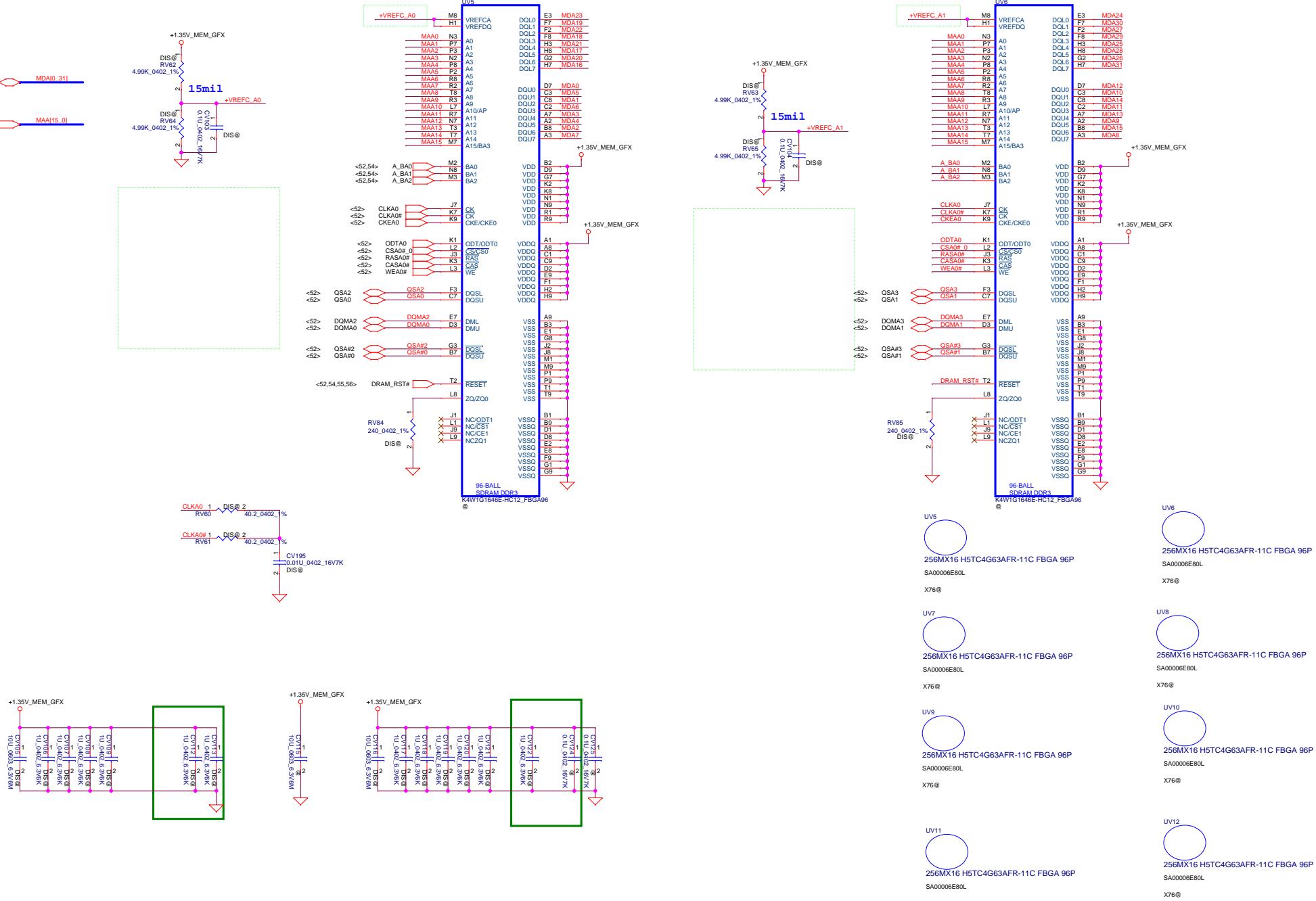
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`DRAM_RST#` is a daisy-chain net that connects to all VRAM

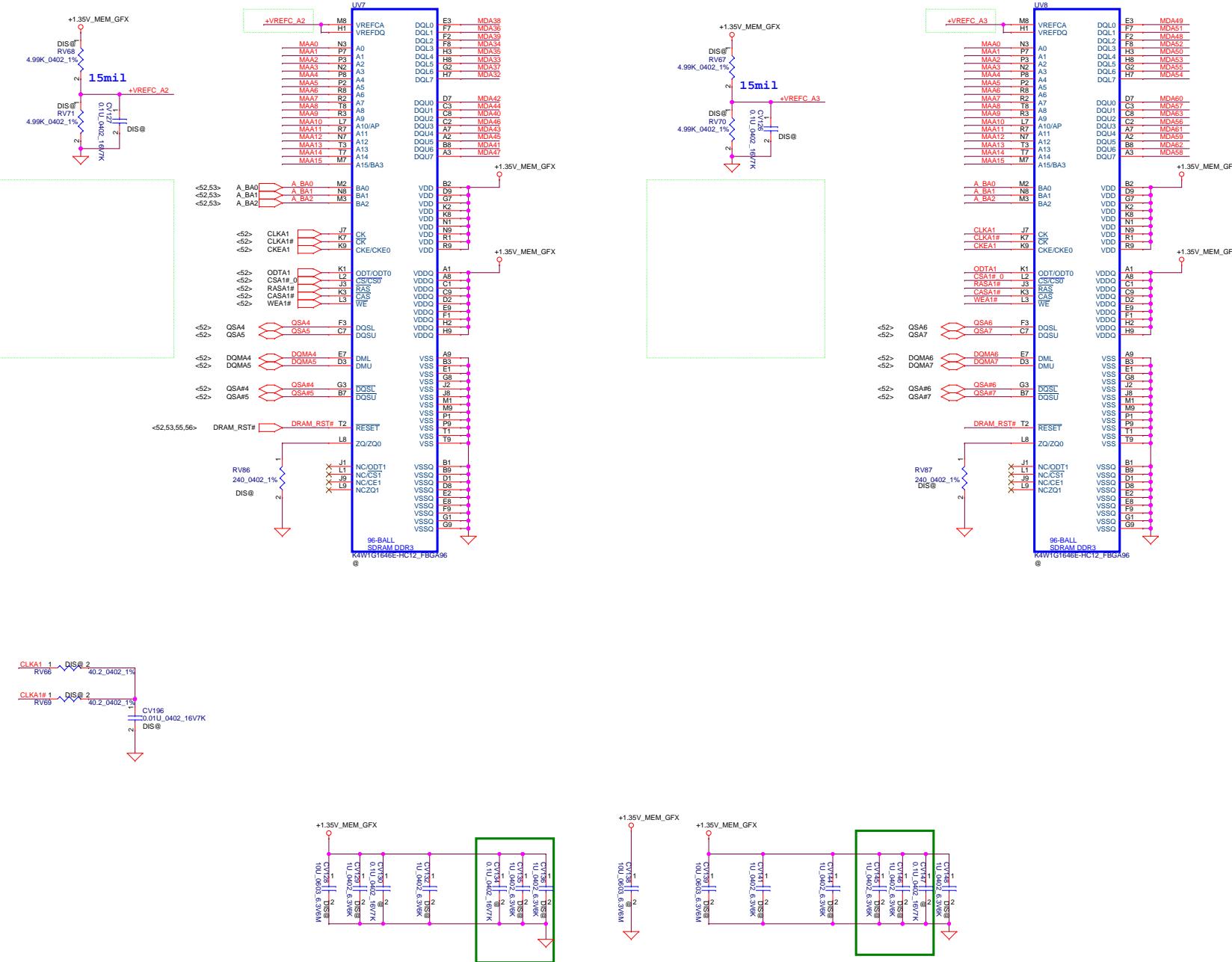
This basic topology should be used for DRAM\_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory .DRAM Load and board to pass Reset Signal Spec.  
Place all these components very close to GPU (Within

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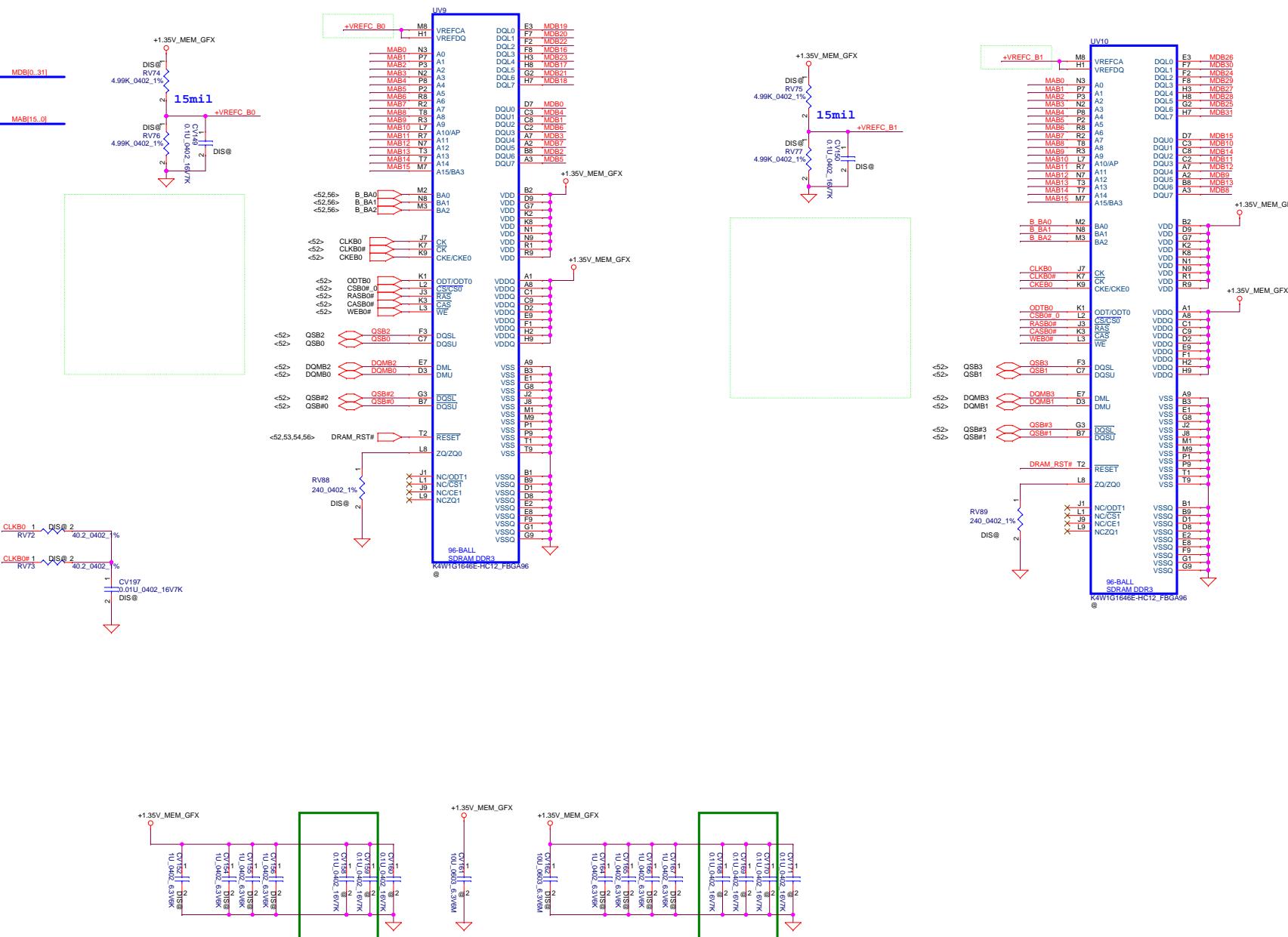
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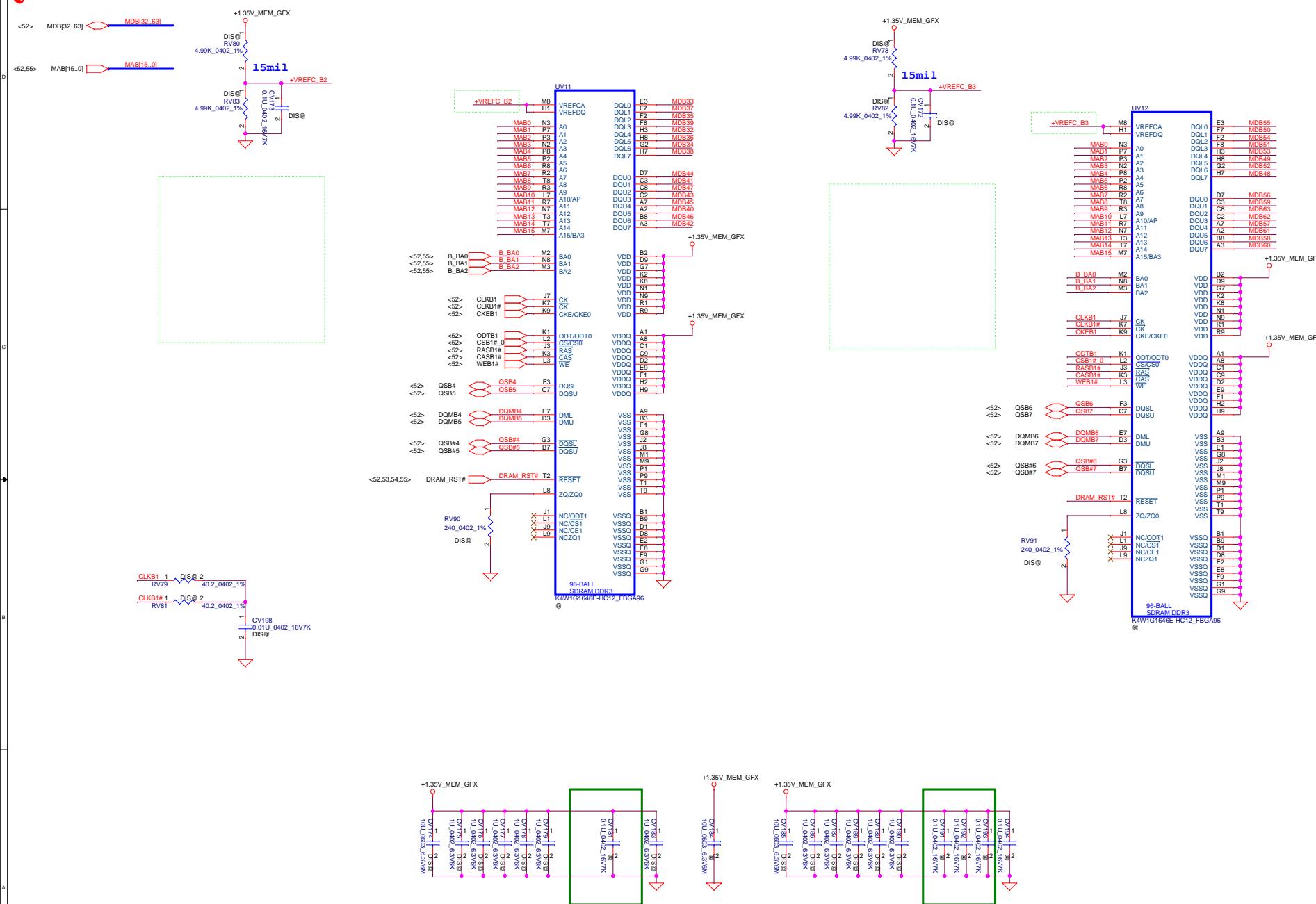
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