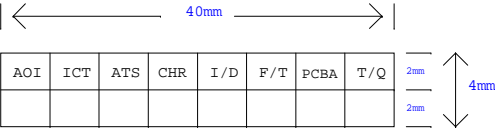


## Project : MB40IAX Schematics Rev : B1

### Intel Sandy Bridge CPU + Intel Cougar Point Chipset + ATi Whistler XT

Page	Content
01	Cover Page
02	System Block Diagram
03	Power Diagram
04	Power Sequence
05	GPIO & Power Consumption
06	Sandy Bridge_DMI,FDI,PEG
07	Sandy Bridge_DDR3
08	Sandy Bridge_Power
09	Sandy Bridge_GND
10	Sandy Bridge_Reserved
11	DDR3 SO-DIMM Channel A,B
12	Cougar Point_RTC,HDA,SATA
13	Cougar Point_PCIE,CLK,SMBus
14	Cougar Point_LVDS,CRT,Manage
15	Cougar Point_PCI,USB
16	Cougar Point_GPIO,MISC
17	Cougar Point_Power1
18	Cougar Point_Power2
19	Cougar Point_GND
20	LVDS/Webcam
21	CRT/HDMI
22	Mini Card/LED/LID/MMB/TP/HDD/ODD/IO Conn
23	Clock Gen (ICS9LRS3197)
24	USB 3.0 (ASMI042)
25	Audio Codec (ALC269)
26	Card Reader (RTS5159-GR)
27	EC (IT8518)/BIOS/KBC
28	Power Switch/Hole/FAN
29	DC In & Charger (OZ8618)
30	+VCC_Core (ISL95831HRTZ)
31	+VGFX_Core (ISL95831HRTZ)
32	+1.0/0.75/1.8/1.8V_DGPU/3VA
33	+5VA/+1.05V_VCCP(OZ815)
34	+1.5VS (OZ8111)/+0.85V
35	+VGA_Core (OZ8117)
36	VGA PCIE/LVDS
37	VGA I/O
38	VGA MEM_Interface
39	VGA Power 1
40	VGA Power 2
41	VGA GND/Straps
42	VGA DDR3_MEM_A
43	VGA DDR3_MEM_B
44	Change Notes

Phase	Revision History	
A0	06/30/2010	Initial REV.A
A1	08/13/2010	Release REV.A1
A2	09/13/2010	Release REV.A2
B0	10/20/2010	Release REV.B
B1	11/08/2010	Release REV.B1
C	??/??/2010	Release REV.C
10	??/??/2010	Release REV.10

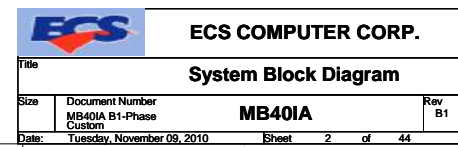


PCB  
 PCB  
 37GMB4100-B1  
 MB40IA MB Ver:B1  
 P/N:37GMB4100-B1  
 PCB M/B MB40IA1 R:B1 201.9\*178.0\*1.2 6L

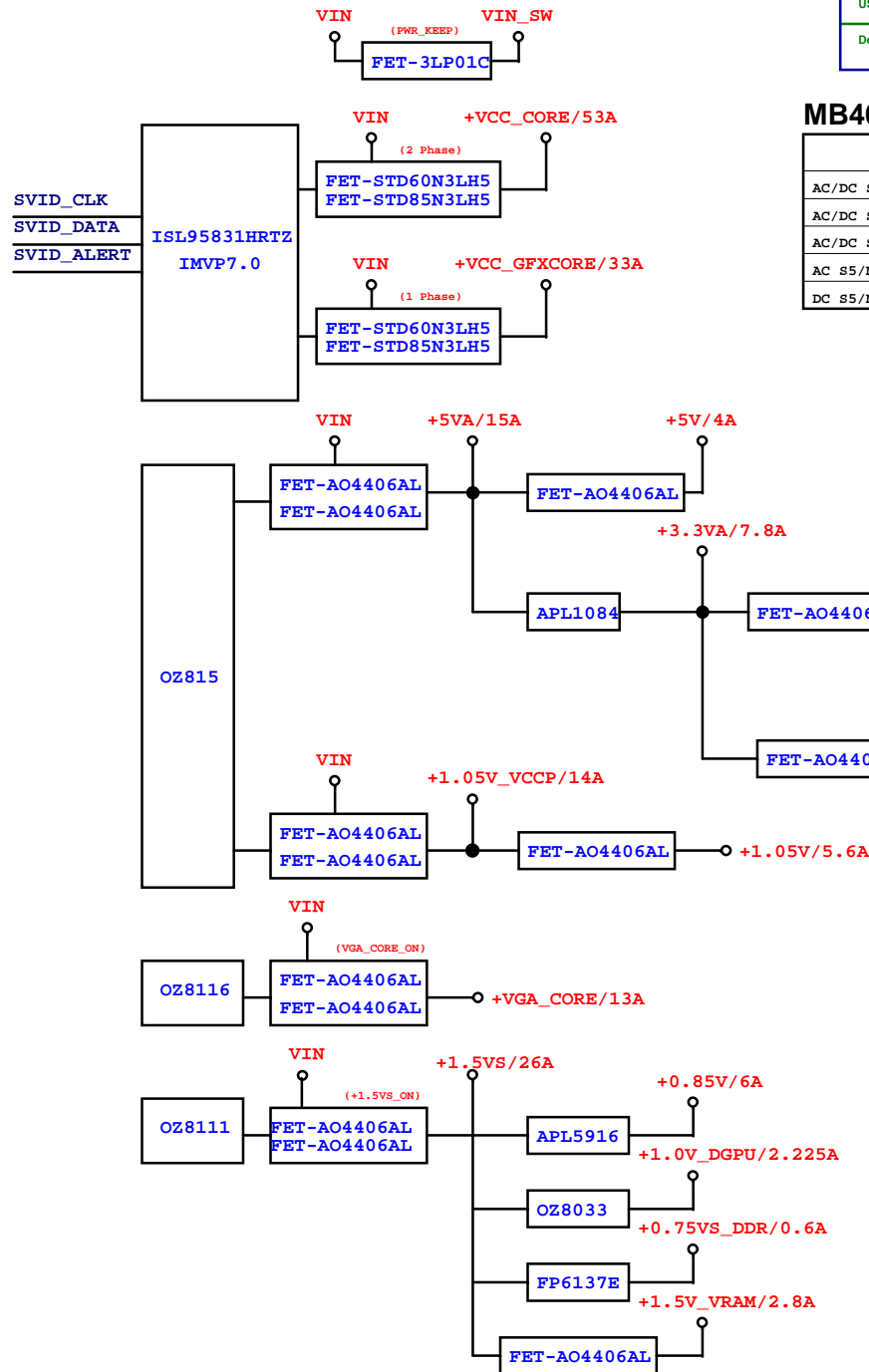
### MB40IA Rev. P/N List :

Phase Revision	PCB P/N	PCBA P/N	PCBA P/N
Initial REV.A0	37GMB4100-A0	82GMB4100-A0	None
Release REV.A1	37GMB4100-A1	82GMB4B00-A1	82GMB4110-A1
Release REV.A2	37GMB4100-A2	82GMB4C00-A2	82GMB4D00-A2
Release REV.B0	37GMB4100-B0	82GXXXXXX-B0	82GMB4D00-B0
Release REV.B1	37GMB4100-B1	82GXXXXXX-B1	82GXXXXXX-B1
Release REV.C	37GXXXXXX-C0	82GXXXXXX-C0	82GXXXXXX-C0
Release REV.10	37GXXXXXX-10	82GXXXXXX-10	82GXXXXXX-10
		Whistler ?G MB40IA2(Haier)	WhistlerPro ?G MB40IA3(Hasee)

www.vinafix.vn



# Power Block Diagram



USB Port Devices Table

USB Ports	USBP0 USBN0	USBP1 USBN1	USBP2 USBN2	USBP3 USBN3	USBP4 USBN4	USBP5 USBN5	USBP6 USBN6	USBP7 USBN7	USBP8 USBN8	USBP9 USBN9	USBP10 USBN10	USBP11 USBN11	USBP12 USBN12	USBP13 USBN13
Devices	Enhance USB	USB Port	None	WLAN	None	Web Camera	Disable	Disable	Finger Print	USB Port	None	Enhance USB	None	Card Reader

MB401A M/B Power Rail State :

	+*V_LDO	+*VA	+*V	+*VS	CLK
AC/DC S0/Moff (Full On)	ON	ON	ON	ON	ON
AC/DC S3/Moff (STR)	ON	ON	ON	OFF	Only MCH BCLK
AC/DC S4/Moff (STD)	ON	ON	OFF	OFF	OFF
AC S5/Moff (Soft Off)	ON	ON	OFF	OFF	OFF
DC S5/Moff (Soft Off)	ON	OFF	OFF	OFF	OFF

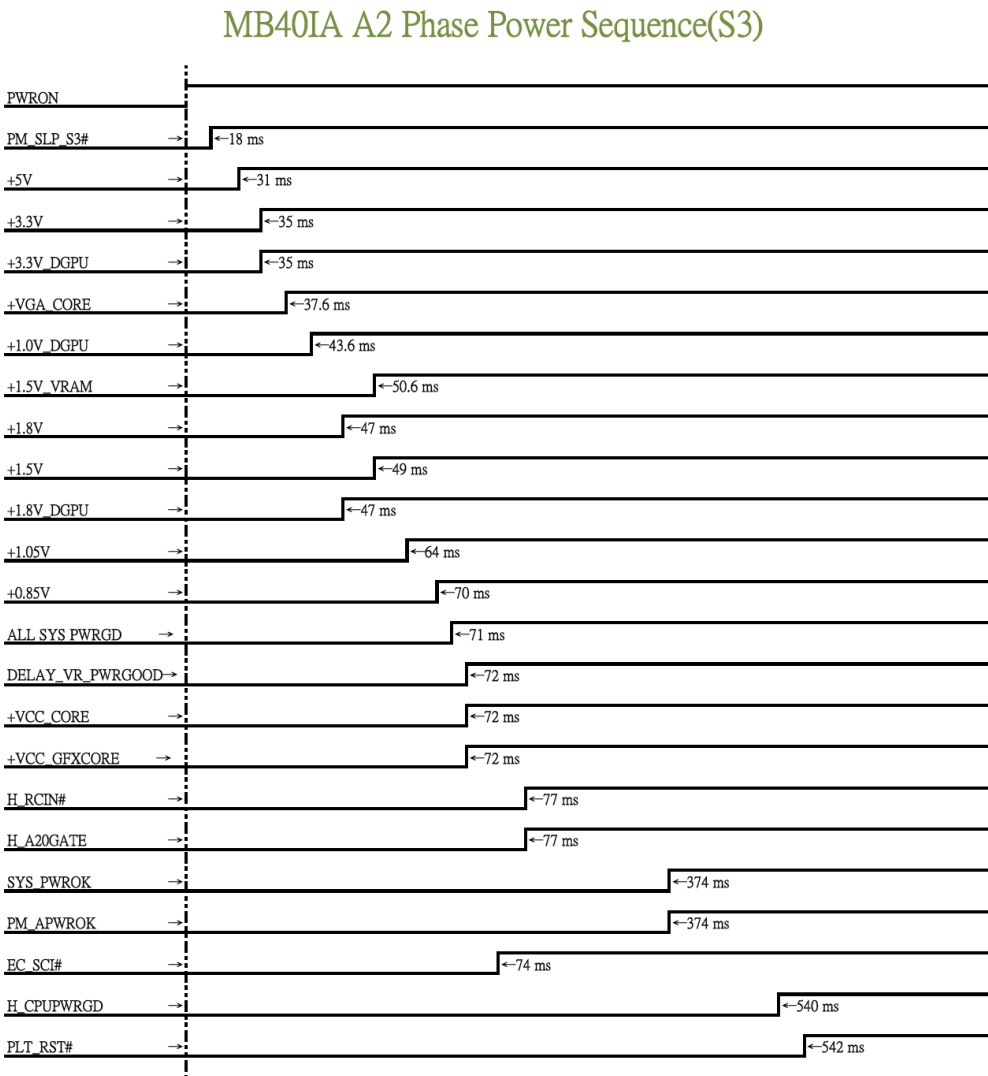
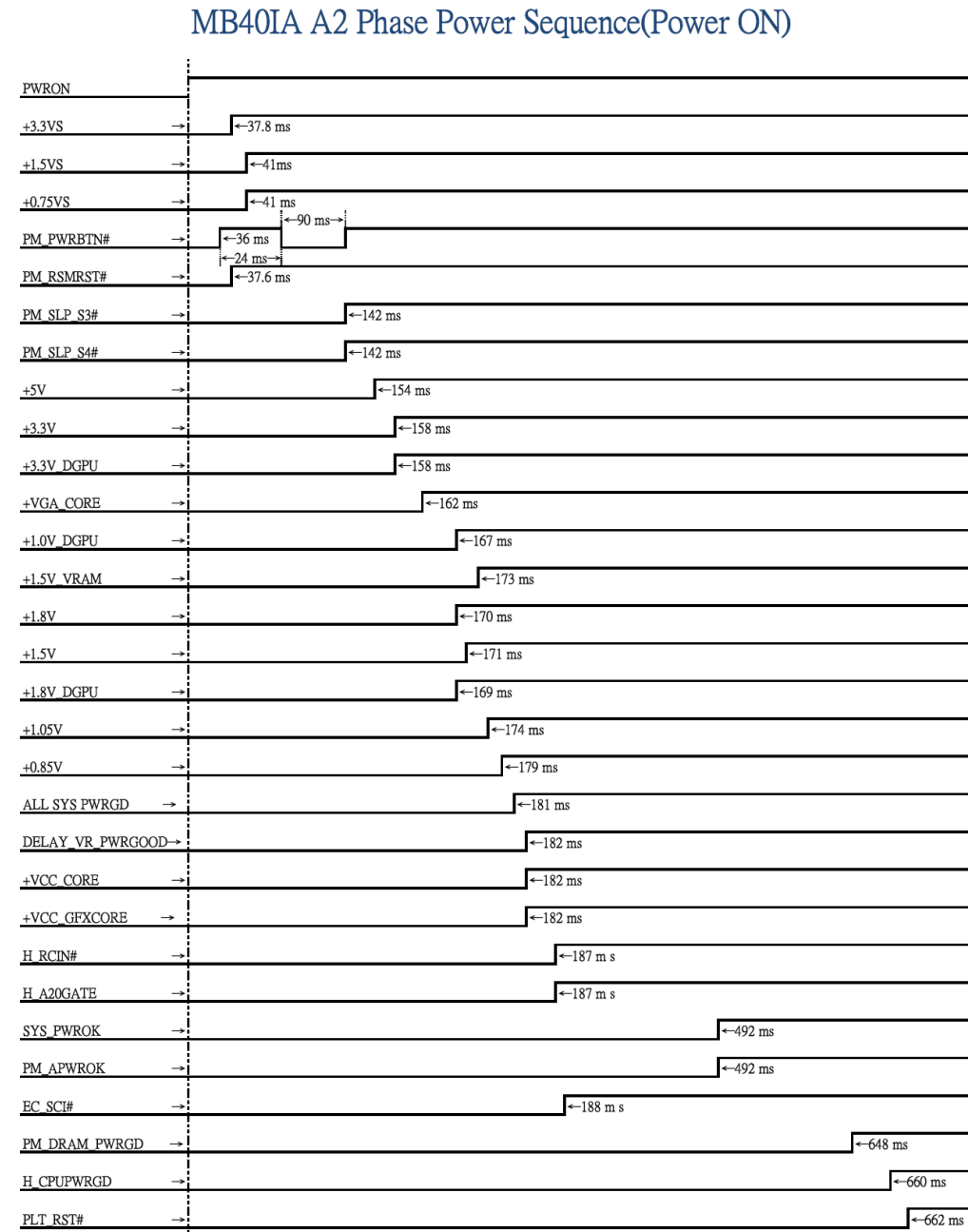
System Power Rail

Voltage Name	Control Pin	S0	S1	S3	S4	S5
+V GFX_CORE	GFX_IMON	ON	ON	OFF	OFF	OFF
+VCC_CORE	+VCC_CORE_ON	ON	ON	OFF	OFF	OFF
+V1.05S	+V1.5S_ON	ON	ON	OFF	OFF	OFF
+V1.5S	+V1.5S_ON	ON	ON	OFF	OFF	OFF
+V3.3S	+V3.3S_ON	ON	ON	OFF	OFF	OFF
+V5S	+V5S_ON	ON	ON	OFF	OFF	OFF
+V1.1S_VTT	+V5S	ON	ON	OFF	OFF	OFF
+V1.8S	+V5S	ON	ON	OFF	OFF	OFF
+V1.1S	+V5S	ON	ON	OFF	OFF	OFF
+V0.75DDR	+V1.5	ON	ON	ON	OFF	OFF
+V1.5	+V1.5_ON	ON	ON	ON	OFF	OFF
+V3.3	+V3.3_ON	ON	ON	ON	OFF	OFF
+V5	+V5_ON	ON	ON	ON	OFF	OFF
VIN_SW	PWR_KEEP	ON	ON	ON	OFF	OFF
+V3.3_AUX	AC:follow VIN up	ON	ON	ON	ON	ON
+V5_AUX	DC:AUX_ON	ON	ON	ON	OFF	OFF
	AC:follow VIN up	ON	ON	ON	ON	ON
	DC:AUX_ON	ON	ON	ON	OFF	OFF

CPU Huron River Power Rail		Laptop Mode				
		S0	S1	S3	S4	S5
VCC	+VCC CORE	ON	ON	OFF	OFF	OFF
VTT	+V1.1S	ON	ON	OFF	OFF	OFF
VAXG	+VCC CORE	ON	ON	OFF	OFF	OFF
VCCPLL1	+V1.8S	ON	ON	OFF	OFF	OFF
VDDQ	+V1.5S	ON	ON	OFF	OFF	OFF

SB Ibex Peak Power Rail		Laptop Mode				
		S0	S1	S3	S4	S5
VCCACLK	+V1.1S	ON	ON	OFF	OFF	OFF
VCCCORE	+V1.1S	ON	ON	OFF	OFF	OFF
VCCAPLLEXP	+V1.1S	ON	ON	OFF	OFF	OFF
VCCIO	+V1.1S	ON	ON	OFF	OFF	OFF
VCC3_3	+V3.3S	ON	ON	OFF	OFF	OFF
VCCFDIPLL	+V1.1S	ON	ON	OFF	OFF	OFF
VCCVRM	+V1.8S	ON	ON	OFF	OFF	OFF
VCCPNAND	+V1.8S	ON	ON	OFF	OFF	OFF
VCCDMI	+V1.1S_VTT	ON	ON	OFF	OFF	OFF
VCCALVDS	+V3.3S	ON	ON	OFF	OFF	OFF
VCCCTX_LVDS	+V1.8S	ON	ON	OFF	OFF	OFF
VCCADAC	+V3.3S	ON	ON	OFF	OFF	OFF
V5REF	+V5S	ON	ON	OFF	OFF	OFF
VCCADPLL	+V1.1S	ON	ON	OFF	OFF	OFF
VCCSATAPLL	+V1.1S	ON	ON	OFF	OFF	OFF
V_CPU_IO	+V1.1S	ON	ON	OFF	OFF	OFF
VCCADPLLA	+V1.1S	ON	ON	OFF	OFF	OFF
VCCLAN	+V1.1S	ON	ON	OFF	OFF	OFF
VCCSUSHDA	+V3.3A	ON	ON	ON	ON	ON
VCCSUS3_3	+V3.3A	ON	ON	ON	ON	ON
VCCRTC	+V3A	ON	ON	ON	ON	ON
V5REF_SUS	+V5A	ON	ON	ON	ON	ON

System Power On Sequence



PCH GPIO	
GPIO0	S_GPIO
GPIO1	SMC_RUNTIME_SCI#
GPIO2	MPC_PWR_CTRL#
GPIO3	SATA_ODD_DA#
GPIO4	EXTTS_SNI_DRV0_PCH
GPIO5	EXTTS_SNI_DRV1_PCH
GPIO6	USB_SMI
GPIO7	PCH_TACH3
GPIO8	ICC_EN#
GPIO9	USB_OC#_10_11
GPIO10	USB_OC#_12_13
GPIO11	PCH_GPIO11
GPIO12	PCH_GPIO12
GPIO13	NC
GPIO14	USB_OC#_13_14
GPIO15	HOST_ALERT#1
GPIO16	SATA_DET#4
GPIO17	PCH_TACH0
GPIO18	CLK_PCIE_LAN_REQ#_R
GPIO19	BBS_BIT0
GPIO20	NC
GPIO21	SATA_DET0#
GPIO22	BIOS_REC
GPIO23	NC
GPIO24	HOST_ALERT#2
GPIO25	NC
GPIO26	CLK_USB_OE#_R
GPIO27	PCH_GPIO27
GPIO28	PLL_ODVR_EN
GPIO29	PM_SLP_LAN#
GPIO30	SUS_PWR_ACK_R
GPIO31	AC_PRESENT
GPIO32	PM_CLKRUN#
GPIO33	PORST#_PCH
GPIO34	PX_MODE
GPIO35	PLTRST#_PCH
GPIO36	PCH_GPIO36
GPIO37	FDI_OVRVLTG
GPIO38	MFG_MODE
GPIO39	GFX_CRB_DET
GPIO40	USB_OC#_2_3
GPIO41	USB_OC#_4_5
GPIO42	USB_OC#_6_7
GPIO43	USB_OC#_8_9
GPIO44	NC
GPIO45	NC
GPIO46	NC
GPIO47	PEG_CLKREQ#
GPIO48	TEST_SET_UP
GPIO49	PCH_GPIO49
GPIO50	DGPU_HOLD_RST
GPIO51	BBS_BIT1
GPIO52	PCI_REQ#2
GPIO53	NC
GPIO54	PCI_REQ#3
GPIO55	STP_A16OVR
GPIO56	NC
GPIO57	TEST_DET
GPIO58	SMB1_CLK_EC
GPIO59	USB_OC#_0_1
GPIO60	RST_GATE
GPIO61	NC
GPIO62	NC
GPIO63	NC
GPIO64	NC
GPIO65	USB_48M_P
GPIO66	LAN25M_P
GPIO67	SEL24_48M_P
GPIO68	10K to +3.3V
GPIO69	1.5K to GND
GPIO70	1.5K to +3.3V
GPIO71	1.5K to +3.3V
GPIO72	PM_BATLOW#
GPIO73	CLK_MINI1_OE#_R
GPIO74	PCH_GPIO74
GPIO75	SMB1_DAT_EC

ITE8518 GPIO Pin Definition list	
GPA0	BTL_BEEP
GPA1	EC_BL_PWM
GPA2	WLAN_ON
GPA3	WEBCAM_EN
GPA4	RF_LED
GPA5	+0.85V_ON
GPA6	RECOVERY
GPA7	BT_EN#
GPB0	SENBAT_V
GPB1	COLOR_ENGINE_EN
GPB2	+VGA_BACO
GPB3	SMBCLK_EC0
GPB4	SMBDAT_EC0
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	OPTION2
GPC0	+1.8V_ON
GPC1	SMBCLK_EC1
GPC2	SMBDAT_EC1
GPC3	SAFETY
GPC4	+3.3V_ON
GPC5	+5V_ON
GPC6	+1.05V_VCCP_ON
GPC7	PM_PWRBTN#
GPD0	AC_IN
GPD1	OPTION1
GPD2	BUF_PLT_RST#
GPD3	EC_SCI#
GPD4	SATA_ODD_PWRGT_EC
	+1.8V_DGPU_ON
GPD5	AC_PRESENT
GPD6	+1.5VS_ON
GPD7	+1.2V_ON
GPE0	PM_RSMRST#
GPE1	FNOPTION
GPE2	PM_APWROK
GPE3	+VGA_ON
GPE4	PWRON
GPE5	OPTION3
GPE6	SATA_LED1#
GPE7	MUTE_AMP#
GPF0	EC_PROCHOT
GPF1	CHG_R_LED
GPF2	CHG_B_LED
GPF3	PWR_LED
GPF4	TP_CLK
GPF5	TP_DATA
GPF6	EC_PECI
GPF7	PM_SYSRST#
GPH0	PWR_KEEP
GPH1	ME_LOCK
GPH2	USB0_EN#
GPH3	PCH_SPI_CS#
GPH4	PCH_SPI_CLK
GPH5	PCH_SPI_SO
GPH6	PCH_SPI_SI
GPG0	EC_BL_EN
GPG1	+3.3VS_ON
GPG2	FLFRAME#
CPG6	LID#
ADC0/GPI0	BATT_TEMP
ADC1/GPI1	ADAPTOR_I
ADC2/GPI2	BAT_I
ADC3/GPI3	BAT_V
ADC4/GPI4	NC
ADC5/GPI5	PM_SLP_S4#
ADC6/GPI6	PM_SLP_S3#
	SUB_PWR_ACK
ADC7/GPI7	SATA_ODD_DA#_EC
	PX_MODE

ITE8518 GPIO Pin Definition list	
DAC0/GPV0	Past-charge-EN
DAC0/GPV1	CHG_ON
DAC0/GPV3	FAN_CTRL0
DAC0/GPV3	CHG_I
DAC0/GPV4	MMB_RESET#
DAC0/GPV5	SET_V

ITE8518 KB Matrk interface	
KS10/STB#	KB_SIN0
KS11/AFD#	KB_SIN1
KS12/INIT#	KB_SIN2
KS13SLIN#	KB_SIN3
KS14	KB_SIN4
KS15	KB_SIN5
KS16	KB_SIN6
KS17	KB_SIN7
KS00/PD0	KB_SOUT0
KS01/PD1	KB_SOUT1
KS02/PD2	KB_SOUT2
KS03/PD3	KB_SOUT3
KS04/PD4	KB_SOUT4
KS05/PD5	KB_SOUT5
KS06/PD6	KB_SOUT6
KS07/PD7	KB_SOUT7
KS08/ACK#	KB_SOUT8
KS09/BUSY	KB_SOUT9
KS10/PE	KB_SOUT10
KS011/ERR#	KB_SOUT11
KS012/SLCT	KB_SOUT12
KS013	KB_SOUT13
KS014	KB_SOUT14
KS015	KB_SOUT15

ITE8518 SPI Flash ROM interface	
FSSC0#//GPG2	FLFRAME#
FSCE#	EC_SPI_CS#
FMOSI	EC_SPI_SI
FMOSO	EC_SPI_SO
DSR0#/GPG6	LID#
FSCK	EC_SPI_CLK
SCI#/GPG0	EC_BL_EN

ITE8518 System & LPC Bus	
LAD0	LPC_AD0
LAD1	LPC_AD1
LAD2	LPC_AD2
LAD3	LPC_AD3
SERIRQ	INT_SERIRQ
LFRAME#	LPC_FRAME#
LPCCCLK	CLK_PCI_KBC
WRST#	LRST1#

ITE8518 Clock	
CLK32K	EC32KI
CK32KE	EC32KO

ITE8518 Power	
VSTBY0	+3.3VA
VSTBY1	+3.3VA
VSTBY2	+3.3VA
VSTBY3	+3.3VA
VSTBY4	+3.3VA
VSTBY5	+3.3VA
VBAT	+3.3VA_RTC
AVCC	+3.3VA
VCC	+3.3V

Gantiga TDP				
	CPU Socket P	GMCH GFX Freq/Core Volt	Memory	TDP
Gantiga	Penryn SV/FSB800	800MHZ/1.05V	DDR3-1066/ 2 CH	12.0W
Gantiga	Penryn SV/FSB800	800MHZ/1.05V	DDR3-1066/ 2 CH	12.0W
Gantiga	Penryn LV/FSB800	800MHZ/1.05V	DDR3-800/ 2 CH	10.5W
Gantiga	Penryn ULV/FSB800	800MHZ/1.05V	DDR3-800/ 2 CH	9.5W

Sandy Bridge CPU			
IMVP-7.0			
Voltage (V)	Current (mA)	Measure	Watt
+VCC_CORE	36000		
+VCC_GFXCORE	33000		
+1.05V_VCCP	8500		
+0.85V	6000		
+1.5VS	3000		
+1.8V	1200		

ITE8518 GND	
AVSS	GND
VSS0	GND
VSS1	GND
VSS2	GND
VSS3	GND
VSS4	GND
VSS5	GND
VSS6	GND

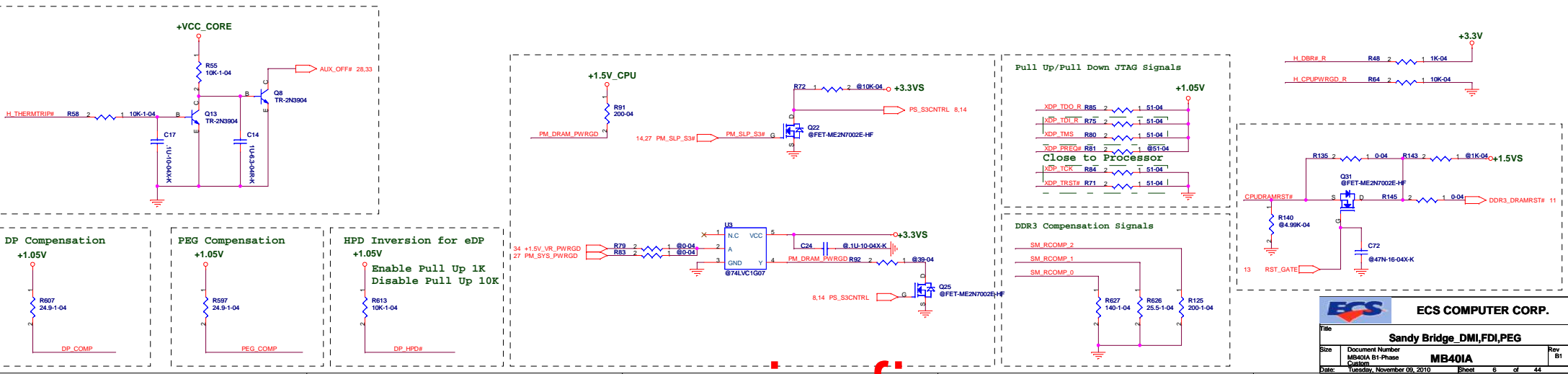
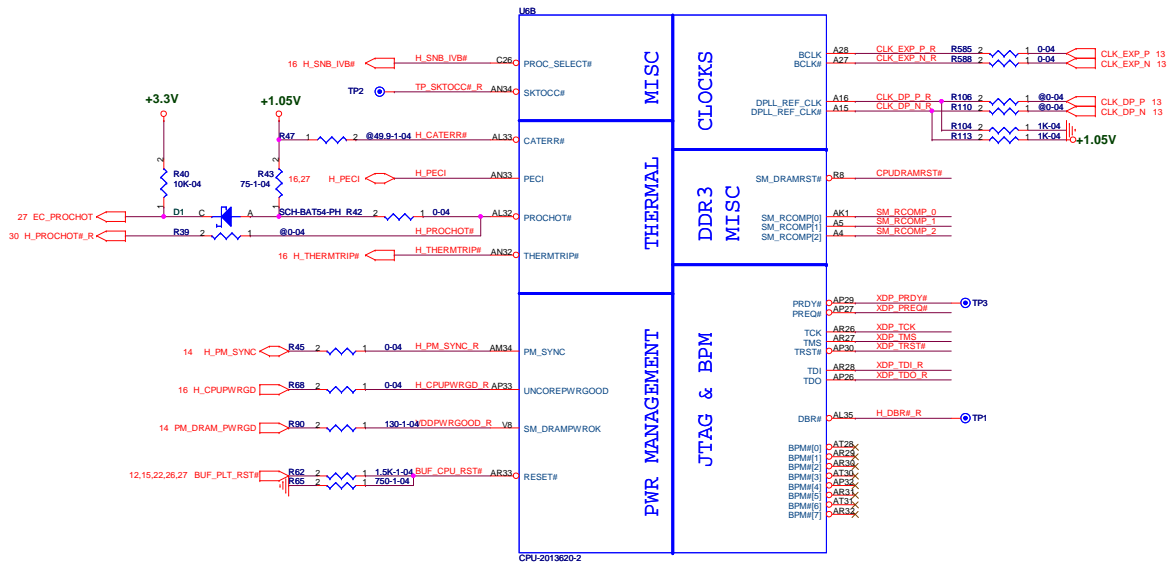
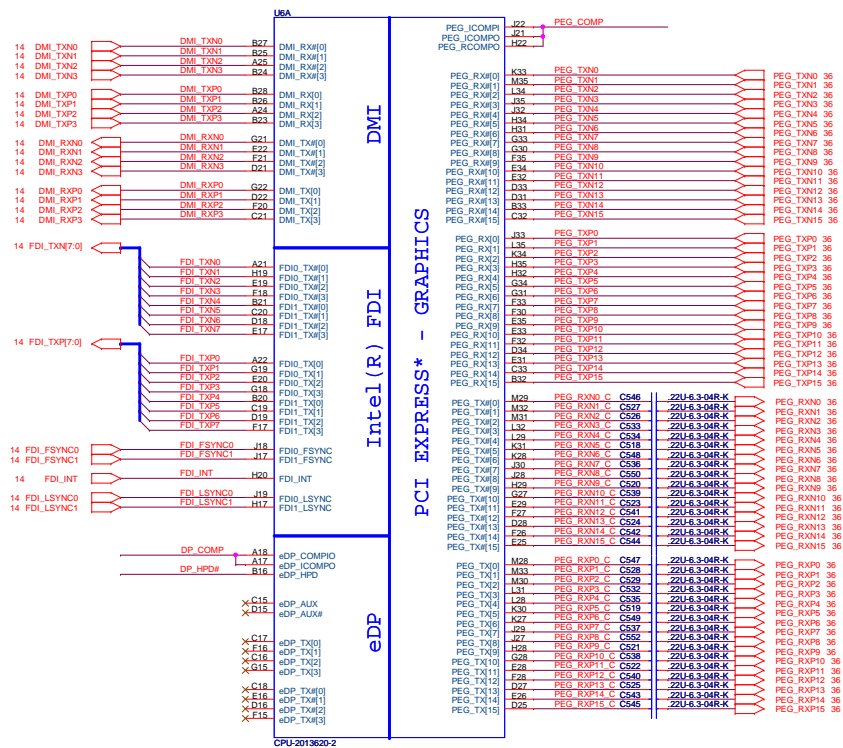
Cantiga			
VCC	ICC (mA)	W	TEMP (°C)
+3.3VS	269	0.887	105
+1.8V	192	0.345	
+1.5VS	76	1.14	
+1.05VS	6013	6.313	
GFX_CORE	6326	6.642	

PCH			
VCC	ICC (mA)	mW	TEMP (°C)
+5V	2	10	70
+5VS	2	10	
+3.3VA	162	534.6	
+3.3VS	320	1056	
+1.5VS	2220	3330	
+1.05V	1636	1717.8	

ITE8518			
VCC	ICC (mA)	mW	TEMP (°C)
+3.3VA	100	330	70

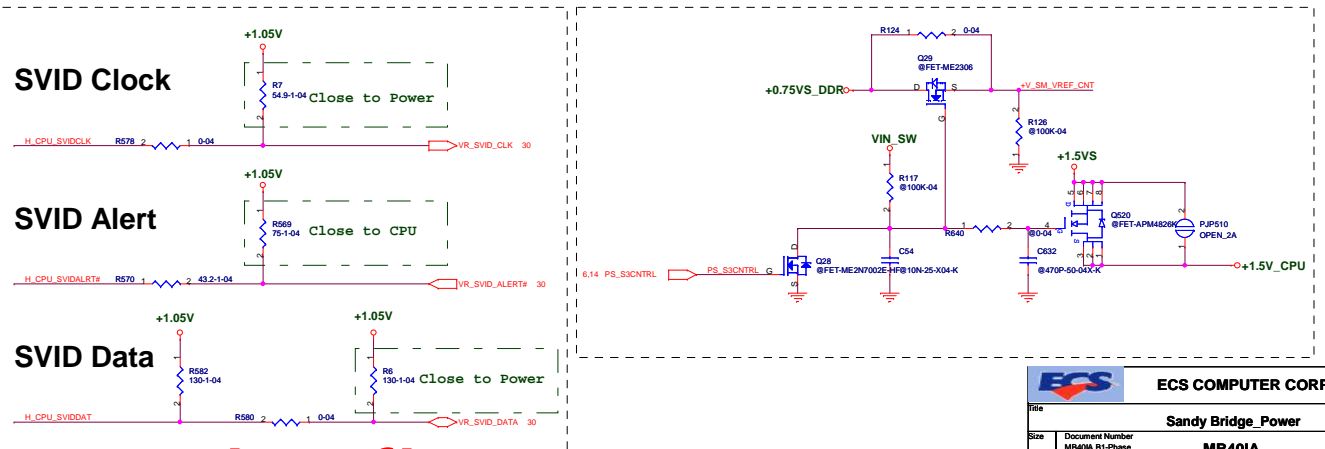
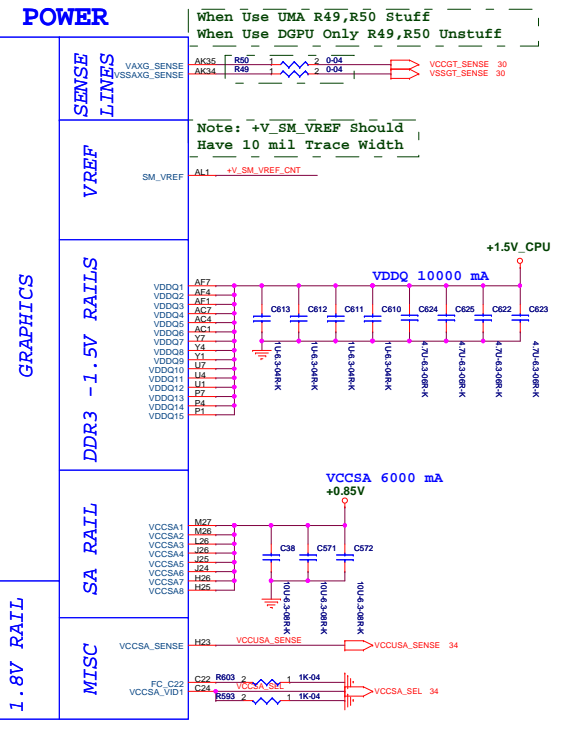
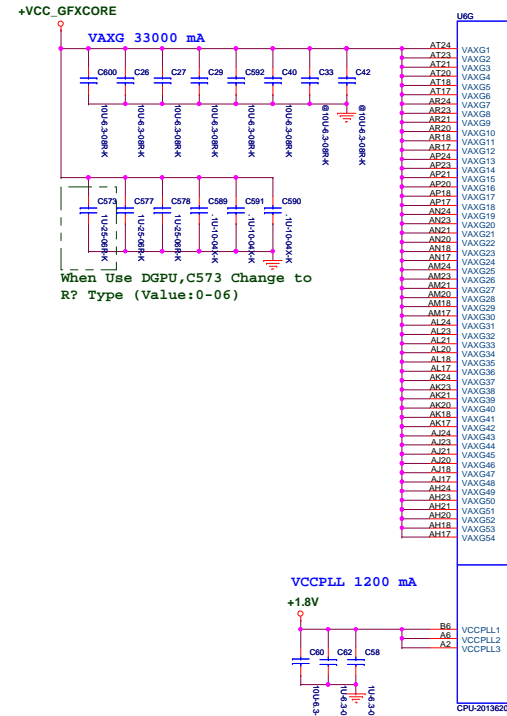
Clock Generator			
VCC	ICC (mA)	mW	TEMP (°C)
+3.3V	270	891	70

Cougar Point PCH			
Voltage (V)	Current (mA)	Measure	Watt
+1.05V_VCCP	43		
+1.05V	5565		
+1.8V	250		
+3.3VS	129		
+3.3V	260		
+5VA	1		
+5V	1		

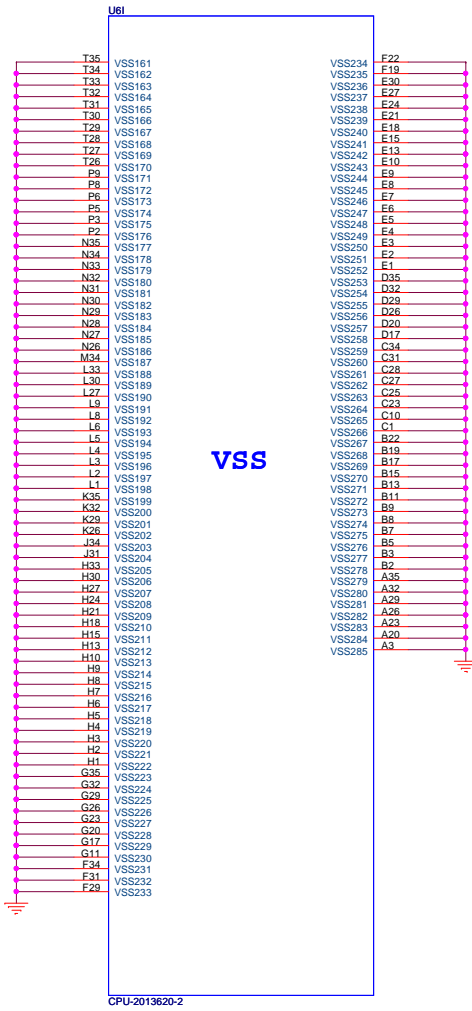
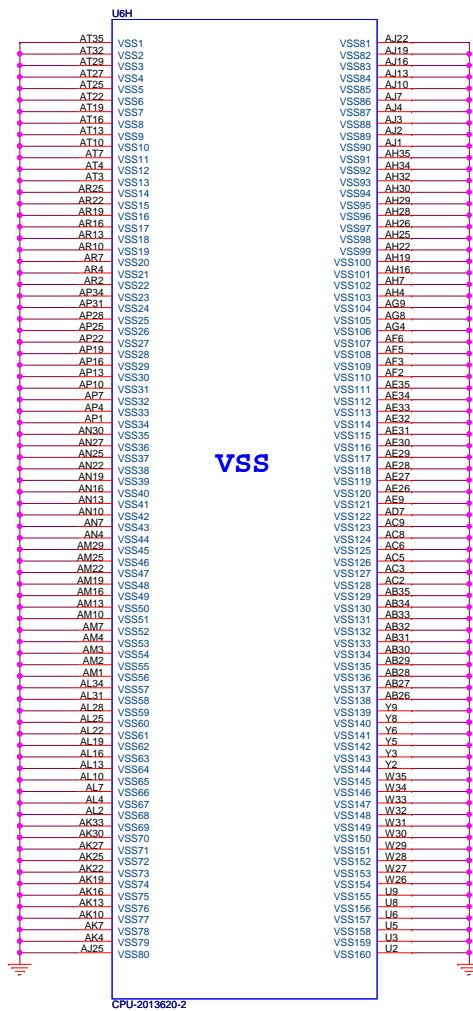


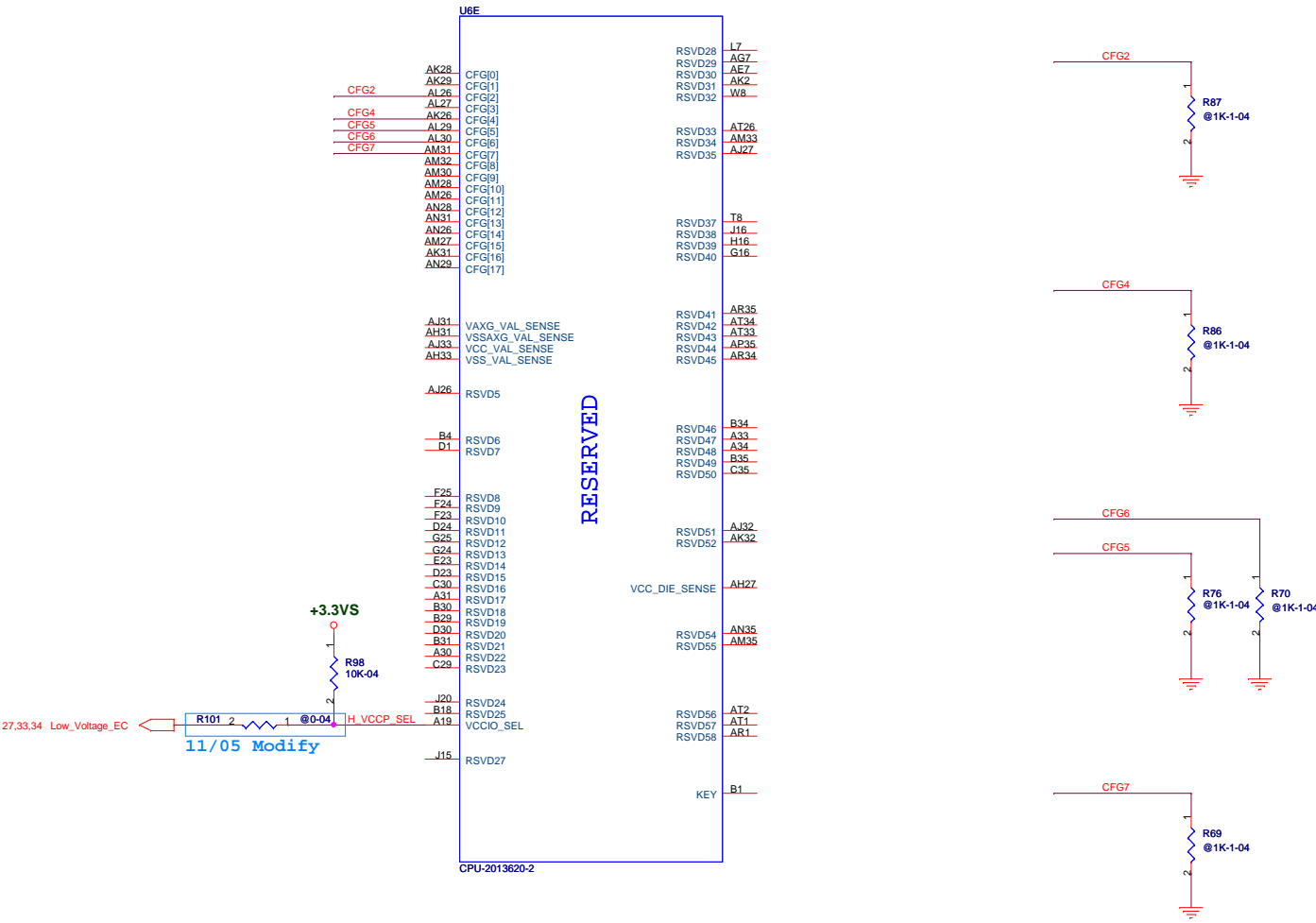












PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

Display Port Presence Strap	
CFG4	1:(Default) Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

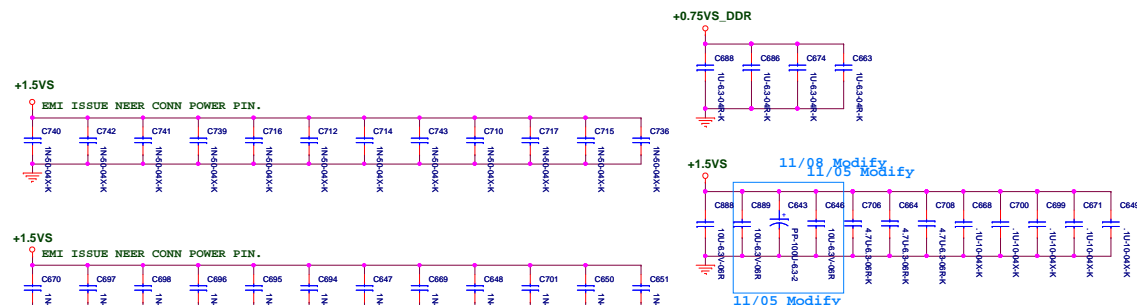
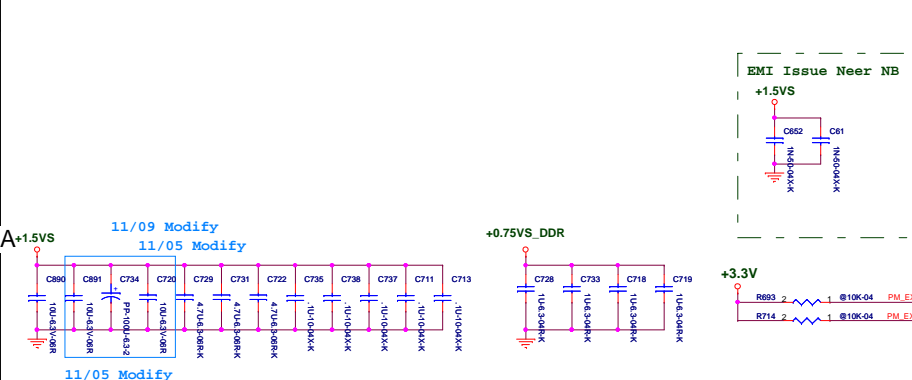
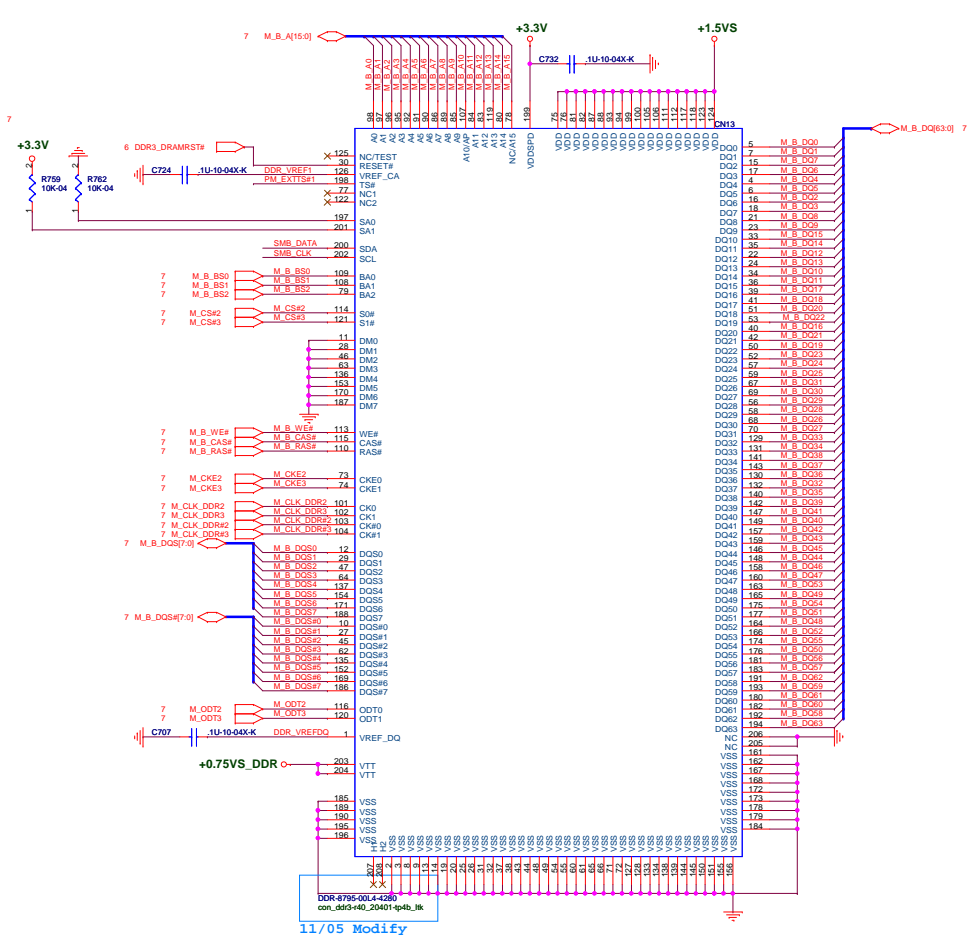
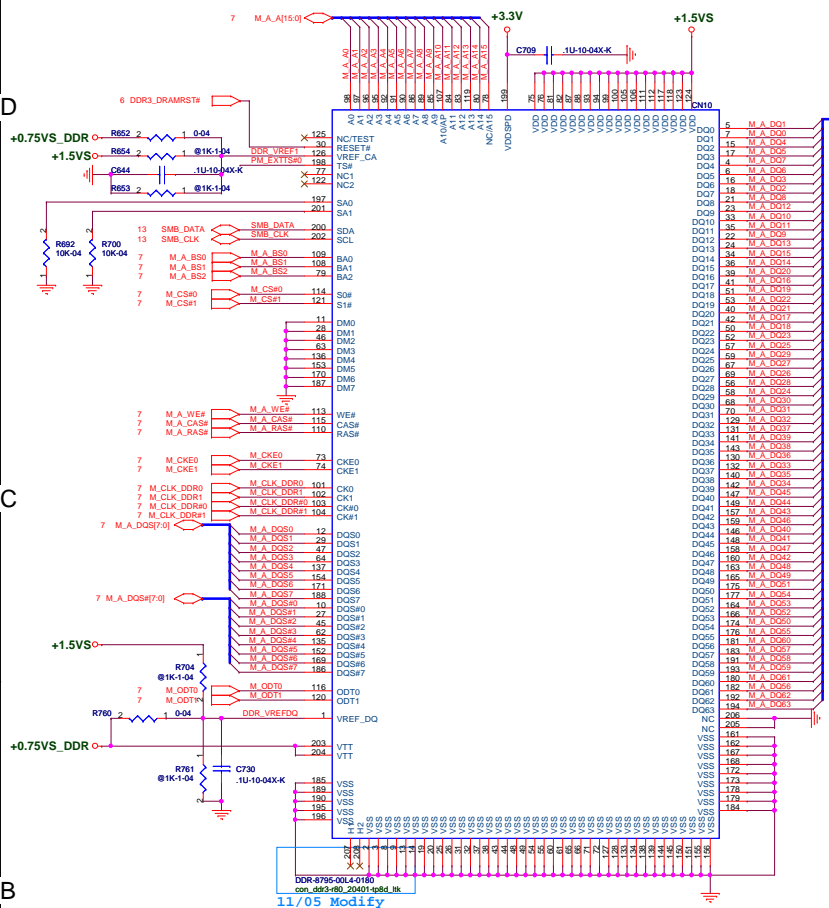
PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training



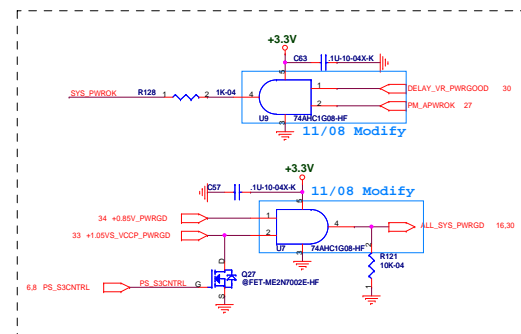
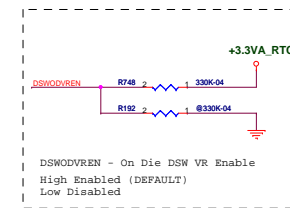
ECS COMPUTER CORP.

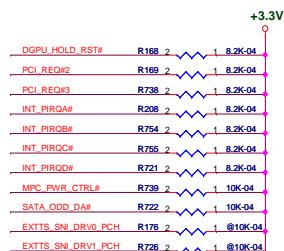
Title			
Sandy Bridge_Reserved			
Size	Document Number	Rev	
	MB40IA B1-Phase Custom	MB40IA	B1
Date:	Tuesday, November 09, 2010	Sheet	10 of 44











A16 swap override Strap	
STP_A16OVR	LOW = A16 swap override High = Default

6.12.22.26.27 BUF\_PLT\_RST#

+3.3V

C747 1U-10-04X-K

C899 @:1U-10-04X-K

R220 100K 1-04

U11 74AHC1G08-HF

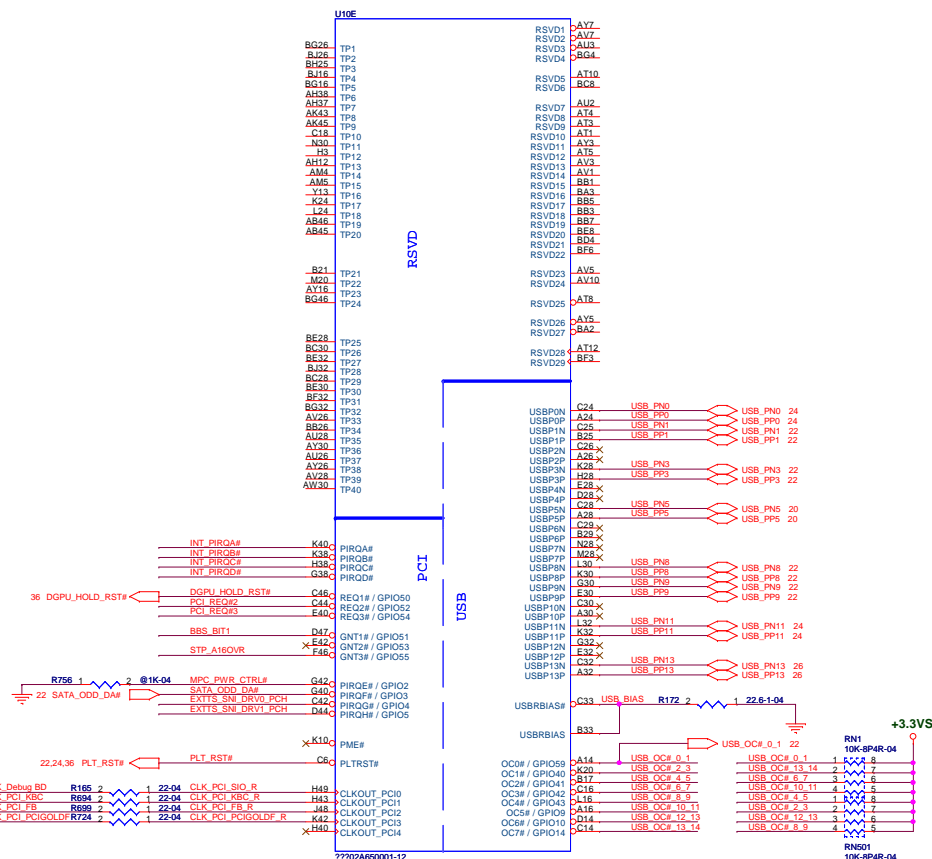
PLT\_RST#

C86 @:1U-10-04X-K

11/02 Modify

11/02 Modify

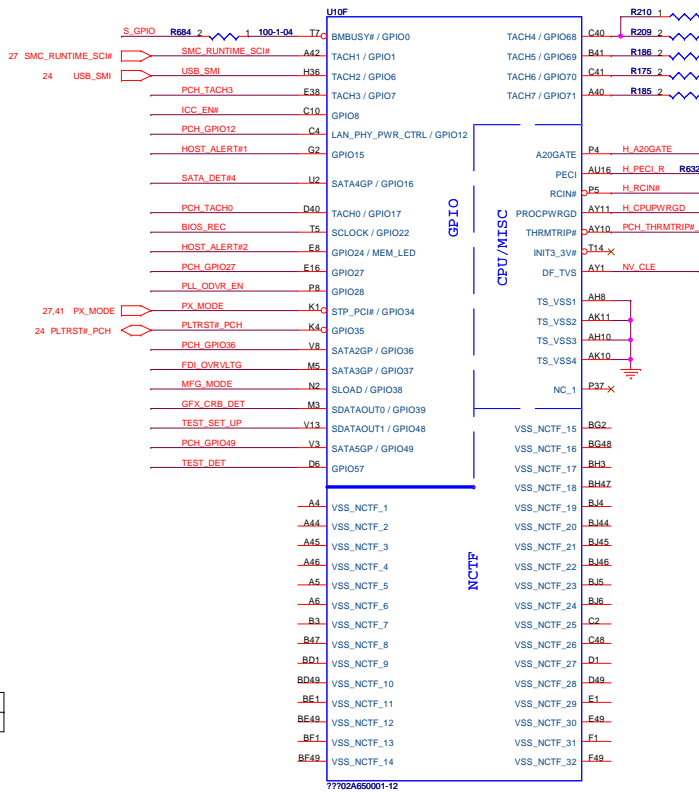
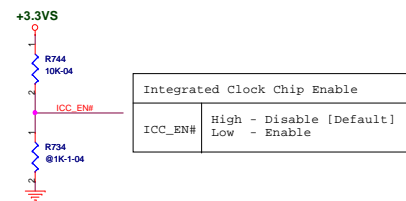
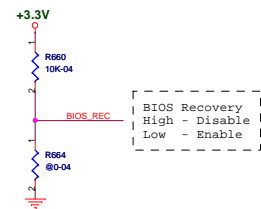
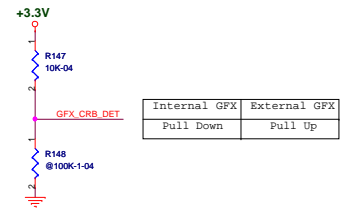
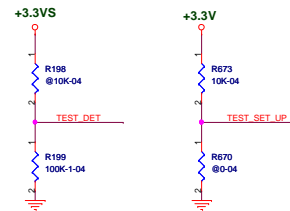
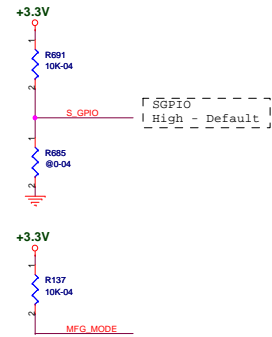
Buffer to reduce loading on PLT\_RST#



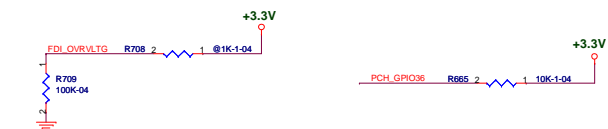
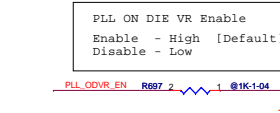
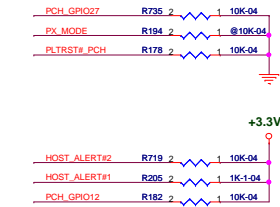
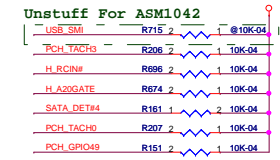
USBP0 USBN0	Enhance USB USB_9
USBP1 USBN1	USB Port USB_1
USBP2 USBN2	
USBP3 USBN3	WLAN USB_3
USBP4 USBN4	
USBP5 USBN5	Web Camera USB_5
USBP6 USBN6	Disable
USBP7 USBN7	Disable
USBP8 USBN8	Finger Print USB_8
USBP9 USBN9	USB Port USB_9
USBP10 USBN10	
USBP11 USBN11	Enhance USB USB_11
USBP12 USBN12	
USBP13 USBN13	Card Reader USB_13



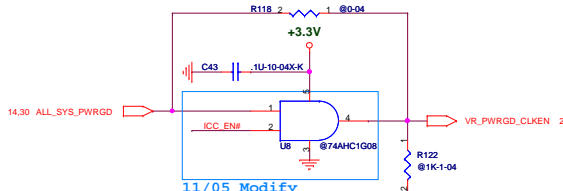
12.22 SATA\_ODD\_PRSNTH# R663 1 2 0-04 PCH.GPIO36

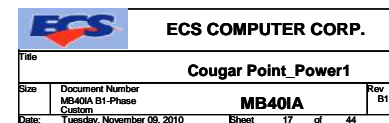


GPIO6 Status	
TACH2 / GPIO6	If not used, request a weak pull up When mount Chip of USB 3.0 , R715 unstuff.

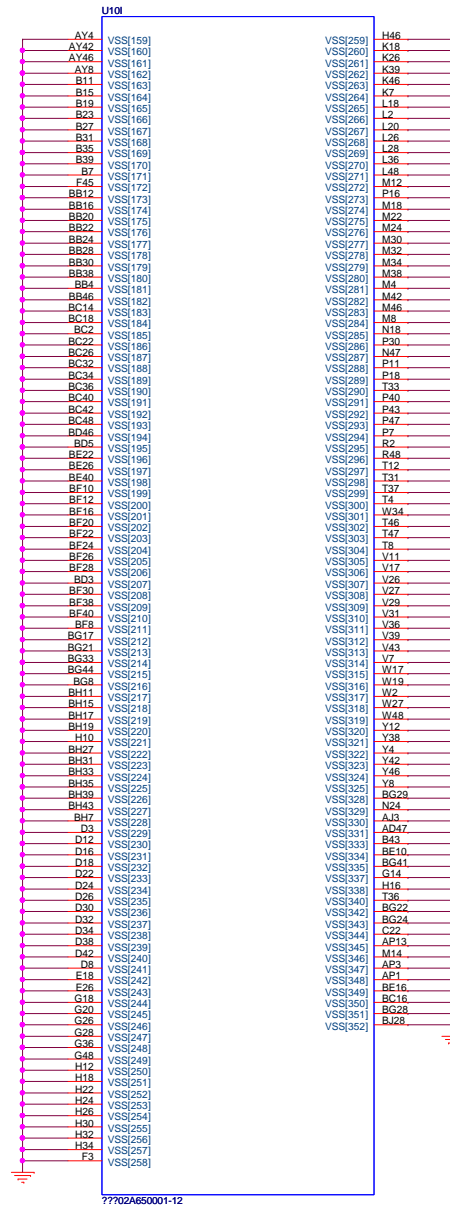
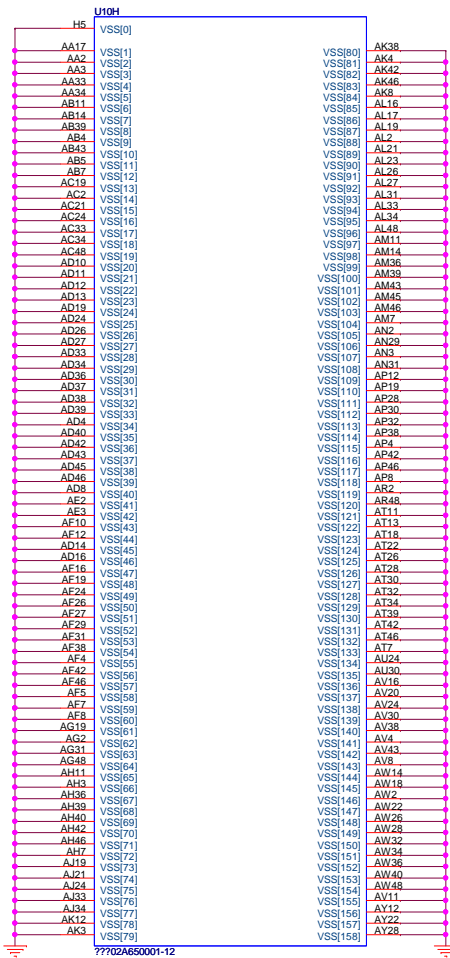


FDI TERMINATION VOLTAGE OVERRIDE		DMI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT	GPIO36 (SATA_ODD_PRSNTH#)	LOW - Tx, Rx terminated to same voltage (DC Coupling Mode) DEFAULT

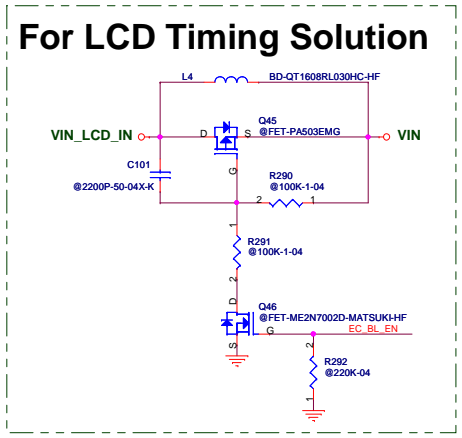
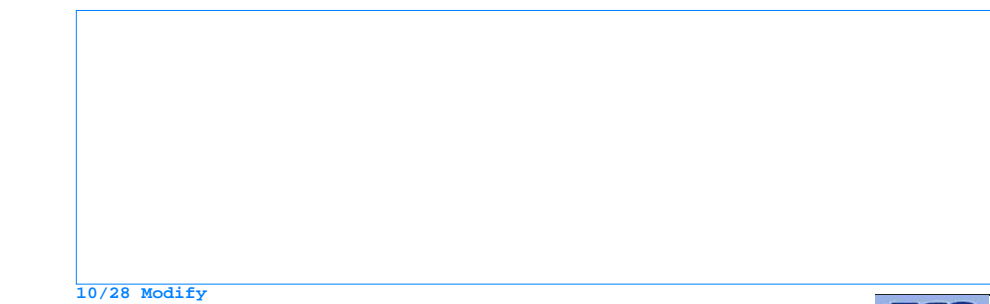
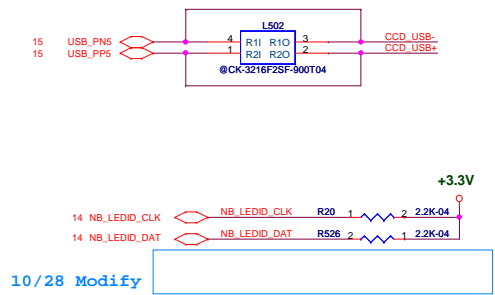
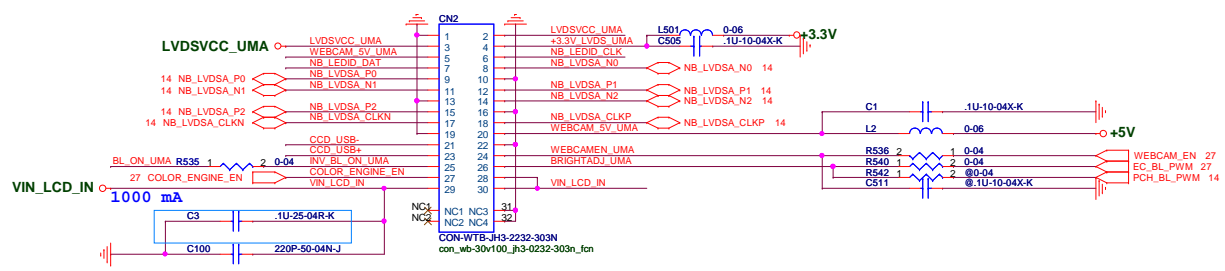
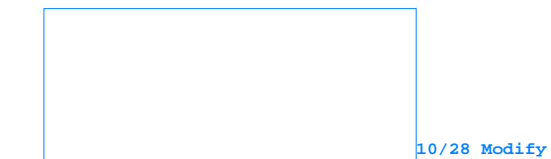
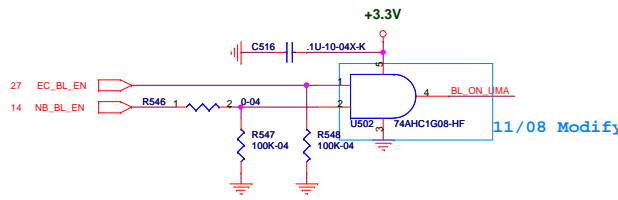
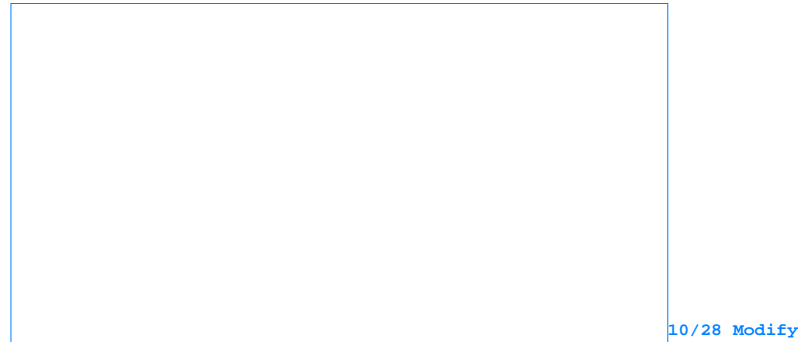
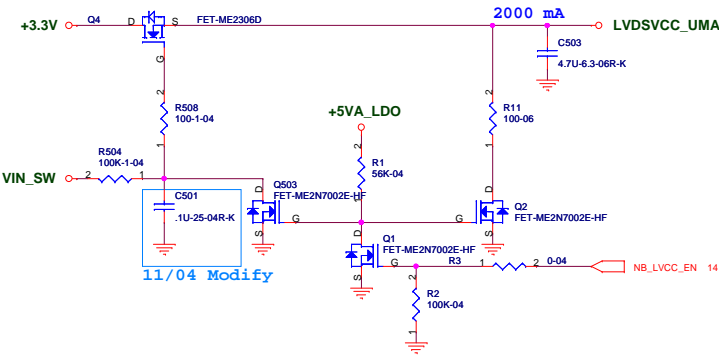







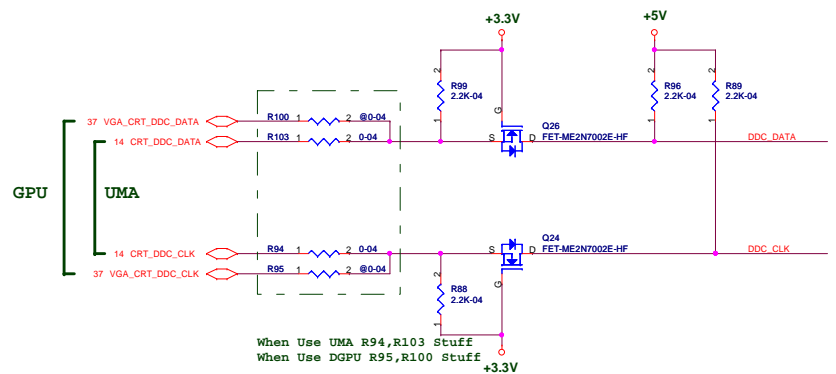
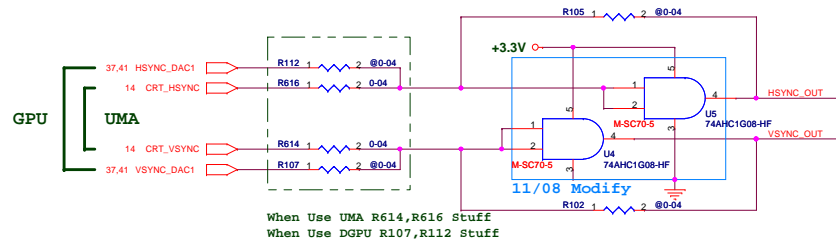
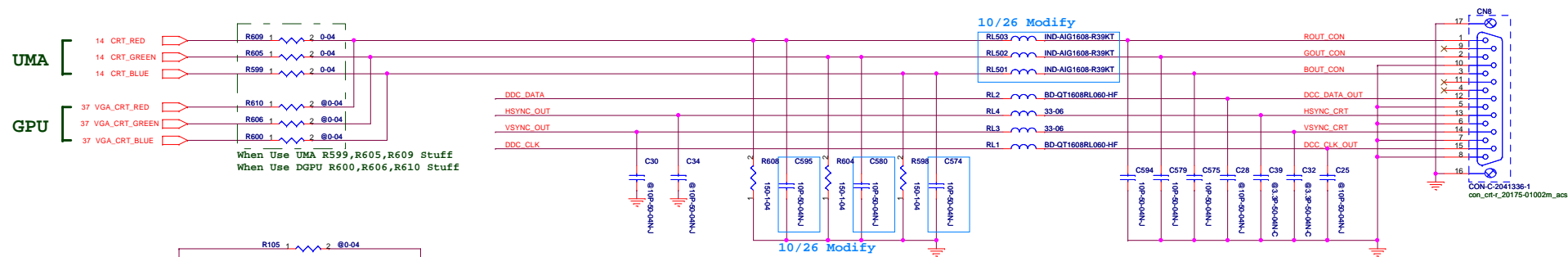


LVDS + Webcam Connector

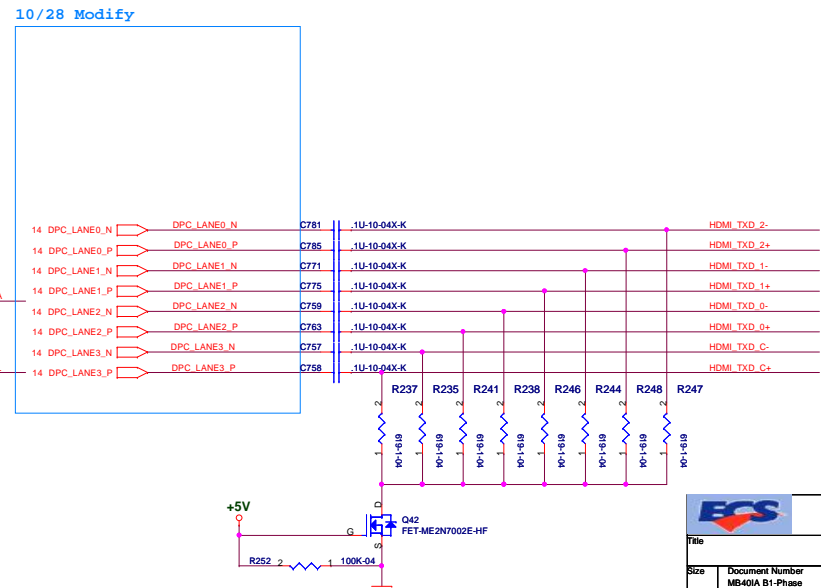
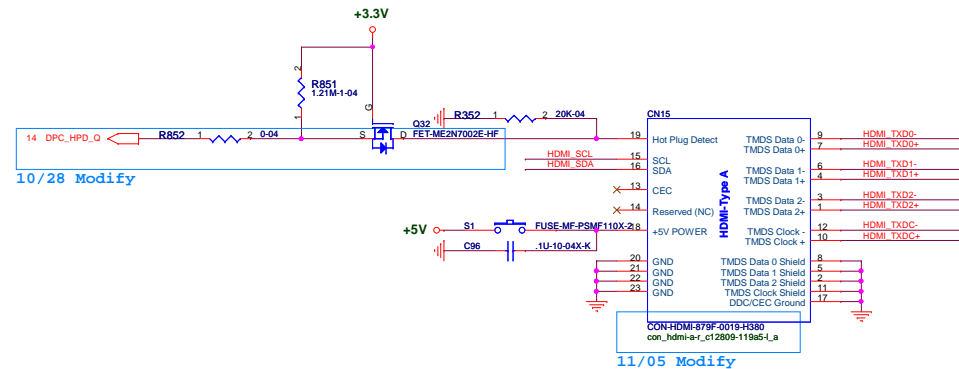


		<b>ECS COMPUTER CORP.</b>	
Title			
LVDS/Webcam			
Size	Document Number		Rev
	MB401A B1-Phase Custom		B1
<b>MB401A</b>			
Date:	Tuesday, November 09, 2010		
	Sheet	20 of 44	

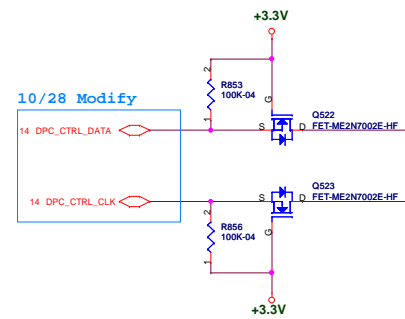
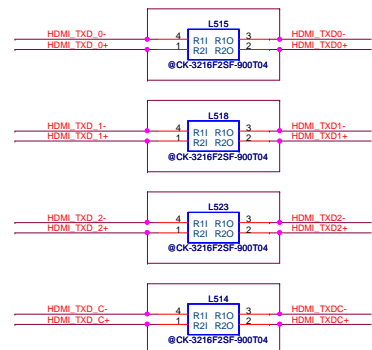
## CRT Connector



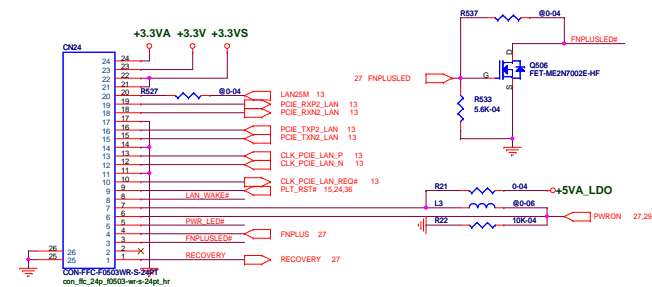
## HDMI Connector



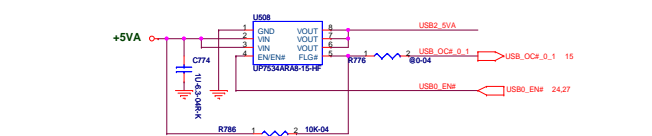
## EMI Issue



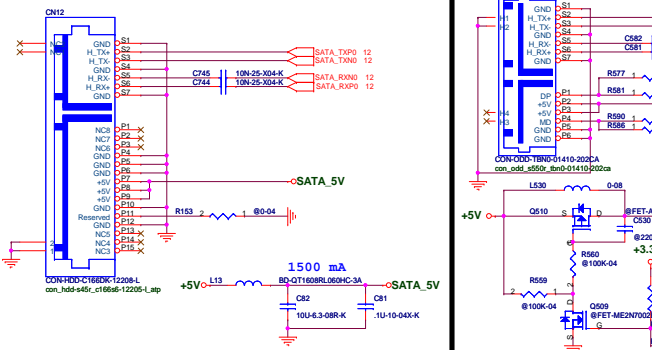
## PWR SW + LAN Connector



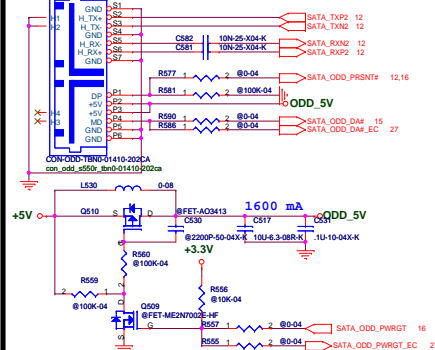
## USB Port 2.0 USB 1 & USB 9



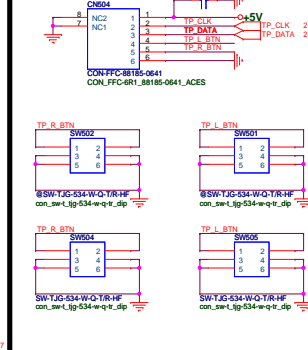
## SATA HDD



## SATA ODD

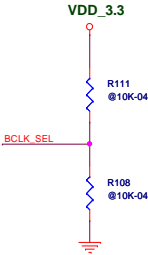
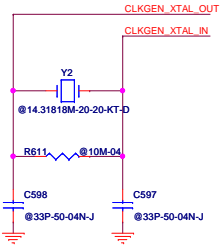


## Touch Pad Connector

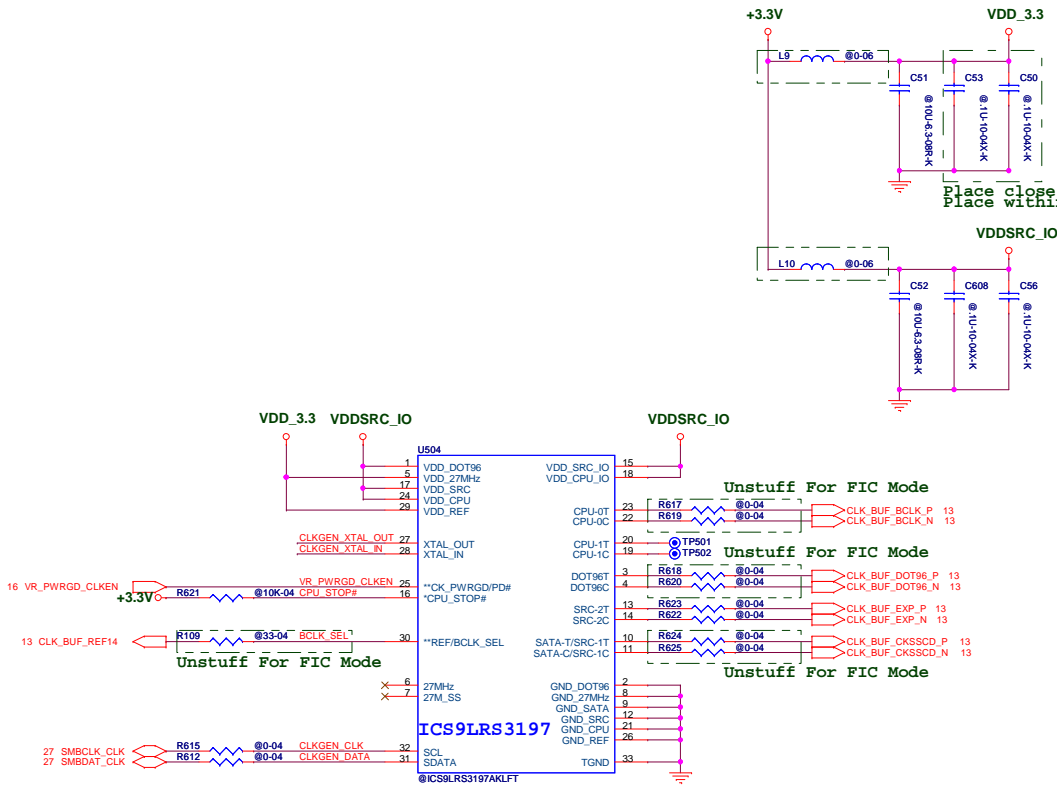





Clock Gen



BCLK_SEL input	BCLK	NOTE
—		
0	133MHz	
1	100MHz	Default



**ECS COMPUTER CORP.**

File

**Clock Gen (ICS9LRS3197)**

Size

Document Number

Rev

MB40IA B1-Phase

**MB40IA**

B1

Date

Tuesday, November 09, 2010

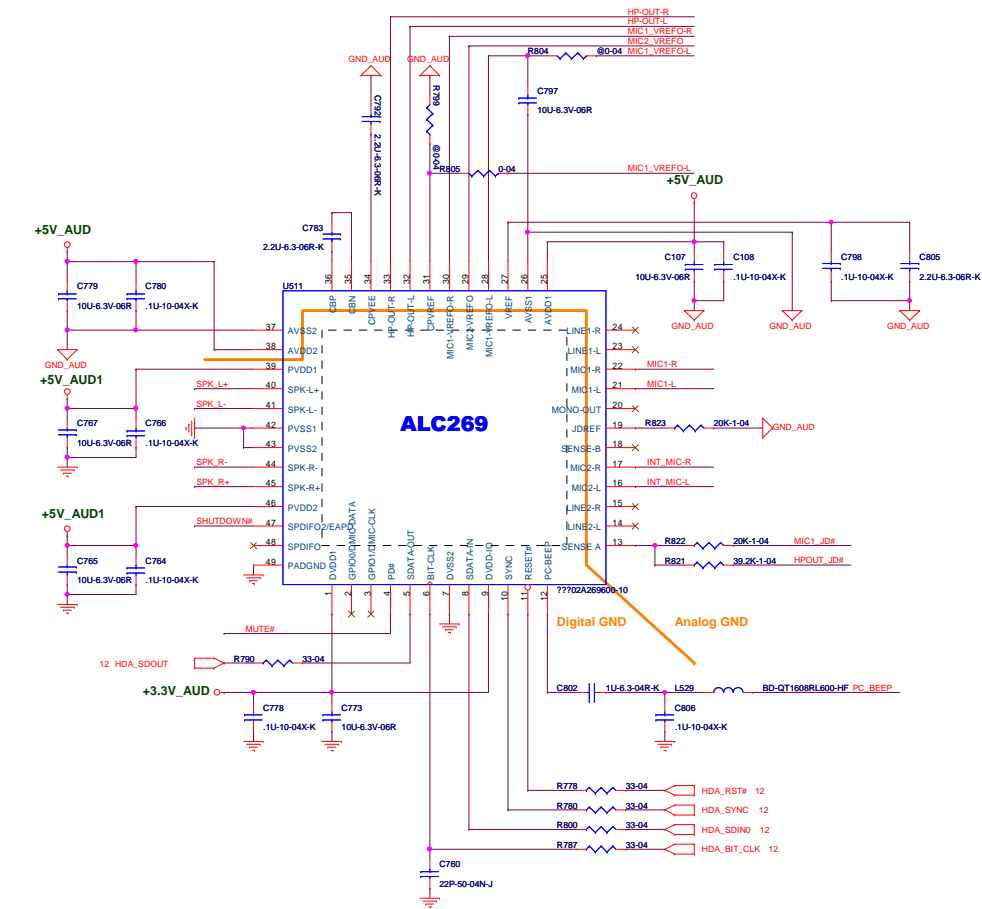
Sheet

23

of

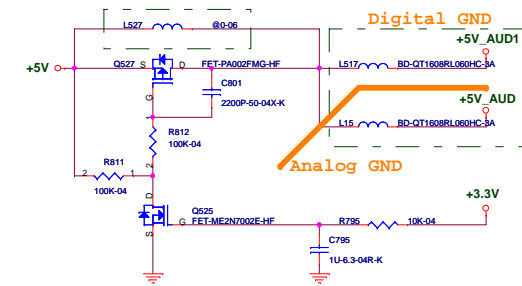
44





	VA	VB
R799	○	×
R804	○	×
R805	×	○
C797	×	○

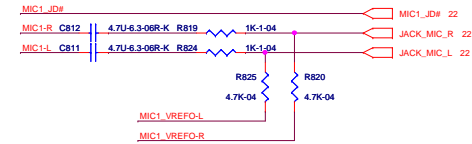
## AMP VDD



When Use ALC269VB; L15, L517, L527 need stuff; other unstuff

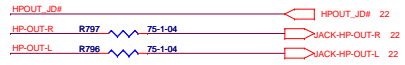
## Microphone + Line In Jack

Component Close to Codec



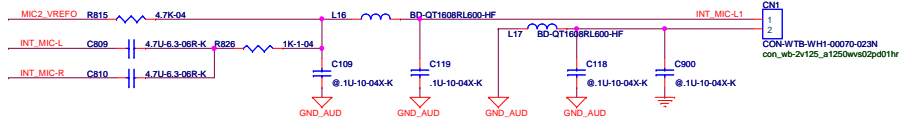
## Headphone Jack

Component Close to Codec

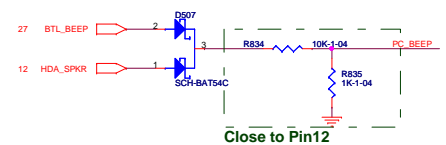
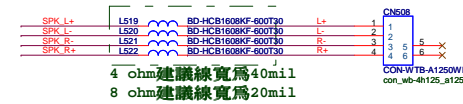


## Internal MIC Connector

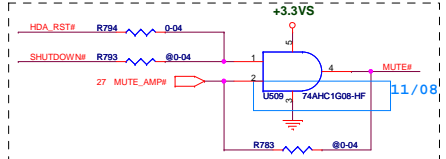
Component Close to Codec



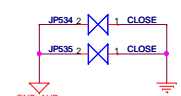
## Speaker Connector



Close to Pin12



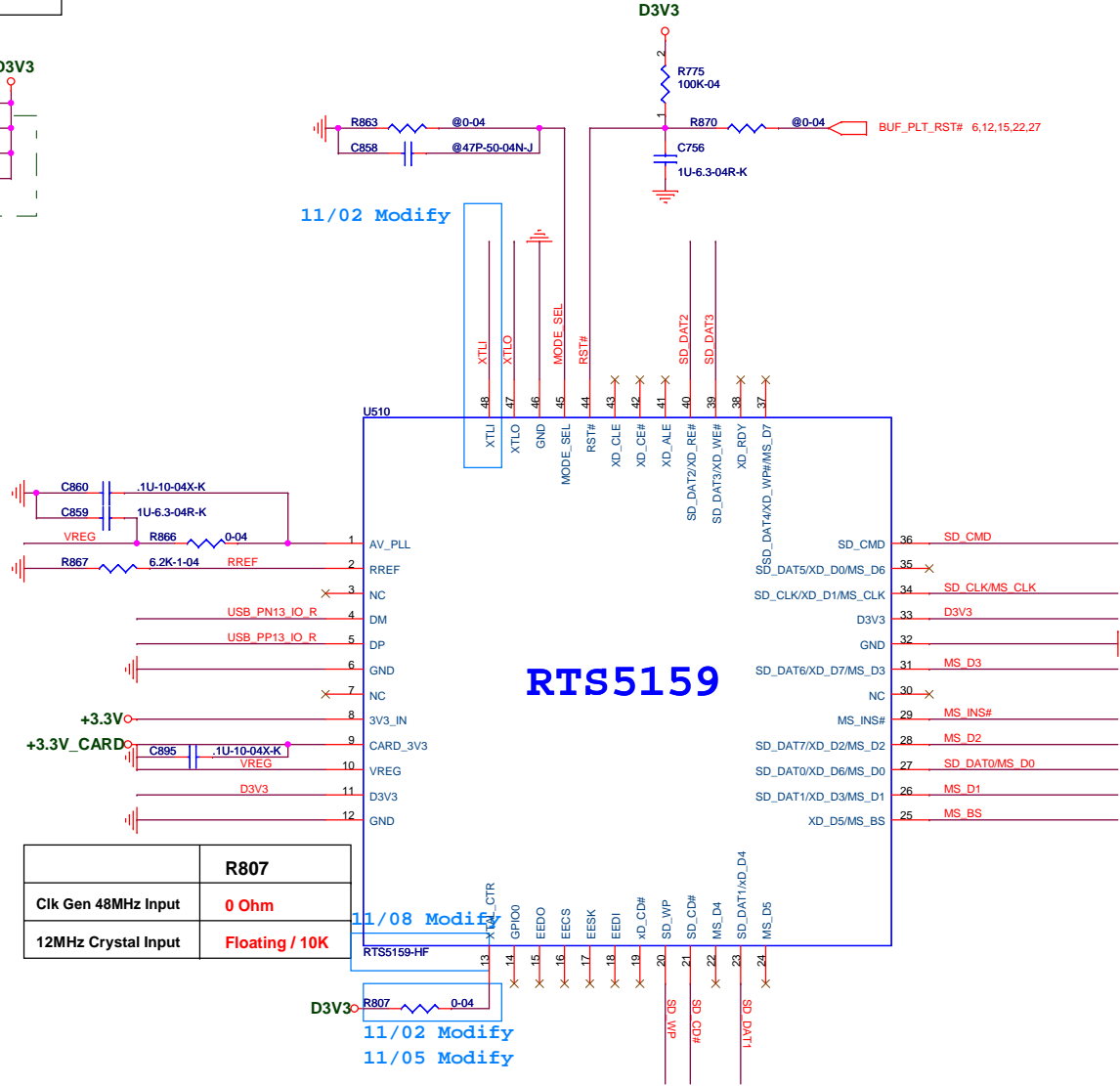
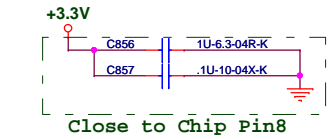
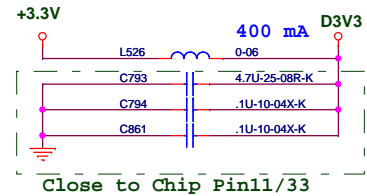
Modify



www.vinafix.vn

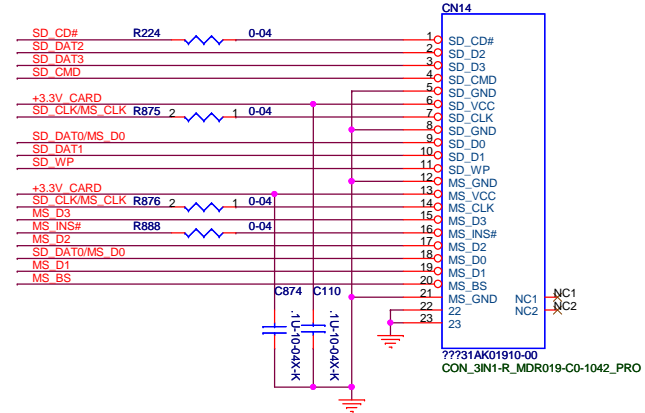
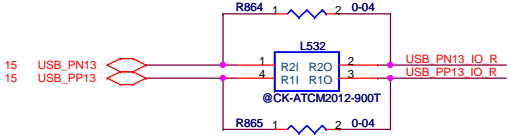
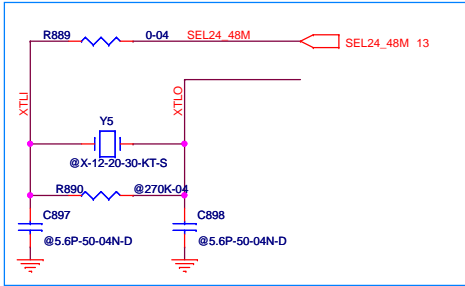
Card Reader


CardReader ID Select		
Haier	IA2	Nustuff; @ Small BD
Hasee	IA3	Stuff; @ MB



	<b>R807</b>
Clk Gen 48MHz Input	0 Ohm
12MHz Crystal Input	Floating / 10K

11/05 Modify  
11/02 Modify  
10/28 Modify  
10/26 Modify





**ECS COMPUTER CORP.**

Title

**Card Reader (RTS5159-GR)**

Size

Document Number

MB40IA B1-Phase

Custom

Rev

B1

Date:

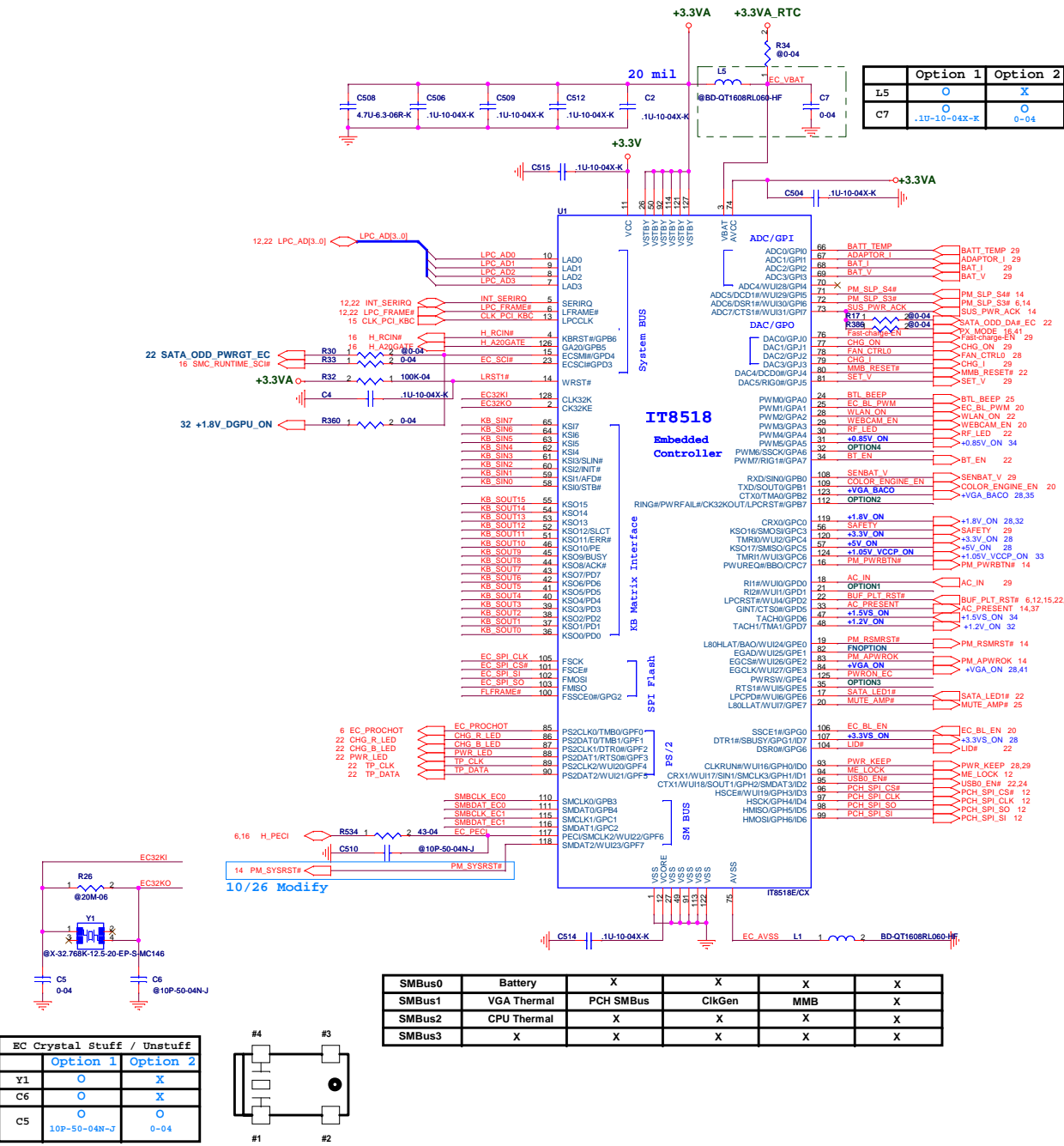
Tuesday, November 09, 2010

Sheet

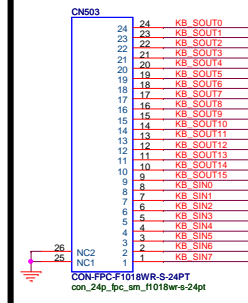
26

of

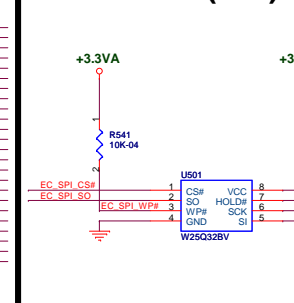
44



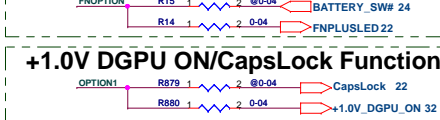
## K/B Connector



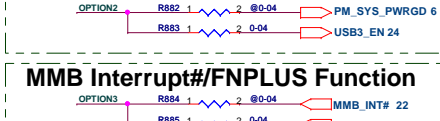
## Flash ROM (SPI)



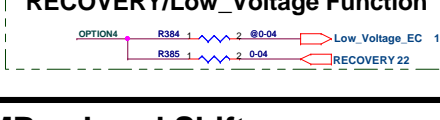
## USB Charger/FNPLUSLED Function



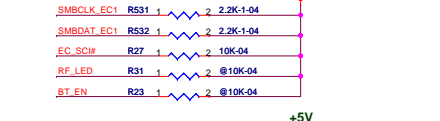
## +1.0V DGPU ON/CapsLock Function



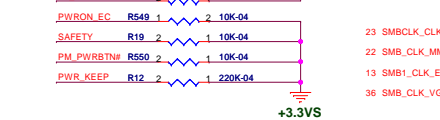
## PM SYS PWRGD/USB3\_EN Function



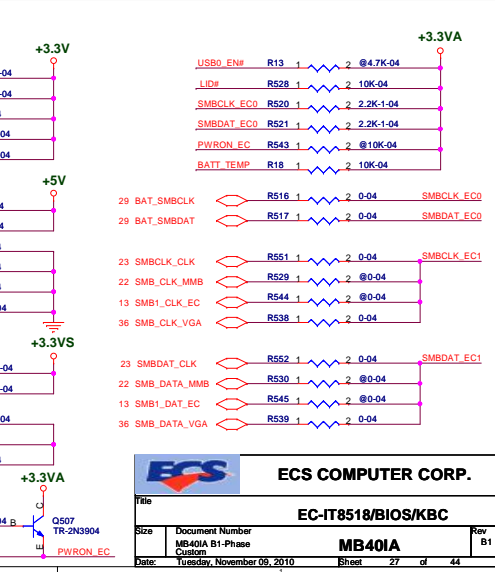
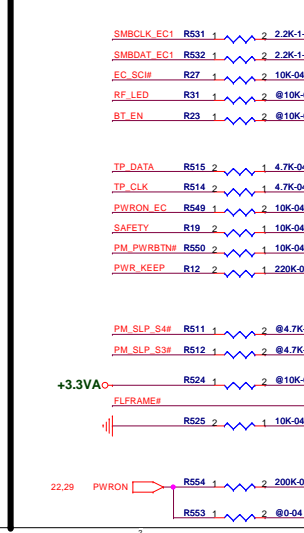
## MMB Interrupt#/FNPLUS Function



## RECOVERY/Low Voltage Function



## SMBus Level Shift



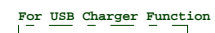
**ECS COMPUTER CORP.**

**EC-IT8518/BIOS/KBC**

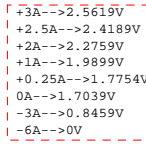
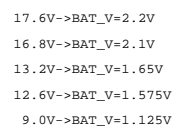
File	Document Number	Rev
MB401A B1-Phase	MB401A	B1

Date	Version	Sheet	of
Tuesday, November 09, 2010	27	27	44





VBAT


$$I_{ac} = I_{ad} \cdot \text{Rad} \cdot 60$$

Vch=Nx(4.1+Vset/10)  
N=Cell (pin7 high ->4cell, low ->3cell H/L=2cell )

CHG_ON	
I	CHARGER ON

CHG\_I=Ich\* Rch \* 60

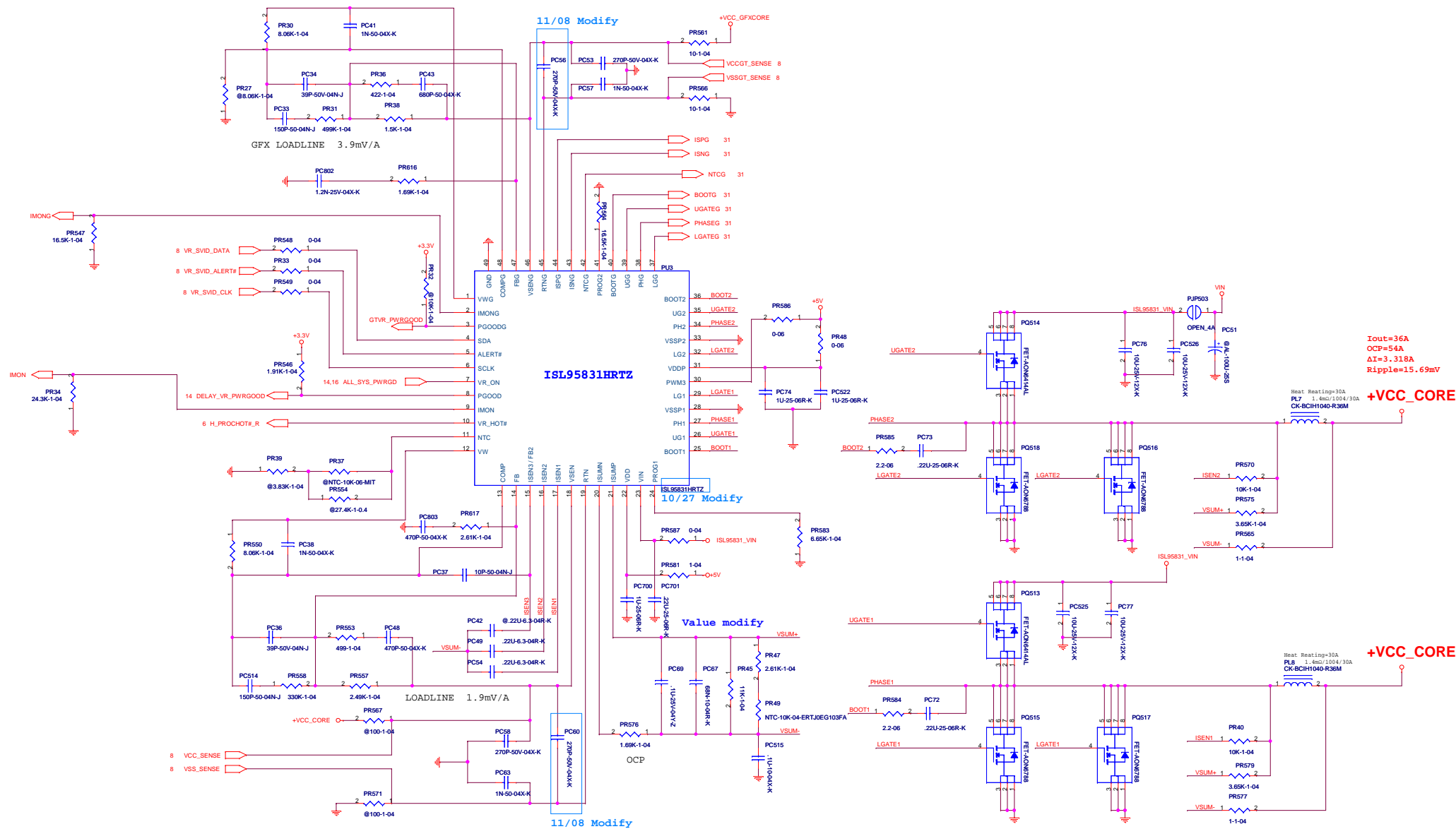
--	--	--

	IA	II
DD519	2.01K 1.04	20K 1.04

Wake up Current set =  $IWK * Rch * 300$

Wake up Voltage set = Cell\*(1.8+WK\_TH)  
When Wake up mode CHG\_I Should > 0.6V



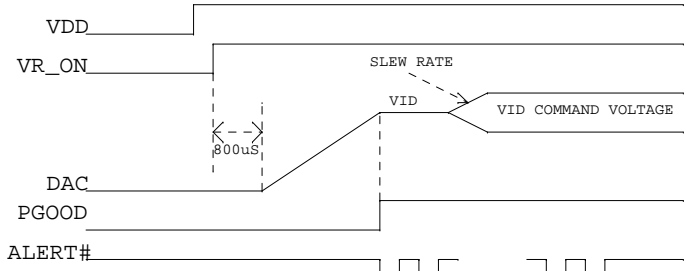


I<sub>out</sub>=36A  
OCP=54A  
ΔI=3.318A  
Ripple=15.69mV

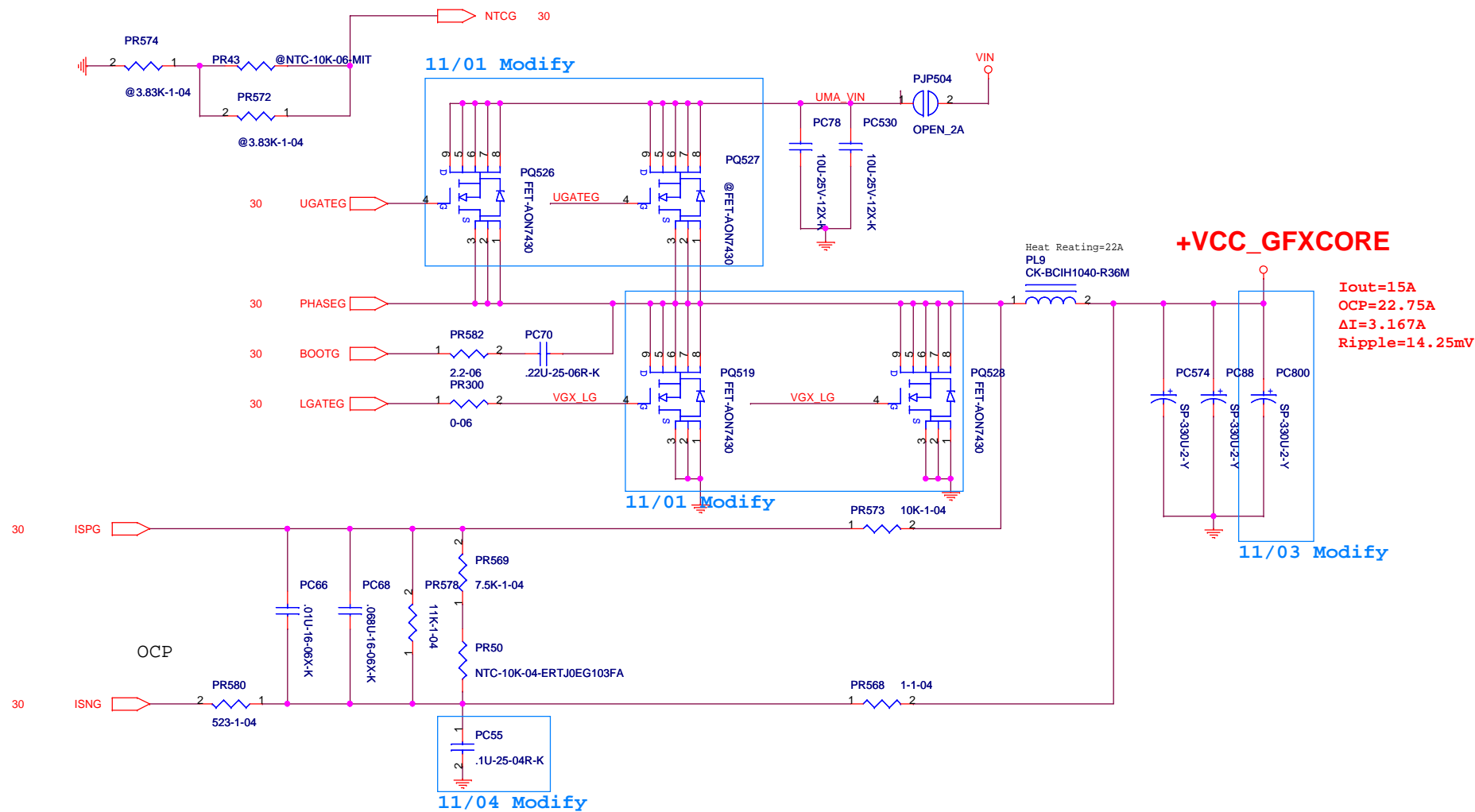
+VCC\_CORE

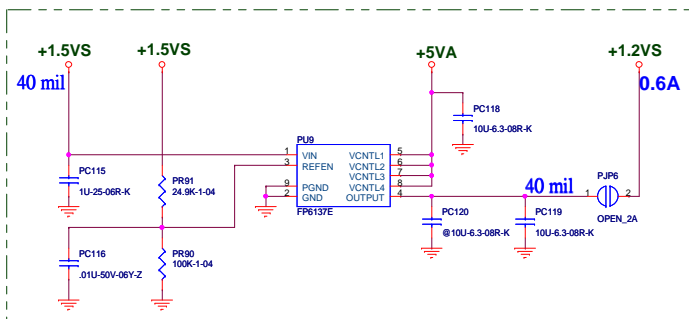
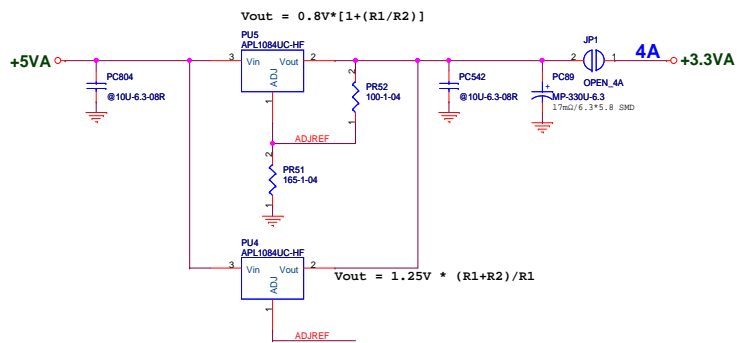
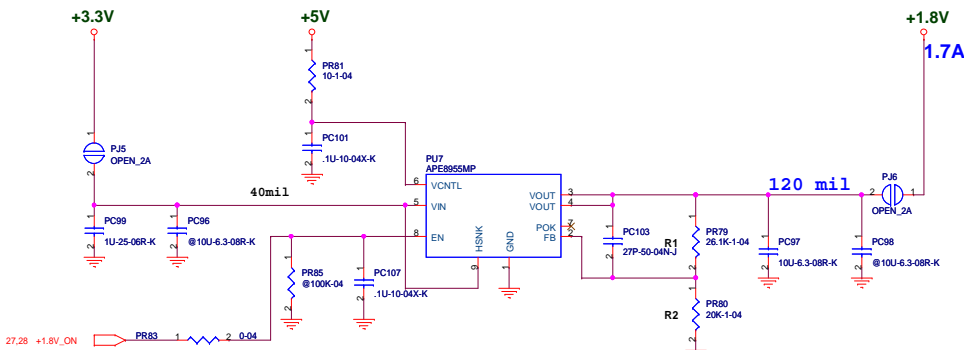
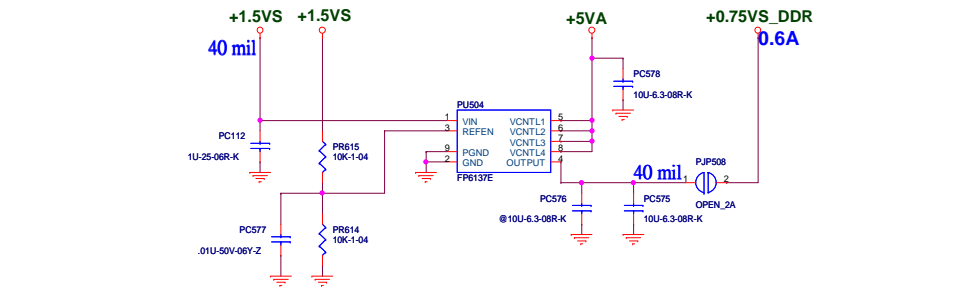
+VCC\_CORE

+VCC\_CORE

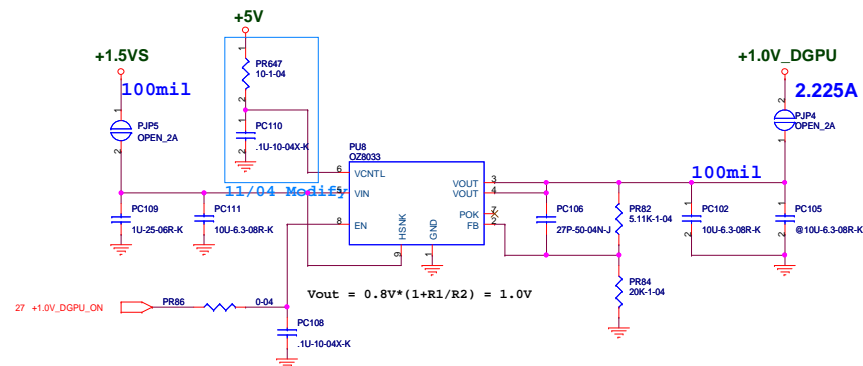


www.vinafix.vn

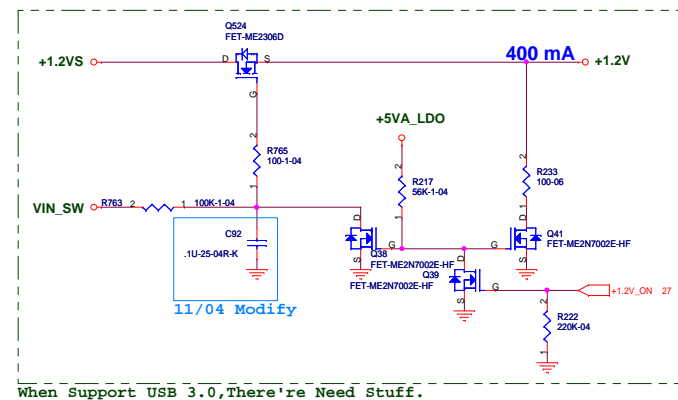
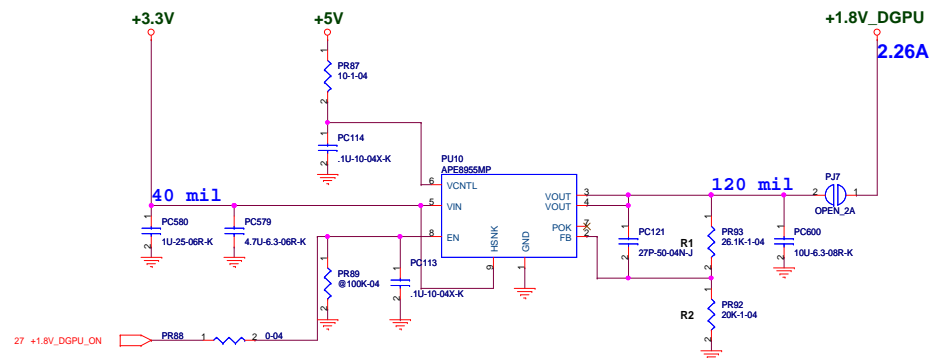




When Support USB 3.0, There're Need Stuff; Except PC120.



$$V_{out} = 0.8V * (1 + R1/R2) = 1.0V$$



When Support USB 3.0, There're Need Stuff.

$$\text{Output Voltage} = \left[ \text{Vref} \times \frac{R2}{R1+R2} \right] \times 2$$

EC L=1.056V

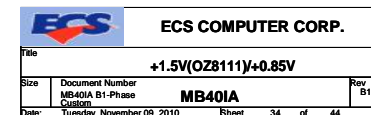
EC H=1.004V

$$\text{Output Voltage} = \left[ \text{Vref} \times \frac{R2}{R1+R2} \right] \times 2$$

$$F = \text{Vset} \times \left( \frac{\text{Vin}}{2 - \text{Vset}} \right) / \left( 2 \times \text{Vtest} \times \frac{\text{Vin}}{2} \right)$$

$$\text{Vset} = \text{Vout} / 2, \text{Vtest} = 2.75\text{V}$$

EC H=1.42V
------------



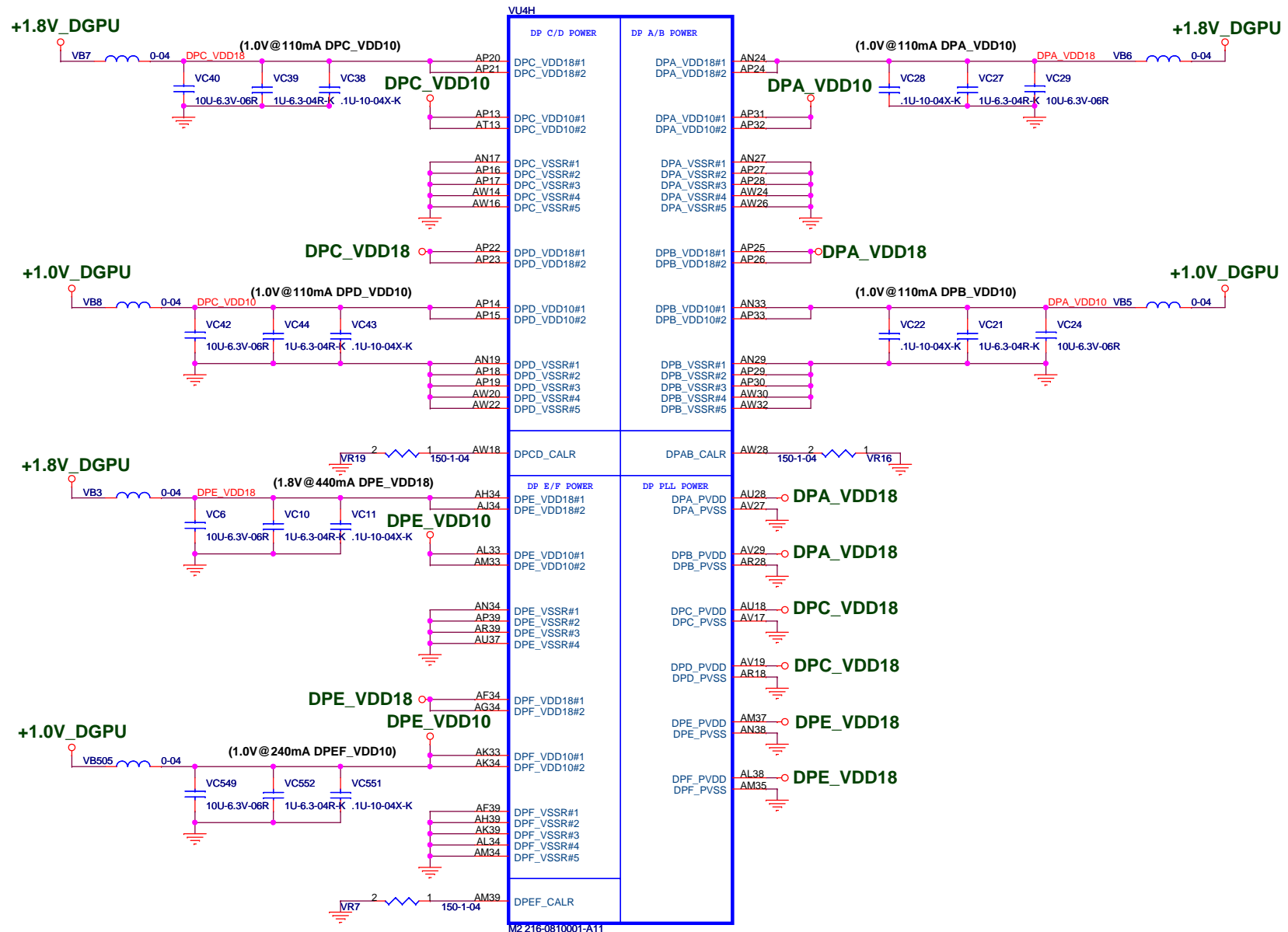












For M97/M96, DPF\_VDD18 can be shared with DPE\_VDD18

For M97/M96, DPF\_VDD10 can be shared with DPE\_VDD10

For dual link DVI using DPA AND DPB, DPA\_VDDxx and DPB\_VDDxx can be shared respectively

For dual link DVI using DPC AND DPD, DPC\_VDDxx and DPD\_VDDxx can be shared respectively

For dual link LVDS, DPE\_VDDxx and DPF\_VDDxx can be shared respectively

www.vinafix.vn



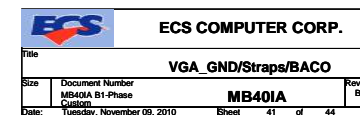
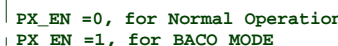
ECS COMPUTER CORP.

Title			VGA Power 1
Size	Document Number	Rev	
	MB40IA B1-Phase	B1	
	Custom	MB40IA	
Date:	Tuesday, November 09, 2010	Sheet	39 of 44

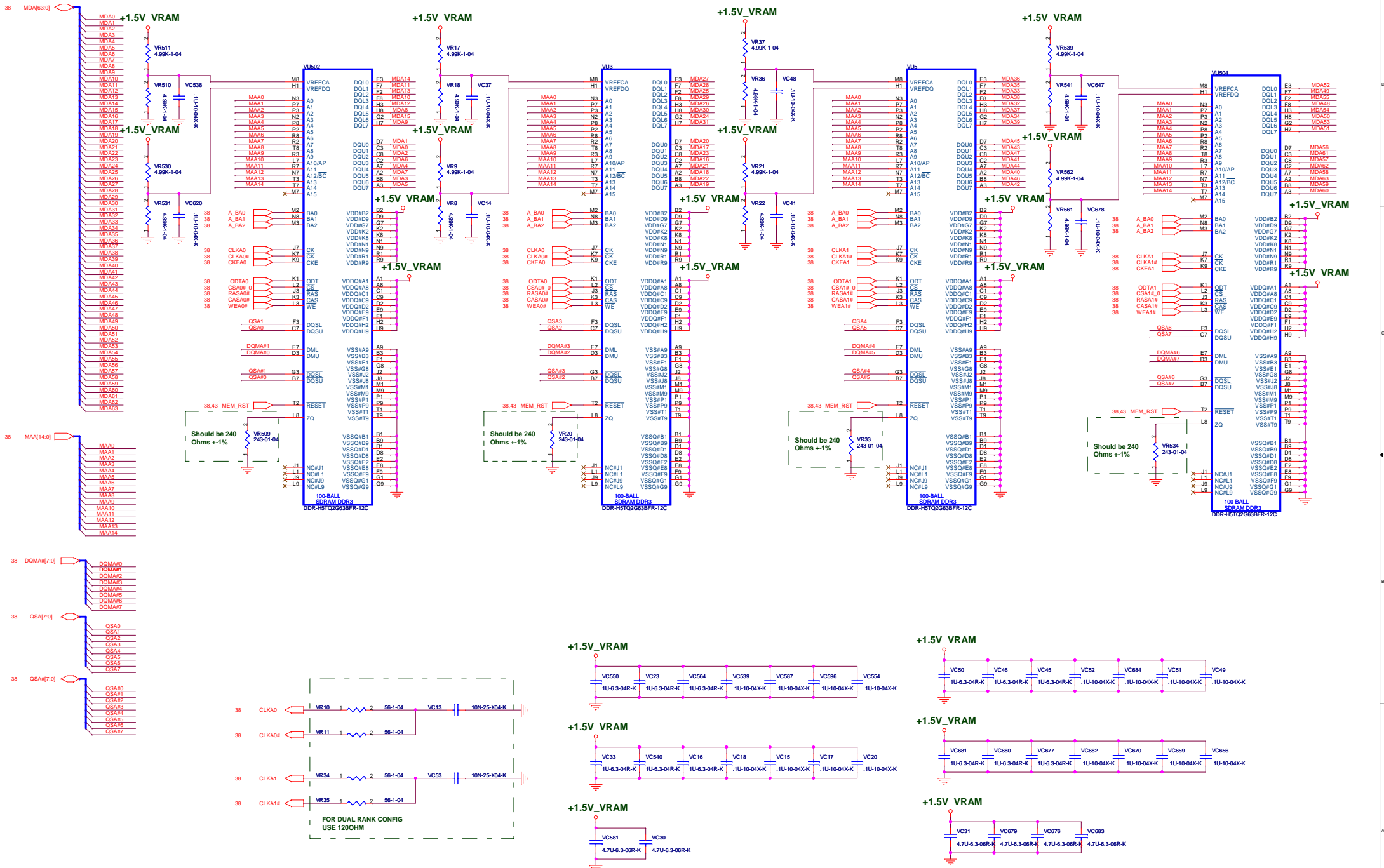




ROM_ID(2:0)	Size
000	128MB
001	256MB
010	64MB
011	32MB

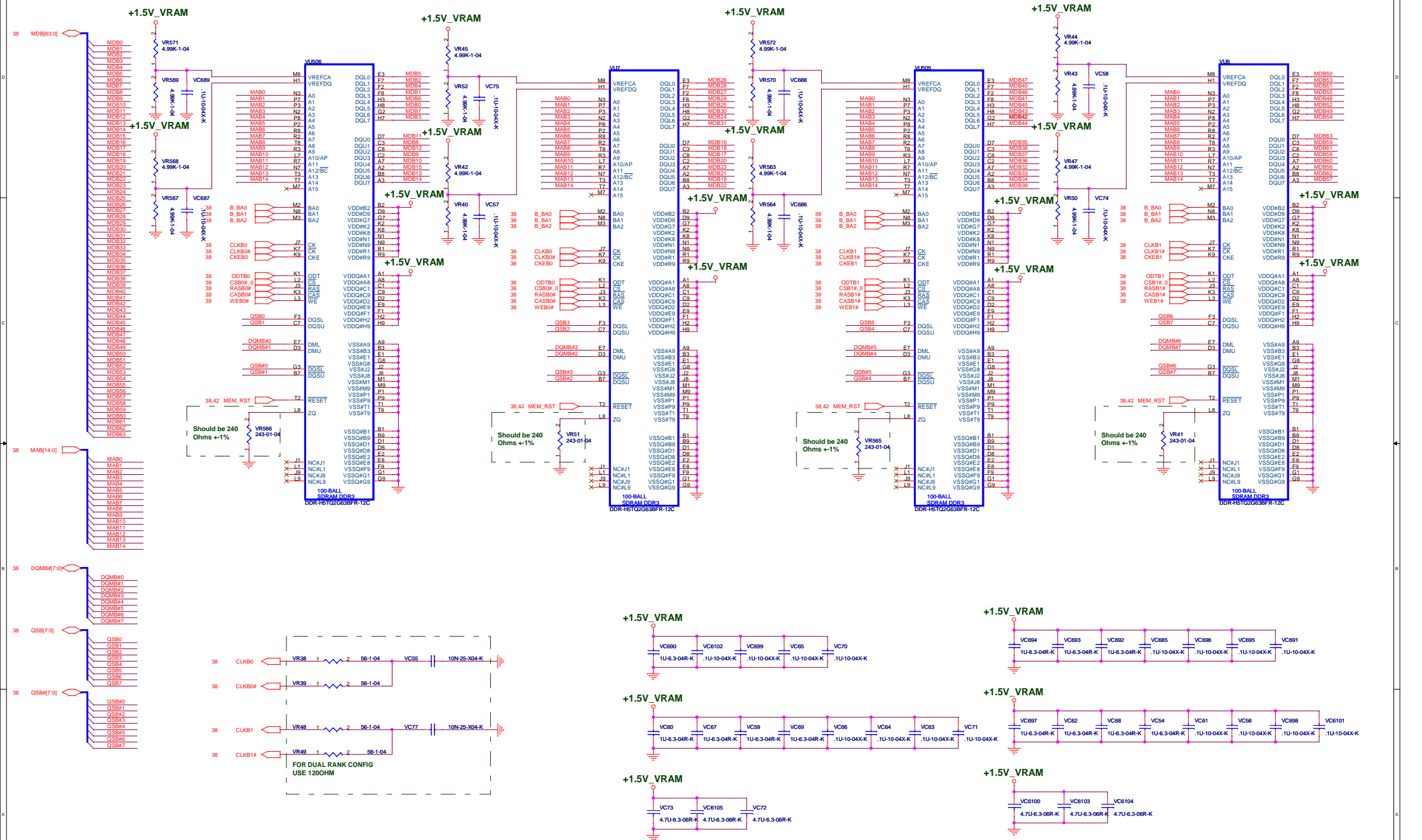


# CHANNEL A: 256MB/512MB DDR3 (RANK0)





# CHANNEL B: 256MB/512MB DDR3 (RANK1)



EE Schematics Modify

10/16 Modify

- 01. Page 12 : R662 change value to 56-1-04.
- 02. Page 13 : Y3 modify;value is X-25M-30-KT-S-HF & footprint is HC-49\_3HSM.
- 03. Page 14 : PM\_SYSTRS# net connect with 118 pin of EC.
- 04. Page 20 : Add LCD timing solution for GPU.
- 05. Page 21 : RL501/RL502/RL503 change value to IND-AIG1608-R39KT;595/C580/C574 stuff.
- 06. Page 26 : Add Y5 crystal For CardReader.
- 07. Page 29 : PF1 cahnge value to FUSE-CC12H5A-TR.
- 08. Page 30 : PU3 change footprint to qfn48\_6x6x1.

10/28 Modify

- 01. Page 20 : Del R576,R575.
- 02. Page 37 : Del VGA\_LEDID\_CLK net & VGA\_LEDID\_DAT net.
- 03. Page 37 : Del VGA\_BL\_EN net
- 04. Page 20 : Del U503/C557/R574/R568R567.
- 05. Page 36 : Del TXCLK\_L+TXCLK\_L-/TXOUT\_L0+TXOUT\_L1-/TXOUT\_L1+TXOUT\_L2-/TXOUT\_L2- net
- 06. Page 36 : Del VGA\_LCDBL\_PWM/VGA\_LVDD\_EN net.
- 07. Page 20 : Del CN5 & Peripheral schematics / Del GPU power switch schematics.
- 08. Page 37 : Del VR557/VR558/VQ504/VR560/VR559.
- 09. Page 21 : Del R854/R855 & Del R766/R768 then be short.
- 10. Page 21 : Del VGA\_HDMI\_DAT net/VGA\_HDMI\_CLK net.
- 11. Page 37 : Del VGA\_HDMI\_DAT net/VGA\_HDMI\_CLK net.
- 12. Page 21 : Del RP1/RP2 ;Del RP502/RP504 then be short.
- 13. Page 21 : Del VGA\_TMDS2+ net/VGA\_TMDS2- net/VGA\_TMDS1+ net/VGA\_TMDS1- net/VGA\_TMDS0+ net/VGA\_TMDS0- net/VGA\_TMD\_CLK+ net/VGA\_TMD\_CLK- net.

10/29 Modify

- 01. Page 29 : H7/H13/H12/H5/H10/H9 change footprint to hc236d118.
- 02. Page XX : Y3/Y5 change footprint to XTAL-2P-11\_4X4\_6X3\_1.
- 03. Page XX : PQ2/PQ7/PQ505/PQ507/PQ508/PQ509/PQ510/PQ511/PQ512/PQ519/PQ520/PQ523/PQ524/PQ526/PQ527/PQ528 change footprint to TDFN8\_3X3X0\_8.
- 04. Page 35 : Add PC831/PC832.

11/02 Modify

- 01. Page 13 : R225 unstuff.
- 02. Page 26 : R889 unstuff;Y5/R890/C897/C898 stuff.
- 03. Page 35 : PC806/PC805 change footprint to M-R0603.
- 04. Page 29 : Add PR646/PC833.
- 05. Page 15 : Add C899.
- 06. Page 26 : R807 unstuff.

11/03 Modify

- 01. Page 31 : Add PC800.(@ bottom side)
- 02. Page 35 : Modify PJP511 (Support 4A.;TOPOPEN-4MM)

11/04 Modify

- 01. Page 35 : PC808 stuff;PC832 unstuff.
- 02. Page 24 : USB Charger Function unstuff.
- 03. Page XX : +1.5VS & +1.05V "Low\_Voltage\_EC" peripheral component all unstuff.

11/05 Modify

- 01. Page 25 : C118 connect with GND\_AUD.
- 02. Page 10 : R101 unsuff.
- 03. Page 11 : C889/C881 stuff;C646/C720 change value to 10U-6.3V-06R.
- 04. Page 16 : R638 change value to 2.2K-04;R641 change value to 1K-04;
- 05. Page 16 : U8 unstuff.
- 06. Page 13 : R225 stuff.
- 07. Page 26 : R807/R889 stuff;Y5/R890/C897/C898 unstuff.
- 08. Page 11 : CN13 chane value to DDR-8795-00L4-4280.
- 09. Page 11 : CN10 chane value to DDR-8795-00L4-0180.
- 10. Page 26 : CN14 chane value to ???31AK01910-00.
- 11. Page 21 : CN15 chane value to CON-HDMI-879F-0019-H380.
- 12. Page 25 : Add C900.

11/08 Modify

- 01. Page 13 : R723 unstuff.
- 02. Page 13 : PC60/PC56 stuff.
- 03. Page 35 : PC819/PC820 change value to 22N-16-04X-K.
- 04. Page 33 : PC833 change value to 2200P-50-06X.
- 05. Page 35 : PR629 change value to 1K-1-04.
- 06. Page 32 : PU4/PU5 change value to APL1084UC-HF.
- 07. Page 35 : PU505 change value to OZ8117LN.
- 08. Page 25 : U509/VU1/U4/U5/U7/U9/U11/VU501/VU502/VU503 change value to 74AHC1G08-HF.
- 09. Page 24 : U13 change value to PM25LV512A-100SCE-HF.
- 10. Page 26 : U510 change value to RTS5159-HF.
- 11. Page XX : U508/U505/U30 change value to UP7534ARA8-15-HF.
- 12. Page 35 : PC811 unstuff;PQ531/PQ532 change value to FET-AON6788. (For 25W)
- 13. Page 12 : R150/R142/R159 unstuff.

11/09 Modify

- 01. Page XX : U10 change value to ??702A650001-12.
- 02. Page 11 : C734/C643 stuff.
- 03. Page 22 : CN30 unstuff.

Power Schematics Modify