AMD AM4

MICRO-STAR INT'L CO.,LTD

MS-7B78

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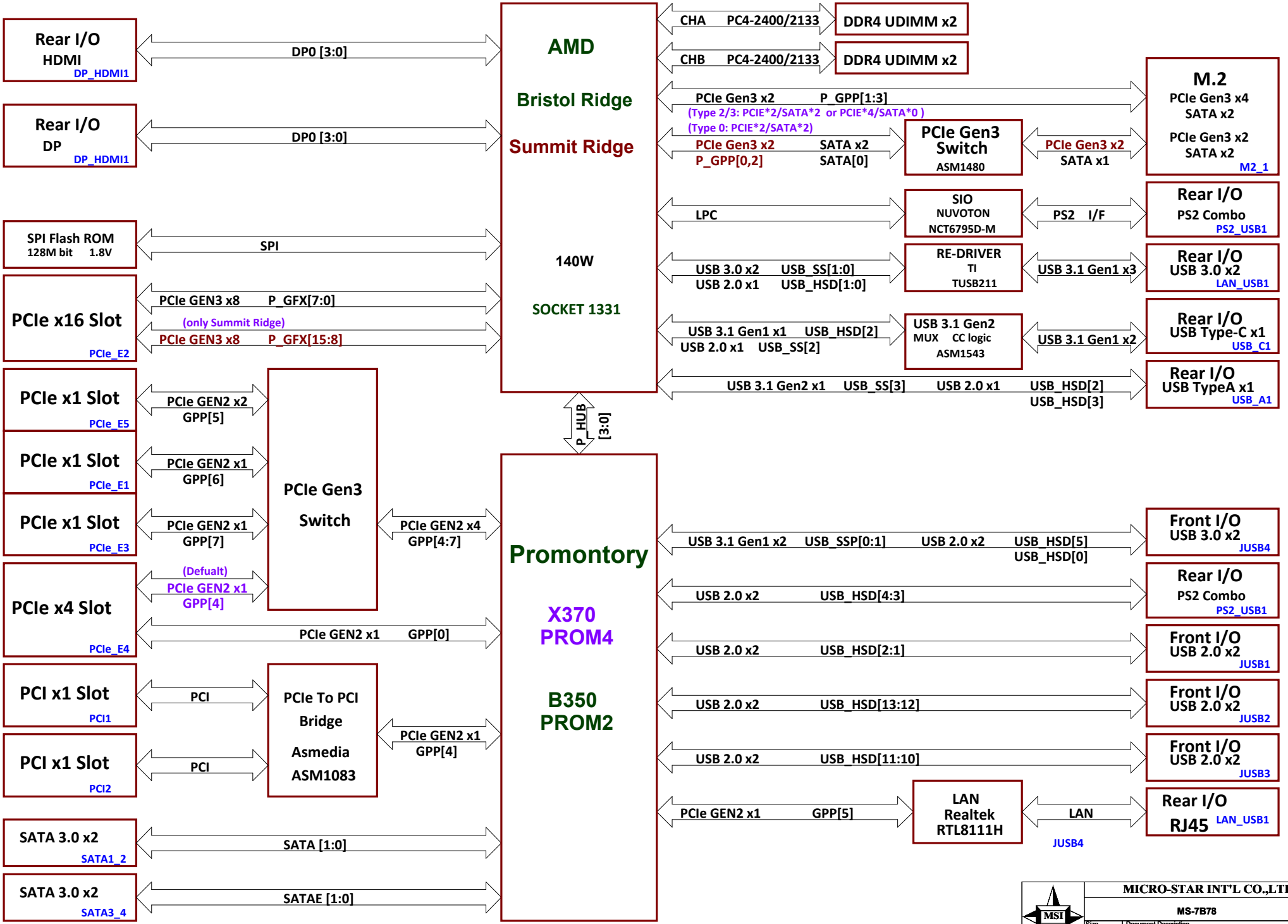

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Size: Custom	Document Description: Block Diagram
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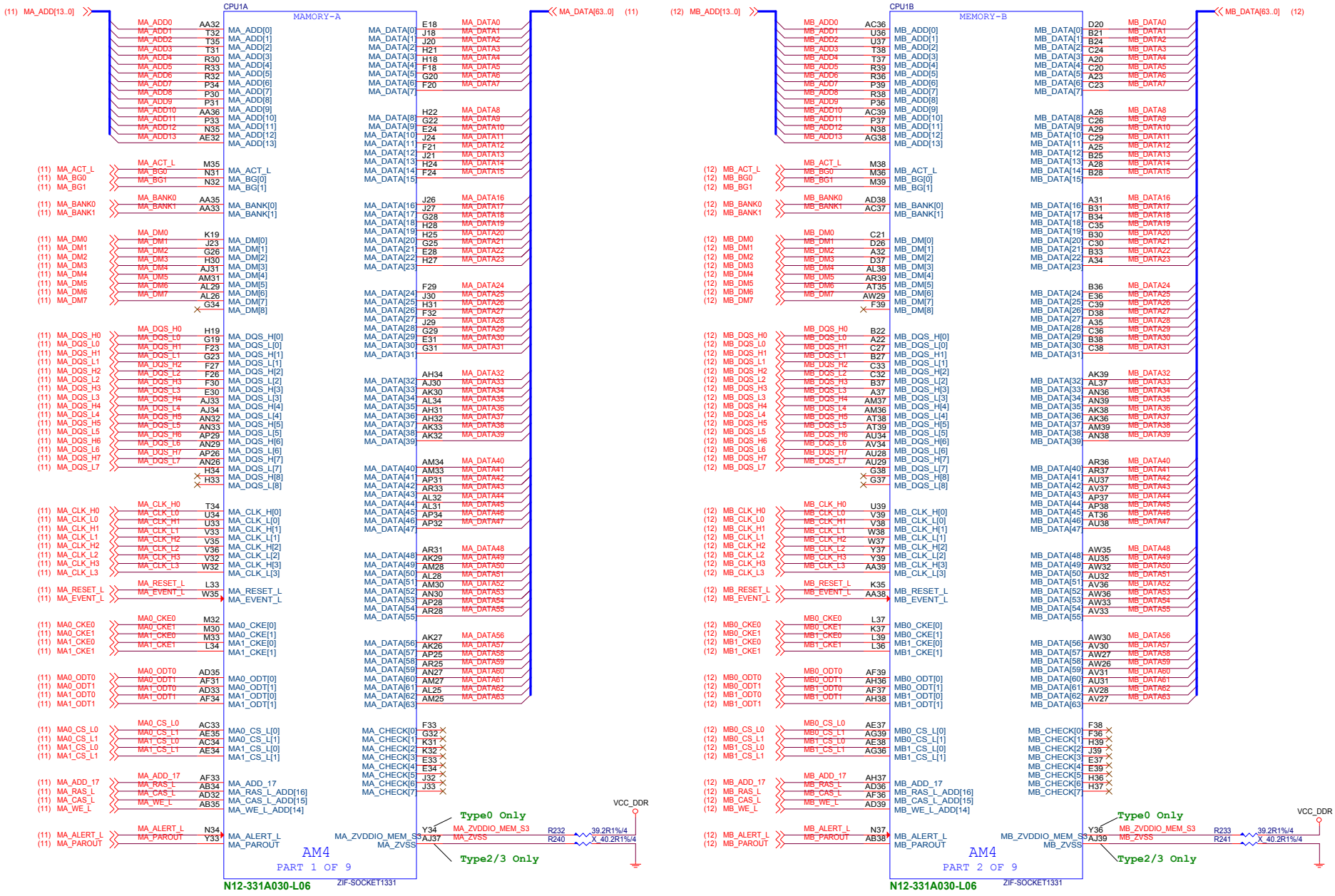

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Custom	AM4 DDR4 I/F	10

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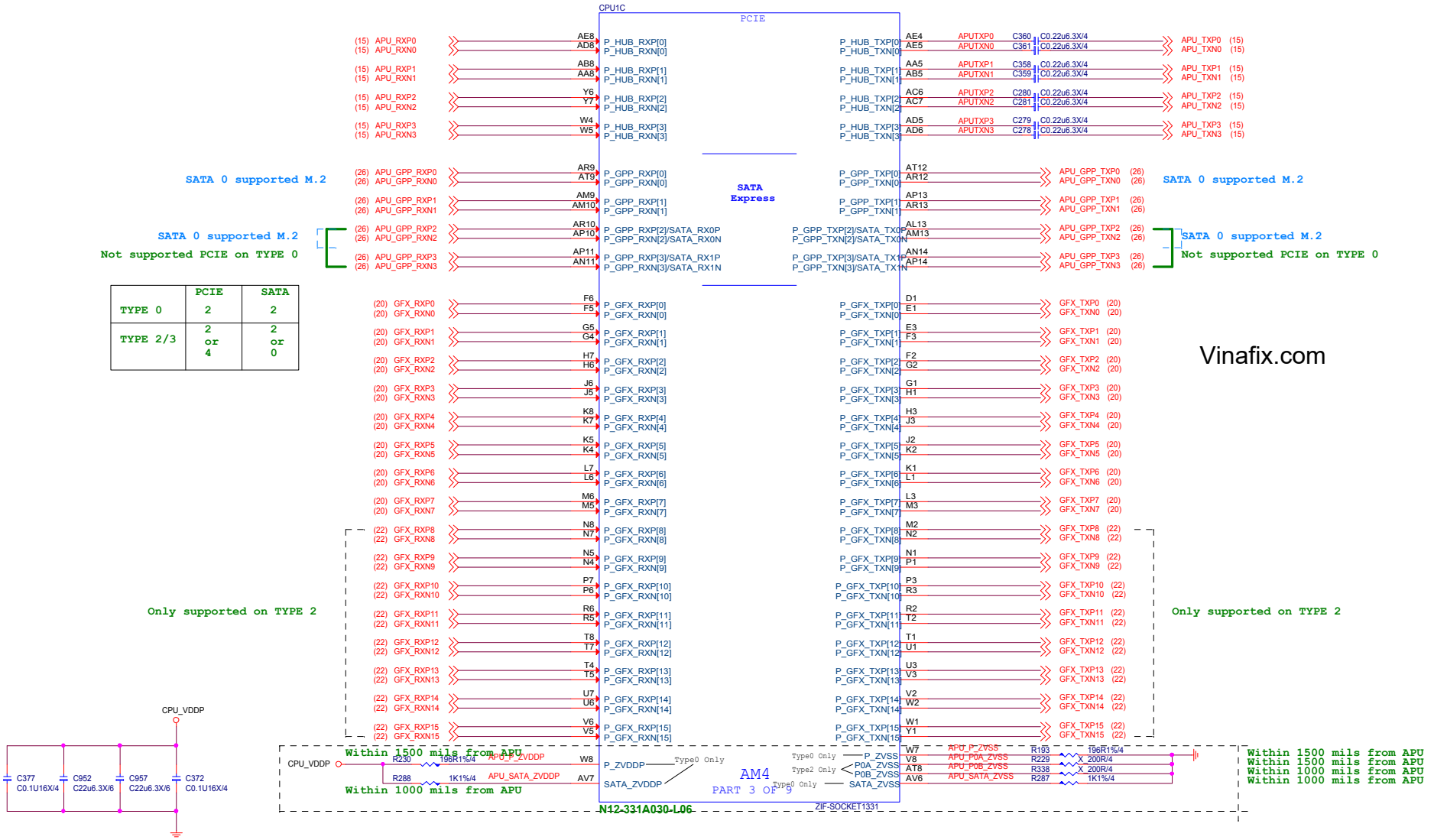

	PCIE	SATA
TYPE 0	2	2
TYPE 2/3	2 or 4	2 or 0

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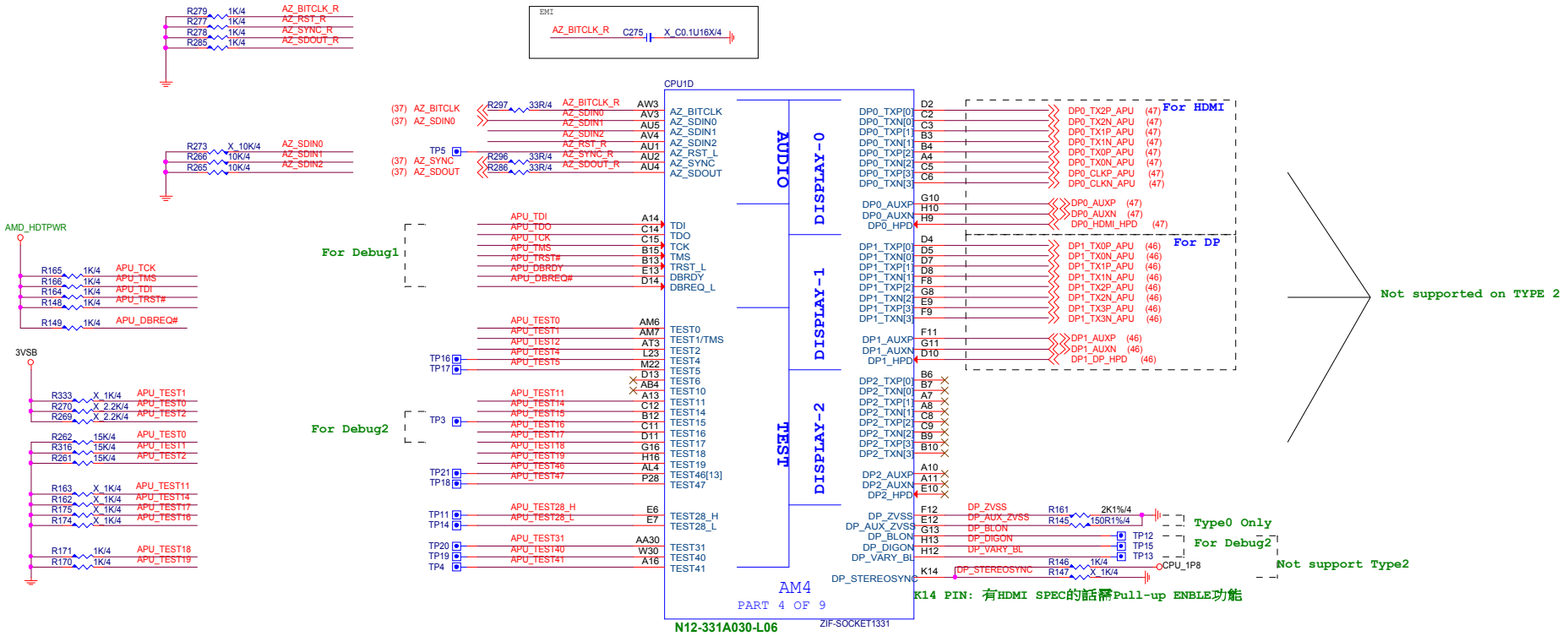
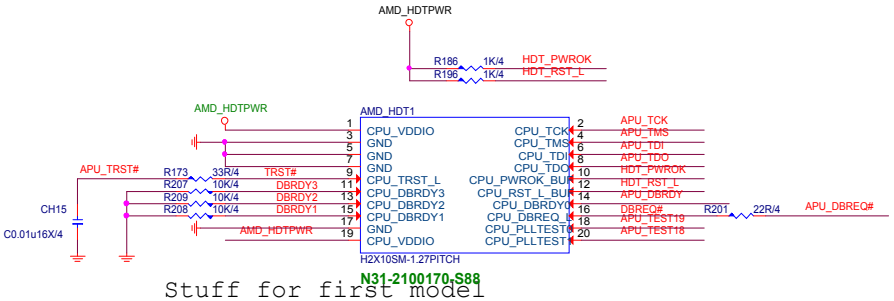
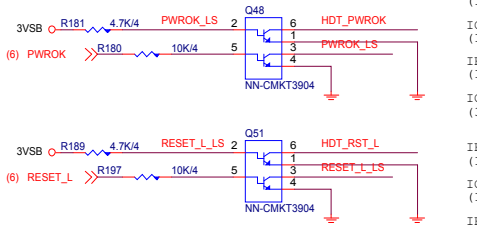






IB=(AMD_HDTPWR-Vbe)/4.7k
(1.8-0.95)/4.7k=0.181mA

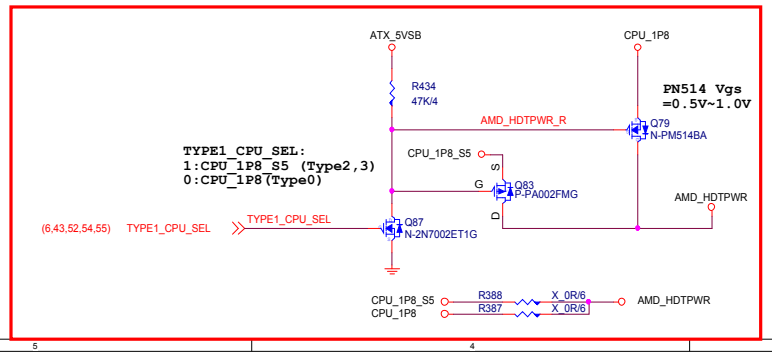
IC=(Vc-Vce)/10k
(1.8-0.2)/10k=0.16mA

B*Ib>Ic=10*0.181=1.81>0.16

IB=(Vb-Vbe)/10k
(1.75-0.95)/10k=0.08mA

IC=(Vc-Vce)/10k
(3.3-0.2)/10k=0.16mA

B*Ib>Ic=10*0.08=0.8>0.16



IB=(AMD_HDTPWR-Vbe)/4.7k
(1.8-0.95)/4.7k=0.181mA

IC=(Vc-Vce)/10k
(1.8-0.2)/10k=0.16mA

B*Ib>Ic=10*0.181=1.81>0.16

IB=(Vb-Vbe)/10k
(1.75-0.95)/10k=0.08mA

IC=(Vc-Vce)/10k
(3.3-0.2)/10k=0.16mA

B*Ib>Ic=10*0.08=0.8>0.16

MICRO-STAR INT'L CO.,LTD

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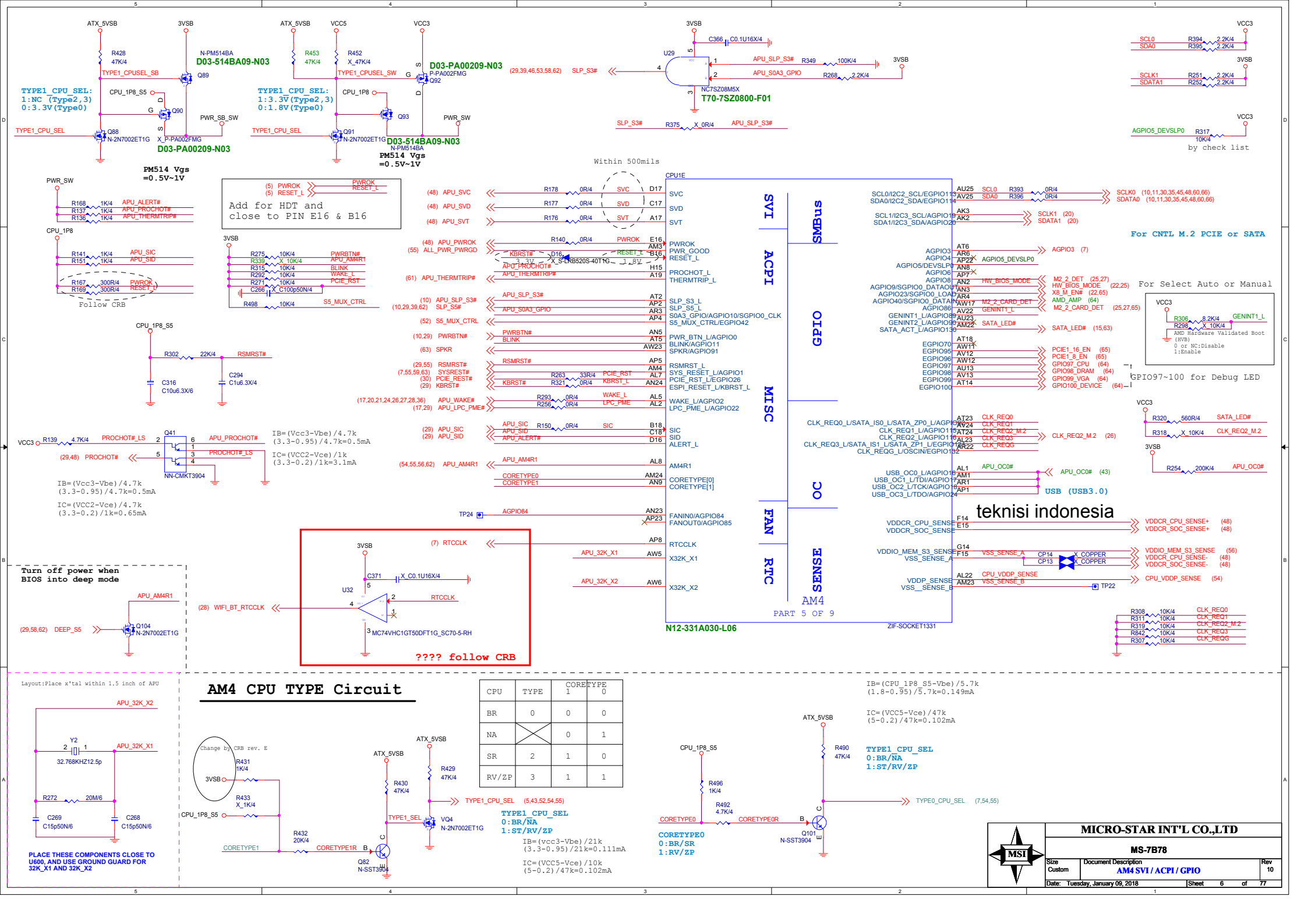

CPU	TYPE	CORETYPE 1	CORETYPE 0
BR	0	0	0
NA	X	0	1
SR	2	1	0
RV/ZP	3	1	1

Size	Custom
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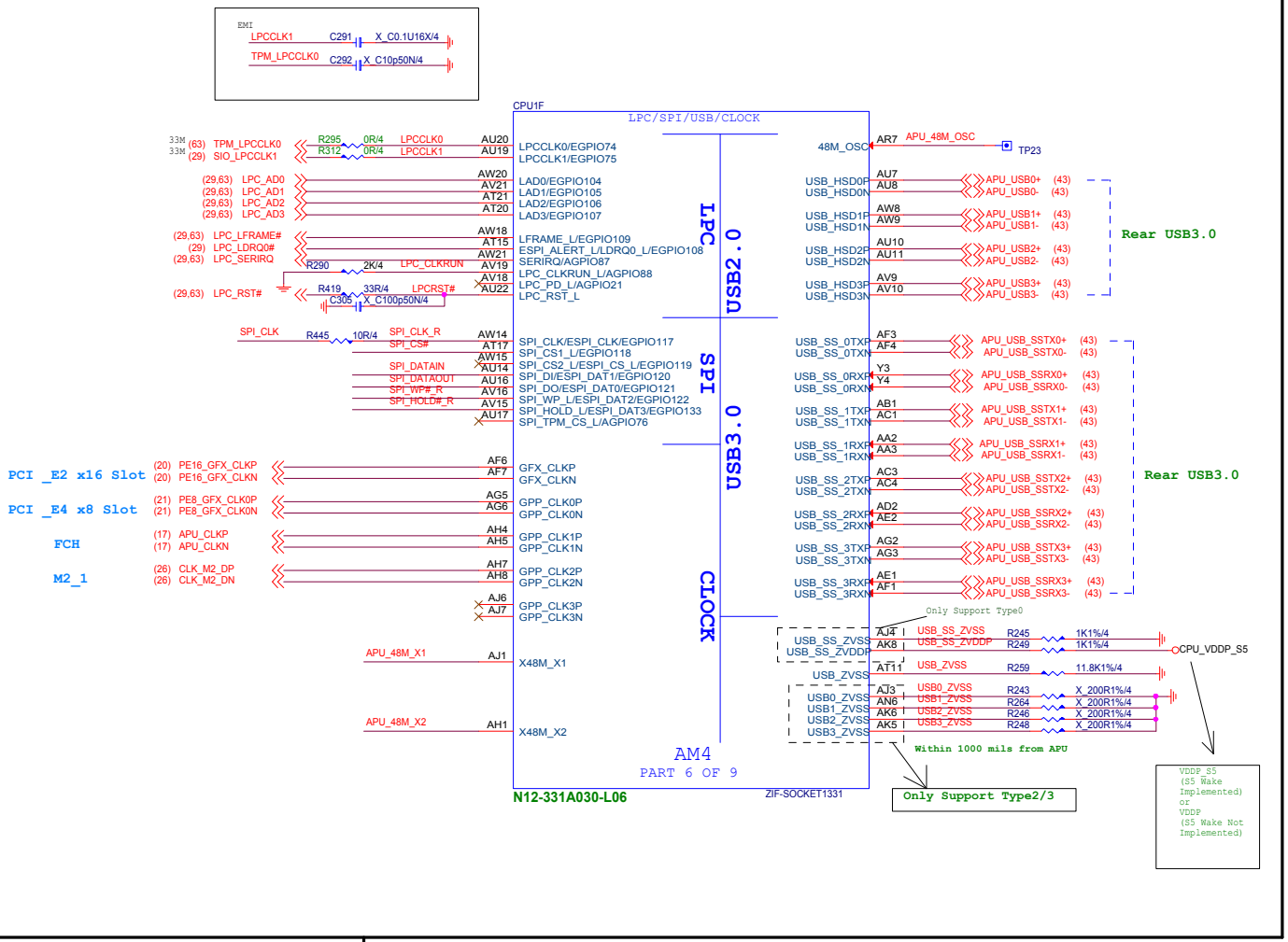
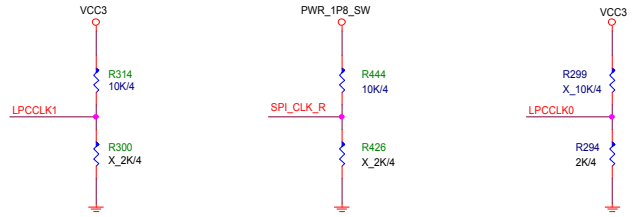
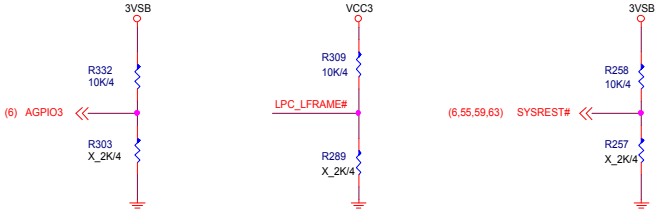


Strapping Options

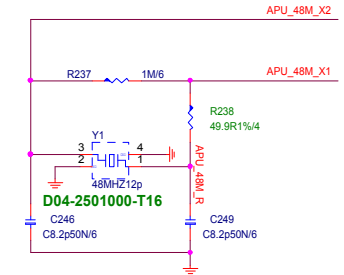


	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	LPC device Boot Fail Timer Enabled
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC device Boot Fail Timer Disabled (Default)



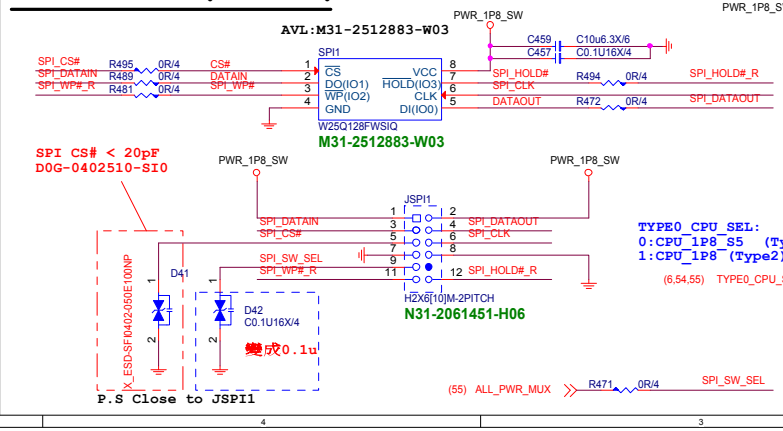
	AGPIO3	SIO_LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

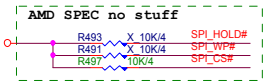
Layout:Place x'tal within 1.5 inch of APU

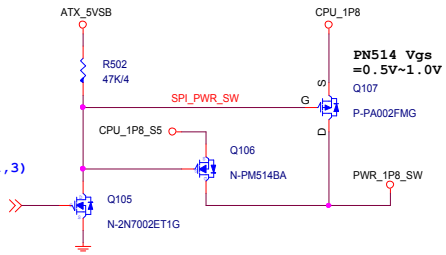


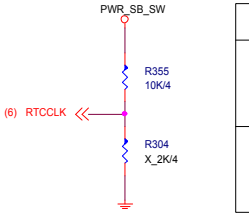
PLACE THESE COMPONENTS CLOSE TO U600, AND USE GROUND GUARD FOR48M_X1 AND 48M_X2

SPI ROM(1.8V)









	RTCCLK
PULL HIGH	RTC Coin Battery is on board (Default)
PULL LOW	RTC Coin Battery is not on board

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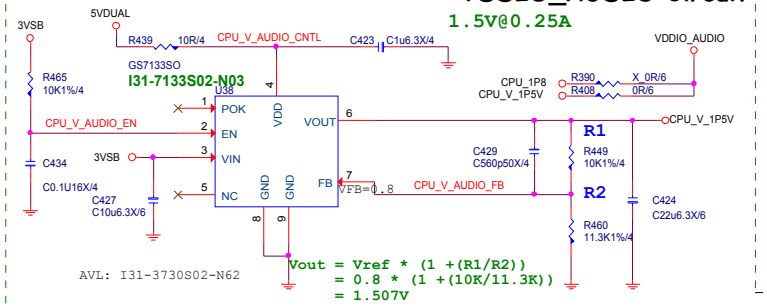
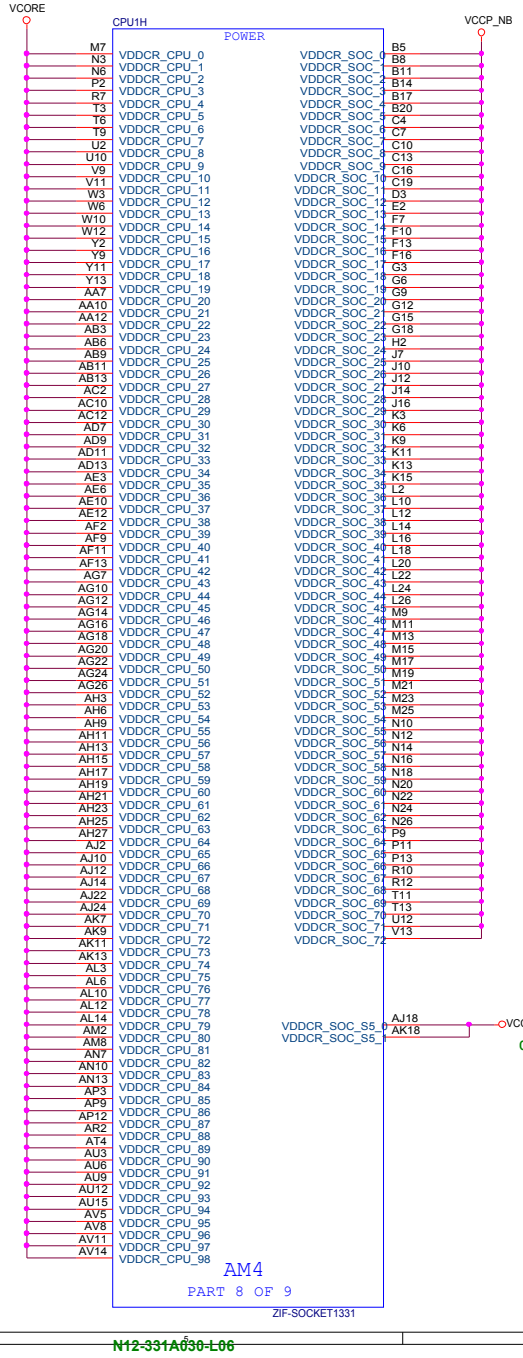
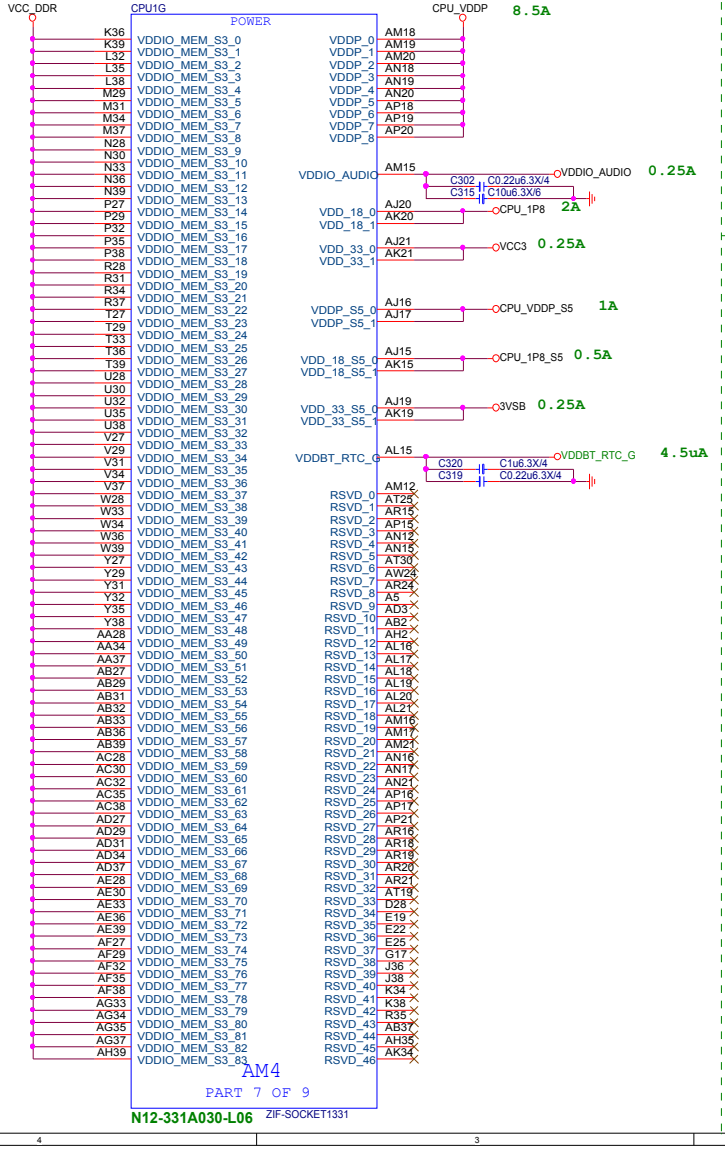
VDDIO_AUDIO Circuit

1.5V@0.25A

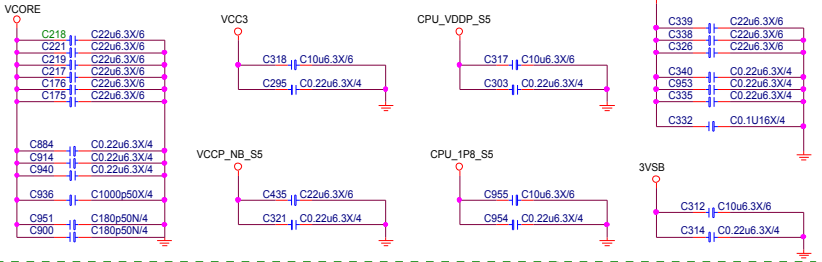


Vinafix.com

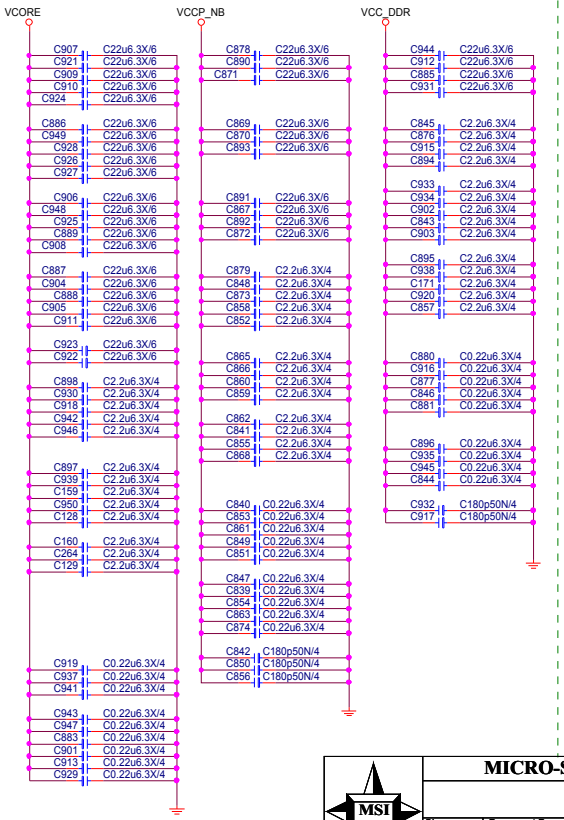




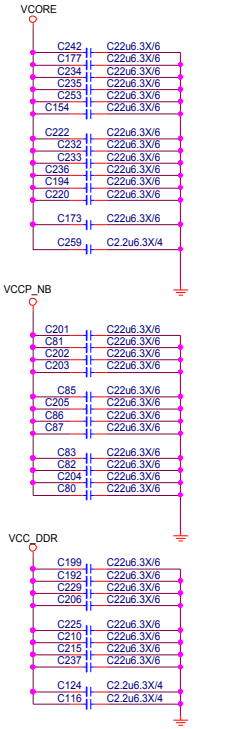
TOP SIDE



BOTTOM SIDE



TOP CAVITY



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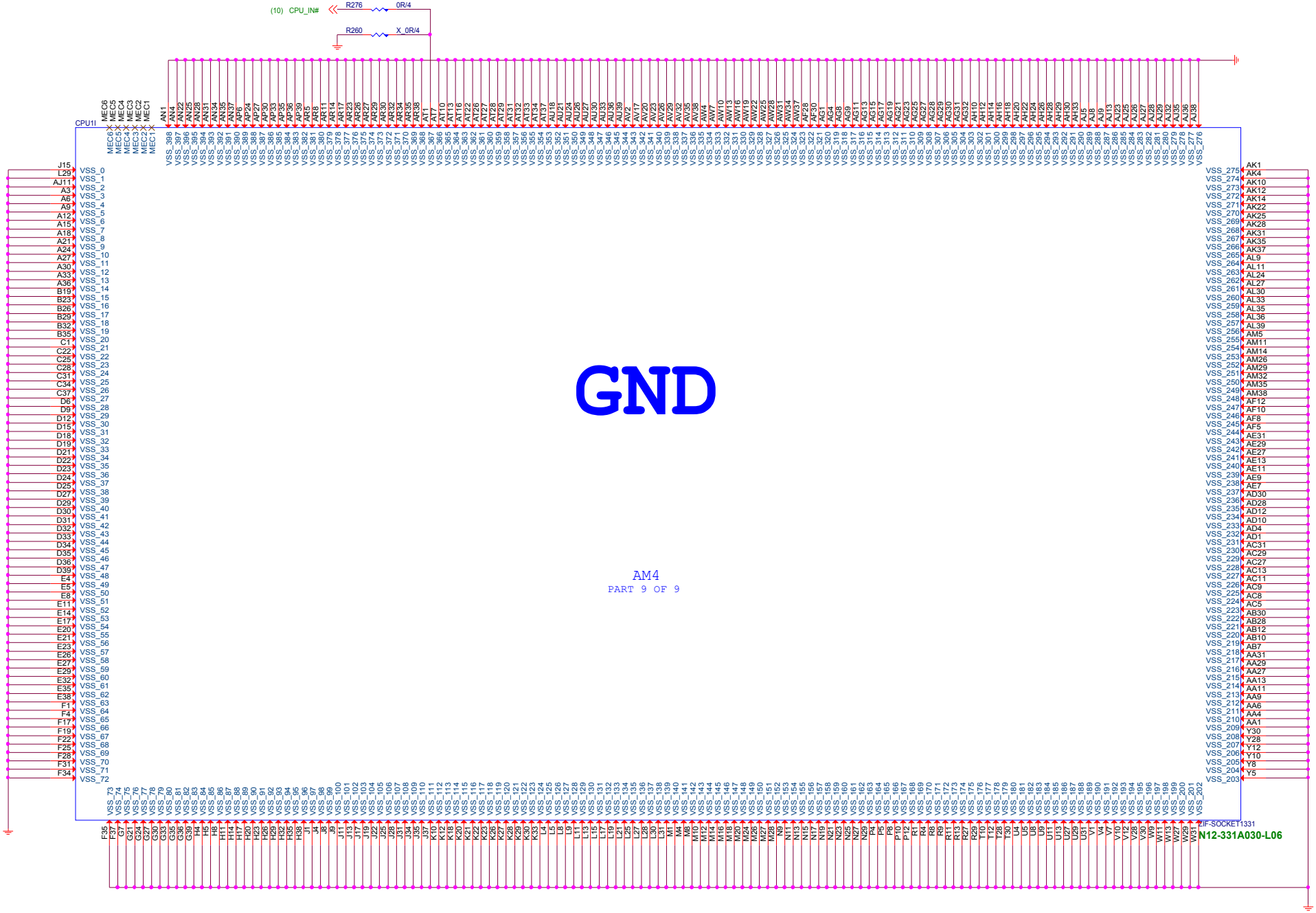

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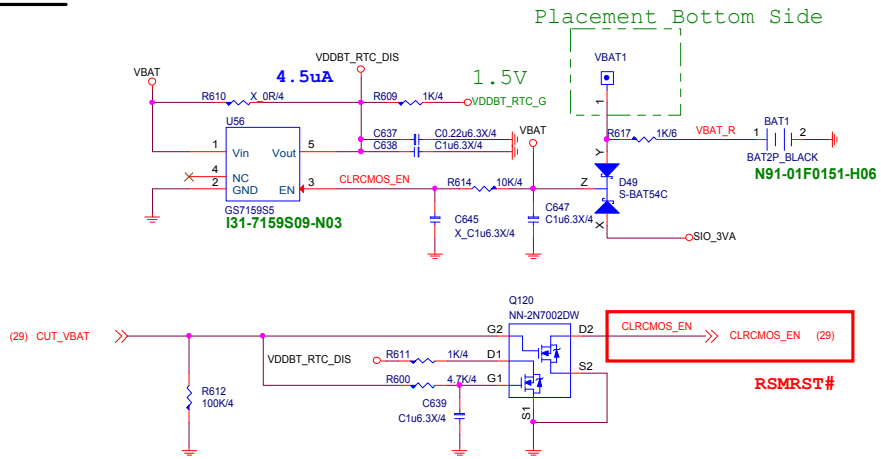
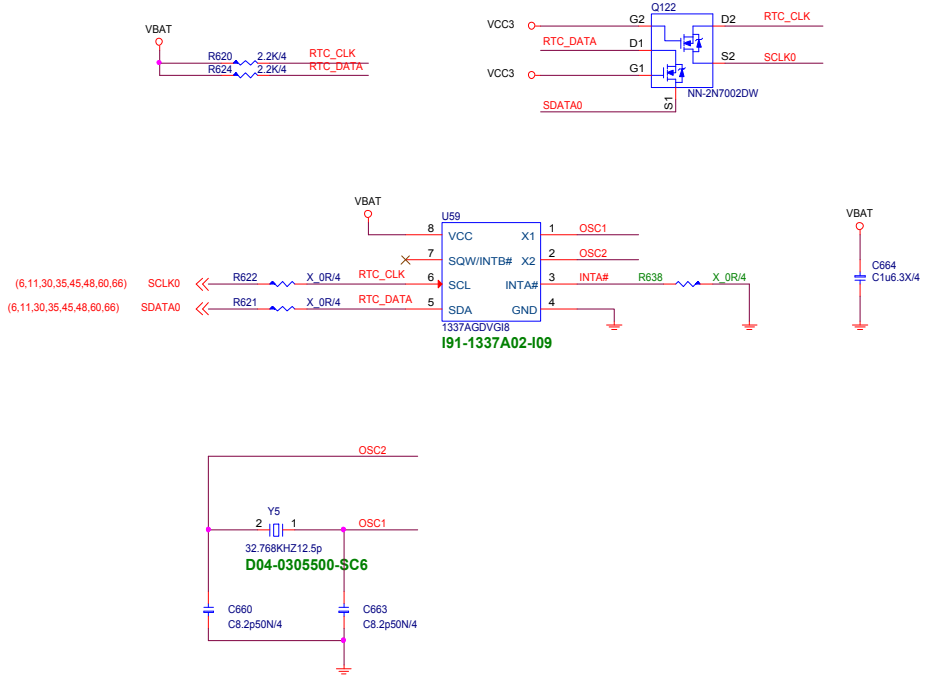
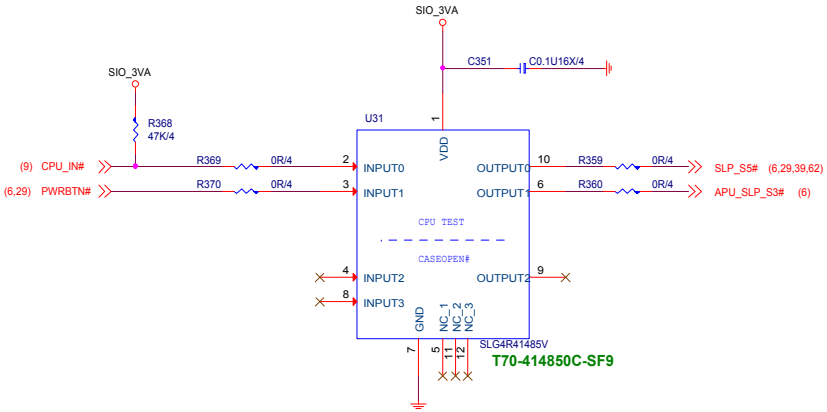
RTC & Clear CMOS Circuit



RTC Backup



Clear CMOS button



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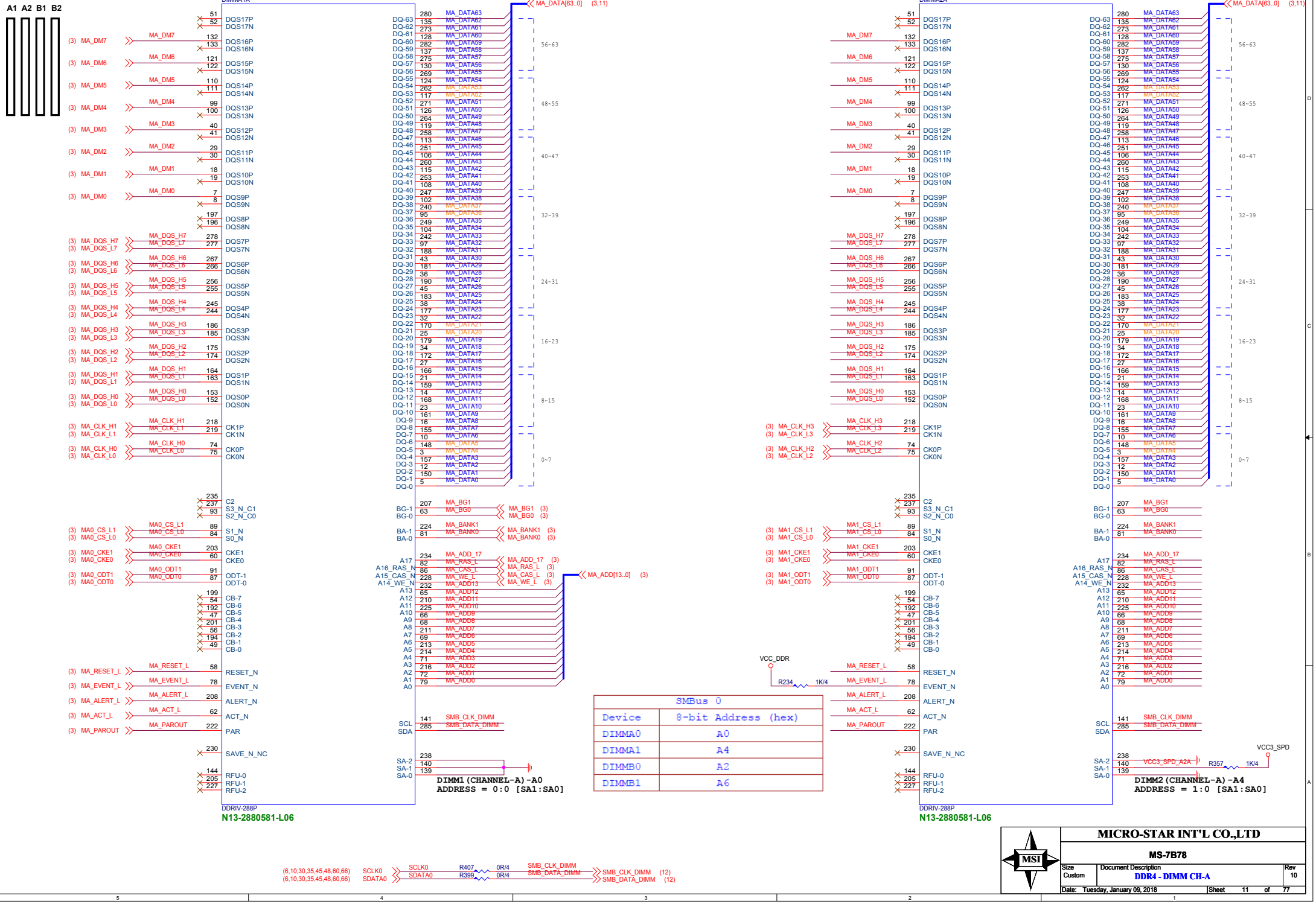
A1 A2 B1 B2
DIMMA1A
DIMMA2A
MA_DATA[63..0] (3,11)
MA_ADD[13..0] (3)
DDRIV-288P
N13-2880581-L06
VCC_DDR
R234 1K/4
VCC3_SPD
R357 1K/4
VCC3_SPD_A2A
SMBus 0
Device | 8-bit Address (hex)
DIMMA0 | A0
DIMMA1 | A4
DIMMB0 | A2
DIMMB1 | A6
DIMM1(CHANNEL-A)-A0
ADDRESS = 0:0 [SA1:SA0]
DIMM2(CHANNEL-A)-A4
ADDRESS = 1:0 [SA1:SA0]
(6,10,30,35,45,48,60,66) SCLK0 SCLK0 R407 0R/4 SMB_CLK_DIMM SMB_CLK_DIMM (12)
(6,10,30,35,45,48,60,66) SDATA0 SDATA0 R399 0R/4 SMB_DATA_DIMM SMB_DATA_DIMM (12)
MICRO-STAR INT'L CO.,LTD
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Document Description DDR4 - DIMM CH-A
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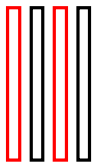

DIMMB1A

DIMMB2A

DDRIV-288P

N13-2880581-L06

DIMM3(CHANNEL-B)-A2
ADDRESS = 0:1 [SA1:SA0]

DIMM4(CHANNEL-B)-A6
ADDRESS = 1:1 [SA1:SA0]

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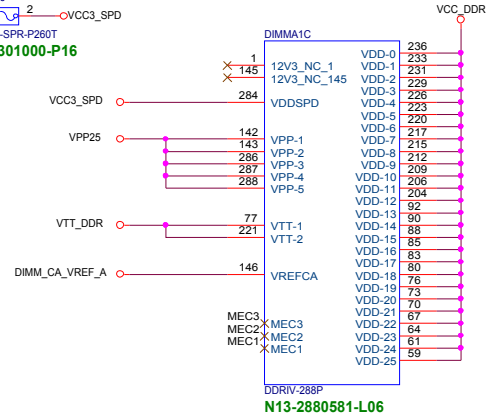
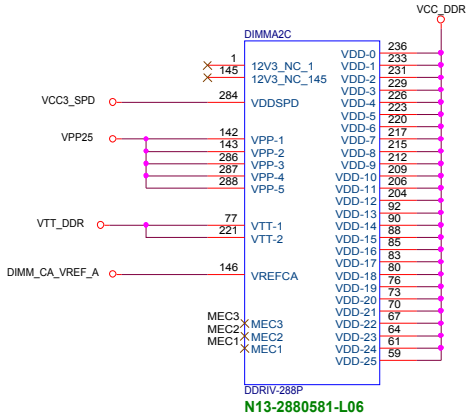
avl:D08-0301100-B07

F6
VCC3 1 2 VCC3_SPD
F-SPR-P260T
D08-0301000-P16

DIMM SLOT PN BY SPEC



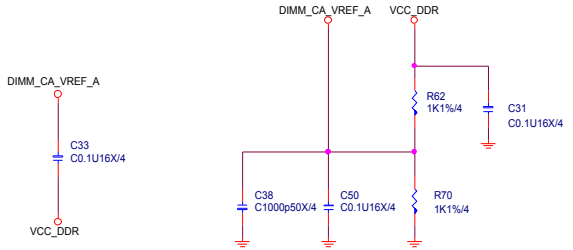
N13-2880581-L06



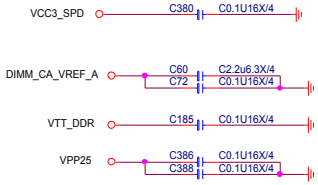
N13-2880581-L06

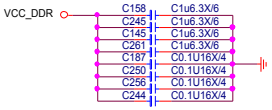
DDR VREF

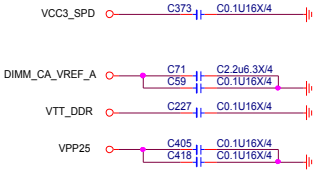
(place resistors close to DIMMs)

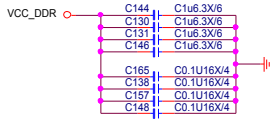


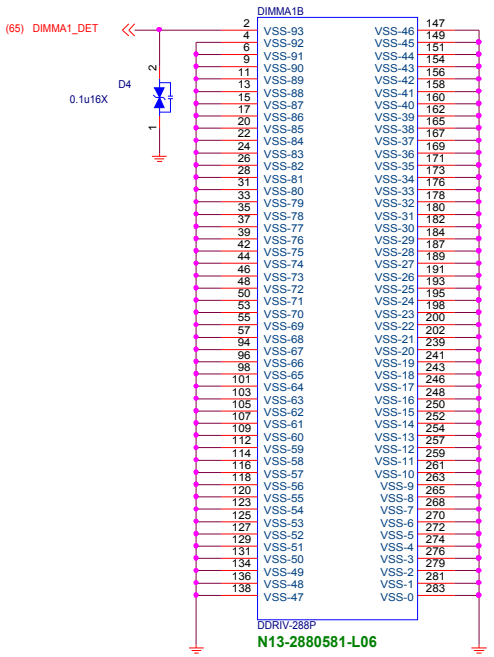
Vinafix.com



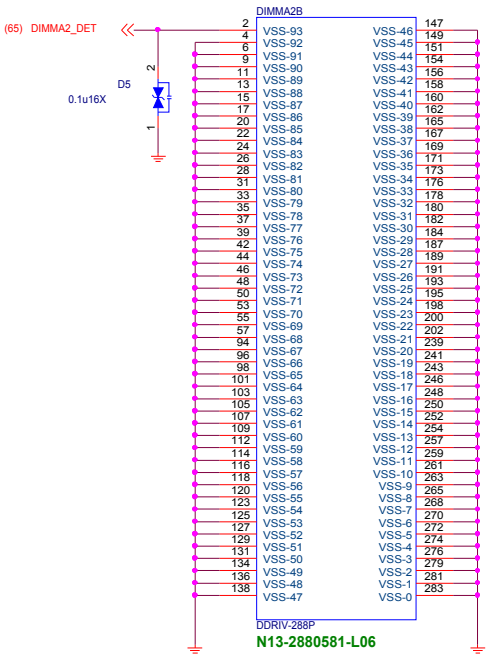








N13-2880581-L06



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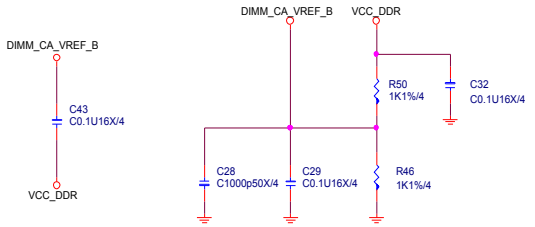
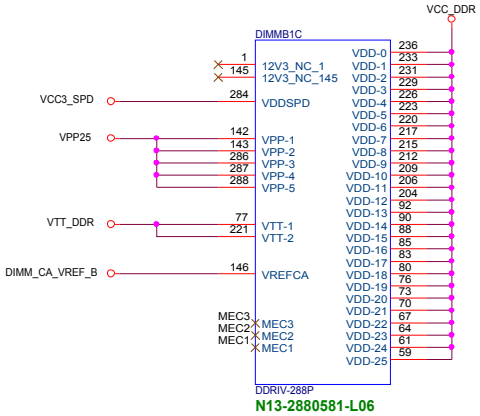
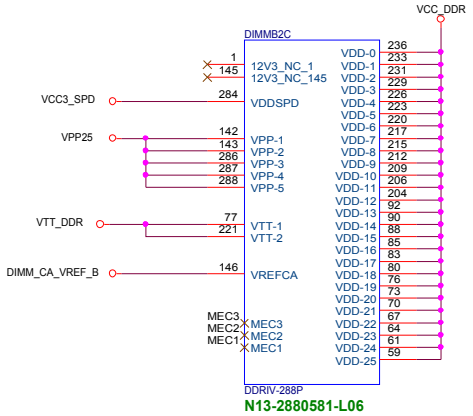
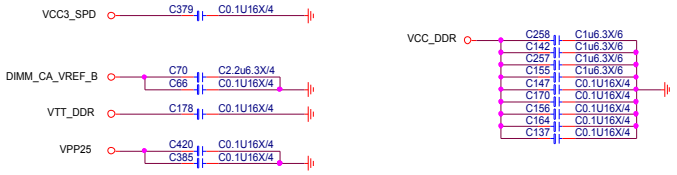
DDR VREF

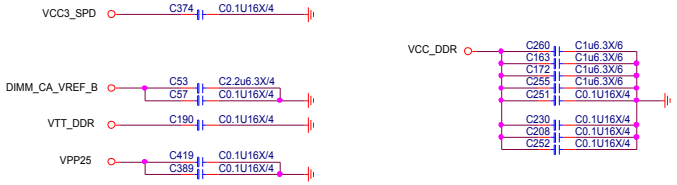
(place resistors close to DIMMs)

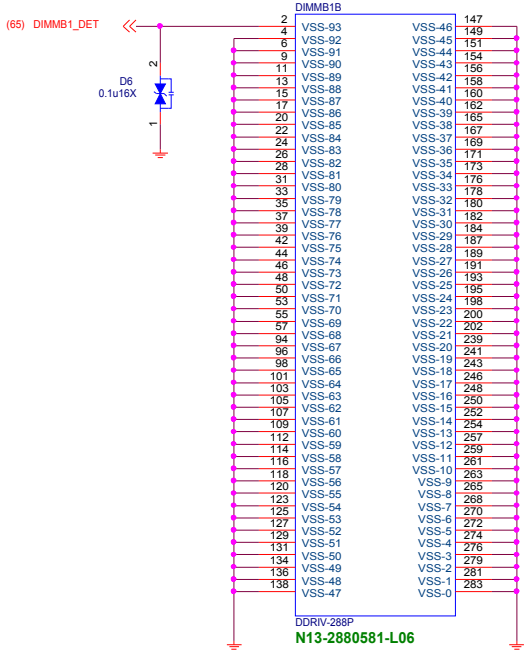


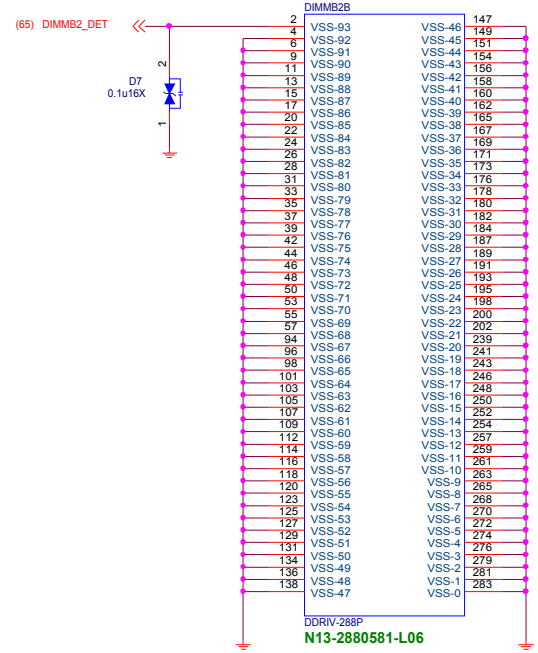












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Custom	DDR4 - POWER/GND-2	10

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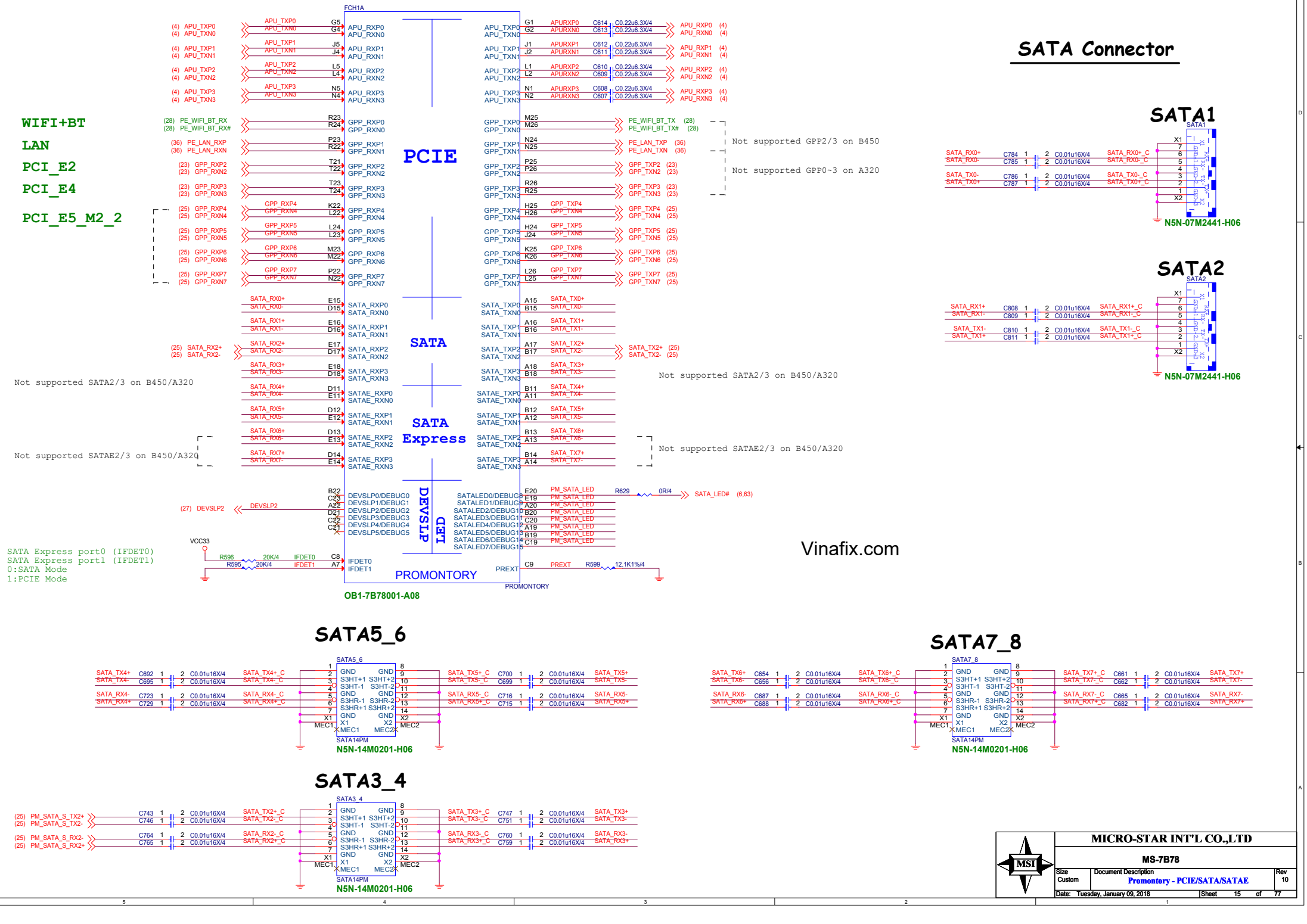
SATA Connector
SATA1
SATA2
SATA5_6
SATA7_8
SATA3_4
WIFI+BT
LAN
PCI_E2
PCI_E4
PCI_E5_M2_2
PCIE
SATA
SATA Express
DEVSLP
LED
PROMONTORY
FCH1A
Not supported GPP2/3 on B450
Not supported GPP0~3 on A320
Not supported SATA2/3 on B450/A320
Not supported SATAE2/3 on B450/A320
SATA Express port0 (IFDET0)
SATA Express port1 (IFDET1)
0:SATA Mode
1:PCIE Mode
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OB1-7B78001-A08
N5N-07M2441-H06
N5N-14M0201-H06
MICRO-STAR INT'L CO.,LTD
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Promontory - PCIE/SATA/SATAE
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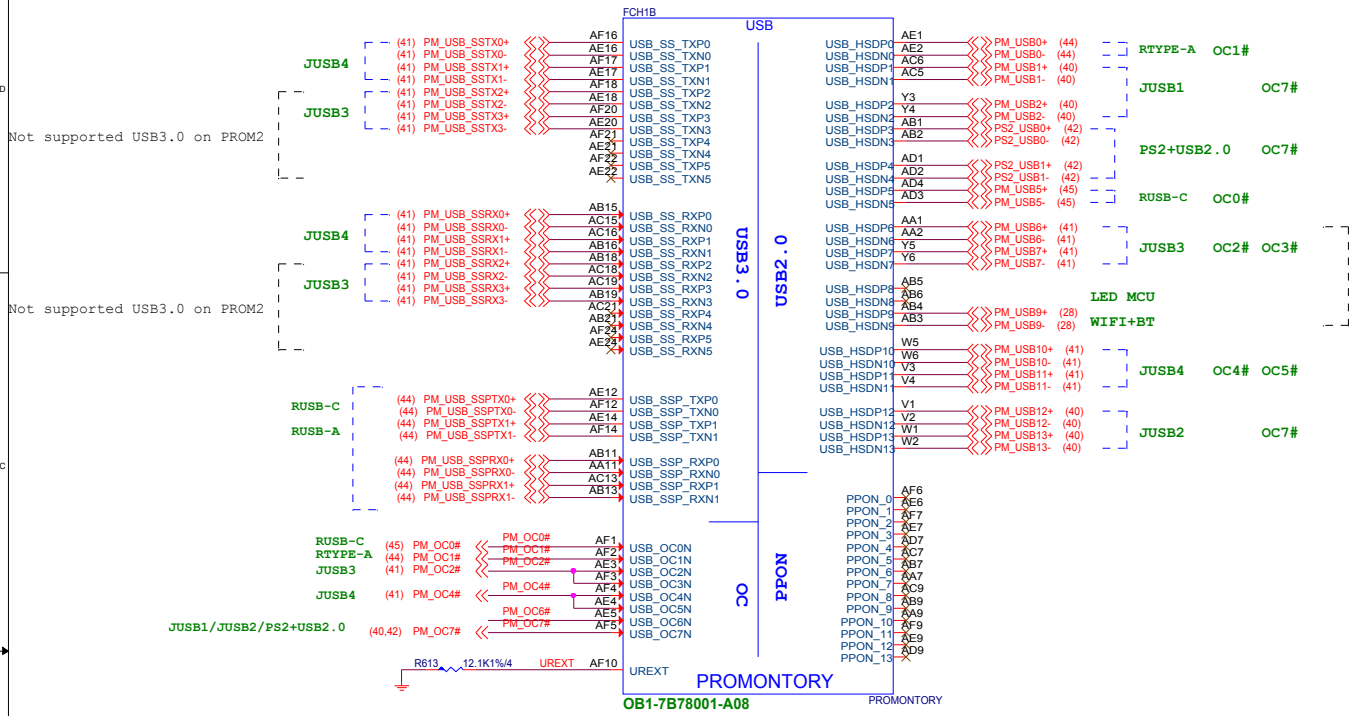

Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	**USB2.0**	**USB_OC**
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

CLK2.3不能用
CLK1-3不能用

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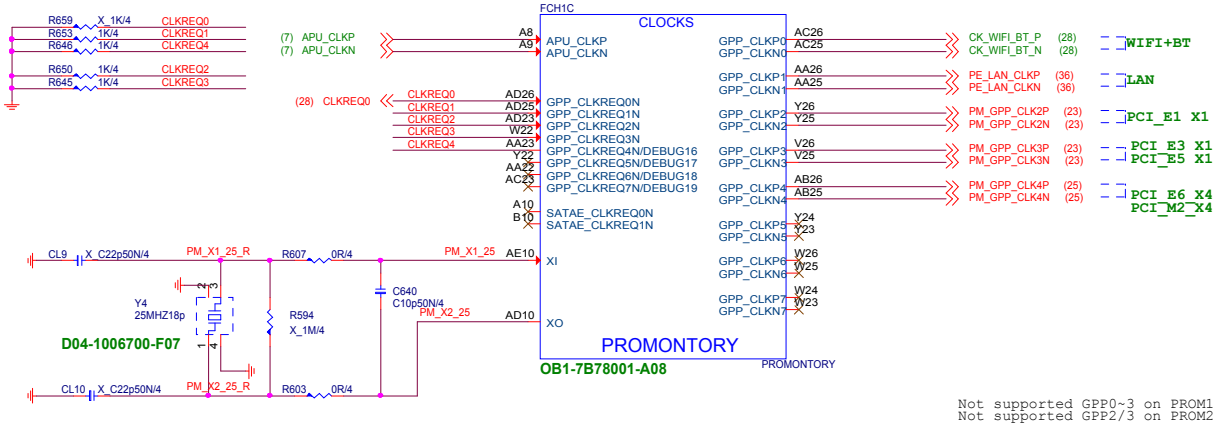
GPP Clock	CLKREQ#
GPP_CLKP/N[0]	GPP_CLKREQ0N
GPP_CLKP/N[1]	GPP_CLKREQ1N
GPP_CLKP/N[2]	GPP_CLKREQ2N
GPP_CLKP/N[3]	GPP_CLKREQ3N
GPP_CLKP/N[4]	GPP_CLKREQ4N
GPP_CLKP/N[5]	GPP_CLKREQ5N
GPP_CLKP/N[6]	GPP_CLKREQ6N
GPP_CLKP/N[7]	GPP_CLKREQ7N



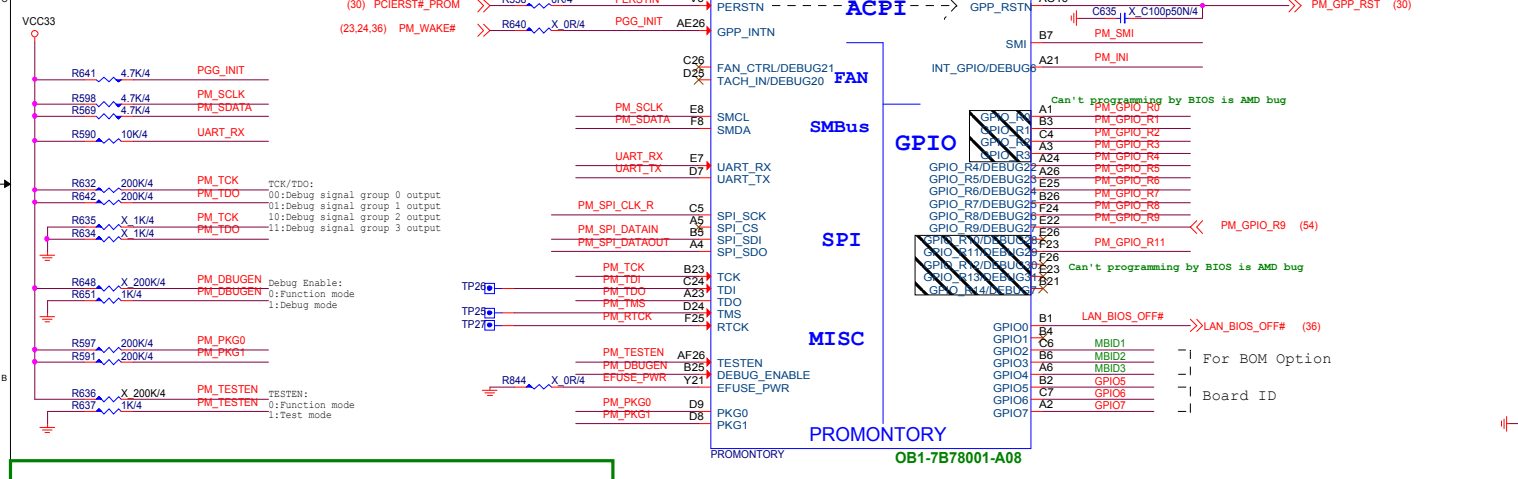
Not supported GPP0~3 on PROM1
Not supported GPP2/3 on PROM2

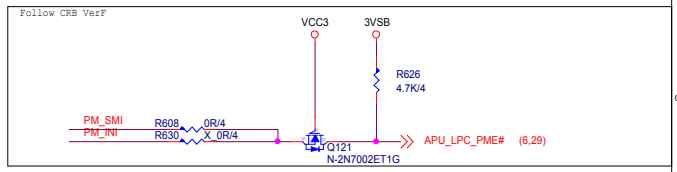
Appendix C Port Mapping for Different Bus Models

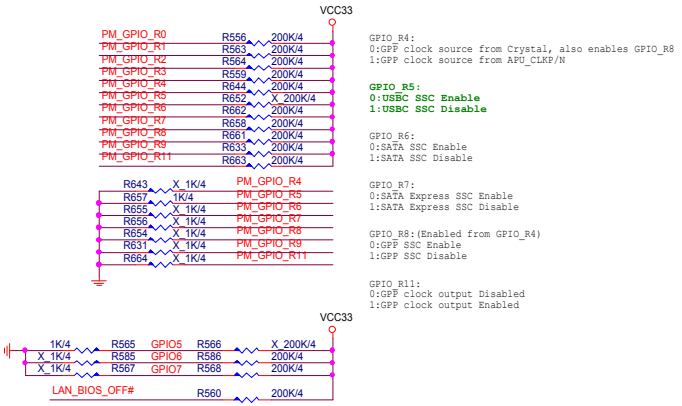
BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

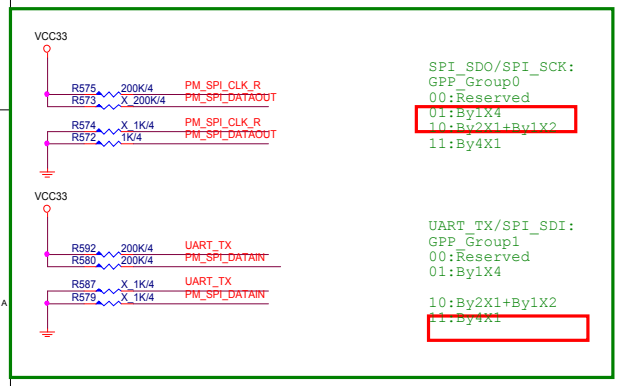
BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

CLK2.3不能用
CLK1-3不能用









	MBID3	MBID2	MBID1
Z470	0	0	0

BOM OPTION

MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: Promontory - CLK/ACPI/GPIO	Rev: 10
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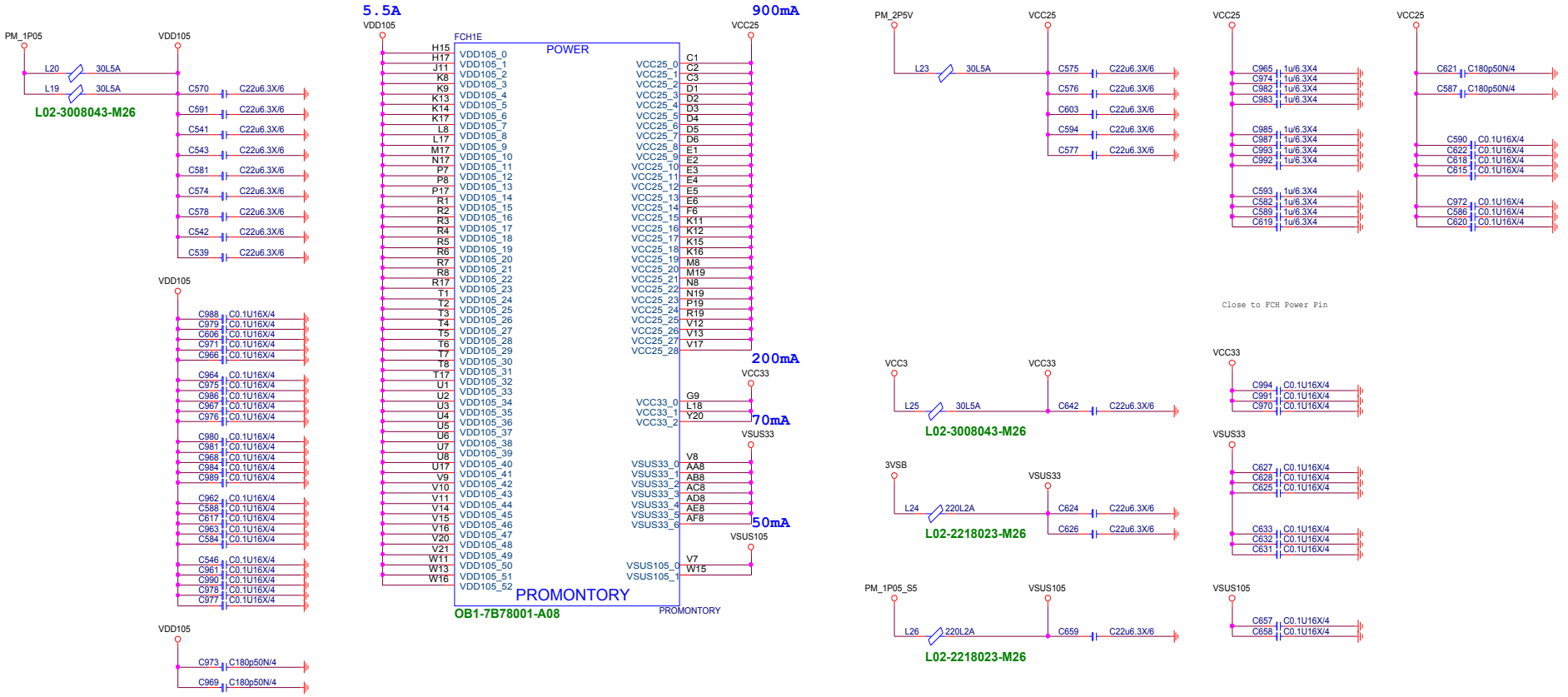

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MS-7B78		
Size: Custom	Document Description: Promontory - Power	Rev: 10
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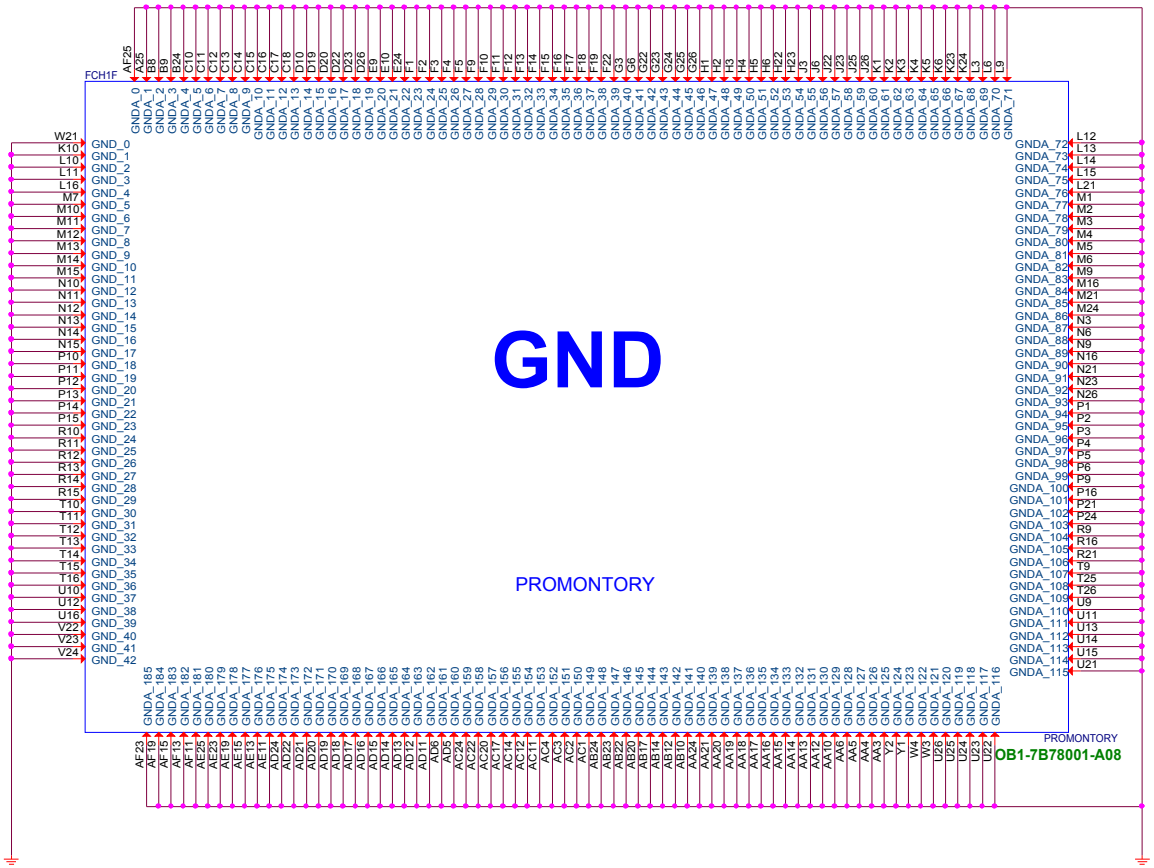

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Size: Custom	Document Description: Promontory - GND	Rev: 10
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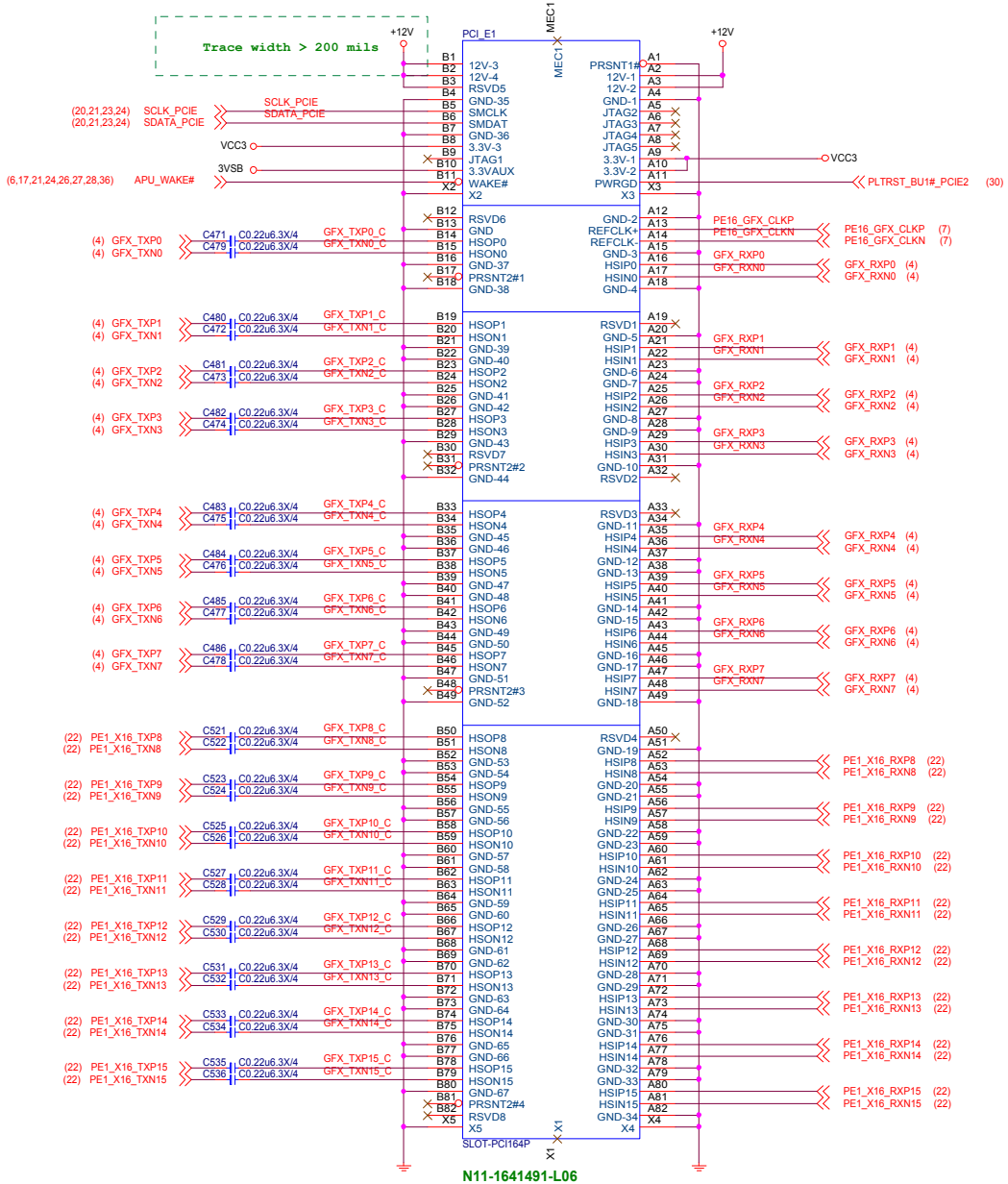
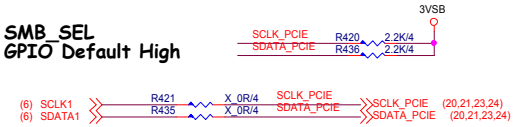
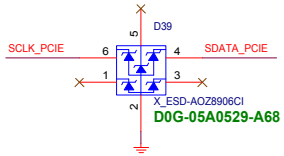
PCI EXPRESS x16 Slot

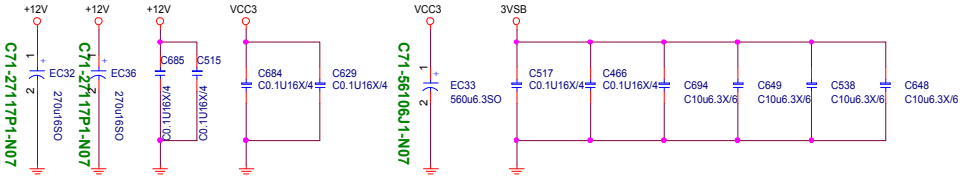
PCI_E1



SMB_SEL
GPIO Default High







PCI Express x16 Slot		
+12V		- 5.5 A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

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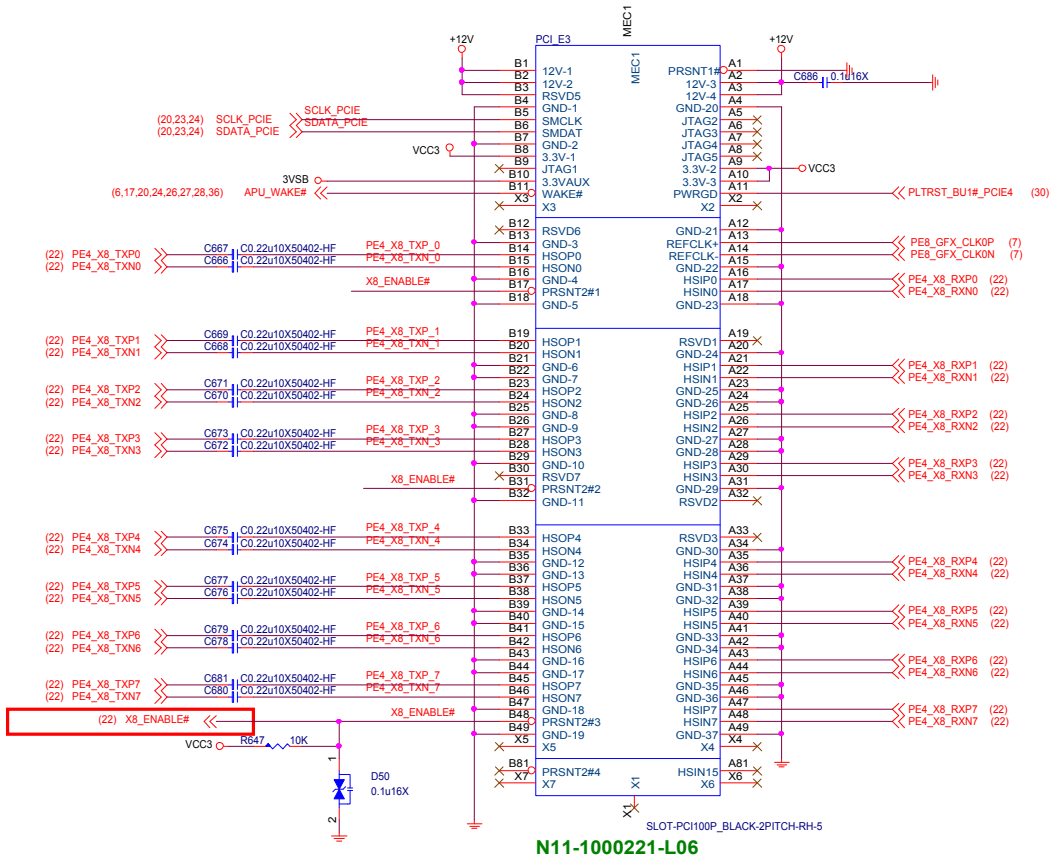
PCI_EXPRESS x8 SLOT

PCI_E3



N11-1000221-L06

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PCI Express x8 Slot		
+12V		- A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

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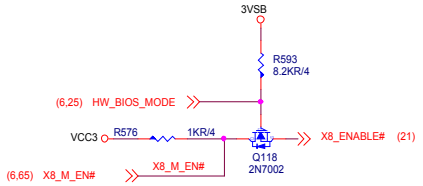
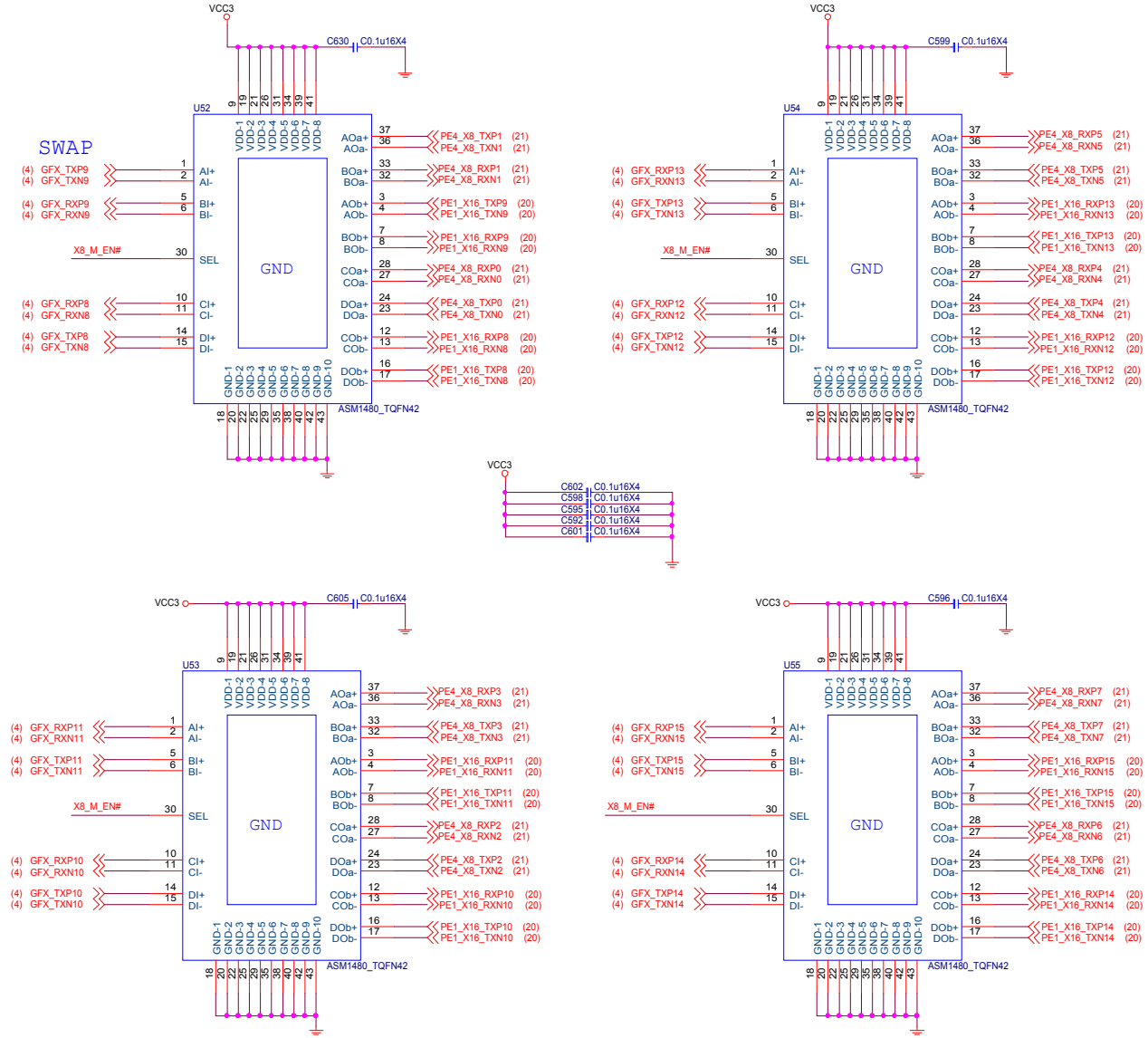
PCI EXPRESS Switch

For PCIE1 & PCIE3

PCIE Lanes control circuit



	HW_BIOS_MODE	X8_M_EN#
Auto	1	1
Manual x16	0	1
Manual x8, x8	0	0



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MS-7B78	
Size: Custom	Document Description: PCIE Switch PE2 / PE4
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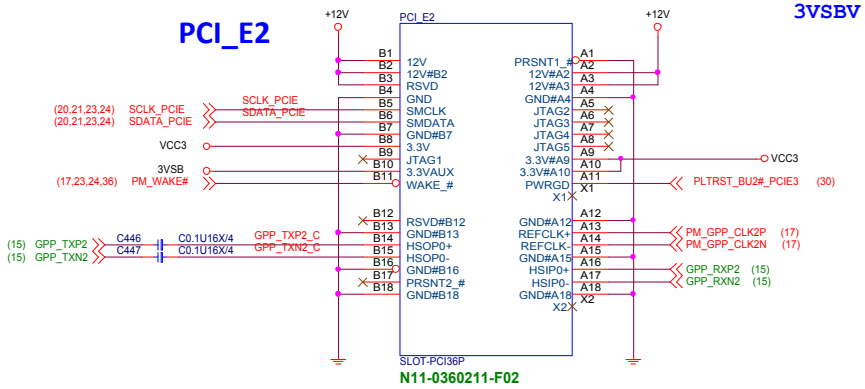
PCI EXPRESS X1 SLOT

12V - 0.5A

VCC3 - 3A

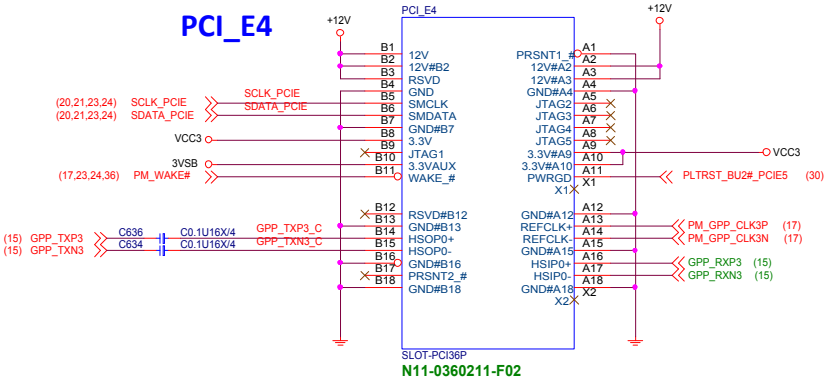
3VSBV - 375mA

PCI_E2



N11-0360211-F02

PCI_E4



N11-0360211-F02

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PCI Express x1 Slot *3		
+12V		- 1.5 A
+VCC3		- 9A
+3V3_S5	(wake)	- 1125mA
+3V3_S5	(no wake)	- 60mA

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Size: Custom	Document Description: PCI_E1_E3_E5 (X1)	Rev: 10
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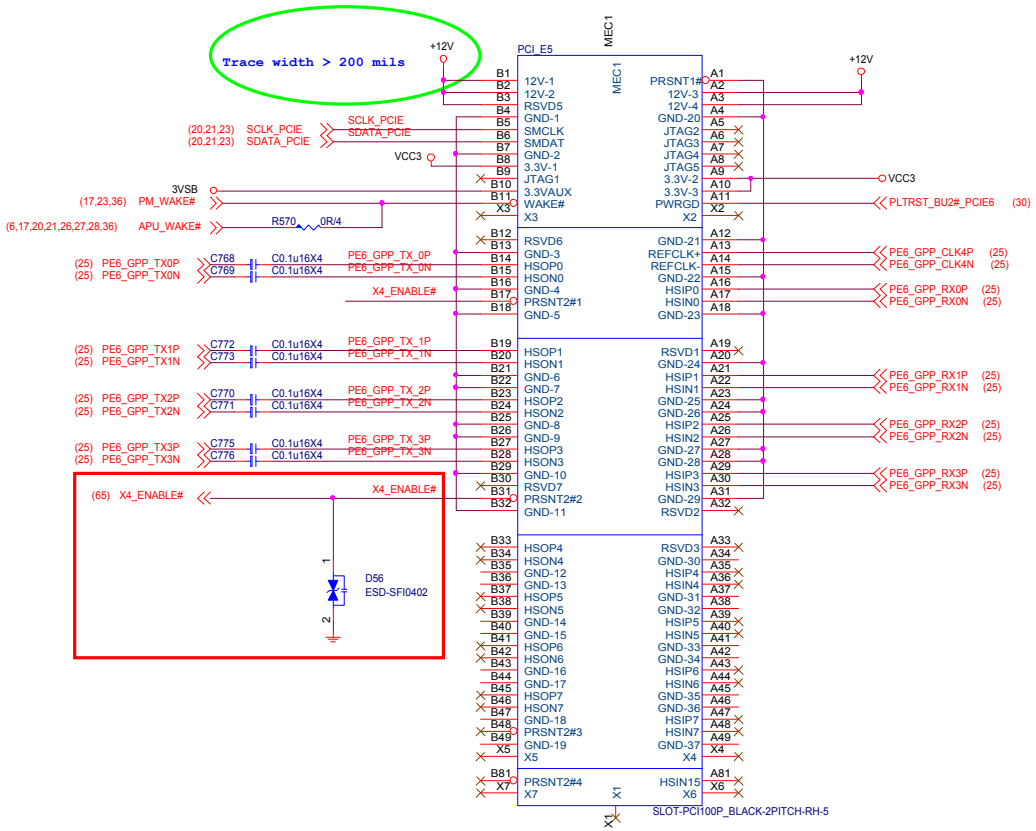
PCI_EXPRESS X4 SLOT

PCI_E6



PCI Express x4 Slot *1		
+12V		- 2.1A
+VCC3		- 3A
+3V3_S5	(wake)	- 375mA
+3V3_S5	(no wake)	- 20mA

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Size: Custom	Document Description: PCI_E6 (X4)	Rev: 10
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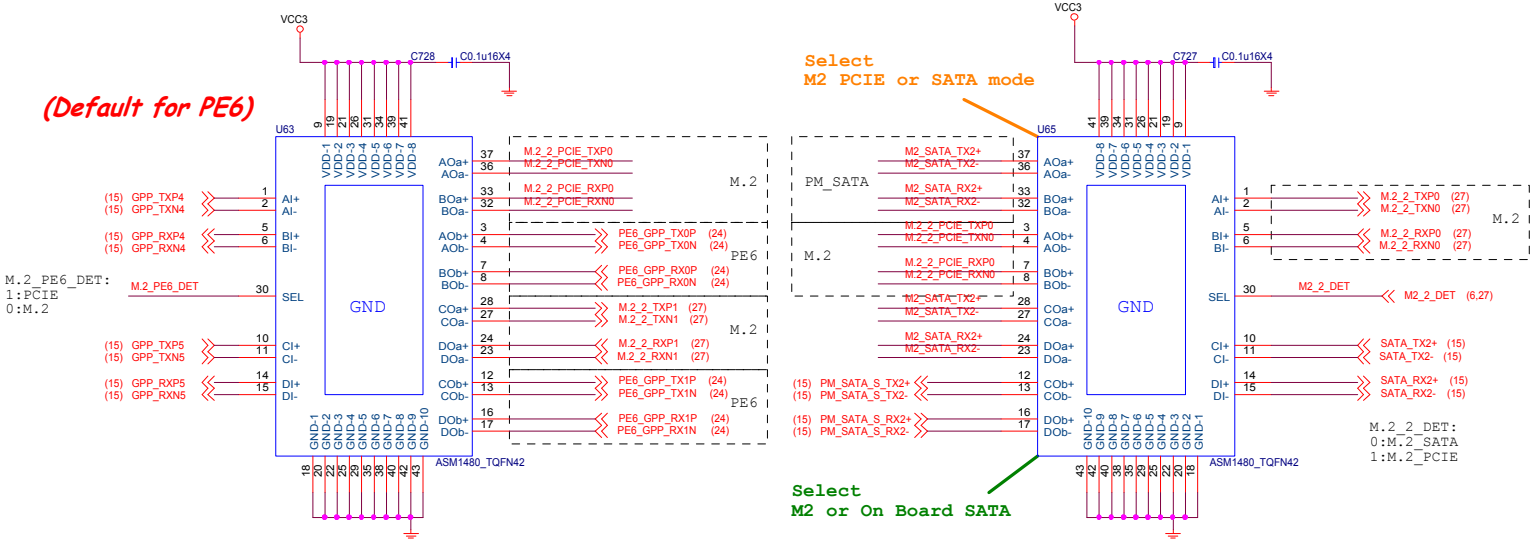
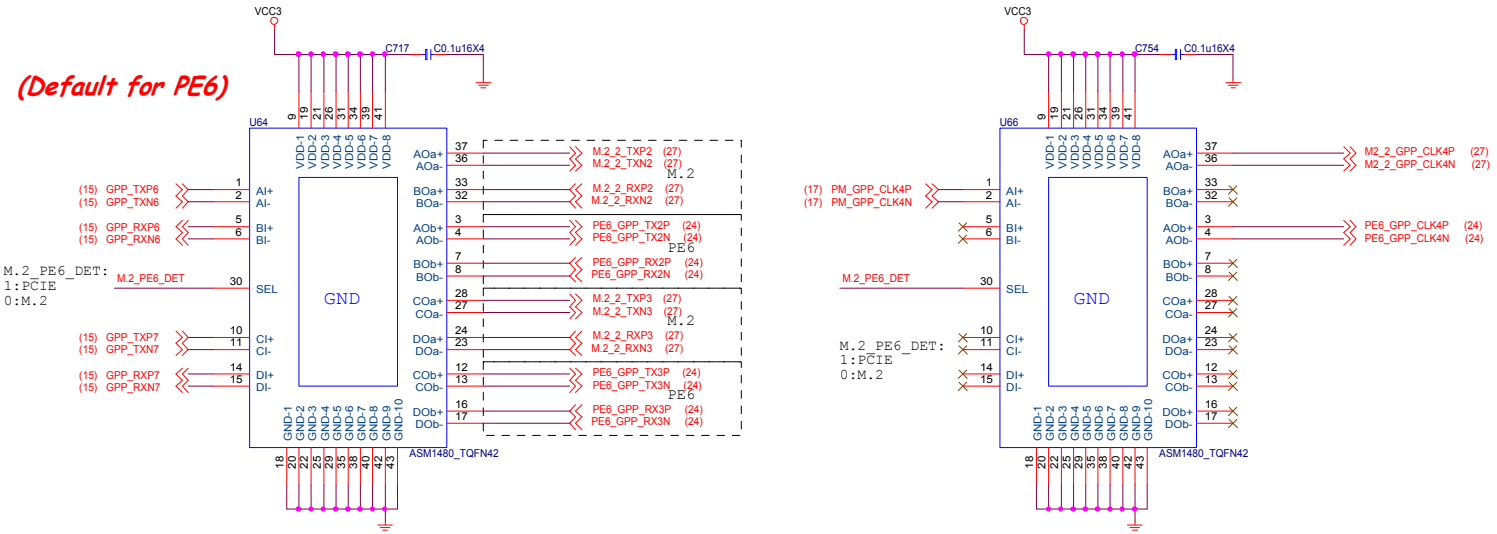
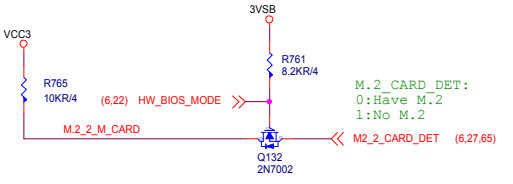
PCI_E6 and M2_2 and SATA1 Switch

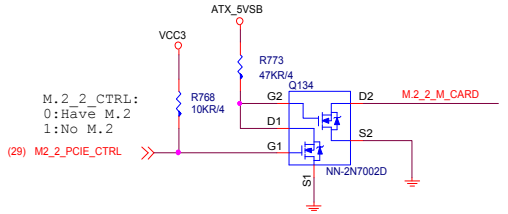


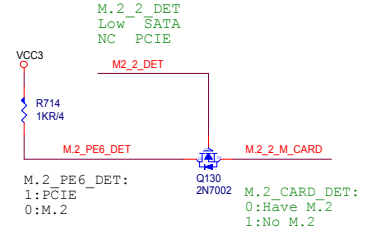


Manufature Control					
	AUTO Mode	PCIE X4	M.2 X4	M.2 SATA	SATA5
HW_BIOS_MODE	1	0	0	1	
M2_2_PCIE_CTRL	0	1	0	0	
Device Detect					
M2_2_CARD_DET		1 0	0	0	1 0
M2_2_DET		1 0	1	0	1

紅色數字為判抓到PCIE或SATA device時所要判斷的訊號







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Size: Custom	Document Description: PCIE Switch PE6 / M2_2	Rev: 10
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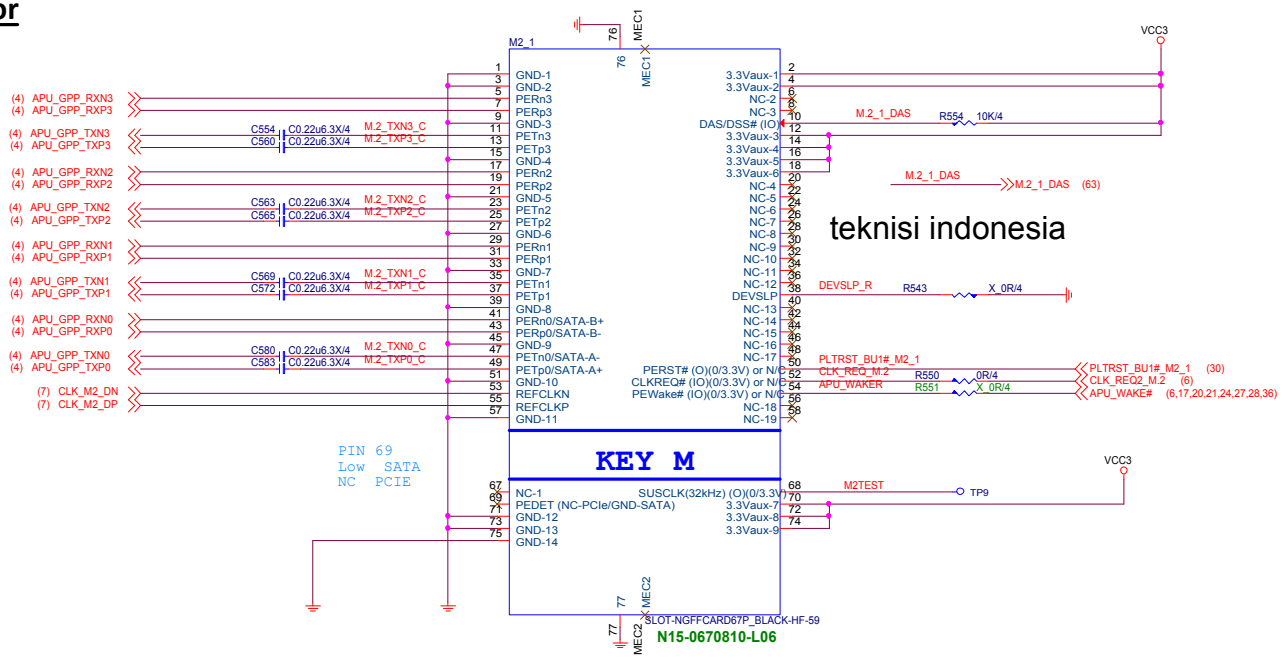
M.2_1 Connector

3.3V@2.5A



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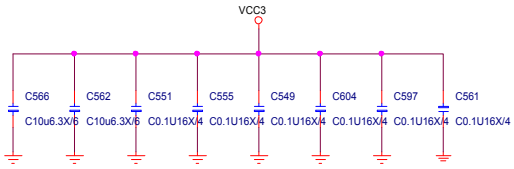
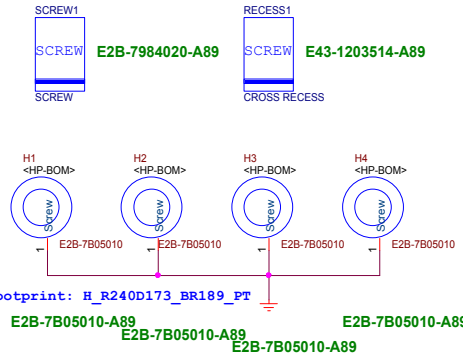
N15-0670810-L06

3.3V@2.5A





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MS-7B78		
Size: Custom	Document Description: M2_1	Rev: 10
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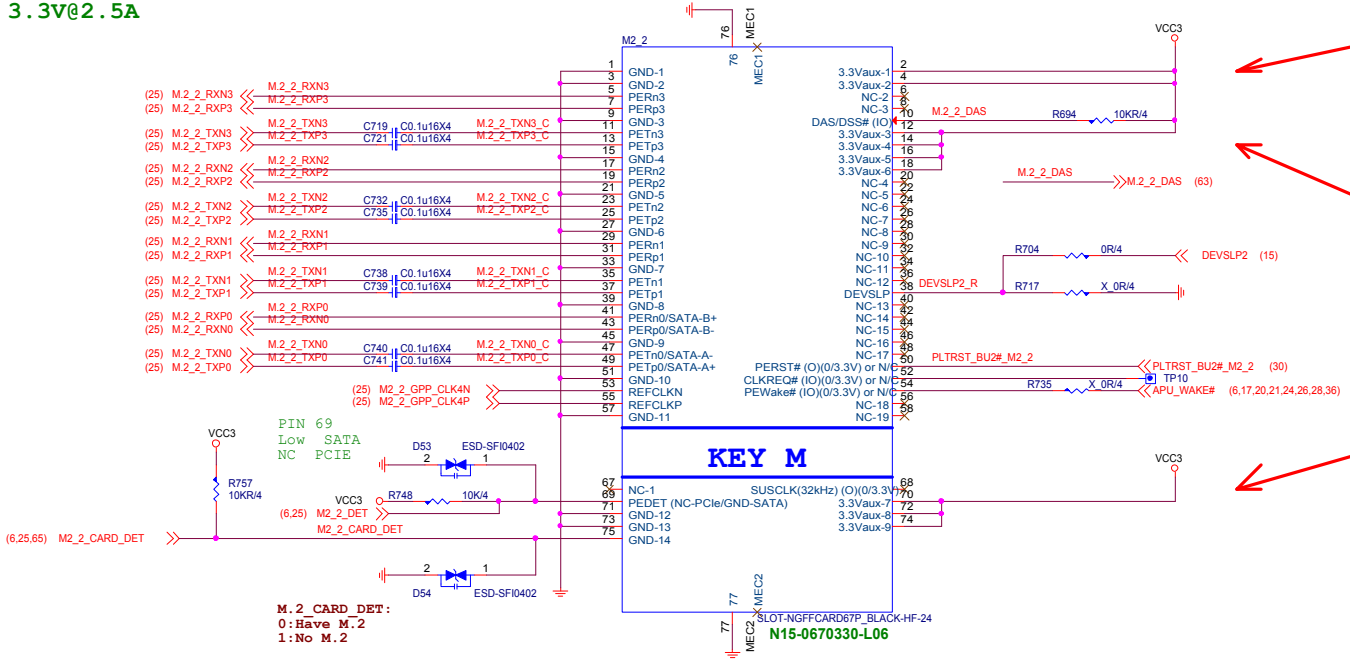
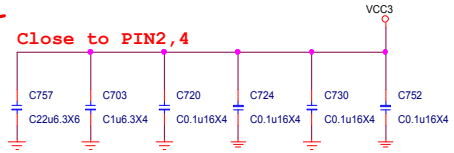
M.2_2 Connector

3.3V@2.5A

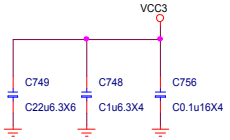


VCC3 2.5A

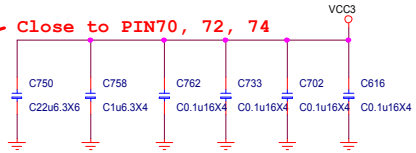
Close to PIN2,4

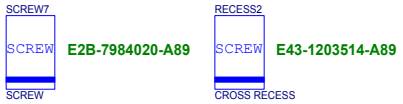


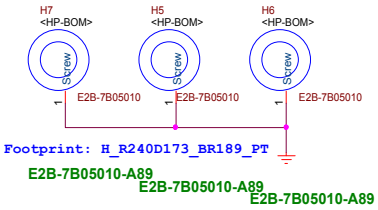
Close to PIN12, 14, 16, 18



Close to PIN70, 72, 74







MICRO-STAR INT'L CO.,LTD		
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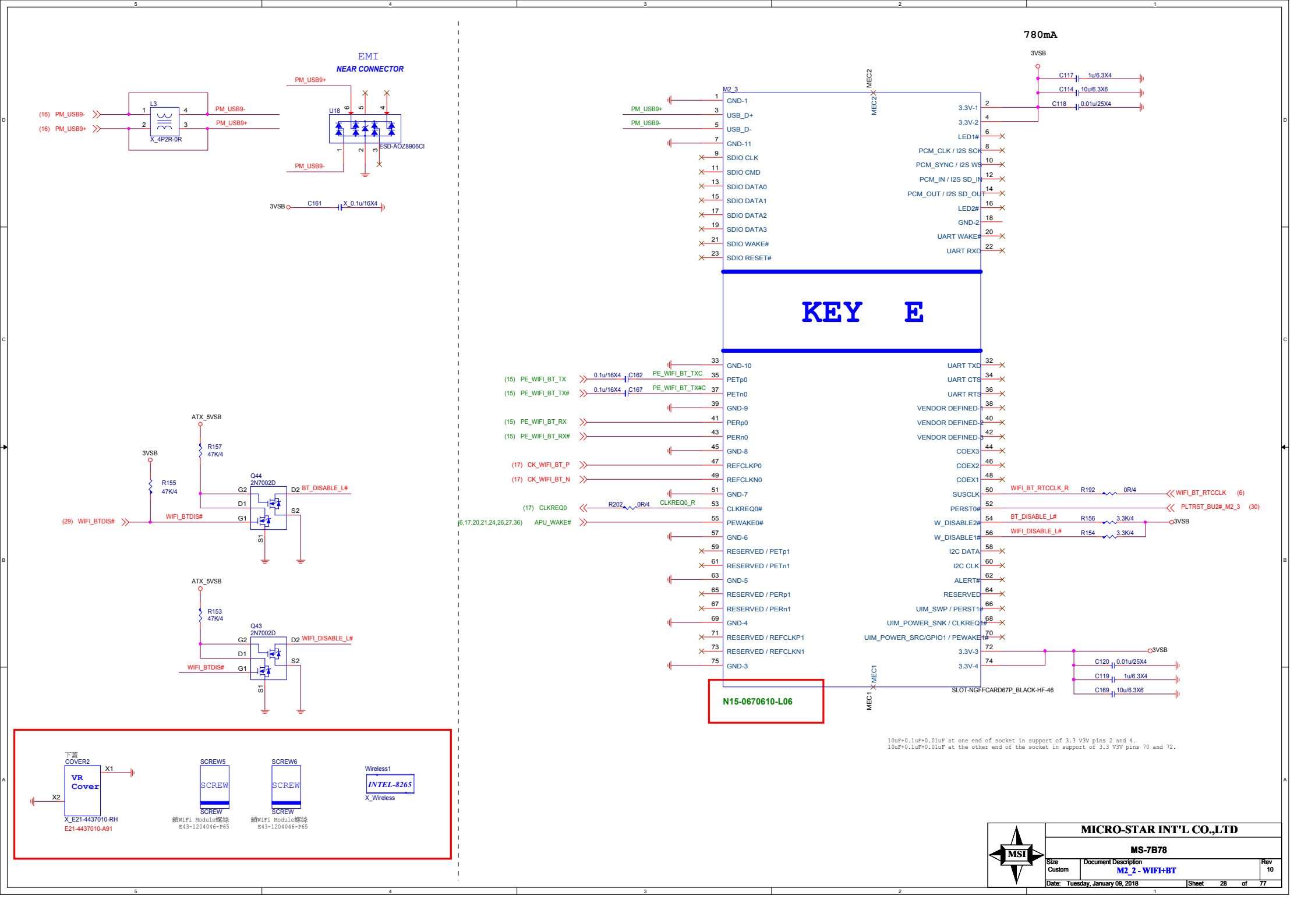
EMI
NEAR CONNECTOR
780mA
KEY E
N15-0670610-L06
MICRO-STAR INT'L CO.,LTD
MS-7B78
M2_2 - WIFI+BT
Date: Tuesday, January 09, 2018
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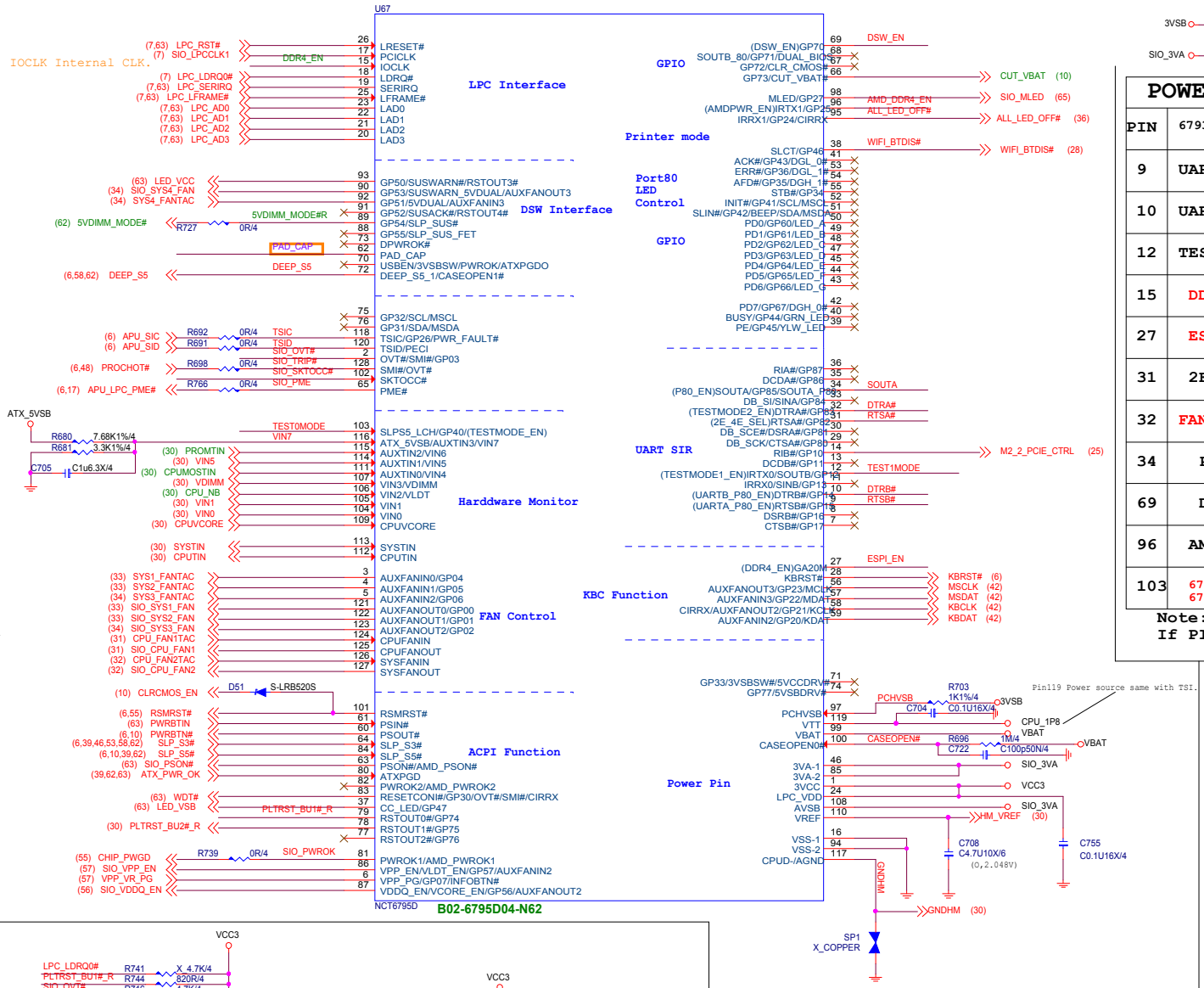
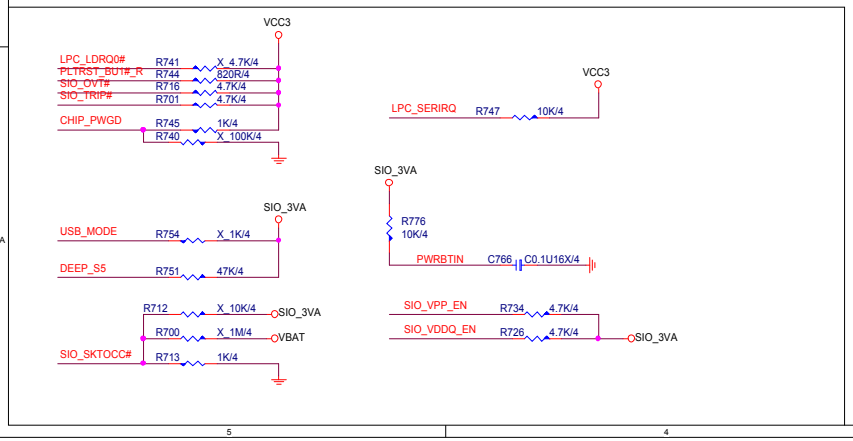
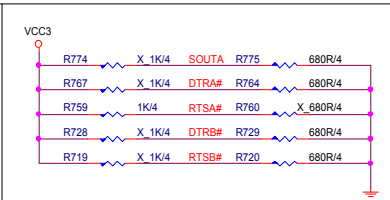


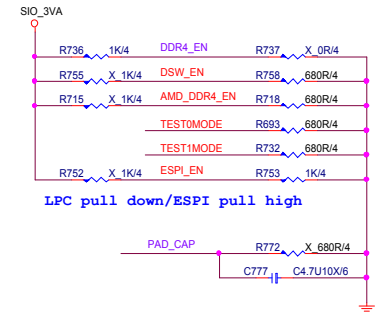


POWER ON STRAPPING PIN FOR NCT6797/6795

PIN	6793/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE1_EN	TESTMODE1_EN	DISABLE TESTMODE1_EN	ENABLE TESTMODE1_EN	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	ESPI_EN	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMD_DDR4_EN	AMD_DDR4_EN	DISABLE AMD DDR4 PWR	ENABLE AMD DDR4 PWR	INTERNAL RSMRST
103	6795 TESTMODE_EN 6797 GP40	6795 WDT# 6797 WDT#	6795 DISABLE TESTMODE	6795 ENABLE TESTMODE	INTERNAL RSMRST

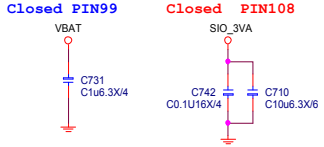
Note:
If PIN34 strapping low,BIOS must programming LPT or GPIO

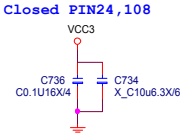


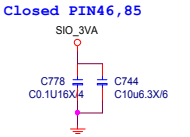


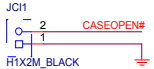
teknisi indonesia

3V Analog Power









N31-1020151-H06

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Custom	SIO - NCT6797D-M	10

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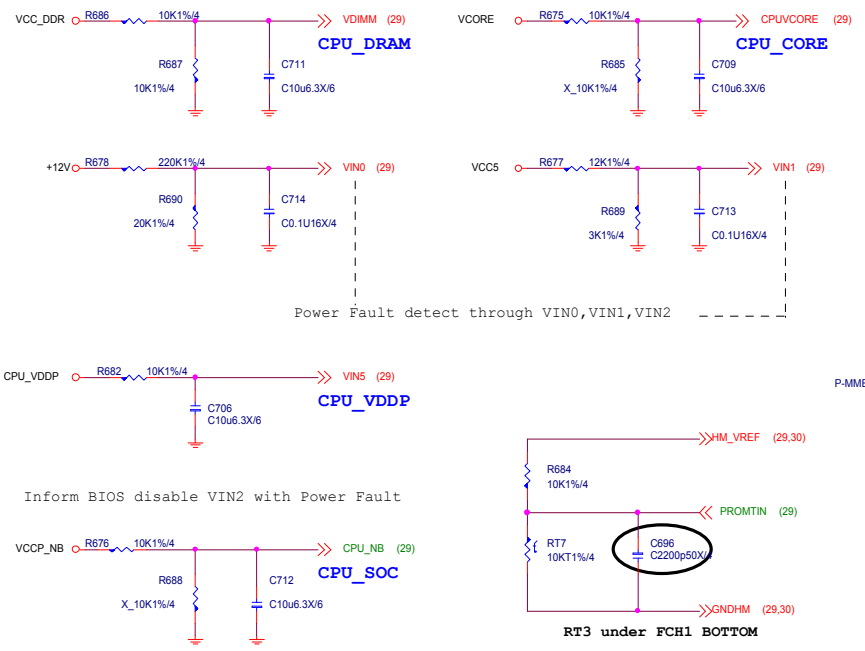
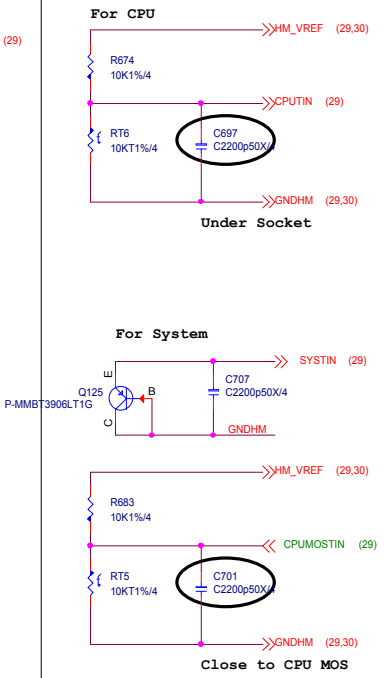
HW Monitor - Voltage

SIO HM Voltage over 2.048V will not detect

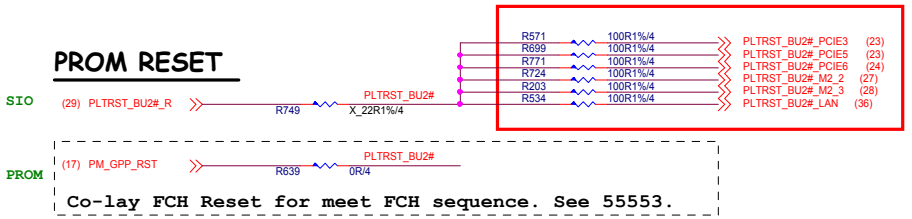


TEMP SENSOR

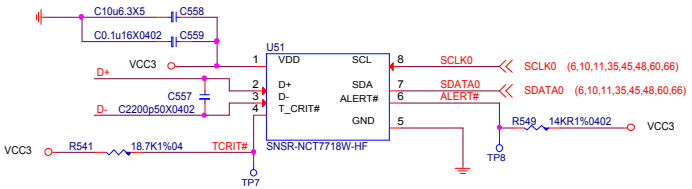


COM PORT

PROM RESET

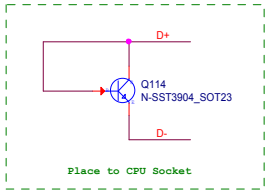


NCT7718W



NCT7718W SM Bus address is 98h (1001100xb)

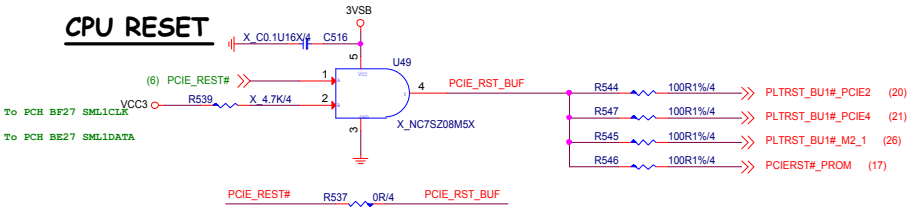
Default: ALERT# Output Comparator Mode



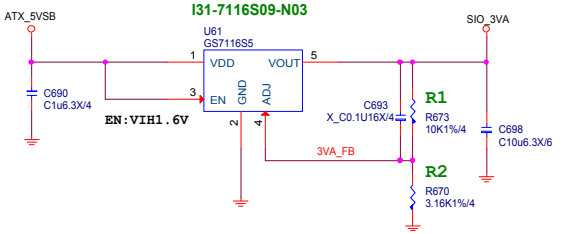
Layout notice:
1. Put the C1 2200pF to close the NCT7718W.
2. Add Ground Shielding For D+ and D- Traces.
3. D+/D- Route Has to be Away From the High Noise Area.
4. The Recommended Traces Width and Ground Shielding Spacing are 10mils.

TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

CPU RESET



SIO_3VA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/3.16K))
= 3.33V

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Custom	SIO - HW Monitor / NCT7718W	10

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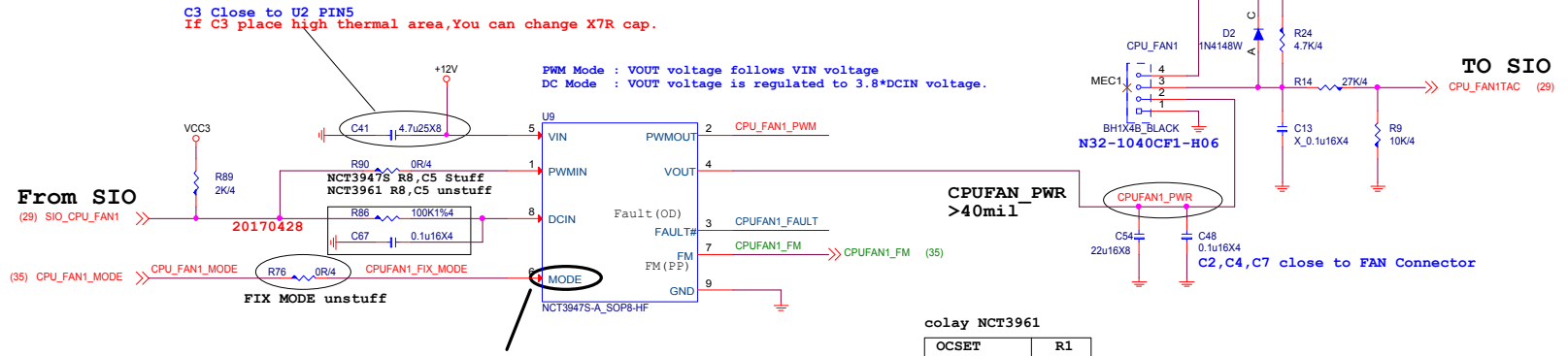
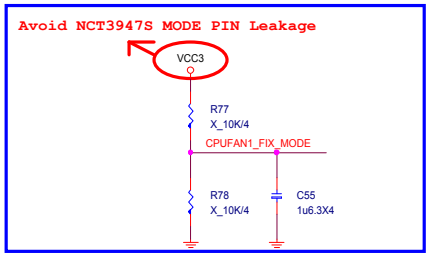
TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

1. PWM/DC/OCP LED
2. Mode GPIO BIOS can swtich PWM/DC MODE
3. OCP connect GPIO for BIOS Use
4. FM:BIOS can read FAN PWM/DC MODE
5. CPUFAN1_LED_OFF_BLINK Use LED On/OFF

CPUFAN1





Resever For FIX DC or PWM MODE USE By PM SPEC

GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating) Default

NCT3947S Internall pull up 1.65V

colay NCT3961

OCSET	R1	
1.2~1.8A	100K	default
2.2~2.8A	49.9K	OC SET By PM SPEC
3.2~3.8A	10K	20170428

VCC3 R84 100K/4 CPUFAN1_FAULT

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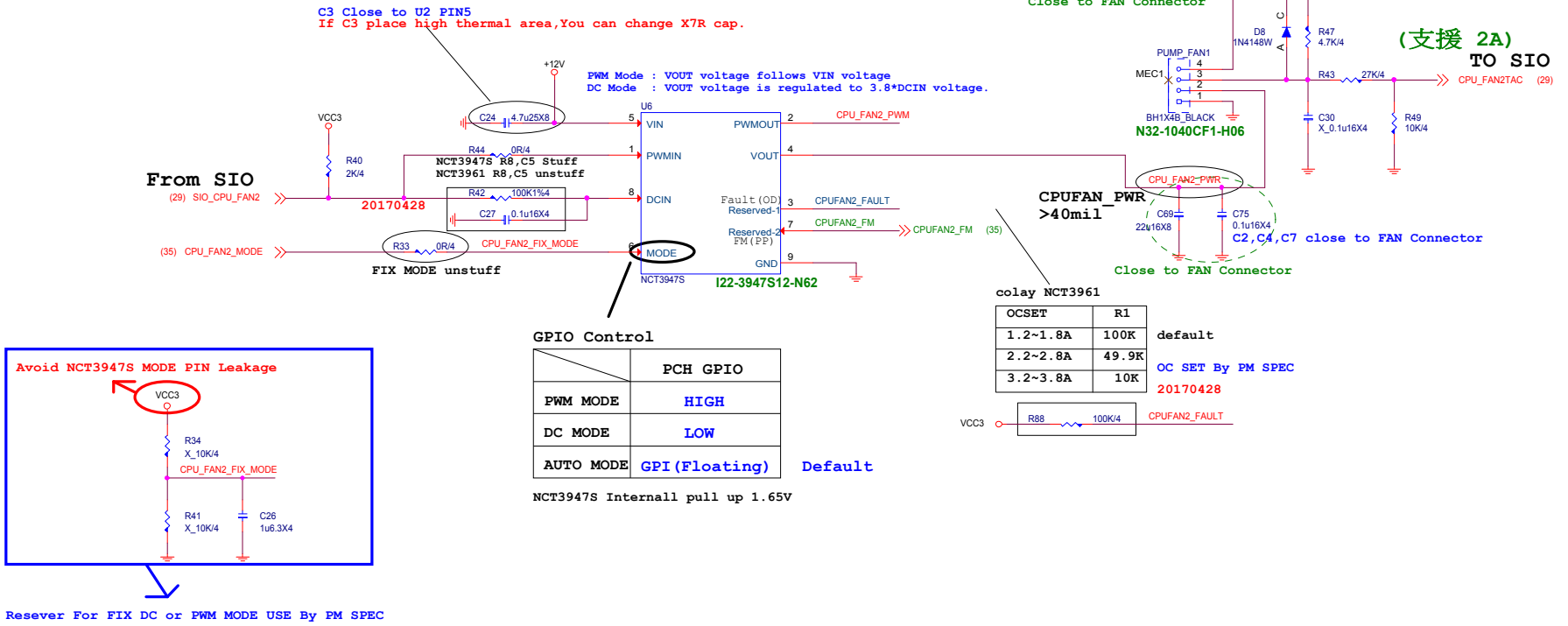
Size: Custom	Document Description: FAN TYPE-J CPUDAN1
Rev: 10	
Date: Tuesday, January 09, 2018	Sheet 31 of 77

TYPE J : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO

PUMPFAN1

1. PWM/DC/OCP LED
2. Mode GPIO BIOS can swtich PWM/DC MODE
3. OCP connect GPIO for BIOS Use
4. FM:BIOS can read FAN PWM/DC MODE
5. CPUFAN1_LED_OFF_BLINK Use LED On/OFF



GPIO Control

	PCH GPIO
PWM MODE	HIGH
DC MODE	LOW
AUTO MODE	GPI(Floating) Default

NCT3947S Internall pull up 1.65V

Resever For FIX DC or PWM MODE USE By PM SPEC

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Size: Custom	Document Description: FAN TYPE-J PUMPFAN1
Rev: 10	
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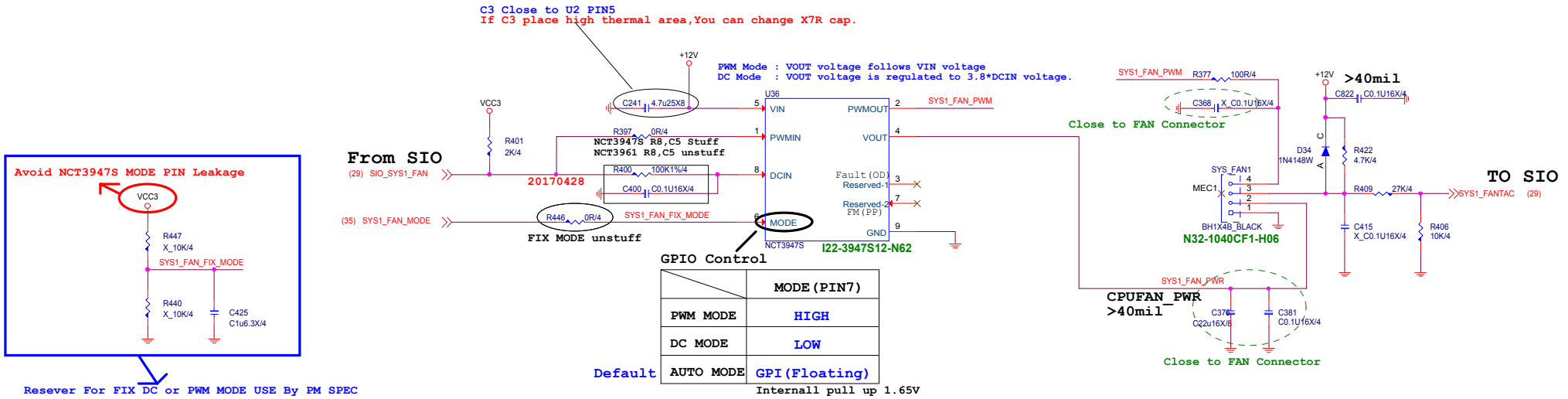
SYSFAN1

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

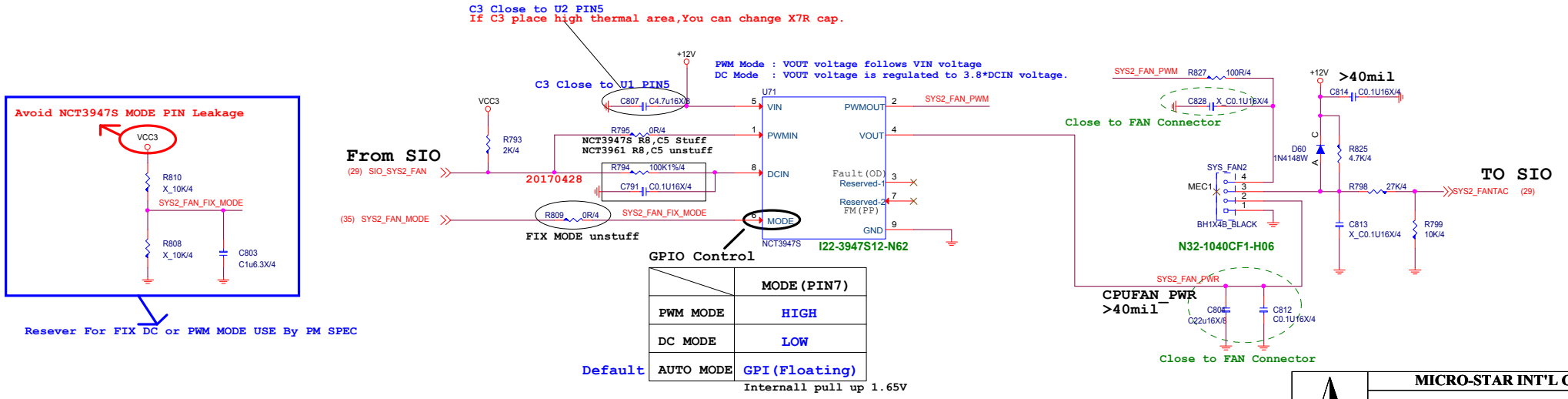
1.Mode GPIO BIOS can swtich PWM/DC MODE



SYSFAN2

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



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Size	Document Description	Rev
Custom	FAN TYPE-K SYSFAN1/2	10

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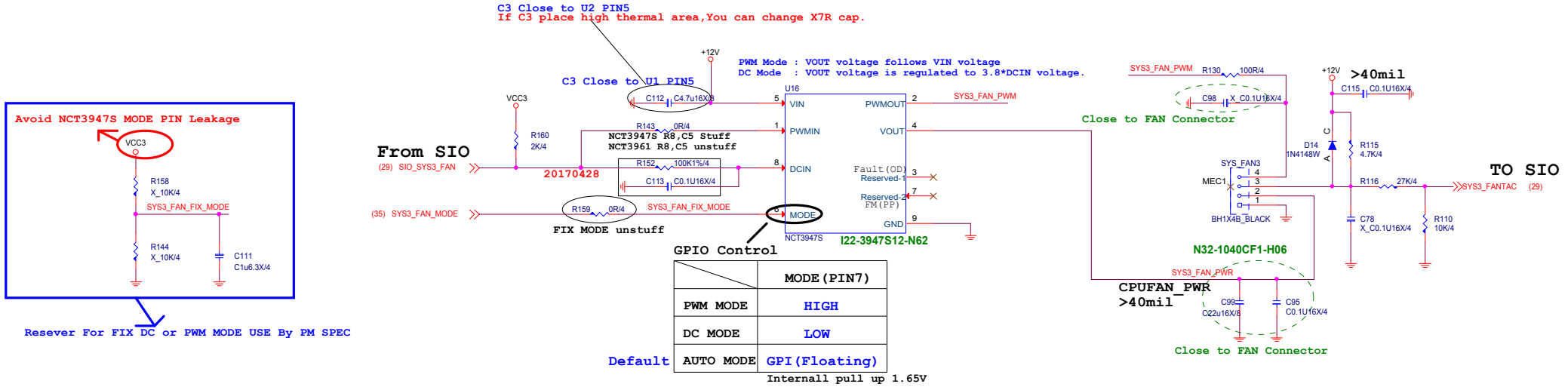
SYSFAN3

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE



SYSFAN4

TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

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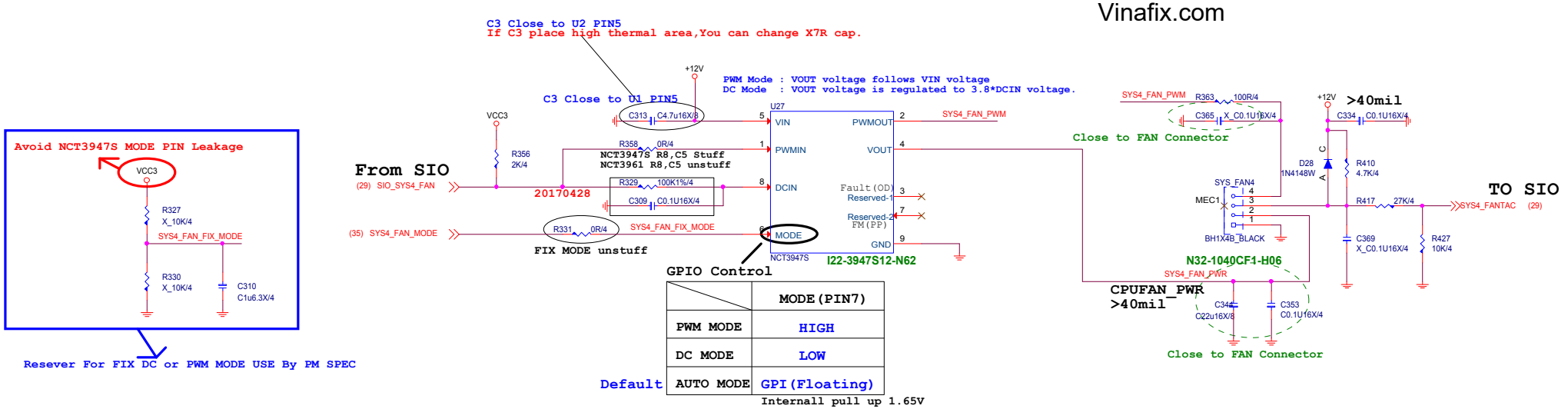

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Size: Custom	Document Description: FAN TYPE-K SYSFAN3/4	Rev: 10
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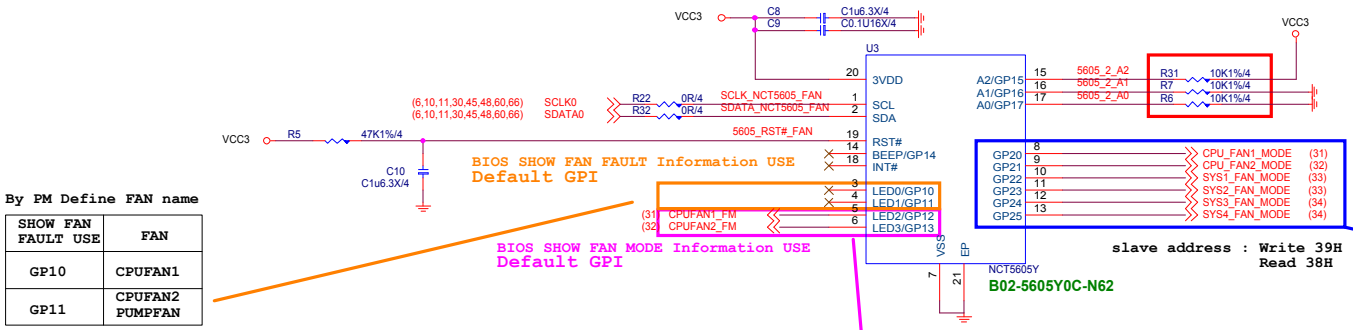
By PM Define FAN name

LED OFF BLINK	FAN
GP16	CPUFAN1
GP17	CPUFAN2 PUMPFAN

USE LED OFF & LED BLINK

Default GPI



By PM Define FAN name

SHOW FAN FAULT USE	FAN
GP10	CPUFAN1
GP11	CPUFAN2 PUMPFAN

By PM Define FAN name

SHOW FAN MODE USE	FAN
GP12	CPUFAN1
GP13	CPUFAN2 PUMPFAN

By PM Define FAN name

FAN MODE USE	FAN
GP20	CPUFAN1
GP21	CPUFAN2 PUMPFAN
GP22	SYSFAN1
GP23	SYSFAN2
GP24	SYSFAN3
GP25	SYSFAN4

1. GENERAL DESCRIPTION

The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPI/O pins. It also can provide SMBus™ address setting pins to set the address during power- on reset or from external reset.

NCT5605Y SMBus™ Address is:

0	0	1	1	A2	A1	A0	R/W

0

1

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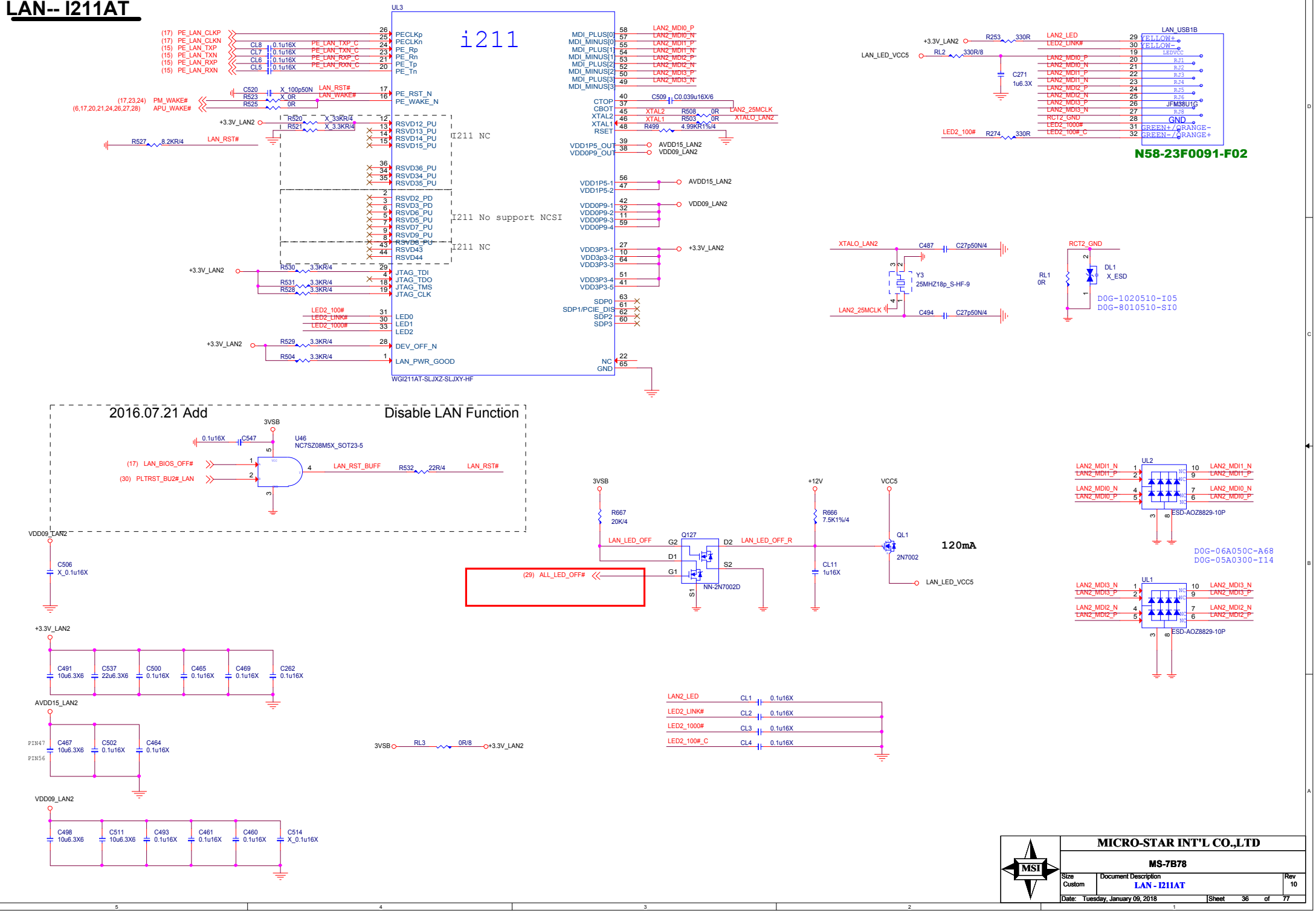
LAN-- I211AT



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Size: Custom	Document Description: LAN - I211AT
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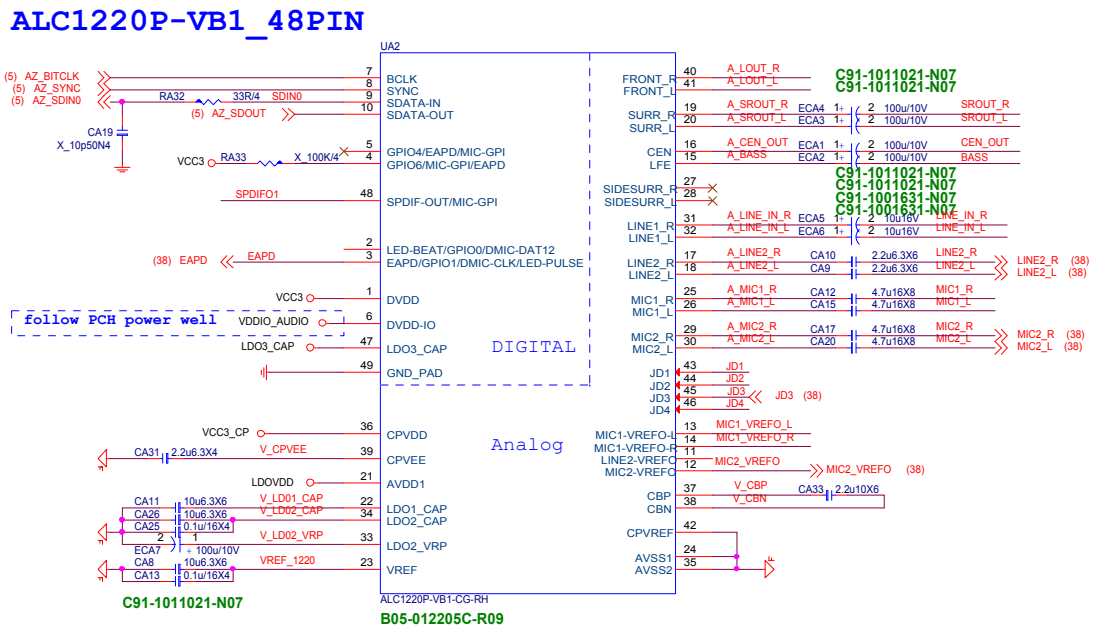
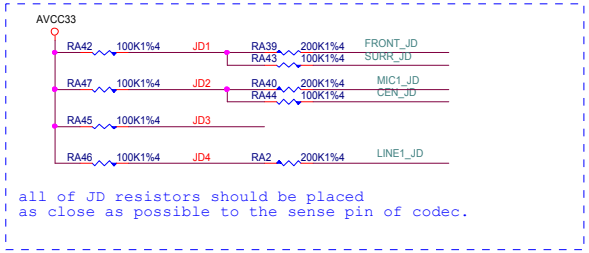
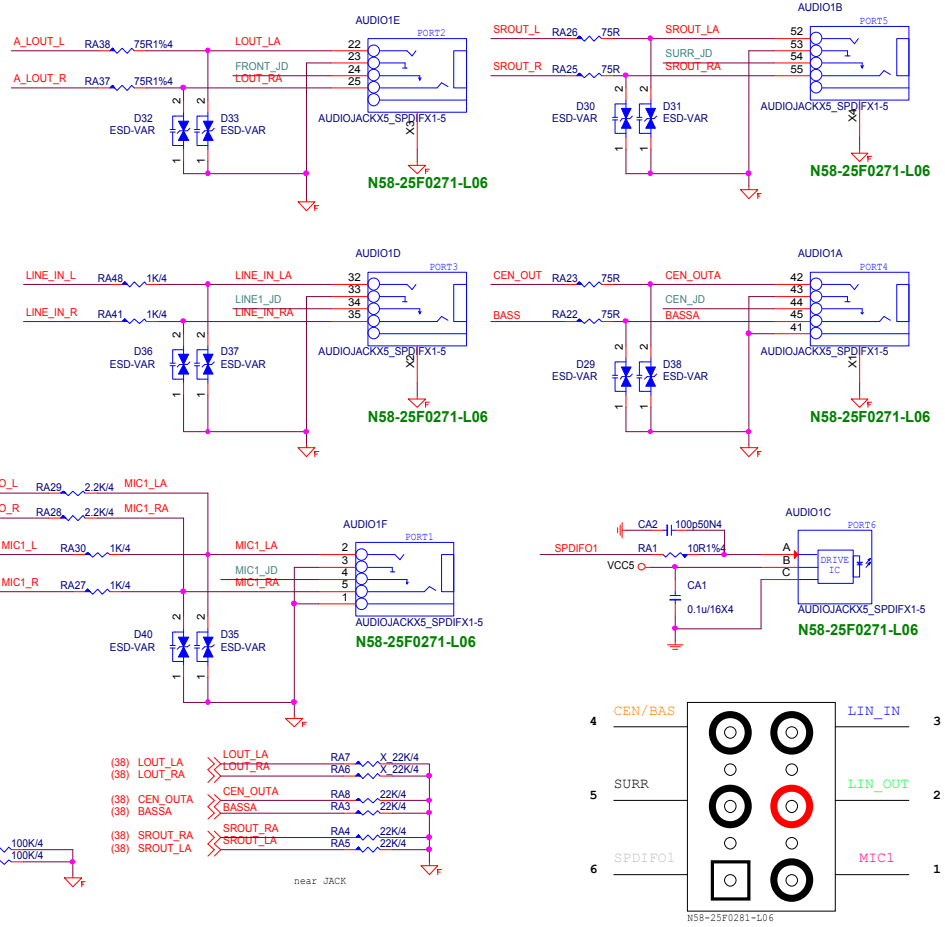
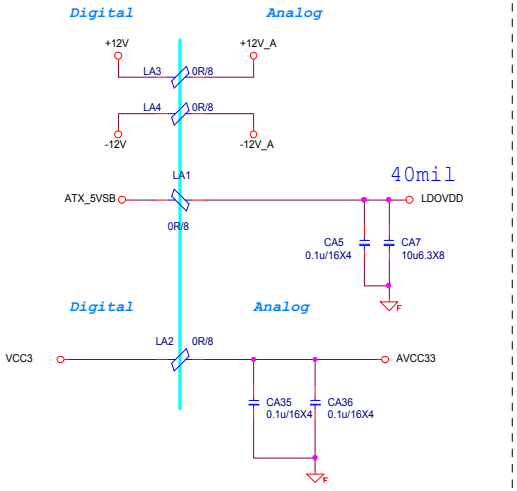
ALC1220P-VB1_48PIN









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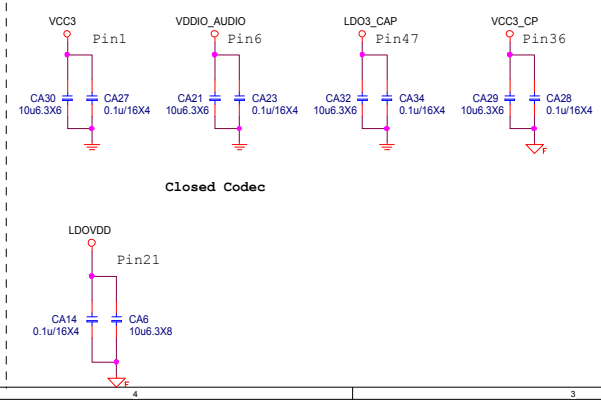
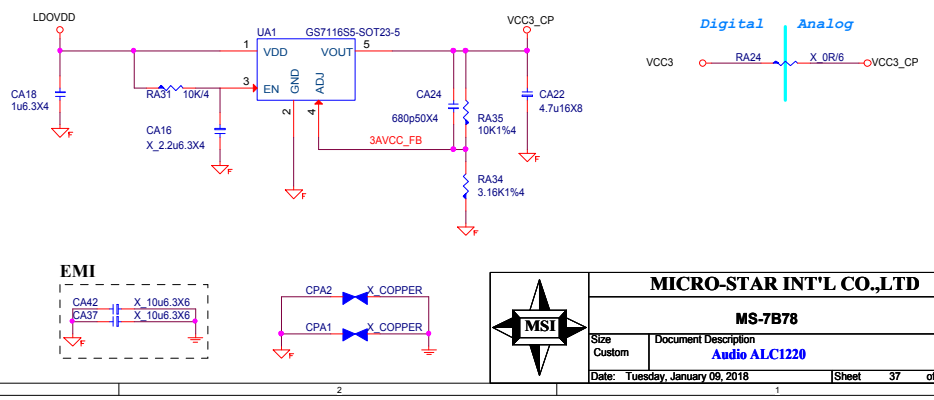


CPVDD POWER:ATX5VSB will Leakage to CVDD by ALC1220, so CVDD must keep 3.3V



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Size: Custom	Document Description: Audio ALC1220	Rev: 10
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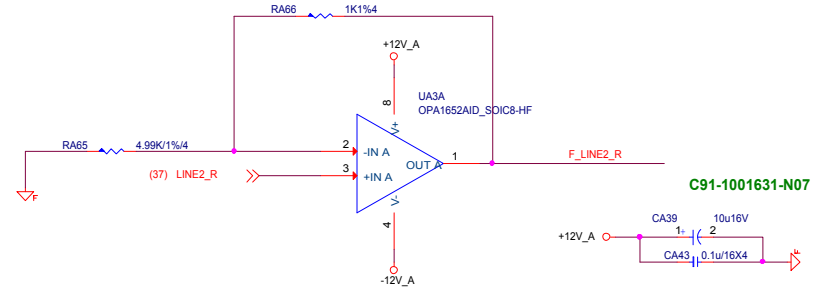
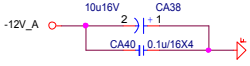
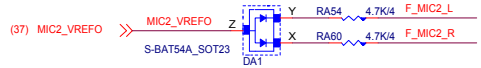


C91-1001631-N07

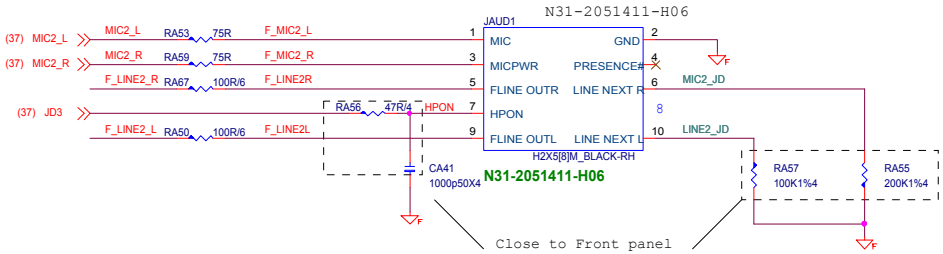
C91-1001631-N07



Close to U3



N31-2051411-H06



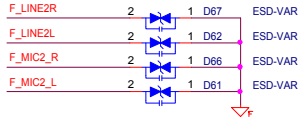
N31-2051411-H06

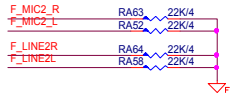
Close to Front panel

For HDA/AC97 front cable.

Close to Jack

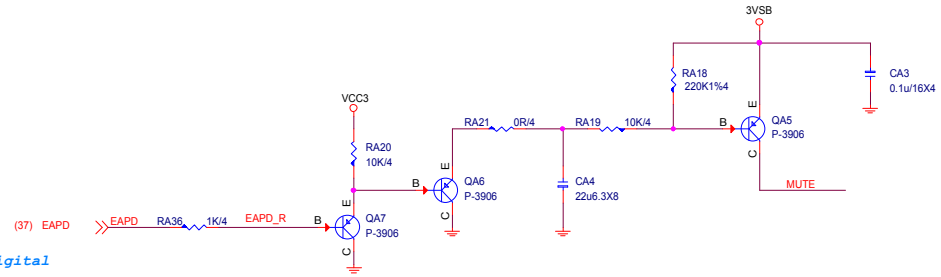
ESD protect





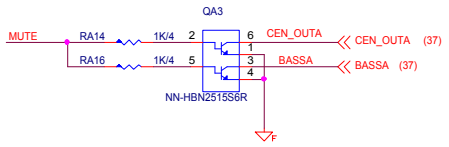
Rear Line OUT De-POP circuit

(De-pop circuit for Rear Line out & Front Headphone out)

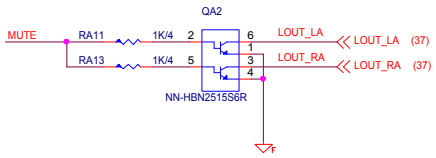


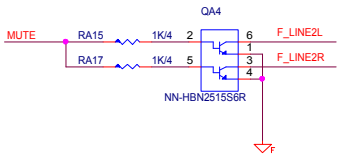
Digital

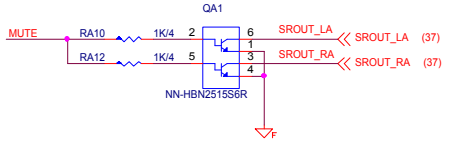
(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change SROUT_LA,SROUT_RA, CEN_OUTA, BASSA to TVS)



Analog







Audio moat is transparent and width 40mil

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MS-7B78		
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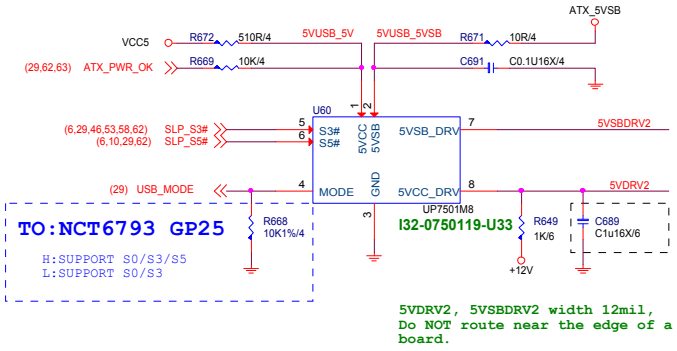
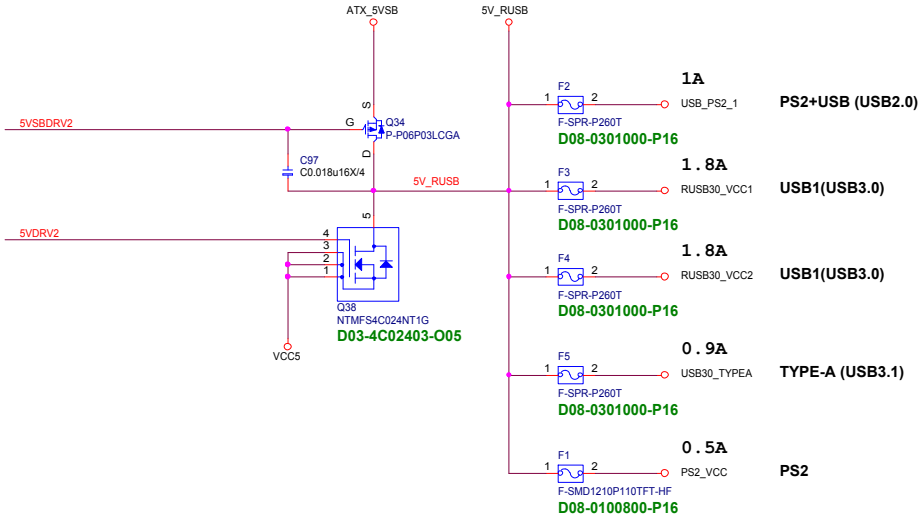
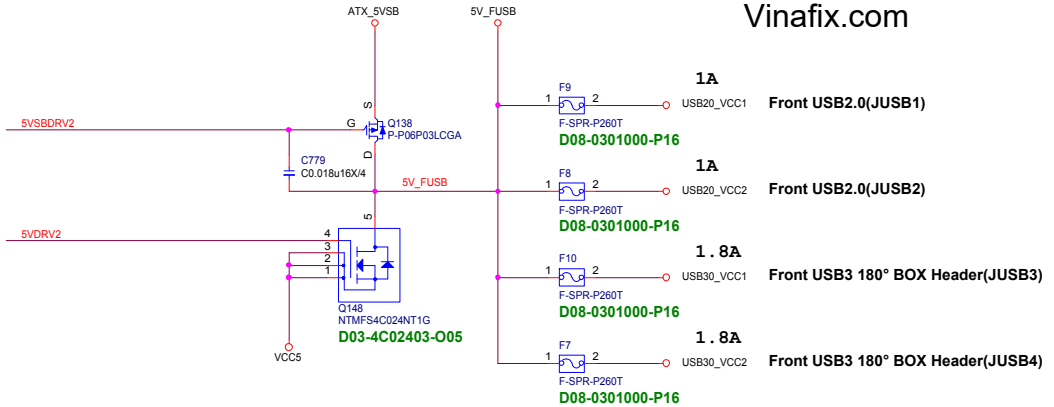
USB Power





Rear (5.1A)

Front (5.6A)



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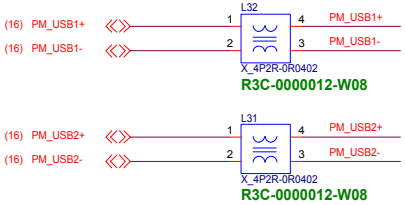
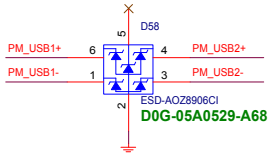
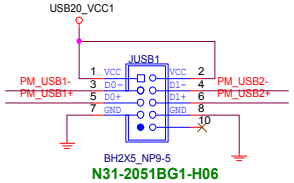
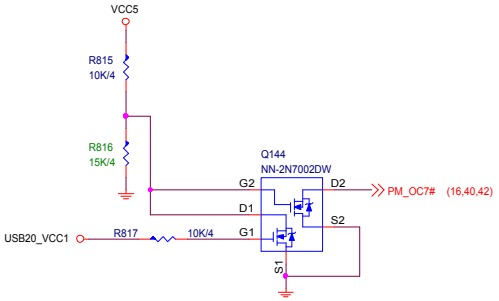
Front USB2.0(JUSB1)

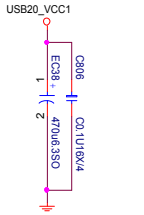
5V@1A





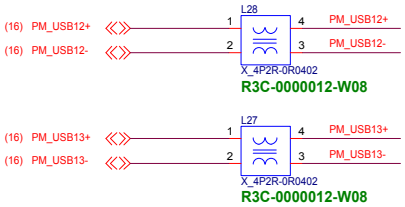


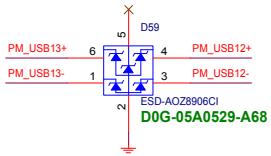


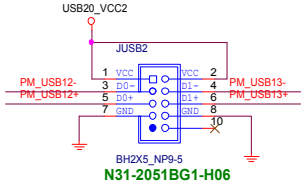


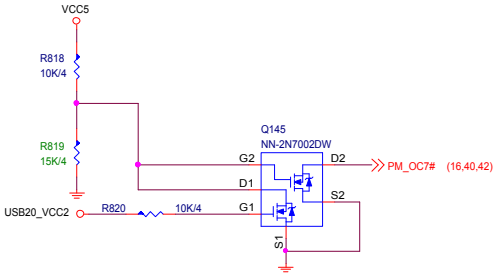
Front USB2.0(JUSB2)

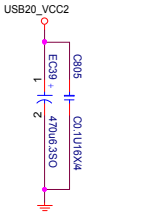
5V@1A











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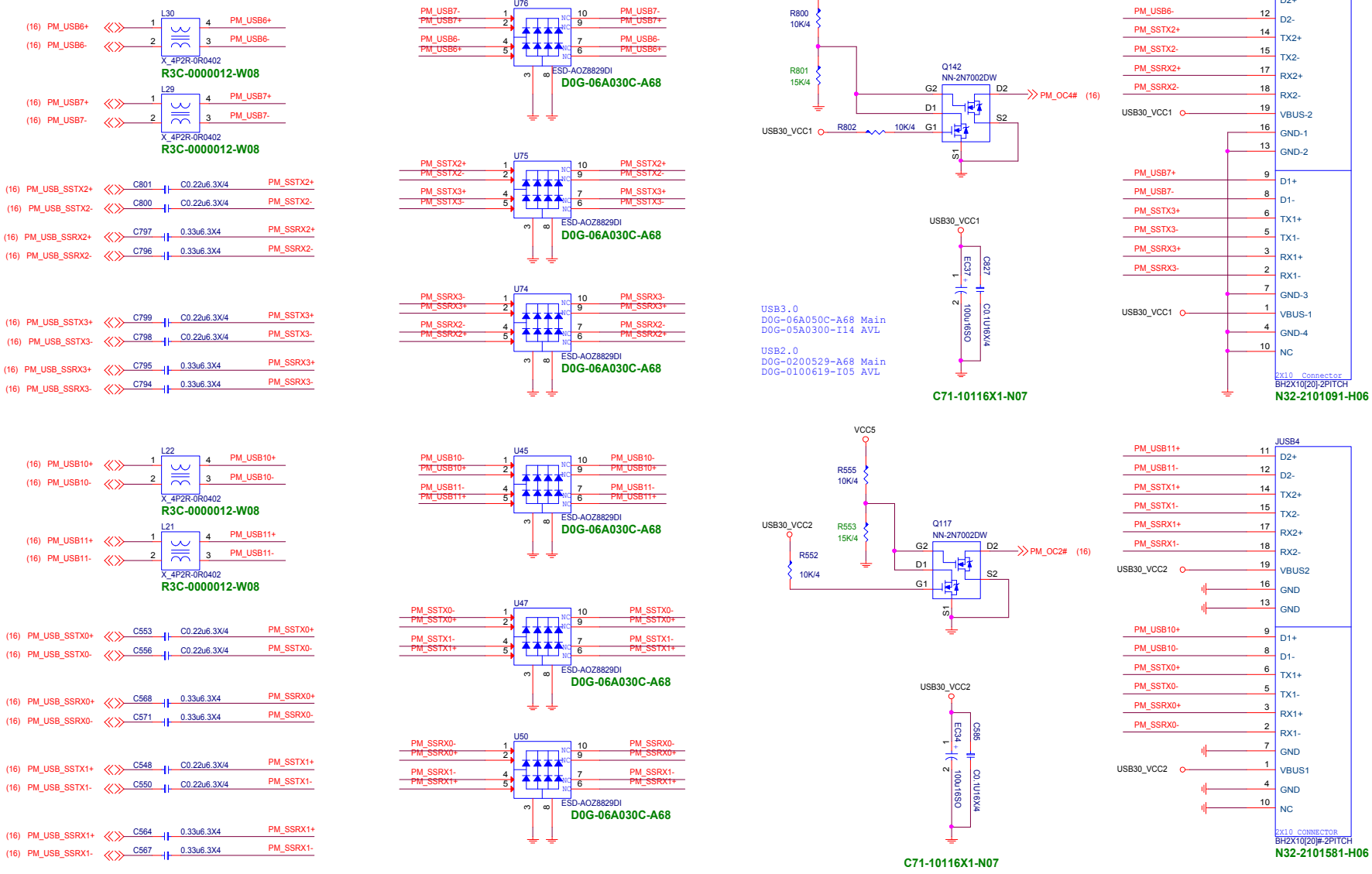
Front USB3 180° BOX Header(JUSB3)

5V@1.8A



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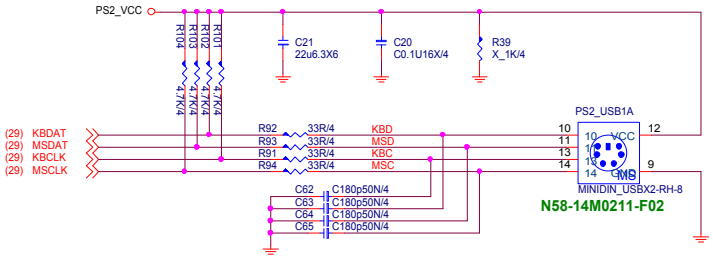
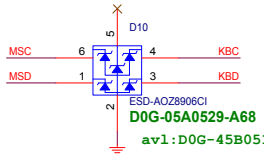
PS2+USB (USB2.0)

5V@1A



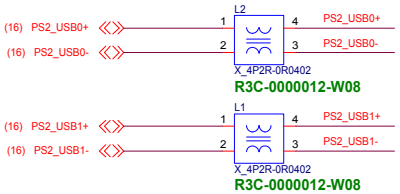
N58-14M0211-F02



D0G-05A0529-A68

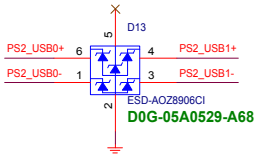
avl:D0G-45B0510-I14

layout note:
C21 must close to TVS pin5
TVS must near KB_MS1 connector and route without branch
Varistor must close to TVS and route without branch

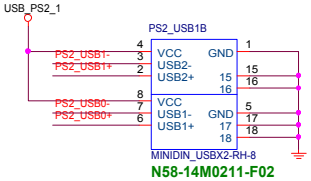


R3C-0000012-W08

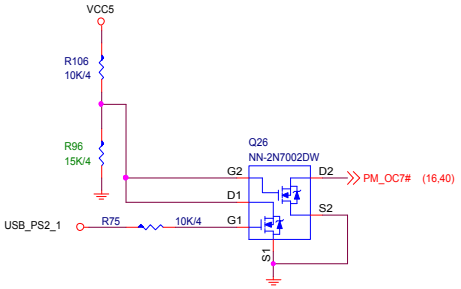
R3C-0000012-W08

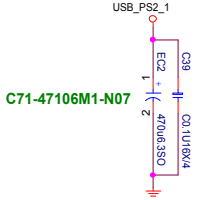


D0G-05A0529-A68



N58-14M0211-F02





C71-47106M1-N07

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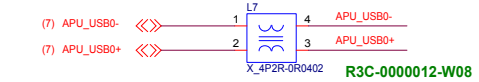
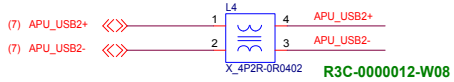
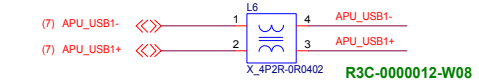
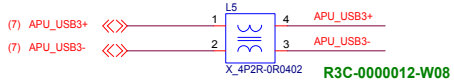
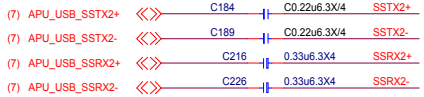
Rear USB3.0 GEN1 5V@1.8A

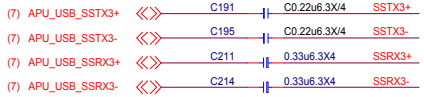


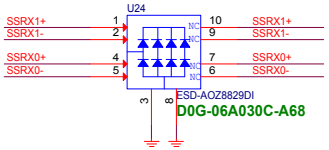


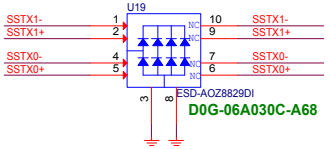


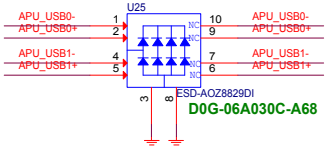


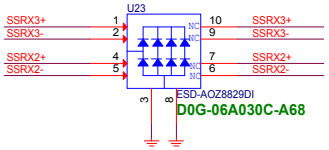


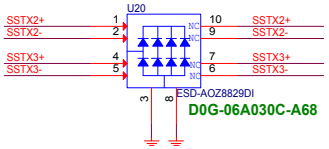


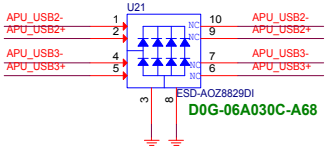


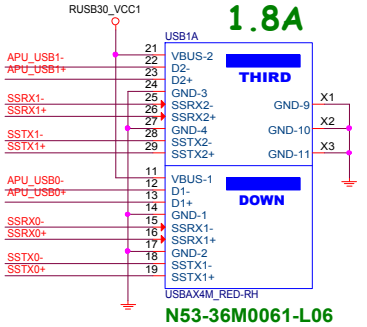


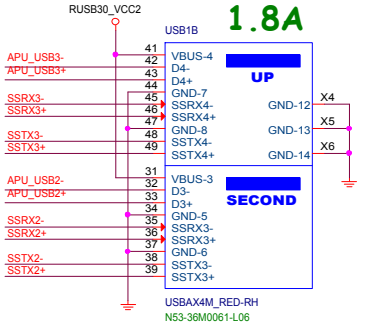


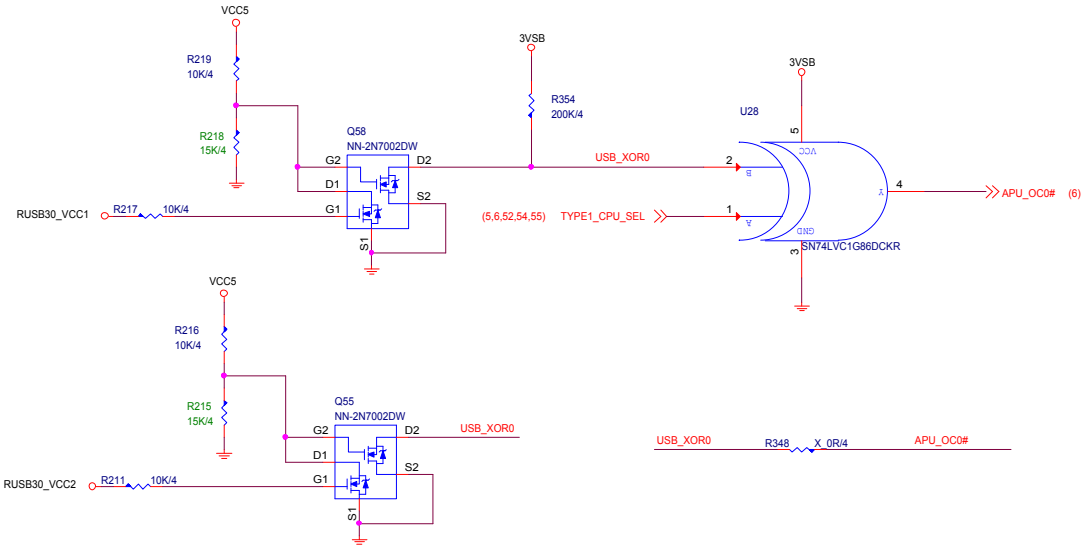












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	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

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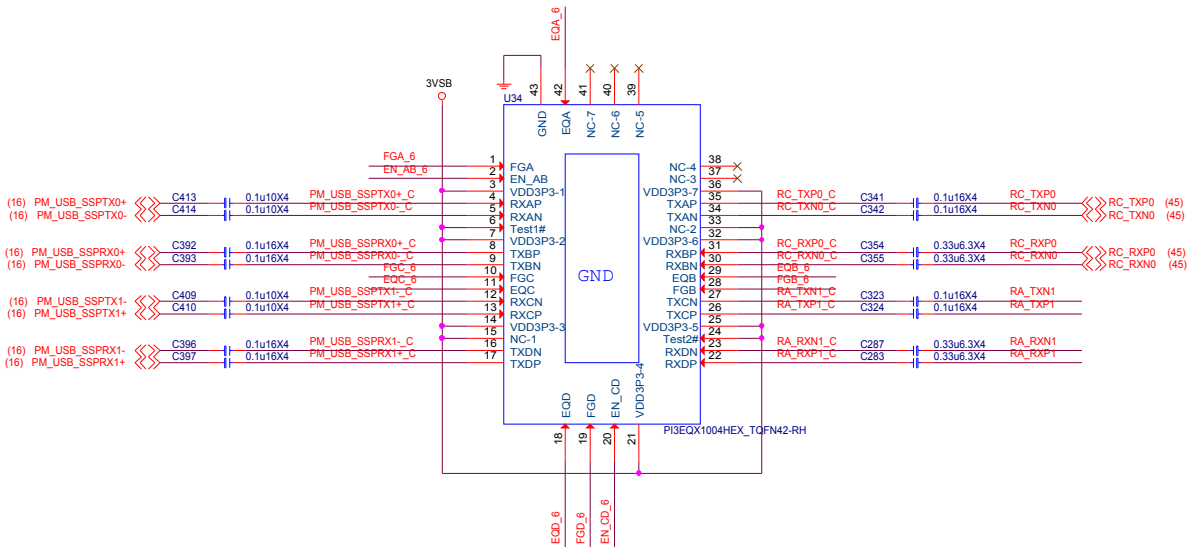
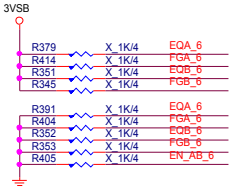
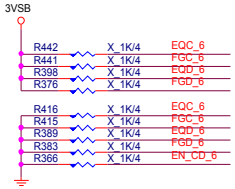
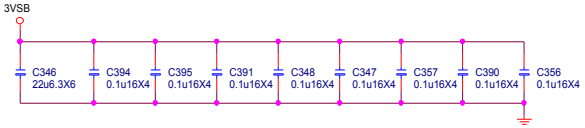
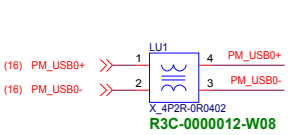
TYPE-A PI3EQX1004 Redriver

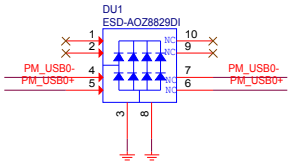


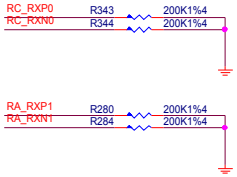


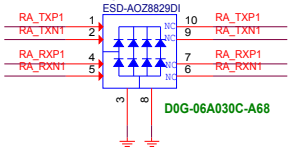


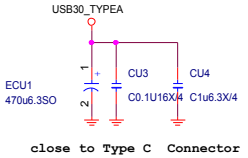


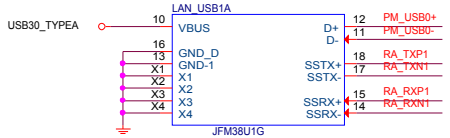


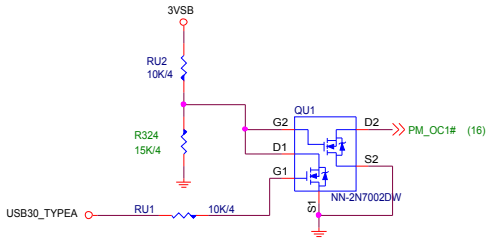












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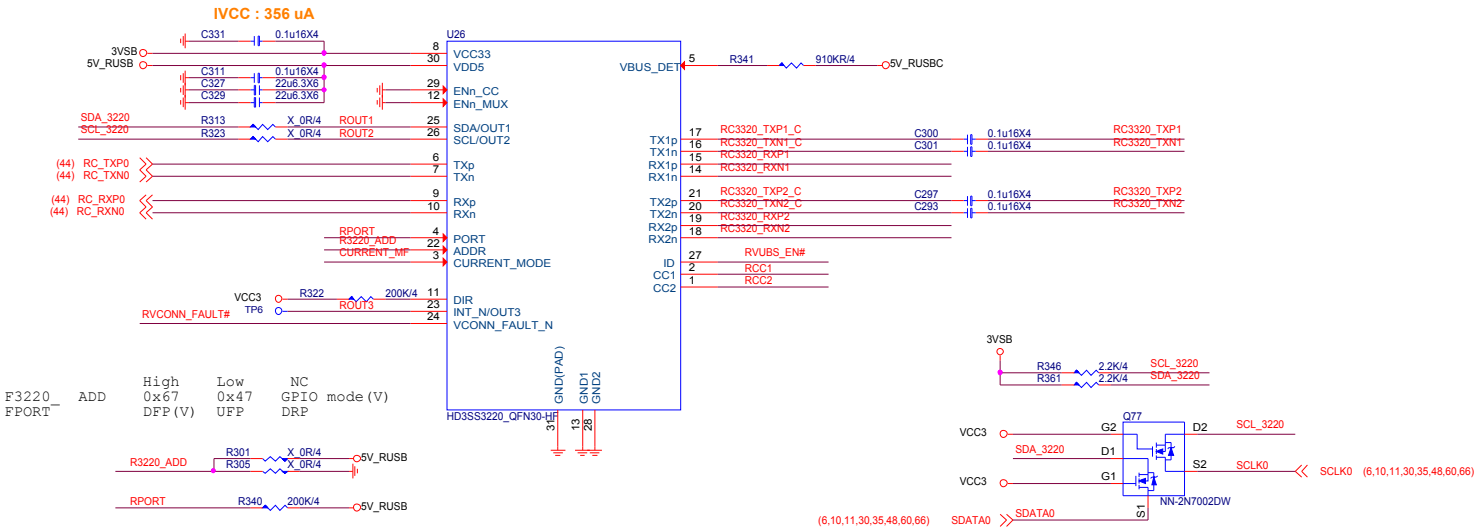
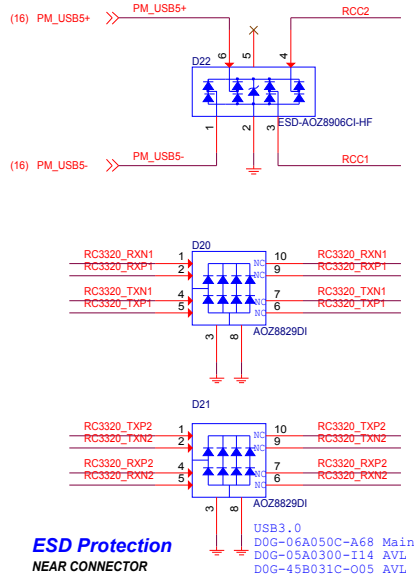
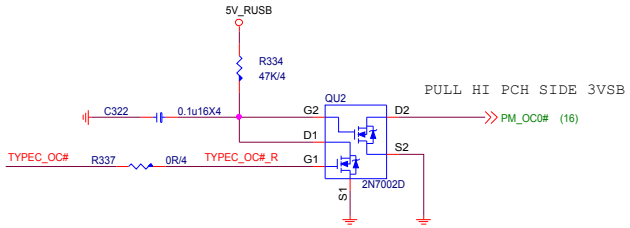
USB 3.1-Type-C

USB Type-C MUX with Configuration Channel (CC)

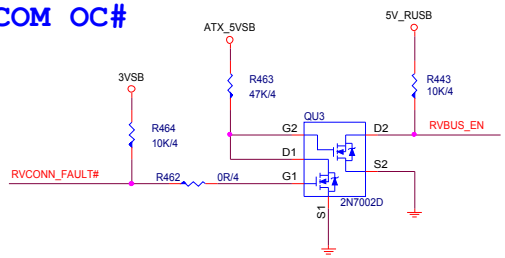




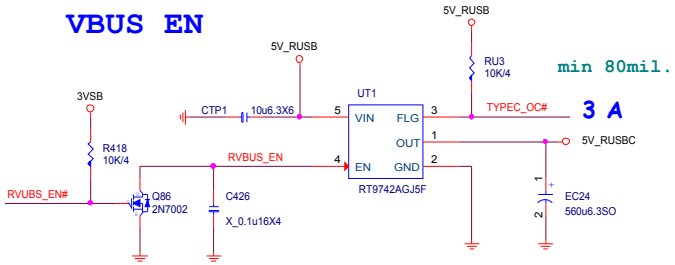
VBUS OC# LEVEL SHIFT

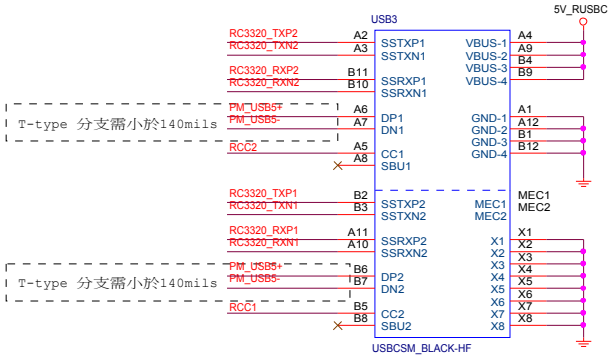


VCOM OC#

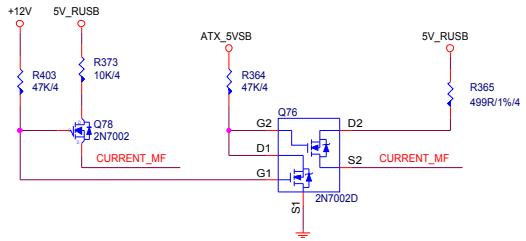


VBUS EN





Current Mode



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Size: Custom	Document Description: Rear USB3.1 Type C / mux
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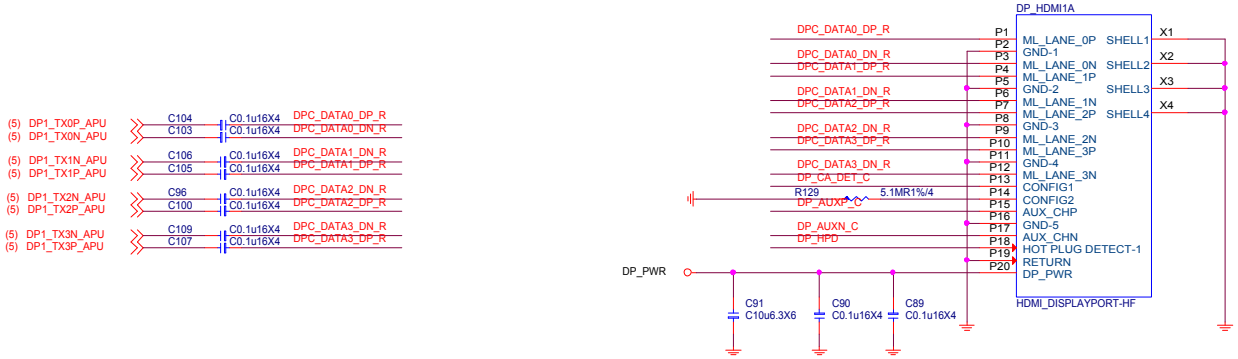
DP CONNECTOR



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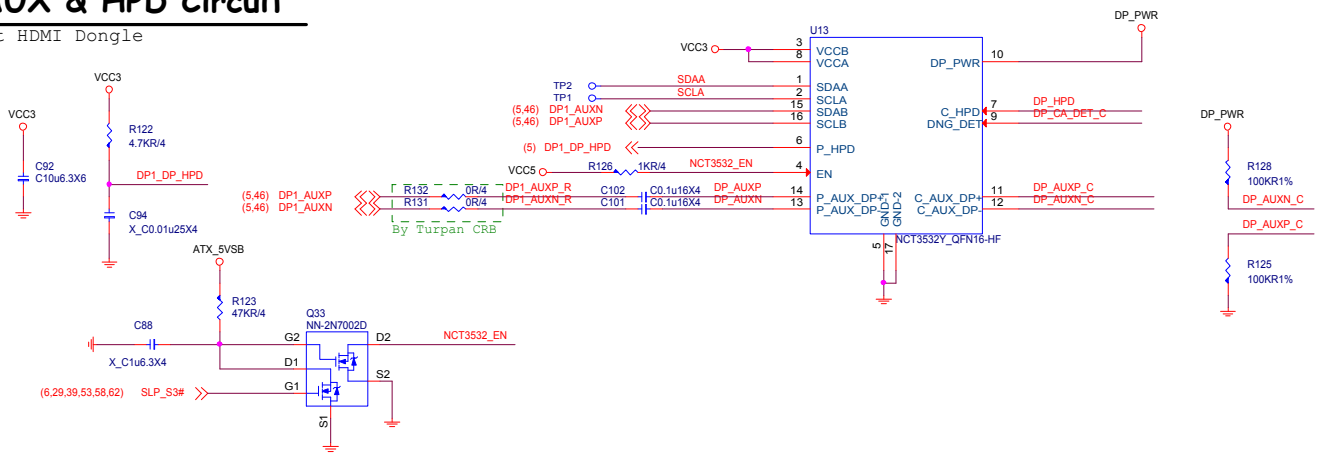
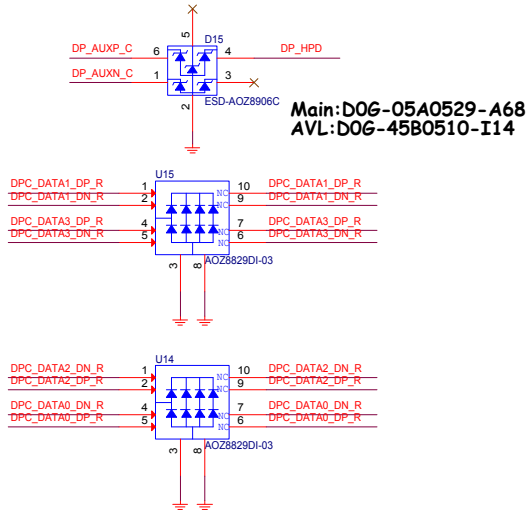
DP AUX & HPD Circuit

Support HDMI Dongle



ESD



MSI	MICRO-STAR INT'L CO.,LTD	
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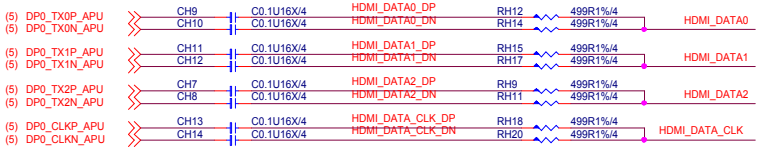
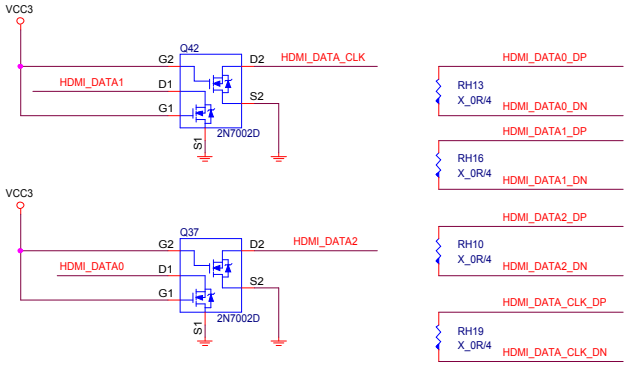
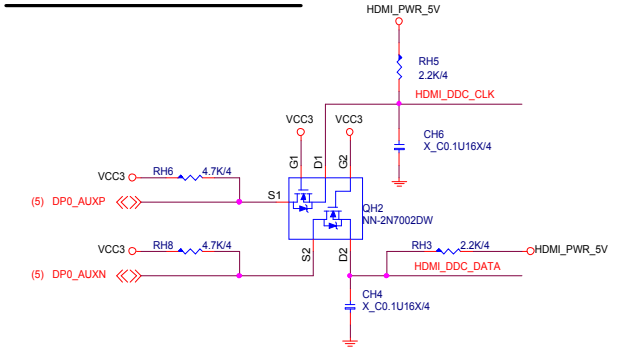
HDMI CONNECTOR

For HDMI 1.4

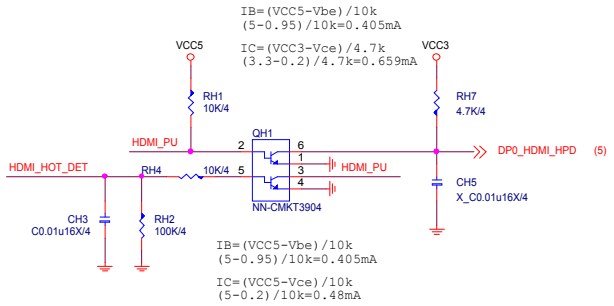




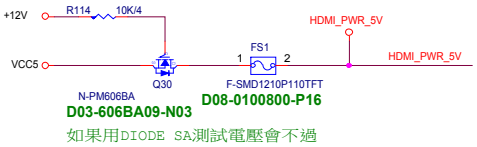
AUX Level Shifter



HPD Circuit

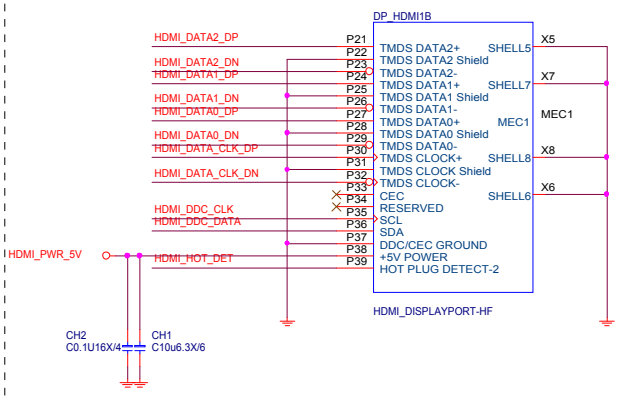


Connector Power

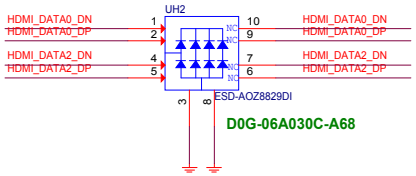


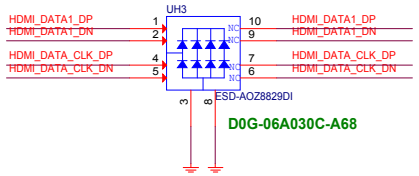
如果用DIODE SA測試電壓會不過

Connector

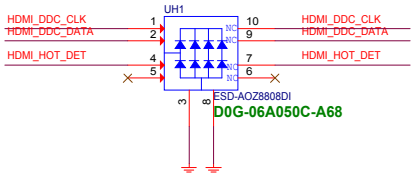


For EMI





注意:耐壓5v零件



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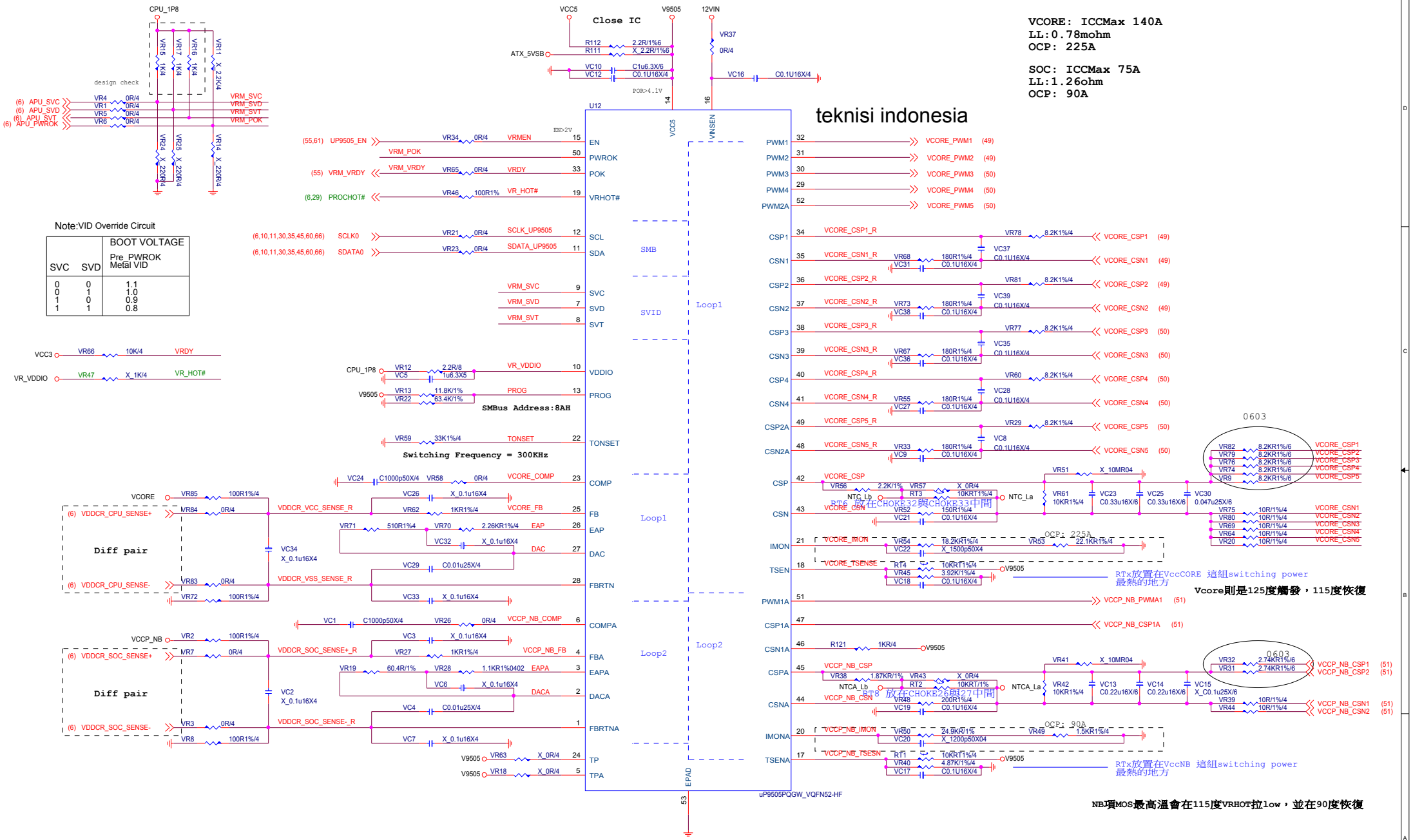
VCORE: ICCMax 140A
LL:0.78mohm
OCP: 225A
SOC: ICCMax 75A
LL:1.26ohm
OCP: 90A
teknisi indonesia
Close IC
design check
Note:VID Override Circuit
BOOT VOLTAGE
Pre_PWROK Metal VID
SVC SVD
0 0 1.1
0 1 1.0
1 0 0.9
1 1 0.8
SMBus Address:8AH
Switching Frequency = 300KHz
Diff pair
Diff pair
SMB
SVID
Loop1
Loop1
Loop2
Loop2
RT6 放在CHOKE32與CHOKE33中間
RT8 放在CHOKE26與27中間
RTx放置在VccCORE 這組switching power 最熱的地方
RTx放置在VccNB 這組switching power 最熱的地方
Vcore則是125度觸發，115度恢復
NB項MOS最高溫會在115度VRHOT拉low，並在90度恢復
uP9505PQGW_VQFN52-HF
MICRO-STAR INT'L CO.,LTD
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CPU Power UP9505 10+2
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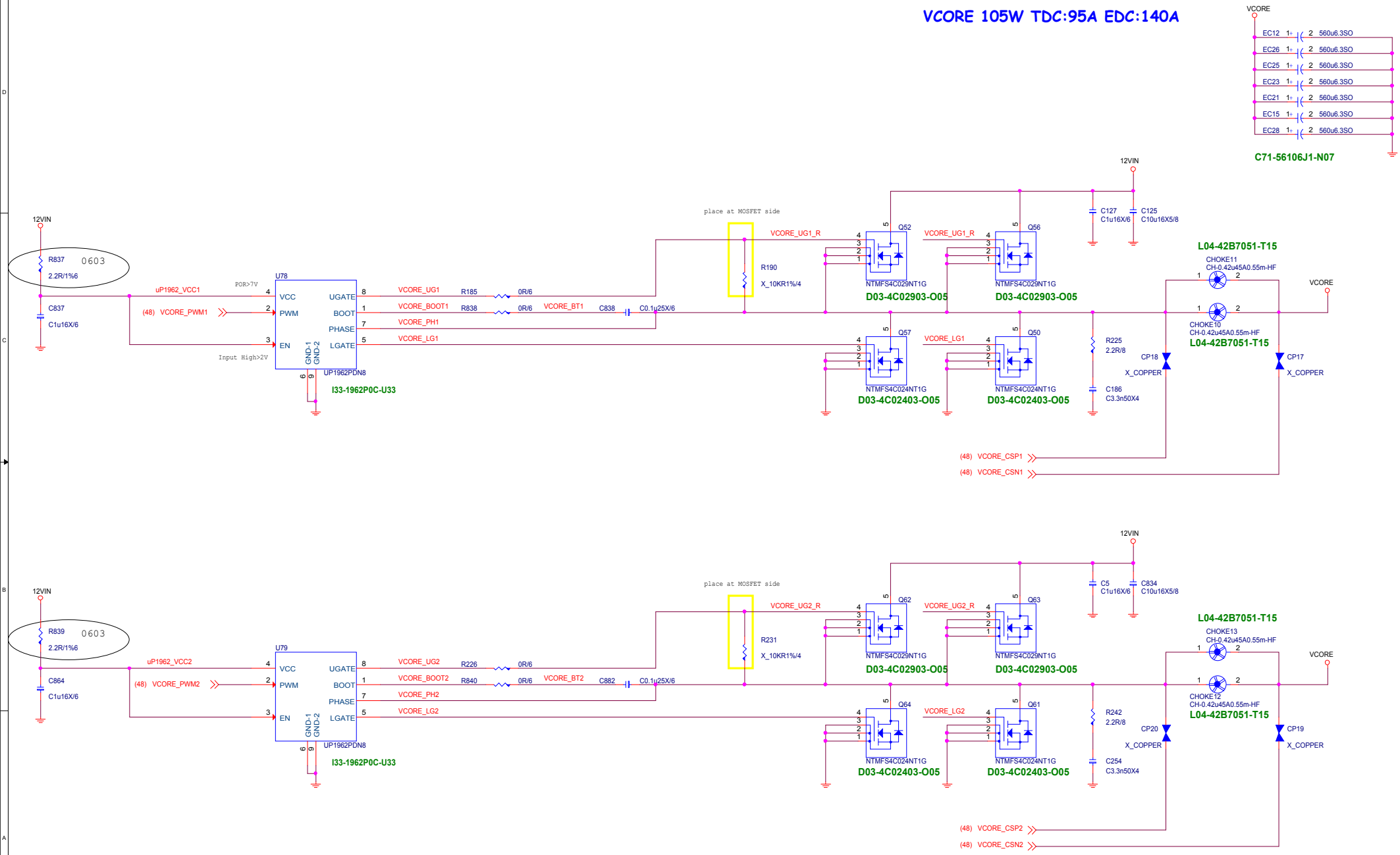
VCORE 105W TDC:95A EDC:140A



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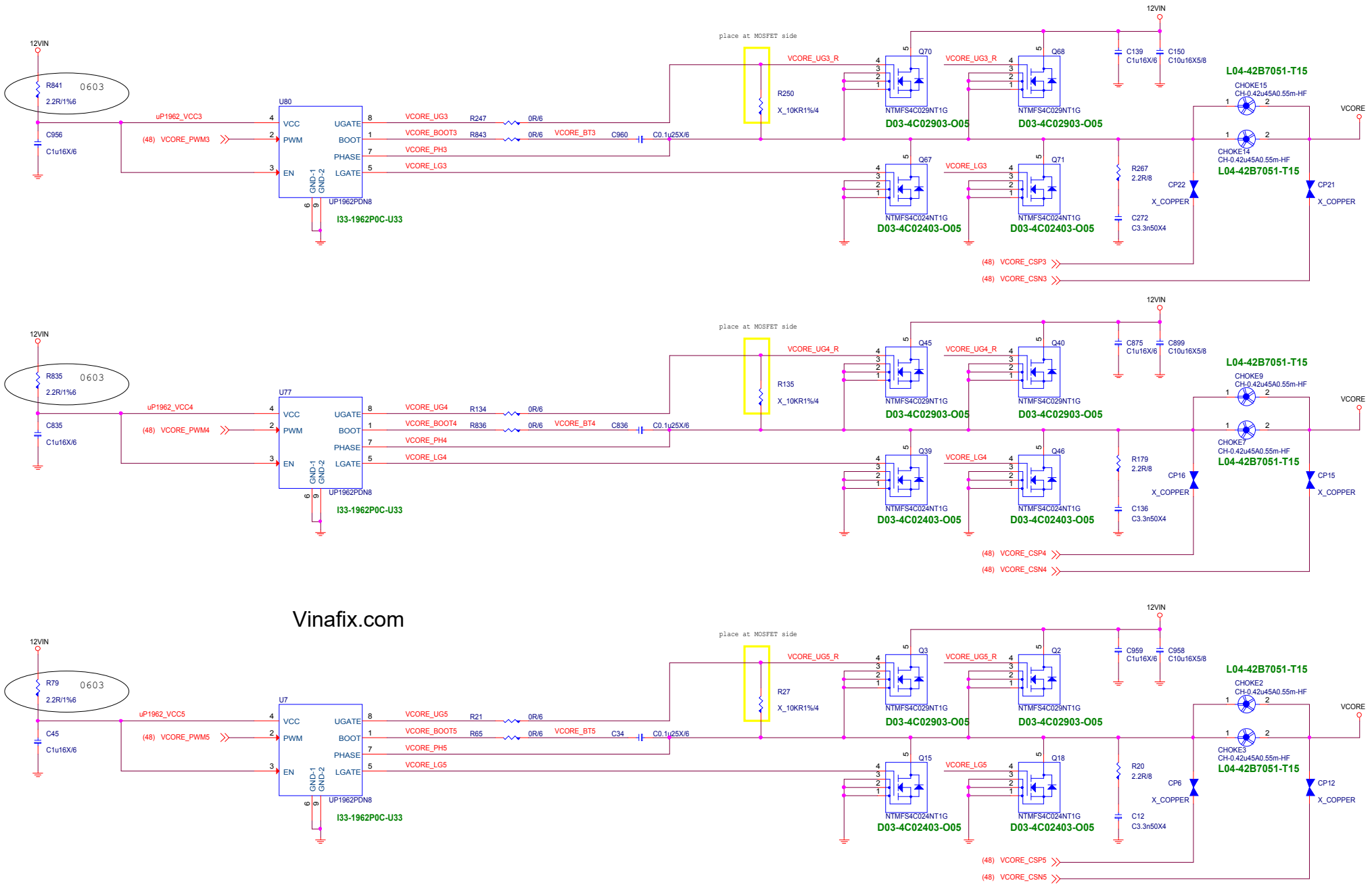

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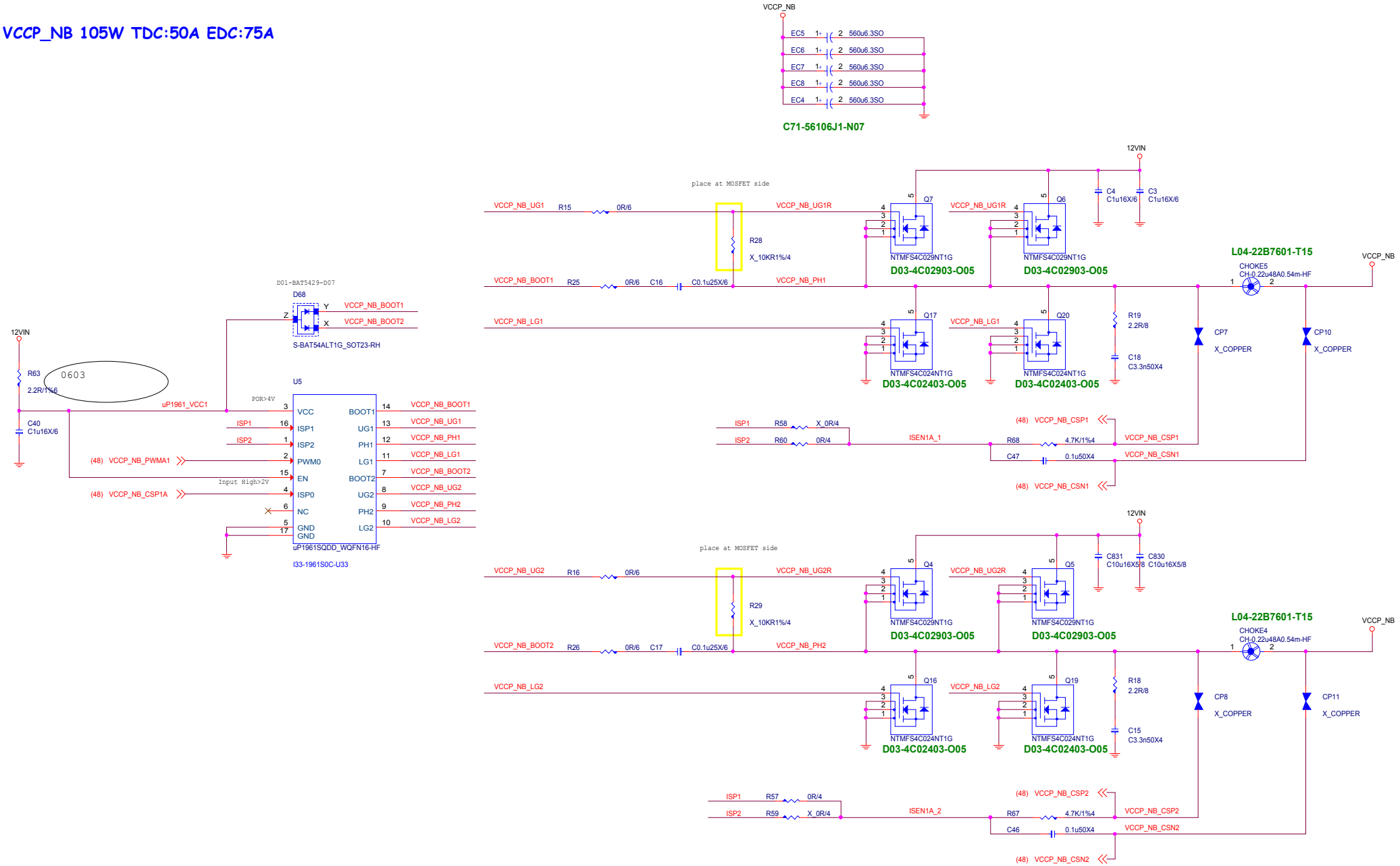
VCCP_NB 105W TDC:50A EDC:75A



MICRO-STAR INT'L CO.,LTD		
MS-7B78		
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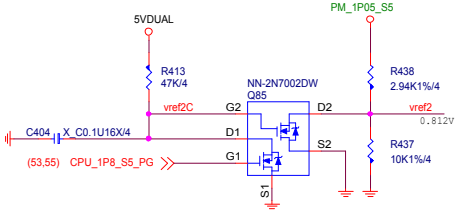
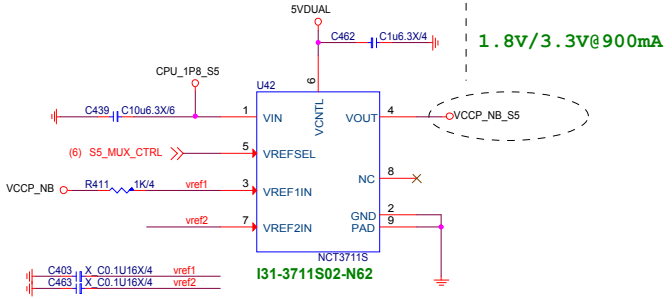
FOR
VCCP_SOC_S5
0.9A

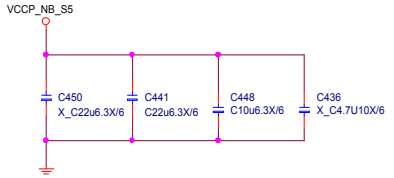
S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

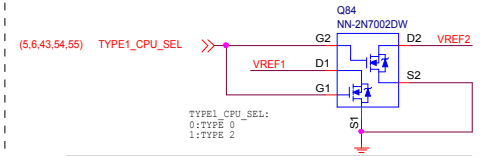
H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)









CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

MICRO-STAR INT'L CO.,LTD

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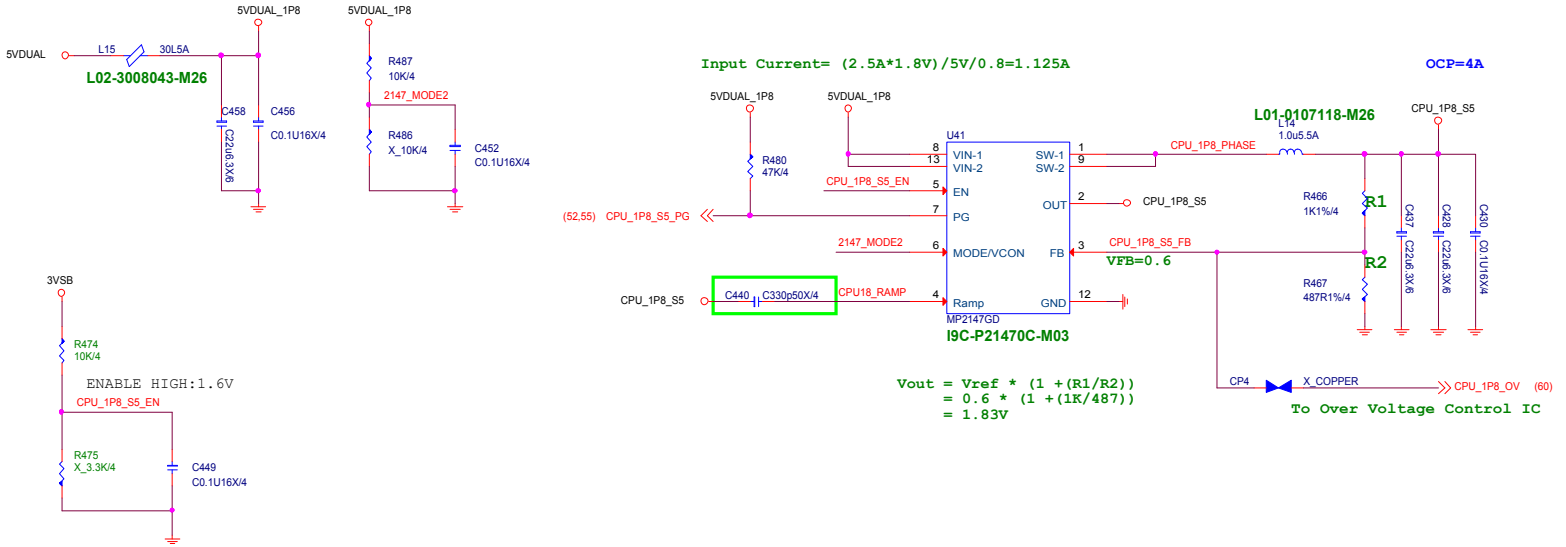
CPU 1.8V S5 @0.5A

1.8V S5@0.5A



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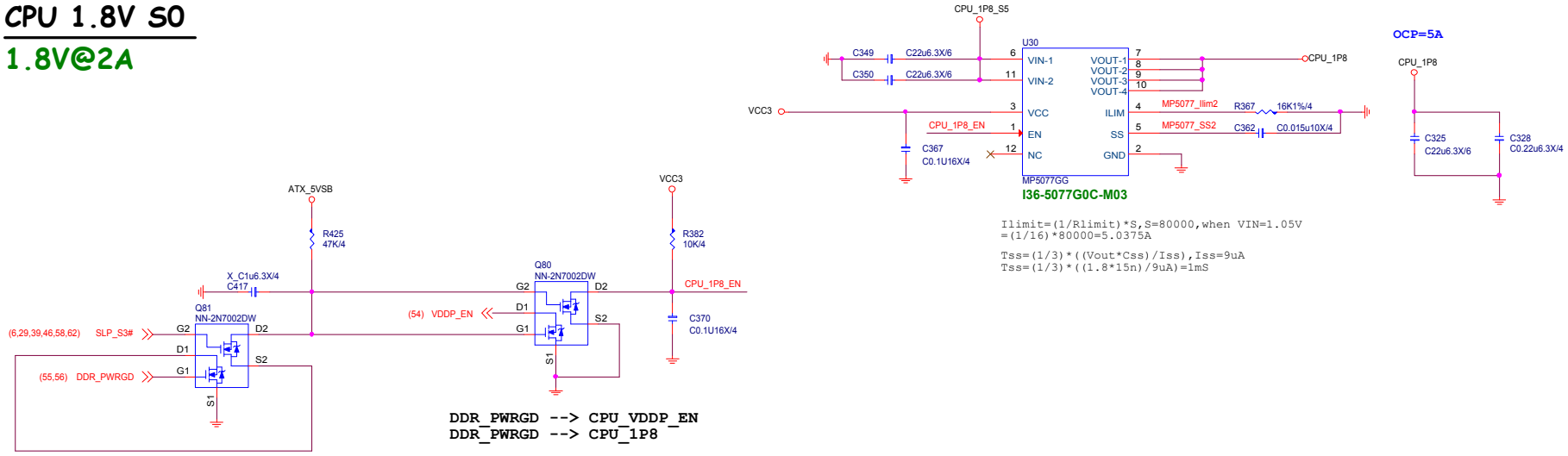
CPU 1.8V S0

1.8V@2A



MICRO-STAR INT'L CO.,LTD		
MS-7B78		
Size: Custom	Document Description: CPU Power 1.8_S0 / S5	Rev: 10
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CPU_VDDP_S0

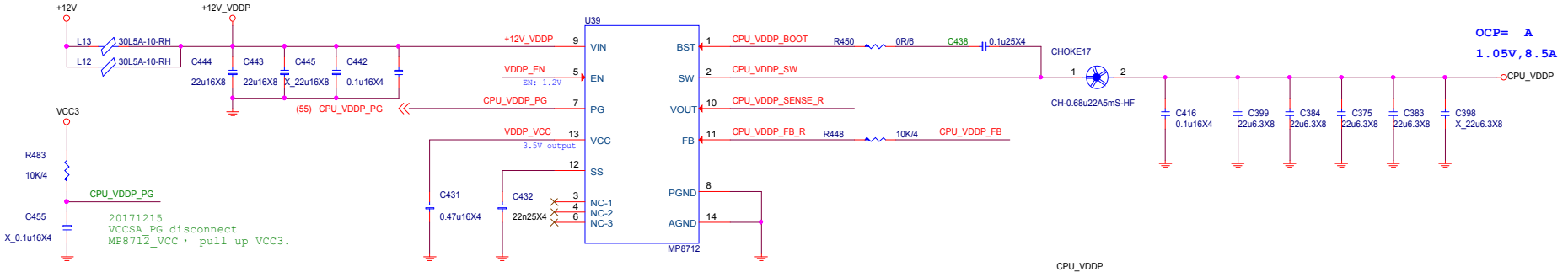
1.05V/0.9V@S0:8.5A

Input Current= (8.5A*1.05V)/12V/0.8=2.23A

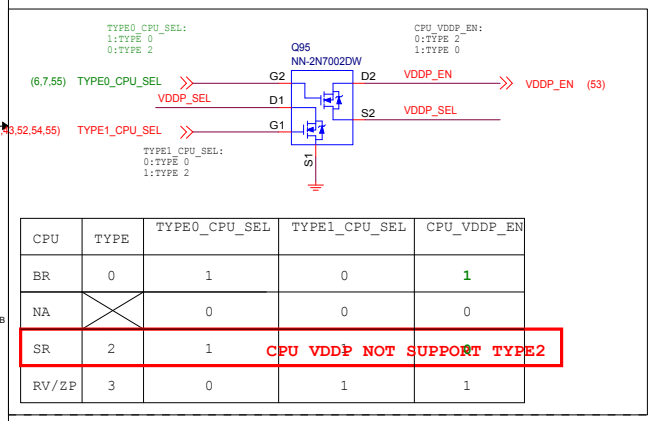
S0:8.5A
S5:1A

OCP=14A

Iin=11.1A*1.05V/0.8/12V=1.21A
L02-3008043-M26
Over 85℃ ,Rated Current
1.5A.

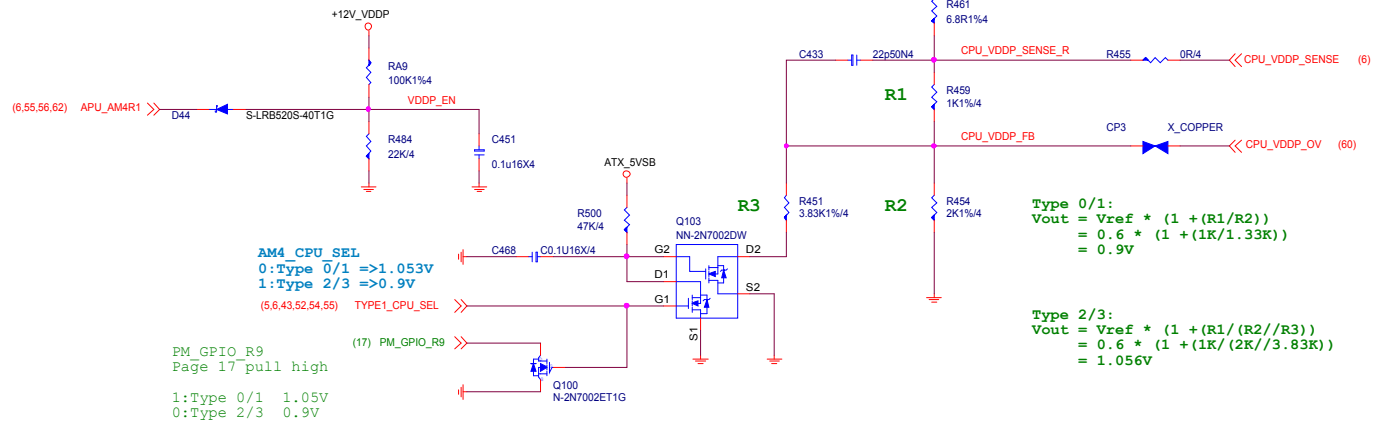


OCP= A
1.05V,8.5A



CPU	TYPE	TYPE0_CPU_SEL	TYPE1_CPU_SEL	CPU_VDDP_EN
BR	0	1	0	1
NA	X	0	0	0
SR	2	1	0	0
RV/ZP	3	0	1	1

CPU VDDP NOT SUPPORT TYPE2



Type 0/1:
Vout = Vref * (1 +(R1/R2))
= 0.6 * (1 +(1K/1.33K))
= 0.9V

Type 2/3:
Vout = Vref * (1 +(R1/(R2//R3))
= 0.6 * (1 +(1K/(2K//3.83K))
= 1.056V

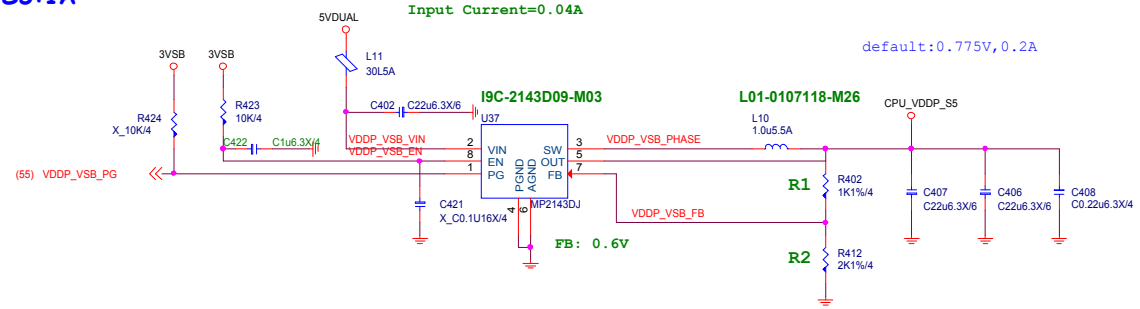
CPU_VDDP_S5

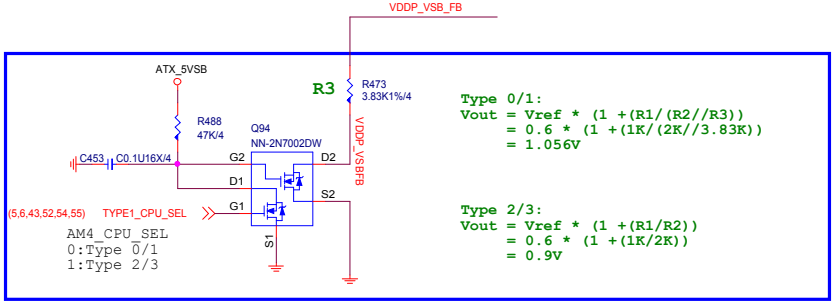
(VDDCR_SOC_S5)

1.05V/0.9V
S5:1A

Input Current=0.04A

default:0.775V,0.2A





Type 0/1:
Vout = Vref * (1 +(R1/(R2//R3))
= 0.6 * (1 +(1K/(2K//3.83K))
= 1.056V

Type 2/3:
Vout = Vref * (1 +(R1/R2))
= 0.6 * (1 +(1K/2K))
= 0.9V

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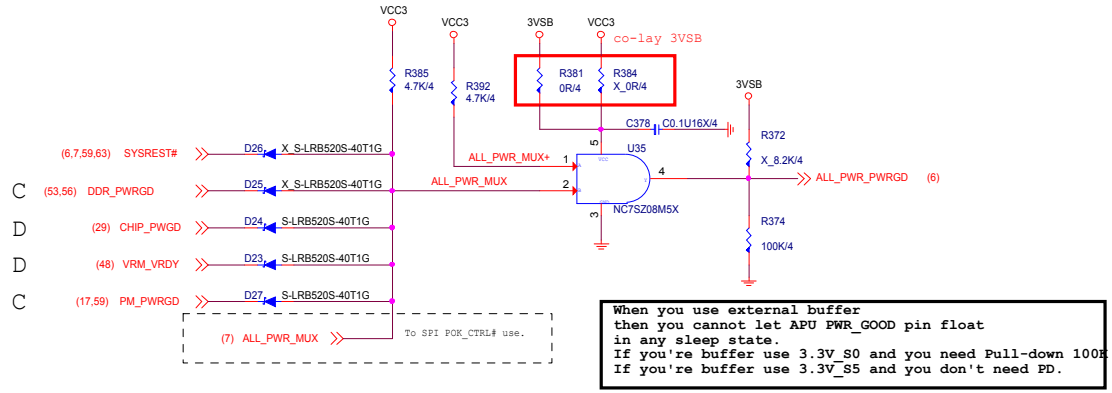
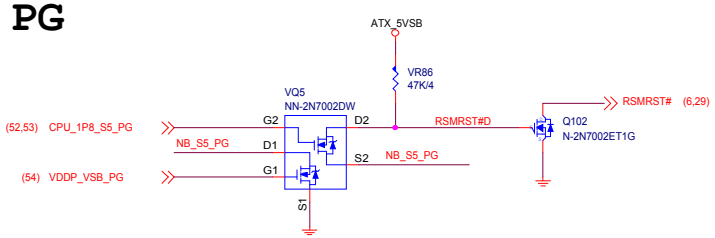
ALL POWER GOOD MUX

S0 PG

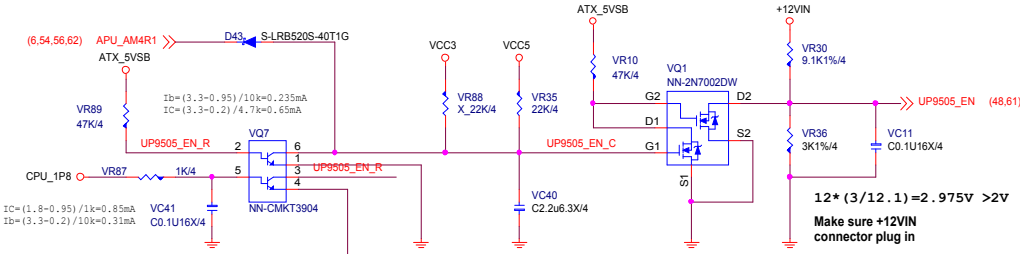


When you use external buffer
then you cannot let APU PWR_GOOD pin float
in any sleep state.
If you're buffer use 3.3V_S0 and you need Pull-down 100R
If you're buffer use 3.3V_S5 and you don't need PD.

S5 PG



VRM_Enable circuit



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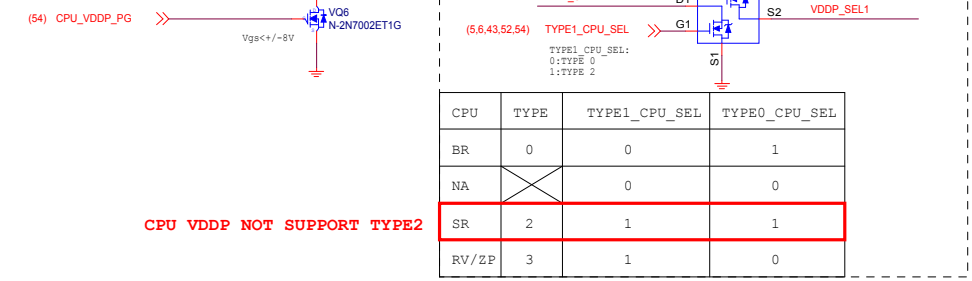

CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA		0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VDDP NOT SUPPORT TYPE2

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DDR4_1.2V@26.2A

15.5A FOR CPU
9.5A FOR 4DIMM
1.2A FOR DDR VTT

Rocpset:4.32K
OCP=Rocset*Rdson(Low side)/10uA
=8.2K*10uA/4mohm
=20.5A

(6,54,55,62) APU_AM4R1 — D18 S-LRB520S-40T1G — DDR_EN
(29) SIO_VDDQ_EN — R198 0R/4 — DDR_EN — 3.12V

EN:VIH2.4V
EN pin Maximum:5.5V,RECOMMENDED:3.6V

Follow CRB

5VDIMM — R188 10K/4

EN:VIH2.4V
EN pin Maimum:6.5V

(53,55) DDR_PWRGD

5VDIMM — R182 10R/8 — DDR_VCC — C134 C4.7u6.3X/6

U17 RT8125EGQW
DDR_EN → EN
PGOOD → (53,55) DDR_PWRGD
DDR_REFOUT → REFOUT
REFIN ← DDR_REFIN
VCC ← 5VDIMM
GND
BOOT → DDR_BOOT1 — R172 0R/4 — C126 C0.1U16X/4
PHASE → DDR_PH1
UGATE → DDR_UG1
LGATE/OCSET → DDR_LG1
FB → DDR_FB

C153 C1000p50X/4
R195 649R1%04
C152 C1000p50X/4

FB:0.8V

I32-8125E0C-R11

Vout = Vref * (1 + (R1/R2))
= 0.8 * (1 + (10K/14.3K))
= 1.218V

R1

VCC_DDR — close to DIMM side — R199 10R/4
DDR_VSENP — R187 10K1%/4 — C151 X_C0.1U16X/4 — R194 0R/4 — VDDIO_MEM_S3_SENSE (6)

R2 — R183 19.1K1%/4

CP1 X_COPPER — DDR_OV (60)

Input Current=(26.2*1.2)/5/0.8=7.86A

L04-12A7811-T15
CHOKE6 CH-1.2u15A1.7m

5VDUAL_IN_DDR
C84 C1u16X/6
C93 C10u6.3X/6
EC9 560u6.3SO
EC10 560u6.3SO
5VDIMM — C140 C0.1U16X/4

C71-56106J1-N07
C71-56106J1-N07

DDR_UG1 — R124 0R/6 — DDR_UG1_R
Q31 NTMFS4C029NT1G D03-4C02903-O05
Q32 NTMFS4C029NT1G D03-4C02903-O05
R127 X_10K/4

L04-47B7981-T15
OCP=32A
CHOKE8 CH-0.47u42A0.81m

DDR_PH1
VCC_DDR
C135 C1u6.3X/4
C110 C22u6.3X/6
EC17 560u6.3SO
EC13 560u6.3SO
EC20 560u6.3SO

C71-56106J1-N07
C71-56106J1-N07
C71-56106J1-N07

DDR_LG1
Q36 NTMFS4C024NT1G D03-4C02403-O05
Q35 NTMFS4C024NT1G D03-4C02403-O05
R138 2.2R/8
C108 C3300p50X/4
snubber

R133 6.8K1%/4

VCC_DDR
EC27 560u6.3SO
EC14 560u6.3SO

C71-56106J1-N07
C71-56106J1-N07

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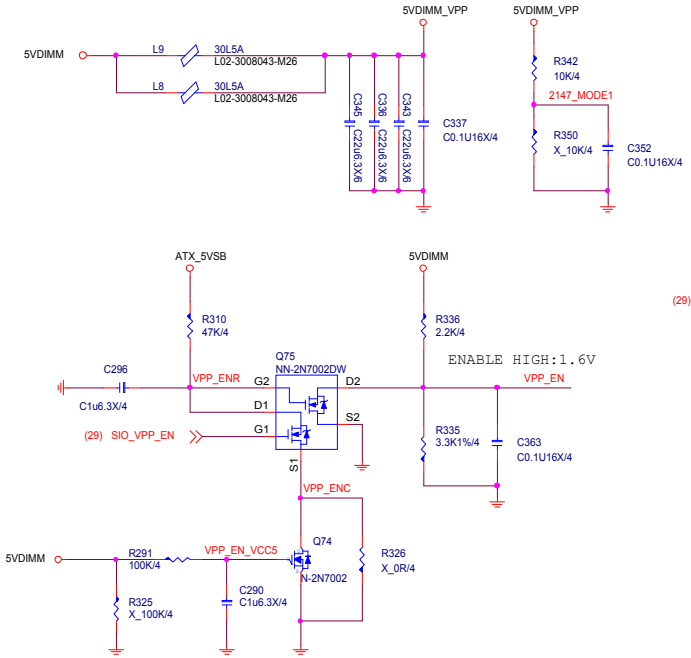
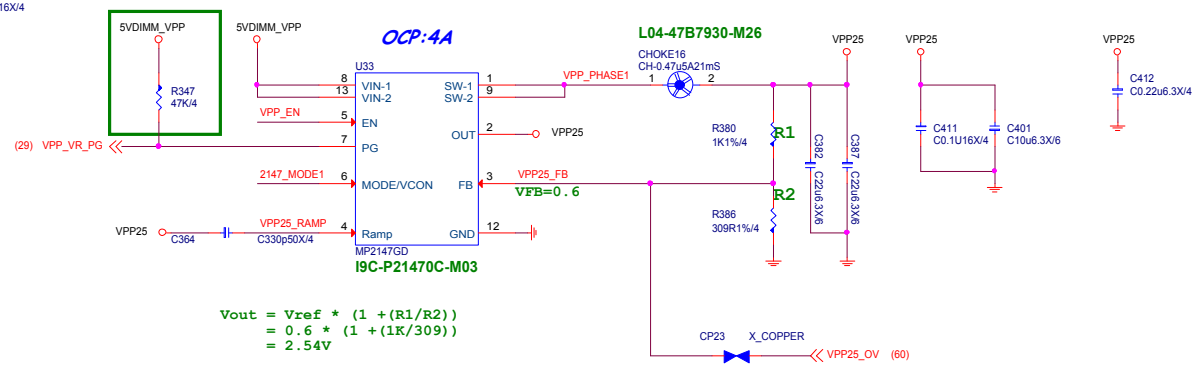
4DIMM : VPP25

2.5V@2.24A



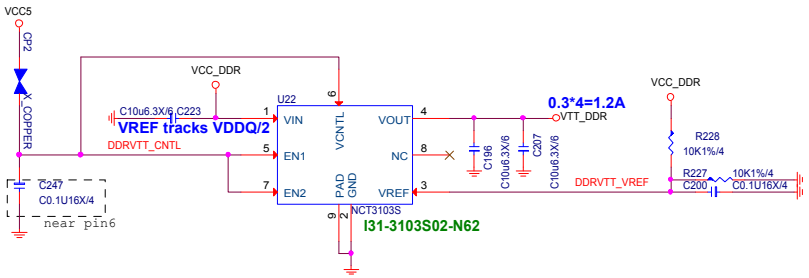
Input Current=(2.5*2.24)/5/0.8=1.4A

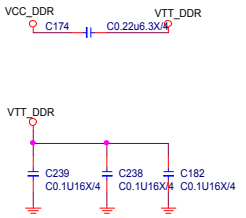


Vout = Vref * (1 +(R1/R2))
= 0.6 * (1 +(1K/309))
= 2.54V

DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .





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Size: Custom	Document Description: DDR VPP25 / VTT	Rev: 10
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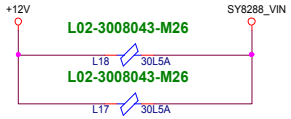
FOR Promontory 1.05V_S0

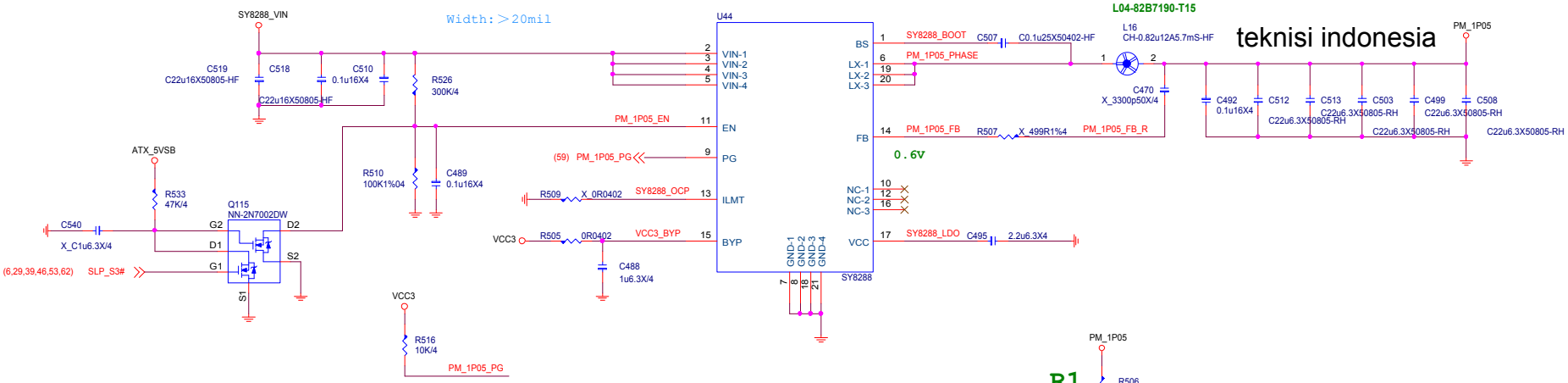
1.05V
S0:5.5A
S5:0.05A



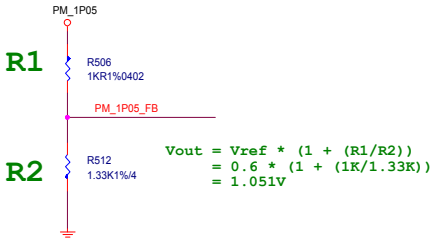
Input Current= (5.5A*1.05V)/12V/0.8=0.6A

OCP=12A

1.05V@5.5A

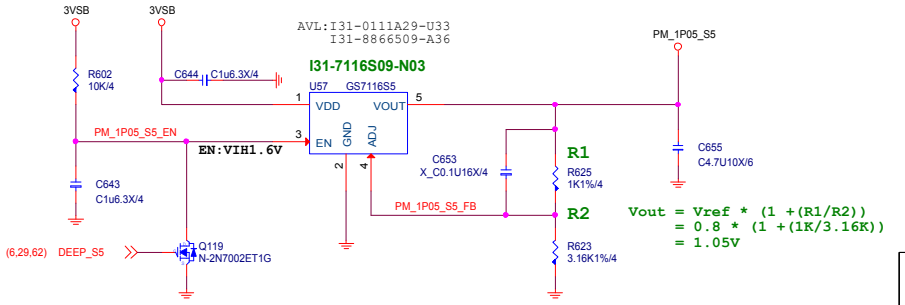


SY8288_OCP	OCP
0	8A
floating	12A
1	16A



FOR Promontory 1.05V_S5

1.05V@0.05A



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Custom	PROM - SY8288RAC / 1.05V	10

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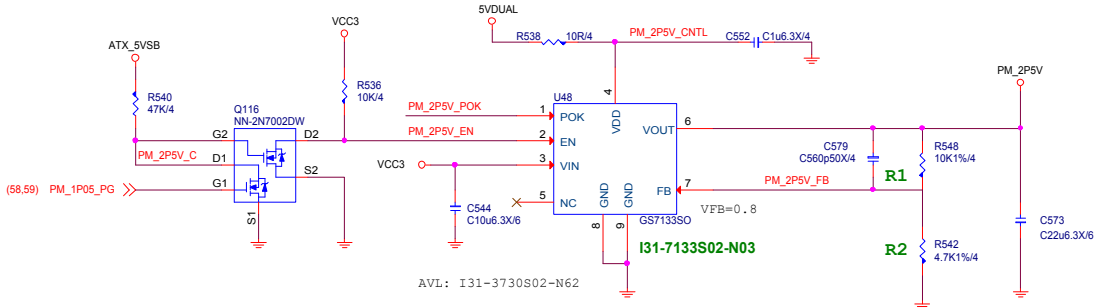
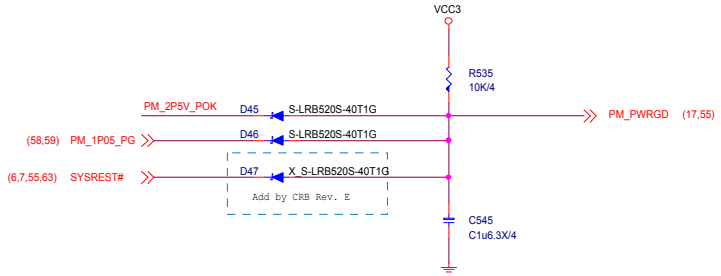
Promontory-2.5V

2.5V@900mA



Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(10K/4.7K))
= 2.502V



MICRO-STAR INT'L CO.,LTD

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Custom	PROM - GS7133 / 2.5V	10

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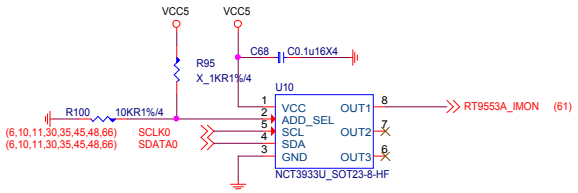
Over Voltage Control IC

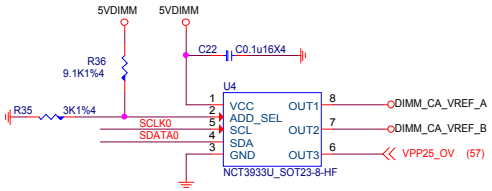
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

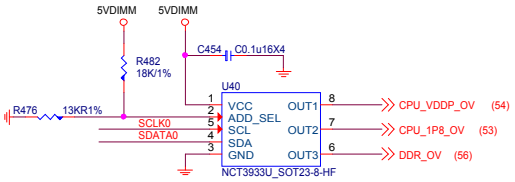
0x2A:RH=OPEN,RL=10K



0x28:RH=9.1K,RL=3K



0x26:RH=18K,RL=13K



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UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0X28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

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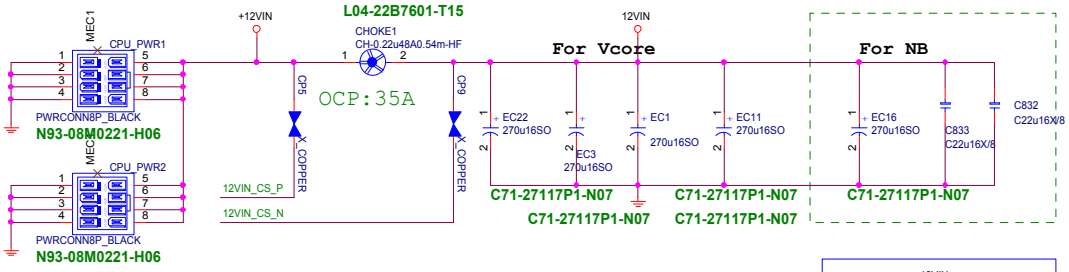
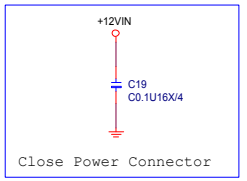
CPU POWER CONNECTOR





NB

D=Vout/Vin			
Vin	= 12		> input voltage
Vout	= 1.4		> output Vcore
D	= 0.116667		

I o = Icore(max)*0.8			
I core(max)	= 75		> Vcore current
I avg.	= 75	A	

I ripple={ Io*√D*√(1-D)} / Phase		
Phase	= 2	phase
I ripple	= 12.03835	A

How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COETEMP	=	1	
Input Cap.	=	3	pcs.

VCCP

D=Vout/Vin			
Vin	= 12		> input voltage
Vout	= 1.4		> output Vcore
D	= 0.116667		

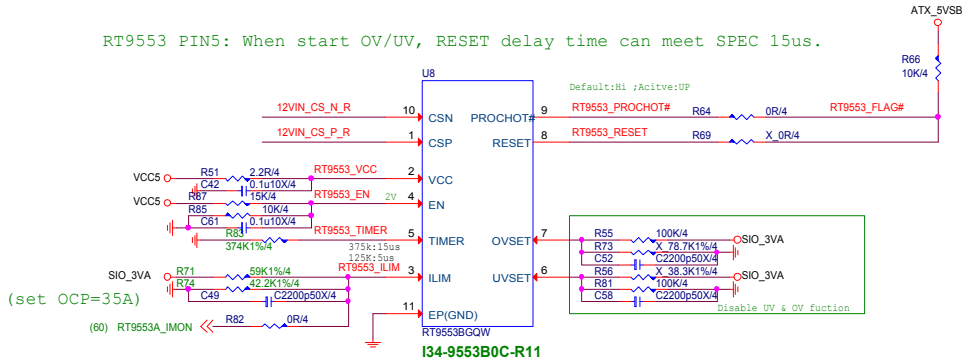
I o = Icore(max)*0.8			
I core(max)	= 125		> Vcore current
I avg.	= 125	A	

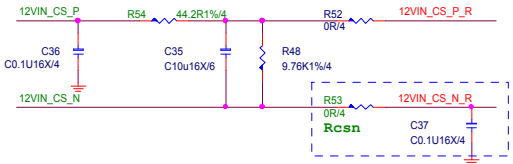
I ripple={ Io*√D*√(1-D)} / Phase		
Phase	= 4	phase
I ripple	= 10.03196	A

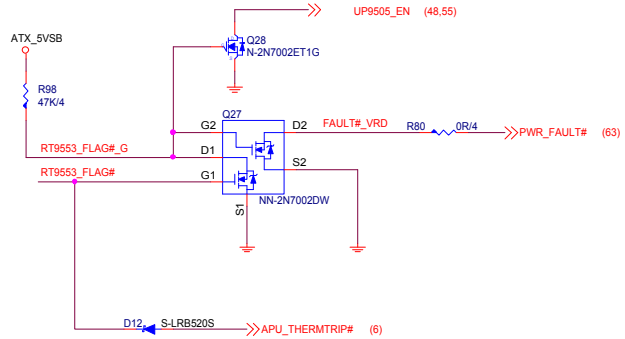
How many pcs. Of Cap.			
I ripple(cap)	=	5000	m A
COETEMP	=	1	
Input Cap.	=	3	pcs.

RT9553B CURRENT SENSE

RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.







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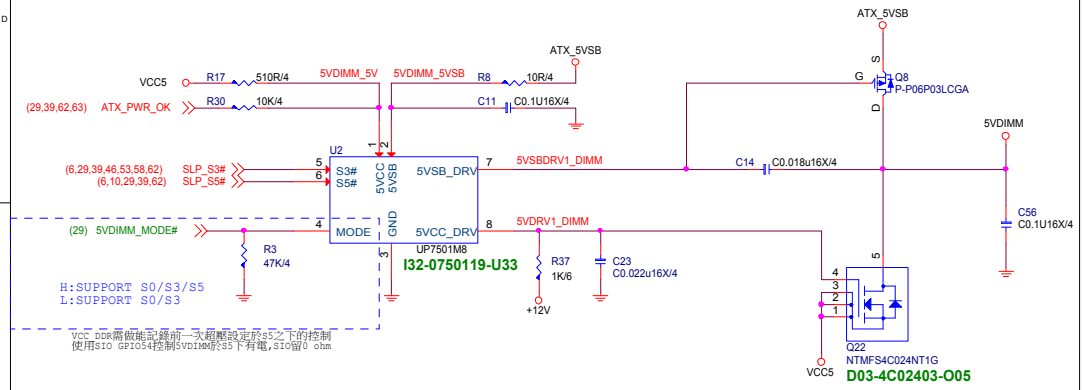
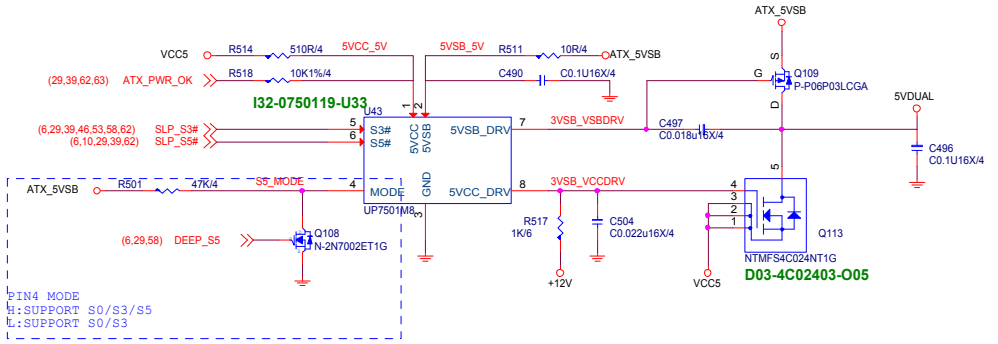
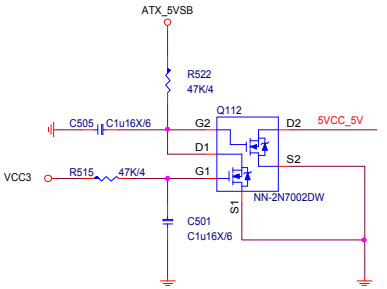
5VDIMM FOR DDR



5VDUAL For 3VSB、CPU 1.8V 、 VDDP





For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

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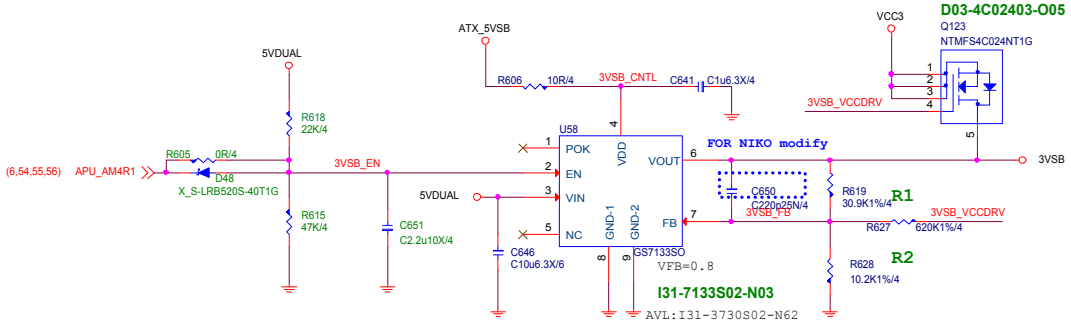
3VSB cost down

3.3V@2.63A

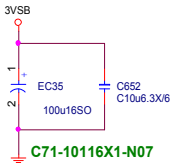
1.05V@0.05A
VDDBT_RTC_G@4.5uA
FCH@0.07A
CPU@0.25A
PCI @0.75A
*PCIE*4 @1.5A*
USB TYPE-C @0.9mA



VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.

Vout = Vref * (1 +(R1/R2))
= 0.8 * (1 +(30.9K/10.2K))
= 3.22V

OCP=12A
2.63A



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	MS-7B78	
Size: Custom	Document Description: ACPI - 5VDIMM / 3VSB	Rev: 10
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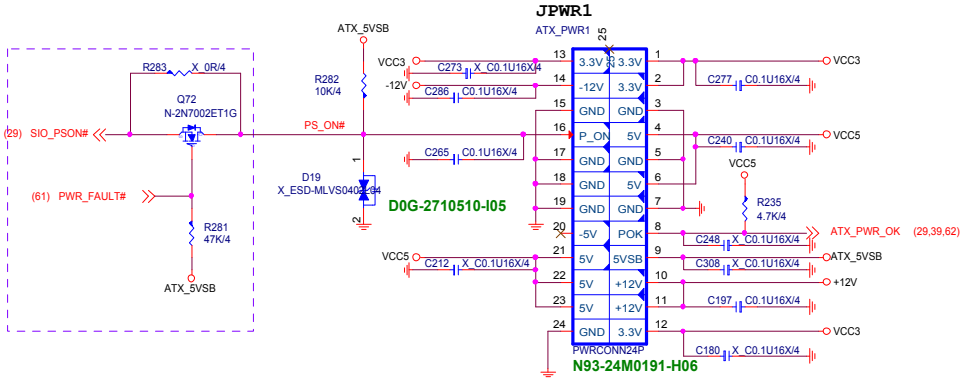
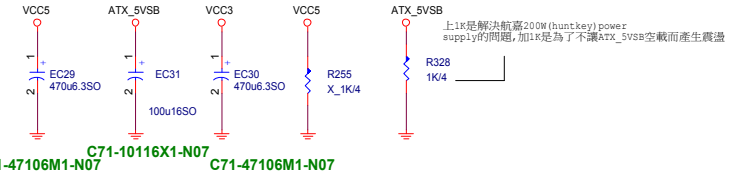
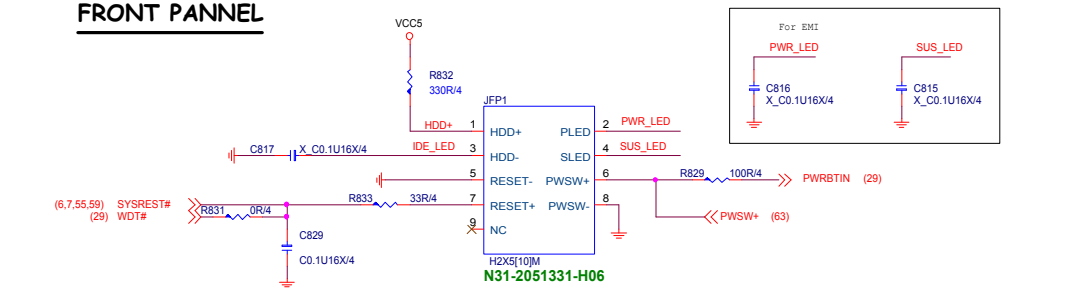
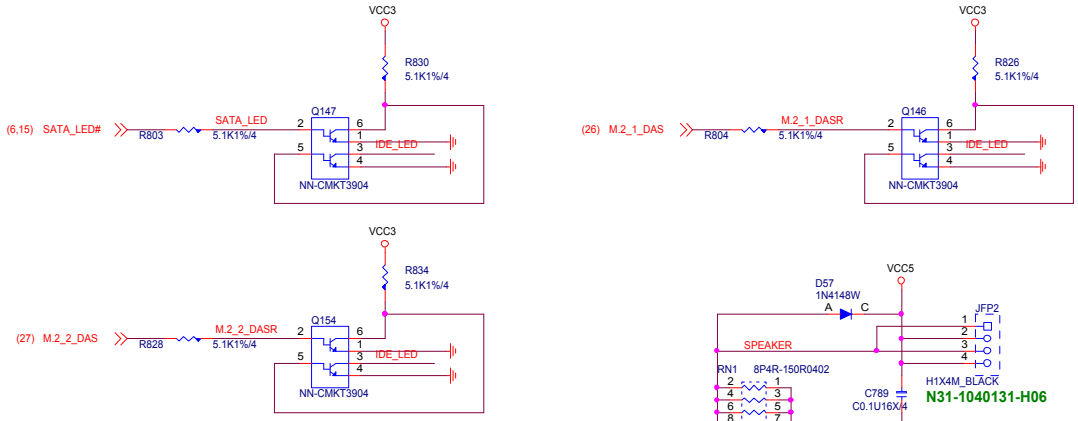
ATX POWER CONNECTOR



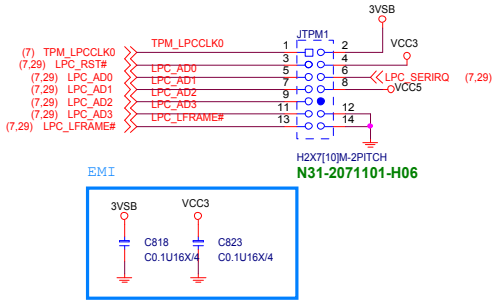


FRONT PANNEL

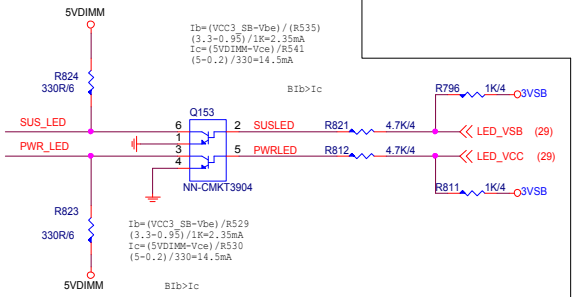




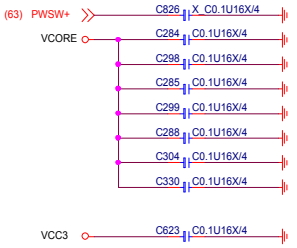
TPM



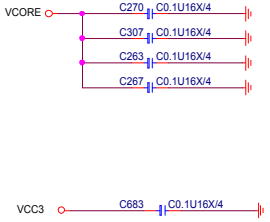
LED (for NCT6793D)

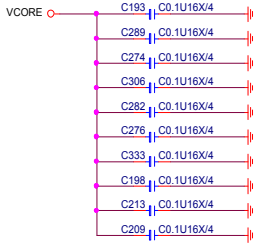


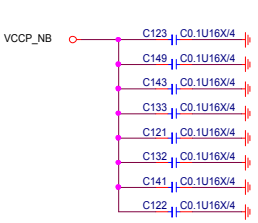
Add for EMI



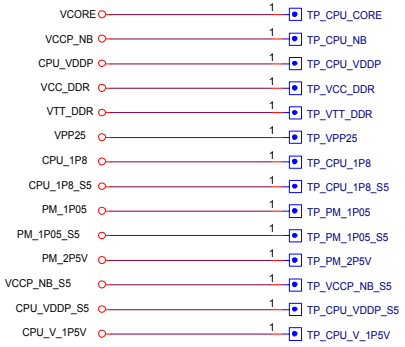
return path







Voltage Mearsure Point



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Size: Custom	Document Description: ATX power - FrontPanel / EMI	Rev: 10
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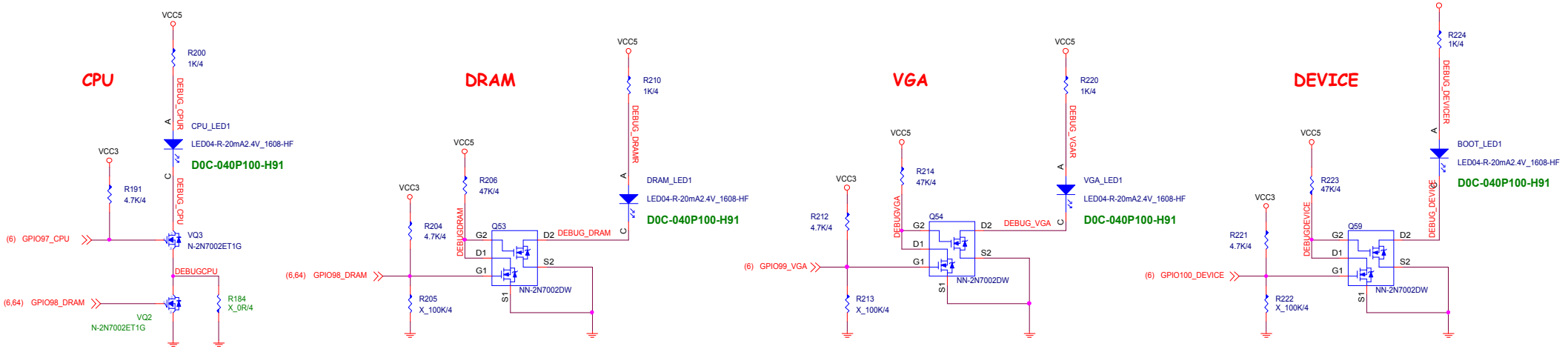
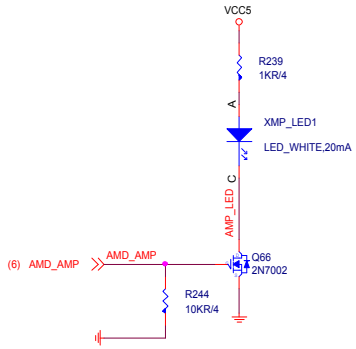
EZ Debug LED



LEDGPIO	GPIO97	GPIO98	GPIO99	GPIO100
亮	GPI PULL HIGH	GPO PO LOW	GPO PO LOW	GPO PO LOW
滅	GPO LOW	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)	GPO HIGH (default HIGH)

LED亮燈時同時將CPU LED關掉

AMD AMP Detect LED



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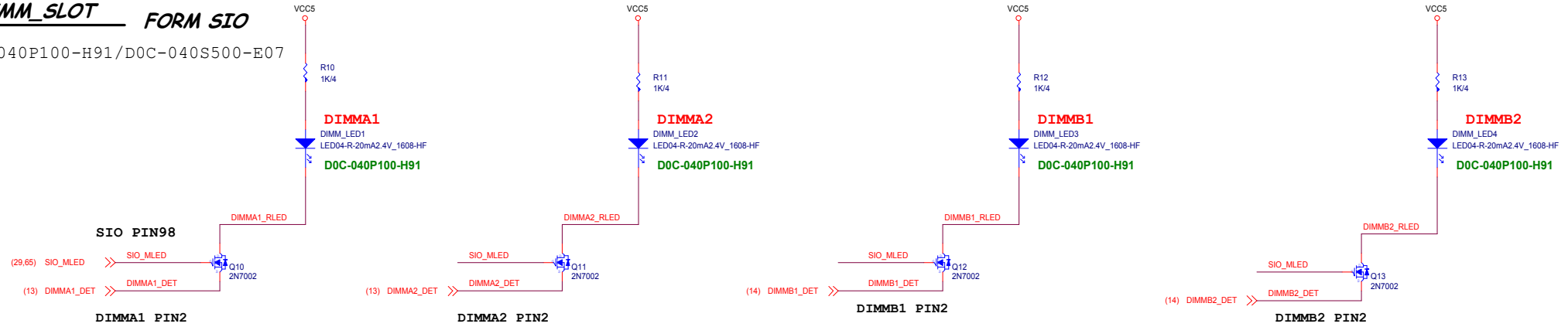
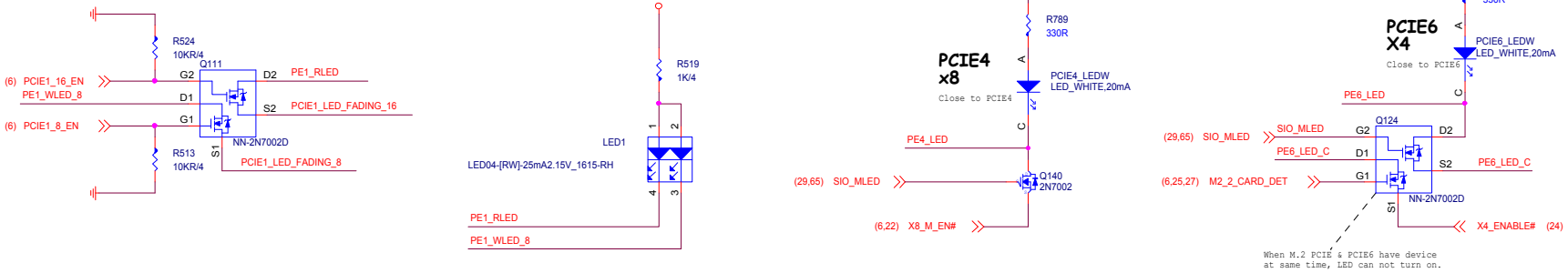
DIMM_SLOT FORM SIO

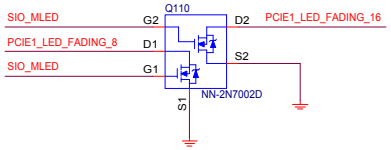
D0C-040P100-H91/D0C-040S500-E07



PCIE_SLOT LED FORM SIO



	x16	x8	x4
PCIE1	Red	X	X
PCIE1	X	White	X
PCIE4	X	White	X
PCIE6	X	X	White



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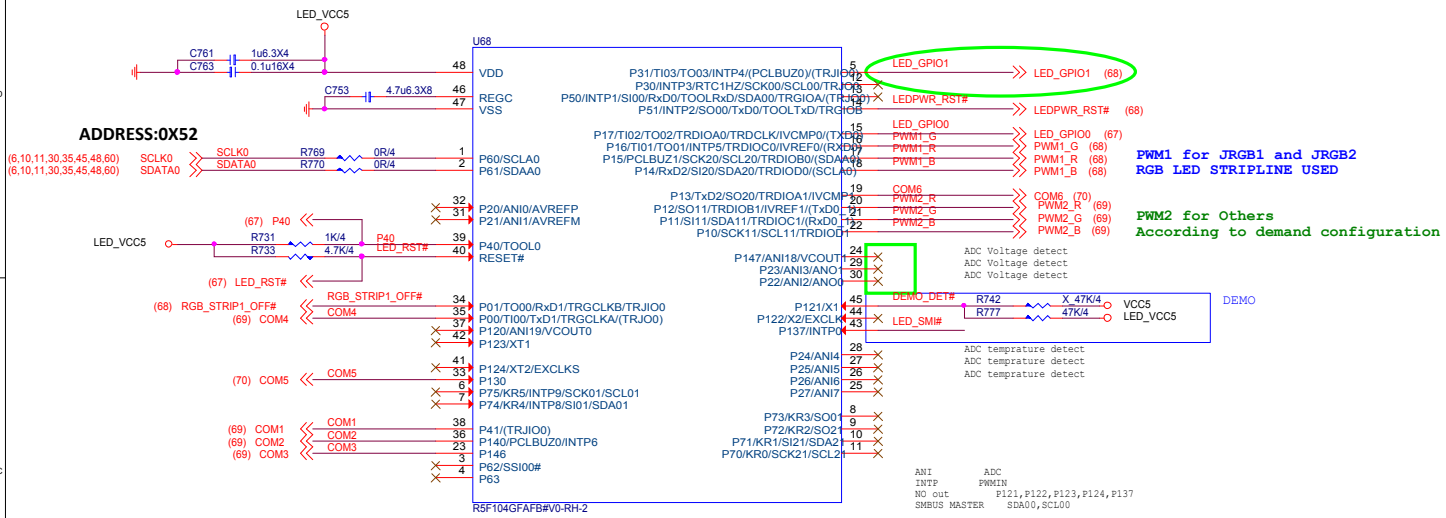
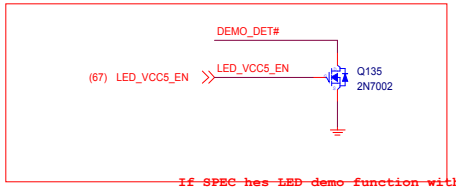
48 PIN LED MCU

C345 & C359 near VDD Pin.



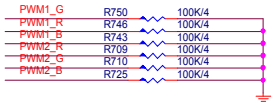
PWM1 for JRGB1 and JRGB2
RGB LED STRIPLINE USED

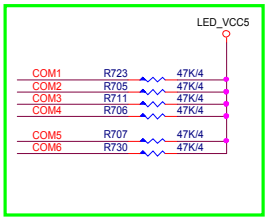
PWM2 for Others
According to demand configuration



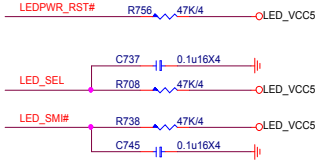
~~If SPEC hes LED demo function without demo button,~~
~~DEMO_DET# must pull up to LED_VCC5 and control by LED_VCC5_EN.~~
~~PS. R1000 remove, R1457 and Q296 need to stuff~~

Control	Net Name	PWM USE	Connector
PCH	LED_GPIO1	No Use	JPIPE_LED2
Audio	COM1~4	PWM2	RGB LED
Board Side LED	COM5~8	PWM2	RGB LED
LED STRIPLINE	RGB_STRIP1_OFF#	PWM1	JLED1
LED STRIPLINE	RGB_STRIP1_OFF#	PWM1	JLED2
IO Cover	LED_GPIO0	No Use	JPIPE_LED1





COM1~8 for PWM2
According to demand configuration.
Can configuration COM1~8,
To achieve 8 group Non-synchronized
onboard LED control.



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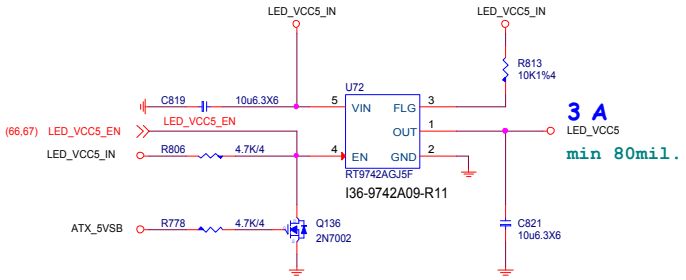
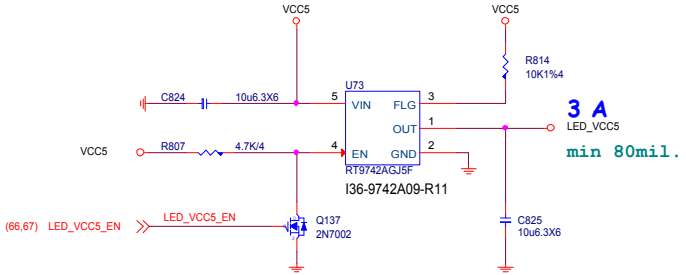
EXTERNAL POWER INPUT

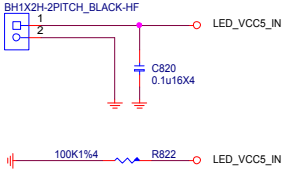




External Power

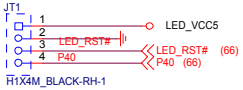
2A Connector

N32-1020CB1-H06



JT1 for FW update

For FW update.

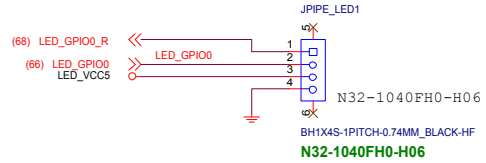


1027 Remove JT1

LED Demo Button

1 PCH HEATSINK LED
PCS LED*0.16W=W

2 AUDIO/IO Cover LED
PCS LED*0.16W=W



3 MOS HEATSINK LED
PCS LED*0.16W=W

Color Demo Jumper

JPIPE_LED3 no SPEC

JPIPE:PIN1:output ,PIN2:input

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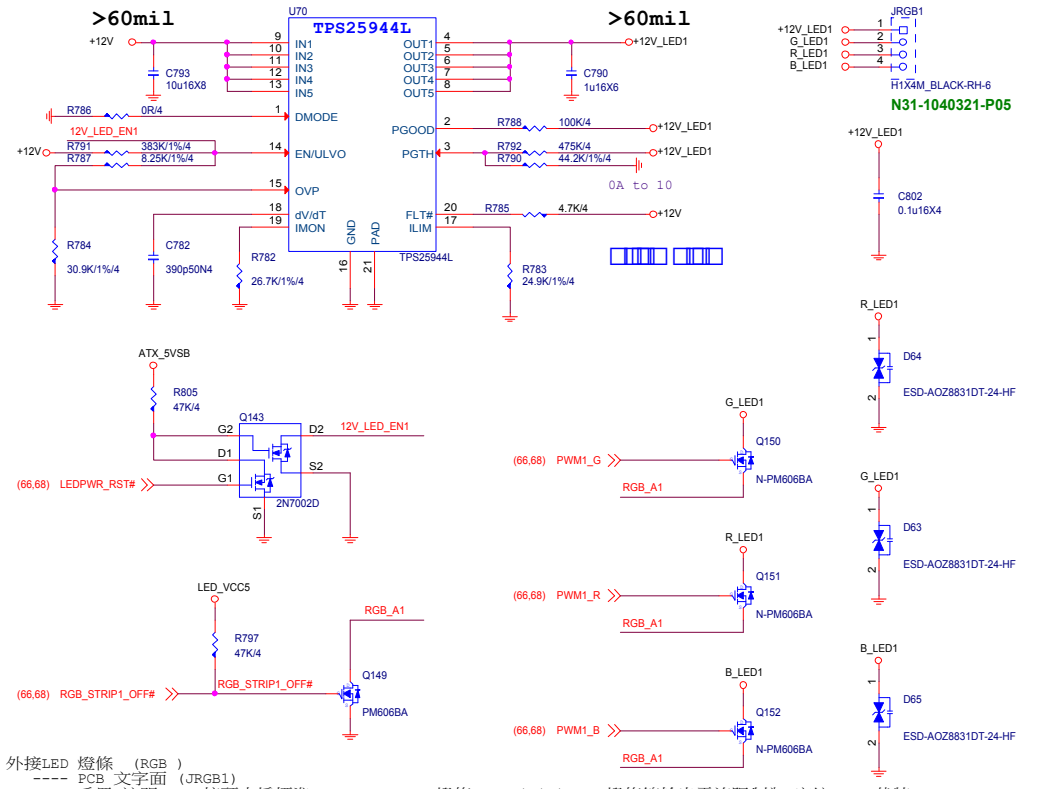
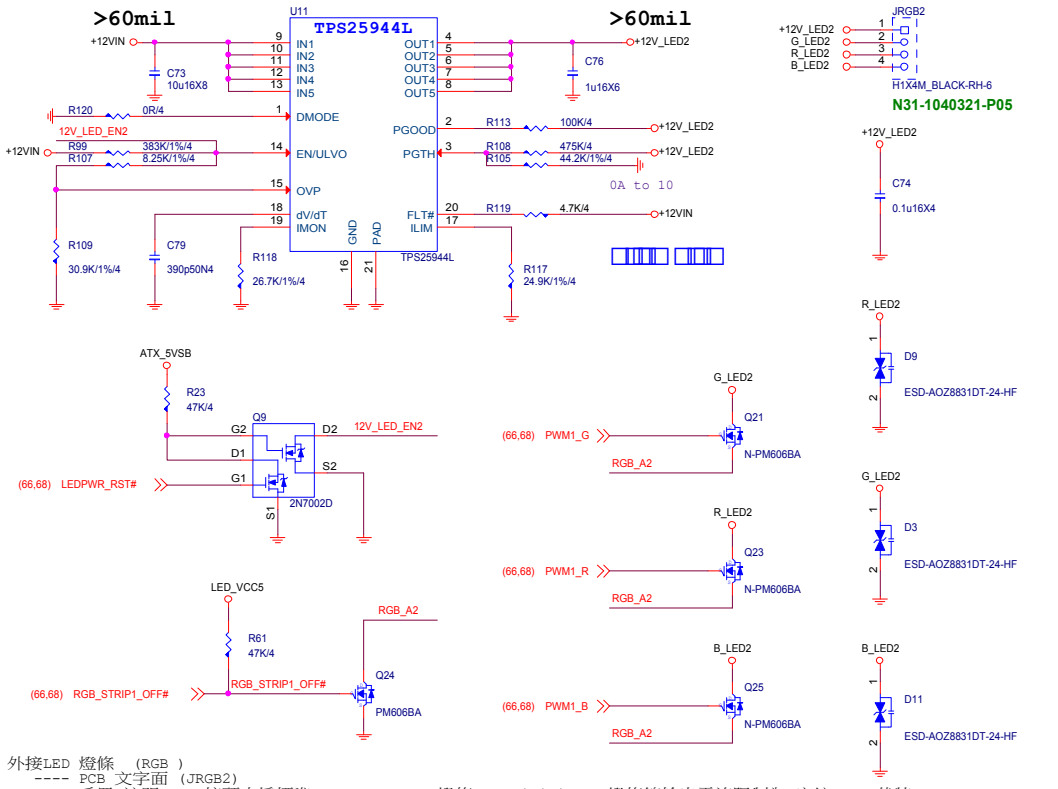
JRGB1



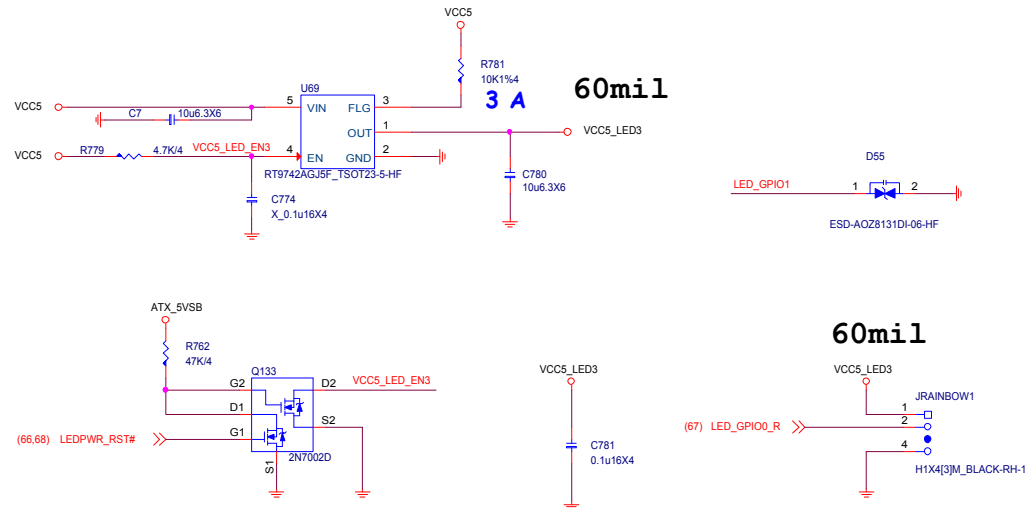
外接LED 燈條 (RGB)
---- PCB 文字面 (JRGB1)
---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

JRGB2

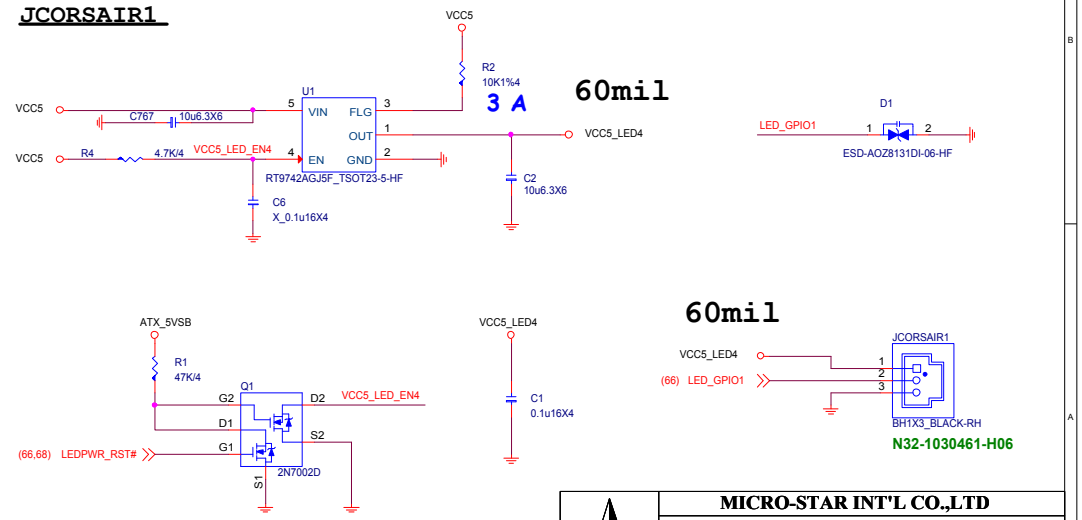


外接LED 燈條 (RGB)
---- PCB 文字面 (JRGB2)
---- 手冊 註明 RGB 接頭支援標準 5050 RGB LED 燈條 (12V/G/R/B) , 燈條總輸出電流限制為3安培 (12 伏特) , 長度限制為2公尺

JRAINBOW1



JCORSAIR1



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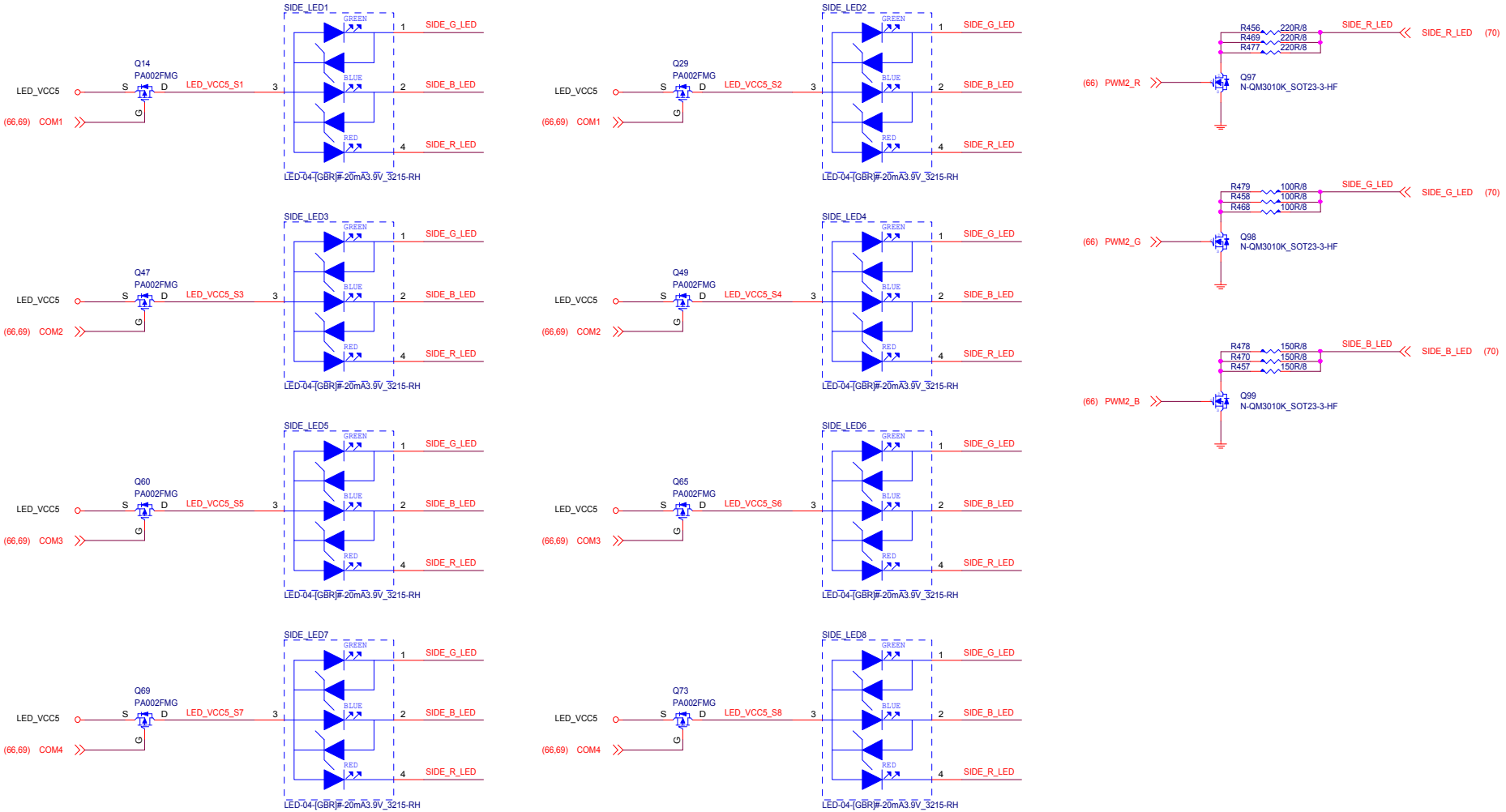
Right Track LED *8



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Size: Custom	Document Description: LED - Mystic Light - 1	Rev: 10
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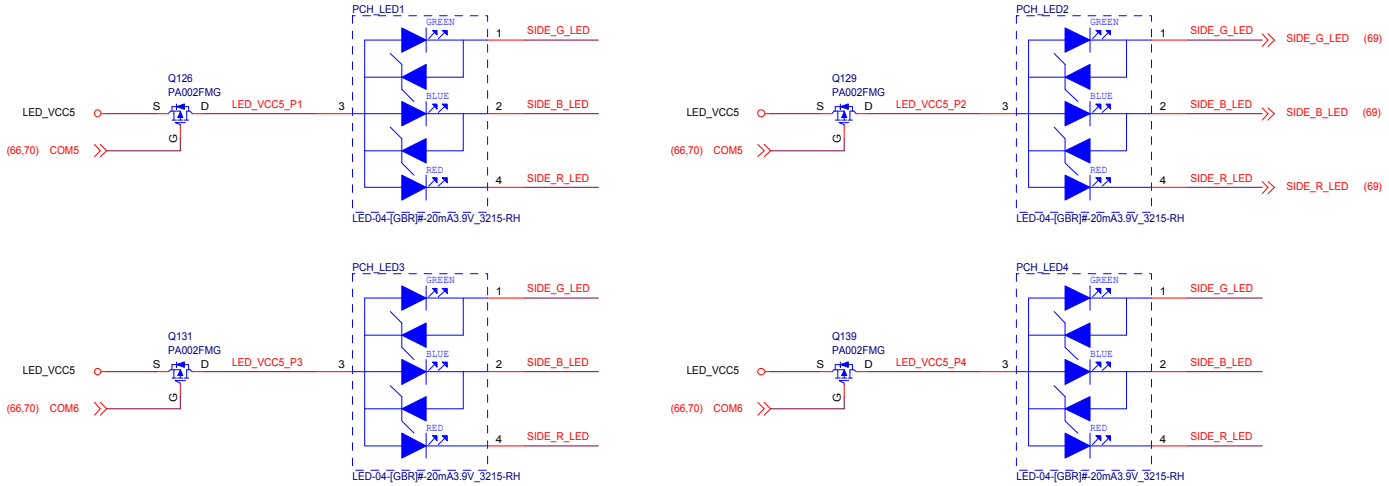
PCH LED *4



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Size	Document Description	Rev
Custom	LED - Mystic Light - 2	10

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Custom	BOM Option	10

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CPU Socket

CPU3

E95-0000021-C22

E95-0000022-C22

Simulation

X_JS3 — SIM1 — X_PIN1*2

X_JS4 — SIM2 — X_PIN1*2

FM9, FM7, FM5, FM2, FM6, FM8, FM10, FM3, FM1, FM4 — X_FM120

Optics Orientation Holes

MH1, MH2, MH3, MH4, MH5, MH6, MH8, MH9, MH7 — X_MH001

C783 0.1u/16X4

C792 0.1u/16X4

MANUAL PART

UEFI1 — G51-M1SPXXA-A09

G51-M1SPXXA-A09

HDMI_LA1 — Label — HDMI

HDMI LABEL

Y01-RHDMI03-000

BAT1_X1

BAT-BCR2032P

AVL:
D06-0100161-F52
D06-0100101-K26

LA6 — MKT

X470

CFOS <MSI-BOM> — Y02-MU000170-CFO

Y02-MU00170-CFO

NAHIMIC <MSI-BOM> — Y02-MU000100-NAH

Y02-MU00100-NAH

SLI <MSI-BOM> — Y01-RNVIDIL-000

Y01-RNVIDIL-000

SSE1 <MSI-BOM>

WIFI

604-4442-020

XSPLIT <MSI-BOM> — X_Y02-MA00401-XSP

Y02-MA00401-XSP

SSE <MSI-BOM> — X_Y02-MA00101-SSE

Y02-MA00101-SSE

PCB

PCB

PCB1

7B78_10

PD0-07B4520-G37

PD0-07B4520-E48

MOS HEATSINK

IO COVER+MOSA

mos heatsink

PCH HEATSINK

PCH_HS1 — MEC1 — MEC2 — msi

X_HS-0408530-RH

PCH Heatsink

Audio COVER

COVER1 — Audio Cover

E21-7A62010-RH

DDR COVER

DDR_COVER1 — DDR COVER — X1 X2 X3 X4 X5

E21-7A63010-RH

0901 Modify DDR_COVER1 PIN X1.X2.X3.X4.X5 Connect to GND

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