

vinafix

MODEL NAME : ZAVA1/ZAVC1
PCB NO : DA80011D000 LA-B015P-R1.0

Compal Confidential

Schematic Document

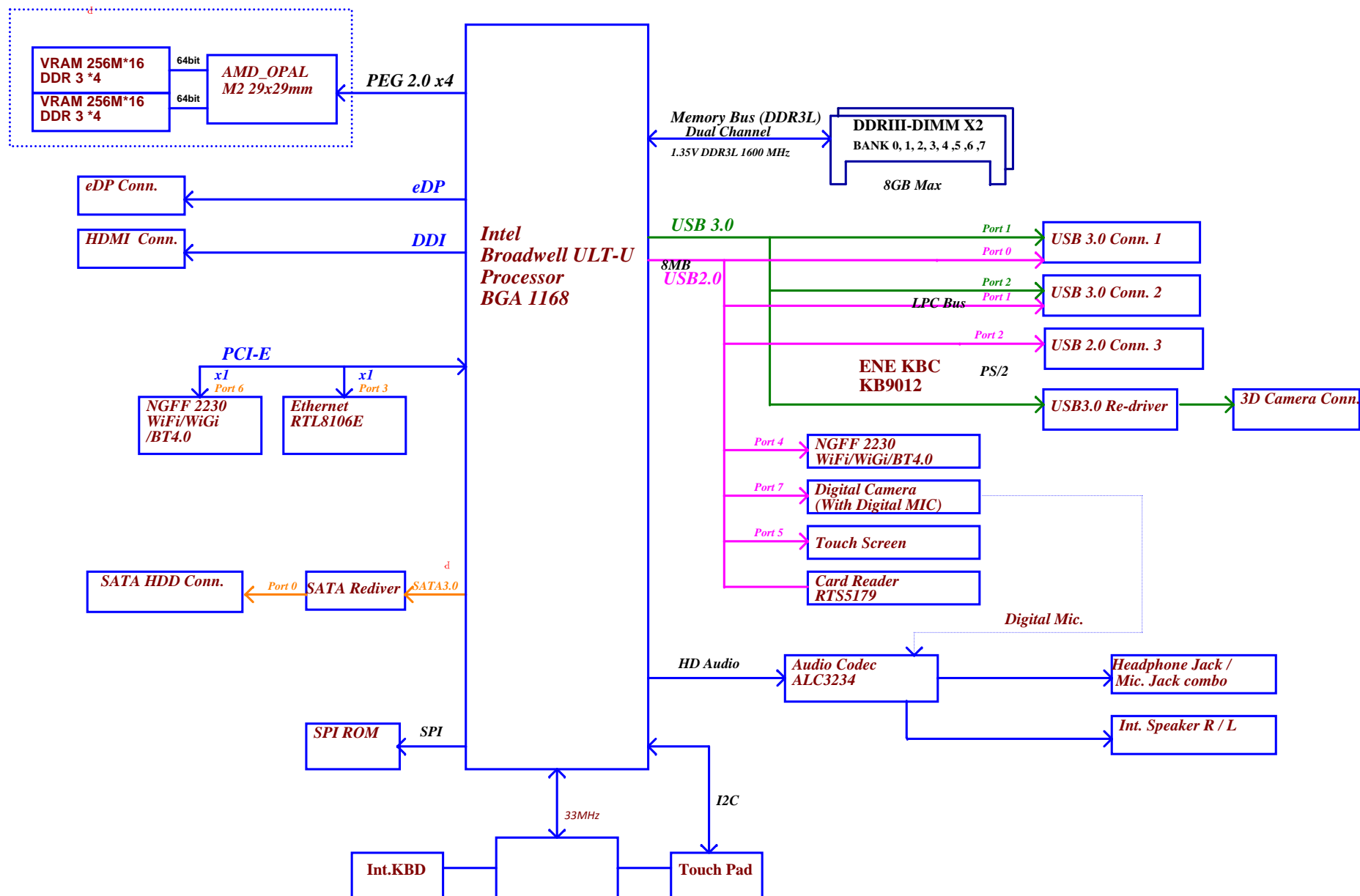
Intel BoardWell ULT
ZAVA1/ZAVC1
DIS AMD 25W/M2+DDR3x8

2014-10-17

Rev: 1.0

<http://vinafix.vn>

Security Classification	Compal Secret Data		Title	
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Board ID Table for AD channel

Vcc	3.3V +/- 1%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0.000V	0.000V	0.300V	0x00 - 0x0B
1	12K +/- 1%	0.347V	0.354V	0.360V	0x0C - 0x1C
2	15K +/- 1%	0.423V	0.430V	0.438V	0x1D - 0x26
3	20K +/- 1%	0.541V	0.550V	0.559V	0x27 - 0x30
4	27K +/- 1%	0.691V	0.702V	0.713V	0x31 - 0x3B
5	33K +/- 1%	0.807V	0.819V	0.831V	0x3C - 0x46
6	43K +/- 1%	0.978V	0.992V	1.006V	0x47 - 0x54
7	56K +/- 1%	1.169V	1.185V	1.200V	0x55 - 0x64
8	75K +/- 1%	1.398V	1.414V	1.430V	0x65 - 0x76
9	100K +/- 1%	1.634V	1.650V	1.667V	0x77 - 0x87
10	130K +/- 1%	1.849V	1.865V	1.881V	0x88 - 0x96
11	160K +/- 1%	2.015V	2.031V	2.046V	0x97 - 0xA3
12	200K +/- 1%	2.185V	2.200V	2.215V	0xA4 - 0xAD
13	240K +/- 1%	2.316V	2.329V	2.343V	0xAE - 0xB7
14	270K +/- 1%	2.395V	2.408V	2.421V	0xB8 - 0xC0
15	330K +/- 1%	2.521V	2.533V	2.544V	0xC1 - 0xC9
16	430K +/- 1%	2.667V	2.677V	2.687V	0xCA - 0xD3
17	560K +/- 1%	2.791V	2.800V	2.808V	0xD4 - 0xDC
18	750K +/- 1%	2.905V	2.912V	2.919V	0xDD - 0xE6
19	NC	3.000V	3.300V	3.300V	0xE7 - 0xFF

SMBUS Control Table

	SOURCE	BATT	Charger	VGA	DIMM	XDP	Thermal Sensor	FFS
EC_SMB_CK1 EC_SMB_DA1	KB9012	V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012			V			V	
SMBCLK SMBDATA	ULT				V			V
SML0CLK SML0DATA	ULT							
SML1CLK SML1DATA	ULT							

HSW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)	DIS(OPAL)
0				
1				
2				
3				
4				
5				
6				
7				
8				
9				
10				
11				
12				
13				
14				
15				

BDW BOARD ID Table

Board ID	UMA	DIS(JET)	DIS(Topaz)	DIS(OPAL)
0	1.0_3D CAM			
1		1.0_3D CAM		
2			1.0_3D CAM	
3	SSI(BDW)			
4		SSI(BDW)		
5			SSI(BDW)	
6	PT(BDW) SSI_3D CAM			
7		PT(BDW) SSI_3D CAM		
8			PT(BDW) SSI_3D CAM	
9	ST(BDW) PT_3D CAM			
10		ST(BDW) PT_3D CAM		
11			ST(BDW) PT_3D CAM	
12	1.0(BDW) ST_3D CAM			
13		1.0(BDW) ST_3D CAM		
14			1.0(BDW) ST_3D CAM	
15				SSI
16				PT
17				ST
18				1.0

CLOCK SIGNAL (Diff. 100MHz)

CLKOUT_PCIE0	
CLKOUT_PCIE1	
CLKOUT_PCIE2	10/100 LAN
CLKOUT_PCIE3	MINI Card (WLAN)
CLKOUT_PCIE4	dGPU
CLKOUT_PCIE5	

ULT

USB3.0

Port1	USB connector 1
Port2	USB connector 2
Port3	
Port4	3D Camera

USB2.0

Port0	USB connector 1
Port1	USB connector 2
Port2	USB connector 3 (D/B)
Port3	
Port4	MINI Card (WLAN)
Port5	Touch Screen Panel
Port6	Card Reader
Port7	Camera

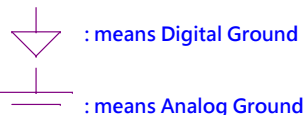
PCI EXPRESS

Lane 1	
Lane 2	
Lane 3	10/100 LAN
Lane 4	MINI Card (WLAN)
Lane 5	PEG (AMD JET/TOBAZ)
Lane 6	

SATA

SATA0	HDD
SATA1	
SATA2	
SATA3	

Symbol Note :



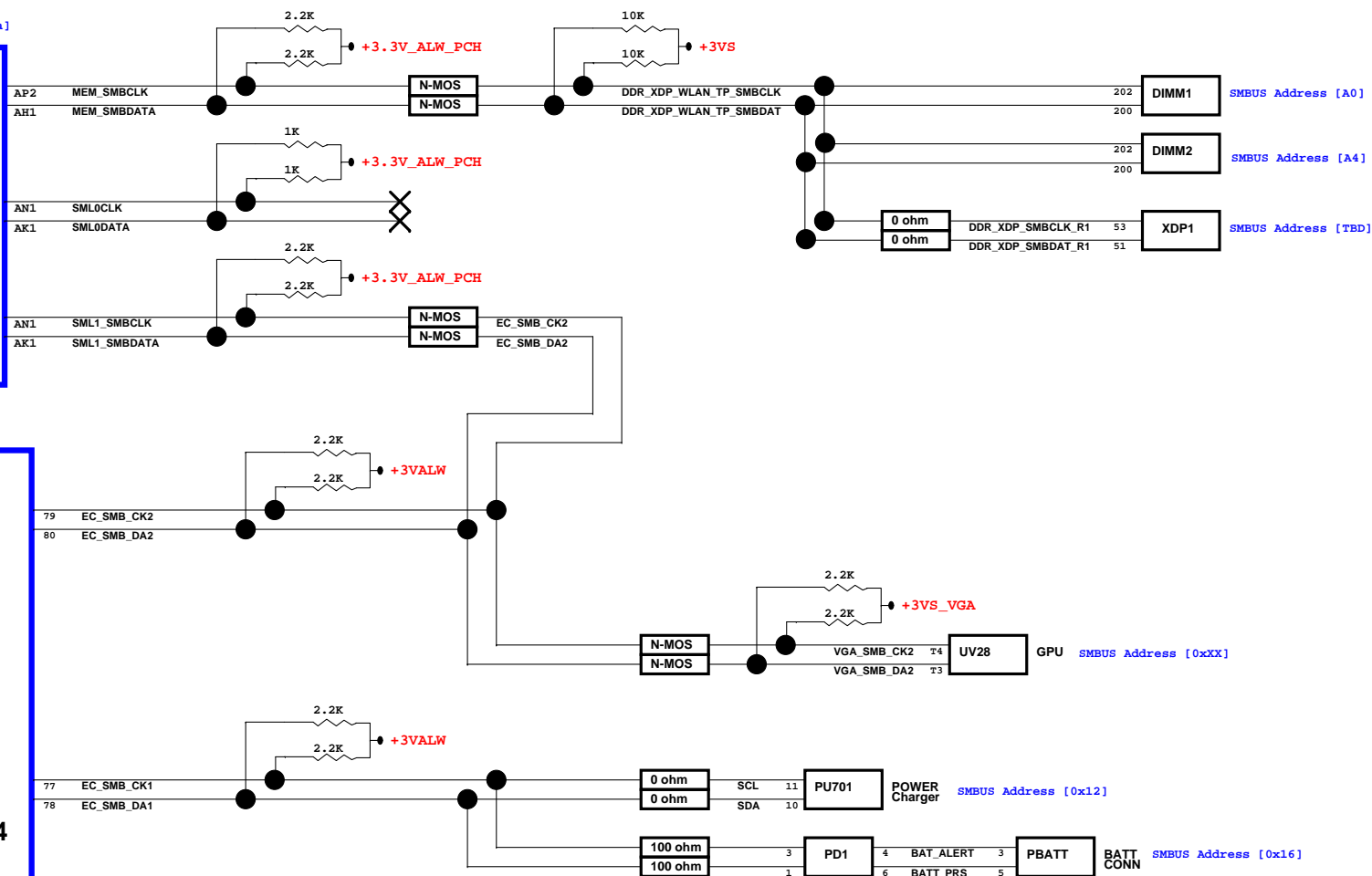
Link

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SMBUS Address [0x9a]

MCH
Shark bay

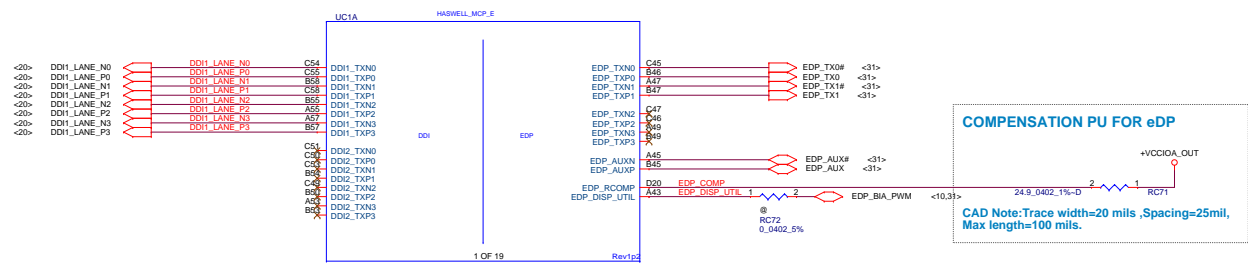
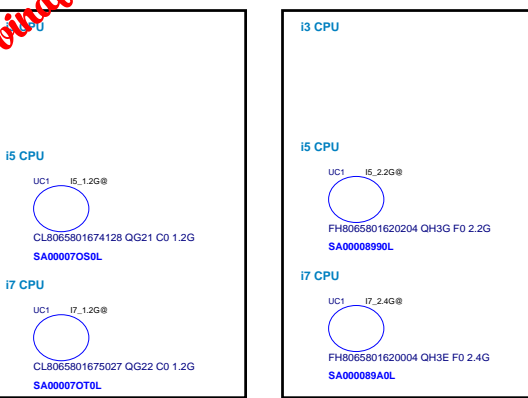
KBC
KB9012A4



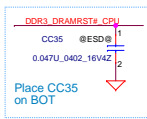
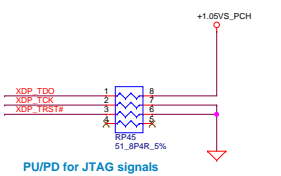
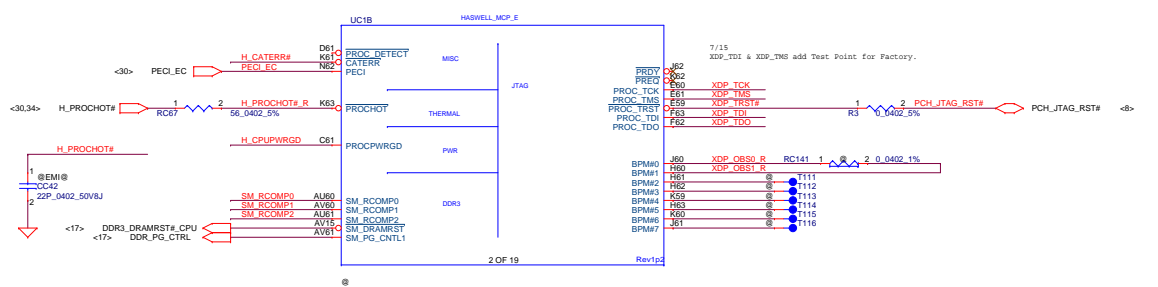
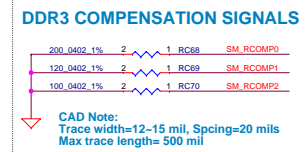
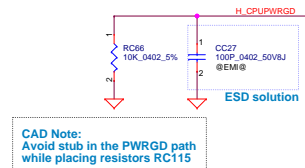
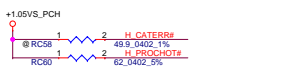
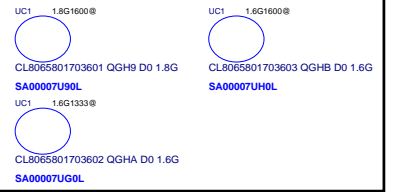
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BDW e-QS for DVT2 BDW_QS for DVT2



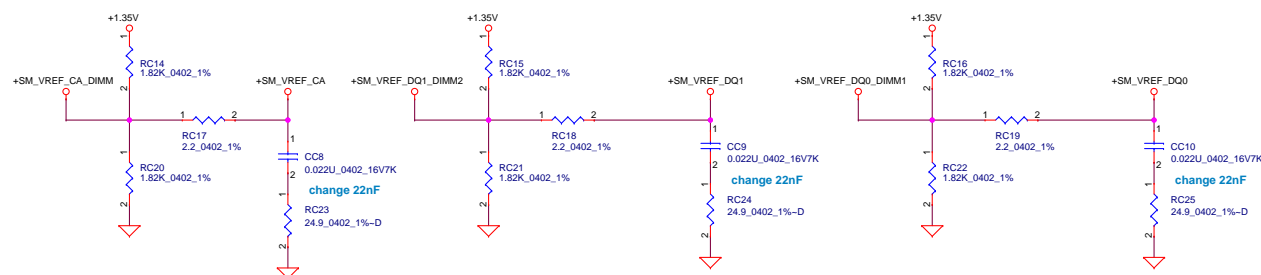
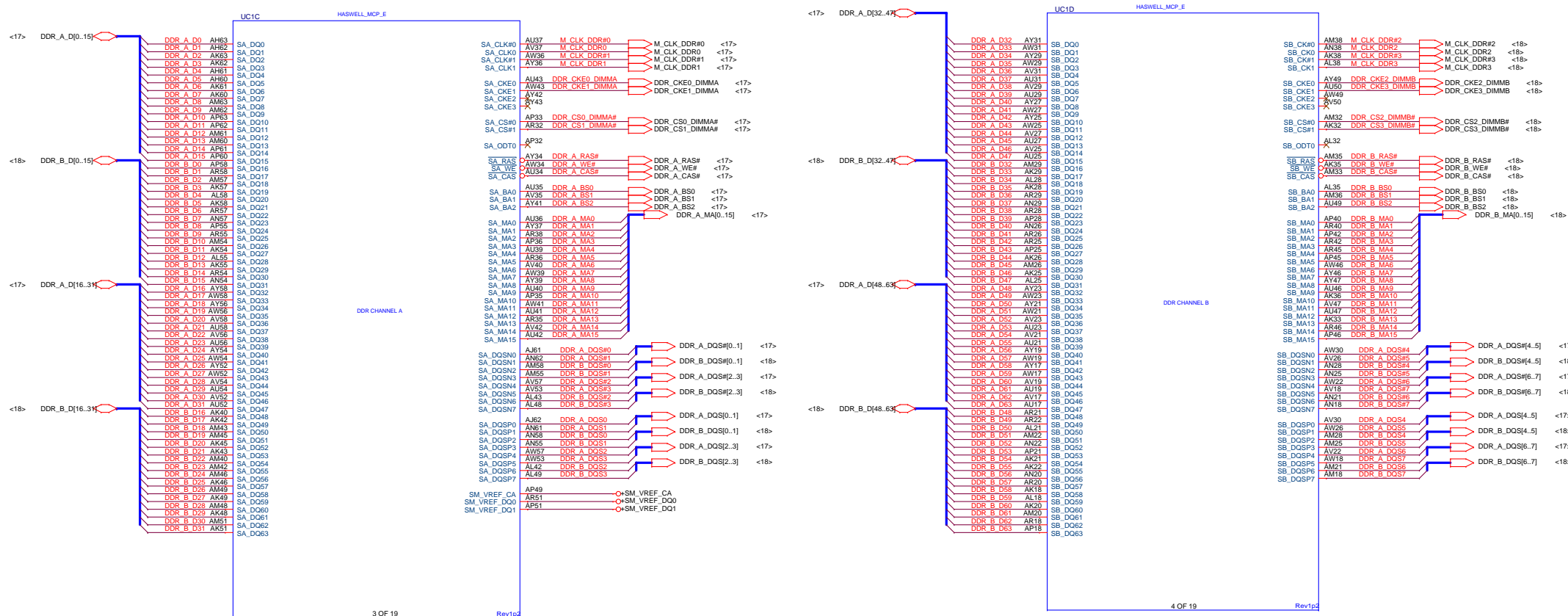
BDW (ES2) CPU for 3D / 4G



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Interleaved Memory



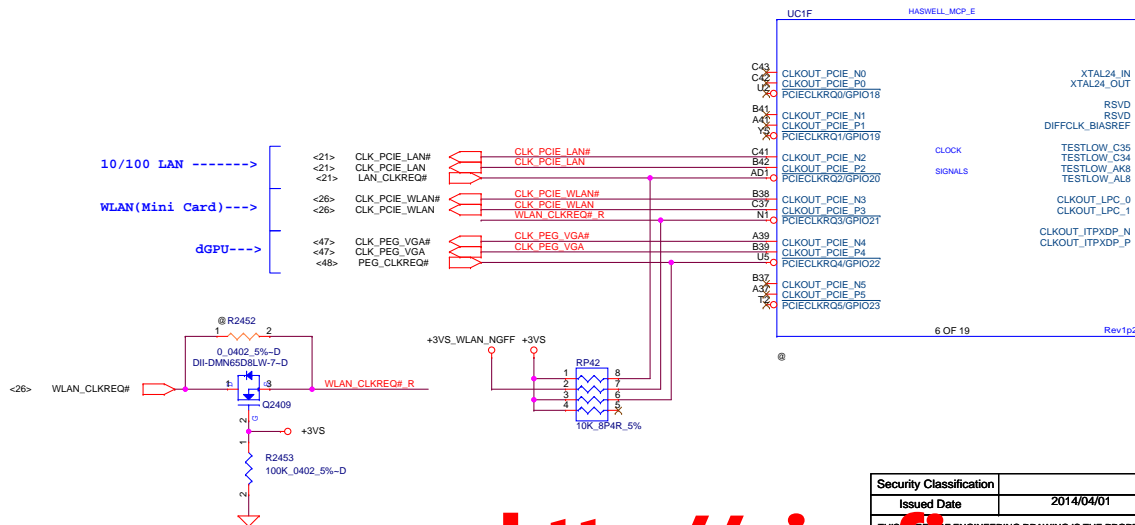
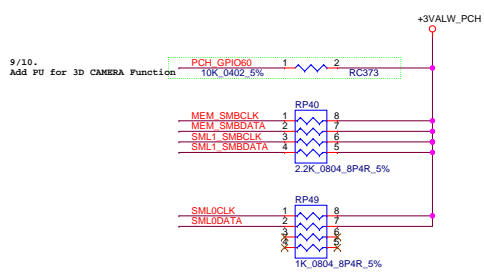
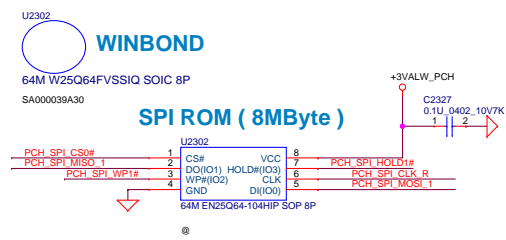
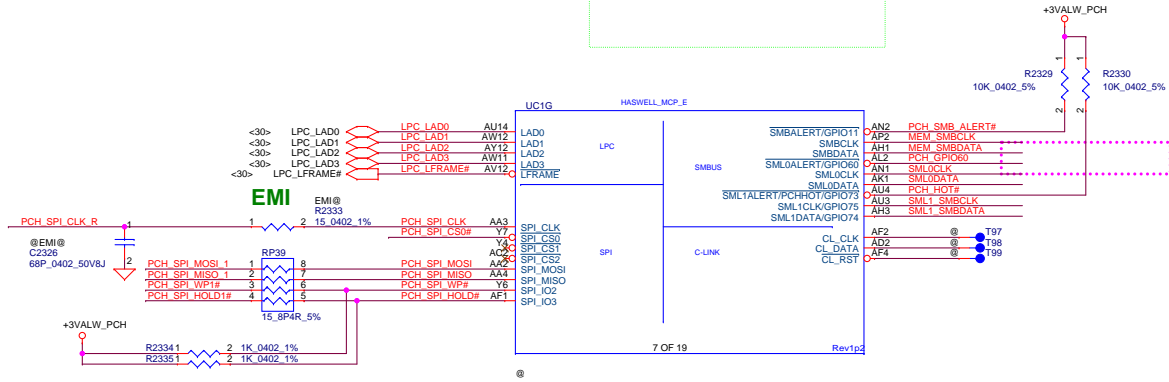
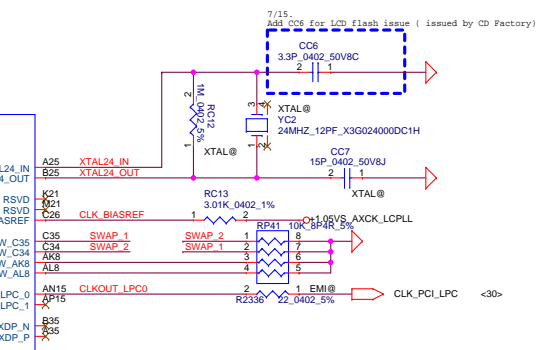
confirm by intel request PDG P141

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				MCP(3,4/19) DDR3	
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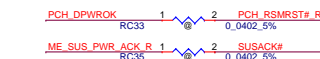
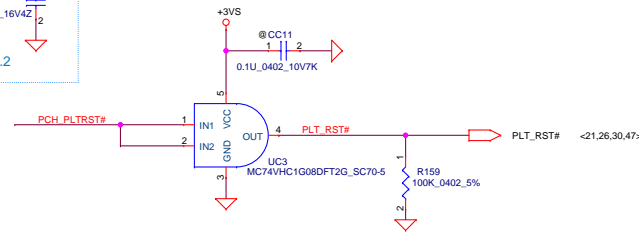
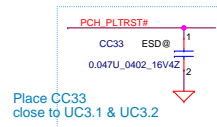
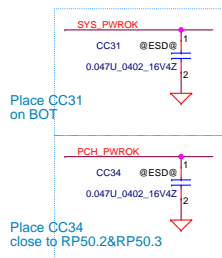
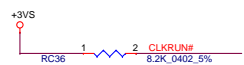
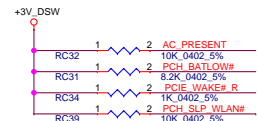
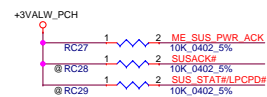
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Pin 1: SML1_SMBCLK (Signal)
Pin 6: +3VALW_PCH (Power)
Pin 4: SML1_SMBDATA (Signal)
Pin 3: QH1A (Signal)

<19> XTAL24_IN XTAL24_IN



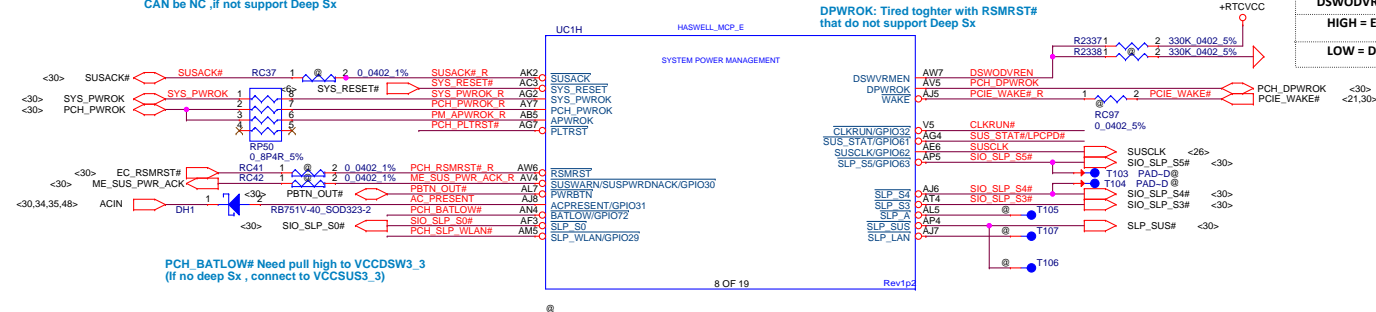
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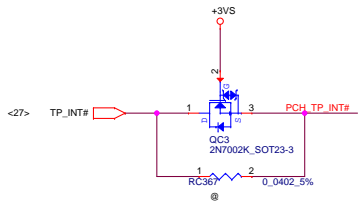
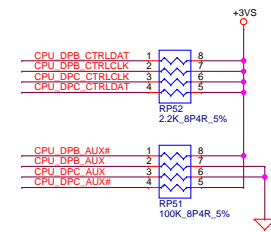
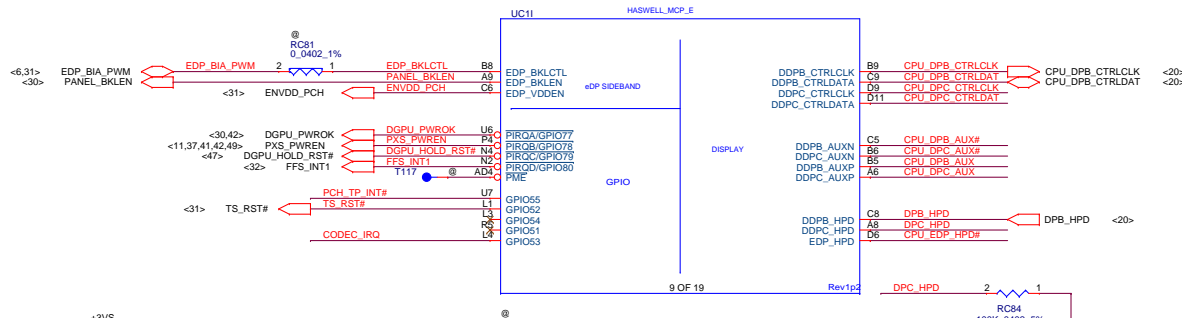
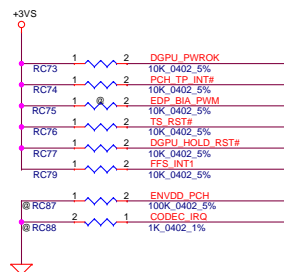
Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit
CAN be NC, if not support Deep Sx

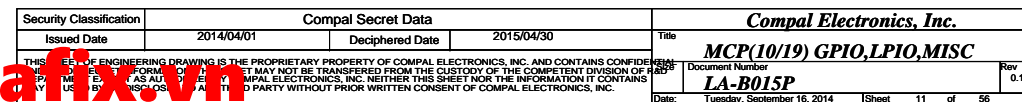
DSWODVREN - On Die DSW VR Enable
*Enable(DEFAULT)
Disable

DSWODVREN - ON DIE DSW VR ENABLE
HIGH = ENABLED (DEFAULT)
LOW = DISABLED

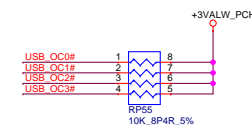
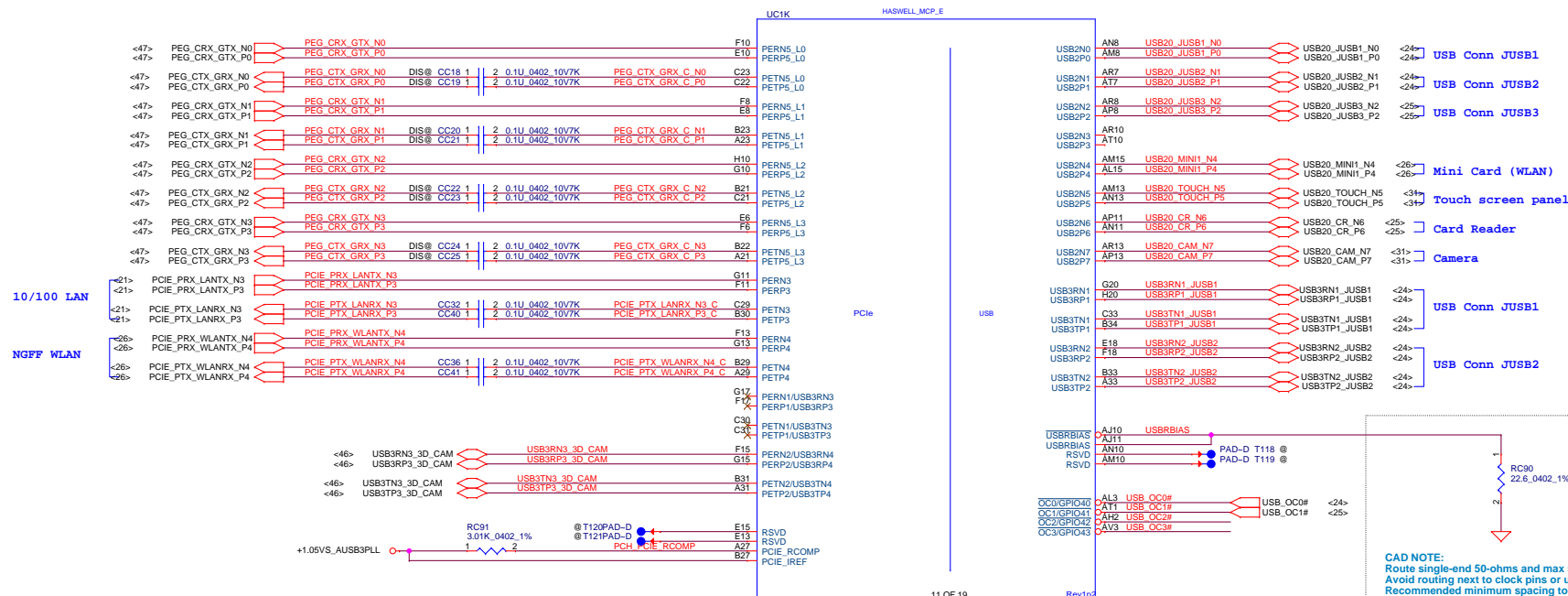


PCH_BATLOW# Need pull high to VCCDSW3_3
(If no deep Sx, connect to VCCSUS3_3)



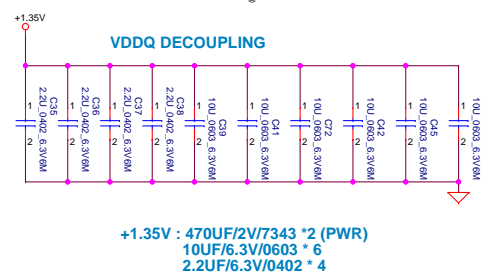
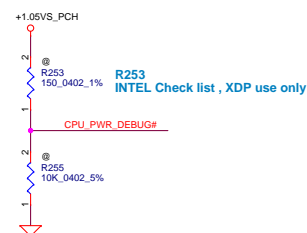
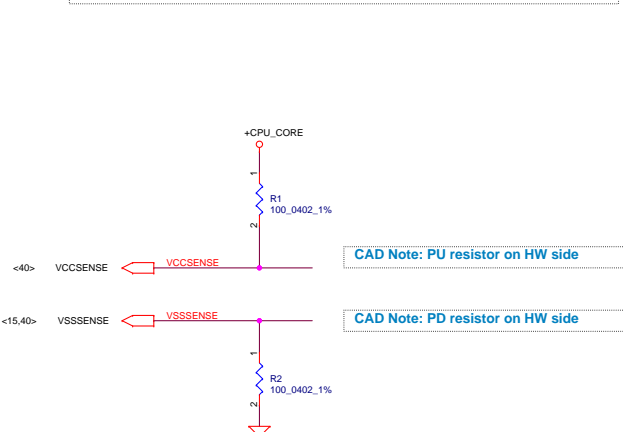
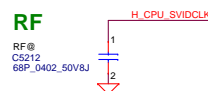
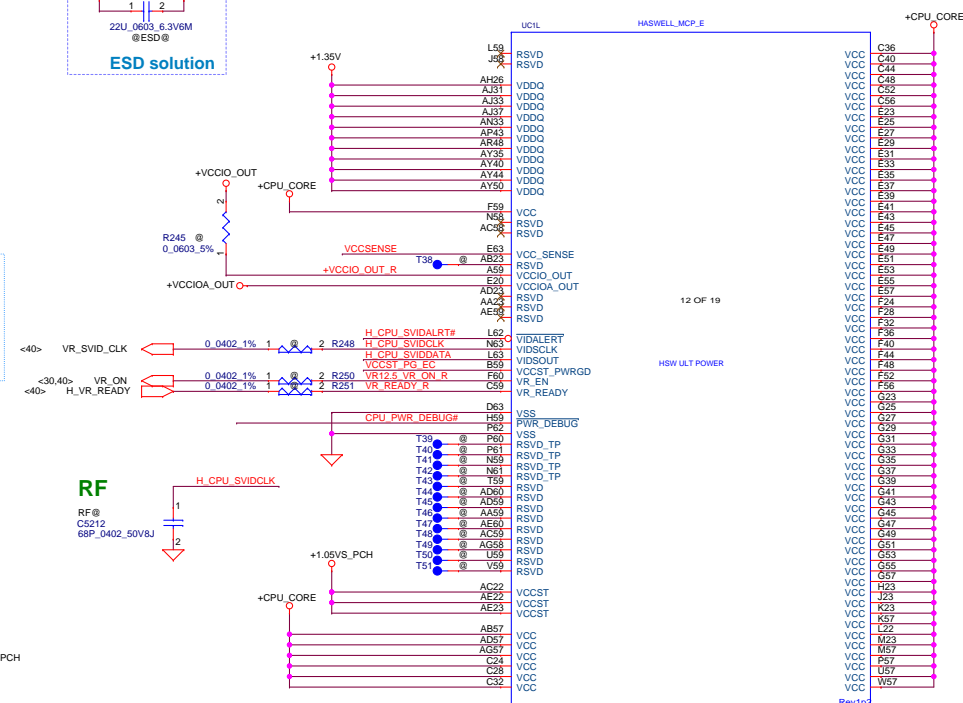
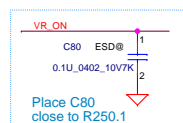
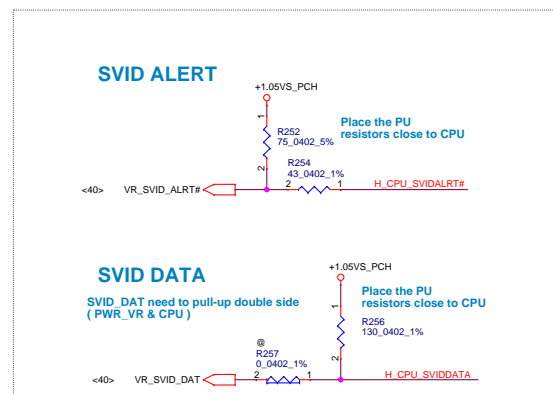
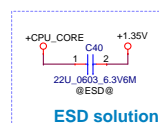
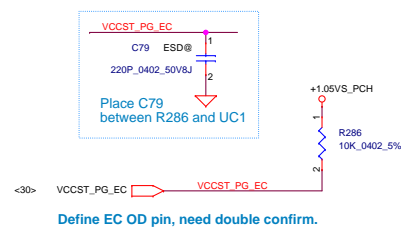


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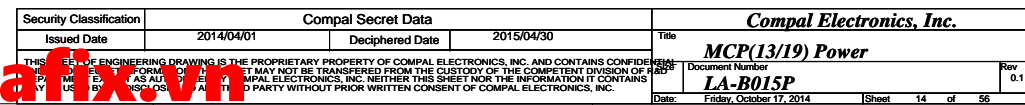
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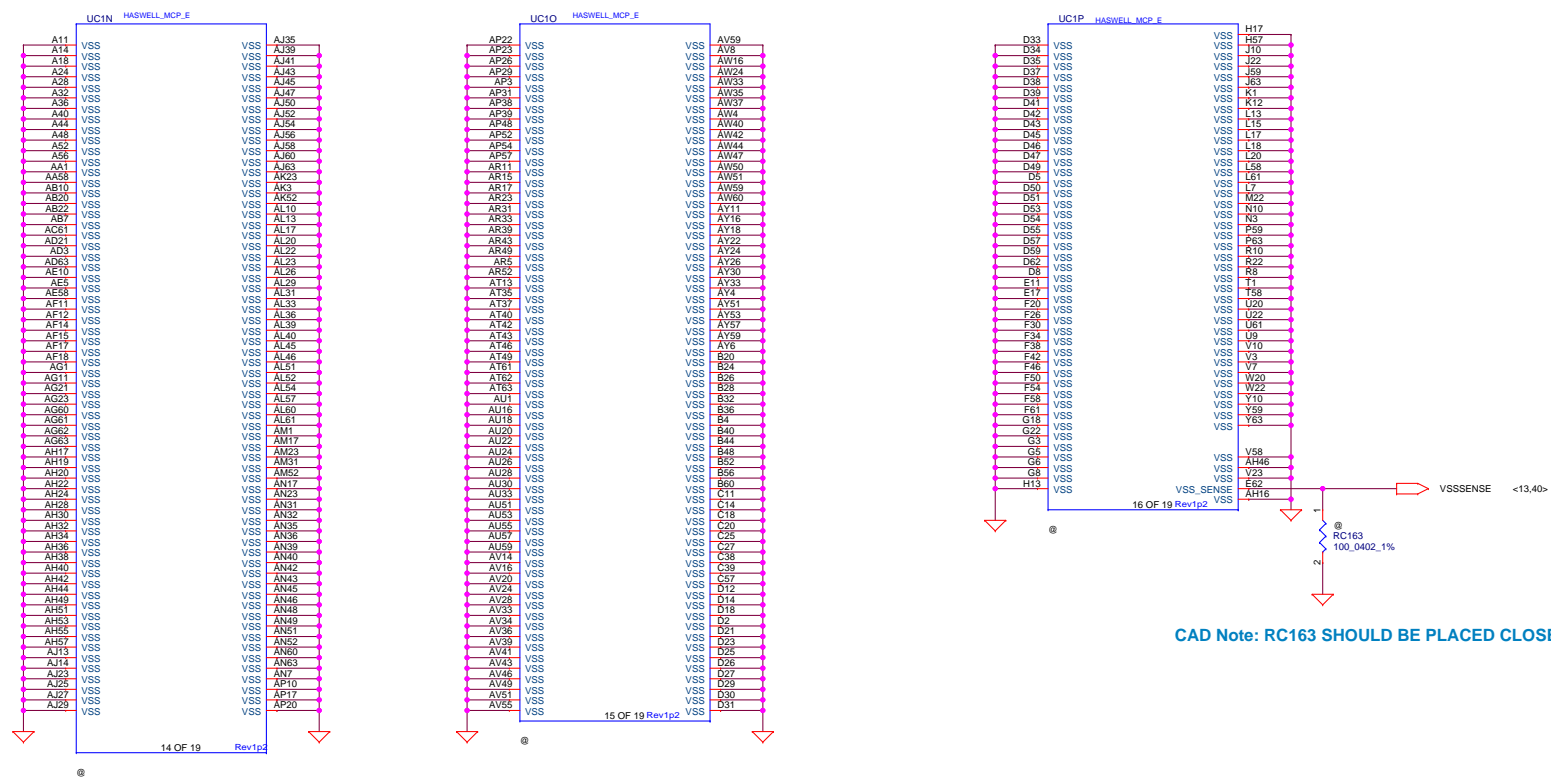
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				2015/04/30	
Title				MCP(12/19) Power	
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Populate RD1, De-Populate RD7 for Intel DDR3
VREFDQ multiple methods M1
Populate RD7, De-Populate RD1 for Intel DDR3
VREFDQ multiple methods M3

<7> DDR_A_DQS#[0..7]

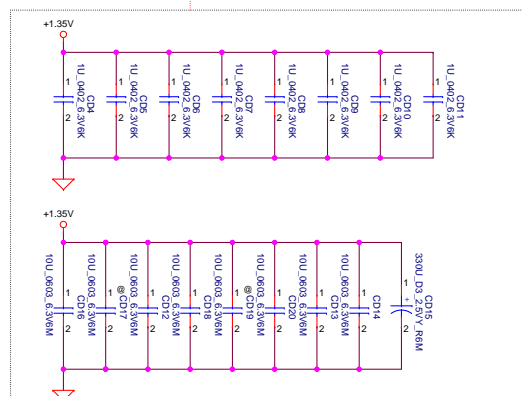
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<7> DDR_A_DQS[0..7]

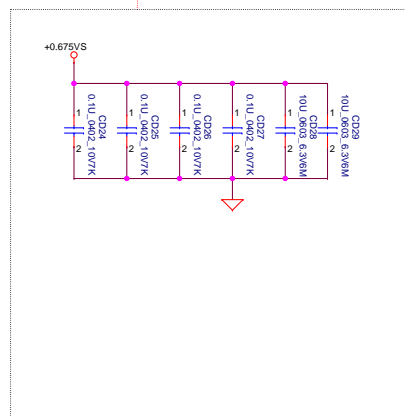
<7> DDR_A_MA[0..15]

Layout Note:
Place near JDIMM1

Note:
Check voltage tolerance of
VREF_DQ at the DIMM socket

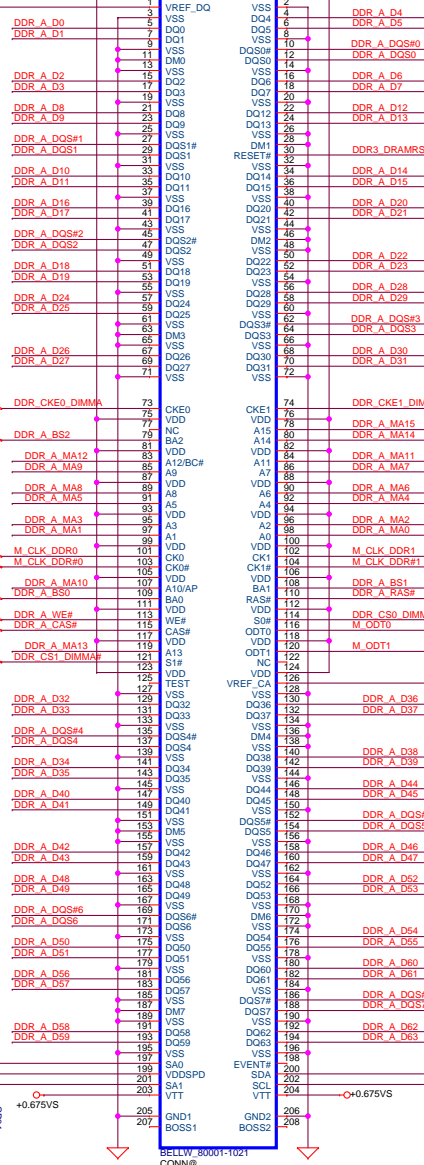


Layout Note:
Place near JDIMM1.203,204

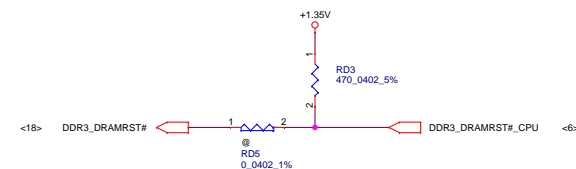


ESD solution

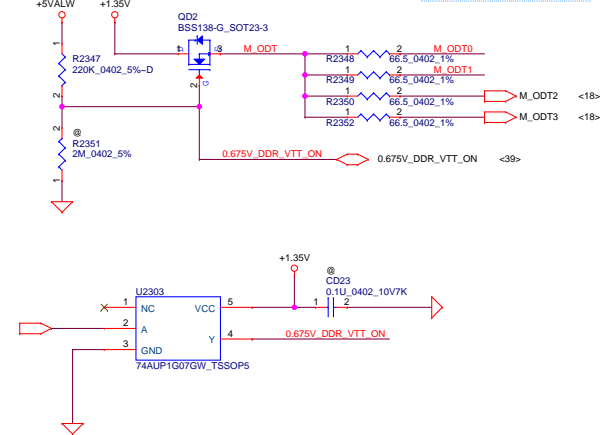
2-3A to 1 DIMMs/channel



CAD NOTE
PLACE THE CAP NEAR TO
DIMM RESET PIN

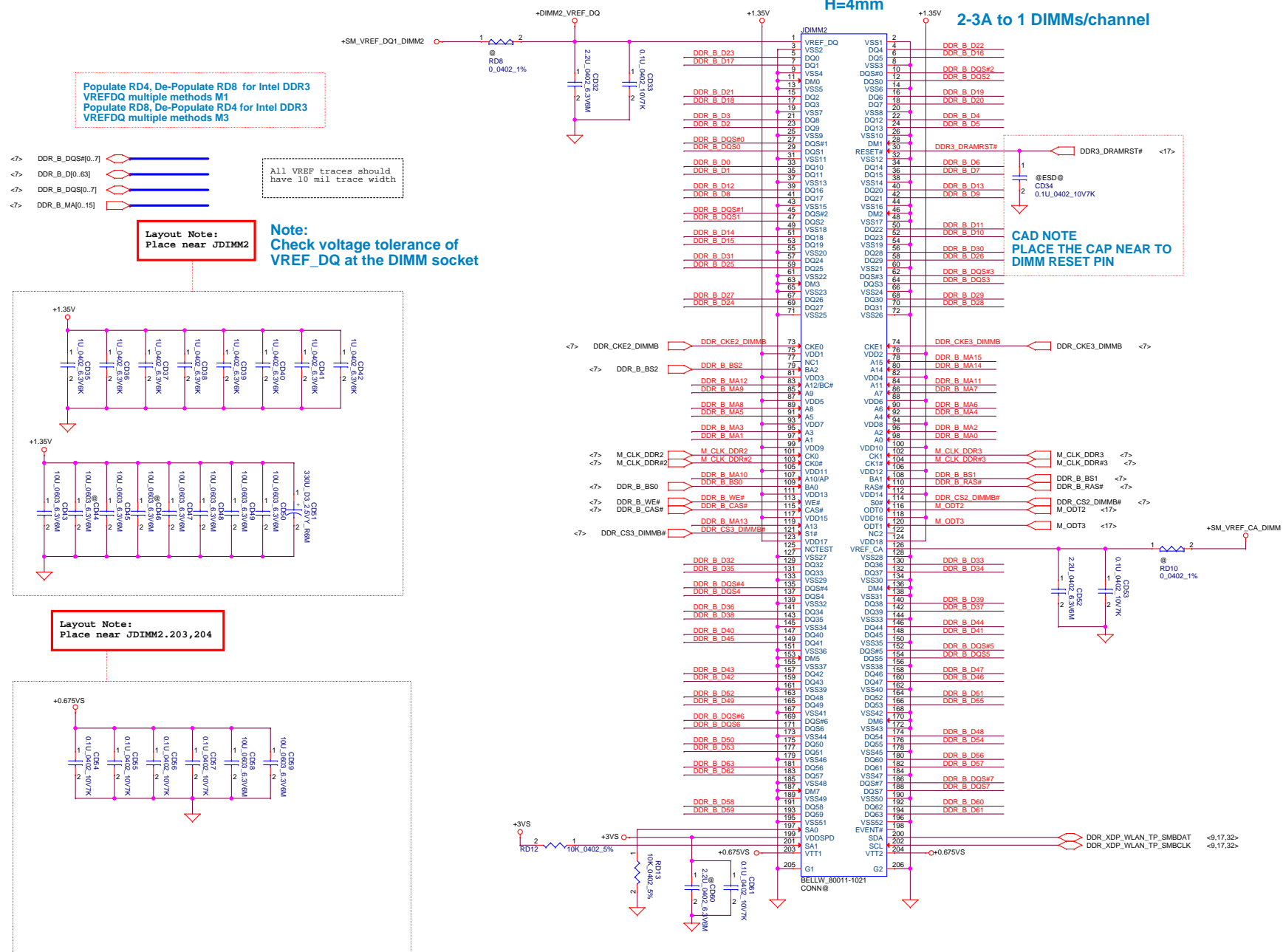


Place CC31 between QD2 and R23



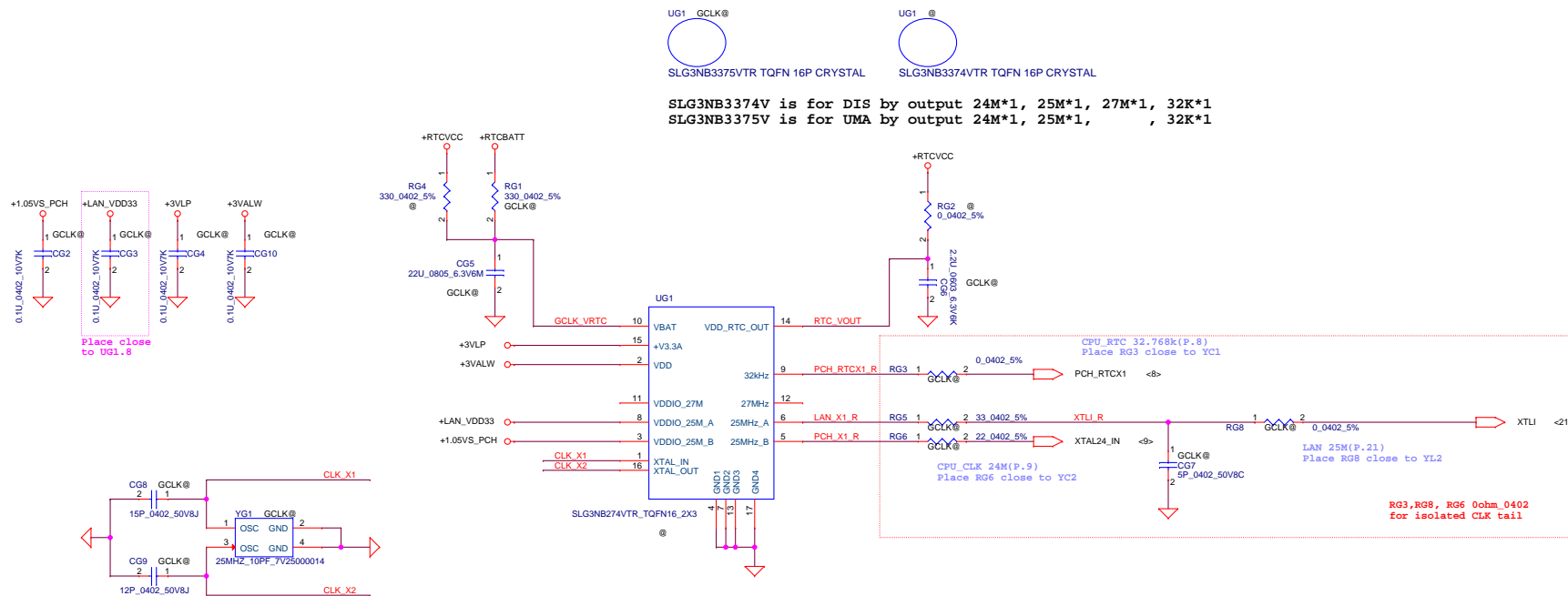
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2-3A to 1 DIMMs/channel



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				2015/04/30	
Title		DDRIII DIMMB			
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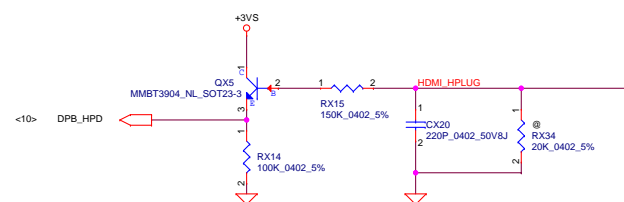
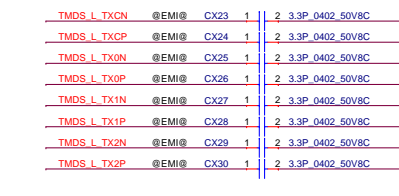
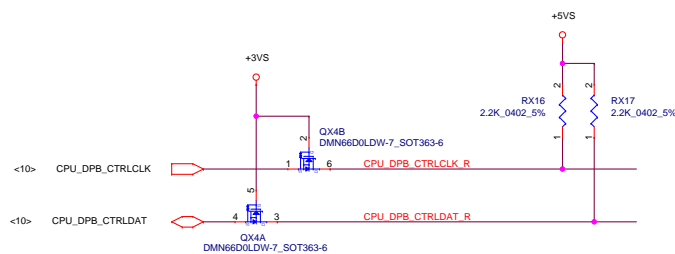
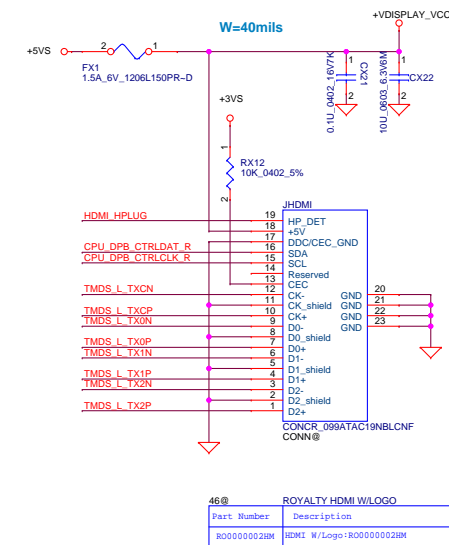
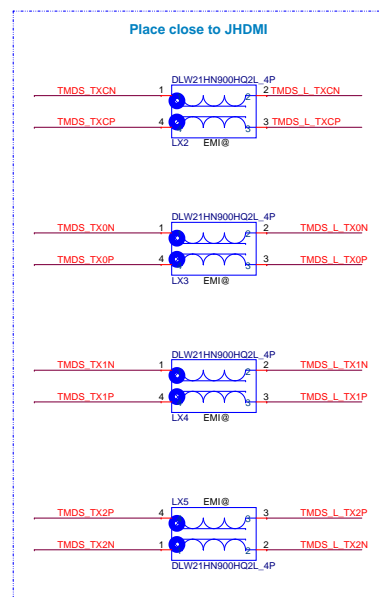
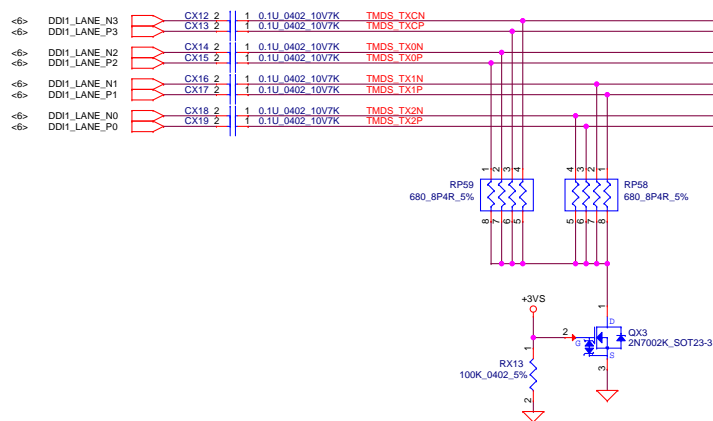
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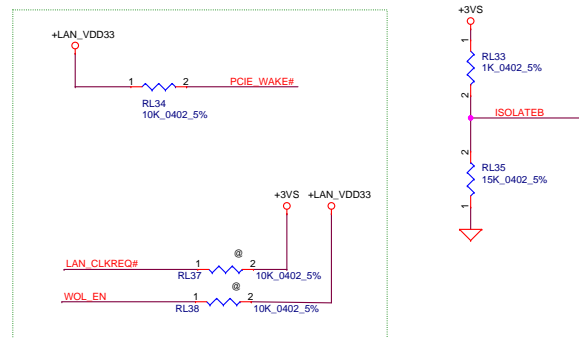
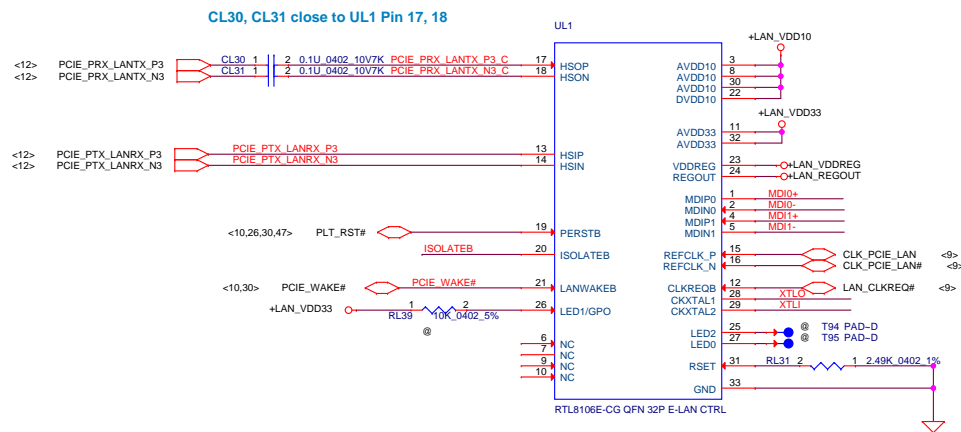
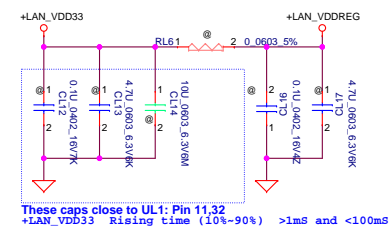
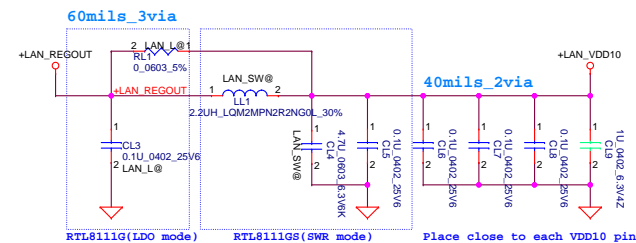
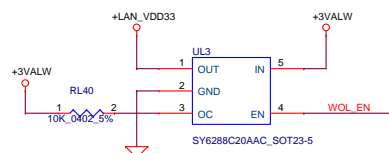
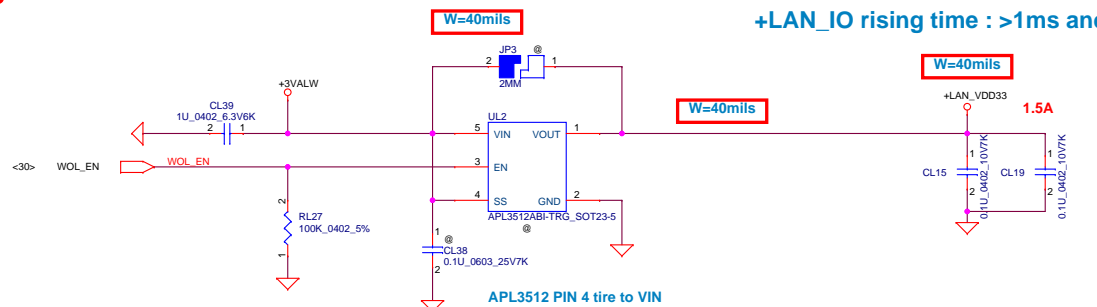
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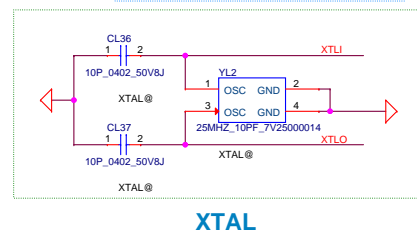
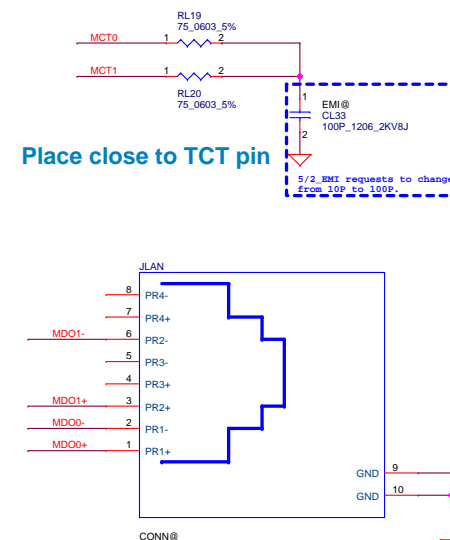
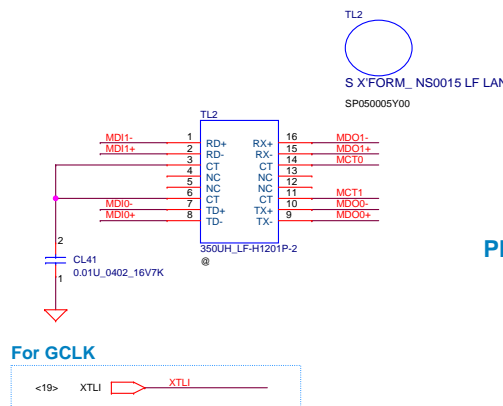


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Reserve 10K pull LAN_IO



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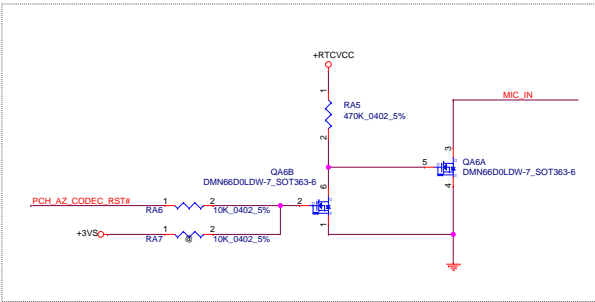
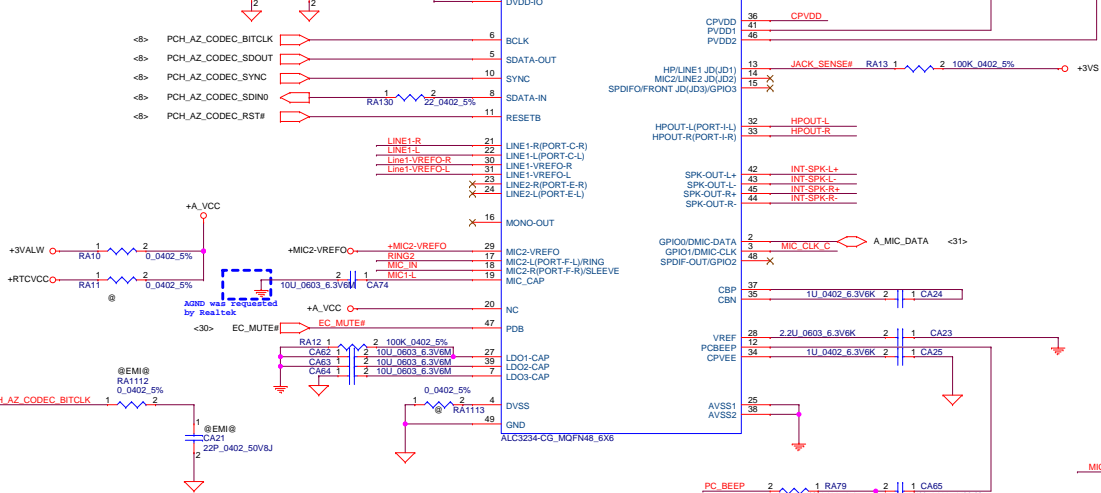
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CA71, CA51 place close to Pin 26

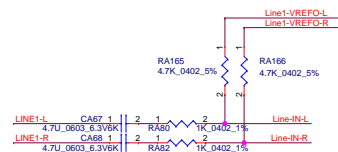
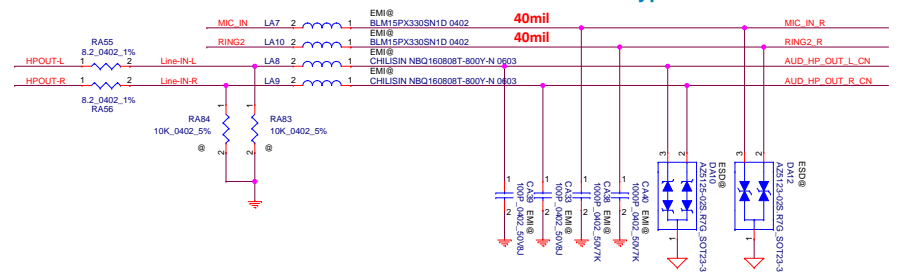
CA53, CA55 change Value from 100U_0603_6.3V6M to 4.7U_0603_6.3V6K

CA57, CA58 close to UA1 pin1

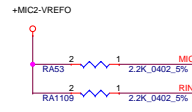
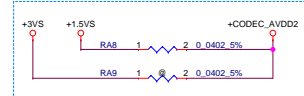
CA59 CA60 close to UA1 pin9



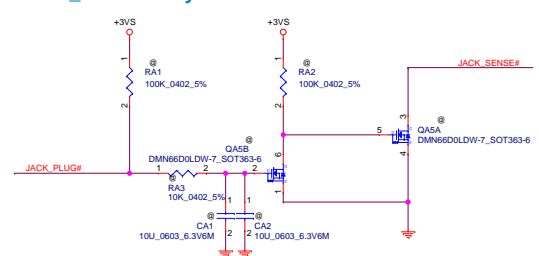
iPhone and Nokia type Combo Jack



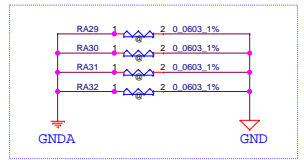
Reserve for HDA issue



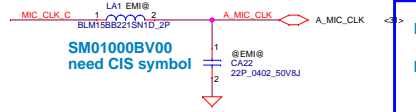
JACK_PLUG Delay circuitis



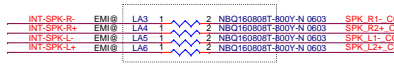
Reserve for cancel Delay circuitis



Place on the moat between GND & GNDA.

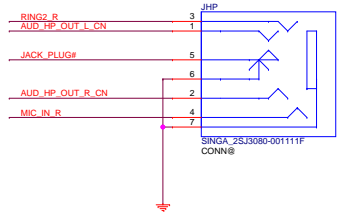
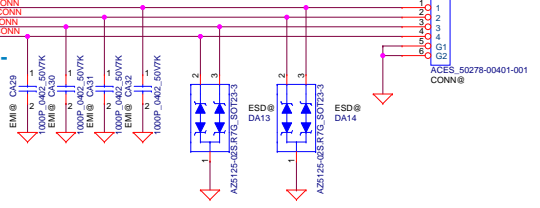


Close to UA1 Pin11,13,14,16



Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
Speaker 4 ohm : 40mil
Speaker 8 ohm : 20mil

close to Codec



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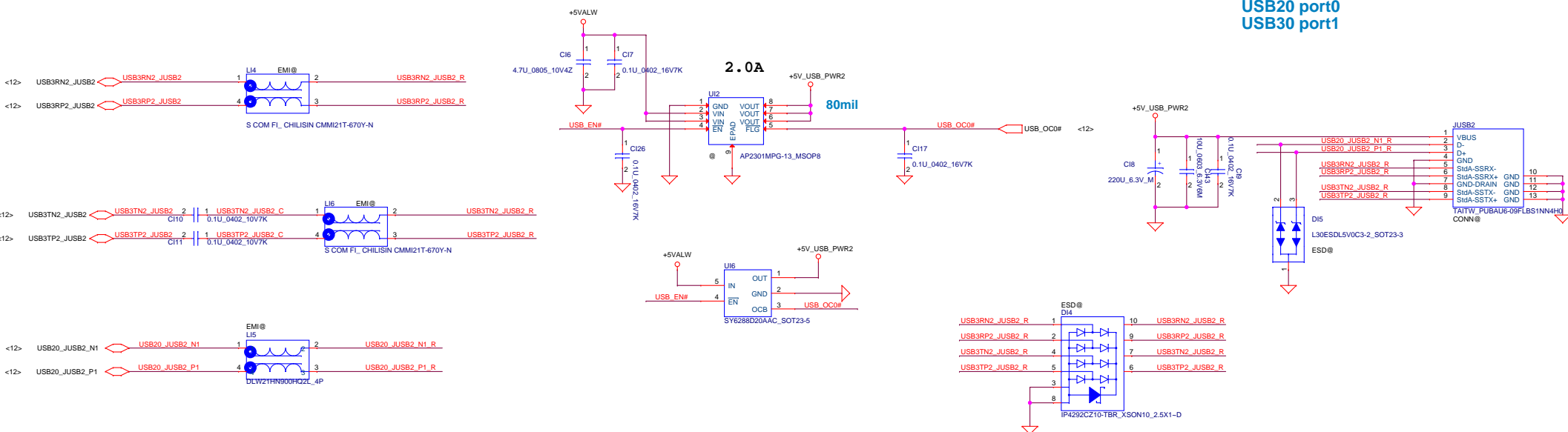


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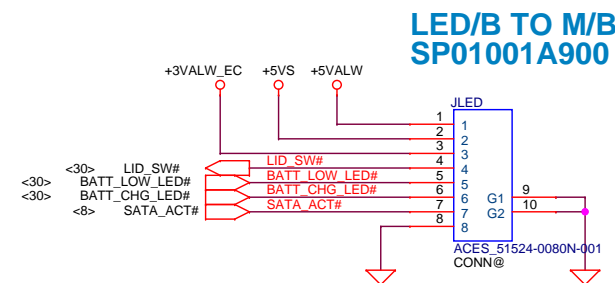
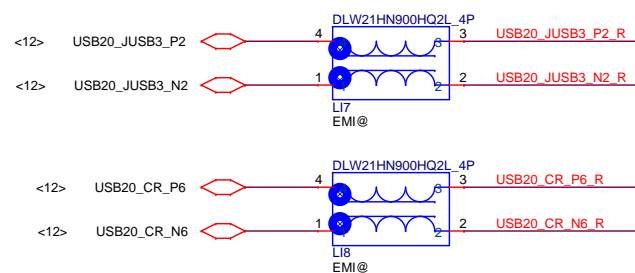
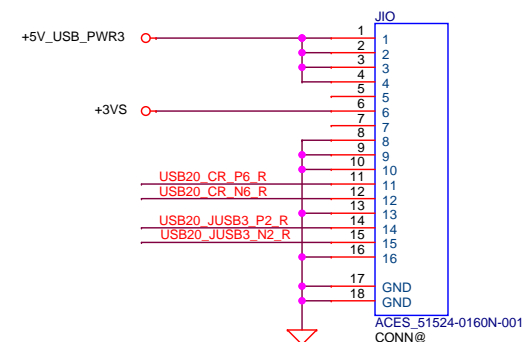
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2014/04/01		2015/04/30		Reserved Page			
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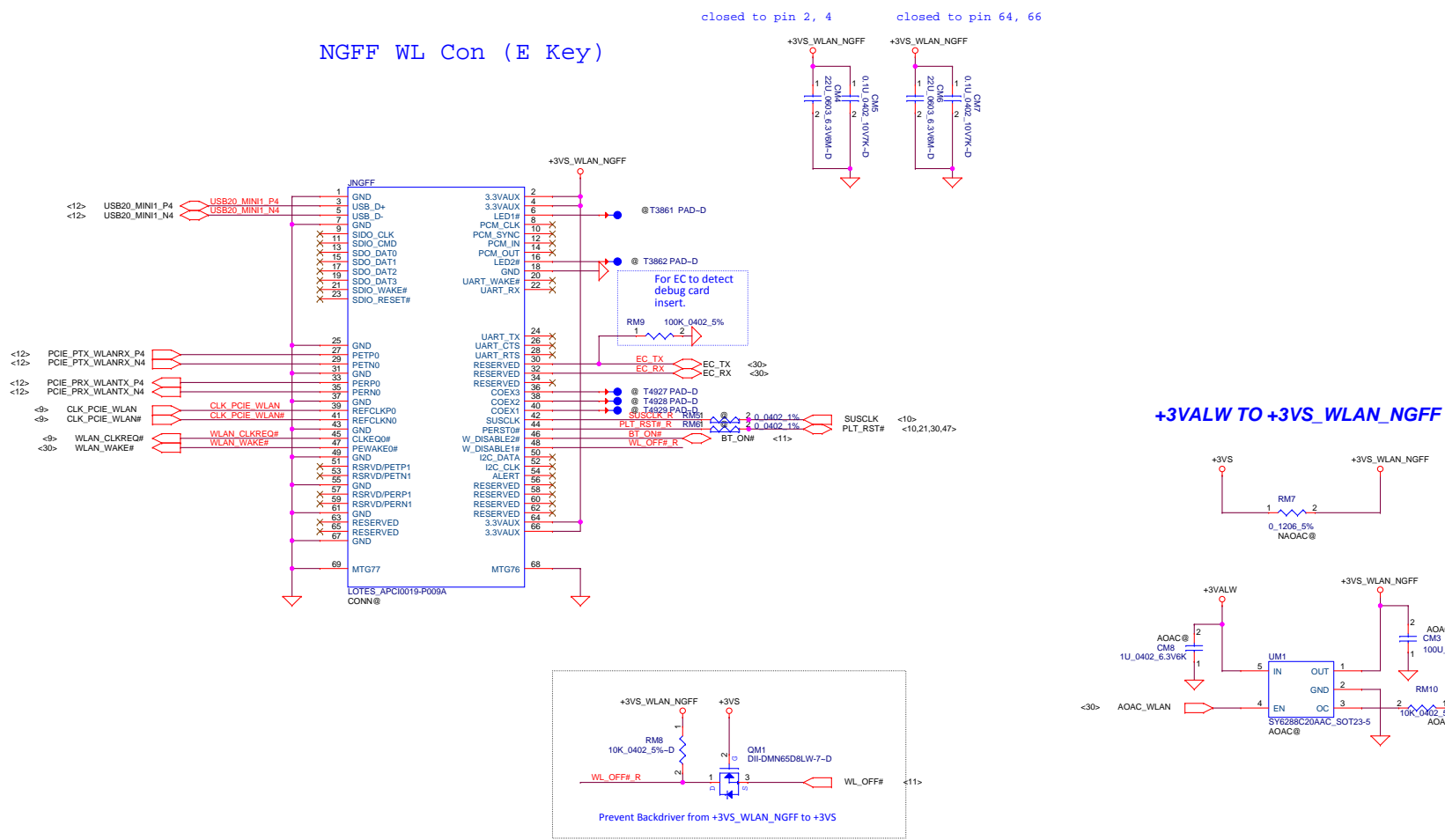
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IO to MB CONN
Substitute:SP01001FS00



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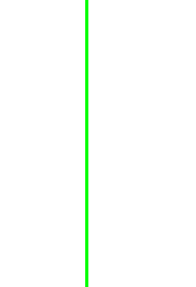
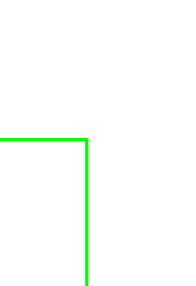
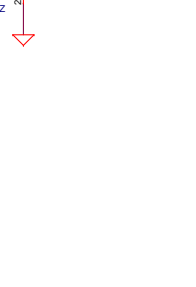
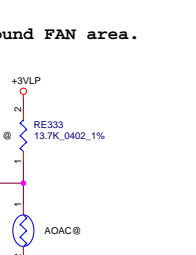
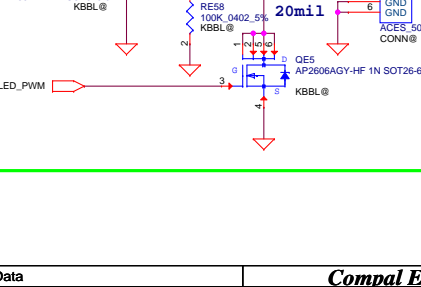
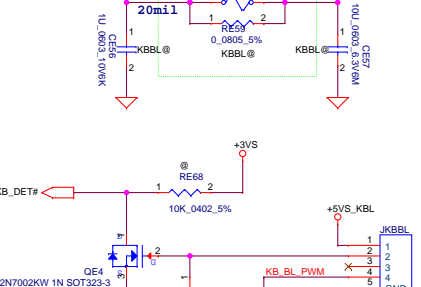
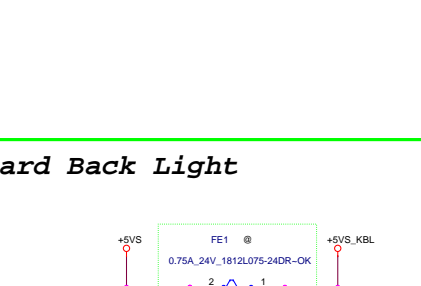
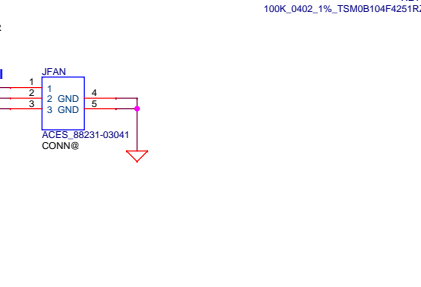
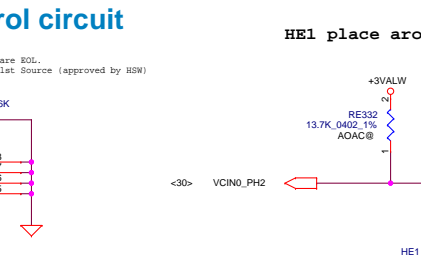
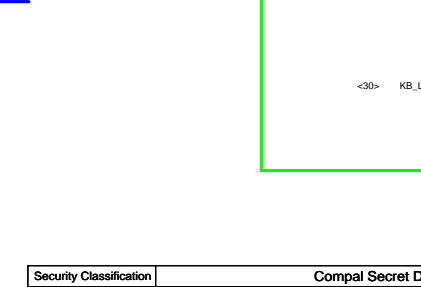
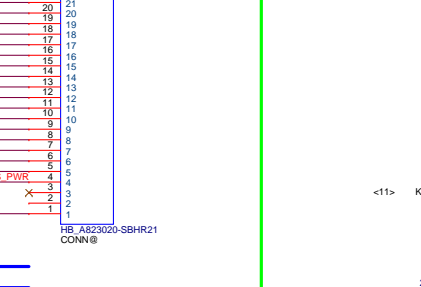
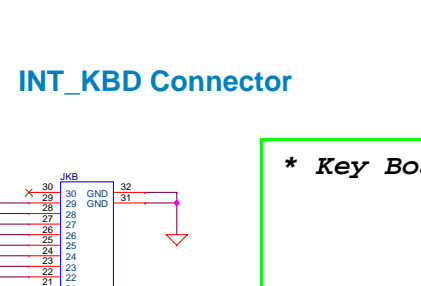
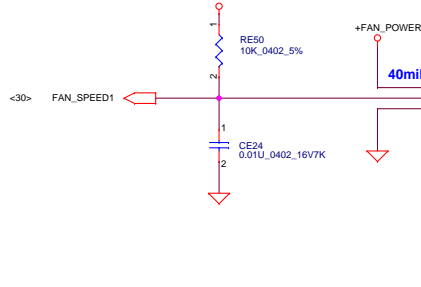
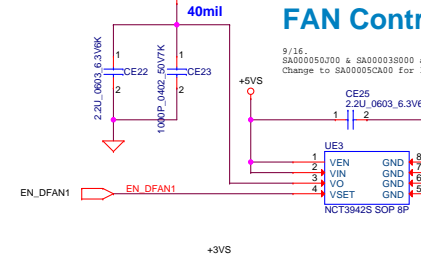
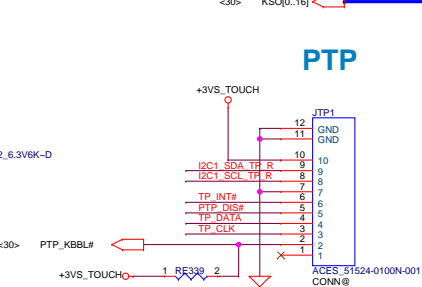
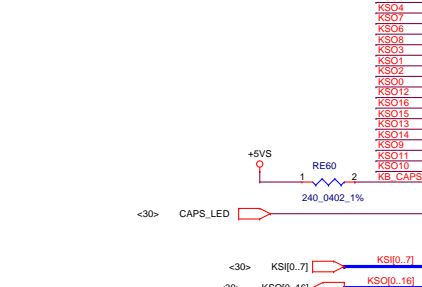
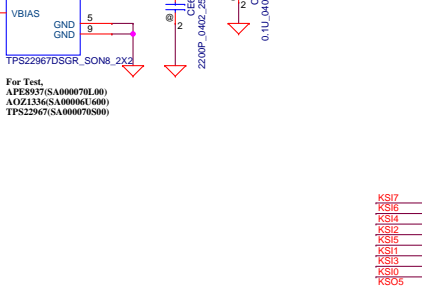
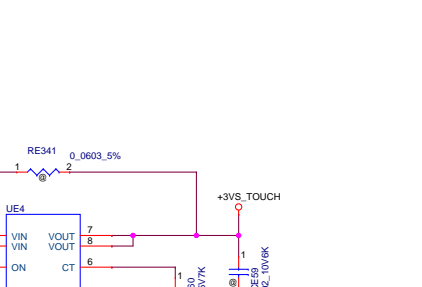
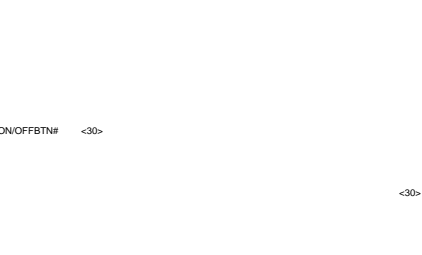
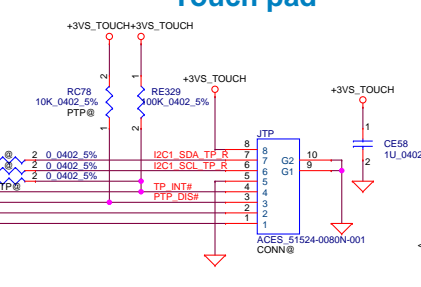
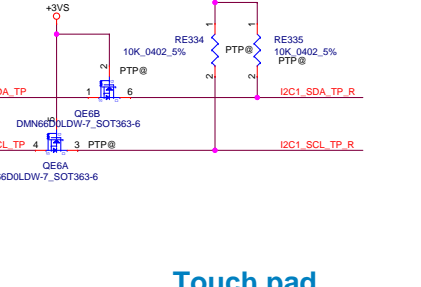
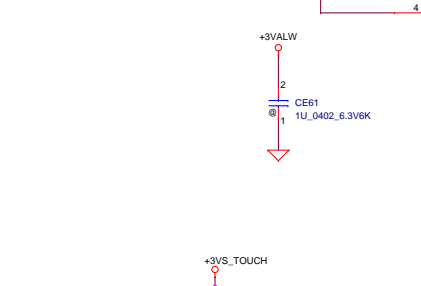
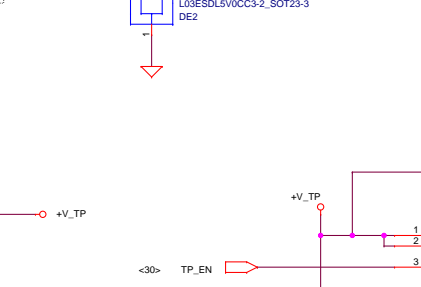
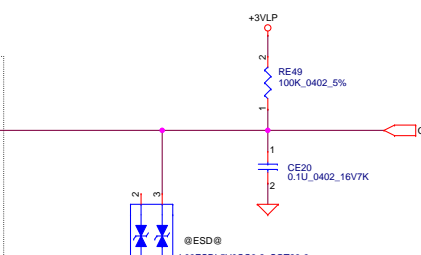
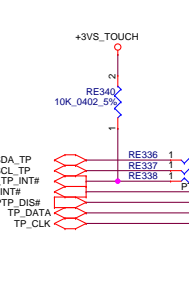
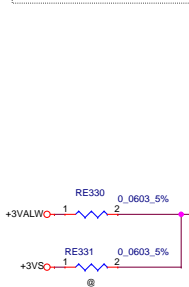
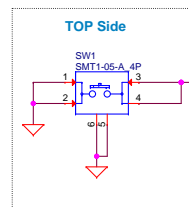
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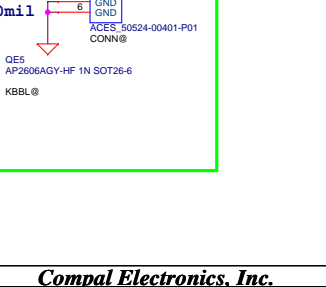
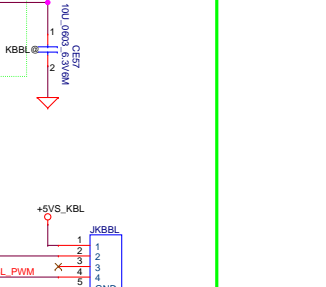
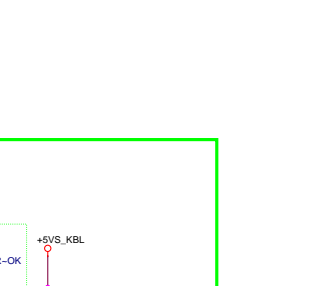
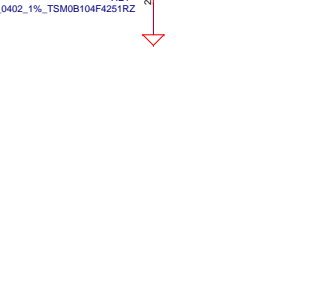
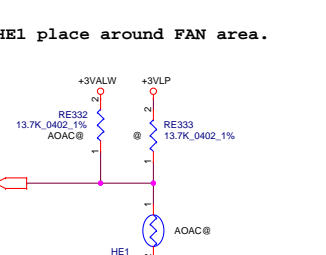
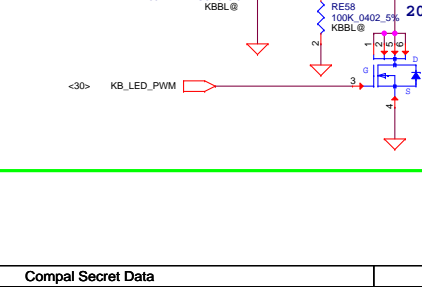
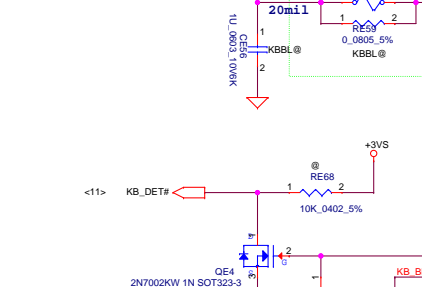
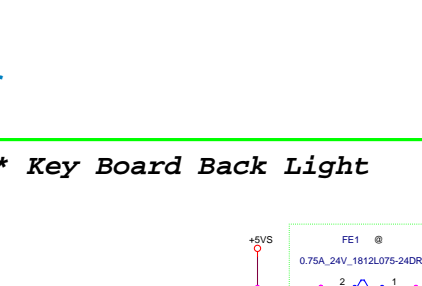
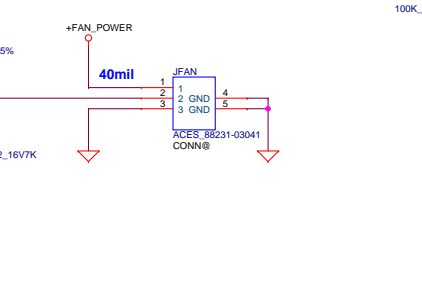
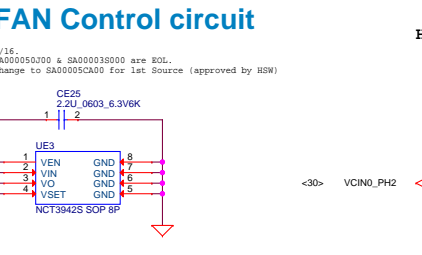
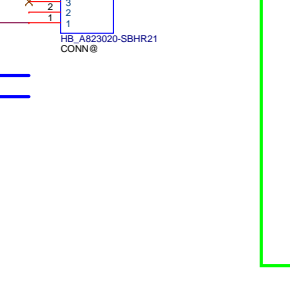
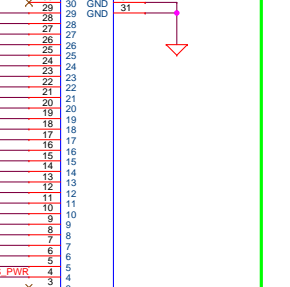
Power ON Circuit

ON/OFF switch

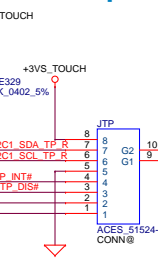


INT_KBD Connector

* Key Board Back Light



Touch pad



PTP

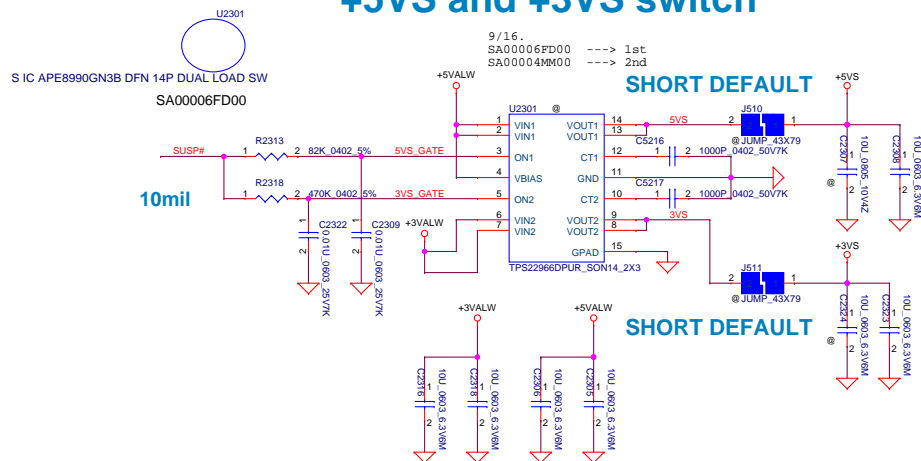


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				LA-B015P	0.1
				Date	Friday, October 17, 2014
				Sheet	27 of 56

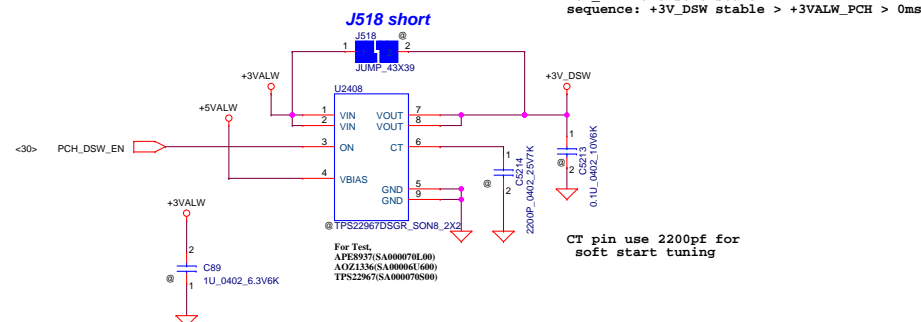
http://vinafix.vn

vinafix

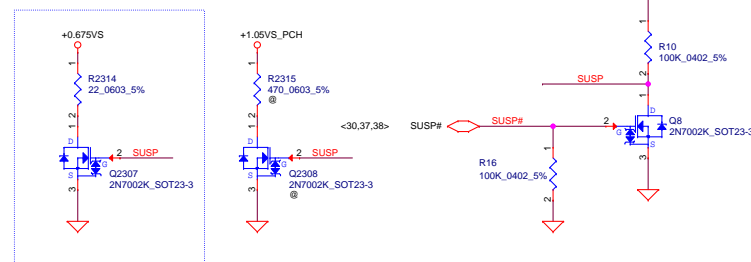
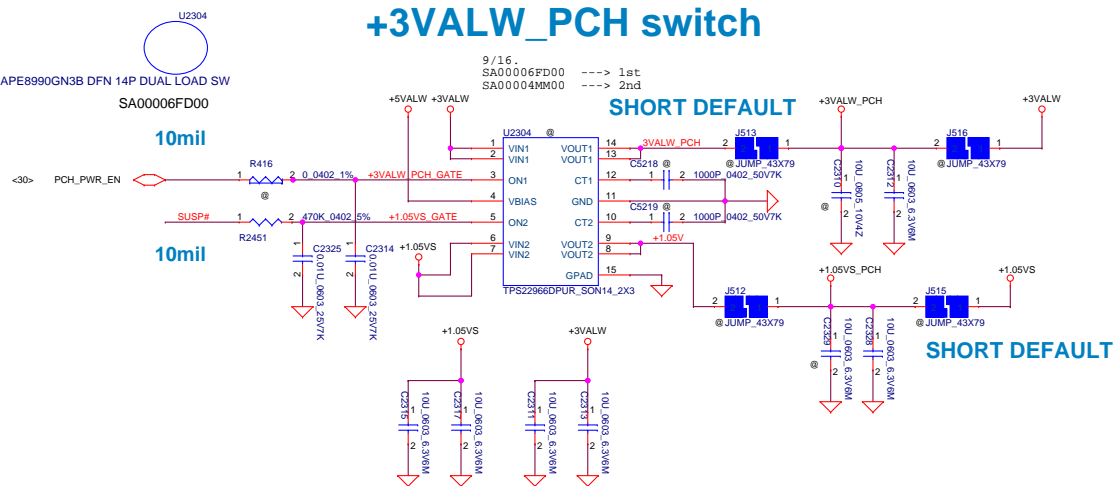
+5VS and +3VS switch



+3VALW TO +3V_DSW



+3VALW_PCH switch

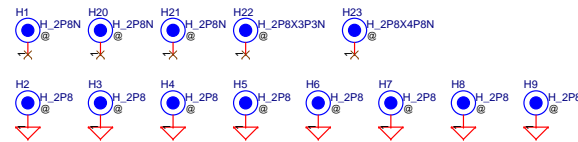


<http://vinafix.vn>

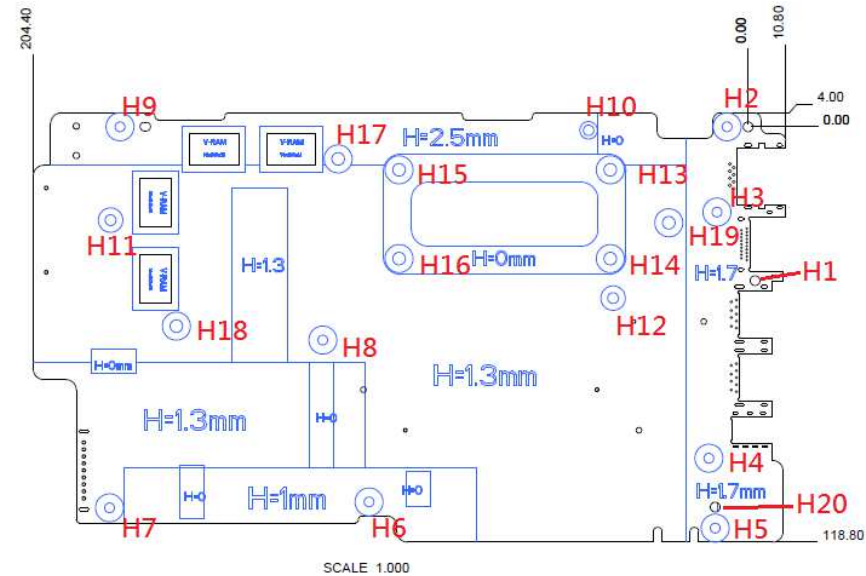
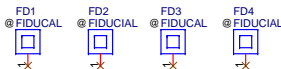
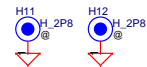
Security Classification		Compal Secret Data		Title	
Issued Date	2014/04/01	Deciphered Date	2015/04/30	Document Number	DC/DC Interface
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Date				Tuesday, September 16, 2014	Sheet 28 of 56

Screw Hole

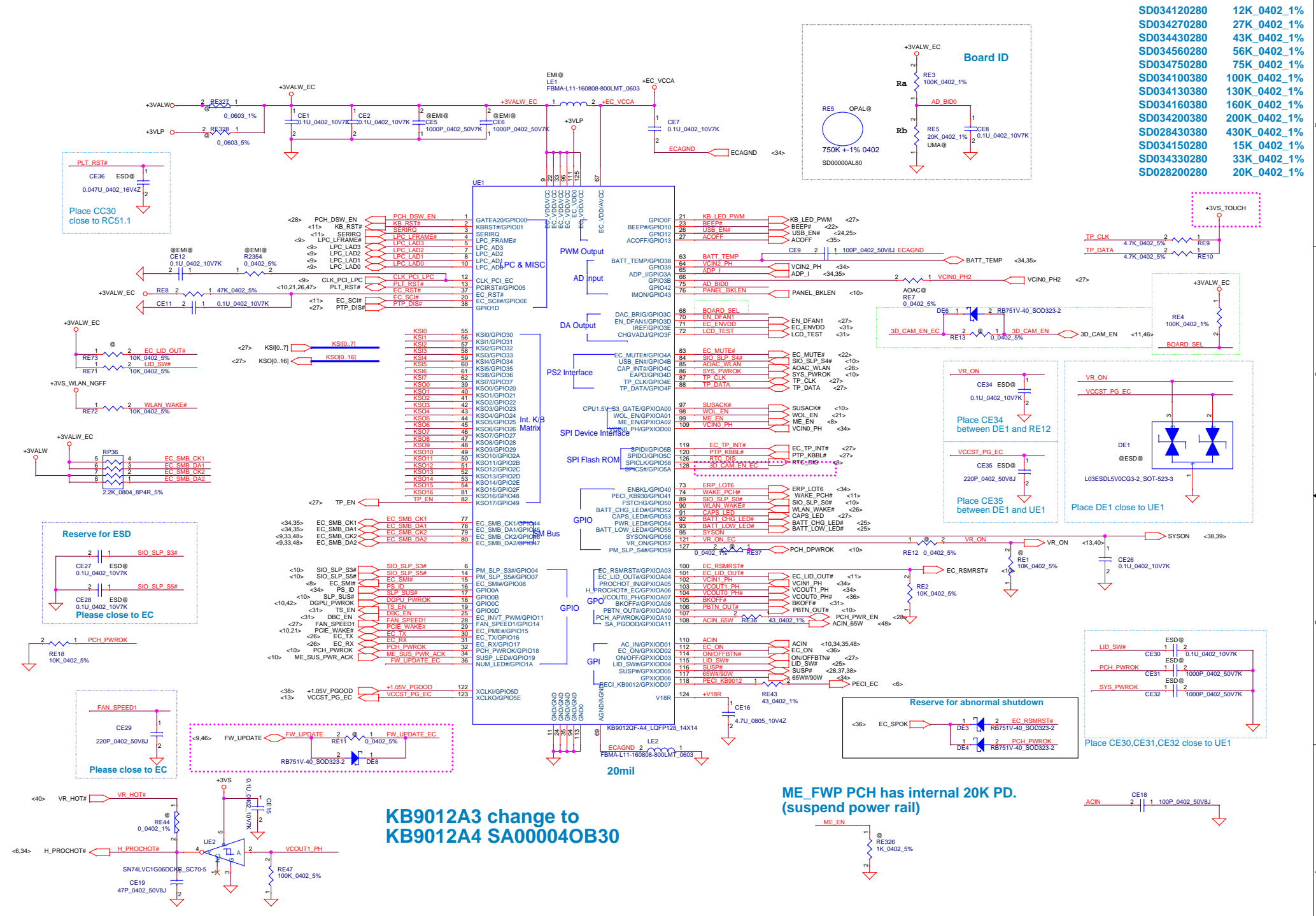
ZZZ
PCB 13G LA-B015P REV0 M/B
DA80011D000



H10 Delete.
Layout informed PCB vendor to do PTH solution.
(Function is same as beofre.)



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Issued Date	2014/04/01	Deciphered Date	2015/04/30	Title	Screw Hole
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				Date	Wednesday, September 10, 2014
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				Rev	0.1

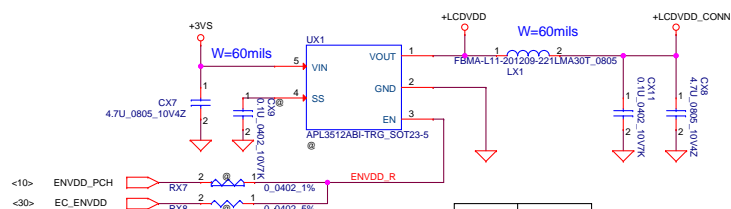
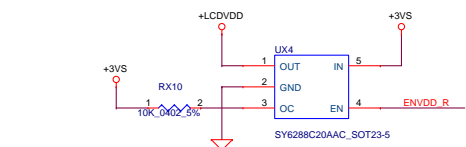


SD034120280	12K_0402_1%
SD034270280	27K_0402_1%
SD034430280	43K_0402_1%
SD034560280	56K_0402_1%
SD034750280	75K_0402_1%
SD034100380	100K_0402_1%
SD034130380	130K_0402_1%
SD034160380	160K_0402_1%
SD034200380	200K_0402_1%
SD028430380	430K_0402_1%
SD034150280	15K_0402_1%
SD034330280	33K_0402_1%
SD028200280	20K_0402_1%

KB9012A3 change to
KB9012A4 SA000040B30

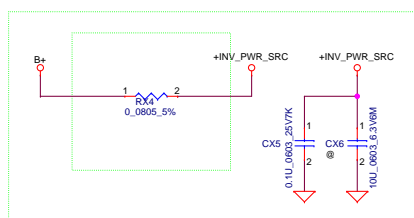
ME_FWP PCH has internal 20K PD.
(suspend power rail)

LCD PWR CTRL

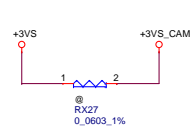


Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

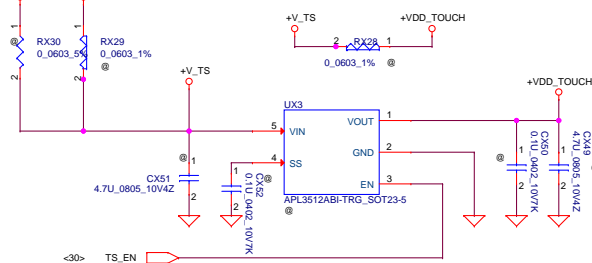
SS table



Webcam PWR CTRL



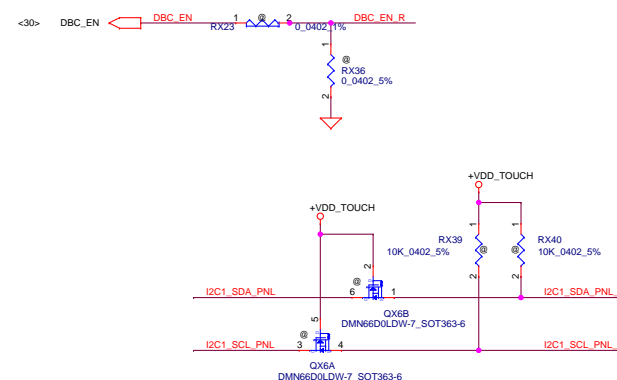
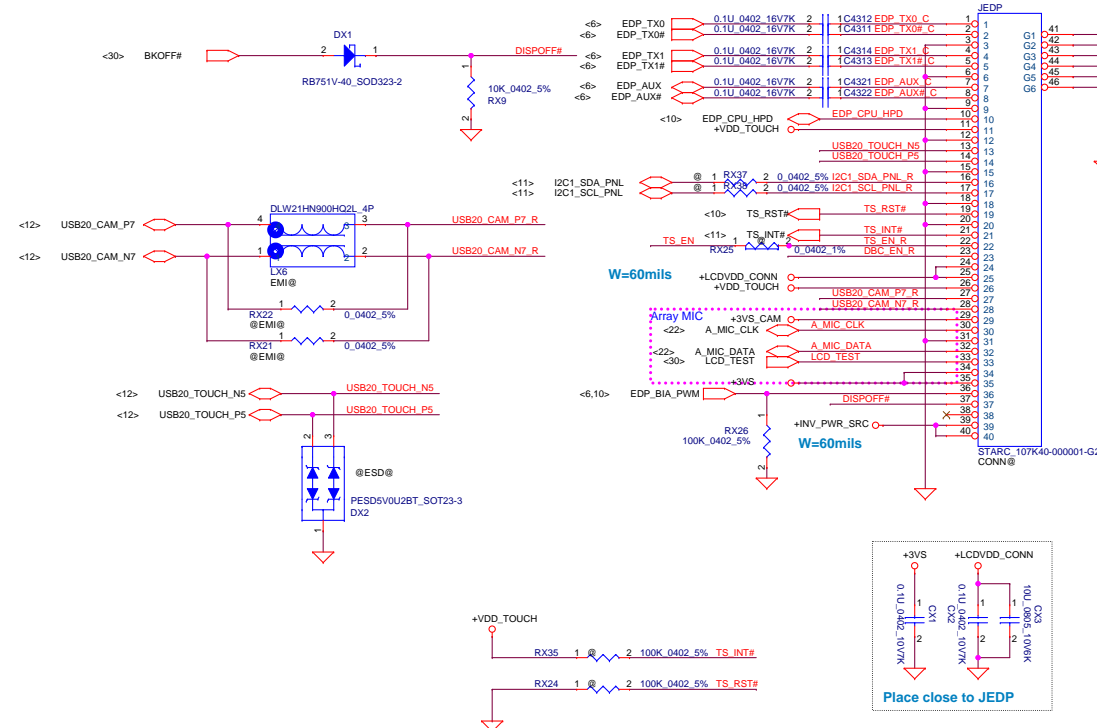
* Touch Screen Panel



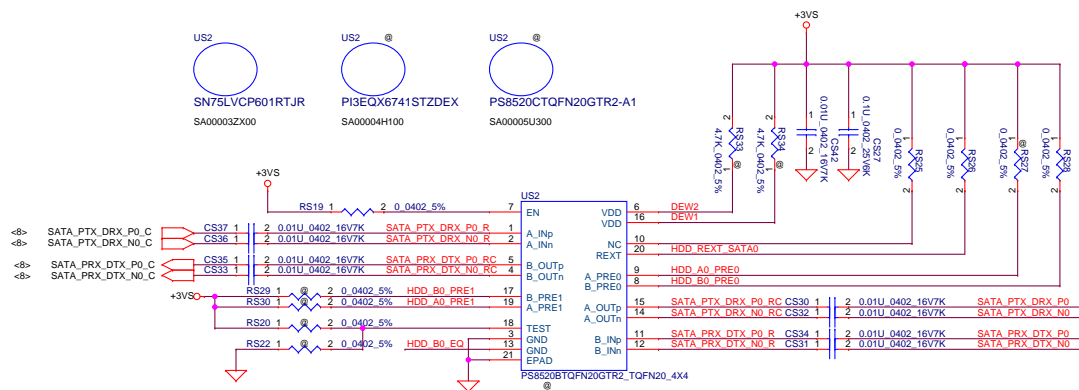
Css	Tss
0.1uF	100mS
10nF	10mS
1nF	1mS
Open or tied to VIN	1mS

```
SS table
```

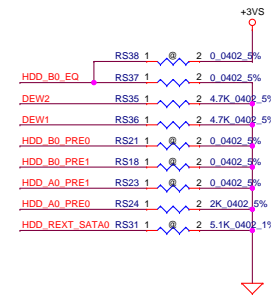
eDP Connector



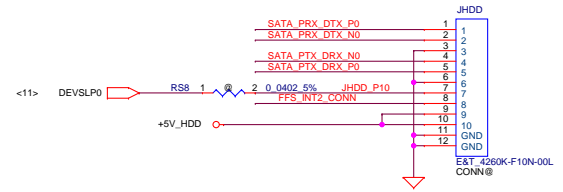
vinafix



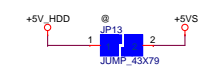
	US2	RS35	RS36	RS18	RS22	RS23	RS24	RS29
TI	SA000032X00	4.7K	4.7K	NC	NC	NC	2K	V
PARADE	SA000071U00	7.5K	NC	V	V	V	NC	NC



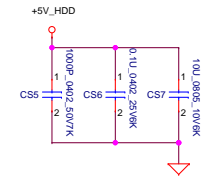
SATA HDD Connector



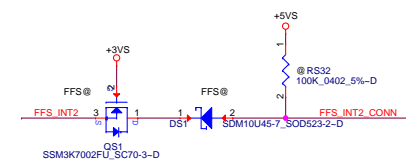
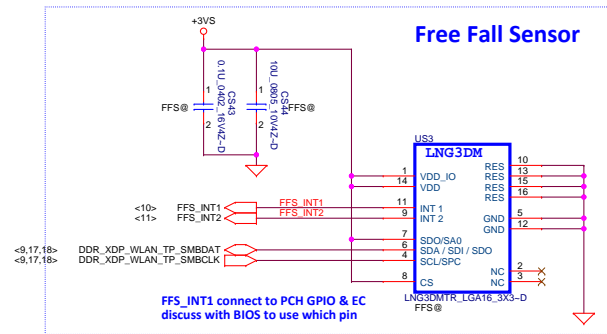
+5V_HDD Source



SHORT DEFAULT

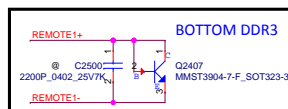
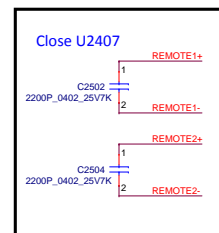
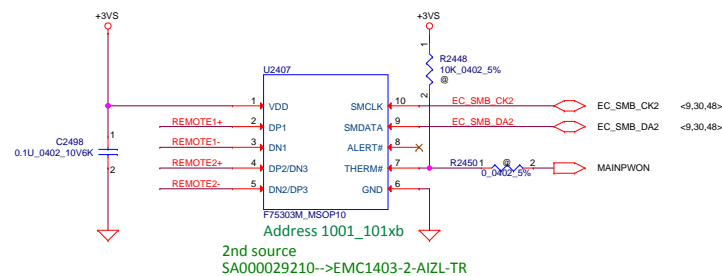


Free Fall Sensor

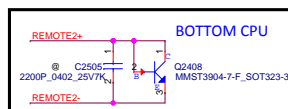


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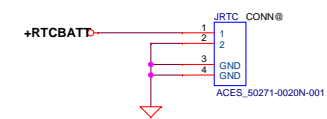
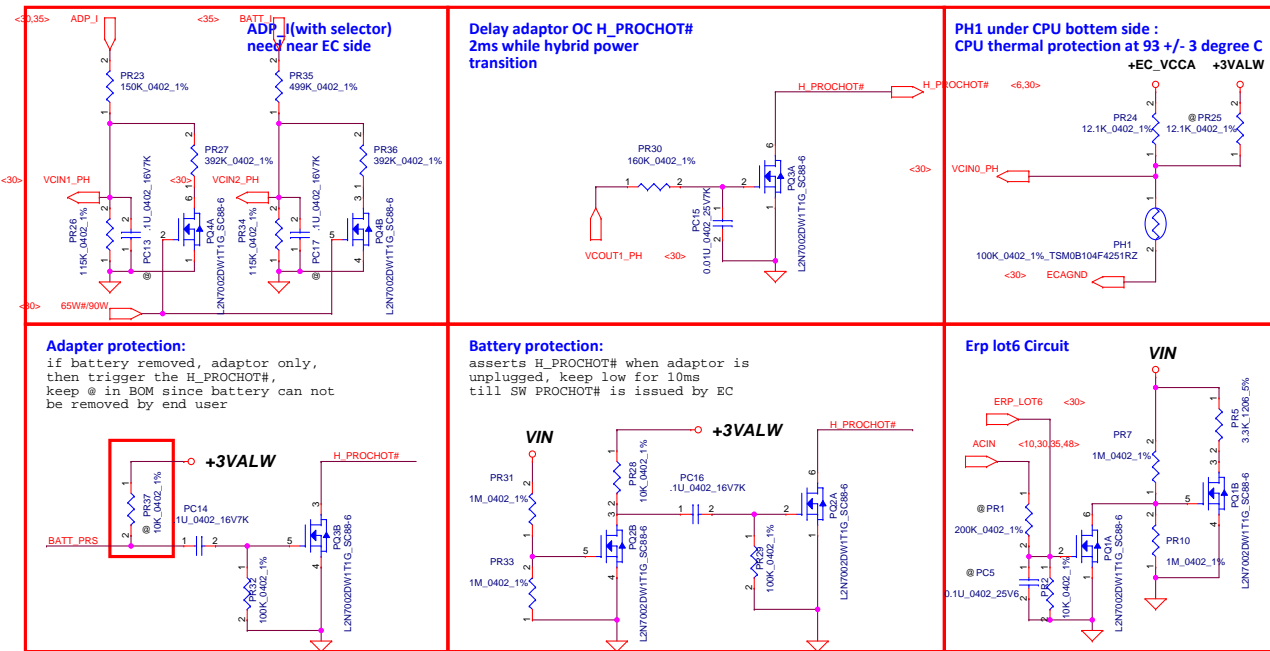
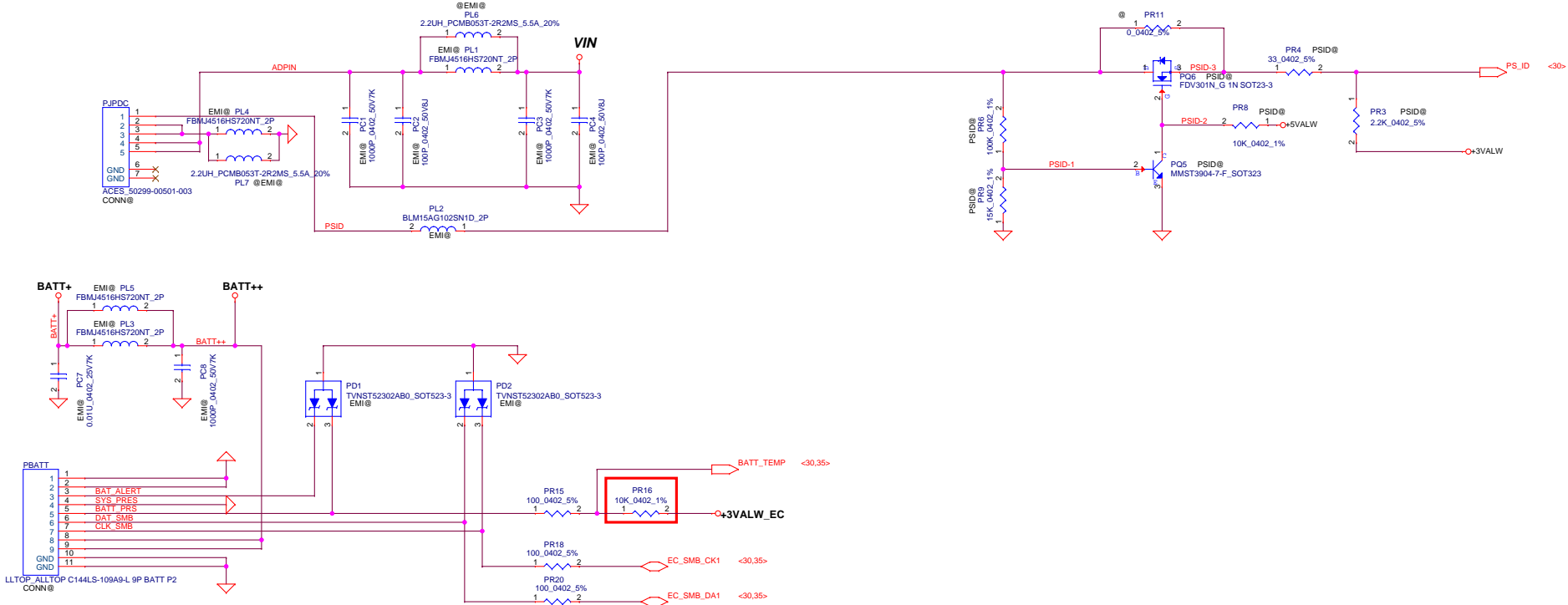
Fintek thermal sensor placed near by TOP DDR3

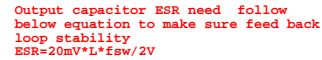


REMOTE1,2 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"



Other component (37.1)

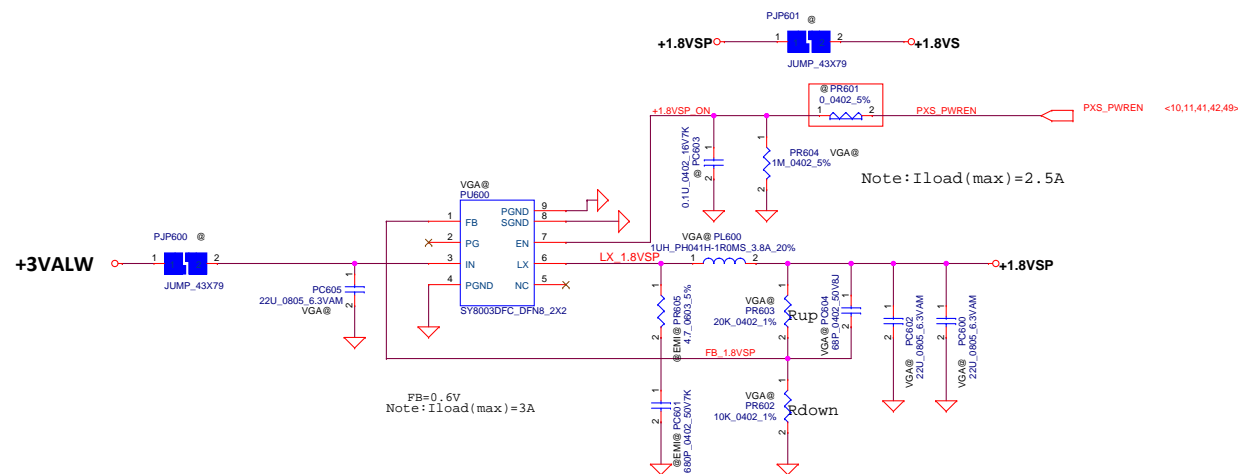
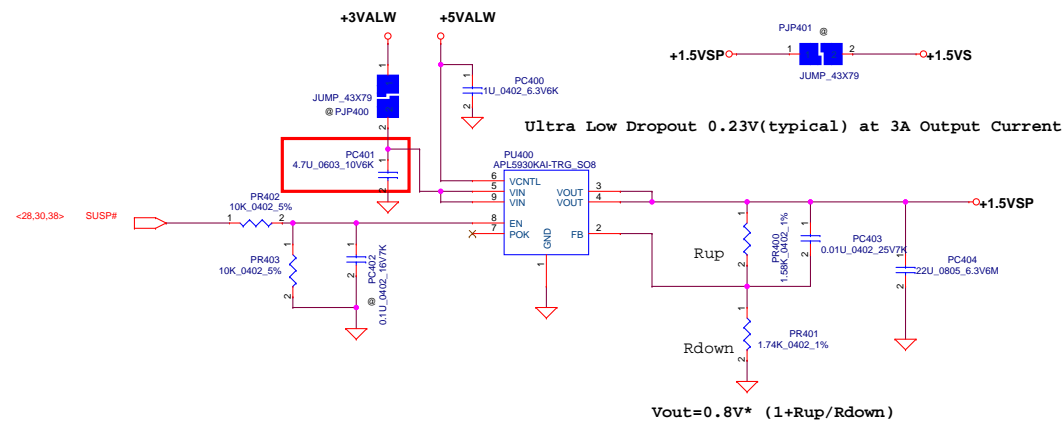




Change to 4.7u for TPS51285

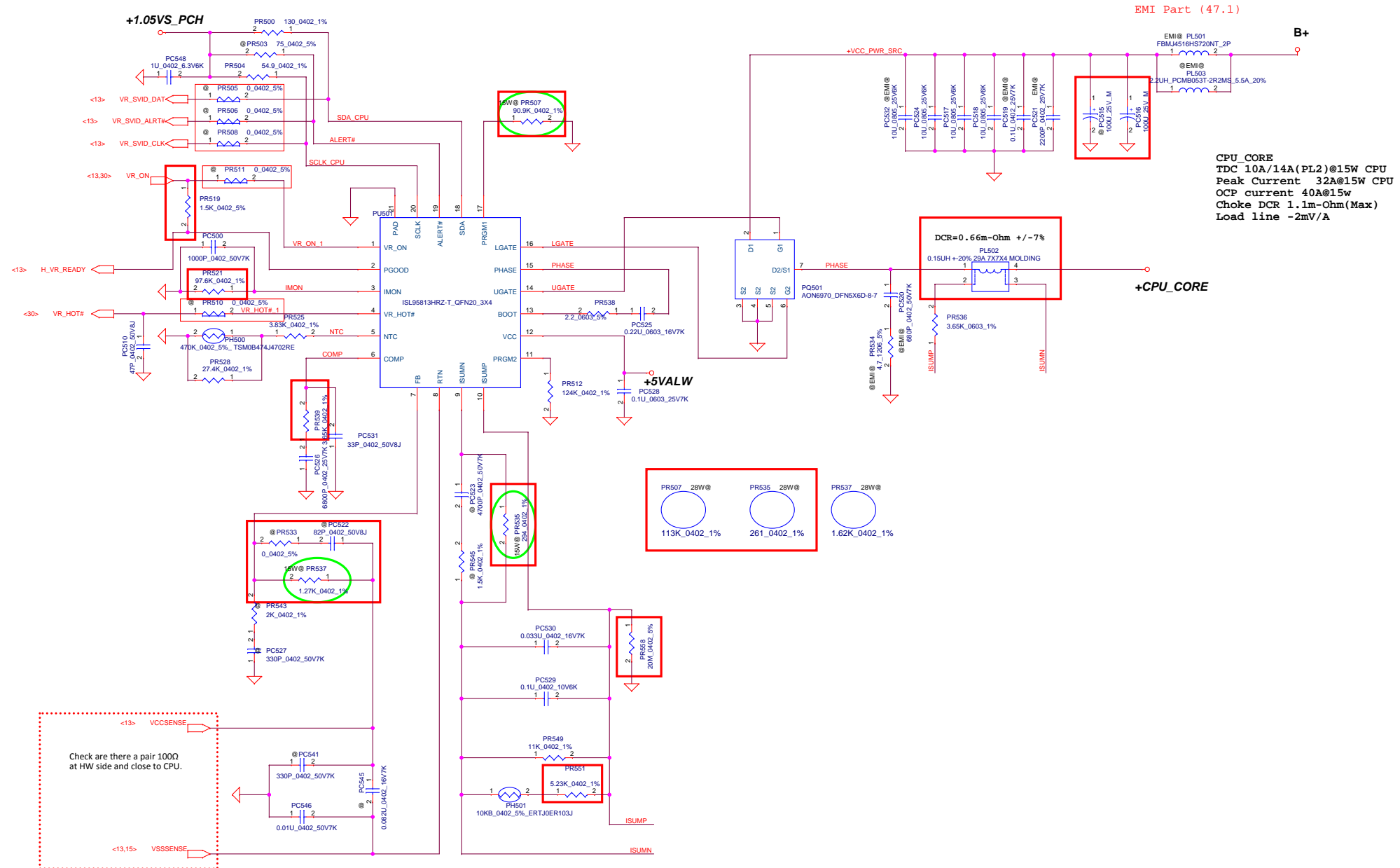
5VALWP	
TDC 5.96A	
Peak Current 8.51A	
OCP current 10.2A	
TYP	MAX
H/S Rds(on) :	22mohm , 30mohm
L/S Rds(on) :	10.8mohm , 13.6mohm

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2014/01/20		2015/01/19		PWR 3.3VALWP/5VALWP	
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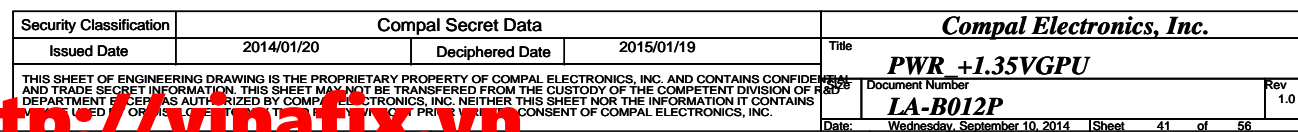
CPU_CORE
TDC 10A/14A(PL2)@15W CPU
Peak Current 32A@15W CPU
OCP current 40A@15w
Choke DCR 1.1m-Ohm(Max)
Load line -2mV/A

Check are there a pair 100Ω
at HW side and close to CPU.

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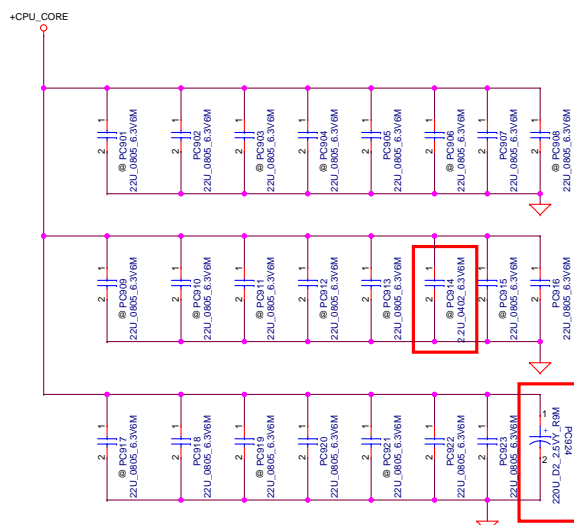
TDC=9A
Peak Current=13A
OCP=16A



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Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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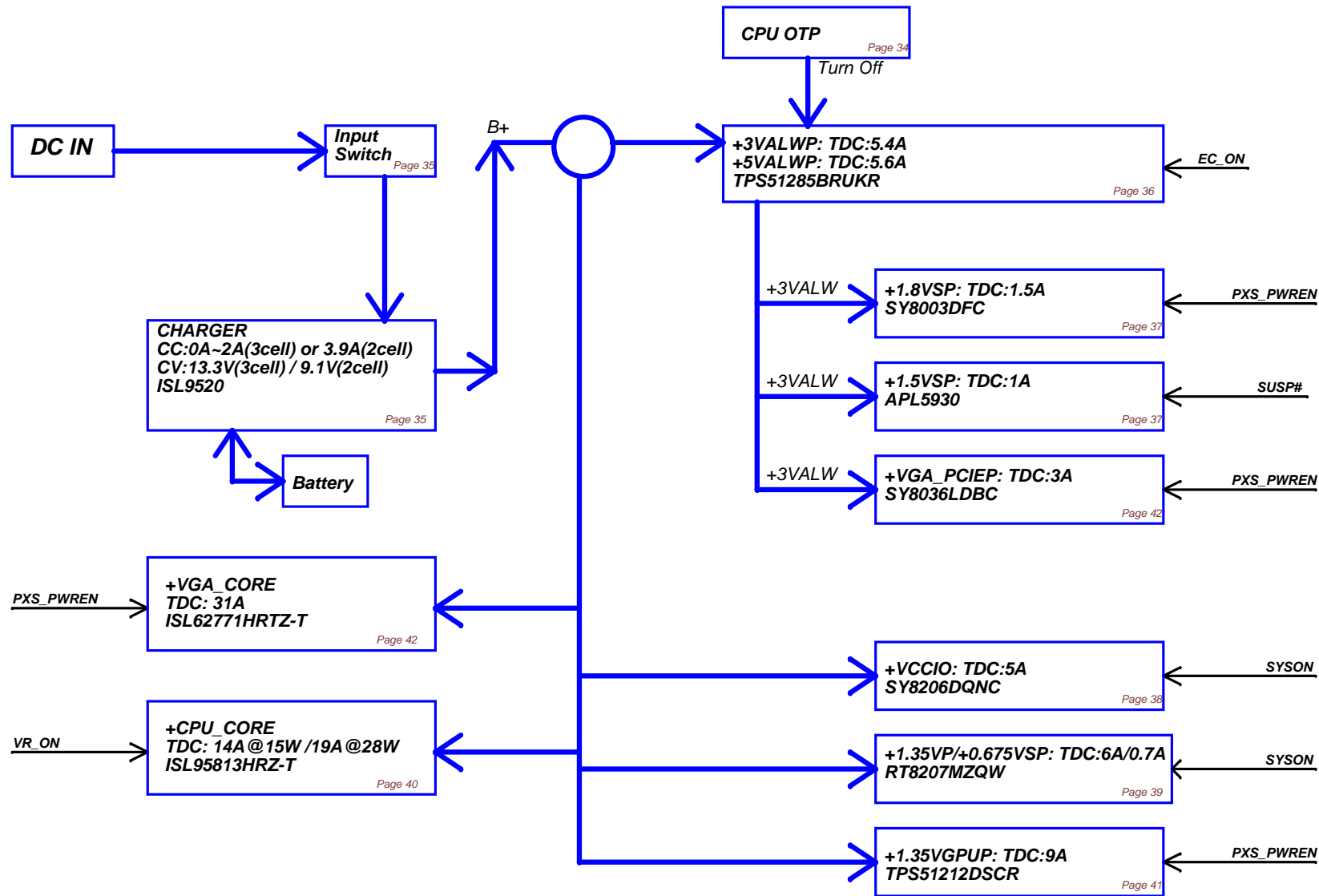


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Power block



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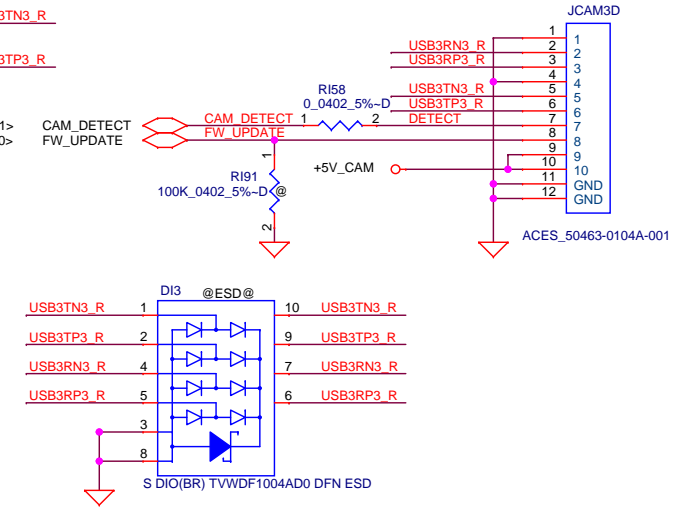
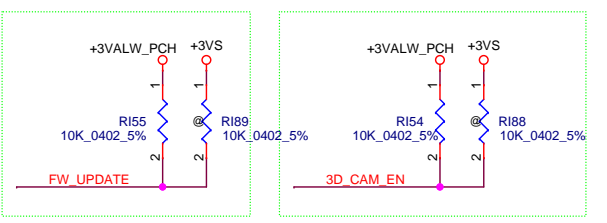
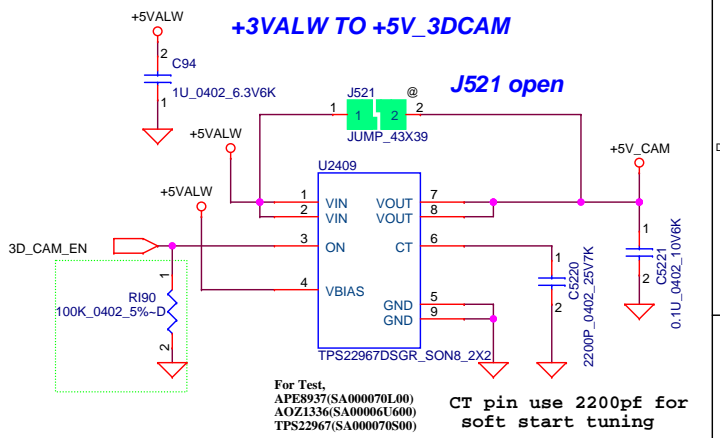
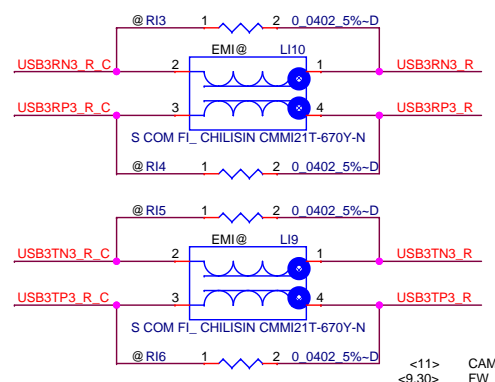
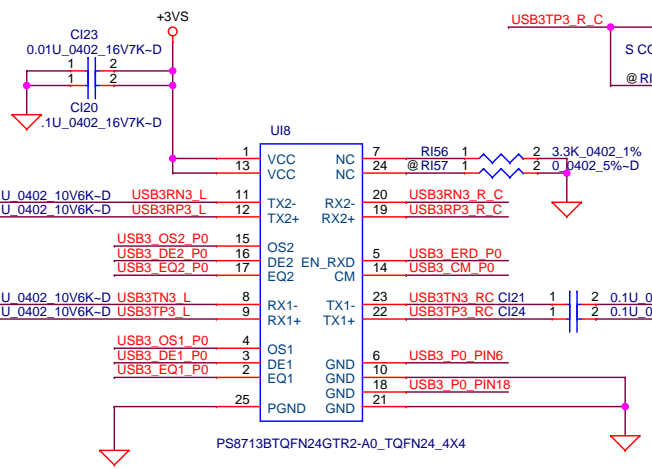
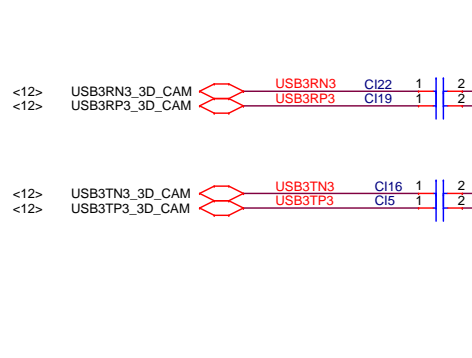
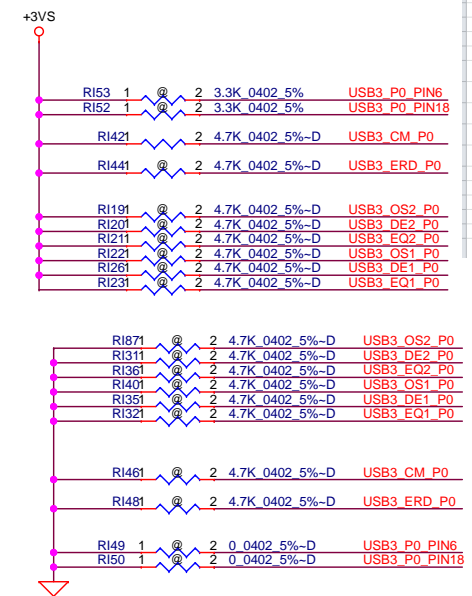
vinafix

1	44	DCIN/BATT CONN/OTP	13/10/24	Morris	design change	change PR16 from 100K to 10K add PR37 10K	0.2
2	45	CHARGER	13/10/24	Morris	design change	change PC711 from 1000pF to 0.01uF change PR711 from 49.9K to 51.1K change PR713 from 10K to 499K change PR724 from 100K to 499K change PC721 from 0.047u to 0.22u change PC722 from 0.1u to 1u add PC732 100u	0.2
3	46	3.3VALWP/5VALWP	13/10/24	Morris	design change for solve can't root issue	change PC104 from 0.1u to 0.22u change PC110 from 0.1u to 0.22u change PR102 from 2.2K to 10K add PR110 20K	0.2
4	50	VCORE	13/10/24	Morris	adjust CPU parameter	change PR507(15W@) from 90.9K to 169K change PR519 from 1.91K to 10K change PR521 from 95.3K to 97.6K change PR539 from 8.06K to 909 change PC515,PC516 from SF0000005100 to SF0000004M00 change PL502 from SH000000NM00 to SH000000PQ00 change PR535(15W@) from 340 to 210 change PR537 from 1.27K to 1.37K change PR535(28W@) from 432 to 261 change PR507(28W@) from 113K to 205K change PR551 from 2.61K to 5.23K add PC522 82pF add PR533 0-ohm	0.2
6	52	VGA_CORE/PCIE	13/10/24	Morris	design change from vendor change LL	change PR1040 from 1.24K to 825	0.2
7	53	PROCESSOR DECOUPLING	13/10/24	Morris	adjust CPU parameter	change PC924 from SGA20331E10 to SGA00009800 remove PC901,PC903,PC904,PC906,PC908,PC909,PC910,PC911,PC912,PC913,PC914,PC915,PC917,PC919,PC921	0.2
8	45	CHARGER	13/10/28	Morris	design change for plug out battery shut down issue	change PC723 from 0.01uF to 0.47uF change PR728 from 0 to 9.09K change PC728 from 4700pF to 2200pF change PC701 from 220pF to 1000pF	0.2
9	46	3.3VALWP/5VALWP	13/12/12	Morris	design change from EE request	add PR115 10K-ohm	0.3
10	50	VCORE	13/12/12	Morris	design change from Intel recommend	change PR519 from 10K to 1.5K	0.3
11	48	+VCCIO	13/12/13	Morris	design change from EE request	delete PR310 and add PR300 0-ohm	0.3
12	50	VCORE	14/01/20	Morris	adjust CPU parameter	change PR507(15W@) from 169K to 90.9K change PR507(28W@) from 205K to 113K	1.0
13	53	PROCESSOR DECOUPLING	14/02/13	Morris	design change from thermal request	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0
14	50	VCORE	14/03/03	Morris	design change for VGA thermal issue	change PC836 PC837 PC838 PC839 from SGA20331E10 to SGA00006A00	1.0

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				LA-B012P	1.0
				Date:	Wednesday, September 10, 2014
				Sheet	45 of 56

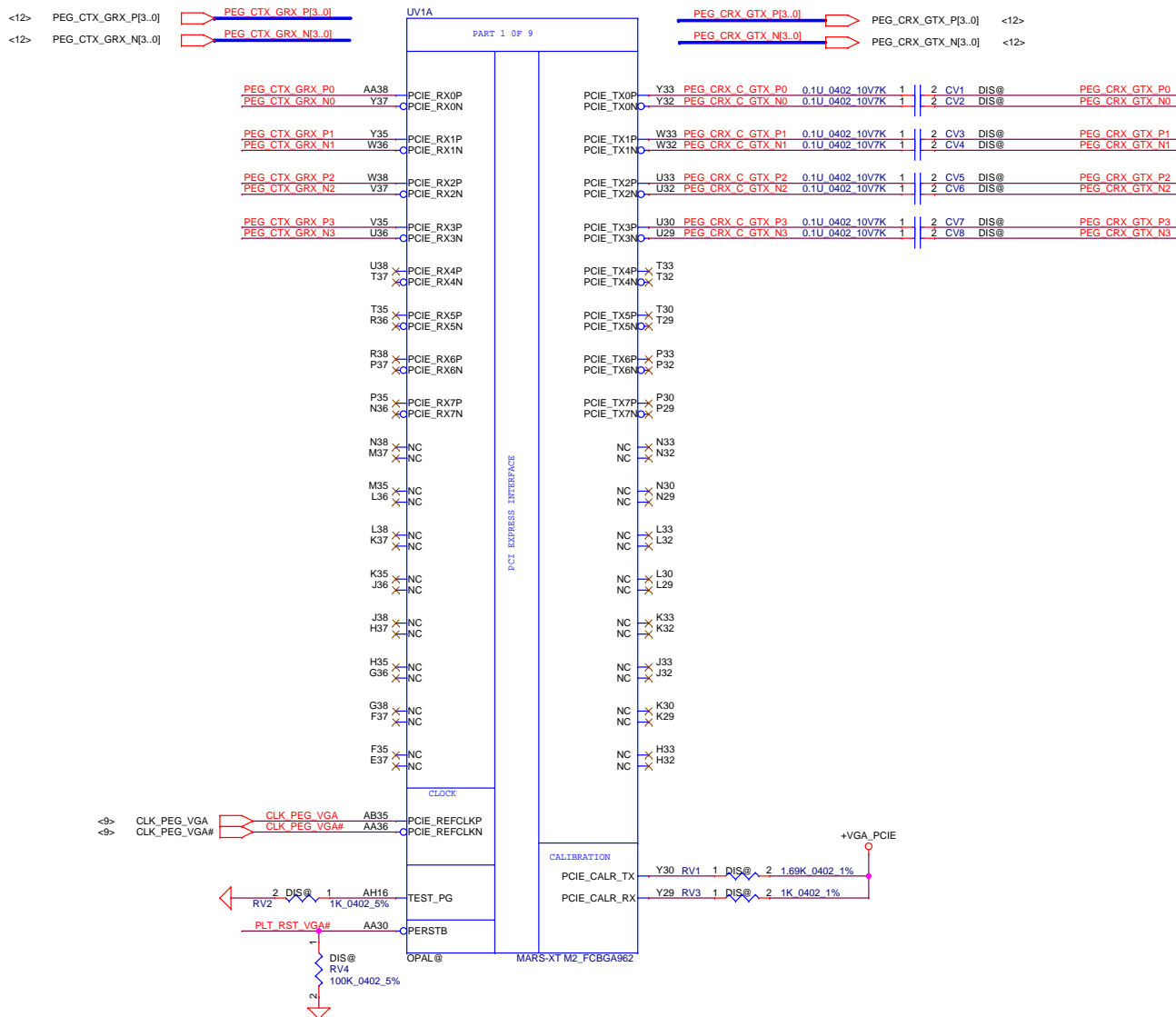
http://vinafix.vn

Vendor	Part	TI	Spec	schematic netname	3Vs	GND
1	YD0	YCC	Same			
2	B_EQ0	EQ1	LL: 9.5dB (default) LH: 13dB HL: 4.5dB HH: 7.7 dB	USB3_EQ1_P0	RI23	@ RI32
3	DE0	DE1	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_DE1_P0	RI26	@ RI35
4	EQ1	OS1	LL: 9.5dB LH: 13dB HL: 4.5dB HH: 7.7 dB	USB3_OS1_P0	RI22	@ RI40
5	PD#	EN_RXD	it can be left open	USB3_ERD_P0	RI44	@ RI48
6	B_DE1	GND	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_P0_PIN6	RI53	@ RI49
7	REXT	NC	4.99K			RI56 4.99K
8	B_ina	RX1-	Same			
9	B_ina	RX1+	Same			
10	GND	GND	Same			
11	A_OUTa	TX2-	Same			
12	A_OUTp	TX2+	Same			
13	VDD	VCC	Same			
14	TS1/NC	CM	4.7K ohm resistor for performance adjustment	USB3_CM_P0	RI42	@ RI46
15	A_EQ1	OS2	LL: 9.5 dB (default) LH: 13 dB	USB3_OS2_P0	RI19	@ RI87
16	A_DE0	DE2	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_DE2_P0	RI20	@ RI31
17	A_EQ0	EQ2	LL: 9.5 dB (default) LH: 13 dB	USB3_EQ2_P0	RI21	@ RI36
18	A_DE1	GND	LL: 3.5dB (default) LH: no DE HL: 2.7dB HH: 5 dB	USB3_P0_PIN18	RI52	@ RI50
19	A_ina	RX2-	Same			
20	A_ina	RX2+	Same			
21	GND	GND	Same			
22	B_OUTp	TX1+	Same			
23	B_OUTa	TX1-	Same			
24	I2C_EN	NC	this pin can be NC or connected to GND	NC		RI57 @

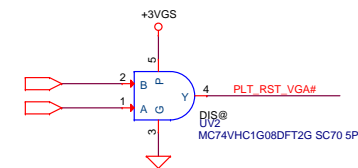
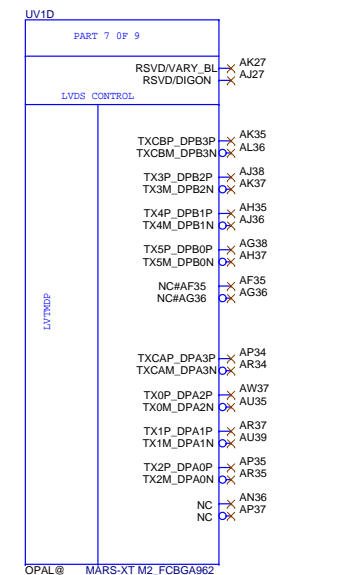


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LVDS Interface



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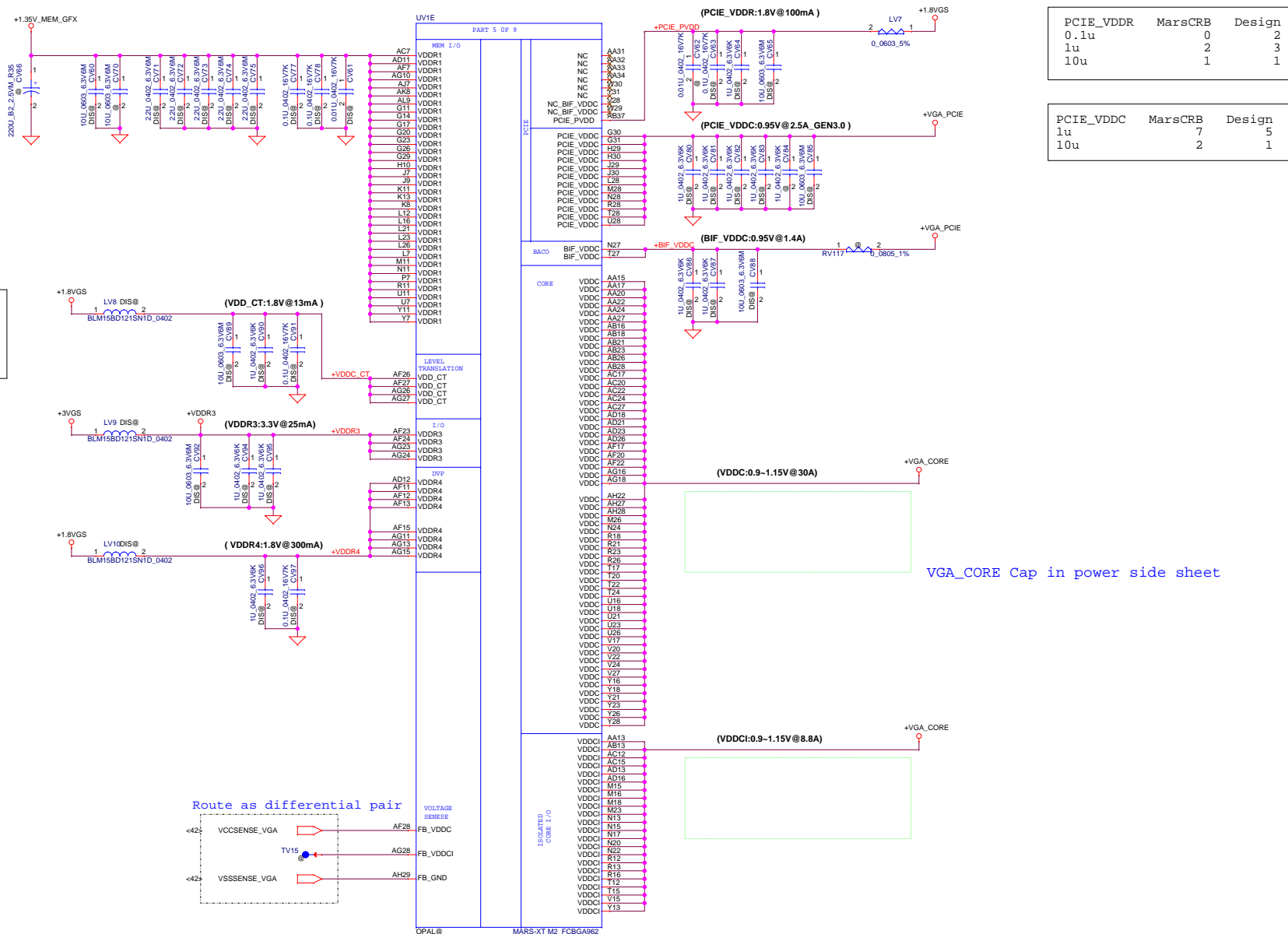
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VDDR1	MarsCRB	Design
0.01u	5	0
0.1u	5	5
1u	0	5
2.2u	5	0
10u	3	5
220u	0	1


VDD_CT	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	3
10u	1	1


VDDR3	MarsCRB	Design
120ohm	1	0
0.1u	1	0
1u	2	3
10u	0	1


VDDR4	MarsCRB	Design
220ohm	1	1
0.1u	1	1
1u	1	1
10u	1	0

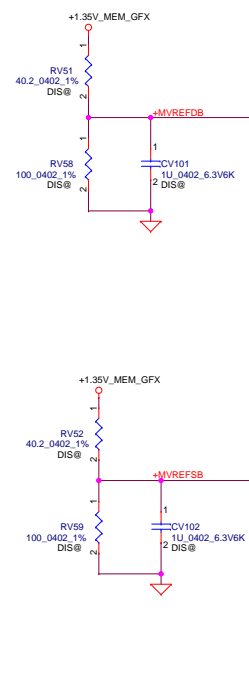


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<55,56> MDB[0..63] 

MAB[15..0] 

B_BA[2..0] 



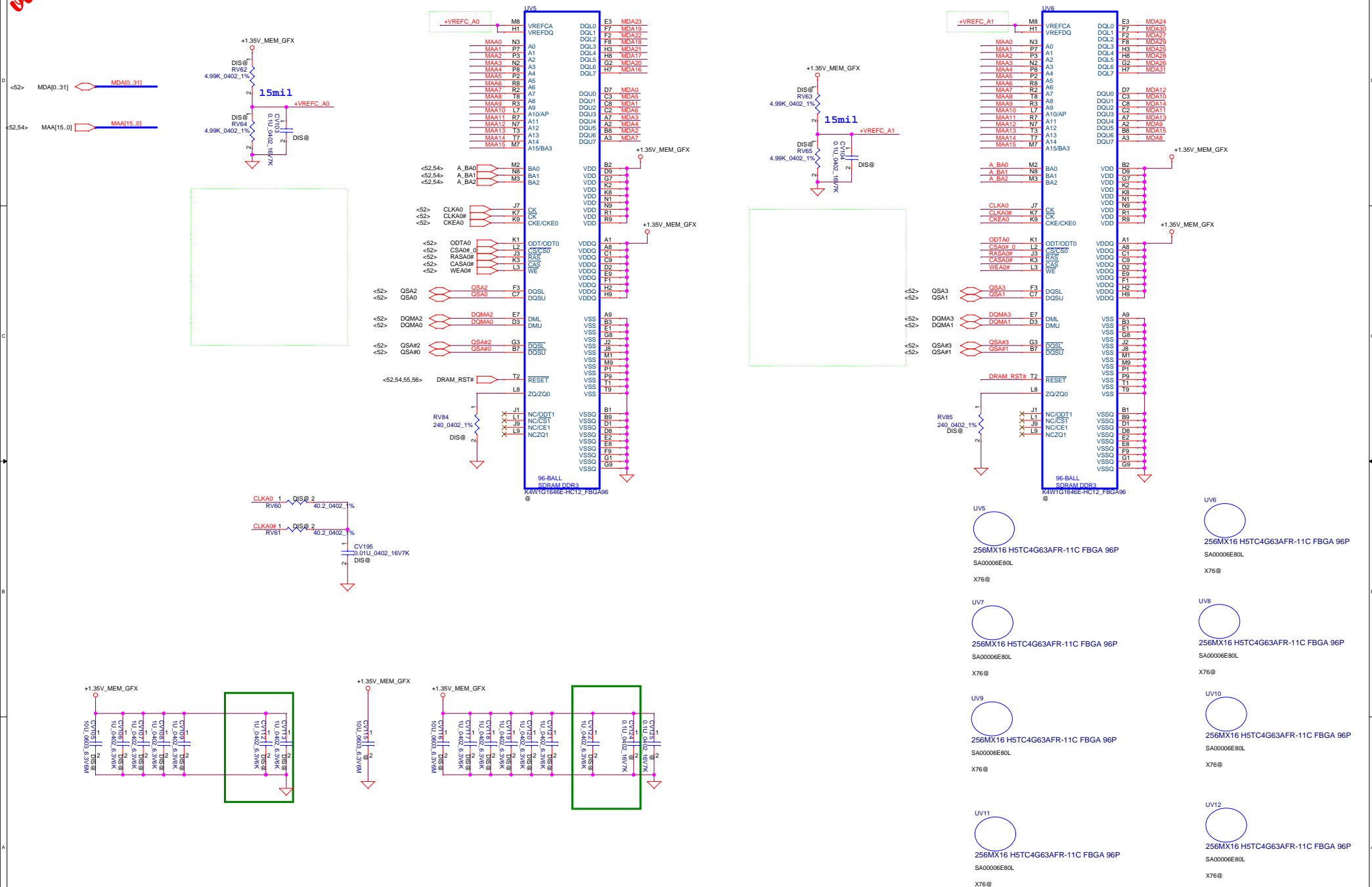
This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitor Resistor values are an example only. The Series R and Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

Place all these components very close to GPU (Within 25mm) and keep all component close to each other (within 5mm) except Rser2

Ball to RV57 < 1"
CV100 to RV57 < 20
CV100 to RV53 < 1"

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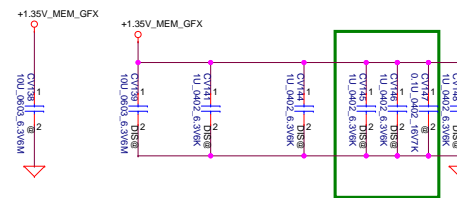
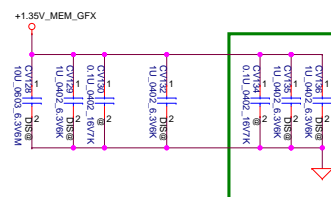
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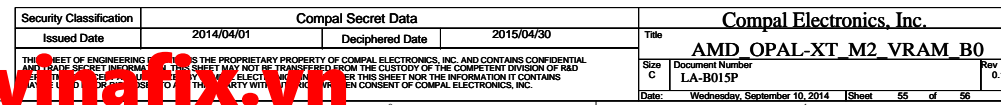
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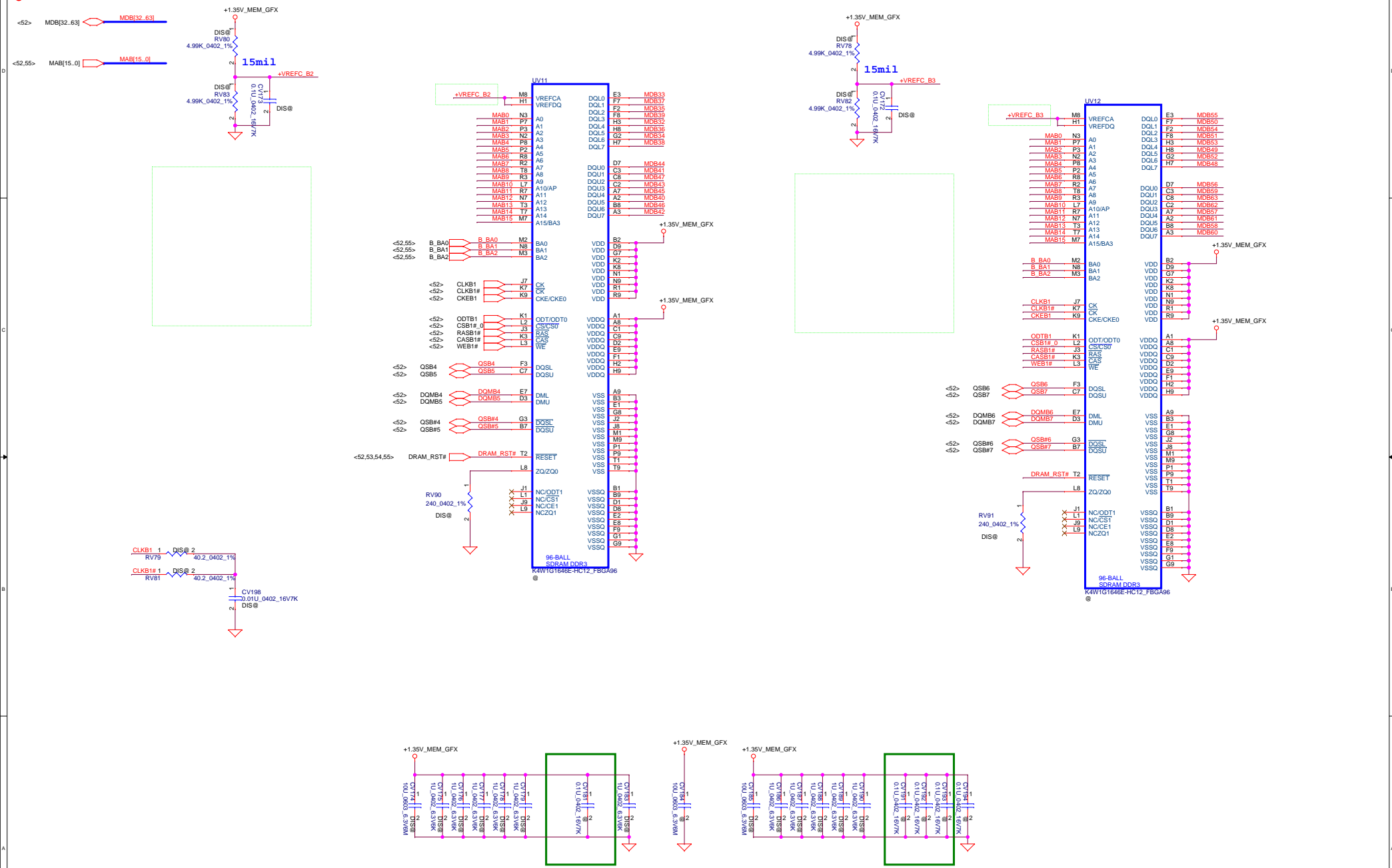


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