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MS-7A43

ATX
Ver:
1.1

Intel -Skylake plamform C232

CPU:

Skylake-S

System Chipset:

C232

Onboard Chip:

HD Audio Codec:ALC892

LAN:Intel I219V

SIO:Nuvoton 6793D

Flash ROM: SPI 64MB /128MB

Main

Memory:

DDRIV (800/1066/1333/1600/2133MHz) * 4 (Dual Channel)

ACPI:

NIKO/UIP

PWM:

IMVP8 -ISL95858

Expansion

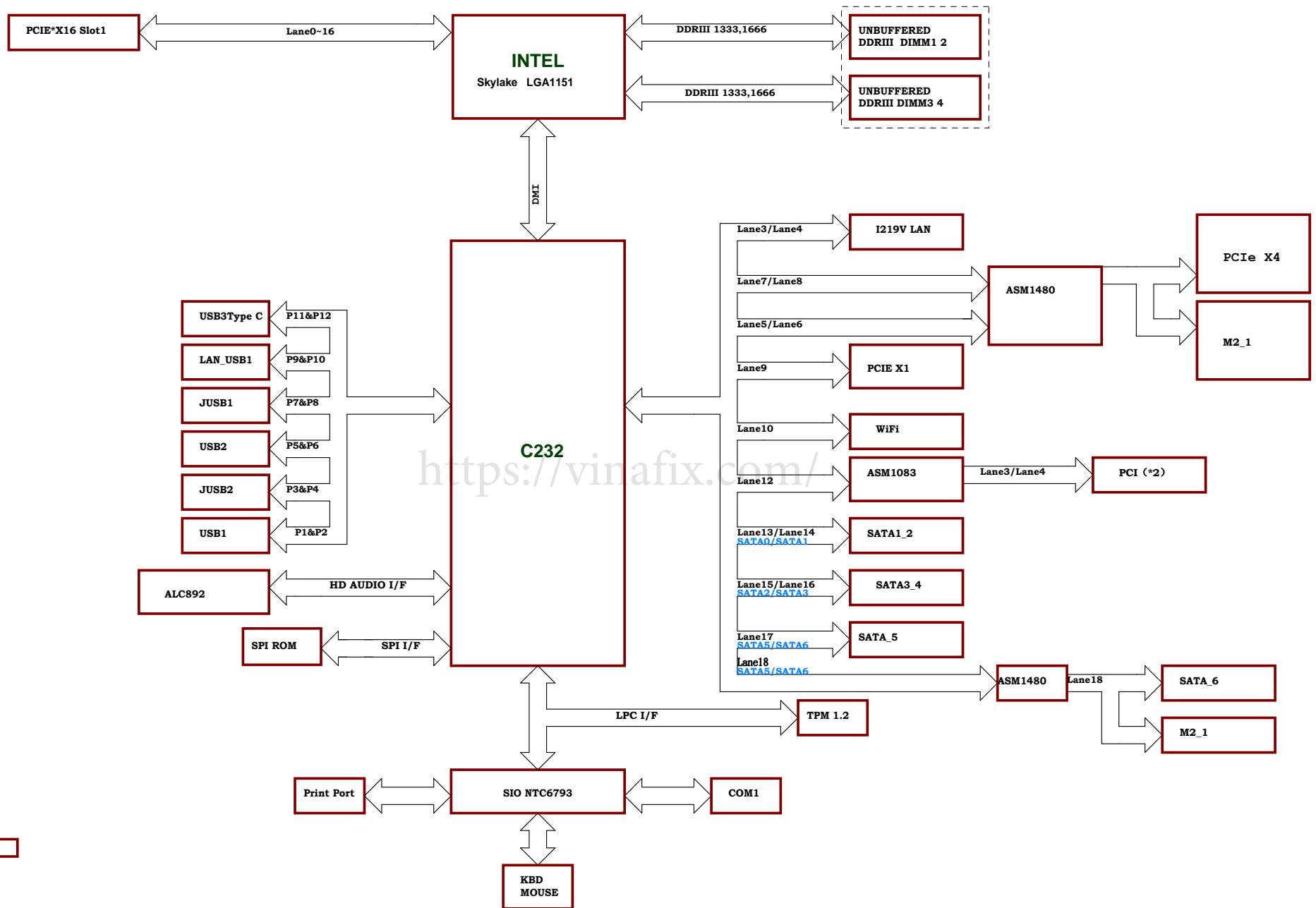
Slots:

PCI Express (X16) Slot *1
PCI Express (X4) Slot * 1
PCI Express (X1) Slot * 2
PCI Slot * 2
M2 * 2

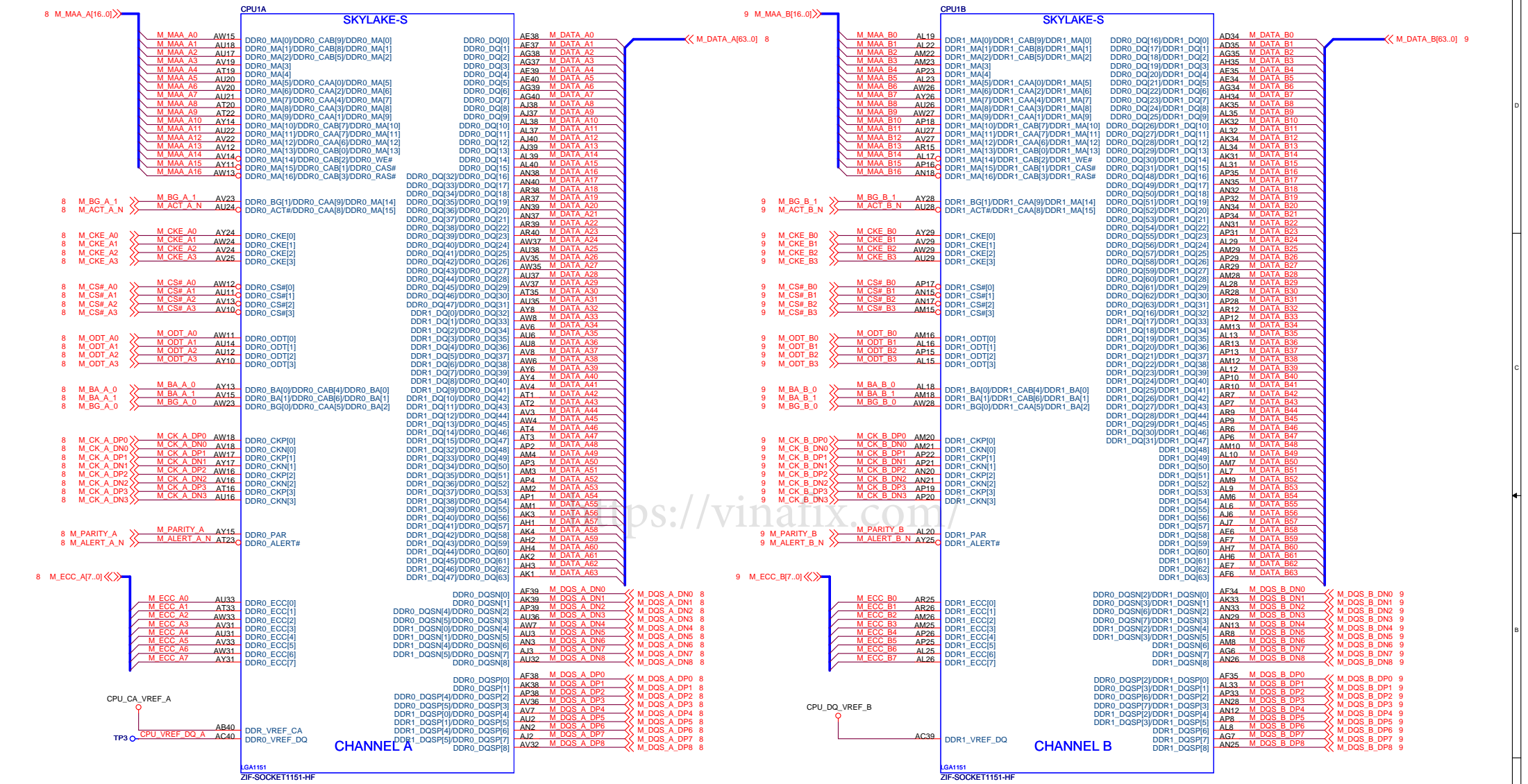
Other:

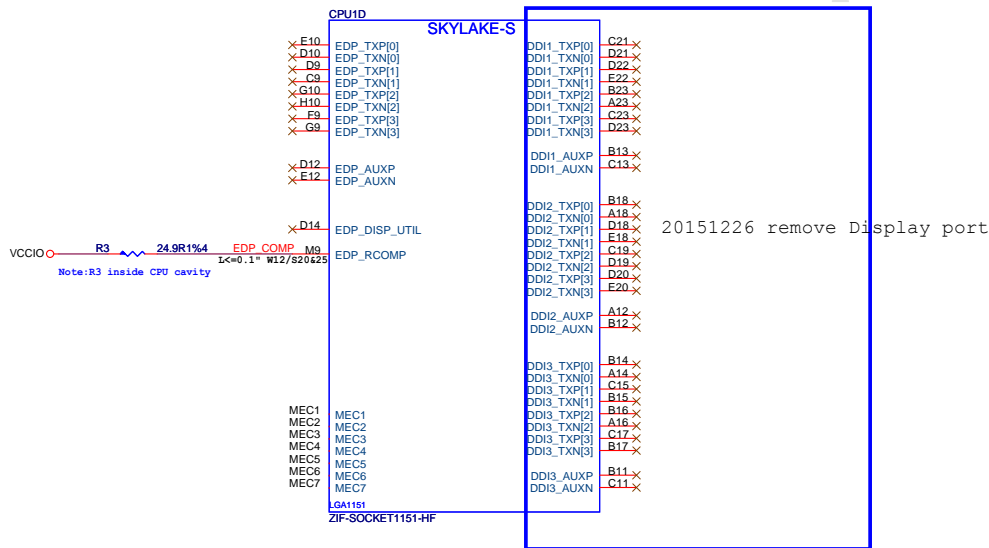
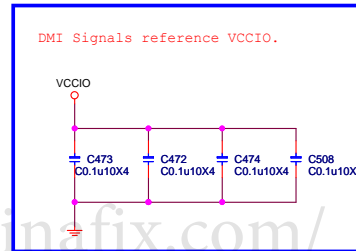
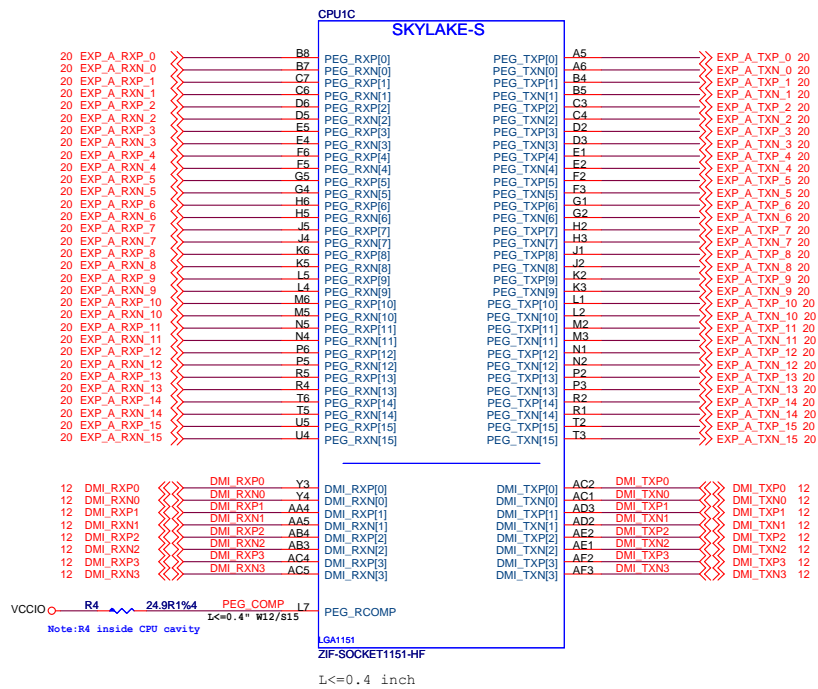
SATA3.0 x6 (PCH)
REAR USB2.0 *2
FRONT USB2.0 *2
FRONTUSB3.0 *4
REAR USB3.0 *2

MS-7A43 Block Diagram

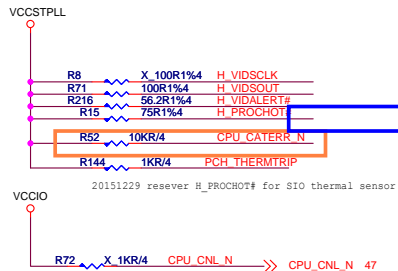


- Slot Sequence:
- PCIE X16
 - PCIE X1
 - PCIE X1
 - PCIE X4
 - PCI
 - PCI



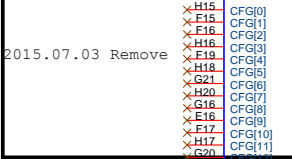


CPU Socket MEC5 Hole top layer add Soldermask, bot layer not add Soldermask.
 1.MEC5 connect to GND.
 2.Add CPU1L.
 3.Footprint change to ZIF SOCK1151_TEST_7978.

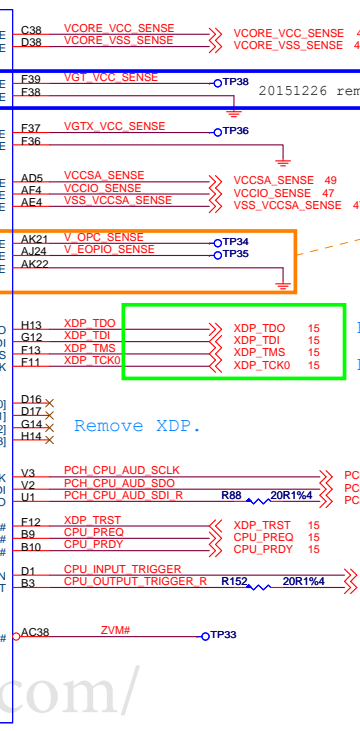
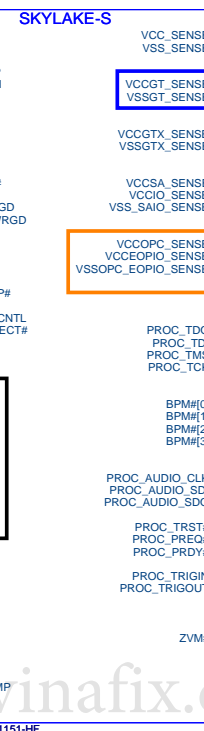


CPU_PM_DOWN_R < 200 mil

Remove XDP.



Remove XDP.



Remove XDP.
Reserve for DCI.

Close CPU <1100 mil
1000 mil < CPU_XDP_MBP0~1 < 6000 mil



NOTE: This CPU LIB only for MS-7978 and MS-7984, other designer please make sure need it

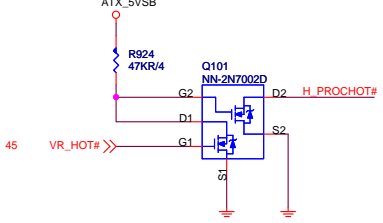
EN#	SLOT2	SLOT5
X8		
0	X8	X8
1	X16	X0

The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.

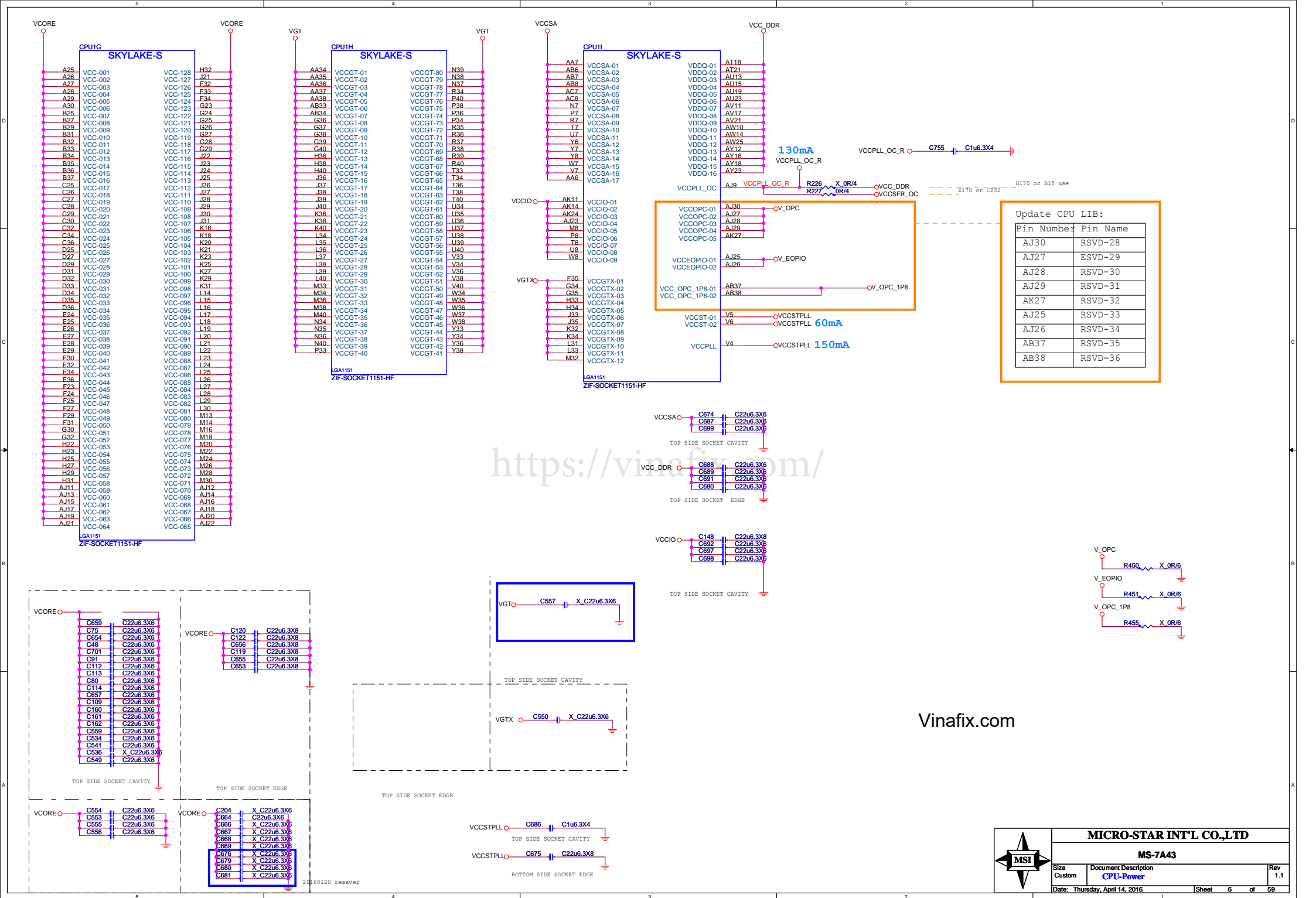
CFG Strap

CFG Table		
	HIGH	LOW
0	No Lock	Lock
1		
2	NORM	REVERSE
3		
4	DISABLE	ENABLE
5	DISABLE	ENABLE
6	DISABLE	ENABLE
7	RESET#	BIOS REQ
8		
9		
10		
11		
12		
13		
14	RSVD	
15	RSVD	

2015.04.23 Remove



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MS-7A43		
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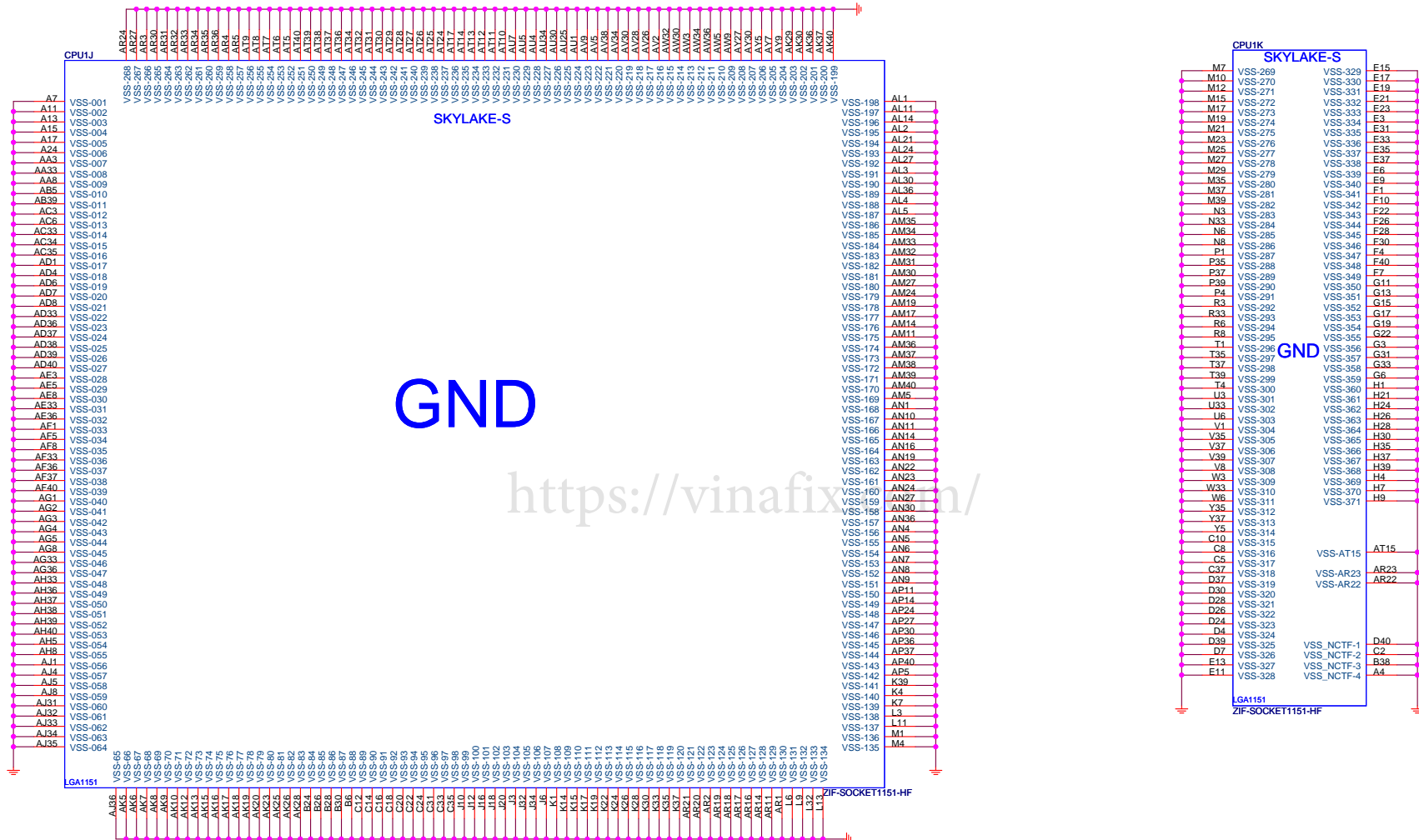
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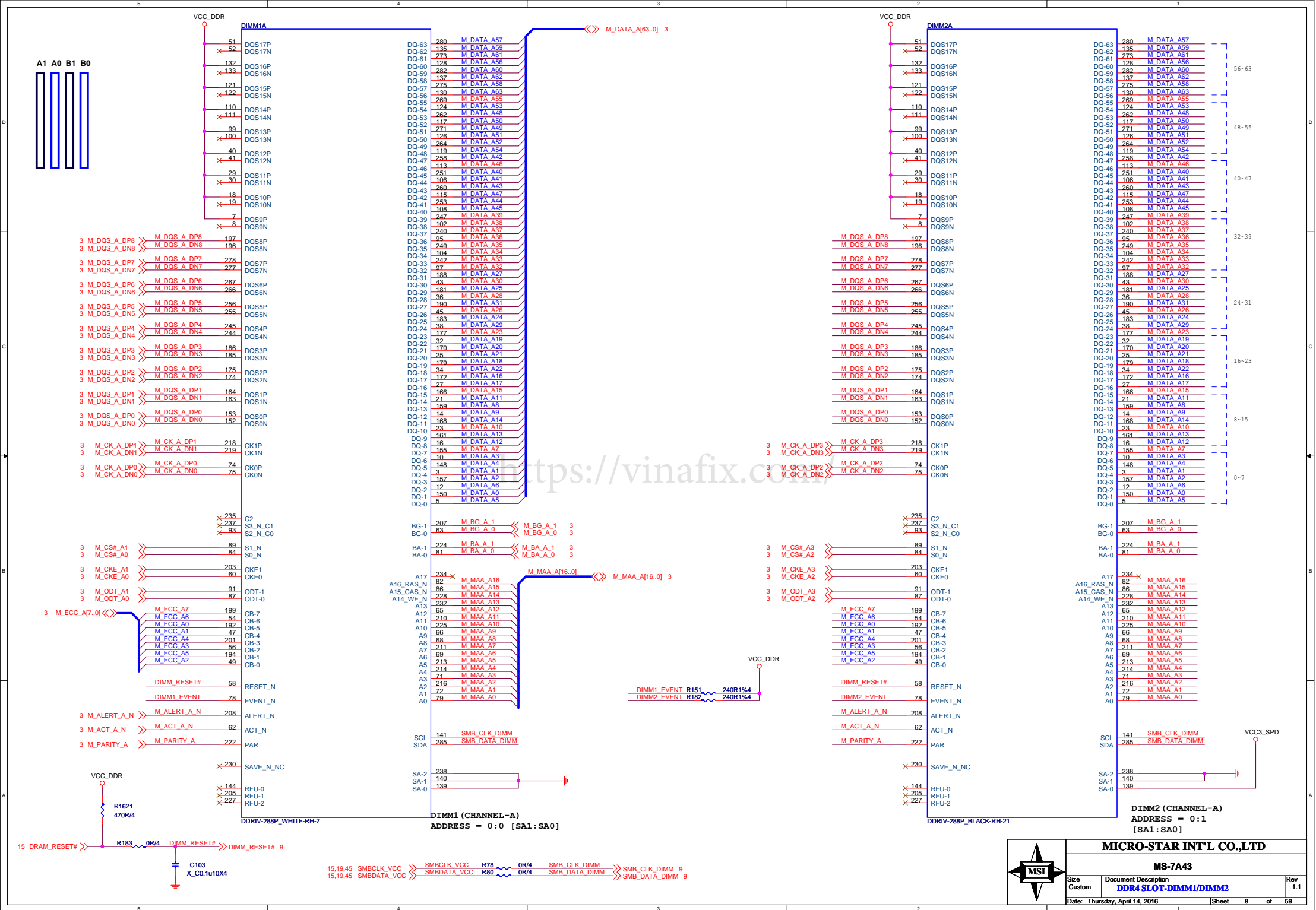


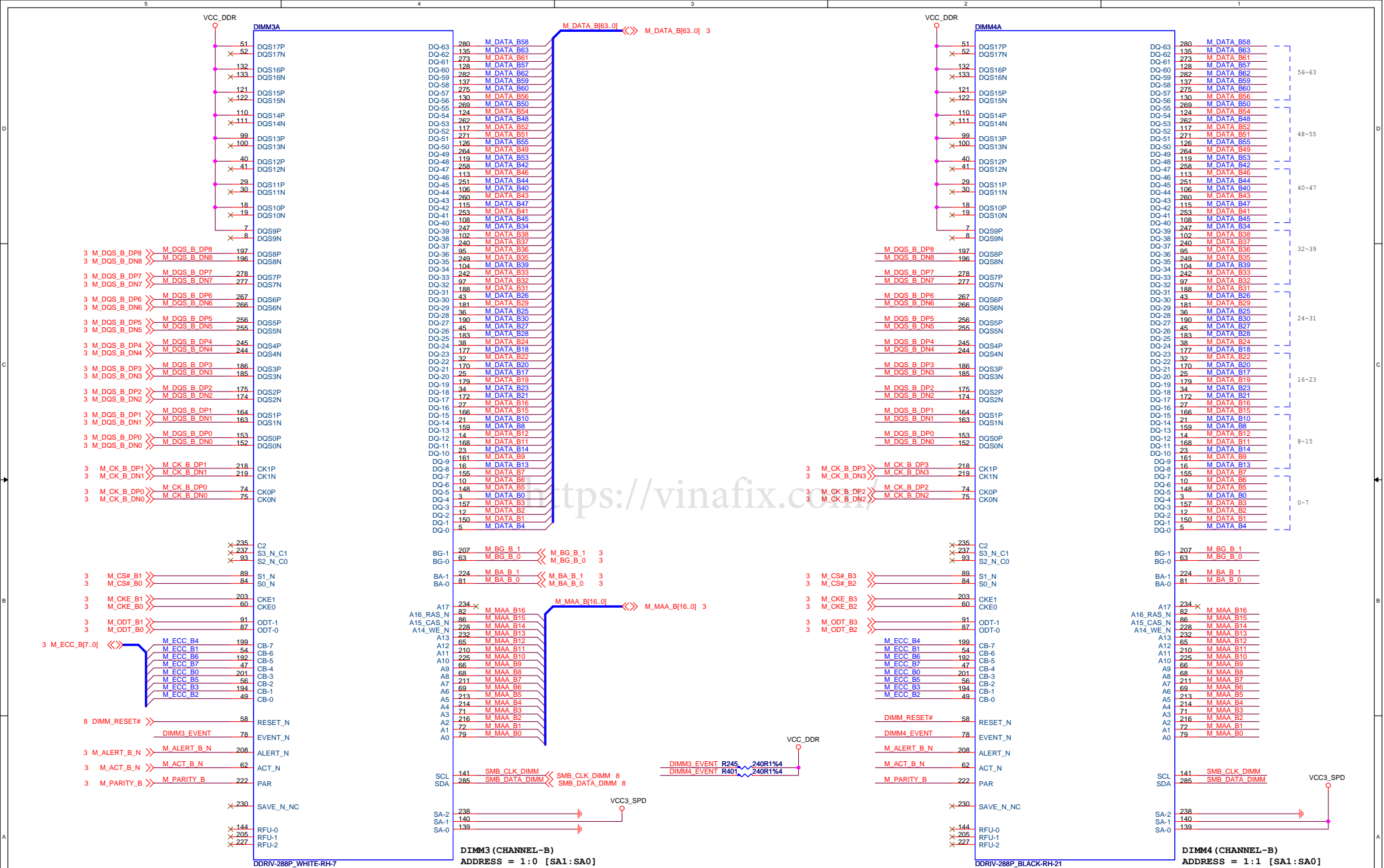
MICRO-STAR INT'L CO.,LTD

MS-7A43

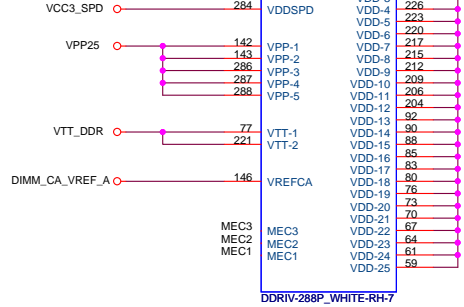
Size	Document Description	Rev
Custom	CPU-Power	1.1
Date: Thursday, April 14, 2016		Sheet 6 of 59



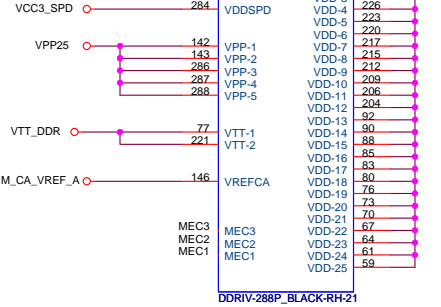
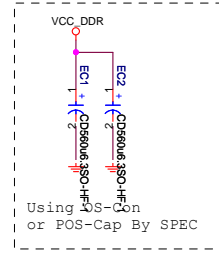




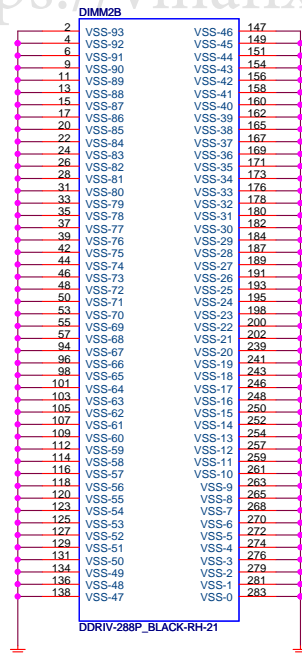
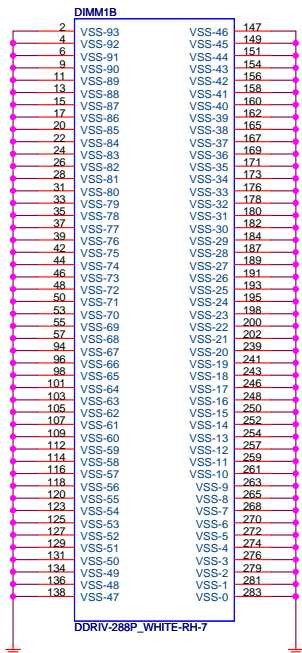
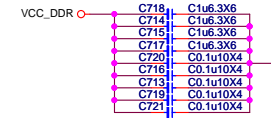
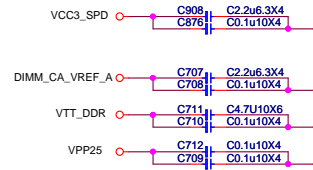
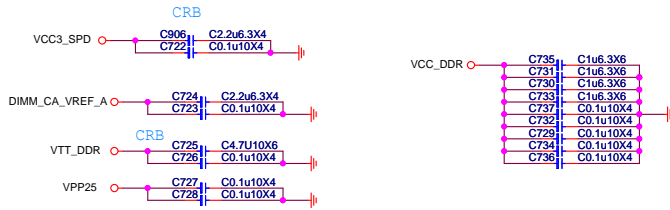
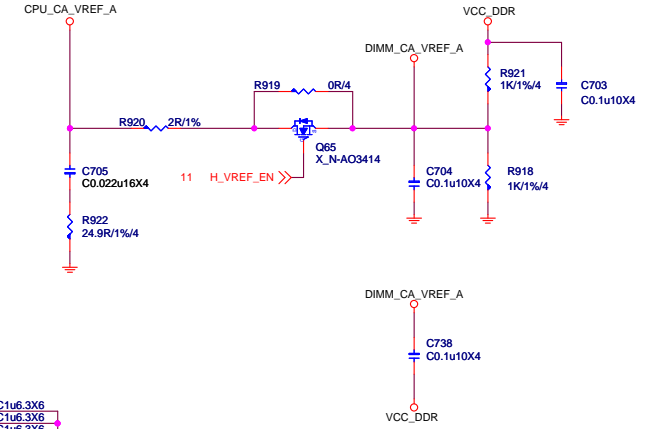
VCC3 1 2 VCC3_SPD
F-SMD1812P110TF-RH



DIMM SLOT PN BY SPEC



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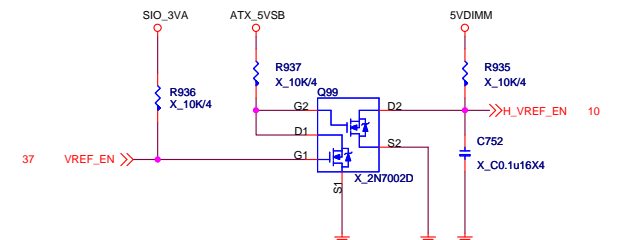
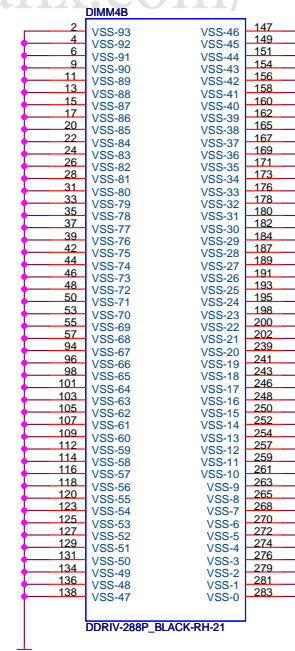
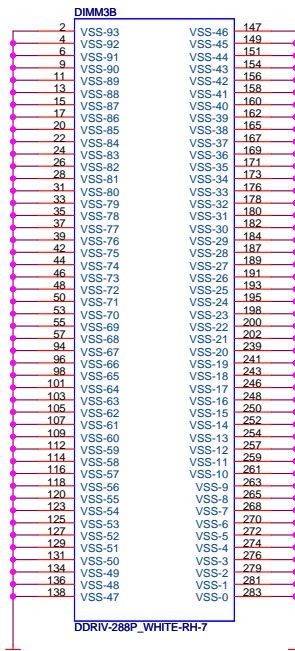
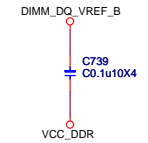
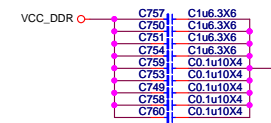
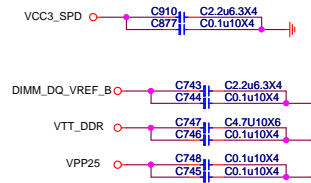
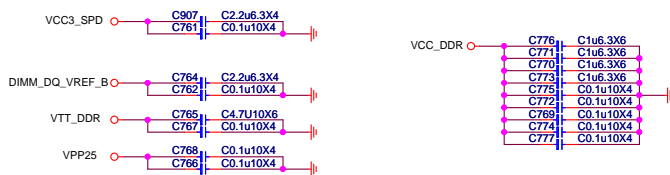
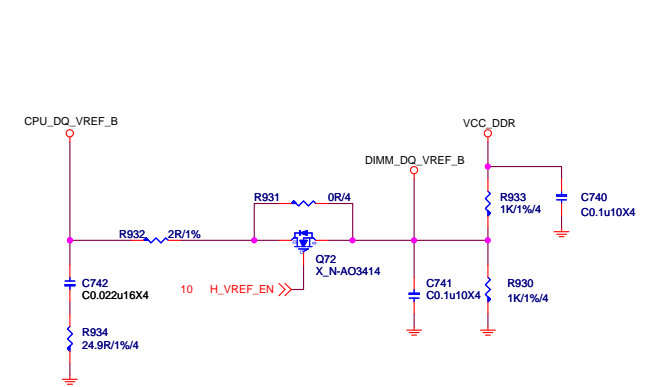
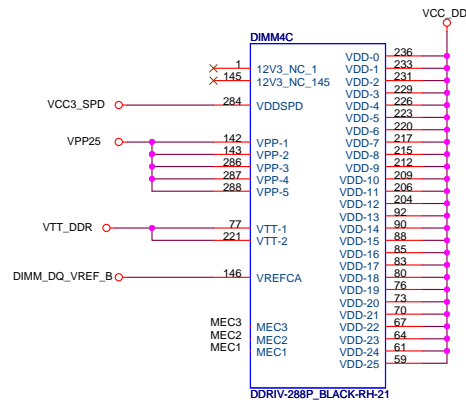
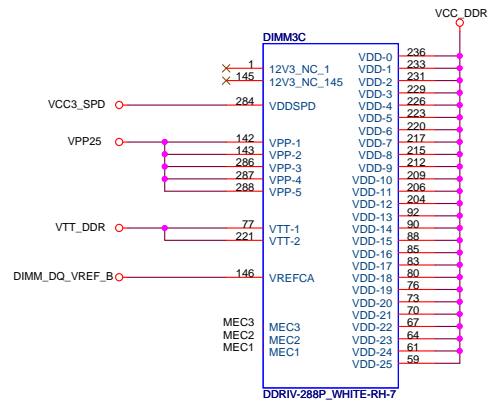
5

4

3

2

1



<https://vinafix.com/>

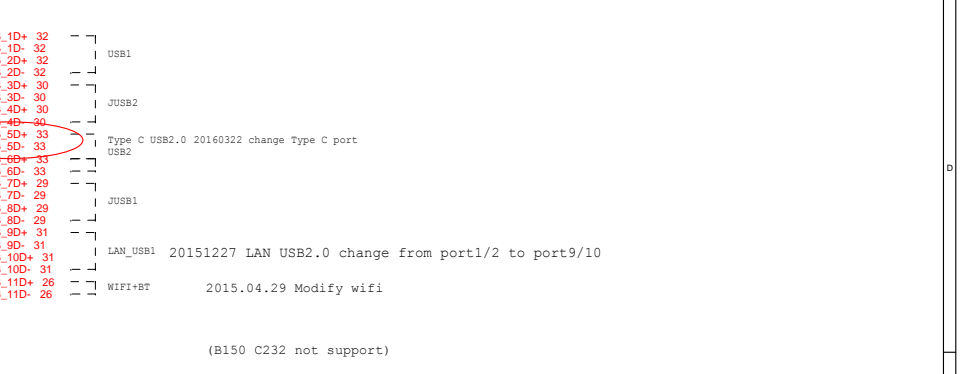
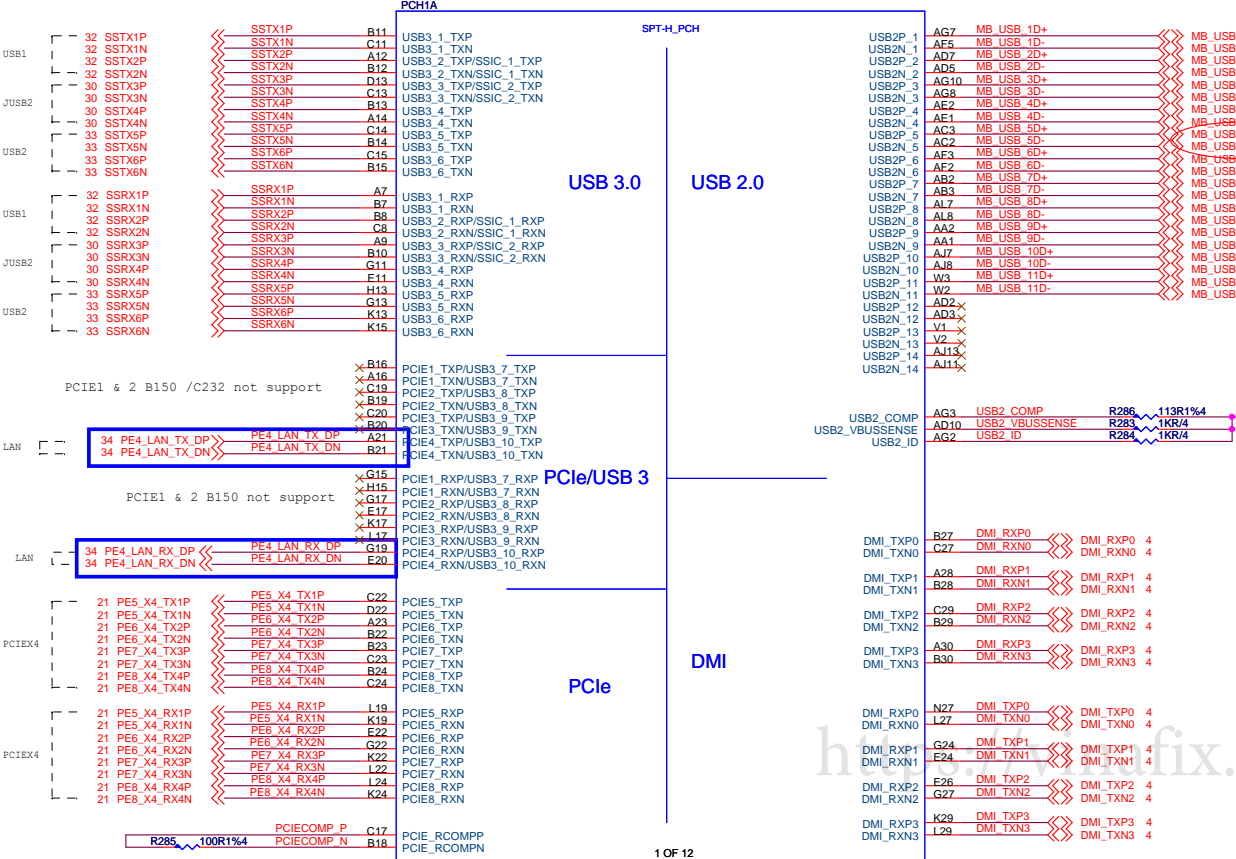


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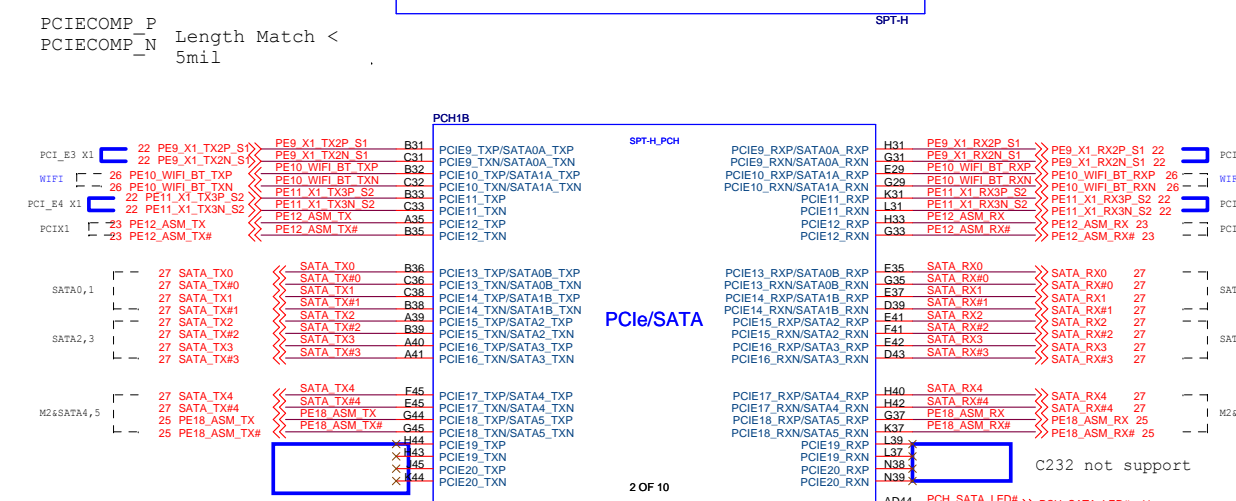
MS-7A43

Size	Document Description	Rev
Custom	DDR4-POWER/GND-2	1.1
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USB1:P1&P2 JUSB2:P3&P4 USB2:P5&P6



sku	1	2	3	4	5	6	7	8	9	10	11	12	13	14
H110	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	N/A	N/A	N/A	N/A	N/A	LAN Only	PCle/ LAN	PCle	PCle	PCle
B150	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	N/A	N/A	N/A	LAN Only	PCle/ LAN	PCle	PCle	PCle
H170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	USB3	USB3	PCle	PCle/ LAN	PCle/ LAN	PCle	PCle	PCle
Z170	USB3/ OTG	USB3/ SSIC	USB3/ SSIC	USB3	USB3	USB3	PCle	PCle	PCle	PCle/ LAN	PCle/ LAN	PCle	PCle	PCle
Sku	15	16	17	18	19	20	21	22	23	24	25	26	RST for PCIe Ports	
H110	PCle/ LAN	PCle	N/A	LAN Only	SATA*/ LAN	SATA*	SATA	SATA	N/A	N/A	N/A	N/A		0
B150	PCle/LAN	PCle/ SATA*	PCle/ LAN	PCle/ LAN	SATA*/ LAN	SATA*	SATA	SATA	SATA	SATA	N/A	N/A		0
H170	PCle/LAN	PCle/ SATA	PCle	PCle/ LAN	PCle/LAN	PCle/ SATA	PCle/ SATA	PCle/ SATA	SATA	SATA	PCle	PCle		2
Z170	SATA	SATA	PCle	LAN	SATA	SATA	SATA	SATA	SATA	SATA	PCle	PCle		3



20160111 Reserver HPD PD resistor

2015.05.05 Modify co-lay circuit to be simple.

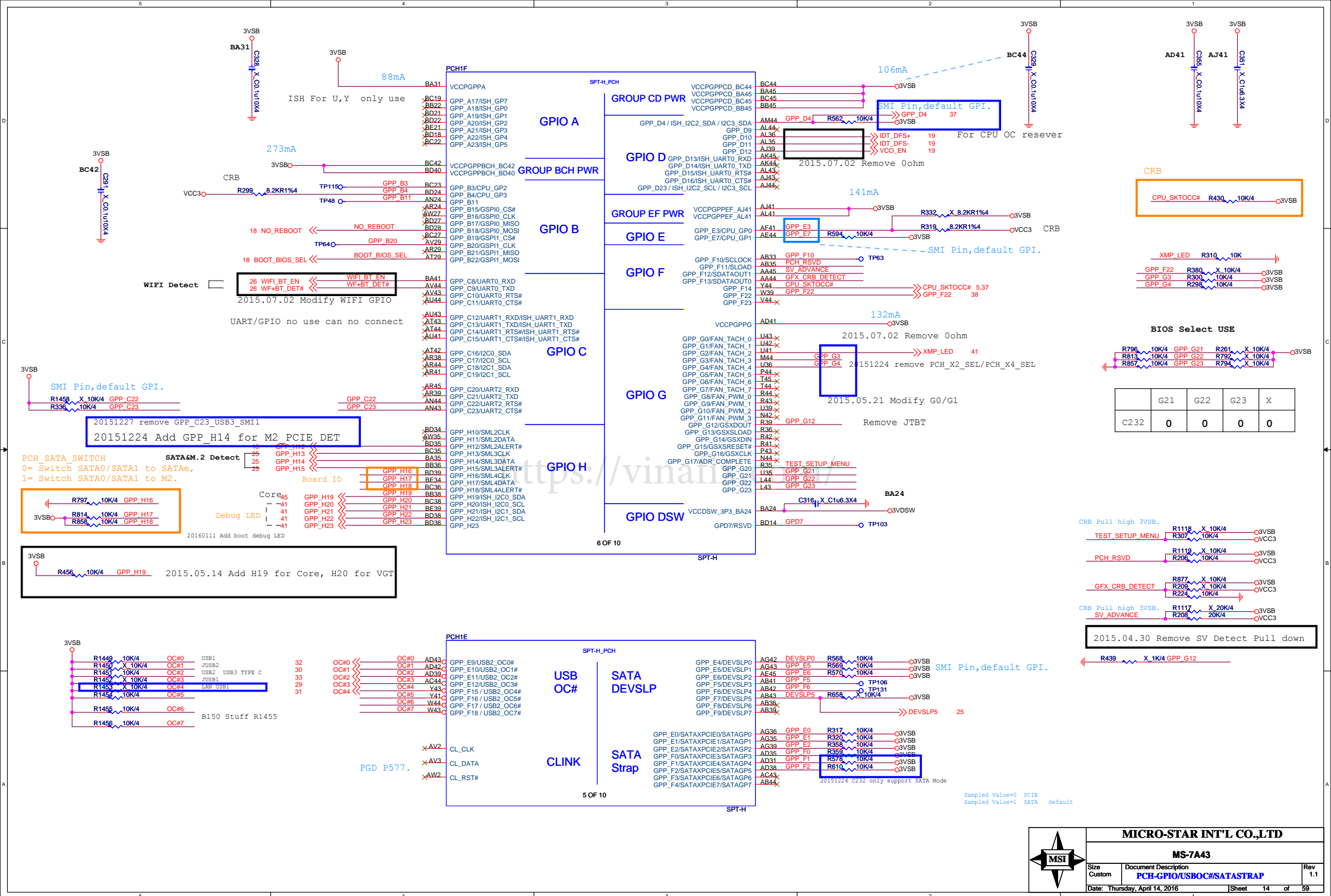
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MS-7A43

Size Custom	Document Description PCH-Audio/Display/Clock	Rev 1.1
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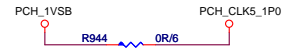


MICRO-STAR INT'L CO.,LTD

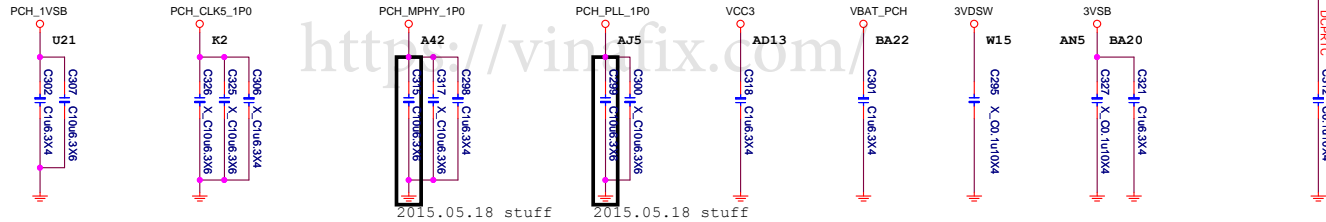
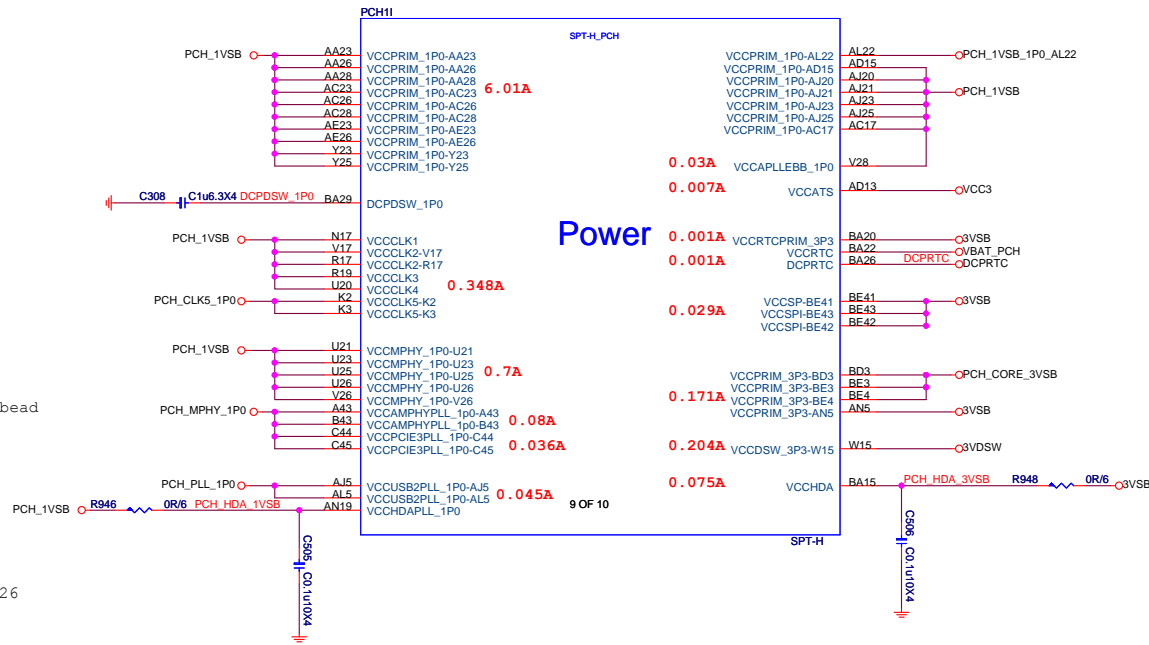
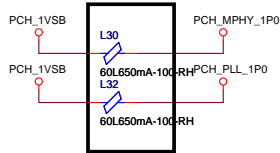
MS-7A43

Size	Document Description
Custom	PCH-GPIO/USBOC#SATASTRAP

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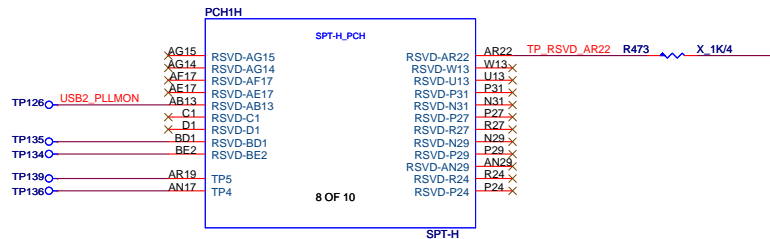
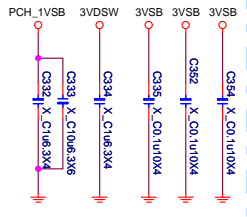
2015.05.18 Modify from 00hm to bead



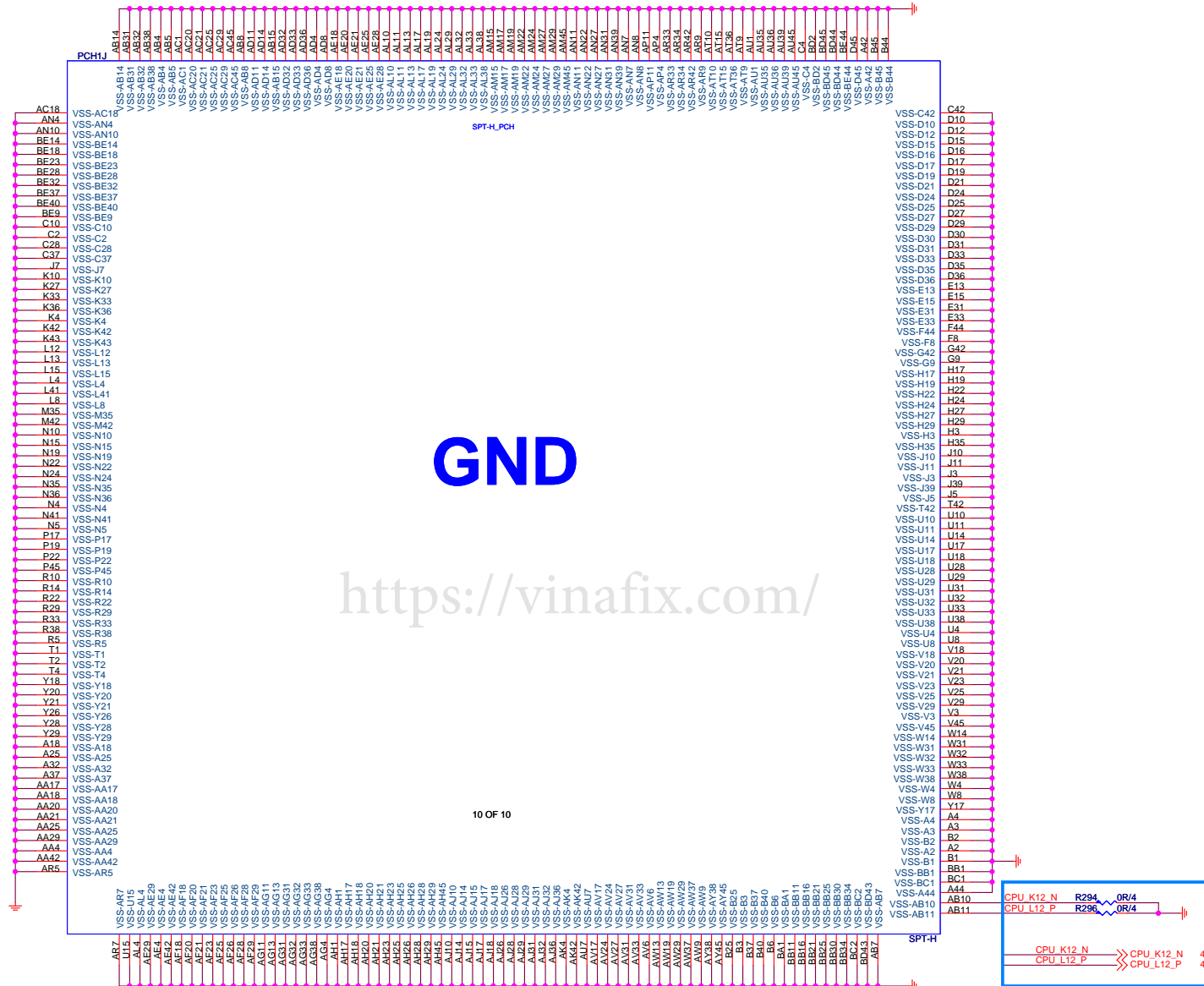
2015.05.18 stuff

2015.05.18 stuff

BOT



MICRO-STAR INT'L CO.,LTD		
MS-7A43		
Size	Document Description	Rev
Custom	PCH-Power	1.1
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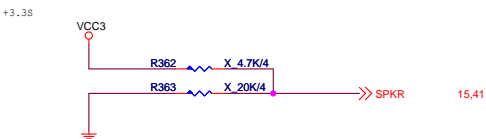


MICRO-STAR INT'L CO.,LTD

MS-7A43

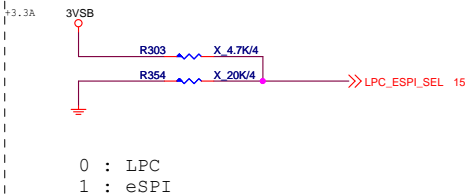
Size	Document Description	Rev
Custom	PCH-GND	1.1
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TOP Swap



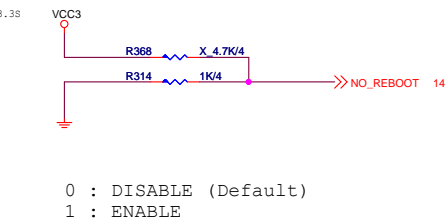
Internal pull-down is disabled after PLTRST#

LPC eSPI Mode



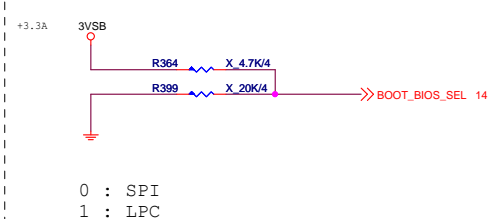
Internal pull-down is disabled after RSMRST

No Reboot



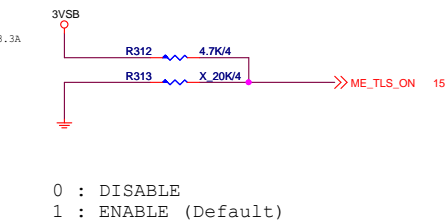
Internal pull-down is disabled after PLTRST#

Boot BIOS



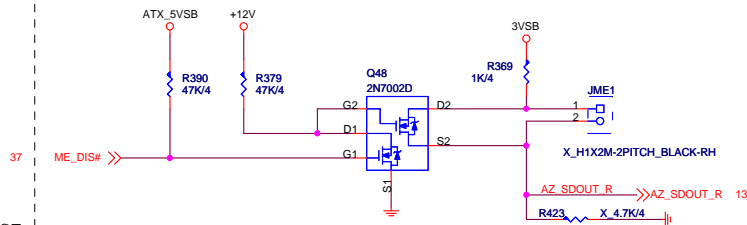
Internal pull-down is disabled after PLTRST#

AMT and SBA with confidentiality

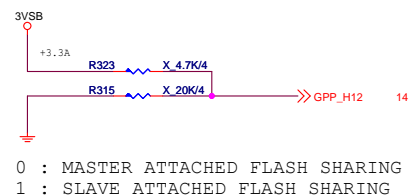


Internal pull-down is disabled after RSMRST

HDA_SDO



ESPI FLASH SHARING MODE



Internal pull-down is disabled after RSMRST

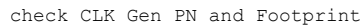
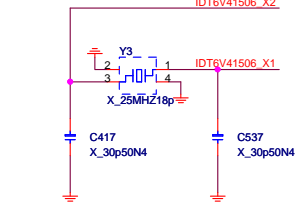
<https://vinafix.com/>



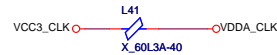
MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description PCH-Strap	Rev 1.1
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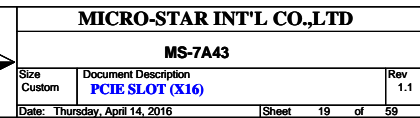
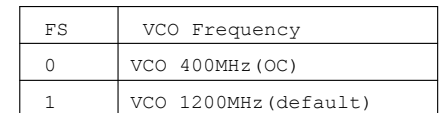
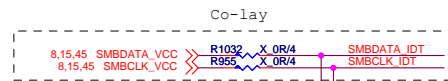
<https://vinafix.com/>



15,28,37,42,44,48,51

SLP_S3

2015.05.18 Enable add SLP

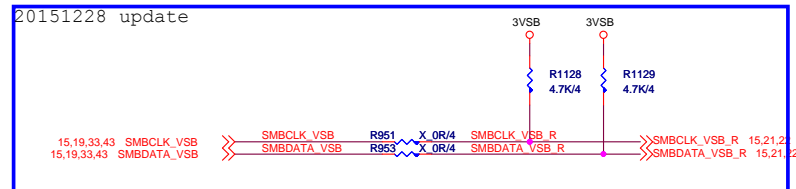


```
support max speed GEN3      Black
```



2015.05.04 Add for improve 5VDUAL Drop issue.

20151228 update



2015.04.23 Remove



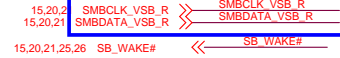
MICRO-STAR INT'L CO.,LTD

MS-7970

Size Custom	Document Description PCIE SLOT (X16)	Rev 1.1
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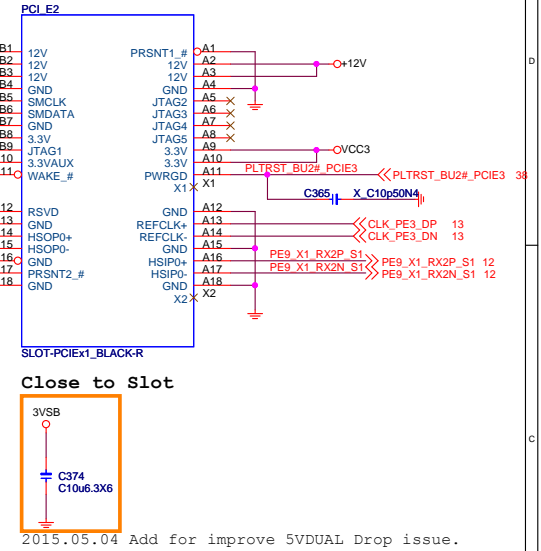
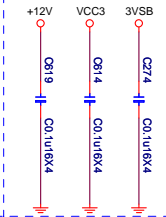
20151224 Remove PCI_E1

20151228 update



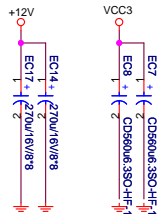
20151224 Remove PCI_E3 DET#

EMI:close pin



PCIE (X1) *2 PCIE (X4) *1 PCIE (X16) *1

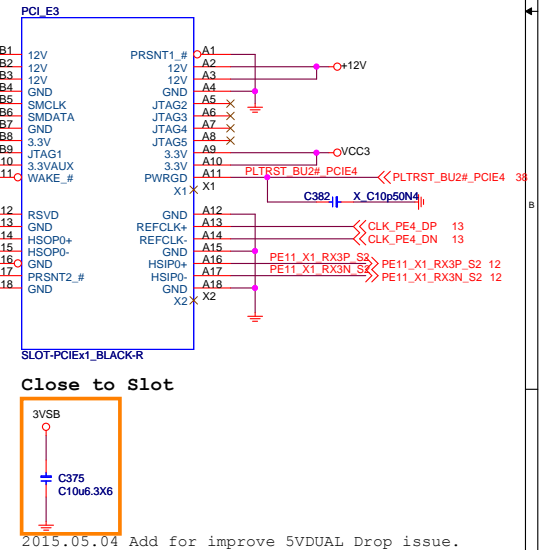
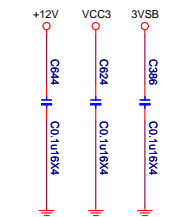
3.3Vaux: 0.375*5=1.5A (wake)
0.02*4=0.1A (no wake)
VCC3: 3*5=15A
+12V: 0.5*3+2.1+5.5=9.1A



<https://vinafix.com/>

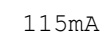
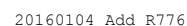
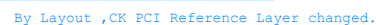
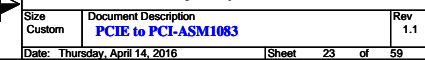
20151224 Remove PCI_E4 DET#

EMI:close pin



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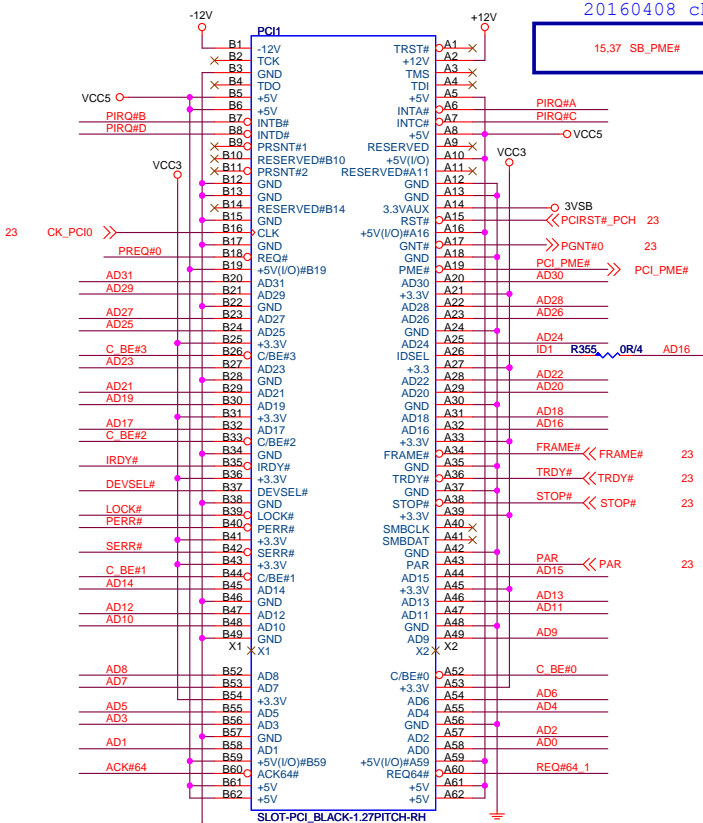
MICRO-STAR INT'L CO.,LTD			
MS-7970			
Size	Document Description		Rev
Custom	PCIE SLOT (X1)		1.1
Date:	Thursday, April 14, 2016	Sheet	22 of 59



20160408 change

15.37 SB_PME# << R956 OR/4 PCI PME#

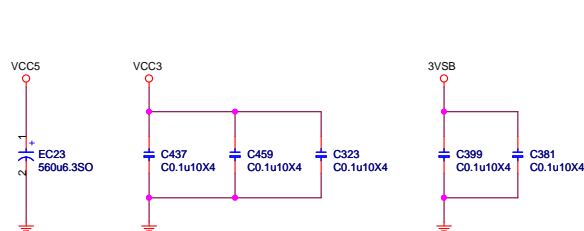
20160321 modify



IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

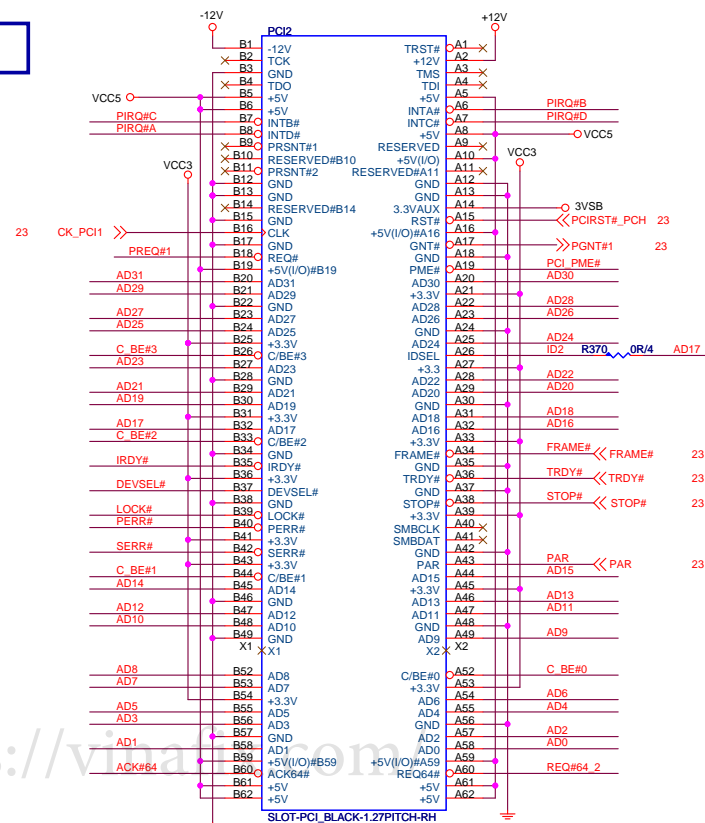
AD[31..0] <<> AD[31..0] 23
C_BE#[3..0] <<> C_BE#[3..0] 23

PCI PULL-UP / DOWN RESISTORS



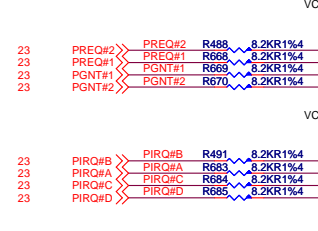
2015.04.23 Add for slot2

REQ#64 1 R431 8.2K1%4
REQ#64 2 R441 8.2K1%4
ACK#64 R432 8.2K1%4



IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

2015.04.23 Add for slot2



PREQ#2 PREQ#2 R488 8.2K1%4
PREQ#1 PREQ#1 R668 8.2K1%4
PGNT#1 PGNT#1 R669 8.2K1%4
PGNT#2 PGNT#2 R670 8.2K1%4
PIRQ#B PIRQ#B R491 8.2K1%4
PIRQ#A PIRQ#A R683 8.2K1%4
PIRQ#C PIRQ#C R684 8.2K1%4
PIRQ#D PIRQ#D R685 8.2K1%4
PREQ#0 PREQ#0 R411 8.2K1%4
PGNT#0 PGNT#0 R410 8.2K1%4

PCI slot (X3)

+3.3Vaux (wake) - 1125mA
+3.3Vaux (no wake) - 60mA

+3.3V - 7.6A

+5V - 15A

+12V - 1.5A

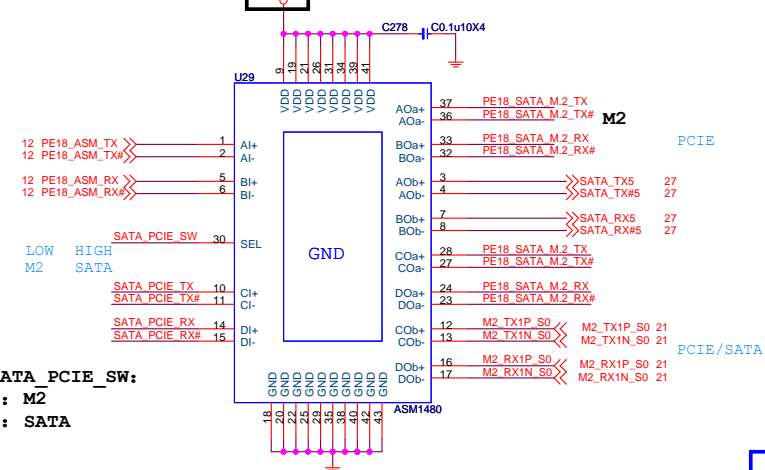


MICRO-STAR INT'L CO.,LTD

MS-7A43

Size	Document Description	Rev
Custom	PCI SLOT	1.1
Date: Thursday, April 14, 2016	Sheet 24 of 59	

2015.07.02 Change power source



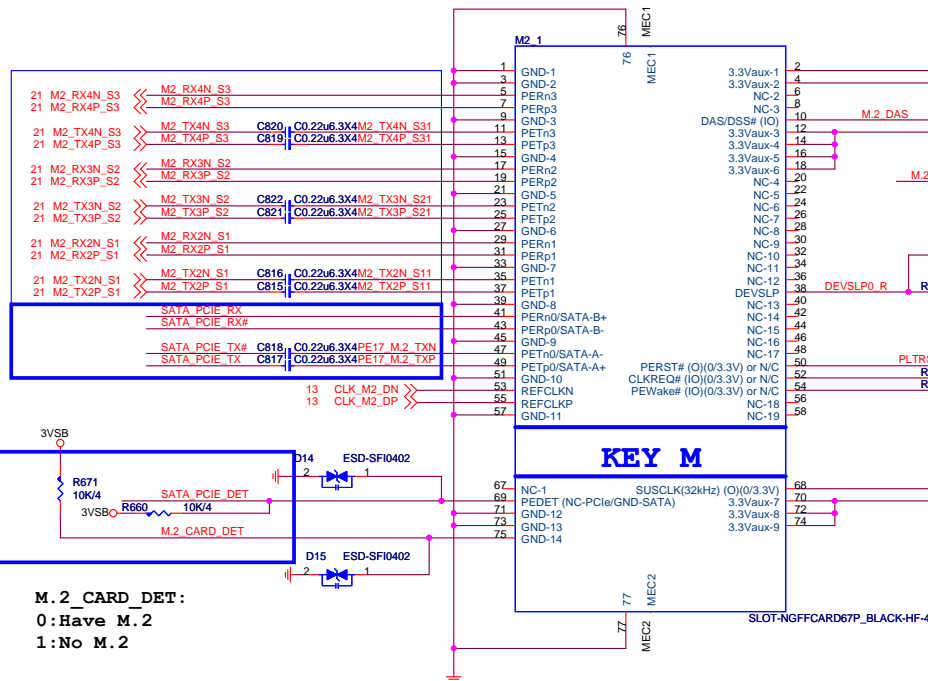
SATA_PCIE_SW:
0: M2
1: SATA

Truth Table

SEL	L	H
Function	IN+ to out+	IN+ to out+
Function	IN+ to out+	IN+ to out+

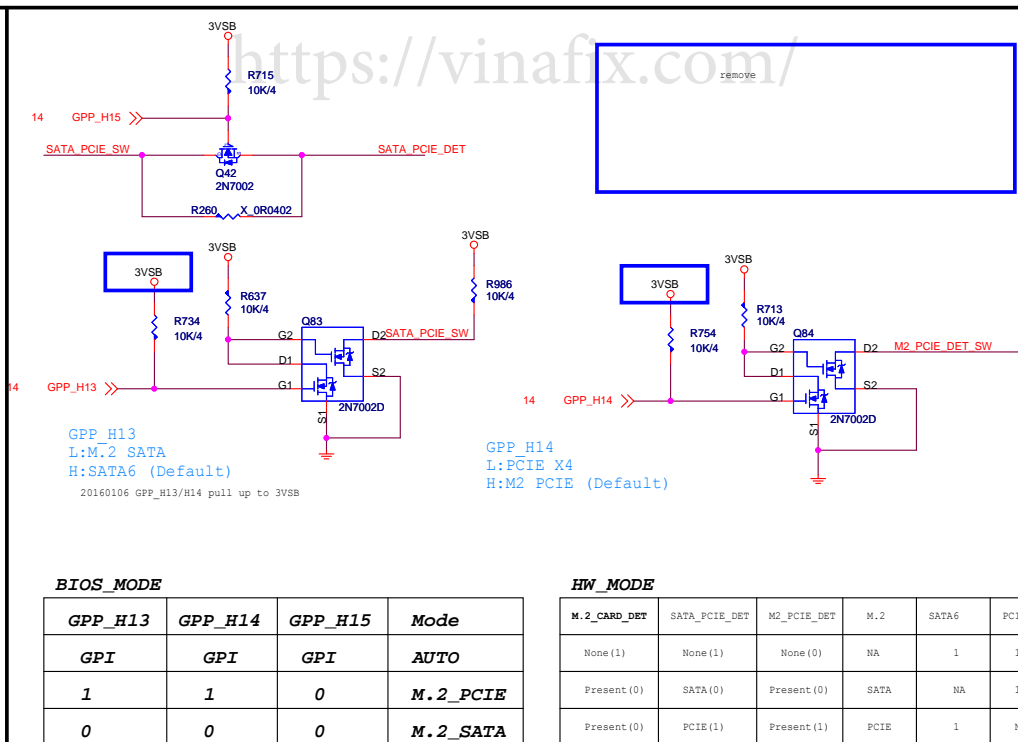
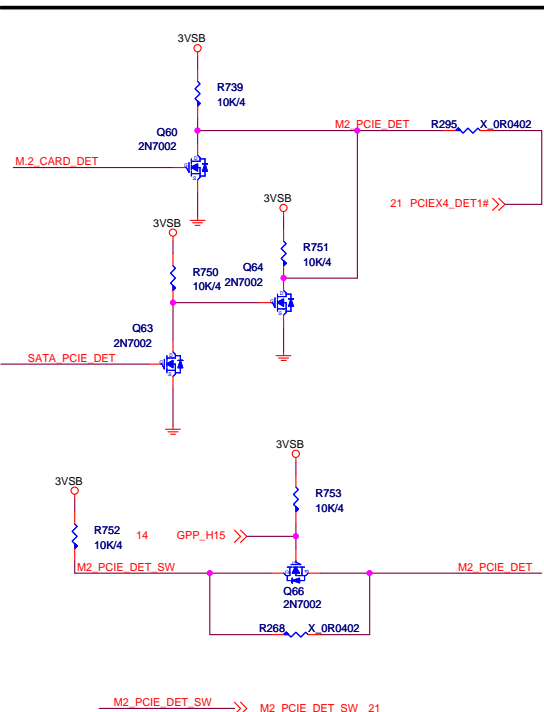
2015.07.02
Remove PU to M2_VCC3

SATA_PCIE_DET:
0: SATA
1: PCIE



BIOS_MODE

M2_2_GPP5	M2_2_GPP7	Mode
0	0	M2-SATA
1	0	M2-PCIE
GPI	1	AUTO



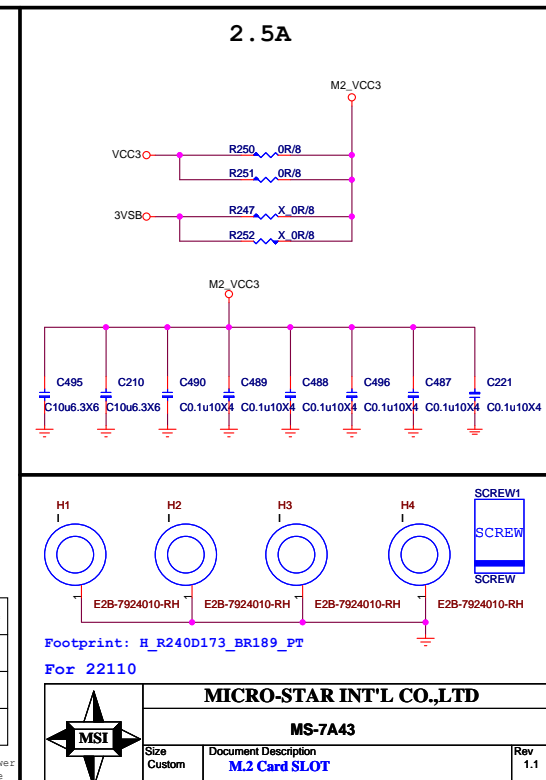
BIOS_MODE

GPP_H13	GPP_H14	GPP_H15	Mode
GPI	GPI	GPI	AUTO
1	1	0	M.2_PCIE
0	0	0	M.2_SATA

HW_MODE

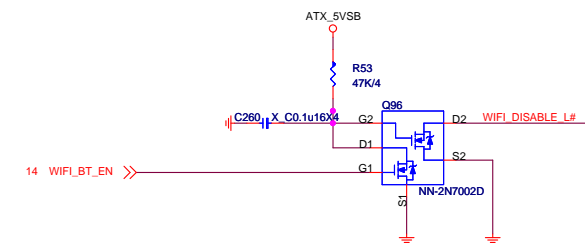
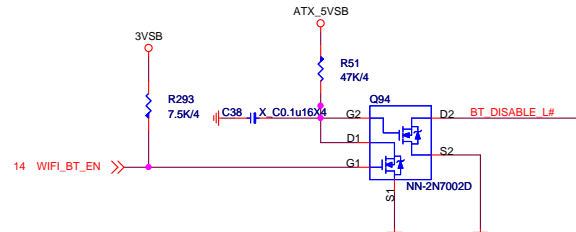
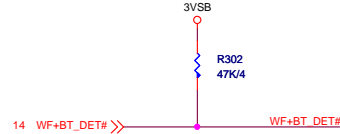
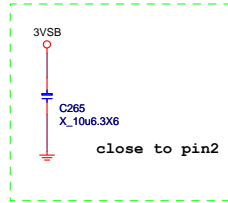
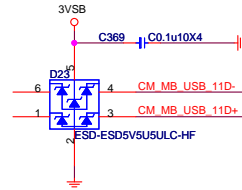
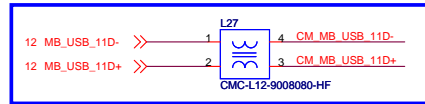
M.2_CARD_DET	SATA_PCIE_DET	M2_PCIE_DET	M.2	SATA6	PCIE_X4
None(1)	None(1)	None(0)	NA	1	1
Present(0)	SATA(0)	Present(0)	SATA	NA	1
Present(0)	PCIE(1)	Present(1)	PCIE	1	NA

SATA5GP
for chipset that main power, if pull up to VSB maybe will leakage power
if sampled value = 1, select SATA; if sampled value = 0, select PCIE

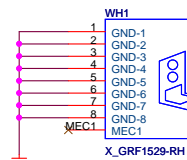
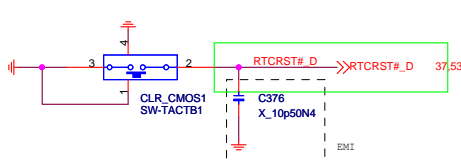


Footprint: H_R240D173_BR189_PT
For 22110

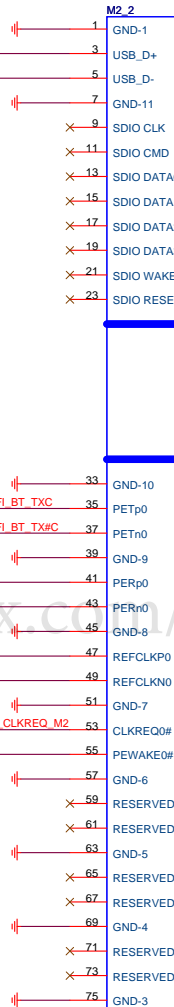
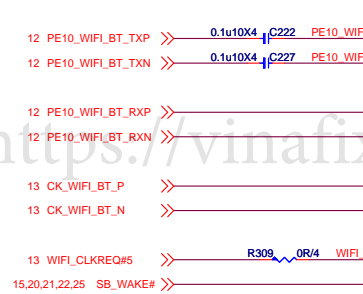
MICRO-STAR INT'L CO.,LTD		
MS-7A43		
Size	Document Description	Rev
Custom	M.2 Card SLOT	1.1
Date: Thursday, April 14, 2016	Sheet 25 of 59	



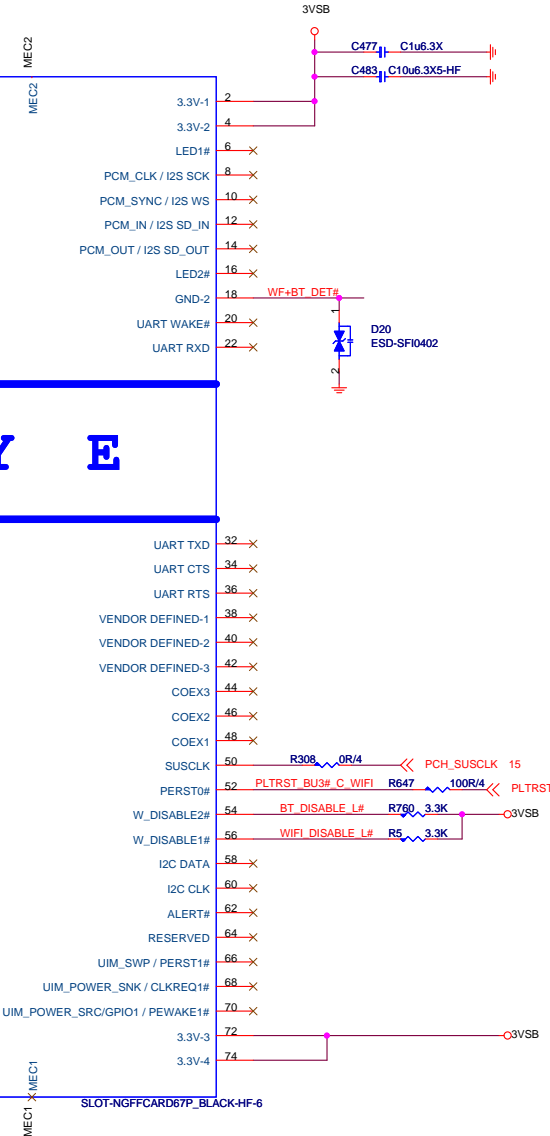
Clear CMOS Button



<https://vinafix.com/>



KEY E

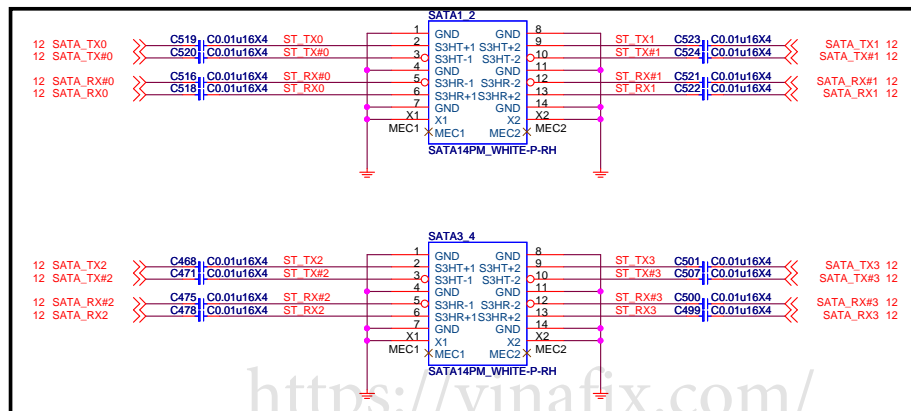


MSI			
MICRO-STAR INT'L CO.,LTD			
MS-7A43			
Size	Document Description	Rev	
Custom	Board LED	1.1	
Date: Thursday, April 14, 2016		Sheet 26 of 59	

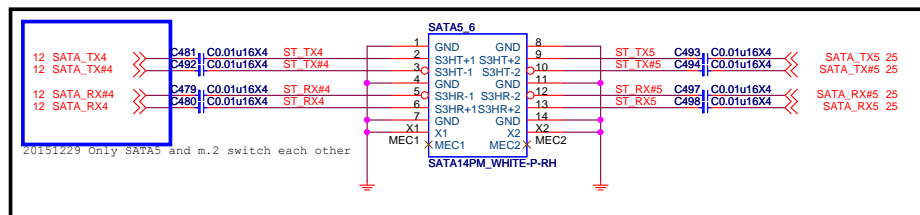
2015.05.12 Remove SE Re-Driver

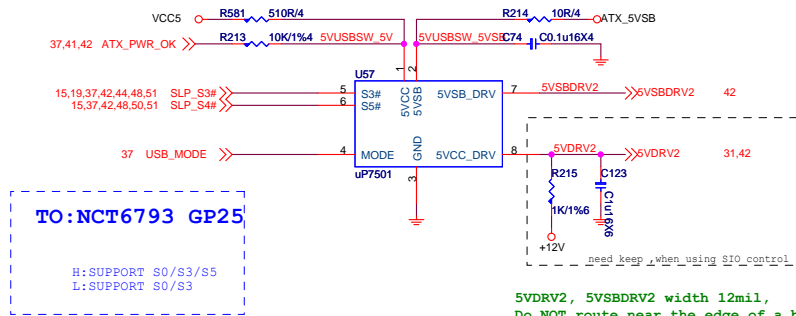
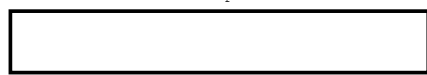
2015.07.02 Remove SE connector

2015.07.02 Modify SPEC

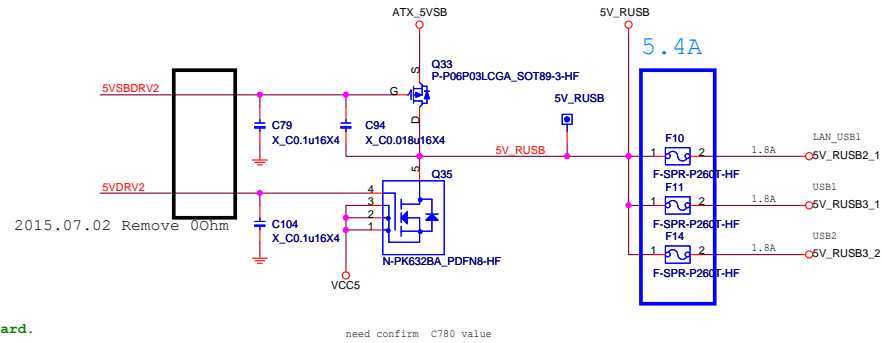


2015.05.13 Change to 90 degree





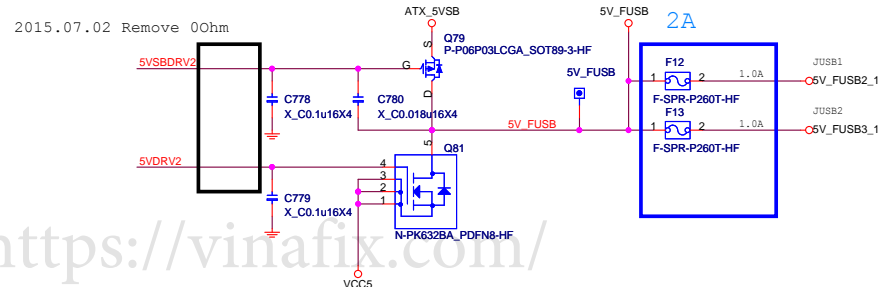
5VSDRV2, 5VSBDRV2 width 12mil,
Do NOT route near the edge of a board.



P-MOS
D03-06P0319-N03

N-MOS
D03-510BA0C-N03
D03-3056M00-U47
D03-4C05N03-O05
D03-3830D09-N47
D03-632BA0C-N03

D08-2000300-P16 (Itrip=3.5A; 0.003ohm)
D08-0300700-P16 (Itrip=2.6A; 0.015ohm)



Front USB2.0 Voltage Drop Fail.

<https://vinafix.com/>



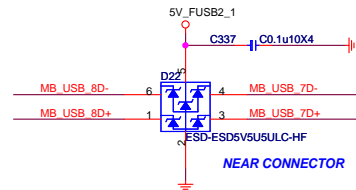
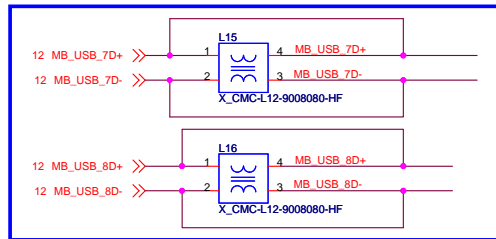
MICRO-STAR INT'L CO.,LTD

MS-7A43

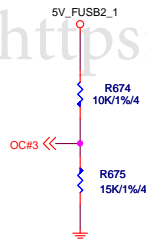
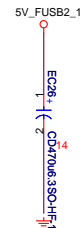
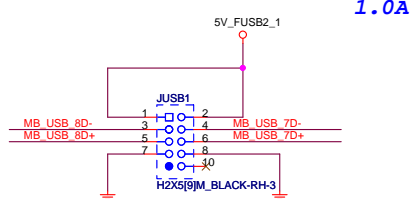
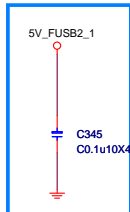
Size	Document Description	Rev
Custom	USB POWER-MP1495/UP7501	1.1
Date: Thursday, April 14, 2016	Sheet 28 of 59	

FRONT USB PORT 7,8

20160401 Short CMC

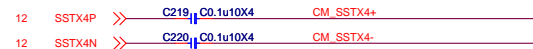
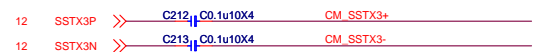
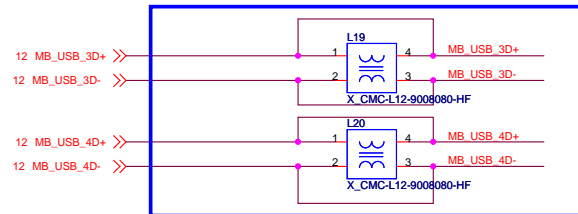


EMI Cap near Connector.

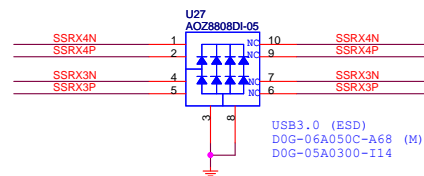
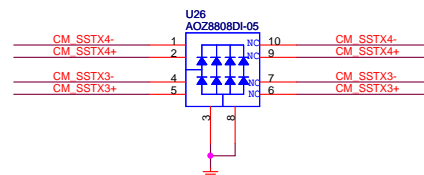
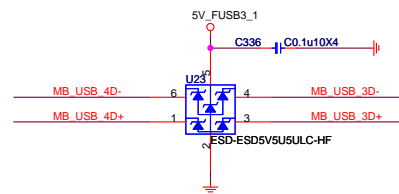


Vinafix.com

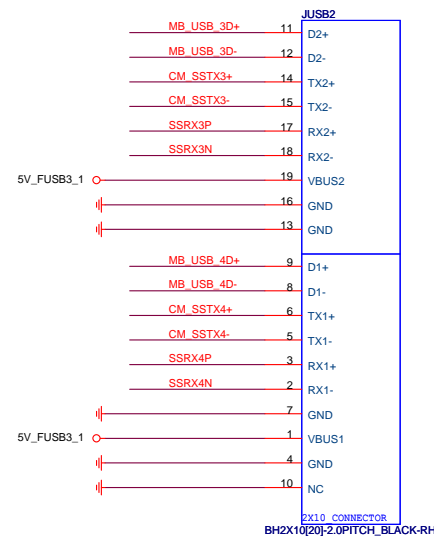
<https://vinafix.com/>



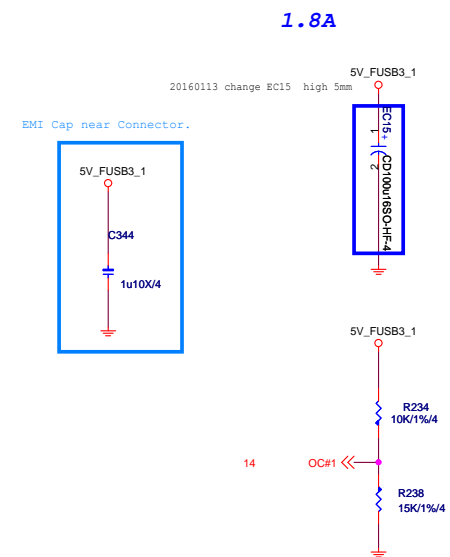
20160401 Short USB2.0 CMC remove USB3.0 CMC



USB3.0 (ESD)
D0G-06A050C-A68 (M)
D0G-05A0300-I14



FRONT USB PORT 13,14 1.8A



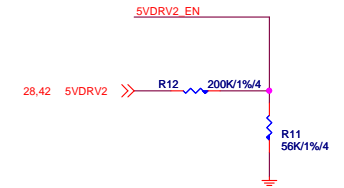
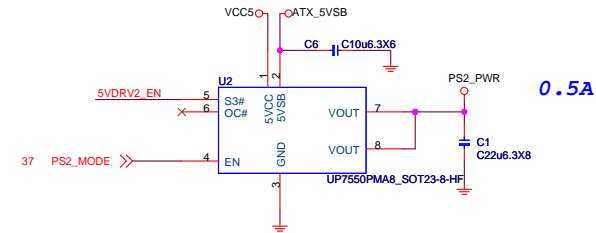
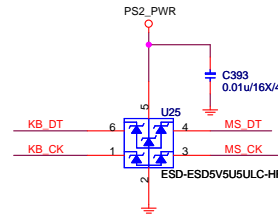
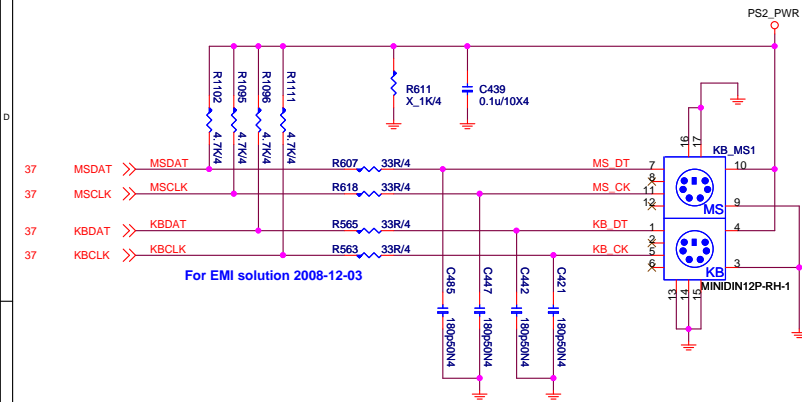
<https://vinafix.com/>

PS2 KEYBOARD & MOUSE CONNECTOR

20151226 change PS2

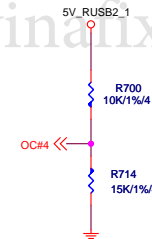
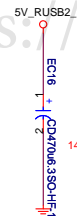
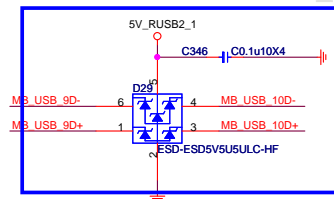
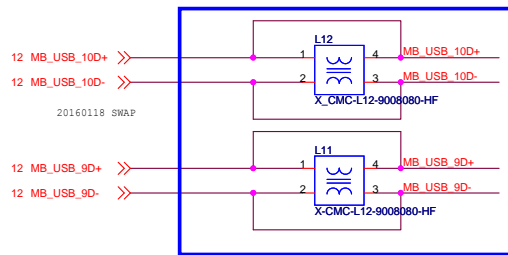
PS2 Power

USB MODE

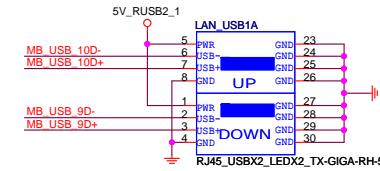
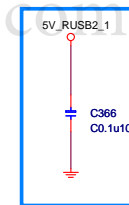


LAN USB2.0

20160401 Short USB2.0 CMC



EMI Cap near Connector.



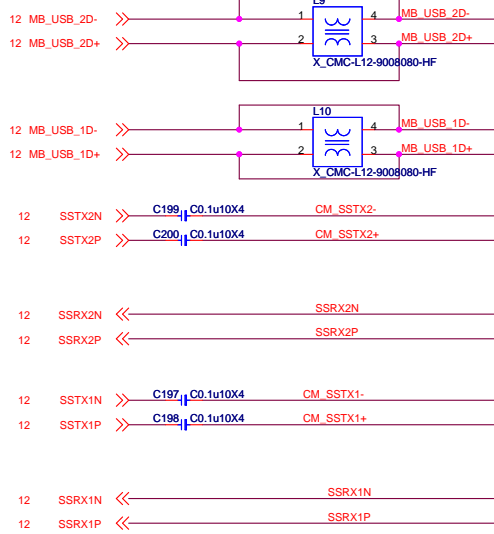
1.0A



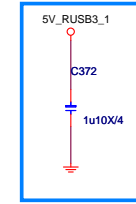
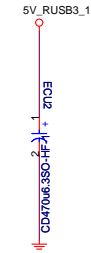
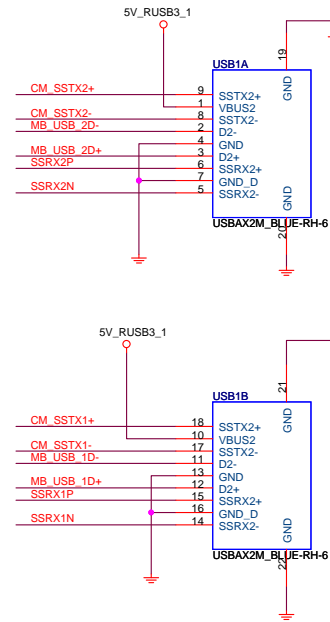
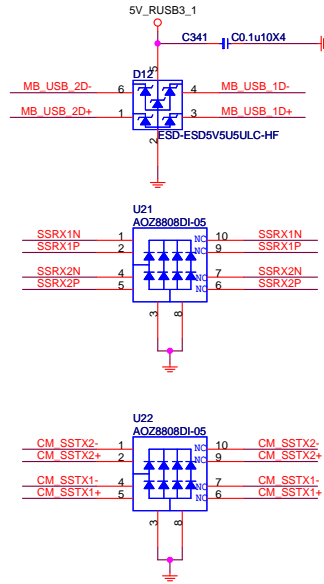
MICRO-STAR INT'L CO.,LTD

MS-7A43

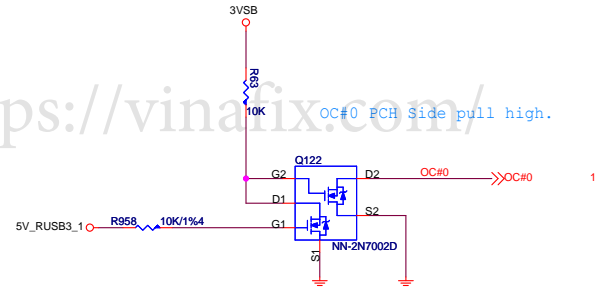
Size	Document Description	Rev
Custom	Rear I/O PS2/LAN_USB1	1.1
Date:	Thursday, April 14, 2016	Sheet 31 of 59



USB3.0 (ESD)
 D0G-06A050C-A68 (M)
 D0G-05A0300-I14



<https://vinafix.com/> OC#0 PCH Side pull high.



Vinafix.com

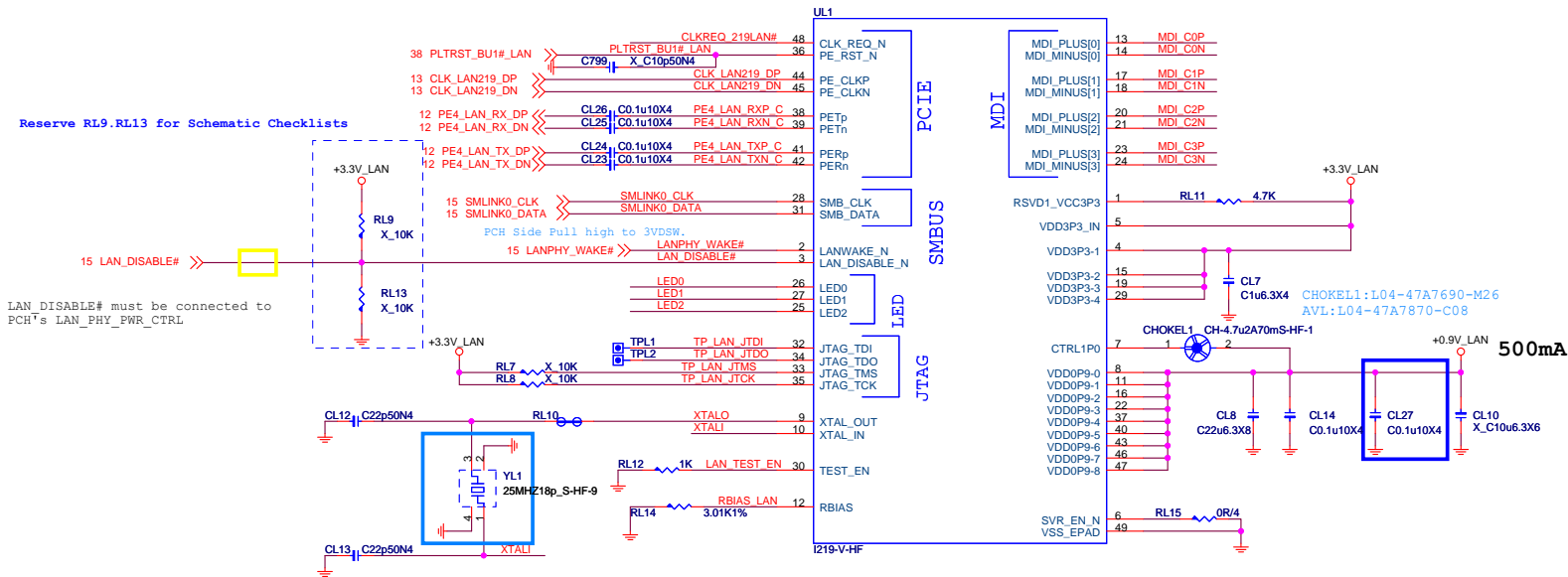


MICRO-STAR INT'L CO.,LTD

MS-7A43

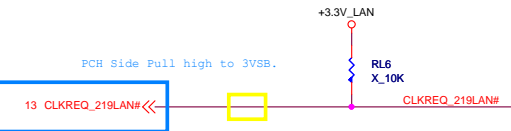
Size	Document Description	Rev
Custom	Real I/O USB3	1.1
Date:	Thursday, April 14, 2016	Sheet 32 of 59

Intel I219V / I218V PHY



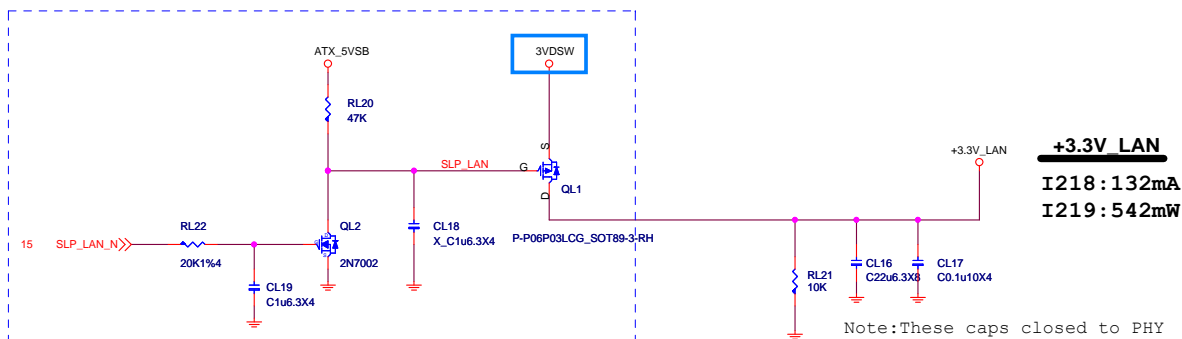
LAN_DISABLE# must be connected to PCH's LAN_PHY_PWR_CTRL

PCH's PCIECLKRQ<n> port must be mapped to PCH's PET/R<n+1>port. If CLK_REQ_N is not used, pin48 is pulled up 10K to 3.3V_LAN



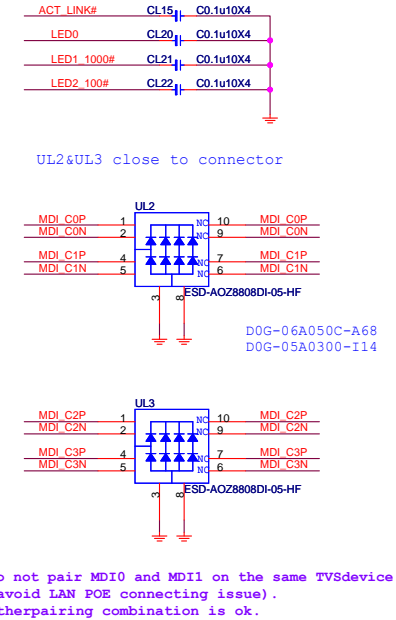
The 10Kohm pull-up resistor (RL18) of CLK_REQ_N is connected to 3.3V Suspend/Core/etc. power well, depending on the power well of PCH's input PCIECLKRQ<n> buffer.

support WOL from Deep Sx:
Power source from 3VA (DSW power) & make sure MAX current is enough to support i218/i219.



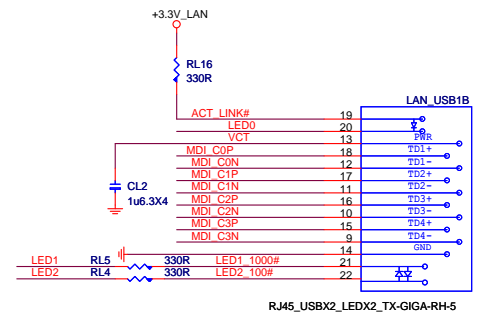
Note: These caps closed to PHY

For EMI



Do not pair MDI0 and MDI1 on the same TVS device (avoid LAN POE connecting issue). Other pairing combination is ok.

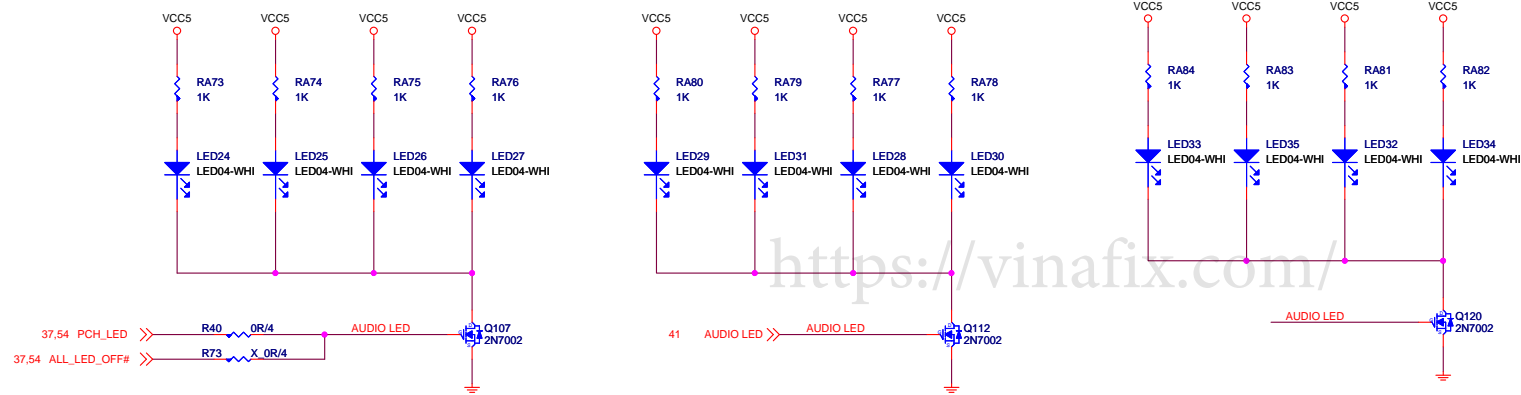
LAN Connector



RJ45_USBX2_LEDX2_TX-GIGA-RH-5

MICRO-STAR INT'L CO.,LTD			
MS-7A43			
Size	Document Description	Rev	
Custom	LAN - I219V/I218V PHY	1.1	
Date:	Thursday, April 14, 2016	Sheet	34 of 59

AUDIO LINE LED



MICRO-STAR INT'L CO.,LTD

MS-7A43

Size Custom	Document Description AUDIO LED	Rev 1.1
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Date: Thursday, April 14, 2016 1 Sheet 35 of 59

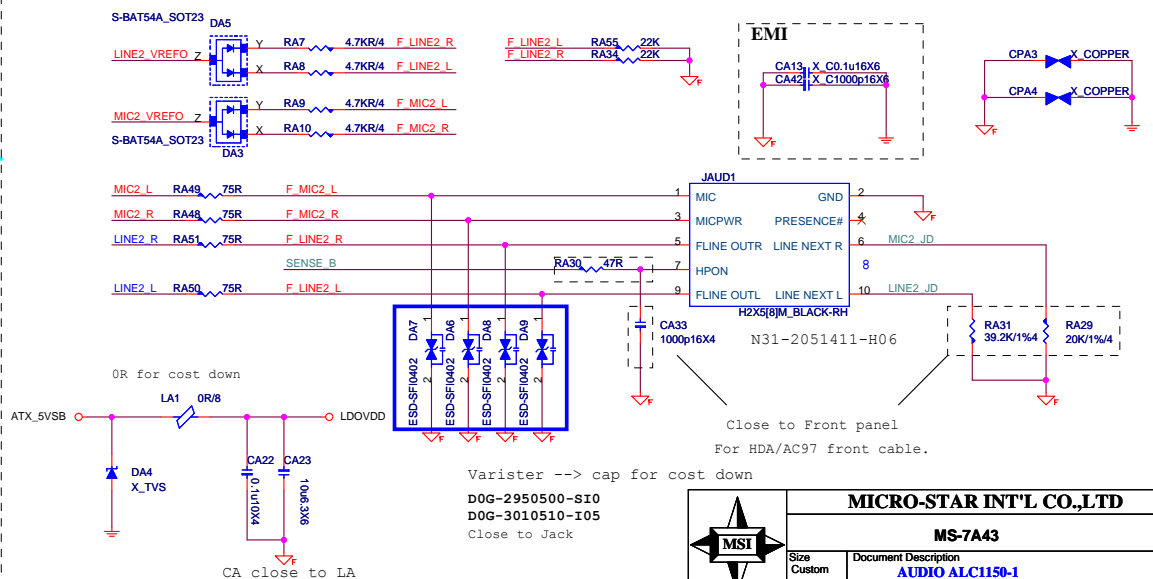
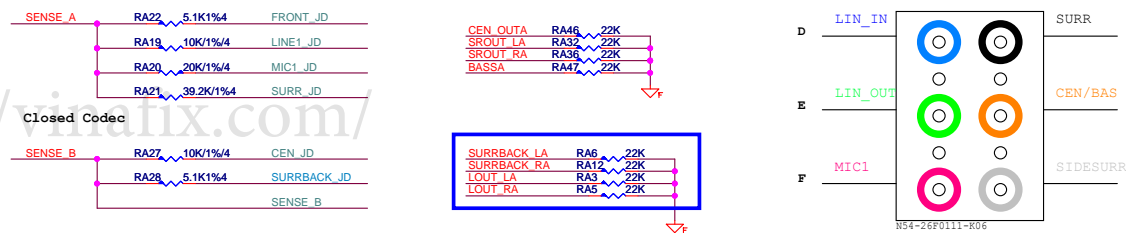
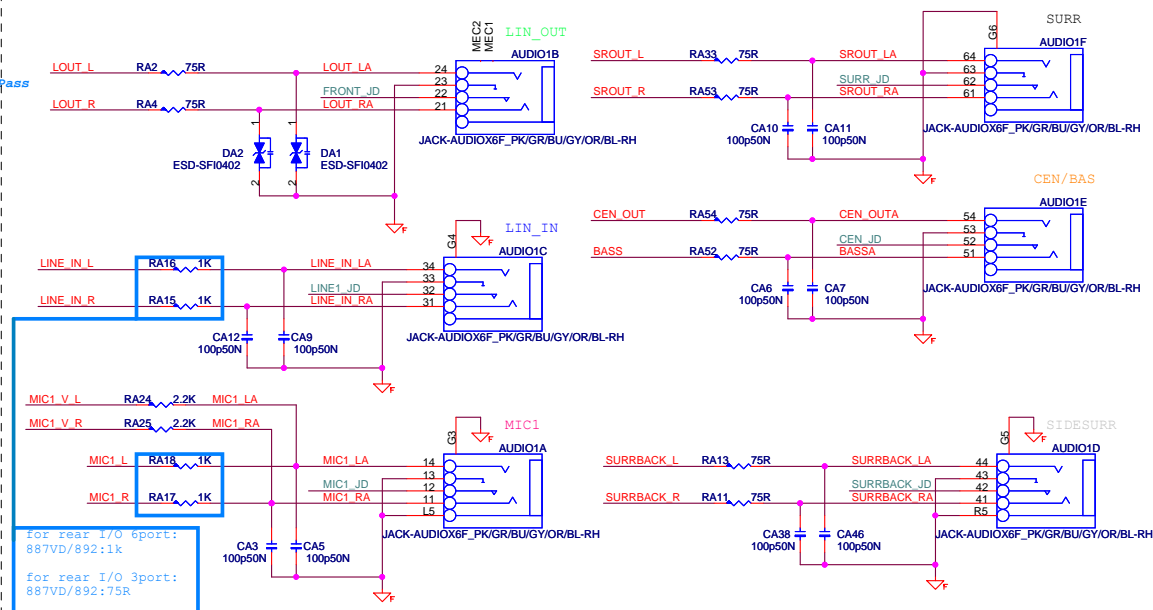
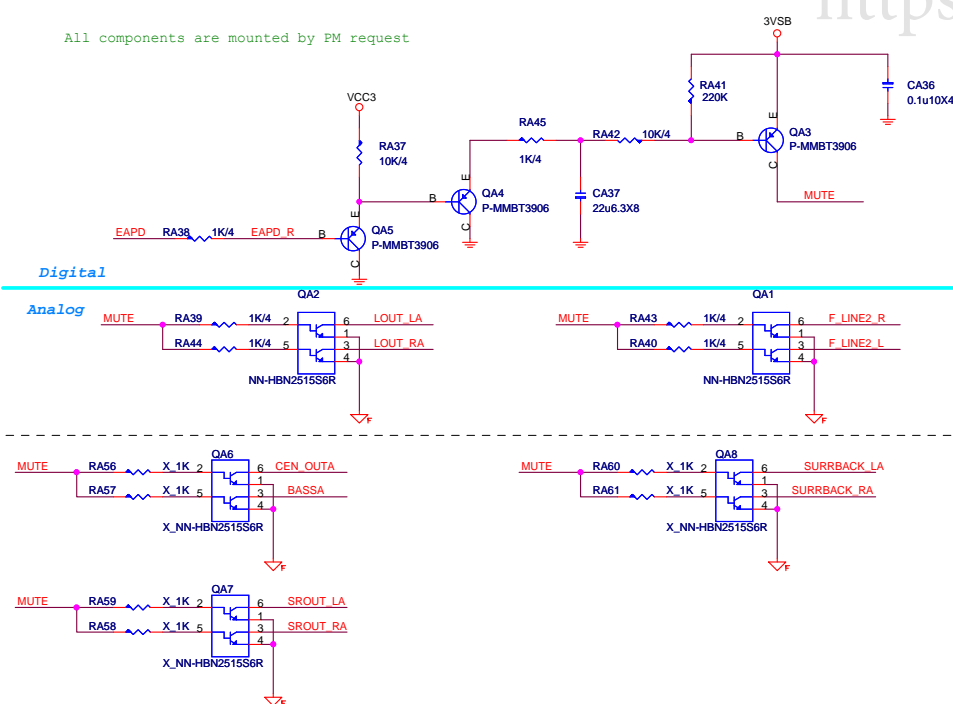
2015.04.24 Modify from
ALC1150 to ALC892

The schematic diagram illustrates the connection of the ALC892-CG-RH audio codec to the AD1975B and AD1975C ICs. Key components and connections include:

- Capacitors:** CA29 (X_0.1p50N4), CA30 (10u6.3X6), CA26 (X_0.1u16X4), CA28 (10u6.3X6), and RA35 (20K/1%4).
- Resistors:** RA23 (22R/4) and RA26 (0R/4).
- Signal Lines:** SDIN0, SDOUT0, SYNC, RESET#, BITCLK, REGREF, SENSE A/B, MIC1 V R, MIC2 VREF0, MIC1 V L, MIC2 VREF0, LINE2 VREF0, VREF AUDIO, BEEP, DVS, AVSS1, and AVSS2.
- ICs:** AD1975B (left) and AD1975C (right).
- Other Labels:** "Closed Codec", "45.8mA", "LDOVDD", "JREF", "BEEP", "DVS", "AVSS1", "AVSS2", and "ALC892-CG-RH".

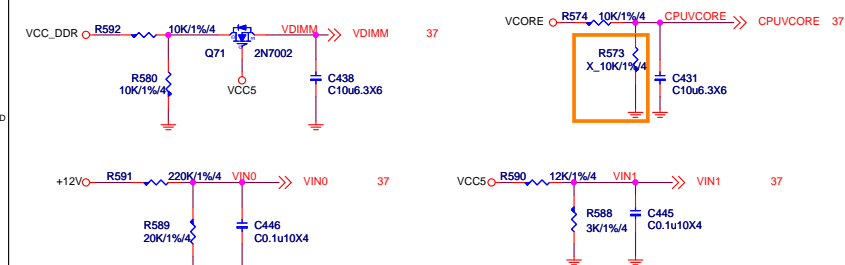
(reserve de-pop circuit for Rear Line out & Front Headphone out)

All components are mounted by PM request

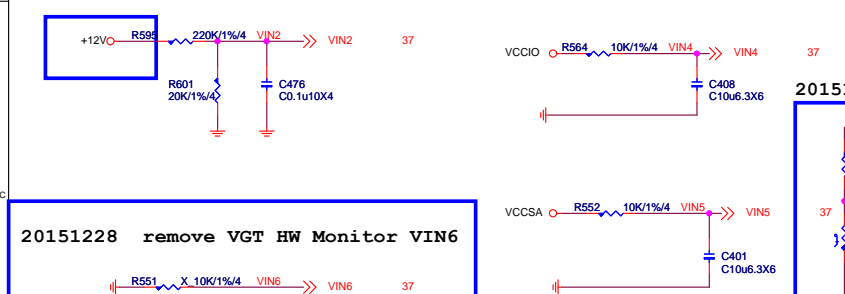


HW Monitor - Voltage

SIO HM Voltage voer 2V will not detect



20151228 update



151228 remove VGT HW Monitor VIN6

Thermal Monitor

2015.07.02
Remove Thermistor.



20160114 remove
MSI_LED

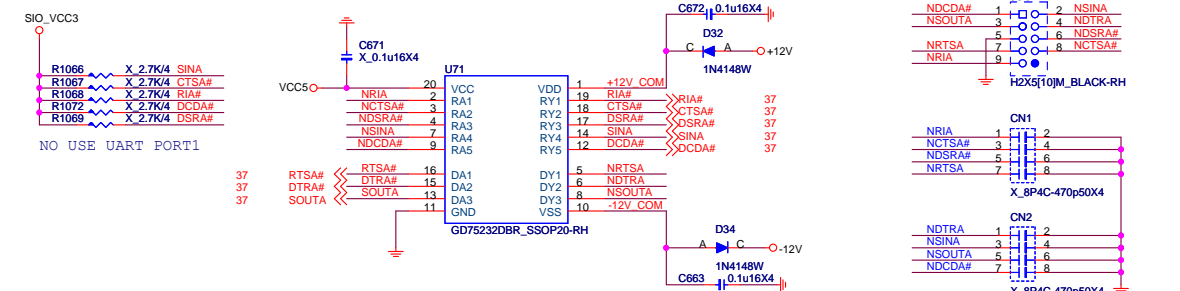
```
20151227 remove ASM1142 reset
```

2015.07.02
Remove SATA Express reset.

20151224 Remove PLTRST BU#2 PCIE1

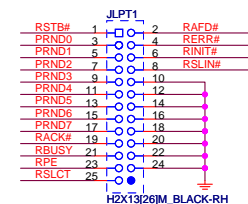
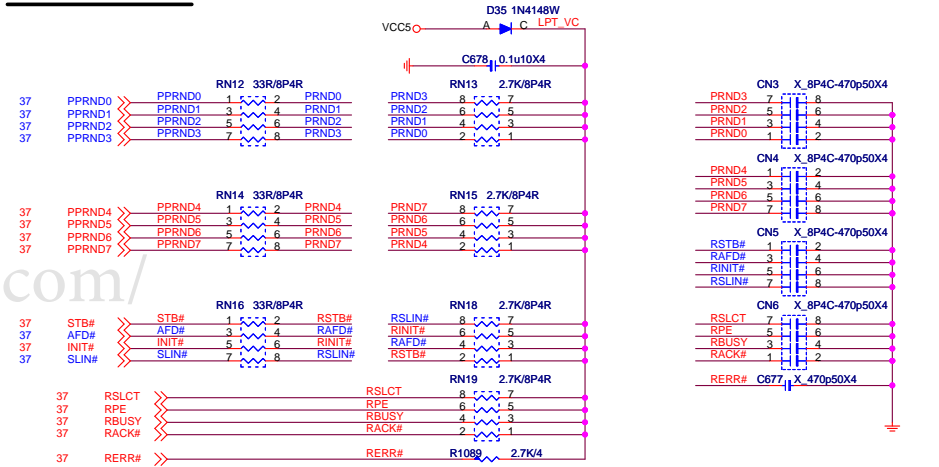
SERIAL PORT 1

2015.04.24 Add



PARALLAL PORT 2015.04.24 Add

T 2015.04.24 Add



N31-2131151-H06 : 2.0mm
N31-2131131-H06 : 2.54mm



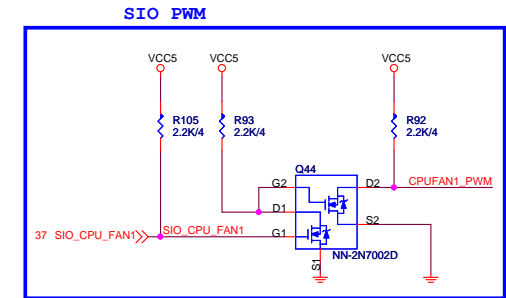
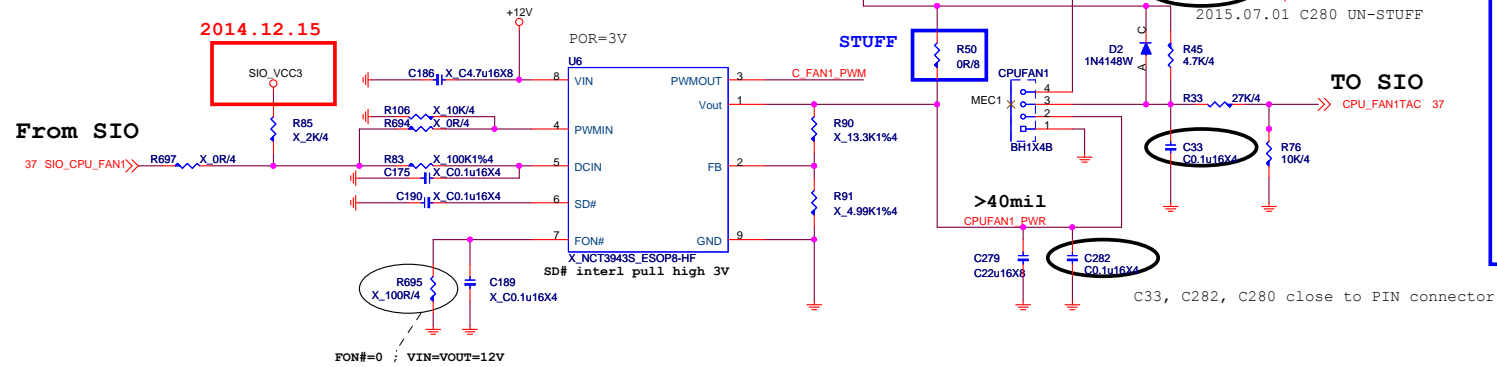
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Size Custom	Document Description SIO-NTC6792D-2	Rev 1.1
Date: Thursday, April 14, 2016		Sheet 38 of 59

CPUFAN

Vinafix.com



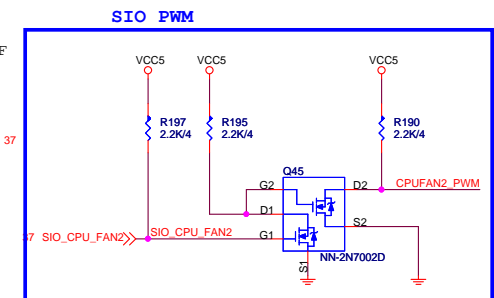
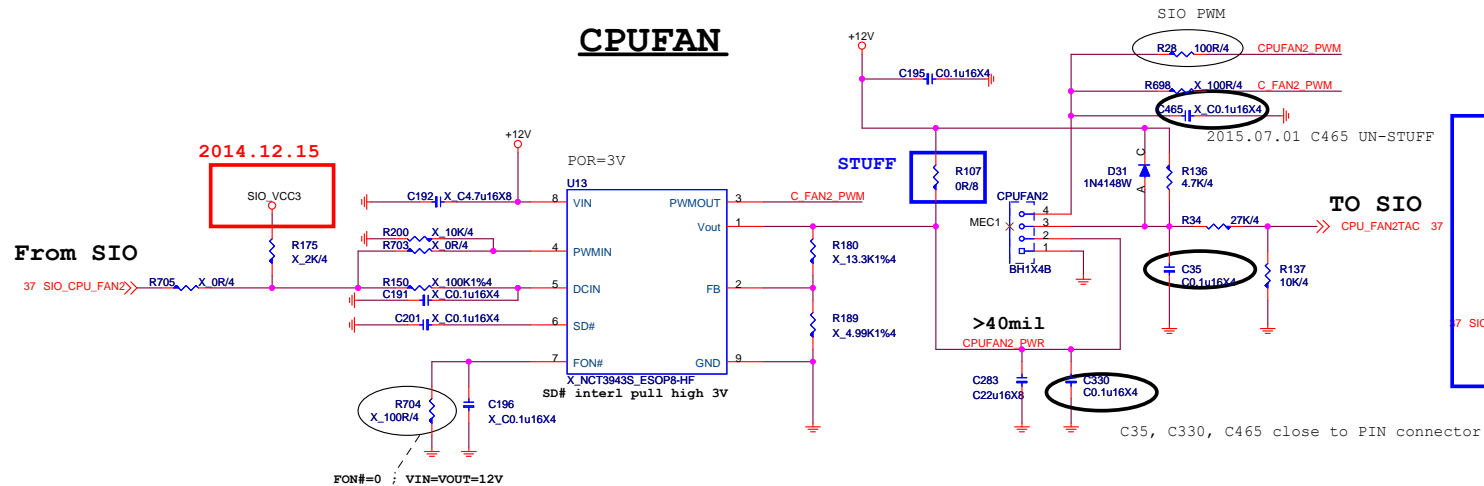
WITHOUT CUT POWER

[illegible]

<https://vinafix.com/>

Type G : 4 PIN CPU FAN USE SIO PWM (Reserve NCT3943S & WITHOUT CUT POWER)

CPUFAN



C35, C330, C465 close to PIN connector

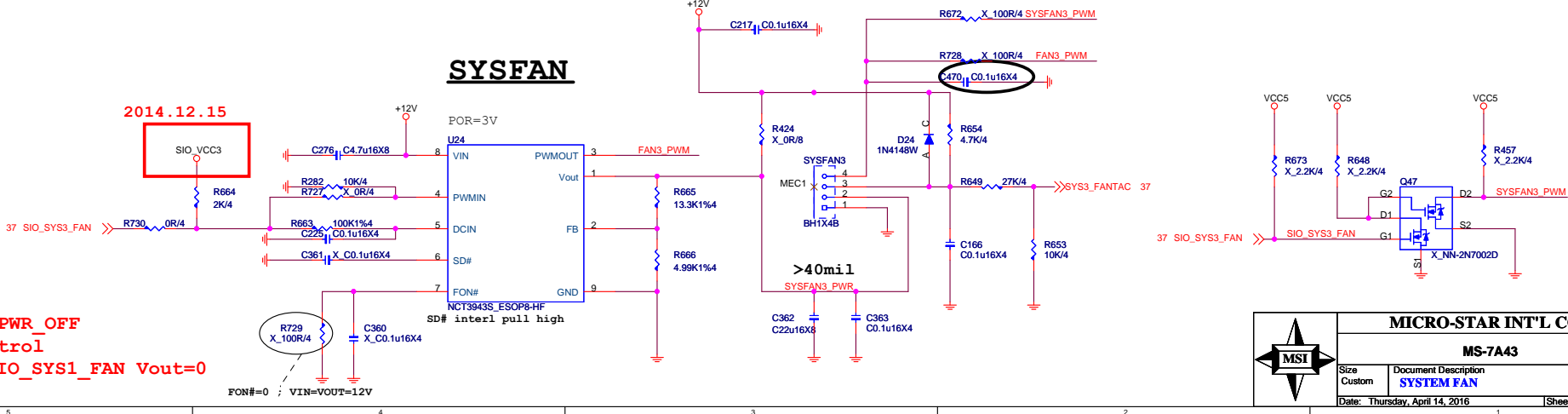
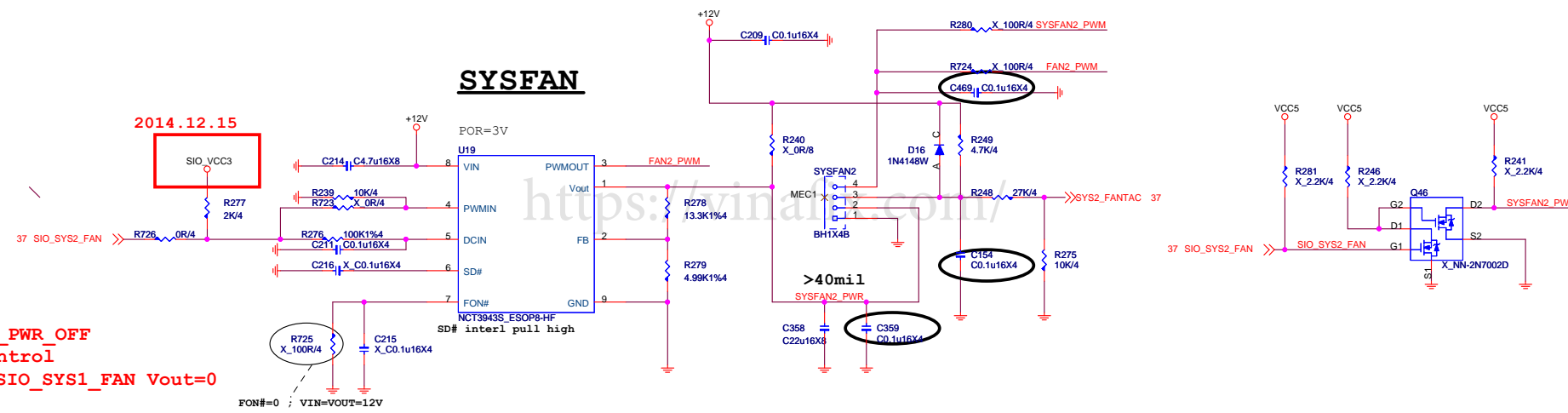
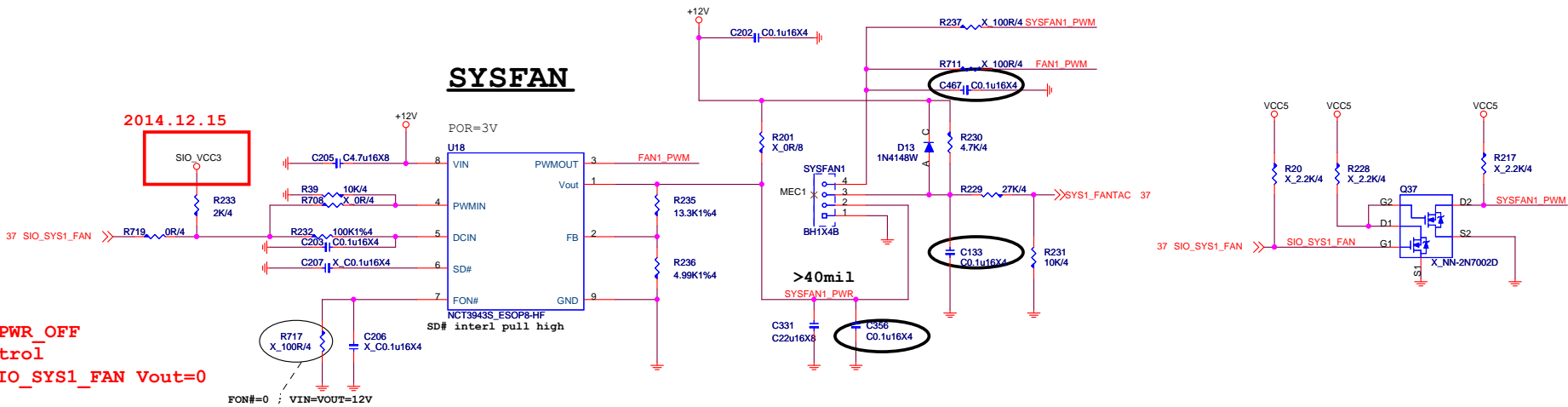


MICRO-STAR INT'L CO.,LTD

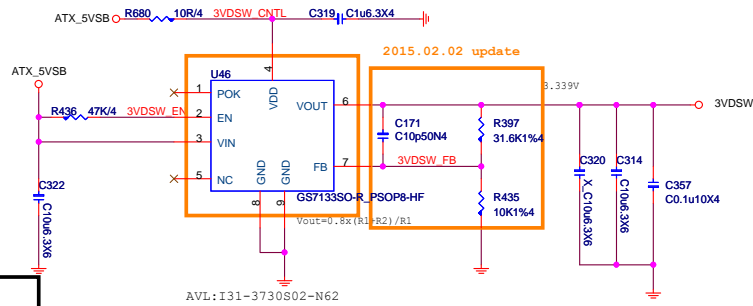
MS-7A43

Size Custom	Document Description CPU FAN	Rev 1.1
Date: Thursday, April 14, 2016		Sheet 39 of 59

Type H : 4/3 PIN SYS FAN FROM NCT3943S(USE SIO CUT POWER)

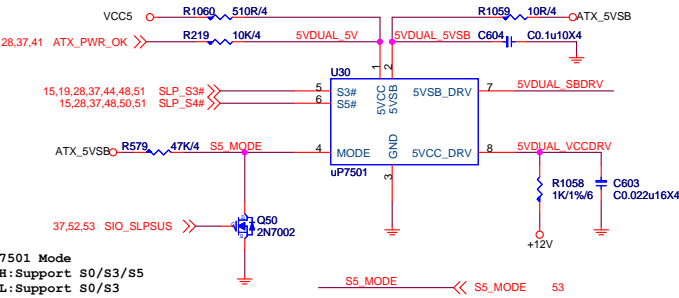


3VDSW



2015.05.25 Remove CUT_VBAT

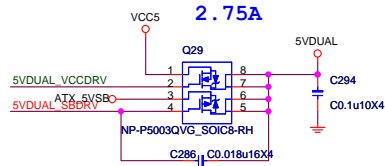
5VDIMM FOR 5VDUAL



7501 Mode
H:Support S0/S3/S5
L:Support S0/S3

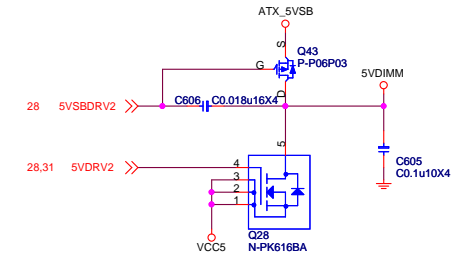
5VDUAL is power source of PCH_1VSB.

5VDUAL



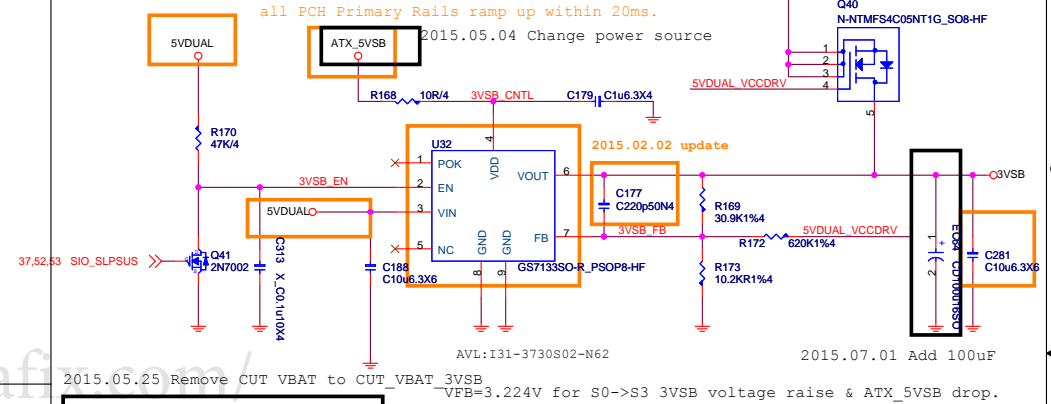
5VDIMM

2015.05.19 Power source change with USB.



Vinafix.com

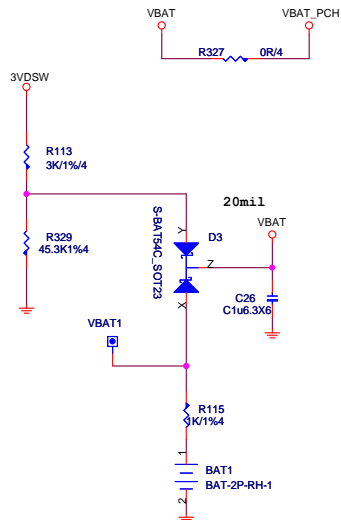
3VSB cost down



2015.05.25 Remove CUT_VBAT to CUT_VBAT_3VSB
VFB=3.224V for S0->S3 3VSB voltage raise & ATX_5VSB drop.

CUT_VBAT

CRB



2015.05.25 Remove CUT_VBAT to 3VDSW

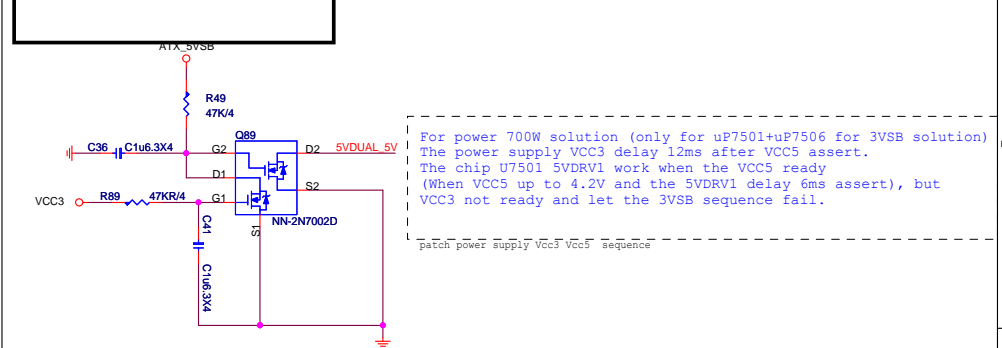
CUT_3VDSW

2015.05.25 Remove CUT_VBAT to CUT_VBAT_3VSB

CUT_3VSB

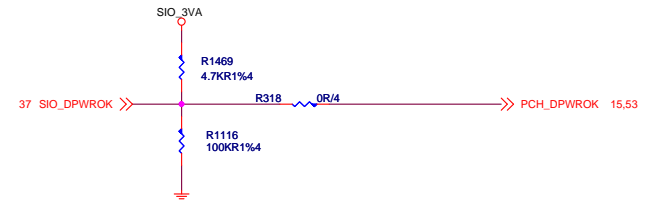
2015.05.25 Remove CUT_VBAT to CUT_1VSB_EN

CUT_PCH_1VSB



For power 700W solution (only for uP7501-uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.

patch power supply Vcc3 Vcc5 sequence



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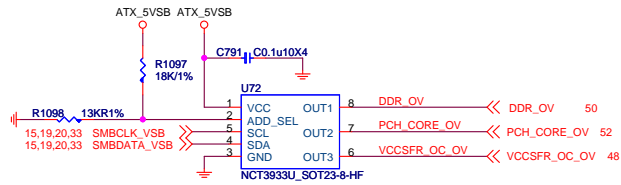
MS-7A43

Size	Document Description	Rev
Custom	ACPI UPI	1.1
Date: Thursday, April 14, 2016	Sheet 42 of 59	

Remove Cut Power.

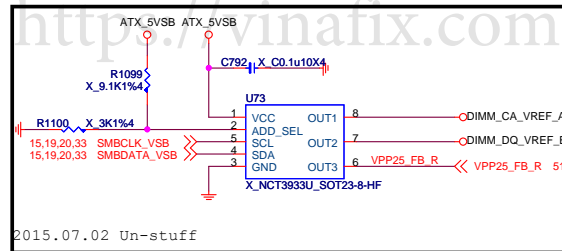
UPI VOLTAGE CONSOLE

0x26: RH=18K, RL=13K



UPI VOLTAGE CONSOLE

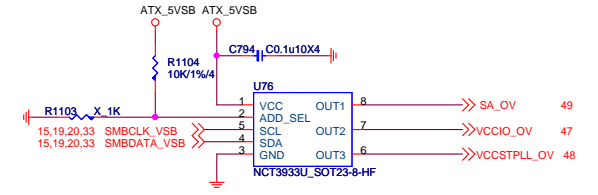
0x28: RH=9.1K, RL=3K



2015.07.02 Un-stuff

UPI VOLTAGE CONSOLE

0x20: RH=10K, RL=OPEN



ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

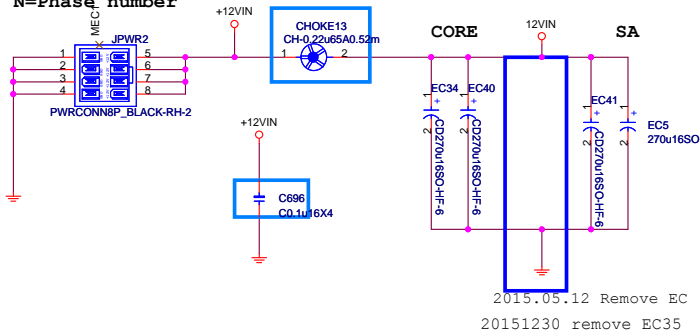


MICRO-STAR INT'L CO.,LTD

MS-7A43

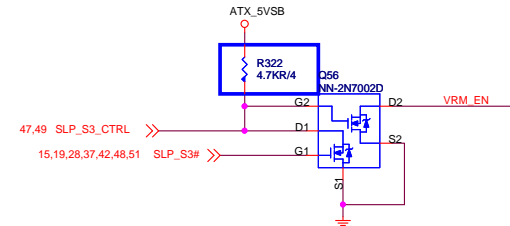
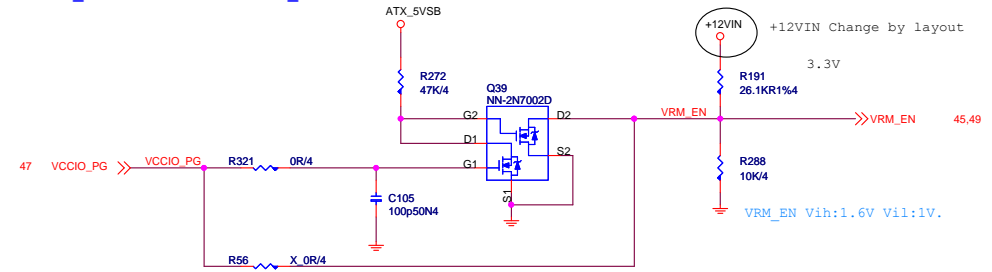
Size	Document Description	Rev
Custom	OV-NCT3933/GPIO-NCT5605	1.1
Date:	Thursday, April 14, 2016	Sheet 43 of 59

$I_{rms} = I_{out} * \sqrt{D/N * (D)^2}$
 $D = V_{out}/V_{in}$
 $N = \text{Phase number}$



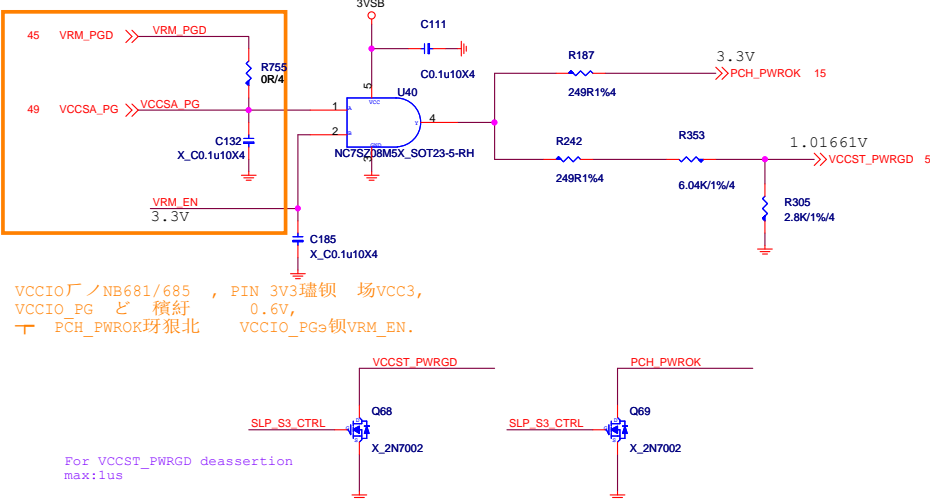
Tripple=23.097A
 VCORE 12.47A
 VGT 7.2977A
 VCCSA 3.33A

VRM_EN Control from VCCIO_PG



PCH_PWROK Control from VCCIO_PG&VCCSA
 VCCST_PWRGD Control from VRM_PGD

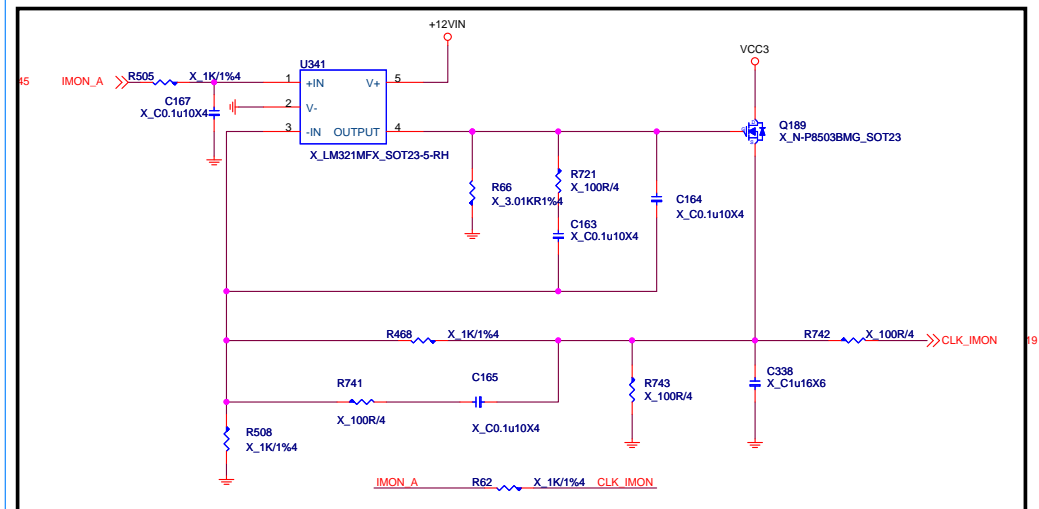
VCCSA&Vcore use same PWM IC, pull up VCC3
 VCCSA&Vcore use different PWM IC,pull up VCCSA
 VCCST_PWRGD can assert before or equal to PCH_PWROK, but must never lag it.



VCCIO厂/NB681/685, PIN 3V3端锁 场VCC3,
 VCCIO_PG と 横紬 0.6V,
 PCH_PWROK珙狼北 VCCIO_PG=锁VRM_EN.

For VCCST_PWRGD deassertion
 max:1us

2015.05.22 Prevent use same IMON cause noise.



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MS-7A43

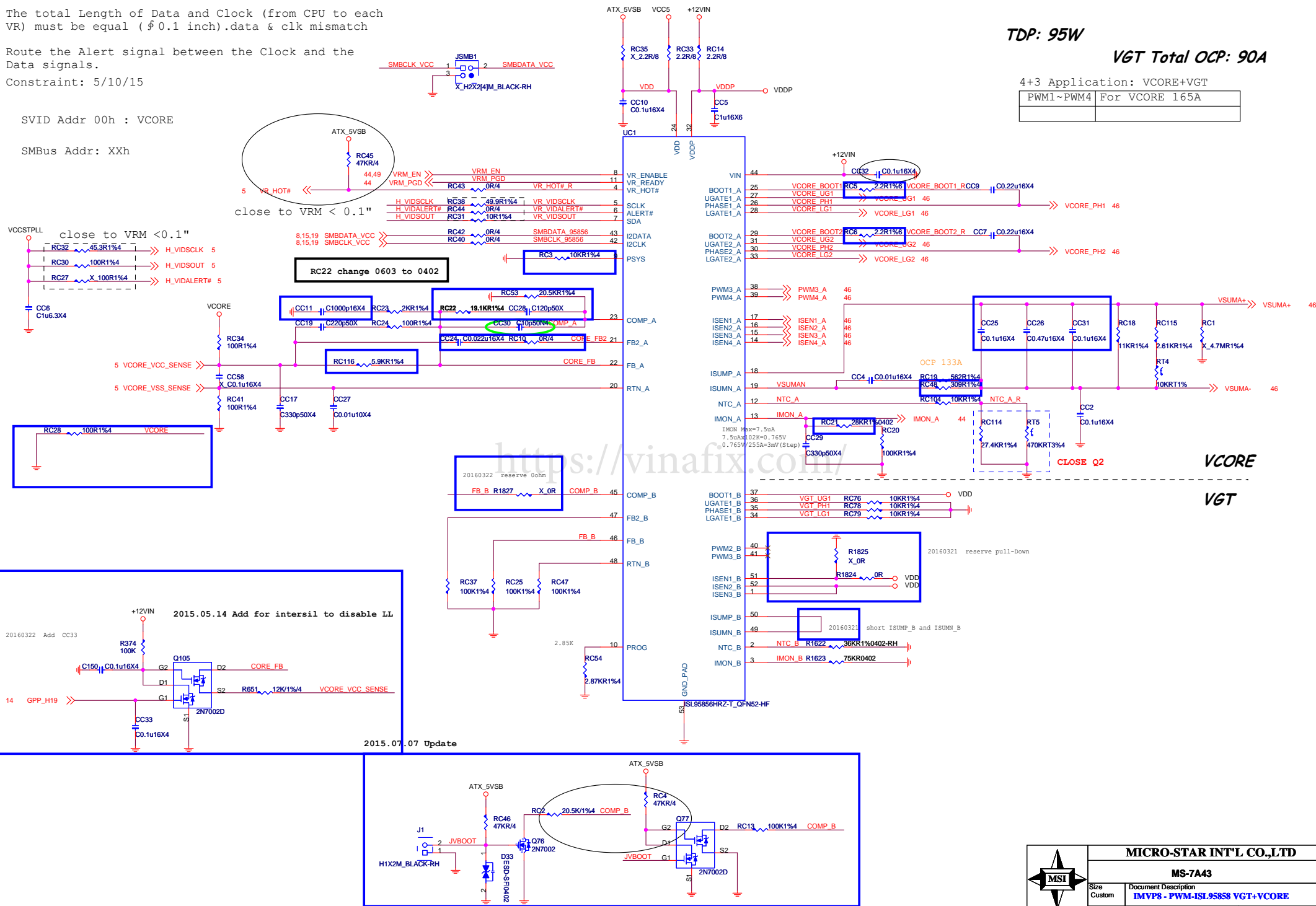
Size	Document Description	Rev
Custom	+12VIN/VRM_EN&PGD	1.1
Date:	Thursday, April 14, 2016	Sheet 44 of 59

SMBus Addr: XXh

VGT Total OCP: 90A

4+3 Application: VCORE+VGT

PWM1~PWM4	For VCORE 165A

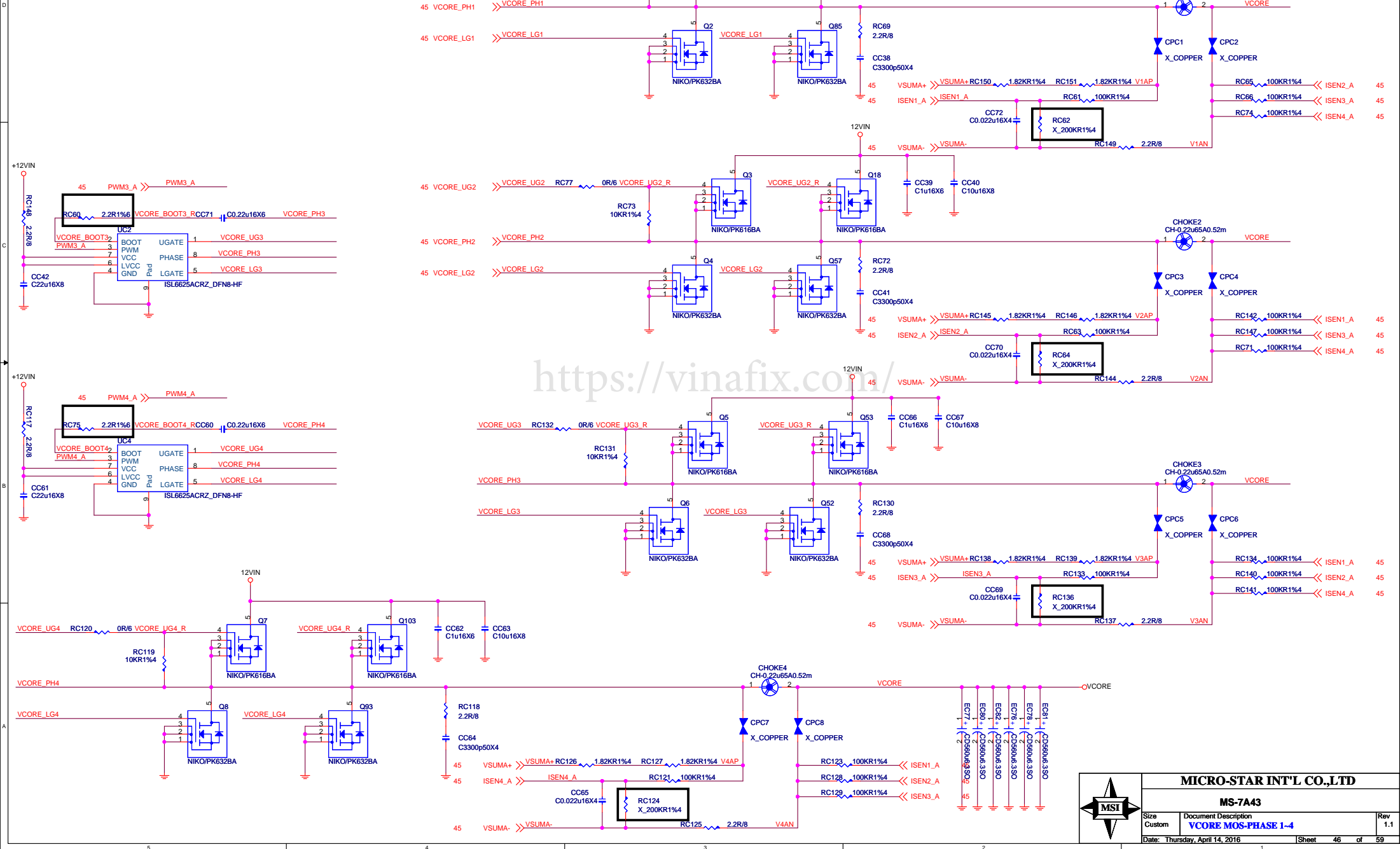


MICRO-STAR INT'L CO.,LTD

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Size Custom	Document Description IMVP8 - PWM-ISL95858 VGT+VCORE	Rev 1.
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2015.04.29 Add 1 low side MOS per phase for Vcore.



VCCIO

0.95V; 5.5A

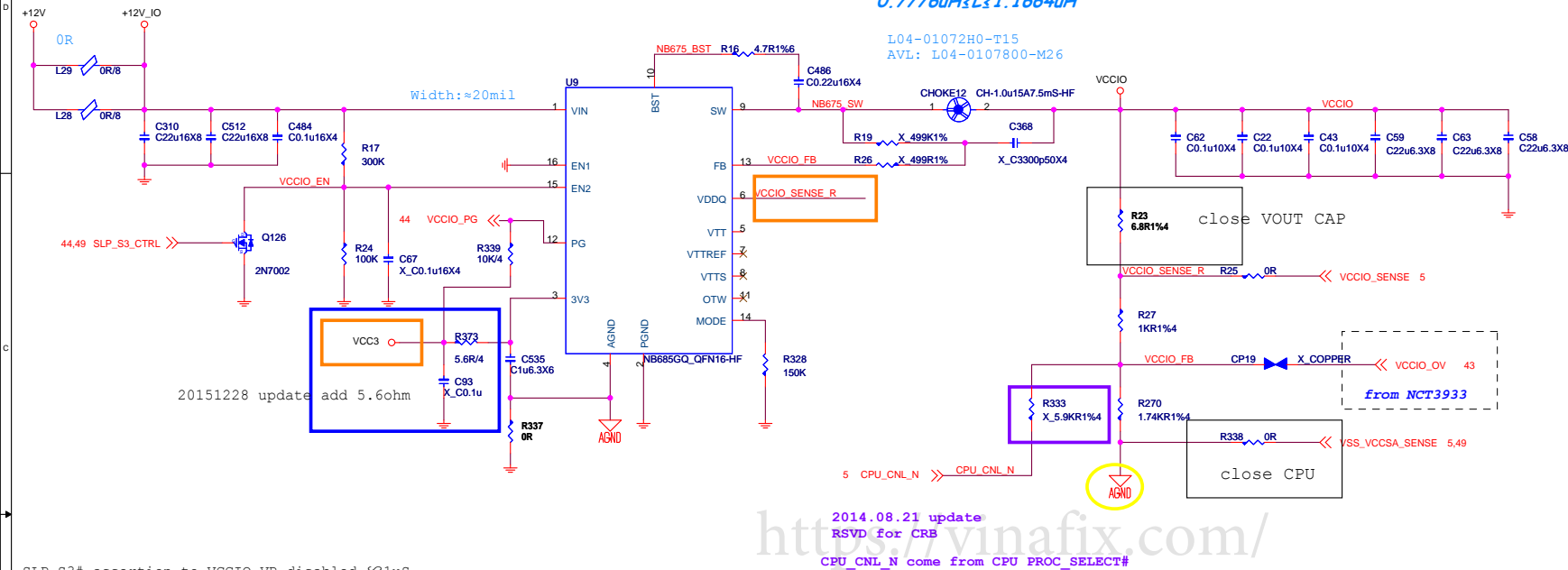
(H110 VCCIO=VCCSA)

IMAX 10A

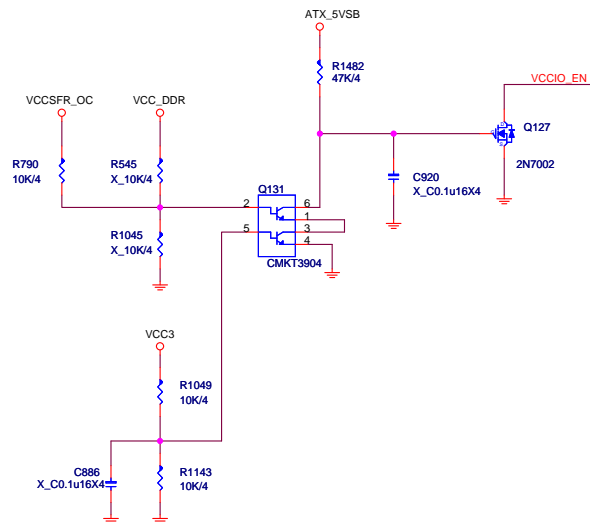
ILIMIT=10A~12A

IOC=ILIMIT+40%*IMAX/2=12A~14A.

Vinafix.com



SLP_S3# assertion to VCCIO VR disabled $\leq 1\mu S$.
SLP_S3# assertion to VCC, VCCGT, VCCIO and
VCCSA rails completely off. <500ms

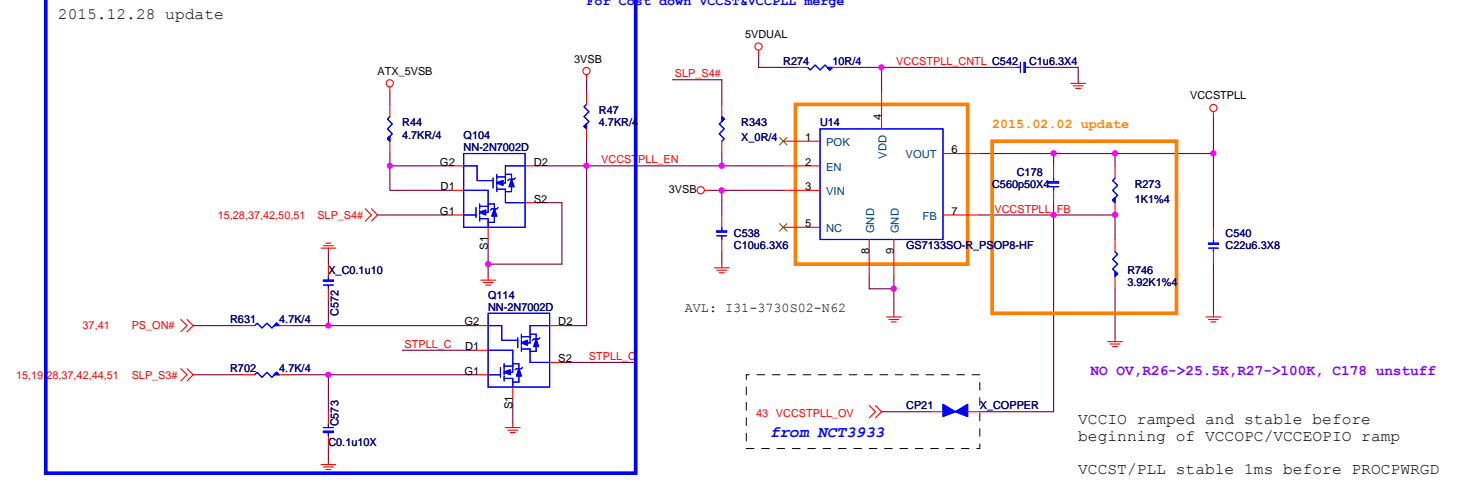


VCCSTPLL

1.0V; 250mA

For Cost down VCCST&VCCPLL merge

for Gaming3/5, Classic, ECO and H110

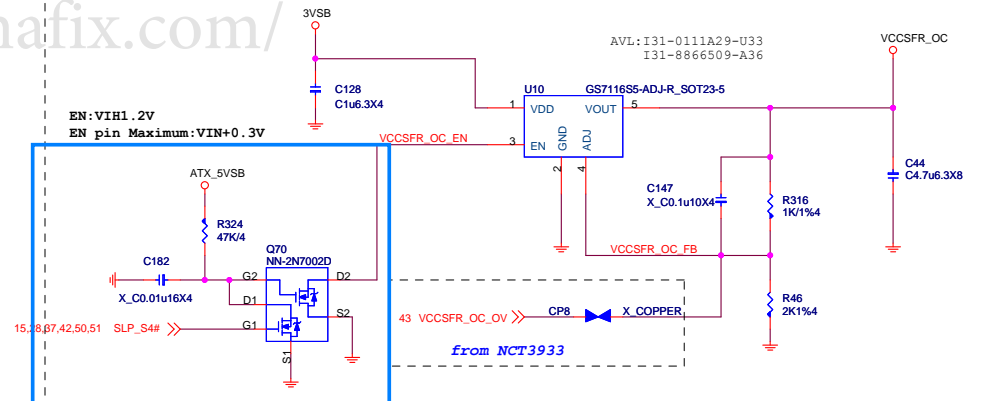


VCCPLL OC

1.2V; 110mA

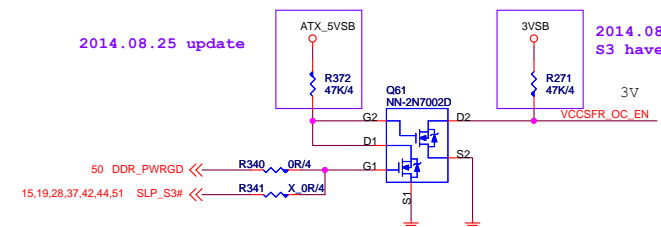
2014.08.21 update

<https://vinafix.com/>



2014.08.25 update

2014.08.25 update
S3 have power



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	CPU PWR ST/PLL	1.1
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SA Power:1.05V,12.3A

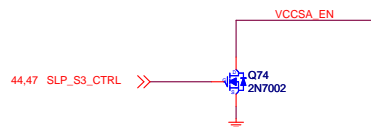
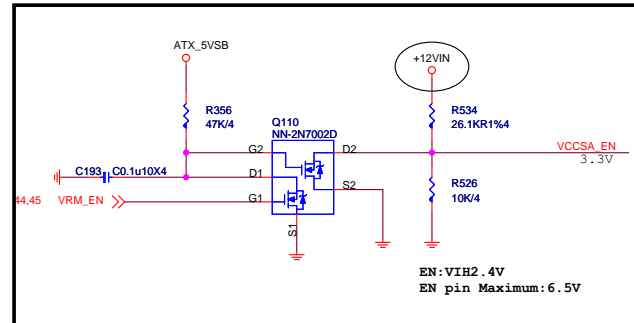
$OCP = 12.3A * 1.4 = 17.22A$

$R_{ocs}(R15) = OCP * R_{dson}(Low\ side) / 3.4mohm / 10uA$
 $= 17.22 * (3.4mohm / 10uA)$
 $= 5.854Kohm$

Rocs: 5.76K, OCP:
D03-4C05N03-005 : 16.94A
D03-632BA0C-N03 : 17.45A
use UBIQ MOS need Check

Rdson (low) 10V
D03-4C05N03-005 : 3.4mohm
D03-632BA0C-N03 : 3.3mohm
D03-3056M00-U47 : 4.2mohm

2015.05.11 Update. To prevent VRM_EN level too low to make PWRGD not output.



SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.

SLP_S3# assertion to VR disabled
max:1us

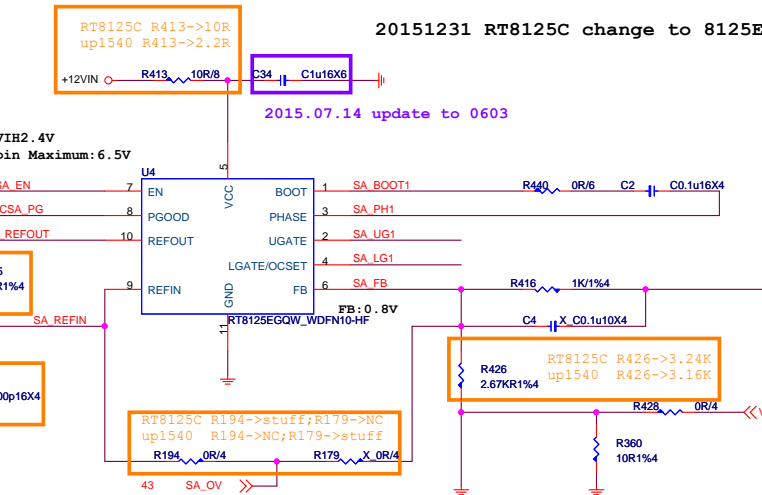
OCPSET:min 5Kohm

OCP
 $= (R417 * 10uA) / DCR$
 $= (5.76k * 10uA) / 3.3m$
 $= 17.4A$

SA UG1

SA PH1

SA LG1



20151231 RT8125C change to 8125E

2015.07.14 update to 0603

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 11.1 * 0.8 * 0.282566$$

$$= 2.509A$$

Footprint:CHK_D2_10_5X7_2_H9_6

1.05V,11.1A

$$L_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

$$= 0.5914uH (K = 30\%)$$

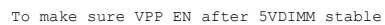
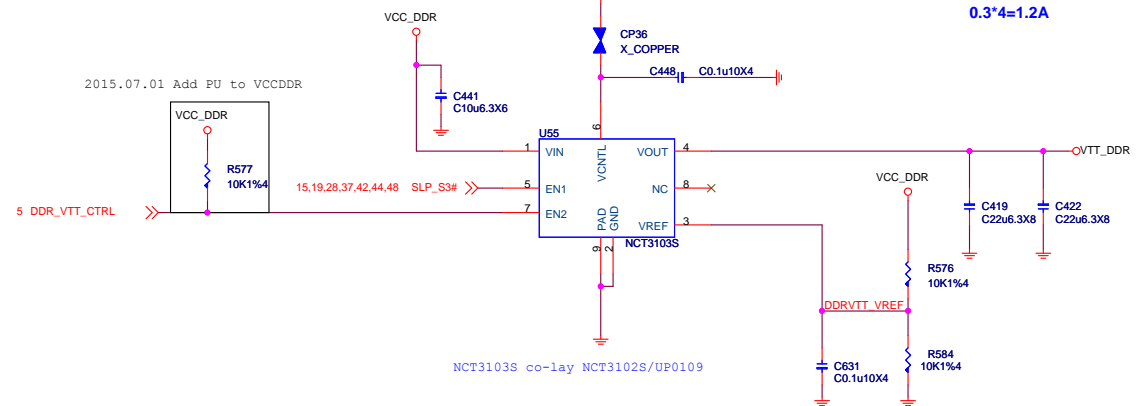


MICRO-STAR INT'L CO.,LTD

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Custom	SA POWER-RT8125C-1PHASE	1.1
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VPP25 Power
2.5V; 2.24A


$$0.3 \times 4 = 1.2A$$


MS-7A43

Size Custom	Document Description DDR4 Power-VPP25	Rev 1.1
Date: Thursday, April 14, 2016		Sheet 51 of 59

PCH 1VSB

1.0V; 11A

OCP = 11.787A

Rocset = $1.5 * I_{max} * R_{dson(LOW)} / I_{ocset}$
 = $1.5 * 7.858 * 5mohm / 10uA$
 = 5.8935K

Rocs:5.9K, OCP:
 D03-4C05N03-005 : 11.8A
 D03-632BA0C-N03 : 12.82A
 use UBIQ MOS need Check

Rdson(LOW) 4.5V
 D03-4C05N03-005 : 5 mohm
 D03-632BA0C-N03 : 4.6mohm
 D03-3056M00-U47 : 6.2mohm

20151231 1540 change to 8125E

20151230 Update

uP1504 & RT8125
 VCC Input Range : 4.5V to 13.2V

L04-47B7730-T15 for OC, Gaming 10, 9, 7, 5
 L04-12A7321-L65 for Gaming 3, SLI, ECO
 L04-12A7721-T15 for cost down

$$I_{rms} = I_{out} * \sqrt{(V_{out}/V_{in}) * (1 - (V_{out}/V_{in}))}$$

$$= 10.664 * 0.4$$

$$= 4.2656A < 5000mA$$

2015.05.25 Remove CUT_VBAT to CUT_1VSB_EN

2014.08.21 update

2015.07.14: Change 1u/0603

MAX: 10.664A

$$L_{min} = ((V_{in} - V_{out}) / (F_{sw} * k * I_{out_max})) * (V_{out}/V_{in})$$

$$= 0.8335uH (K = 30\%)$$

$$V_{out} = V_{ref} * (1 + R_{821}/R_{822})$$

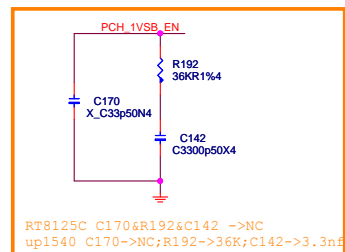
$$= 0.8 * (1 + 1K/3.92K)$$

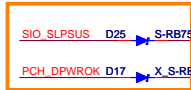
$$= 0.8 * 1.2551$$

$$= 1.004V$$

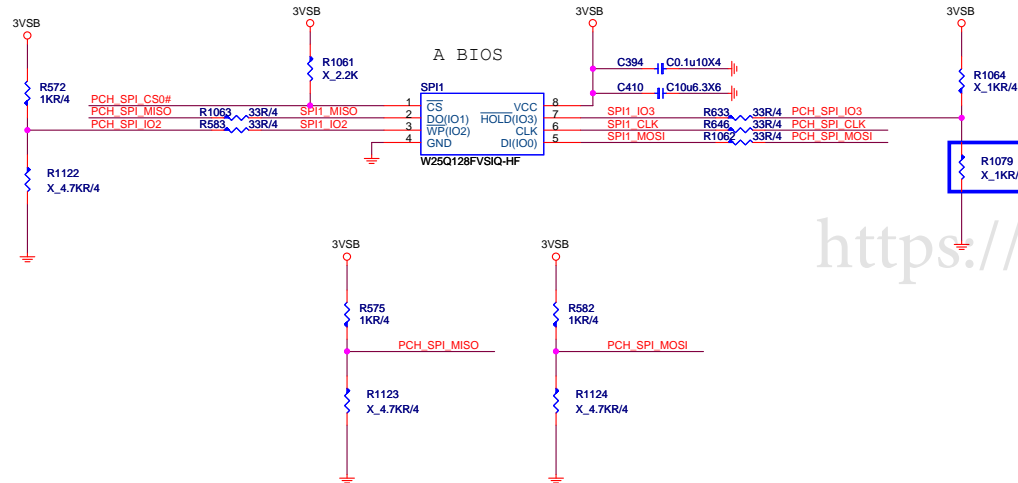
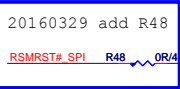
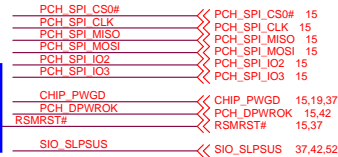
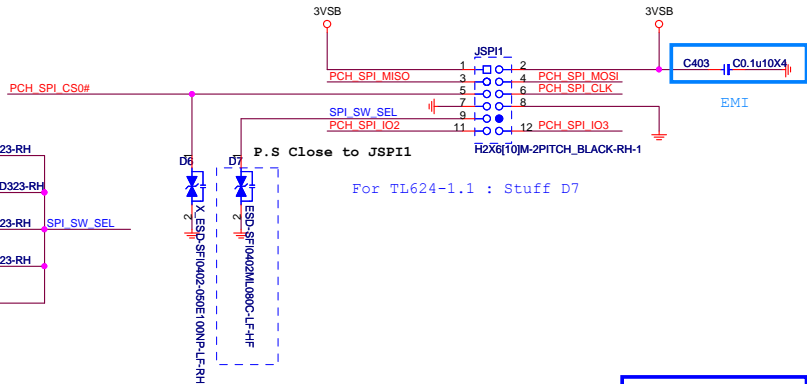
PCH 1P8

Remove circuit





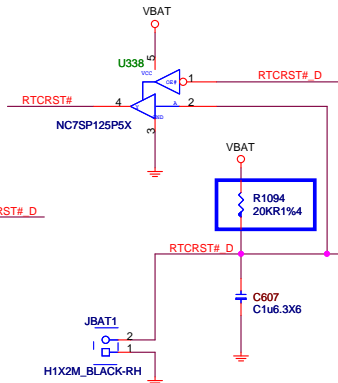
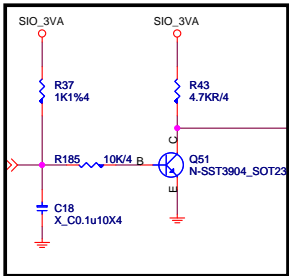
For Tl624 1.1



<https://vinafix.com/>

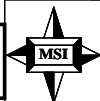
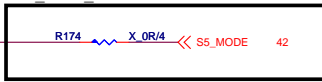
CLR_CMOS

2015.04.23 Modify R37 Q51 & Add R185



connector to other RTCRST#

2015.05.25 Remove CUT VBAT to CUT_1VSB_EN&CUT_3VDSW



tri-state		
INPUT		outout
PIN1	PIN2	pin4
L	H	H
L	L	L
H	X	Z

	R57	U338	R1094	C607
USE U338	X	O	O	O
Auto CLR_CMOS				
NOT USE U338	O	X	X	X
Auto CLR_CMOS				

MICRO-STAR INT'L CO.,LTD		
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Custom	BIOS & Clear CMOS	1.1
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PCB



7A43 1.1
PD0-07A4311-G37

CPU Socket



Battery



BAT-BCR2032P-RH

PCH

SBC Label

VIT_LA1
Label
VIRTUAL
VIT LABEL

BIOS Label

AML_LA1
AMI BIOS
LABEL
BIOS_LABEL

Marketing Label

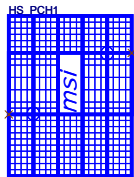
C232_LA1
Label
237-Gaming3
MKT-LABEL

Gaming LAN
Label
237-Gaming3
Gaming LAN

Y02-MU00170-CFO

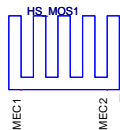
20160414 Add Gaming LAN Manager

PCH Heatsink



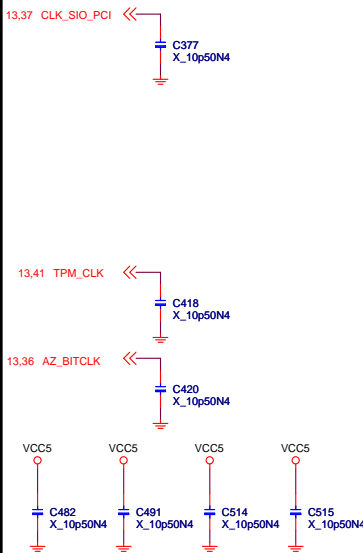
HS-0407630-RH

MOS Heatsink

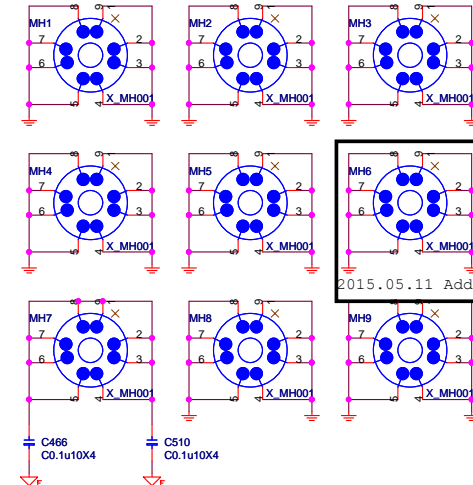


HS-0503920-HF

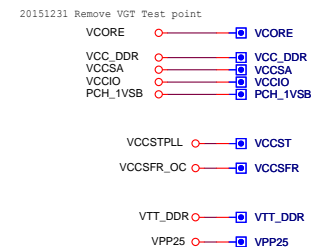
2015.05.11 Add EMI suggestion



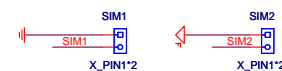
Mounting Holes



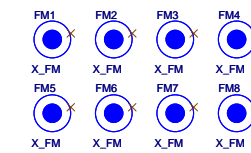
Test point



Simulation

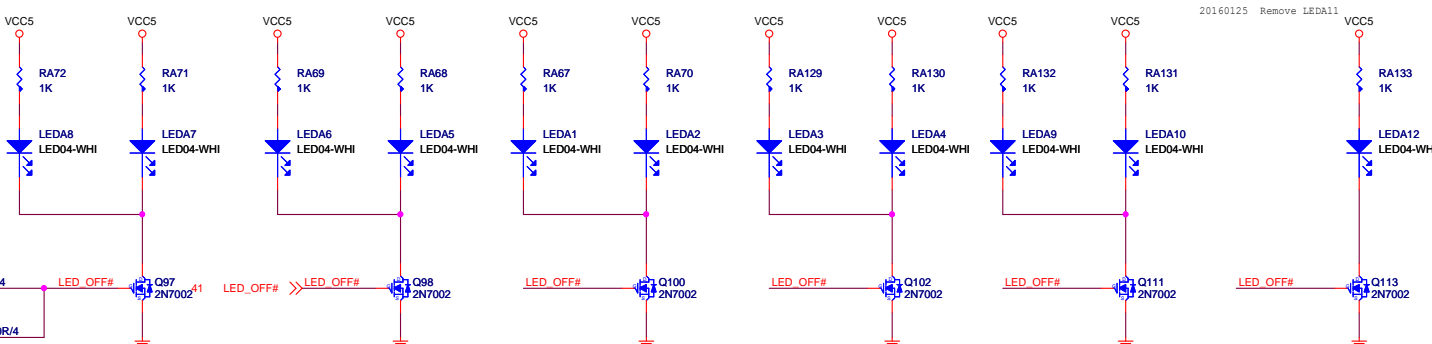


Optical Fiducial Marks-120



2015.04.28 Add

LED placed in the four corners of board.



2015.07.03 Add

2015.07.03 Add

20160125 Remove LEDA11




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