Compal Confidential

G470/G570 UMA M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH

2010-10-22

LA-6752P / LA-6754P

REV:0.2

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.			
Title: Cover Page			
Size: Custom	Document Number: LA-6752P		Rev: 0.2
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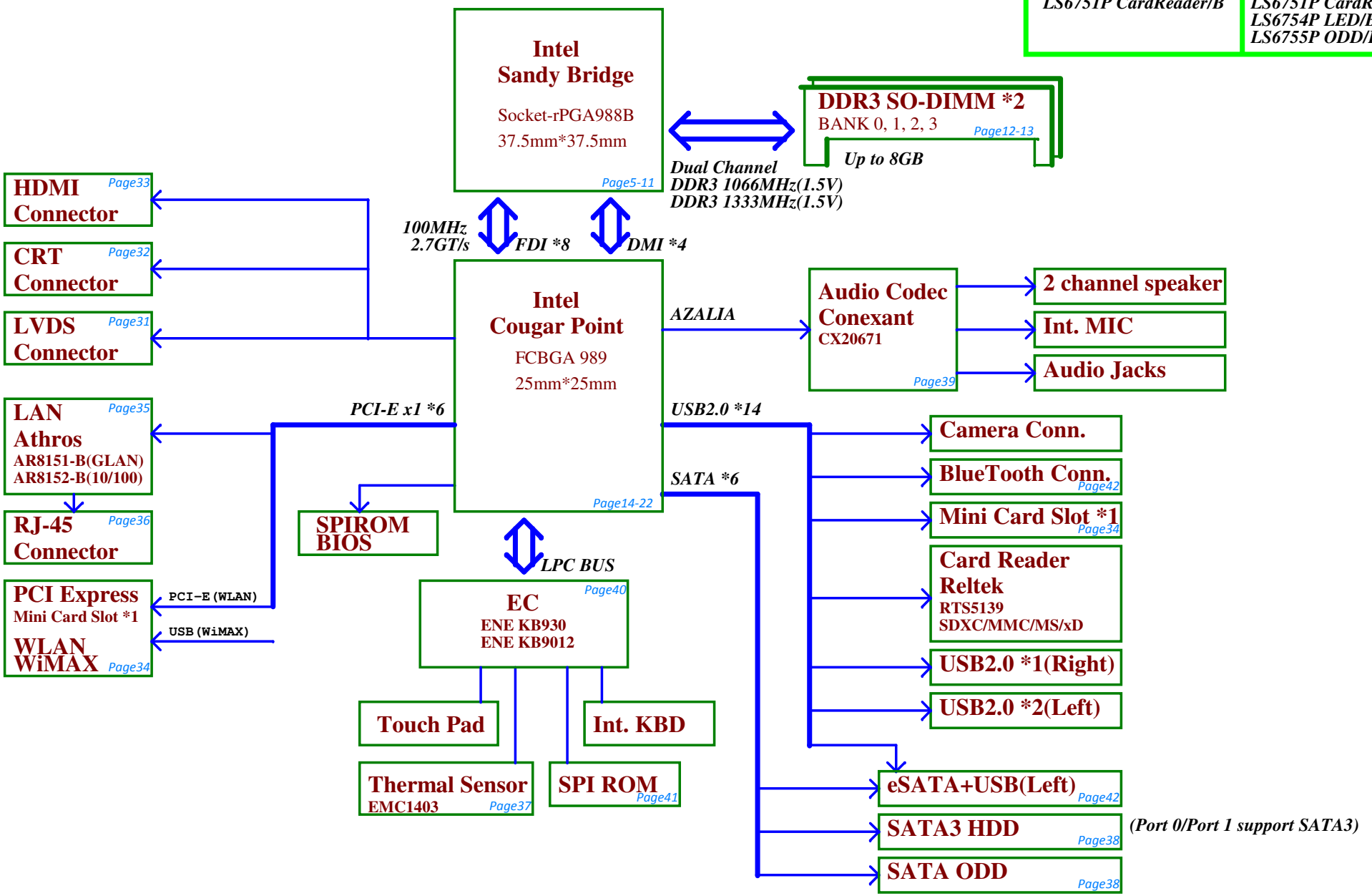
Compal confidential
File Name : G470/G570

For 14"(Page 4x)	For 15"(Page 4x+1)
LS6753P PWR/B	LS6753P PWR/B
LS6751P CardReader/B	LS6751P CardReader/B
	LS6754P LED/B
	LS6755P ODD/B



Security Classification	Compal Secret Data		
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Title: Block Diagram

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Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SIGNAL / STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max	
0	0	0 V	0 V	0 V	EVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	DVT
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	PVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	MP
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	
5	100K +/- 5%	1.453 V	1.650 V	1.759 V	
6	200K +/- 5%	1.935 V	2.200 V	2.341 V	
7	NC	2.500 V	3.300 V	3.300 V	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB Port (Left Side)
		3	USB Port (Left Side)
	UHCI2	4	
		5	Camera
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	
	UHCI5	10	
		11	Card Reader
	UHCI6	12	
		13	Blue Tooth

BOM Structure Table

BTO Item	BOM Structure
CAMERA DEVICE	CMOS@
Blue Tooth	BT@
eSATA	ESATA@
COMMON HDMI	HDMI@
Connector	ME@
45 LEVEL	45@
10/100 LAN	8152@
GIGA LAN	GIGA@
Unpop	@

SMBUS Control Table

	SOURCE	VGA	BATT	KE930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

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Title: Notes List

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Power-Up/Down Sequence

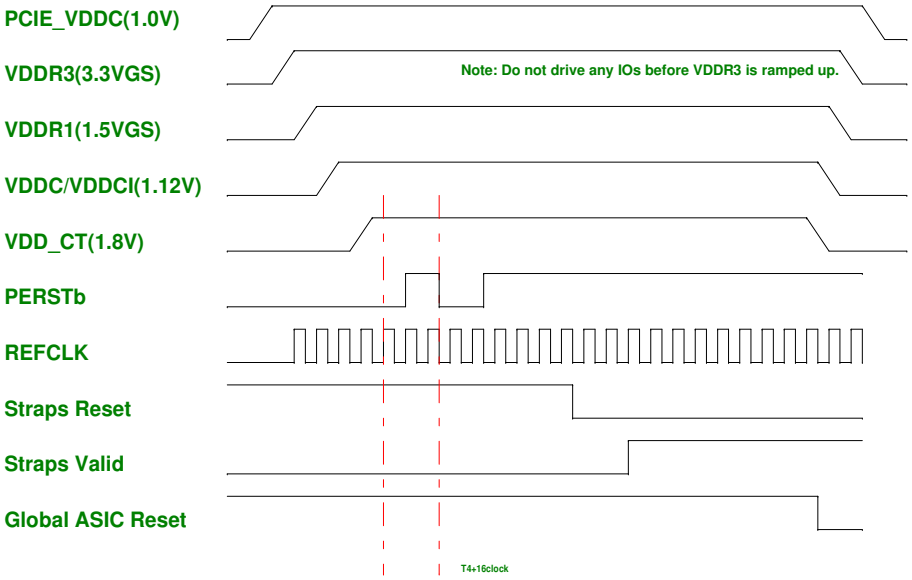
All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

VDDR3 should ramp-up before or simultaneously with VDDC.

For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation

PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

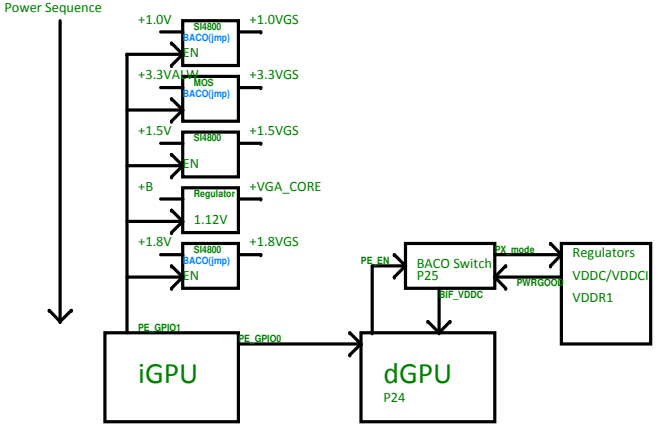
BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)

PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A

Power Sequence



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Title: CLOCK GENERATOR

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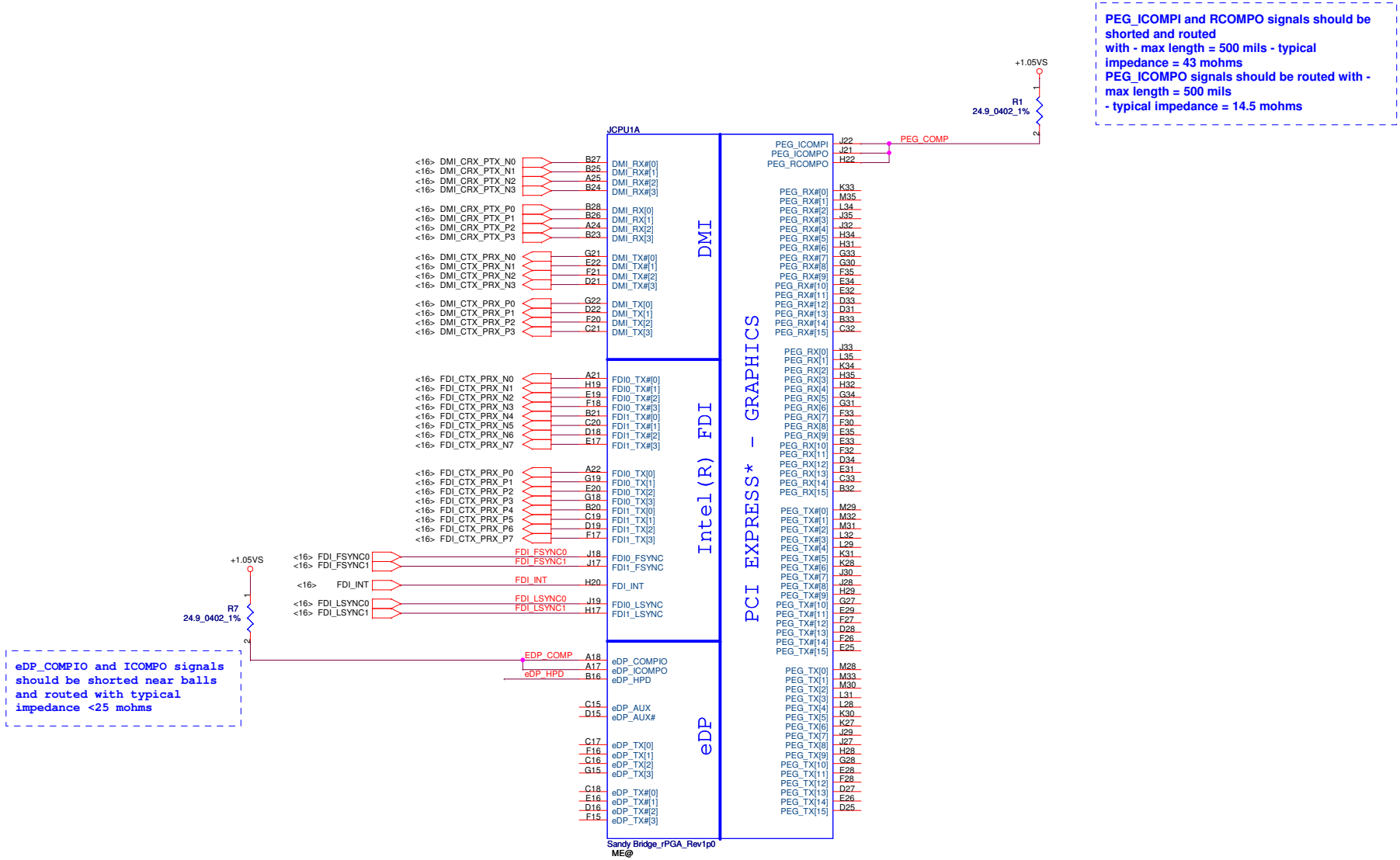

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Title: PROCESSOR(1/7) DMI,FDI,PEG

Size	Document Number	Rev
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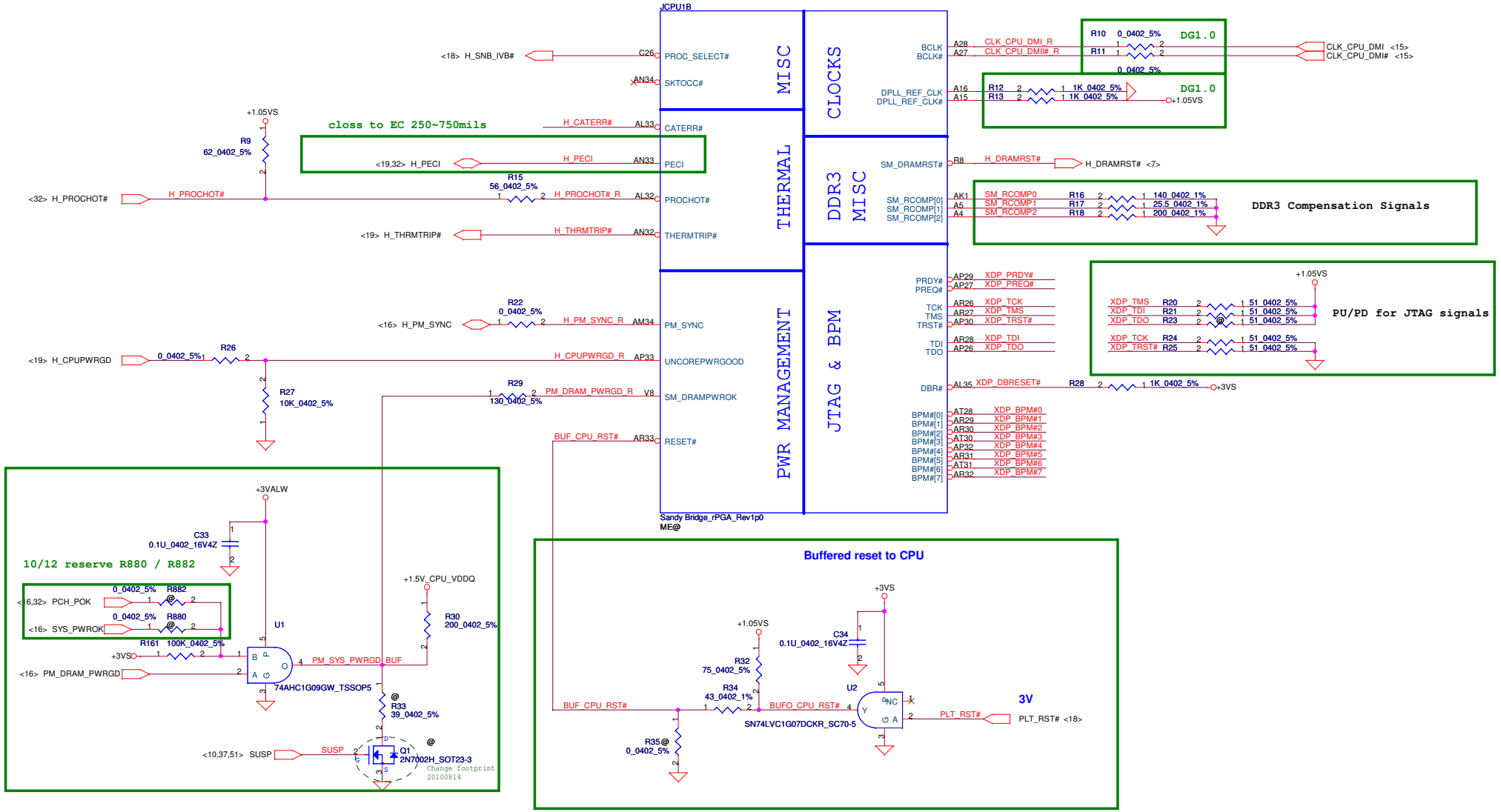

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Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title: PROCESSOR(2/7) PM,XDP,CLK			
Size: Custom	Document Number: LA-6752P		Rev: 0.2
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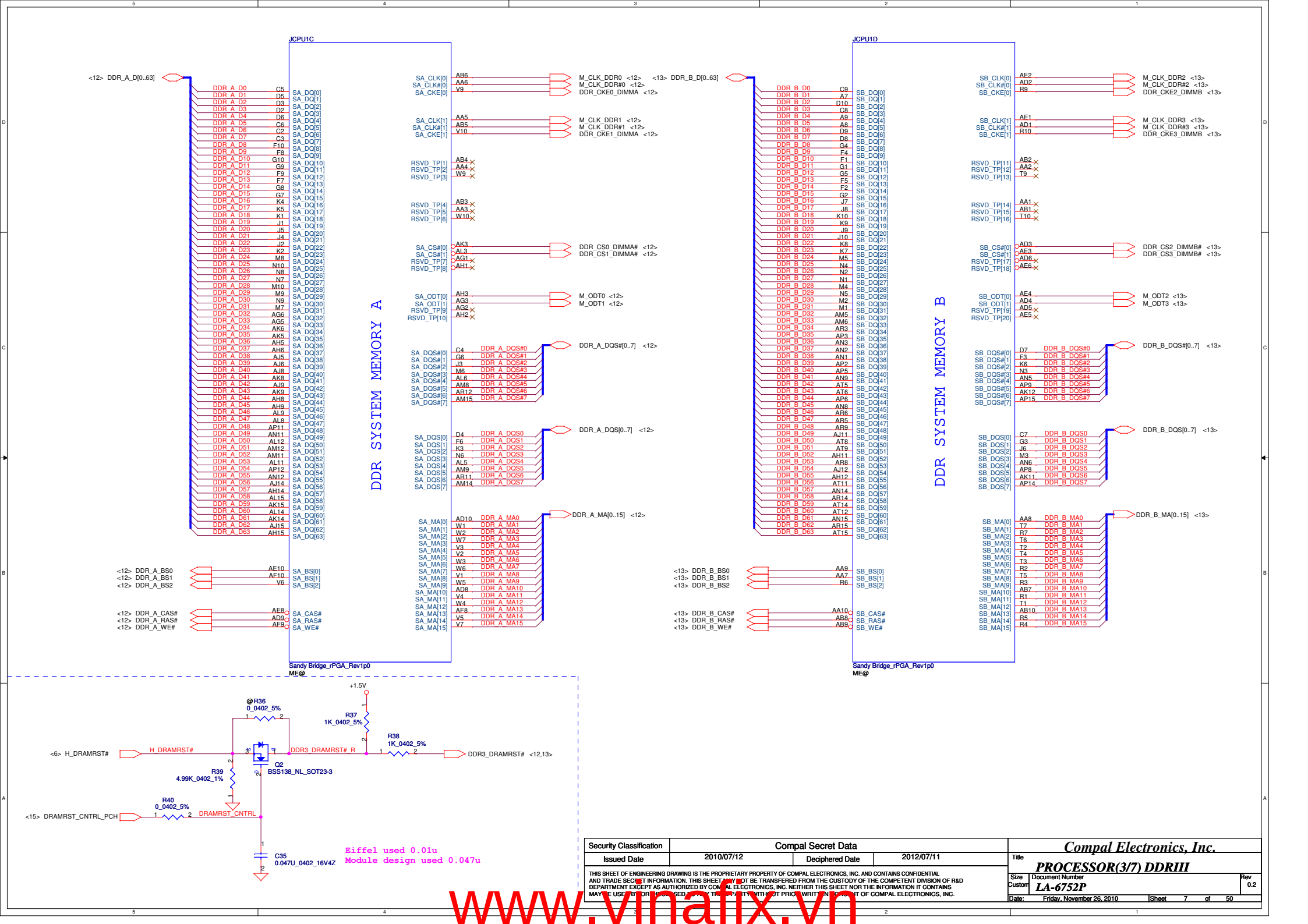
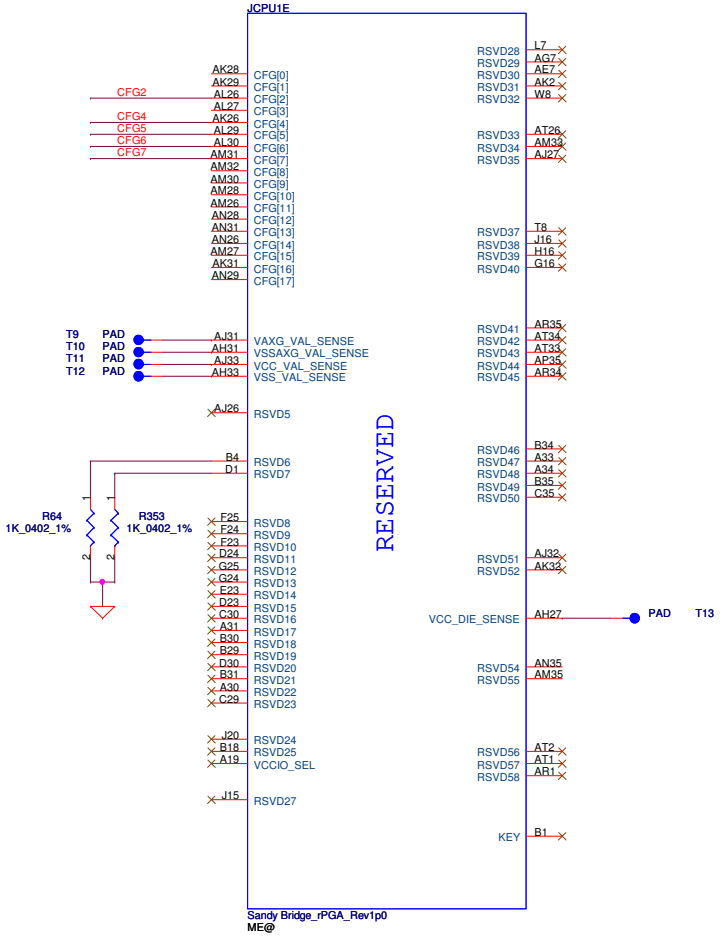
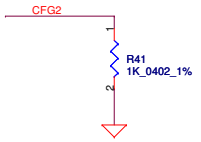
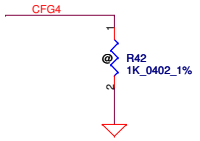


CFG Straps for Processor

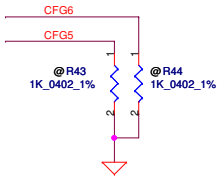




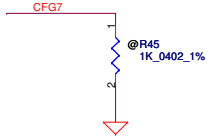
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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POWER

JCPU1F

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

+CPU_CORE

(6/16 change 10uF_0603_6.3V)*5

C36 10U_0805_6.3V6M
C37 10U_0805_6.3V6M
C38 10U_0805_6.3V6M
C39 10U_0805_6.3V6M
C40 10U_0805_6.3V6M
C48 10U_0603_6.3V6M
C49 10U_0603_6.3V6M
C50 10U_0603_6.3V6M
C51 10U_0603_6.3V6M @
C52 10U_0603_6.3V6M
C53 10U_0603_6.3V6M

QC=94A
DC=53A

+CPU_CORE

(22uF_0805_6.3V)*16

C66 22U_0805_6.3V6M @
C67 22U_0805_6.3V6M
C68 22U_0805_6.3V6M
C70 22U_0805_6.3V6M
C71 22U_0805_6.3V6M
C74 22U_0805_6.3V6M
C75 22U_0805_6.3V6M
C76 22U_0805_6.3V6M
C77 22U_0805_6.3V6M
C78 22U_0805_6.3V6M
C79 22U_0805_6.3V6M
C80 22U_0805_6.3V6M
C81 22U_0805_6.3V6M @
C82 22U_0805_6.3V6M @
C83 22U_0805_6.3V6M
C84 22U_0805_6.3V6M
C85 22U_0805_6.3V6M
C86 22U_0805_6.3V6M
C87 22U_0805_6.3V6M

+CPU_CORE

(330uF)*4

C88 330U_X_2VM_R6M
C89 330U_X_2VM_R6M
C90 330U_X_2VM_R6M
C91 330U_X_2VM_R6M

C394 @ C399

330U_X_2VM_R6M
330U_X_2VM_R6M

8/23 modify

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

Cap quantity follow HR_PDDG_Rev07
22uF*7 NO-STUFF

18A

OSCAN(22uF_0805_6.3V)*13

+1.05VS

C41 C42 C43 C44 C54 C45 C46 C55 C56 C47 22U_0805_6.3V6M
C57 C58 C59 @ C60 @ C61 @ C62 @ C63 @ C64 @ C65 @ 22U_0805_6.3V6M

C69 220U_6.3V_M
C72 220U_6.3V_M
C73 @ 330U_D2_2.5VY_R9M

OSCAN
(220uF_6.3V_4.2L_ESR17m)*2=(SF000002Y00)

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 E11 E14 E12 E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23

+1.05VS

R46 75_0402_5%

VR_SVID_CLK series-resistors close to VR

VIDALERT# AJ29 H_CPU_SVIDALRT# R47 43_0402_5%
VIDSCLK AJ30 H_CPU_SVIDCLK R48 0_0402_5%
VIDSOUT AJ28 H_CPU_SVIDDAT R49 0_0402_5%

VR_SVID_ALRT# <53>
VR_SVID_CLK <53>
VR_SVID_DAT <53>

R50 130_0402_5%

+1.05VS

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

+CPU_CORE

R51 100_0402_1%

VCC_SENSE AJ35 VCCSENSE_R R52 0_0402_5%
VSS_SENSE AJ34 VSSSENSE_R R53 0_0402_5%

VCCSENSE <53>
VSSSENSE <53>

R54 100_0402_1%

VCCIO_SENSE B10
VSSIO_SENSE A10

R74 0_0402_5% @
VCCIO_SENSE <51>
VSSIO_SENSE
R75 0_0402_5% @

VSS_SENCE 100ohm +-1% pull-down to GND near processor

8/12 Modify, need follow diffential routing
R74 close CPU,R75 close PWR

Sandy Bridge_rPGA_Rev1p0
ME@

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Title: PROCESSOR(5/7) PWR,BYPASS

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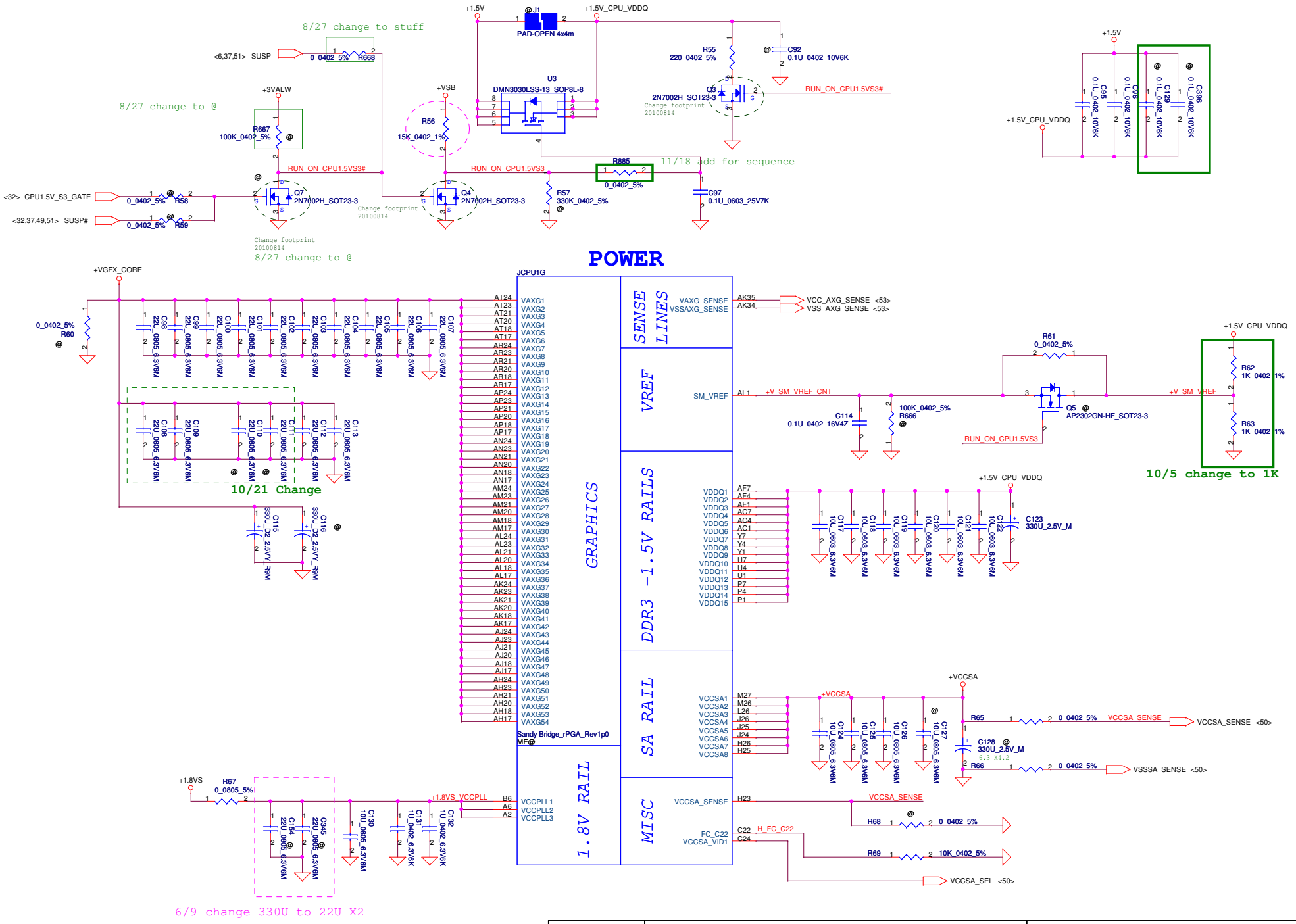

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Title: PROCESSOR(6/7) PWR

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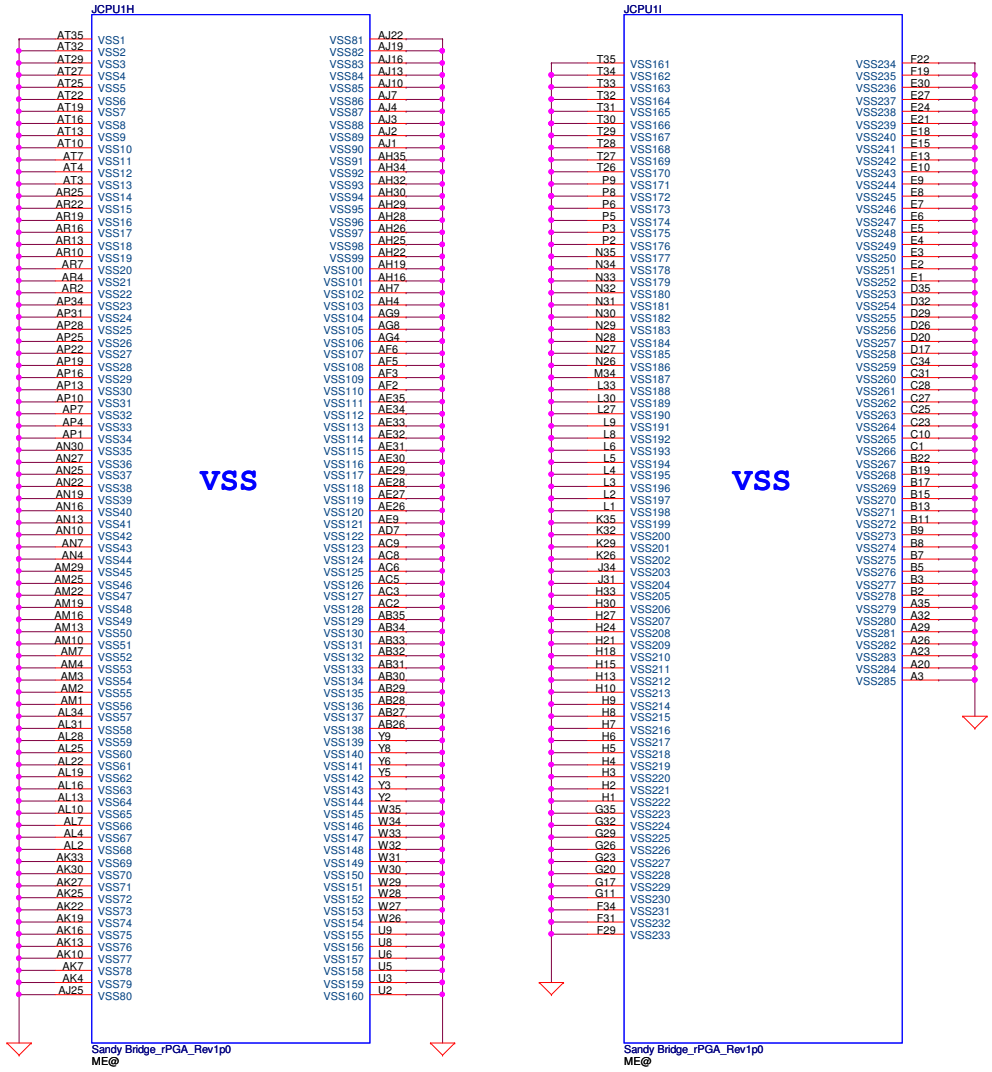

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Title: PROCESSOR(7/7) VSS

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DDR3 SO-DIMM A

JDIMM1

FOX_AS0A626-U4SN-7F

ME@

DDR3_DRAMRST# <7,13>

DDR_CKE1_DIMMA <7>

M_CLK_DDR1 <7>
M_CLK_DDR#1 <7>

DDR_A_BS1 <7>
DDR_A_RAS# <7>

DDR_CS0_DIMMA# <7>
M_ODT0 <7>

M_ODT1 <7>

SMB_DATA_S3 <13,15,26>
SMB_CLK_S3 <13,15,26>

0.5A@, 75V

<7> DDR_A_D[0..63]
<7> DDR_A_DQS[0..7]
<7> DDR_A_DQS#[0..7]
<7> DDR_A_MA[0..15]

R70 1K_0402_1%
R71 1K_0402_1%
R72 1K_0402_1%
R73 1K_0402_1%

R87 10K_0402_5%
R83 10K_0402_5%

OSCAN (220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)
(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

Layout Note:
Place near DIMM

7/28 Update connect GND directly

VDDQ(1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
3*0805 10uf 4*0402 1uf

VREF =
1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V)=
1*0402 0.1uf 1*0402 2.2uf

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Title: DDRIII-SODIMM SLOT1

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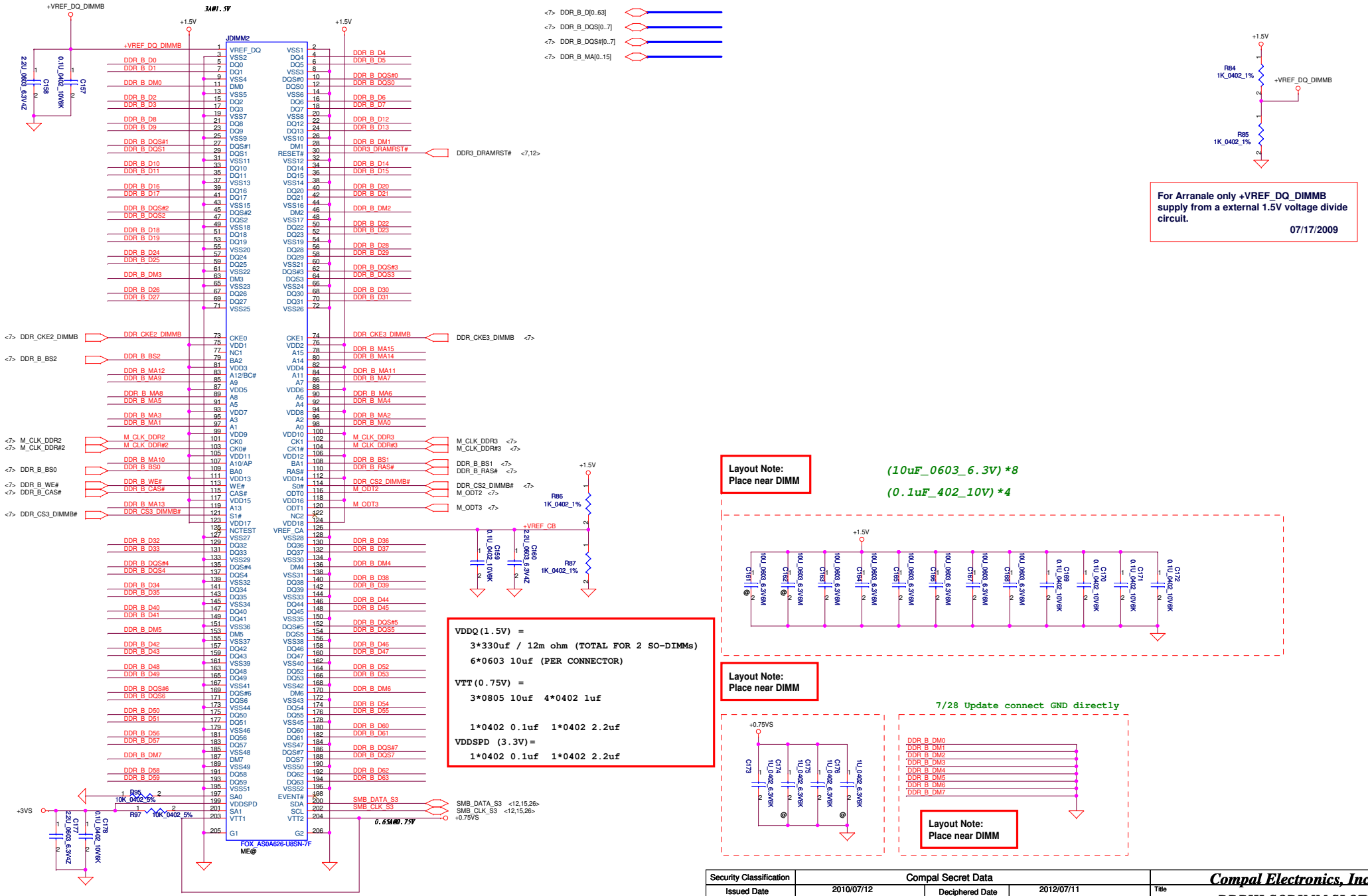

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT2**

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W=20mils
W=20mils
+RTCVCC
+RTCBATT
R99
1K_0402_5%
C179
1U_0603_10V4Z
CLRP1
SHORT PADS
PCH_RTCX1
PCH_RTCX2
R98
10M_0402_5%
R663 0_0402_5%
R670 0_0402_5%
PCH_RTCX1_OUT <32>
PCH_RTCX2_OUT <32>
6/24 Update R663,R670 must be close Y1
Y1
32.768KHZ_12.5PF_9H03200413
C180
15P_0402_50V8J
C181
15P_0402_50V8J
CMOS
+RTCVCC
R101 1M_0402_5% SM_INTRUDER#
R102 330K_0402_5% PCH_INTVRMEN
INTVRMEN
★ H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)
C183
1U_0603_10V4Z
R103 20K_0402_5%
R100 20K_0402_5%
C182
1U_0603_10V4Z
CLRP2
SHORT PADS
CLRP3
SHORT PADS
U4A
PCH_RTCX1 A20 RTCX1
PCH_RTCX2 C20 RTCX2
PCH_RTCRST# D20 RTCRST#
PCH_SRTCRST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC
LPC
FWH0 / LAD0 C38 LPC_AD0
FWH1 / LAD1 A38 LPC_AD1
FWH2 / LAD2 B37 LPC_AD2
FWH3 / LAD3 C37 LPC_AD3
FWH4 / LFRAME# D36 LPC_FRAME#
LDRQ0# E36
LDRQ1# / GPIO23 K36
SERIRQ V5
LPC_AD0 <26,32>
LPC_AD1 <26,32>
LPC_AD2 <26,32>
LPC_AD3 <26,32>
LPC_FRAME# <26,32>
SERIRQ <32>
EC and Mini card debug port
+3VS
R104 10K_0402_5%
SERIRQ
+3VS
R105 1K_0402_5% HDA_SPKR
HIGH= Enable (No Reboot)
LOW= Disable (Default)
HDA_BIT_CLK N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
HDA_SPKR T10 SPKR
HDA_RST# K34 HDA_RST#
<31> HDA_SPKR
IHDA
+3VALW
R106 1K_0402_5% HDA_SDOUT
★ Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]
<31> HDA_SDIN0 HDA_SDIN0 E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
+3VALW
R108 1K_0402_5% HDA_SYNC
This signal has a weak internal pull-down
On Die PLL VR Select is supplied by
★ 1.5V when smapled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom
<32> ME_FLASH
R109
0_0402_5%
HDA_SDOUT A36 HDA_SDO
R107 1K_0402_1% PCH_GPIO33 C36 HDA_DOCK_EN# / GPIO33
<56,57> Kill_SW# Kill_SW# N32 HDA_DOCK_RST# / GPIO13
R110
51_0402_5%
PCH_JTAG_TCK J3 JTAG_TCK
PCH_JTAG_TMS H7 JTAG_TMS
PCH_JTAG_TDI K5 JTAG_TDI
PCH_JTAG_TDO H1 JTAG_TDO
JTAG
SATA
SATA 6G
SATA0RXN AM3
SATA0RXP AM1
SATA0TXN AP7
SATA0TXP AP5
SATA_ITX_C_DRX_N0 0.01U_0402_16V7K C184
SATA_ITX_C_DRX_P0 0.01U_0402_16V7K C185
SATA_DTX_C_IRX_N0
SATA_DTX_C_IRX_P0
SATA_ITX_DRX_P0
SATA_DTX_C_IRX_N0 <30>
SATA_DTX_C_IRX_P0 <30>
SATA_ITX_DRX_N0 <30>
SATA_ITX_DRX_P0 <30>
HDD
SATA1RXN AM10
SATA1RXP AM8
SATA1TXN AP11
SATA1TXP AP10
SATA2RXN AD7
SATA2RXP AD5
SATA2TXN AH5
SATA2TXP AH4
SATA_ITX_C_DRX_N2 0.01U_0402_16V7K C186
SATA_ITX_C_DRX_P2 0.01U_0402_16V7K C187
SATA_DTX_C_IRX_N2
SATA_DTX_C_IRX_P2
SATA_ITX_DRX_N2_CONN
SATA_ITX_DRX_P2_CONN
SATA_DTX_C_IRX_N2 <56,57>
SATA_DTX_C_IRX_P2 <56,57>
SATA_ITX_DRX_N2_CONN <56,57>
SATA_ITX_DRX_P2_CONN <56,57>
ODD
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7
SATA4RXP Y5
SATA4TXN AD3
SATA4TXP AD1
SATA_ITX_C_DRX_N4 0.01U_0402_16V7K C188
SATA_ITX_C_DRX_P4 0.01U_0402_16V7K C189
ESATA@
SATA_DTX_C_IRX_N4
SATA_DTX_C_IRX_P4
SATA_ITX_DRX_N4
SATA_ITX_DRX_P4
SATA_DTX_C_IRX_N4 <35>
SATA_DTX_C_IRX_P4 <35>
SATA_ITX_DRX_N4 <35>
SATA_ITX_DRX_P4 <35>
ESATA
7/28 change from port 5 to port 4
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATAICOMPO Y11
SATAICOMPI Y10
SATA_COMP
R111 37.4_0402_1% +1.05VS_VCC_SATA
SATA3RCOMPO AB12
SATA3COMPI AB13
SATA3_COMP
R113 49.9_0402_1% +1.05VS_SATA3
SATA3RBIAS AH1
RBIAS_SATA3 R115 750_0402_1%
R117 10K_0402_5% +3VS
SATALED# P3
HDD_LED#
HDD_LED# <56,57>
SATA0GP / GPIO21 V14
PCH_GPIO21
R119 10K_0402_5% +3VS
SATA1GP / GPIO19 P1
PCH_GPIO19
R187 10K_0402_5% +3VS
@
SPI_CLK_PCH_R T3 SPI_CLK
SPI_SB_CS0# Y14 SPI_CS0#
T1 SPI_CS1#
SPI_SI V4 SPI_MOSI
SPI_SO_R U3 SPI_MISO
SPI
COUGARPOINT_FCBGA989
<31> HDA_BITCLK_AUDIO
R112 33_0402_5%
HDA_BIT_CLK
<31> HDA_SYNC_AUDIO
R114 33_0402_5%
HDA_SYNC_R
<31> HDA_RST_AUDIO#
R116 33_0402_5%
HDA_RST#
<31> HDA_SDOUT_AUDIO
R118 33_0402_5%
HDA_SDOUT
+3VS
Q10
BSS138_NL_SOT23-3
HDA_SYNC
R878
1M_0402_5%
@R325
0_0402_5%
9/27 reserve R878 for DG1.5
+3VALW
+3VALW
+3VALW
R121 200_0402_5%
R122 200_0402_5%
R123 200_0402_5%
PCH_JTAG_TDO
PCH_JTAG_TMS
PCH_JTAG_TDI
R125 100_0402_1%
R126 100_0402_1%
R128 100_0402_1%
DPDG1.1
6/30 update R121, R122, R123
8/16 reserved for MOW
4MB SPI ROM FOR ME
& Non-share ROM.
+3VS
R127 3.3K_0402_5% SPI_WP#
R129 3.3K_0402_5% SPI_HOLD#
SPI_CLK_PCH
R124 33_0402_5%
@
C190
22P_0402_50V8J
@
+3VS
C191
0.1U_0402_16V4Z
R130 0_0402_5%
SPI_SB_CS0#
SPI_SO_R
SPI_SO_L
SPI_WP#
33_0402_5%
R131
U5
CS#
SO
WP#
GND
VCC
HOLD#
SCLK
SI
SPI_HOLD#
SPI_CLK_PCH
SPI_SI_R
0_0402_5% R132
SPI_CLK_PCH_R
SPI_SI
33_0402_5%
R133
S IC FL 32M W25Q32BVSSIG SOIC 8P
Security Classification: Compal Secret Data
Issued Date: 2010/07/12
Deciphered Date: 2012/07/11
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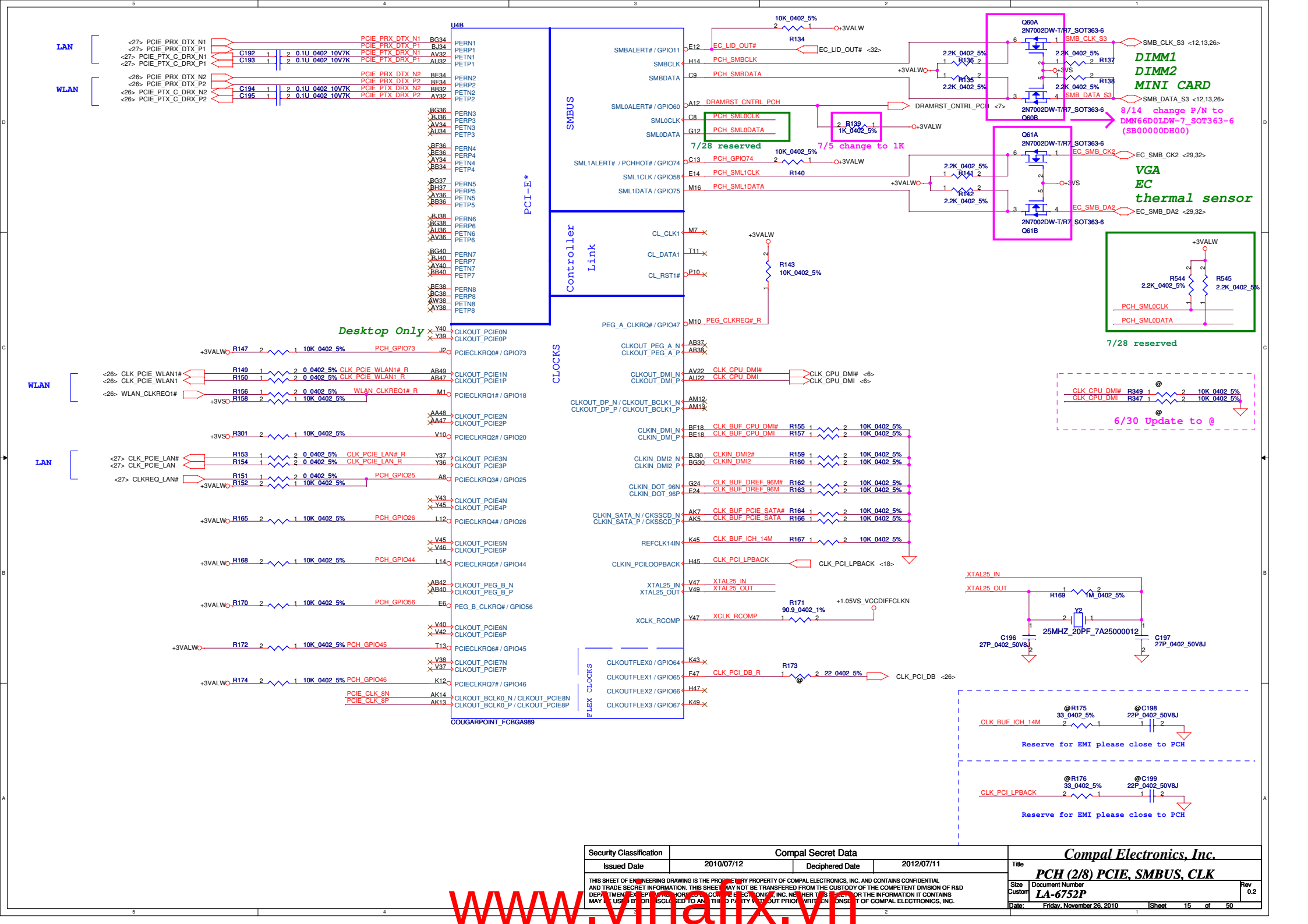
Compal Electronics, Inc.
Title: PCH (1/8) SATA,HDA,SPI, LPC, XDP
Size: Custom
Document Number: LA-6751P
Rev: 0.2
Date: Friday, November 26, 2010
Sheet 14 of 50



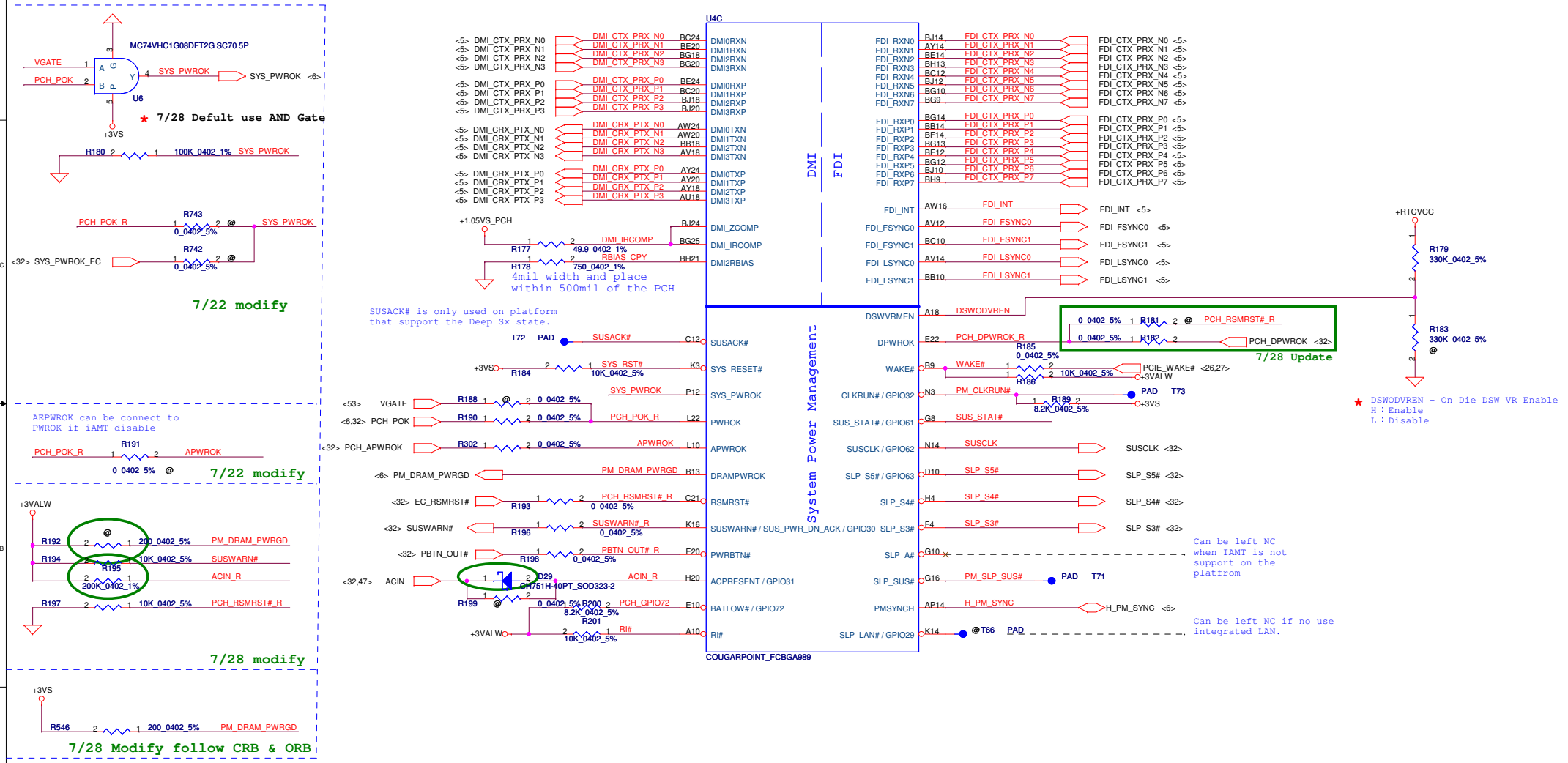
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (2/8) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	LA-6752P	0.2

Date: Friday, November 26, 2010 Sheet 15 of 50



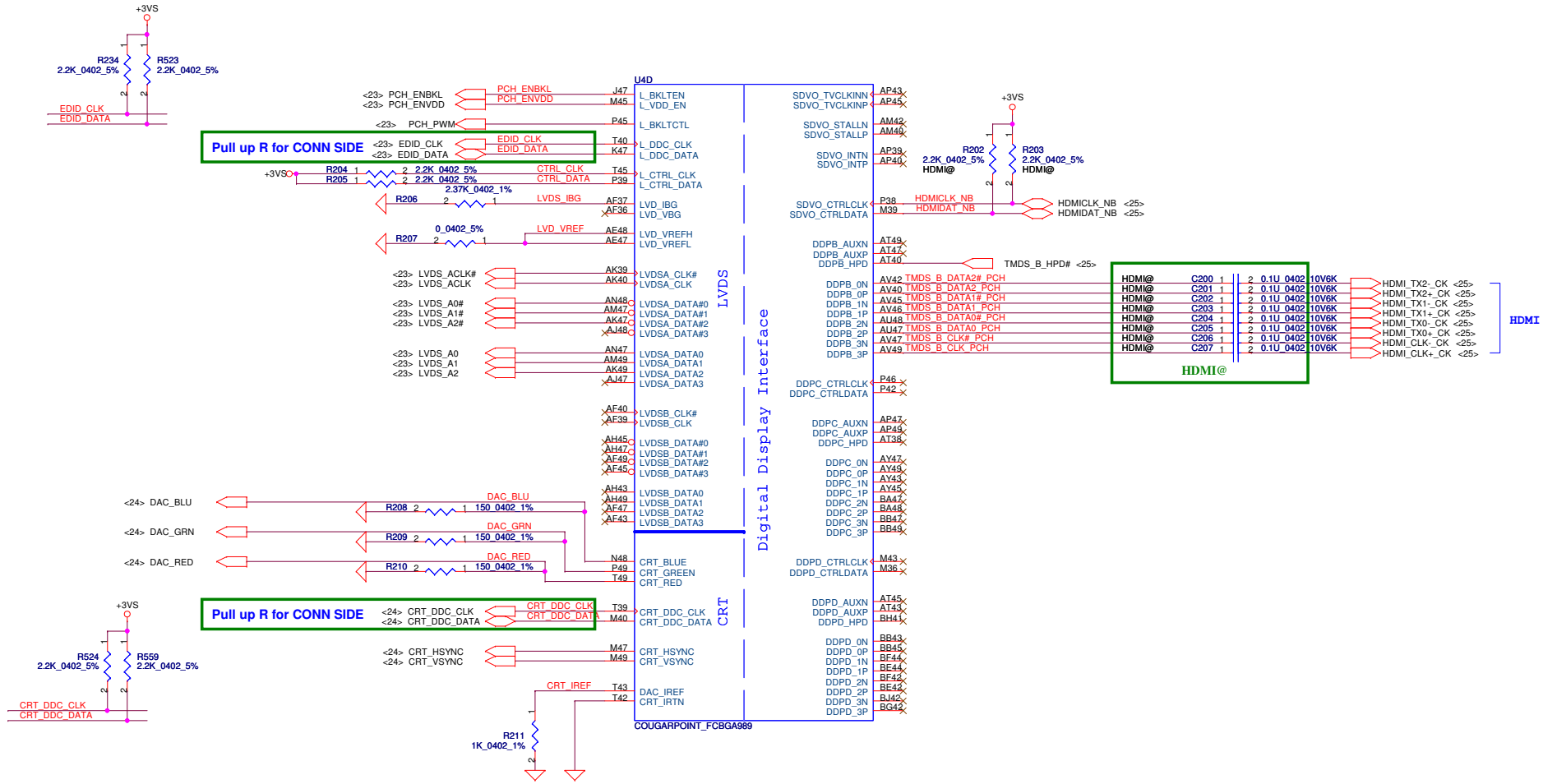
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,

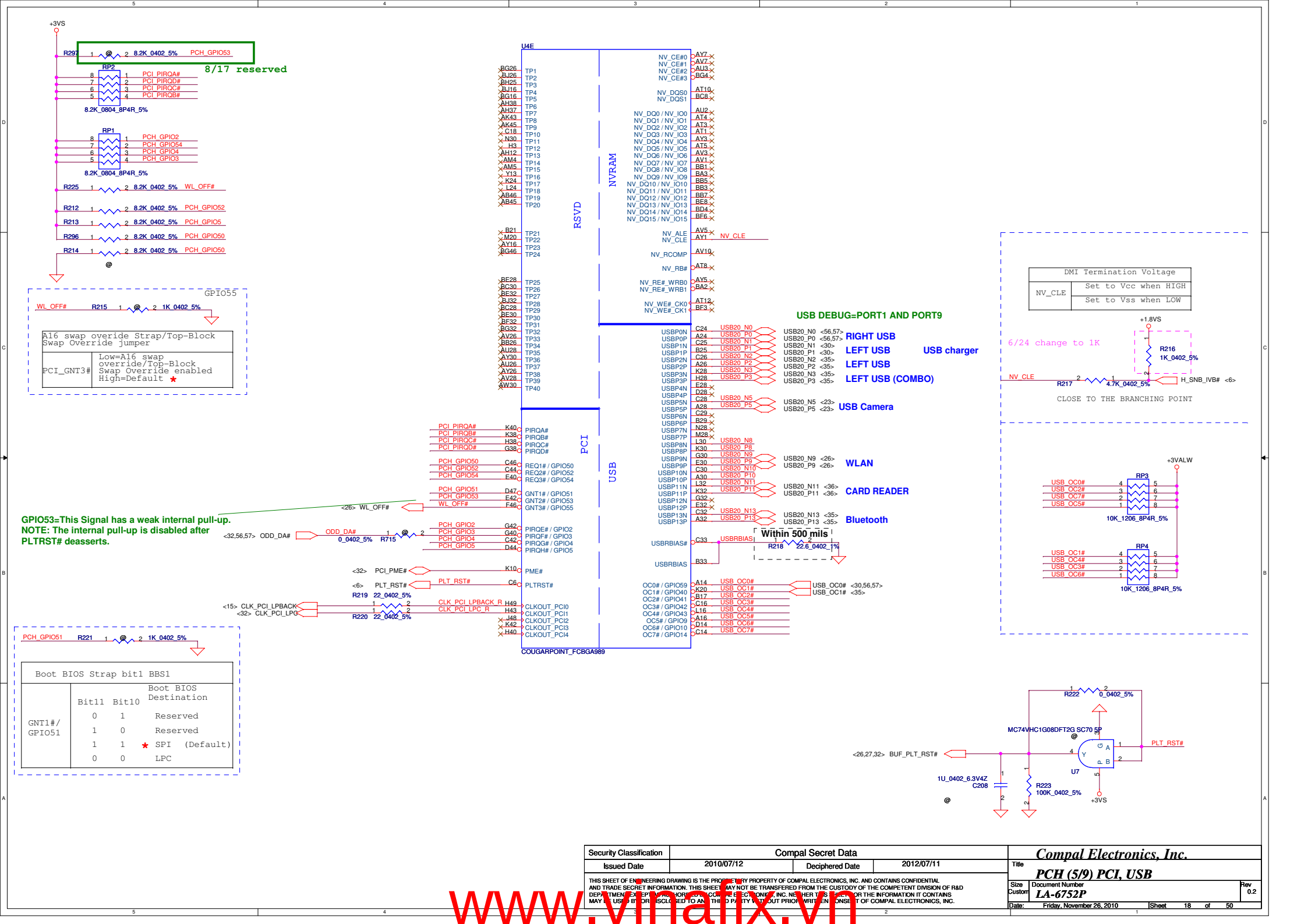
Size	Document Number	Rev
Custom	LA-6752P	0.2

Date: Friday, November 26, 2010 Sheet 16 of 50



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: PCH (4/9) LVDS,CRT,DP,HDMI			
Size: Custom	Document Number: LA-6752P		Rev: 0.2
Date: Friday, November 26, 2010	Sheet 17 of 50		



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

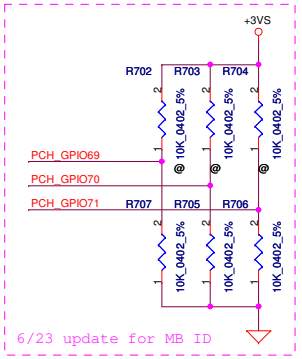
Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB

Size	Document Number	Rev
Custom	LA-6752P	0.2

Date: Friday, November 26, 2010 Sheet 18 of 50

PCH_GPIO69	PCH_GPIO70	PCH_GPIO71	Function
0	0	0	UMA *
1	0	0	DIS
0	1	0	PX3.0
1	1	0	PX4.0



ICC_EN#
Integrated Clock Chip Enable
H ; Disable
L ; Enable
R235 1K_0402_5% EC_SMI#
Weak internal pull-high

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable
R240 1K_0402_5% PCH_GPIO28

PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable
R245 10K_0402_5% PCH_GPIO27

R250 10K_0402_5% PCH_GPIO36
R547 10K_0402_5%
8/5 update to pull down

R881 10K_0402_5% PCH_GPIO37

10/8 update to pull down for checklist Rev1.2

7/22 update to reserve only

7/22 update to used intel function

R233 10K_0402_5% PCH_GPIO0
ESATA_DET# R303 0_0402_5%
R227 10K_0402_5%
R228 10K_0402_5% PCH_GPIO6
<32> EC_SCI# EC_SCI#
<32> EC_SMI# EC_SMI#
R229 10K_0402_5% CPUSB#
R230 1K_0402_5% PCH_GPIO15
R231 10K_0402_5% PCH_GPIO16
<35> ESATA_DET# R542 0_0402_5%
R232 10K_0402_1% GPIO17
R238 10K_0402_5% PCH_GPIO22
<30> ODD_EN ODD_EN
R241 10K_0402_5% PCH_GPIO27
<35> BT_OFF# R242 10K_0402_5% PCH_GPIO28
BT_OFF#
R243 10K_0402_5% PCH_GPIO35
PCH_GPIO36
R244 10K_0402_5% PCH_GPIO37
R246 10K_0402_5% PCH_GPIO38
R247 10K_0402_5% PCH_GPIO39
R248 10K_0402_5% PCH_GPIO48
R249 10K_0402_5% ESATA_DET#_R
PCH_GPIO57
R251 10K_0402_5%

U4F

T7	BMBUSY# / GPIO0	TACH4 / GPIO68	C40 PCH_GPIO68
A42	TACH1 / GPIO1	TACH5 / GPIO69	B41 PCH_GPIO69
H36	TACH2 / GPIO6	TACH6 / GPIO70	C41 PCH_GPIO70
E38	TACH3 / GPIO7	TACH7 / GPIO71	A40 PCH_GPIO71
C10	GPIO8		
C4	LAN_PHY_PWR_CTRL / GPIO12		
G2	GPIO15		
U2	SATA4GP / GPIO16		
D40	TACH0 / GPIO17		
T5	SCLOCK / GPIO22		
E8	GPIO24 / MEM_LED		
E16	GPIO27		
P8	GPIO28		
K1	STP_PCI# / GPIO34		
K4	GPIO35		
V8	SATA2GP / GPIO36		
M5	SATA3GP / GPIO37		
N2	SLOAD / GPIO38		
M3	SDATAOUT0 / GPIO39		
V13	SDATAOUT1 / GPIO48		
V3	SATA5GP / GPIO49		
D6	GPIO57		
		A20GATE	P4
		PECI	AU16 PCH_PECI_R
		RCIN#	P5 KB_RST#
		PROCPWRGD	AY11
		THRMTRIP#	AY10 PCH_THRMTRIP#_R
		INIT3_3V#	T14
		NC_1	AH8
		NC_2	AK11
		NC_3	AH10
		NC_4	AK10
		NC_5	P37

GPIO | CPU/MISC

A4	VSS_NCTF_1	VSS_NCTF_15	BG2 @T15 PAD
A44	VSS_NCTF_2	VSS_NCTF_16	BG48 @T16 PAD
A45	VSS_NCTF_3	VSS_NCTF_17	BH3 @T17 PAD
A46	VSS_NCTF_4	VSS_NCTF_18	BH47 @T18 PAD
A5	VSS_NCTF_5	VSS_NCTF_19	BJ4 @T20 PAD
A6	VSS_NCTF_6	VSS_NCTF_20	BJ44 @T22 PAD
B3	VSS_NCTF_7	VSS_NCTF_21	BJ45 @T24 PAD
B47	VSS_NCTF_8	VSS_NCTF_22	BJ46 @T26 PAD
BD1	VSS_NCTF_9	VSS_NCTF_23	BJ5 @T28 PAD
BD49	VSS_NCTF_10	VSS_NCTF_24	BJ6 @T30 PAD
BE1	VSS_NCTF_11	VSS_NCTF_25	C2 @T32 PAD
BE49	VSS_NCTF_12	VSS_NCTF_26	C48 @T34 PAD
BF1	VSS_NCTF_13	VSS_NCTF_27	D1 @T36 PAD
BF49	VSS_NCTF_14	VSS_NCTF_28	D49 @T38 PAD
		VSS_NCTF_29	E1 @T40 PAD
		VSS_NCTF_30	E49 @T42 PAD
		VSS_NCTF_31	F1 @T44 PAD
		VSS_NCTF_32	F49 @T46 PAD

PAD T19 @ PAD T21 @ PAD T23 @ PAD T25 @ PAD T27 @ PAD T29 @ PAD T31 @ PAD T33 @ PAD T35 @ PAD T37 @ PAD T39 @ PAD T41 @ PAD T43 @ PAD T45 @

NCTF

COUGARPOINT_FCBGA989

R236 10K_0402_5%
GATEA20 <32>
H_PECI <6,32>
R237 0_0402_5%
KB_RST# <32>
H_CPUPWRGD <6>
H_THRMTRIP# <6>
R239 390_0402_5%

INIT3_3V
This signal has weak internal PU, can't pull low

Intel schematic reviwe recommand.

PCH_GPIO68 R224 10K_0402_5%
KB_RST# R226 10K_0402_5%

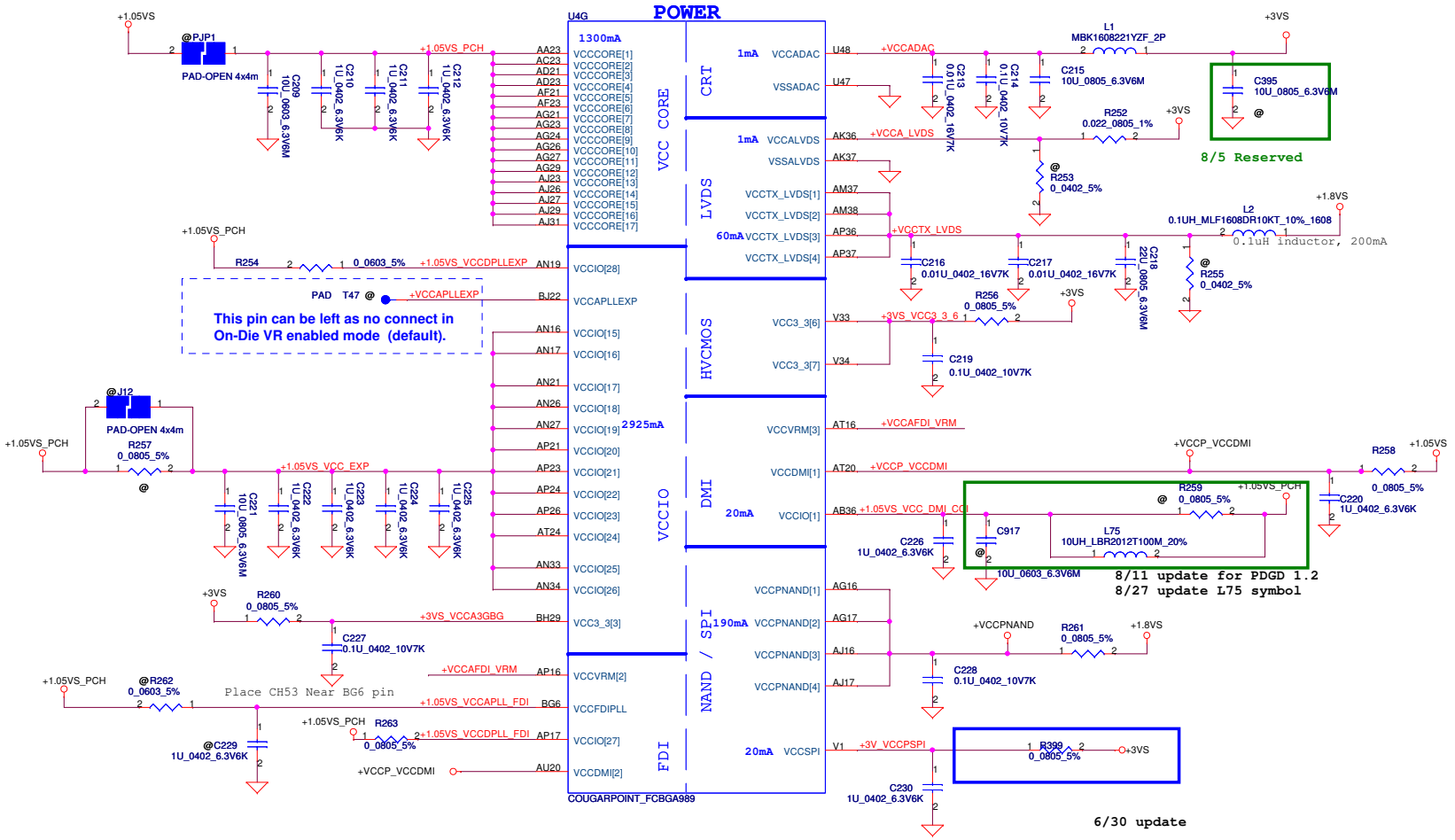
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: LA-6752P | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 19 of 50



PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

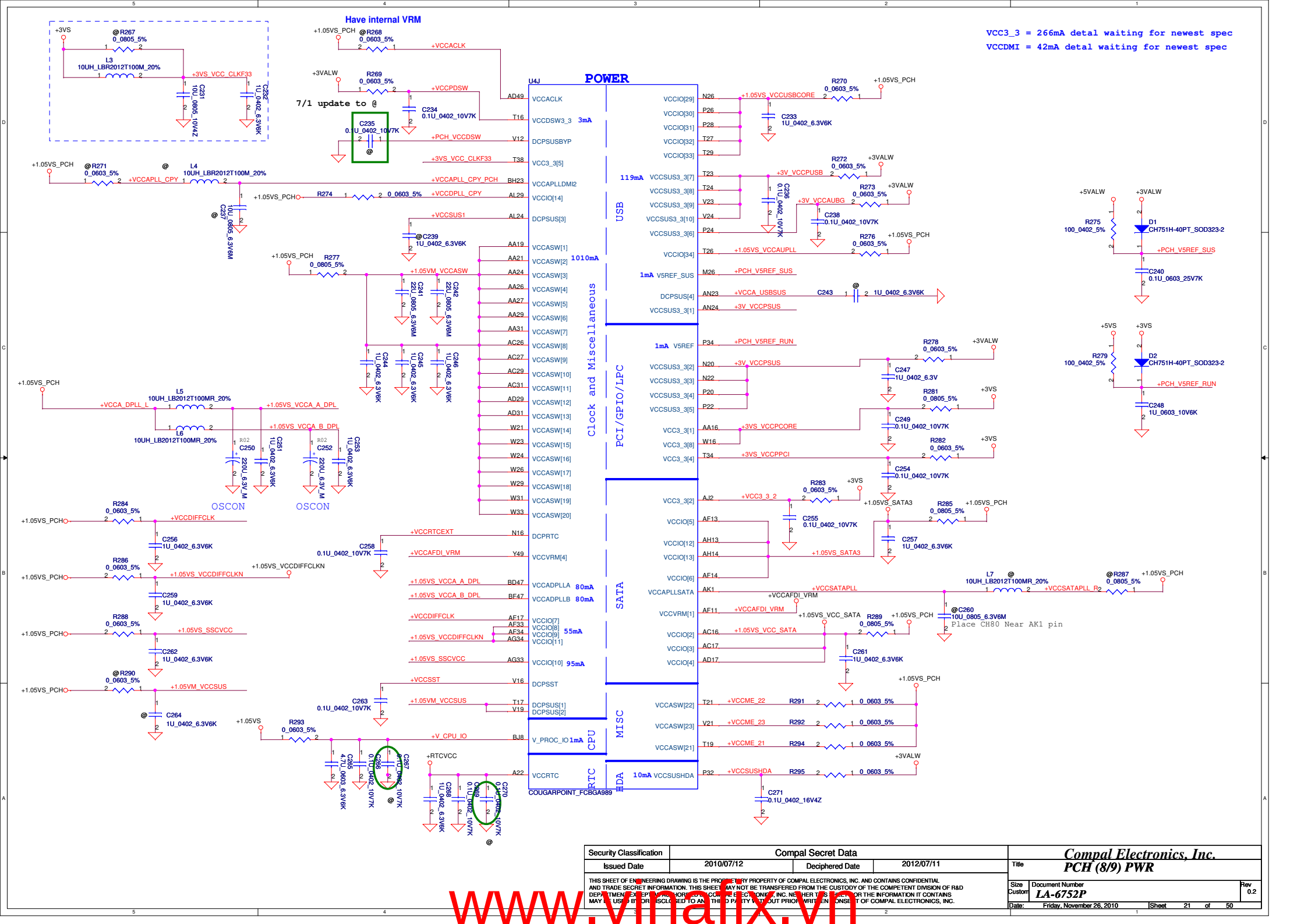
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: PCH (7/9) PWR

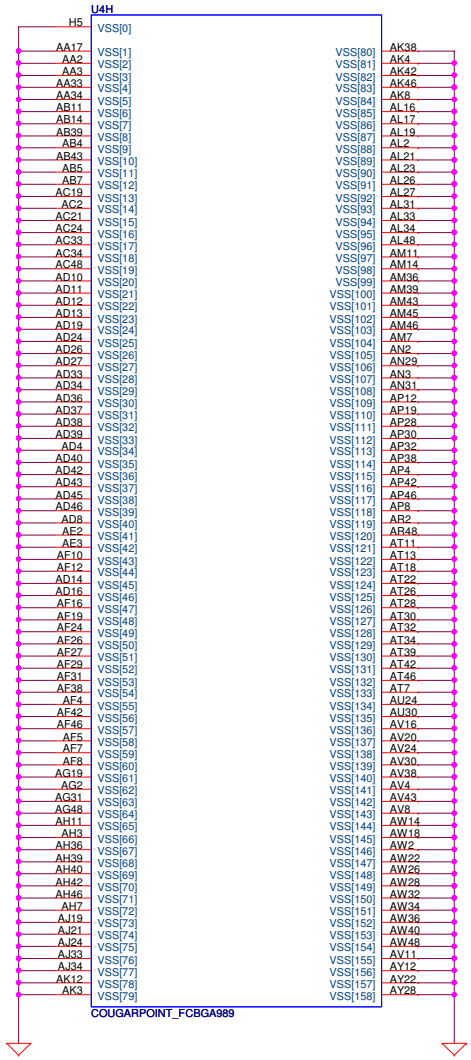
Size: Custom | Document Number: LA-6752P | Rev: 0.2

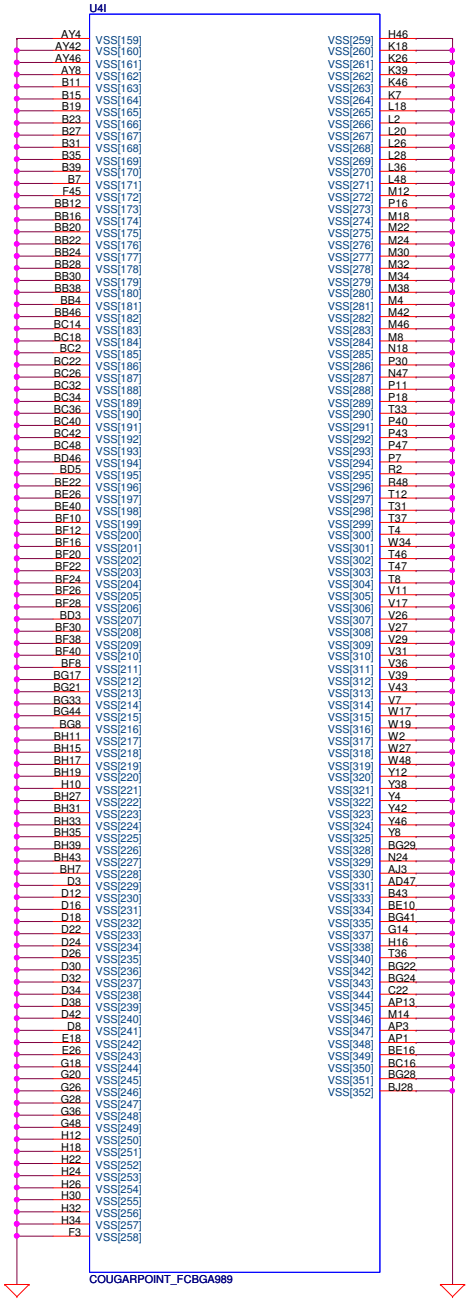
Date: Friday, November 26, 2010 | Sheet 20 of 50



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Title	Compal Electronics, Inc. PCH (8/9) PWR		
Size: Custom	Document Number: LA-6752P		Rev: 0.2
Date: Friday, November 26, 2010	Sheet 21 of 50		





Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

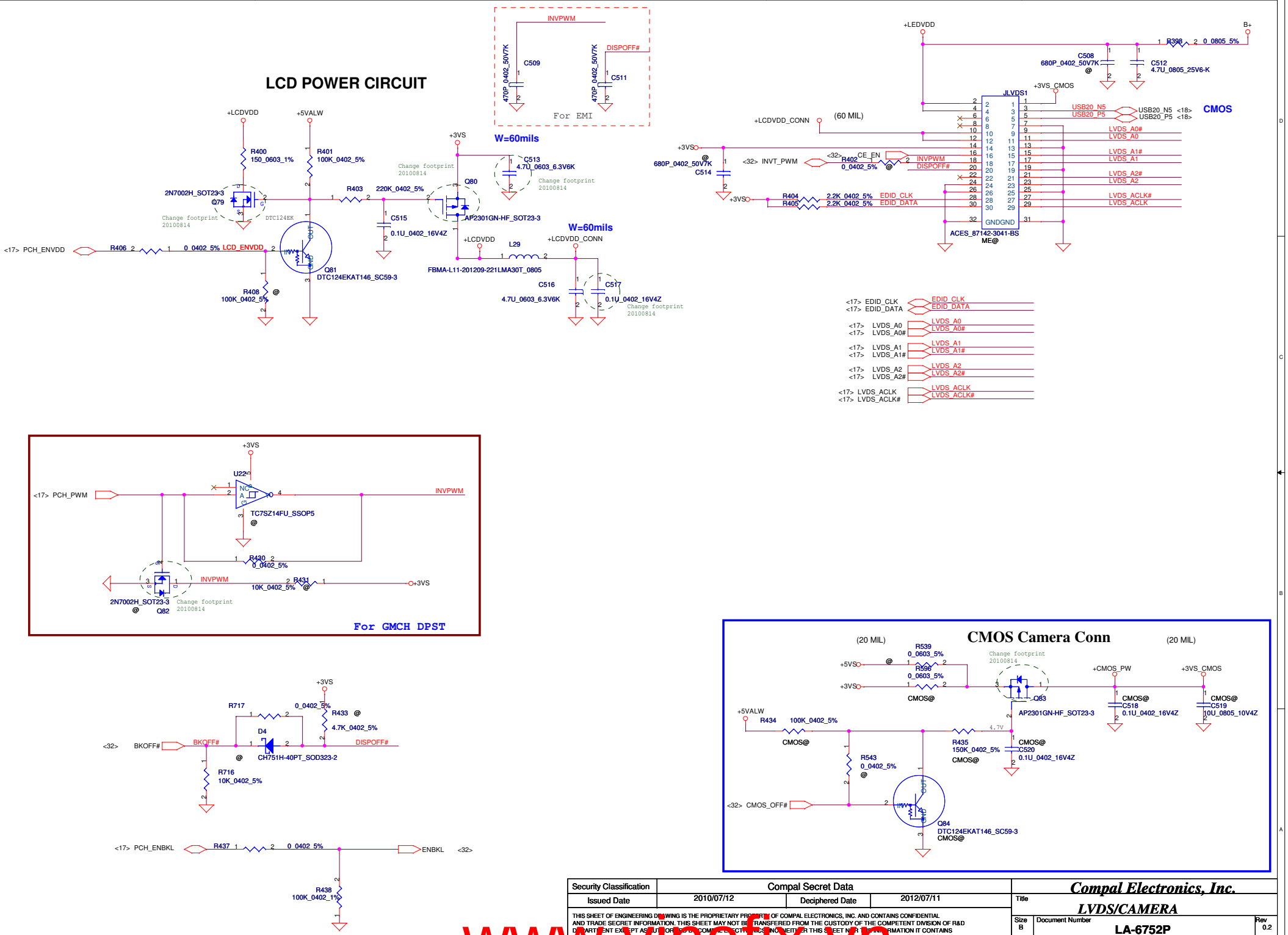
Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size: Custom | Document Number: LA-6752P | Rev: 0.2

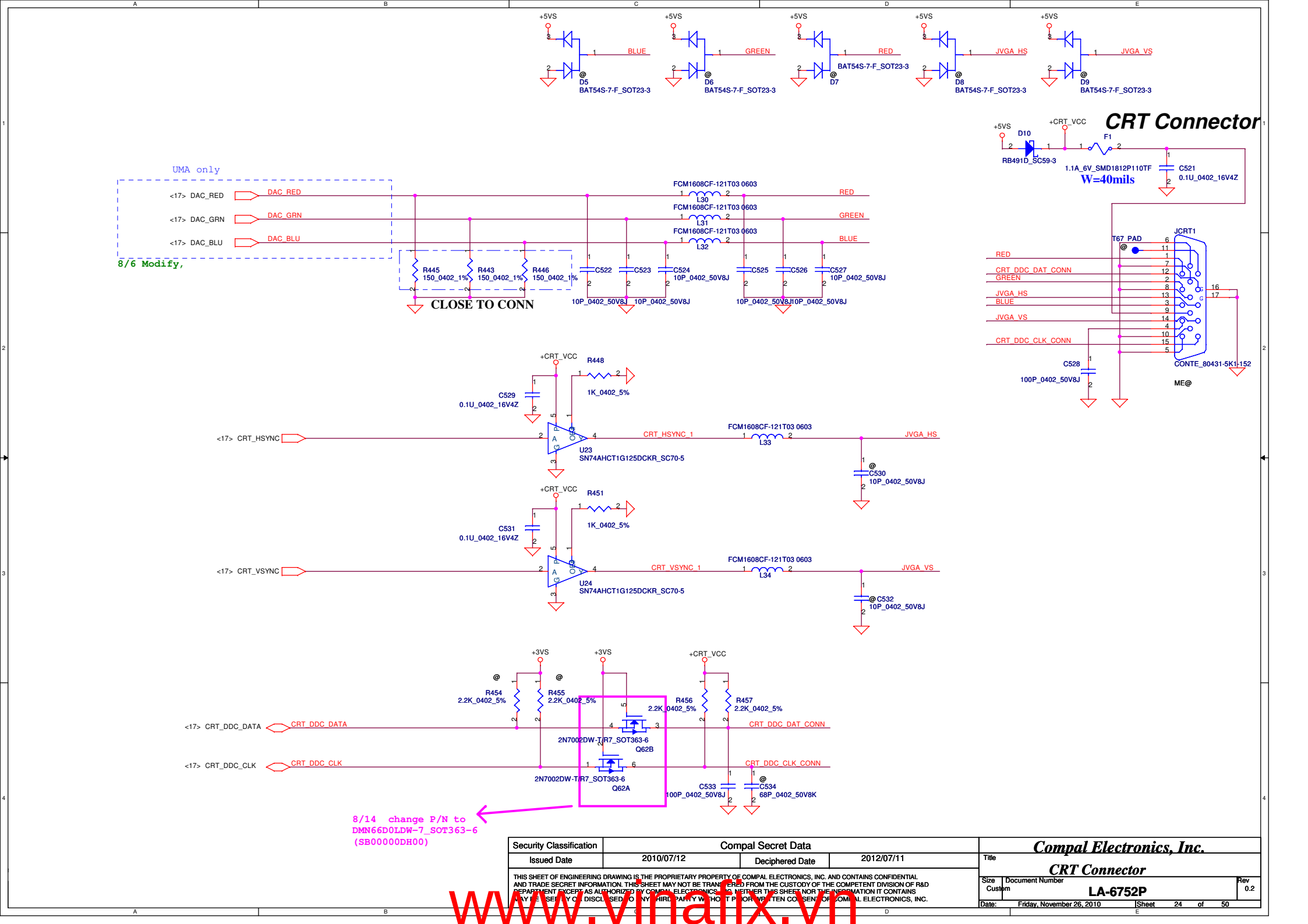
Date: Friday, November 26, 2010 | Sheet 22 of 50

LCD POWER CIRCUIT



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: LVDS/CAMERA			
Size: B	Document Number: LA-6752P		Rev: 0.2
Date: Friday, November 26, 2010	Sheet 23 of 50		



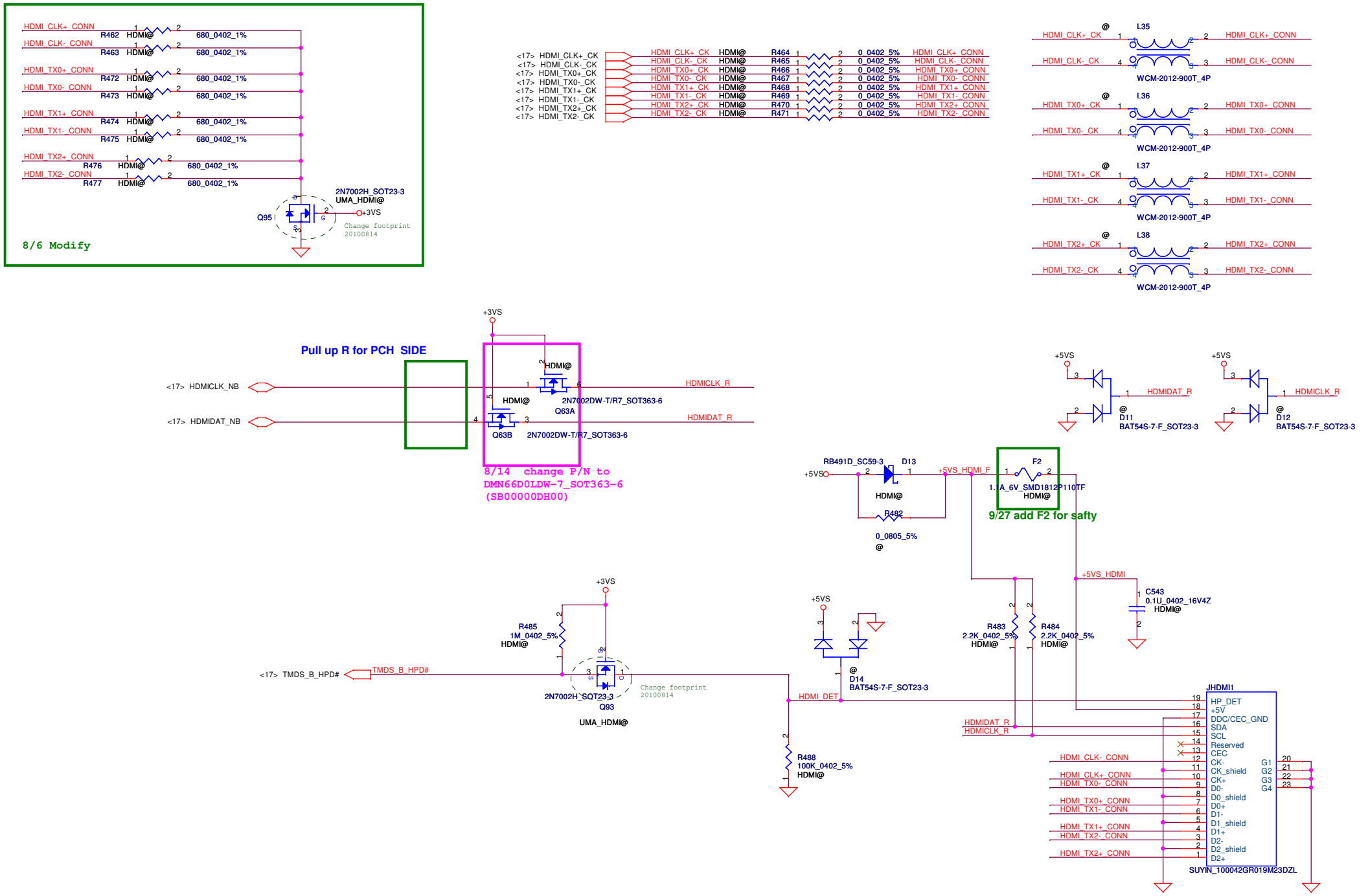
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: CRT Connector

Size: Custom | Document Number: LA-6752P | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 24 of 50



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

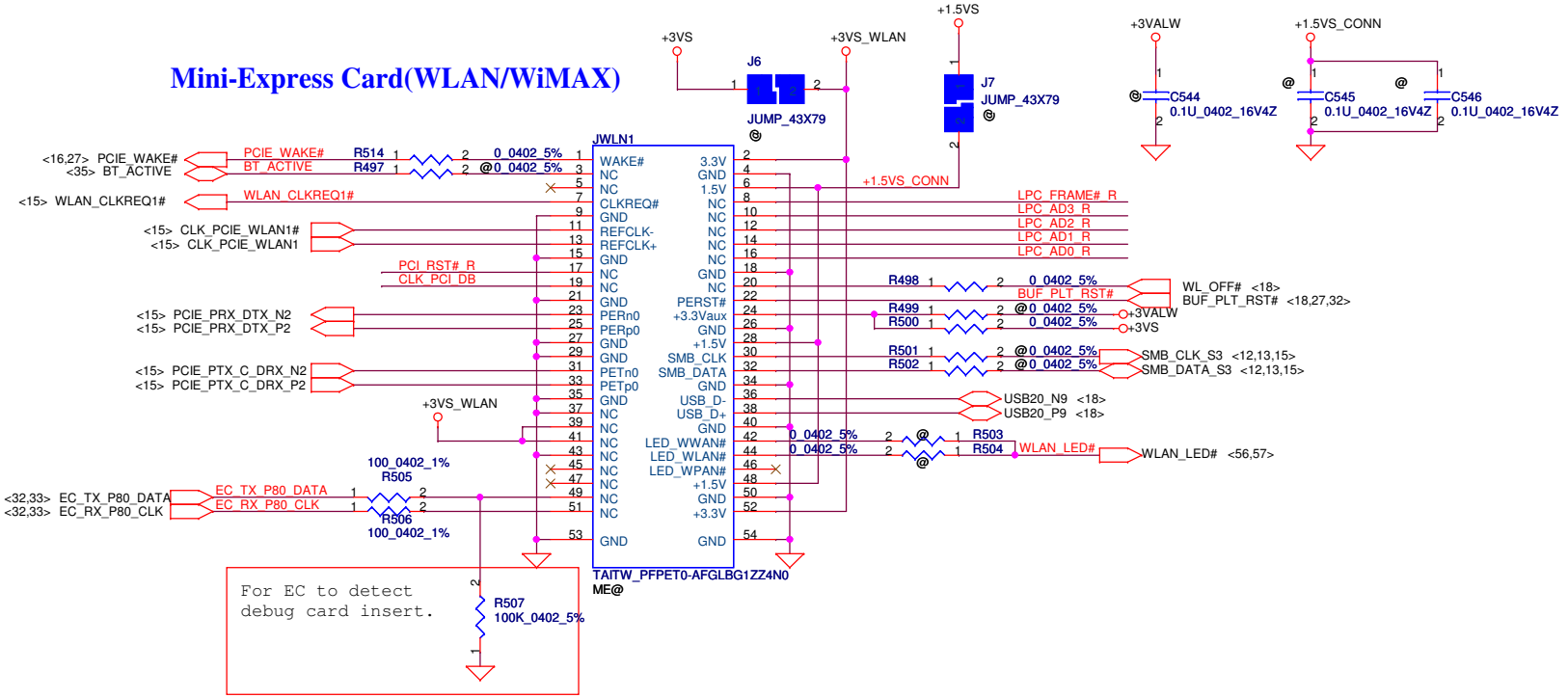
Compal Electronics,Ltd.

Title: HDMI CONN

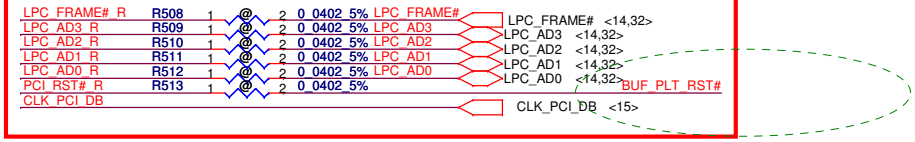
Size	Document Number	Rev
Custom	LA-6752P	0.2

Date: Friday, November 26, 2010 Sheet 25 of 50

Mini-Express Card for WLAN/WiMAX(Half)



Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title	Mini-Card/NEW Card/SIM		
Size	Document Number	LA-6752P	Rev 0.2
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+3VALW

+3V_LAN

J8

JUMP_43X79

Layout Notice : Place as close chip as possible.

Atheros request can't disable LAN power

+1.7_VDDCT

+1.7_LX

Close together

L39 4.7UH_SIA4012-4R7M_20%

C549 1000P_0402_50V7K

C548 0.1U_0402_16V4Z

C547 10U_0805_10V4Z

Note: Place Close to LAN chip
L39 DCR< 0.15 ohm
Rate current > 1A

Close to Pin40

Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable *	H
LED2	H:SWR Switch mode regulator Select * AR8151 Pin23=LED2. AR8152, Pin23 is CLKREQ	--

U26 8152@

S IC AR8152-AL1E QFN 40P E-LAN CTRL

Place Close to Chip

U26

LED0,1,2 intel Pull UP

Atheros 8151-AL1A

<15> PCIE_PRX_DTX_N1 C553 0.1U_0402_16V7K PCIE_PRX_C_DTX_N1

<15> PCIE_PRX_DTX_P1 C552 0.1U_0402_16V7K PCIE_PRX_C_DTX_P1

<15> PCIE_PTX_C_DRX_N1

<15> PCIE_PTX_C_DRX_P1

<15> CLK_PCIE_LAN# R517 0_0402_5% CLK_PCIE_LAN#_C

<15> CLK_PCIE_LAN R518 0_0402_5% CLK_PCIE_LAN_C

<18,26,32> BUF_PLT_RST# BUF_PLT_RST#

<16,26> PCIE_WAKE# R519 @0_0402_5% PCIE_WAKE#_R

<32> LAN_WAKE# R521 0_0402_5%

TX_N TX_P RX_N RX_P REFCLK_N REFCLK_P PERST# WAKE# SMCLK SMDATA TEST_RST TESTMODE XTLO XTLI CLKREQ# AVDDL AVDDL AVDDL AVDDL AVDDL AVDDL_REG GND

AR8151-AL1A_QFN40_5X5

GIGA@

C559 8152@ 0.1U_0402_16V4Z

LAN_XTALO LAN_XTALI

<15> CLKREQ_LAN# R525 GIGA@ 0_0402_5%

CLKREQ_LAN# CLKREQ_LAN#_R

+1.1_AVDDL

Near Pin13 Near Pin19 Near Pin31 Near Pin34 Near Pin6

Y4 25MHZ_20PF_7A25000012

C578 27P_0402_50V8J

C579 27P_0402_50V8J

LED_0 LED_1 LED_2

ACTIVITY LAN_LINK#

ACTIVITY <28> LAN_LINK# <28> CLKREQ_LAN#

R516 8152@ 0_0402_5%

no overclocking
PD 5.1K

R515 5.1K_0402_5%

TRXN0 TRXP0 TRXN1 TRXP1 TRXN2 TRXP2 TRXN3 TRXP3

MDI0- MDI0+ MDI1- MDI1+ MDI2- MDI2+ MDI3- MDI3+

MDI0- <28> MDI0+ <28> MDI1- <28> MDI1+ <28> MDI2- <28> MDI2+ <28> MDI3- <28> MDI3+ <28>

RBIAS LAN_RBIAS

R522 2.37K_0402_1%

Close Pin 10

C554 & C555 Close pin1 < 200mil
C557 & C558 Close pin < 400mil

VDD33 +3V_LAN

LX +1.7_LX

VDDCT +1.7_VDDCT

C561 0.1U_0402_16V4Z

DVDDL DVDDL_REG +1.1_DVDDL

AVDDH AVDDH AVDDH_REG +2.7_AVDDH

Near Pin9 Near Pin22 Near Pin16 Near Pin37 Near Pin24

Place Close to LAN chip

MDI0+ R526 49.9_0402_1% C574 1000P_0402_50V7K

MDI0- R527 49.9_0402_1% C575 0.1U_0402_16V4Z

MDI1+ R528 49.9_0402_1% C576 1000P_0402_50V7K

MDI1- R529 49.9_0402_1% C577 0.1U_0402_16V4Z

MDI2+ R530 GIGA@ 49.9_0402_1% C580 1000P_0402_50V7K

MDI2- R531 GIGA@ 49.9_0402_1% C581 0.1U_0402_16V4Z

MDI3+ R532 GIGA@ 49.9_0402_1% C582 1000P_0402_50V7K

MDI3- R533 GIGA@ 49.9_0402_1% C583 0.1U_0402_16V4Z

Note 1 : 8152 no mount MDI3+, MDI3-, MDI2-, MDI2+ resister and cap

Note 2 : C574, C576, C580, C582, reserved for EMI.

	Pin4	Configure R525	Configure C559		Pin23	Configure R516
AR8152	VDDCT_REG		*		CLKREQn	*
AR8151	CLKREQn	*			LED[2]	

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: LAN-AR8151/8152

Size: Custom | Document Number: LA-6752P | Rev: 0.2

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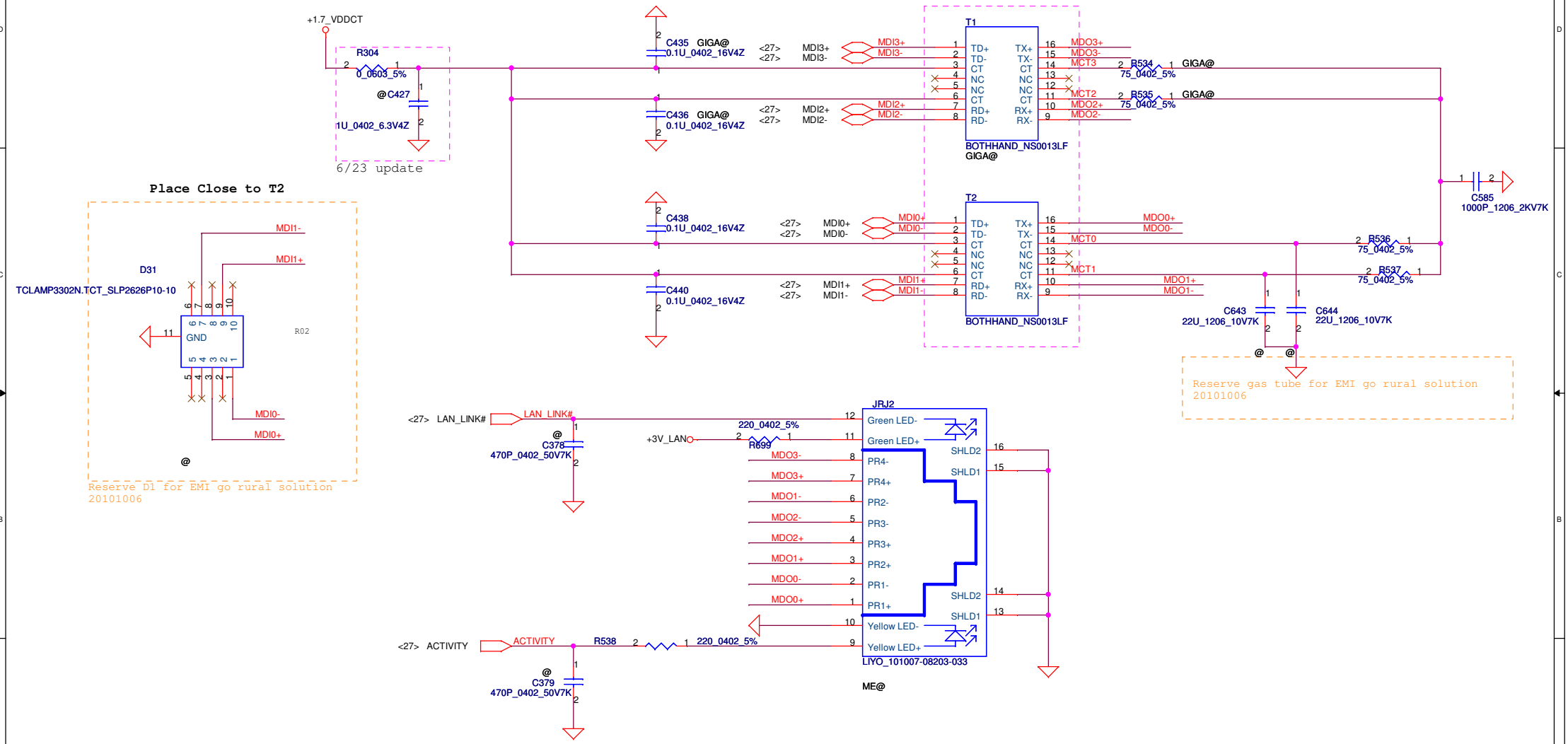
8/23 Change T1,T2 P/N to SP050006E00



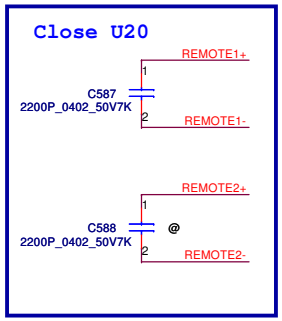
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

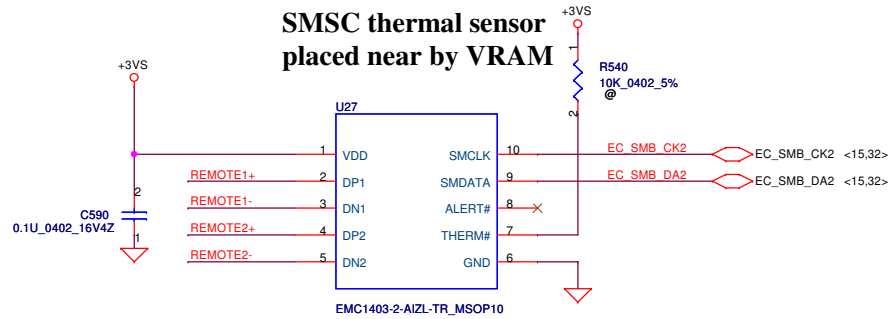
Compal Electronics, Inc.

Title: **LAN_Transformer**

Size	Document Number	Rev
B	LA-6752P	0.2

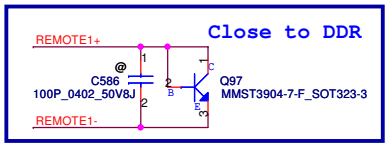
Date: Friday, November 26, 2010 Sheet 28 of 50

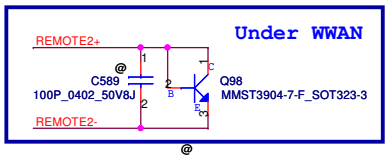




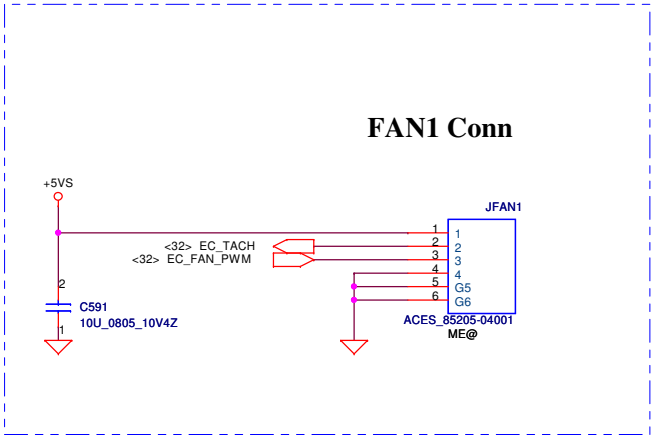
Address 1001_101xb

10/5 change P/N to SA000046C00





REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

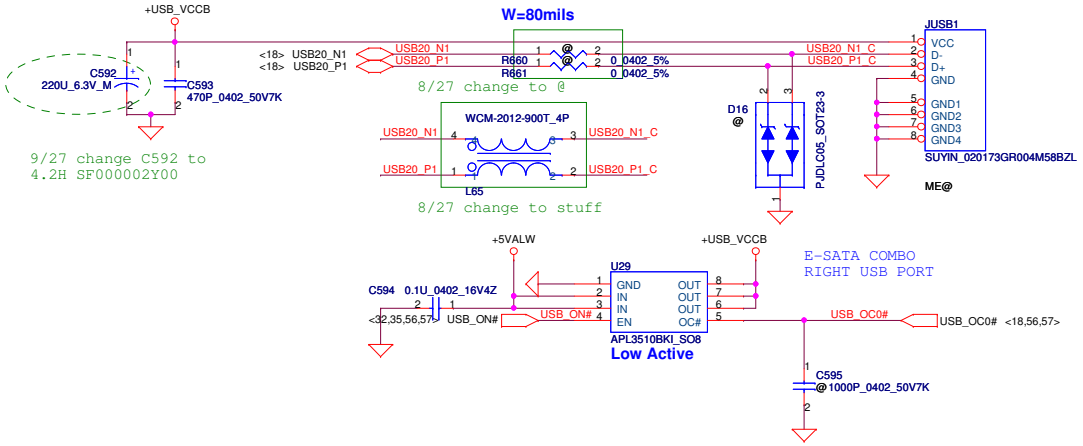
Compal Electronics,Ltd.

Title: EMC1403_Thermal sensor/FAN

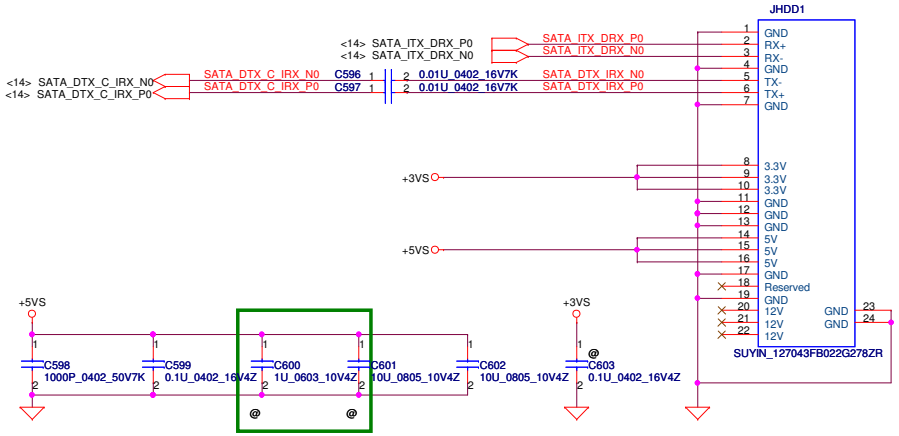
Size: Custom | Document Number: LA-6752P | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 29 of 50

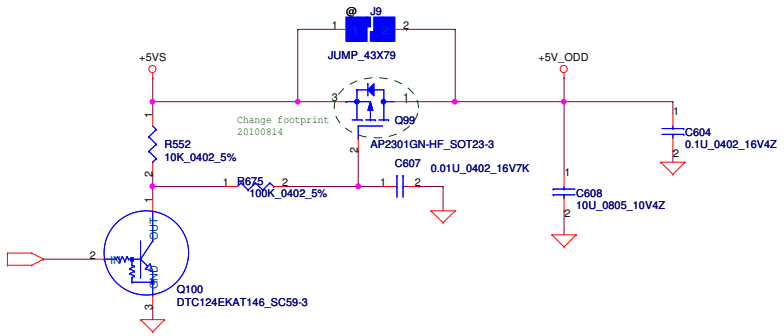
Left USB Conn.



SATA HDD Conn.



ODD Power Control

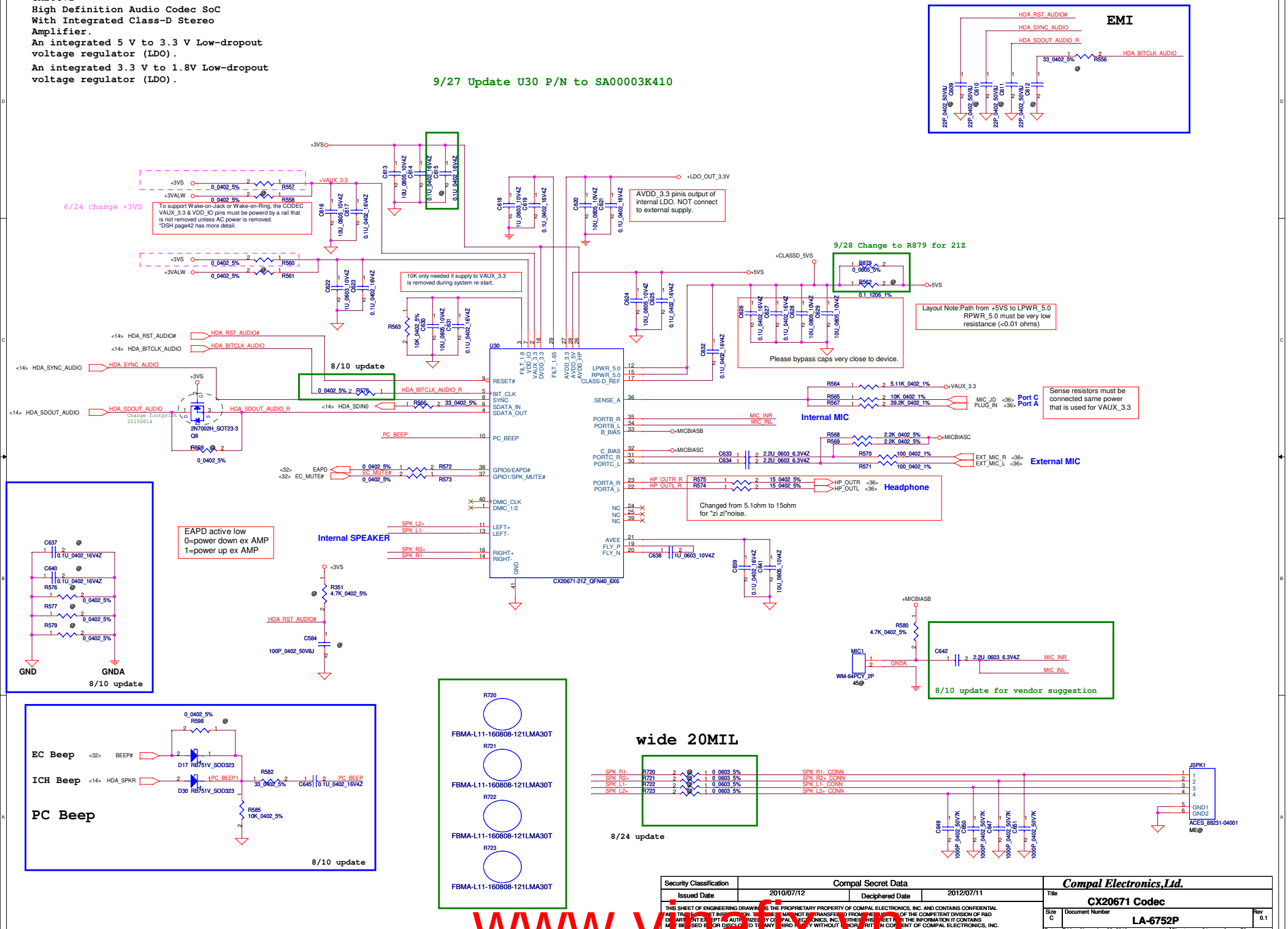


Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title: HDD/ODD Connector			
Size: B	Document Number: LA-6752P		Rev: 0.2
Date: Friday, November 26, 2010	Sheet 30 of 50		

CX20671
High Definition Audio Codec SoC
With Integrated Class-D Stereo
Amplifier.
An integrated 5 V to 3.3 V Low-dropout
voltage regulator (LDO).
An integrated 3.3 V to 1.8V Low-dropout
voltage regulator (LDO).

9/27 Update U30 P/N to SA00003K410



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

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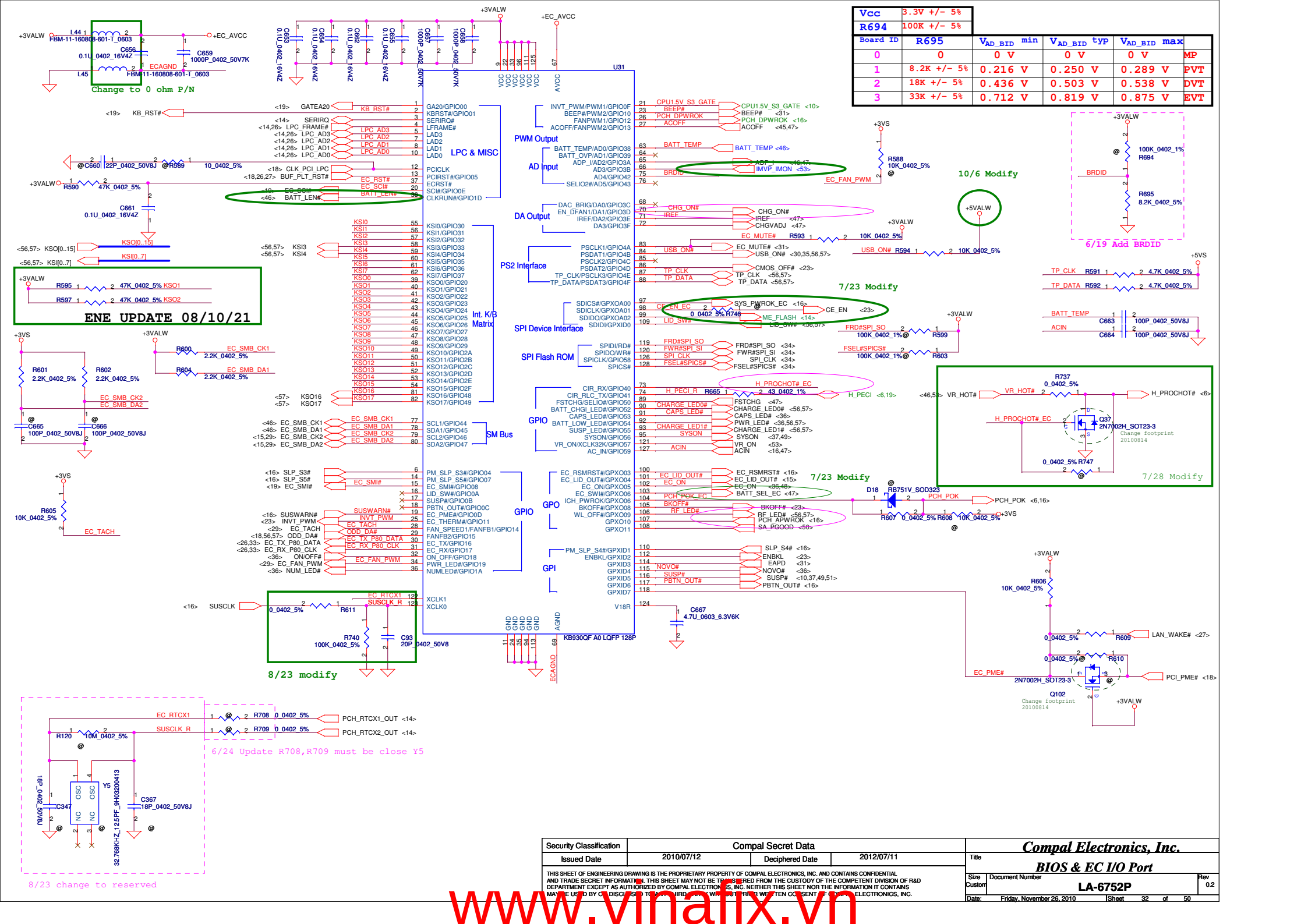
Compal Electronics,Ltd.

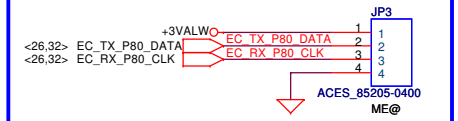
Title: CX20671 Codec

Size: C | Document Number: LA-6752P | Rev: 0.1

Date: Friday, November 26, 2010 | Sheet 31 of 50

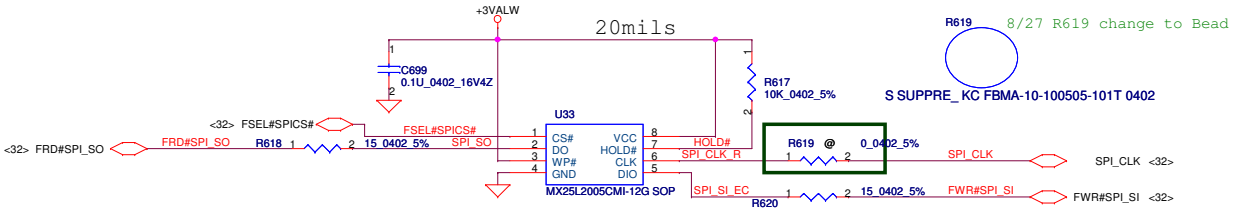


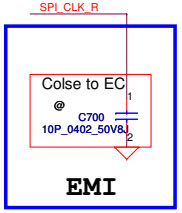
EC DEBUG PORT

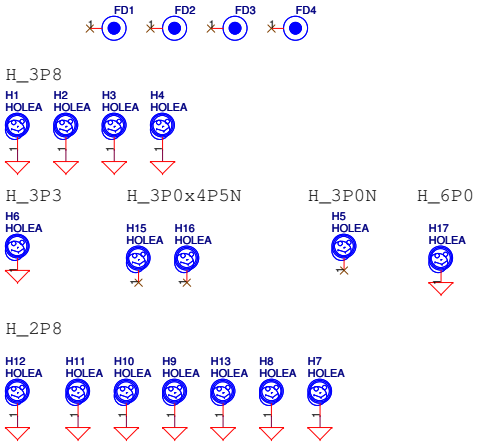


Compal Electronics, Inc.		
Title: KB /SW /LPC Debug Conn.		
Size: B	Document Number: LA-6752P	Rev: 0.2
Date: Friday, November 26, 2010	Sheet 33 of 50	

FOR EC 128KB SPI ROM
(150mil PACKAGE)
SA00003FL10
SA00003JD00

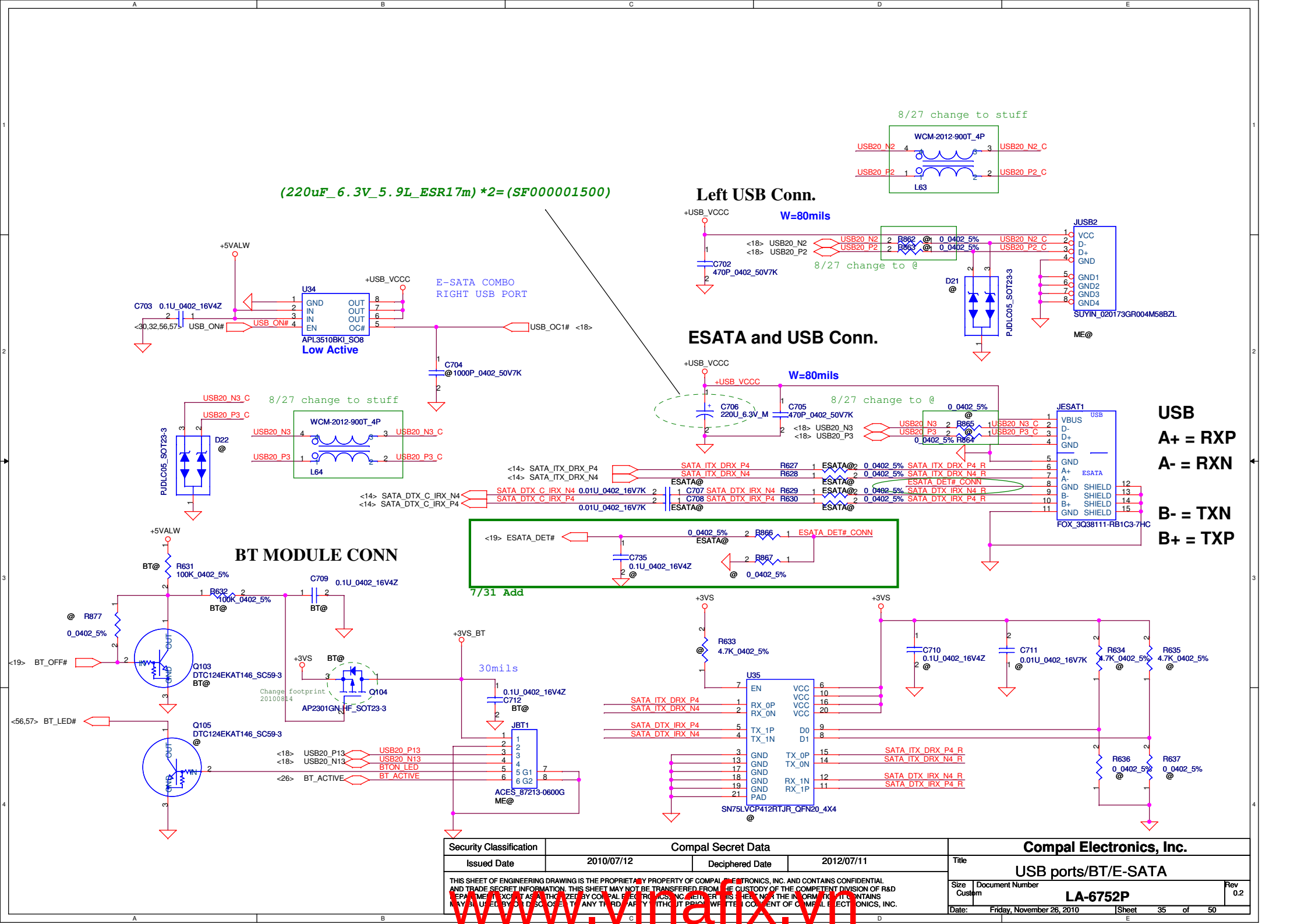






Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.			
Title	LED/EC SPI ROM		
Size B	Document Number LA-6752P		Rev 0.2
Date: Friday, November 26, 2010	Sheet 34 of 50		



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

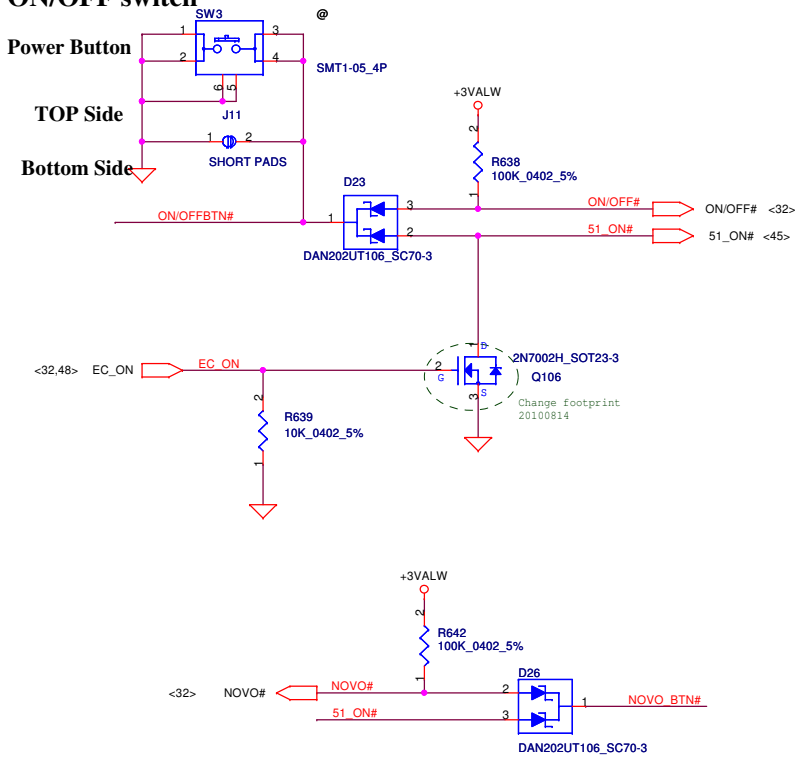
Compal Electronics, Inc.

Title: USB ports/BT/E-SATA

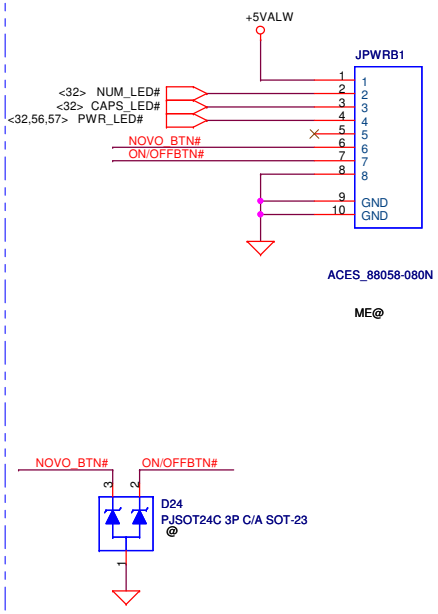
Size	Document Number	Rev
Custom	LA-6752P	0.2

Date: Friday, November 26, 2010 | Sheet 35 of 50

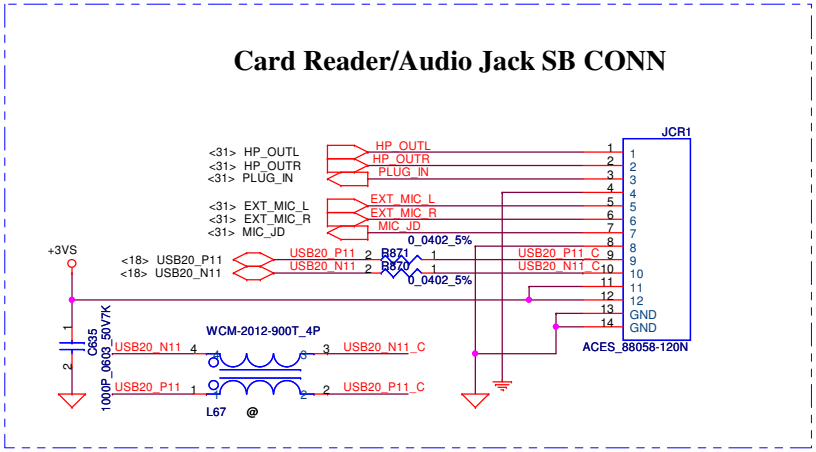
ON/OFF switch



Power Bottom Board Conn. 8pin



Card Reader/Audio Jack SB CONN



EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

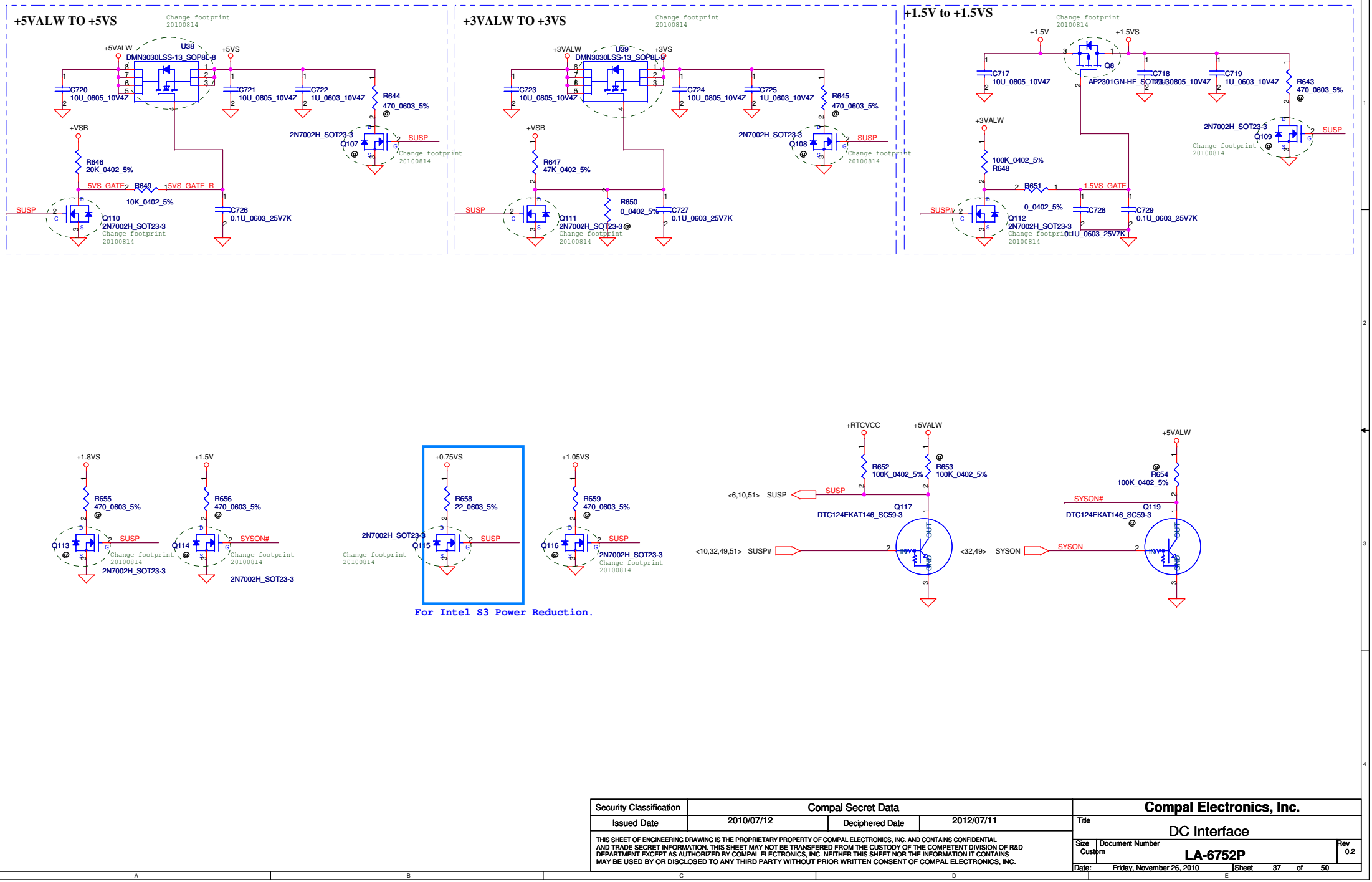
Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics,Ltd.

Title: **other IO connector**

Size	Document Number	Rev
Custom	LA-6751P	0.2

Date: Friday, November 26, 2010 | Sheet 36 of 50



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

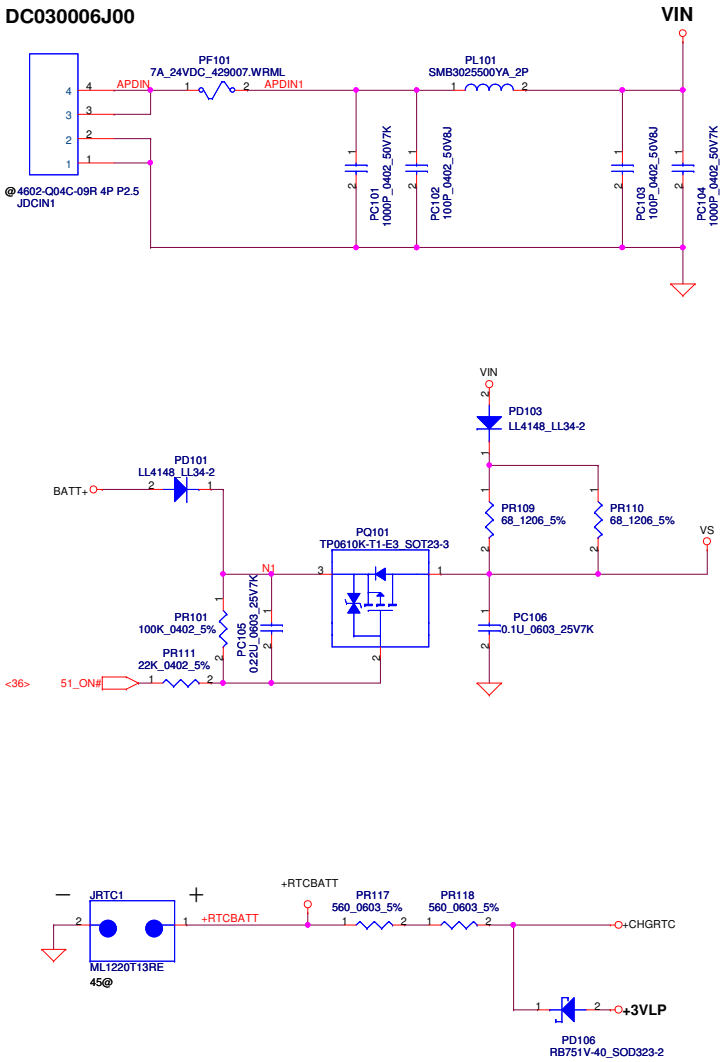
Compal Electronics, Inc.

Title: DC Interface

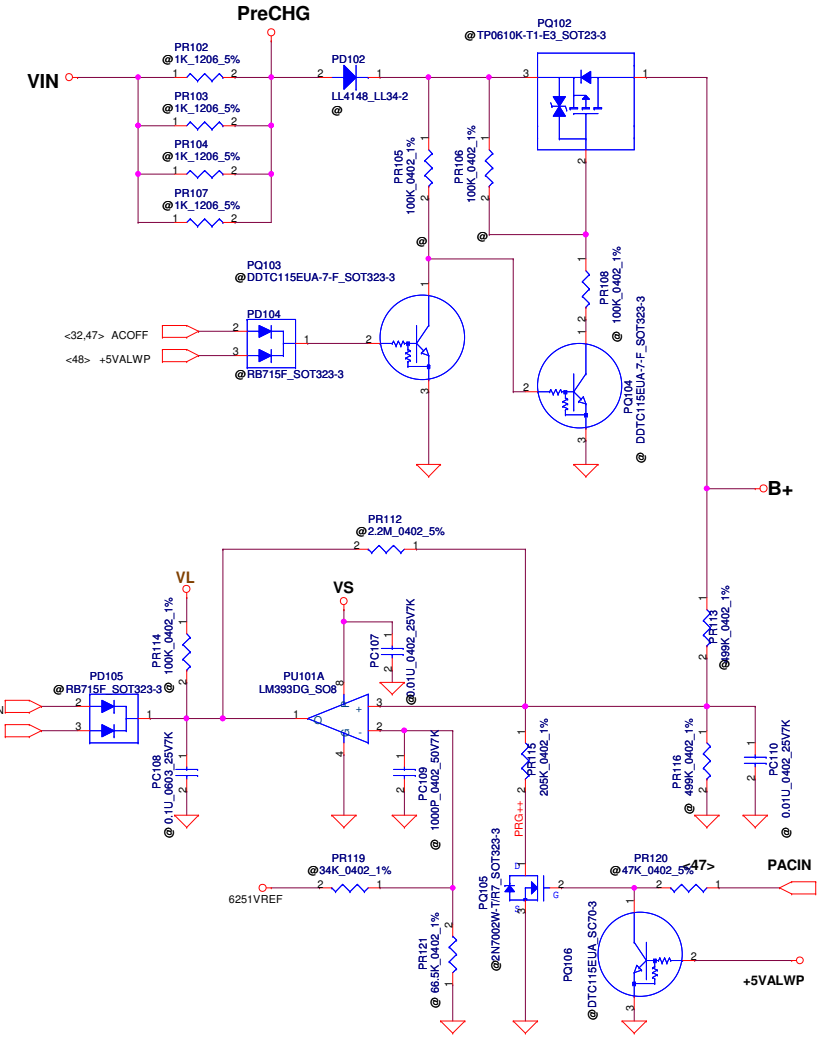
Size: Custom | Document Number: LA-6752P | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 37 of 50

DC030006J00



Precharge detector
15.97V/14.84V FOR ADAPTOR



ACIN

Precharge detector	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

BATT ONLY

Precharge detector	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

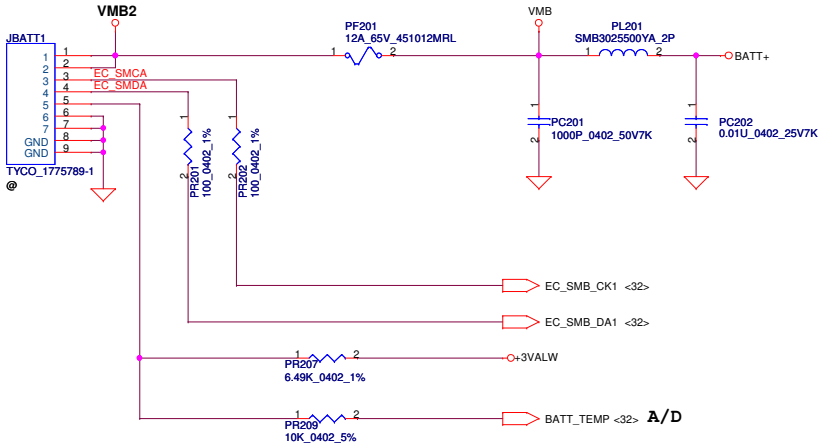
Compal Electronics, Inc.

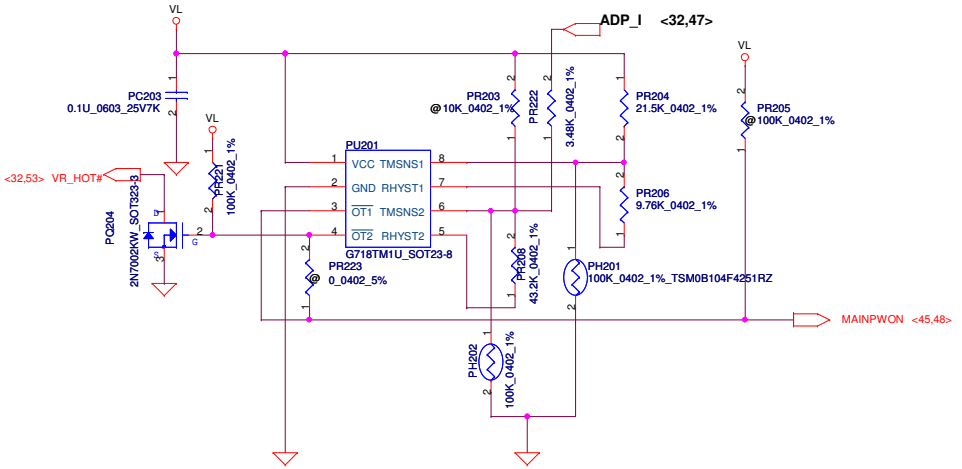
Title: PWR DCIN / Vin Detector /Pre-charge

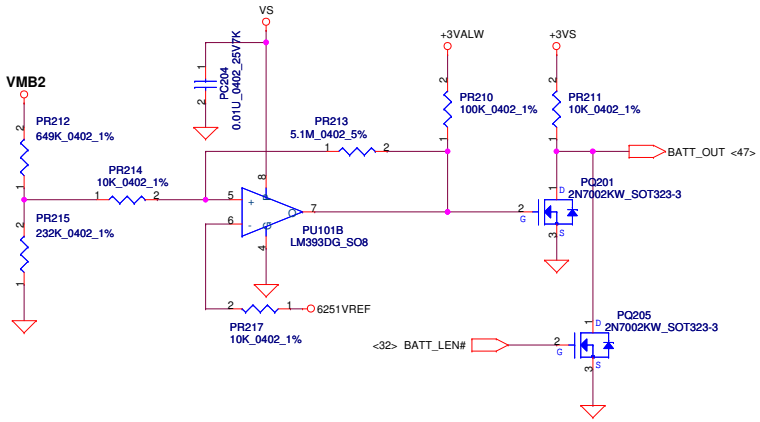
Size: Custom | Document Number: PIWG1/G2(LA-6759P/LA-675AP) | Rev: 0.1

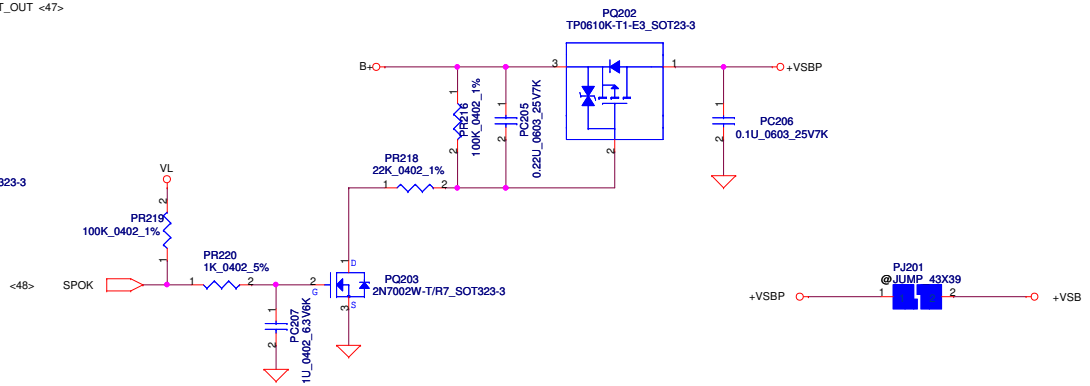
Date: Friday, November 26, 2010 | Sheet 45 of 54

PH201 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



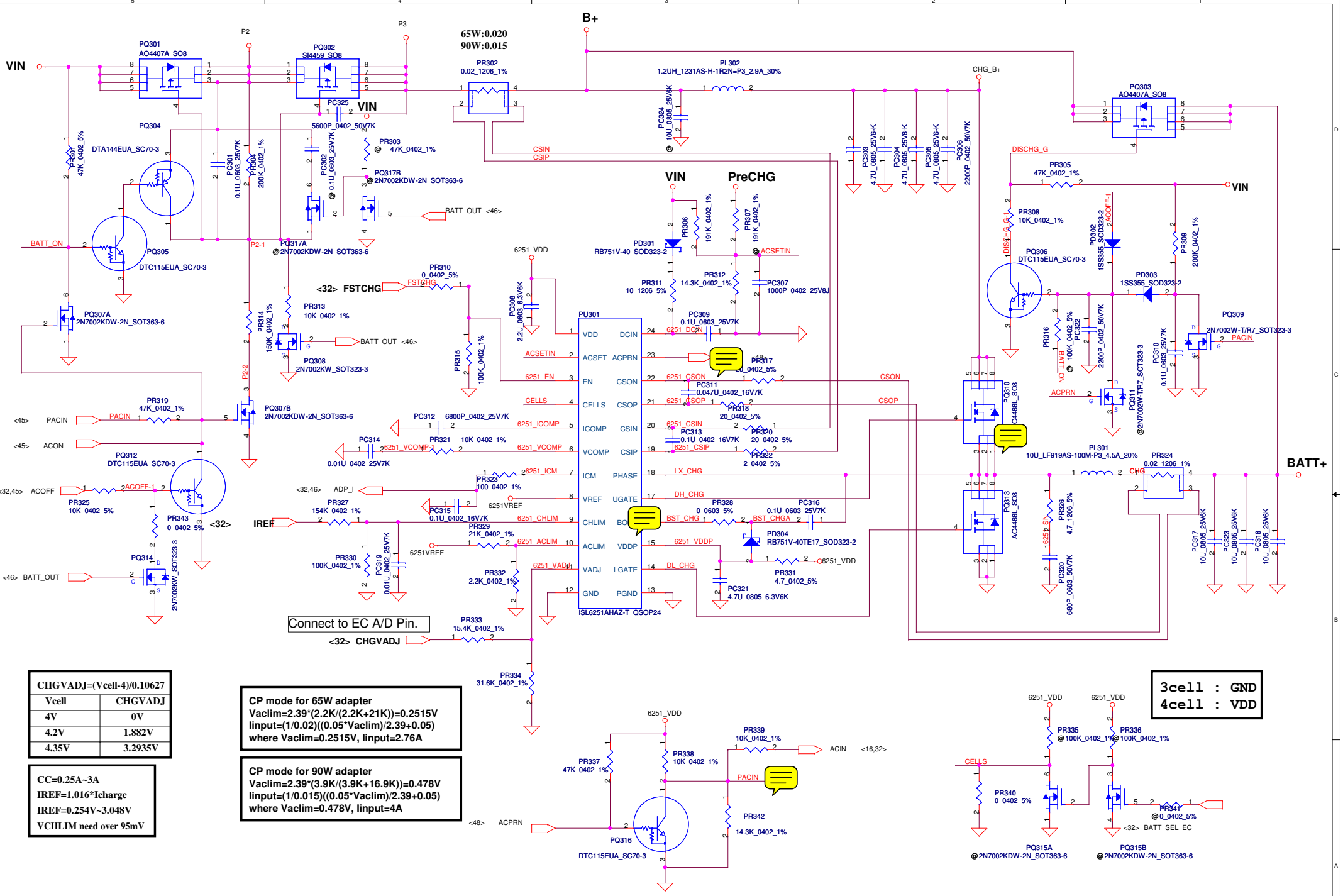






Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.	
Title	PWR-BATTERY CONN/OTP
Size: Custom	Document Number: PIWG1/G2(LA-6759P/LA-675AP)
Rev	0.1
Date: Friday, November 26, 2010	Sheet 46 of 54



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

CP mode for 65W adapter
Vaclim=2.39*(2.2K/(2.2K+21K))=0.2515V
linput=(1/0.02)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.2515V, linput=2.76A

CP mode for 90W adapter
Vaclim=2.39*(3.9K/(3.9K+16.9K))=0.478V
linput=(1/0.015)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.478V, linput=4A

3cell : GND
4cell : VDD

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

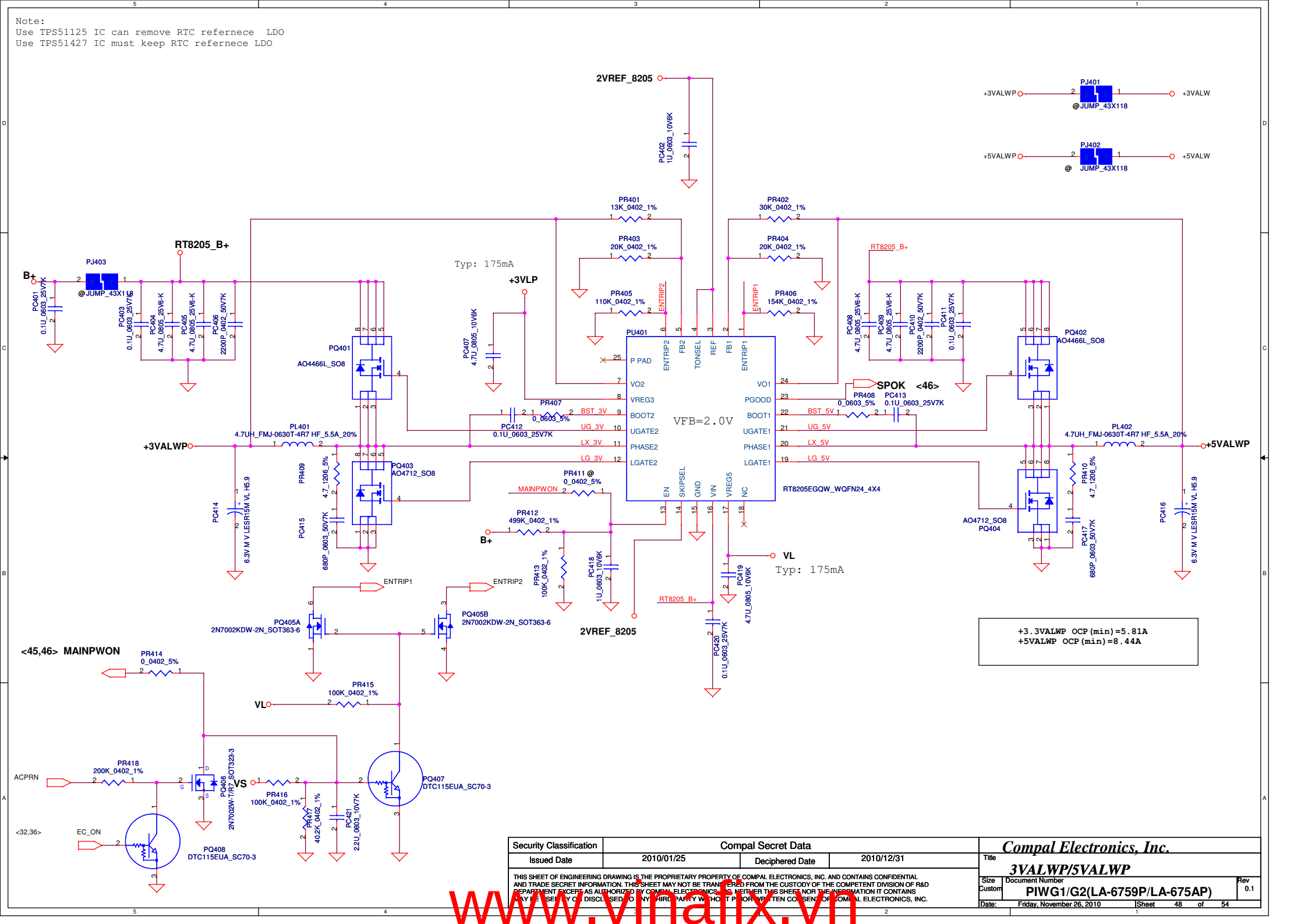
Compal Electronics, Inc.

Title: CHARGER

Size: | Document Number: PIWG1/G2(LA-6759P/LA-675AP) | Rev: 0.2

Date: Friday, November 26, 2010 | Sheet 47 of 54

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



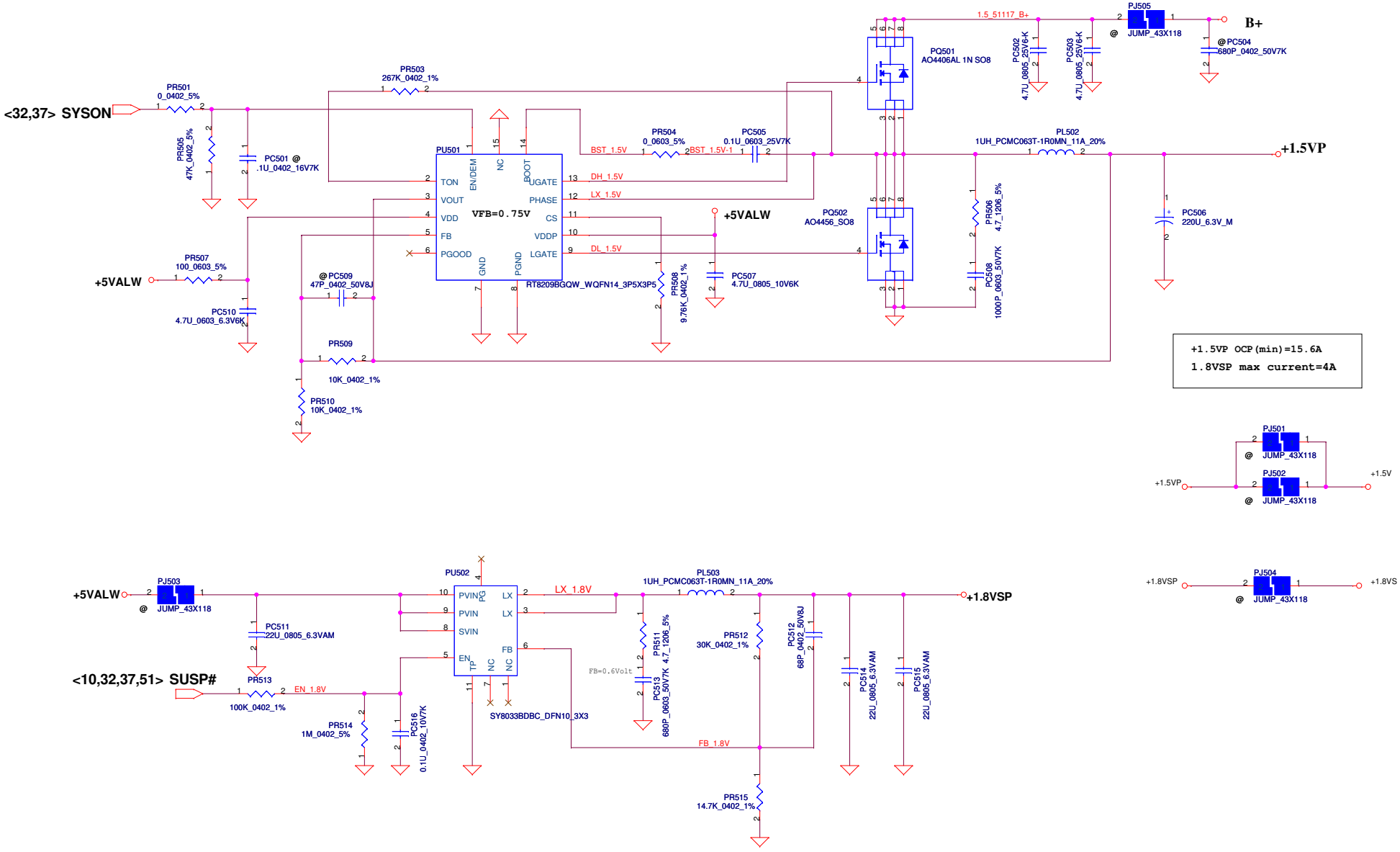
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

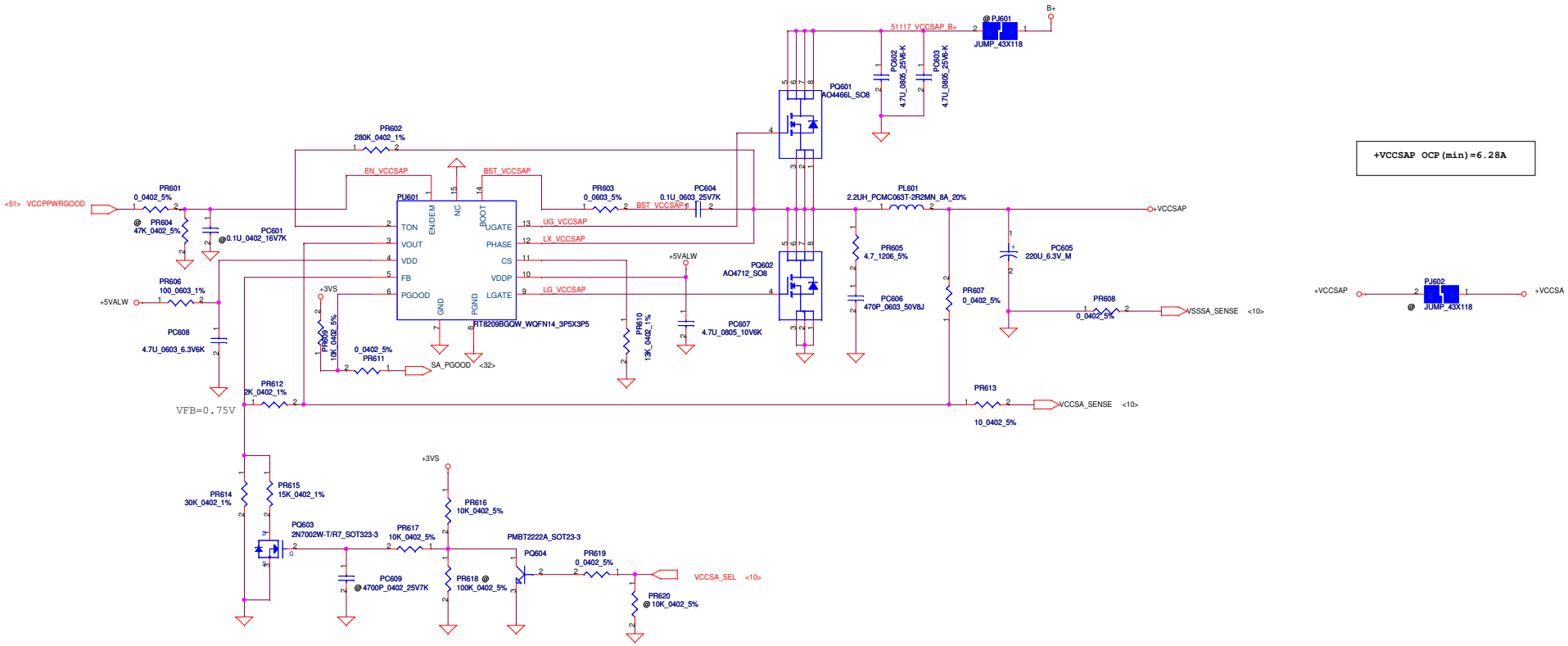
Size: Custom | Document Number: PIWG1/G2(LA-6759P/LA-675AP) | Rev: 0.1

Date: Friday, November 26, 2010 | Sheet 48 of 54



Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.	
Title	PWR-+1.5VP/+1.8VSP
Size: Custom	Document Number: PIWG1/G2(LA-6759P/LA-675AP)
Rev	0.1
Date: Friday, November 26, 2010	Sheet 49 of 54



+VCCSAP OCP(min)=6.28A

VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.725V	No/Yes
1	1	0.675V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR +VCCSAP

Size	Document Number	Rev
C	PIWG1/G2(LA-6759P/LA-675AP)	0.1

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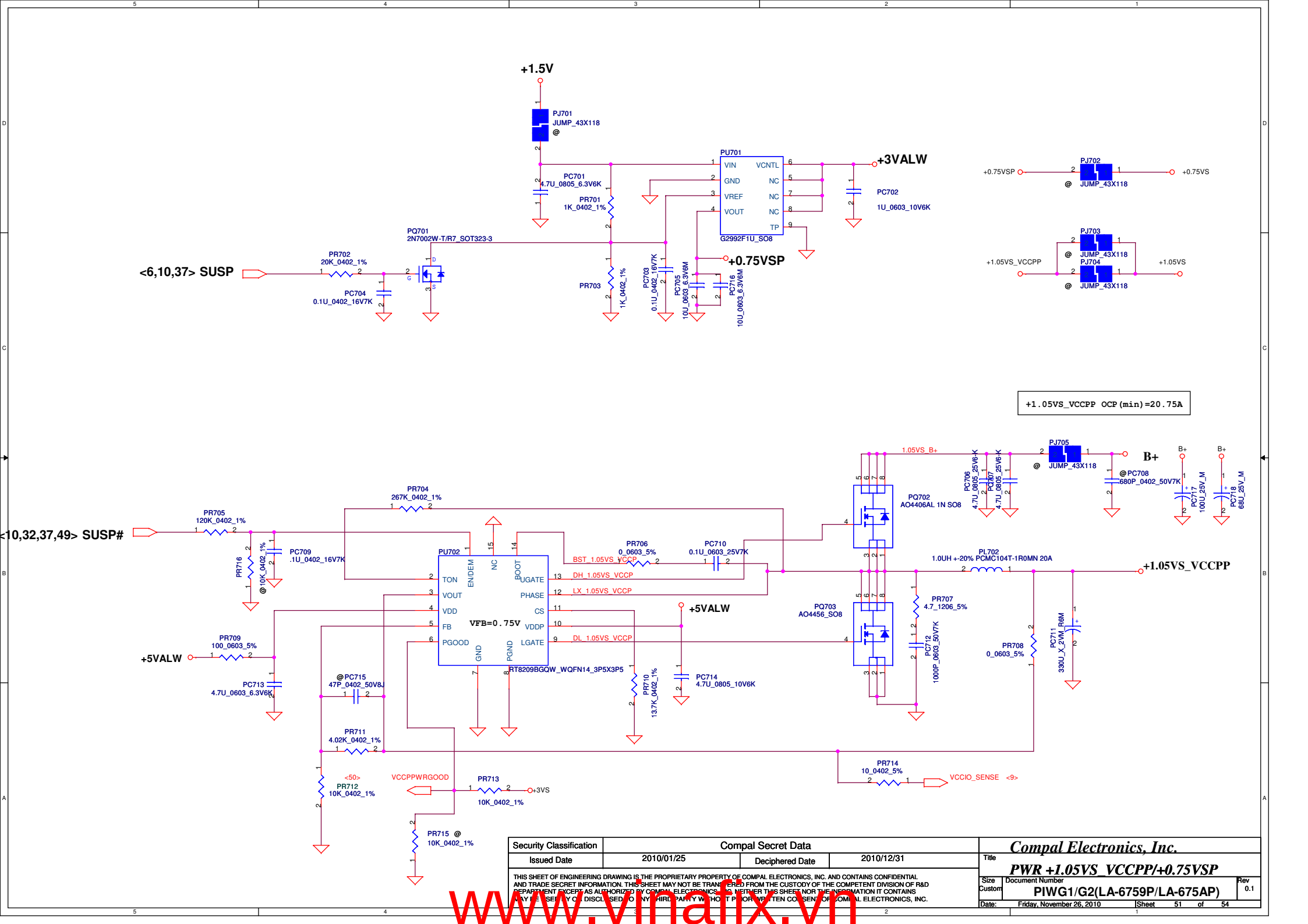

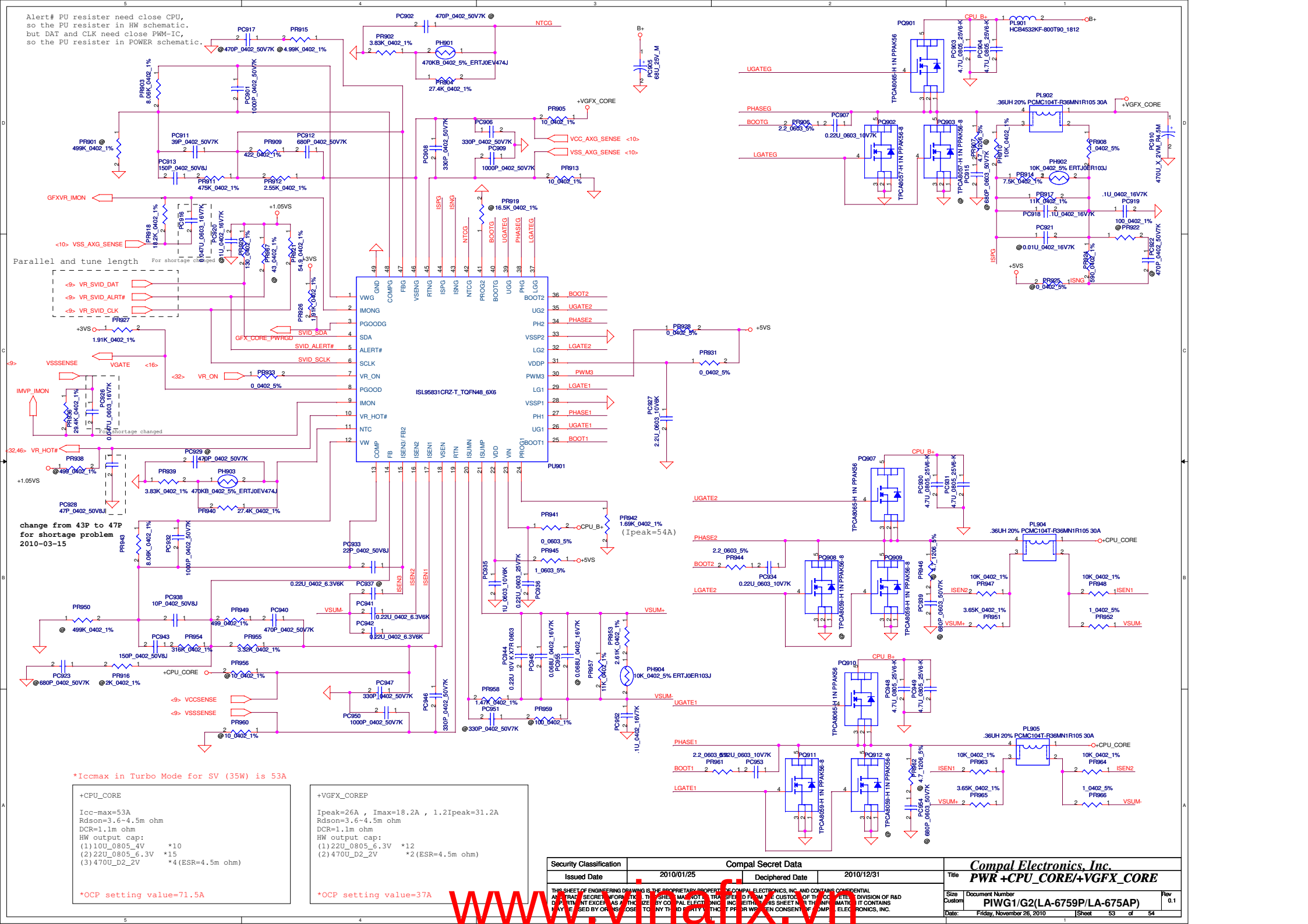
Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.
Parallel and tune length
change from 43P to 47P
for shortage problem
2010-03-15
ISL95831CRZ-T_TQFN48_6X6
PU901
*Iccmax in Turbo Mode for SV (35W) is 53A
+CPU_CORE
Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)10U_0805_4V *10
(2)22U_0805_6.3V *15
(3)470U_D2_2V *4(ESR=4.5m ohm)
*OCP setting value=71.5A
+VGFX_COREP
Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)22U_0805_6.3V *12
(2)470U_D2_2V *2(ESR=4.5m ohm)
*OCP setting value=37A
Security Classification
Compal Secret Data
Issued Date
2010/01/25
Deciphered Date
2010/12/31
Compal Electronics, Inc.
PWR +CPU_CORE/+VGFX_CORE
PIWG1/G2(LA-6759P/LA-675AP)
Rev 0.1
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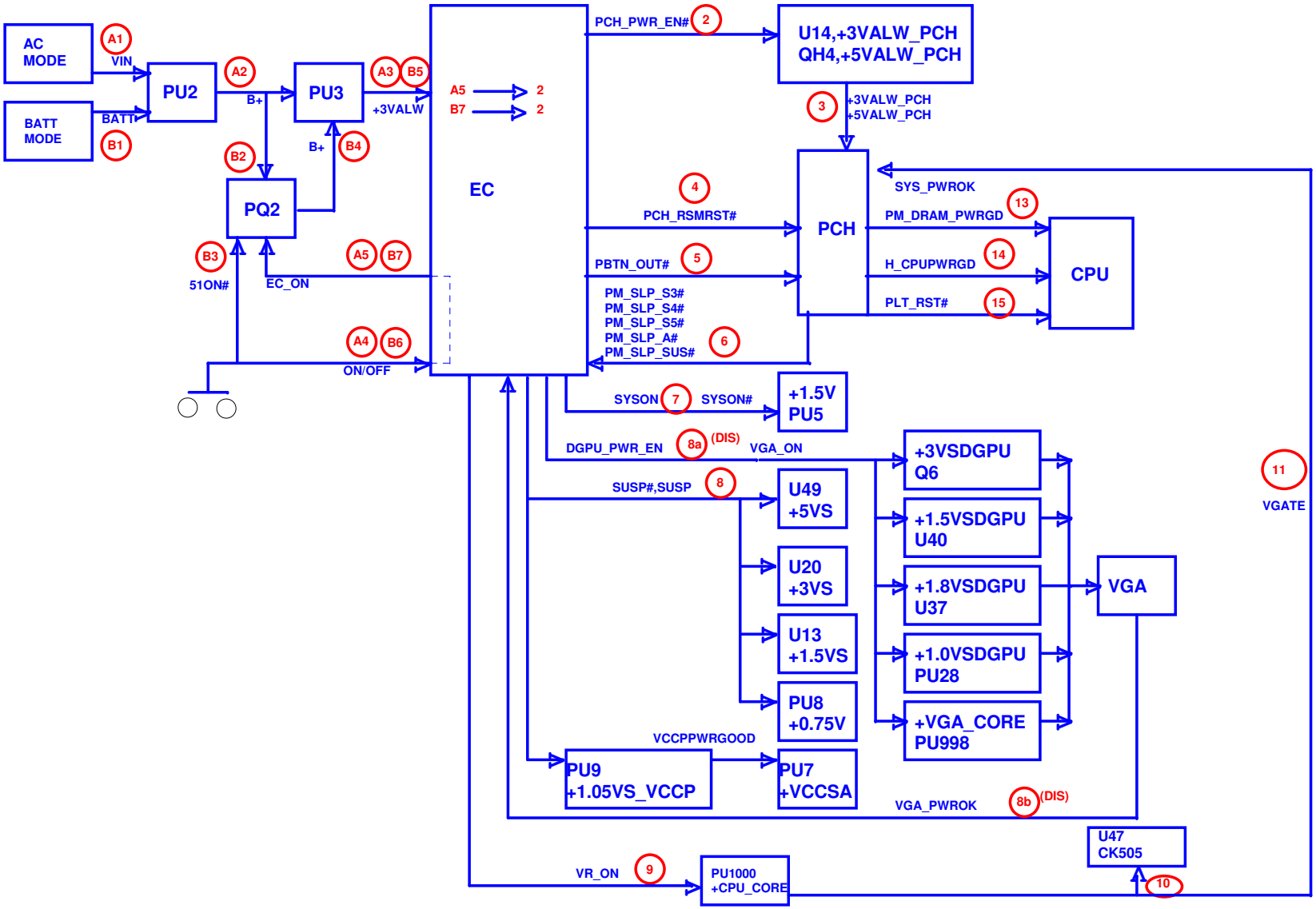
www.vinafix.vn

Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Compal Electronics, Inc.		
Title: PIR (PWR)		
Size: Custom	Document Number: PIWG1/G2(LA-6759P/LA-675AP)	Rev: 0.1
Date: Friday, November 26, 2010	Sheet 54 of 54	



Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: Power sequence

Size	Document Number	Rev
Custom	LA-6752P	0.2

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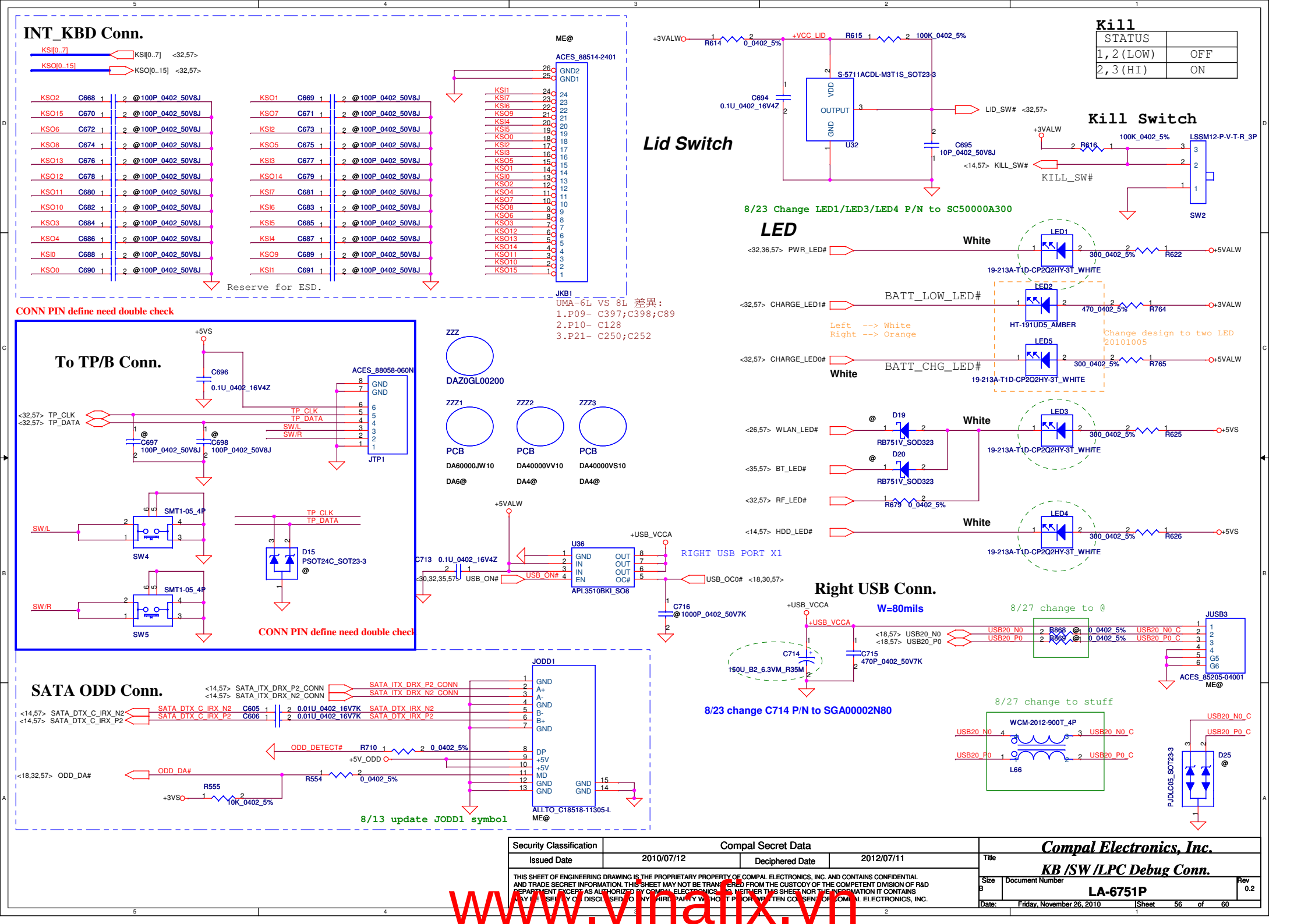

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

Title: KB /SW /LPC Debug Conn.

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INT_KBD Conn.

KSI[0..7] <32,56>
KSO[0..17] <32,56>

KSO2 C668 @100P_0402_50V8J
KSO15 C670 @100P_0402_50V8J
KSO6 C672 @100P_0402_50V8J
KSO8 C674 @100P_0402_50V8J
KSO13 C676 @100P_0402_50V8J
KSO12 C678 @100P_0402_50V8J
KSO11 C680 @100P_0402_50V8J
KSO10 C682 @100P_0402_50V8J
KSO3 C684 @100P_0402_50V8J
KSO4 C686 @100P_0402_50V8J
KSI0 C688 @100P_0402_50V8J
KSO0 C690 @100P_0402_50V8J

KSO16 C693 @100P_0402_50V8J
KSO17 C692 @100P_0402_50V8J
KSO1 C669 @100P_0402_50V8J
KSO7 C671 @100P_0402_50V8J
KSI2 C673 @100P_0402_50V8J
KSO5 C675 @100P_0402_50V8J
KSI3 C677 @100P_0402_50V8J
KSO14 C679 @100P_0402_50V8J
KSI7 C681 @100P_0402_50V8J
KSI6 C683 @100P_0402_50V8J
KSI5 C685 @100P_0402_50V8J
KSI4 C687 @100P_0402_50V8J
KSO9 C689 @100P_0402_50V8J
KSI1 C691 @100P_0402_50V8J

KSO16 <32>
KSO17 <32>

JKB1
KSI1 KSI7 KSI6 KSO9 KSI4 KSI5 KSO0 KSI2 KSI3 KSO5 KSO1 KSI0 KSO2 KSO4 KSO7 KSO8 KSO6 KSO3 KSO12 KSO13 KSO14 KSO11 KSO10 KSO15 KSO16 KSO17
GND GND
ACES_88514-3001
ME@

CONN PIN define need double check

Reserve for ESD.

ZZZ DAZ0GM00200
ZZZ1 PCB DA60000JY10 DA6@
ZZZ2 PCB DA40000VV10 DA4@
ZZZ3 PCB DA40000VS10 DA4@
ZZZ4 PCB DA40000VT10 DA4@
ZZZ5 PCB DA40000VU10 DA4@

UMA-6L VS 8L 差異:
1.P09- C397;C398;C89
2.P10- C128
3.P21- C250;C252

+5VALW
C713 0.1U_0402_16V4Z
<30,32,35,56> USB_ON#
USB_ON#
U36
GND IN IN EN OUT OUT OUT OC#
APL3510BKI_SO8
+USB_VCCA
USB_OC0# <18,30,56>
C716 @1000P_0402_50V7K
RIGHT USB PORT X1

To TP/B Conn.

+5VS
C696 0.1U_0402_16V4Z
<32,56> TP_CLK
<32,56> TP_DATA
C697 @ 100P_0402_50V8J
C698 @ 100P_0402_50V8J
JTP1
TP_CLK TP_DATA SW/L SW/R GND GND
ACES_88058-060N
ME@

SW/L
SW4 SMT1-05_4P
SW/R
SW5 SMT1-05_4P

TP_CLK
TP_DATA
D15 PSOT24C_SOT23-3 @

CONN PIN define need double check

Right USB Conn.

+USB_VCCA
W=80mils
8/27 change to @
C714 220U_6.3V_M
C715 470P_0402_50V7K
<18,56> USB20_N0
<18,56> USB20_P0
USB20_N0 R868 @ 0_0402_5% USB20_N0_C
USB20_P0 R869 @ 0_0402_5% USB20_P0_C
JUSB3
G5 G6
ACES_85205-04001
ME@

8/14 change to OSCAN 220U
(220uF_6.3V_4.2L_ESR17m)*1=(SF000002Y00)

8/27 change to stuff
WCM-2012-900T_4P
L66
PJDLC05_SOT23-3
D25 @

SATA ODD FFC Conn.

<14,56> SATA_ITX_DRX_P2_CONN
<14,56> SATA_ITX_DRX_N2_CONN
<14,56> SATA_DTX_C_IRX_N2
<14,56> SATA_DTX_C_IRX_P2
C605 0.01U_0402_16V7K
C606 0.01U_0402_16V7K
SATA_DTX_IRX_N2
SATA_DTX_IRX_P2
ODD_DETECT#
R710 0_0402_5%
+5V_ODD
<18,32,56> ODD_DA#
ODD_DA#
R554 0_0402_5%
R555 10K_0402_5%
+3VS
JP2
GND GND
ACES_87056-01001-001
ME@

<26,56> WLAN_LED#
<35,56> BT_LED#
<32,56> RF_LED#
D19 @ White
D20 @
RB751V_SOD323
RF_LED# R
R679 0_0402_5%

For 15" M/B to LED/B

KILL_SW# R884 @ 100K_0402_5%
11/16modify

+3VALW R615 100K_0402_5%
LID_SW#
7/22 modify

+5VALW
+3VALW
+5VS
<32,56> LID_SW#
<32,36,56> PWR_LED#
<32,56> CHARGE_LED1#
<32,56> CHARGE_LED0#
<14,56> HDD_LED#
<14,56> KILL_SW#
JP13
GND1 GND2
ACES_88514-01201-071
ME@

Security Classification	Compal Secret Data		
Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.
Title: KB /SW /LPC Debug Conn.
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PHASE	PAGE	Modification list	PURPOSE
0.2	P31	Change CRT Symbol	For CRT footprint issue
0.2	P31	Del C510	For Non-used part
0.2	P39	change C610 pin 1 net name	change C610 pin 1 net name to correct
0.2	P35	U25 change to U26	For co-lay 10/100 and GIGA
0.2	P40	Add R740, C93	For EC request
0.2	P18	Change R215 pin1 net name	Change R215 pin1 net name to correct
0.2	P16	Add R742, R743	For PCH power sequence
0.2	P38	Del U28, R542~R551 , J12	Del USB charger circuit
0.2	P40	Add EC pin 97,98,103	Add EC pin 97 for SYS_PWROK_EC , pin 98 for CE_EN , pin 103 for BATT_SEL_EC
0.2	P39	Change J10 footprint and Add J13	Change J10 footprint by DFx request and Add J13 by vendor suggestion
0.2	P39	Change PC_Beep circuit	Change PC_Beep circuit
0.2	P6	Add R161,	Follow ORB circuit
0.2	P58/59	Add R615 in 15" and 17" page	Pull high LID_SW# at M/B side
0.2	P31	Add Q83 pin 1 power net name +CMOS_PW	For power trace net
0.2	P56/57/58	Change JP21 to JKB1	Change connector to standard name
0.2	P56/57/58	Change JP4 to JTP1	Change connector to standard name
0.2	P43/60	Change JP6 to JPWRB1	Change connector to standard name
0.2	P34	Change JP1 to JWLN1	Change connector to standard name
0.2	P42	Change JP5 to JBT1	Change connector to standard name
0.2	P43/60	Change JP7 to JCR1	Change connector to standard name
0.2	P19	Add R542	For ESATA detect function
0.2	P42	Add R866, R886 , C735	For ESATA detect function
0.2	P31	Add R543	For reserve EC control directly
0.2	P39	Change J10 footprint, Del C635, C636	Change J10 for DFx and Del component for layout
0.2	P42	Add R877	For reserve EC control directly
0.2	P42	SW3 BOM structure change to @	For ME ASSY concern
0.2	P42	Change ESATA from port 5 to port 4	For intel risk
0.2	P15	Add R544,R545	For Pull high SMBus
0.2	P12/13	Del R74~R80,R82 R88~R94,R96	For DDR3 DM Bus to GND
0.2	P16	Add R182,R546	Add 186 for reserve sequence, Add R546 for follow CRB & ORB
0.2	P20	Del Add J12, R257 change to @	For voltage drop
0.2	P6	R161 change to 100K	Follow CRB
0.2	P19	Add R547 , R250 change to @	Follow Module and CRB
0.2	P18	WLAN USB port for port8 to port9	For debug port
0.2	P39	Del J13	For layout space
0.2	P20,39,42	Add C395 , R581 , R583 , R584 , R586 , R587	For customer request reserved
0.2	P20	Add C129, C396 , Del R264	For reserved
0.2	P40	Add PIN 66 , R740,C93 change to @	Add IMVP_IMON
0.2	P9	Add R74	For VCCIO_SENSE / VSSIO_SENSE differential routing
0.2	P30	Del R419~425, R427~R429	Del 0 ohm for UMA only
0.2	P31	Del R439 , R440, R441	Del 0 ohm for UMA only
0.2	P32	Del RQ51 ~ Q54 Add Q95	For DIS HDMI
0.2	P38	Del J10, C637,C640,R576,R577,R579 change to @ , L40~L43 change to R720~R723	For Vendor suggestion and EMI
		Del C643, R578 , MIC_INR connect MIC_INL , Add R578	Del C653, R578 connect MIC_INR/L for vendor suggestion , Add R578 for EMI
0.2	P20	Add L75 , R264 , C917, R259 C226 change to @	For intel PDDG update
0.2	P43	C714 change to OSCON CAP	C714 change to OSCON CAP
0.2	P9	Add C394, C397 ,C398 , C399 ,Add R75	For CPU_CORE power reserved at Bottom side, Add R75 for reserved at cpu side and pwr side
0.2	P42	Change C706 P/N to SF000001500	Change to H=6 OSCAN
0.2	P10	Change C128 to @	For Reserved
0.2	P56	Update JODD1 symbol	For ME update drawing

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PHASE	PAGE	Modification list	PURPOSE
0.2	P16	D29 change to @	For AC detect issue
0.2	P24	R548,R549 change to DIS@	For AC detect issue
0.2	P10	C128 change to stuff	For test on DVT
0.2	P44	Del Q118, R657	For not need
0.2		Change R513, R516 ,R667 P/N and from 0805 to 0603	For common part
0.2		Change C633, C634 , C642	For common part
0.2		Change D3, D29 P/N and symbol	For common part
0.2		Change U3,U11,U13,U14,U38,U39 P/N and symbol	For common part
0.2		Change U3,U11,U13,U14,U38,U39 P/N and symbol	For common part
0.2		Change Q8,Q65,Q80,Q83,Q99,Q104 P/N and symbol	For common part
0.2		Change Q1,Q37,Q93 P/N and symbol	For common part
0.2		Change Q94, Q95 P/N and symbol	For common part
0.2		Change Q3,Q4,Q7,Q9,Q66,Q67,Q68,Q73,Q74,Q75,Q76,Q77,Q78, Q79,Q82,Q85,Q86,Q87,Q102,Q106,Q107,Q108,Q109,Q110,Q111,Q112,Q113,Q114,Q115,Q116 P/N and symbol	For common part
0.2		Change C635 part and change to @	For EMI
0.2	P18	Reserved R297	Reserved
0.2	P9	Change C53,C85,C86,C87 ,C397,C398,C399 to stuff and change ,C48,C80,C81,C82, C90,C91 to @ Del C89	For CPU_CORE
0.2	P10	Change C110,C111,C112,C113 to stuff	For VGFX_CORE
0.2	P56	Change LED1/LED3/LED4 P/N to SC50000A300	Change P/N
0.2	P36	Change T1,T2 P/N to SP050003N00	For test pass part
0.2	P40	Change R611,R740,C93 to stuff and change Y5,C347,C367 to @ Change R695 to 18K, Q37 change to @, R747 change to stuff,	For SUS_CLK R695 for Board ID, Q37, R747 for VR_HOT
0.2	P40	Change U33 P/N to SA00003FL10	For BIOS ROM
0.2		Change C509,C511,C635 to stuff	For EMI
0.2	P56	Change 14" C714 P/N to SGA00002N80	For Sourcer request
0.2	P39	Change R720,R721,R722,R723 P/N to SM01000BZ00(Bead), and Change C647,C649,C650,C651 to Stuff	For EMI request
0.2	P19	Change R303 to Stuff, and change R542 to @	For BIOS ESATA detect function
0.2	P56	Change U32 P/N to SA000031C00	For common part
0.2	P36	Change T1,T2 P/N to SP050006E00	For correct part
0.2	P10	R688 change to stuff , R687 ,Q7 change to @	For S3 power reduction
0.2		Change R660,R661,R862,R863,R864,R865,R868,R869 to @ , change L63,L64,L65,L66 to stuff , change R619 to Bead (SM01000DI00)	For EMI
0.2	P20	Change L75 symbol	For common part
0.2	P30	Change R402 to @	For DPST
0.3	P10	Update Q5 symbol	For update symbol
0.3	P33	Add F2	For safty request
0.3	P39	Update U30 P/N to SA00003K410 and Add R879	For Audio update to 21Z
0.3	P10	Change C128 to D2 size and @	Change size for M/E issue
0.3	P14	Add reserve R878	For Intel DG 1.5
0.3	P37	C592 change P/N to SF000001500 (H=6)	For ME Z high ok
0.3	P29	R369 P/N change to SD034100A80	For GP part
0.3	P6	Reserved R880 to SYS_PWROK	Follow ORB
0.3	P10	R62,R63 change to 1K	Follow CRB
0.3	P33	R483,R484 change connect to +5V_HDMI_F	For Add F2
0.3	P37	Change U27 P/N to SA000046C00	For Fintek
0.3	P40	Change R594 pull high to +5VALW	For leakage issue

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Issued Date	2010/07/12	Deciphered Date	2012/07/11

Compal Electronics, Inc.

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PHASE	PAGE	Modification list	PURPOSE
0.3	P19	R881 change to Dtuff, R244 change to @	For intel MRC Rev0.9
0.3	P14	R878 change to stuff	For intel DG 1.5
0.3	P31	Del R432	For non-used part
0.3	P36	Reserved D31 , C643 , C644	For reserved EMI parts
0.3	P37	Del R581	For non-used part
0.3	P38	Del R550	For non-used part
0.3	P38	Change C592 P/N to SF000002Y00	For M/E Z high limlt
0.3	P39	Del R584, R586 , R587	For non-used part
0.3	P40	Change R600, R604 to 2.2K Change R695 to 8.2k	Change R600, R604 for Battery SMBus, R695 for Board ID
0.3	P42	Del R583	For non-used part
0.3	P31	Del R449, R452, R458, R460 (UMA change only)	For non-used part
0.3	P32	Del R478, R480, R486 (UMA change only)	For non-used part
0.3	P6	Reserved R882 connect to PCH_PWROK	Reserved for intel
0.3	P56	R765 change to 300 ohm	For LED

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Issued Date	2010/07/12	Deciphered Date	2012/07/11

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Title: PIR		
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