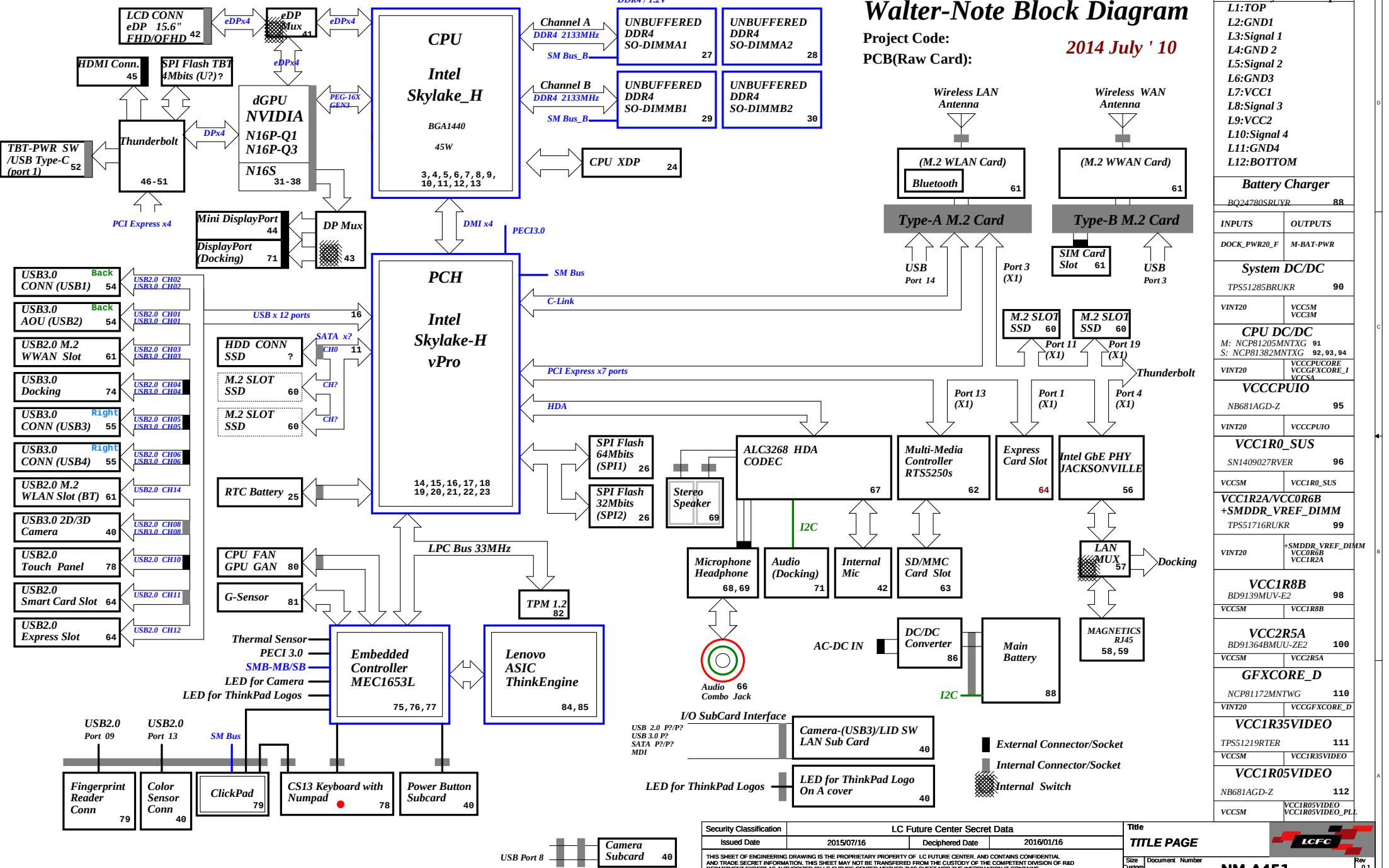


Walter-Note Block Diagram

Project Code:

2014 July '10

PCB(Raw Card):



vinafix

TABLE: SYSTEM POWER STATE

Gx State (System State)	Sx State (System State)	Mx State (System State)	SW Power	M Power	SUS Power	AMT Power	A Power	B Power	User Observation	Chipset
G0	S0	M0	ON	ON	ON	ON	ON	ON	System Operating	Full On
	S3	M3	ON	ON	ON	ON	ON	OFF	Standby	
		M-OFF	ON	ON	ON	OFF	ON	OFF	Standby with USB wake enabled	Suspend-to-RAM (STR)
G1	Deep S3	M-OFF	ON	ON	OFF	OFF	ON	OFF	Standby	
	S4	M3	ON	ON	ON	ON	OFF	OFF	Hibernation with RTC wakeup	Suspend-to-Disk (STD)
	Deep S4	M-OFF	ON	ON	OFF	OFF	ON	OFF	Hibernation or Shutdown	
G2	S5	M3	ON	ON	ON	ON	OFF	OFF	Hibernation or Shutdown	
	Deep S5	M-OFF	ON	ON	OFF	OFF	ON	OFF		Soft Off
	S5 EC OFF	M-OFF	OFF	OFF	OFF	OFF	OFF	OFF		
G3	---	---	OFF	OFF	OFF	OFF	OFF	OFF	No Power	Mechanical off

Schematics Mark Definition

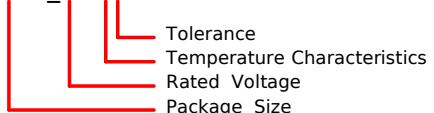
BOM Structure	BTO Item
@	Not assembled.
EMC@	Assembled. EMC related parts.
RF@	Assembled. RF related parts.
ME@	Assembled. ME related parts.
PRxxx, PCxxx, PLxxx	PWR related parts. If @, not assembled.
N16P@	Assembled. for N16P GPU SKU
N16S@	Assembled. for N16S GPU SKU
VP@	Assembled. for support vPro
NVP@	Assembled. Not support vPro

Any other mark like below is prohibited on Payton/Walter.
 ESD@,EMI@,EMC_NS@,EMC_PX@,EMC_OPT@,CONN@,
 CONN_NS@... RH,CH,LH(PCH related RLC)..

Capacitor Naming Note

Ceramic Capacitors:

0.1U_0402_6.3VXX



Temperature Characteristics:

Symbol	0	1	2	3	4	5	6	7	8	9	A
Code	Z5U	Z5V	Z5P	Y5U	Y5V	Y5P	X5R	X7R	NPO	COG	X6S

B	C	D	E	F	G	H	I	J	K	L
BJ	CH	CJ	CK	SH	SJ	UJ	UK	SL	X5S	NOJ

Tolerance:

Symbol	A	B	C	D	F	G	H	J	K	M	N
Tolerance	+0.05PF	+0.1PF	+0.25PF	+0.5PF	+1%	+2%	+3%	+5%	+10%	+20%	+30%

Symbol	P	Q	V	X	Z	S	Y
Tolerance	+100,-0%	+30,-10%	+20,-10%	+40,-20%	+80,-20%	+50,-20%	-30% ~ 10%

EC SMBus0 address

Device	Address
Smart Battery	0001 011X b
G-Senor (LIS3DH)	0011 000Xb

EC SMBus1 address

Device	Address
G-Senor (KX023)	0011 110Xb
Master VGA	0x9E

EC SMBus2 address

Device	Address
Charge Controller	0001 0010

EC SMBus10 address

Device	Address
Master VGA	0x9E

PCH SM Bus address

Device	Address
CH-A P DDR DIMM0	1001 0000b
CH-A S DDR DIMM1	1001 0001b
CH-B P DDR DIMM2	1001 0010b
CH-B S DDR DIMM3	1001 0011b

PCH SM Bus0 address

Device	Address
Intel Lan_I219	0XC8

CPU		PCB	
U1	U1	U1	U1
i5 45W (vPro) SA00007HA10 i5@	i7 45W Non-vPro SA00007HB10 i7NV@	i7 45W vPro SA00007HC10 i7VP@	Z1 45W vPro SA00007HD10 Z1@
Z2 45W vPro SA00007HF10 Z2@	Z2 45W vPro SA00007HF10 Z2@	PCB NNM-A451 DAZ0Z600100	PCB NNM-A451 DAZ0Z600100

Security Classification: **Blank**

LC Future Center Secret Data:

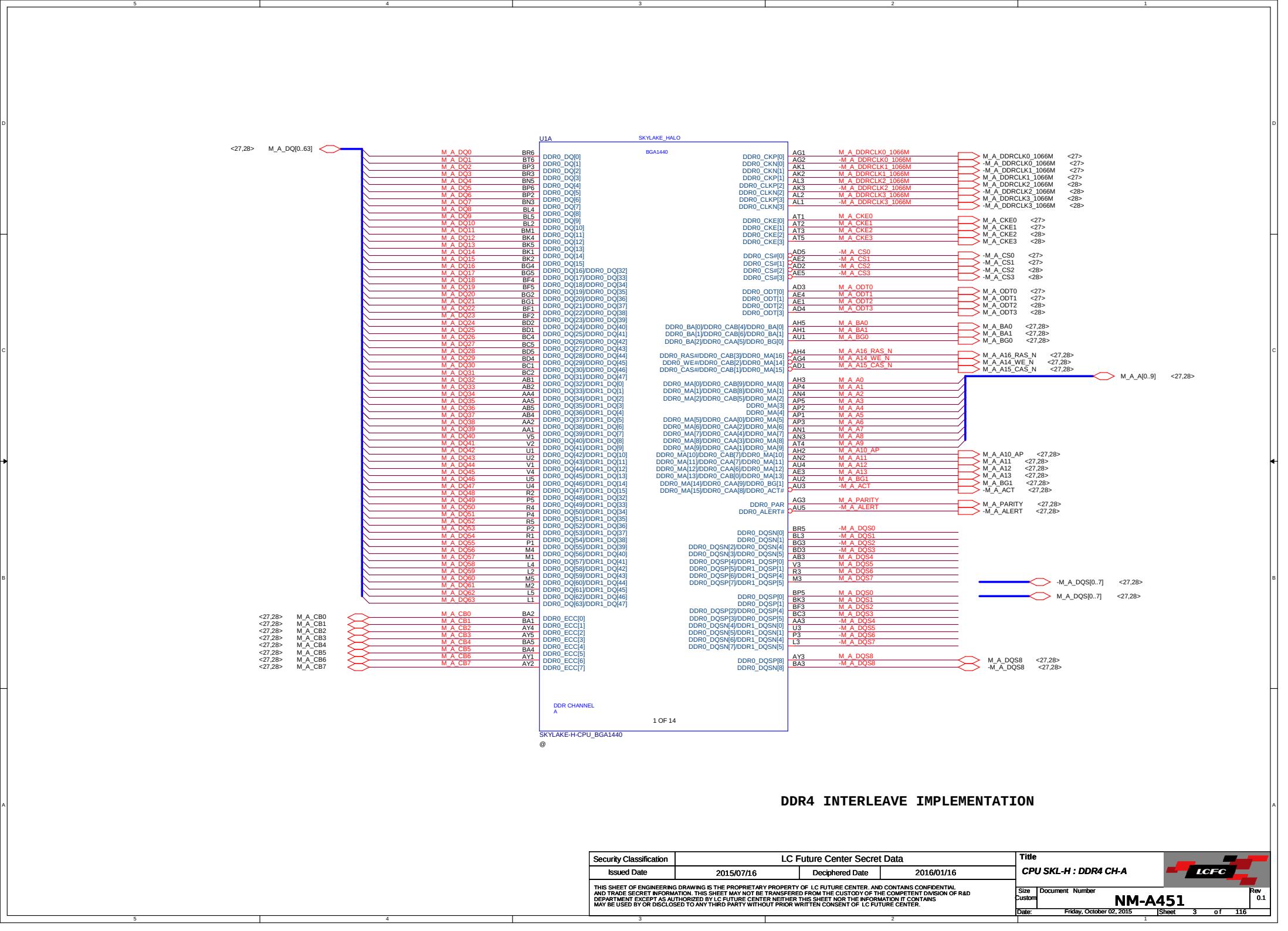
Issued Date: 2015/07/16	Deciphered Date: 2016/01/16
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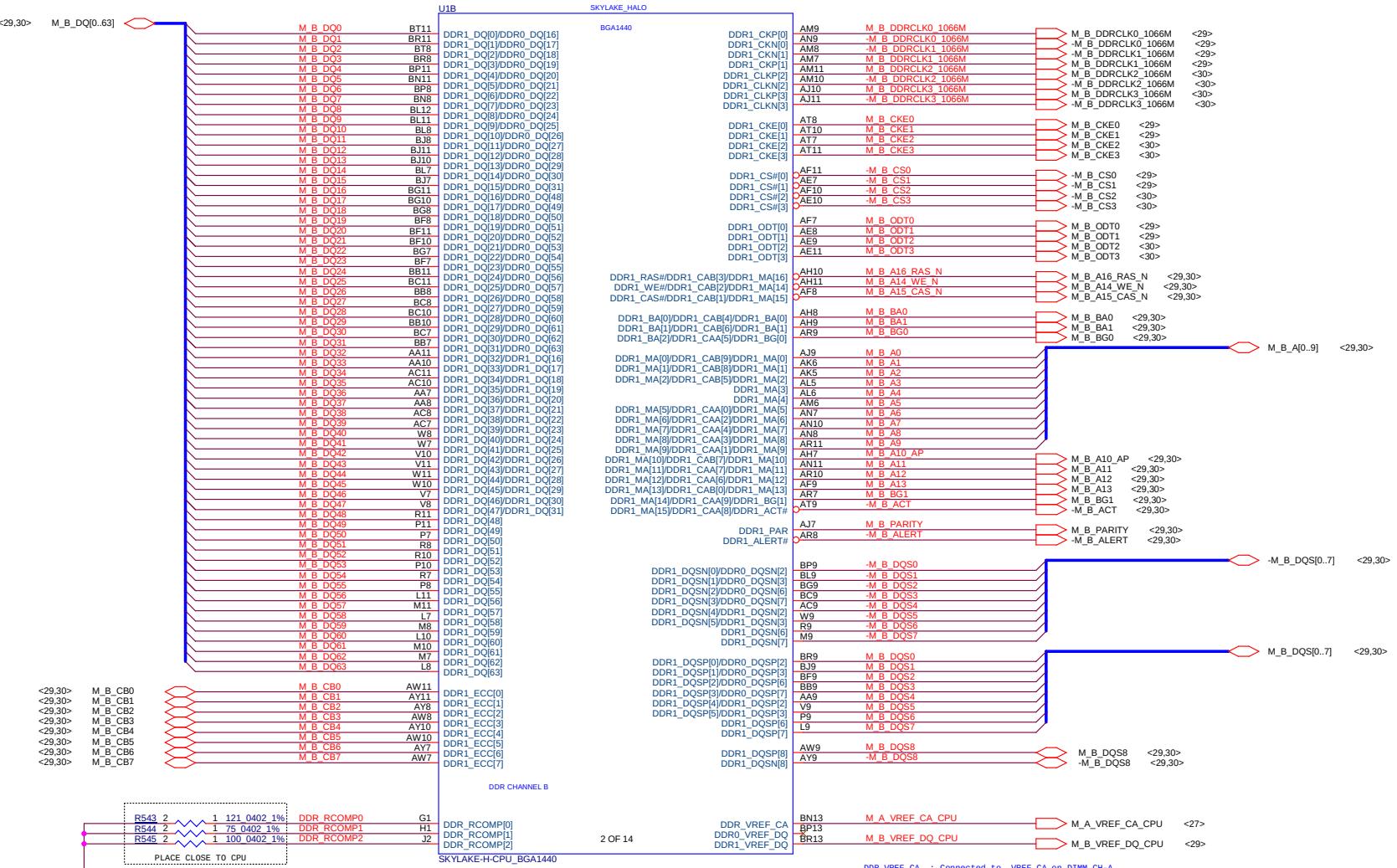
Date: Friday, October 02, 2015

Sheet 2 of 116

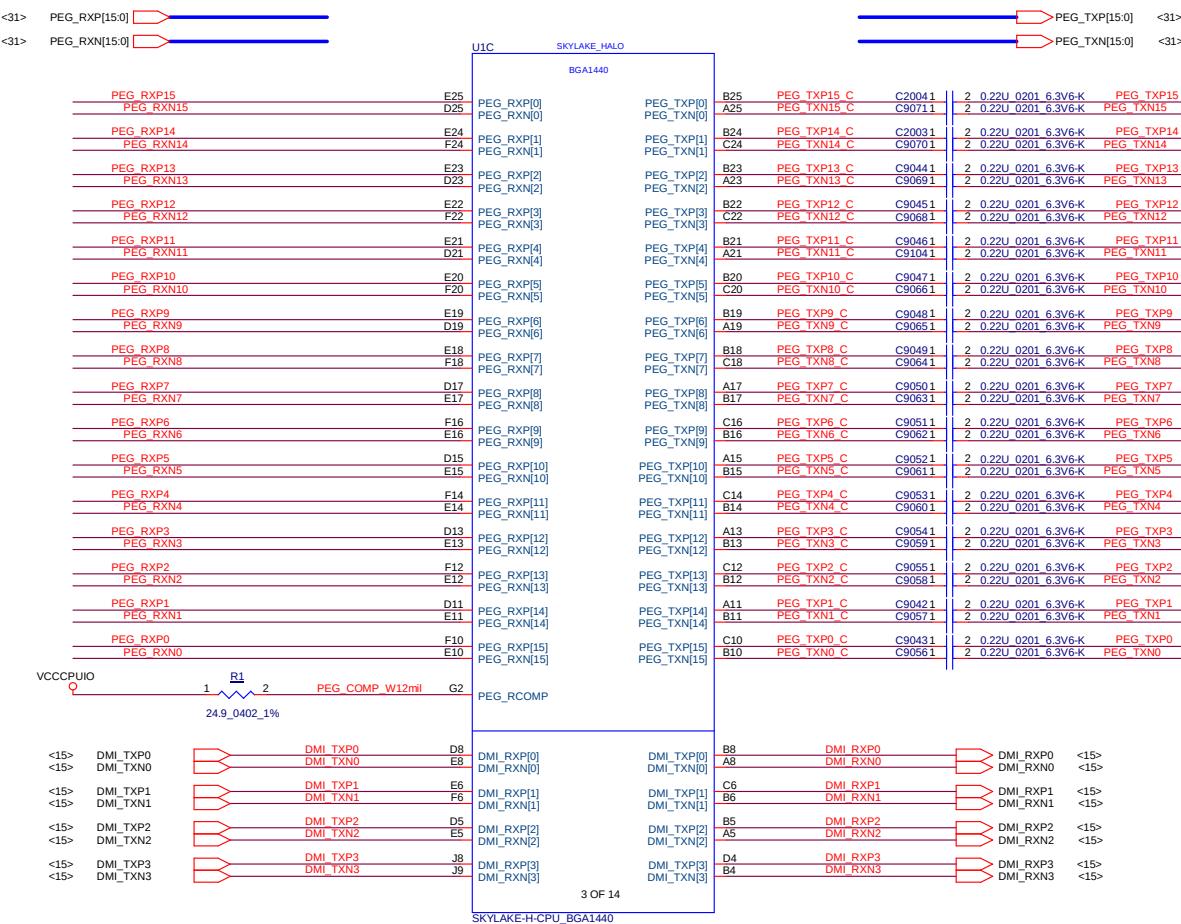


DDR4 INTERLEAVE IMPLEMENTATION

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Date: Friday, October 02, 2015	Sheet	3	of	116



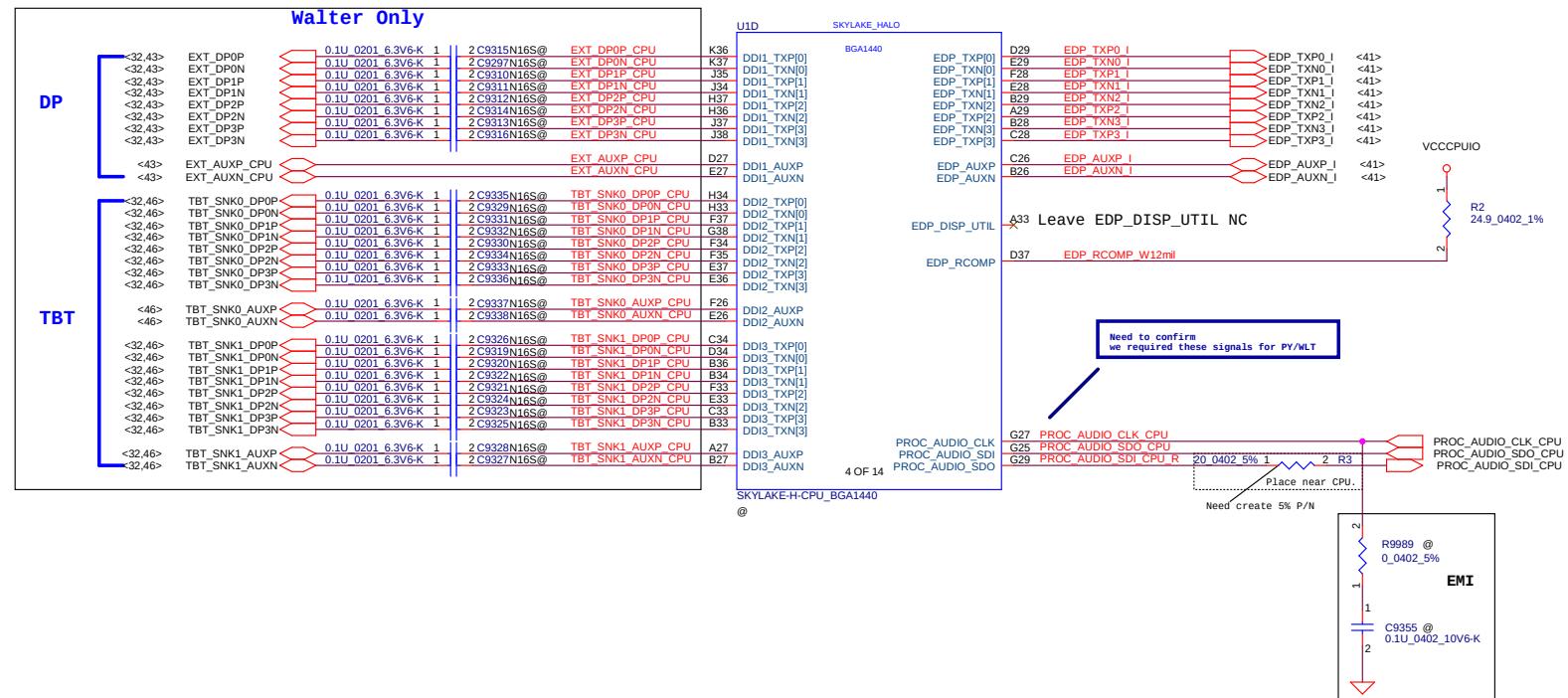
Security Classification	LC Future Center Secret Data			Title	LCFC	
Issued Date	2015/07/16	Deciphered Date	2016/01/16	CPU SKL-H : DDR4 CH-B		
Size	Document	Number				Rev
Custom		NM-A451				0.1
Date:	Friday, October 02, 2015		Sheet	4	of	116

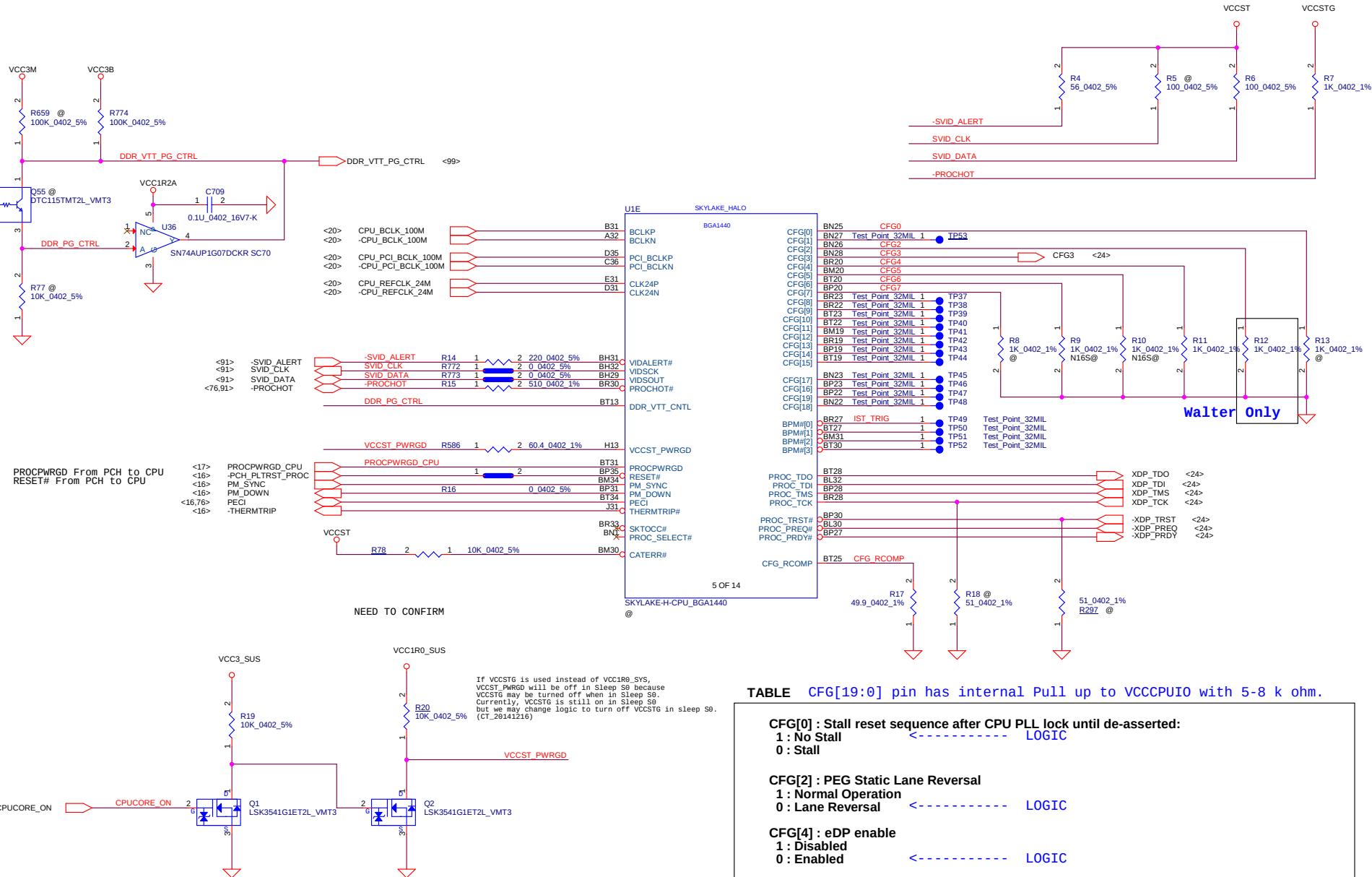


Security Classification	LC Future Center Secret Data		
Issued Date	2015/07/16	Deciphered Date	2016/01/16

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Title				
CPU SKL-H : PEG/DMI				
Size Custom	Document Number	NM-A451		Rev 0.1
Date Friday, October 02, 2015		1Sheet	5	of 116





VCCST_PWRGD requirements (546884_SKL_H_PDG_Rev0_71)

- Indication that the VCCST/VDDQ power supplies are stable and within specification. (Table 41-1)
- VCCST_PWRGD must go low during Sx pwr states, regardless of the voltage level of VCCST. (Figure 41-1 Note 1)
- VCCST_PWRGD should be equal or earlier than PCH_PWROK. (Table 41-5, TCPU16. See also 543016_SKL_PDG_UY_1_0)
- VCCST_PWRGD is typically made from ALL_SYS_PWRGD (CPUCORE_ON/VR_ON for CPU DCDC), not PCH_PWROK (CPUCORE_PWRGD). (Figure 41-1)

TABLE CFG[19:0] pin has internal Pull up to VCCCPUIO with 5-8 k ohm.

CFG[0] : Stall reset sequence after CPU PLL lock until de-asserted:
1 : No Stall 0 : Stall

CFG[2] : PEG Static Lane Reversal
1 : Normal Operation 0 : Lane Reversal

CFG[4] : eDP enable
1 : Disabled 0 : Enabled

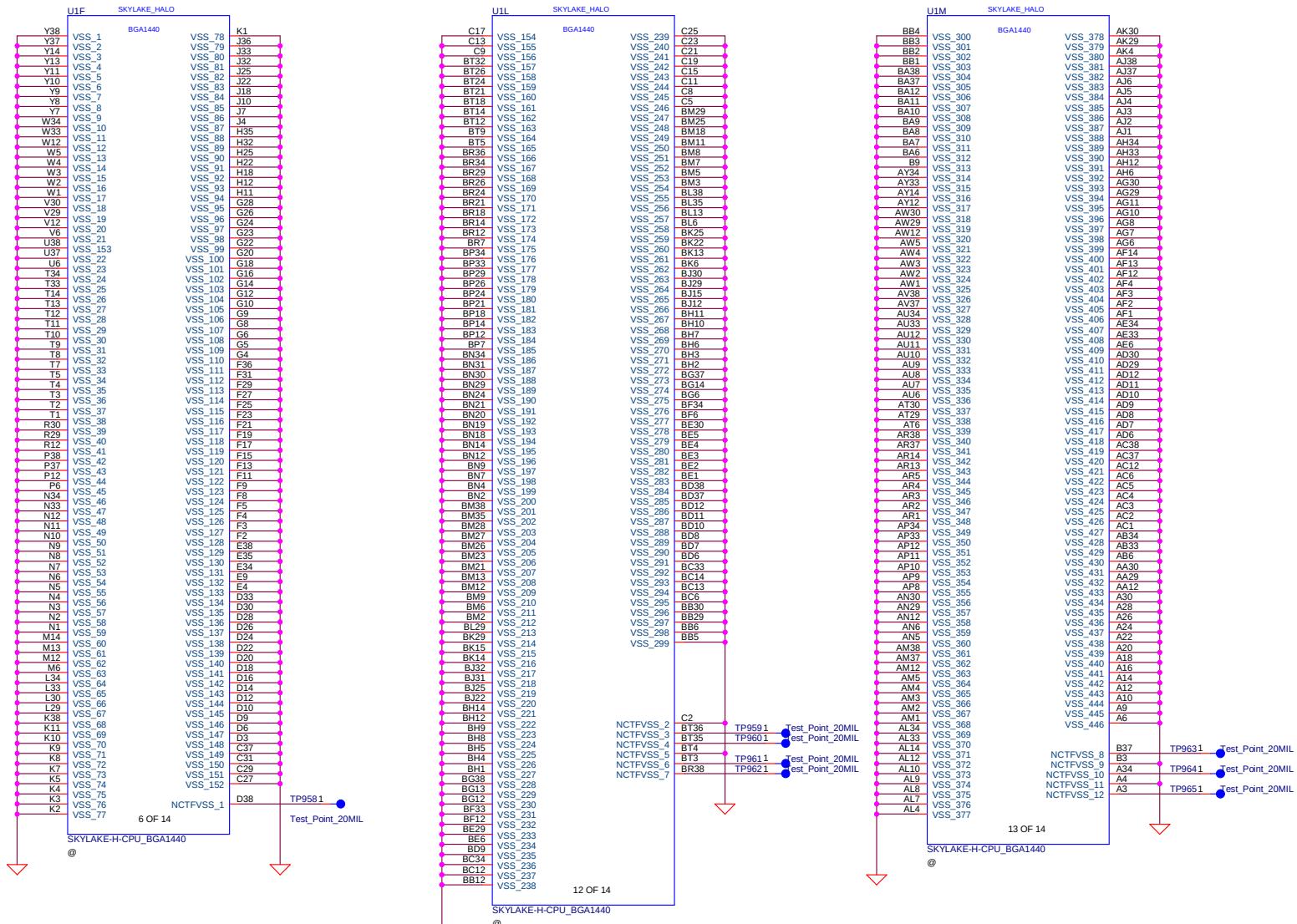
CFG[6:5] : PEG Bifurcation, bus#:dev#:func#=0:1:0
11 : 1x16

CFG[7] : PEG Training
1 : PEG Train immediately following RESET# deassertion 0 : PEG Wait for BIOS for training

CFG[19:8] : Reserved

For x16 Reversal Lanes - CFG[6/5/2] setting is 110
For x4 Reversal Lanes - CFG[6/5/2] setting is 000

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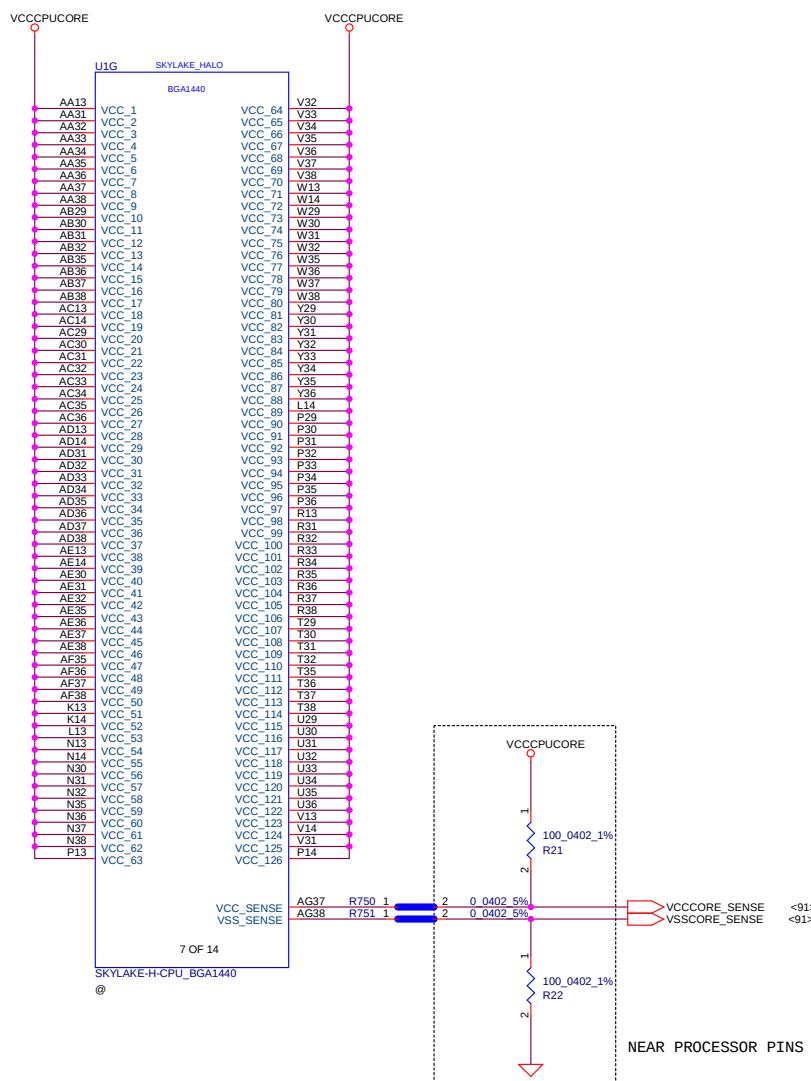


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	2015/07/16		

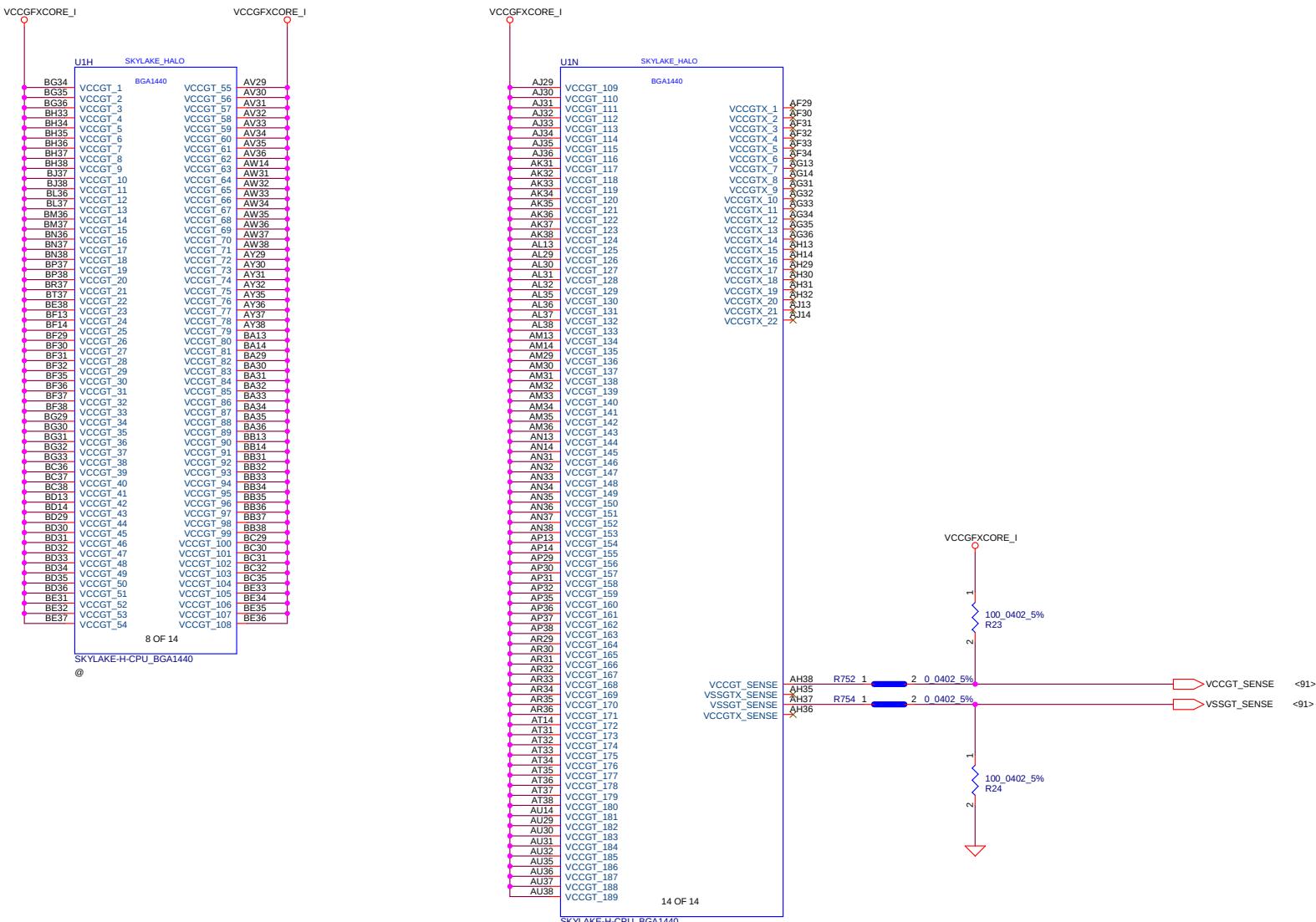
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Title
CPU SKL-H : GND

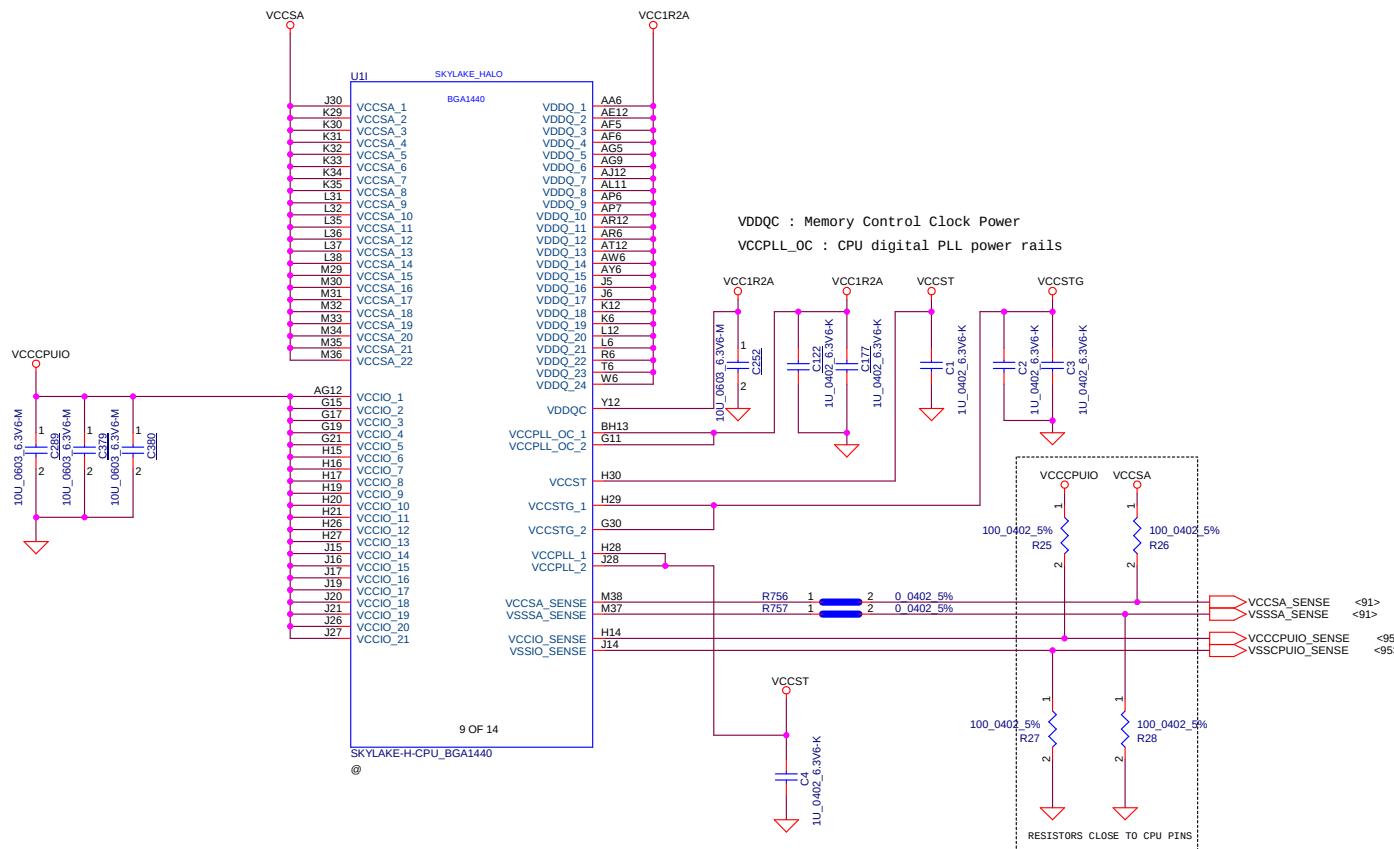
Size Document Number Rev
Custom NM-A451 0.1



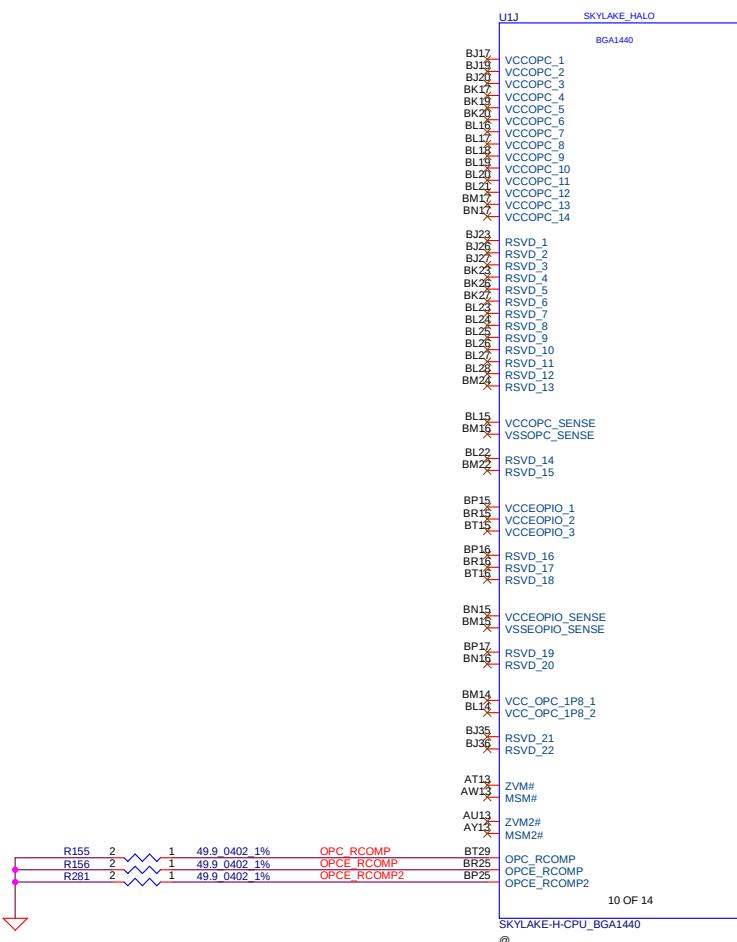
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Issued Date	2015/07/16		Deciphered Date	2016/01/16	CPU SKL-H : VCC
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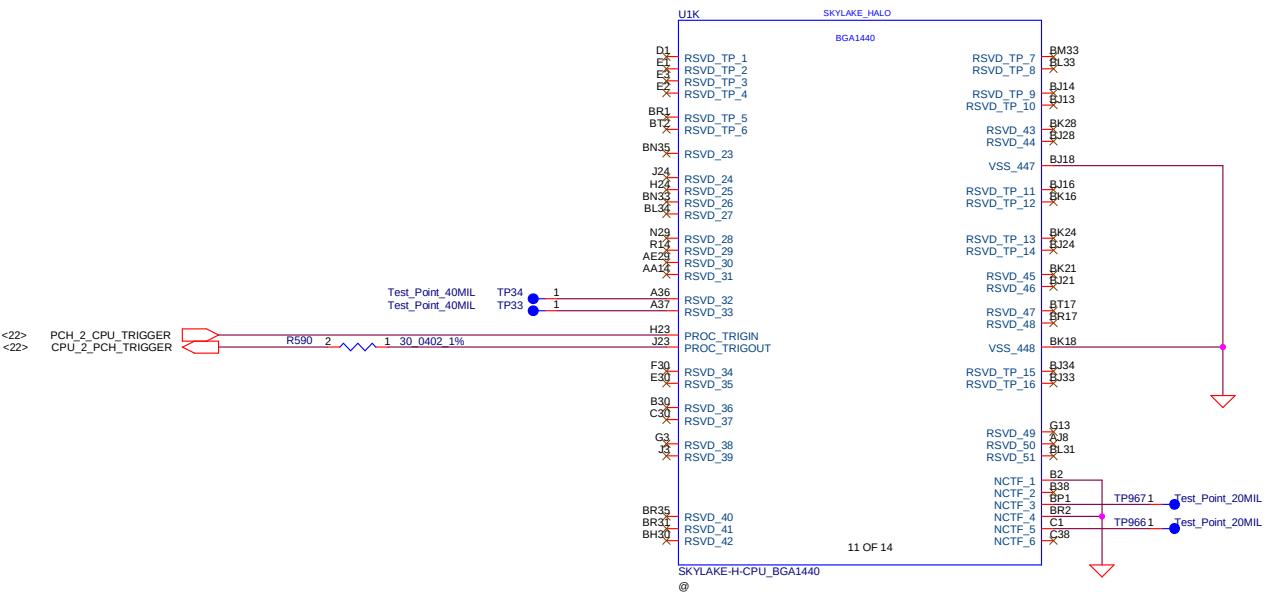


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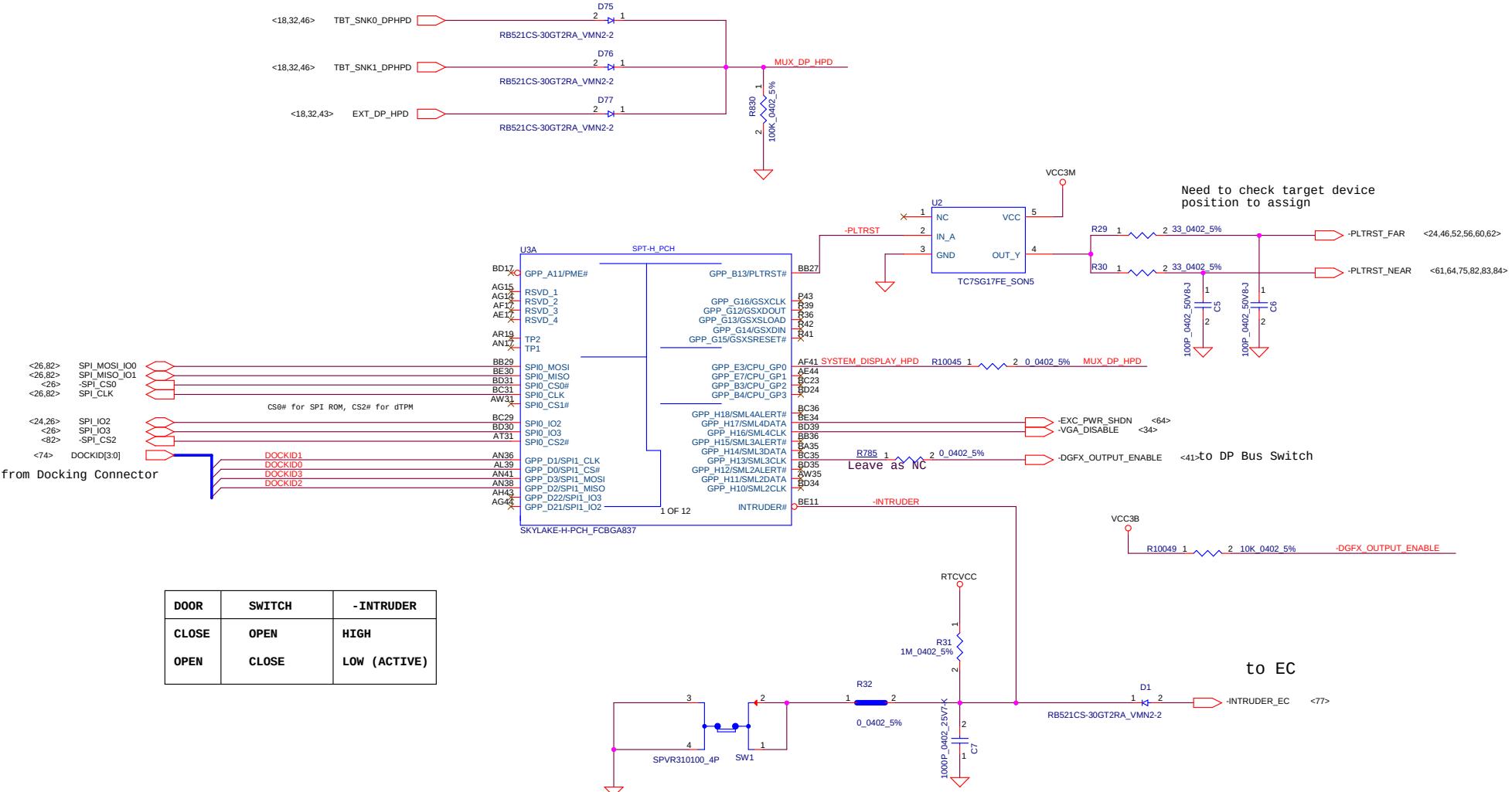


R155 2 2 1 49.9 0402 1% OPC_RCOMP
R156 2 2 1 49.9 0402 1% OPC_E_RCOMP
R281 2 2 1 49.9 0402 1% OPC_E_RCOMP2

Security Classification		LC Future Center Secret Data				Title
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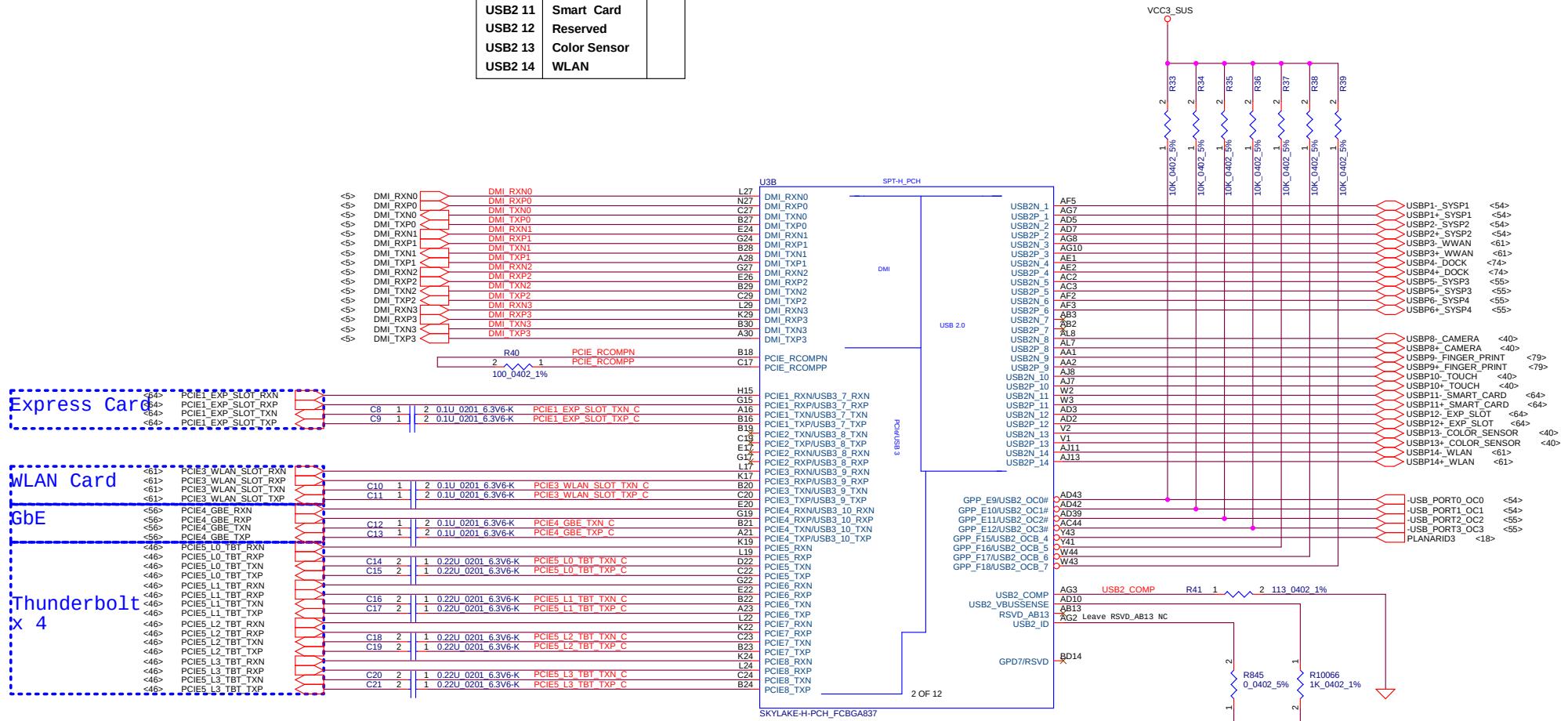
DOOR	SWITCH	-INTRUDER
CLOSE	OPEN	HIGH
OPEN	CLOSE	LOW (ACTIVE)

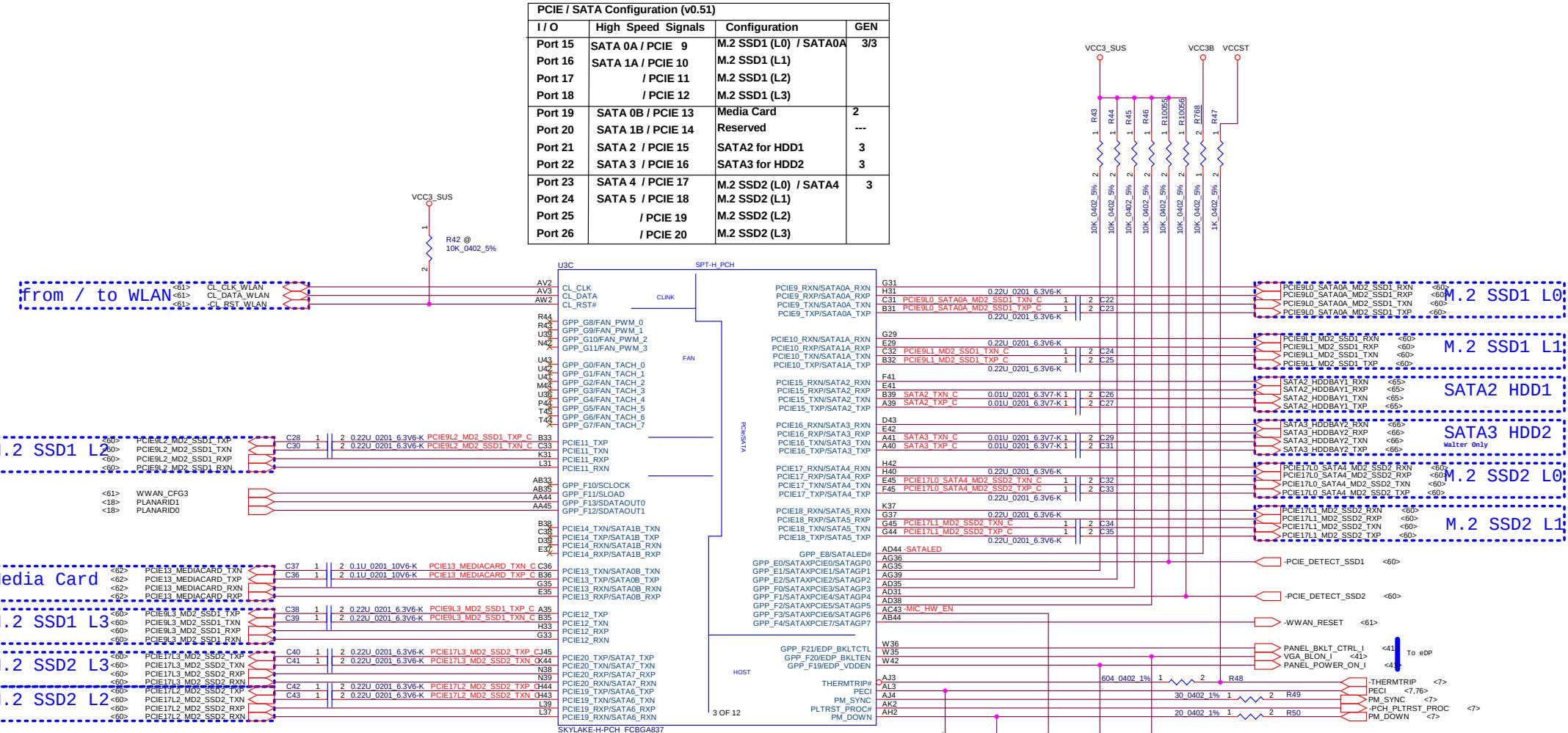
Flexible I/O Configuration (v0.51)			
I/O	High Speed Signals	Configuration	Net Name
Port 1 - 6			Please see Page 19
Port 7	USB3 7 / PCIE 1	USB3 7 or PCIE 1	PCIE1_EXP_SLOT
Port 8	USB3 8 / PCIE 2	USB3 8	
Port 9	USB3 9 / PCIE 3	PCIE 3	PCIE3_WLAN_SLOT
Port 10	USB3 10 / PCIE 4 (GBE)	GBE	PCIE4_GBE
Port 11	PCIE 5 (GBE)	PCIE 5	PCIE5_L0_TBT
Port 12	PCIE 6	PCIE 6	PCIES_L1_TBT
Port 13	PCIE 7	PCIE 7	PCIES_L2_TBT
Port 14	PCIE 8	PCIE 8	PCIE5_L3_TBT

USB2.0 Configuration (v0.51)		
USB2 #	Assignment	OCx #
USB2 1	System Port 1	0
USB2 2	System Port 2	1
USB2 3	WWAN	
USB2 4	DOCK	
USB2 5	System Port 3	2
USB2 6	System Port 4	3
USB2 7	Reserved	
USB2 8	Camera	
USB2 9	Finger print	
USB2 10	Touch panel	
USB2 11	Smart Card	
USB2 12	Reserved	
USB2 13	Color Sensor	
USB2 14	WLAN	

PCIE Configuration (v0.51)		
PCIE #	High Speed Signals	GEN
PCIE 1		
PCIE 2		
PCIE 3	WLAN Card	2
PCIE 4	GBE	
PCIE 5	Thunderbolt 1	3
PCIE 6	Thunderbolt 2	
PCIE 7	Thunderbolt 3	
PCIE 8	Thunderbolt 4	
PCIE 9 - 20	Please see Page 16	

USB 3#	High Speed Signals
USB3 1 - 6	Please see Page 19
USB3 7	
USB3 8	
USB3 9	
USB3 10	





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TABLE : Functional Strap

HDA_SDO	
Flash Descriptor Security Override	
HIGH	Disable Flash Descriptor Security (Override)
LOW	Enable Flash Descriptor Security (Default)

HDA_SDO is used to update the Descriptor and/or the ME regions of the SPI after MFG Done bit is set.

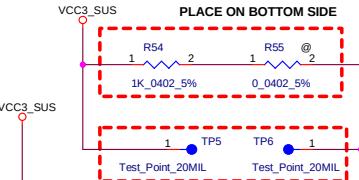


TABLE : Functional Strap

GPP_C5/SML0ALERT#(LPC or SPI)	
HIGH	eSPI is selected
LOW	LPC is selected(Default)

TABLE : Functional Strap

GPP_C5/SML0ALERT#(TLS Confidentiality)	
HIGH	Enable ME Crypto TLS with Confidentiality
LOW	Disable ME Crypto TLS(Default)

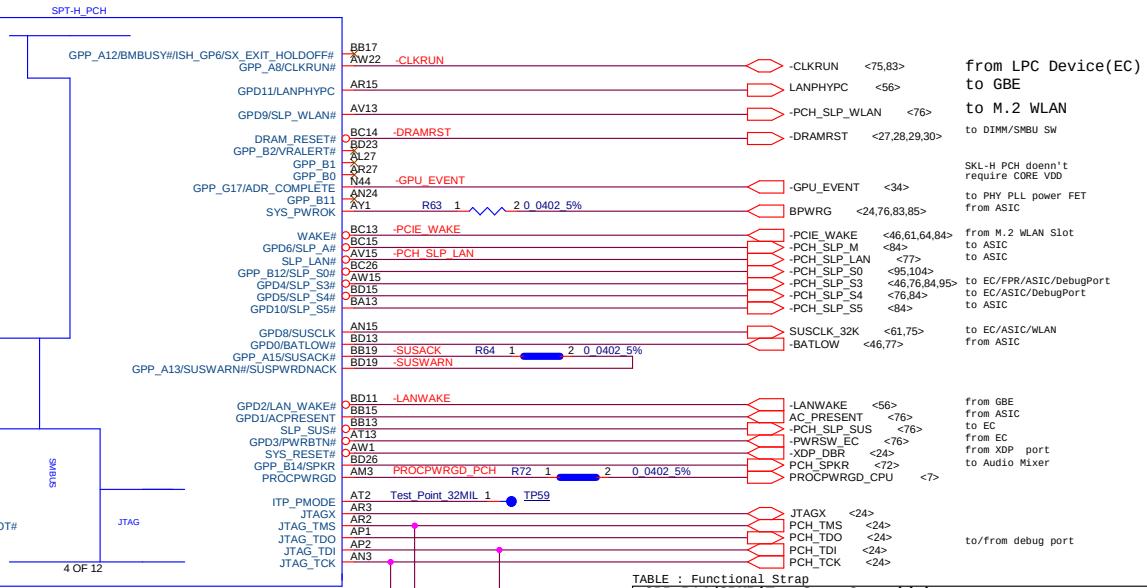
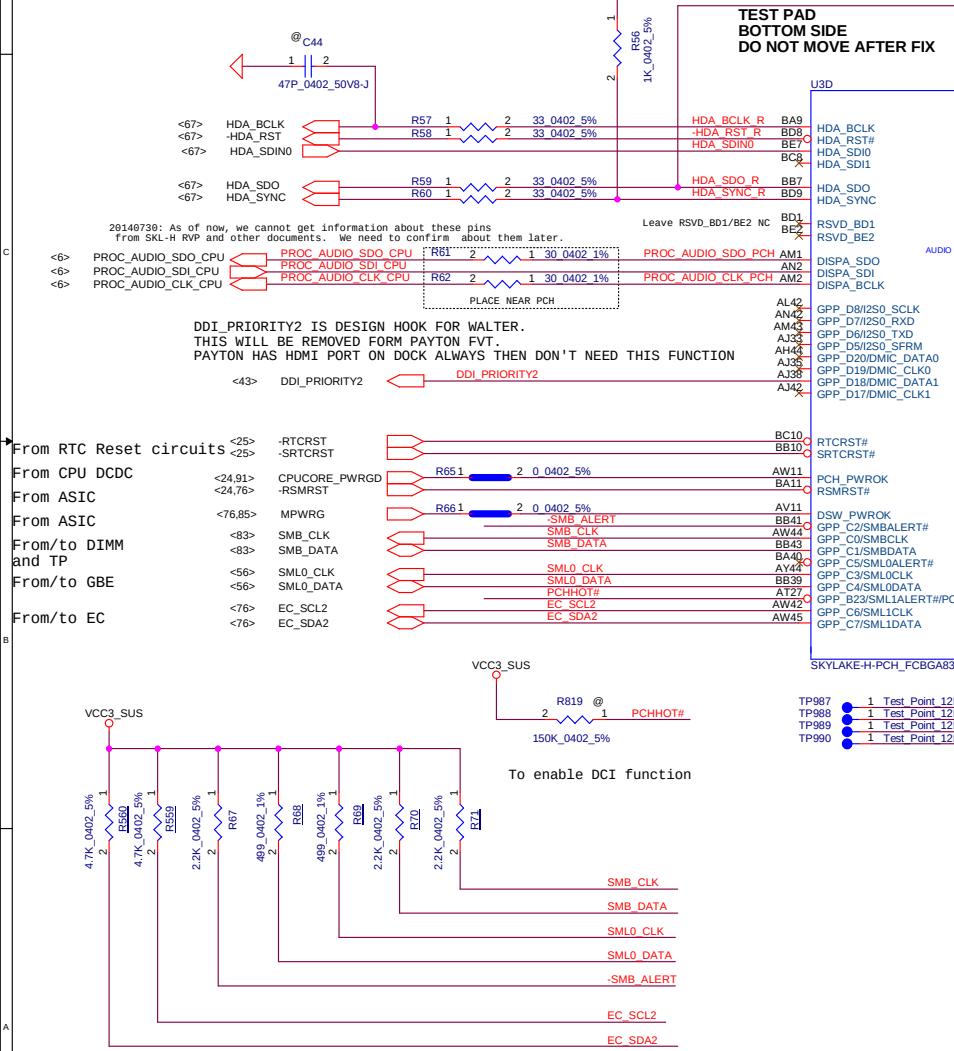
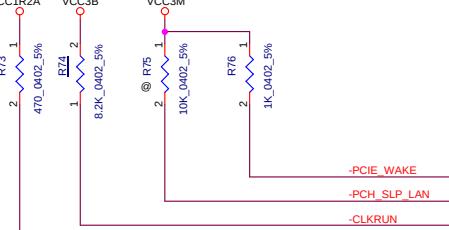
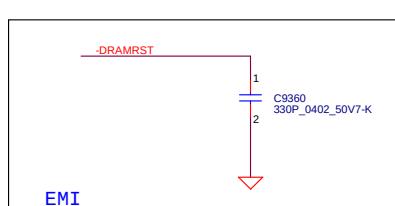


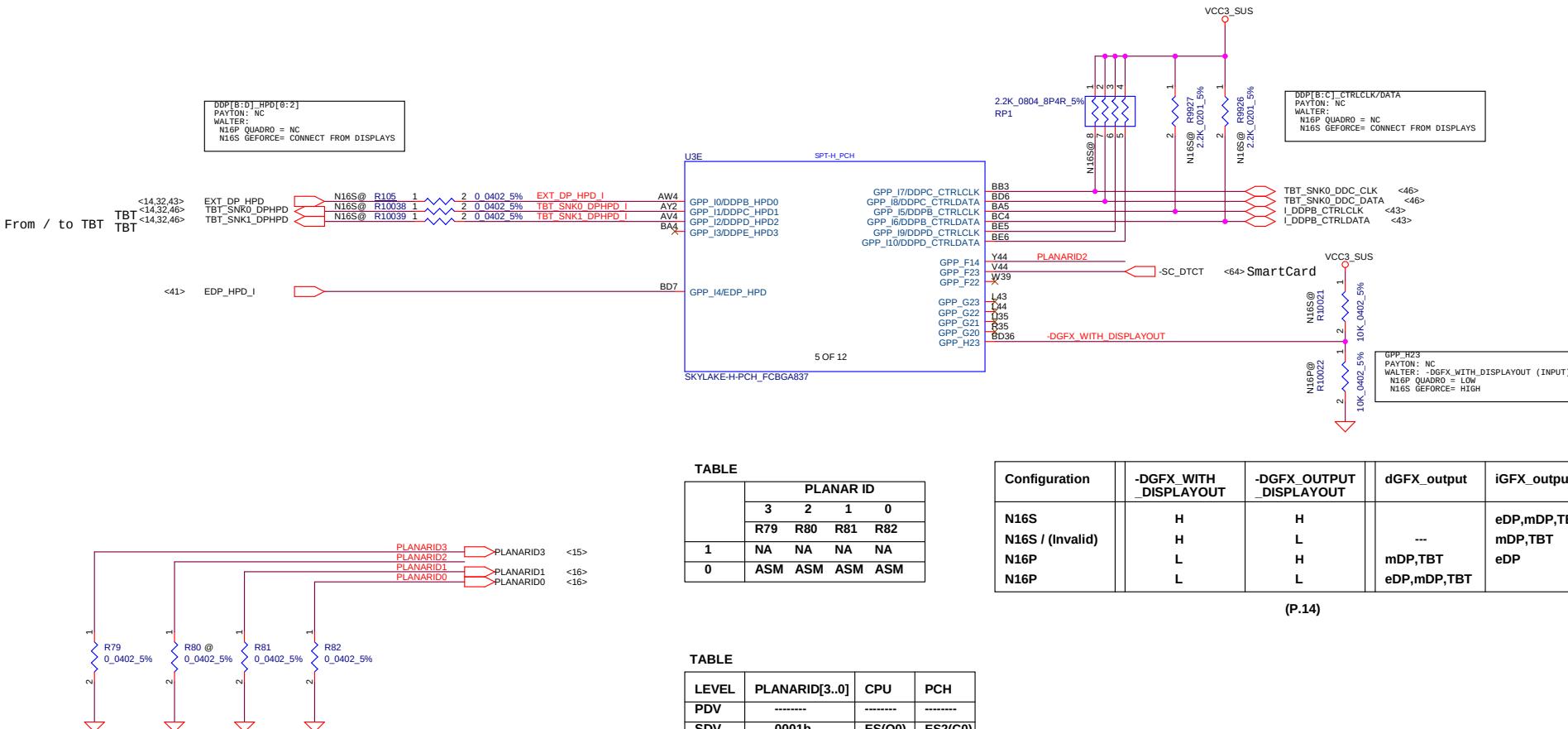
TABLE : Functional Strap

HIGH	Enable "TOP Swap" Mode
LOW	Disable "TOP Swap" Mode (Default by Internal PD)

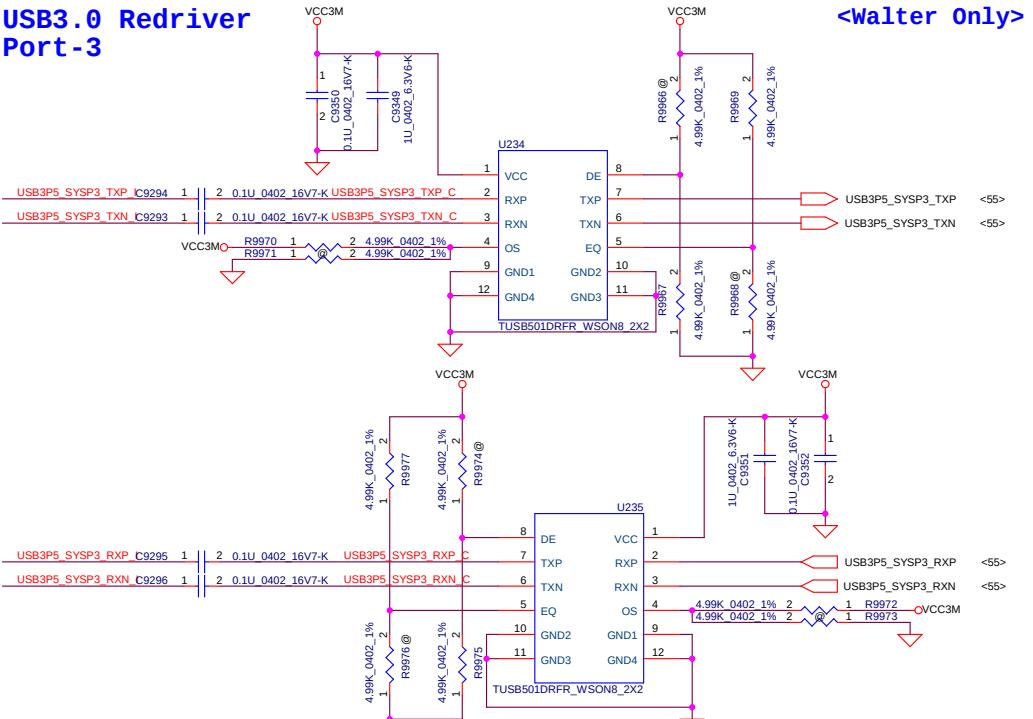
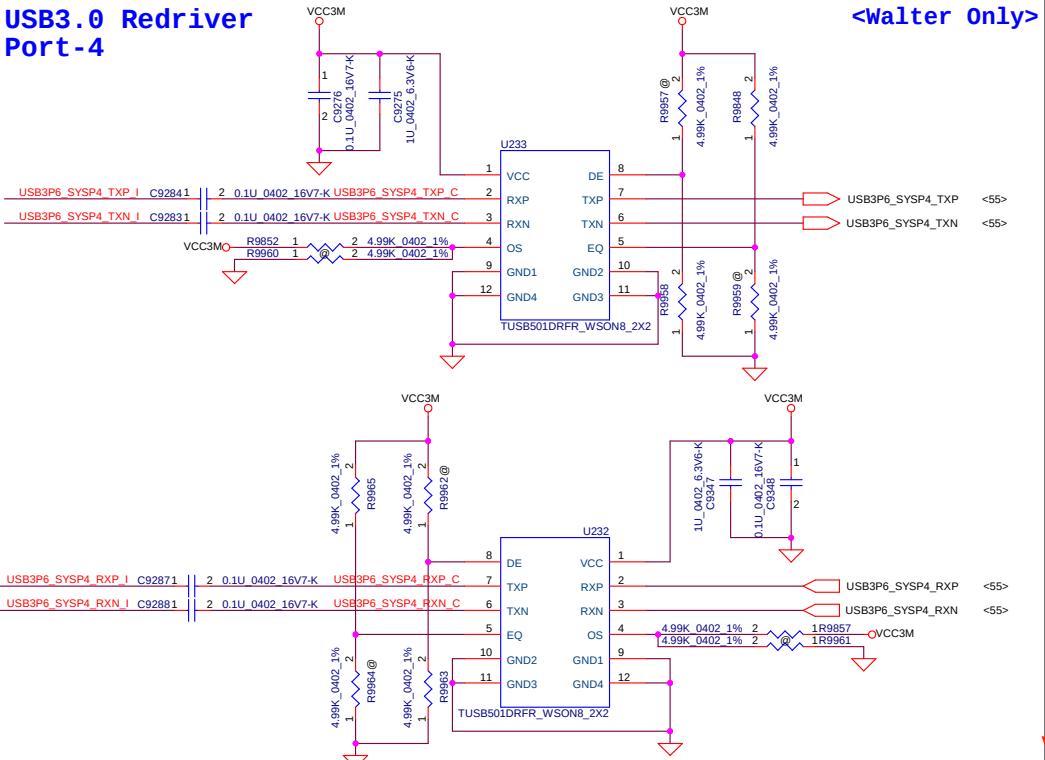
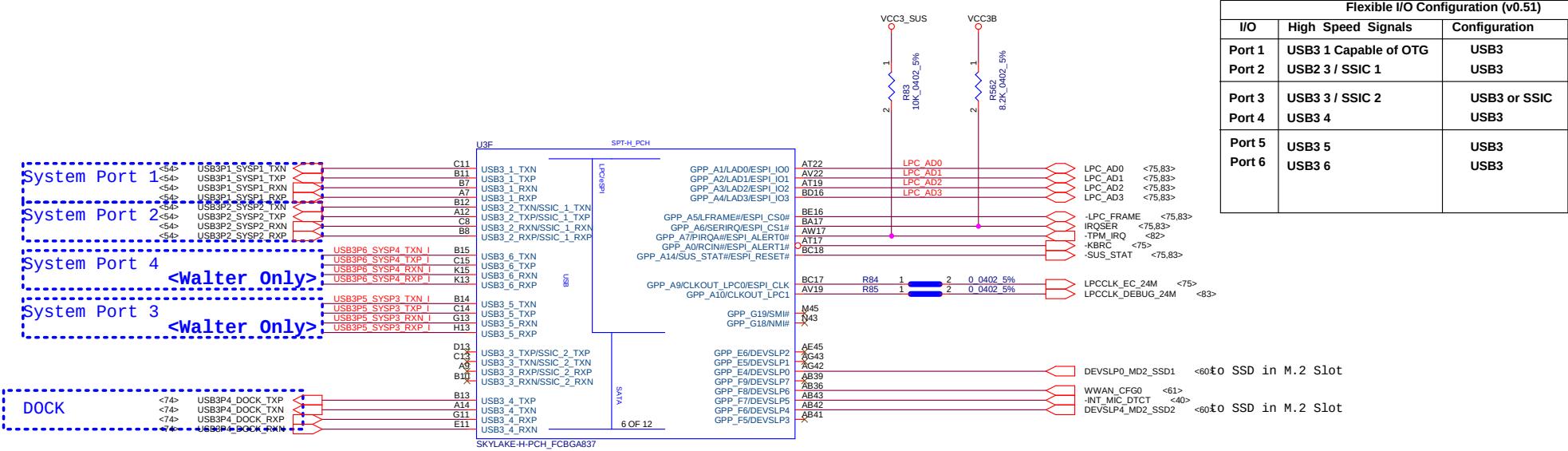


EC SD

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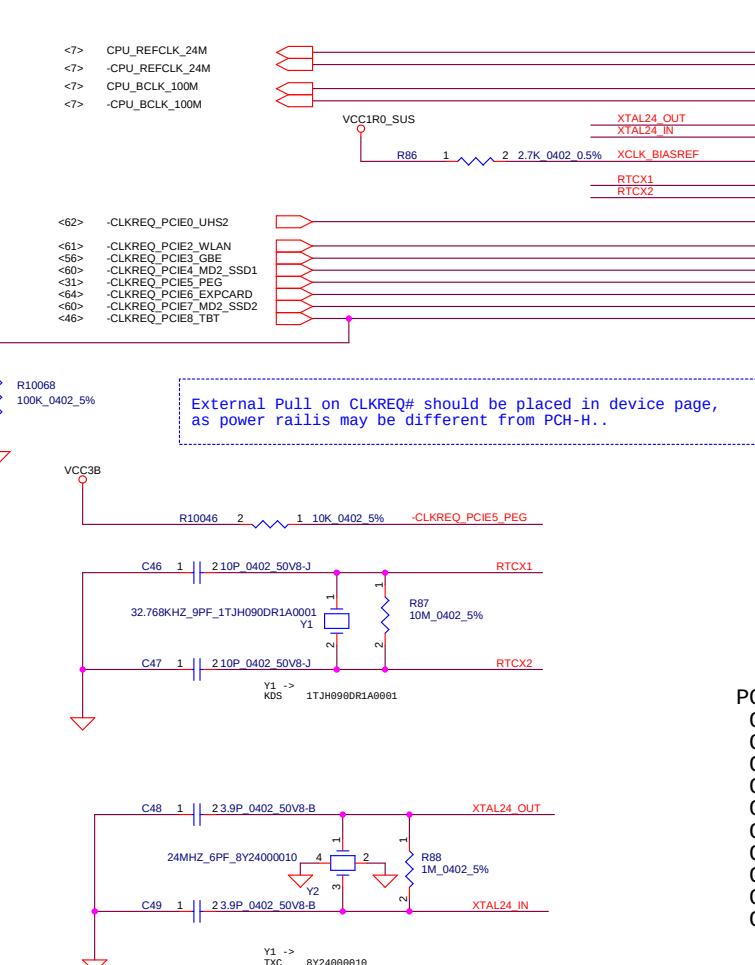


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<7> CPU_REFCLK_24M
 <7> -CPU_REFCLK_24M
 <7> CPU_BCLK_100M
 <7> -CPU_BCLK_100M

<62> -CLKREQ_PCIE0_UHS2
 <61> -CLKREQ_PCIE2_WLAN
 <60> -CLKREQ_PCIE3_GBE
 <60> -CLKREQ_PCIE4_MD2_SSD1
 <31> -CLKREQ_PCIE5_PEG
 <64> -CLKREQ_PCIE6_EXPCARD
 <60> -CLKREQ_PCIE7_MD2_SSD2
 <46> -CLKREQ_PCIE8_TBT

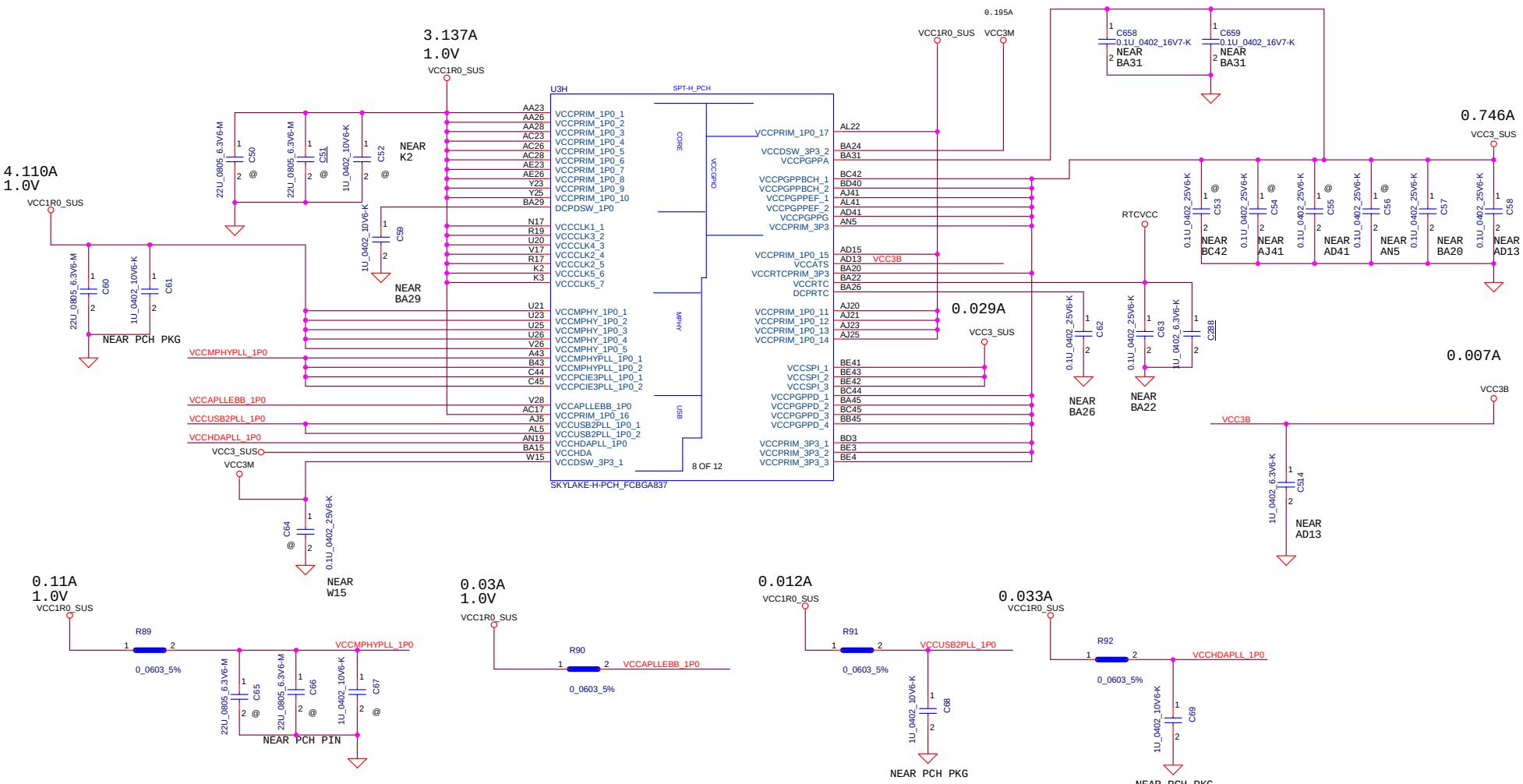


PCIE Clock Assignment

- Clock 0 : UHS II
- Clock 1 : NA
- Clock 2 : Wireless LAN M.2 Slot
- Clock 3 : Giga Bit Ethernet
- Clock 4 : PCIe SSD on M.2 Slot
- Clock 5 : Discrete GFX(MXM or Onboard)
- Clock 6 : Express Slot
- Clock 7 : PCIe SSD on M.2 Slot
- Clock 8 : Thunderbolt
- Clock 9 - 15 : NA

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Custom				
Date:	Friday, October 02, 2015	Sheet	20	of 116

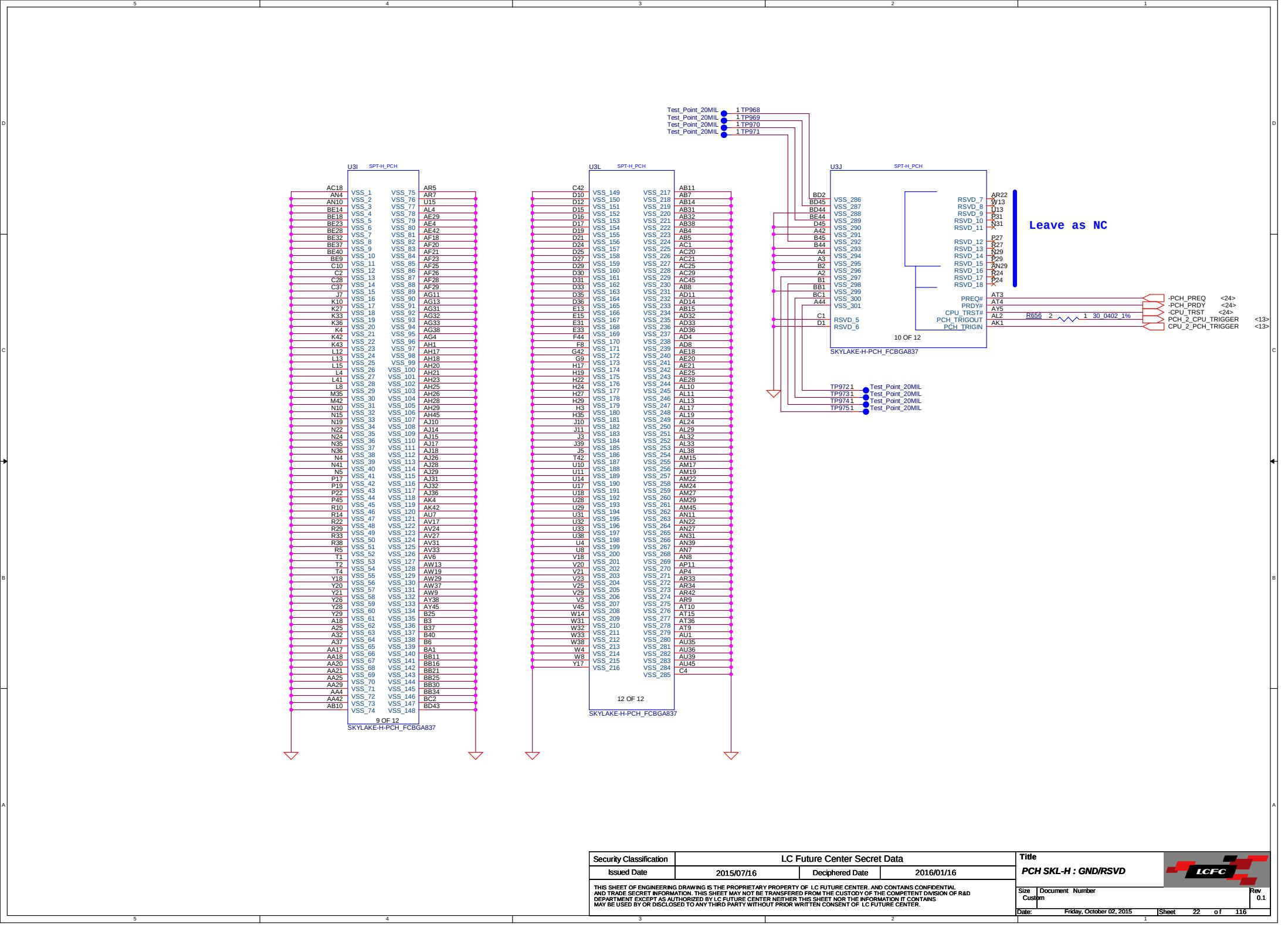
To use eSPI, VCCPGPPA should have 1.8V

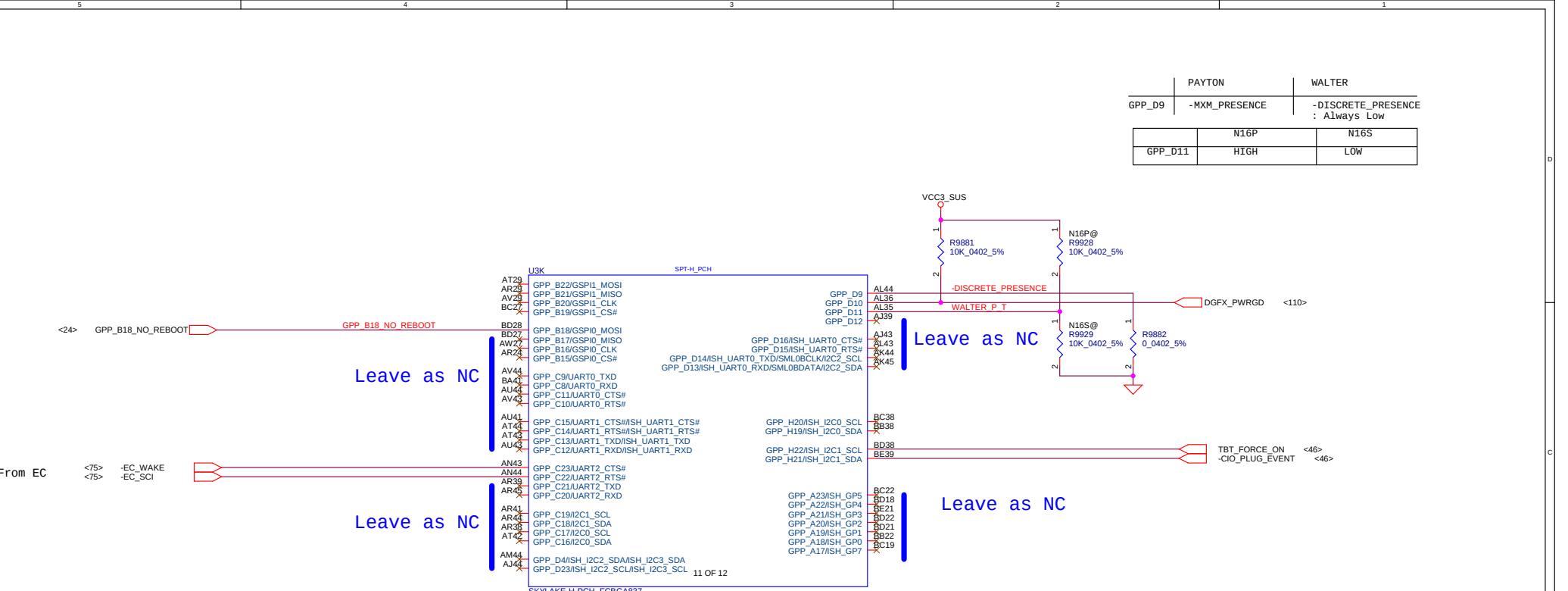


Note 1: Ampere in this page means Iccmax current described in SKL PCH H EDS r0.91 page 57.

Note 2: Decoupling capacitors refers SKL H PDG r0.7 page 507.
SKL H RVP11 schematics r0.5 also referred.

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TABLE : CPU ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R591	NO ASM	NO ASM	ASM
R593	NO ASM	NO ASM	ASM
R594	NO ASM	NO ASM	ASM
R595	NO ASM	NO ASM	ASM
R596	NO ASM	NO ASM	ASM
R657	NO ASM	NO ASM	ASM
R658	NO ASM	NO ASM	ASM
R102	NO ASM	ASM	NO ASM
R597	NO ASM	ASM	NO ASM
R9907	NO ASM	ASM	ASM
JXDP1	NO ASM	ASM	NO ASM
C70	NO ASM	ASM	NO ASM
R96	ASM	ASM	ASM
R101	NO ASM	ASM	NO ASM
R9909	NO ASM	ASM	ASM
R9910	NO ASM	ASM	ASM
R9916	NO ASM	ASM	ASM
R99	NO ASM	ASM	ASM
R9912	NO ASM	ASM	ASM
R9934	NO ASM	ASM	ASM
R9930	NO ASM	ASM	ASM
R9931	NO ASM	ASM	ASM
R9932	NO ASM	ASM	ASM
R9933	NO ASM	ASM	ASM

↑
LOGIC

TABLE : PCH ITP DEBUG REPORT

	No use	Individual Port	DCI 2.0 w/o connector
R93	NO ASM	ASM	NO ASM
JXDP1	NO ASM	ASM	NO ASM
R9917	NO ASM	ASM	NO ASM
R101	NO ASM	ASM	NO ASM
R9908	NO ASM	ASM	NO ASM
R9911	NO ASM	ASM	NO ASM
R9913	NO ASM	ASM	NO ASM
R9915	NO ASM	ASM	NO ASM

1

R820	NO ASM	ASM	NO ASM
R821	NO ASM	ASM	NO ASM
R822	NO ASM	ASM	NO ASM

SHEET 4

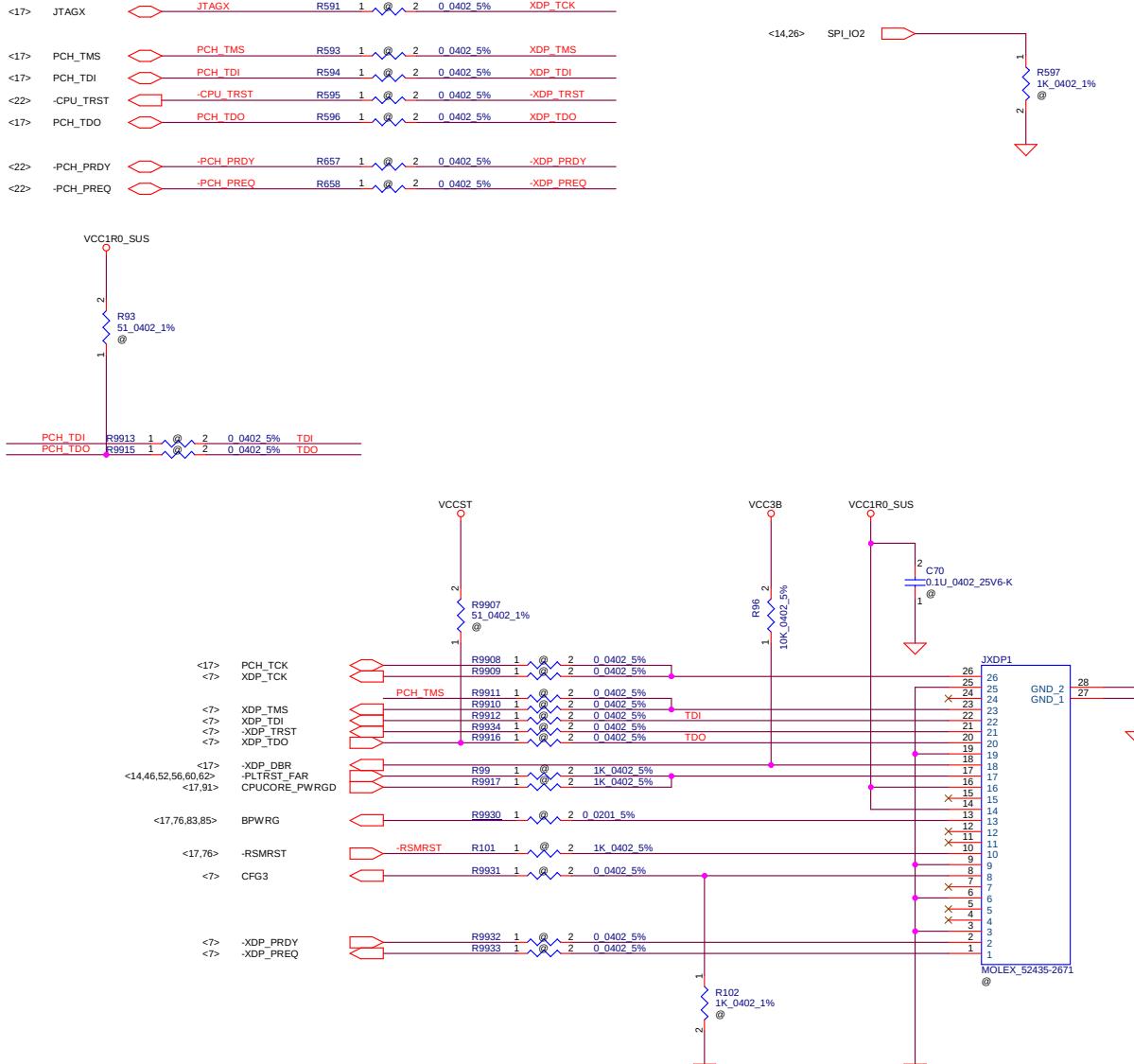


TABLE : Functional Strain

TABLE 1: Functional Setup		
GPP_B18/GSPI10_MOSI (No Reboot)		R563
HIGH	Enable "No Reboot" Mode	ASM
LOW	Disable "No Reboot" Mode (Default)	NO ASM

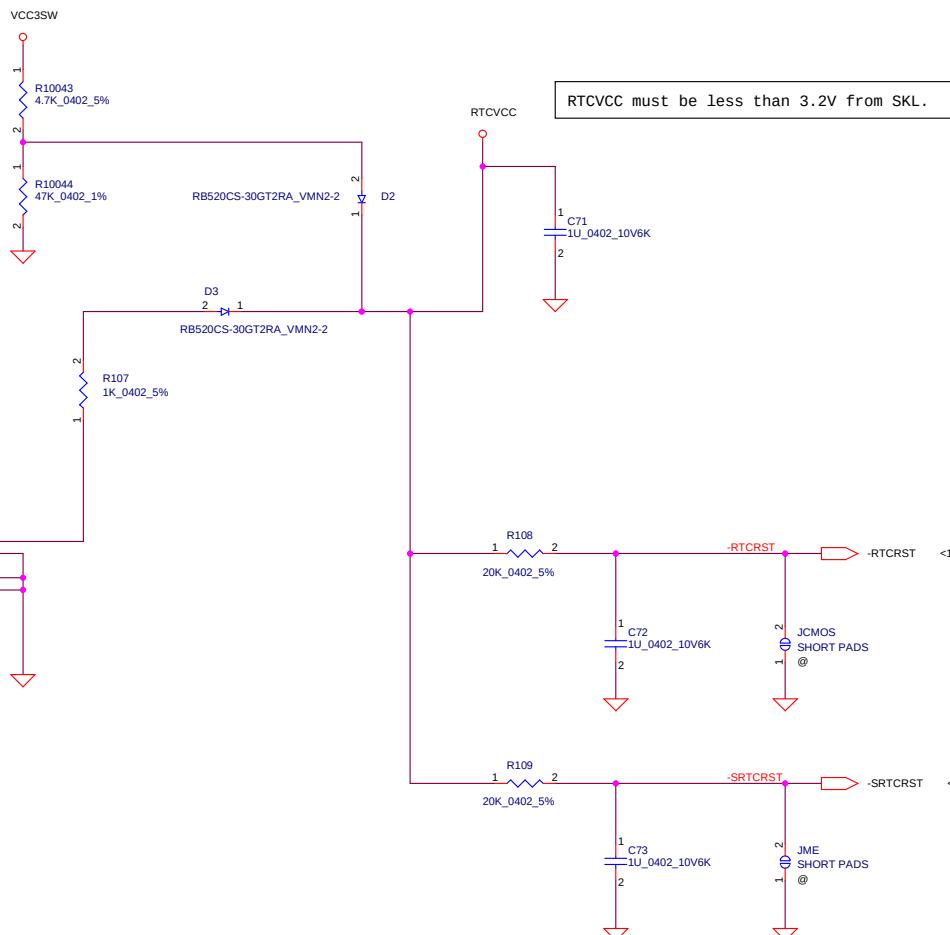
1 R563
2 @
Place near PCH

GPP_B18_NO_REBOOT

<23>

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Title				
XDP CONNECTOR				
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	R110	R598	U5	R592	R358
PRE ES1 ES1/ES2	NO ASM	ASM	QE="1"	ASM	ASM
AFTER QS	ASM	NO ASM	QE= Don't Care	NO ASM	NO ASM

LOGIC

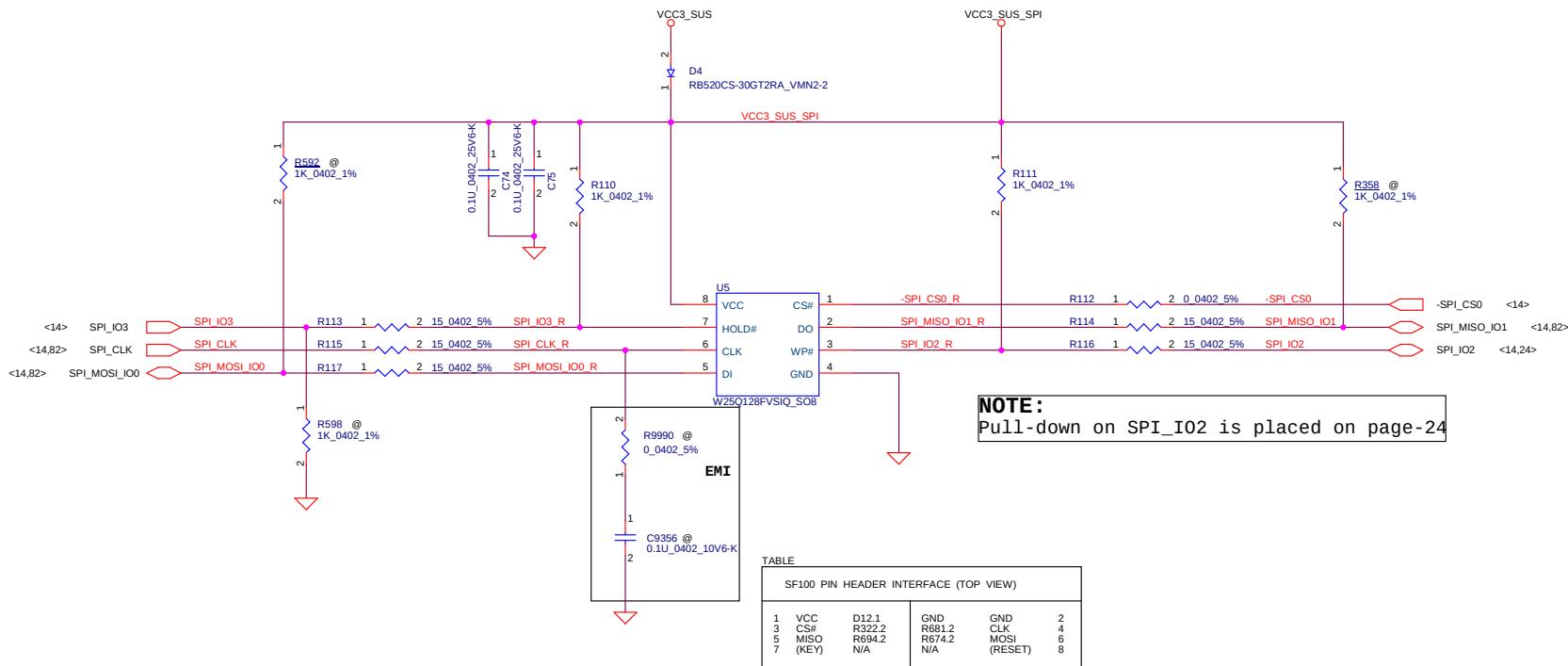
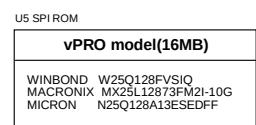
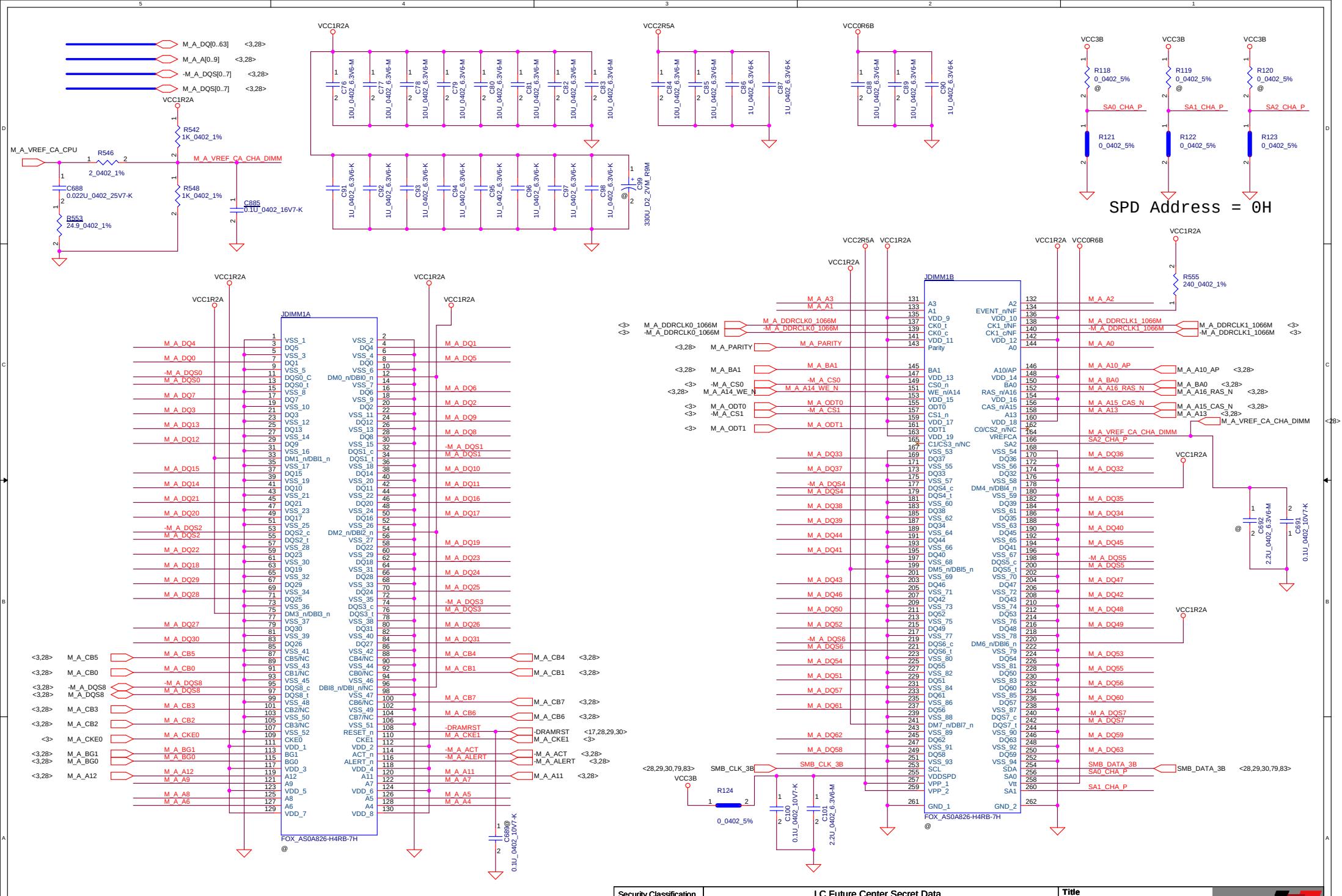


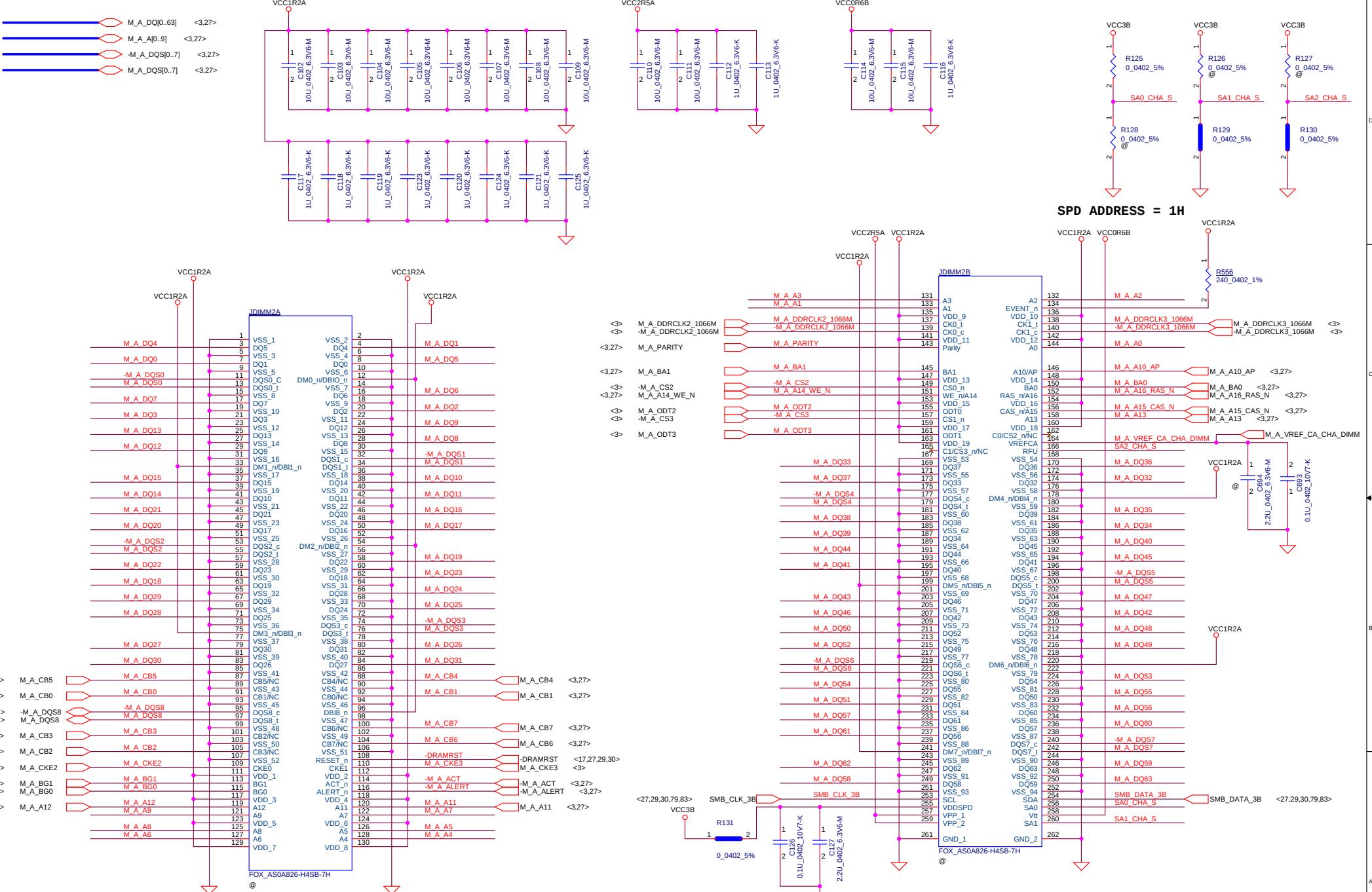
TABLE							
SF100 PIN HEADER INTERFACE (TOP VIEW)							
1	VCC	D12.1	GND	2			
3	CS#	R322.2	R681.2	4			
5	MISO (KEY)	R694.2	R674.2	6			
7		N/A	N/A	8			



vinafix



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Title

DDR4 CH-A SECONDARY



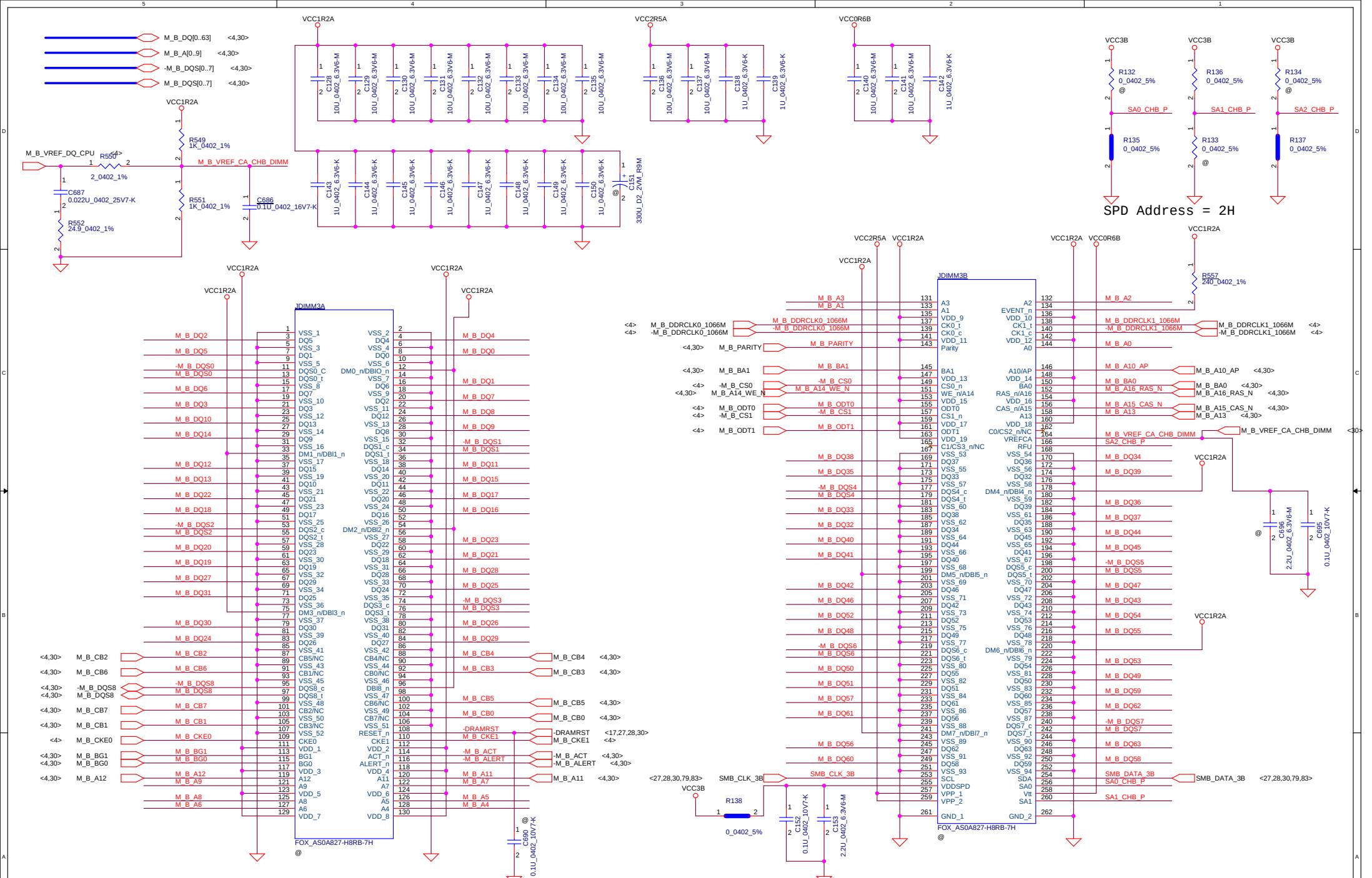
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Title

DDR4 CH-B PRIMARY



Size

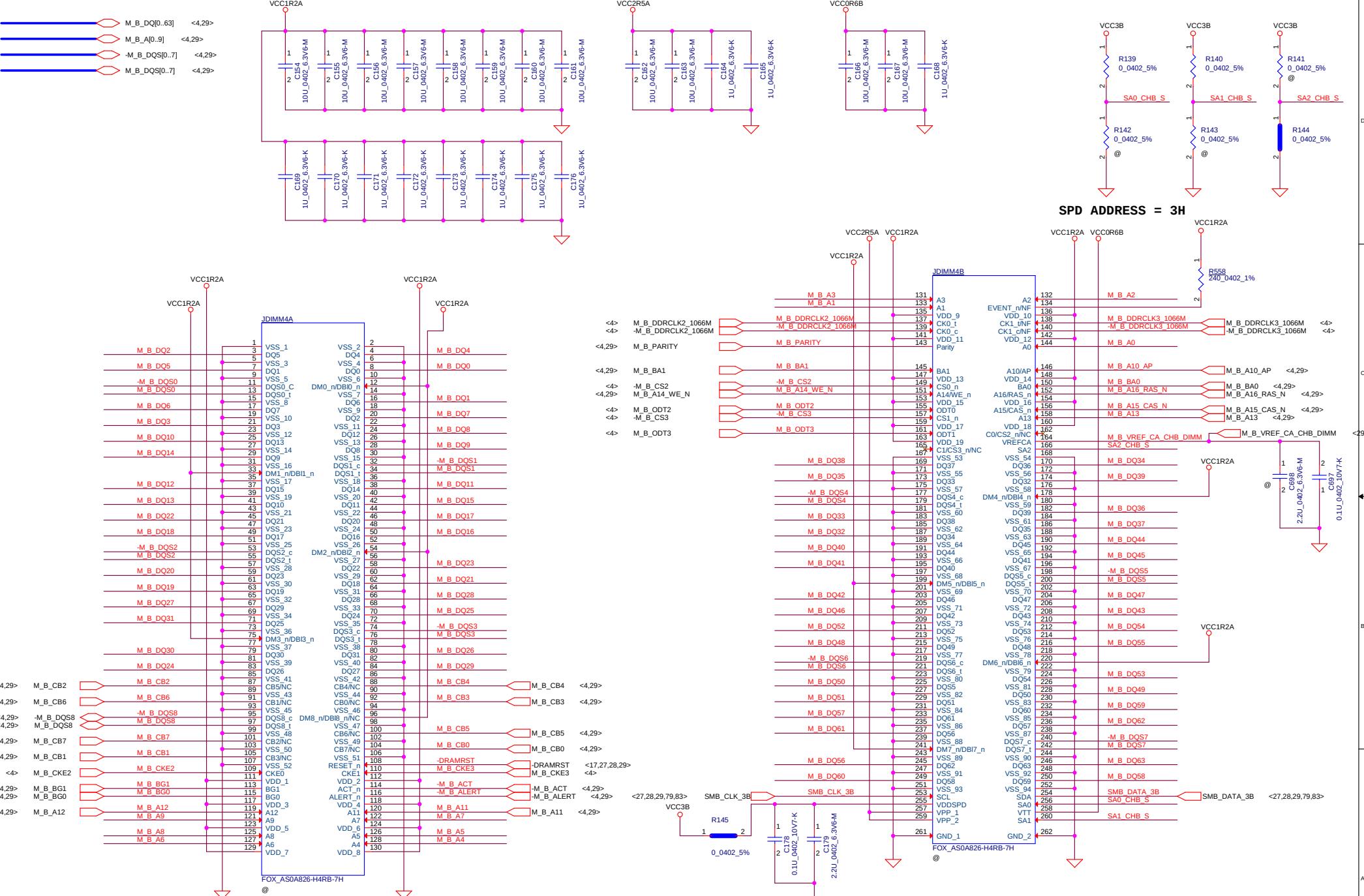
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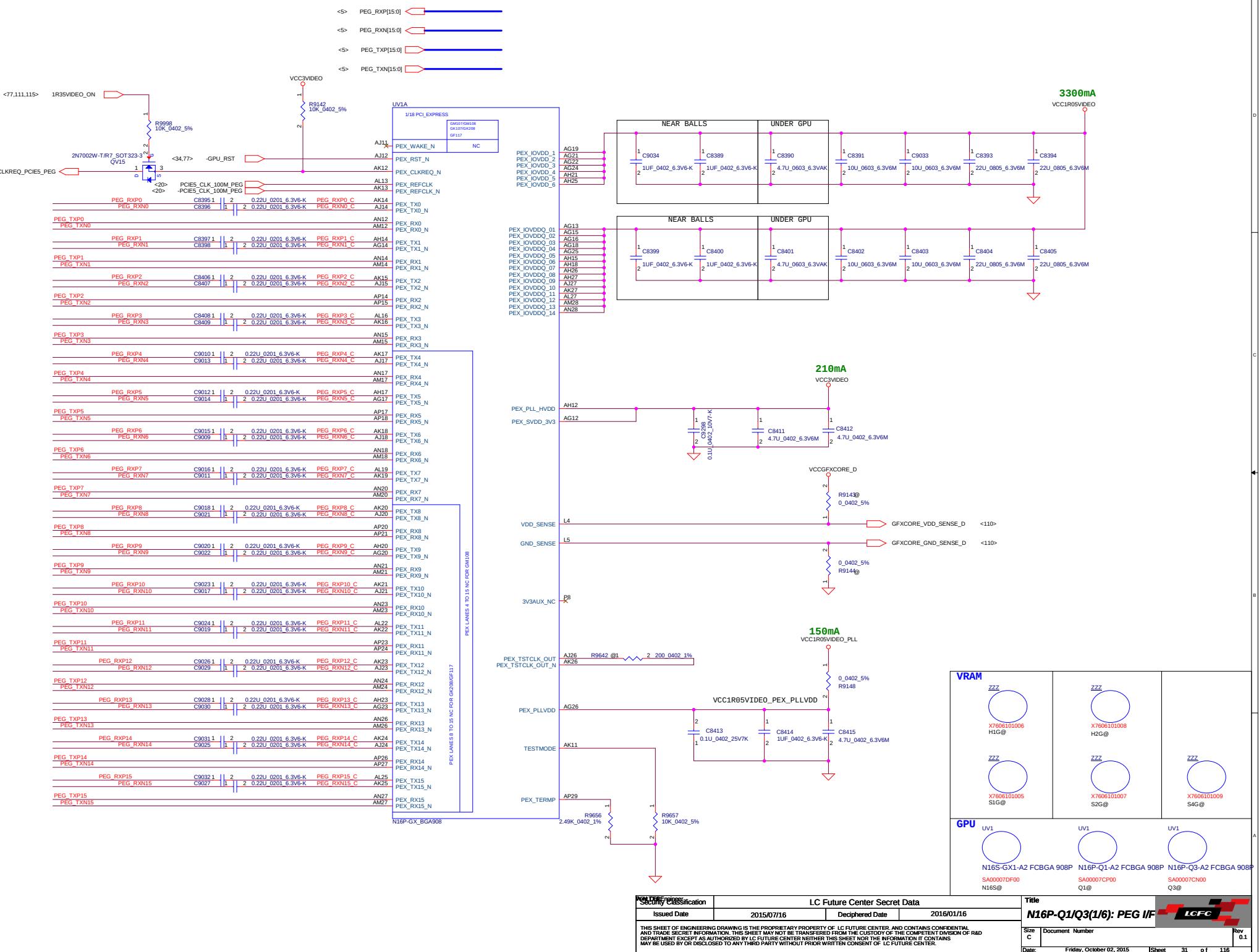
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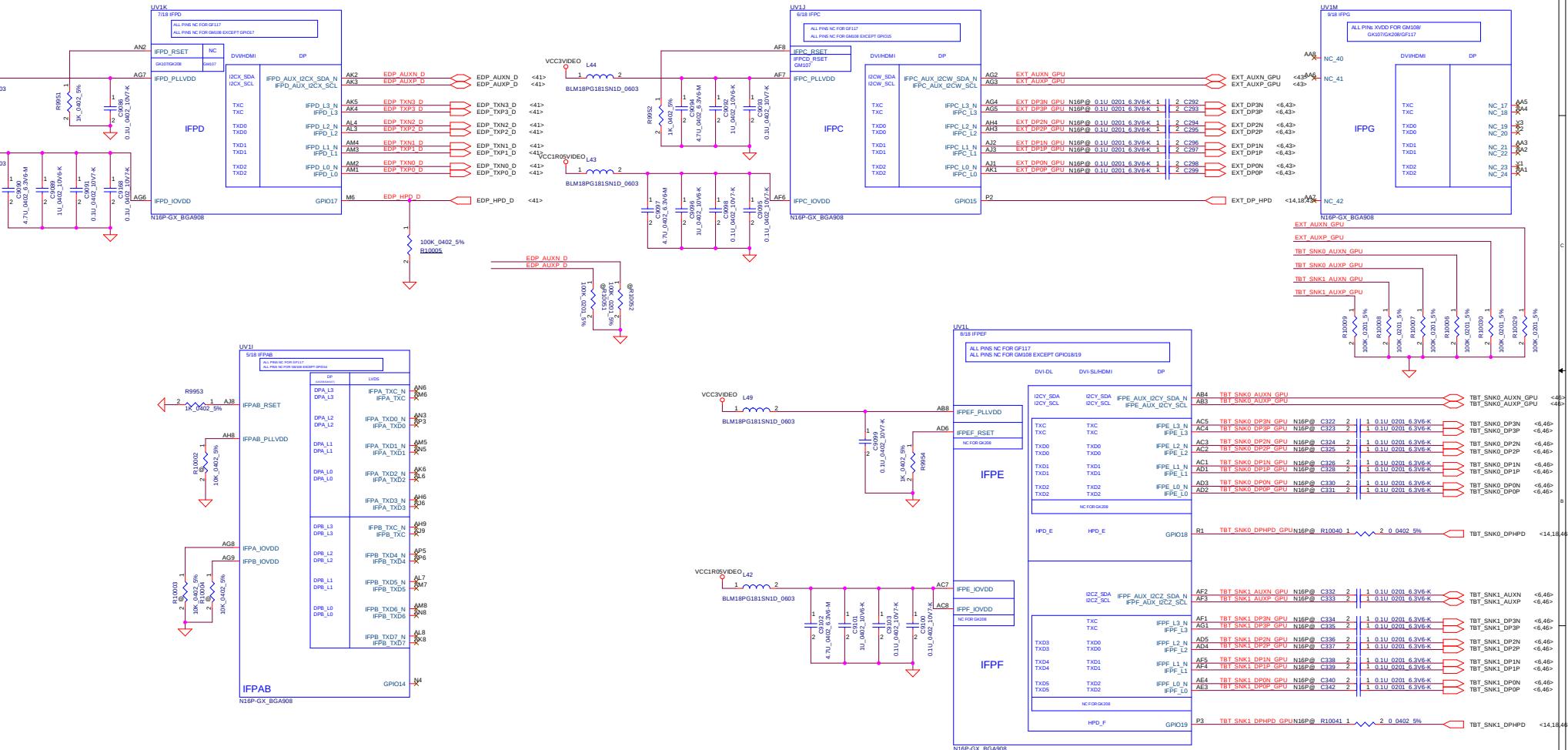
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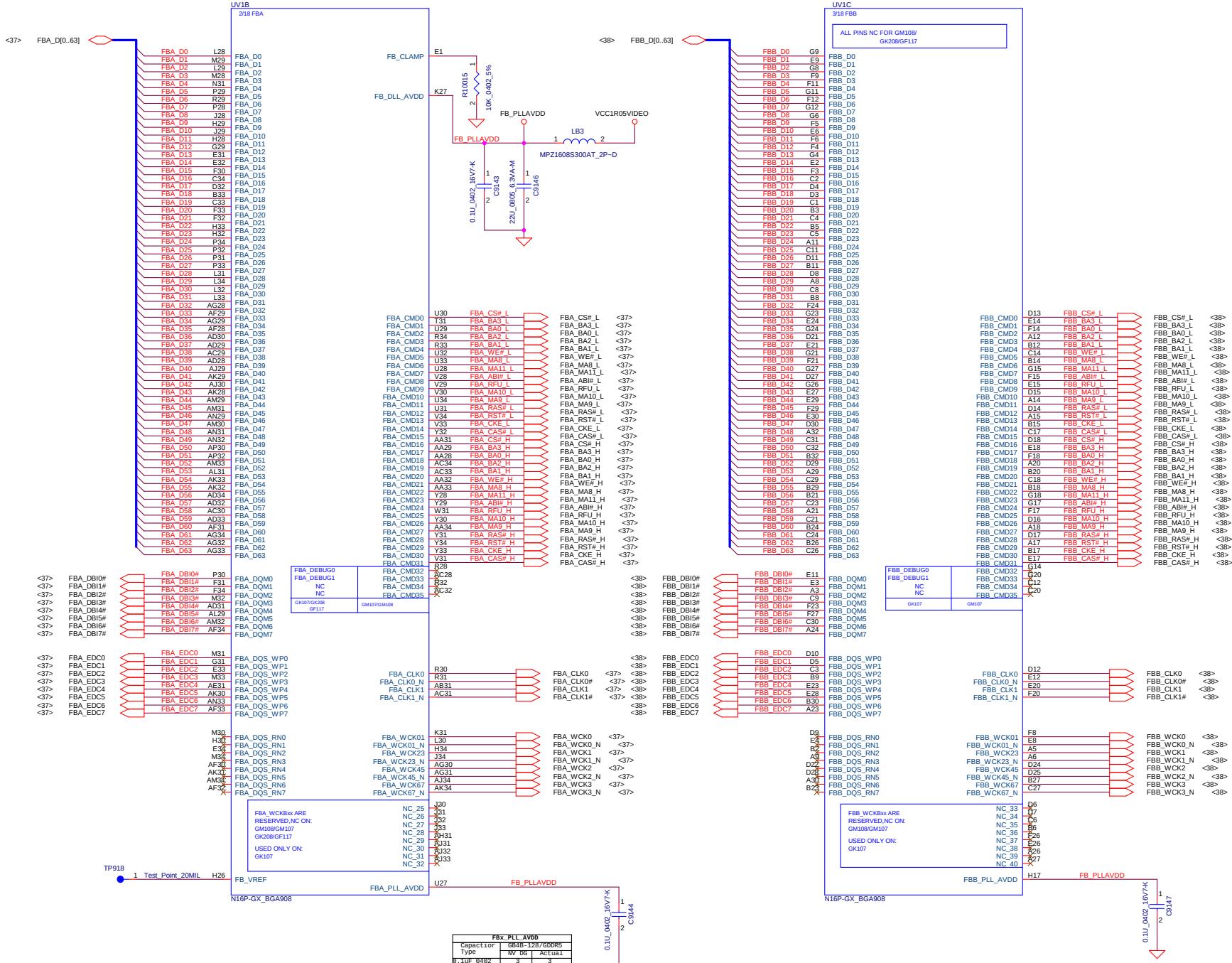
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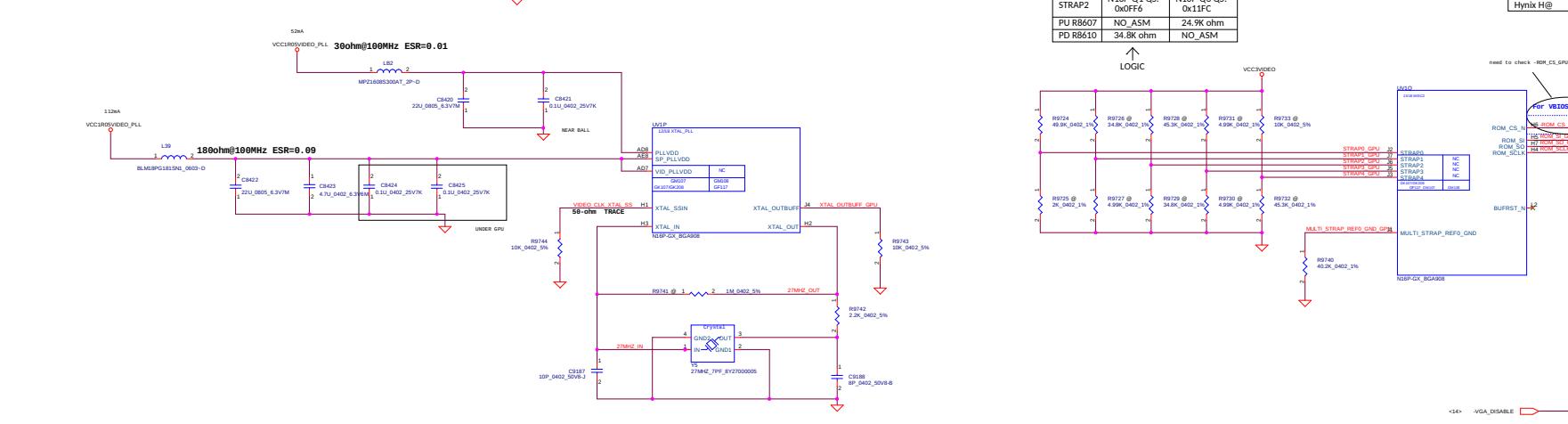
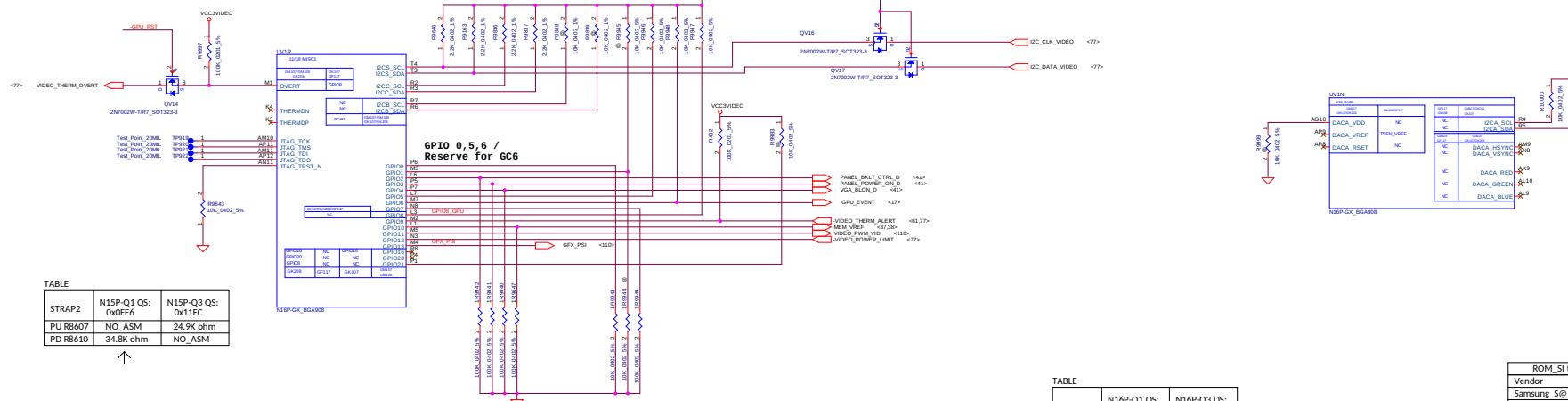




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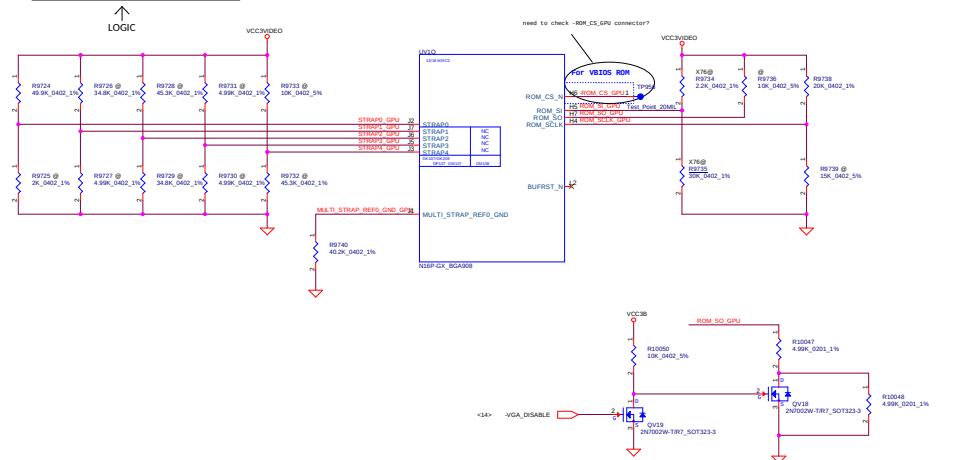
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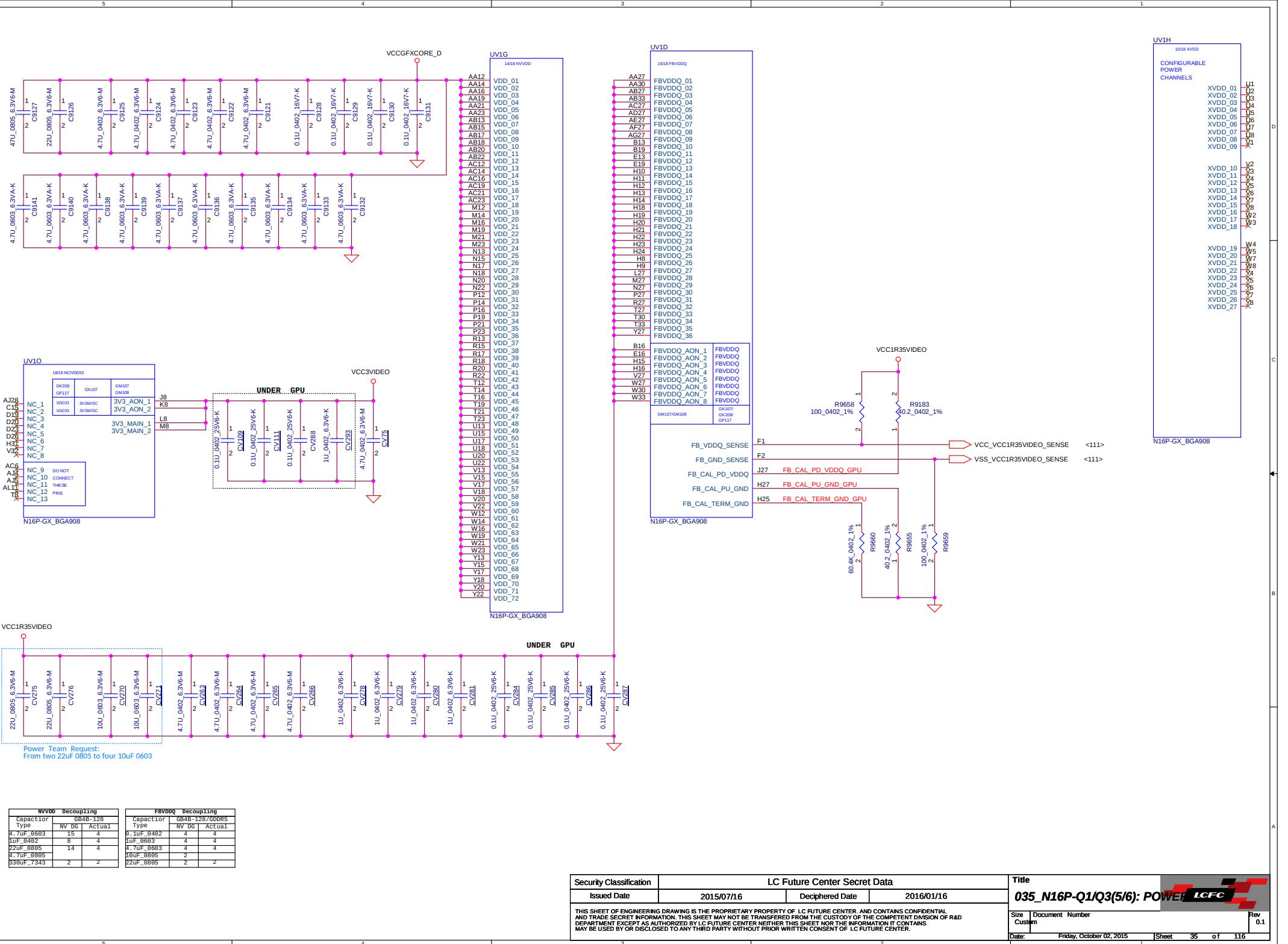


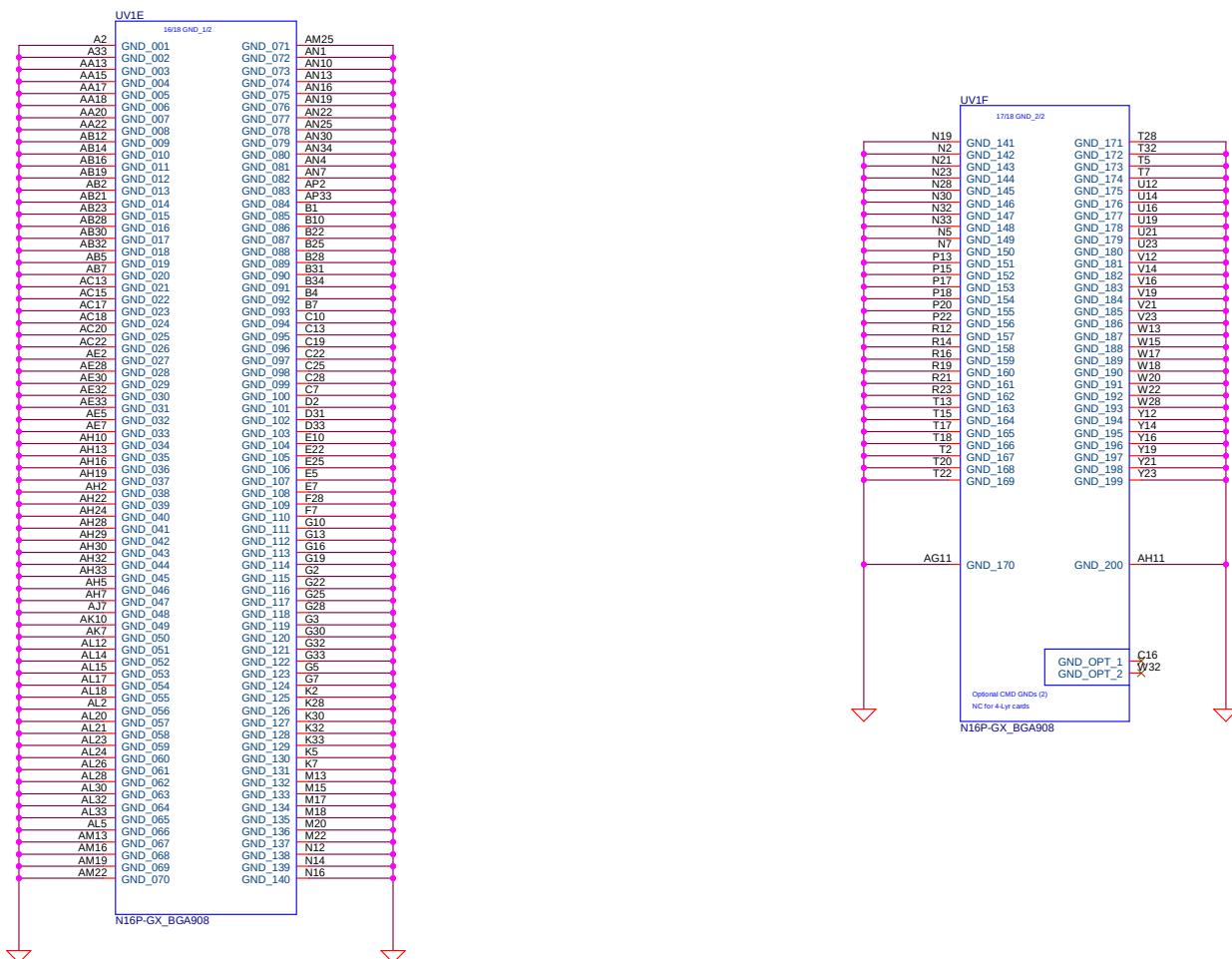
STRAP2	N16P-Q1 QS: 0x0FF6	N16P-Q3 QS: 0x11FC
PU R8607	NO_ASM	24.9K ohm
PD R8610	34.8K ohm	NO_ASM

ROM_SI table for VRAM vendor		
Vendor	PD R9735	LCFC P/N
Samsung S@	20K_1%	SD02820028T
Samsung S@G	4.99K	SD03449910T

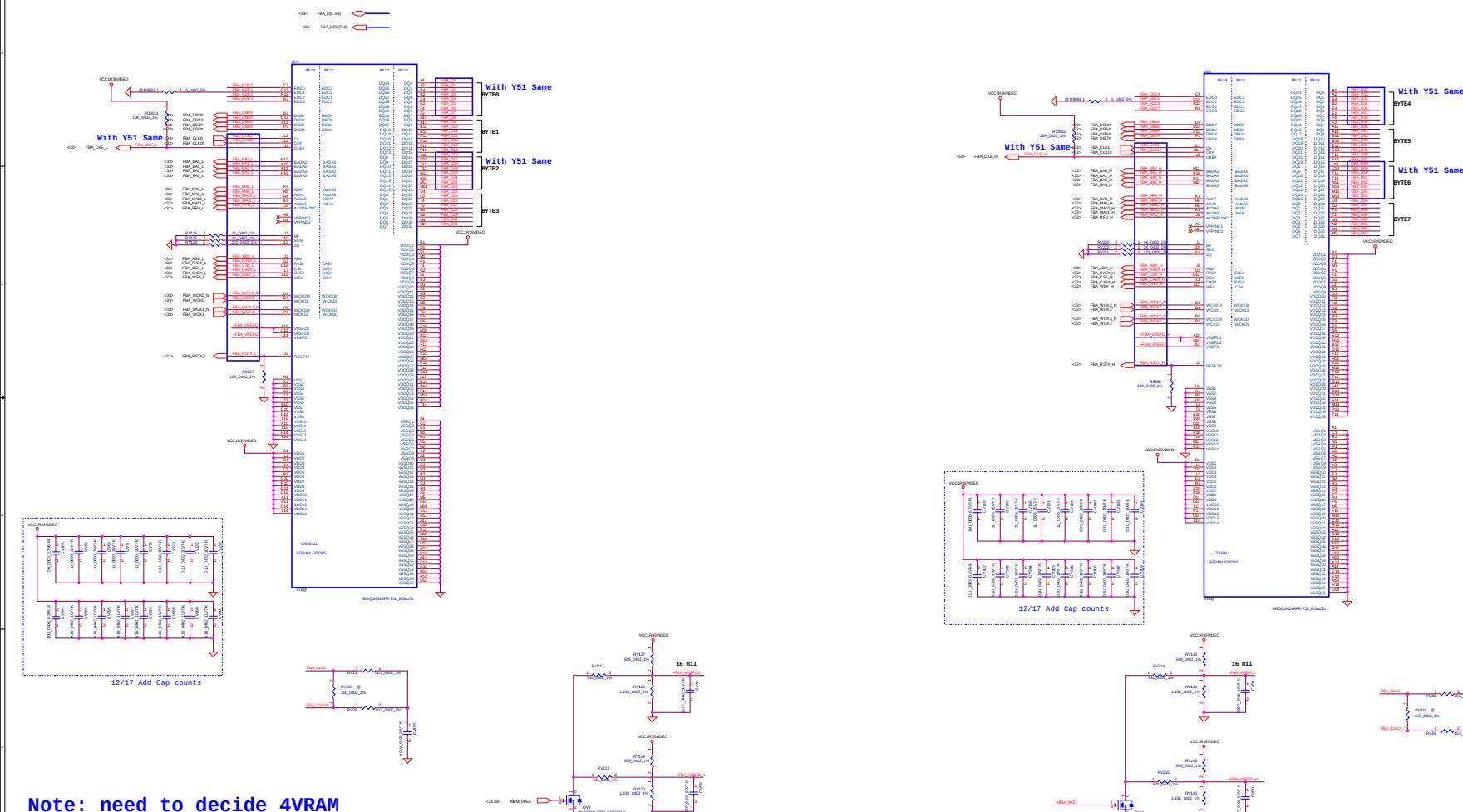
ROM_SI table for 8G VRAM		
Vendor	PU R9734	LCFC P/N
Hynix H@	34.8K_1%	SD03434828T





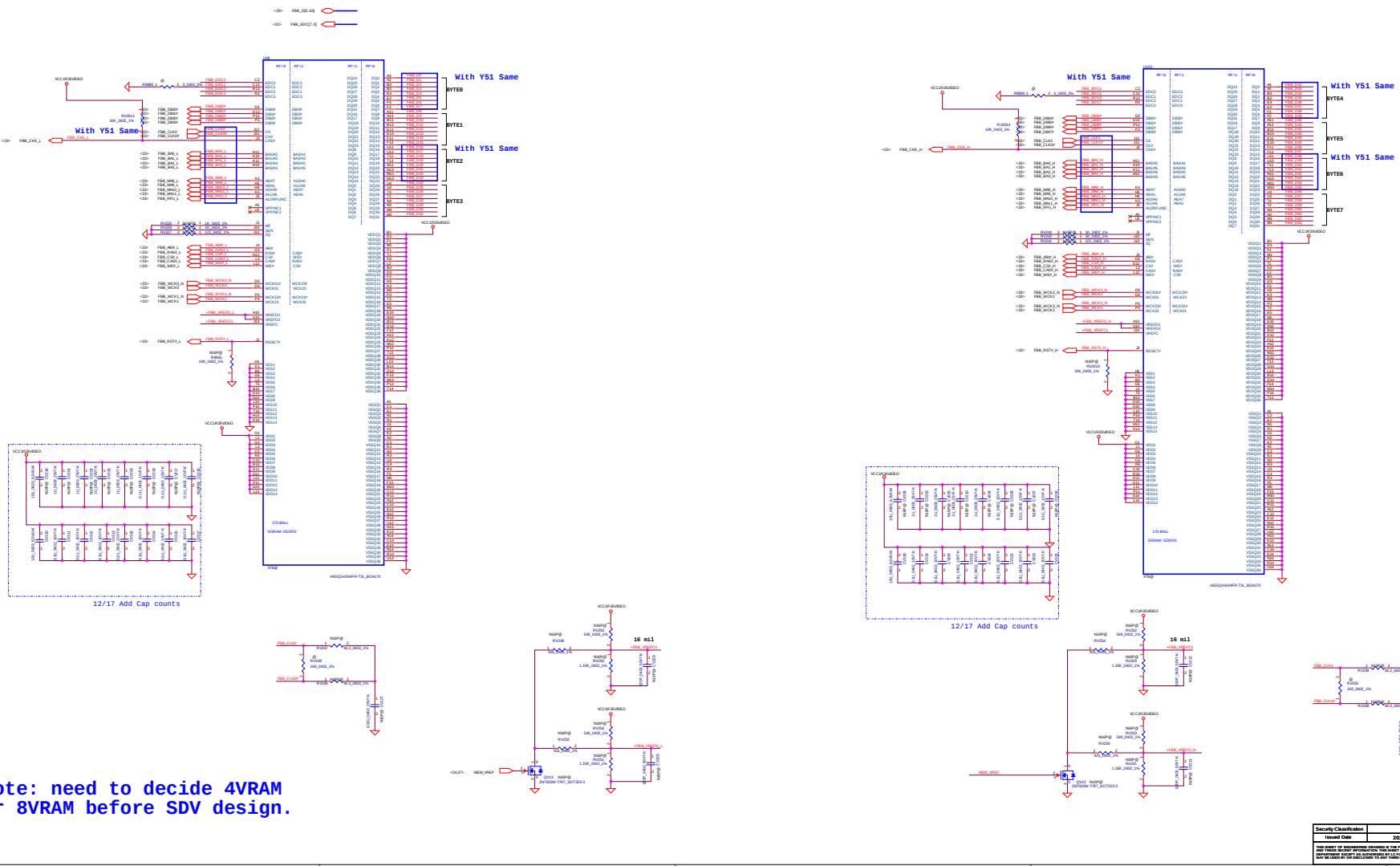


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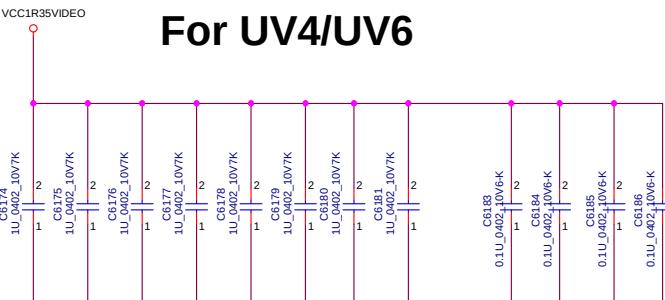
Note: need to decide 4VRAM or 8VRAM before SDV design.

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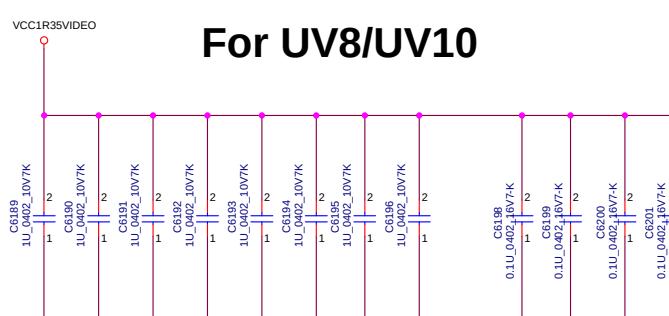
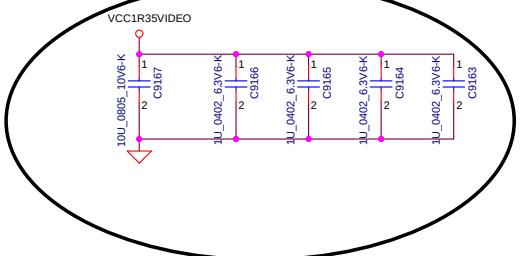
Note: need to decide 4VRAM or 8VRAM before SDV design.

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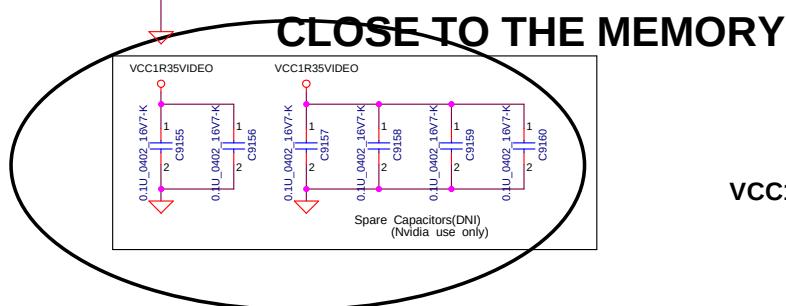


For UV4/UV6

CLOSE TO THE MEMORY



For UV8/UV10

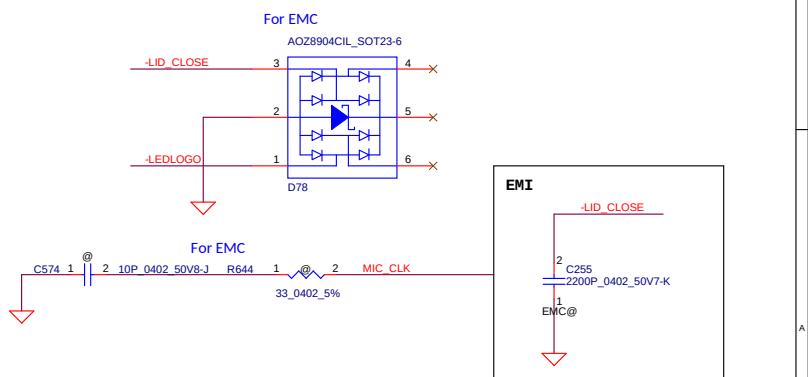
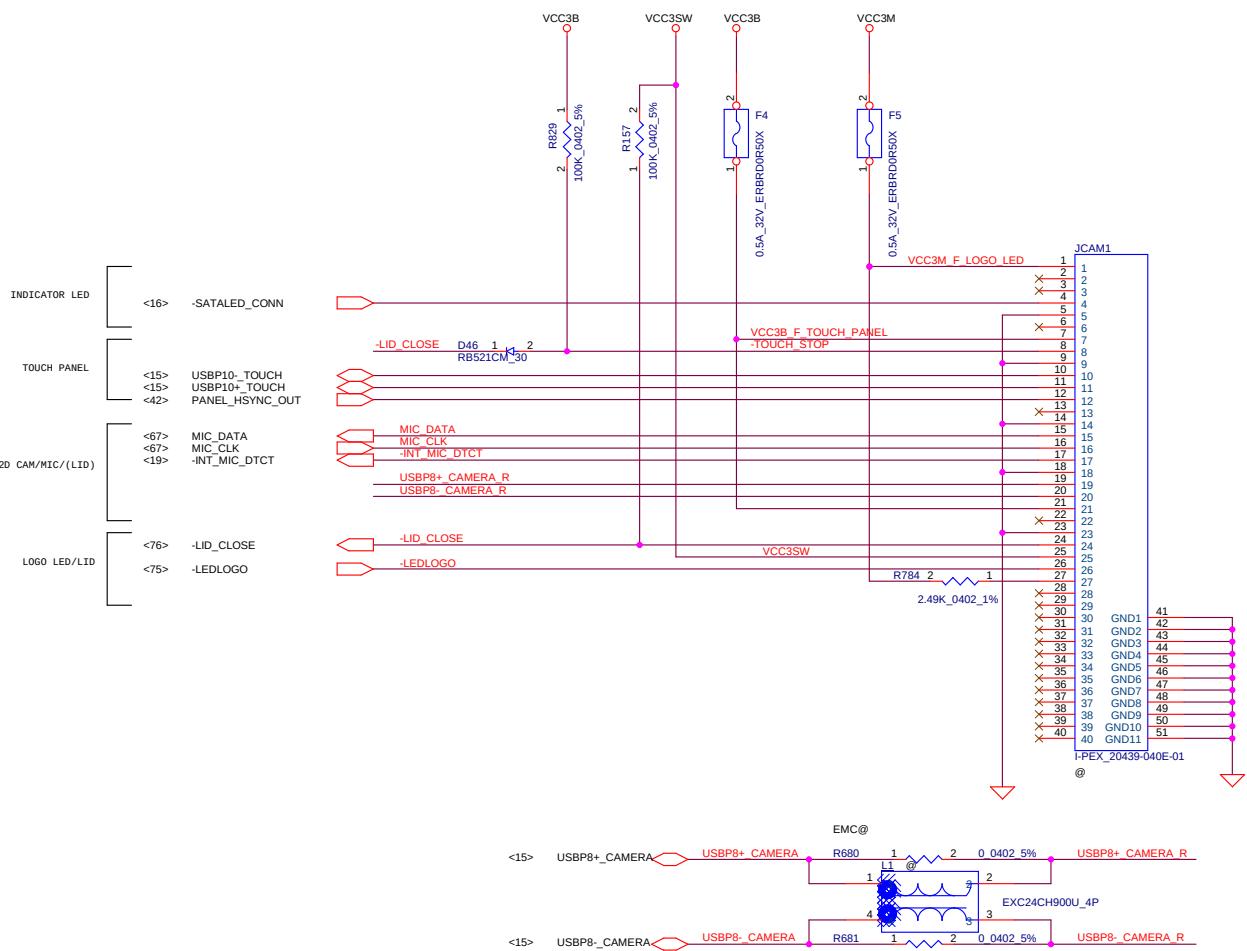
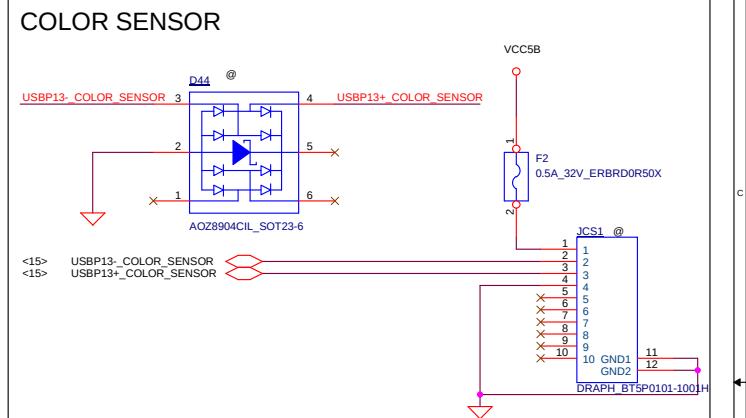
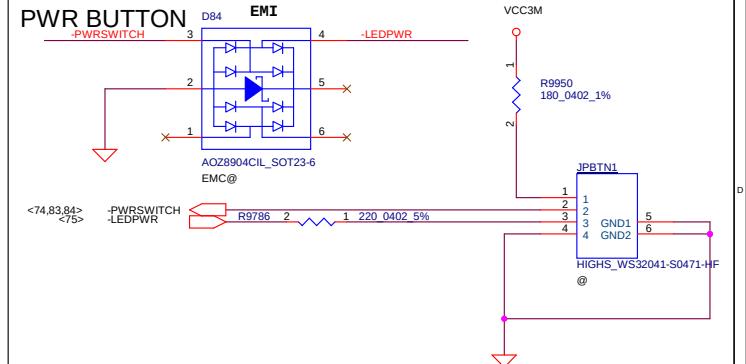


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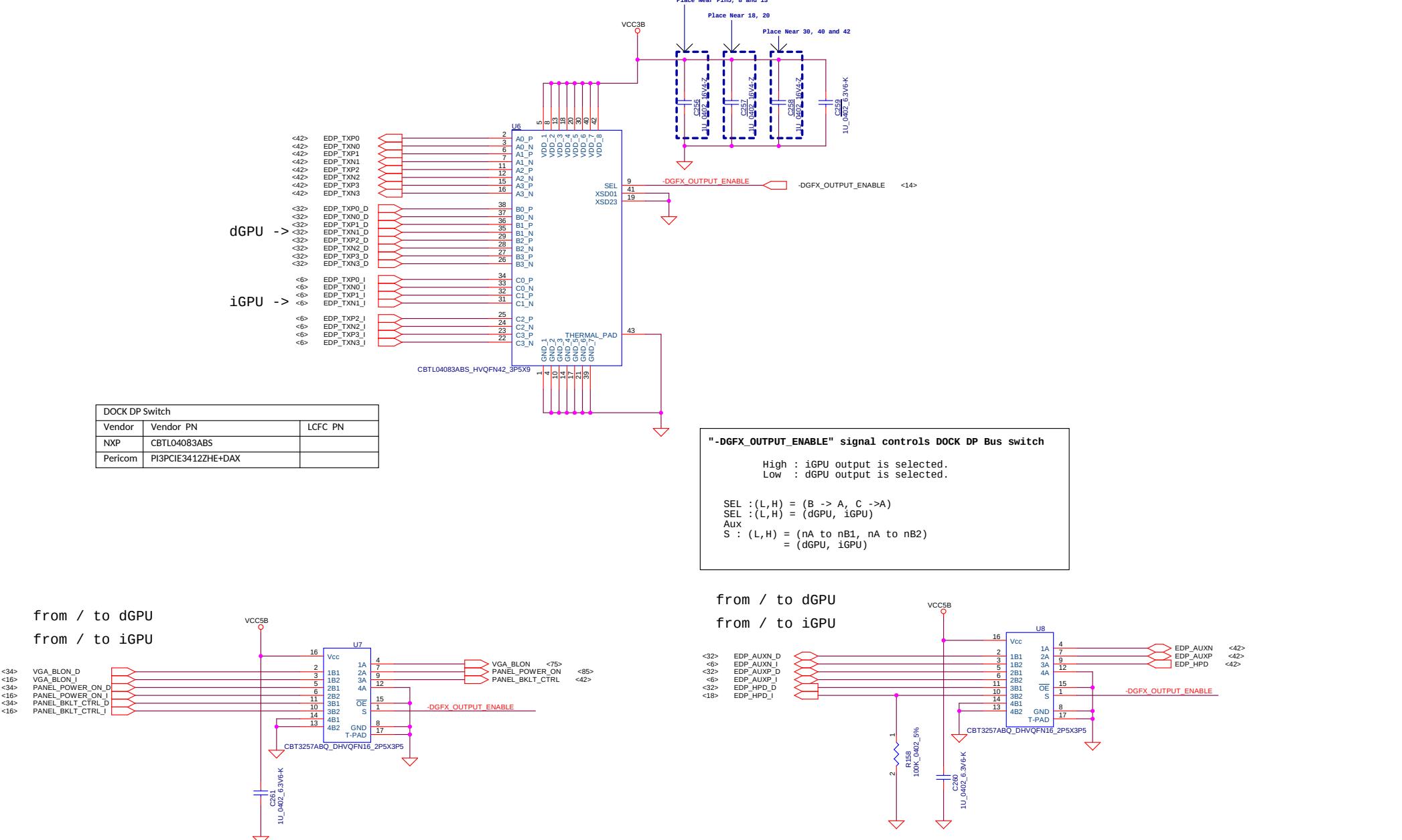
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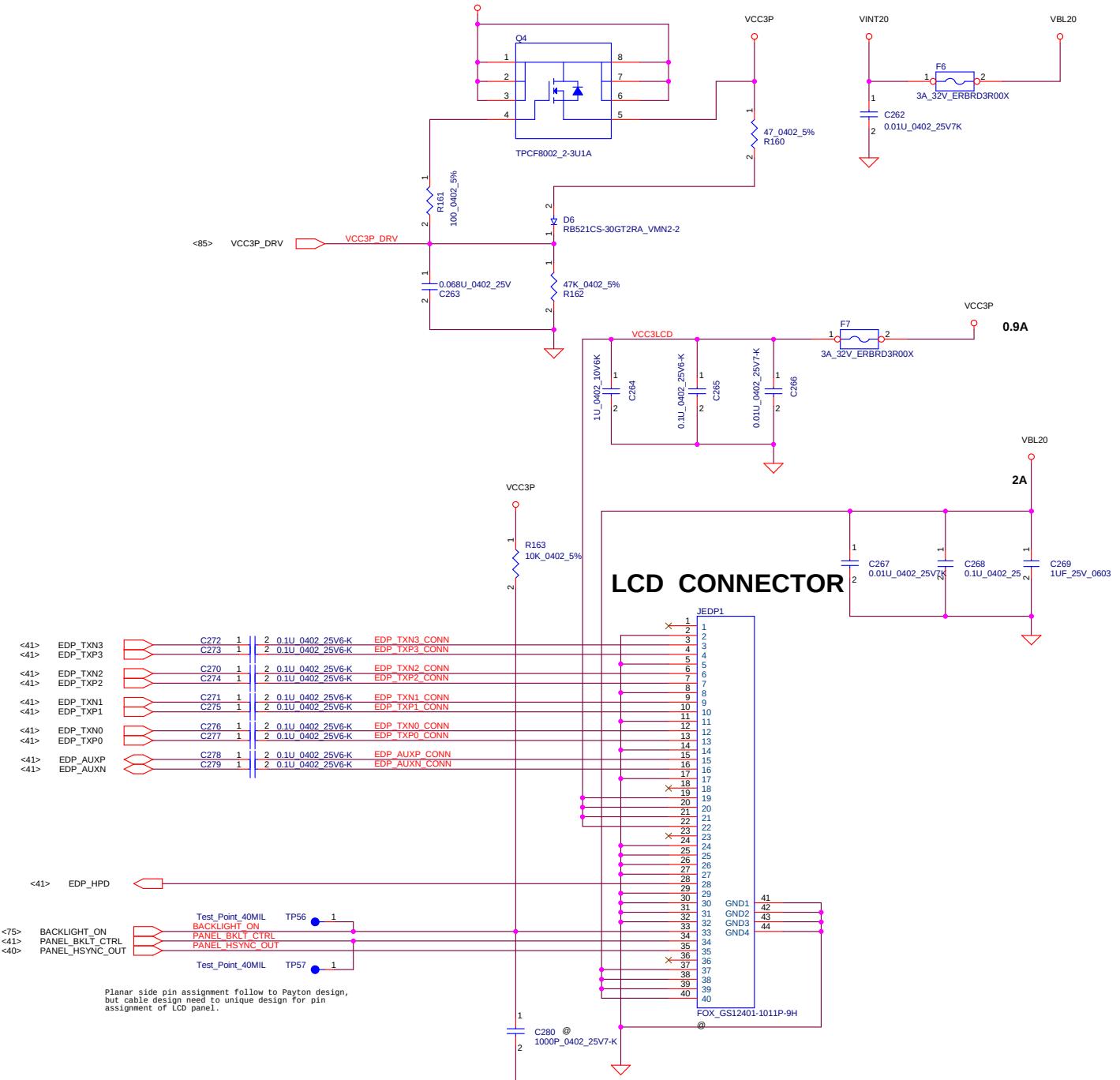
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Title

LCD CONNECTOR



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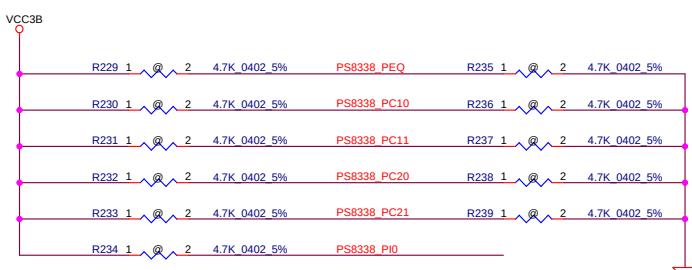
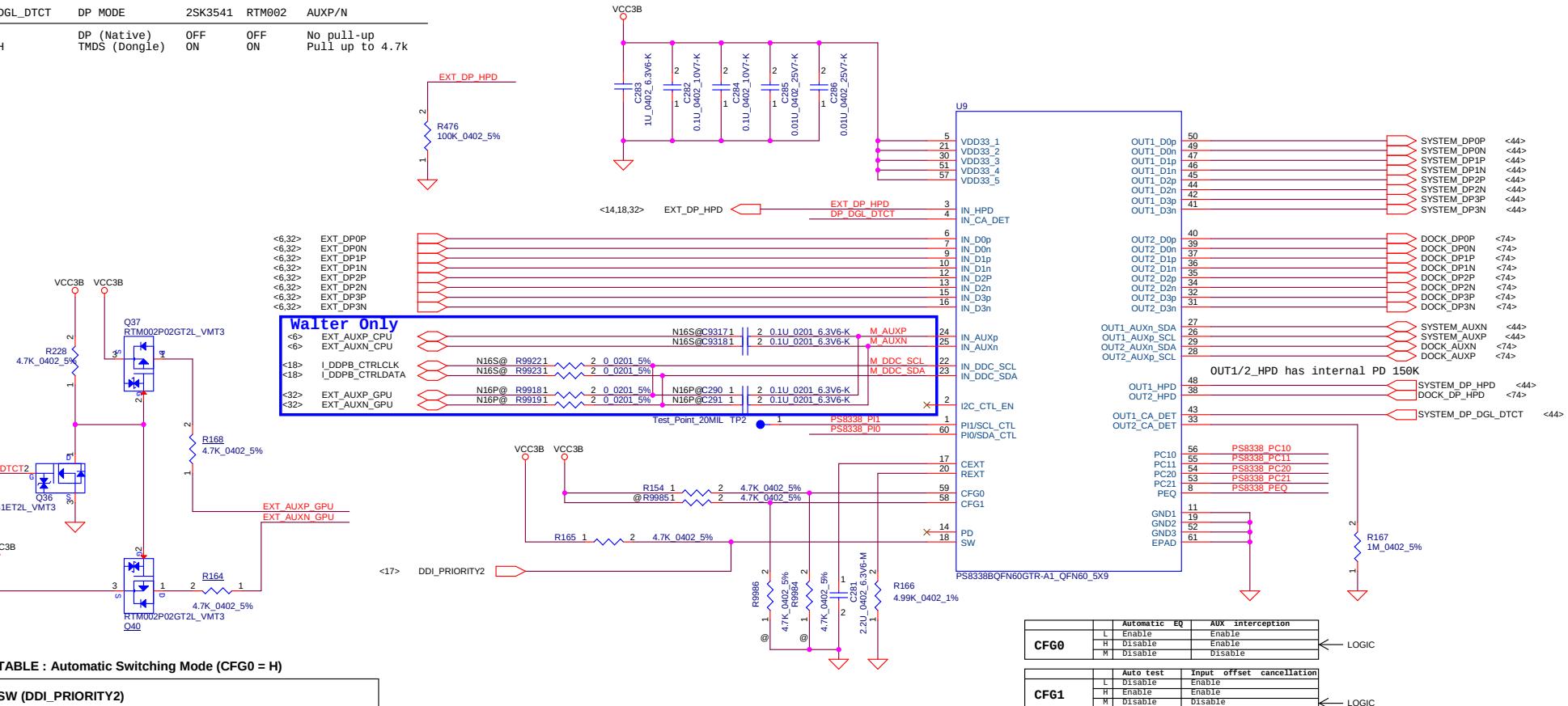
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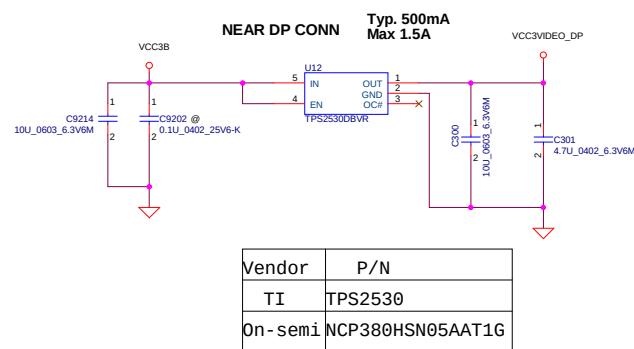
Rev 0.1

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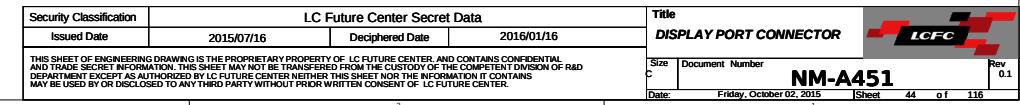
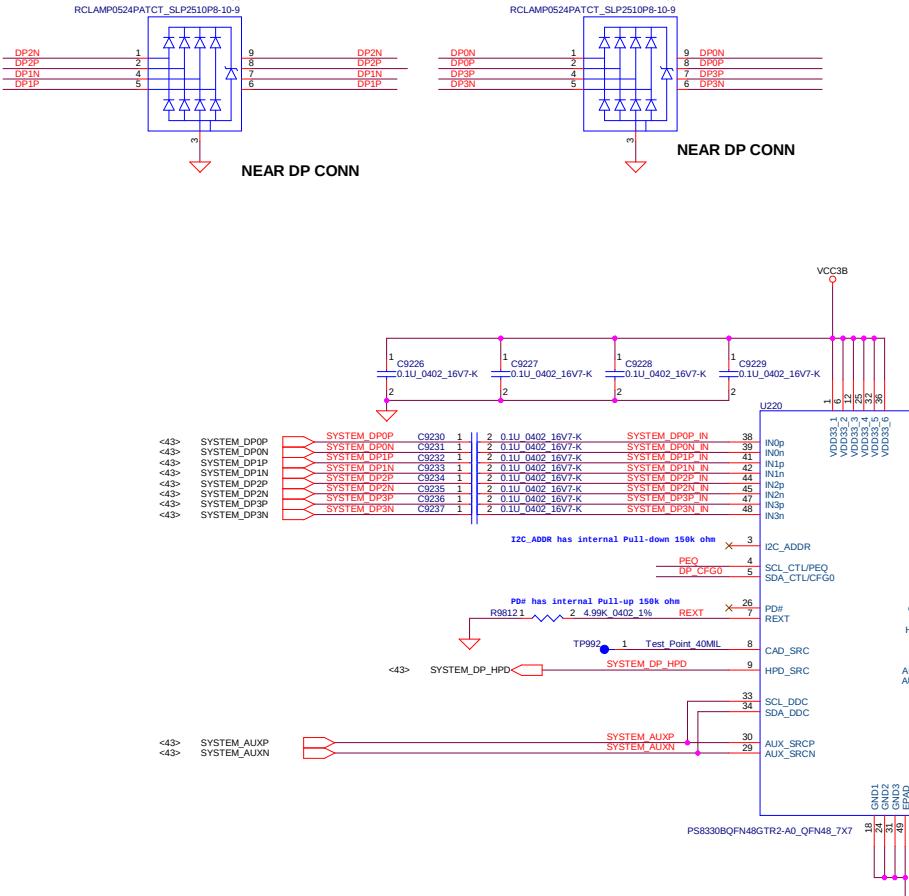
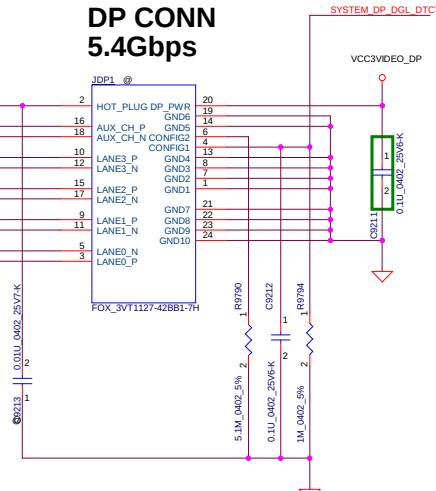
Circuit to turn on/off pull up resistors on AUXP/AUXN to support DP dongles.

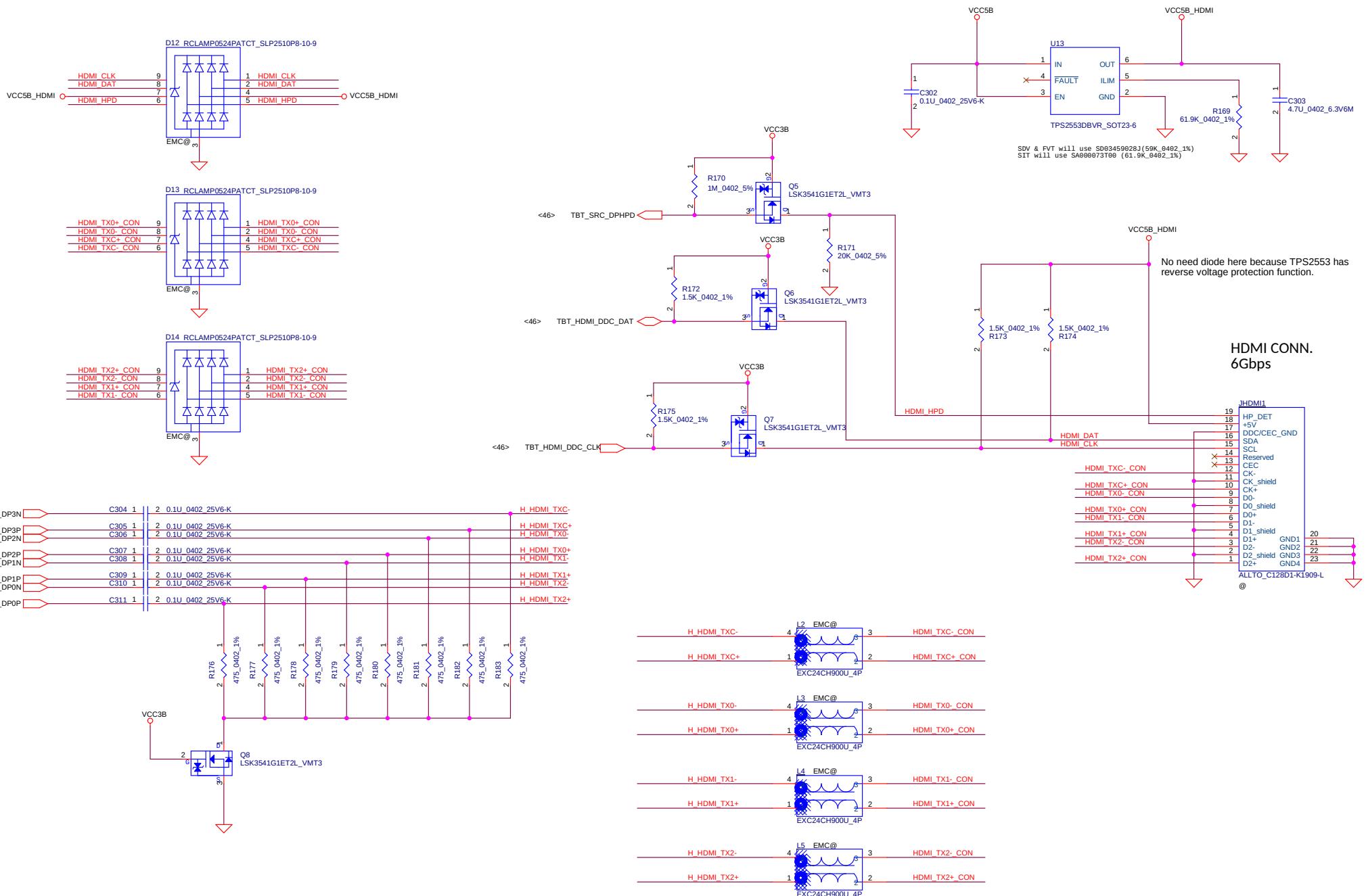
DP_DGL_DTCT	DP MODE	2SK3541	RTM002	AUXP/N
LOW	DP (Native) TMDS (Dongle)	OFF ON	OFF ON	No pull-up Pull up to 4.7k



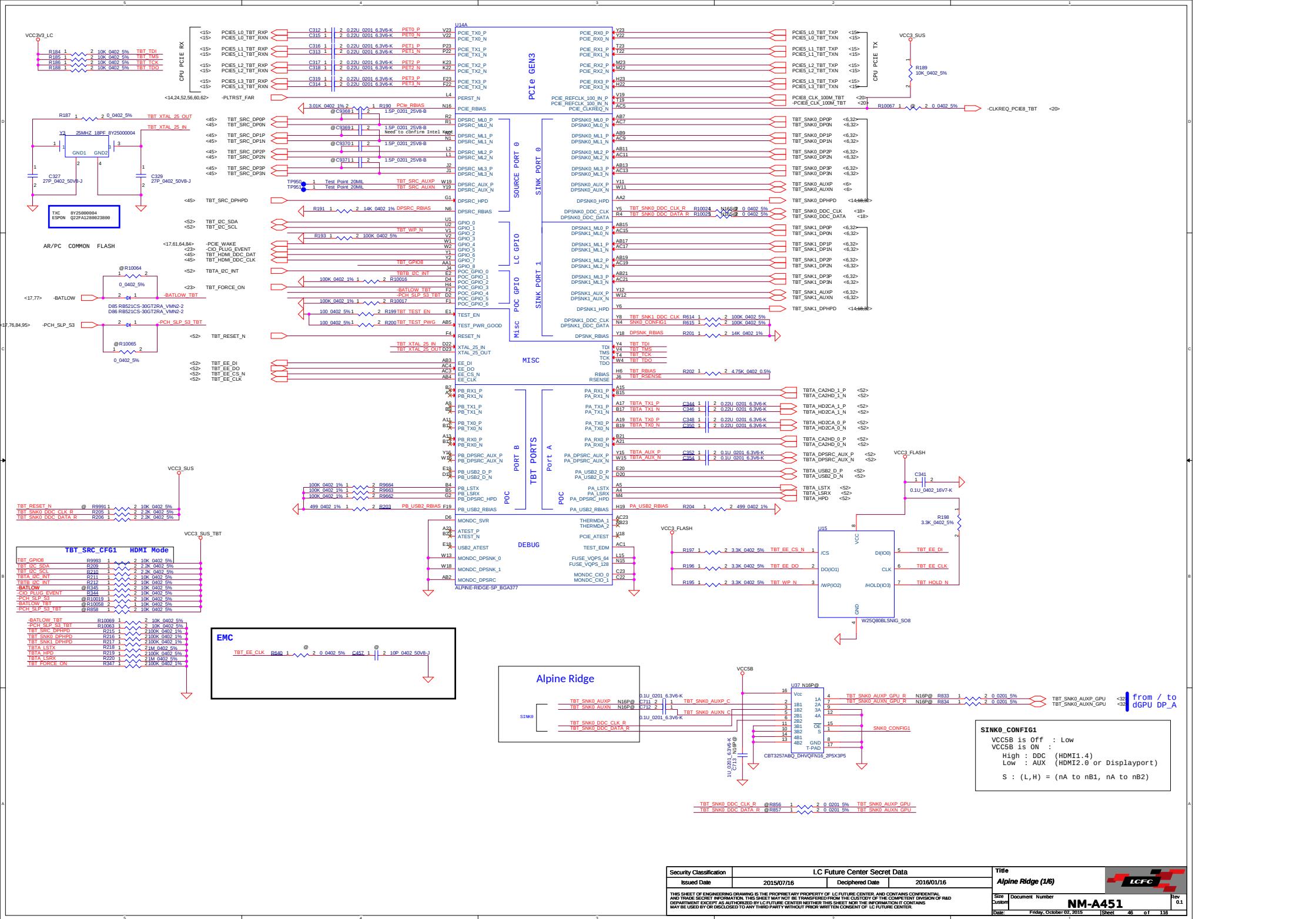


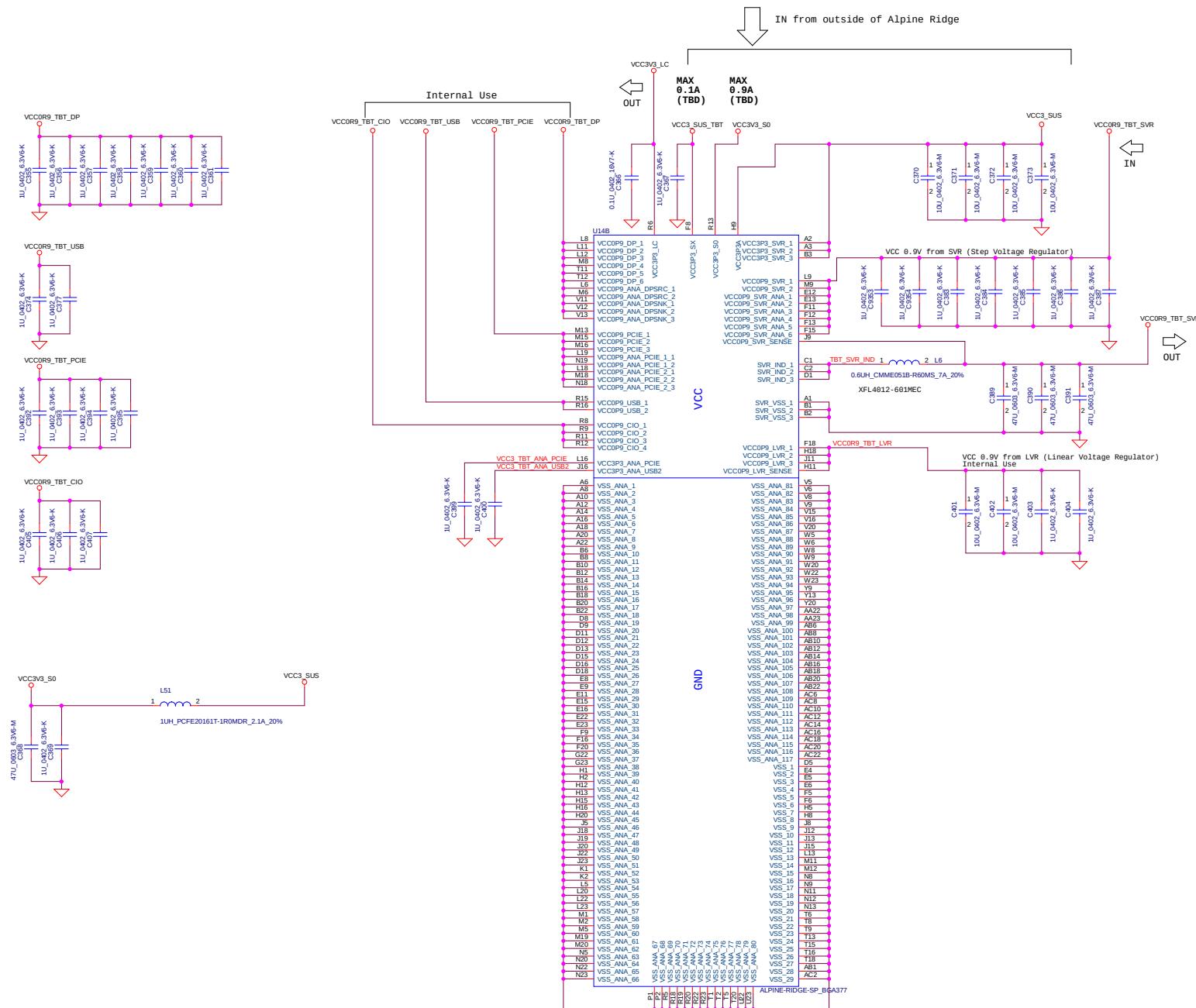
**DP CONN
5.4Gbps**





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Size Custom	Document Number NM-A451	Rev 0.1						
Date Friday, October 02, 2015	Sheet 48	of 116						

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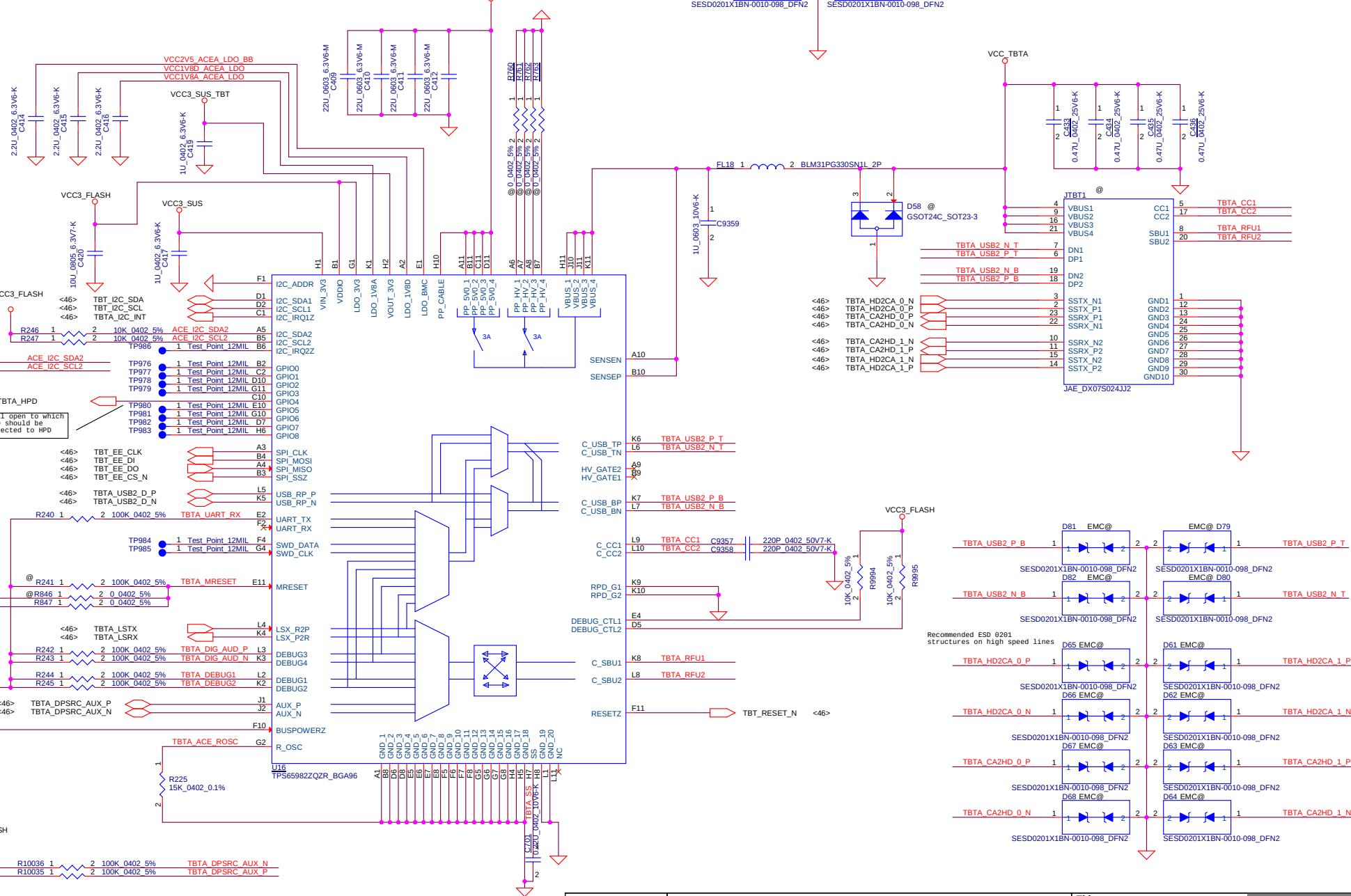
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Security Classification	Issued Date	Deciphered Date	2016/01/16	Alpine Ridge (4/6)	
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Security Classification

LC Future Center Secret Data

Title

Thunderbolt Power TPS65982/USB Type-C

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Document Number

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Date:

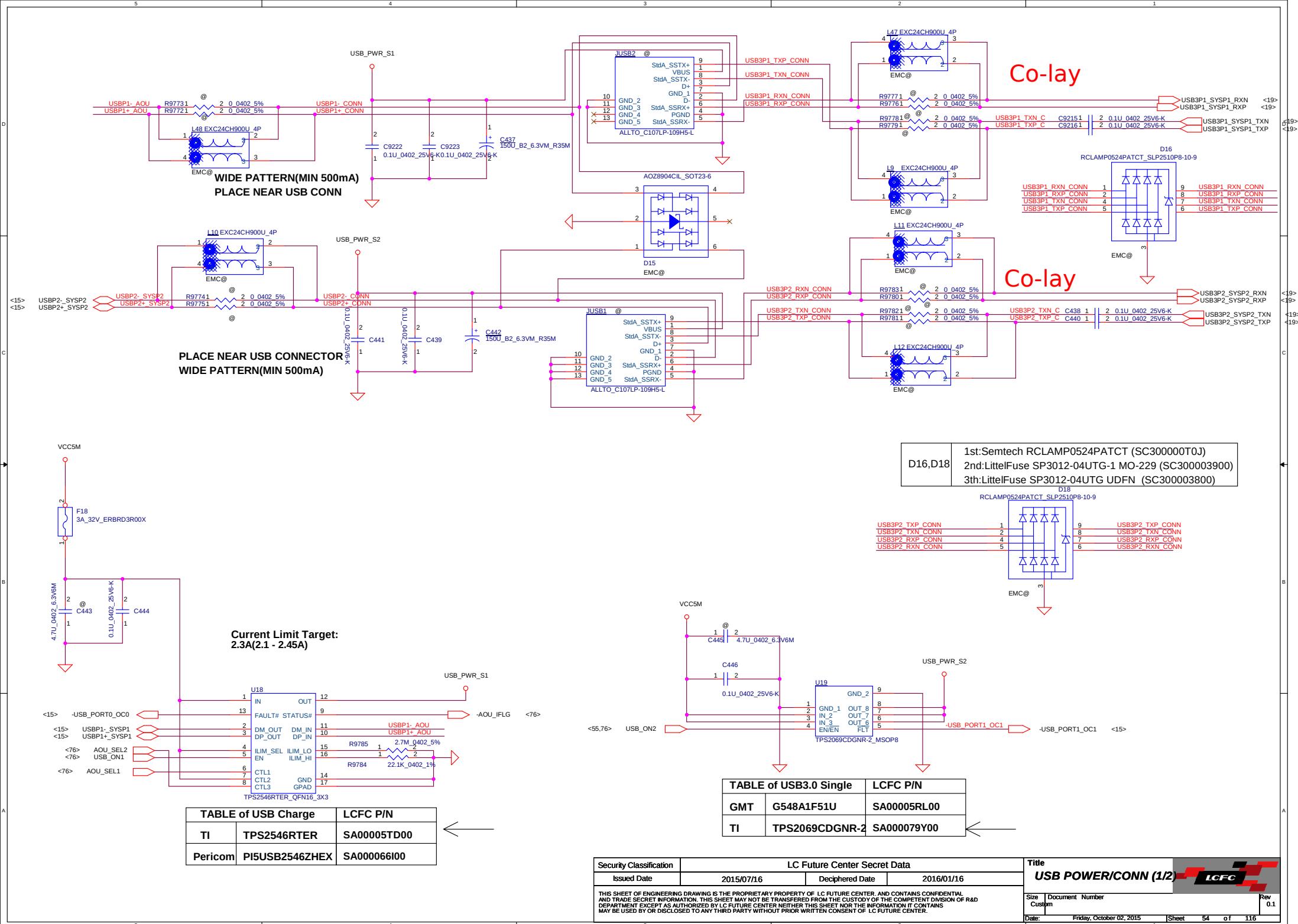
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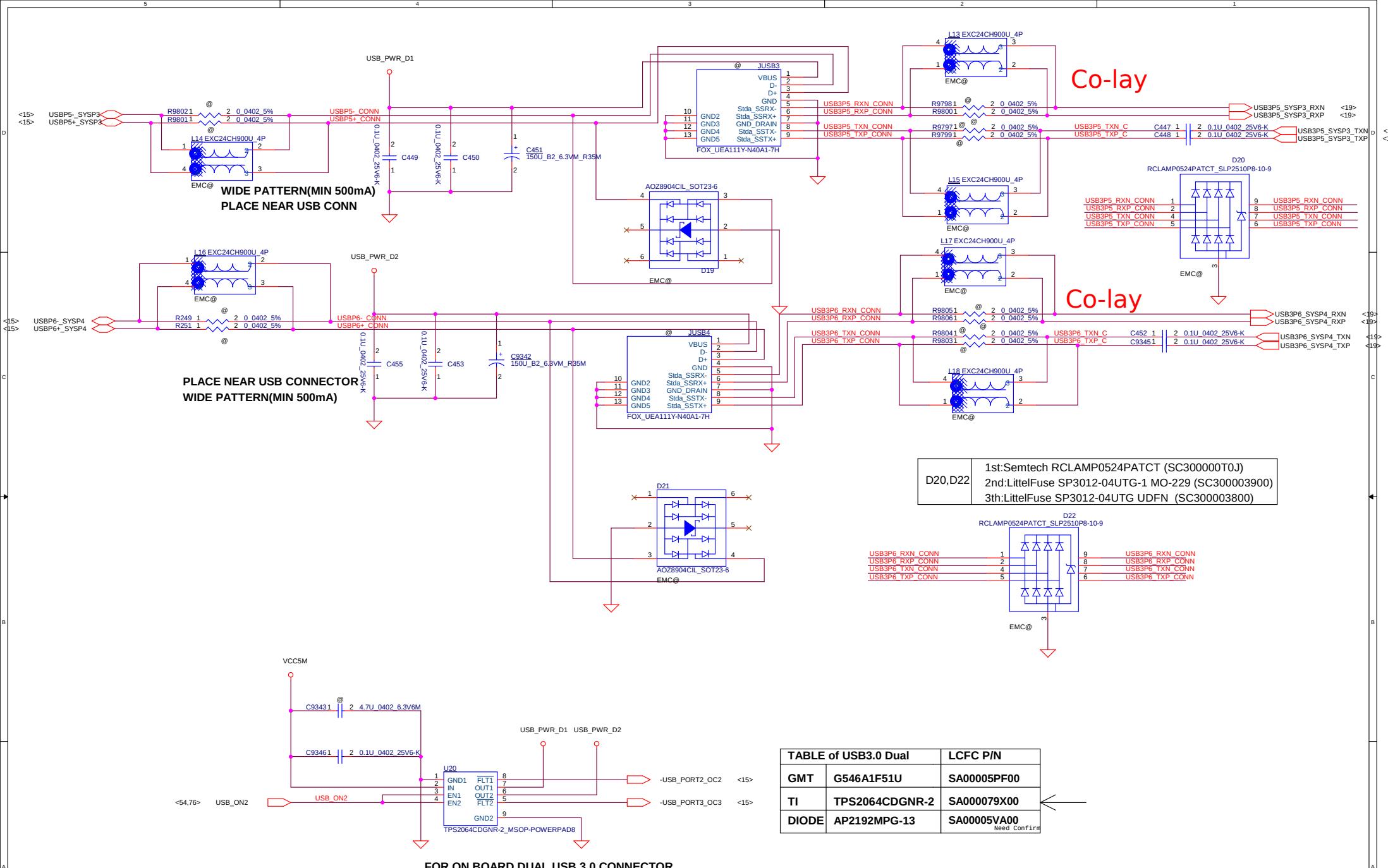
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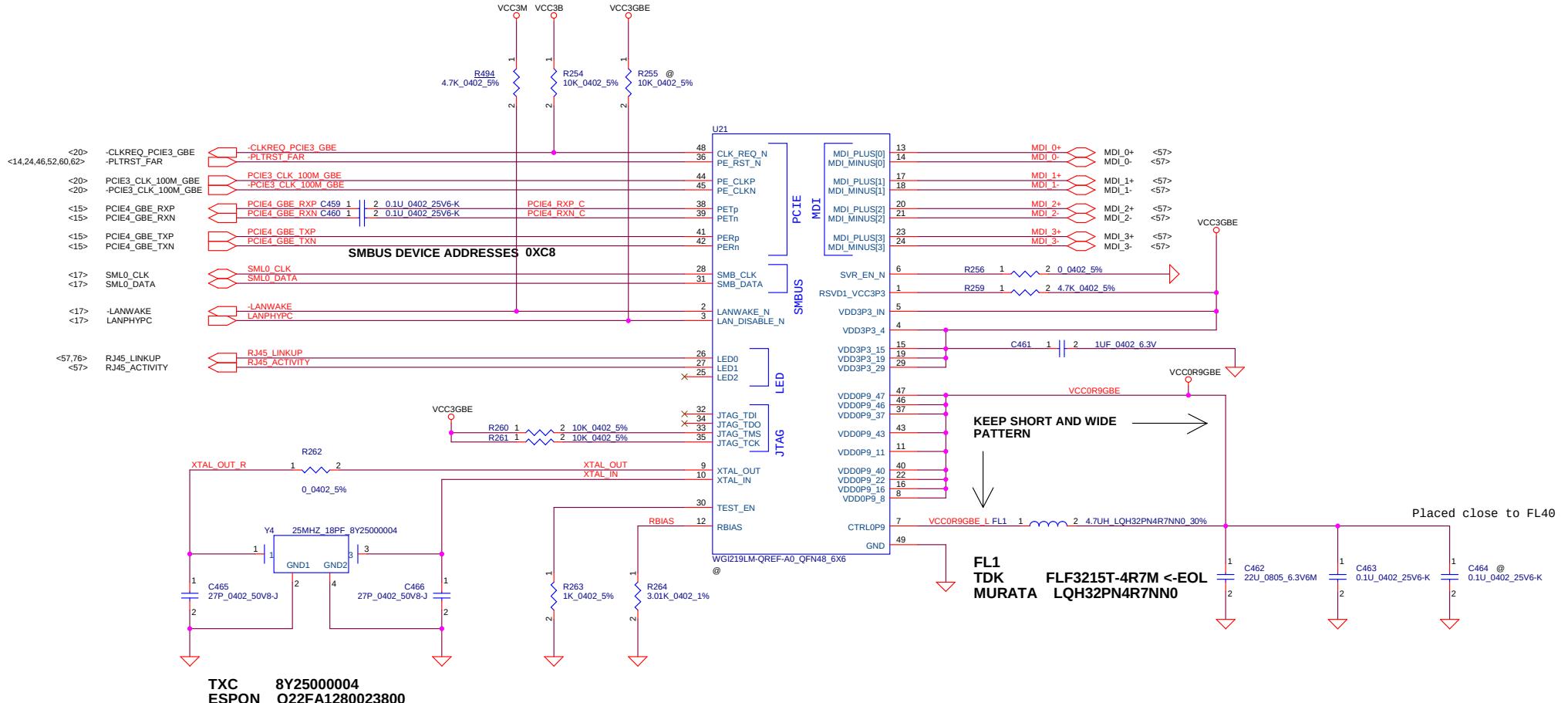
of 116

LC Future Center Secret Data				Title	
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				Custom	NM-A451
					Rev 0.1
				Date:	Friday, October 02, 2015
				Sheet:	53 of 116

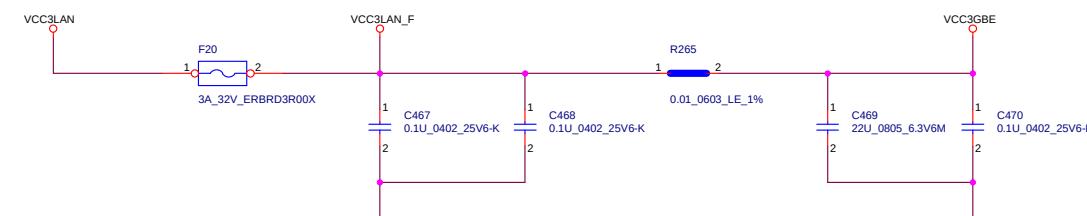




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Issued Date	2015/07/16	Deciphered Date	2016/01/16	USB POWER/CONN (2/2) LCFC
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Custom				



U21 GBE PHY	
vPRO Model	Non-vPRO Model
I219LM	I219V

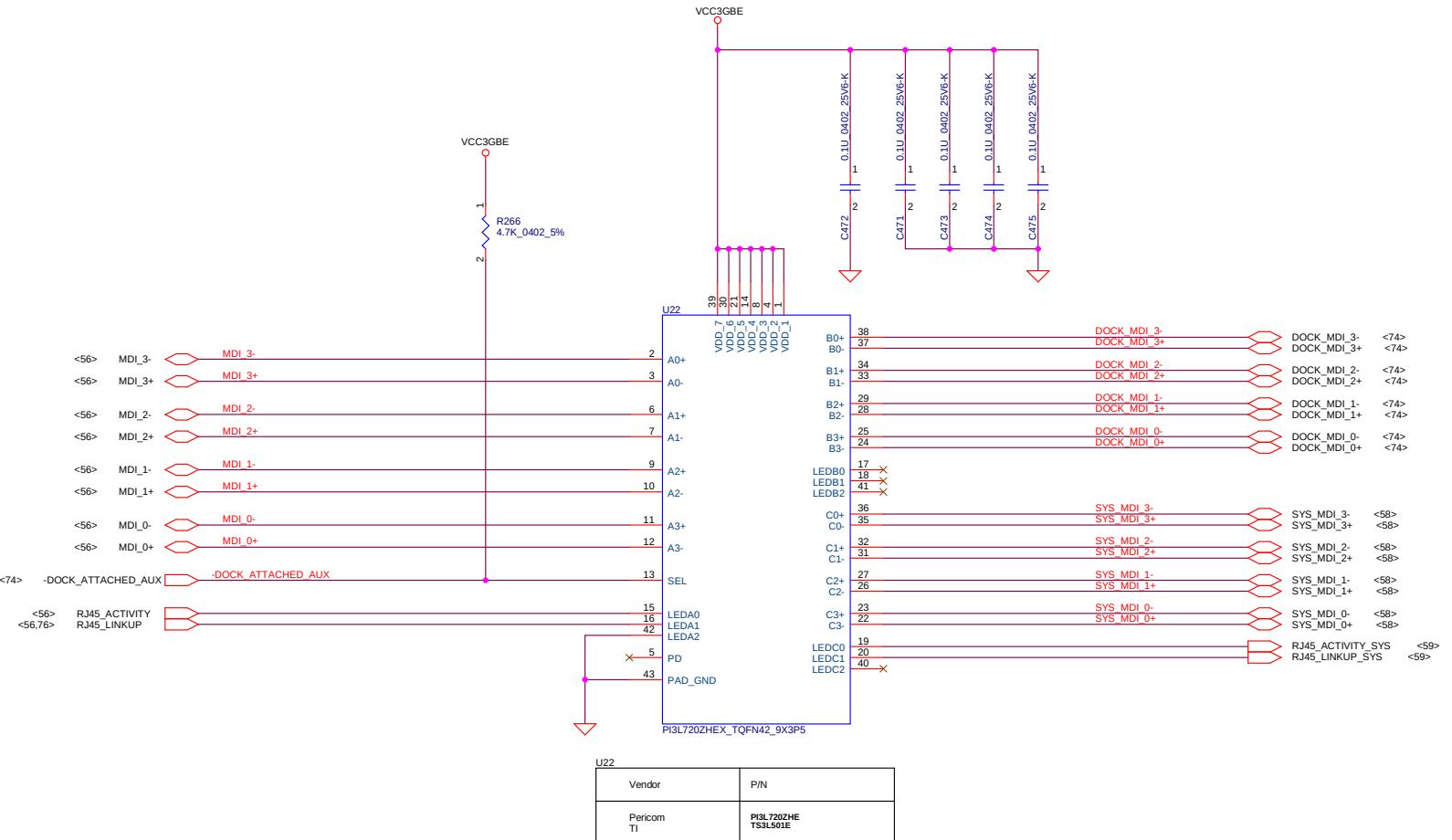


 U21	 U21
Intel Ethernet I219V	Intel Ethernet I219LM
SA000072Z10	SA000073020

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LC Future Center Secret Data

Title

GBE LAN SWITCH



Issued Date

2015/07/16

Deciphered Date

2016/01/16

Size

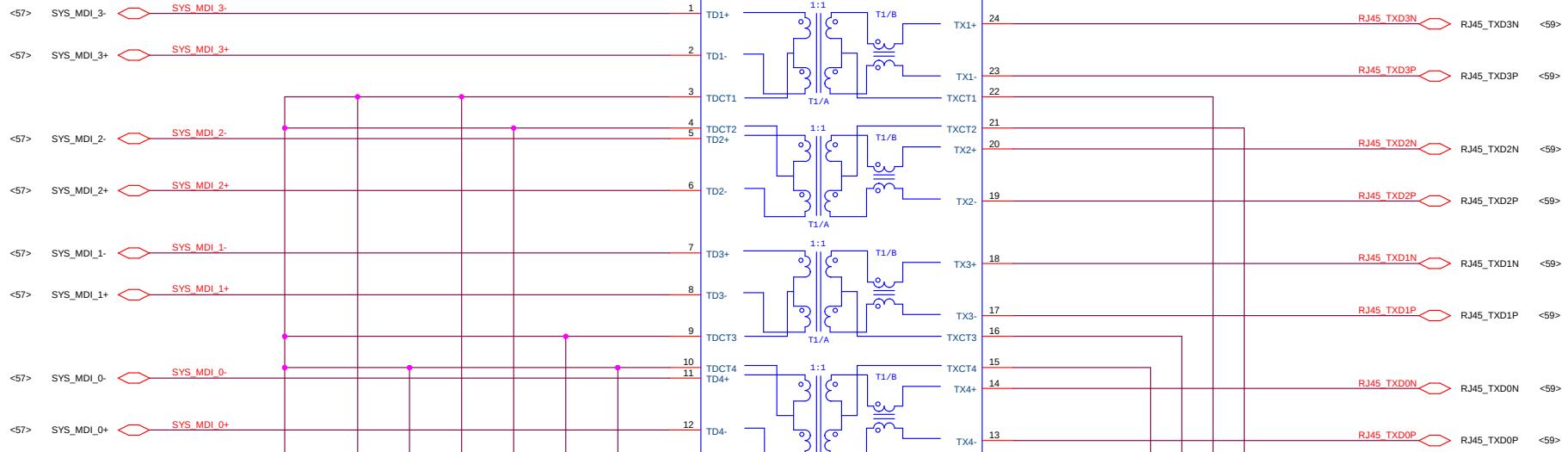
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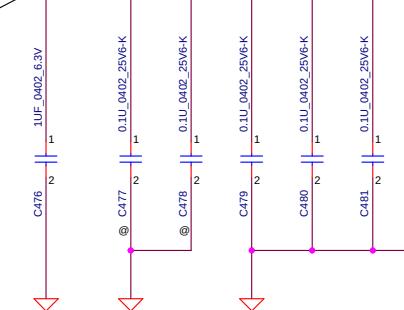
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C303
SHOULD BE PLACED AS CLOSE
TO MAGNETICS AS POSSIBLE.

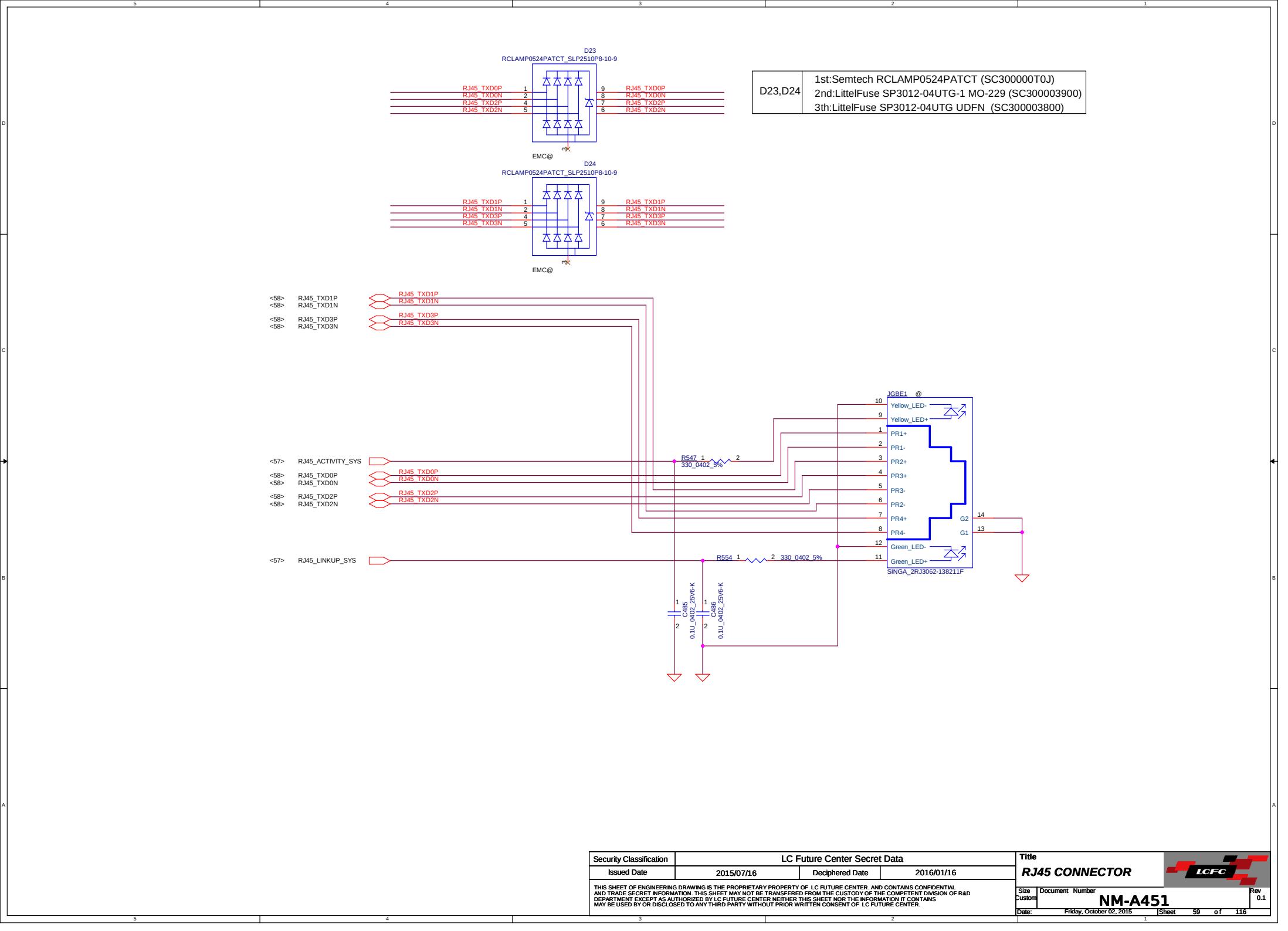


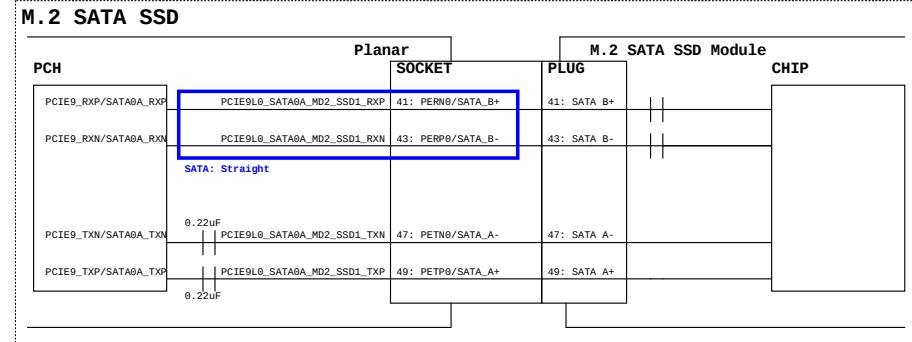
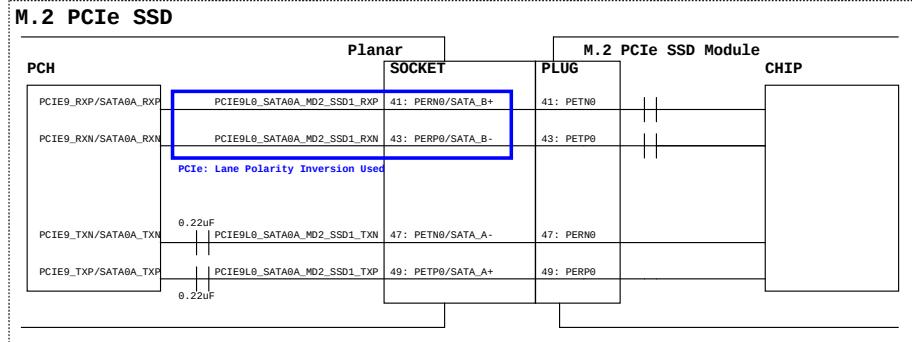
PATTERN MUST BE
SHORT AND WIDE.

HIGH VOLTAGE
1500PF CAP
IS OPTIONAL

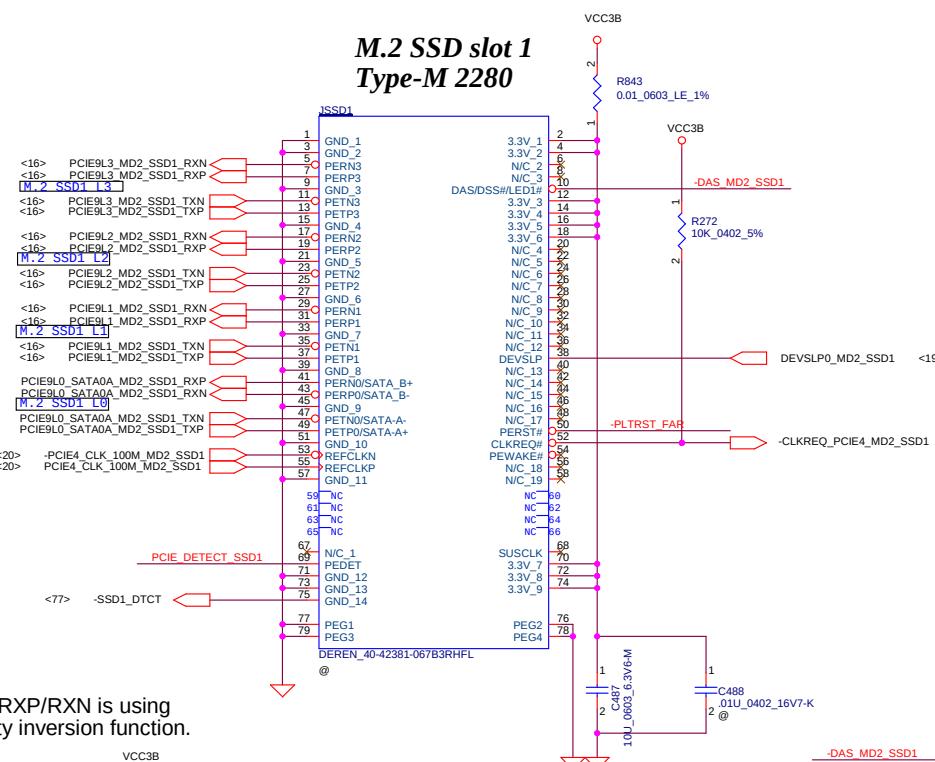
Vendor	P/N
Timag	IH-115-F
Bothhand	NA69LF

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M.2 SSD slot 1 Type-M 2280



PCIe RXP/RXN is using polarity inversion function.

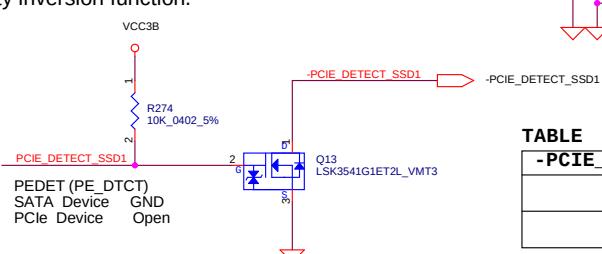


TABLE	
-PCIE_DETECT_SSD1	Device
High	SATA SSD
LOW	PCIe SSD

*M.2 SSD slot 2
Type-M 2280*

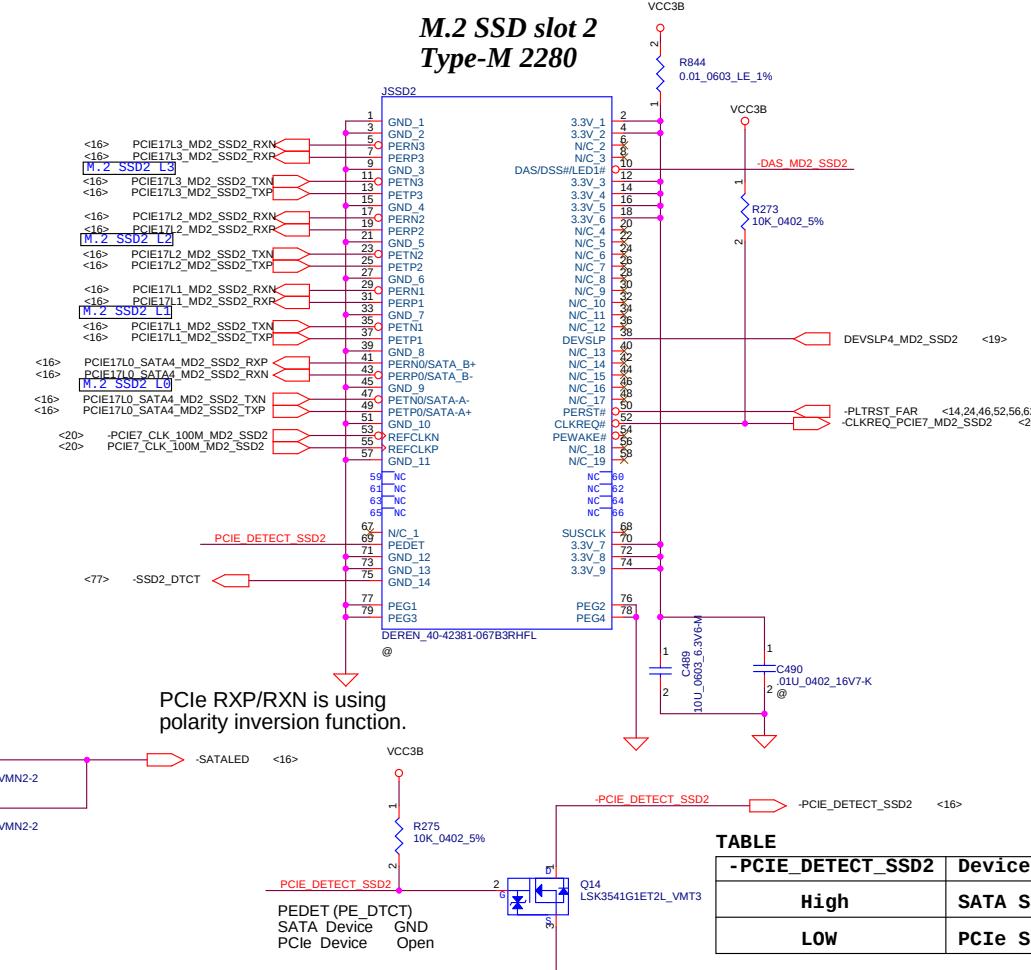
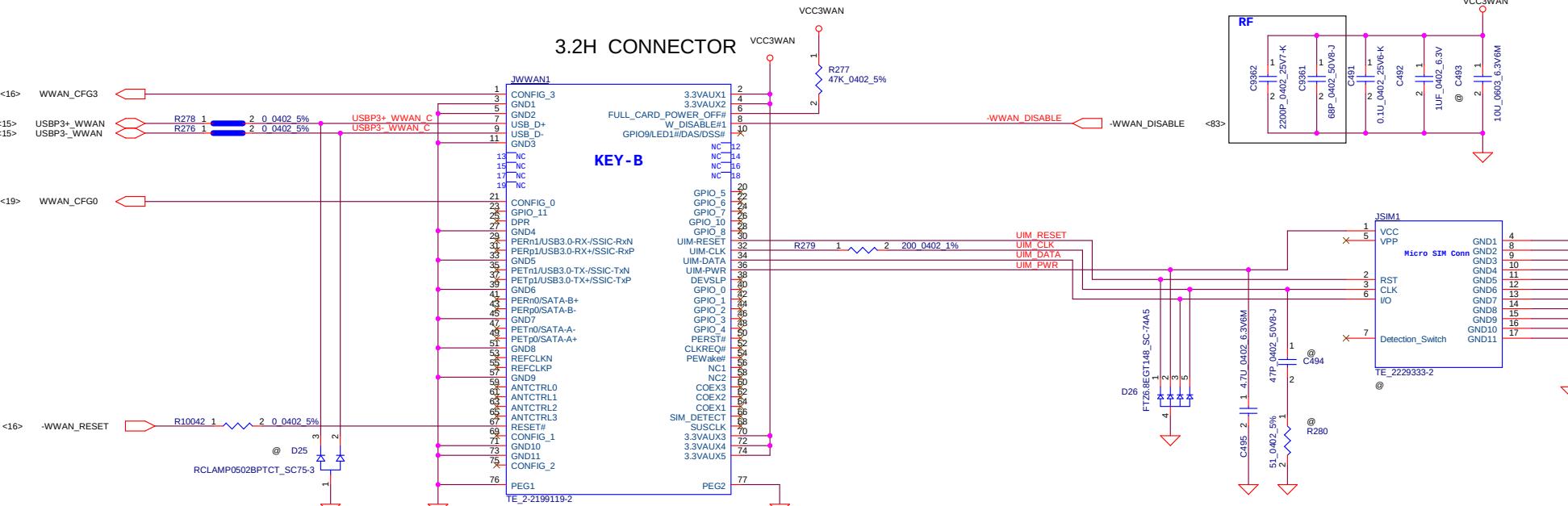
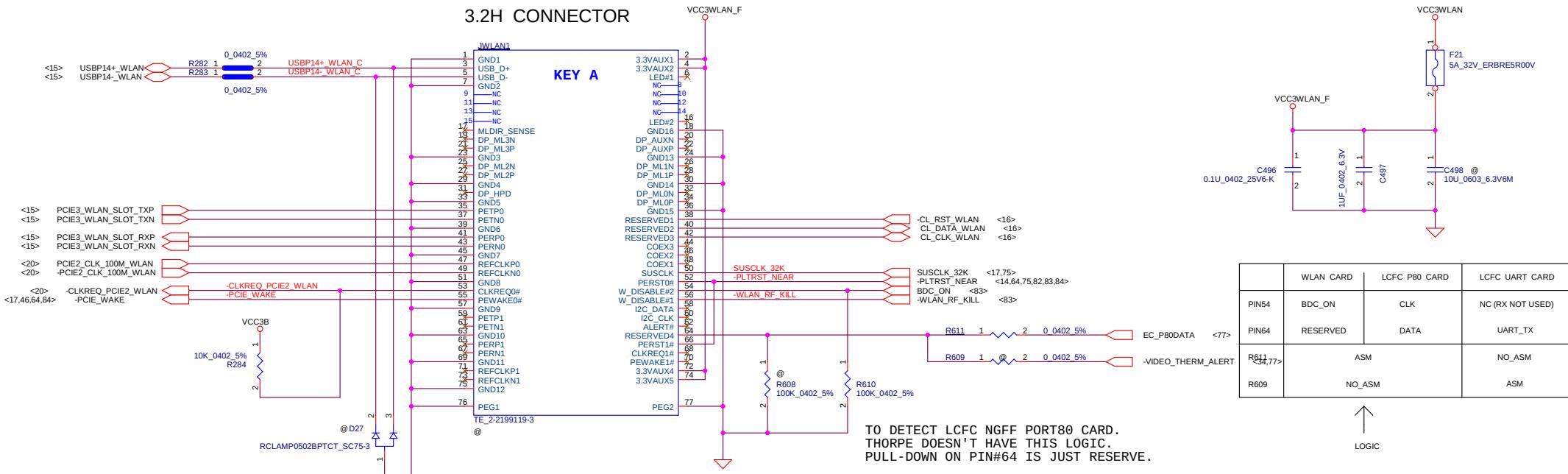


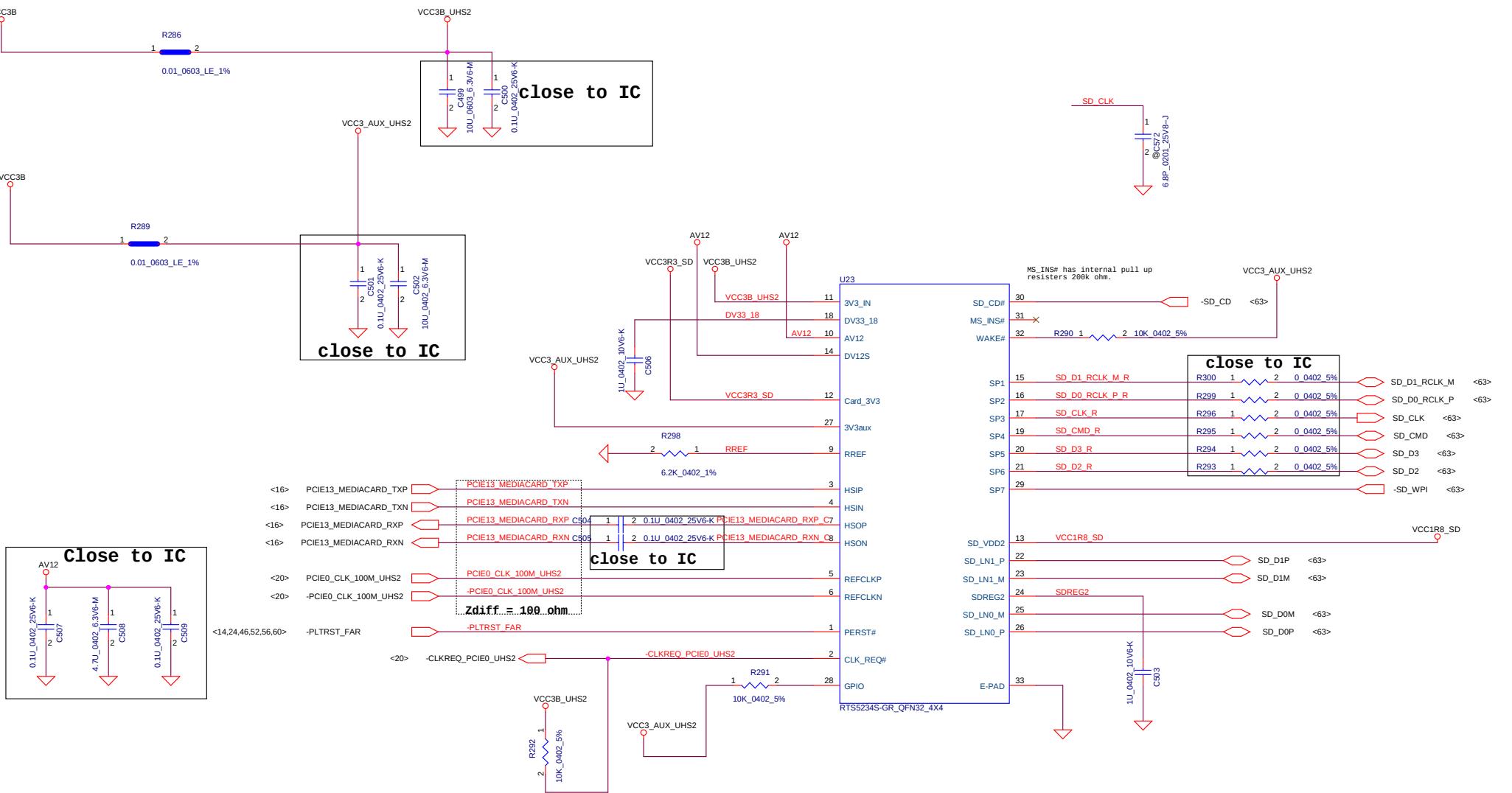
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-PCIE_DETECT_SSD2	Device	
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Low	PCIe SSD	

TYPE-B NGFF CCARD FOR WWAN

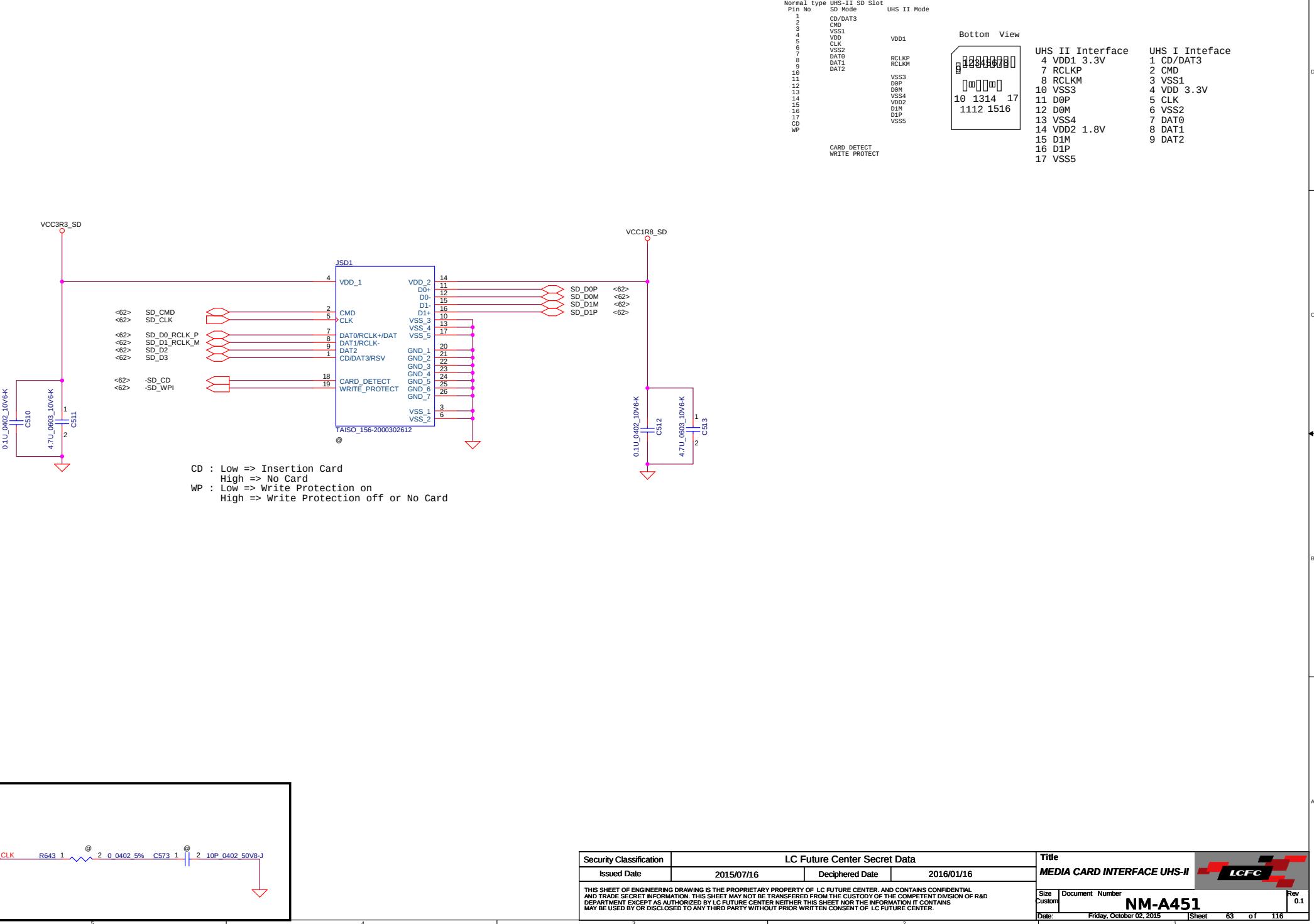


TYPE-A NGFF CCARD FOR WLAN

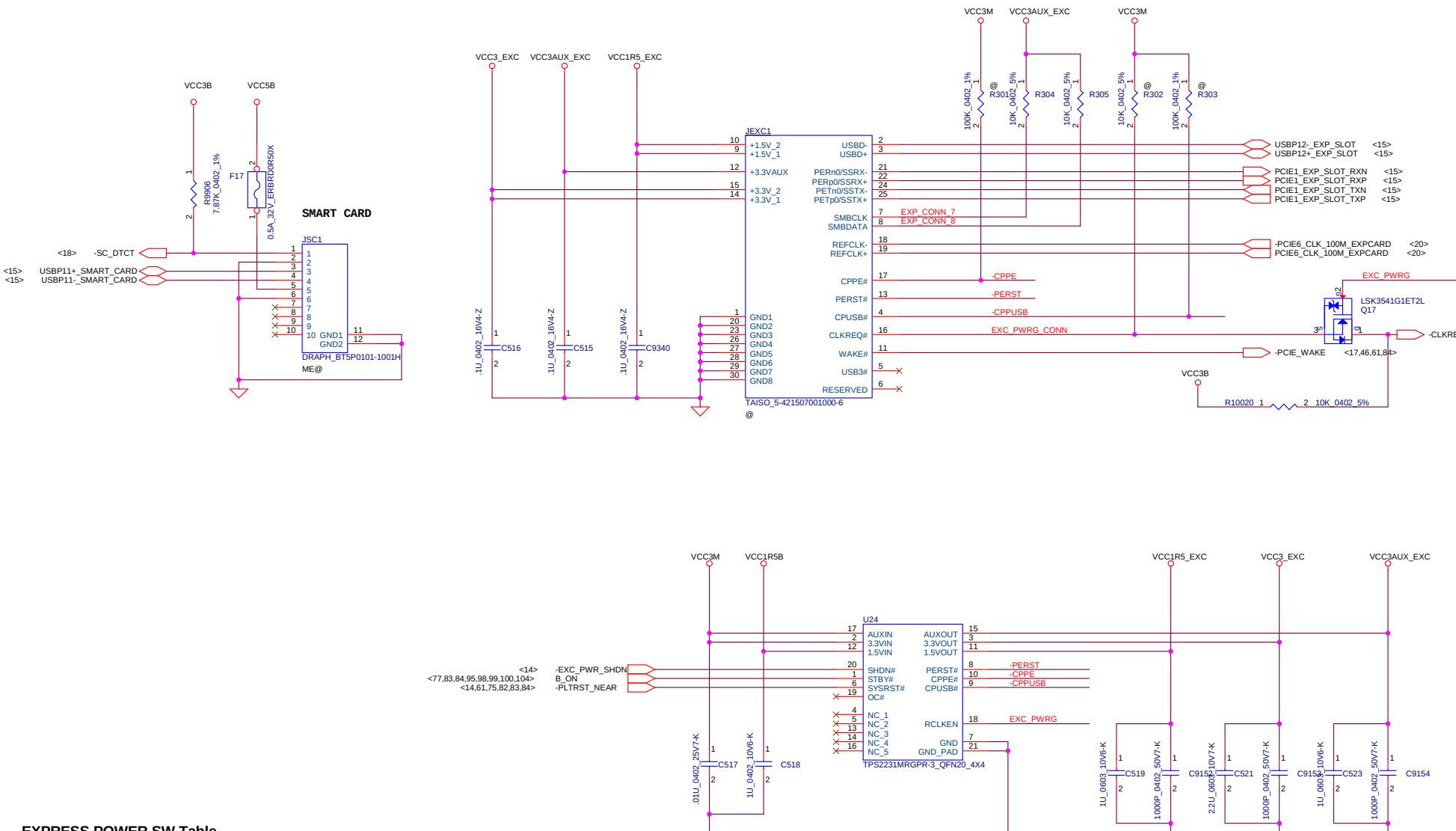




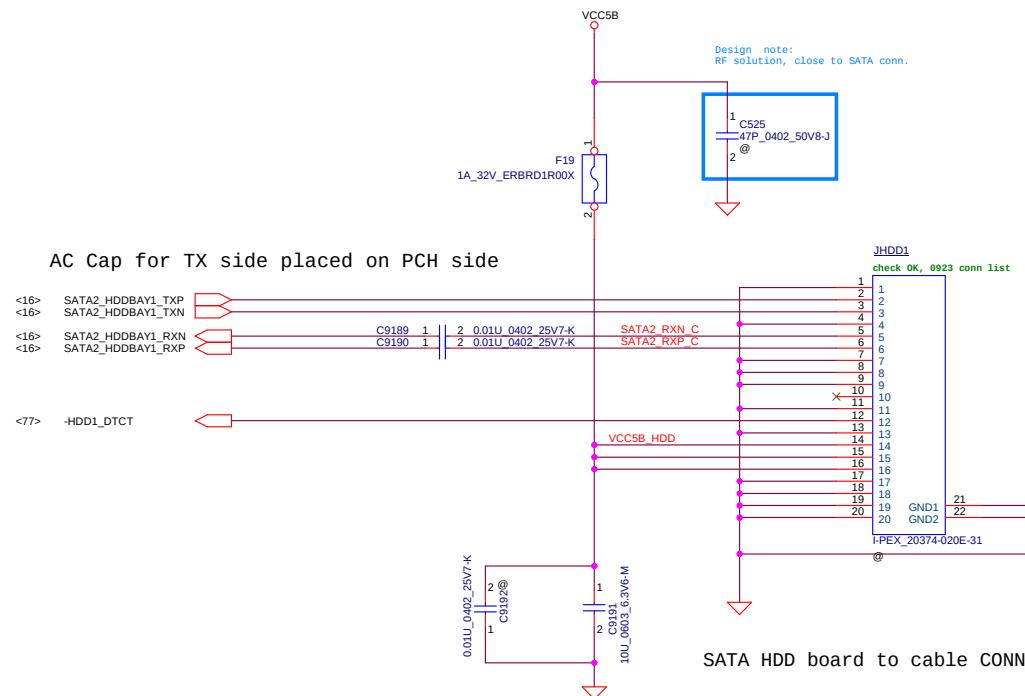
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3	2	1												



**EXC POWER IC has internal PU for
PIN#9(-CPUSB), PIN#10(-CPPE)**

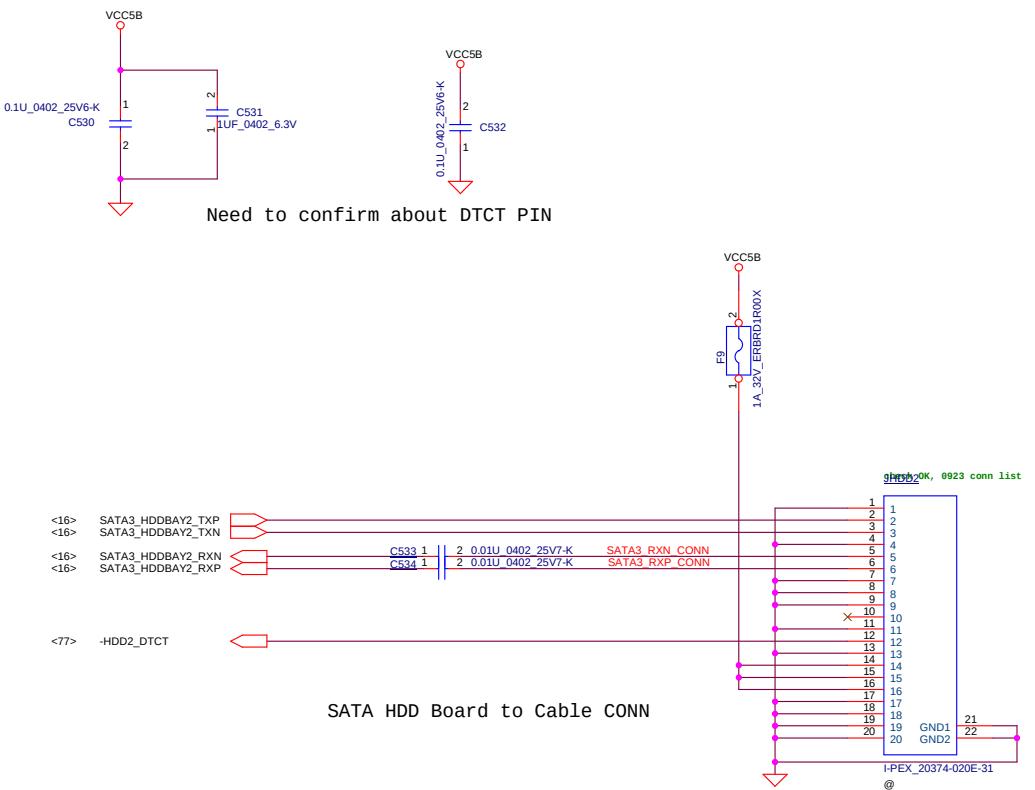


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Date: Friday, October 02, 2015	Sheet:	1	64	of 116

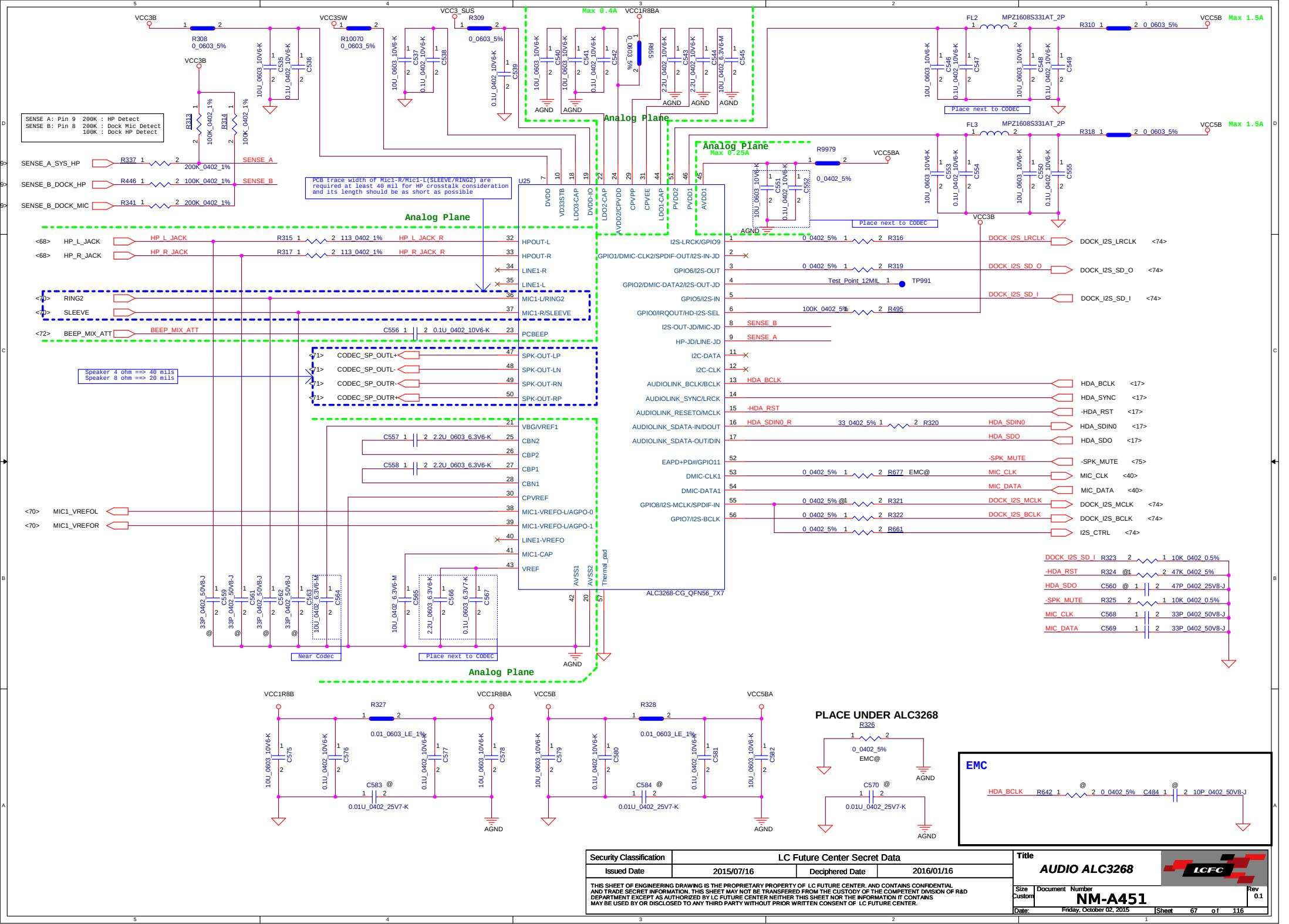


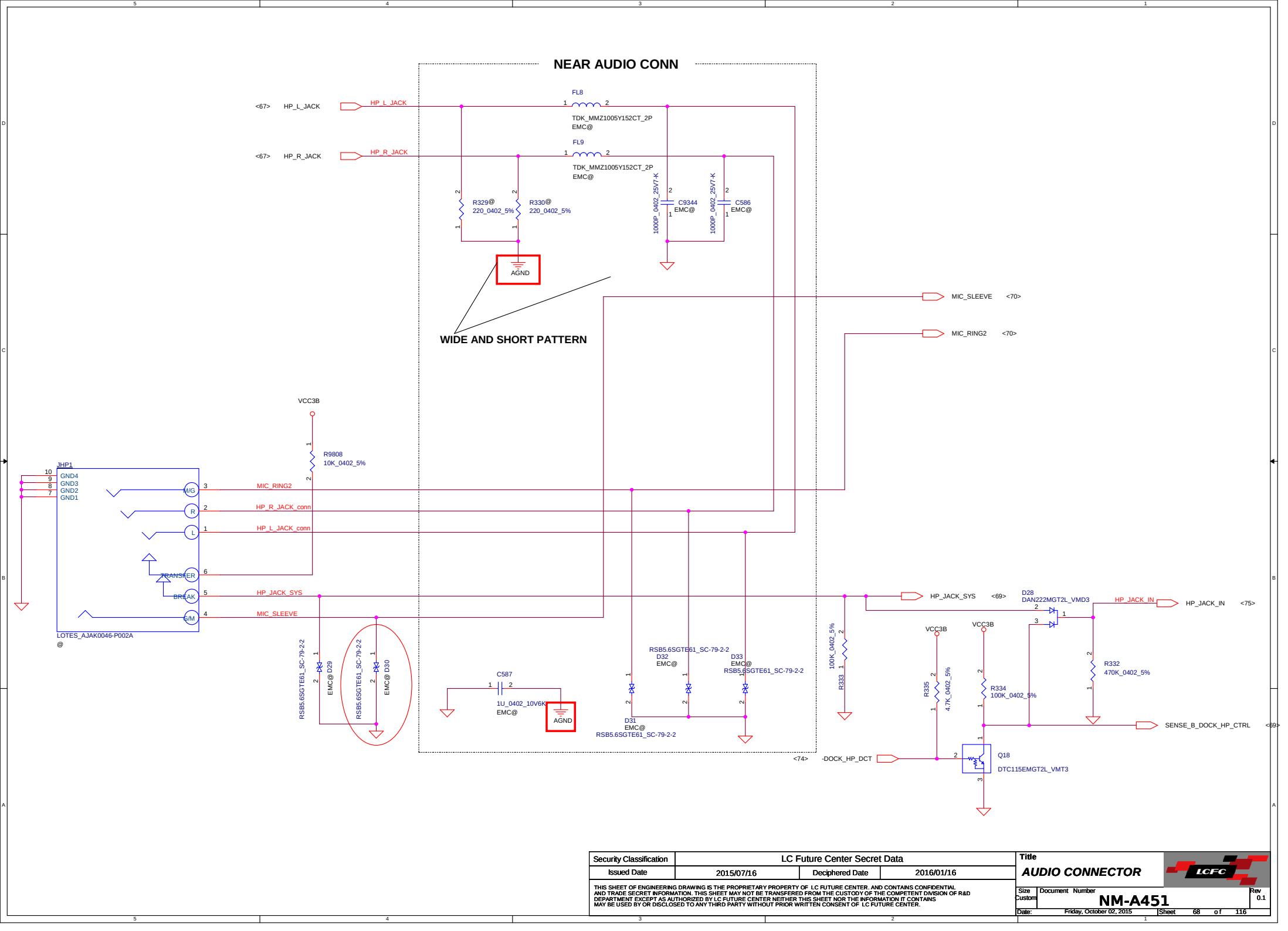
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Issued Date	2015/07/16	Deciphered Date	2016/01/16	SATA HDD CONN
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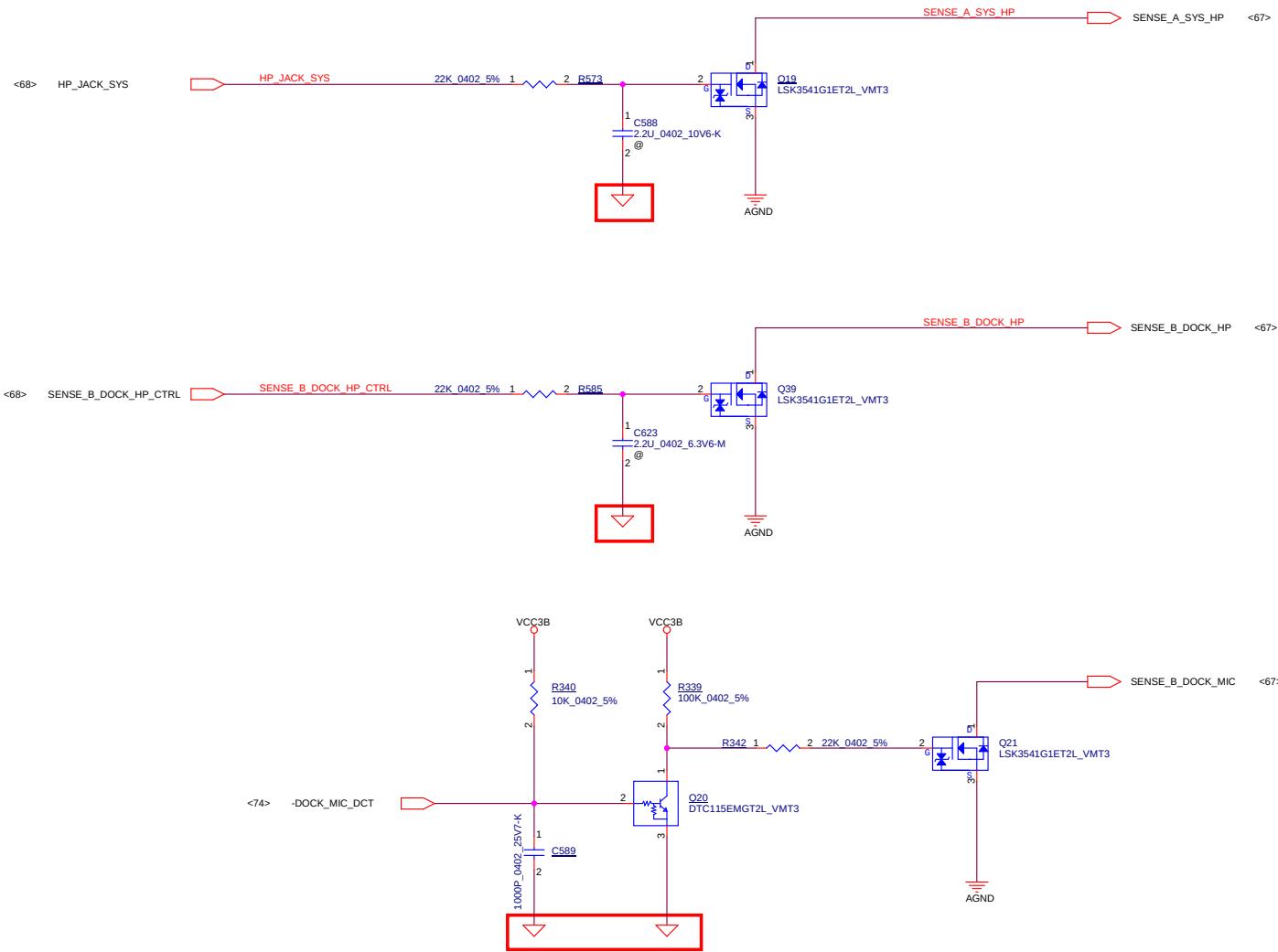
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Title

AUDIO JACK SENSE



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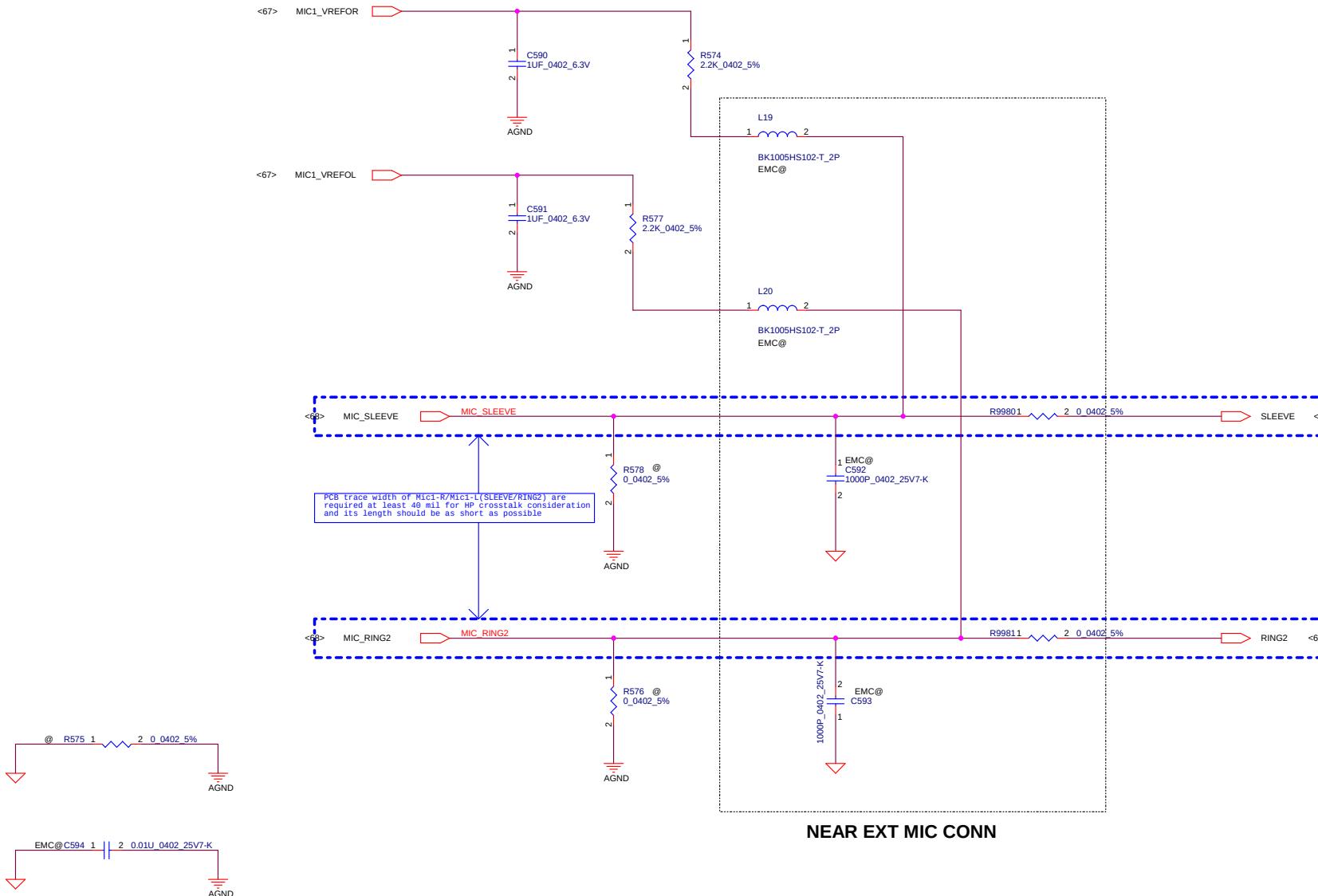
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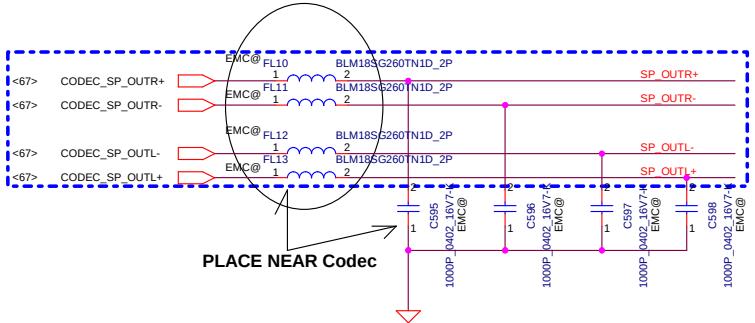
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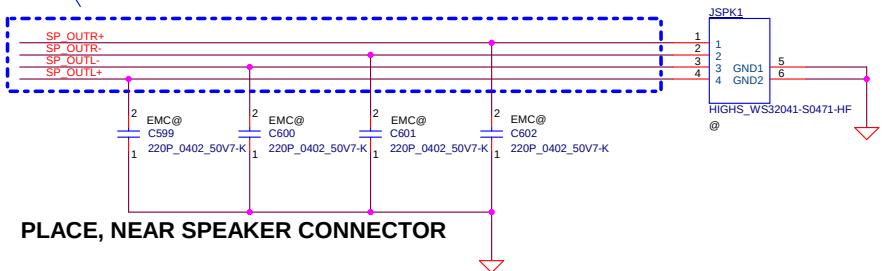
NEAR EXT MIC CONN

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Issued Date	2015/07/16	Deciphered Date	2016/01/16	AUDIO EXT MIC I/F	
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ALC3268 speaker output part

Speaker 4 ohm ==> 40 mils
Speaker 8 ohm ==> 26 mils



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2016/01/16

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Title

AUDIO SPEAKER



Size

Custom

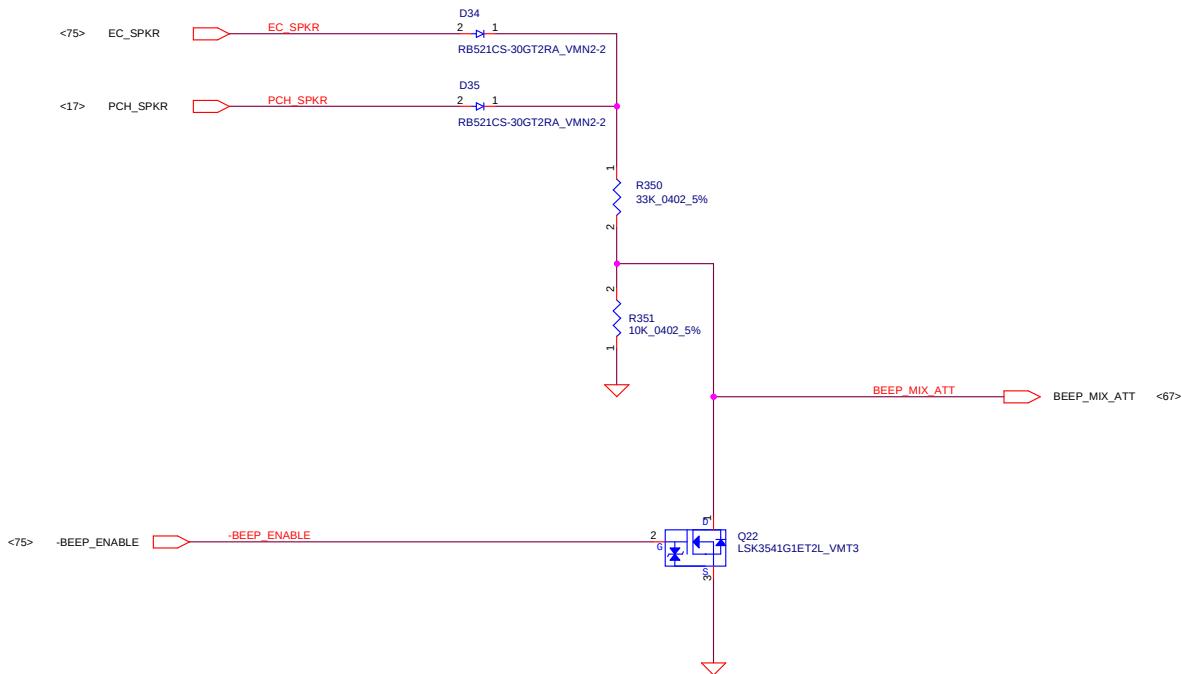
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NM-A451

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0.1

Date: Friday, October 02, 2015 Sheet 1 of 116



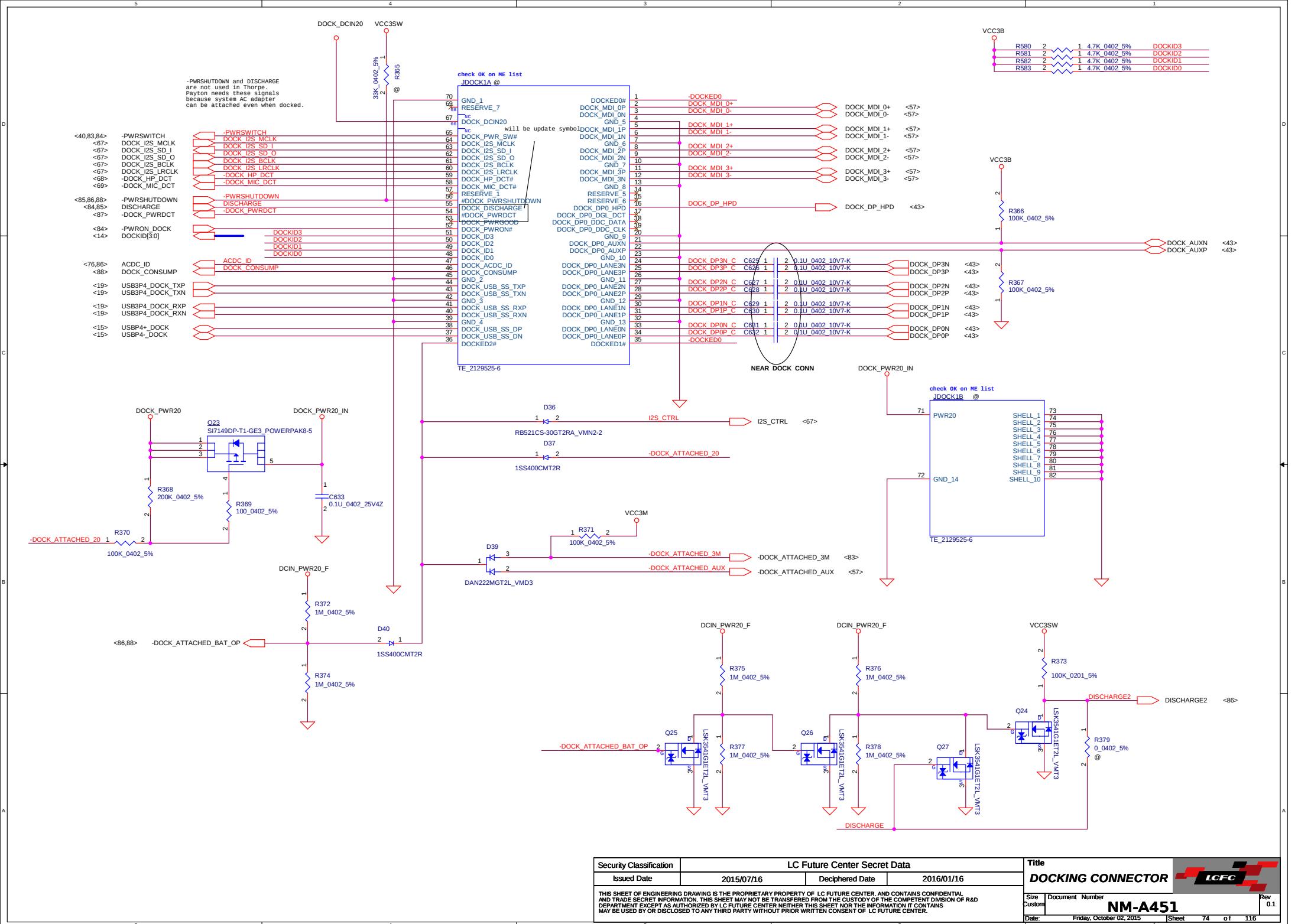
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Issued Date	2015/07/16	Deciphered Date	2016/01/16

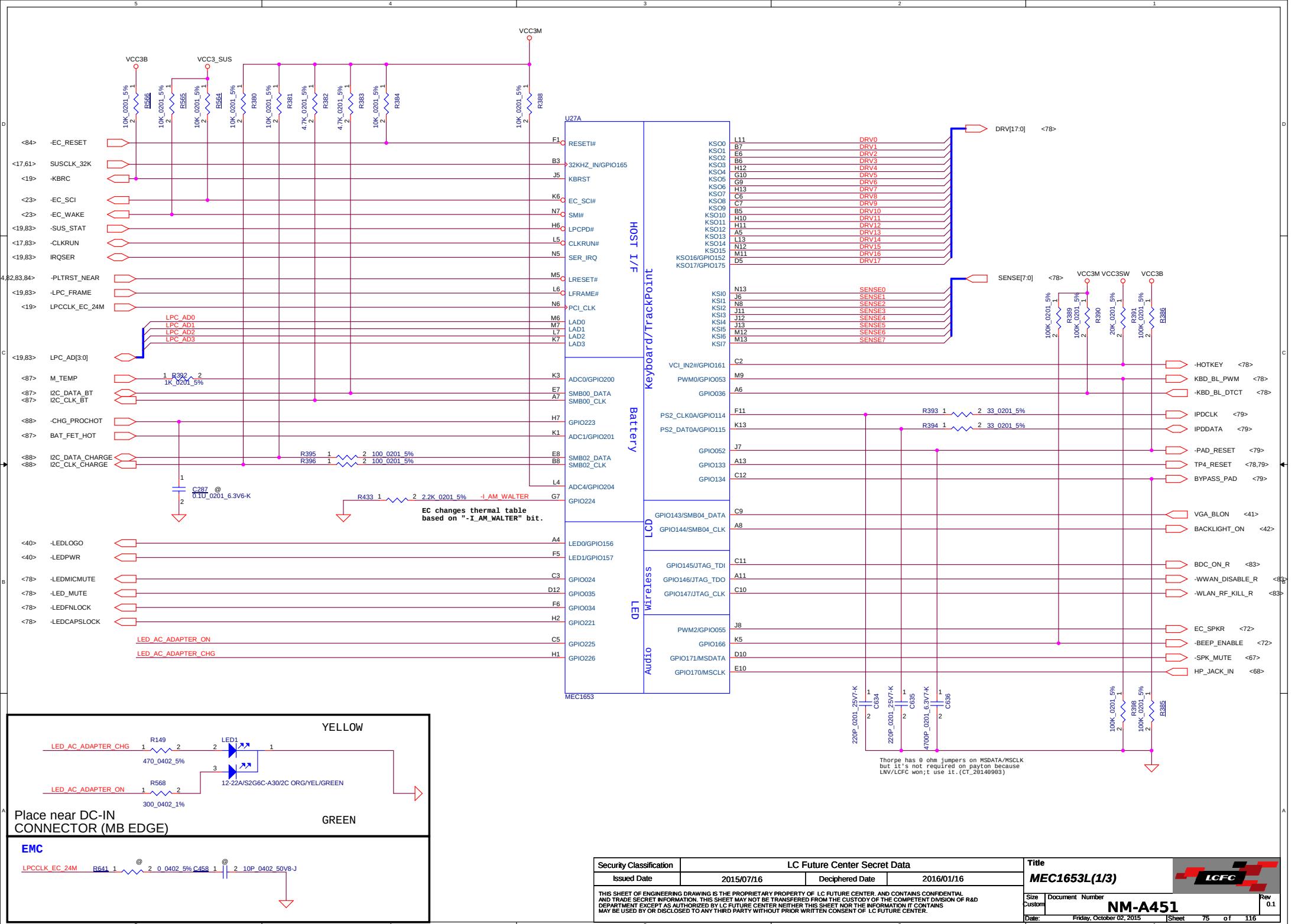
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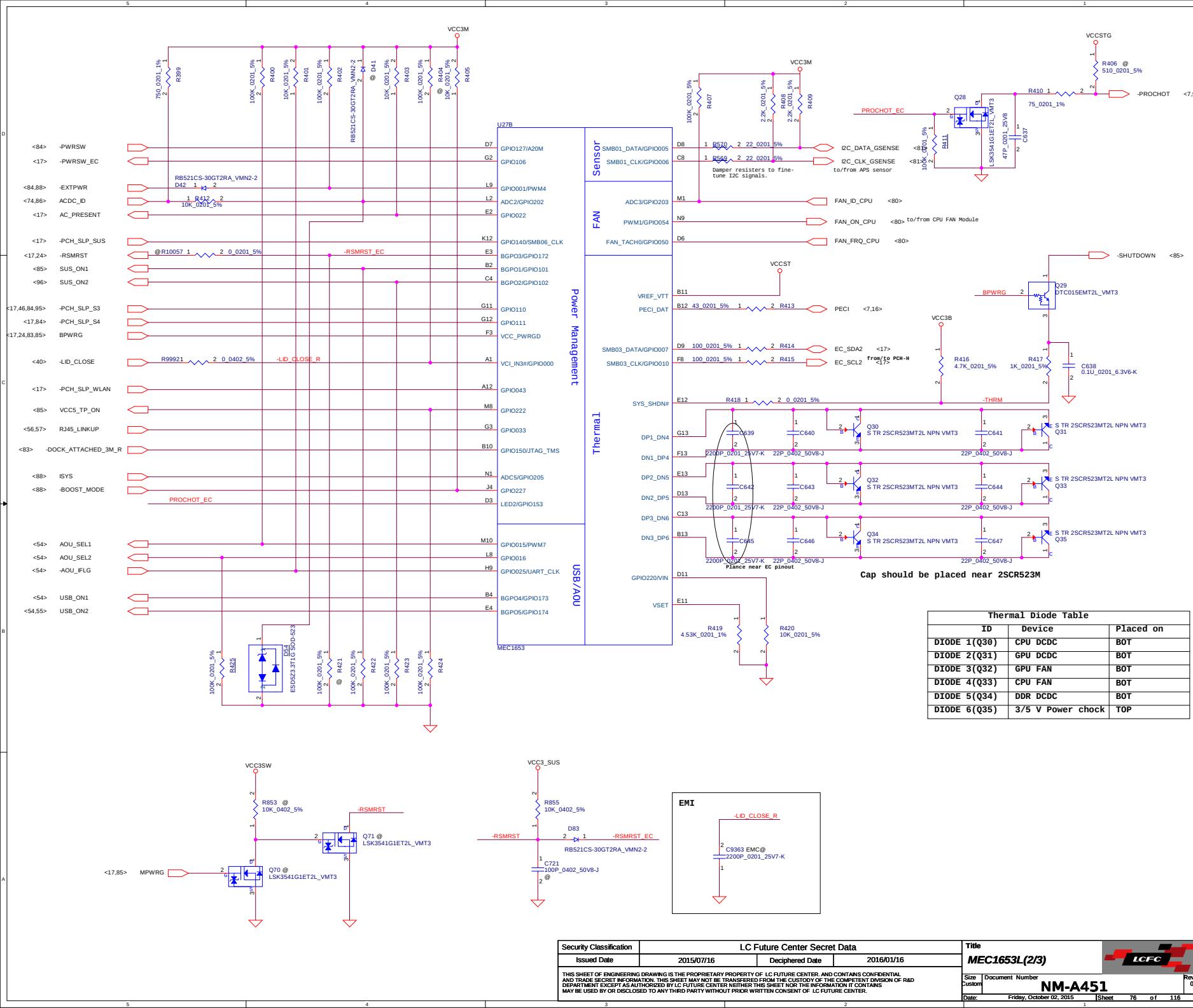
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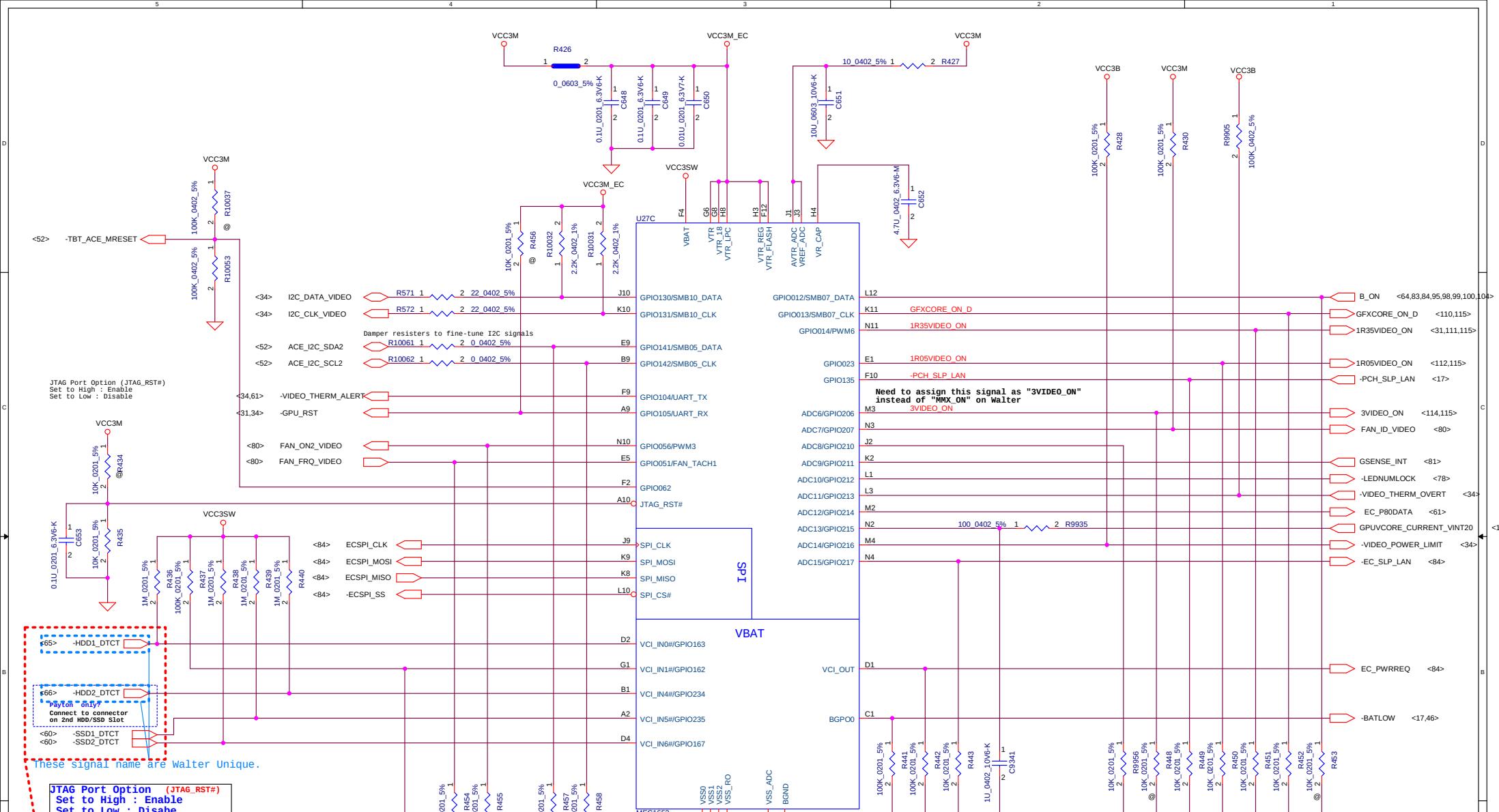
Size Custom	Document Number	NM-A451	Rev 0.1
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LC Future Center Secret Data				Title		
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These are device tamper detection pins. If storage is detached, BIOS will not automatically send password to storage.

INTRUDER pin has two function.

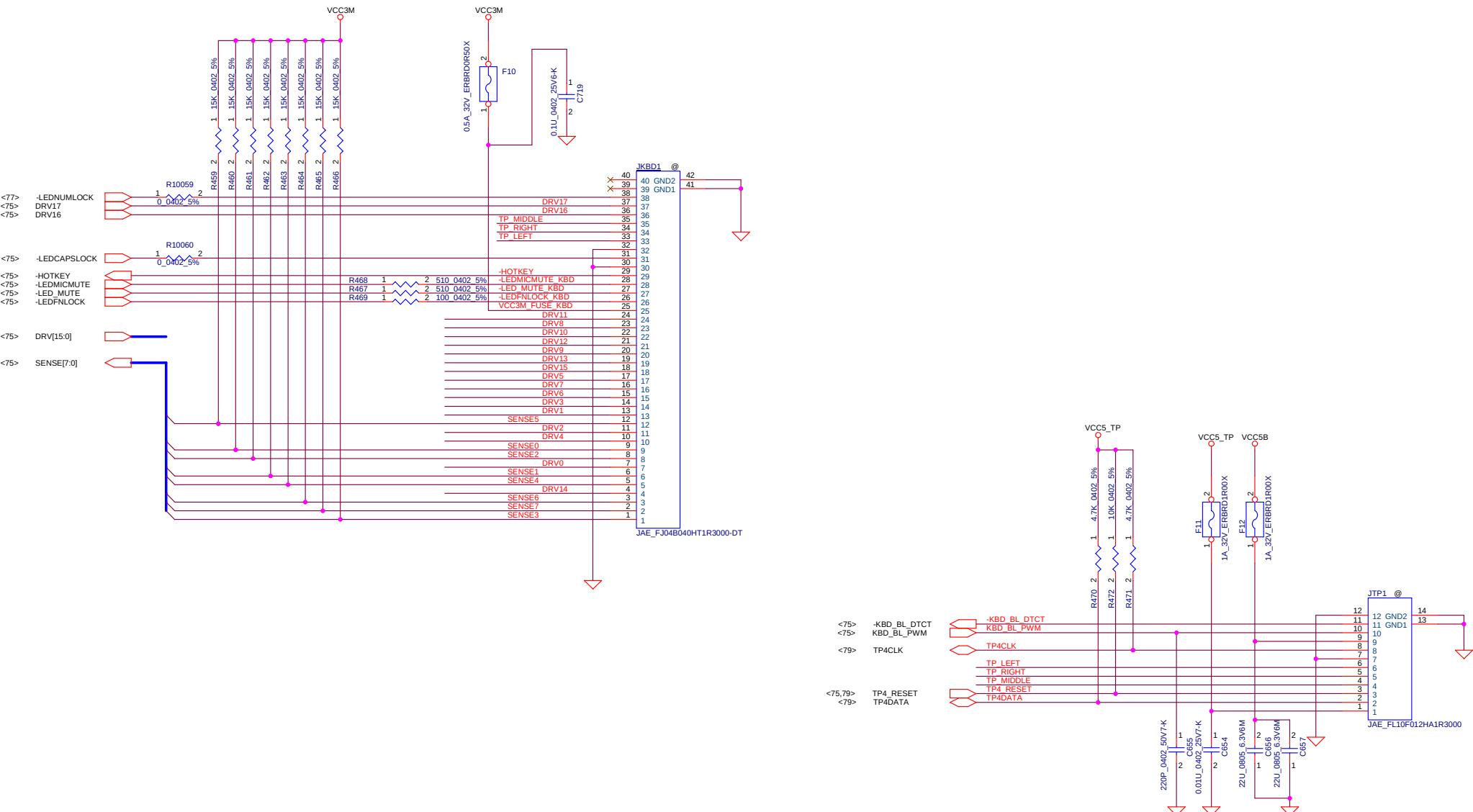
- (1) **FAST POST**
BIOS will skip device test in POST if door is not opened.
- (2) **SAFE BOTTOM ACCESS**
EC will turn off power of devices if door is opened to be safe.

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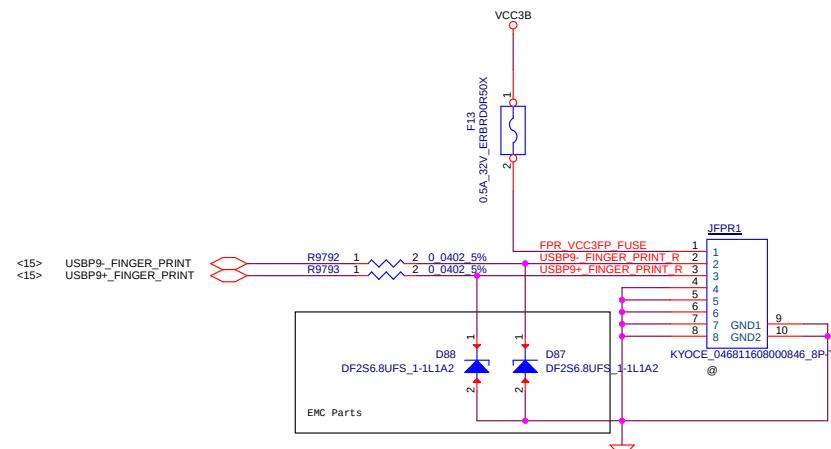
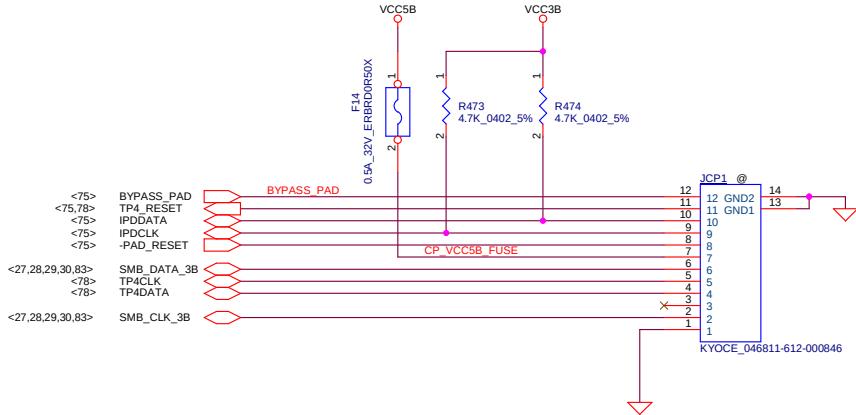
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Size Document Number **Rev**
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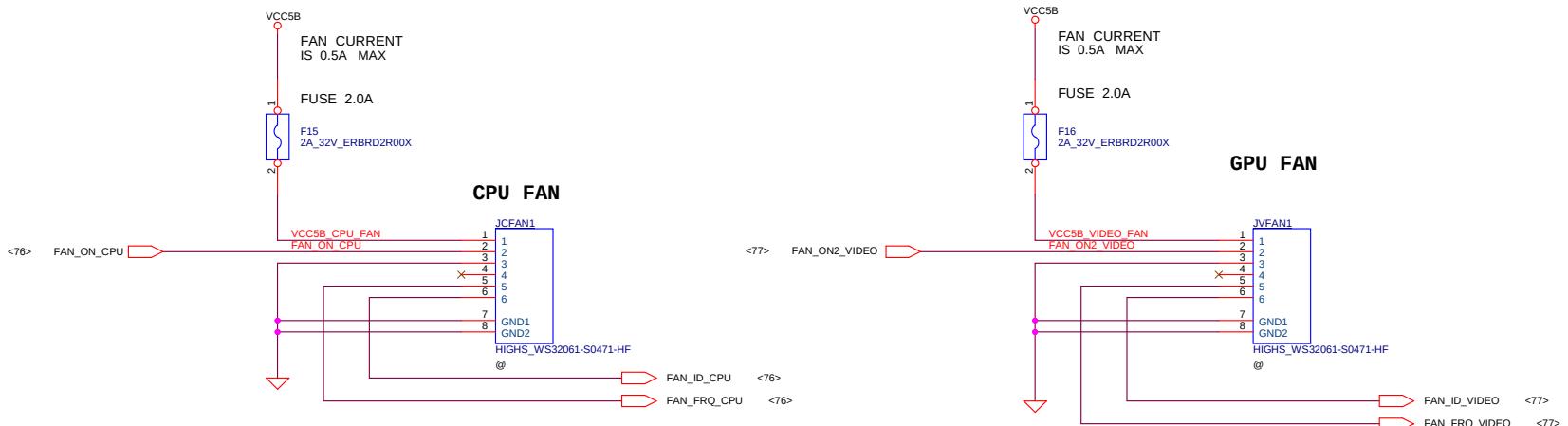


Need confirm 5BCP conn
and change to symbol

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Issued Date	2015/07/16			KEYBOARD CONNECTOR				
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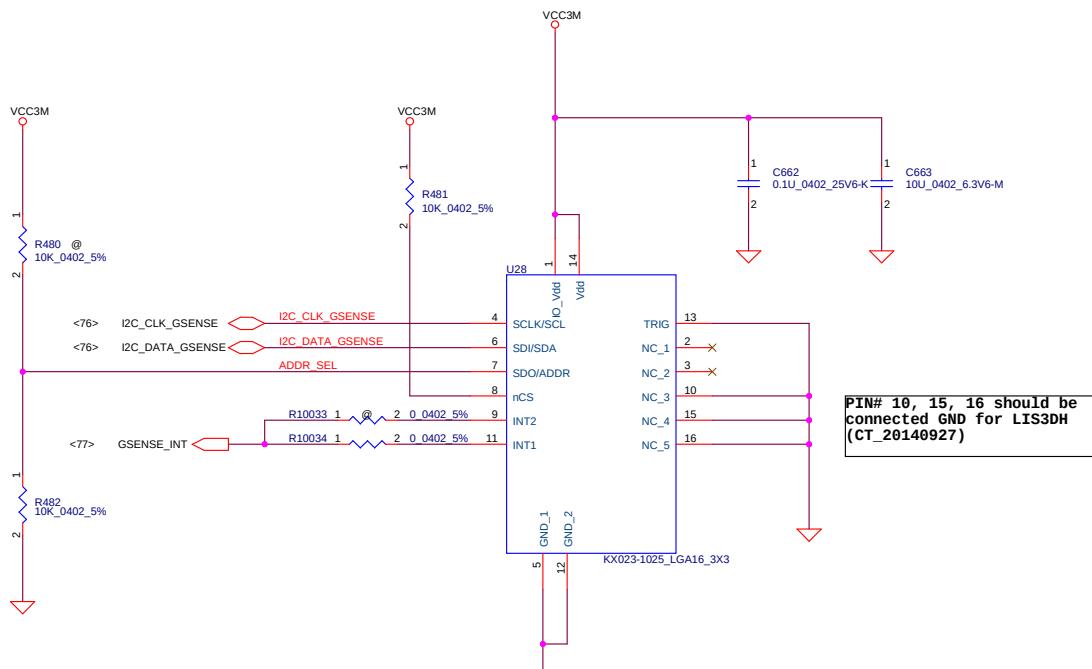
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TABLE

P/N	ADDR_SEL	Address
LIS3DH	H L	32h (W) & 33h (R) 30h (W) & 31h (R)
KX023-1025	H L	3Eh (W) & 3Fh (R) 3Ch (W) & 3Dh (R)

TABLE

CS	Mode Selection
H	I2C Mode
L	SPI Mode



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2015/07/16

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Deciphered Date

2016/01/16

Title

G-SENSOR



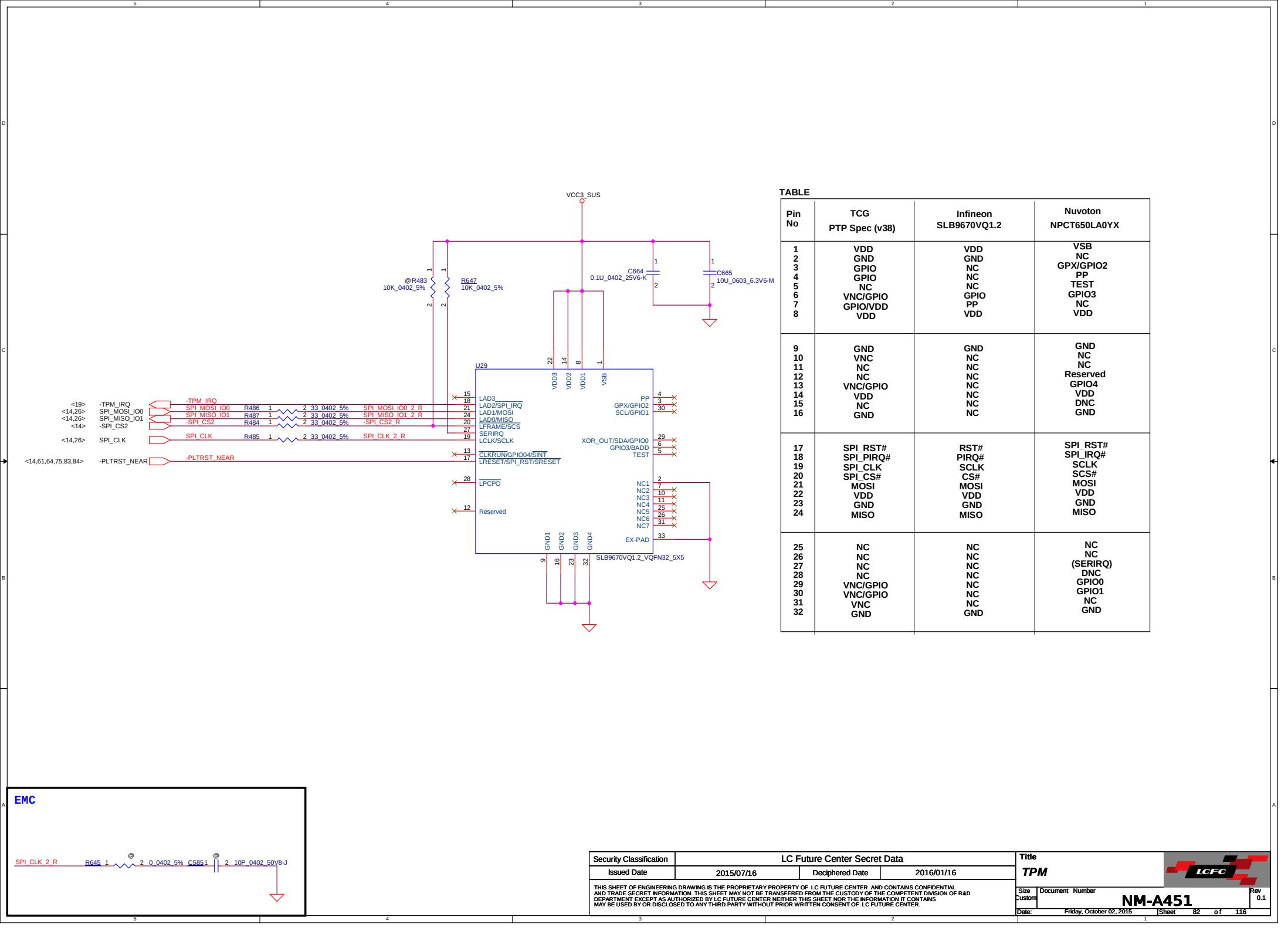
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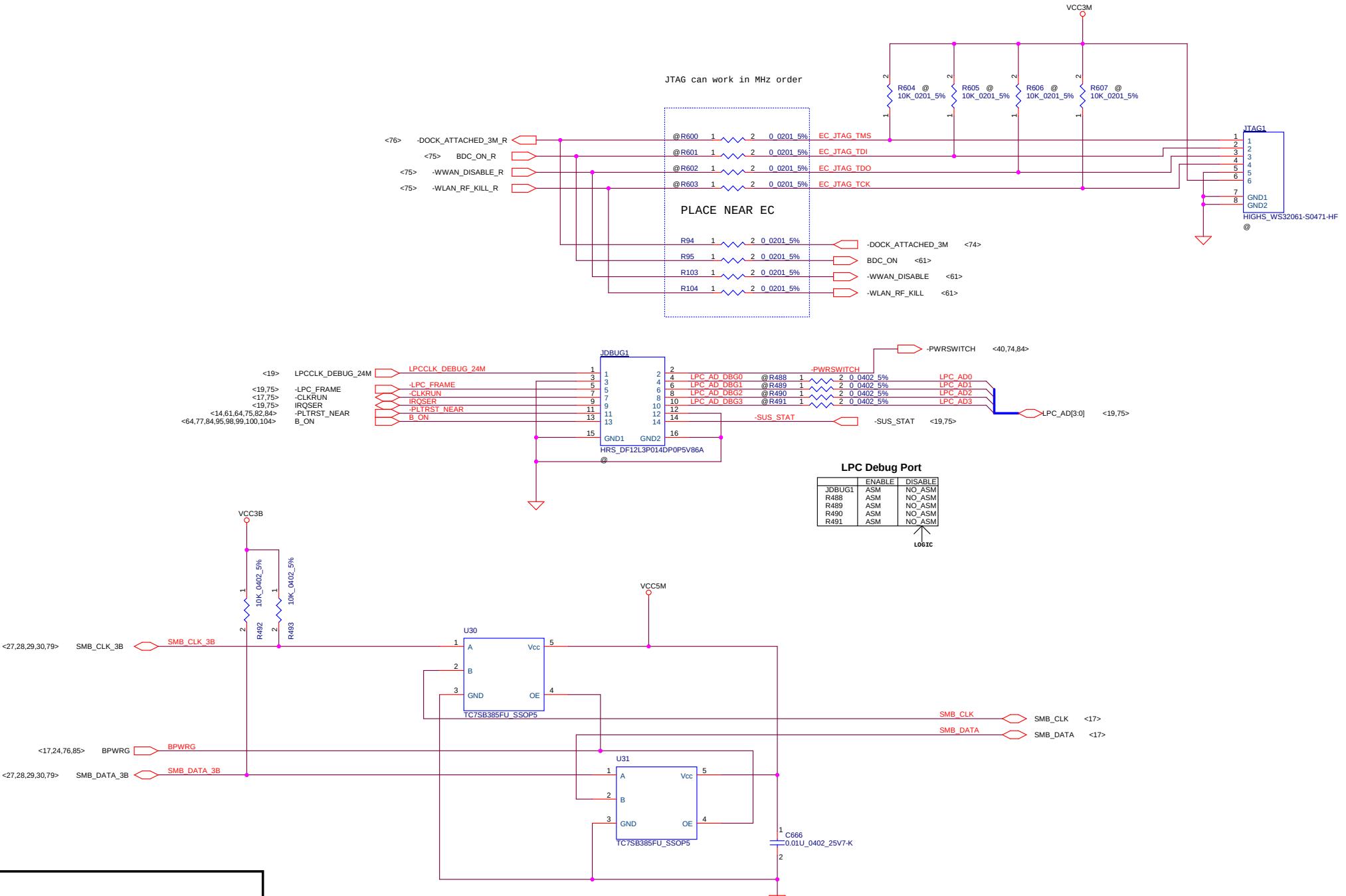
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EEPROM/SMBUS SW



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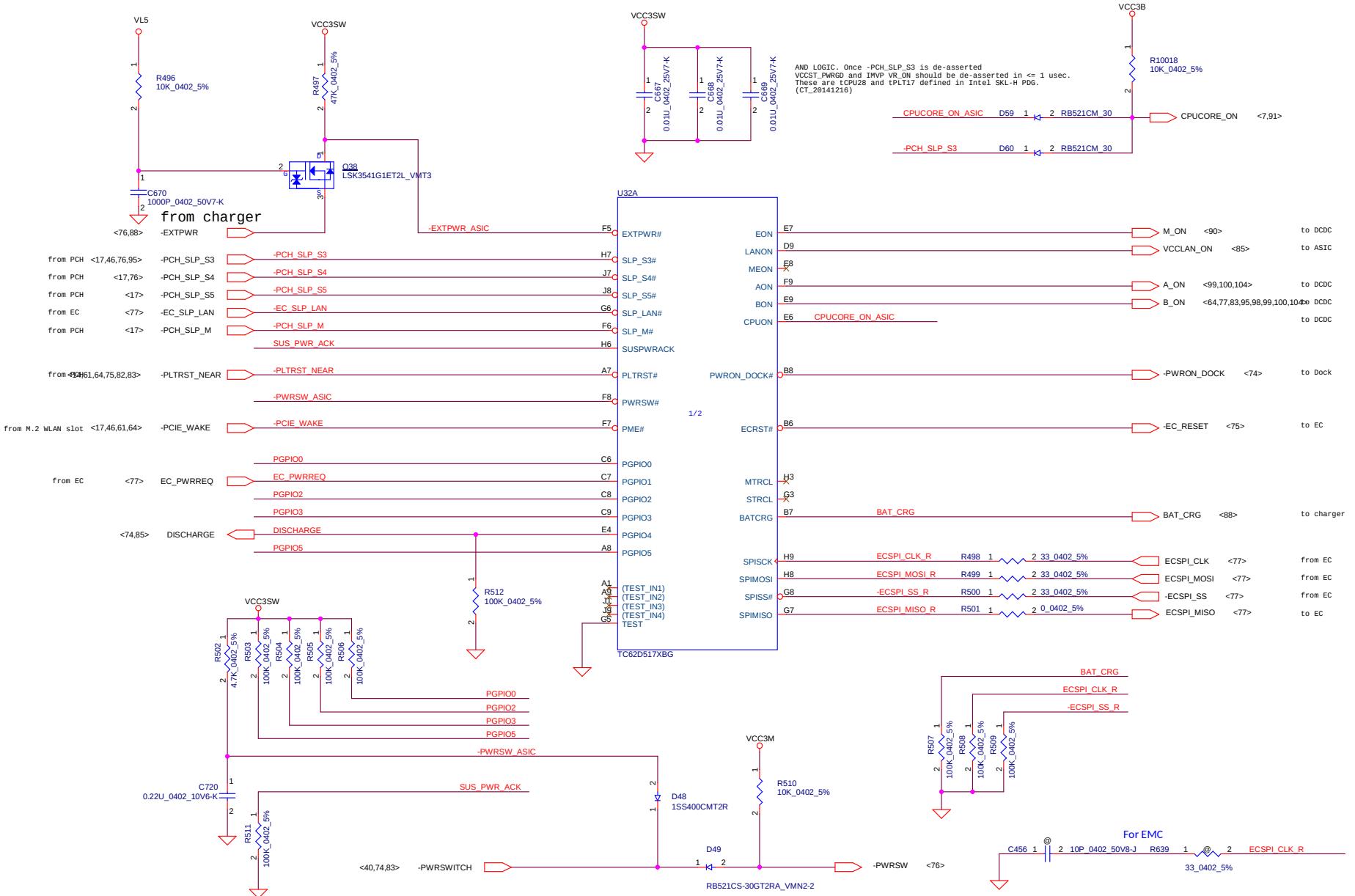
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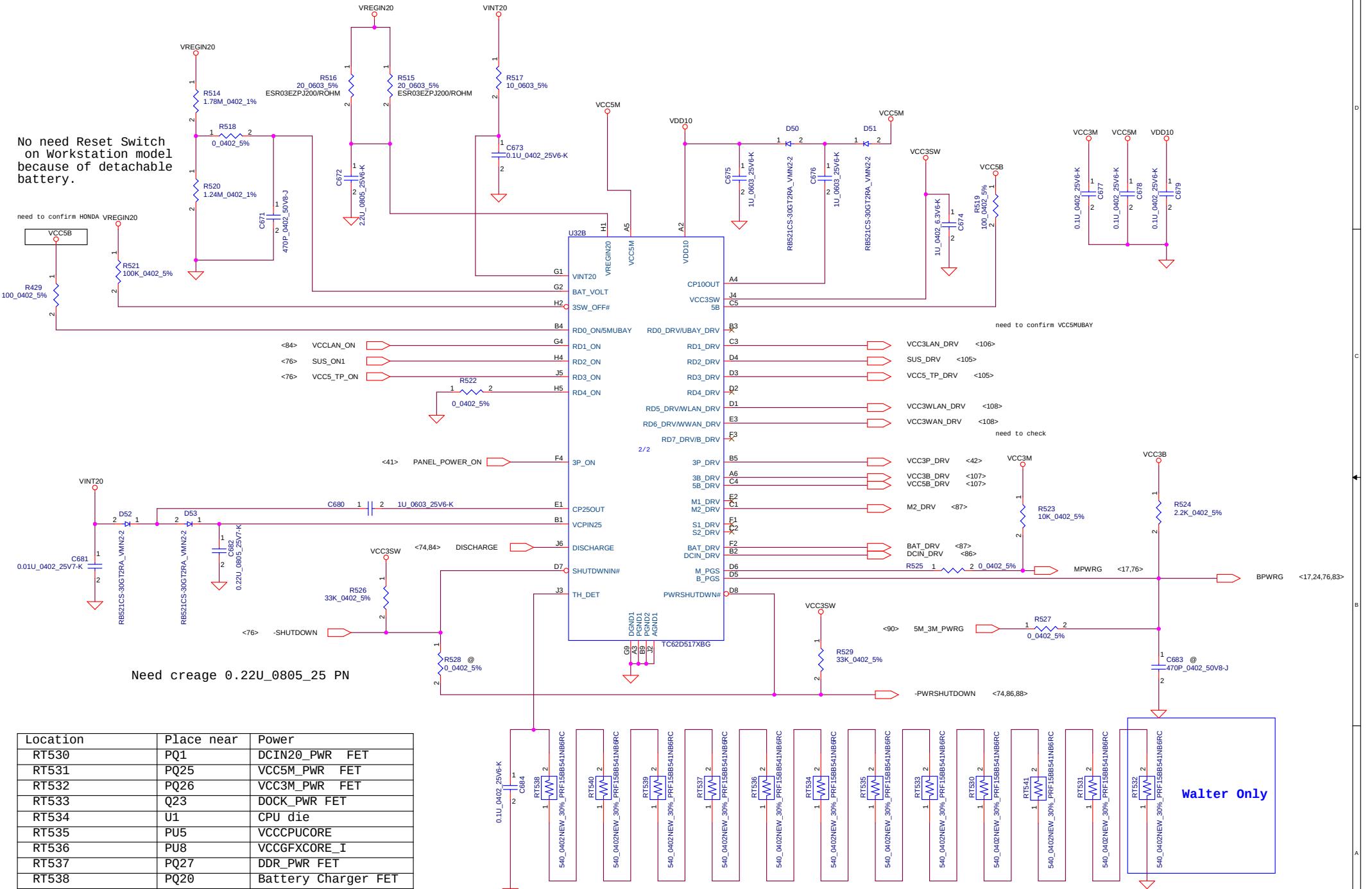
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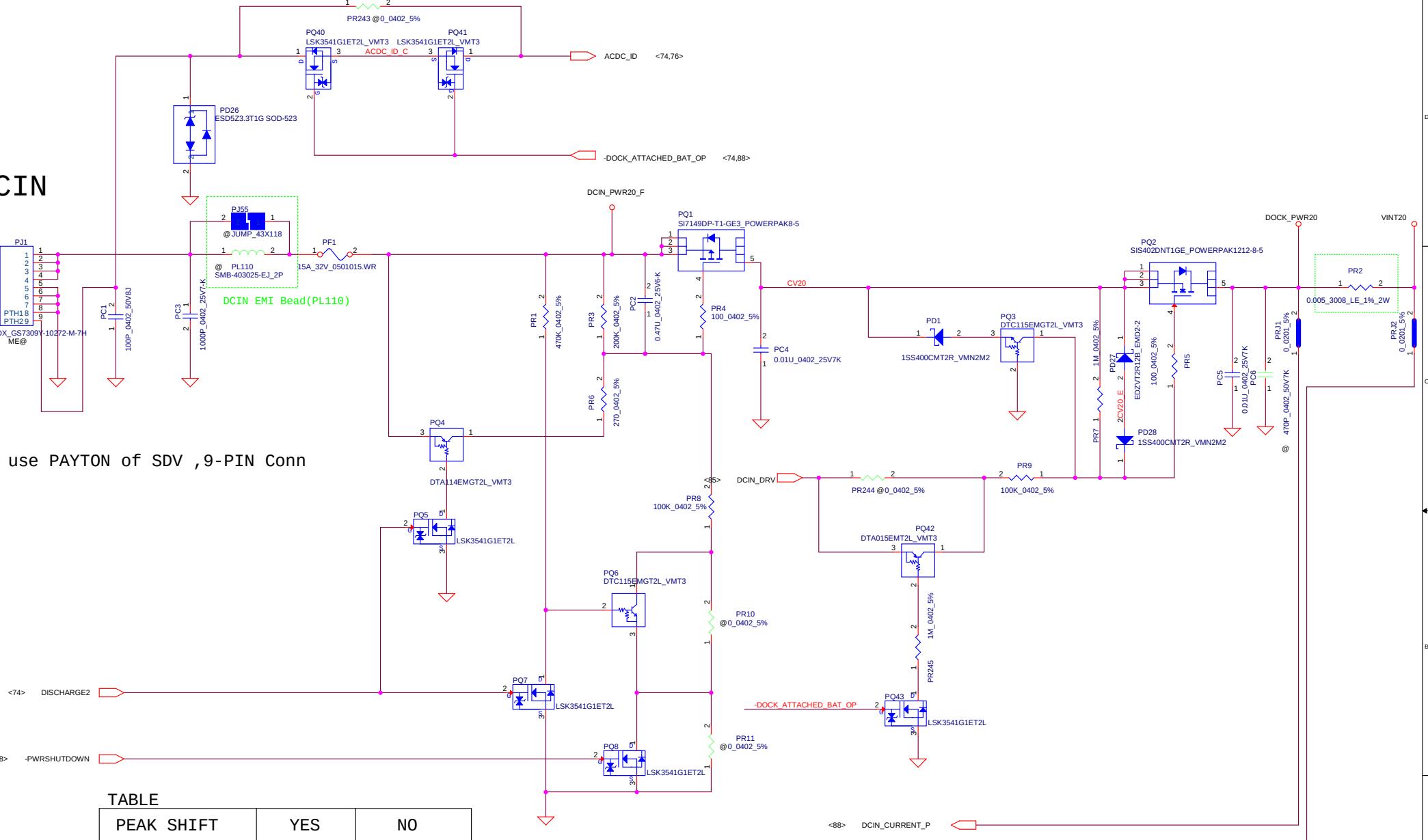
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DCIN

SDV use PAYTON of SDV , 9-PIN Conn



TABLE

PEAK SHIFT	YES	NO
PR10	NO-ASM	ASM
PR1	ASM	NO-ASM
PQ6	ASM	NO-ASM
PQ7	ASM	NO-ASM

LOGIC

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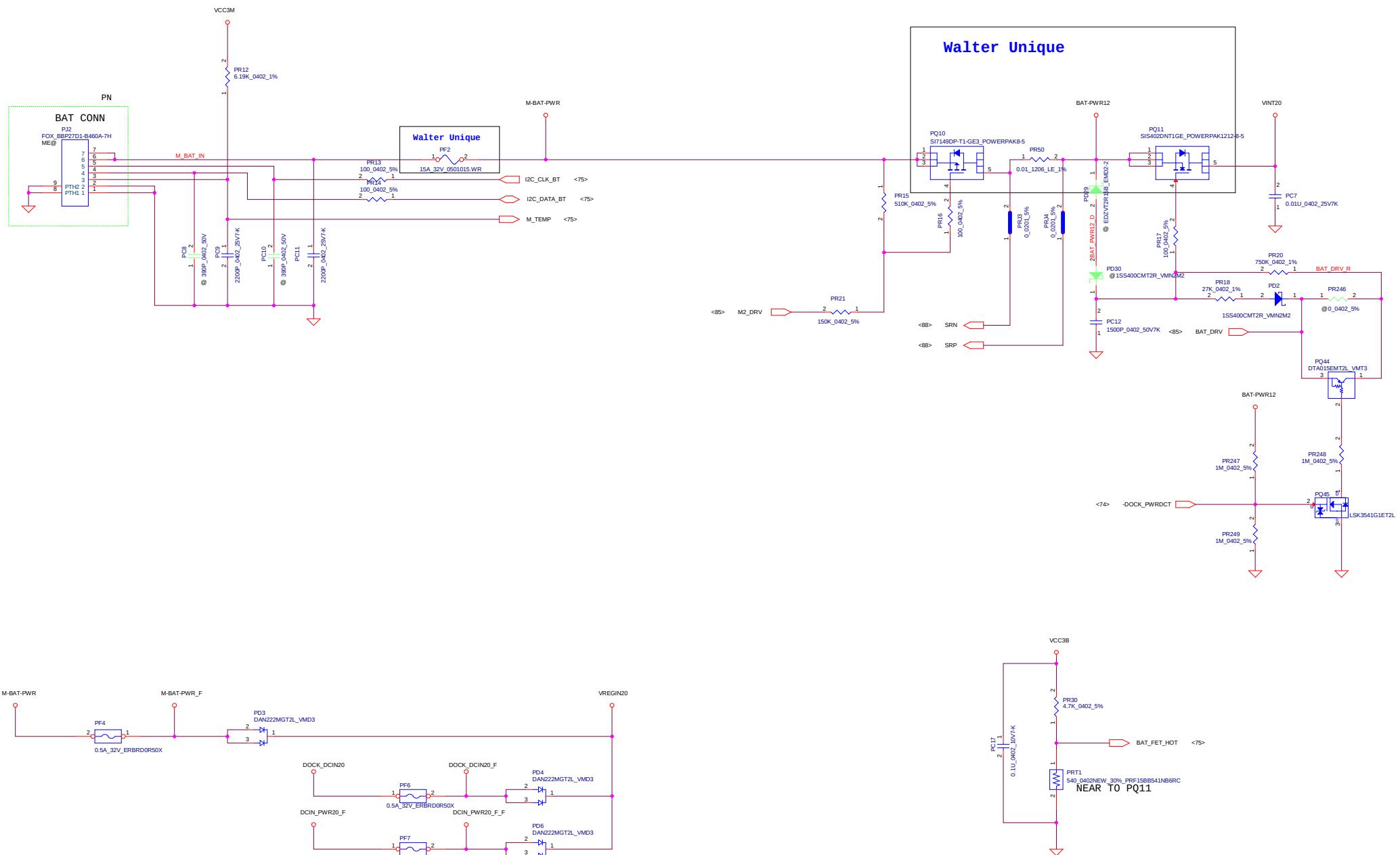
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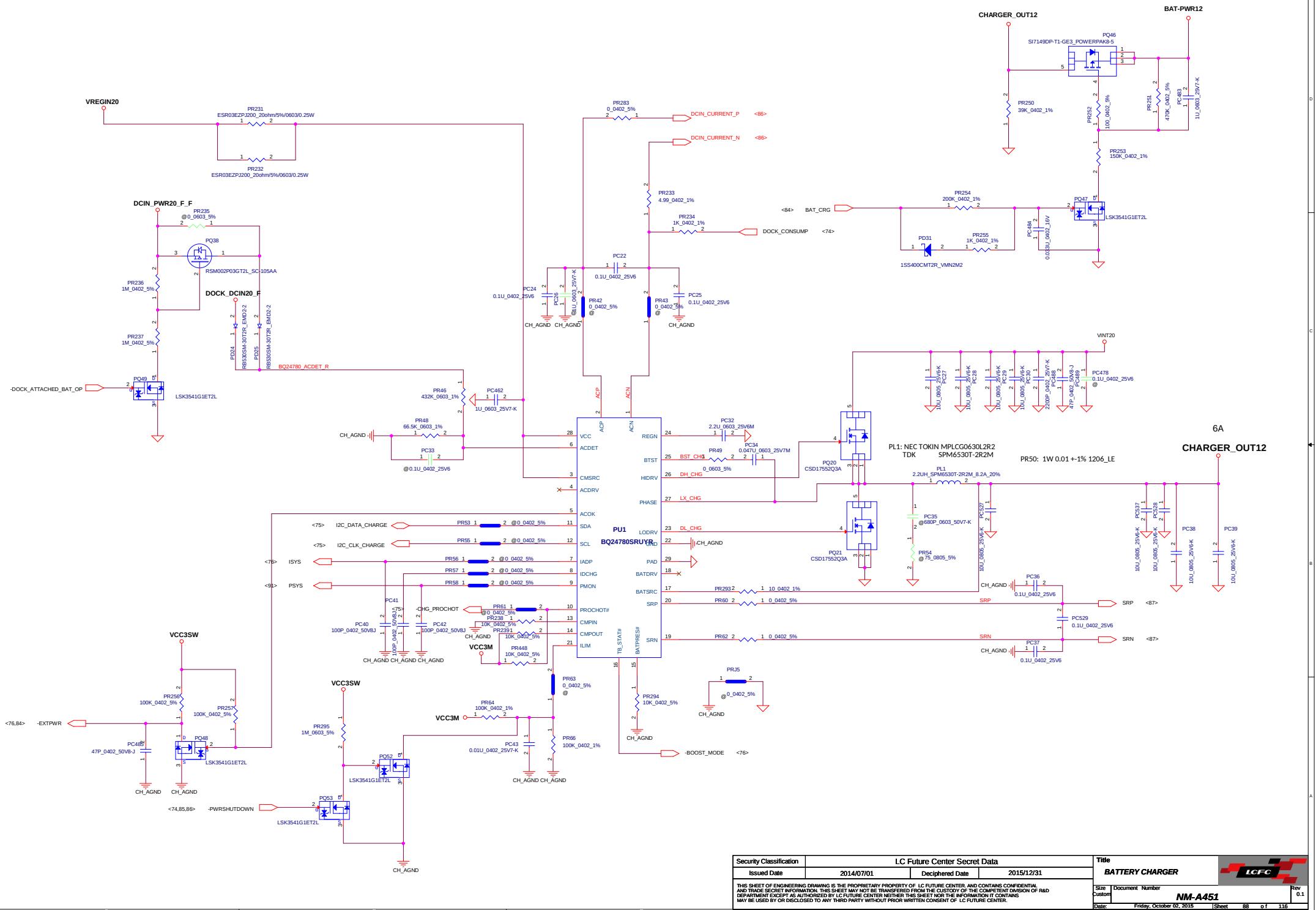
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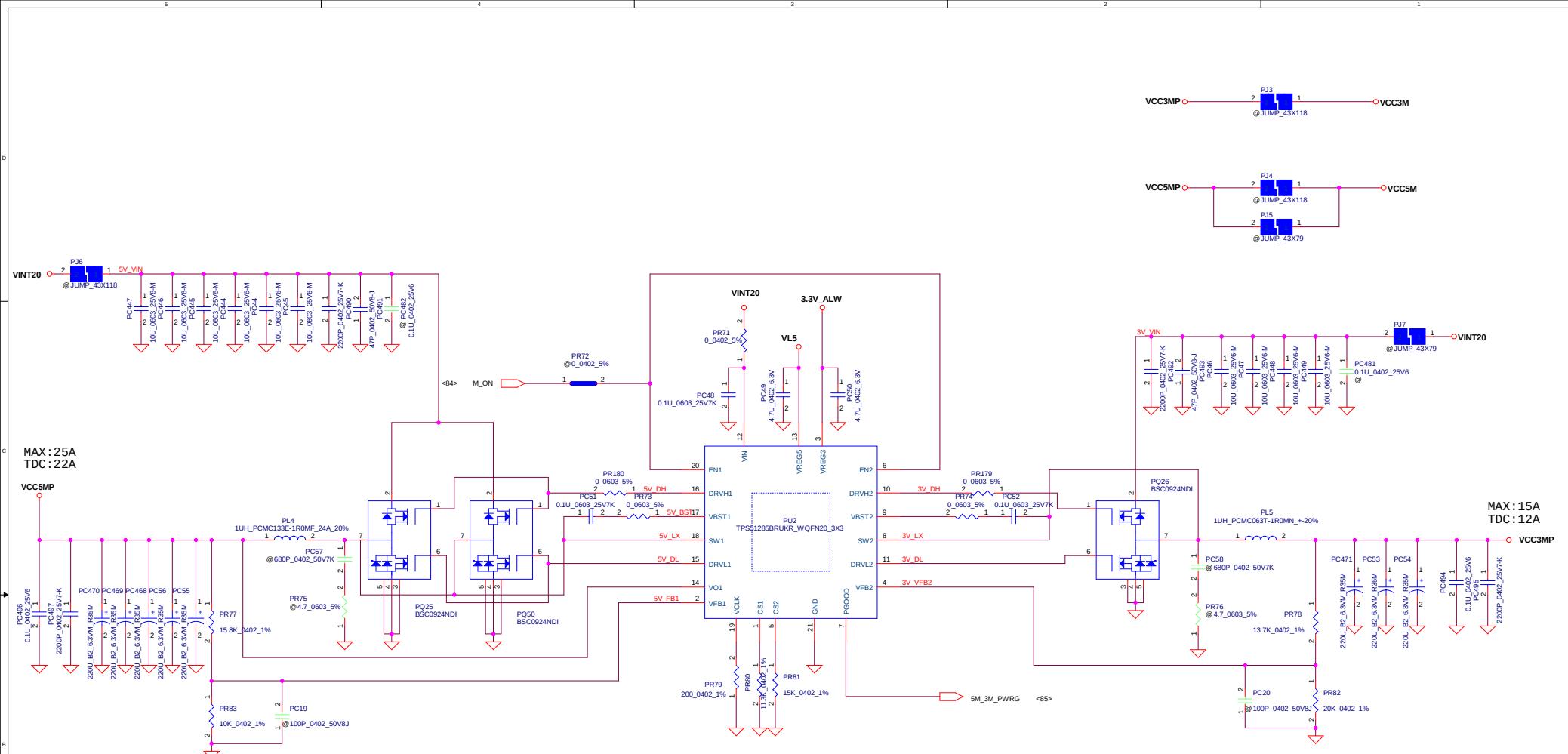


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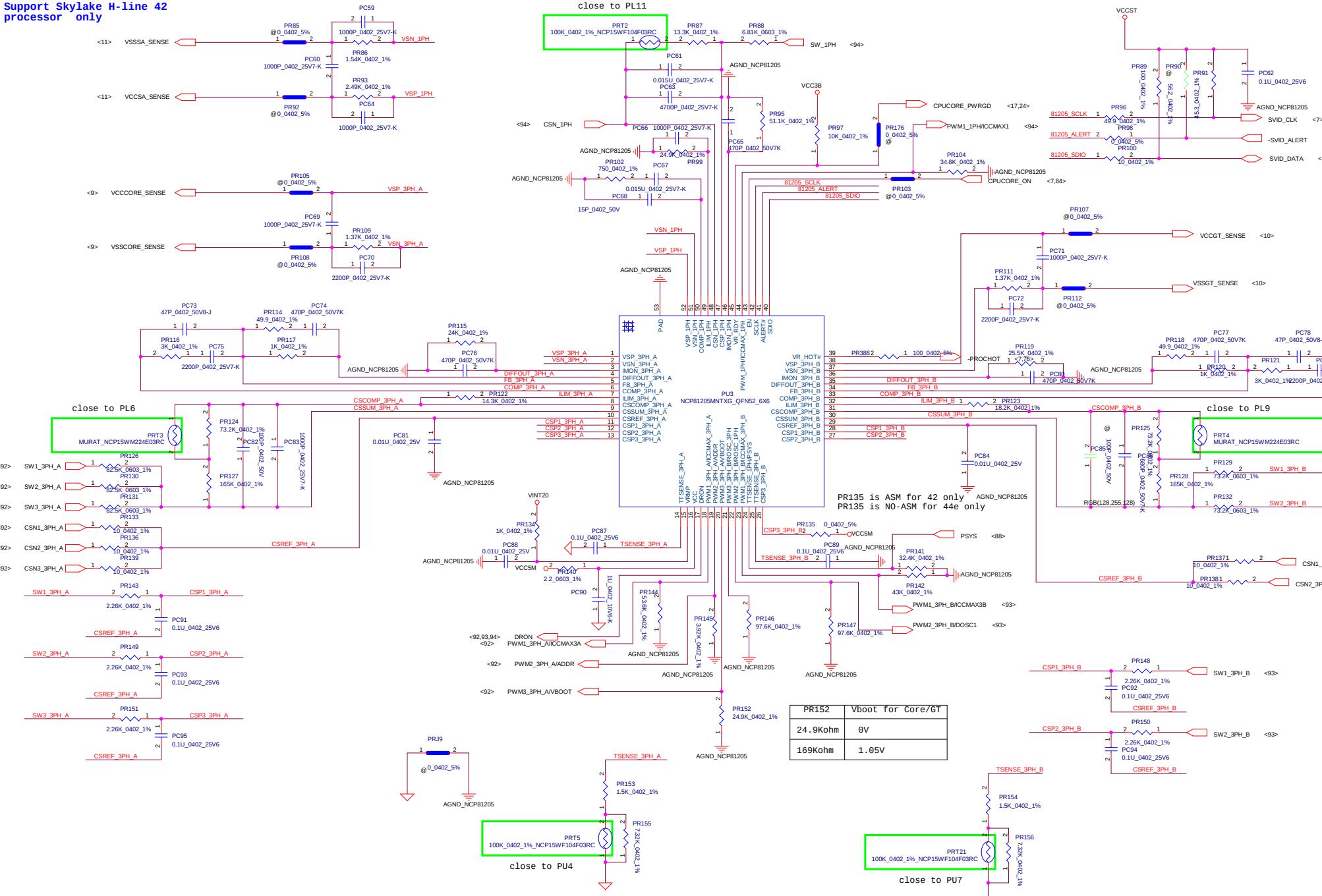
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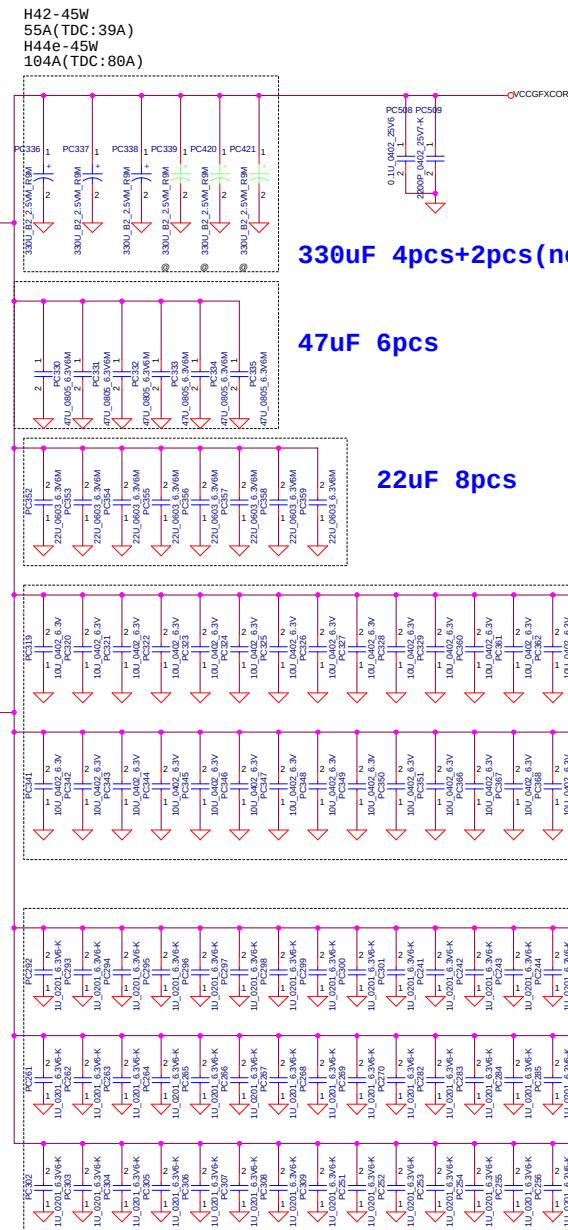
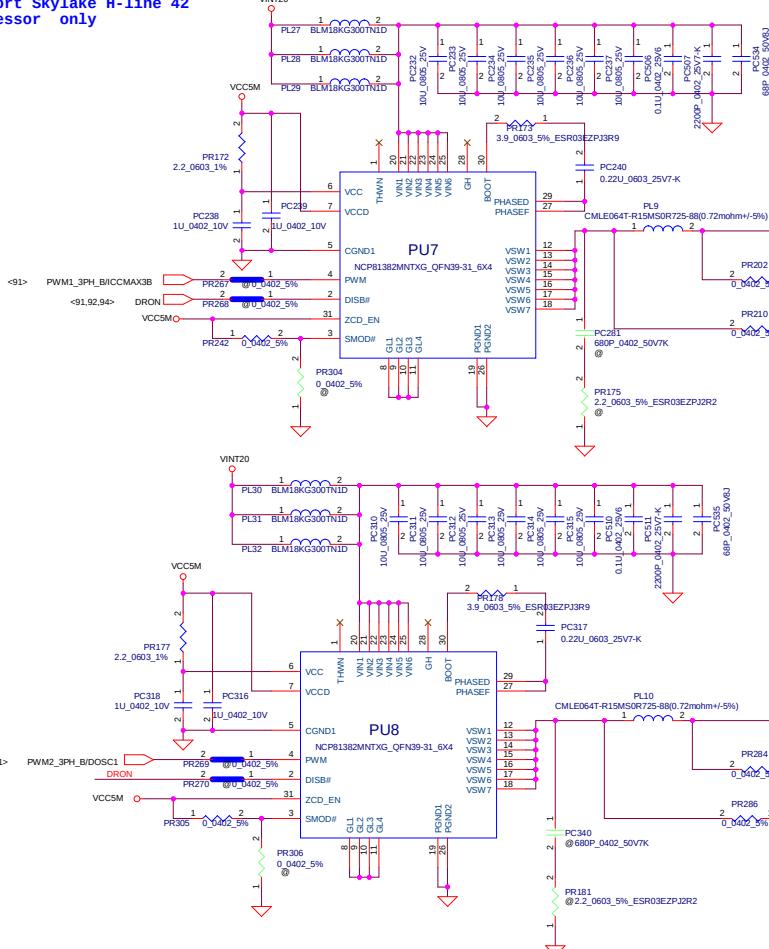
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Support Skylake H-line 42 processor only



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Support Skylake H-line 42
processor only



330uF 4pcs+2pcs (no mount)

47uF 6pcs

22uF 8pcs

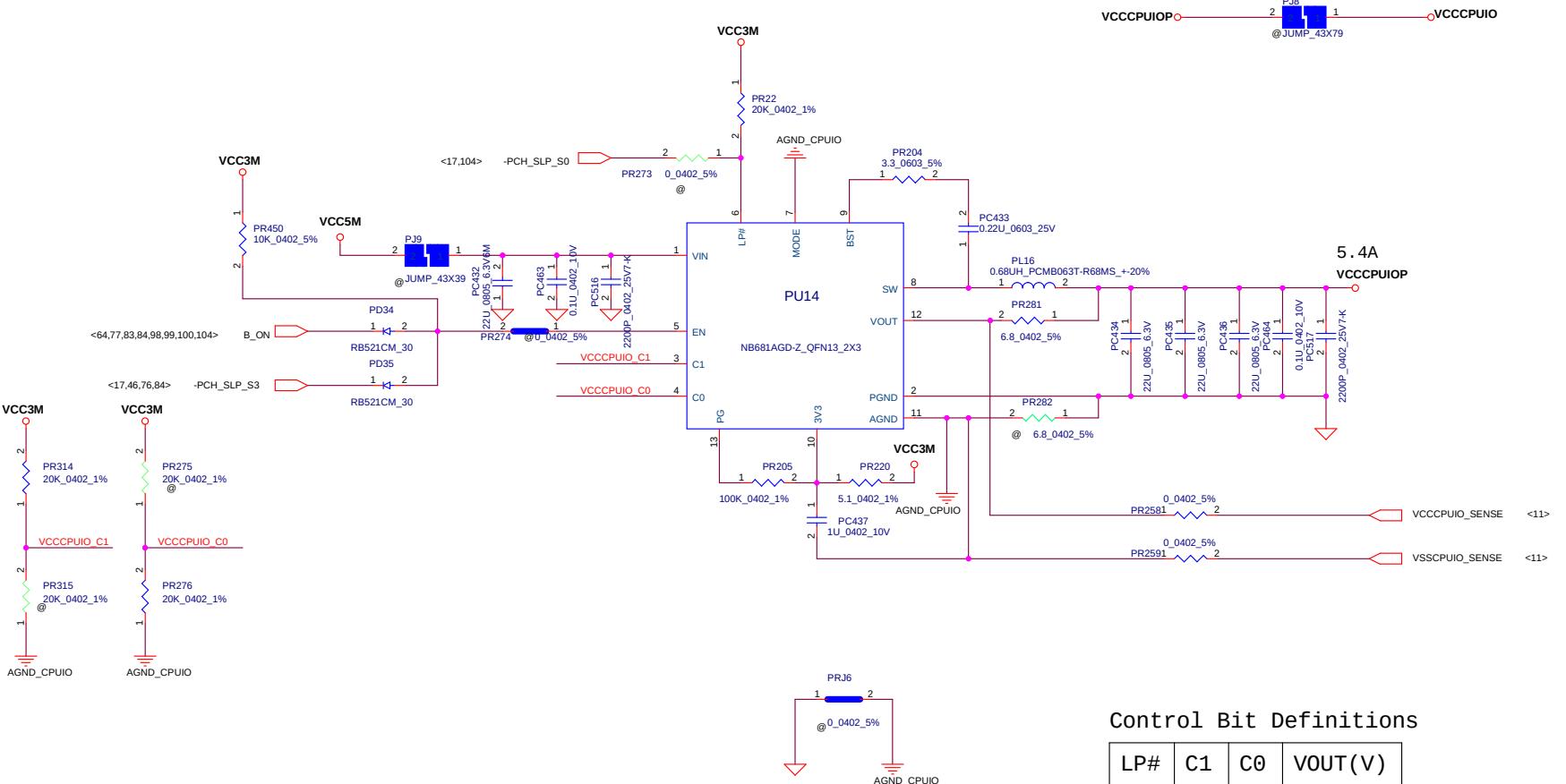
10uF 35pcs

1uF 68pcs

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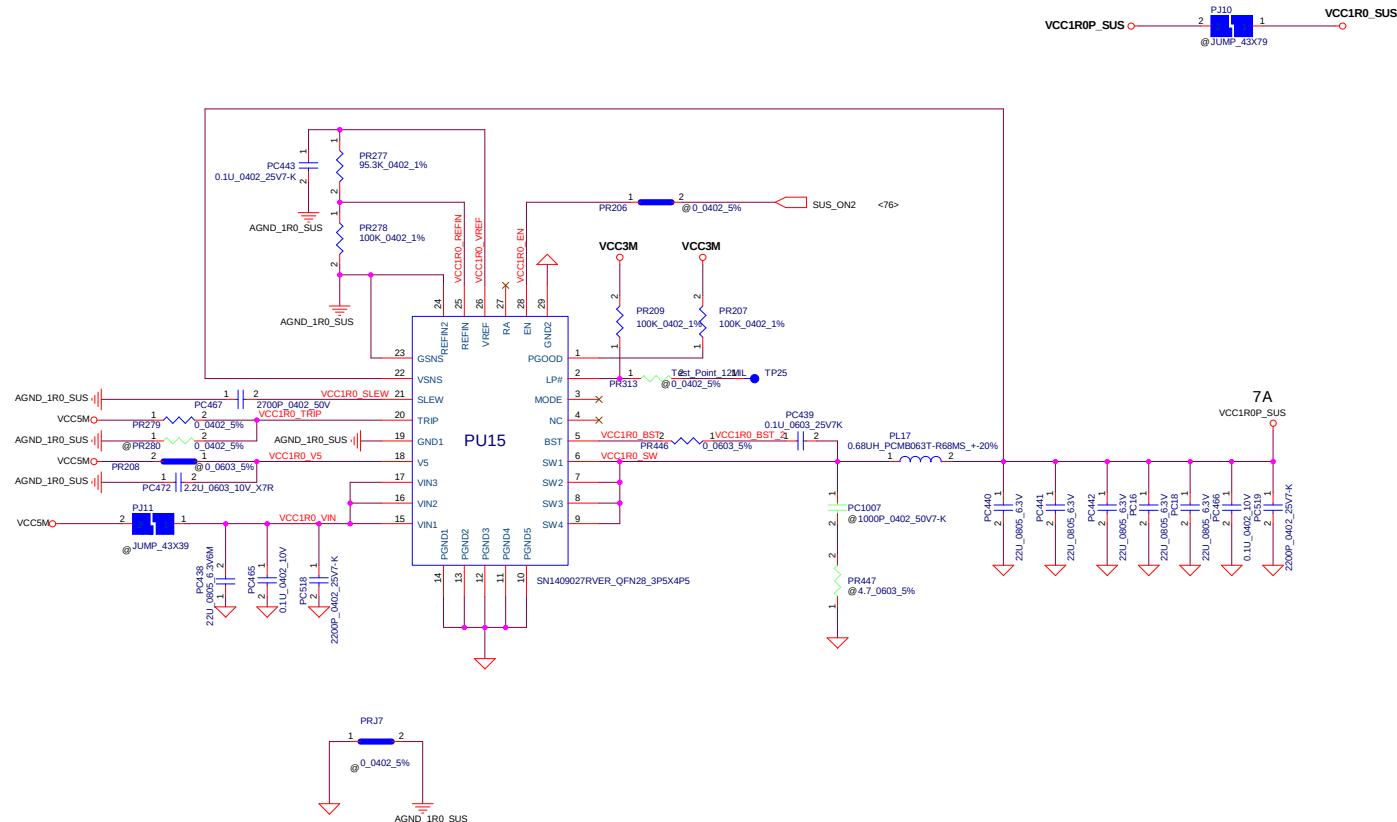
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Size		Document Number		Rev							
Custom		NM-A451		0.1				Date:	Friday, October 02, 2015	Sheet	94 of 116



Control Bit Definitions

LP#	C1	C0	VOUT(V)
0	X	X	0
1	0	0	0.85
1	0	1	0.875
1	1	0	0.95
1	1	1	0.975

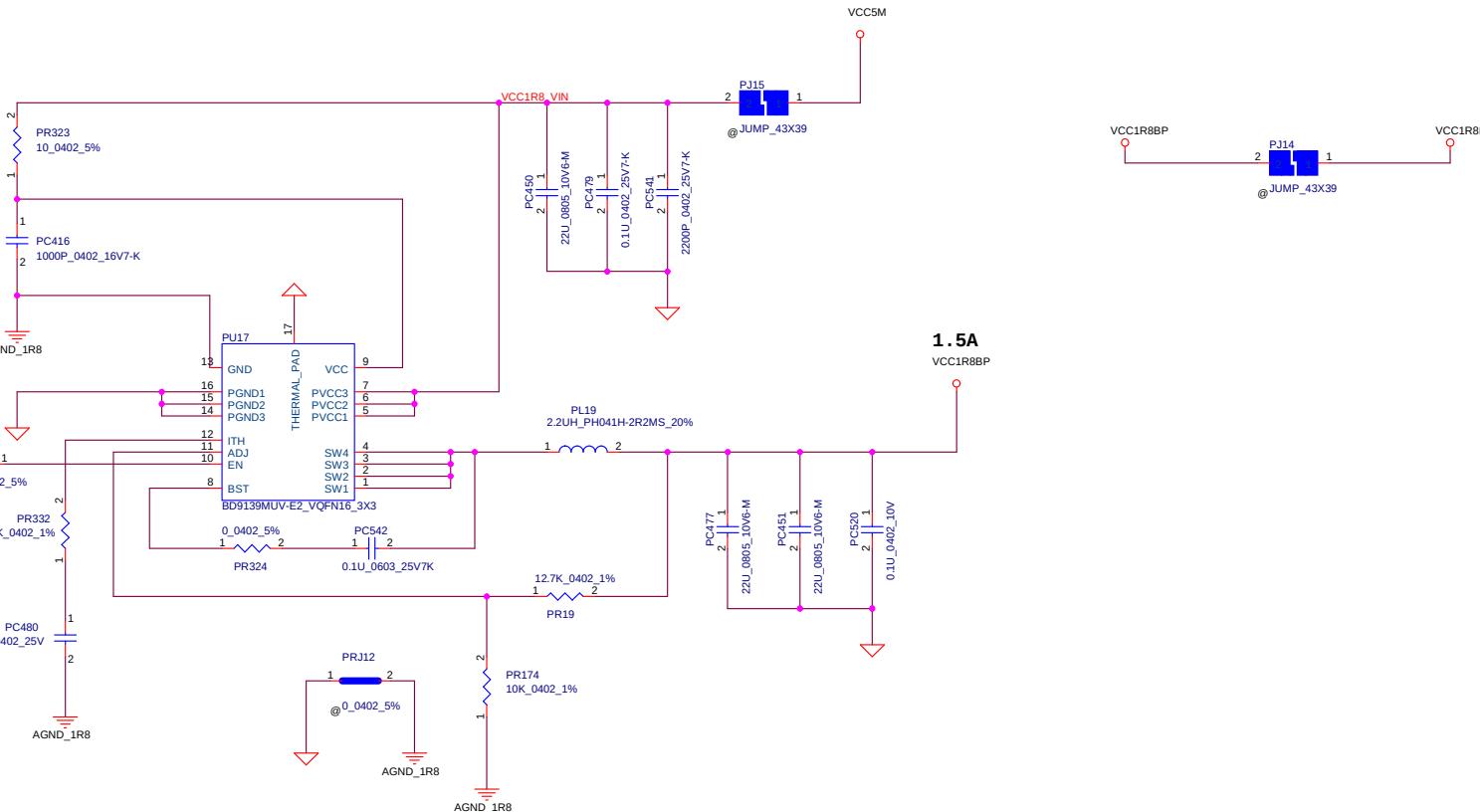


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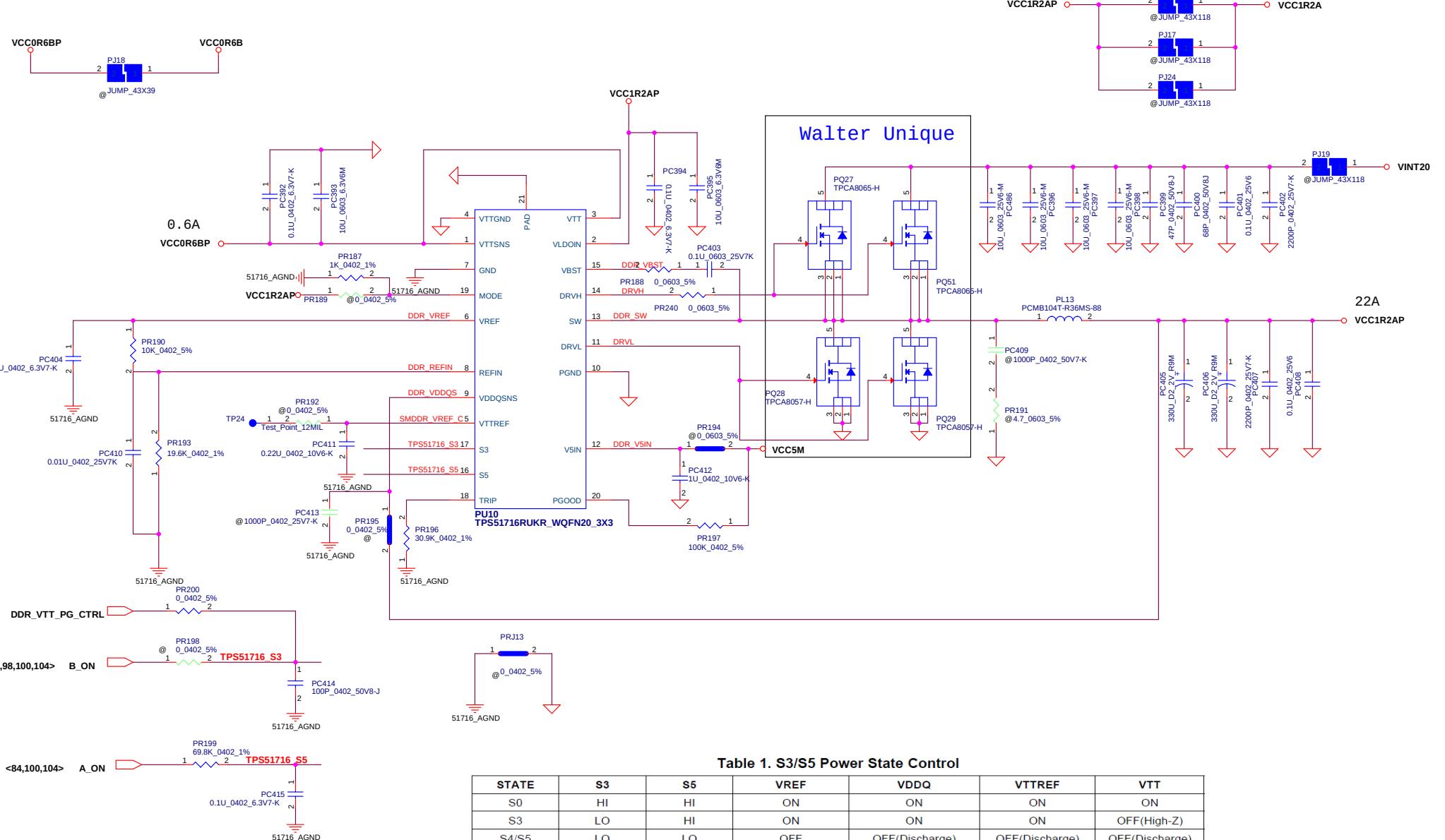
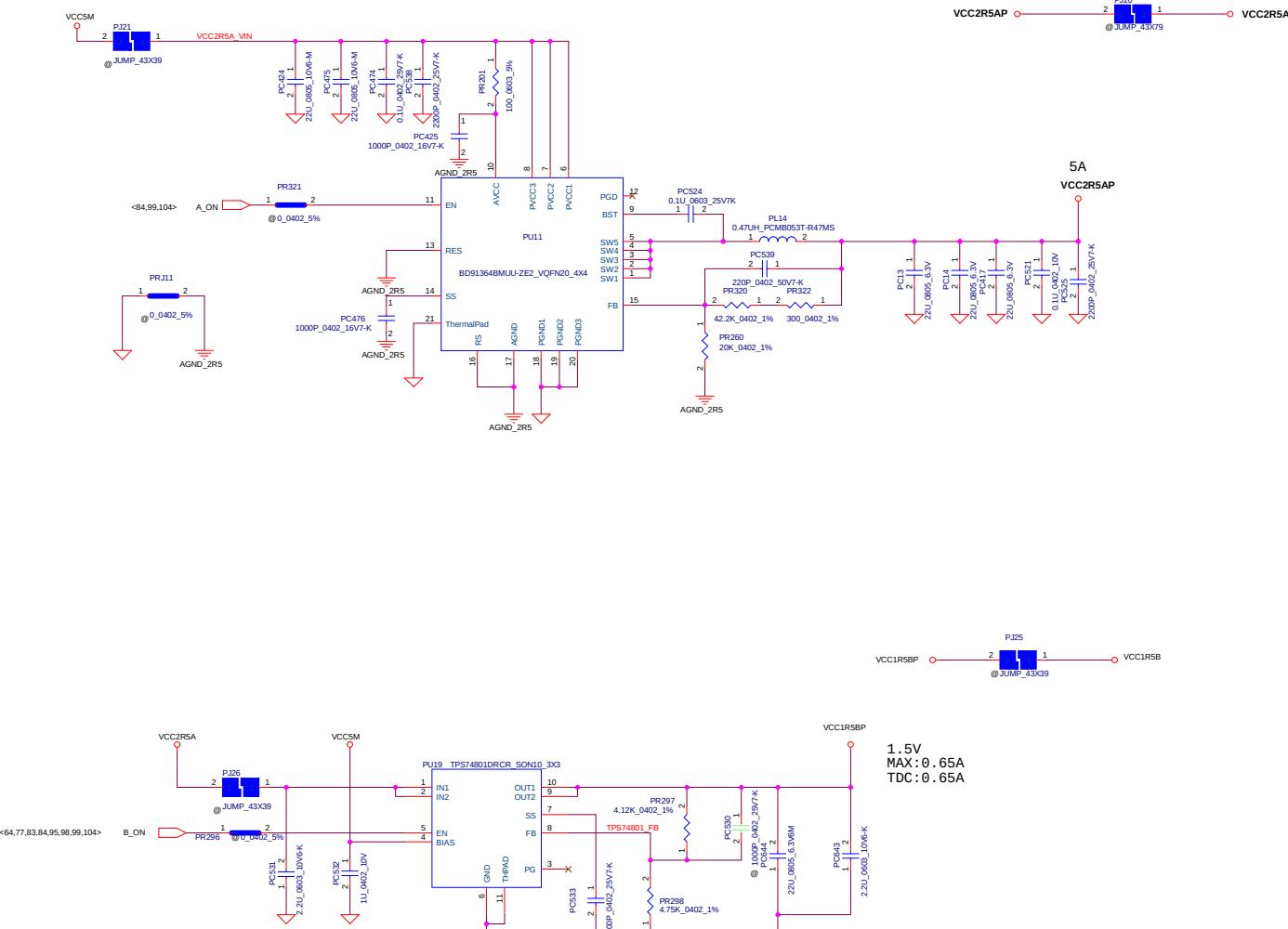


Table 1. S3/S5 Power State Control

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)



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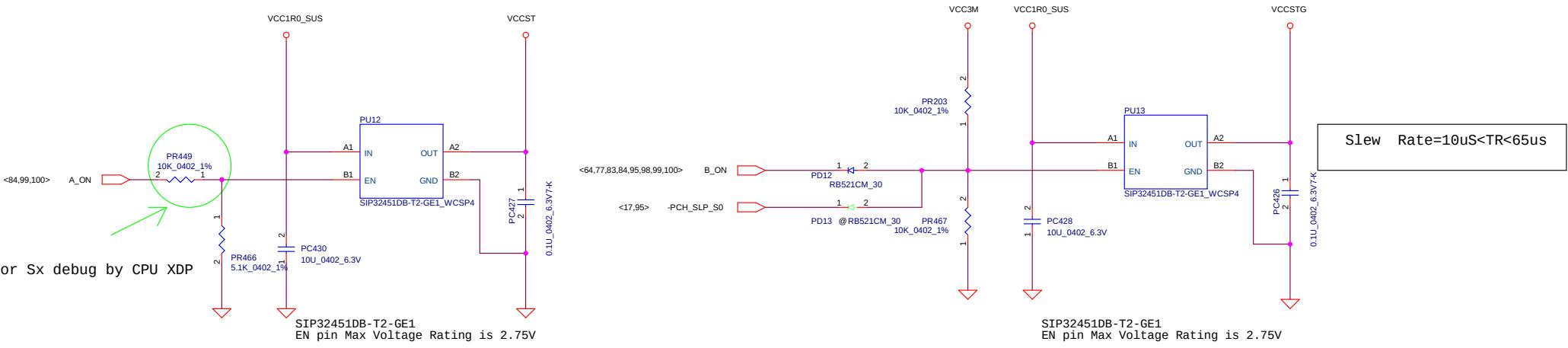
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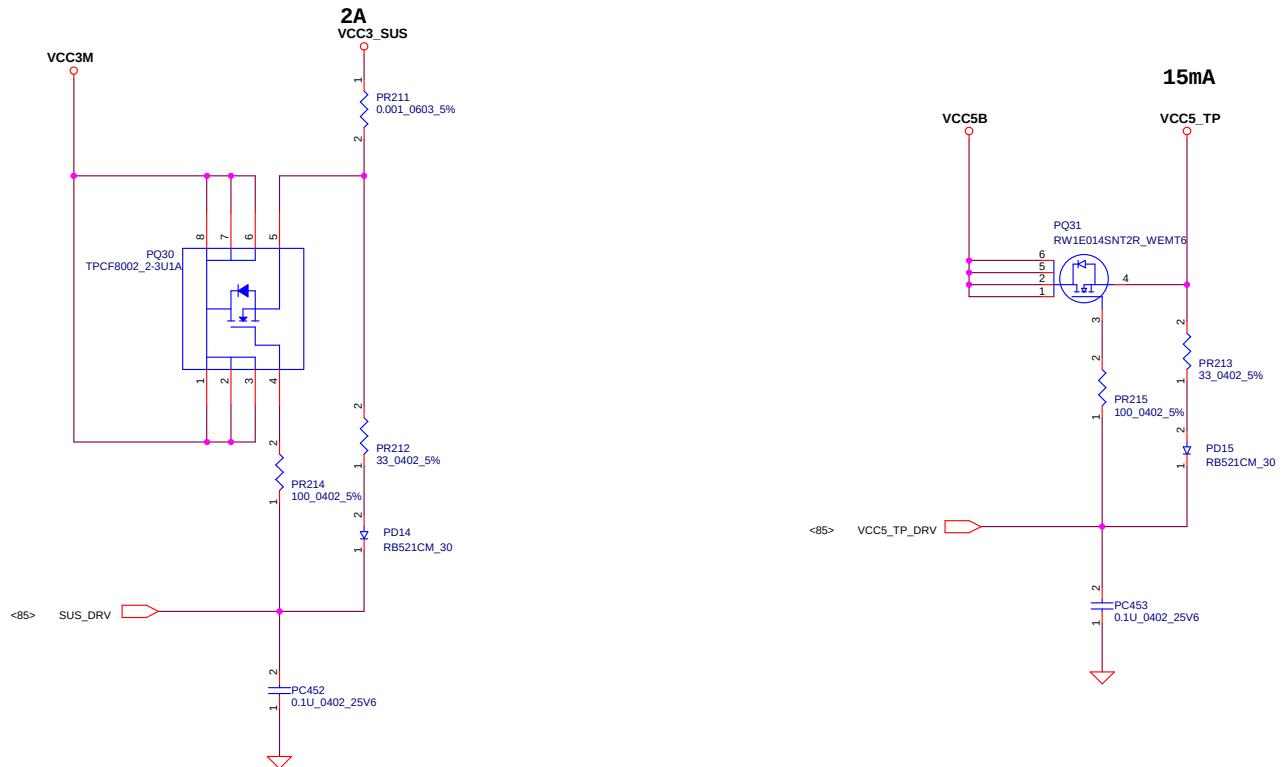
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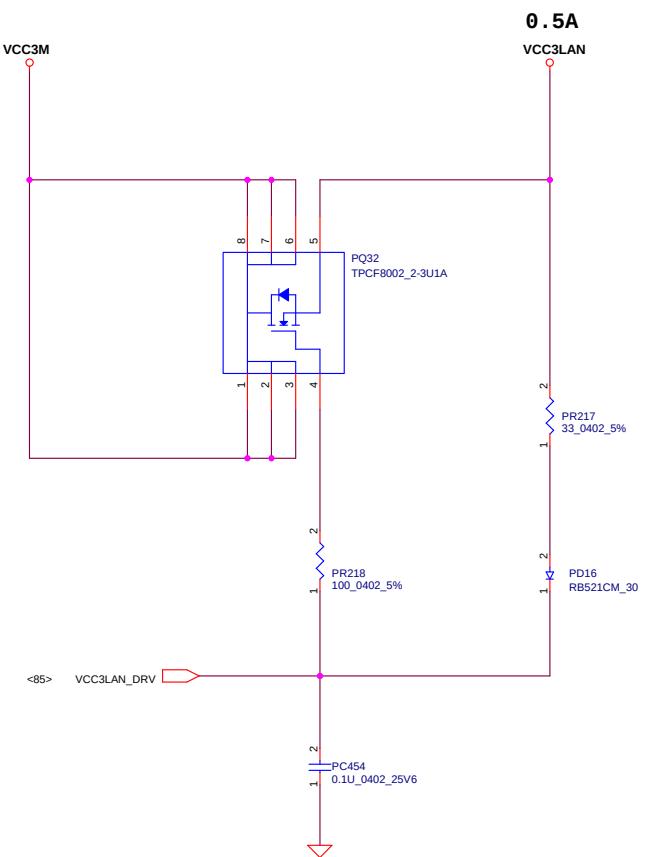
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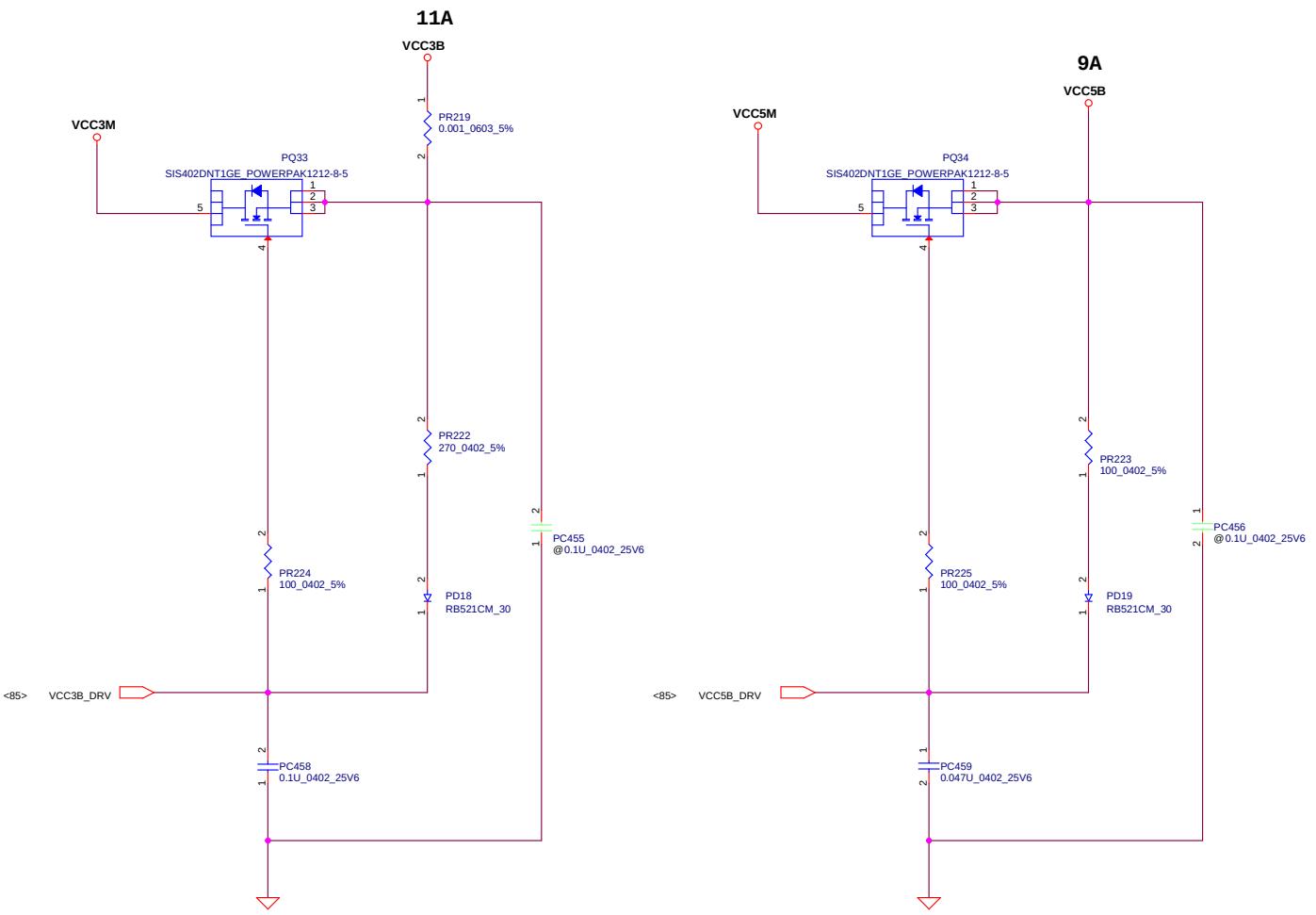




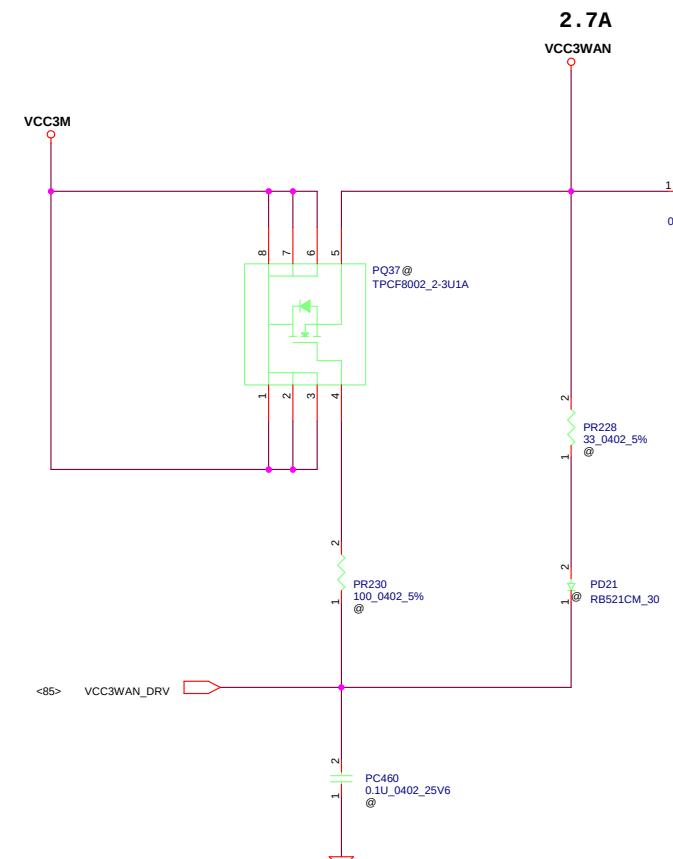
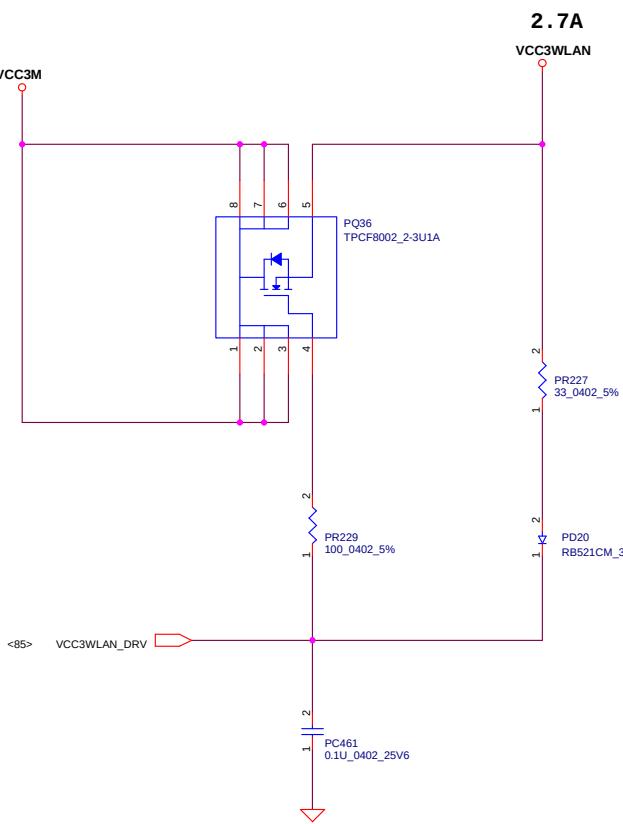
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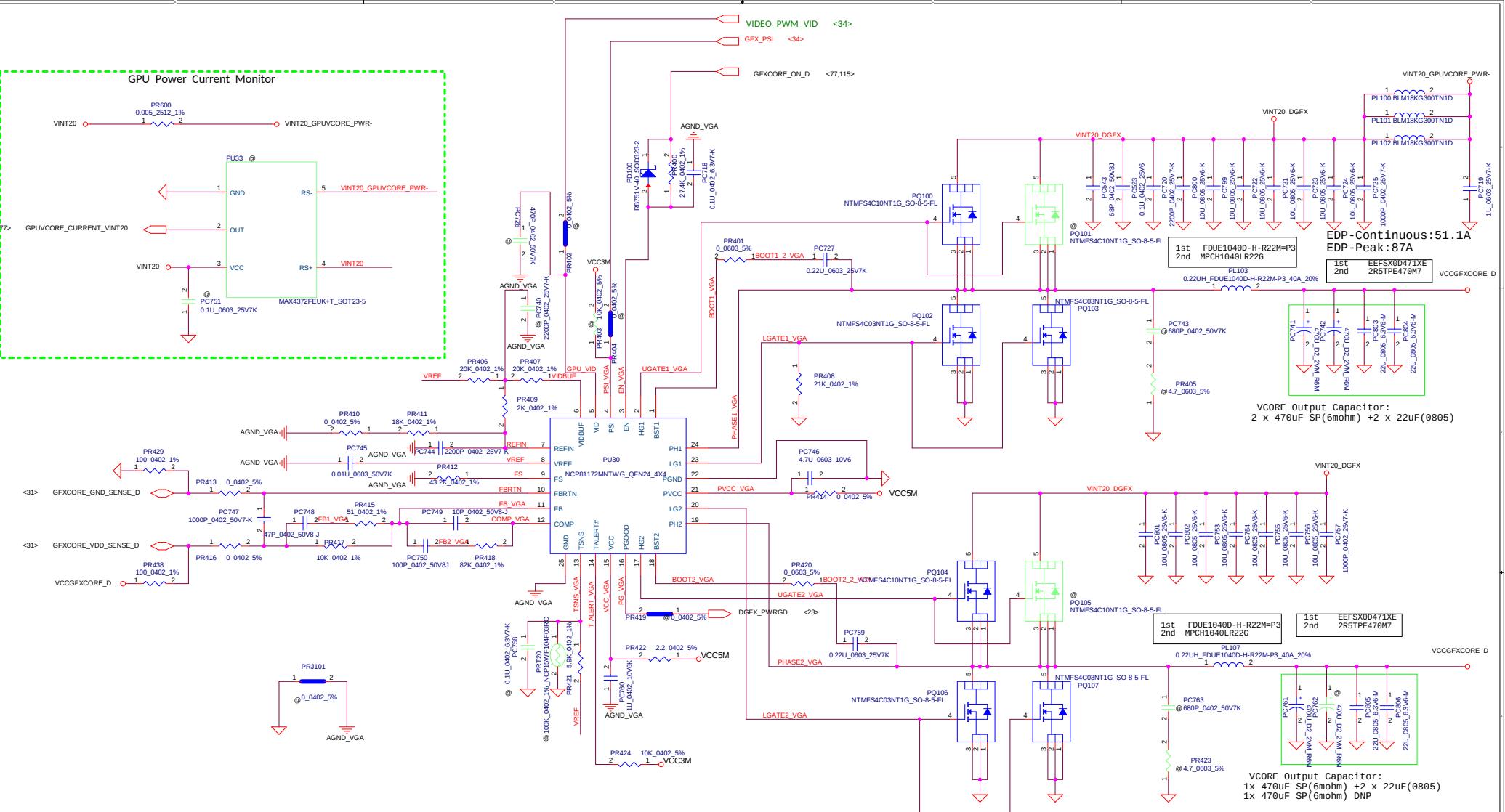
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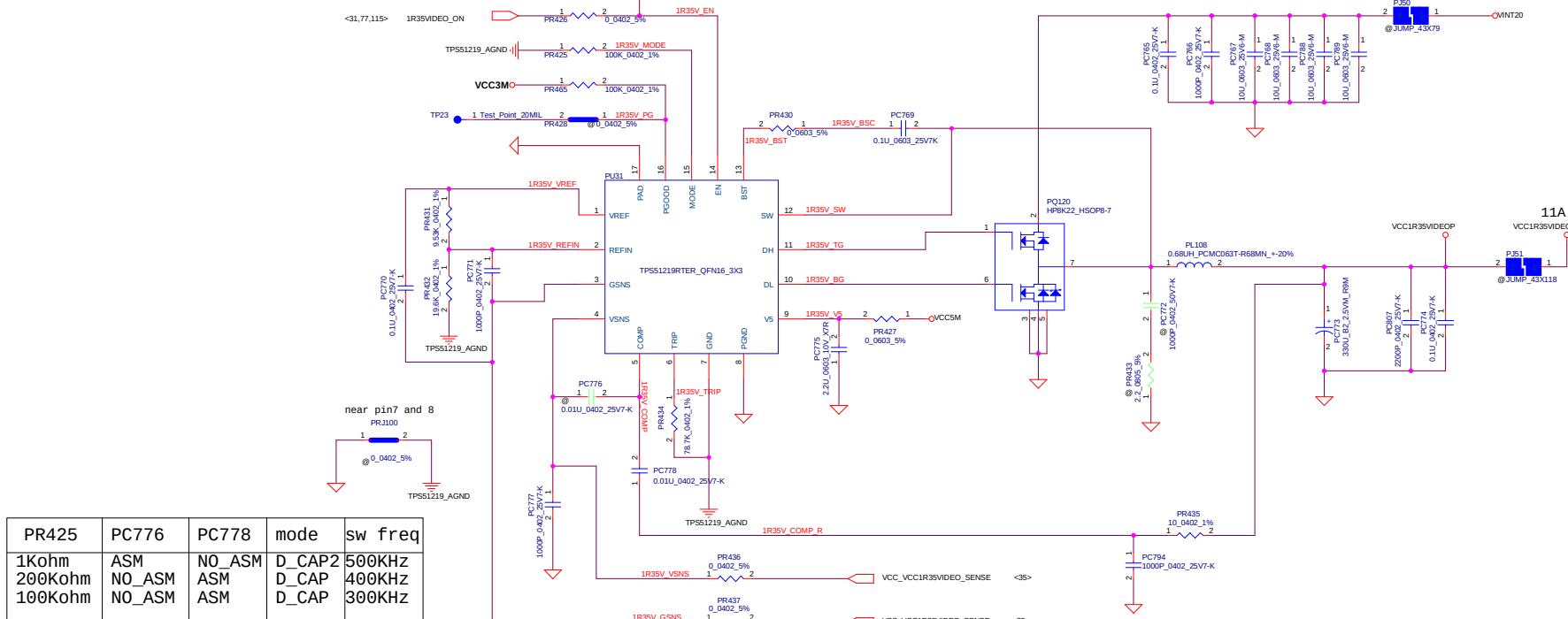
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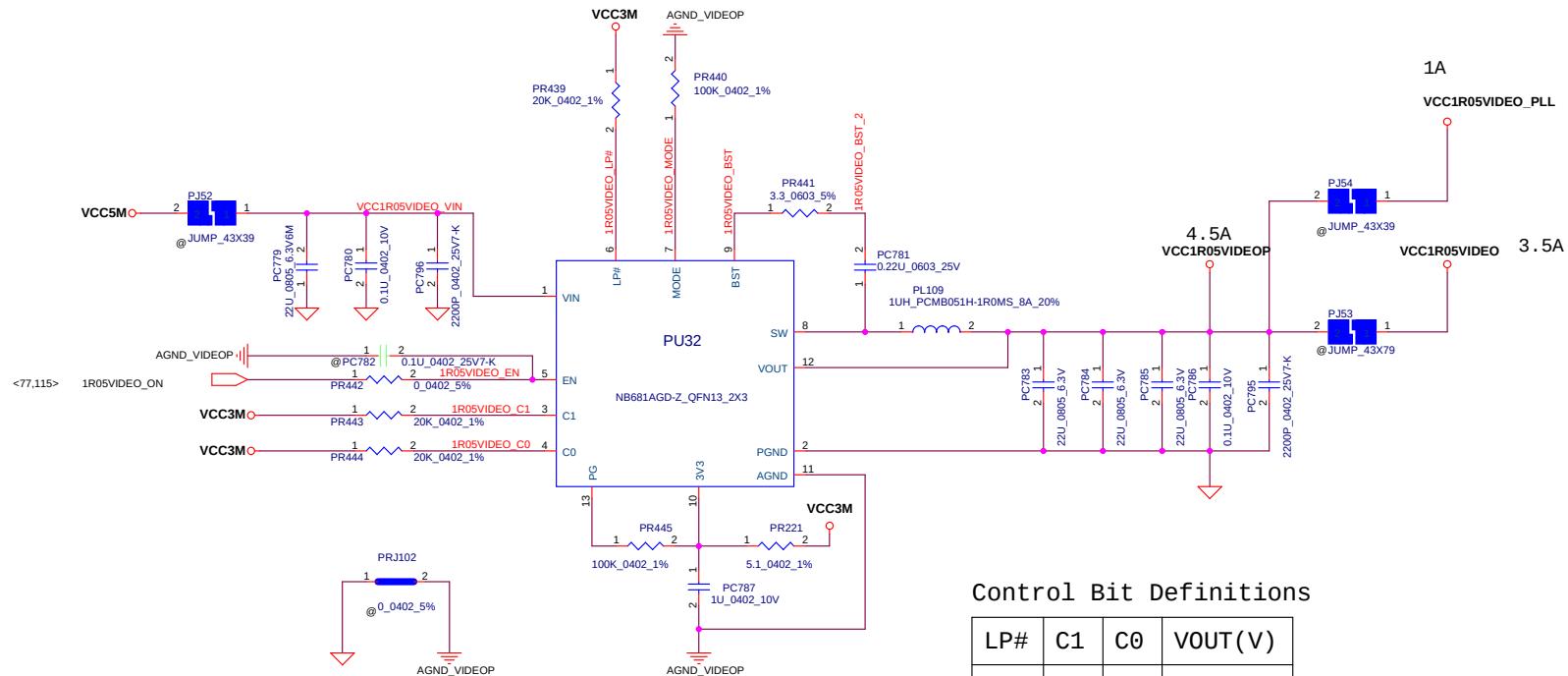


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PR425	PC776	PC778	mode	sw freq
1Kohm	ASM	NO_ASM	D_CAP2	500KHZ
200Kohm	NO_ASM	ASM	D_CAP	400KHZ
100Kohm	NO_ASM	ASM	D_CAP	300KHZ

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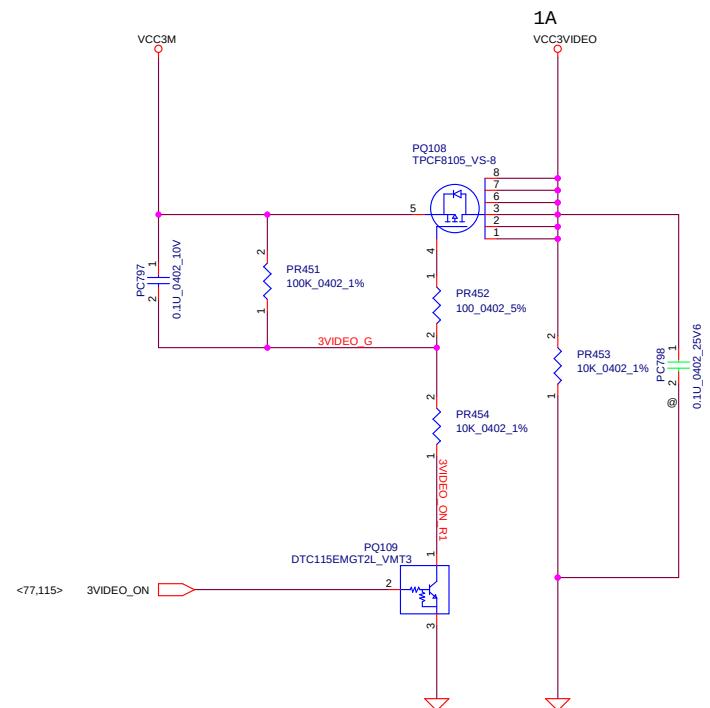


Control Bit Definitions

LP#	C1	C0	VOUT (V)
0	X	X	0
1	0	0	0.8
1	0	1	0.95
1	1	0	1
1	1	1	1.05

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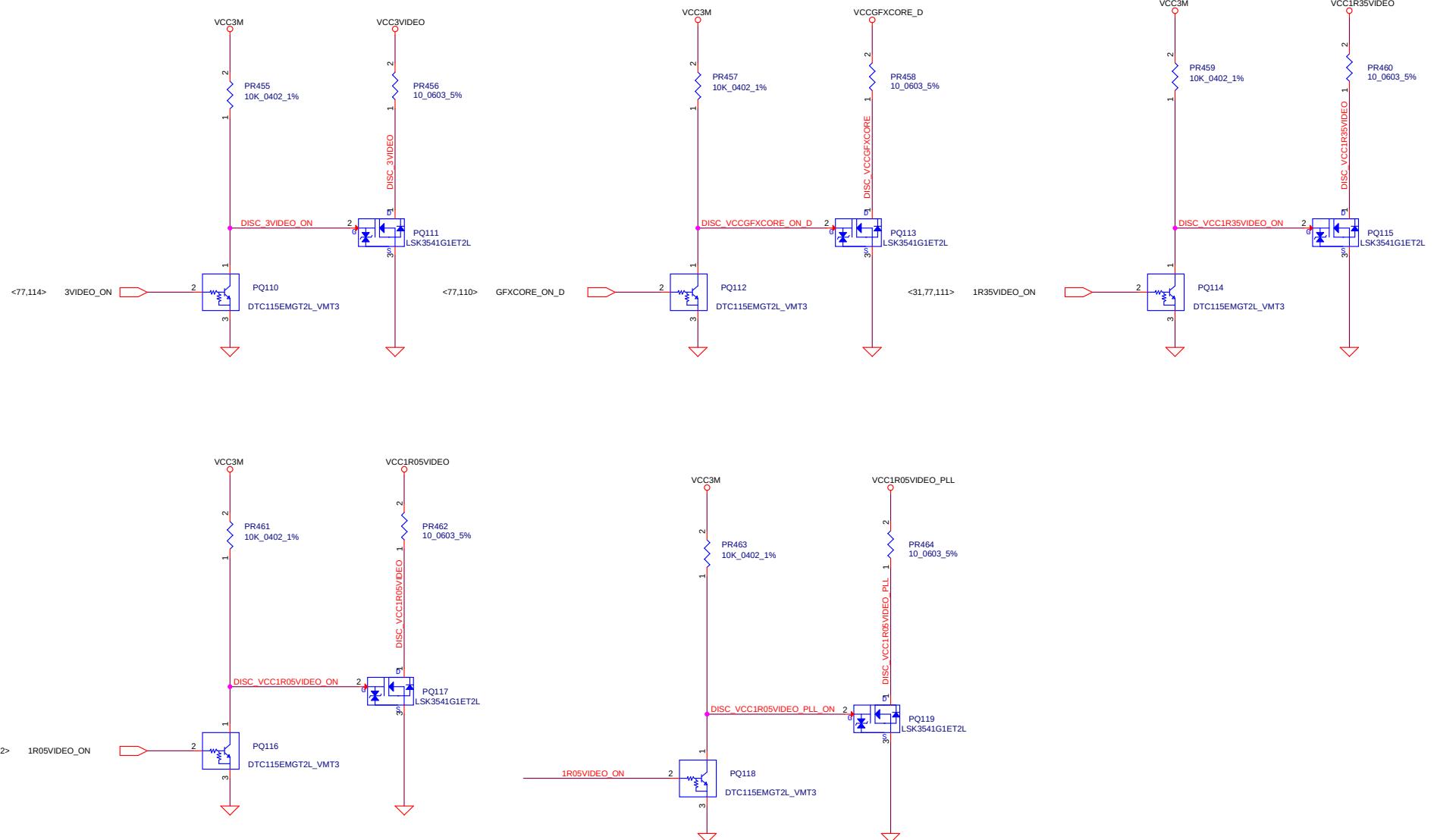
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