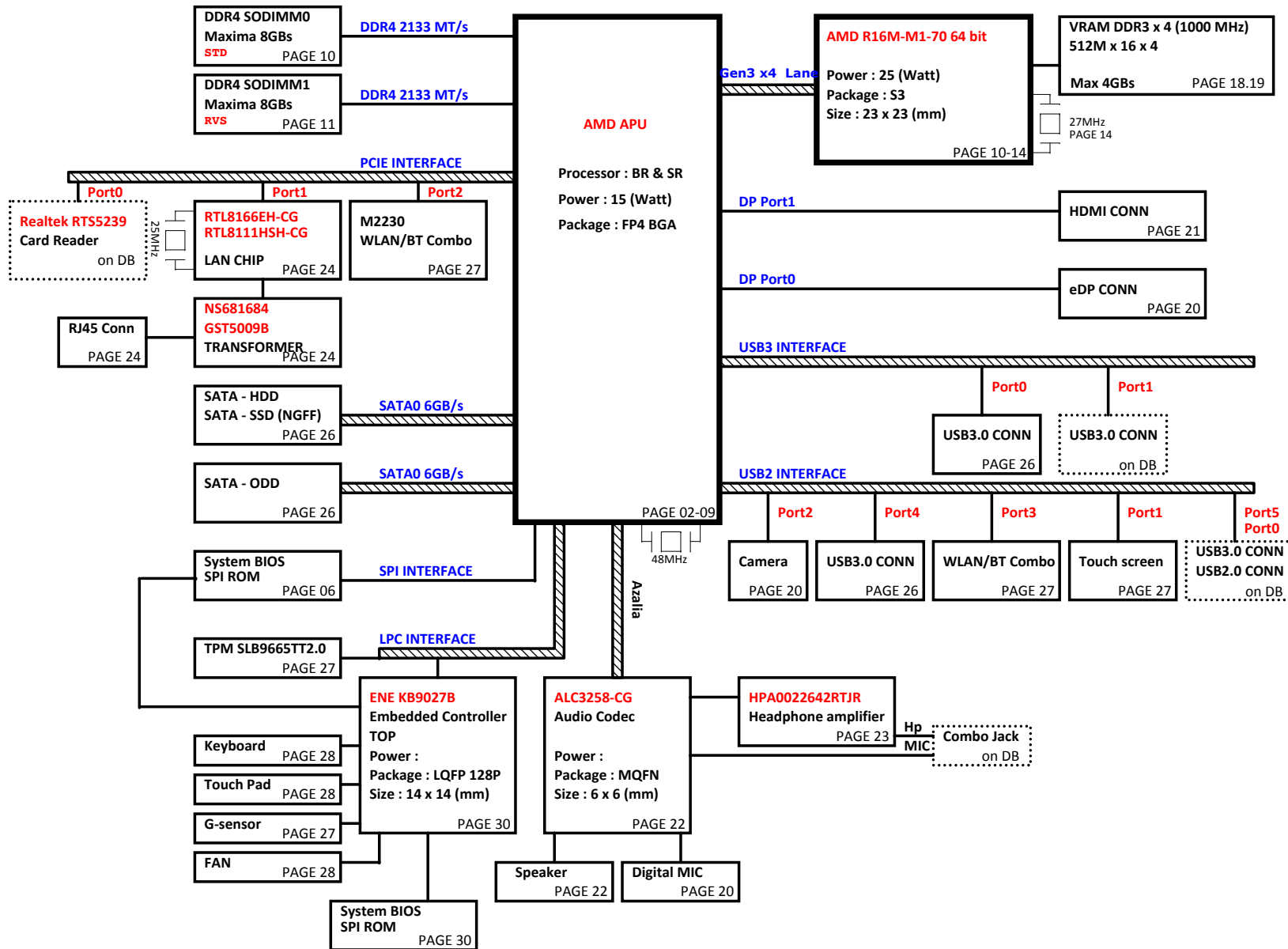


Dessert AMD BR & SR DIS/UMA 15.6"



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

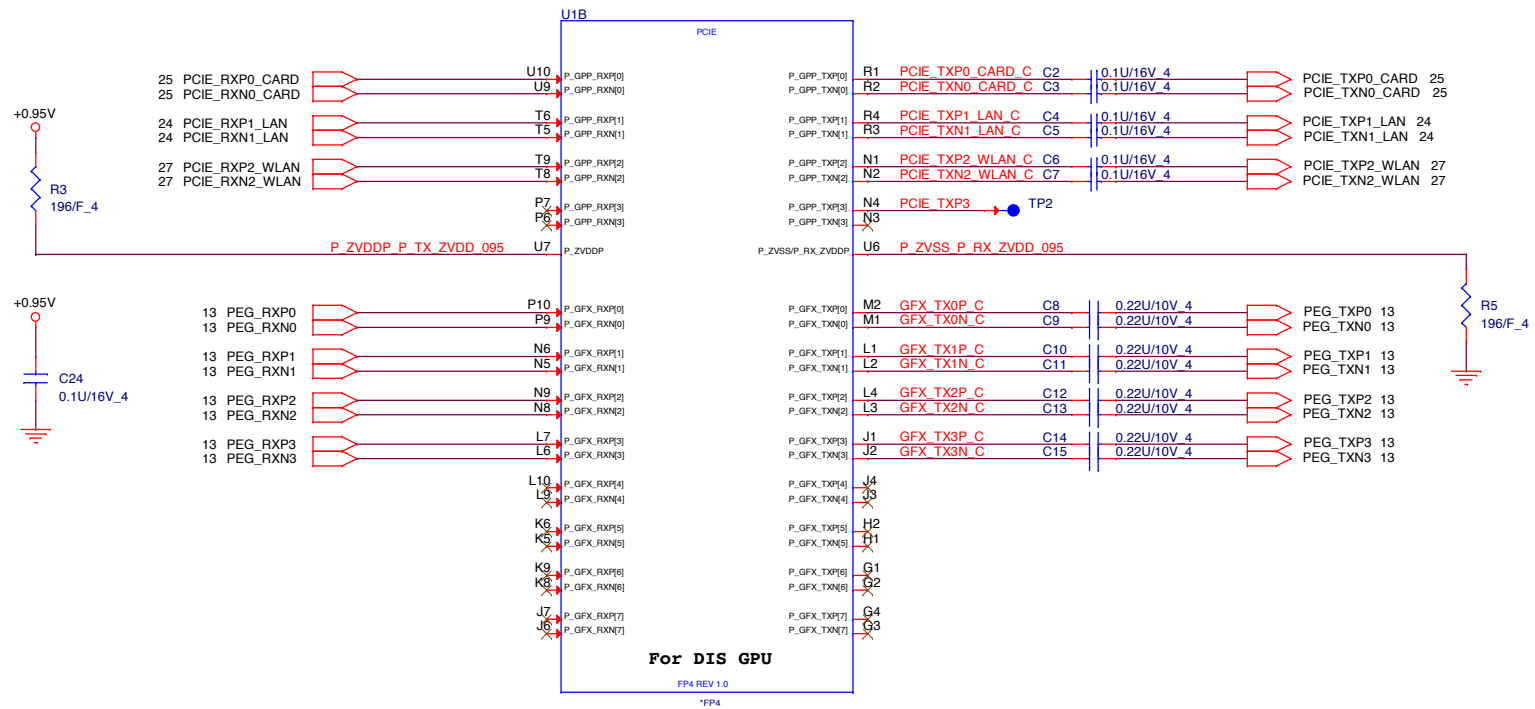
Power Source

ISL88750 System Charge Power (+BATCHG) PAGE 31
SY8208B/SY8286C System Power (+3VPCU/+5VPCU/+3VS5/+5VS5) PAGE 32
RT8231B System Memory Power (+1.2VSUS/+0.6V_DDR_VTT/+2.5VSUS) PAGE 33
APW8826/APW8826/G9336 Processor Power (+0.95VS5/1.5VS5/0.77VS5) PAGE 34
AO21267/RT8068AZQW Processor Power (+0.95V/+1.8VS5) PAGE 35
ISL62771 Processor Power (+VCC_CORE/+VDDNB_CORE) PAGE 36.37
ISL62771 Processor Power (+APU_VDDGFX) PAGE 38.39
APL3523A *3 System Power (+3/+3VLAVCC/+5V/+3VSUS/ +1.5V/+1.8V_ROM/+1.8V) PAGE 40
G5018 Processor Power (+VDDCR_FCH_S5) PAGE 41
RT3662EB/AO21236 DGPU Power (+VGA_CORE/+1.35V_VGA) PAGE 42~44
RT8068A/APL3523A DGPU Power (+0.95V_VGA/+3V_VGA/+1.8V_VGA) PAGE 45



PROJECT : G54A
Quanta Computer Inc.

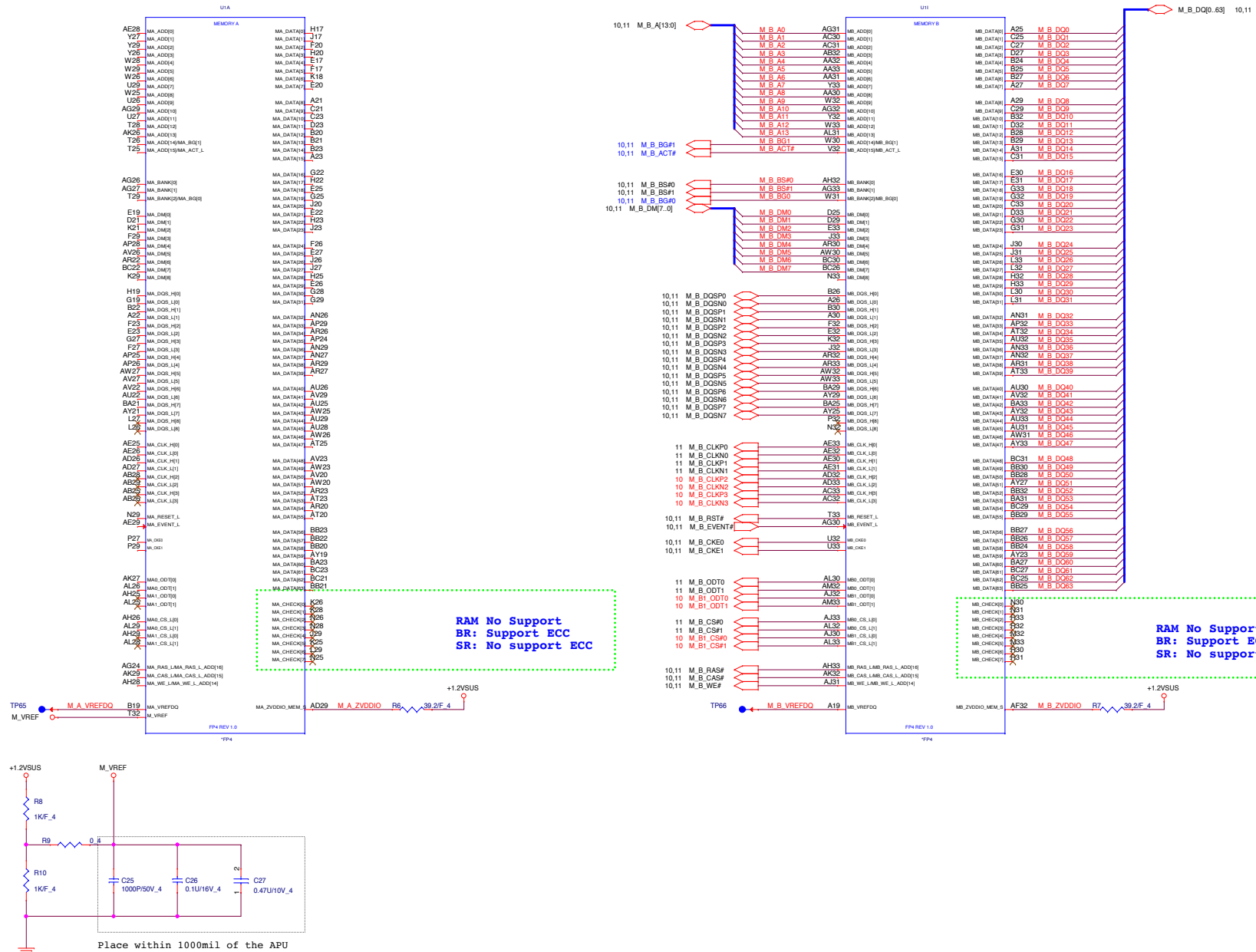
Size	Document Number	Rev
	Block Diagram	1A
Date: Monday, January 11, 2016	Sheet	1 of 46

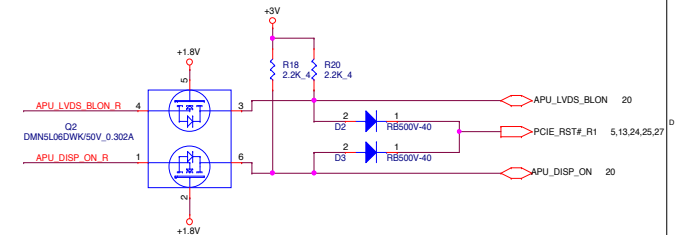
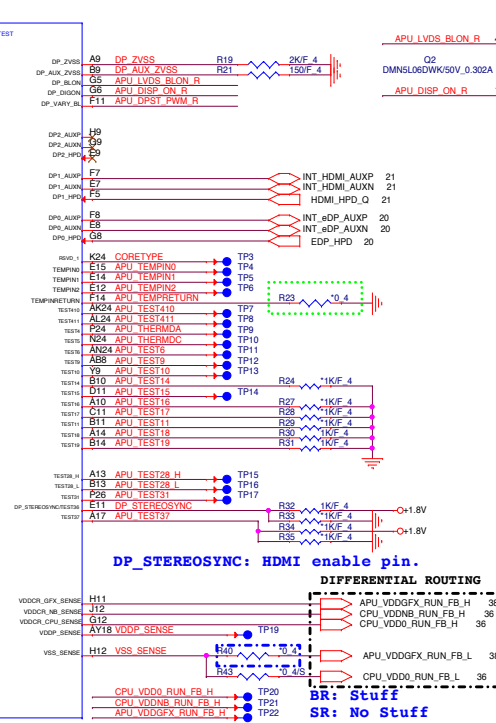
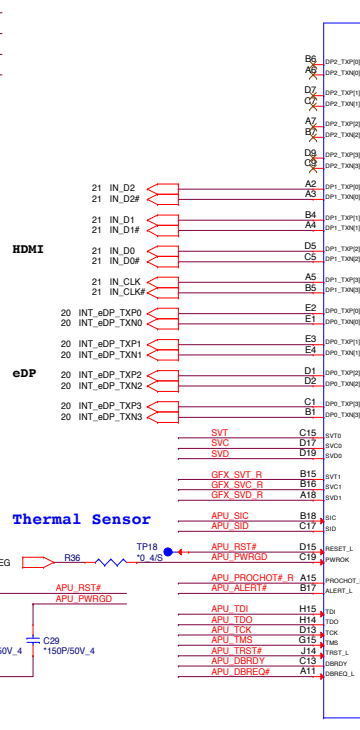
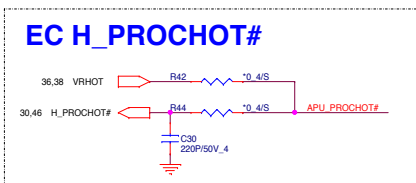
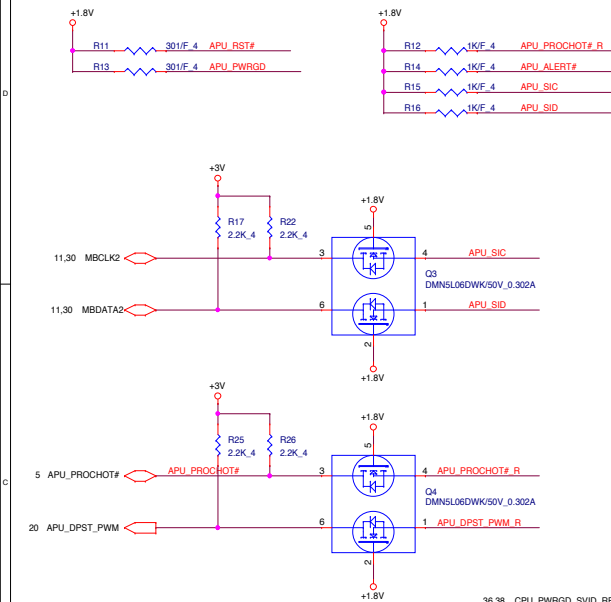


PROJECT : G54A
Quanta Computer Inc.

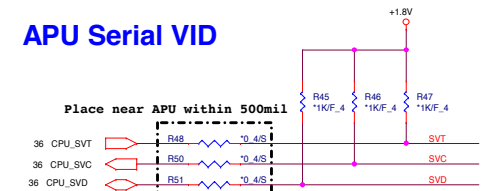
Size	Document Number	Rev
	BR & SR 1/7(PCIE)	1A
Date: Monday, January 11, 2016	Sheet 2 of 46	

SB only channel B



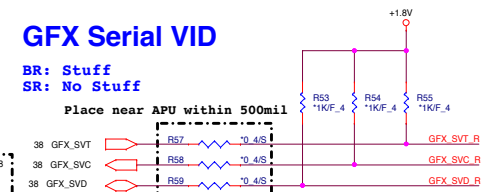


APU Serial VID



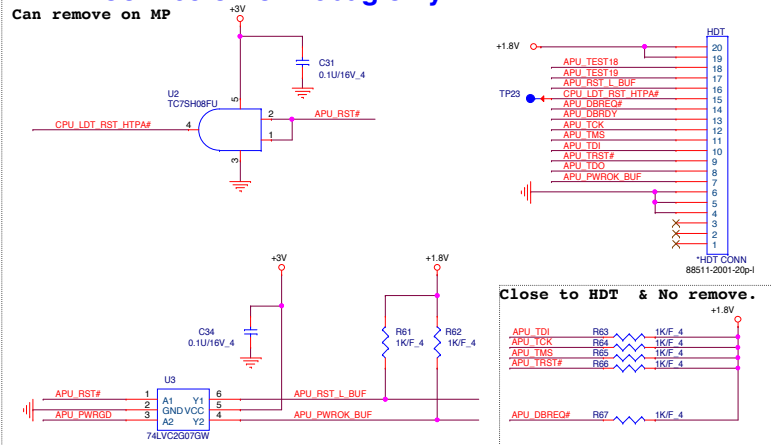
GFX Serial VID

```
BR: Stuff
SR: No Stuff
```

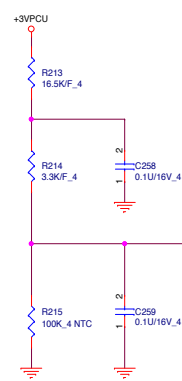


HDT+ Connector for Debug only

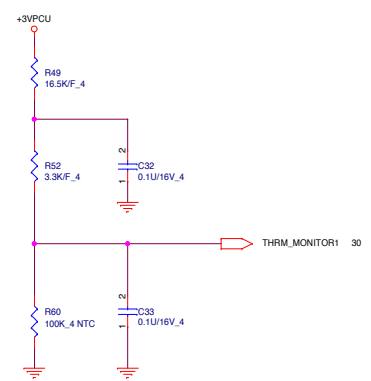
Can remove on MP

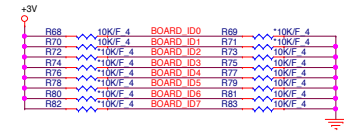
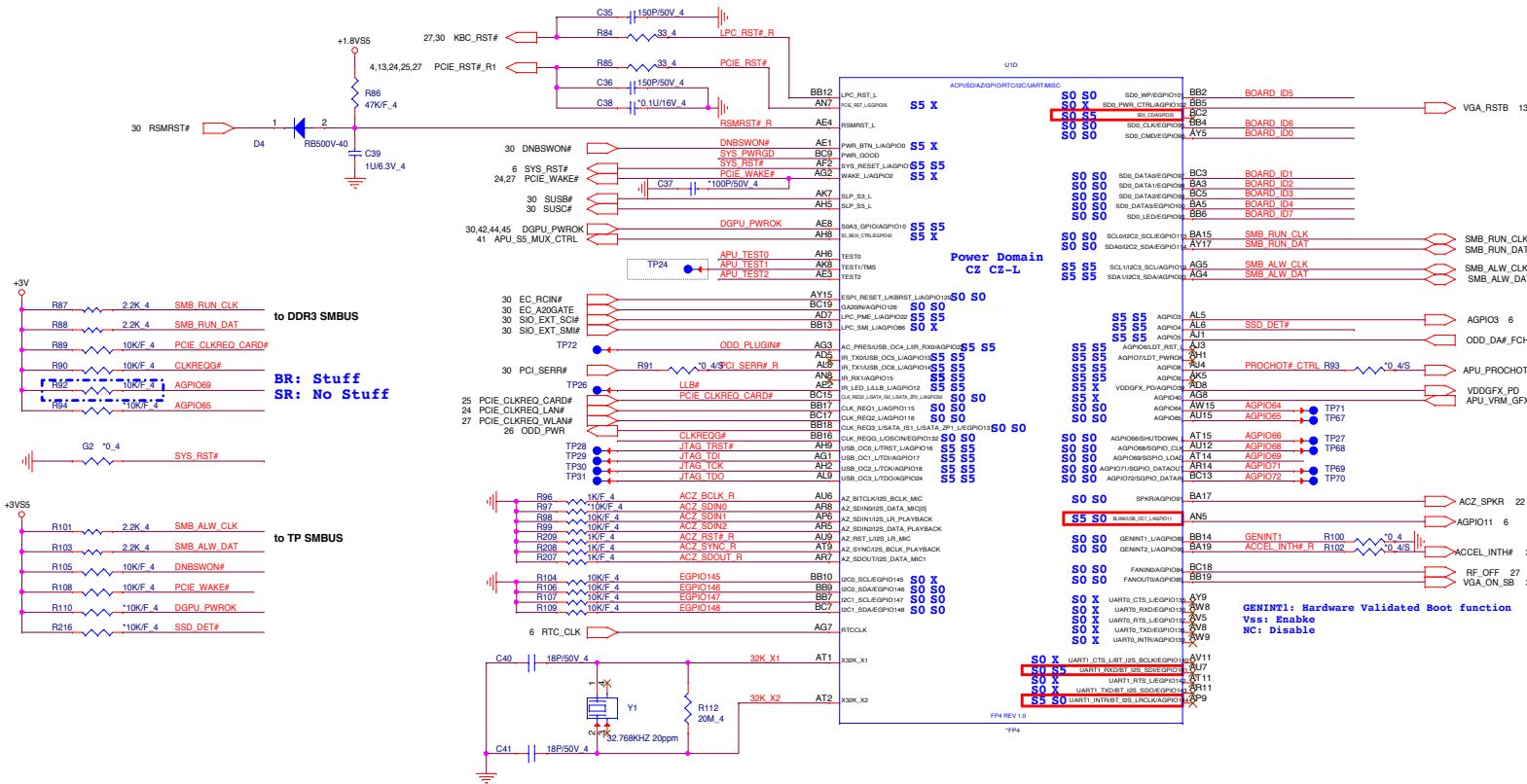


CPU Thermal Protect



Pipe Thermal Protect





BOARD ID SETTING

Board ID 0	Definition
0	UMA
1	DIS

Board ID [2:1]	Definition
00	14"
01	15"
10	17"
11	Reserve

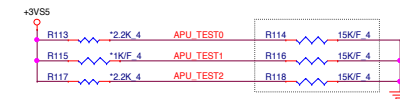
Board ID [4:3]	Definition
00	Pavilion
01	Reserve
10	Reserve
11	Reserve

Board ID [5]	Definition
0/1	BR/SR

Board ID [6]	Definition
0/1	Reserve

Board ID [7]	Definition
0/1	Reserve

Follow AMD checklist 53537_1_09 suggestion.

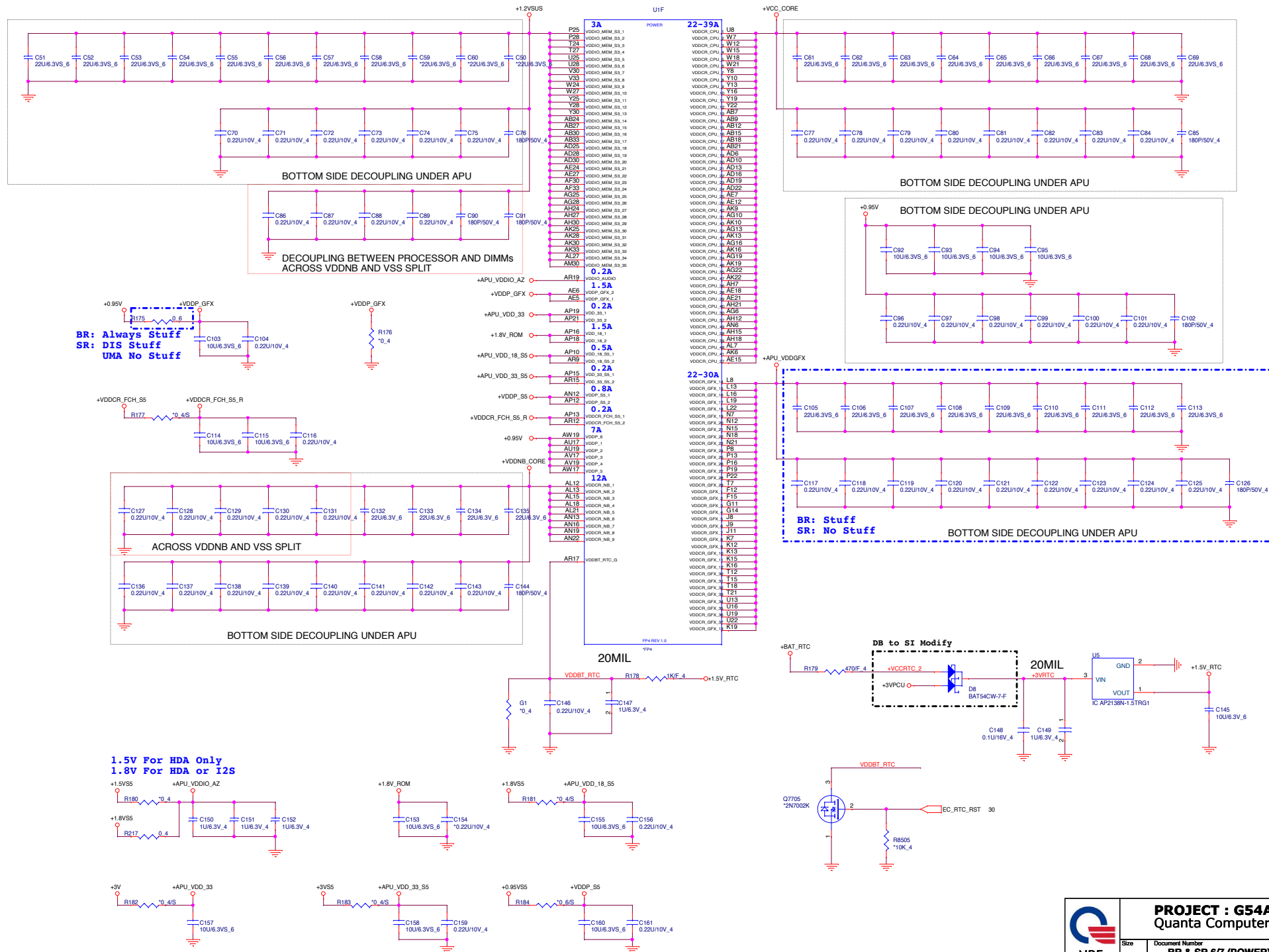


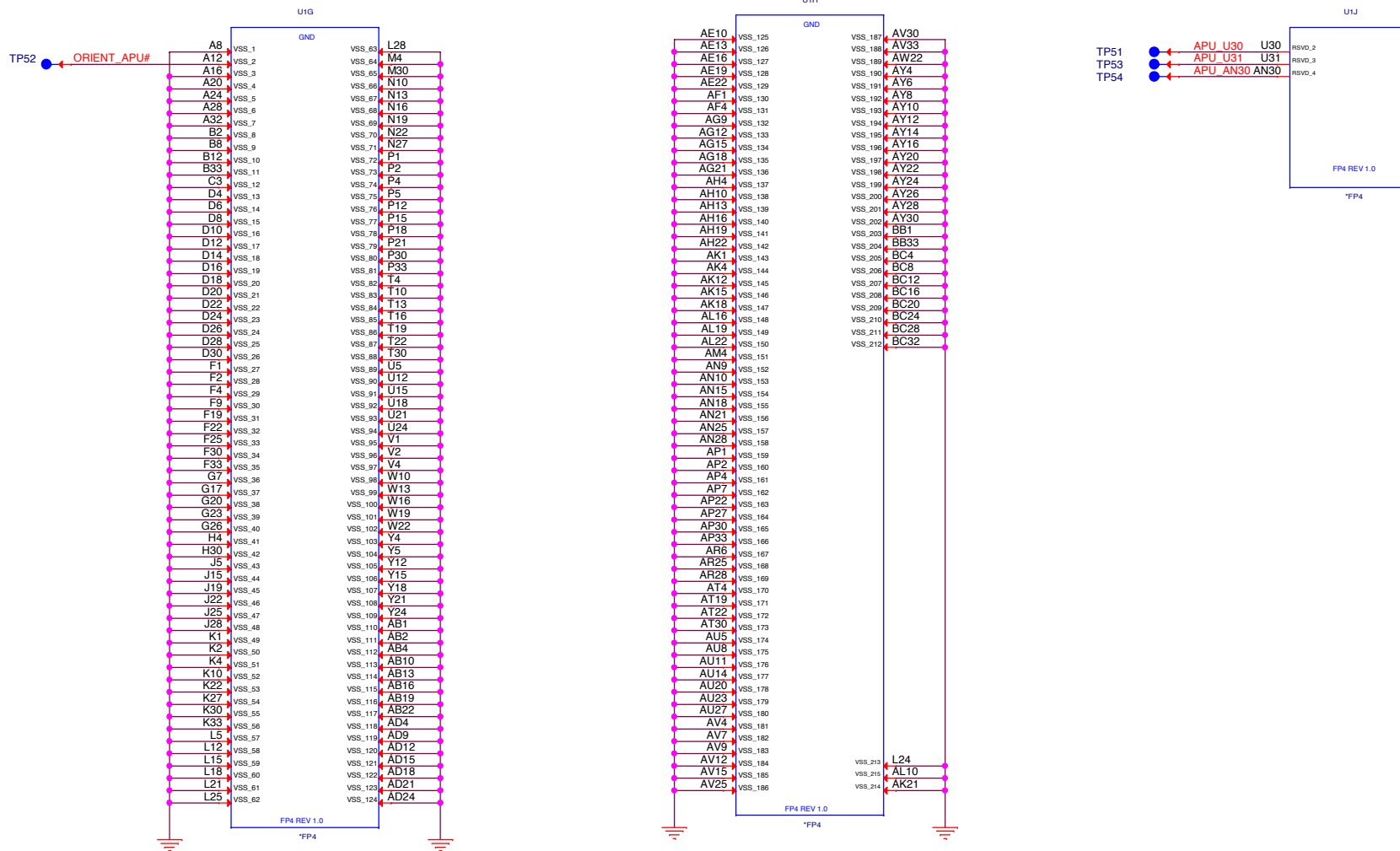
TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



PROJECT : G54A
Quanta Computer Inc.

Size Document Number
BR & SR 47(GPIO/AZ/UART) Rev 1A
Date: Monday, January 11, 2016 Sheet 5 of 46






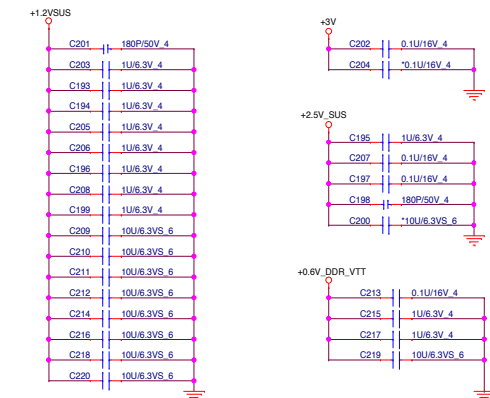
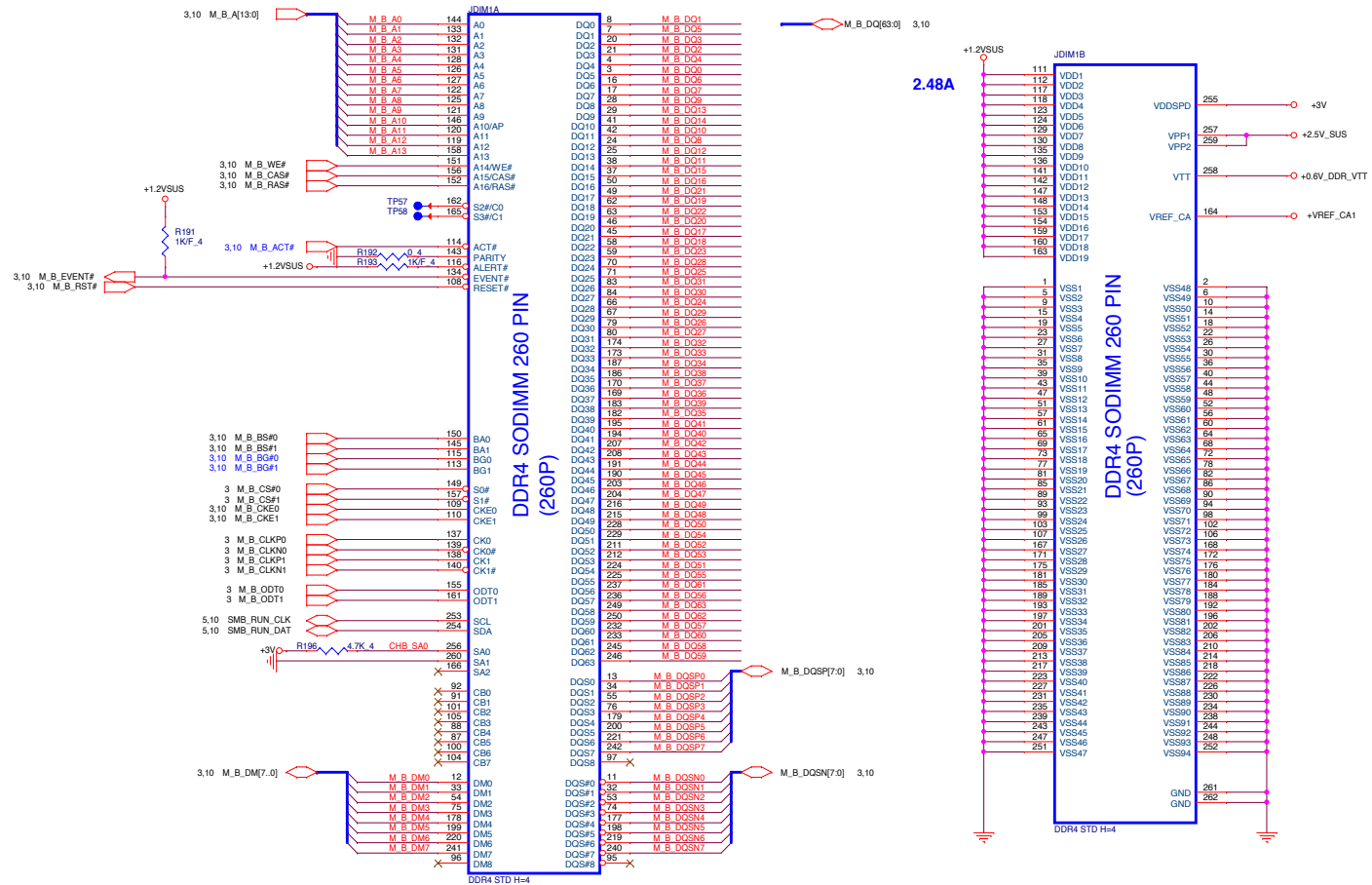
PROJECT : G54A
Quanta Computer Inc.

Size	Document Number	Rev
	BR & SR 7/7 (GND)	1A
Date: Monday, January 11, 2016		Sheet 8 of 46

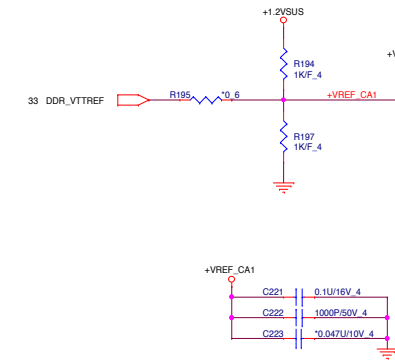
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	PROJECT : G54A Quanta Computer Inc.		
	Size A	Document Number Reserved	Rev 1A
	Date: Monday, January 11, 2016 Sheet 9 of 46		

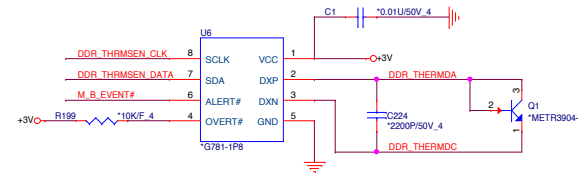
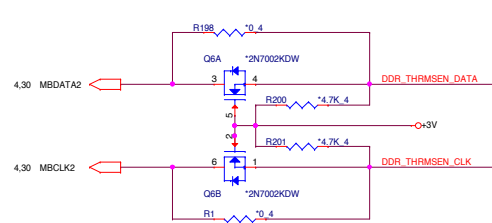
Place these Caps near SODIMM



1uF/10uF 4pcs on each side of SODIMM



Local Thermal Sensor




Main:AL000781039	G781-1P8(9Ah)
2nd:AL001412005	EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003	EMC1412-1-ACZL-TR(98h)
2nd:AL000431014	TMP431ADGKR(98h)

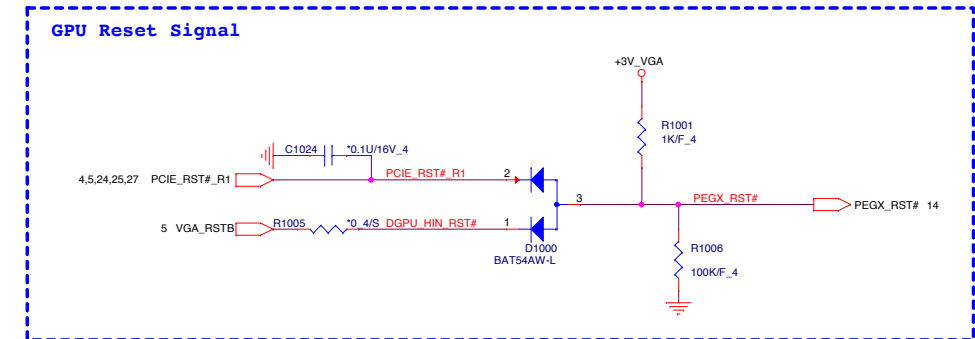
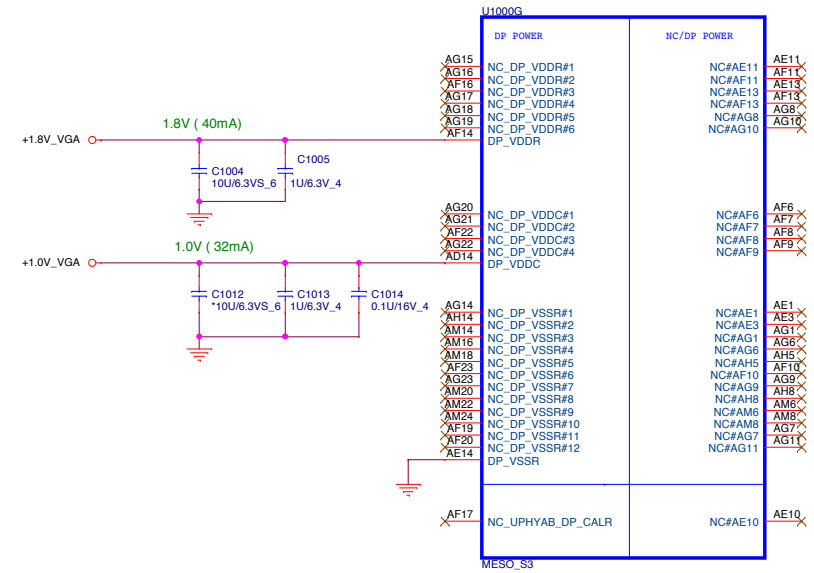
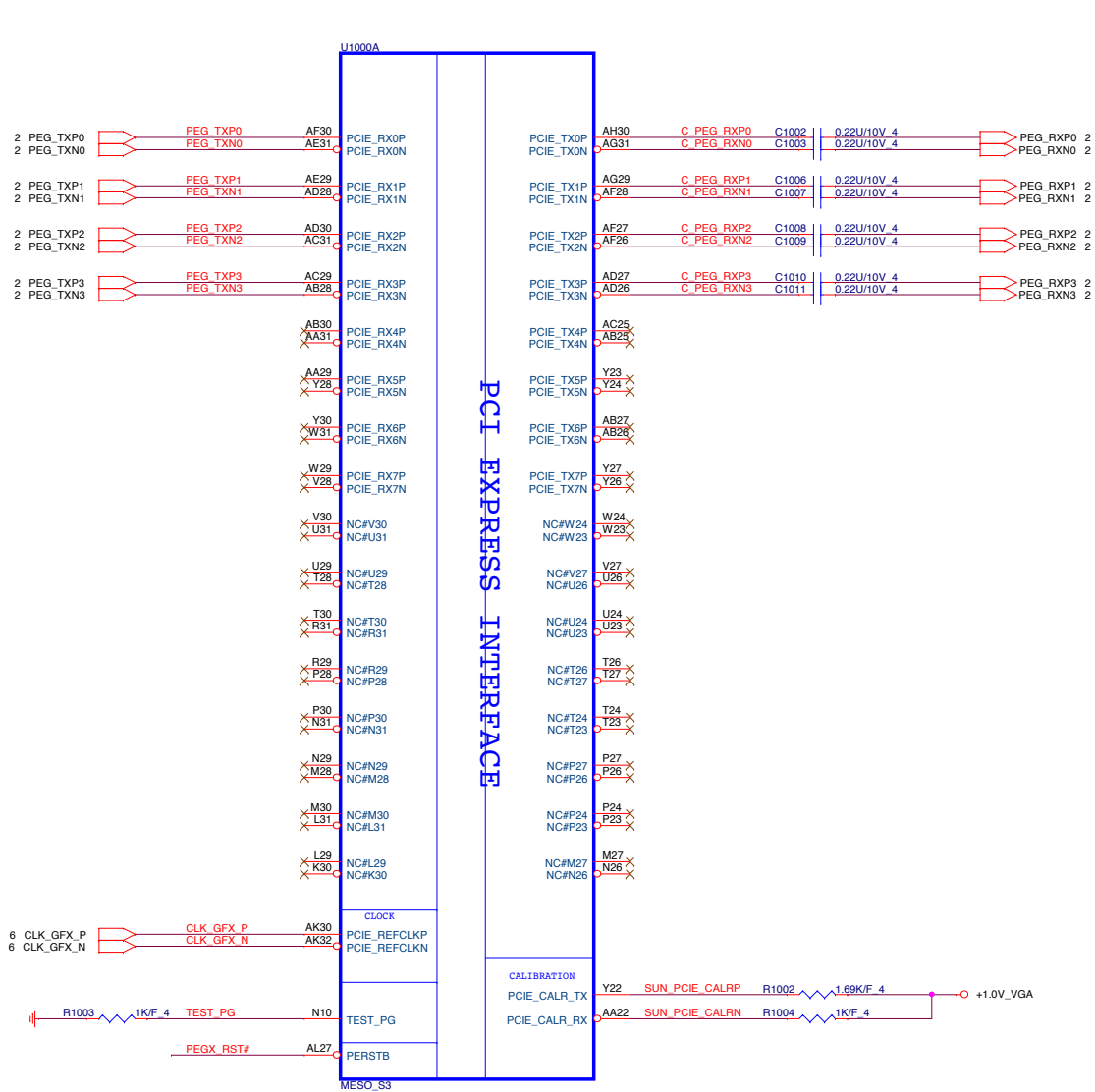


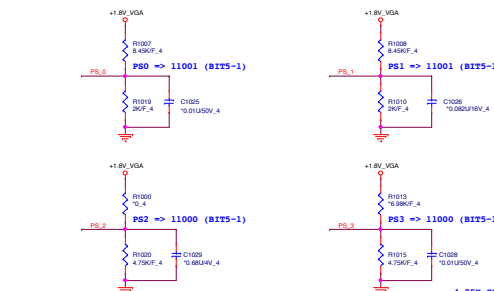
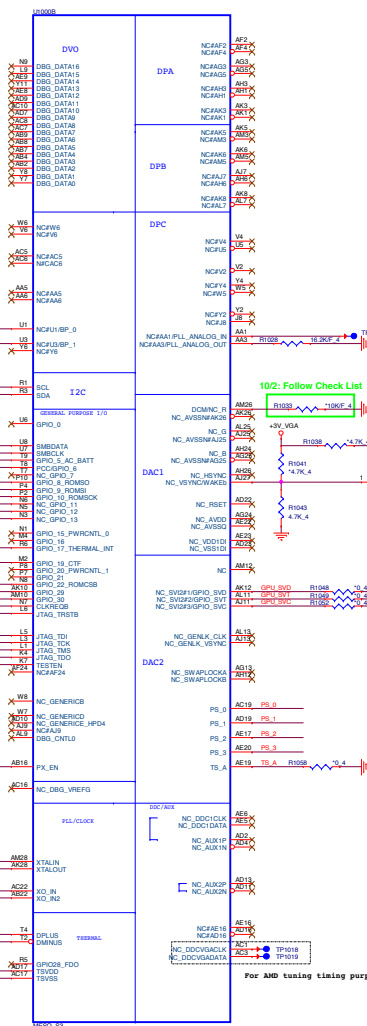
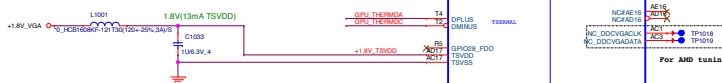
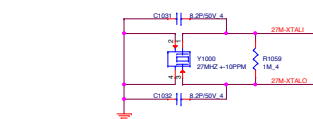
PROJECT : T15-BA
Quanta Computer Inc.

Size C	Document Number CHB DDR4 DIMM1-STD(4.0H)	Rev 1A
Date: Monday, January 11, 2016		Sheet 11 of 46

<Reserved for CHB – DIMM2>

 NB5	PROJECT : G54A Quanta Computer Inc.		
	Size A	Document Number CHB DDR4 DIMM2-RVS(4.0H)	Rev 1A
	Date: Monday, January 11, 2016		Sheet 12 of 46



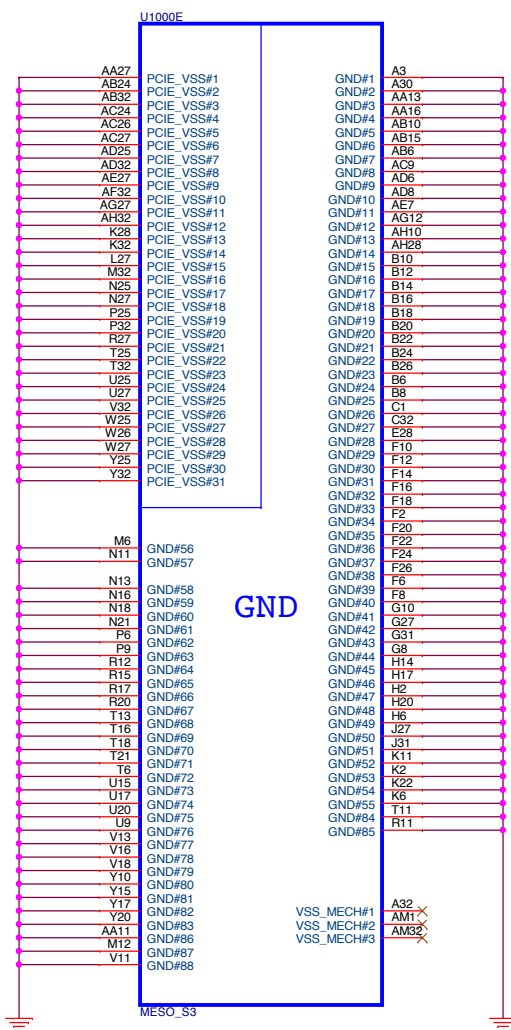


PS_3[3:1]	Vendor	Type	Vendor P/N	FU	PD
000	Micron (DDP)	512Mb16 *4, 1000MHz	H7413512H168A-1070A	HC	4.758
001	Hyunix (DDP)	512Mb16 *4, 1000MHz	HSTC806JCH-11C	8.45K	2.009
010	Hyunix	256Mb16 *4, 900MHz	HSTC4663FR-N0C	4.53K	2.009
011	Micron	512Mb16 *4, 900MHz	H741J256M16L7-0919N	6.98K	4.99K
100	Samsung	256Mb16 *4, 900MHz	K4M4G1646C-BA1E	4.53K	4.99K
101					

Table 3-24 Primary Memory Aperture Sizes Requested at PCI Configuration

Size of the Primary Memory Apertures	ROM_CONFIG2
128 MB	000
256 MB	001
64 MB	010
Reserved	011
512 MB	Not Supported
1 GB	Not Supported
2 GB	Not Supported
4 GB	Not Supported

PSP ID	Strap Name	Description	Recommended Settings
PS_003	RON_CONF001	If STRAP_RON_EN = 1, RION_CONF001 will format the RION.	Design dependent; see the description.
PS_004	RON_CONF011	Reserved for internal use only.	1
PS_006	N/A	Must be 1 at reset.	1
PS_008	N/A	Reserved.	1
PS_103	STRAP_BUF_GEN_EN_A	PCIE GEN3 capability. • PCIE GEN3 is supported. • PCIE GEN3 is not supported. Disconnection whether or not the PCIe configuration space management capability is reported in the PCIe configuration space management feature as CLEAREP.	Design dependent; see description.
PS_104	STRAP_BUF_CLK_PEN	0 • The CLKREQ power management capability is disabled. 1 • The CLKREQ power management capability is enabled.	0
PS_109	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_114	STRAP_TX_CTL_DRV_RST_OVERRIDE	0 • The transmitter full-half swing mode. 1 • The transmitter half-swing is enabled.	1
PS_120	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 • Tx de-emphasis disabled. 1 • Tx de-emphasis enabled.	Design dependent; see the description.
PS_211	N/A	Reserved.	0
PS_212	N/A	Reserved.	0
PS_220	STRAP_R0N_EN	To enable the external R0N device. 0 • Disable the external R0N device. 1 • Enable the external R0N device.	Design dependent; see the description.
PS_240	N/A	Reserved.	0
PS_242	N/A	Reserved.	0
PS_303	BOARD_CONFIG01	Board configuration related information such as board type.	Design dependent; see the description.
PS_304	BOARD_CONFIG02	Reserved.	0
PS_305	N/A	Reserved.	0



CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
 0= DO NOT INSTALL RESISTOR
 1 = INSTALL 3K RESISTOR
 X = DESIGN DEPENDANT
 NA = NOT APPLICABLE

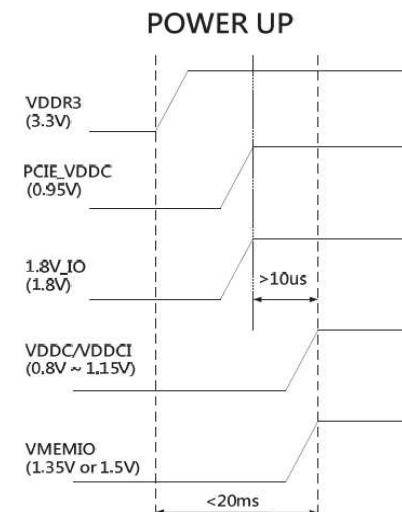
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

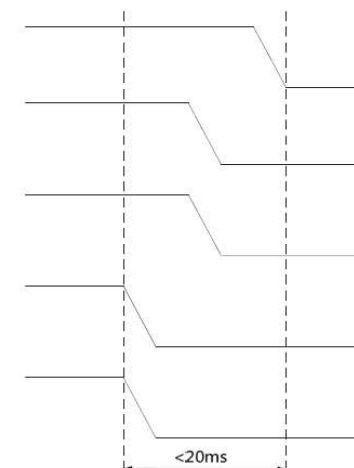
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE

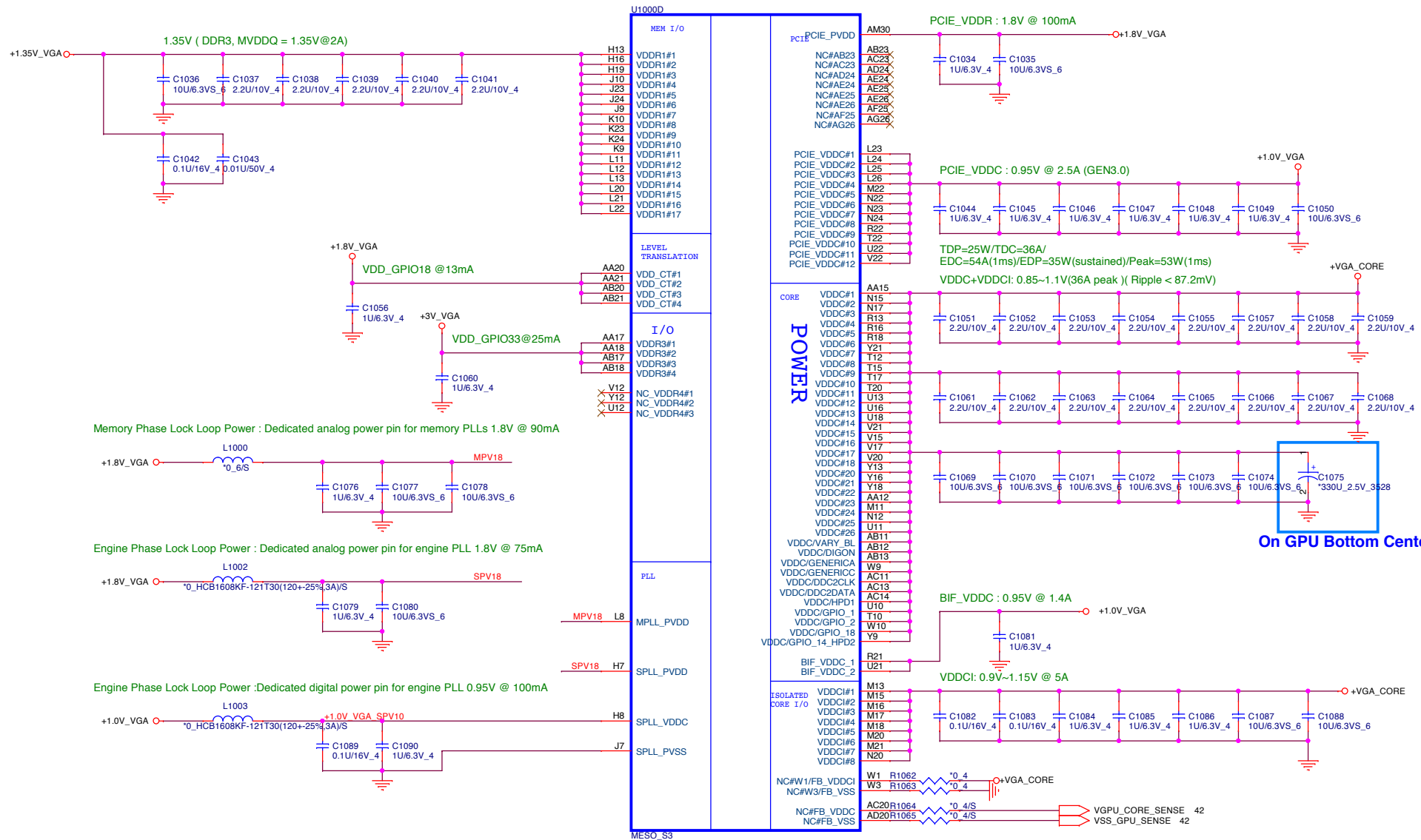


POWER DOWN



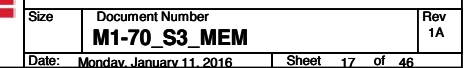
PROJECT : G54A
 Quanta Computer Inc.

Size	Document Number	Rev
	M1-70_S3_GND/LVDS/Strap	1A
Date:	Monday, January 11, 2016	Sheet 15 of 46

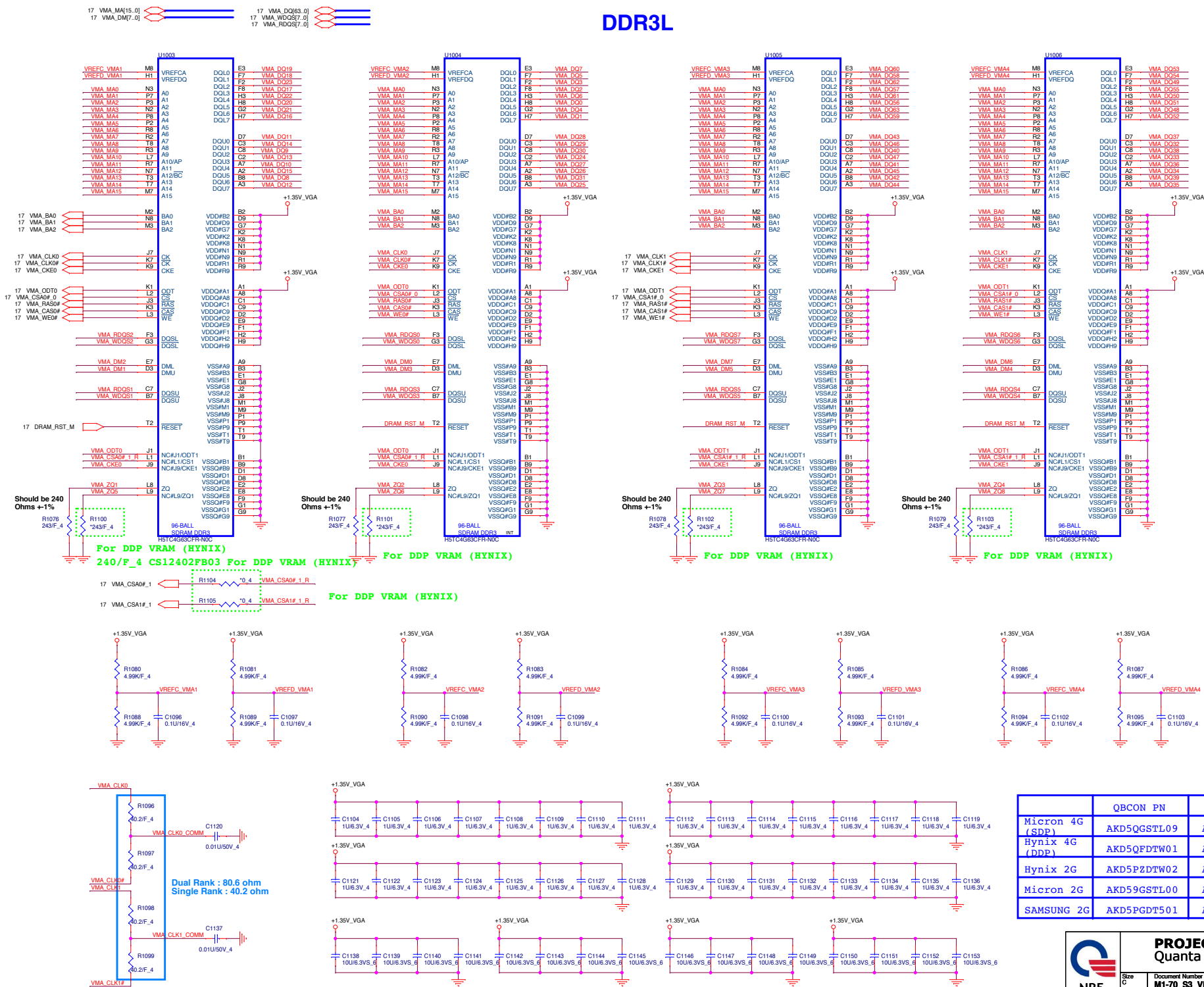


PROJECT : G54A
Quanta Computer Inc.

Size	Document Number	Rev
	M1-70_S3_POWER	1A
Date:	Monday, January 11, 2016	Sheet 16 of 46




DDR3L

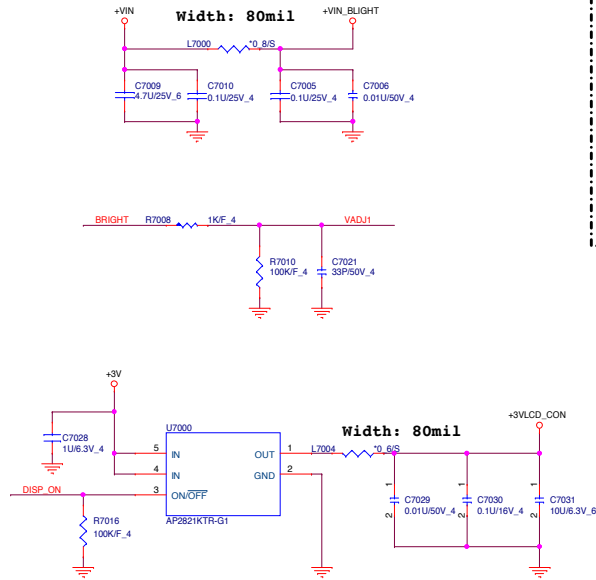
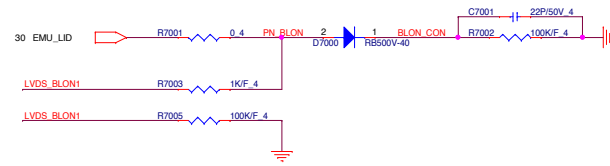


	QBCON PN	TOP BSQ
Micron 4G (SDD)	AKD5QGSTL09	AKD5QGSTL05
Hynix 4G (DDE)	AKD5QFTDW01	AKD5QFTDW00
Hynix 2G	AKD5PZDTW02	AKD5PZDTW01
Micron 2G	AKD59GSTL00	AKD59GSTL01
SAMSUNG 2G	AKD5PGDT501	AKD5PGDT500

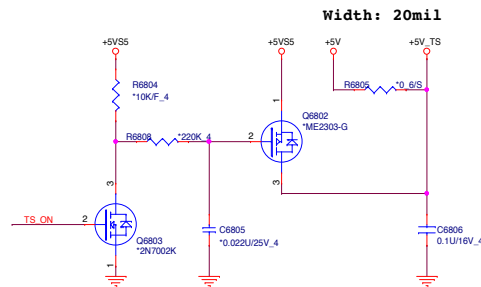
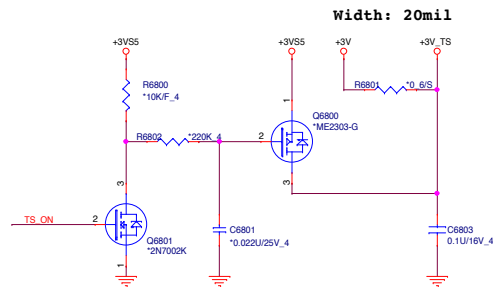
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	PROJECT : G54A Quanta Computer Inc.		
	Size A	Document Number Reserved	Rev 1A
	Date: Monday, January 11, 2016		Sheet 19 of 46

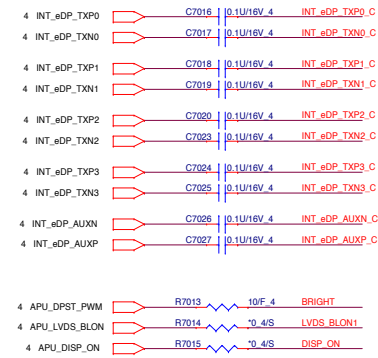
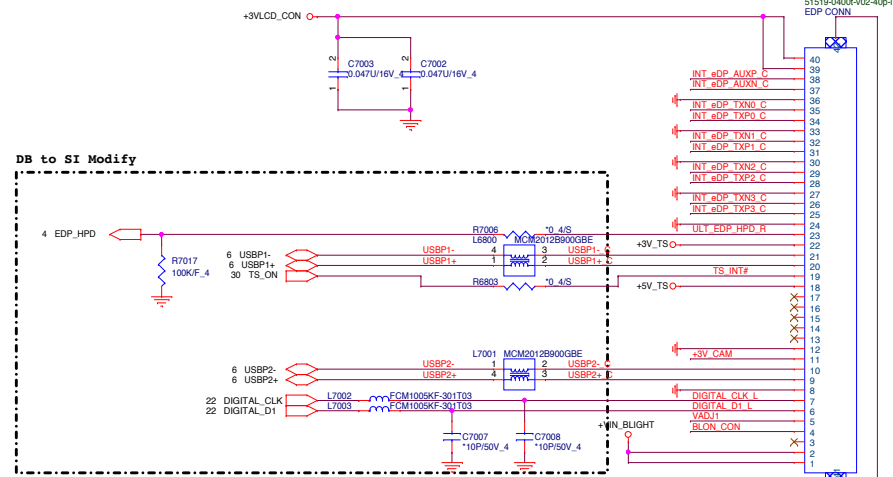
LID Switch



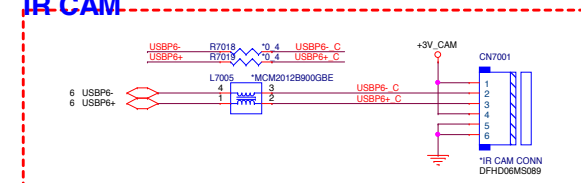
Touch screen

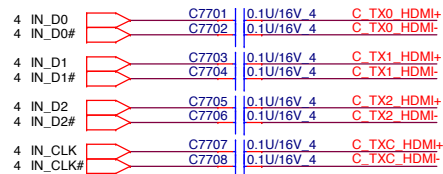


eDP CONN.

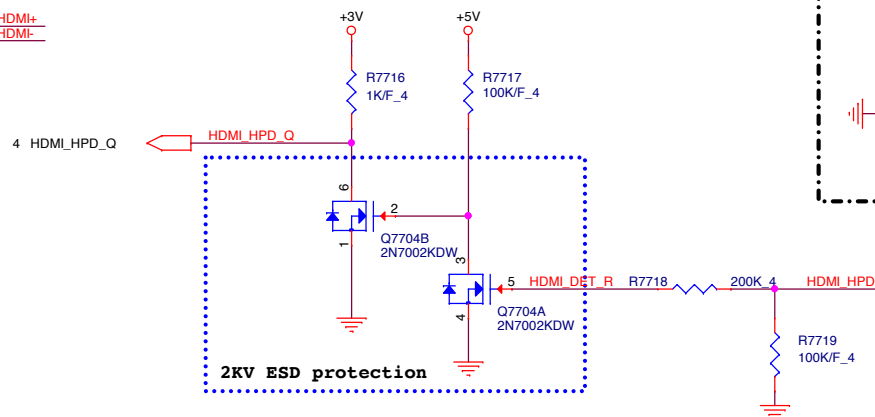
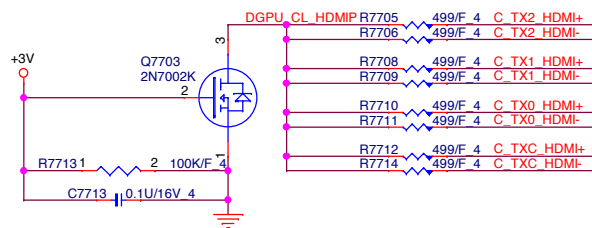
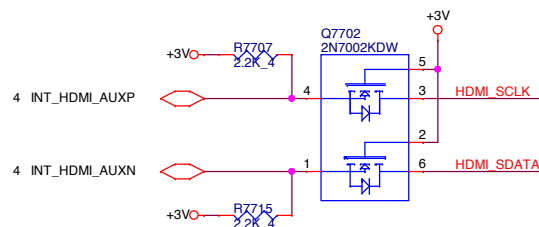


IR CAM



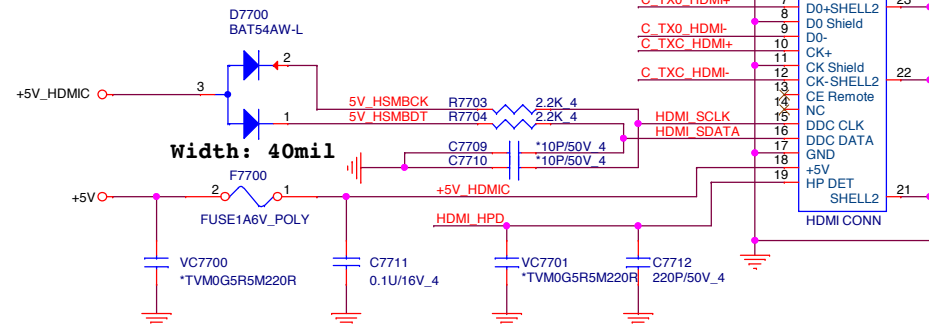


HDMI SMBus Isolation

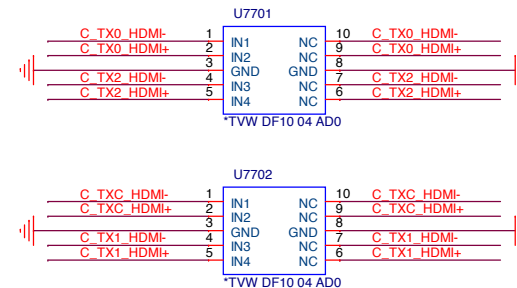


DB to SI Modify

For EMI

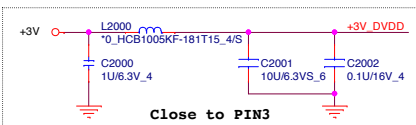


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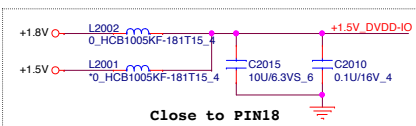


PROJECT : G54A
Quanta Computer Inc.

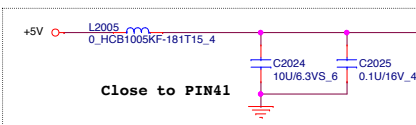
Size B	Document Number HDMI CONN	Rev 1A
Date: Monday, January 11, 2016	Sheet 21 of 46	



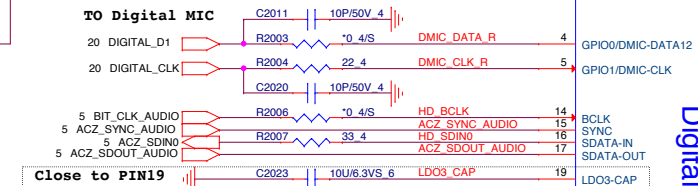
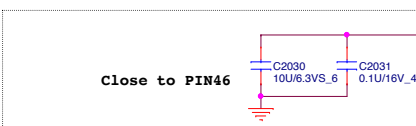
30mA



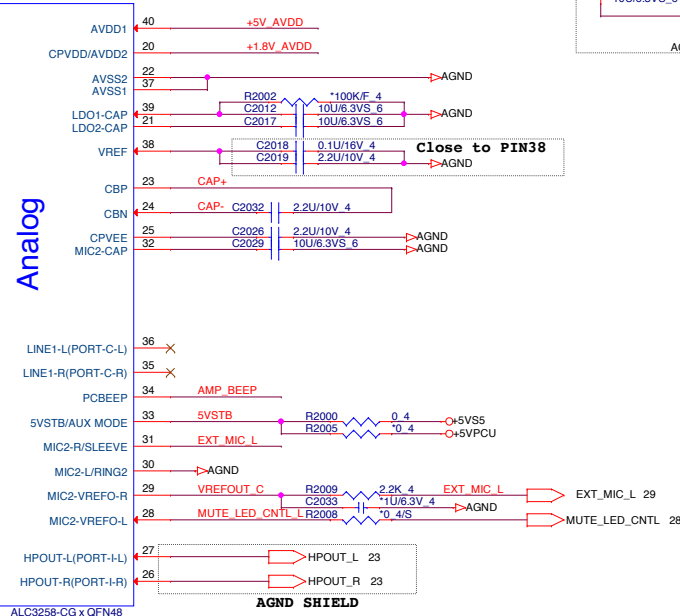
10mA



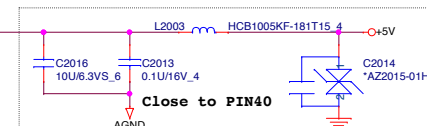
1000mA



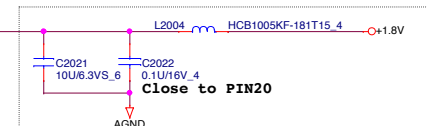
Analog



30mA

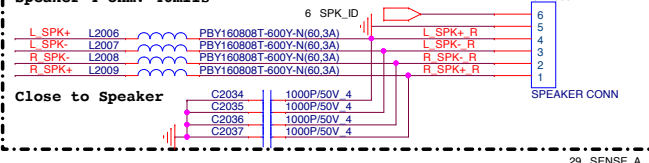


250mA

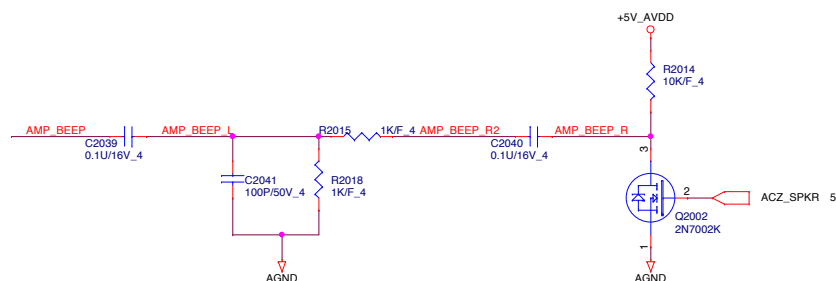
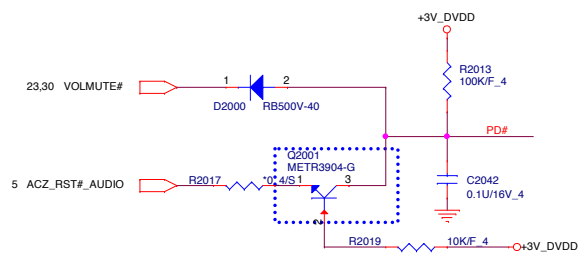


DB to SI Modify

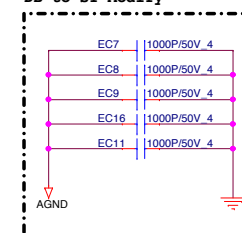
Speaker 4 ohm: 40mils



Speaker 4 ohm: 40mils



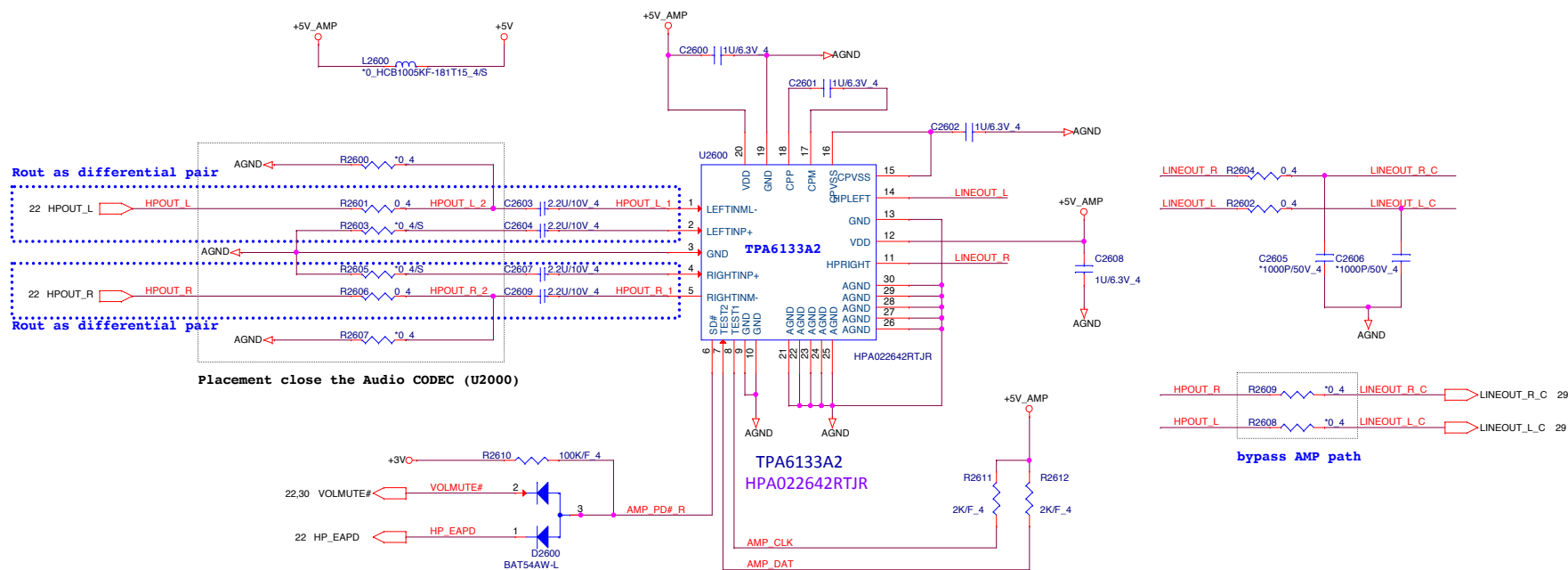
DB to SI Modify



place to near or under codec



Head Phone Out

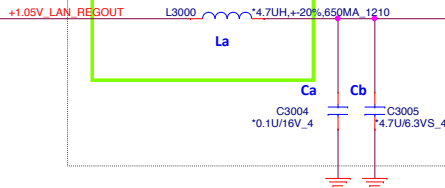


For SWR mode support RTL8111HSH

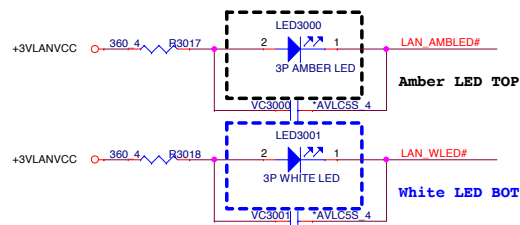
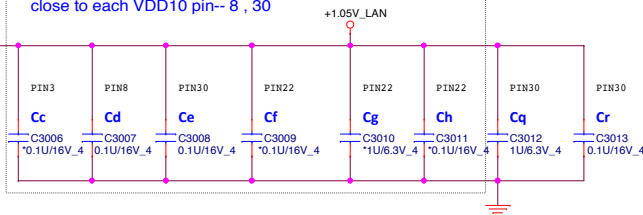
Stuff La, Ca ,Cb
For LDO mode support RTL8166EH
NA : La, Ca, Cb

SI change to 0 ohm

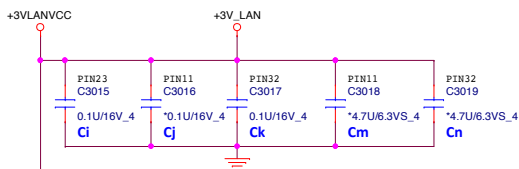
Power trace Layout 寬度 >60 mil



- * Place Cc,Cd,Ce,Cf for RTL8111H(S)
close to each VDD10 pin-- 3, 22, 8, 30
- * Place Cg,Ch for RTL8111H(S)
close to each VDD10 pin-- 22(reserved)
- * Place Cq,Cr for RTL8166EH
close to each VDD10 pin-- 30(reserved)
- * Place Ce,Cd for RTL8166EH
close to each VDD10 pin-- 8, 30



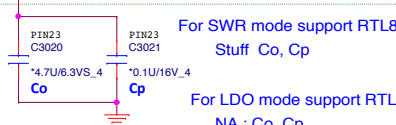
- * Place Ci and Ck, close to each VDD33 pin-- 23, 32 for RTL8166EH
- * Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8111H(S)
- * For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)



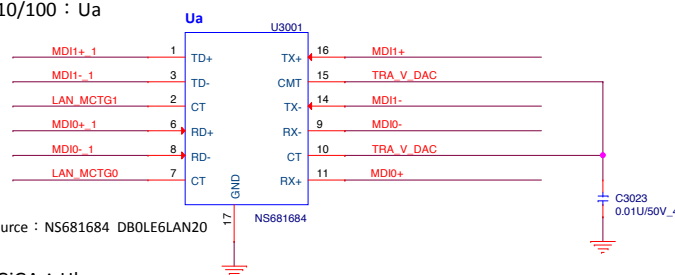
For SWR mode support RTL8111HS
Stuff Co, Cp

5V_4

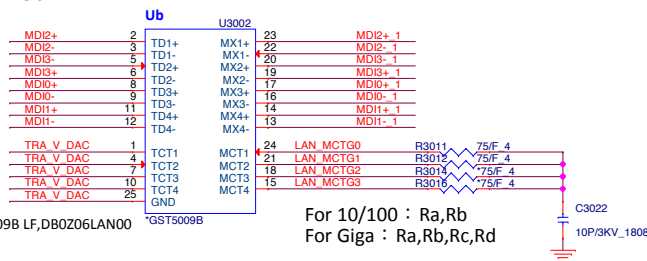
For LDO mode support RTL8166EH
NA : Co, Cp



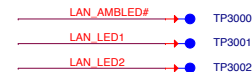
For 10/100 : Ua



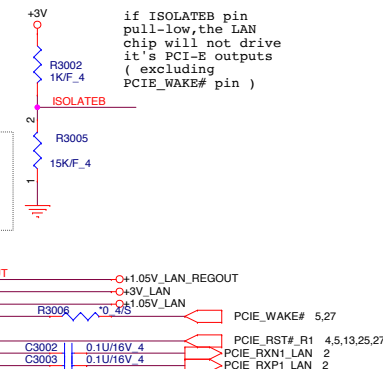
For GiGA : Ub



For 10/100 : Ra,Rb
For Giga : Ra,Rb,Rc,Rd



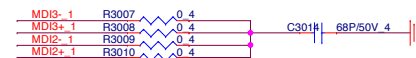
```
if ISOLATED pin
pull-low, the LAN
chip will not drive
it's PCI-E outputs
( excluding
PCIE_WAKE# pin )
```



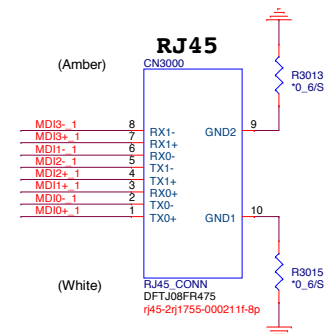
For GbE
* Place RTL8111HSH-CG

For 10/100
* Place RTL8166EH-CG

For 10/100 stuff only Close RJ45

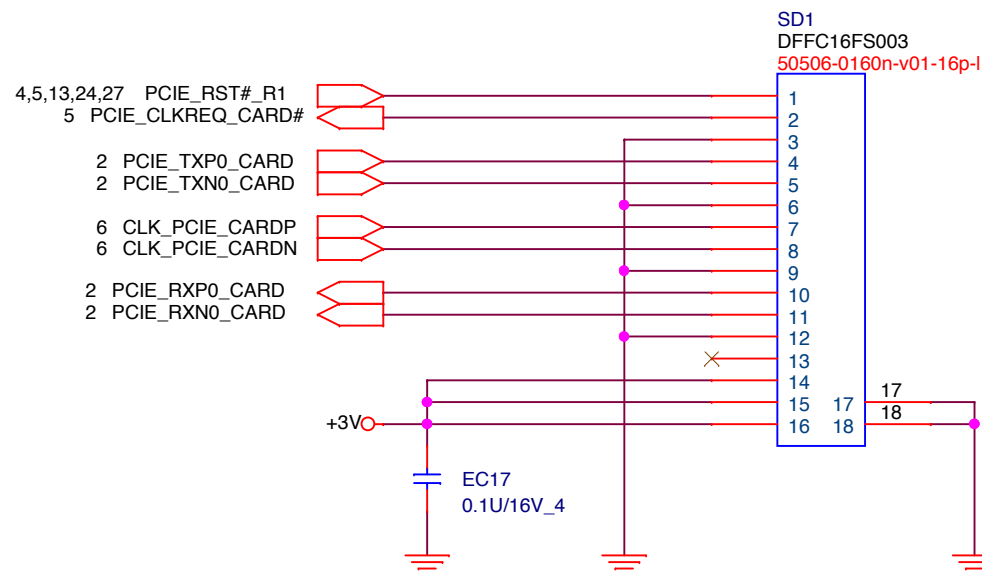


RJ45
(Amber) CN3000

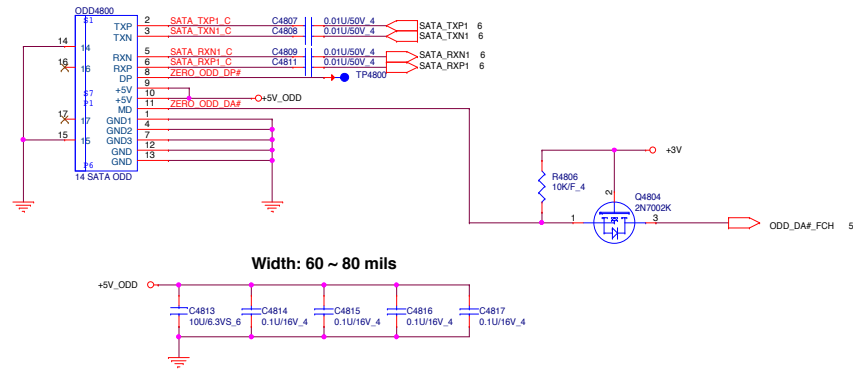


PROJECT : G54A
Quanta Computer Inc.

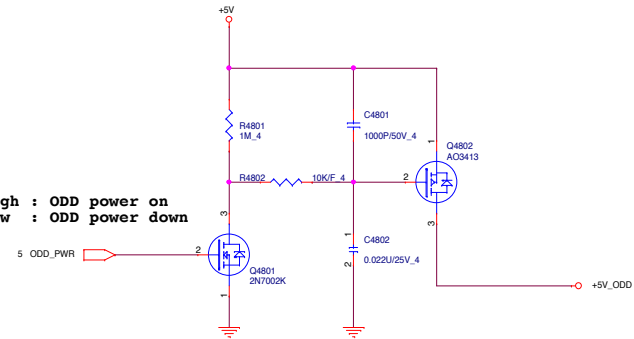
Size Custom	Document Number LAN RTL8166EH-CG/RJ45	Rev 1A
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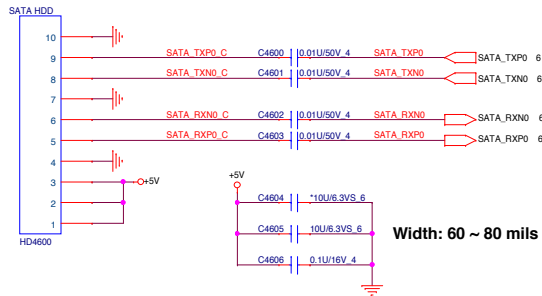
SATA ODD



High : ODD power on
Low : ODD power down

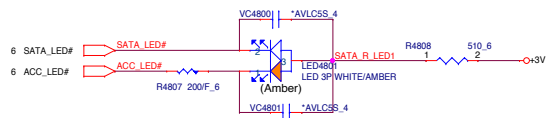


SATA HDD

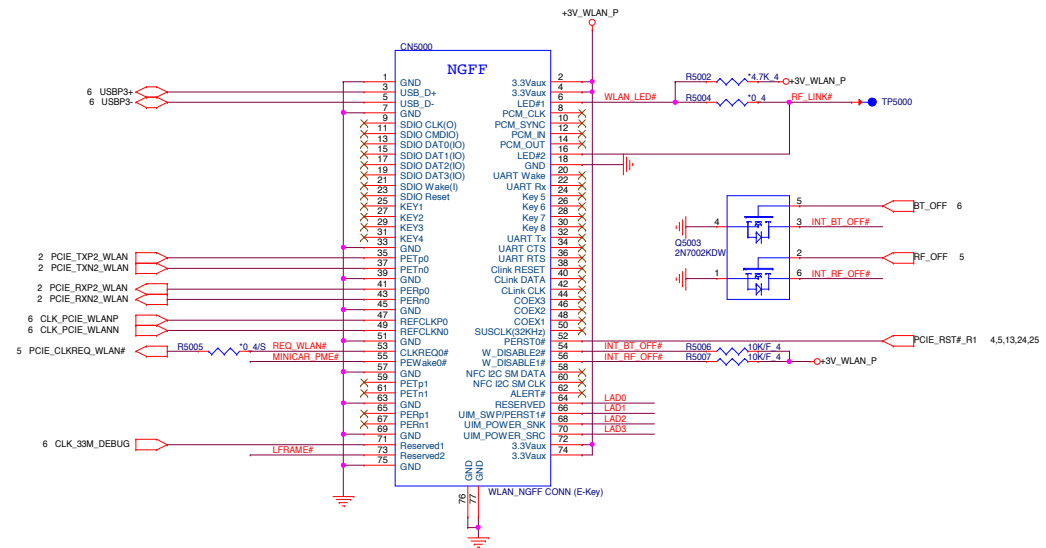
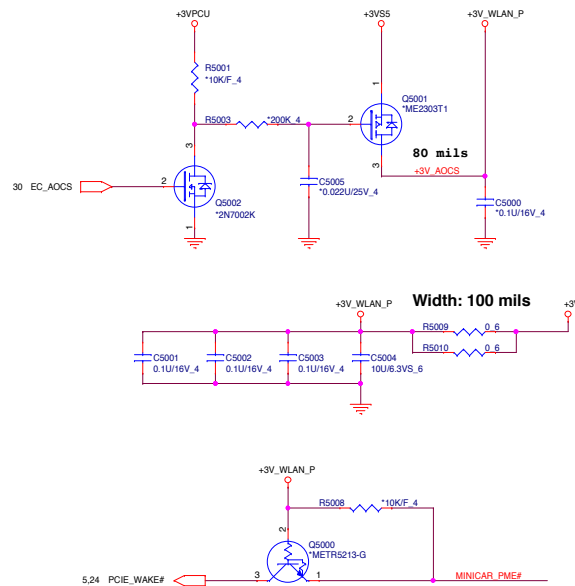
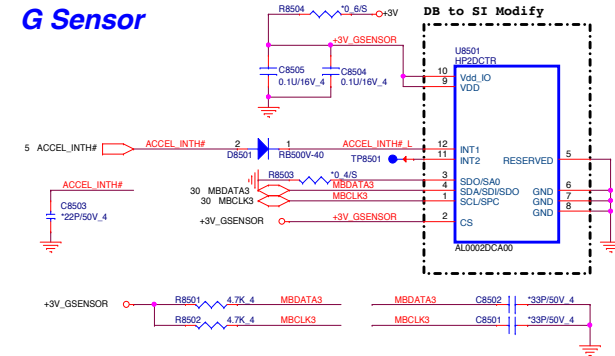
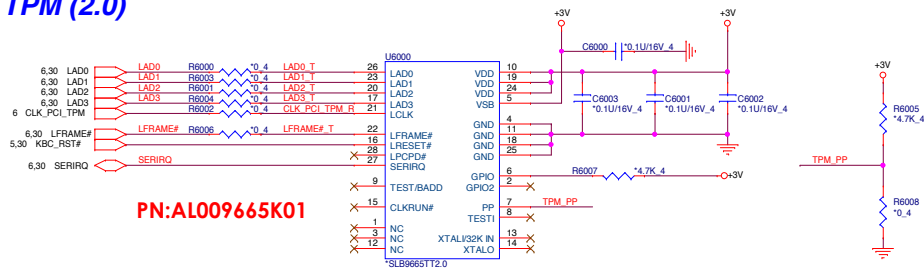


SATA SSD

SATA LED

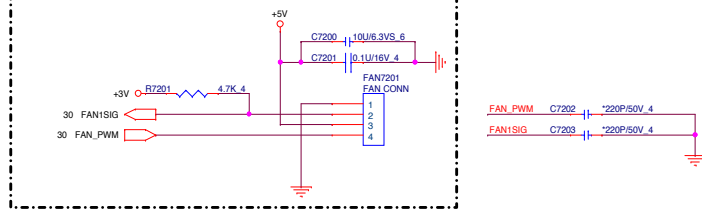


G Sensor

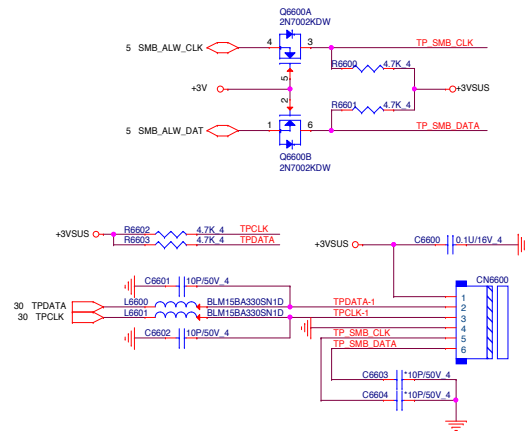


DB to SI Modify

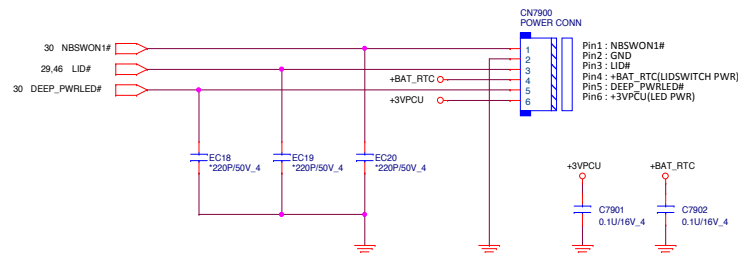
FAN CONN.



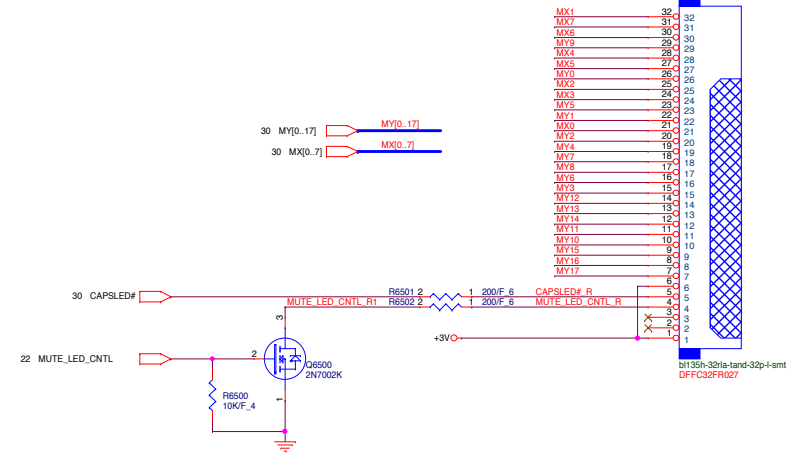
Touch Pad CONN.



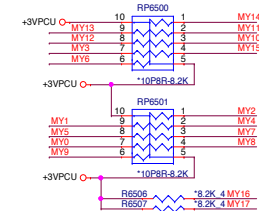
POWER BOARD CONN.



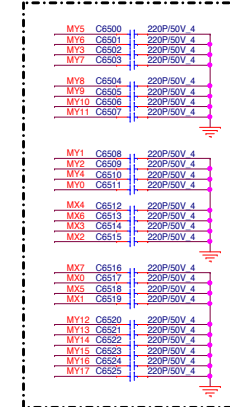
KB CONN.



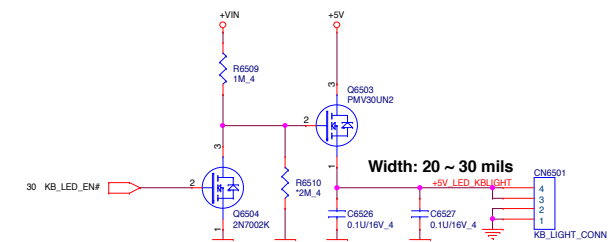
KEYBOARD PULL-UP



DB to SI Modify



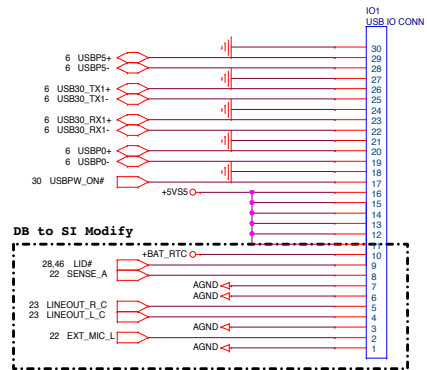
KB LIGHT CONN.



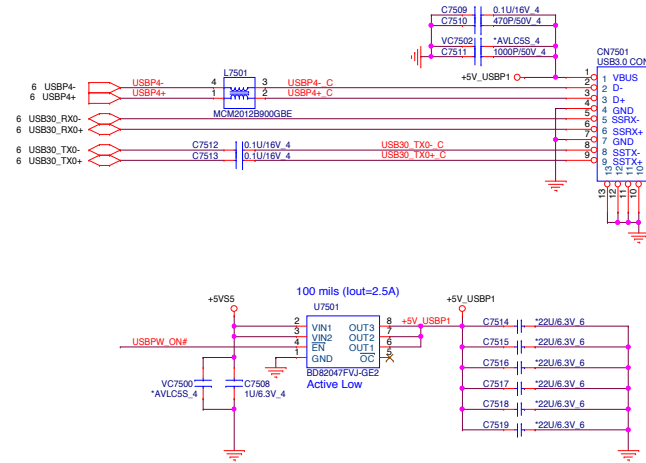
PROJECT : G54A
Quanta Computer Inc.

Size Document Number
TP/FAN/KB/PB
Date: Monday, January 11, 2016 Sheet 26 of 46

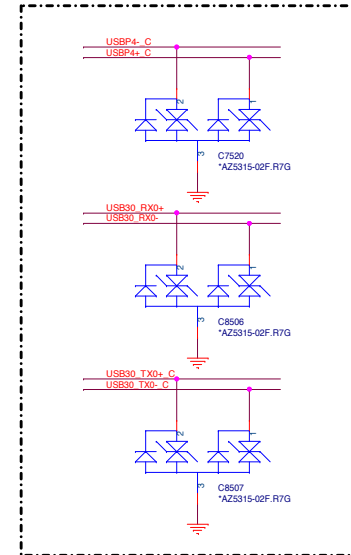
IO CONN.



USB3.0 CONN.

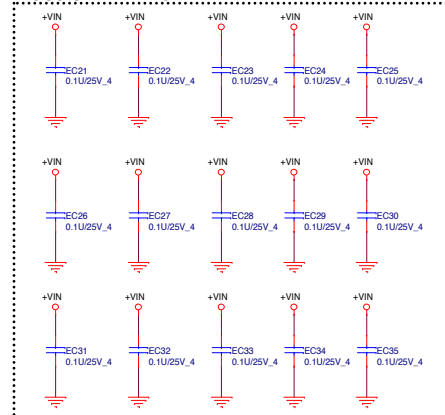


DB to SI Modify



EMI CAPS

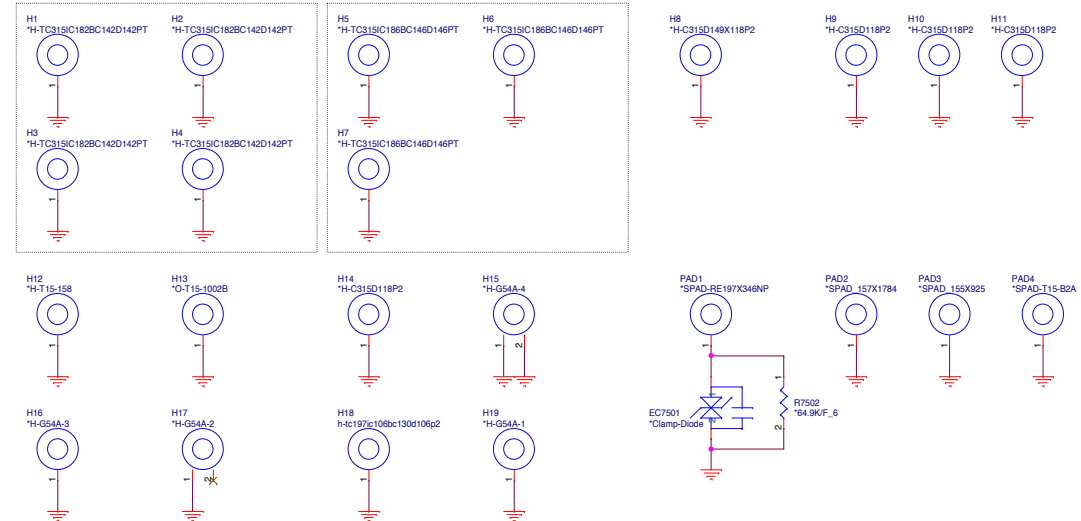
Place on +VIN Path

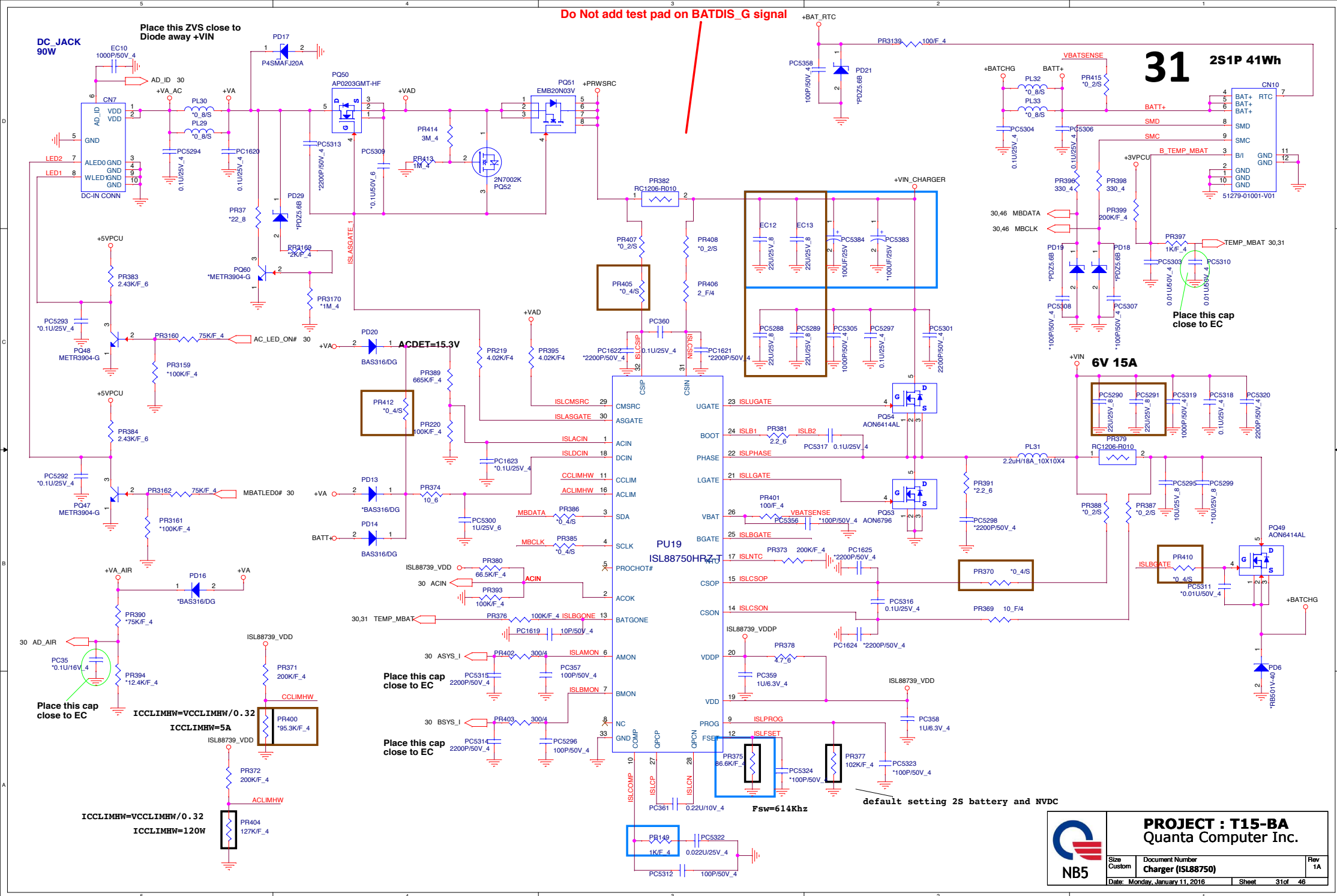


For ISN



HOLES & PADs





32

DC/DC +3VS5/+5VS5

DC/DC +3VS5/+5VS5

+3.3 Volt +/- 5%
TDC:8A
EDP:9A

+5 Volt +/- 5%
TDC:8A
EDP:9A

Do Not add test pad on VCC & LDO pin

Do Not add test pad on VCC & LDO pin

Reserve

Reserve for USB Charge

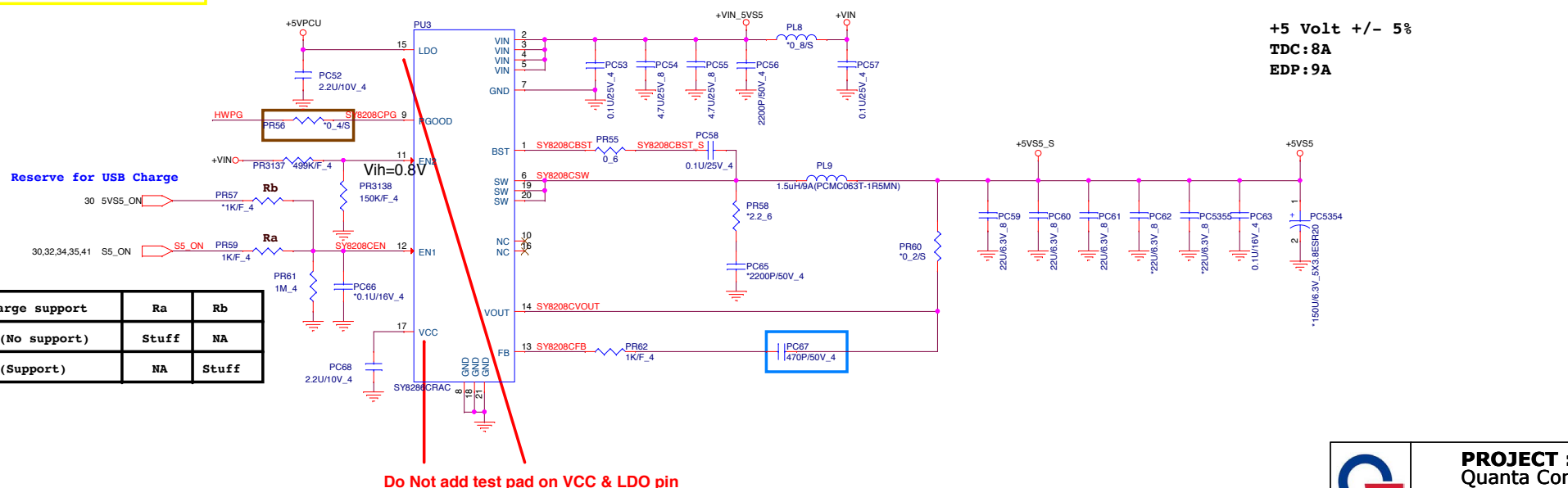
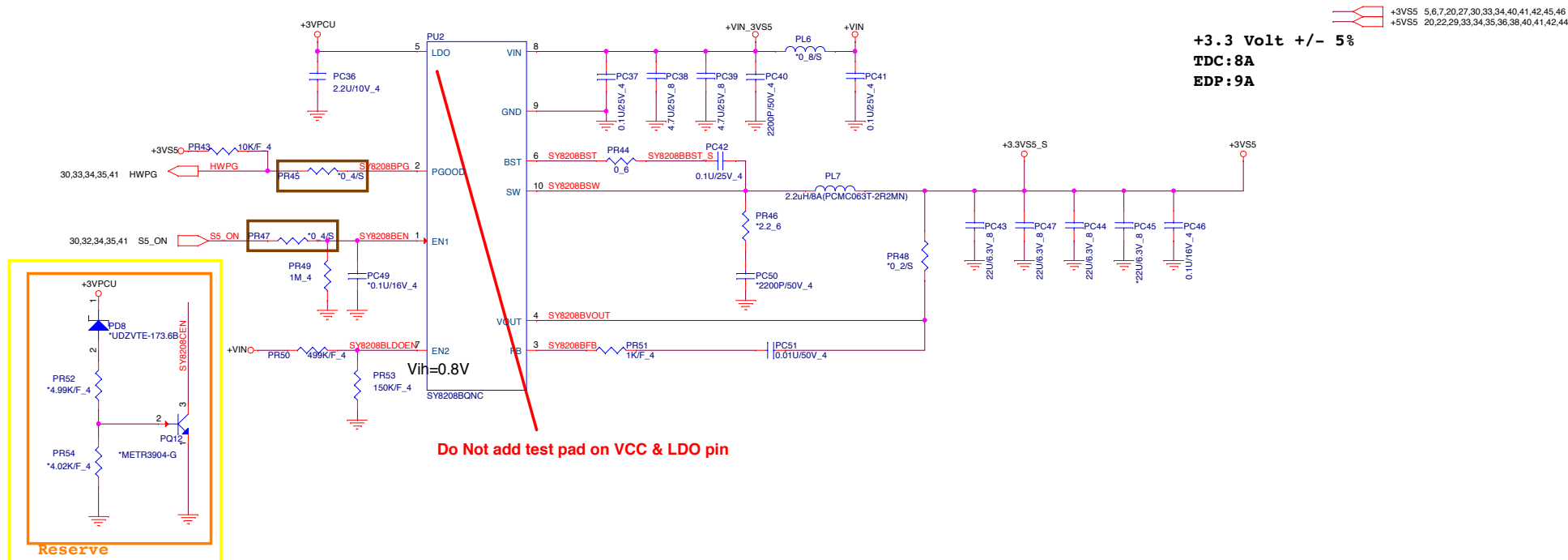
USB Charge support	Ra	Rb
Vine (No support)	Stuff	NA
Envy (Support)	NA	Stuff

PROJECT : T15-BA
Quanta Computer Inc.

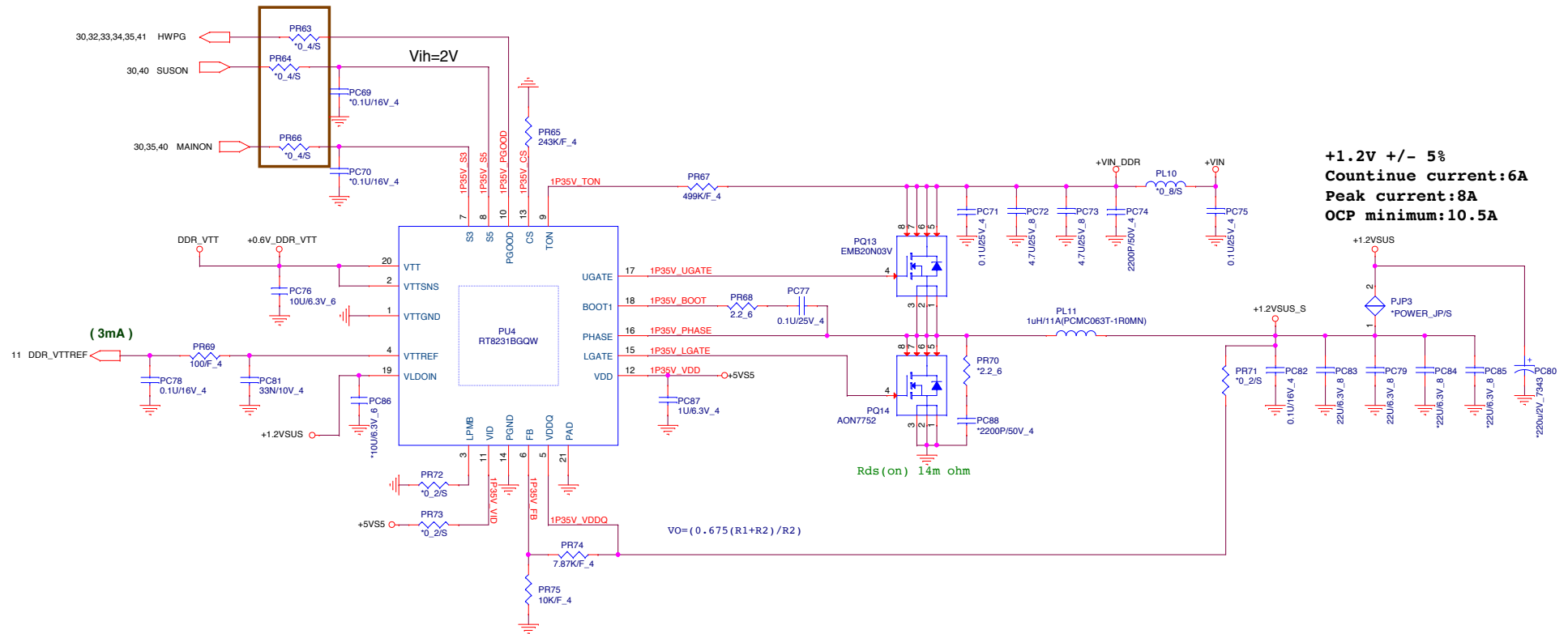
NB5

Size Custom Document Number 3/5VS5 (SY8208B/SY8286C) Rev 1A

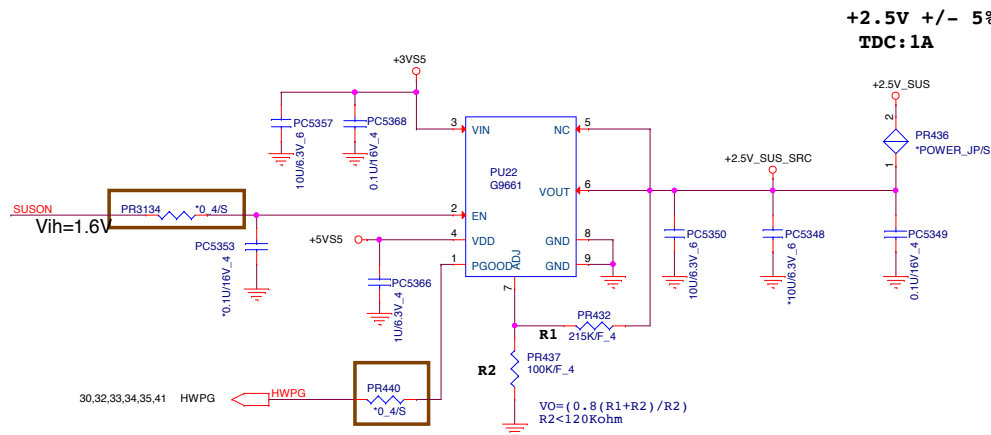
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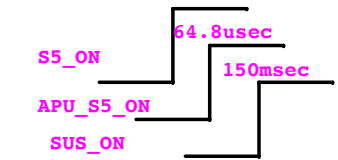
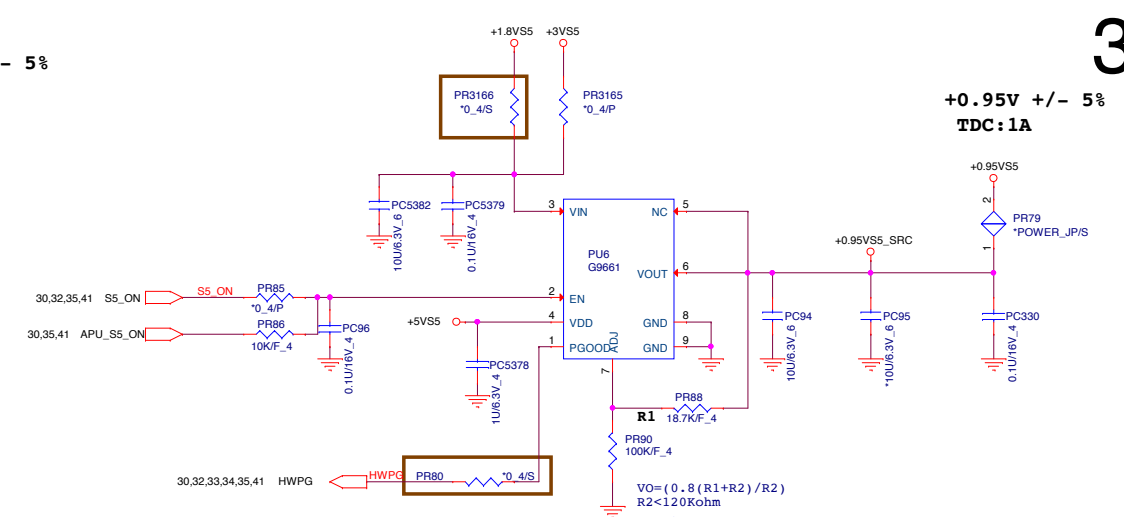
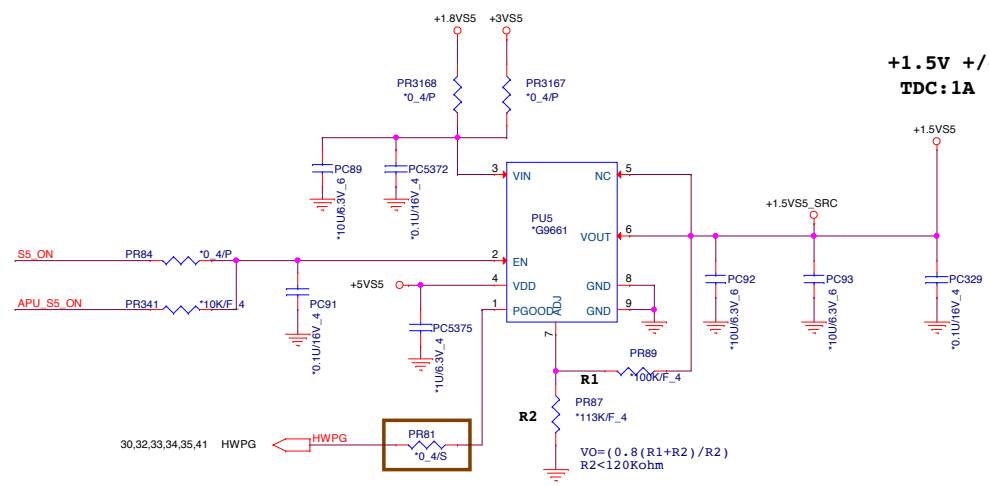


USB Charge support	Ra	Rb
Vine (No support)	Stuff	NA
Envy (Support)	NA	Stuff



+1.2V +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:10.5A

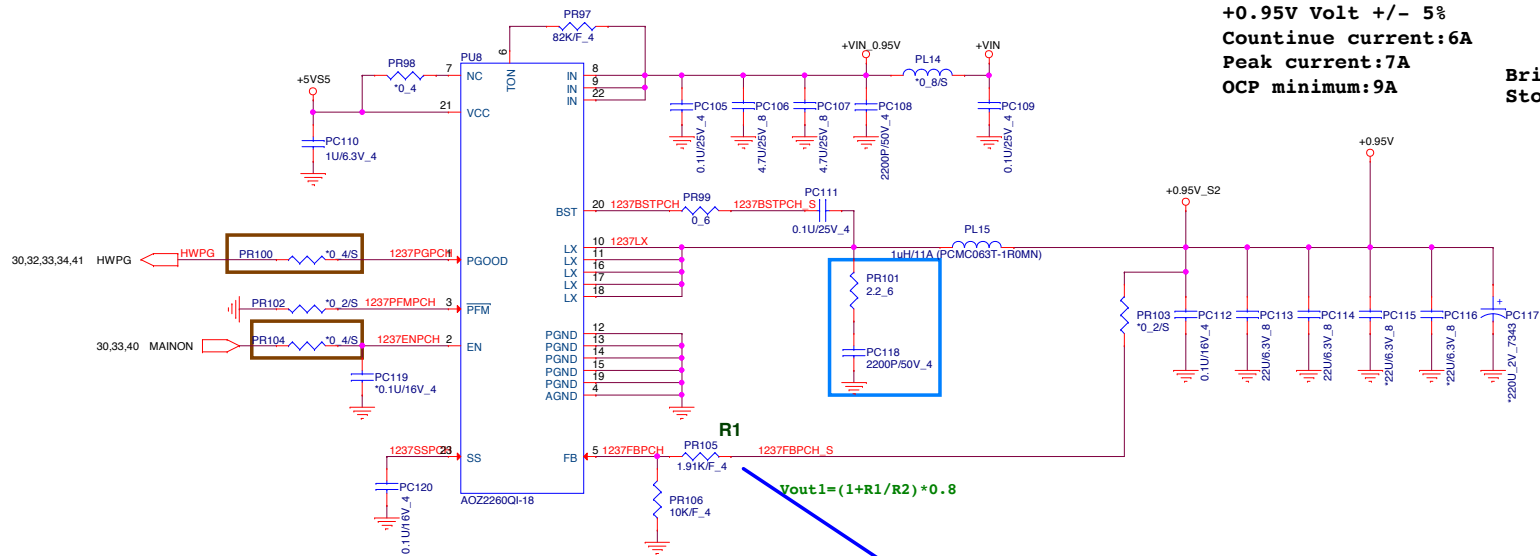




R1

	R1		
Stoney	18.7K	CS31872FB19	0.95V
Bristol	31.6K	CS33162FB14	1.05V

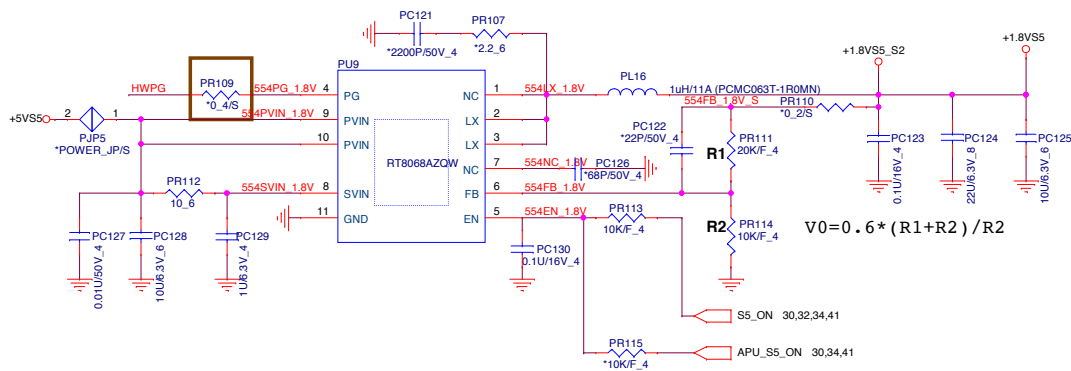
Bristol VDDP=1.05V
Stoney VDDP=0.95V

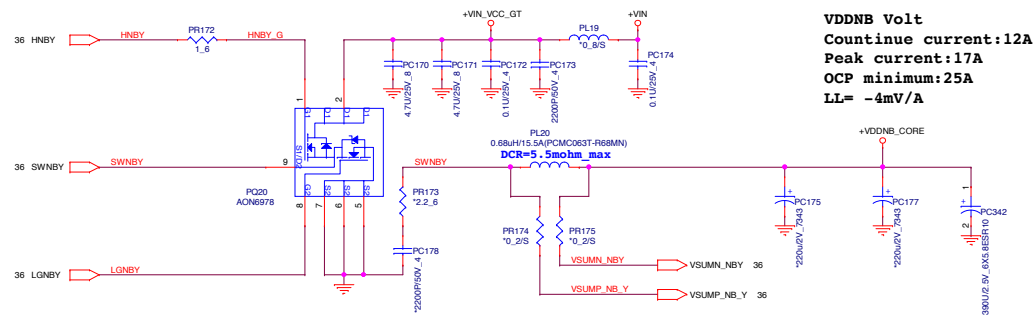
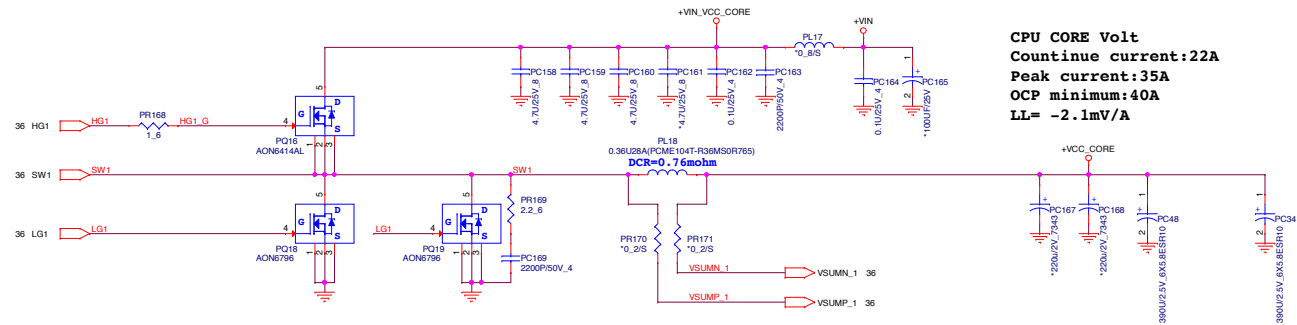


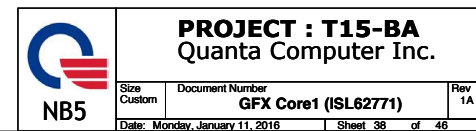
Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

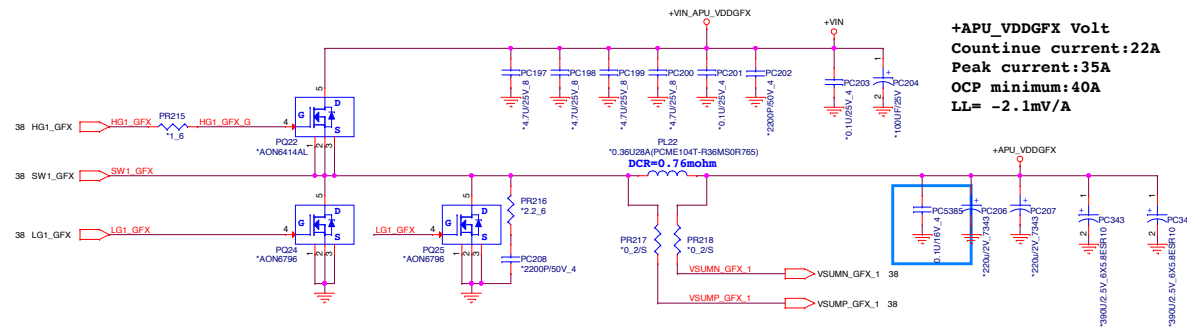
	R1		
Stoney	1.91K	CS21912FB13	0.95V
Bristol	3.16K	CS23162FB04	1.05V

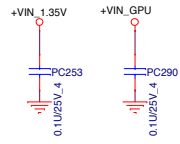
1.8VS5 +/- 3%
TDC: 3A
EDP: 4A





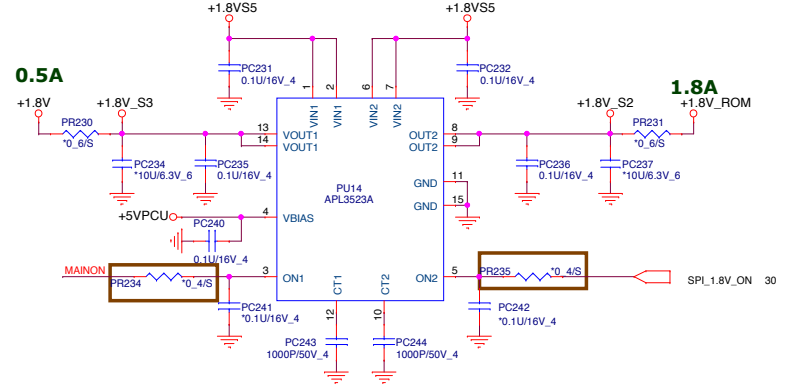
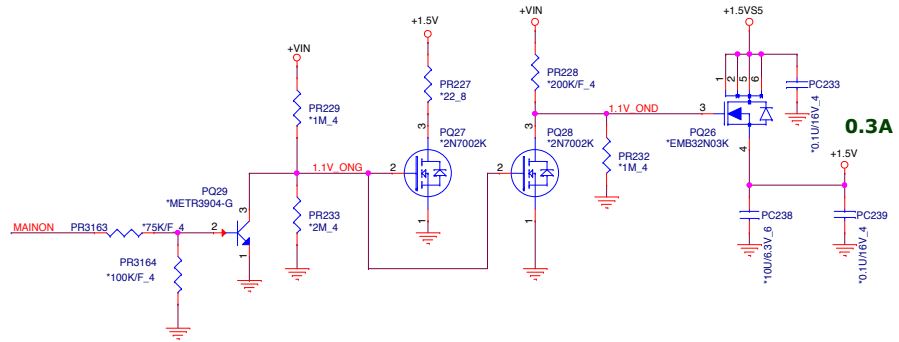
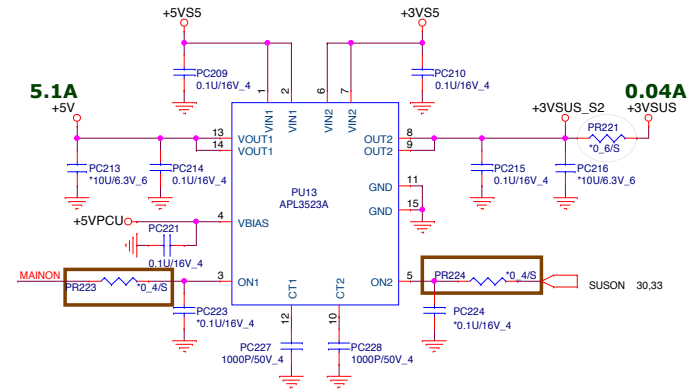






The schematic diagram illustrates the LAN module's internal components and connections. The central component is the PUI2 APL3523A IC, which is configured with several pins connected to external power and signal sources. Key connections include:

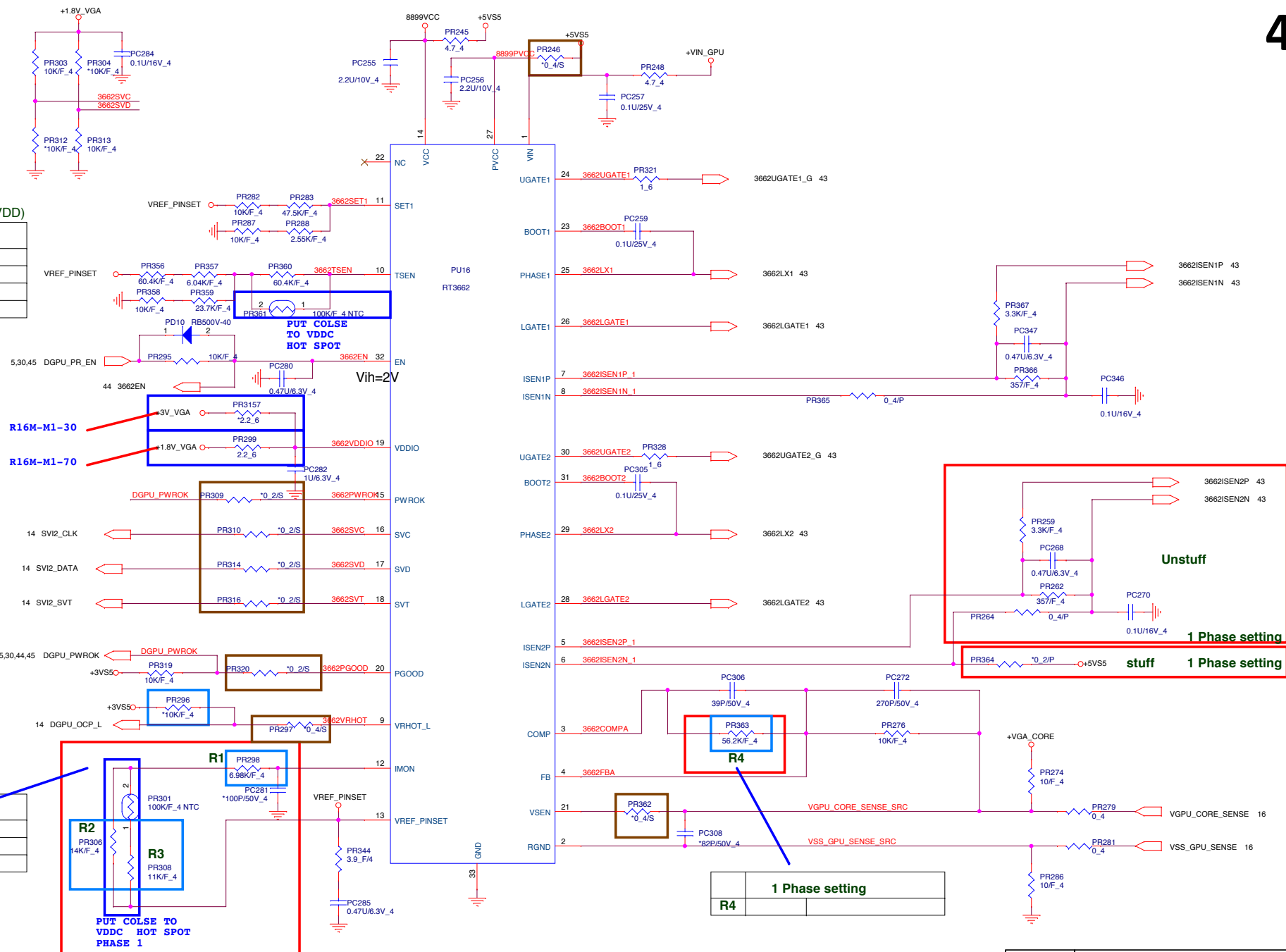
- Power Connections:**
 - +3V5:** Connected to pins 1, 6, and 7.
 - +3V:** Connected to pin 13 (VIN1).
 - +5VPCU:** Connected to pin 4 (VBIAS).
 - +3VLANVCC:** Connected to pins 8 and 9 (OUT2).
 - LAN_POWER:** Connected to pin 5 (ON2).
- Signal Connections:**
 - 30,33,35 MAINON:** Connected to pin 3 (ON1).
 - LAN_POWER:** Connected to pin 5 (ON2).
- Ground Connections:**
 - GND:** Connected to pins 11 and 15.
- Capacitors:**
 - PC211, PC212:** 0.1uF/16V_4 capacitors connected to the +3V5 supply.
 - PC217, PC218:** 10uF/6.3V_6 and 0.1uF/16V_4 capacitors connected to the +3V supply.
 - PC222:** 0.1uF/16V_4 capacitor connected to the +5VPCU supply.
 - PC225, PC226:** 0.1uF/16V_4 capacitors connected to the +3VLANVCC supply.
 - PC229, PC230:** 1000pF/50V_4 capacitors connected to the LAN_POWER supply.
 - PC219, PC220:** 0.1uF/16V_4 and 10uF/6.3V_6 capacitors connected to the LAN_POWER supply.
- Resistors:**
 - PR225, PR226:** 0.4/S resistors connected to the LAN_POWER supply.
 - PR222:** 0.6/S resistor connected to the LAN_POWER supply.





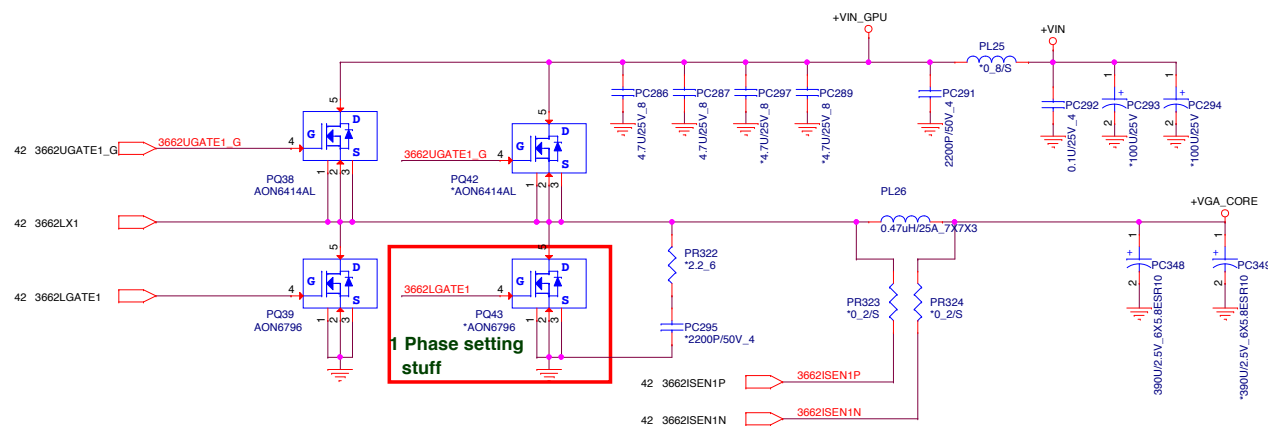
VID Override table (VDD)

SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

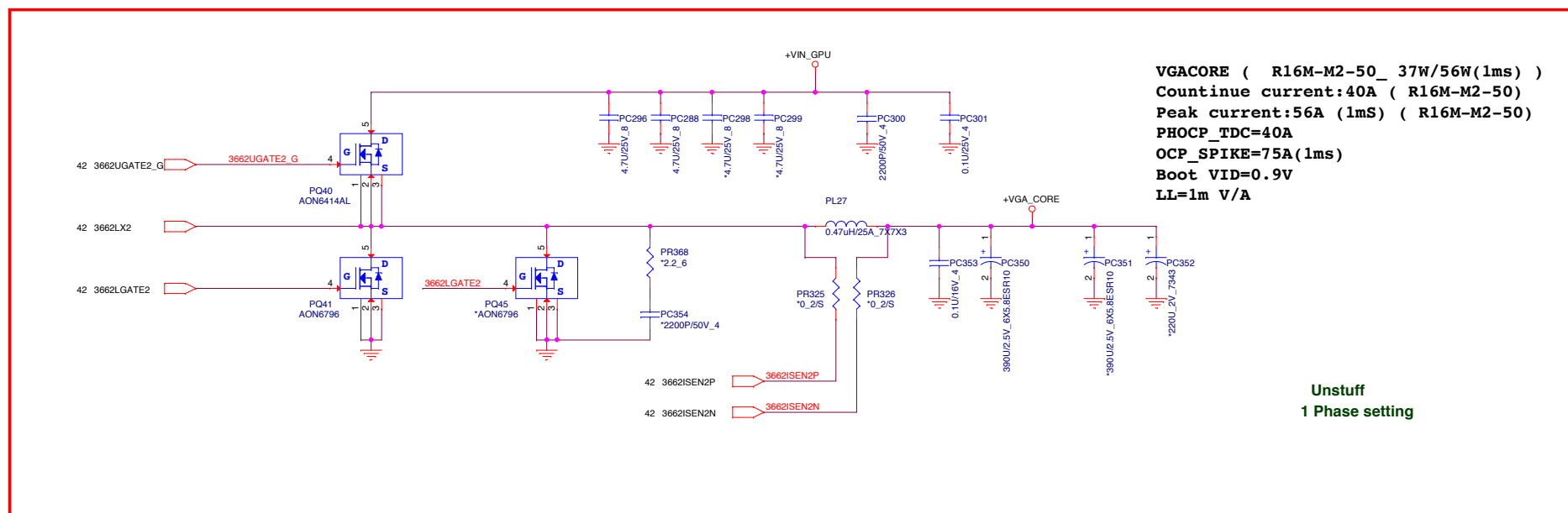


	1 Phase setting	
R1		
R2		
R3		

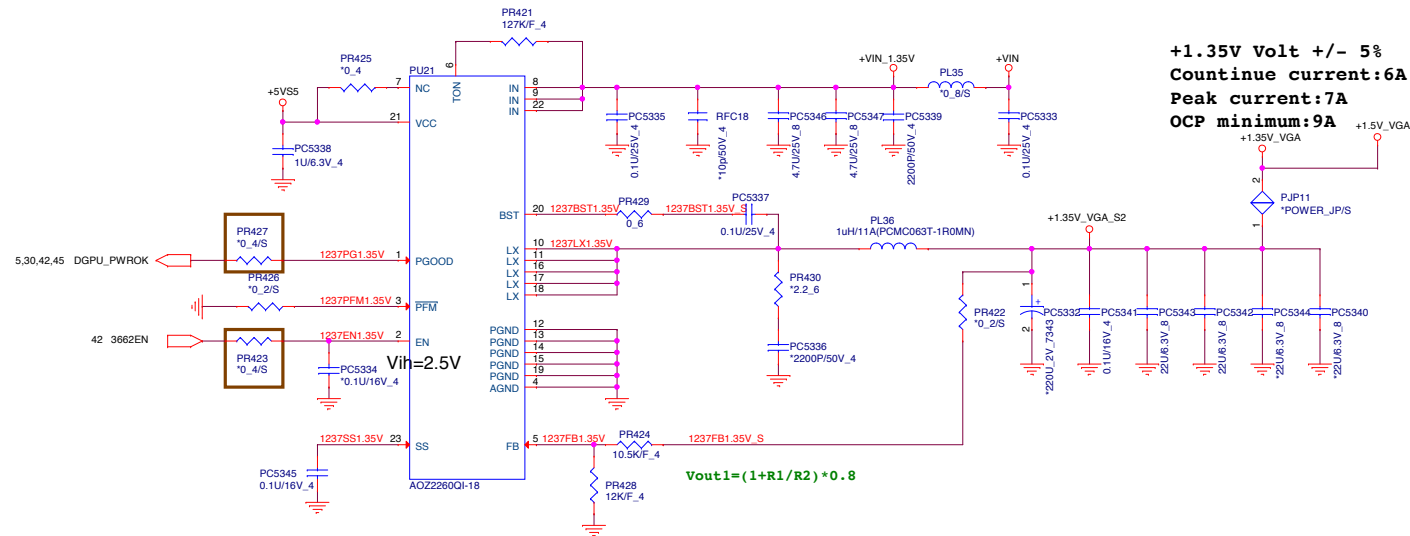
	1 Phase setting	
R4		



VGACORE (R16M-M1-70_ 25W/38W(1ms))
Countinue current:28A
Peak current=38A (1ms)
PHOCP_TDC=40A (soft-start only)
OCP_SPIKE=55A(1ms)
Boot VID=0.9V
LL=1m V/A



VGACORE (R16M-M2-50_ 37W/56W(1ms))
Countinue current:40A (R16M-M2-50)
Peak current:56A (1mS) (R16M-M2-50)
PHOCP_TDC=40A
OCP_SPIKE=75A(1ms)
Boot VID=0.9V
LL=1m V/A



Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k



PROJECT : T15-BA
Quanta Computer Inc.

Size	Document Number	Rev
	+1.5V_VGA(AOZ1236)	1A
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