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MS-7717 Ver: 22 uATX(244mm X 244mm)

CPU:

INTEL -Sandy Bridge LGA 1155 (SOCKET H2)

System Chipset:

INTEL-H67 (COUGAR POINT)

OnBoard Chipset:

Audio Codec ALC887-VD

LAN: Gigabit LAN - INTEL 82579

IO: Fintek F71889AD

Flash ROM: 32 Mb SPI (CHIP)

Main Memory:

DDRIII (1066/1333MHz) * 4 (Dual Channel) max:16GB

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

PCI Slot * 1

PWM:

Controller:Intersil ISL6364 4-Phase -- 95W

Other:

SATA(SATA2-300MB/s) *4+(SATA3-600MB/s) *2

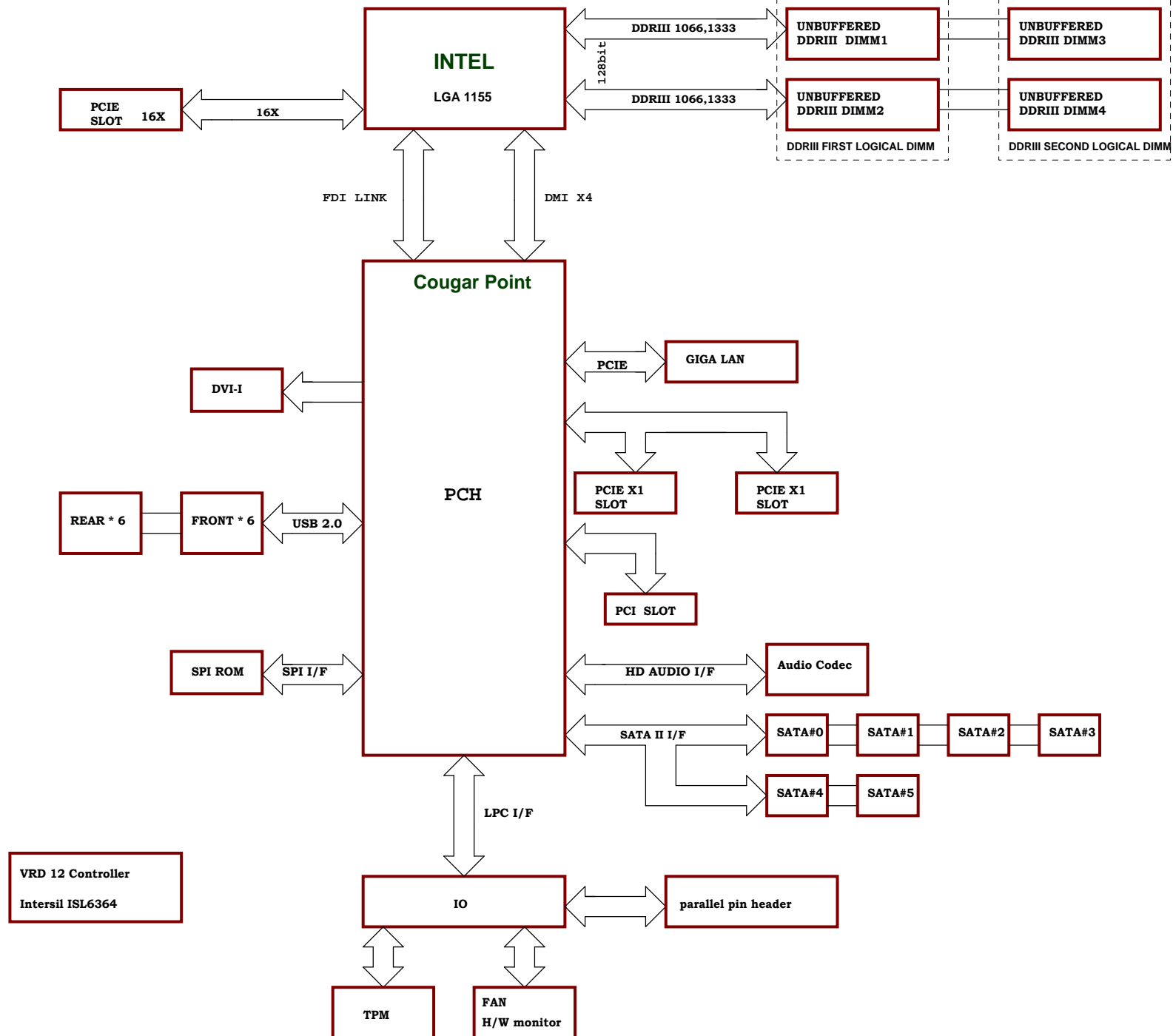
USB2.0 *12 (Rear*6 / Front*6)

DVI-I PORT*1

COM port * 2



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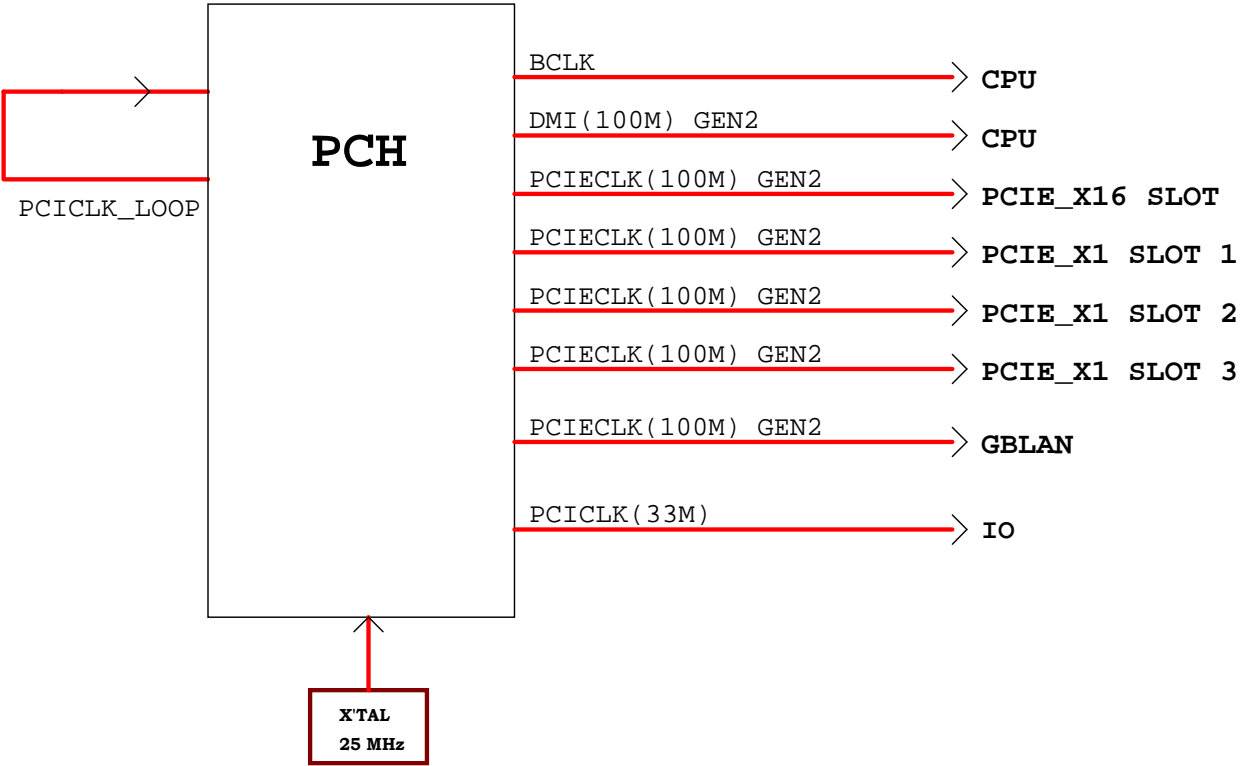
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DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100001B	MEM_MA_CLK_H2/L2 MEM_MA_CLK_H3/L3
DIMM 1 CH-A	10100000B	MEM_MA_CLK_H0/L0 MEM_MA_CLK_H1/L1
DIMM 4 CH-B	10100011B	MEM_MB_CLK_H2/L2 MEM_MB_CLK_H3/L3
DIMM 3 CH-B	10100010B	MEM_MB_CLK_H0/L0 MEM_MB_CLK_H1/L1



Name	Net Name	Power Well	Default	NOTES
GPIO00	BM_BUSY#	Core	GPI	not use pull up VCC3
GPIO01	CPC_BPC_SW	Core	GPI	not use pull up VCC3
GPIO02	PIRQ#E	Core	GPI	not use pull up VCC3
GPIO03	PIRQ#F	Core	GPI	not use pull up VCC3
GPIO04	PIRQ#G	Core	GPI	not use pull up VCC3
GPIO05	PIRQ#H	Core	GPI	not use pull up VCC3
GPIO06	Mini_PCIE1_GPIO	Core	GPI	not use pull up VCC3
GPIO07	Mini_PCIE2_GPIO	Core	GPI	not use pull up VCC3
GPIO08	IGC_EN_N	Suspend	GPO	not use 1K to GND (FCIM Function)
GPIO09	OC#4_5	Suspend	Native	not use pull up 3VSB
GPIO10	OC#6_7	Suspend	Native	not use pull up 3VSB
GPIO11	PCH_SMBALERT#	Suspend	Native	not use pull up 3VSB
GPIO12	LAN_DISABLE#	Suspend	Native	pull up 3VSB LAN_PHY_PWR_CTRL
GPIO13	SLOT_PWR_SW	Suspend	GPI	pull up 3VSB (GPO: Slot power function)
GPIO14	OC#6_7	Suspend	Native	not use pull up 3VSB
GPIO15	PCH_GPIO15	Suspend	GPO	not use Strapping : internal pull-down(TLS function)
GPIO16	JUSB30_SENSE#A	Core	GPI	not use pull up VCC3
GPIO17	BOOT_BLOCK_RECOVERY	Core	GPI	not use pull up VCC3
GPIO18 (Mobile Only)		Core	Native	NA
GPIO19	JUSB2_SENSE#B	Core	GPI	Strapping :Pull-up resistors are not required
GPIO20	PCH_GP20	Core	Native	not use pull up VCC3
GPIO21	JUSB2_SENSE#A	Core	GPI	not use pull up VCC3
GPIO22	MB_ID0	Core	GPI	not use pull up VCC3
GPIO23	LDRQ1#	Core	Native	Internal pull-up
GPIO24	H_SKTOCC_PCH_R	Suspend	GPO	pull up 3VSB (GPI:CPU detect: Low Active)
GPIO25 (Mobile Only)		Suspend	Native	NA
GPIO26 (Mobile Only)		Suspend	Native	NA
GPIO27	HDOUT_AMP_DIS#	DSW	GPI	not use pu 3VA
GPIO28	OD_PLL_VR_EN	Suspend	GPO	not use pull up 3VSB
GPIO29	SLP_LAN#	Suspend	GPI	SLP_LAN# function
GPIO30	SUS_WARN#	Suspend	Native	SUS_WARN# function

ADD:

GPIO46 : Use to control ME Flash function
 Enable : Low
 Disable : High
 Default : High

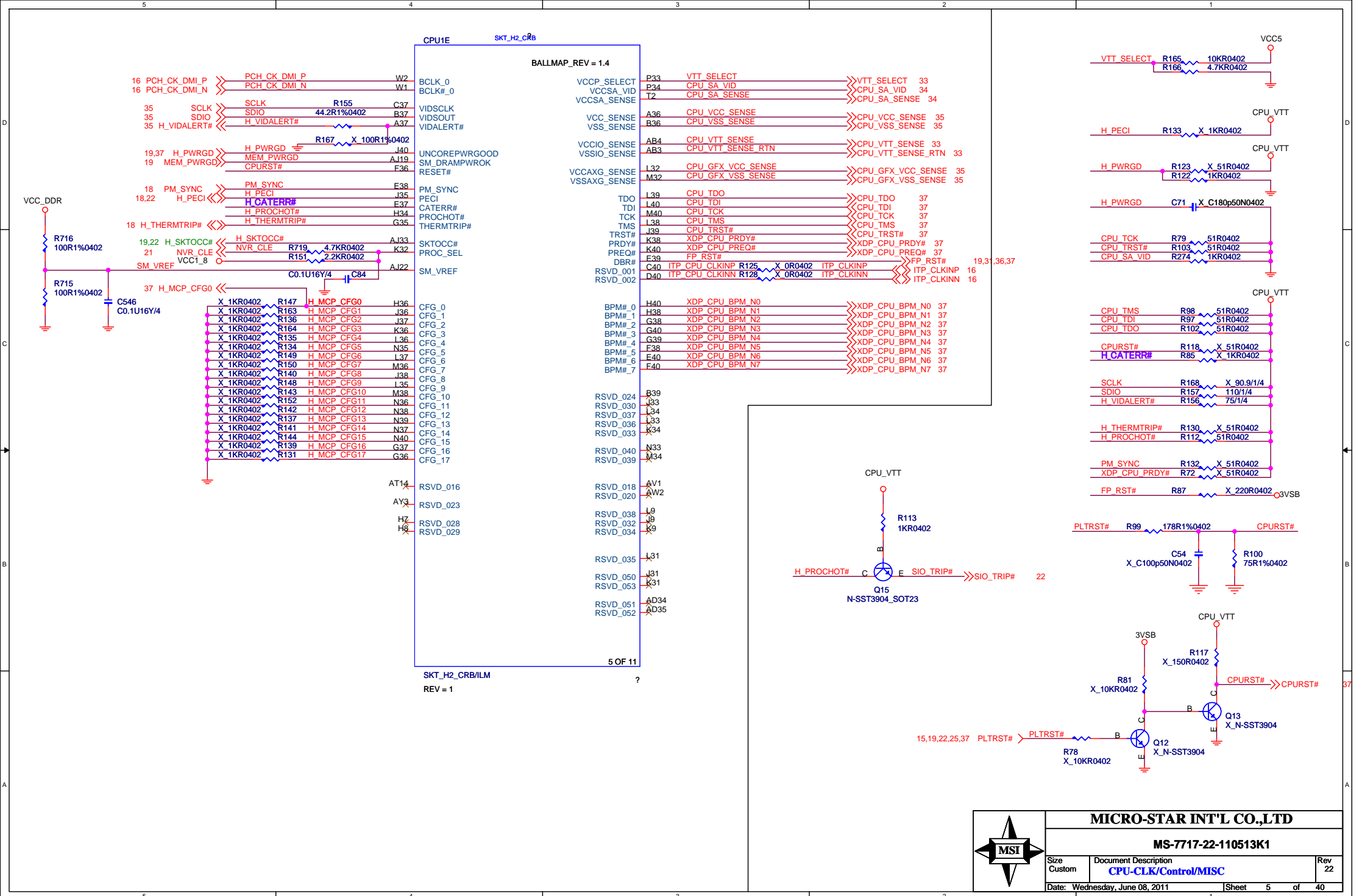
GPIO31	FRONT_OUT_DISABLE	DSW	GPI	not use pu 3VA
GPIO32	SPL_WF#	Core	GPO	pull up 3VSB SPL_WF# function Active Low
GPIO33	SPL_HOLD_GPO#	Core	GPO	SPL_HOLD_GPO# Active Low
GPIO34	HOOD_SW_DET#	Core	GPI	not use pull up VCC3
GPIO35	PCH_GPIO35	Core	GPO	not use
GPIO36	JUSB3_SENSE#A	Core	GPI	not used NC
GPIO37	JUSB3_SENSE#B	Core	GPI	not used NC
GPIO38	MB_ID1	Core	GPI	not use pull up VCC3
GPIO39	MB_ID2	Core	GPI	not use pull up VCC3
GPIO40	OC#0_1	Suspend	Native	not use pull up 3VSB
GPIO41	OC#2_3	Suspend	Native	not use pull up 3VSB
GPIO42	OC#2_3	Suspend	Native	not use pull up 3VSB
GPIO43	OC#4_5	Suspend	Native	not use pull up 3VSB
GPIO44	PCIECLKRQ5#	Suspend	Native	pull up 3VSB
GPIO45	PCH_GPIO45	Suspend	Native	not use pull up 3VSB
GPIO46	CLEAR_PWD	Suspend	Native	not use pull up 3VSB
GPIO47 (Mobile Only)		Suspend	Native	NA
GPIO48	MB_ID3	Core	GPI	not use pull up VCC3
GPIO49	JUSB30_SENSE#B	Core	GPI	not use pull up VCC3
GPIO50	PREQ#1	Core	Native	not use pull up VCC3
GPIO51	PGNT#1	Core	Native	Strapping :Pull-up resistors are not required
GPIO52	PREQ#2	Core	Native	not use pull up VCC3
GPIO53	PGNT#2	Core	Native	not use Do not pull low,
GPIO54	PREQ#3	Core	Native	not use pull up VCC3
GPIO55	PGNT#3	Core	Native	Pull-up resistors are not required on these signals
GPIO56 (Mobile Only)		Suspend	Native	NA
GPIO57	USB_DET1	Suspend	GPI	not use pull up 3VSB
GPIO58	PCH_SML1CLK	Suspend	Native	not use pull up 3VSB
GPIO59	OC#0_1	Suspend	Native	not use pull up 3VSB
GPIO60	PCH_SML0ALERT#	Suspend	Native	not use pull up 3VSB
GPIO61	USB_DET2	Suspend	Native	not use pull up 3VSB
GPIO62	SUSCLK	Suspend	Native	No external resistors required
GPIO63	SLP_S5#	Suspend	Native	No pull up/down resistors needed
GPIO64	TP_CLKOUTFLEX0	Core	Native	not use
GPIO65	TP_CLKOUTFLEX1	Core	Native	not use
GPIO66	TP_CLKOUTFLEX2	Core	Native	not use
GPIO67	CK_48M_SIO_R	Core	Native	SIO_48M_clock
GPIO68	JUSB1_SENSE#A	Core	GPI	not use pull up VCC3
GPIO69	JUSB1_SENSE#B	Core	GPI	not use pull up VCC3
GPIO70	TP_GPIO70	Core	Native	not use pull up VCC3
GPIO71	TP_GPIO71	Core	Native	not use pull up VCC3
GPIO72	HOOD_SENSE#	Suspend	Native (Mobile Only)	not use pull up 3VSB
GPIO73 (Mobile Only)				NA
GPIO74	PCH_SML1ALERT#	Suspend	Native	not use pull up 3VSB
GPIO75	PCH_SML1DATA	Suspend	Native	not use pull up 3VSB



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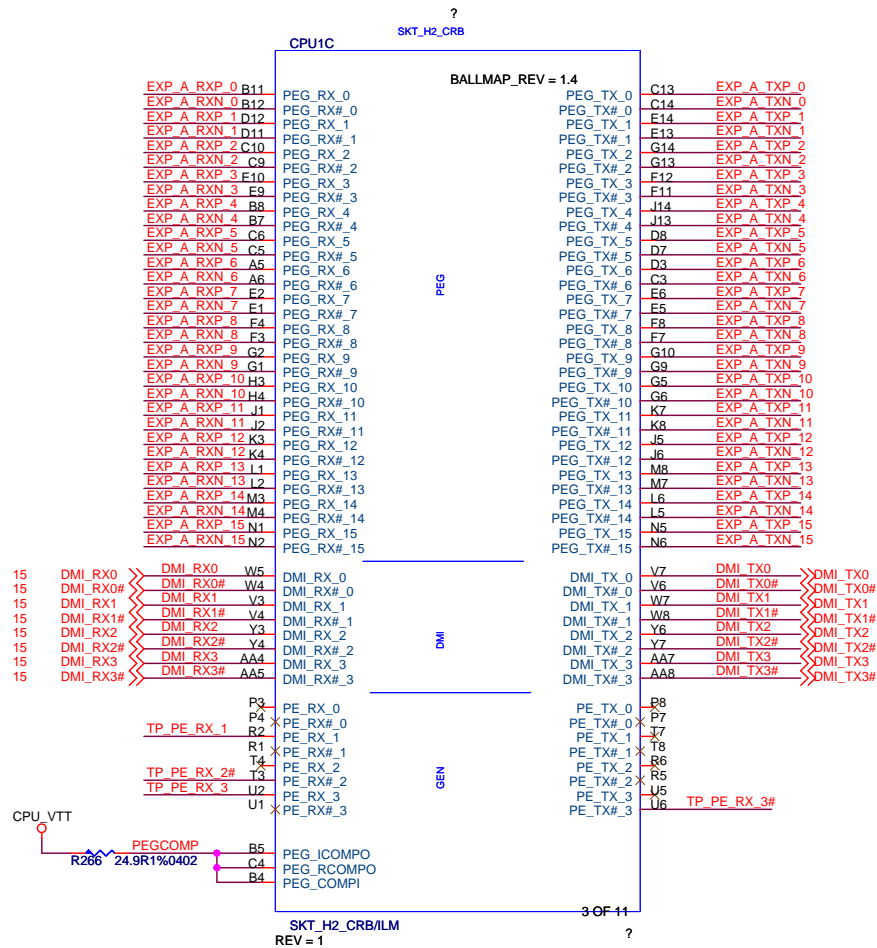
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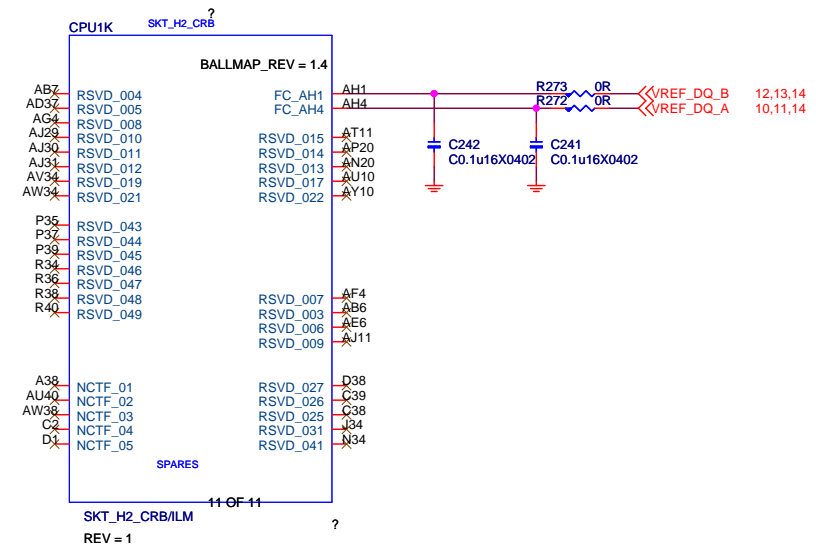
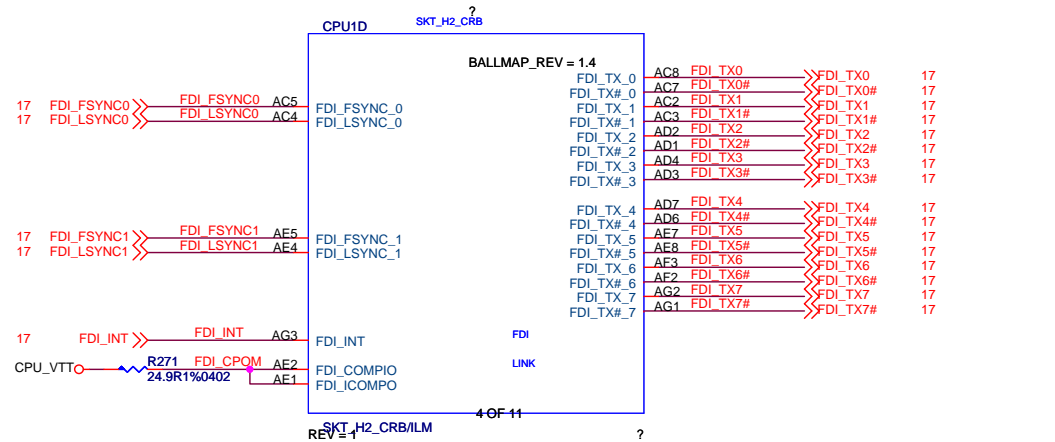


PEG & DMI

23 EXP_A_RXP_[15..0] >> EXP A RXP [15..0]
 23 EXP_A_RXN_[15..0] >> EXP A RXN [15..0]
 23 EXP_A_TXP_[15..0] << EXP A TXP [15..0]
 23 EXP_A_TXN_[15..0] << EXP A TXN [15..0]



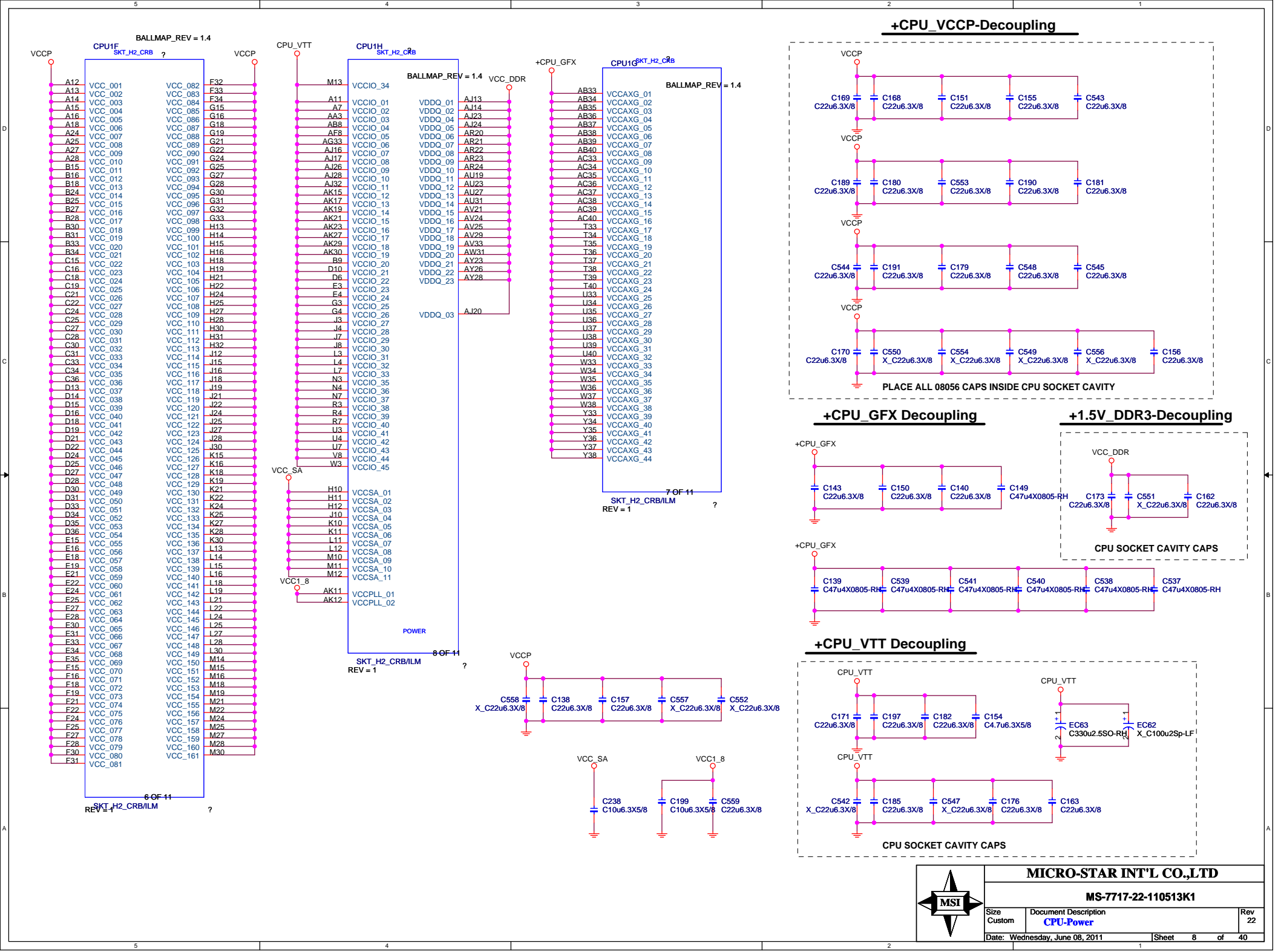
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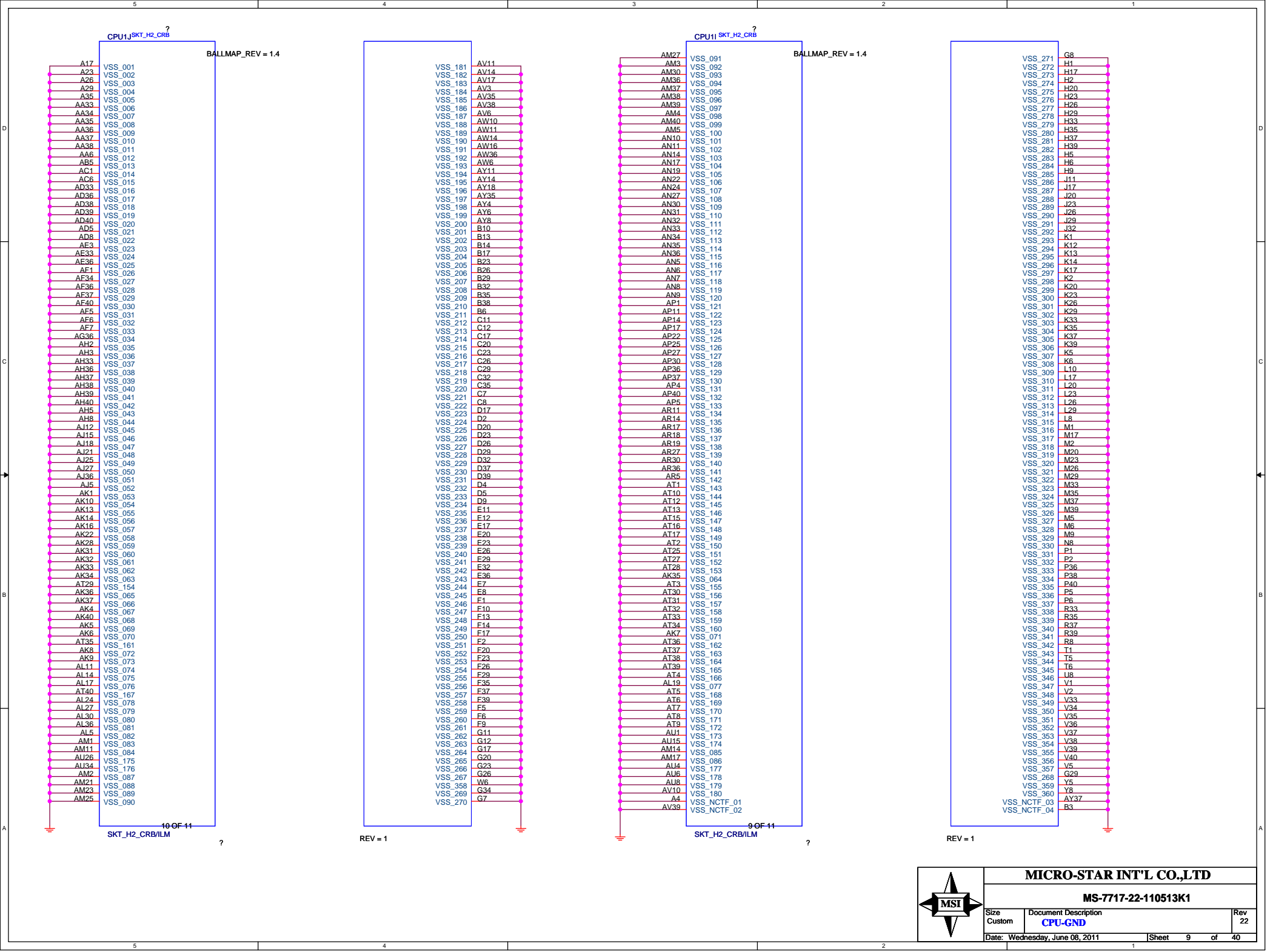


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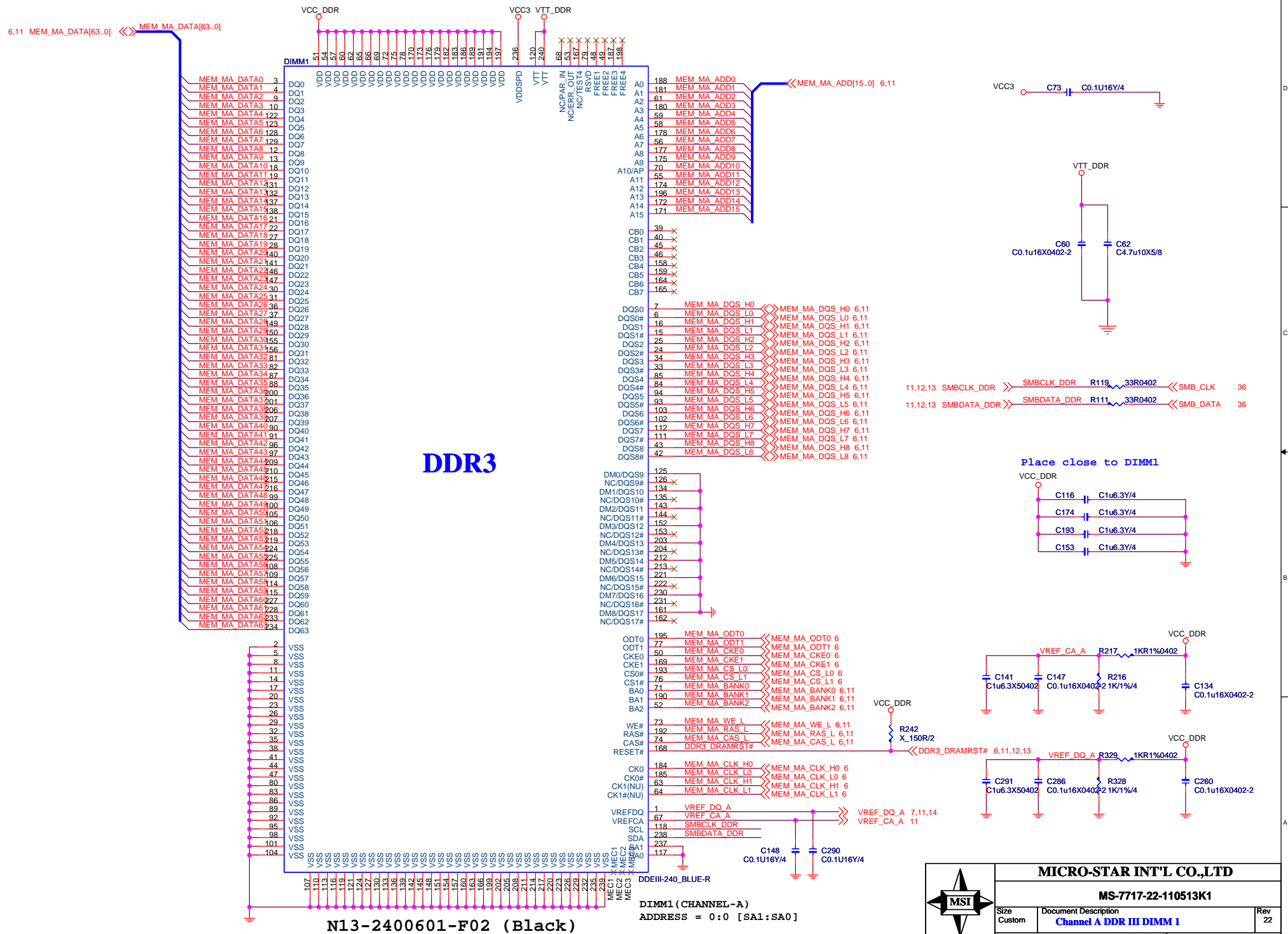
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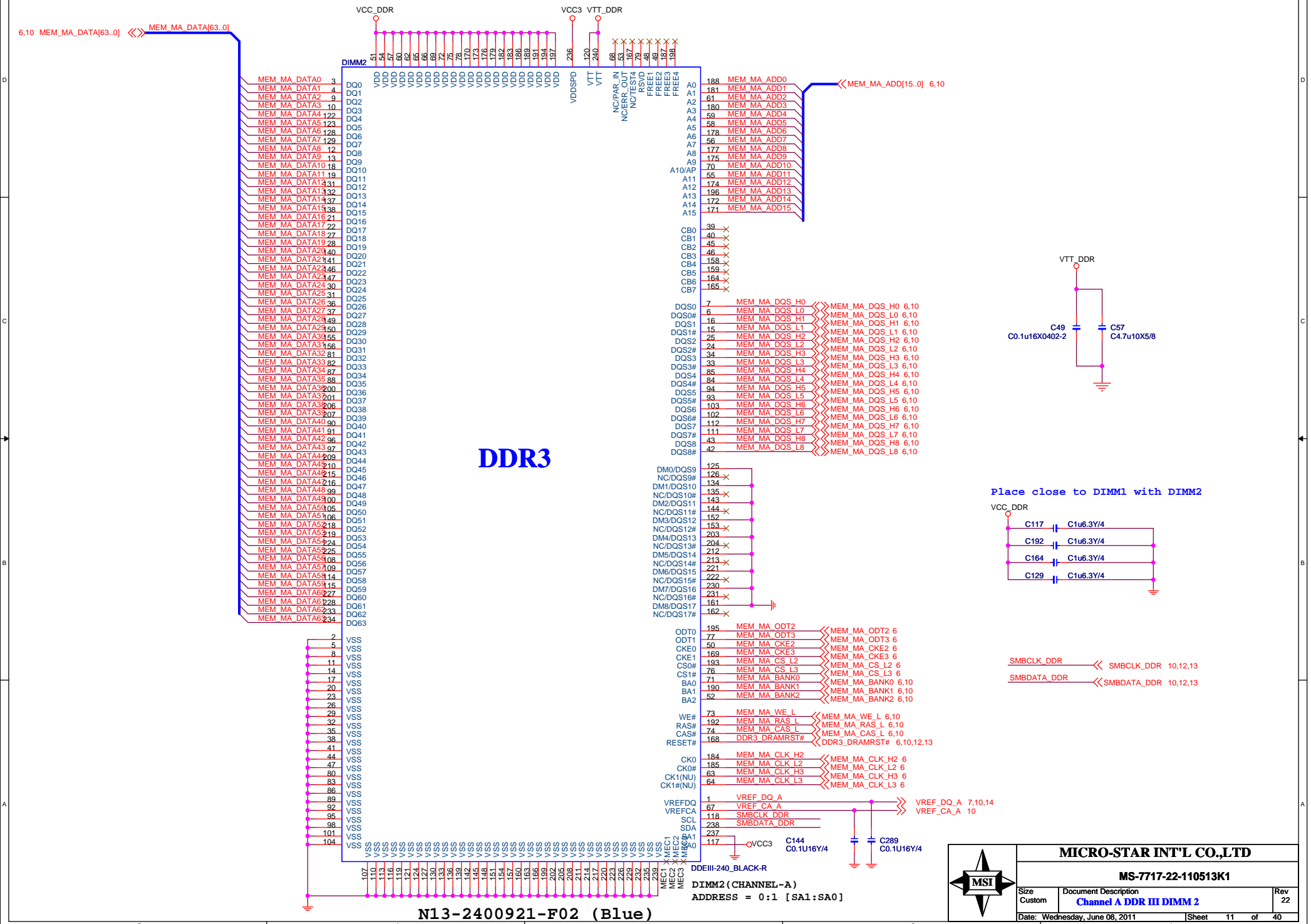
DDRIII DIMM_A1



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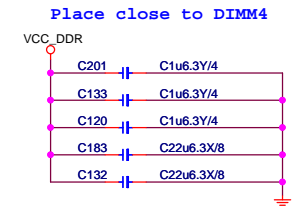
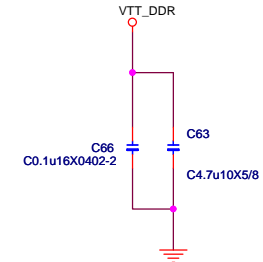
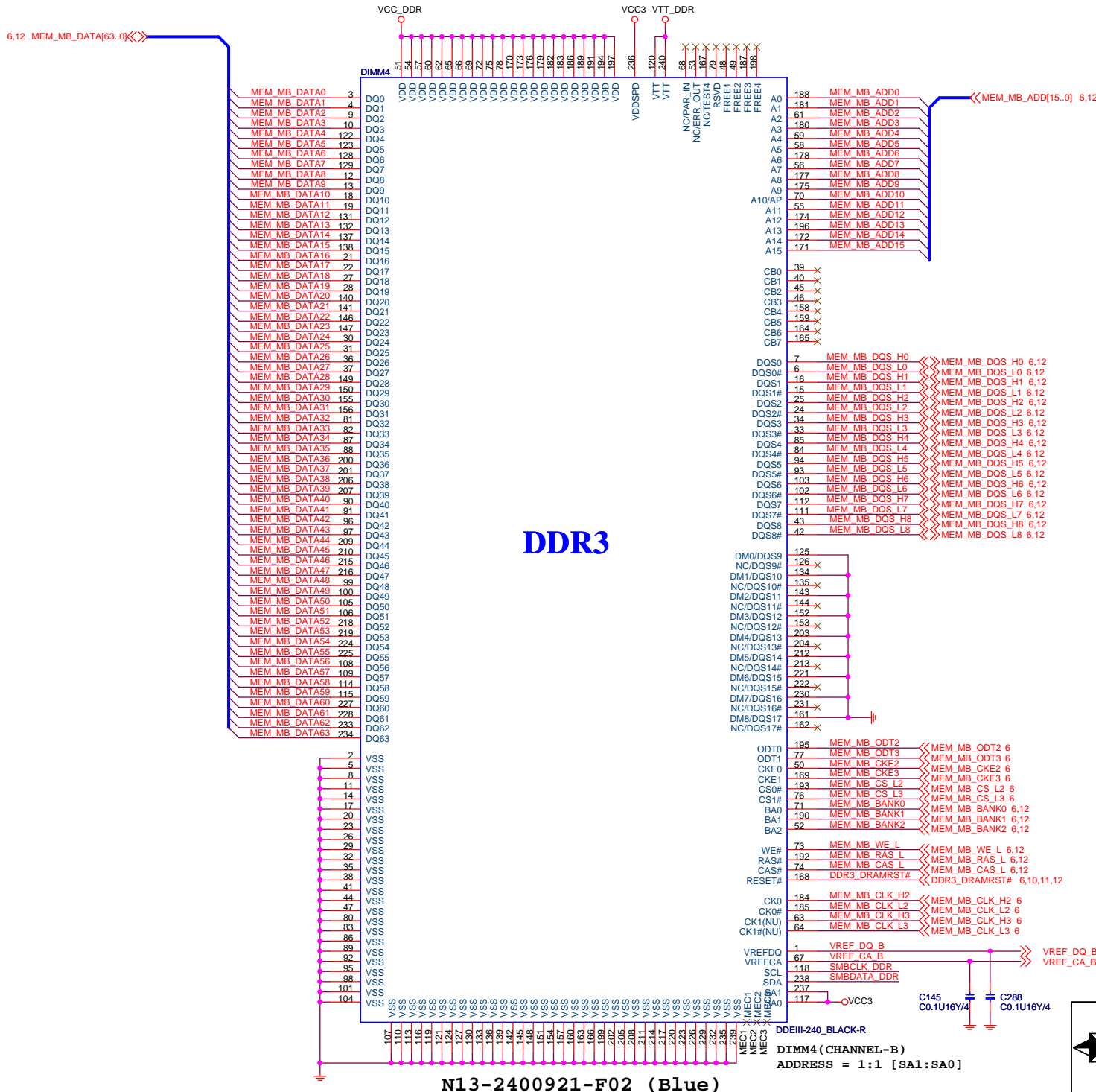


N13-2400601-F02 (Black)



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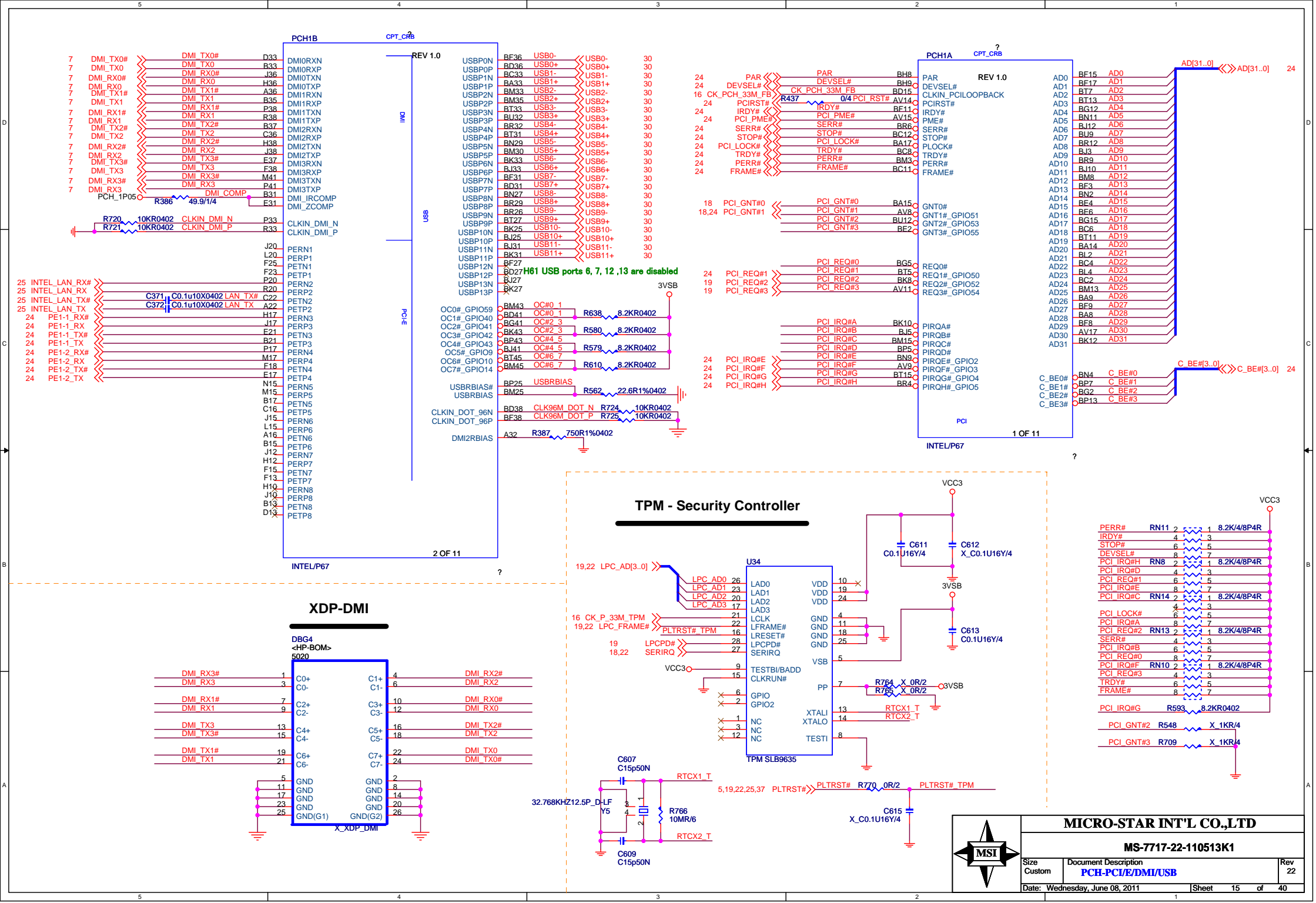
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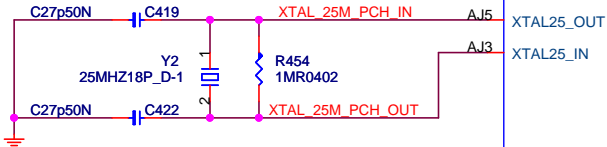
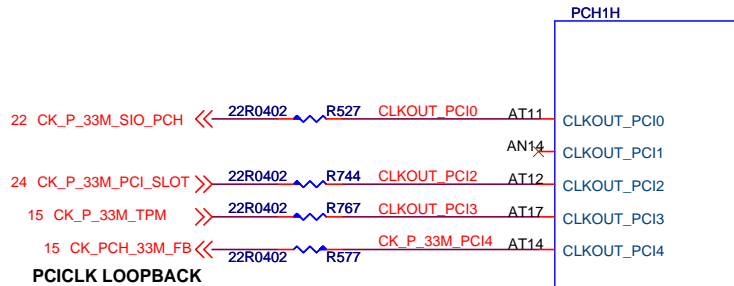


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SMBDATA_DDR << SMBDATA_DDR 10,11,12



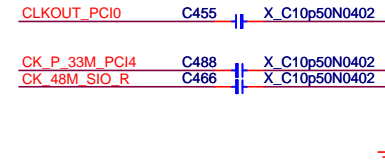
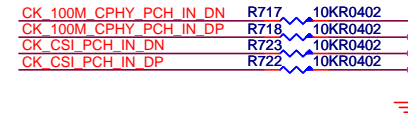
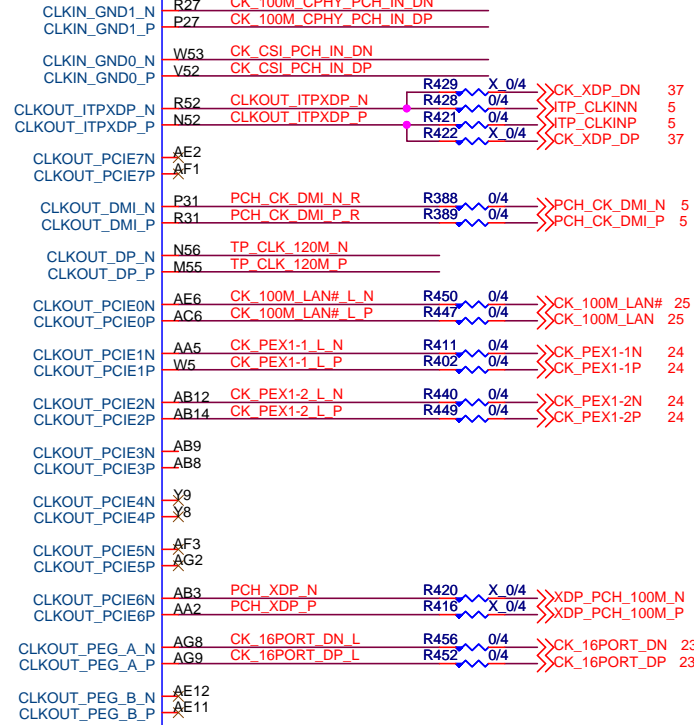
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CPT_CRB

REV 1.0



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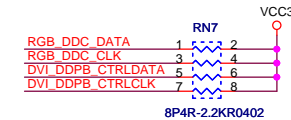
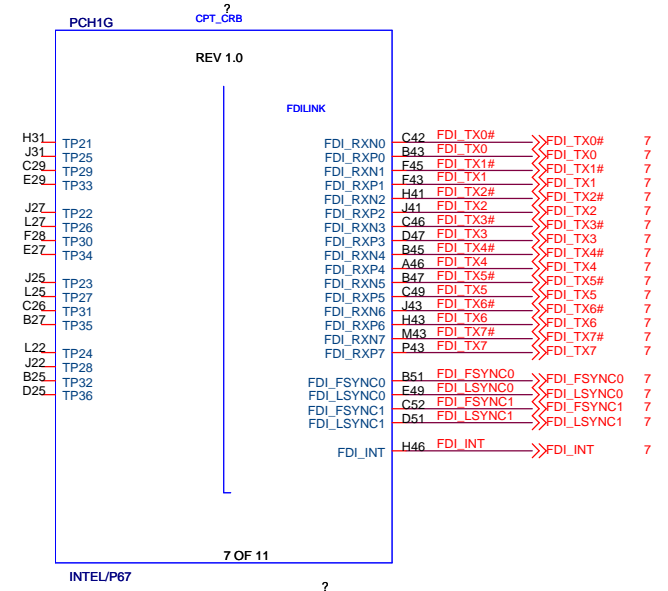
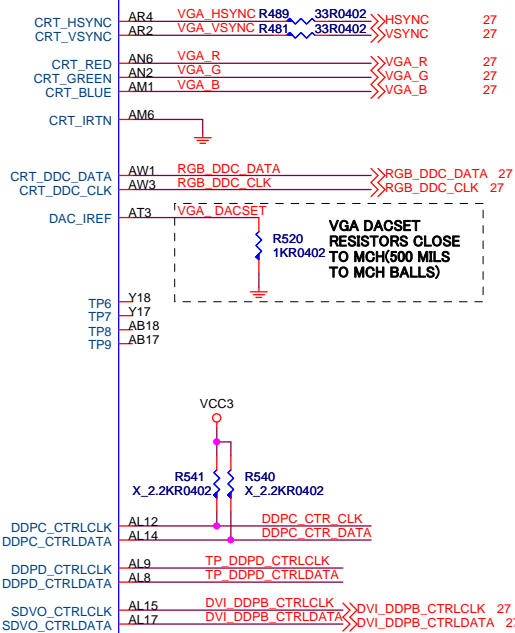
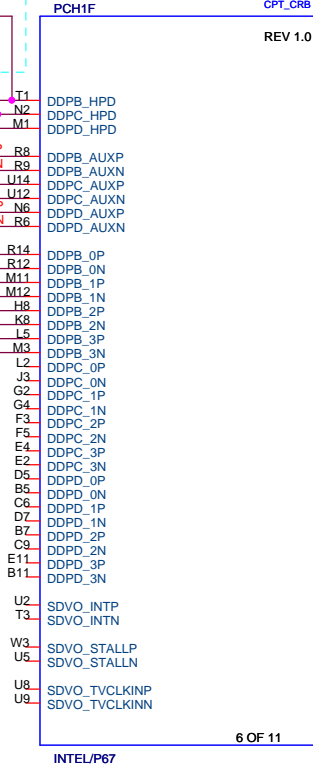
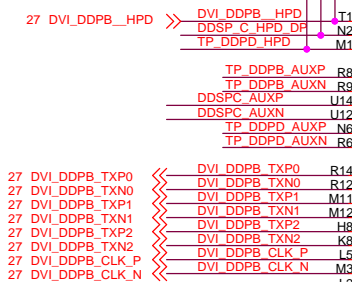
INTEL/P67



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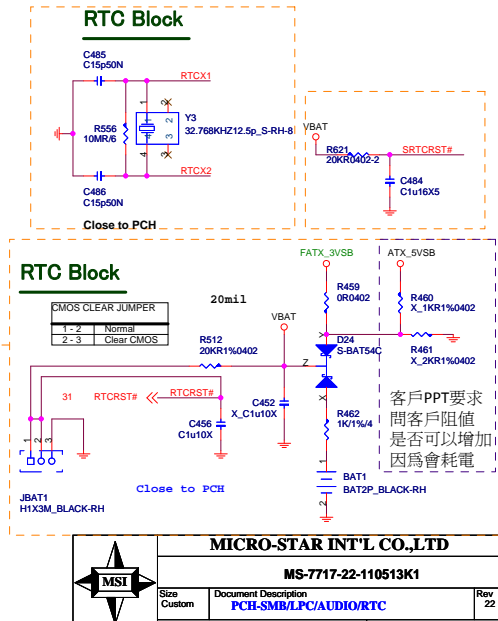
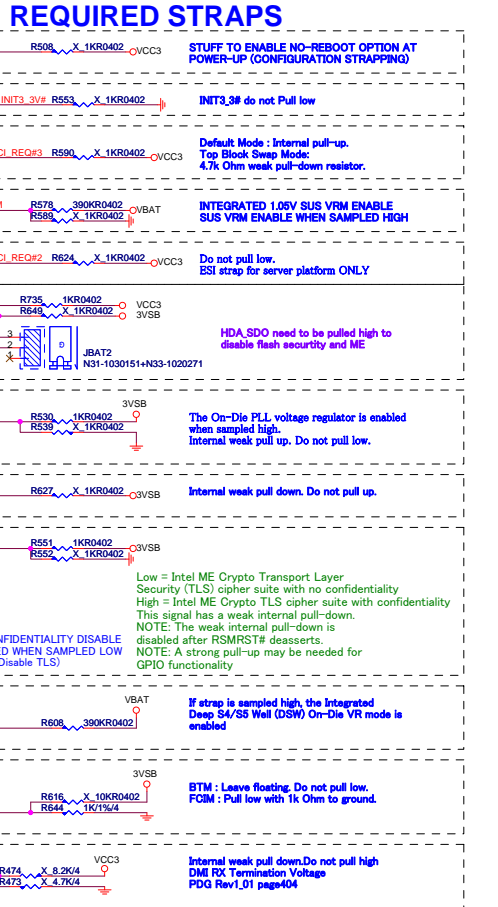
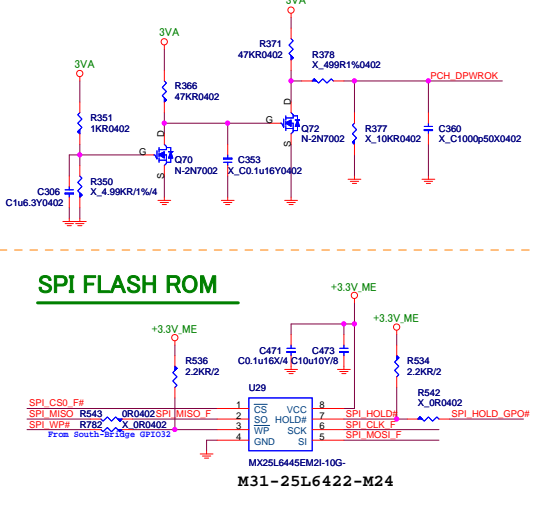
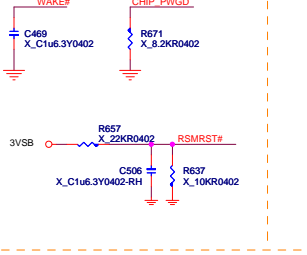
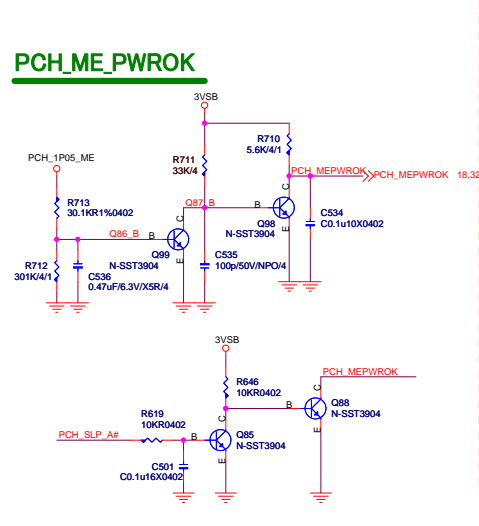
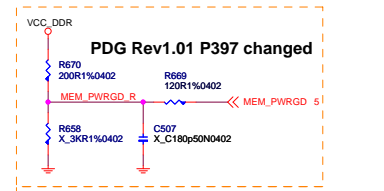
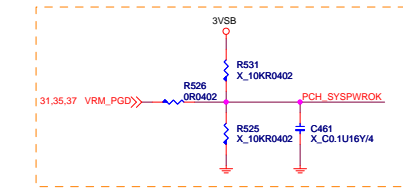
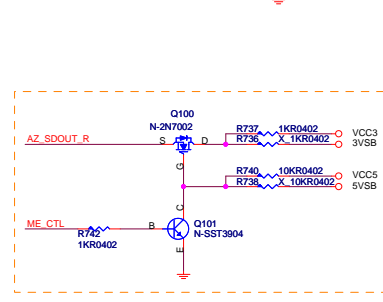
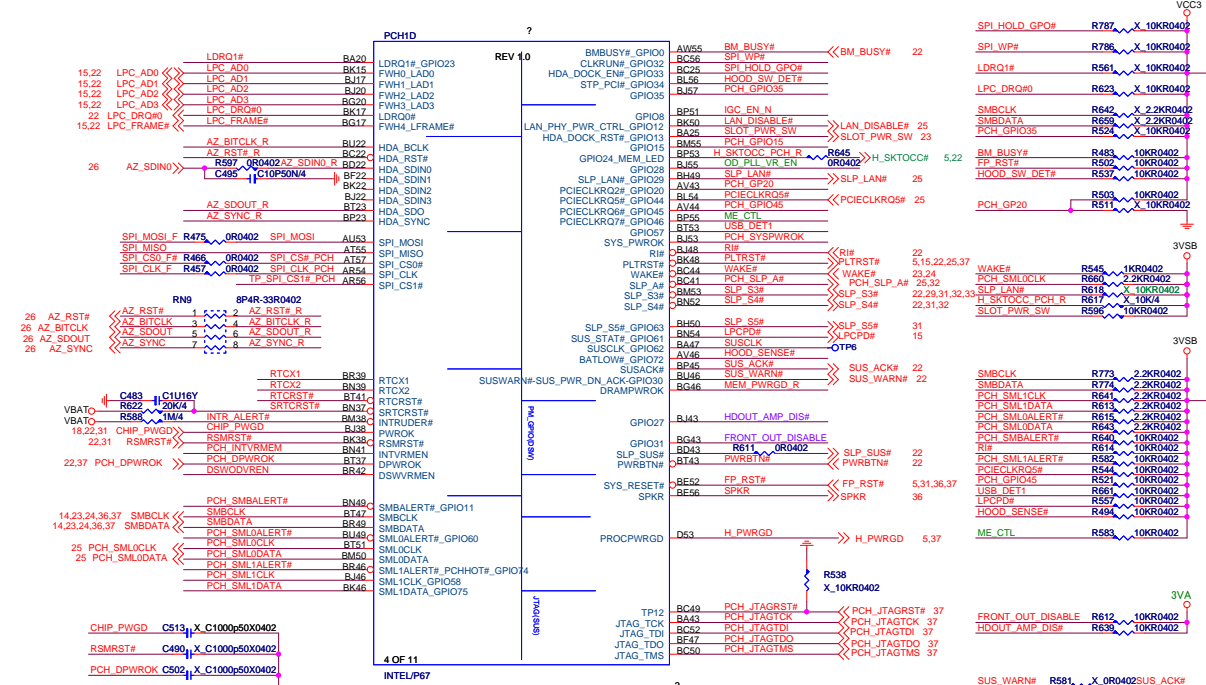
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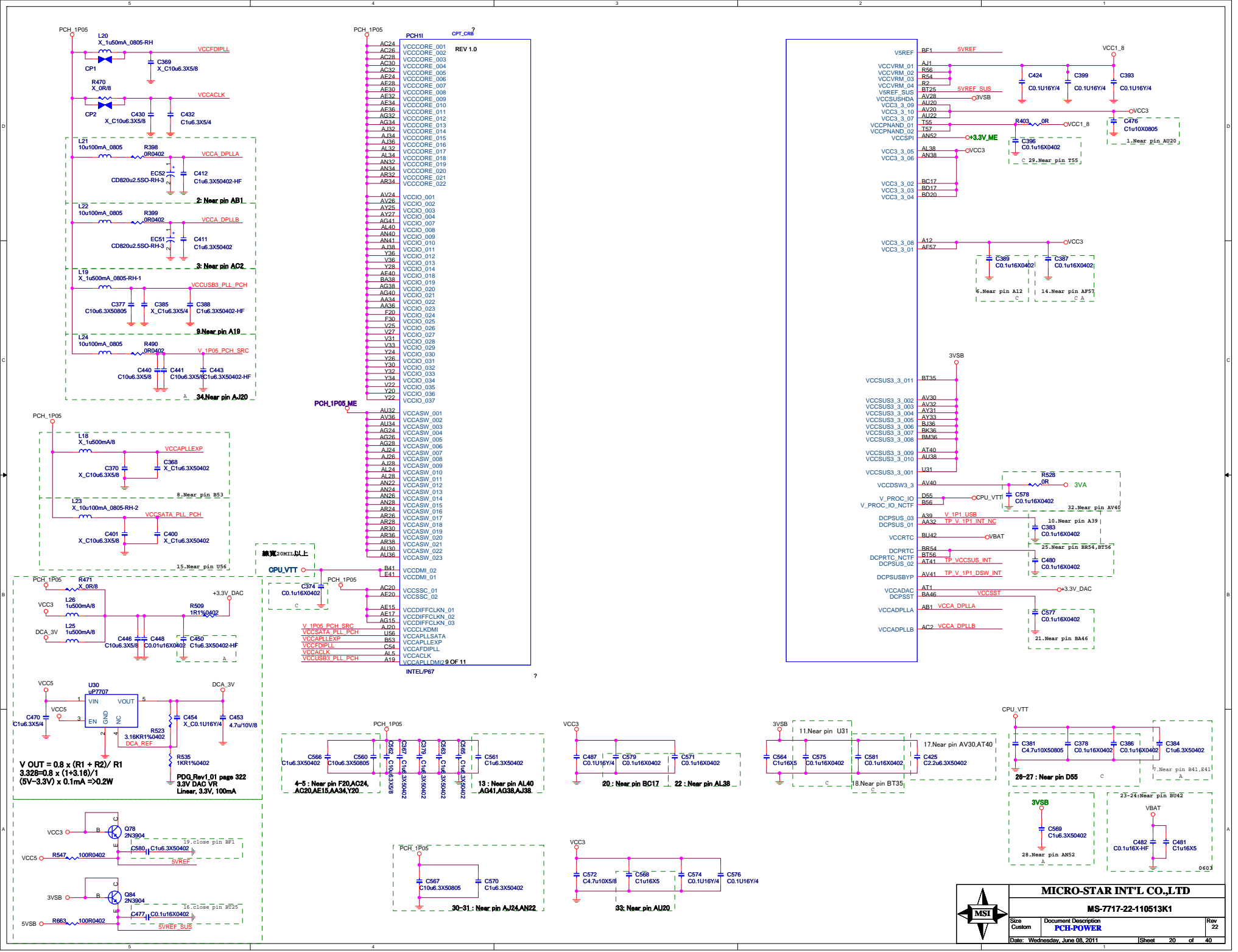
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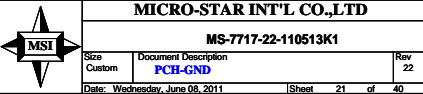
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22

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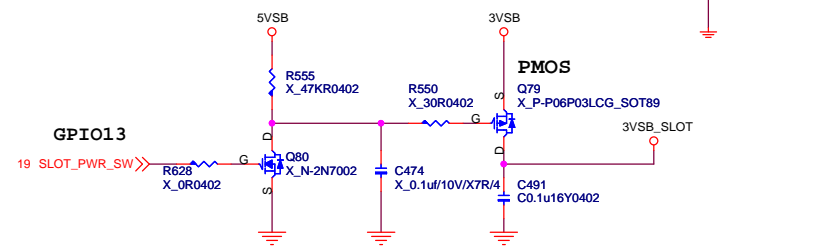
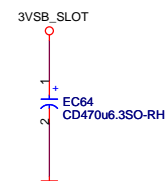
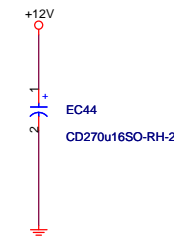
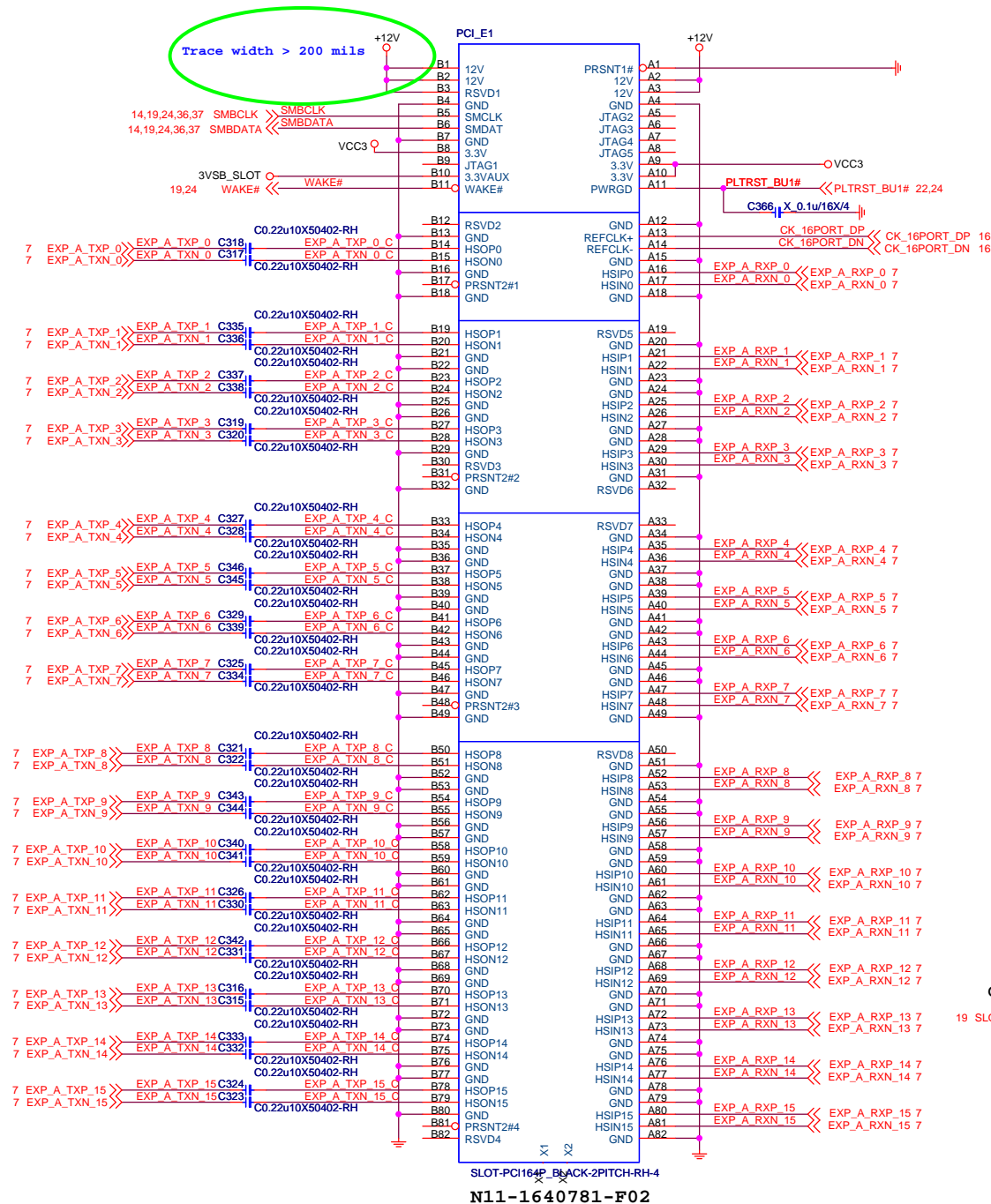
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PCI_Express X16 slot

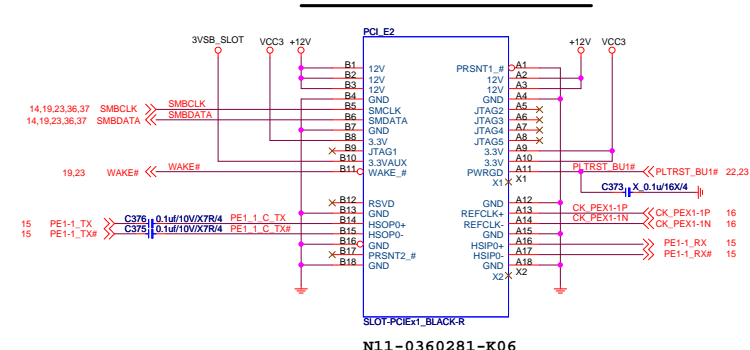


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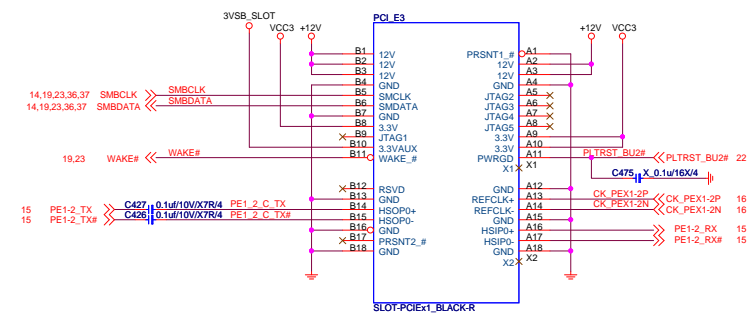
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PCI EXPRESS x1-PORT1

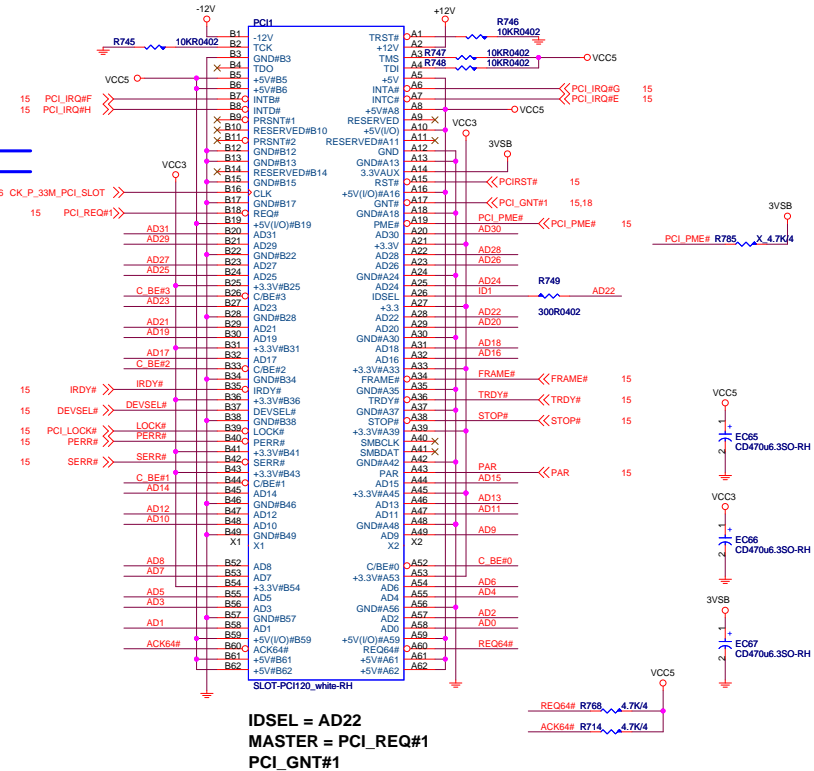


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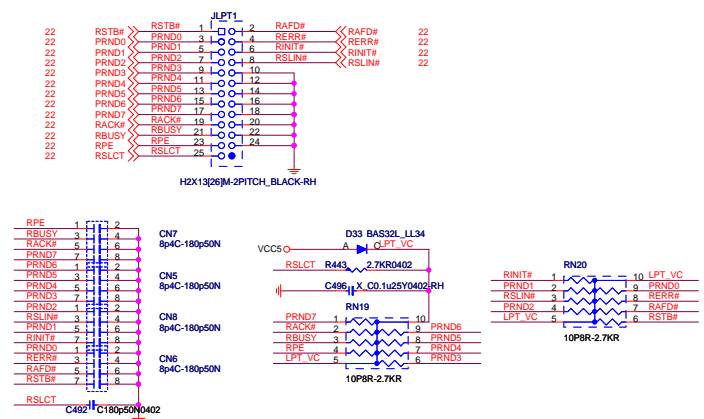
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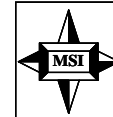
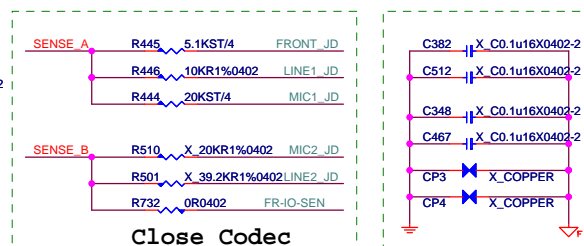
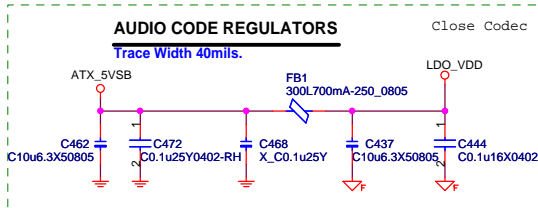
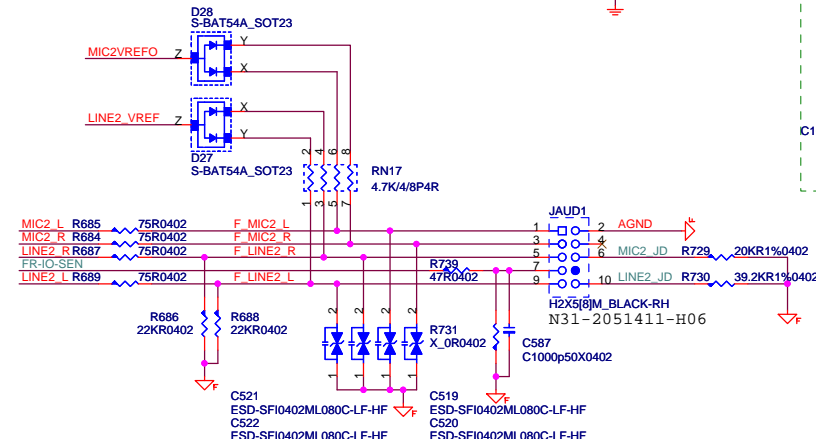
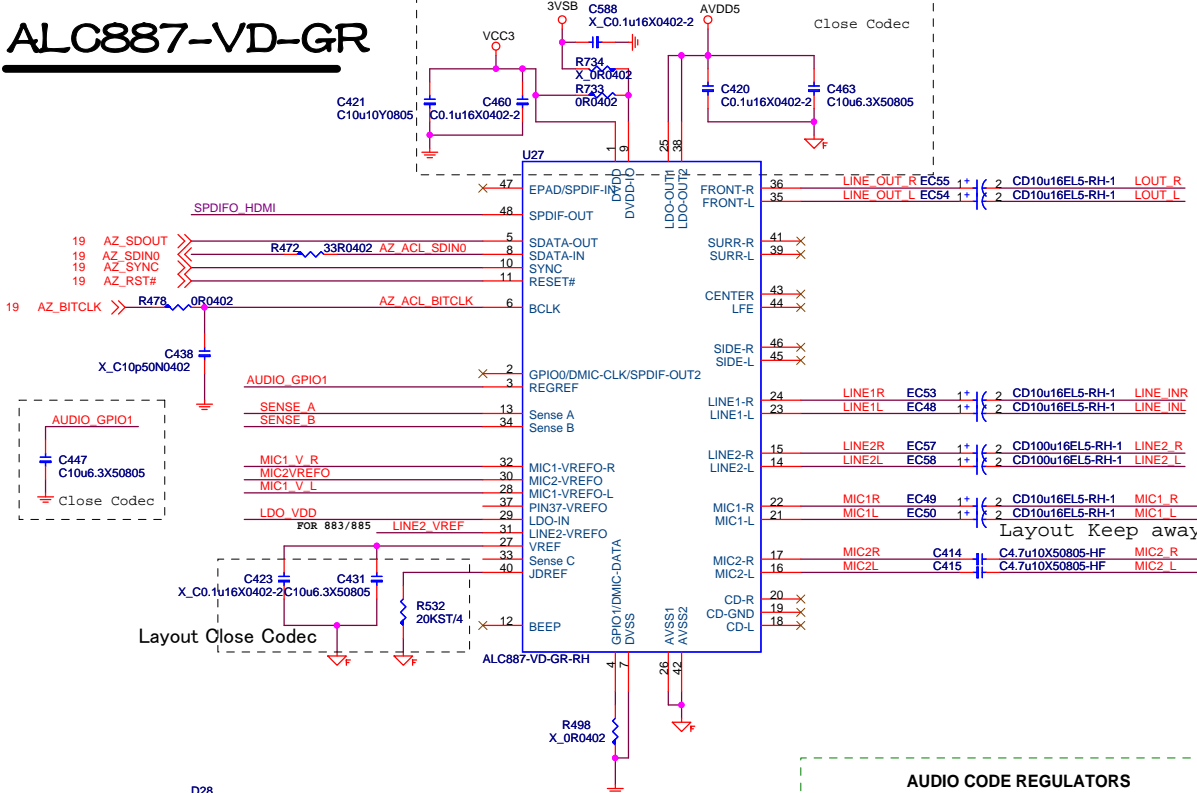
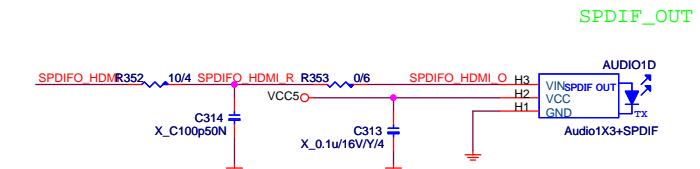
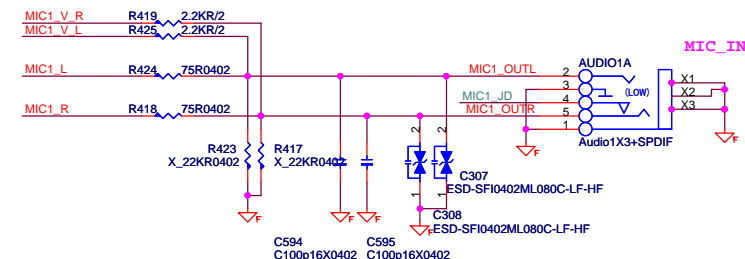
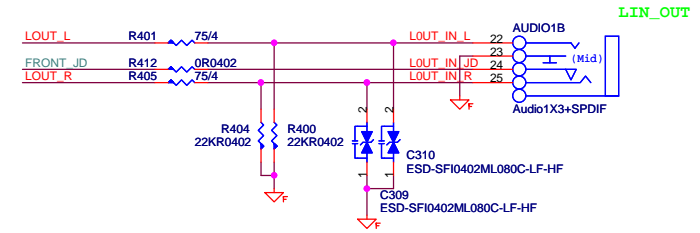
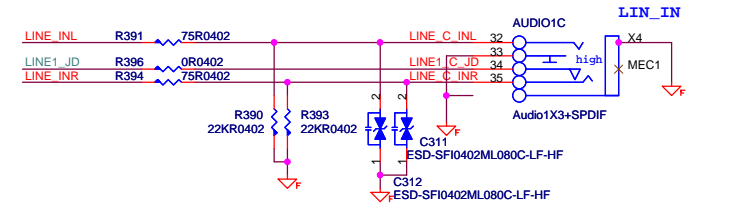


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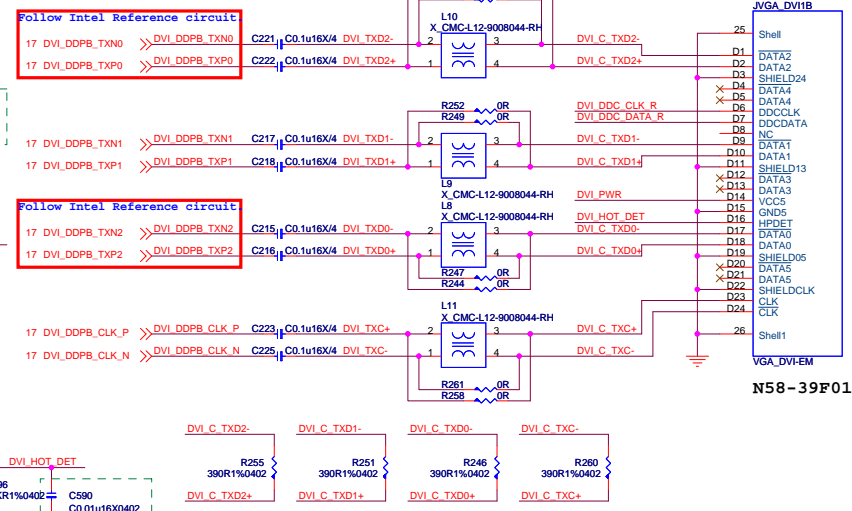
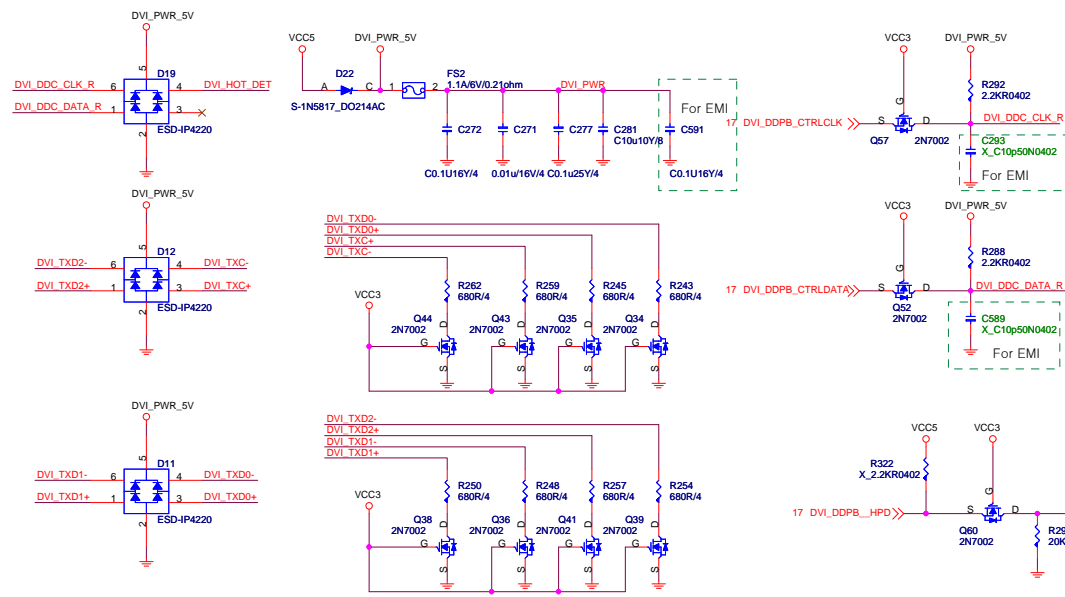
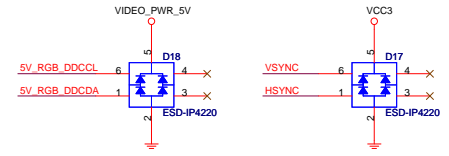
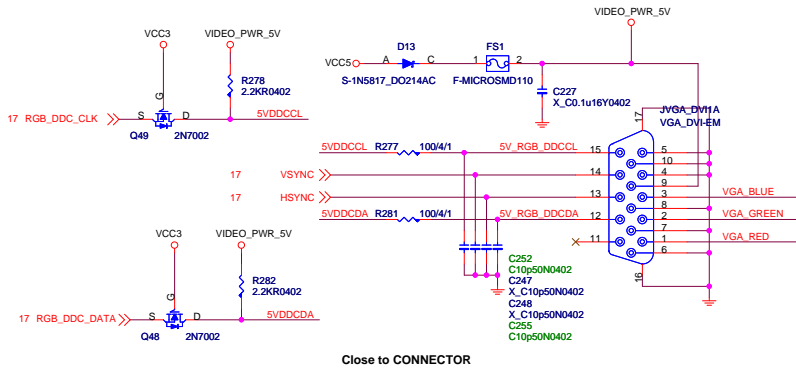
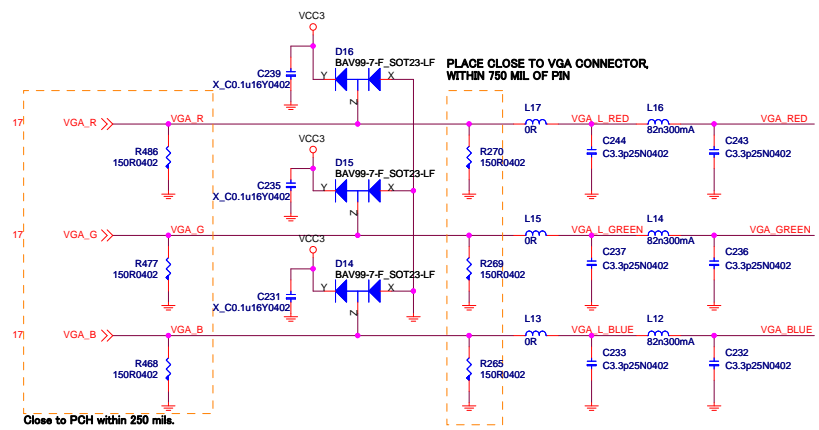


Parallel Port



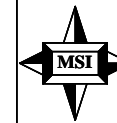
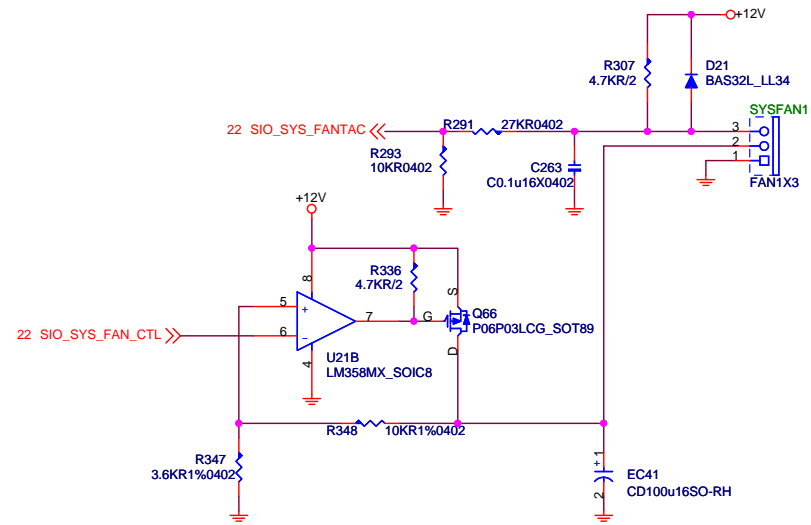
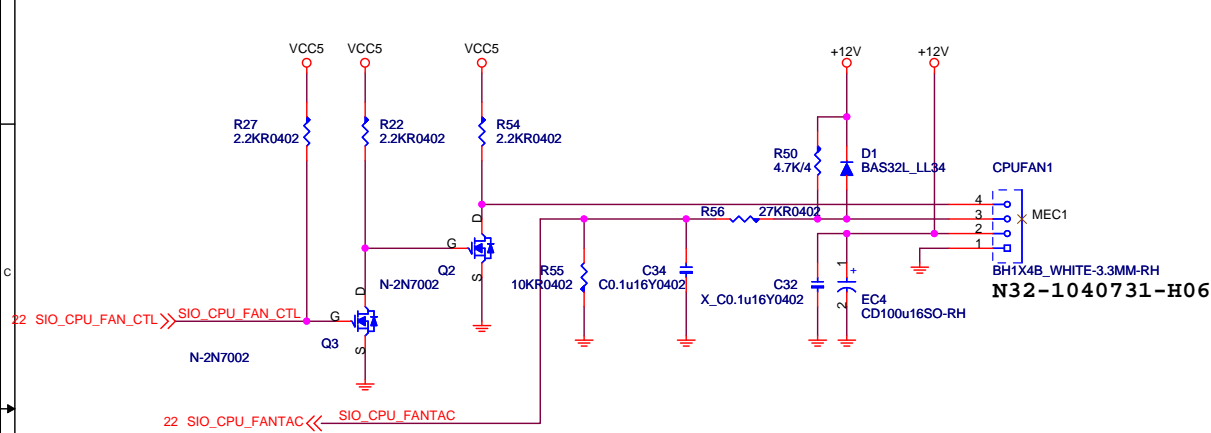


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N58-39F0131-SK7

FAN-COUNTROL CIRCUIT

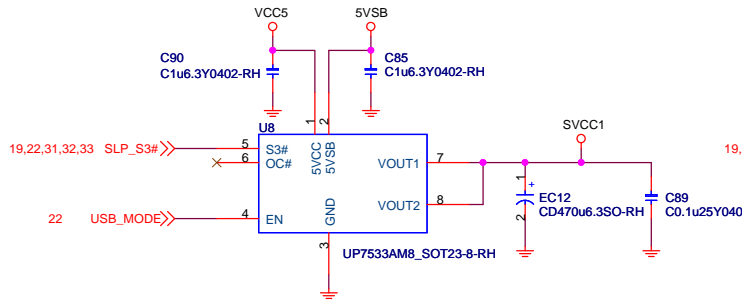


MICRO-STAR INT'L CO.,LTD

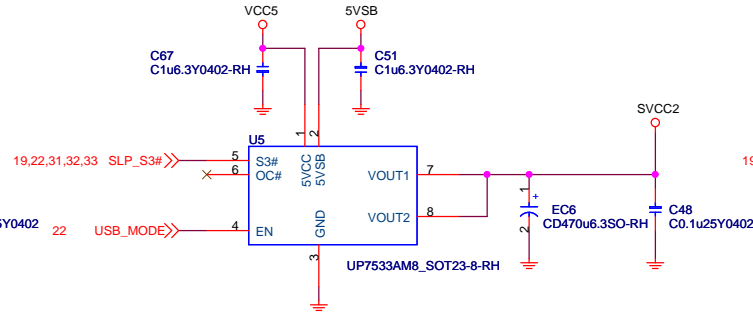
MS-7717-22-110513K1

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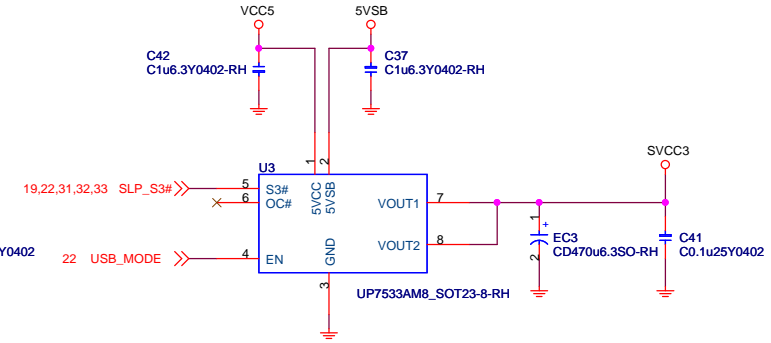
POWER CIRCUIT FOR USB PORT 10, 11



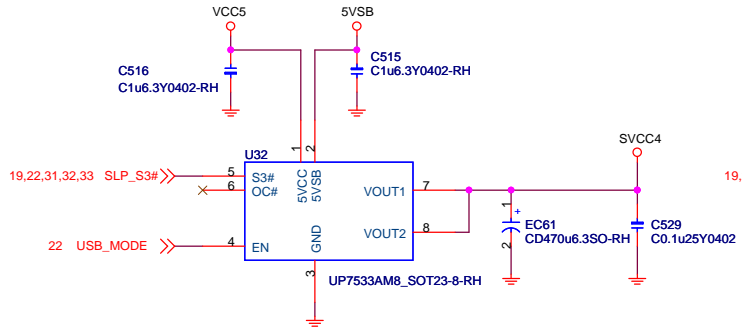
POWER CIRCUIT FOR USB PORT 4, 5



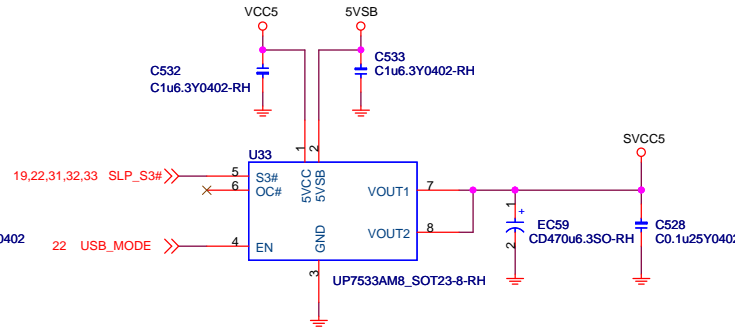
POWER CIRCUIT FOR USB PORT 0, 1



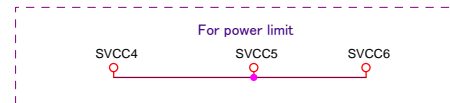
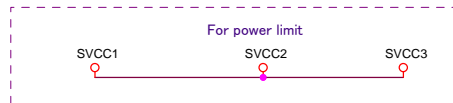
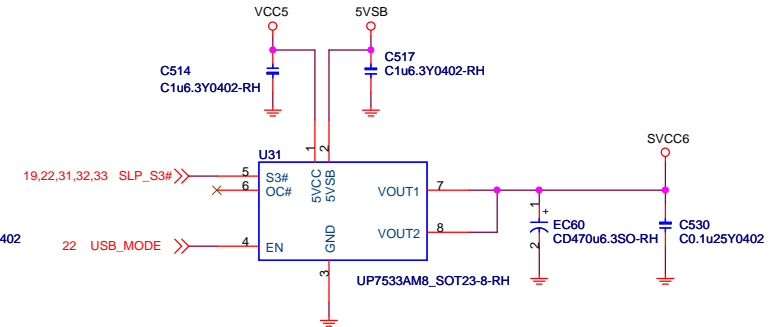
POWER CIRCUIT FOR USB PORT 2, 3



POWER CIRCUIT FOR USB PORT 6, 7



POWER CIRCUIT FOR USB PORT 8, 9

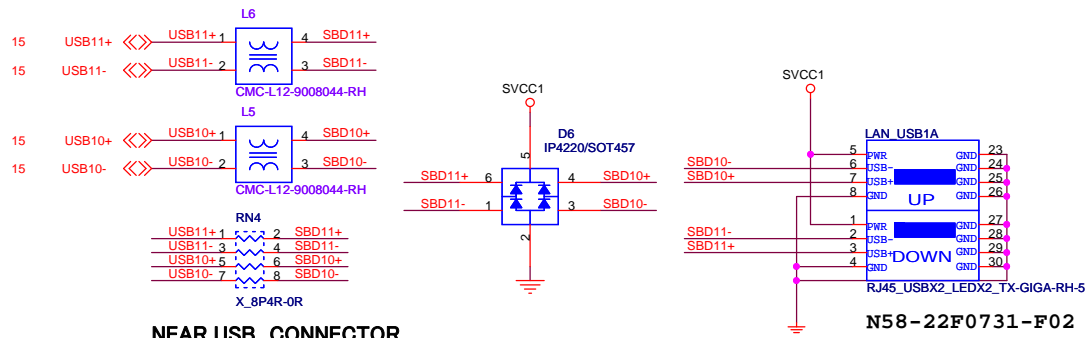


MICRO-STAR INT'L CO.,LTD

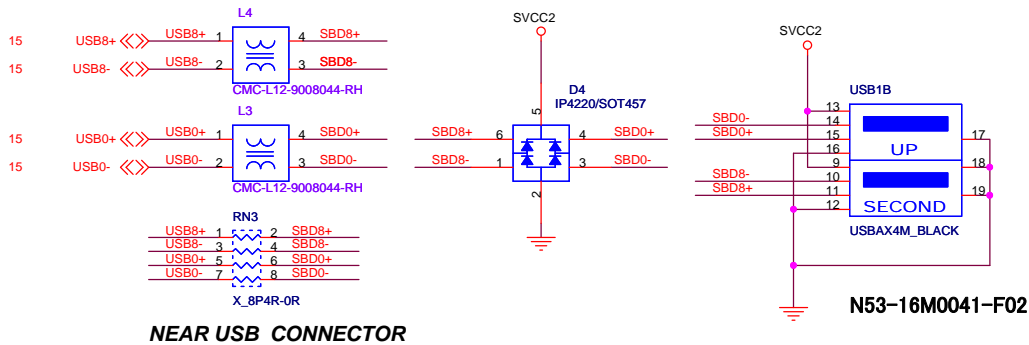
MS-7717-22-110513K1

Size	Document Description	Rev
Custom	USB POWER	22
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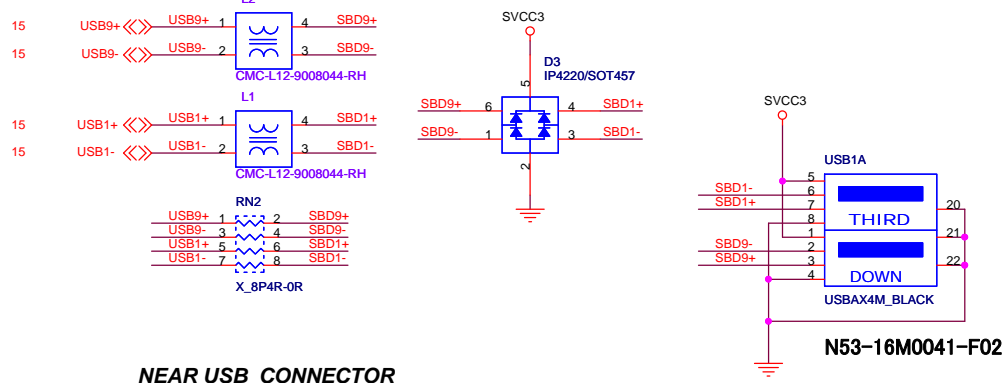
REAR PANEL USB CONNECTOR FOR USB PORT 10,11



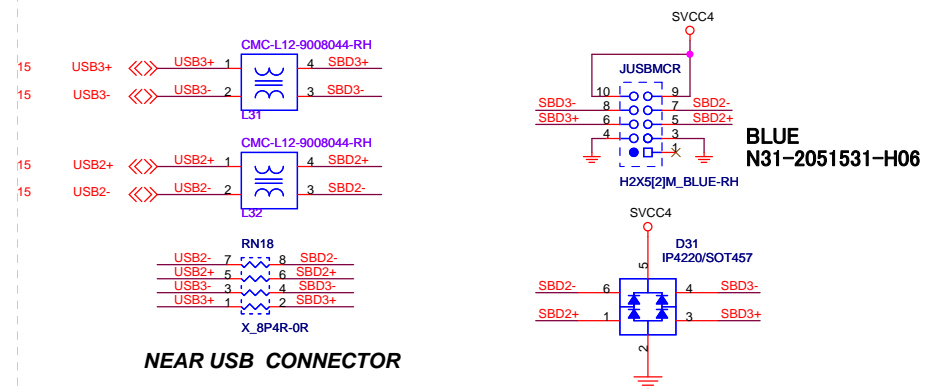
REAR PANEL USB CONNECTOR FOR USB PORT 0,8



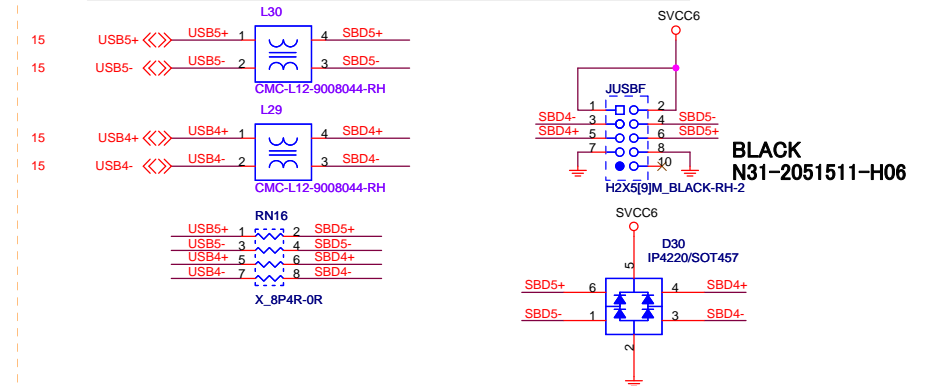
REAR PANEL USB CONNECTOR FOR USB PORT 1,9



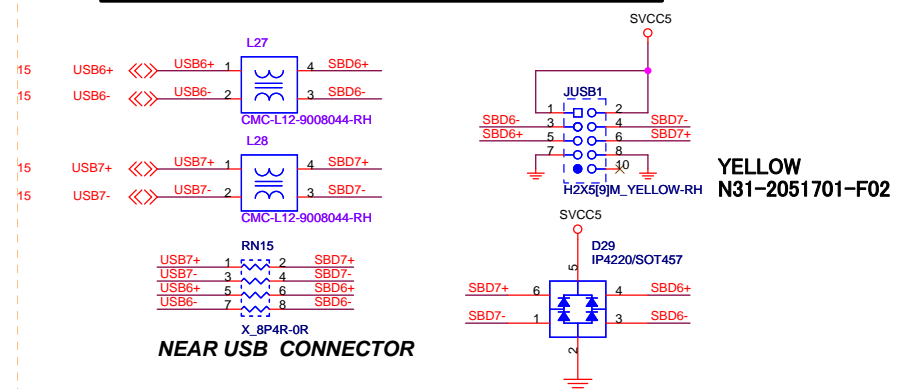
FRONT PANEL USB CONNECTOR FOR USB PORT 2,3



FRONT PANEL USB CONNECTOR FOR USB PORT 12,13



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

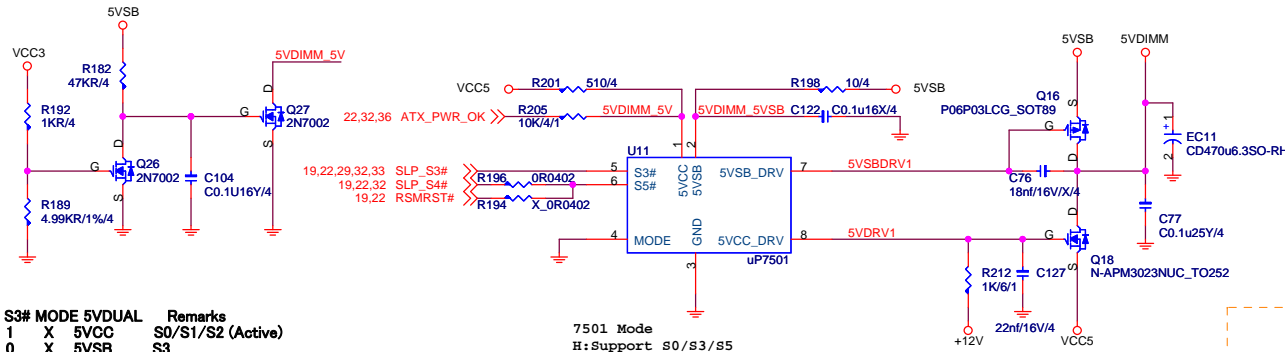


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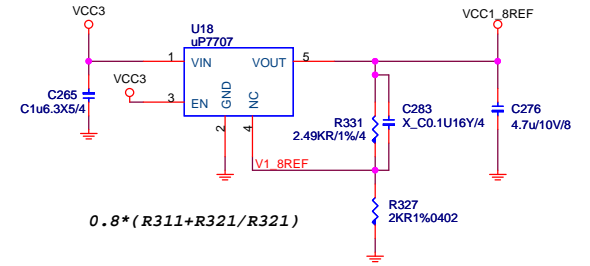
5VDIMM FOR DDR



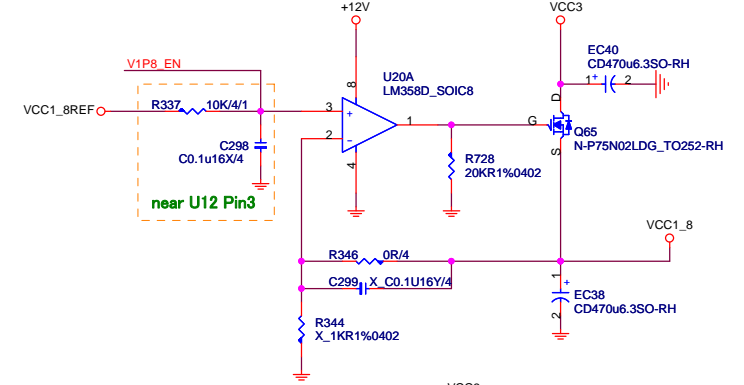
S5#	S3#	MODE	5VDUAL	Remarks
1	1	X	5VCC	S0/S1/S2 (Active)
1	0	X	5VSB	S3
0	X	1	5VSB	S4/S5
0	X	0	Shutdown	S4/S5

```
7501 Mode
H:Support S0/S3/S5
L:Support S0/S3
```

VCC1_8REF

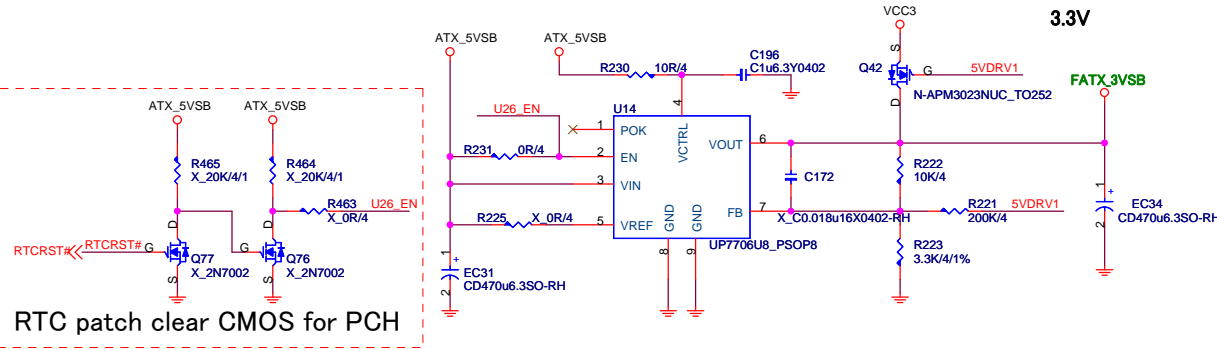


1.8 V Power For CPU & PCH



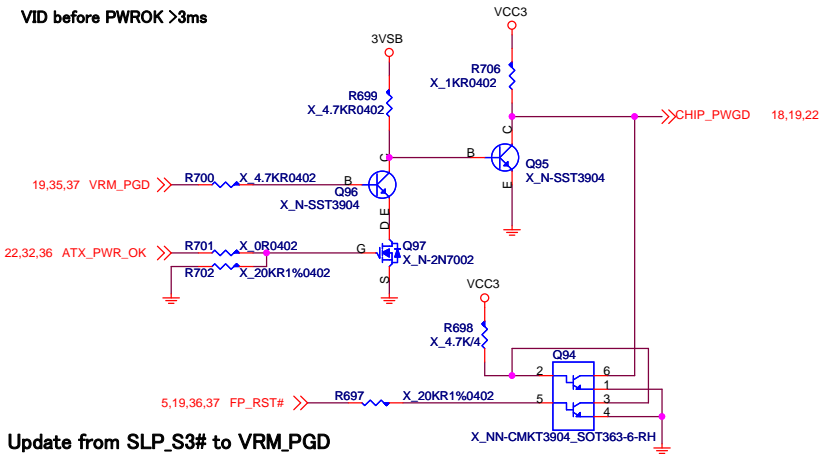
DSW_3VSB

3.3V

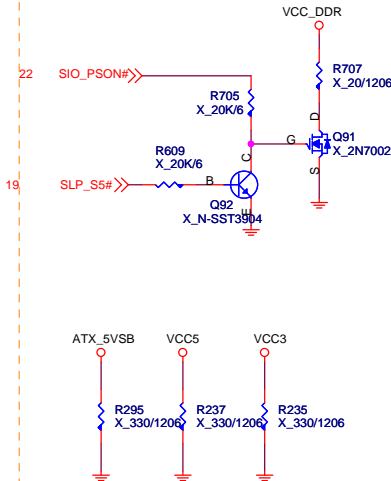


PWROK DELAY

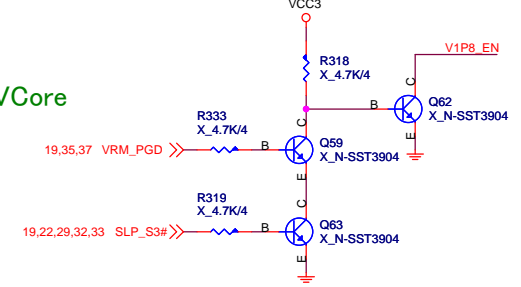
VID before PWROK >3ms



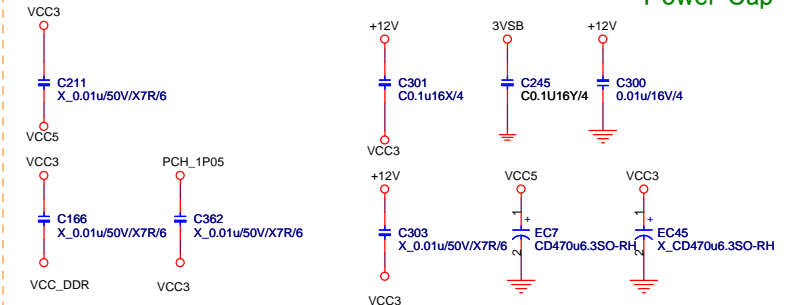
Discharge Circuit



CPUVtt & PCH VCore
wait 1.8v



Power Cap



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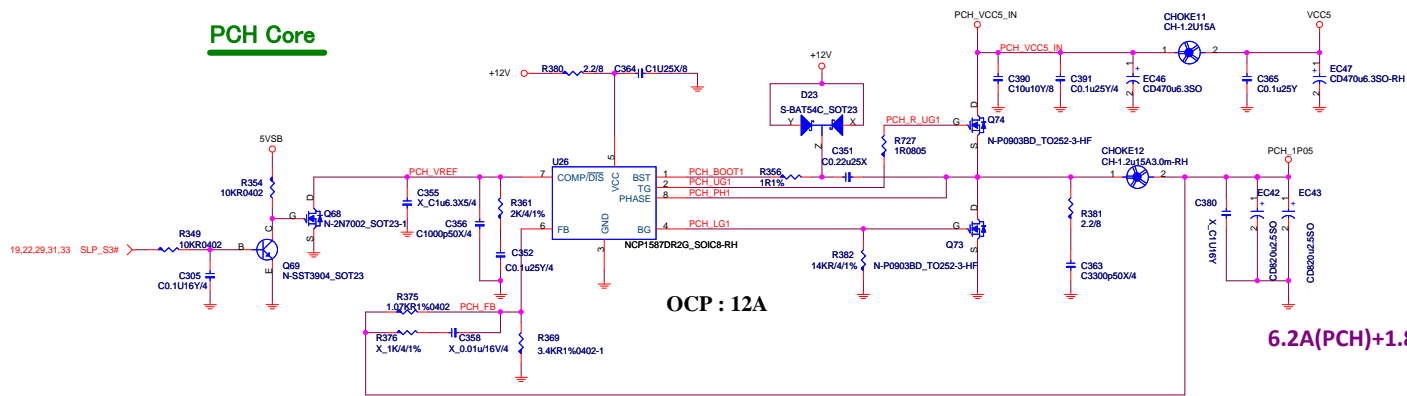
Size Custom	Document Description ACPI Controller 1
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22

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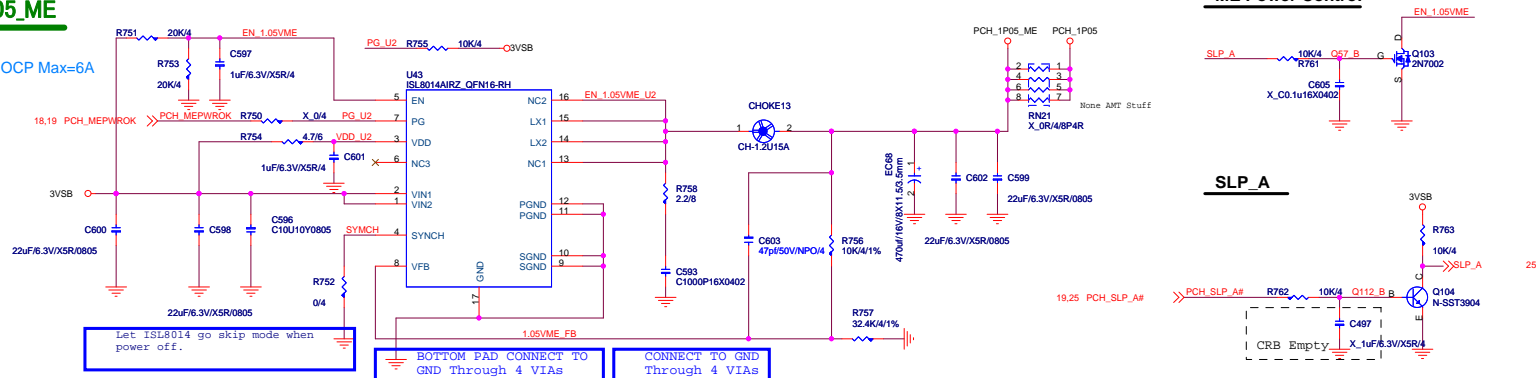
PCH Core



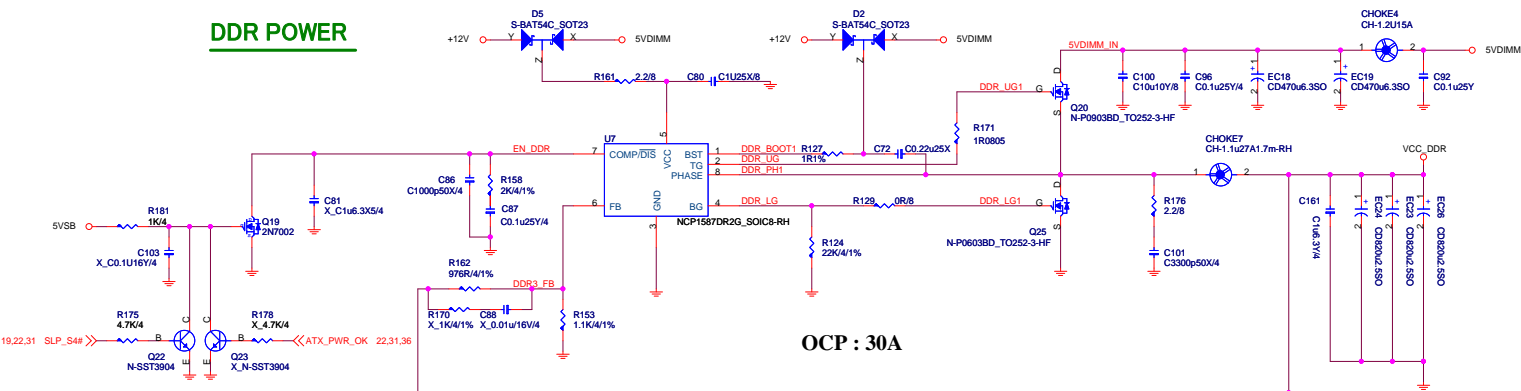
PCH_1P05_ME

 $(4 > 1.8A)$

VCCIO_ME : OCP Max=6A

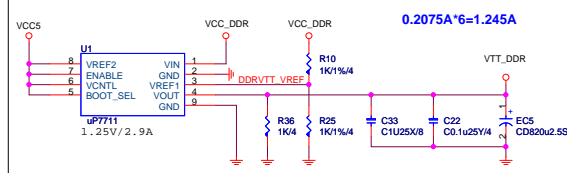


DDR POWER



DDR VTT Power

To CPU Copper trace width > 250mils ,
Fill island behind DIMM > 400mils .

$$0.2075A \cdot 6 = 1.245A$$


DDR3_1.5V
16A



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CPU VTT Power

1.0V/1.05V - (17A-I_{max})

VCCIO_SEL=1 : 1.05V
VCCIO_SEL=0 : 1.00V

VID0=0, VID1=0 -> VCCIO=1.05V
VID0=1, VID1=0 -> VCCIO=1.00V

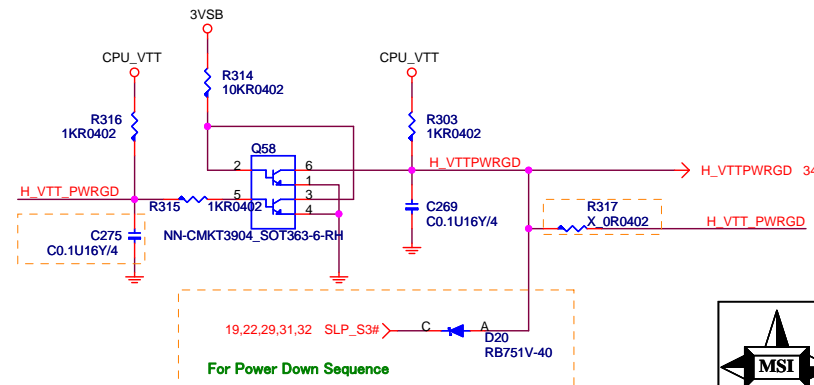
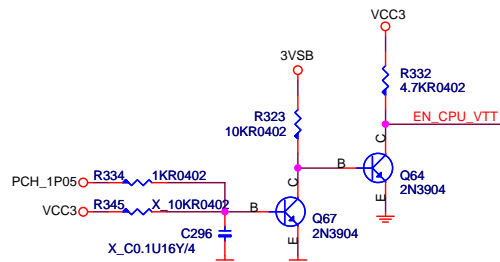
5 VTT_SELECT

5 CPU_VTT_SENSE
5 CPU_VTT_SENSE_RTIN

17A

GND PAD
CONNECT TO
GND THROUGH 4
VIAS

1. $R_{ocset} = I_{out} \cdot DCR / I_{ocset}$; $I_{ocset} = 10uA$
If $DCR = 1m$; $I_{out} = 20A$, $R_{ocset} = 20A \cdot 1m / 10uA \rightarrow R_{ocset} = 2K$
2. $C_{sen} = L / R_{ocset} \cdot DCR$
If $DCR = 1m$; $L = 1U$, $C_{sen} = 1U / 2K \cdot 1m \rightarrow C_{sen} = 0.5U$

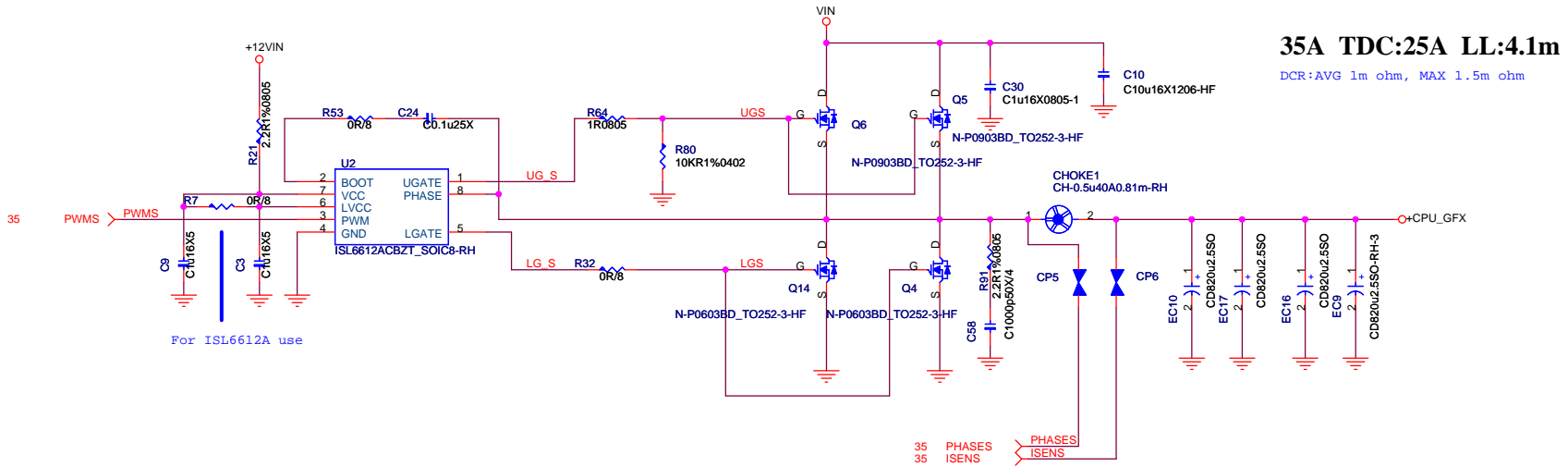


MICRO-STAR INT'L CO.,LTD

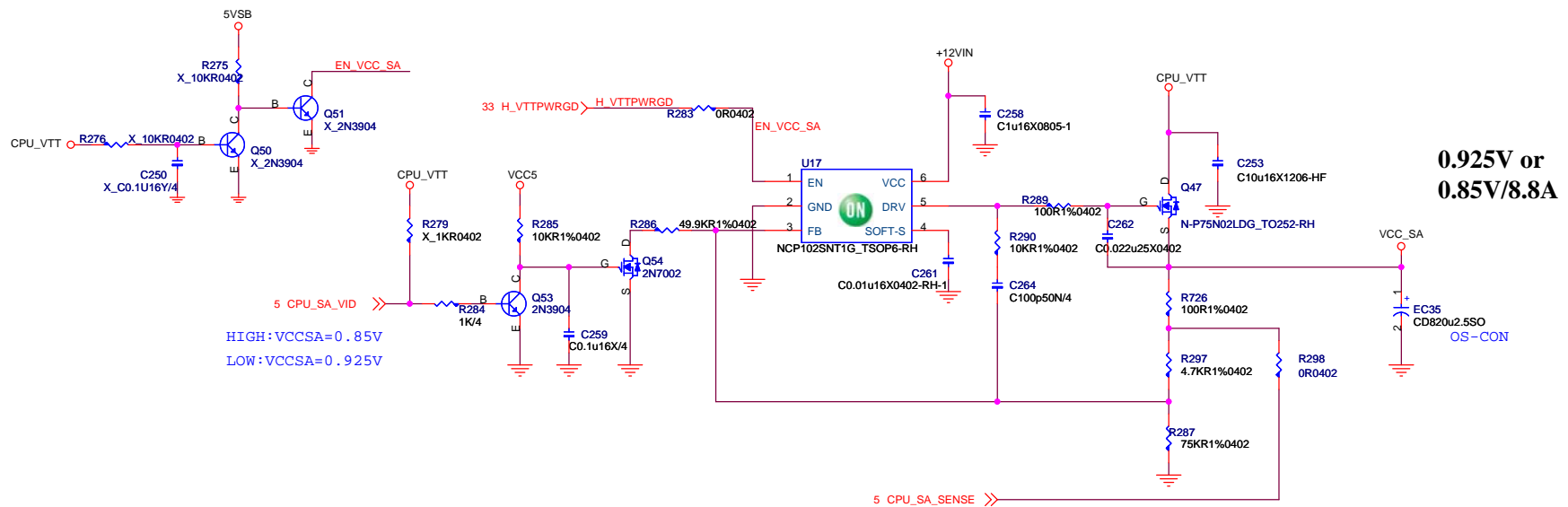
MS-7717-22-110513K1

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GPU POWER



VCCSA



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Size	Custom
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Document Description
GPU Power ISL6625/ISL6622CBZ

Rev
22

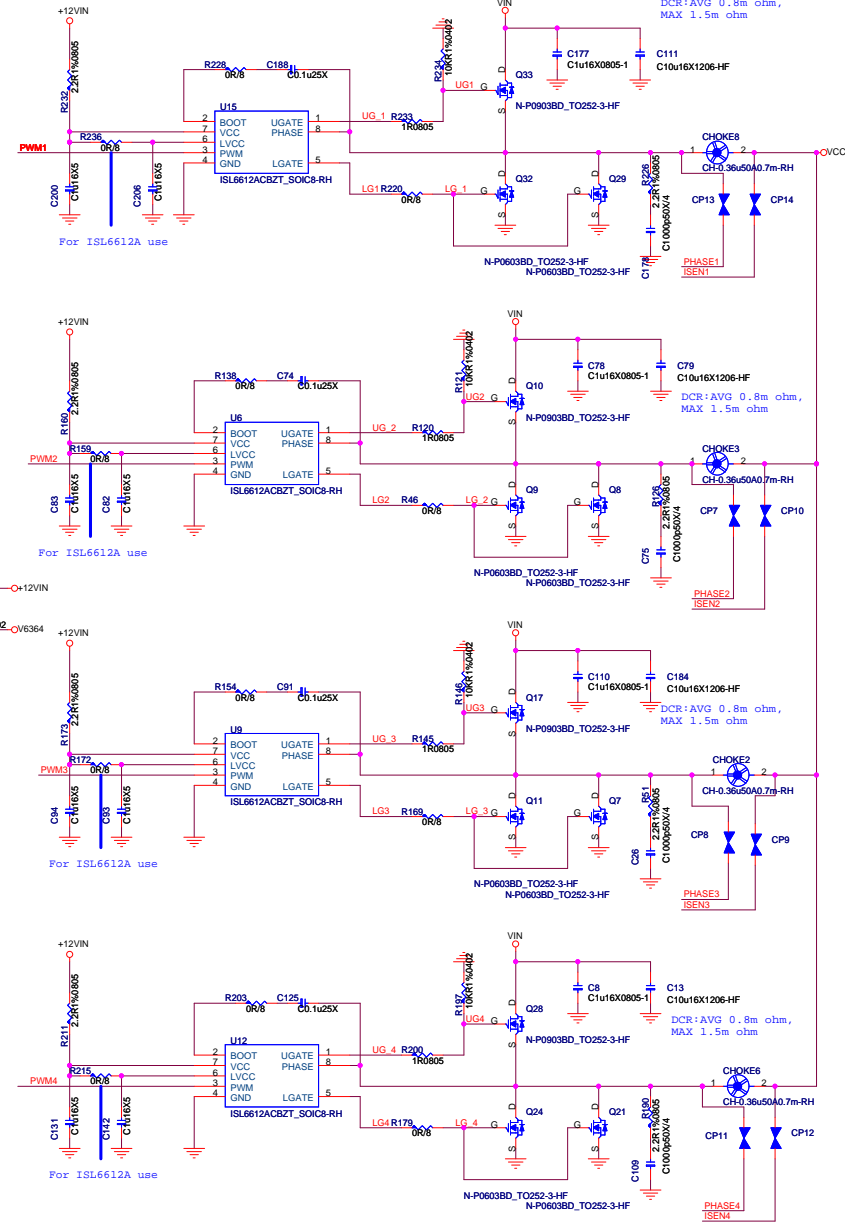
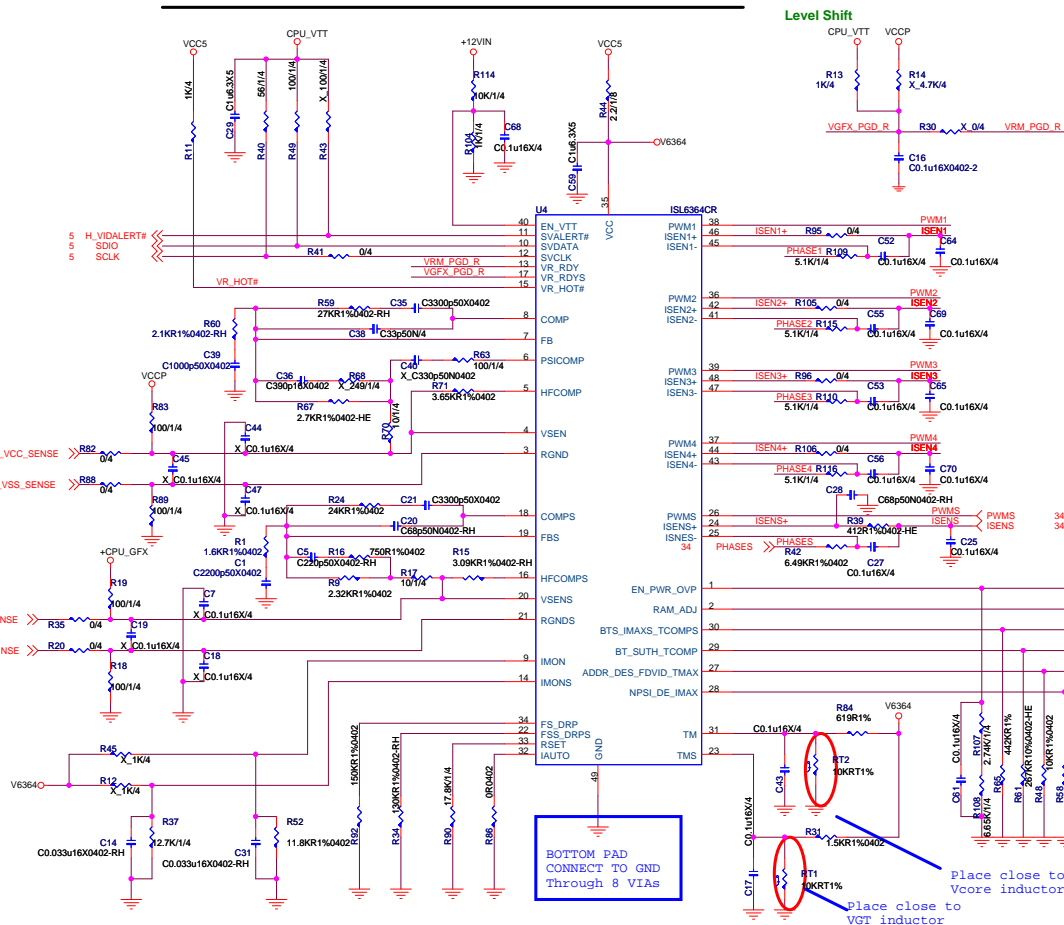
Date: Wednesday, June 08, 2011

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Voltage Regular Module (VRD12)

112A TDC:85A
LL:1.7m

DCR:AVG 0.8m ohm,
MAX 1.5m ohm



DCR:AVG 0.8m ohm,
MAX 1.5m ohm

DCR:AVG 0.8m ohm,
MAX 1.5m ohm

DCR:AVG 0.8m ohm,
MAX 1.5m ohm

OS-CON CAP

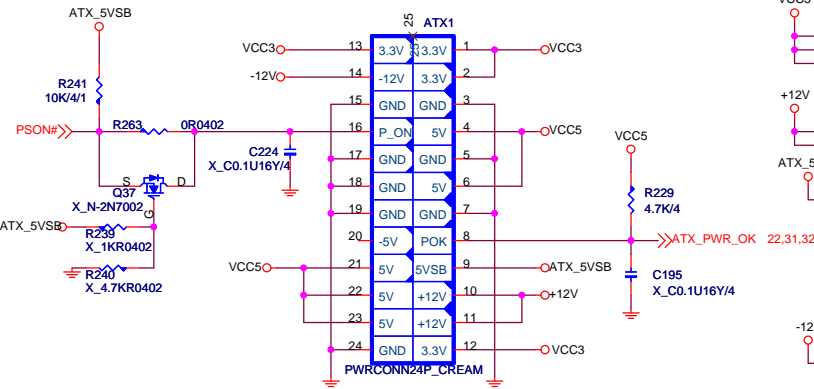


MICRO-STAR INT'L CO.,LTD

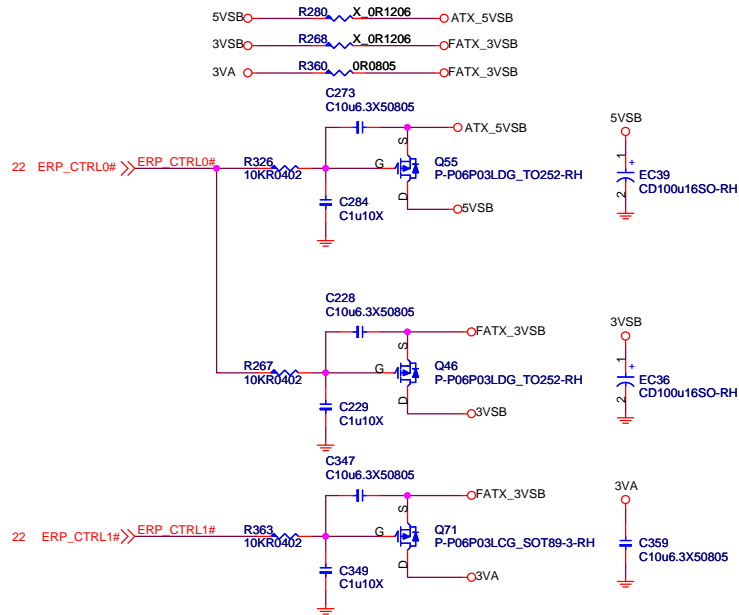
MS-7717-22-110513K1

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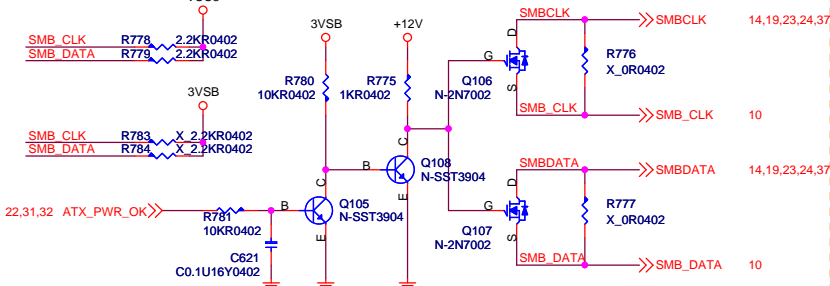
ATX POWER CONNECTOR



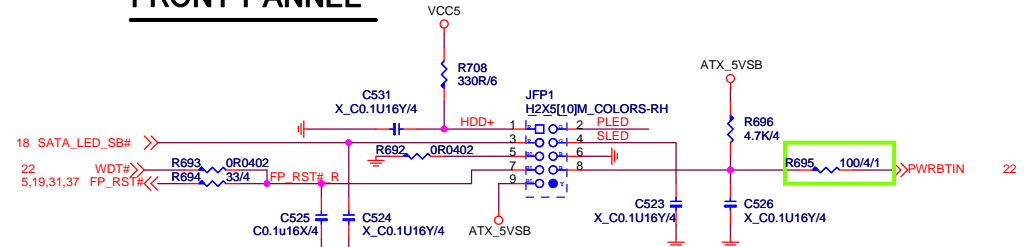
DSW POWER CONTROL



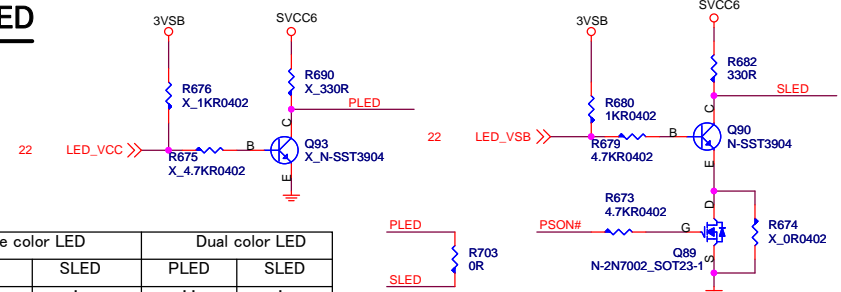
SMB Isolation



FRONT PANNEL

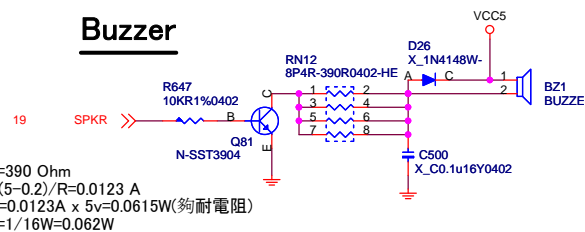


LED

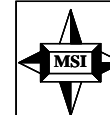
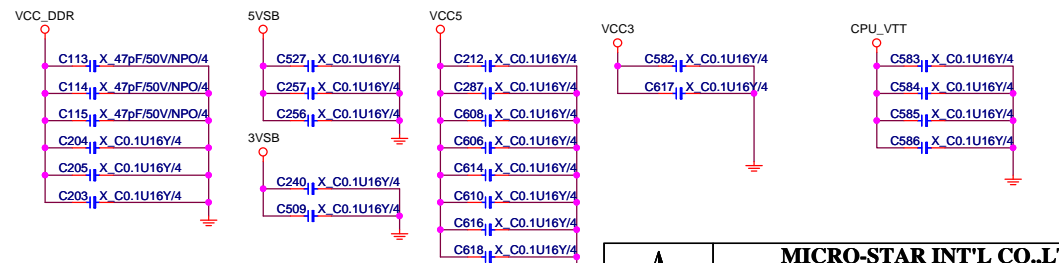


	Single color LED		Dual color LED	
	PLED	SLED	PLED	SLED
S0	H	L	H	L
S1/S3	Blinking	Blinking	L	H
S4/S5	L	L	L	L

Buzzer



For EMI

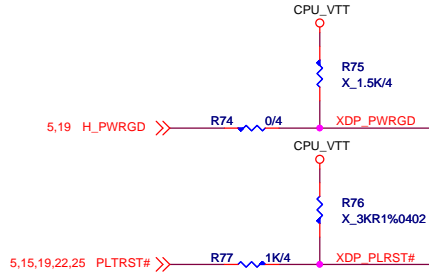


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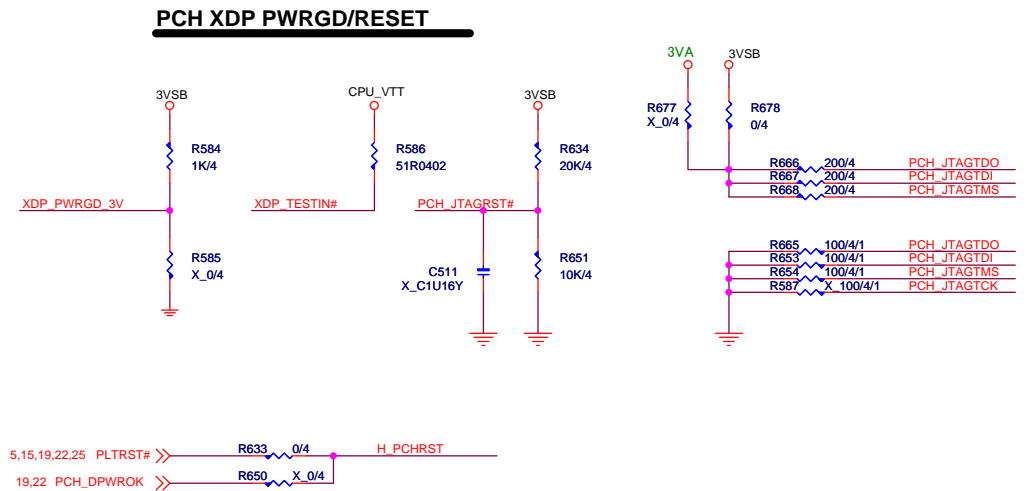
Size	Document Description	Rev
Custom	ATX PWR/LED/DSW	22
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CPU XDP



N5C-60F0040-S88

PCH XDP



N5C-60F0040-S88



MICRO-STAR INT'L CO.,LTD

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Size	
Custom	

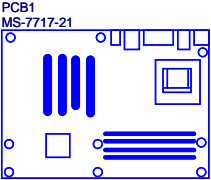
Document Description
CPU/PCH XDP

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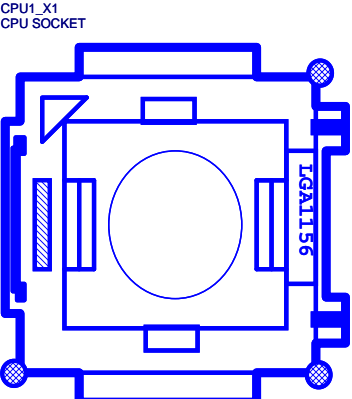
PCB



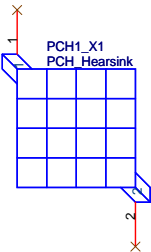
PCB
PN : P30-0771722-G37
AVL : P30-0771722-E36



CPU SOCKET

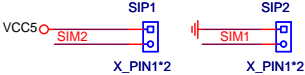


E21-7557050-L06

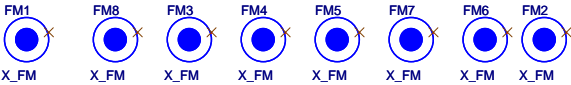


E31-0401634-K08

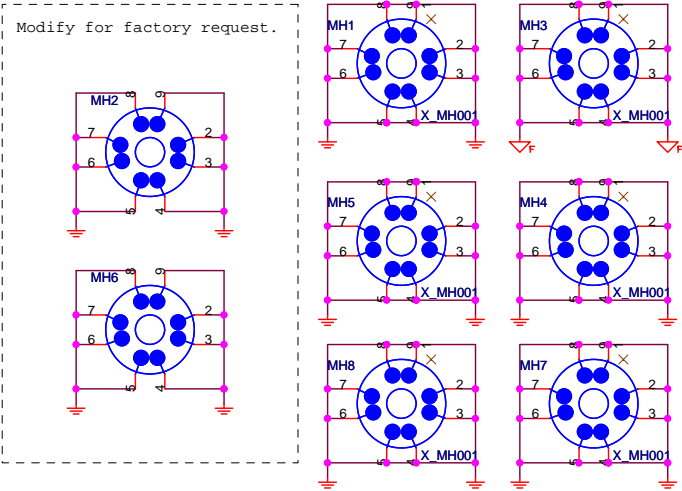
Simulation



Optical Fiducial Marks-120



Mounting Holes



1.EC63 change to 330uF C71-33102YE-P01 For power solution
2.CHOKE1 change to 0.5uH L04-05A7211-L65 For power solution
3.R42 change to 6.2K Ohm R11-0622T12-W08 For power solution
4.R39 change to 412 Ohm R11-4120T12-W08 For power solution
5.R9 change to 2.05K Ohm R11-2051T12-W08 For power solution
6.R84 change to 2.7K Ohm R11-0272T13-W08 For power solution
7.R92 change to 180K Ohm R11-0184T12-W08 For power solution
8.R34 change to 180K Ohm R11-0184T12-W08 For power solution
9.R67 change to 2.7K Ohm R11-0272T12-W08 For power solution
10.R24 change to 10K Ohm R11-0103T12-W08 For power solution
11.C21 Keep 2.2nF C11-2222022-W08 For power solution
12.C20 change to 68pF C11-6801812-W08 For power solution
13.R15 change to 2.15K Ohm R11-2151T12-W08 For power solution
14.C5 Keep 1nF C11-1022012-W08 For power solution
15.R71 change to 3.65K Ohm R11-3651T12-W08 For power solution
16.C35 change to 3.3nF C11-3322012-W08 For power solution
17.R59 change to 10K Ohm R11-0103T12-W08 For power solution
18.C40 Keep 330pF C11-3311812-W08 For power solution
19.EC9 change to 820uF C71-8210271-N07 For power solution
20.C139 change to 47uF C11-4767224-M09 For power solution
21.C537 change to 47uF C11-4767224-M09 For power solution
22.C538 change to 47uF C11-4767224-M09 For power solution
23.C539 change to 47uF C11-4767224-M09 For power solution
24.C540 change to 47uF C11-4767224-M09 For power solution
25.C541 change to 47uF C11-4767224-M09 For power solution
26.c1 change to 2.2nF C11-2222022-W08 For power solution
27.Add Q100 Q101 R742 R737 R740 for HAD_SDO(JBAT2) jumper change
28.Add R733 R735 Not Stuff R734 R649 C588 for HAD_SDO Reserved
29.Add R728 For U20.G driving pin loading
30.Not Stuff R515 R529 For double pull-up
31.Not Stuff R280,R268 For Deep Sleep
32.Add R730 R732 R739 C587 R729 Not Stuff R501 R731 R510 For Audio jack detection change
33.Not Stuff R692 For Touch switc
34.C105 C106 change to 27pF For made Y1 more close 25MHz
35.R375 change to 1.07k ohm For adjust PCH_1P05 more close 1.05V
36. Add C293 C589 C591 C590For EMI
37.R246 R251 R255 R260 change to180 ohm For EMI
38.Reserve C592 For EMI
39.change PCIE X16 SLOT remove JP1
40.change D7 D8 footprint the same with D9D10
41.Change the power source from ATX_5VSB
42.Add C594 C595 For Rear Mic port circuit
43.Add CP17 For EMI
44. R65 change to 442k Ohm For power solution
45. R66 change to 365k Ohm For power solution
46. R31 change to 1.5k Ohm For power solution
47. RT1 change to 10k Ohm For power solution
48. R92 change to 150k Ohm For power solution
49. R34 change to 130k Ohm For power solution
50. R42 change to 7.5k Ohm For power solution
51. R9 change to 2.32k Ohm For power solution
52. R24 change to 34.8k Ohm For power solution
53. R93 change to 1m Ohm For power solution
54. R59 change to 27k Ohm For power solution
55. C20 change to 33pF For power solution
56. C21 change to 3.3nF For power solution
57. C149 change to 47uF For power solution
58. C40 change to NC For power solution
59. R15 change to NC For power solution
60. Add R343 and Q61 change to 3904 Reserve R320.Q56 For power solution
61. PCIE _E1 Chang Footprint to SLOT_PCIEXP164_3
62. 3VDual Disable circuit Q76,Q77,R463,R464,R465 change to reserve
63. R740 pull to VCC5,R738 pull to 5VSB
64. Add D32 ,C4 ,CP18 For EMI
65 R246 R251 R255 R260 change to 330ohm
66 Add PECl sot 3VSB CAP EC64 R741 page 23
67.REmove CP18 For EMI requests
68.R84 change to 2k Ohm For power solution
69.R67 change to 3.3k Ohm For power solution

V10 Modify List:

1. R15 Change to 3.09k Ohm P/N: R11-3091T12-W08 For power solution
2. R16 Change to 750 Ohm P/N: R11-0751T12-R01 For power solution
3. R24 Change to 24K Ohm P/N: R11-0243T12-W08 For power solution
4. R42 Change to 6.49K Ohm P/N: R11-6491T12-W08 For power solution
5. R52 Change to 11.8K Ohm P/N: R11-1182T12-W08 For power solution
6. R61 Change to 267K Ohm P/N: R11-2673T12-Y01 For power solution
7. R62 Change to 866KOhm P/N: R11-8663T12-W08 For power solution
8. R67 Change to 2.7k Ohm P/N: R11-0272T12-W08 For power solution
9. R84 Change to 619Ohm P/N: R11-6190T12-W08 For power solution
10. R86 Change to 0 Ohm P/N: R11-0000012-W08 For power solution
11. RT2 Change to 10K Ohm P/N: R51-0103T13-M05 For power solution
12. C5? Change to 220 pF P/N: C11-2212812-W08 For power solution
13. C16 Change to 0.1 uF P/N: C11-1047512-W08 For power solution
14. C20 Change to 68 pF P/N: C11-6801812-W08 For power solution
15. R68 Remov For power solution
16. C247 Remove For D-sub SA
17. C248 Remove For D-sub SA

2.0 Modify List:

1. 2011 01 20 Modify and Add the power item for ME power Page.32
2. 2011 01 20 Add TPM function Page.32
3. 2011 01 20 Add the PCI Slot Page.24 (The layout trace spacing is 4/4/5 and impact the PCI trace law in Design Guide (4/5/5) because the spacing is not enough in MB after add PCI function.)
4. 2011 01 20 Add the parallel pin header Page.24
5. 2011 01 21 Add EMI reservr CAP C606,C614,C610,C616,C608
6. 2011 01 24 Modify the R749 from 100ohm to 300ohm
7. 2011 01 25 Modify the C607,C609 value from 12p to 15p
8. 2011 01 26 Add EMI requirement the C617,C618 value 104p

2.1 Modify List:

1. 2011 03 08 Modify value R255.R251.R246.R260 from 330ohm to 390ohm
2. 2011 03 08 Add Q102,R759,C604 and unload R850 for ME +3.3V_ME power
3. 2011 03 12 Add R772 and resever C620,619 for LAN power

2.2 Modify List:

1. 2011 05 18 Add solution for ME MOff wakeup issue.
Add Part :Q106,Q107,Q105,Q108,R775,R773,R774,R778,R779,R780,R781,C621
Remove Part: R642,R659
2. 2011 05 18 Modify LAN Voltage schematic
Modify Part : R772 from 10k to 0 ohm; R214 from 4.7k to 15k ohm
3. 2011 05 20 Stuff R551 for support ME function.
4. 2011 05 20 Use R782 to Cut of SPL_WP# reference CRB design.
Reserve GPIO32(SPL_WP#) pull-high to VCC3 with R786
5. 2011 05 20 Reserve PCL_PME# pull-high to 3VSB
6. 2011 05 20 Reserve GPIO33(SPL_HOLD_GPO#) pull-high to VCC3 with R787
7. 2011 05 20 Change the SATA2 connector color from RED to BLUE.
Change the SATA3 color from BLUE to Orange.



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