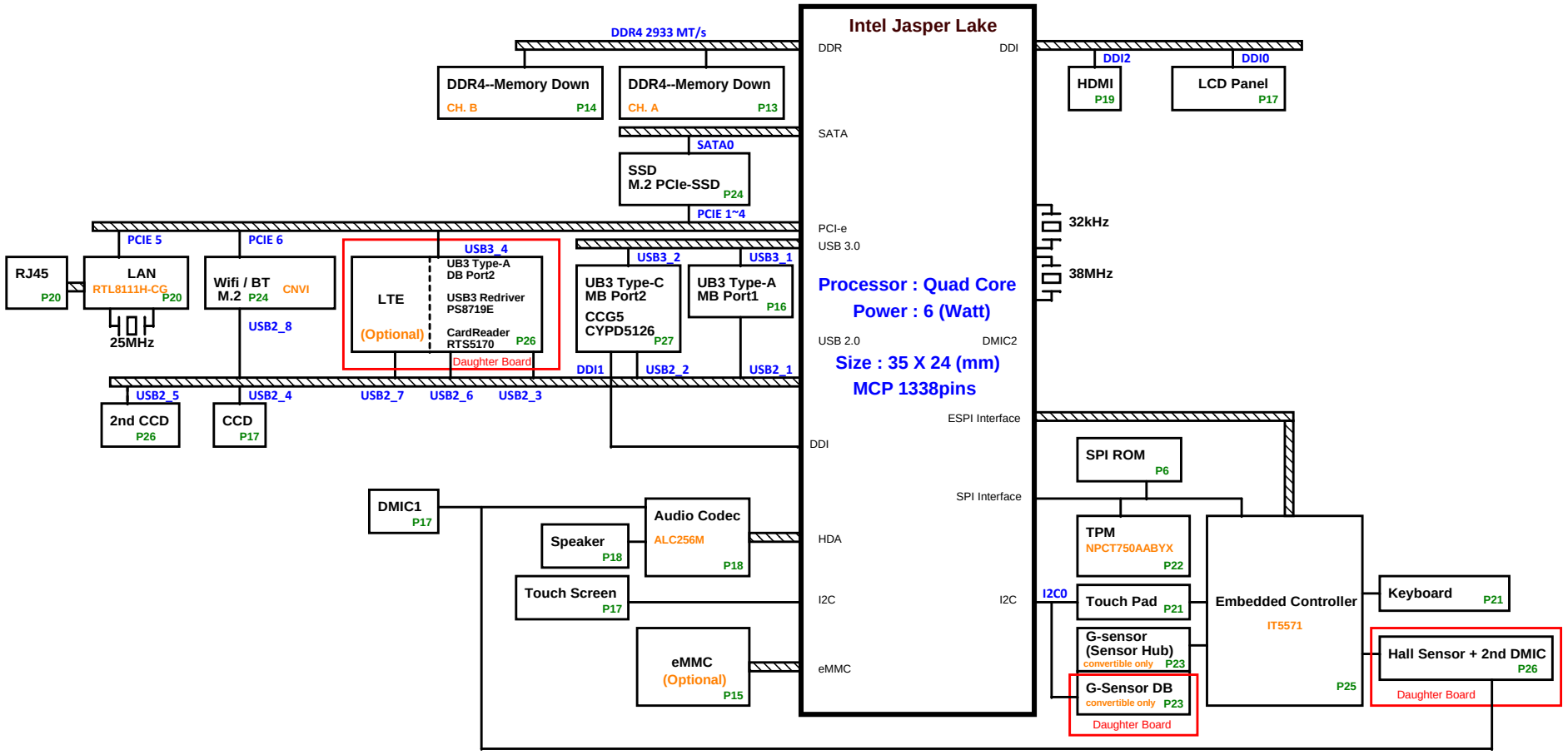
ZBK ZBKA Intel JSL Platform Block Diagram

01



BOM option

MMC@ : eMMC function
MMC_N@ : No eMMC function
CON_GS@:Convertible+G Sensor
CLM@:Clamshell
MP@:CPU MP
QS@:CPUQS
TSI@ : Touch screen I2C
TSI_N@ : No Touch screen
MDB@:B channel
OCH@:One chennel
SSD@:Solid-state disk
P_SSD@ : PCIE Solid-state disk
S_SSD@ : SATA Solid-state disk
DBG@ : for Debug Functiion
SP@:Special Part
LAN@:LAN Power
LTE@:LTE

Power solution

Batery Charger ISL9241HRTZ-T P31	+VNN_EXT SYV659LQWC P34	+2.5V_SUS JW5252SOTB#TRPBF P35	+1.8V AOSS32334C P38	+VCCST DMG3414U-7 P12
+3VPCU/+5VPCU RT6256BGQUF P32	+1.05V_EXT SYV659LQWC P34		+1.2V_S5 JW5252SOTB#TRPBF P38	
+3V_S5/+5V_S5 JW7110DFNC P32	+1.2VSUS G5619RZ1U P35	+VCCIN UP9523QQKI P36	+VCCPLL_OC DMG3414U-7 P12	
+3V/+5V JW7110DFNC P32	+VDDQ_VTT G5619RZ1U P35	+VCCIN_AUX RT6543AGQW P37	+VCC1P8A DMG3414U-7 P12	
+VCCIO NB692GD-Z P33	+VDDQ G5619RZ1U P35	+1.8V_S5 JW5213DFND_TRPBF P38	Thermal protection TMP708AIDBVR P34	

LED P17
Daughter Board

Quanta Computer Inc.
PROJECT : ZBK_ZBKA

Size	Document Number	Rev
	Block Diagram	1A

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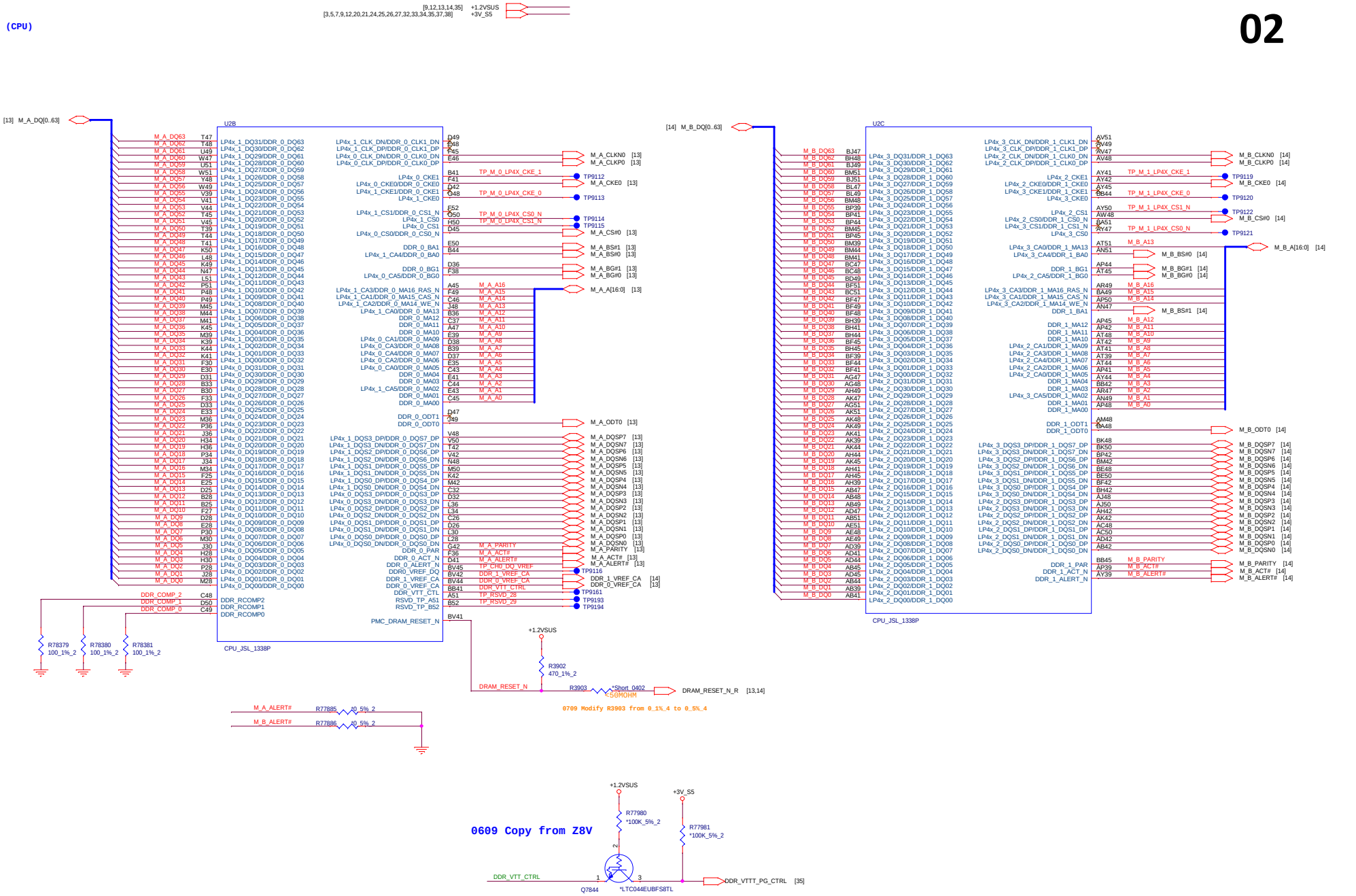
(CPU)

02



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PROJECT : ZBK_ZBKA		
Size	Document Number: JSL+: MEMORY	Rev: 1A
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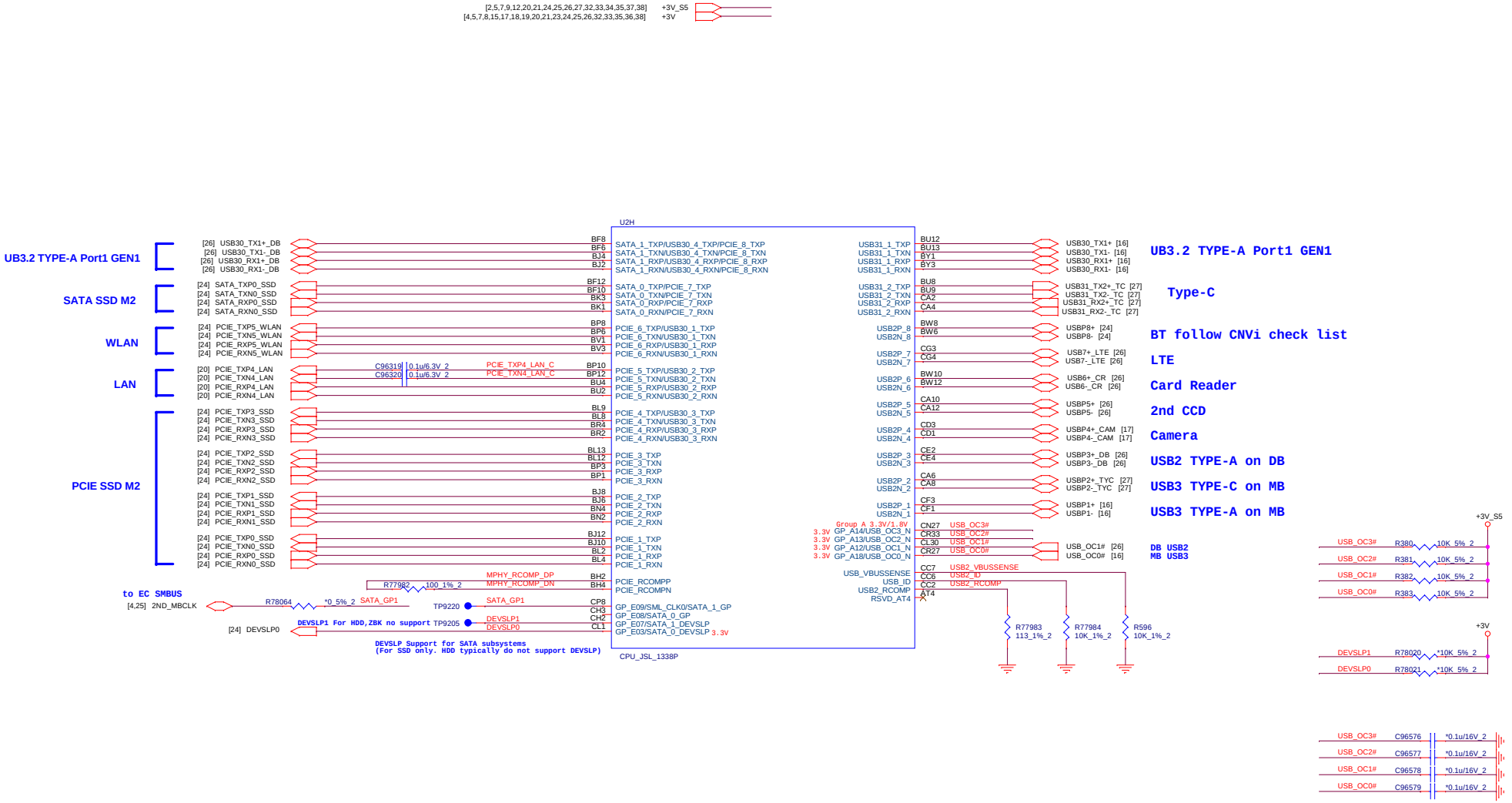
(CPU)

03



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PROJECT : ZBK_ZBKA		
Size	Document Number	Rev
	JSL+: USB, PCIE, CNVI	1A
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(CPU)

04

eDP Panel

TypeC DP

HDMI

U2A

CPU_JSL_1338P

required 330n or 100K to GND

USED FOR MIPI PANELS

eDP

TypeC

HDMI

DDI2_HPD IS ON SPI PAGE

Strap Pin reserve +3V_DEEP_SUS
Pull-up on page.8

U2F

CPU_JSL_1338P

Touch Screen

Touch Pad

SENSOR HUB

reserve for G sensor

to EC SMBUS

Strap Pin reserve +3V_DEEP_SUS
Pull-up on page.8

CPU Thermal Sensor (THM)

Base: PIN 1
Emitter: PIN 2
Collector: PIN 3

1019 Add Q36 (Thermal to EC)

0701_2 Correct the Location to Q5545B
0702 Delete Q5545 because SMBUS from EC is Master,so modify to SMLink

Address 9AH

Quanta Computer Inc.			
PROJECT : ZBK_ZBKA			
Size	Document Number		Rev
	JSL+: DISPLAY, CAMERA, I2C		1A
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(CPU)

[2,3,7,9,12,20,21,24,25,26,27,32,33,34,35,37,38] +3V_S5
[12,17,20,26,27,29,30,31,32] +3VPCU
[8,9,25] +3V_RTC
[3,4,7,8,15,17,18,19,20,21,23,24,25,26,32,33,35,36,38] +3V

U2J

CPU_JSL_1338P

0604 TODO: INTEL TO CONFIRM IF R312 AND D8519 ARE NEEDED?
0709 DNS R312/D8519/R77908 and modify R312 to 100 ohm

Touch screen had internal PU

U2G

CPU_JSL_1338P

U2I

CPU_JSL_1338P

PCIE SSD M2
LAN
WLAN

CAD NOTE:
GUARD THE CRYSTAL INOUT WITH GROUND TRACE AS PER PDG ADDITIONAL GUILDLINES

DESIGN NOTE:
XTAL ESR = 30 OHM MAX, CL = 10PF, C0 = 3PF, MAX DRIVE = 300UW

DESIGN NOTE:
REFER PDG ADDITIONAL GUIDELINES FOR CRYSTAL ROUTING

RAM ID

ID3	ID2	ID1	ID0	Vendor	Vendor PN	Quanta PN
0	0	0	0	KINGSTON 8Gb 2666	D5116AN9CXGRK	AKD5QGSTP00
0	0	0	1	Hynix 8Gb 3200	H5AN8G6NDJR-XNC	AKD5QGSTW30
0	0	1	0	SAMSUNG 8Gb 2666	K4A8G165WC-BCTD	AKD5QGST512
0	0	1	1			

BOARD ID

BOARD_ID5		R2349 H	R2350 L
BOARD_ID2	R2360 H	SANDISK (W128G) Default	SANDISK (W64G)
	R2361 L	C stage KINGSTON (K64G) KINGSTON (K128G)	RAMP KINGSTON (K64G) KINGSTON (K128G)

	High	Low
BOARD_ID0	eMMC(MMC@)	Non eMMC(MMC_N@)
BOARD_ID1	Clamshell(ZBK,CLM@)	Convertible + G sensor (ZBKA,CON_GS@)
BOARD_ID2	eMMC Board ID	
BOARD_ID3	Non I2C Touch screen (TSI_N@)	I2C touch screen (TSI@)
BOARD_ID4	2channel(MDB@)	1channel(OCH@)
BOARD_ID5	eMMC Board ID	
BOARD_ID6	Single MIC	2nd MIC (Control by DB)
BOARD_ID7	SATA SSD (S_SSD@)	PCIE_SSD (P_SSD@)
BOARD_ID8	Reserve(default) Control by DB	LTE
BOARD_ID9	Reserve(default) Control by DB	11 : no support LTE 10 : u-SIM 01 : e-SIM 00 : u-SIM+e-SIM

RTC Circuitry(RTC) (RTC)

RTC Power trace width 20mils.

update footprint to bat-aaa-bat-046-k03-2p-smt and change pin defined 4/17

EC reset RTC

From EC

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PROJECT : ZBK_ZBKA		
Size	Document Number: JSL+: AUDIO, SD, EMMC, CNVI, CLOCKS	Rev: 1A
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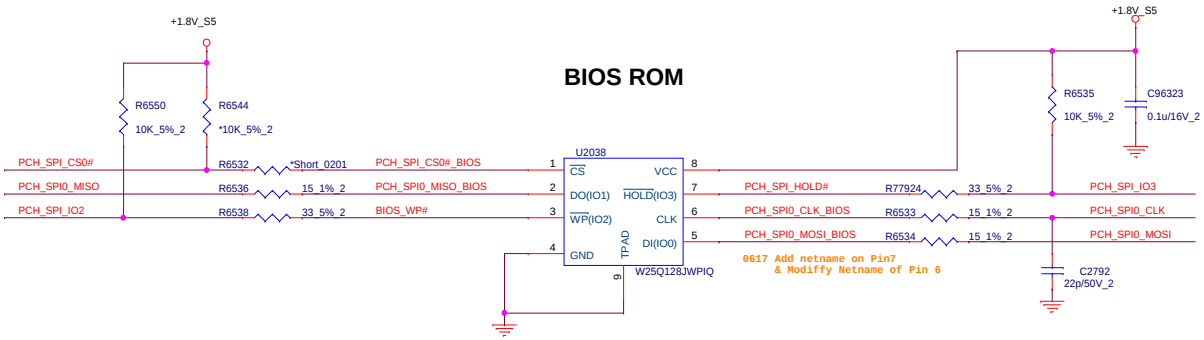
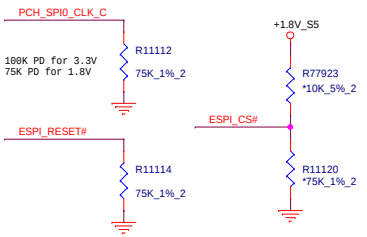
[9,12,22,23,25,26,37,38] +1.8V_S5

(CPU)

BIOS ROM



PCH GLITCH MITIGATION



PCH SPI ROM(CLG)

	Vender	Size	P/N	WSON-8 6x5-mm
JSL	Winbond	16M	AKE5DF-KN00	W25Q128JWPIQ
	GigaDevice	16M	AKE5DZNKQ04	GD25LB128DWIGR
	XMC	16M	AKE5DZ-KX00	XM25QU128BWIQ(need P/R)
	MAX	16M		

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PROJECT : ZBK_ZBKA
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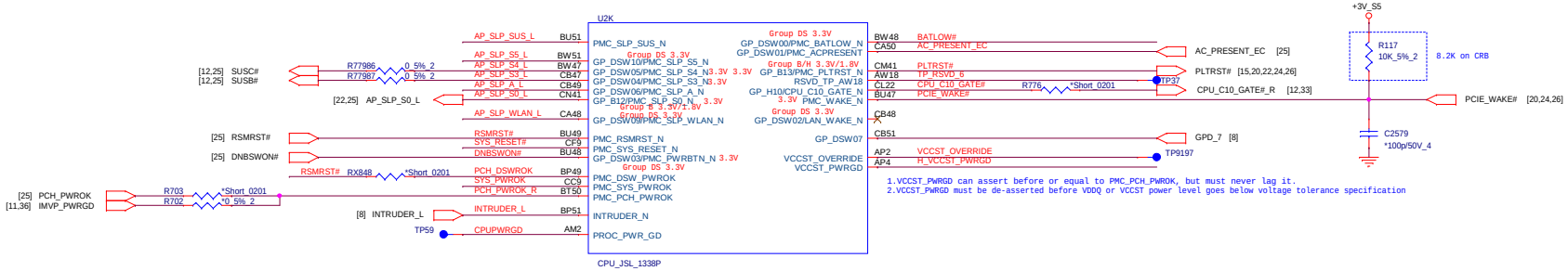
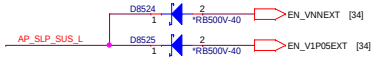
JSL+: ESPI, SPI
Date: Monday, January 04, 2021 | Sheet 6 of 39

[2,3,5,9,12,20,21,24,25,26,27,32,33,34,35,37,38] +3V_S5
[3,4,5,8,15,17,18,19,20,21,23,24,25,26,32,33,35,36,38] +3V
[9,11,12,31,36] +VCCST

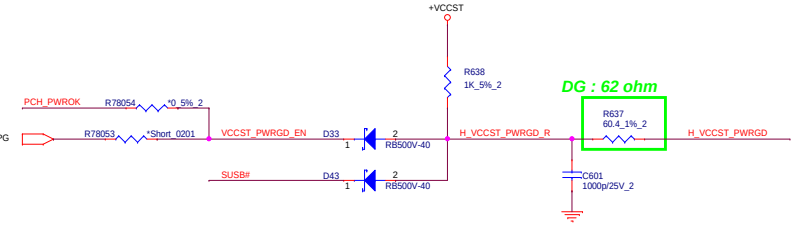
(CPU)

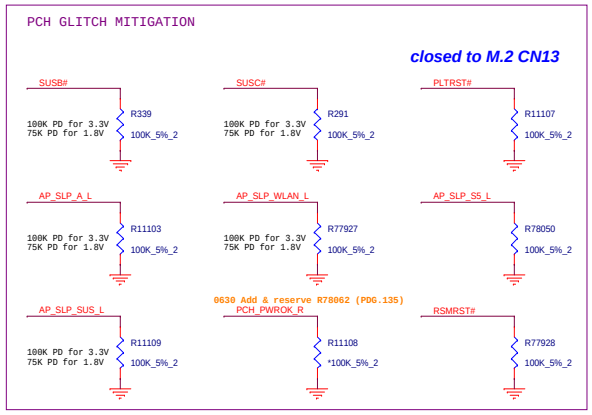
RSMRST_PWRGD_L DIODE IS NEEDED TO MEET TPLT19 TIMING PARAMETER:
10US MAX FROM RSMRST_PWRGD_L ASSERTION TO AP_RSMRST_L ASSERTION

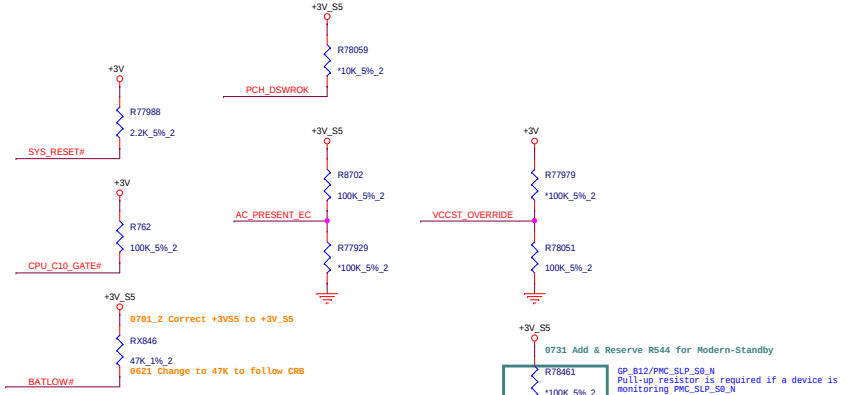


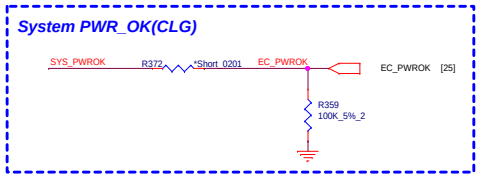


RX288 close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"









Quanta Computer Inc.		
PROJECT : ZBK_ZBKA		
Size	Document Number	Rev
	JSL+: POWER SEQUENCING	1A
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[3,4,5,7,15,17,18,19,20,21,23,24,25,26,32,33,35,36,38] +3V
[9] +3V_DEEP_SUS
[9,24] +1.8V_DEEP_SUS
[5,9,25] +3V_RTC
[9,12] +VCC1.05_OUT_FET

(CPU)

BSSB LSX #0 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

INTERNAL PD

[4] GP_E14_DDI0_DDC_SDA

+3V_DEEP_SUS

R6D46 *4.7K_5%_2

R78027 *20K_1%_2

0709 DNS R78027

BSSB LSX #1 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

INTERNAL PD

[4,25] SIO_EXT_SCI#

+3V_DEEP_SUS

R6D42 *4.7K_5%_2

R78028 *20K_1%_2

0709 DNS R78028

BSSB LSX #2 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

INTERNAL PD

[4,19] INT_HDMI_SDA

+3V_DEEP_SUS

R6D40 *4.7K_5%_2

R78029 *20K_1%_2

0709 DNS R78029

BSSB LSX #3 PINS VCCIO CONFIGURATION

HIGH: 3.3V

LOW: 1.8V

INTERNAL PD

[4] GPPC_E_12_IMGCLKOUT_4

+3V_DEEP_SUS

R6D39 *4.7K_5%_2

R78030 *20K_1%_2

RESERVED

[4] GPPC_D_9_GSPI2_CLK_UART0A_TXD

+3V_DEEP_SUS

R1G3 100K_5%_2

R1G1 *4.7K_5%_2

RESERVED

[4] GPPC_D_8_GSPI2_CSOB_UART0A_RXD

+3V_DEEP_SUS

R6D34 100K_5%_2

R6D29 *4.7K_5%_2

RESERVED

THIS STRAP HAS A 20K INTERNAL PULL-DOWN

DO NOT PULL THIS PIN HIGH ON BOARD

[4] GPPC_D_10_GSPI2_MISO_UART0A_RTSB

+3V_DEEP_SUS

R6D41 *4.7K_5%_2

R6D38 *20K_1%_2

ESPI OR EC LESS

HIGH: ESPI IS DISABLED
LOW: ESPI SELECTED

WEAK INTERNAL PD 20K

[4] GPPC_C_9_UART0_TXD

+3V_DEEP_SUS

R7D40 *4.7K_5%_2

R6D86 *20K_1%_2

RESERVED

GPPC_E10

0702 Delete R77904 (PU 20K to +3V_DEEP_SUS because duplication PU on EC side)

+1.8V_DEEP_SUS

R77903 *20K_1%_2

GPPC_E_10

[4] GPPC_E_10

R4F25 *4.7K_5%_2

FLASH DESCRIPTOR SECURITY OVERRIDE

HIGH: OVERRIDEN
LOW: SECURITY MEASURES NOT OVERRIDEN

WEAK INTERNAL PD 20K
SAMPLING- PCH_PWROK

0622_2 Add ME_WR#

[25] ME_WR#

R78054 1K_5%_2

+3V_DEEP_SUS

R3C14 *4.7K_5%_2

[4] GPPC_A_15

Reserve

GPPC_E6

+3V_DEEP_SUS +1.8V_DEEP_SUS

R77895 20K_1%_2

R77896 *20K_1%_2

[4] GPPC_E_6_IMGCLKOUT_3

R3C35 *4.7K_5%_2

XTAL SEL1

LOW: 38.4/19.2MHZ (DEFAULT)
HIGH = 24MHZ

(25 MHZ WHEN XTAL FREQ DIVIDER NON ZERO)

WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

+3V_DEEP_SUS +1.8V_DEEP_SUS

R6D67 *4.7K_5%_2

R6D66 *4.7K_5%_2

[4] GPPC_E_0_IMGCLKOUT_0

R78031 *20K_1%_2

Reserve

GPPC_E11

+1.8V_DEEP_SUS +3V_DEEP_SUS

R77900 *20K_1%_2

R77899 20K_1%_2

GPPC_E_11

[4] GPPC_E_11

R4F24 *4.7K_5%_2

MAF/SAF STRAP

LOW-> MAF ENABLE
HIGH-> SAF ENABLE

WEAK INTERNAL PD 20K

+3V_DEEP_SUS

R1H18 *2.2K_5%_2

[4] GPPC_D_11_GSPI2_MOSI_UART0A_CTSB

R78033 *20K_1%_2

CPUNSSC CLOCK FREQ

HIGH: 19.2MHZ CLOCK FROM DIVIDER
(DERIVED FROM 38.4MHZ CRYSTAL)

LOW: 38.4MHZ CLOCK FROM DIRECT
CRYSTAL (DEFAULT)

WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

+3V_DEEP_SUS

R4E63 *4.7K_5%_2

[4] GP_C13_UART1_TXD

R78034 *20K_1%_2

TLS CONFIDENTIALITY

LOW - TLS CONFIDENTIALITY DISABLE
HIGH - TLS CONFIDENTIALITY ENABLE

WEAK INTERNAL PD 20K
SAMPLING - RSMRSTB

+3V_DEEP_SUS

R7D25 *4.7K_5%_2

[4,23] ACCEL_INT1

R78036 *20K_1%_2

BOOT HALT

HIGH - DISABLED
LOW- ENABLED

NO INTERNAL PU/PD
SAMPLING - RSMRSTB

+3V_DEEP_SUS

R77902 100K_5%_2

[4] GP_C10_UART0_RTS_N

R3C24 *4.7K_5%_2

NO REBOOT

HIGH - NO REBOOT
LOW- REBOOT ENABLED

WEAK INTERNAL PD 20K
SAMPLING- PCH_PWROK

+3V

R8A7 *4.7K_5%_2

[5] GPPC_C_2

R78041 *20K_1%_2

TOP SWAP OVERRIDE

HIGH- TOP SWAP ENABLED
LOW-DISABLED

WEAK INTERNAL PD 20K
SAMPLING- PCH_PWROK

0604 CRB reserve 20K pull down

+3V

R7D35 *4.7K_5%_2

[5] GPPC_C_1

R78042 *20K_1%_2

Reserve

GPPC_E23

+1.8V_DEEP_SUS

R4F27 *4.7K_5%_2

[5,24] CNV_RGI_RSP

R77921 *20K_1%_2

M.2 CNVI MODES

LOW-> INTEGRATED CNVI ENABLE
HIGH-> INTEGRATED CNVI DISABLE

NO INTERNAL PU/PD
SAMPLING - RSMRSTB

+3V_DEEP_SUS

R6D5 *20K_1%_2

[5,24] CNV_RGI_DT

R6D24 *4.7K_5%_2

Reserve

GPPC_E21

+1.8V_DEEP_SUS

R4F26 *4.7K_5%_2

[5,24] CNV_BRI_RSP

CNV_BRI_RSP

R77920 *20K_1%_2

RESERVED

THIS STRAP HAS A 20K INTERNAL PULL-UP

+VCC1.05_OUT_FET

R78055 1K_5%_2

[11] DBG_PMODE

0622_2 Add R78055 for safe

R5G69 *1K_5%_2

CFG4 DISPLAY PORT PRESENCE STRAP

0: ENABLED

AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT

1: DISABLED; (DEFAULT)

NO PHYSICAL DISPLAY PORT ATTACHED TO THE EMBEDDED DISPLAY PORT

[11] MIPI60_CFG4_N

R5M19 1K_5%_2

CFG_00

EAR

1 = (Default) Normal Operation

0 = Reserved.

[11] MIPI60_CFG0_N

R4D6 *1K_5%_2

SPI Voltage Configurati on

0 = SPI operation voltage is 3.3 V

1 = SPI operation voltage is 1.8 V

NO INTERNAL PU/PD

SAMPLING - SRTCRST_N

+3V_RTC

R3C18 1M_1%_2

[7] INTRUDER_L

R2C20 *10K_5%_2

RESERVED

THIS STRAP HAS A 20K INTERNAL PULL-DOWN

+3V_RTC

R7D26 *4.7K_5%_2

[7] GPD_7

R7D24 *20K_1%_2

Quanta Computer Inc.

PROJECT : ZBK_ZBKA

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	JSL+: STRAPS	1A

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Jasper Lake (POWER)

EDGE DECAPS
FOR EXPOSED POWER PLANES

(CPU)

[26] +VCCIN
[37] +VCCIN_AUX
[9] +3V_DEEP_SUS
[8,24] +1.8V_DEEP_SUS
[8,12] +VCC1.05_OUT_FET
[34] +VNN_EXT
[34] +1.05V_EXT
[5,8,25] +3V_RTC
[2,3,5,7,12,20,21,24,25,26,27,32,33,34,35,37,38] +3V_S5
[12] +VCC1P8A
[2,12,13,14,35] +1.2VSUS
[8,12,22,23,25,26,37,38] +1.8V_S5
[11,33] +VCCIO
[7,11,12,31,36] +VCCST
[12] +VCCPLL_OC
[11] +VCCSTG_TERM

Icc(max):35A

Primary side
Backside
Backside Underneath
EMC CAPS
PLACE <5mm FROM SOC VCCIN
Place with at least 5 qty at < 7mm distance from the package-egde VCCIN BGAs.
The remaining caps can be placed at distance < 10mm.
Place underneath the VCCIN BGAs and equally distribute
0609 Add by PDG suggestion
U2L
CPU_JSL_1338P

Icc(max):24A

EMC CAPS PLACE <5mm FROM SOC VCCIN
VCC_PGPPE is input supply for the GP_E GPIOs.
Shute to Cost optimized
Supplied directly by V1.8A for cost optimized
U2N
CPU_JSL_1338P

Icc(max):3.5A

EMC CAPS - PLACE <4MM FROM SOC VDDQ, WITH EACH PAIR <12MM APART
U2M
CPU_JSL_1338P
Can't down size

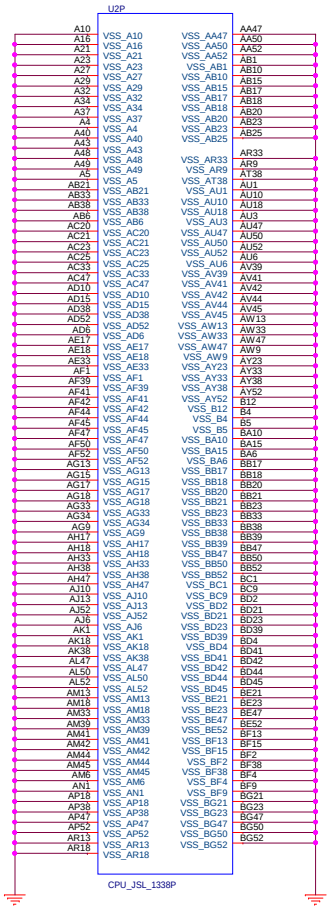
Rail	Voltage	Icc(max)	
VCCIN	0 V(MIN)~2 V(MAX)	35 A	VDC
VCCIN_Aux	1.65 or 1.8 V -Actice 1.1 V - Retention Off - Idle States	24 A	VDC
VDDQ	1.2 V (DDR4)	3.5 A	VDC
VCCPRIM_3P3	3.3 V	0.232 A	
VCCIPRIM_1P8	1.8 V	0.089 A	
VCC_VNNEXT_1P05 (Optional)	1.05 V or 0.76 V	0.5 A	
VCC_V1P05EXT_1P05 (Optional)	1.05 V	0.5 A	
VCCIO_EXT	1 V (Type)	5 A	VDC
VCCPLL	1.05 V	0.1 A	
VCCST	1.05 V	0.6 A	
VCC_OUT_FET_1P05	1.05 V	0.7 A	PCH FIVR
VCCSTG	1.05 V	0.15 A	PCH FIVR
VCCSTG_OUT	1.05 V	0.15 A	PCH FIVR
VCCLDOSTD_0P85	0.85 V		
VCCPRIM_1P05	1.05 V		PCH FIVR
VCCA_CLKLDO_1P8	1.8 V	0.12 A	
VCCDPHY_1P24	1.24 V		
VCCPGPPR	1.8 V / 3.3 V	0.000237 A	
VCC1P8A	1.8 V	0.7 A	VDC
VCCRTC	3 V	0.001 A	
VCCPLL_OC	1.1 V / 1.2 V	0.1 A	
VCCSPI	1.8 V / 3.3 V	0.003 A	
VCCDSW_3P3	3.3 V	0.001 A	VDC

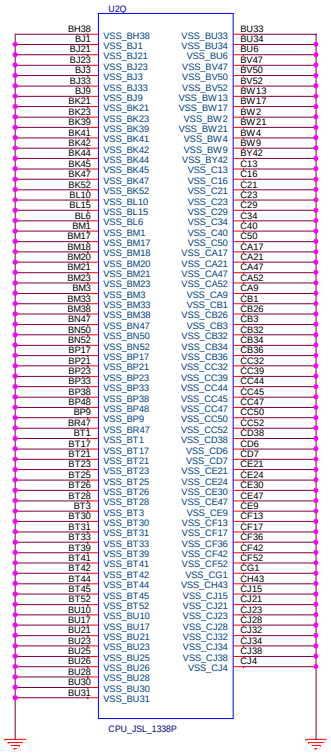
0709 Add R78072/R78071
R78072 can rework to Inductor if needed

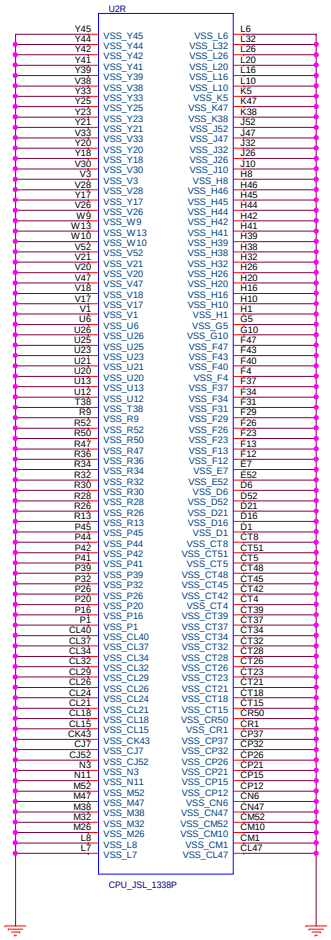
For DSX/NDSX option
Non-DSX(+3V5S)
For DSX(+3VPCU)

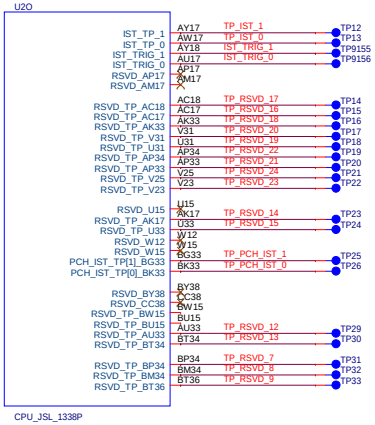
(CPU)

10









Quanta Computer Inc.

PROJECT : ZBK_ZBKA

Size	Document Number	Rev
	JSL+: GROUND, RESERVED	1A
Date: Monday, January 04, 2021	Sheet 10 of 39	

(CPU)

[9] +VCCSTG_TERM
[9,33] +VCCIO
[7,9,12,31,36] +VCCST

U2D

CPU_POPIRCOMP — R7D9 49.9_1%_2

[8] DBG_PMODE — DBG_PMODE — PROC_POPIRCOMP — DBG_PMODE

CPU_TCK — CPU_JTAG_TCK
CPU_TDO — CPU_JTAG_TDO
CPU_TDI — CPU_JTAG_TDI
CPU_TRST# — CPU_JTAG_TRST_N
CPU_TMS — CPU_JTAG_TMS

CPU_VIDALERT# — SVID_ALERT_N
TP65 BMP3# — BPM3_N
TP64 BMP2# — BPM2_N
BMP1# — BPM1_N
BMP0# — BPM0_N

PCH_JTAG_TMS — PCH_TMS — RX782 *Short_0201 — CPU_TMS
PCH_JTAG_TDO — PCH_TDO — RX783 *Short_0201 — CPU_TDO
PCH_JTAG_TDI — PCH_TDI — RX784 *Short_0201 — CPU_TDI
PCH_JTAG_TCK — PCH_TCLK — RX785 *Short_0201 — CPU_TCK
PCH_JTAG_X — PCH_JTAGX — RX786 *Short_0201 — CPU_TRST#
PCH_JTAG_TRST_N
JTAG_PREQ_N — XDP_PREQ#
JTAG_PRDY_N — XDP_PRDY#
PROCHOT_N — AP_PROCHOT_ODL
CATERR_N — H_CATERR_N
THRMTRIP_N — PM_THRMTRIP#
SVID_DATA — CPU_SVID_DAT
SVID_CLK — CPU_SVID_CLK
PCH_OPIRCOMP — PCH_OPIRCOMP — R6E5 49.9_1%_2

CPU_JSL_1338P

CPU_TMS — TP9162
CPU_TDO — TP9163
CPU_TDI — TP9164
PCH_TCLK — TP9165
CPU_TCK — TP9166
CPU_TRST# — TP9167

U2S

[8] MIPI60_CFG4_N
[8] MIPI60_CFG0_N
RX701 51_1% 2
RX702 51_1% 2
TP9158 MIPI60_CFG_STB1_DP — CFG_AVRB_STB_1P
MIPI60_CFG_STB1_DN — CFG_AVRB_STB_1N
TP9159 MIPI60_CFG_STB0_DP — CFG_AVRB_STB_0P
MIPI60_CFG_STB0_DN — CFG_AVRB_STB_0N

MIPI60_CFG15_N N6 CFG_15
MIPI60_CFG14_N R8 CFG_14
MIPI60_CFG13_N U8 CFG_13
MIPI60_CFG12_N R12 CFG_12
MIPI60_CFG11_N R10 CFG_11
MIPI60_CFG10_N R6 CFG_10
MIPI60_CFG9_N N8 CFG_09
MIPI60_CFG8_N N9 CFG_08
MIPI60_CFG7_N W4 CFG_07
MIPI60_CFG6_N U2 CFG_06
MIPI60_CFG5_N U4 CFG_05
MIPI60_CFG4_N T1 CFG_04
MIPI60_CFG3_N R4 CFG_03
MIPI60_CFG2_N T3 CFG_02
MIPI60_CFG1_N P3 CFG_01
MIPI60_CFG0_N R2 CFG_00

AY21 RSVD_AY21
AY20 RSVD_AY20
CA15 RSVD_CA15
CA13 RSVD_CA13
BC10 RSVD_TP_BC10
BC12 RSVD_TP_BC12
TP9180 TP_2 — BC15 TP_BC15
TP9181 TP_1 — BC13 TP_BC13
AU12 RSVD_AU12
AU13 RSVD_AU13
CT2 RSVD_CT2
CP3 RSVD_CP3
TP9182 TP_4 — CR52 TP_CR52
TP9183 TP_3 — CT49 TP_CT49
CN52 RSVD_CN52
TP9184 RSVD_TP_30 — BD33 RSVD_TP_BD33
TP9185 RSVD_TP_31 — BE33 RSVD_TP_BE33
B3 RSVD_B3
D3 RSVD_D3
BB34 RSVD_BB34
BD34 RSVD_BD34
U30 RSVD_U30
U28 RSVD_U28
BJ15 RSVD_TP_BJ15
BJ13 RSVD_TP_BJ13
TP9186 RSVD_TP_33 — CE40 RSVD_TP_CE40
BP13 RSVD_TP_BP13
BP15 RSVD_TP_BP15
TP9189 RSVD_TP_26 — BT38 RSVD_TP_BT38
AR1 RSVD_TP_AR1
CC4 RSVD_TP_CC4
CFG_RCOMP — N1 CFG_RCOMP
TP9192 RSVD_TP_32 — AR17 RSVD_TP_AR17
[25] EC_PECI — EC_PECI — AM4 PECI
R6F3 49.9_1%_2

CPU_JSL_1338P

0701_2 Correct Pin.AM4 Netname to EC_PECI

XDP

VCCSTG=1.05V

+VCCSTG_TERM

XDP_PREQ# RX748 *51_1%_2
XDP_PRDY# RX749 *51_1%_2
CPU_TMS RX750 *51_1%_2
CPU_TDI RX751 *51_1%_2
CPU_TDO RX752 100_1%_2
PCH_TDO RX753 100_1%_2
PCH_TDI RX754 51_1%_2
PCH_TMS RX755 51_1%_2
PCH_TRST# RX756 *51_1%_2
CPU_TCK RX757 51_1%_2
PCH_JTAGX RX758 *51_1%_2
PCH_TCLK RX759 *51_1%_2

+VCCIO

BMP1# RX777 10K_5%_2
BMP0# RX778 10K_5%_2

+VCCST

H_CATERR_N R8602 49.9_1%_2

0620 Delete PU to VCCST of PM_THRMTRIP#

+VCCST

CLOSE TO SOC

RX763 56_1%_2
RX761 *43_5%_2
RX762 100_1%_2

ROUTE CPU_VIDALERT# BETWEEN CLK AND DATA

CPU_VIDALERT# — RX764 *Short_0201 — TO POWER PAGE VR_SVID_ALERT# [36]
CPU_SVID_CLK — RX765 *Short_0201 — VR_SVID_CLK [36]
CPU_SVID_DAT — RX766 *Short_0201 — VR_SVID_DATA [36]

VIDSDAT Rpu1=100Ω, Rpu2=100Ω
VIDSCK Rpu1=N/A, Rpu2=45Ω
VIDSALERT# Rpu1=56Ω, Rpu2=N/A

THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches

+VCCST

[7,36] IMVP_PWRGD — Q12 DMG301NU-7
R187 *100K_5%_2
R188 1K_5%_2
R196 1K_5%_2
[4,25,32,38] SYS_SHDN# — Q11 METR3904-G — PM_THRMTRIP#

CAD NOTE:
PLACE 'RA' CLOSE TO MCP - WITHIN 40MM

CAD NOTE:
PLACE 'RB' AT THE END OF DIASY CHAIN

+VCCSTG_TERM
RA RA RB
R8603 1K_5%_2
R8609 *10K_5%_2
AP_PROCHOT_ODL — R8606 499_1%_2 — H_PROCHOT# [5,25,31,36]
C2596 *0.1u/16V_2

From EC/Power

RX705 *1K_5%_2 MIPI60_CFG15_N
RX706 *1K_5%_2 MIPI60_CFG14_N
RX707 *1K_5%_2 MIPI60_CFG13_N — RX723 1K_5%_2
RX708 *1K_5%_2 MIPI60_CFG12_N — RX724 1K_5%_2
RX709 *1K_5%_2 MIPI60_CFG11_N — RX725 *10K_5%_2
RX710 *1K_5%_2 MIPI60_CFG10_N — RX726 1K_5%_2
RX711 *1K_5%_2 MIPI60_CFG9_N — RX727 1K_5%_2
RX712 *1K_5%_2 MIPI60_CFG8_N — RX728 1K_5%_2
RX713 *1K_5%_2 MIPI60_CFG7_N — RX729 *1K_5%_2
RX714 *1K_5%_2 MIPI60_CFG6_N — RX730 *1K_5%_2
RX715 *1K_5%_2 MIPI60_CFG5_N — RX731 *1K_5%_2
MIPI60_CFG4_N — RX732 *1K_5%_2
RX717 *1K_5%_2 MIPI60_CFG3_N — RX733 *1K_5%_2
RX718 *1K_5%_2 MIPI60_CFG2_N — RX734 *1K_5%_2
RX719 *1K_5%_2 MIPI60_CFG1_N — RX735 1K_5%_2
MIPI60_CFG0_N — RX736 1K_5%_2

+VCCIO
RX737 *Short_0402
+VCCIO

Quanta Computer Inc.
PROJECT : ZBK_ZBKA

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	JSL+: DEBUG, MIPI60	1A
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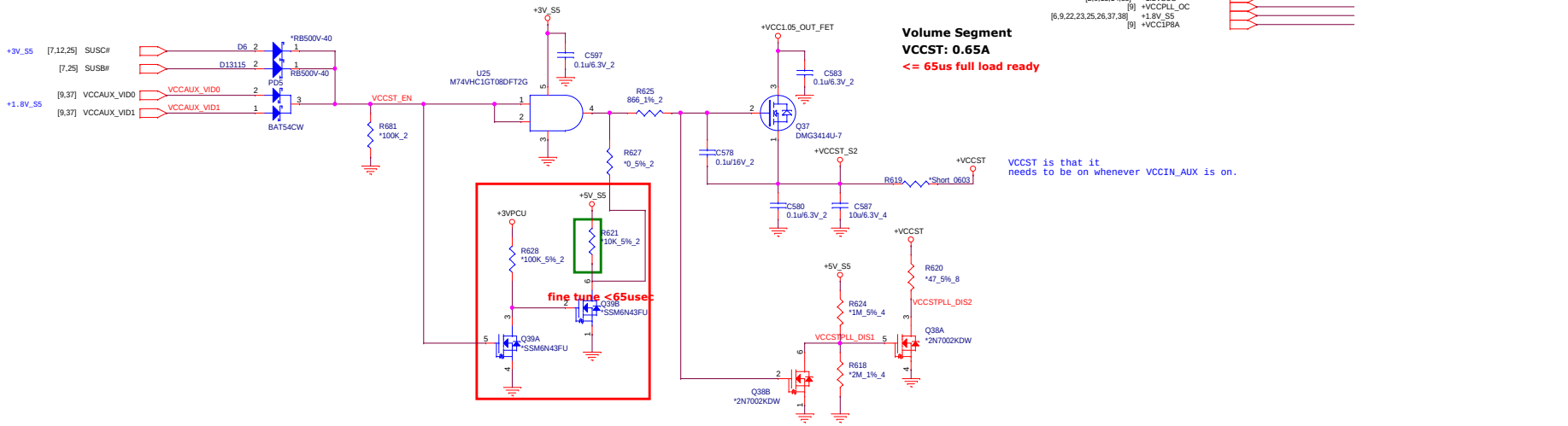
Volume Segment
ICL U42

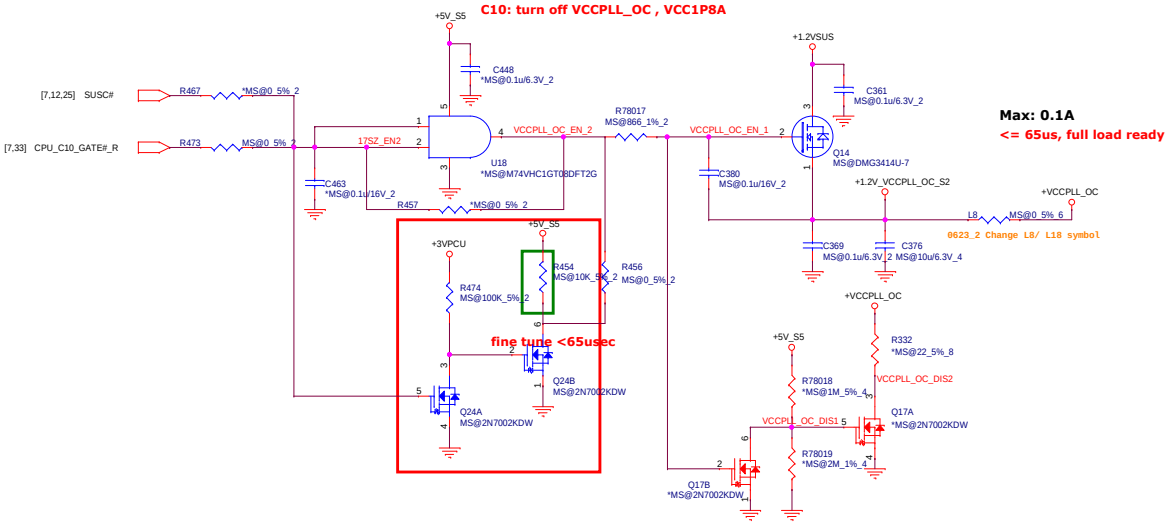
[2,3,5,7,9,20,21,24,25,26,27,32,33,34,35,37,38] +3V_S5
[5,17,20,26,27,29,30,31,32] +3VPCU
[16,26,32,35,36,37] +5V_S5
[7,9,11,31,36] +VCCST
[8,9] +VCC1.05_OUT_FET
[2,9,13,14,35] +1.2VSUS
[9] +VCCPLL_OC
[6,9,22,23,25,26,37,38] +1.8V_S5
[9] +VCCIP8A



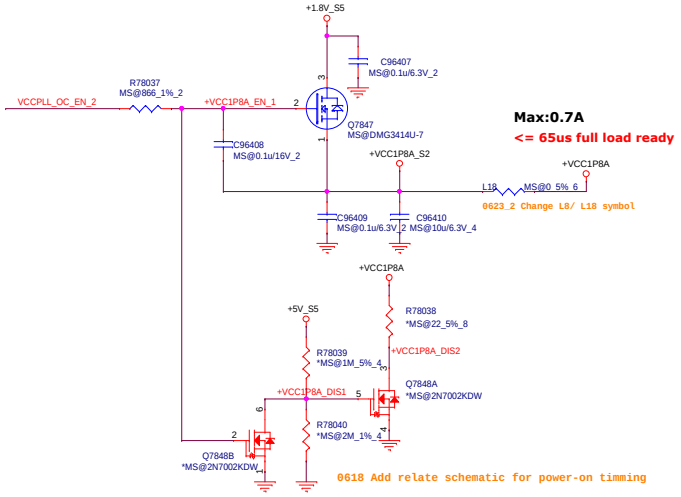
Volume Segment
VCCST: 0.65A
<= 65us full load ready

VCCST is that it
needs to be on whenever VCCIN_AUX is on.

C10: turn off VCCPLL_OC , VCC1P8A

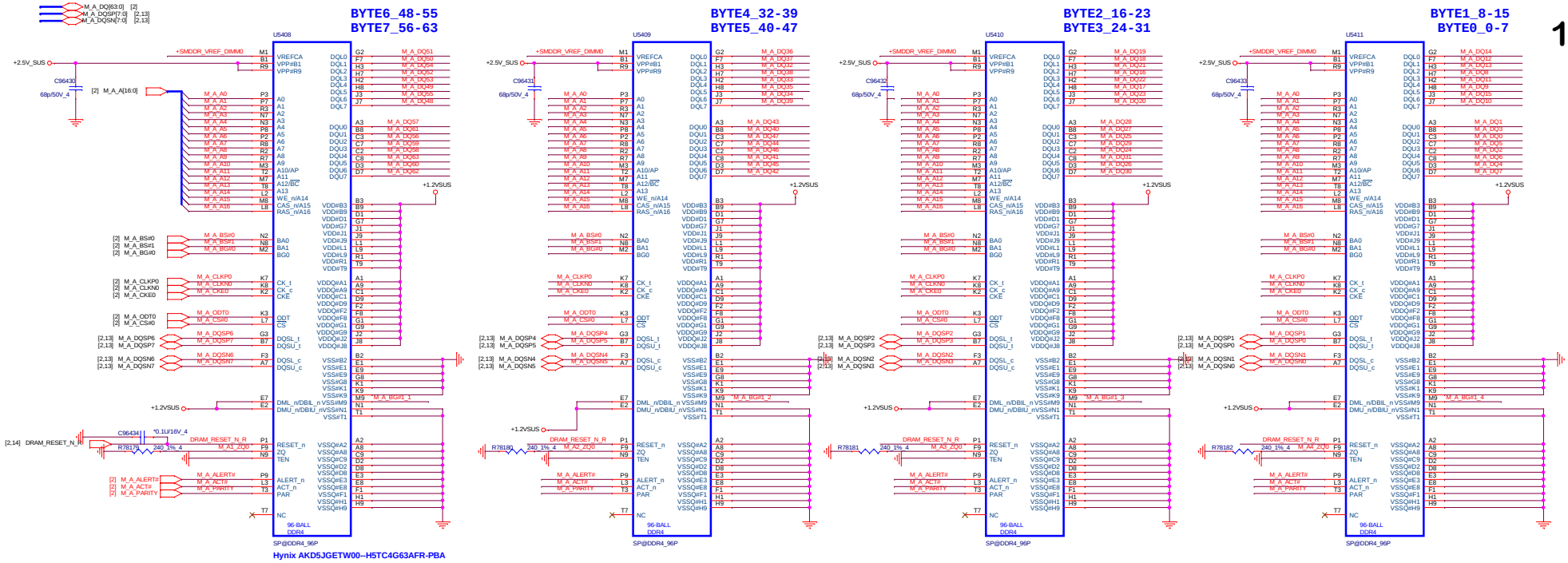


Max: 0.1A
<= 65us, full load ready

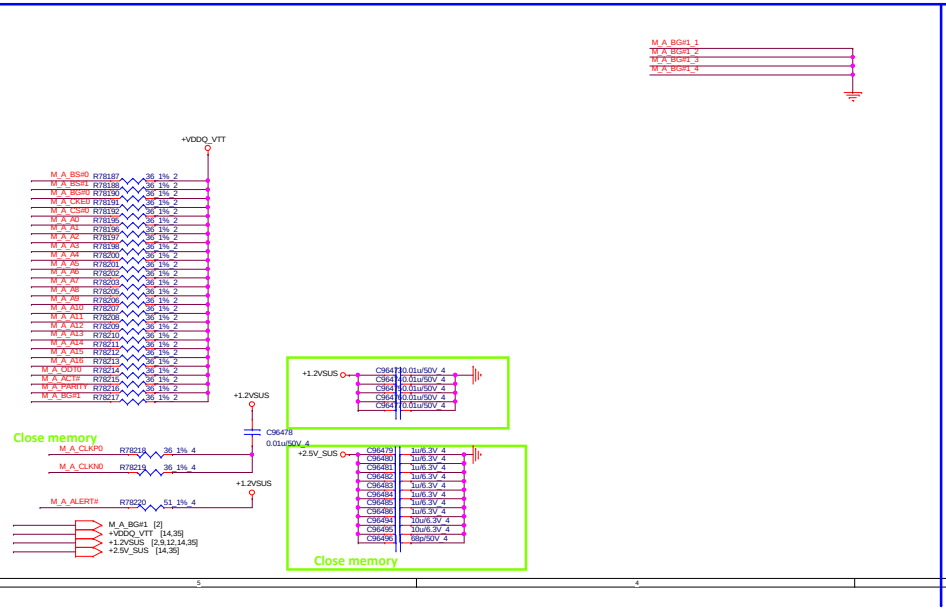


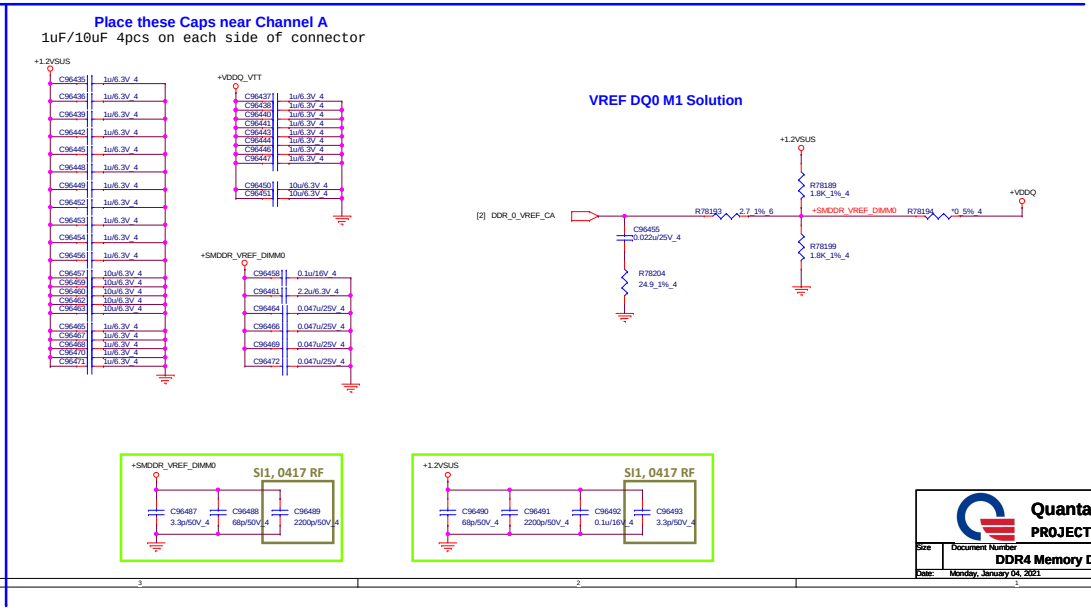
Max:0.7A
<= 65us full load ready

BU5	**PROJECT : G7AL** Quanta Computer Inc.	
Size C	Document Number +1.0V/+VCCSTPLL	Rev 1A
Date: Monday, January 04, 2021	Sheet 12 of 39	

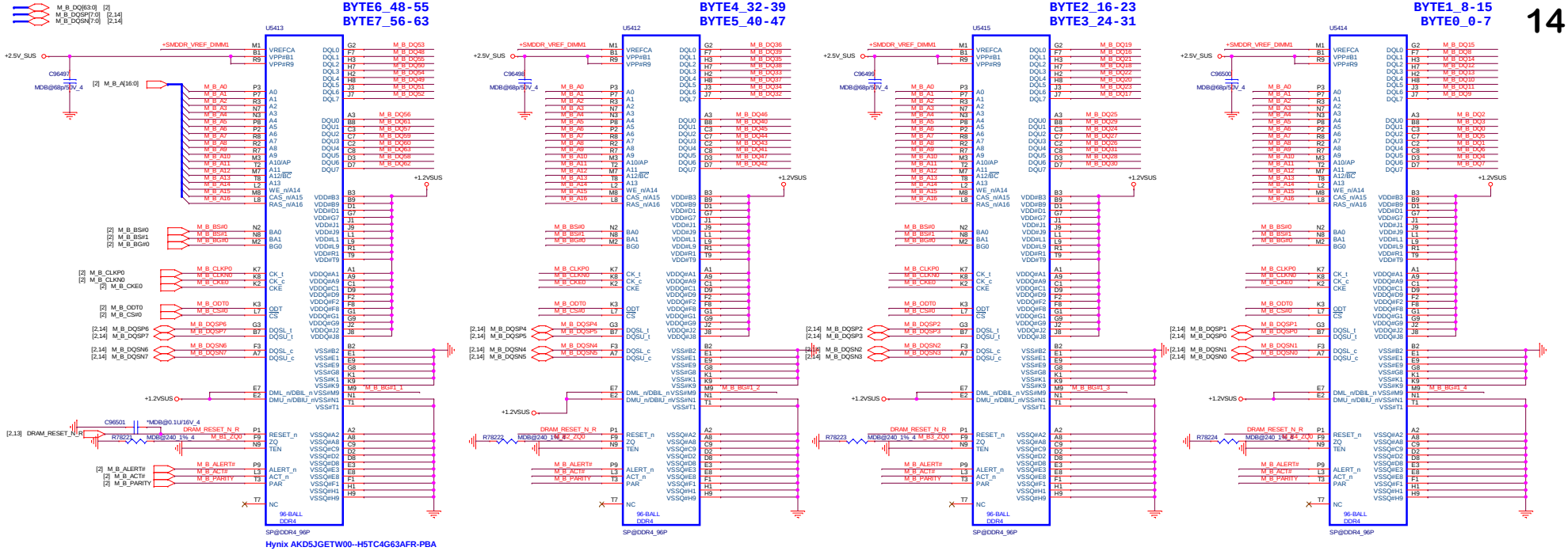


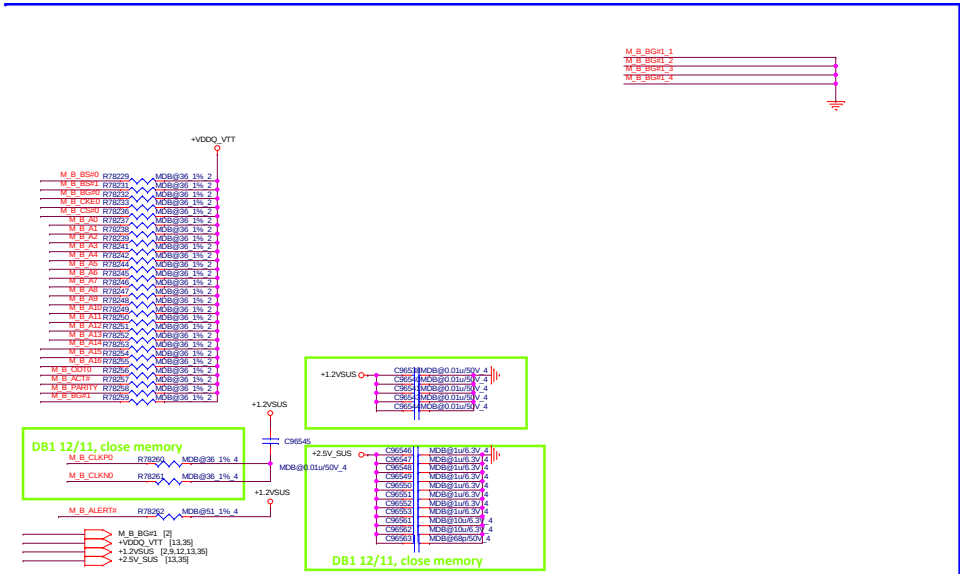
13

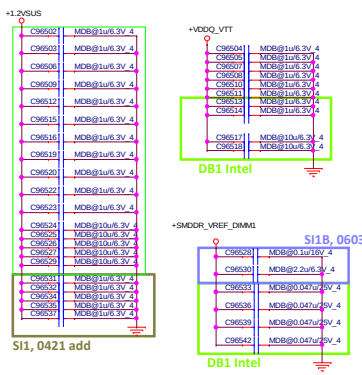


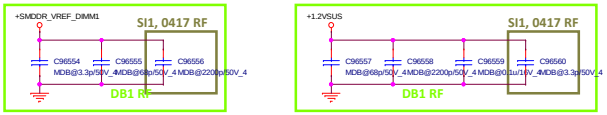


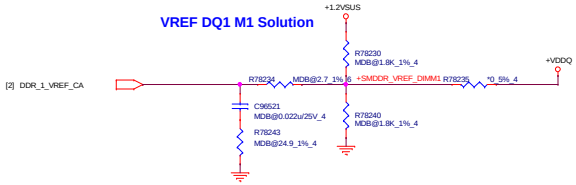
Quanta Computer Inc.			
PROJECT : ZBK_ZBKA			
Size	Document Number		Rev
	DDR4 Memory Down (CH. A)		1A
Date: Monday, January 04, 2021	Sheet 13 of 39		











Quanta Computer Inc.
PROJECT : ZBK_ZBKA

Size	Document Number	Rev
	DDR4 Memory Down (CH. B)	1A
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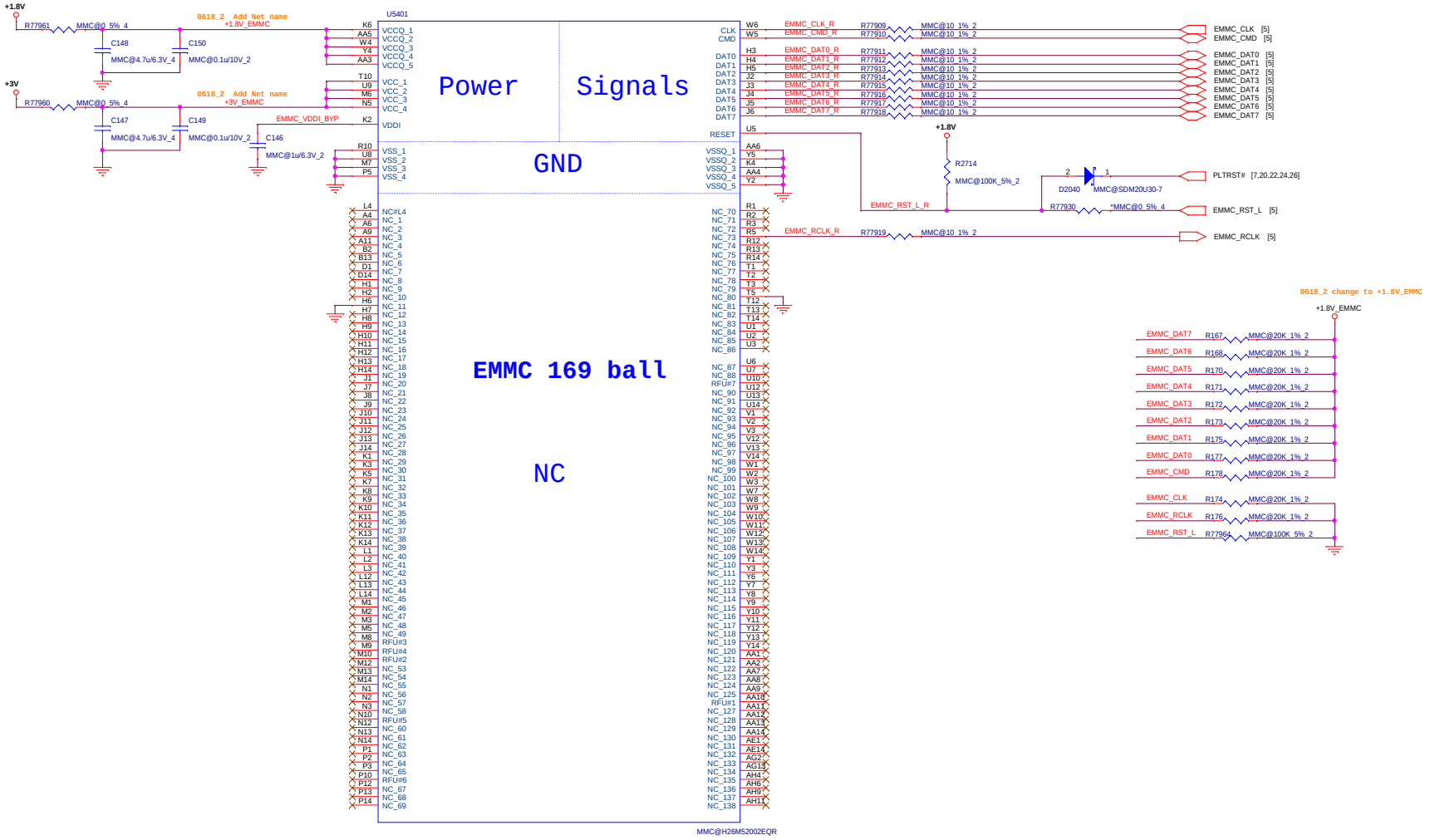
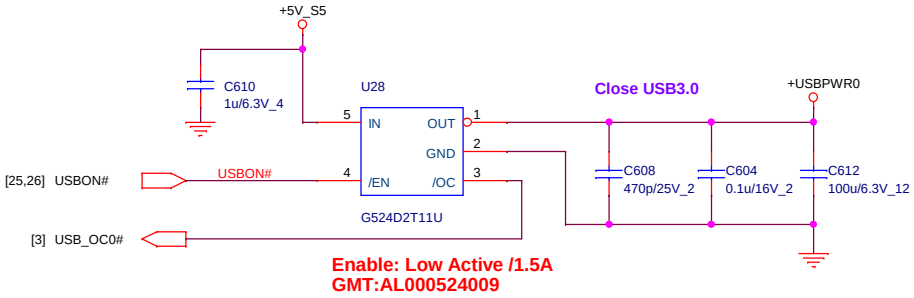
[18,25,38] +1.8V
[3,4,5,7,8,17,18,19,20,21,23,24,25,26,32,33,35,36,38] +3V

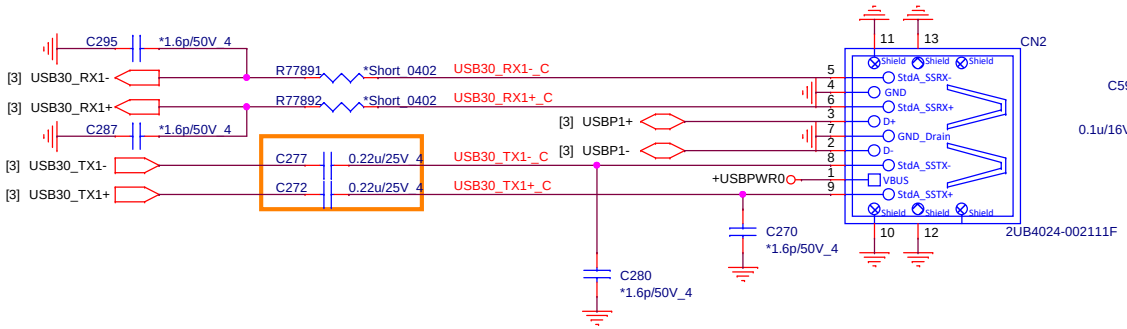


Quanta Computer Inc.		
PROJECT : ZBK_ZBKA		
Size	Document Number: eMMC(169 ball)	Rev: 1A
Date: Tuesday, January 26, 2021	Sheet 15 of 39	

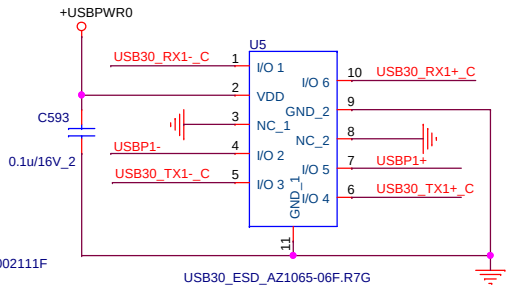
USB 3.0 Connector (UB3)

[12,26,32,35,36,37] +5V_S5





(EMC)



USB protection diodes for ESD.
as close as possible to USB connector pins.

CAP close to different CONN

Quanta Computer Inc.		
PROJECT : ZBK_ZBKA		
Size	Document Number	Rev
	USB3/Charger	1A
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eDP Conn.

eDP 2lane+ CCD(w/DMIC) + I2C touchscreen +LED/B

(LDS)

2A / 80mils

2A/80mils

0710 Adjust R18 pull down to GND and Move R18/R22 to PCH side

0620 Delete R26

CCD DMIC POWER
Touch Screen Power

touch screen[5] BOARD_ID3
Low = 1. CMI finger touch , High = 3. HH stylus touch

CCD-USB

Touch Screen-I2C

2.5A / 100mils

Enable:High Active /2.5A
GMT: AL000524004
SGY : AL006288003
BCD : AL022811000
EMS : AL005203000

Touch screen level shift I2C

(TSN)

0611 ADD

Different with Z8Y

Dual

LCD back light

PCH

EC

LID591#,EC intrnal PU

Touch Screen Power for Modern Standby

(TSN)

LED(UIF)

Adjust for ME

Blue

Amber

FULL LED

CHG LED

12-12/S2BHC-A30/2C

Quanta Computer Inc.
PROJECT : ZBK_ZBKA

Size	Document Number	Rev
	eDP/LID/CCD/TS/DMIC/LED	1A

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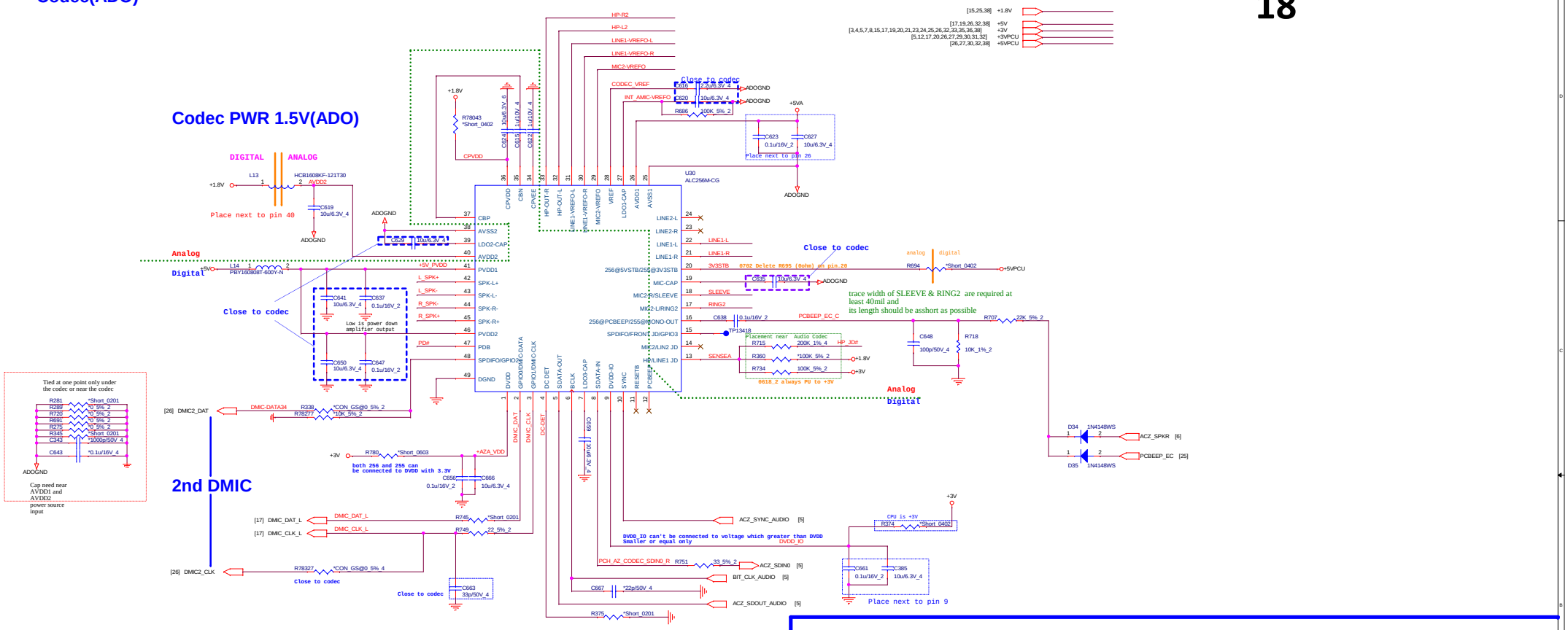
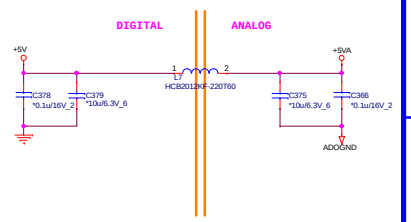
Codec(ADO)

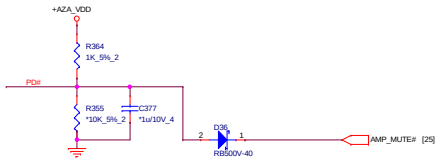


HEADPHONE/MIC/LINE combo (ADO)

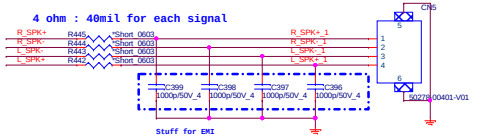
Codec PWR 5V(ADO)



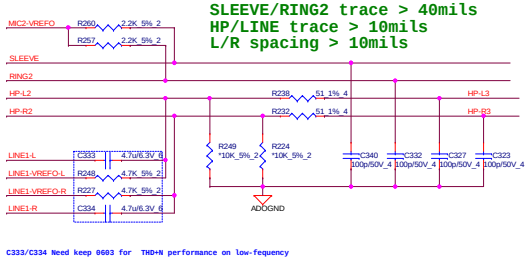
Mute(ADO)

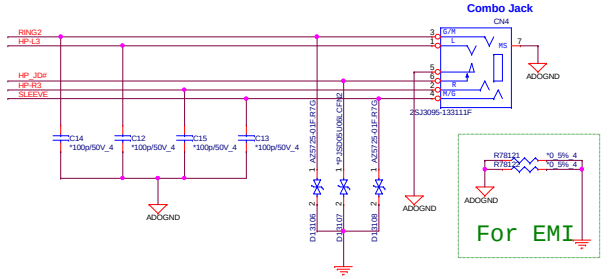


Internal Speaker



Universal Audio Jack





Quanta Computer Inc.
PROJECT : ZBK_ZBKA
Size | Document Number: Audio Codec/HP/SPK/Hole | Rev: 1A
Date: Monday, January 04, 2021 | Sheet 18 of 39

HDMI

[3,4,5,7,8,15,17,18,20,21,23,24,25,26,32,33,35,36,38] +3V
[17,18,26,32,38] +5V

Reserve

TXC_HDMI+ — C206 *3.3p/50V_4 — TXC_HDMI-

[4] IN_D2 / [4] IN_D2# — C181 / C182 0.1u/6.3V_2 — TX2_HDMI+ / TX2_HDMI-
[4] IN_D1 / [4] IN_D1# — C187 / C193 0.1u/6.3V_2 — TX1_HDMI+ / TX1_HDMI-
[4] IN_D0 / [4] IN_D0# — C196 / C202 0.1u/6.3V_2 — TX0_HDMI+ / TX0_HDMI-
[4] IN_CLK / [4] IN_CLK# — C203 / C205 0.1u/6.3V_2 — TXC_HDMI+ / TXC_HDMI-

R111, R78098, R78099, R124, R78099, R144, R153, R157: 470_1%_2

+3V — Q34 DMN601K-7

S0 S0

[6] HDMI_HPD_Q — R78101 *Short_0402 — HDMI_MB_HPD_R

HDMI SMBus Isolation

+3V — R96 1M_5%_2 — HDMI_MB_HPD_R
+3V — Q10 2N7002K — HDMI_HPD

CPU

+3V — R129 2.2K_5%_2 — [4] INT_HDMI_SCL — Q7846A — HDMI_SCLK
[4,8] INT_HDMI_SDA — Q7846B — HDMI_SDATA
+3V — R116 2.2K_5%_2
SSM6N43FU
+5V

For ESD
Layout note:Place close to HDMI Conn

U29 *AZ1045-04F.R7G
TX2_HDMI+ / TX2_HDMI- / TX1_HDMI+ / TX1_HDMI-

U27 *AZ1045-04F.R7G
TX0_HDMI- / TX0_HDMI+ / TXC_HDMI- / TXC_HDMI+

Layout note:Place close to HDMI Conn
0709 Add D13105 by Intel suggest

D13105 BAT54AW-L
+5V_HDMIC — R121 2.2K_5%_2 — HDMI_SCLK
R122 2.2K_5%_2 — HDMI_SDATA
RV2 *TVM0G5R5M220R_22p
RV1 *TVM0G5R5M220R_22p

U4 G5250Q1T73U
40 mils
+5V — C96399 *220p/25V_2 — RV6 *TVM0G5R5M220R_22p — HDMI_HPD
R78104 *Short_0402 — HDMI_HPD_C
RV5 *TVM0G5R5M220R_22p
C96401 220p/25V_2

R93 20K_1%_2

checklist REV 2.0 : PD 20K

CN18 — 30235-01902-V01

Quanta Computer Inc.	
PROJECT : ZBK_ZBKA	
Size	Document Number: HDMI/Re-timer PS8209A — Rev: 1A
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RTL8111H-CG (LAN)

For LDO mode support
RTL8107ESH-CG/RTL8111HSH-CG
Stuff: La, Ca ,Cb

RTL8111HS
the switching regulator 1.0V output pin (REGOUT)
must be connected only to DVDD10 and AVDD10

* Place Cc,Cd,Ce,Cf for RTL8107ESH-CG/RTL8111HSH-CG close to each VDD10 pin-- 3, 22, 8 , 30

* Place Cg,Ch for RTL8107ESH-CG/RTL8111HSH-CG close to each VDD10 pin-- 22(reserved)

Power trace Layout > 60mil

+1.05V_LAN_REGOUT — R4 La *Short_0805 — +1.05V_LAN

PIN3 Cc C64 0.1u/16V_2
PIN8 Cd C58 0.1u/16V_2
PIN30 Ce C65 0.1u/16V_2
PIN22 Cf C45 0.1u/16V_2
PIN22 Cg C93 1u/6.3V_4
PIN22 Ch C39 0.1u/16V_2
C22 0.1u/16V_2

[3,4,5,7,8,15,17,18,19,21,23,24,25,26,32,33,35,36,38] +3V
[5,12,17,26,27,29,30,31,32] +3VPCU
[2,3,5,7,9,12,21,24,25,26,27,32,33,34,35,37,38] +3V_S5

LAN_AMBLED# TP4
LAN_LED1 TP2
LAN_LED2 TP3

if ISOLATEB pin pull-low,
the LAN chip will not drive it's PCI-E outputs
(excluding PCIE_WAKE# pin)

+1.05V_LAN
R6 2.49K_1%_4
+3V_LAN
LAN_AMBLED#
LAN_LED1
RSET XTAL2 XTAL1 ONN_LED1 DAN_LED2

U1 RTL8111H-CG
GND (33) — Add 9 GND VIAs with thermal PAD
AVDD33#2 RSET AVDD33#3 CKXTAL2 CKXTAL1 LED1/GPO LED2

+3V
R31 1K_5%_2
ISOLATEB
R30 15K_1%_4

XTAL1
Y1 25MHZ/30ppm
XTAL2_R R15 680_1%_2 XTAL2
C33 18p/50V_2
C32 18p/50V_2

MDI0+ MDI0- MDI1+ MDI1- MDI2+ MDI2- MDI3+ MDI3-
MDIP0 MDIN0 AVDD10#1 MDIP1 MDIN1 MDIP2 MDIN2 AVDD10#2
MDIP3 MDIN3 AVDD33#1 CLKREQB HSIP HSIN REFCLK_P REFCLK_N

REGOUT VDDREG DVDD10 LANWAKEB ISOLATEB PERSTB HSON HSOP
+1.05V_LAN_REGOUT
+3V_LAN
R6643 *Short_0201
PCIE_WAKE# [7,24,26]
*ISOLATEB
*PLTRST#
PLTRST# [7,15,22,24,26]
*PCIE_RXN_LAN_L C88 0.1u/16V_2
*PCIE_RXP_LAN_L C94 0.1u/16V_2
PCIE_RXN4_LAN [3]
PCIE_RXP4_LAN [3]

CLK_PCIE_LANN [5]
CLK_PCIE_LANP [5]
PCIE_TXN4_LAN [3]
PCIE_TXP4_LAN [3]

For GbE
* Place RTL8111HSH-CG AL008111014
For 10/100
* Place RTL8107ESH-CG AL008107000

Leakage circuit (MPC)

PCIE_CLKREQ_LAN# have PU 10k.
S0 [5] PCIE_CLKREQ_LAN#
+3V — R55 *10K_5%_2 — MAIN POWER(3V_S0)
Q6 *2N7002K
PCIE_REQ_LAN#_R
R44 *Short_0201

* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8107ESH-CG/RTL8111HSH-CG

* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

+3V_LAN
PIN11 C42 0.1u/16V_2 Cj
PIN32 C51 0.1u/16V_2 Ck
PIN11 C30 *4.7u/6.3V_4 Cm
PIN32 C31 *4.7u/6.3V_4 Cn

H=4

For Giga：Ub

U13 NS892407
TD1+ TD1- TD2+ TD2- TD3+ TD3- TD4+ TD4-
MX1+ MX1- MX2+ MX2- MX3+ MX3- MX4+ MX4-
TRA_V_DAC TCT1 TCT2 TCT3 TCT4
MCT1 MCT2 MCT3 MCT4
LAN_MCTG0 Ra R78343 75_1%_8
LAN_MCTG1 Rb R78344 75_1%_8
LAN_MCTG2 Rc R3 75_1%_8
LAN_MCTG3 Rd R2 75_1%_8
C96624 0.01u/50V_4
C321 10p/3KV_1808
LANGND

For 10/100：Ra,Rb
For Giga：Ra,Rb,Rc,Rd

For GiGA
BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00
EOH:GS2411C DBG7AKLAN00

RJ45

30mil
CN6
MDI3-_1 MDI3+_1 MDI1-_1 MDI2-_1 MDI2+_1 MDI1+_1 MDI0-_1 MDI0+_1
2RJ3057-008211F

LAN Wake Power Control (Control by Bios Menu)

Q2 LAN@DMP2130L-7
+3VPCU
C28 LAN@0.1u/16V_2
R5 LAN@100K_5%_2
[25] LANPWR#
R14 LAN@10K_5%_2
C37 LAN@1000p/50V_4
+3V_LAN
R7 *0_5%_8
+3V_S5
C23 10u/6.3V_6
C25 0.1u/16V_2
C24 0.1u/16V_2
C29 0.1u/16V_2

C96403 *0.1u/16V_4
C96404 *0.1u/16V_4
C96405 *0.01u/50V_4
C96406 *0.01u/50V_4
R78024 *Short_0603
R78025 *Short_0603
LANGND

(EMC)
MDI0+_1 MDI0-_1 D13100 *MESD05N92ULA LANGND
MDI1+_1 MDI1-_1 D13101 *MESD05N92ULA LANGND
MDI2+_1 MDI2-_1 D13102 *MESD05N92ULA LANGND
MDI3+_1 MDI3-_1 D13103 *MESD05N92ULA LANGND

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	LAN RTL8166EH/RTL8111HSH	1A

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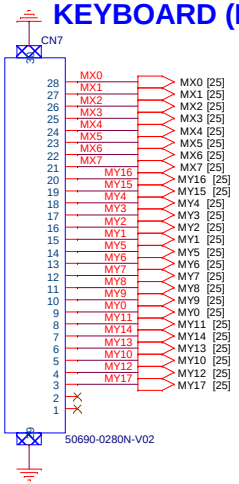
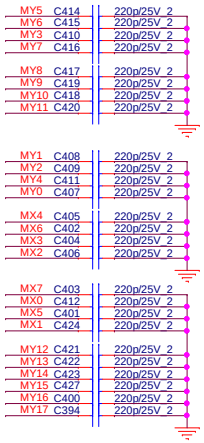
KEYBOARD (KBC)

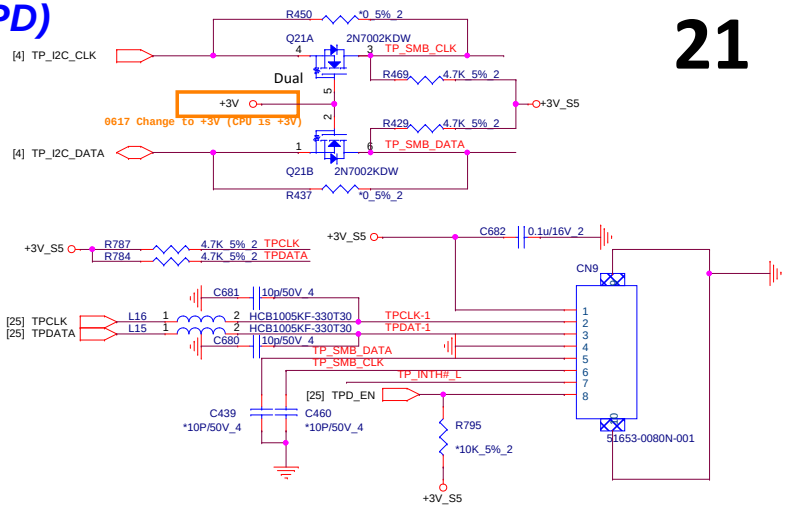


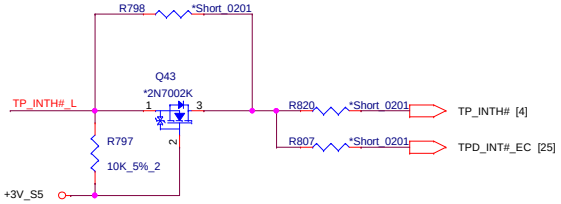


(EMC)

KB_BL LED (KBL)

Touch Pad (TPD)





FAN (THM)

21

Quanta Computer Inc.

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	KB/TP	1A

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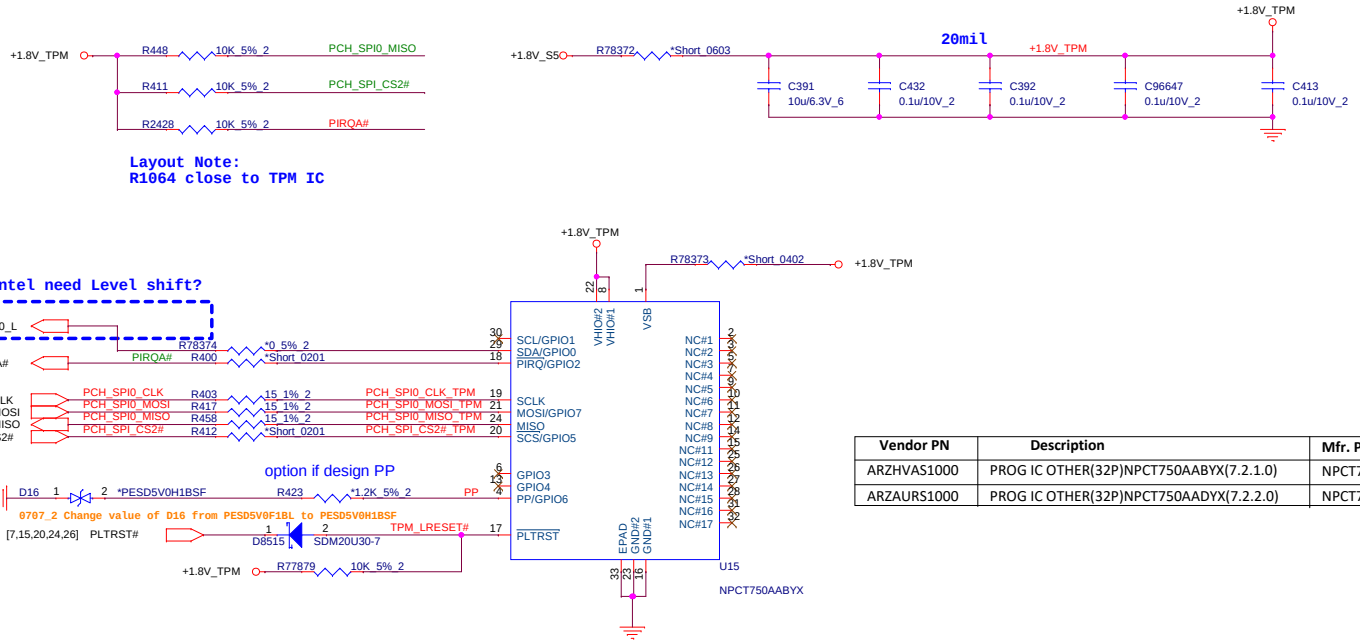
TPM NPCT750

(TPM)

[15,18,25,38] +1.8V
[3,4,5,7,8,15,17,18,19,20,21,23,24,25,26,32,33,35,36,38] +3V
[5,12,17,20,26,27,29,30,31,32] +3VPCU
[6,9,12,23,25,26,37,38] +1.8V_S5



Vendor PN	Description	Mfr. Part Number
ARZHVAS1000	PROG IC OTHER(32P)NPCT750AABYX(7.2.1.0)	NPCT750AABYX
ARZAURS1000	PROG IC OTHER(32P)NPCT750AADYX(7.2.2.0)	NPCT750AADYX

0707_2 Change TPM from NPCT750AAAYX(7.2.0.1) to NPCT750AABYX(7.2.1.0)

PBA (PBA@)

(FPD)

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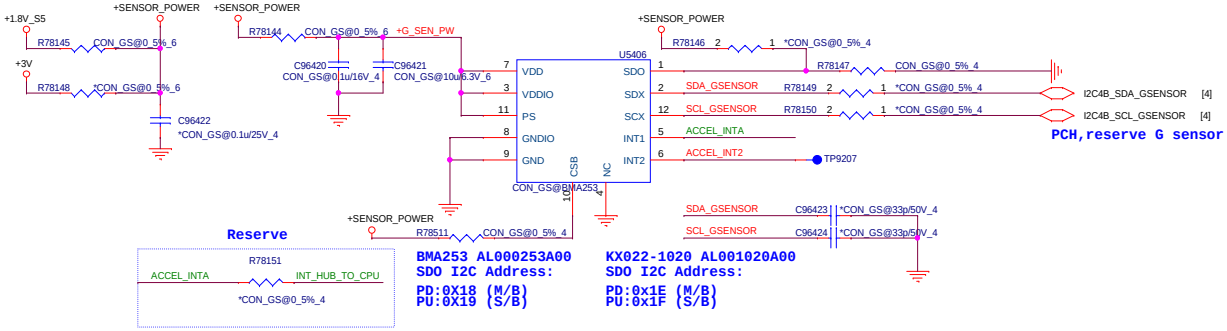
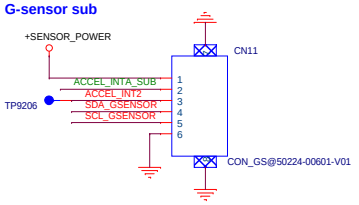
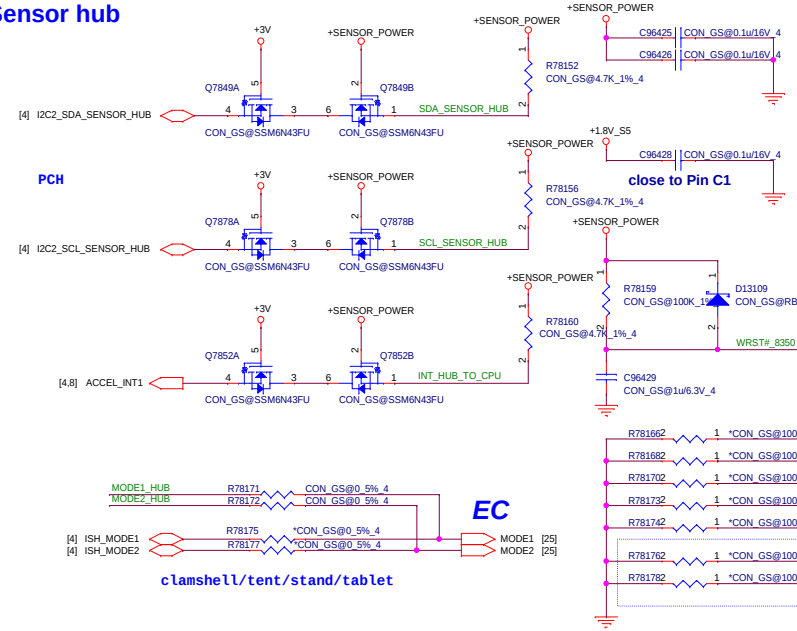
G-sensor

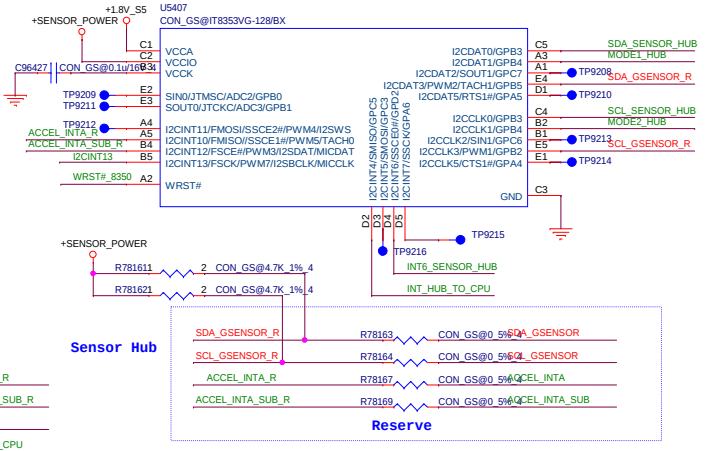


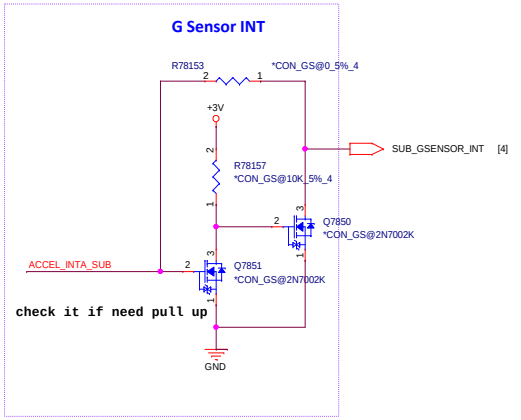
G-sensor sub



Sensor hub







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	SENSOR HUB	1A
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SSD

PCIE SSD M2

SATA SSD M2

CN12 NGFF MKEY

100 mils 1.4A

0603 Follow ICELAKE to reverse it

0709 Delete R847/R848 by Intel suggest connect to Conn directly

SSD PCIE I/F --> L

SSD SATA I/F --> H

0612 Change Detect design for SATA/PCIE compatible

0629 DNS Q59 & R894 for un-use

SSD@NASM0-B6701-TS18

SATA SSD M2

Close to R849/R850/C96311/C96312

0624_2 Add for SATA SSD

WLAN(Wifi)

(NGF)

CN13 NGFF EKEY

NASE0-S6701-TSH4

Different with ZBY

Close Pin4

Close Pin72

Close Pin2

100mils

M2 WLAN PCIE RTD3

Quanta Computer Inc.			
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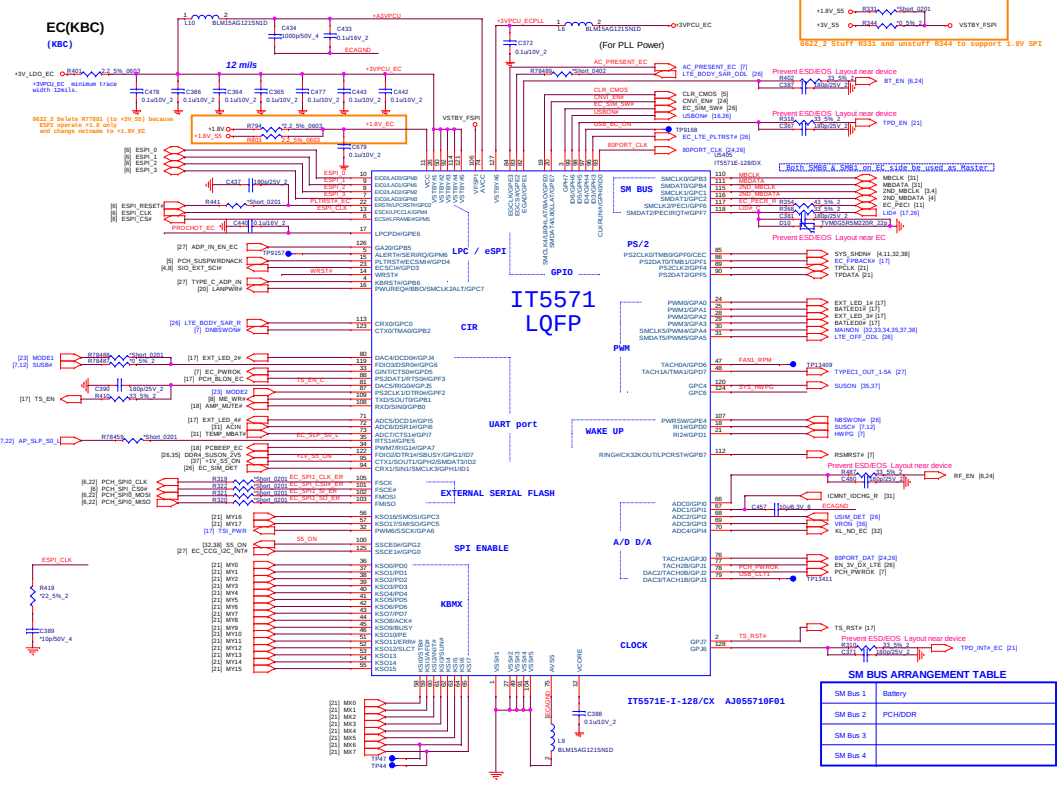
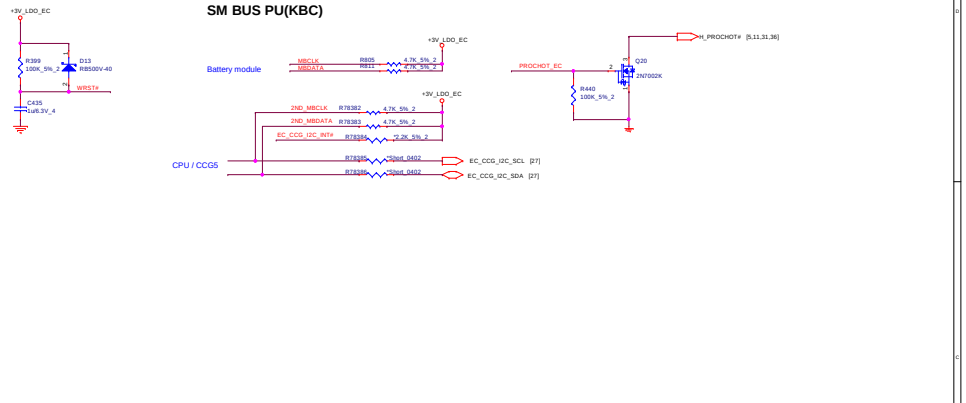
EC(KBC)

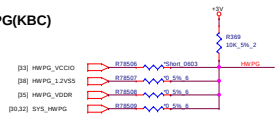
(KBC)



SM BUS PU(KBC)

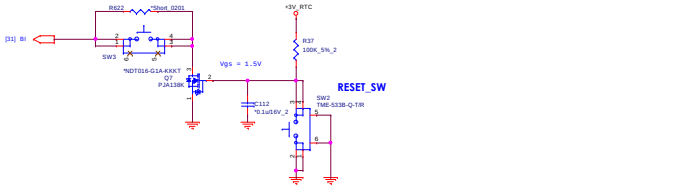


HWPG(KBC)

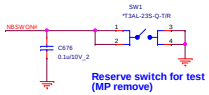


Reset SW (FSW)

Battery Detect Switch



Reserve switch for test (MP remove)



Reserve switch for test (MP remove)

recommad use same as SW2 shortage problem

Quanta Computer Inc.
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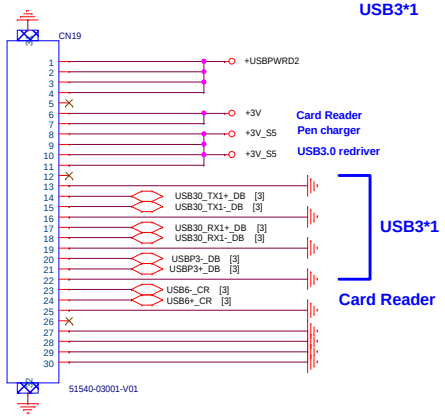
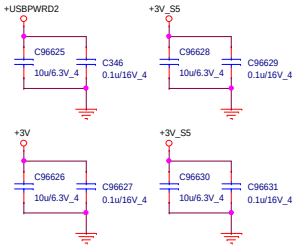
USB Board (OTH)

D/B Port

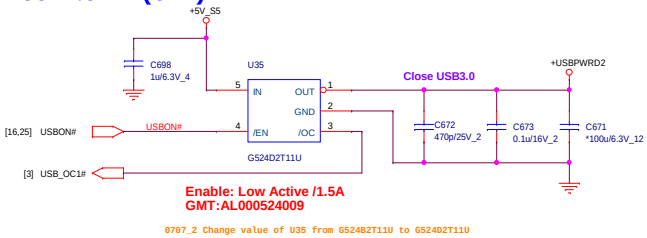
[3,4,5,7,8,15,17,18,19,20,21,23,24,25,32,33,35,36,38] +3V
[5,12,17,20,27,29,30,31,32] +3VPCU
[17,18,19,32,38] +5V
[12,16,32,35,36,37] +5V_S5

USB3*1

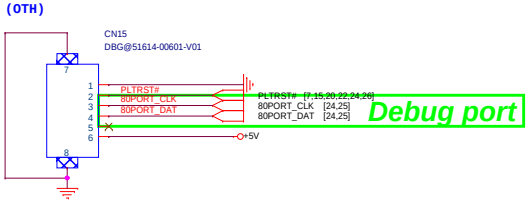




USB2.0 DB (UB2)

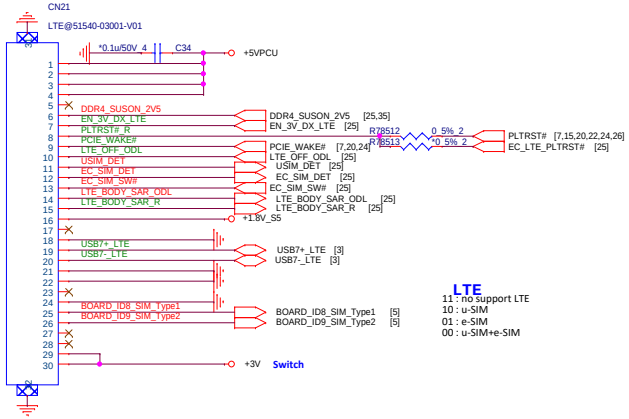


(OTH)

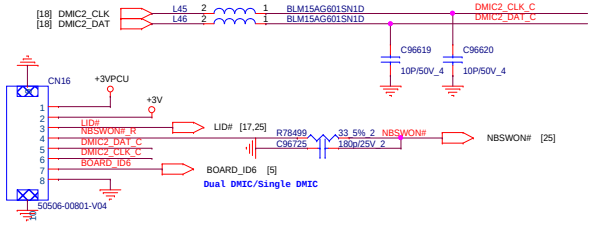


LED(UIF)

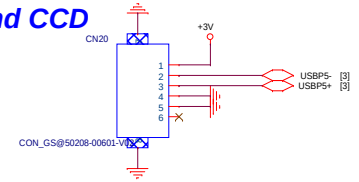
LTE Connector



Hall sensor + 2nd DMIC DB



2nd CCD



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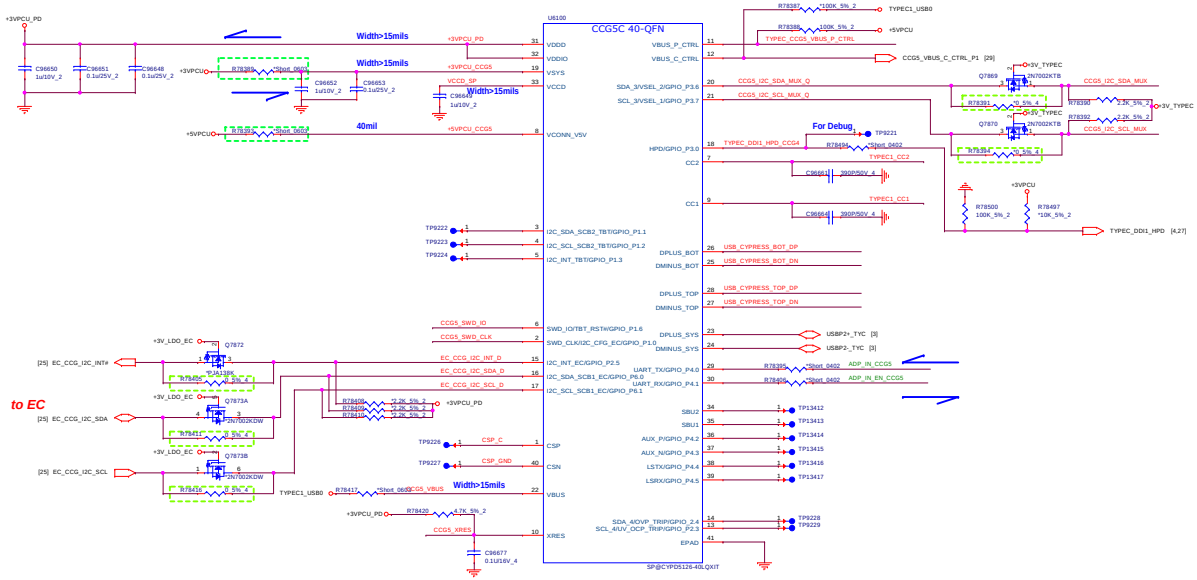
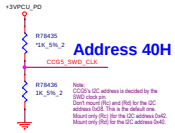
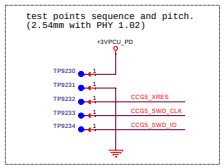
CCG5

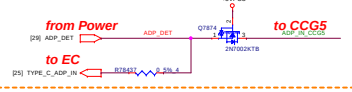






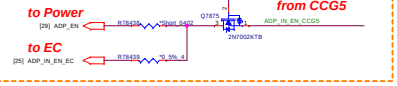
Detect DC Jack plug-in

ADP Insert	ADP_DET
Y	Hi
N	Low

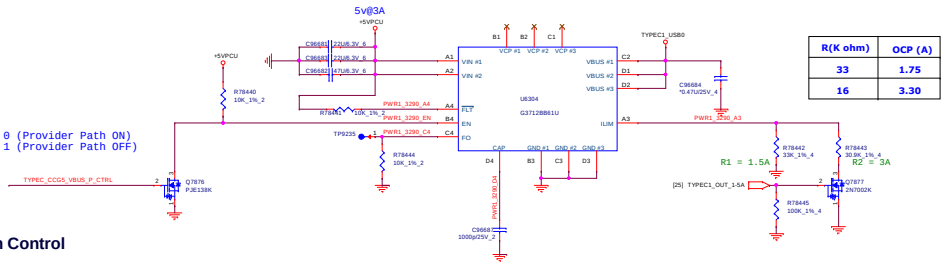


Control let Adaptor Power in or not

ADP_EN	ADP Switch
Hi	ON
Low	OFF

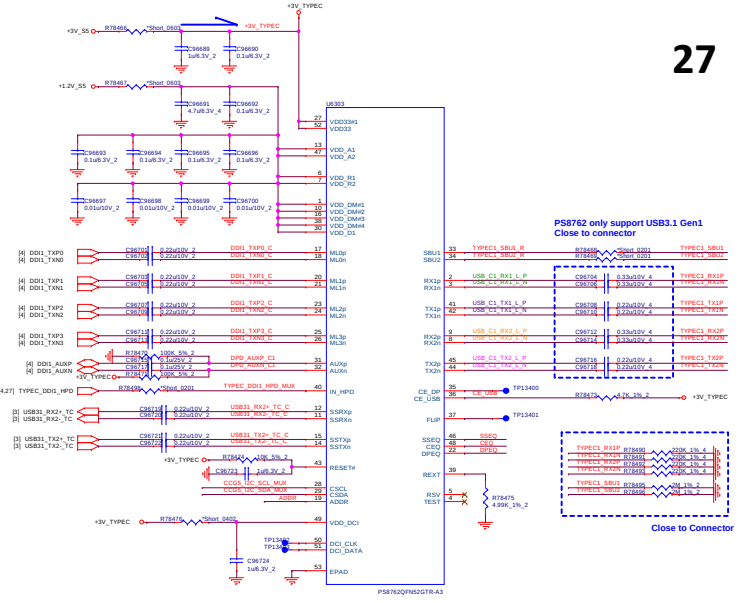


PD



R(K ohm)	OCP (A)
33	1.75
16	3.30

Provider Path Control

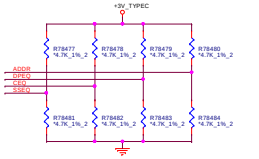


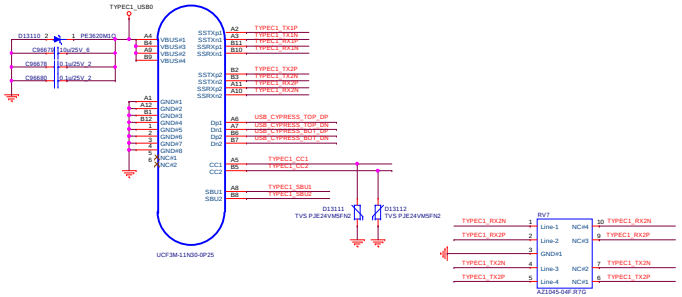
ADDR: I2C control bus address. Internally pull down at 150kΩ, 3.3V I/O.
L: Slave address 0x10-0x2F(default)
H: Slave address 0x30-0x4F

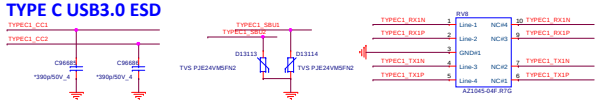
DPEQ:DP Receiver equalization setting; Internally pull down at 150kΩ, 3.3V I/O.
L: Compensation for channel loss up to 12dB(Default)
H: Compensation for channel loss up to 18dB

CEQ: USB Type-C connector facing Rx channel receiver equalization setting; Internally pull down at 150kΩ, 3.3V I/O.
L: Compensation for channel loss up to 16dB(Default)
H: Compensation for channel loss up to 18dB

SSEQ: USB Host facing Rx channel receiver equalization setting; Internally pull down at 150kΩ, 3.3V I/O.
L: Compensation for channel loss up to 12dB(Default)
H: Compensation for channel loss up to 18dB







Hole

HOLE1
*H-C276D236P2

HOLE3
*H-TC276IC98BC221D98P2

HOLE4
*H-C315D126P2

HOLE5
*H-TC276IC98BC221D98P2

HOLE6
*H-TC295BIC236D126P2

HOLE7
*H-C295D126P2

HOLE8
*H-C256D126P2

HOLE10
*H-C315IC165D165P2

HOLE11
*H-C315IC165D165P2

HOLE12
H-C236D148P2

WiFi Nut

HOLE13
*H-C276IC165D165P2

HOLE15
*H-TC236IC98BC197D98P2

HOLE14
*H-C118D118N

HOLE16
*o-zbk-1

2D Bar Code

HOLE17
*2D-BARCODE-6X6-S

HOLE18
*2D-BARCODE-8X8-S

PAD

PAD1
*SPAD-ZBK-1

PAD2
*SPAD-ZBK-2

PAD3
*SPAD-315X197

PAD4
*SPAD-138X315

PAD5
*SPAD-138X315

PAD6
*SPAD-315X236

PAD7
*SPAD-138X315

PAD8
*SPAD-ZBK-3

PAD9
*SPAD-394X369

PAD10
*SPAD-C315P

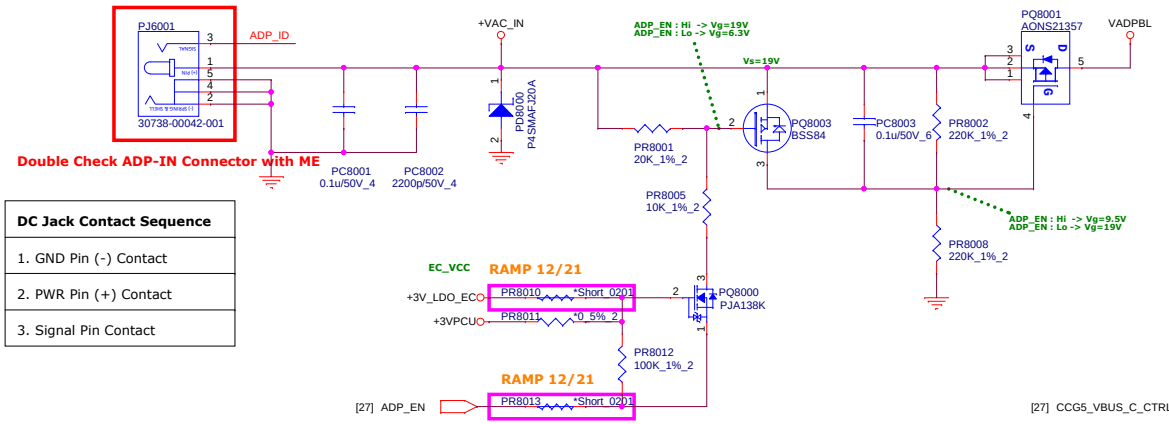
PAD11
*SPAD-RE322X98

Quanta Computer Inc.

PROJECT : ZBK_ZBKA

Size	Document Number	Rev
	HOLE	1A
Date: Monday, January 04, 2021	Sheet 28 of 39	

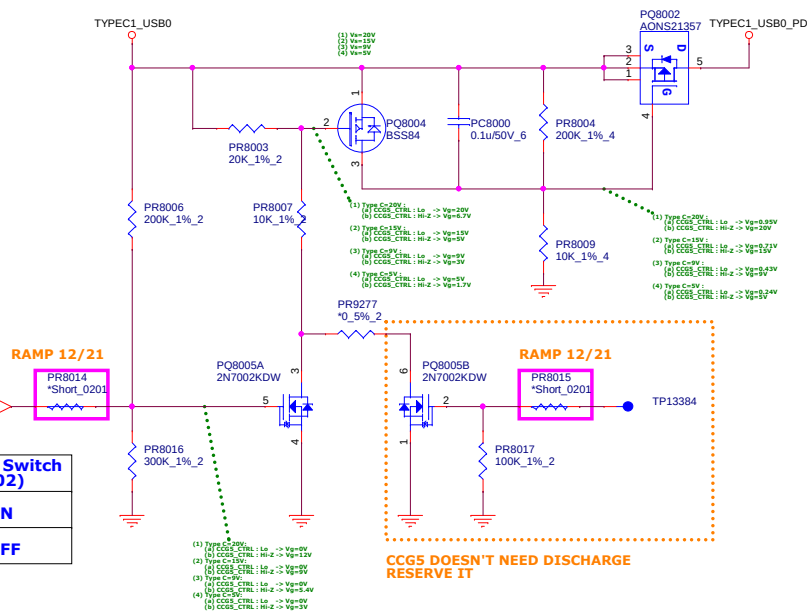
ADP = 19V



DC Jack Contact Sequence
1. GND Pin (-) Contact
2. PWR Pin (+) Contact
3. Signal Pin Contact

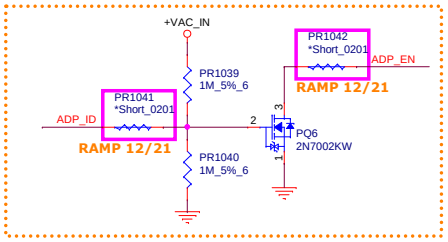
ADP_EN	ADP Switch (PQ8001)
Hi	ON
Low	OFF

Type C = 20V/15V/9V/5V (USB PD 3.0)



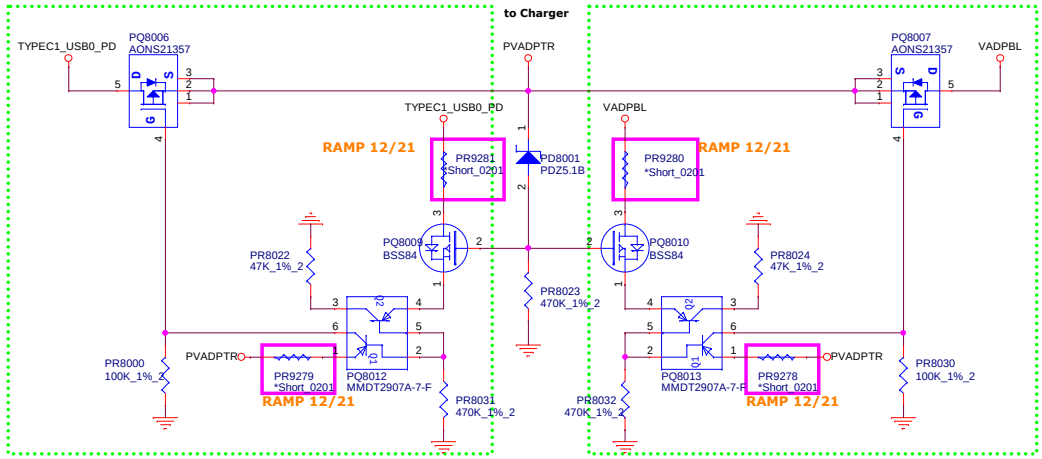
CCG5_CTRL	Type C Switch (PQ8002)
Low	ON
High-Z	OFF

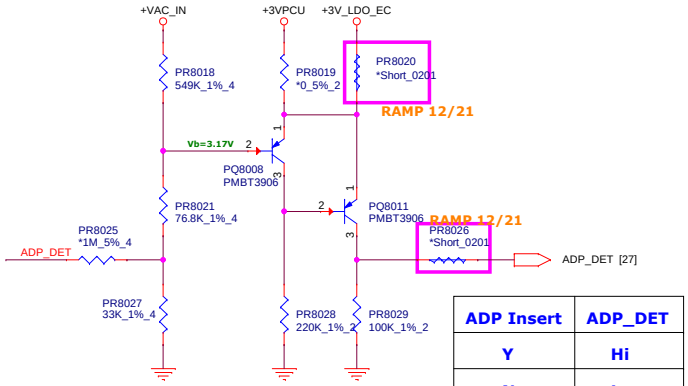
Adaptor ID Pin



Ideal Diode for Type-C Port

Ideal Diode for Adapter





ADP Insert	ADP_DET
Y	Hi
N	Low

Vi compare	Vo (=PVADPTR)
TYPEC1_USB0 > VADPBL	TYPEC1_USB0
TYPEC1_USB0 < VADPBL	VADPBL

Quanta Computer Inc.
PROJECT : Z8I_ZAI_Z8J

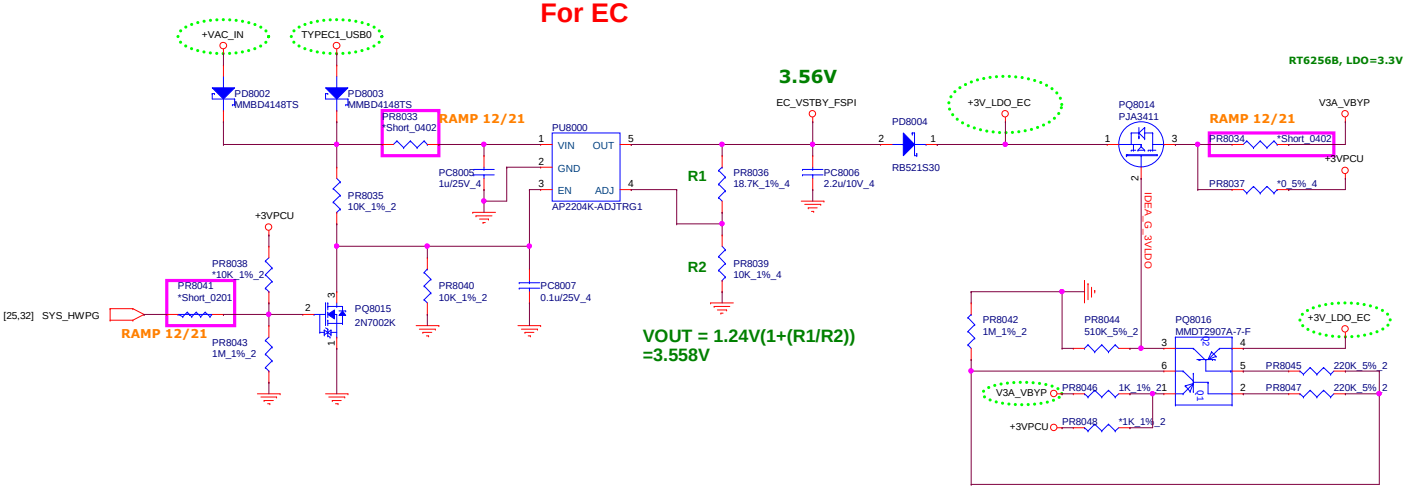
Size	Document Number	Rev
	ADP-IN & TYPE-C	1A

Date: Monday, February 01, 2021 Sheet 29 of 39

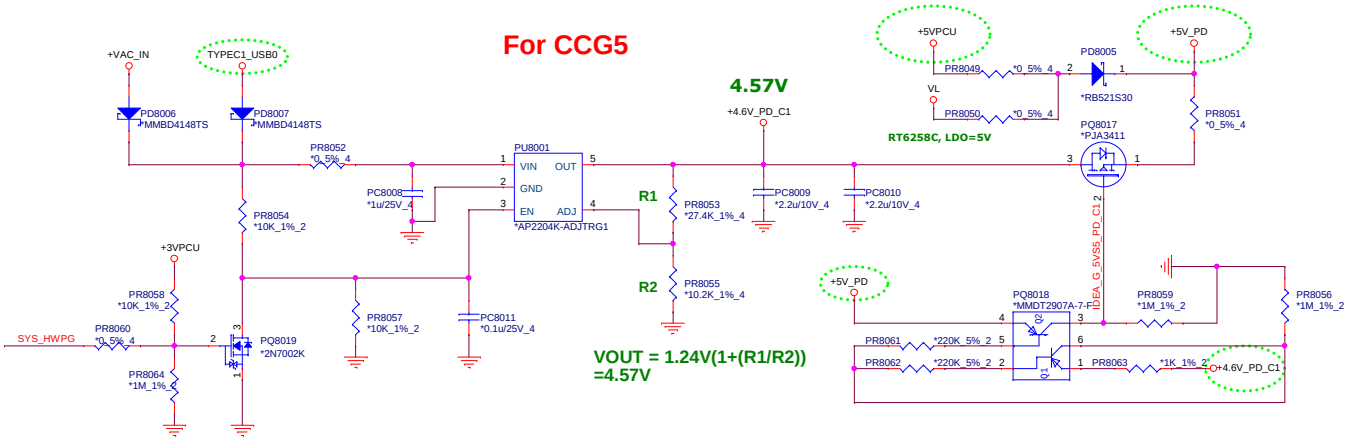
Dead Battery

+VAC_IN [29]
TYPEC1_USB0 [27,29]
V3A_VBYP [32]
+3V_LDO_EC [25,27,29,32]
+3VPCU [5,12,17,20,26,27,29,31,32]
+5VPCU [18,26,27,32,38]

For EC



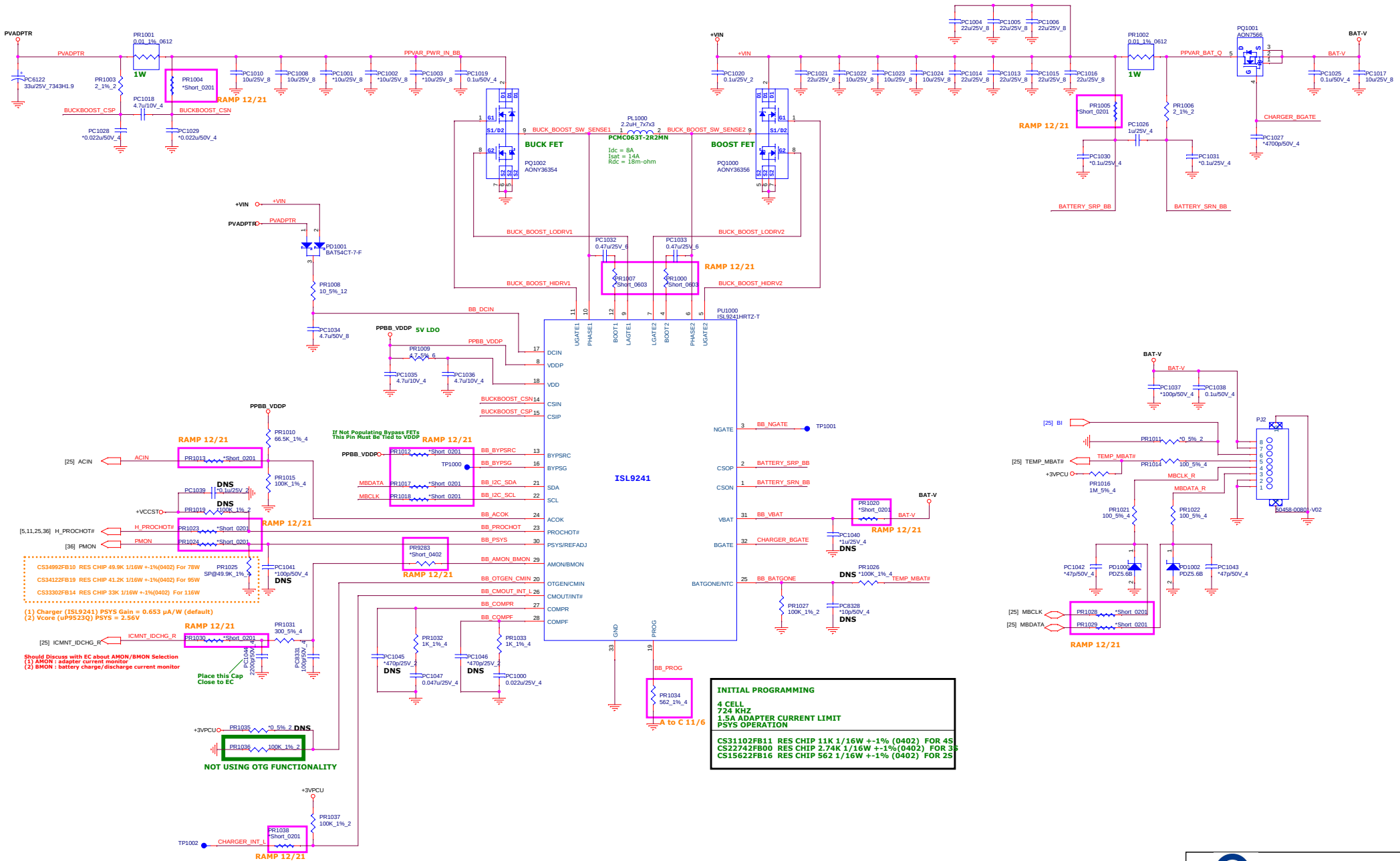
For CCG5



Quanta Computer Inc.		
PROJECT :		
Size	Document Number: Dead Battery	Rev: 1A
Date: Monday, January 11, 2021	Sheet 30 of 39	

INTERSIL BUCK-BOOST CHARGER

PVADPTR [29]
+VIN [17,32,33,35,36,37,38]
+3VPCU [5,12,17,20,26,27,29,30,32]
+VCCST [7,9,11,12,36]



Quanta Computer Inc.			
PROJECT : Z8Y			
Size	Document Number		Rev
	Charger (ISL9241HRTZ-T)		1A
Date: Monday, January 04, 2021	Sheet 31 of 39		

+VIN [17,31,33,35,36,37,38]
+3VPCU [5,12,17,20,26,27,29,30,31]
+5VPCU [18,26,27,30,38]
VL [30,38]

+5V [17,18,19,26,38]
+5V_S5 [12,16,26,35,36,37]
+3V [3,4,5,7,8,15,17,18,19,20,21,23,24,25,26,33,35,36,38]
+3V_S5 [2,3,5,7,9,12,20,21,24,25,26,27,33,34,35,37,38]

+3VPCU
3.3 Volt +/- 5%
TDC : 6A
Width : 240mil
FSW : 500KHZ

To Thermal Protection

RAMP 12/21

(1) USM : 0.8V-1.7V
(2) Normal Mode : >2.3V

PU14 RT6256BGQUF

LDO=3.3V/100mA

High frequency noise eliminate circuit

Power Auto Recovery
(Stuff on dead battery page)

VCC=5V
(DON'T Connect to External Load)

TDC : 2.71A
PEAK : 3.6A
Width : 120mil

TDC : 4.8A
PEAK : 5.28A
Width : 200mil

PU4 JW7110DFNC_TRPBF

+5VPCU
5 Volt +/- 5%
TDC : 8A
Width : 320mil
FSW : 750KHZ

PU16 RT6258CGQUF

LDO=5V/100mA

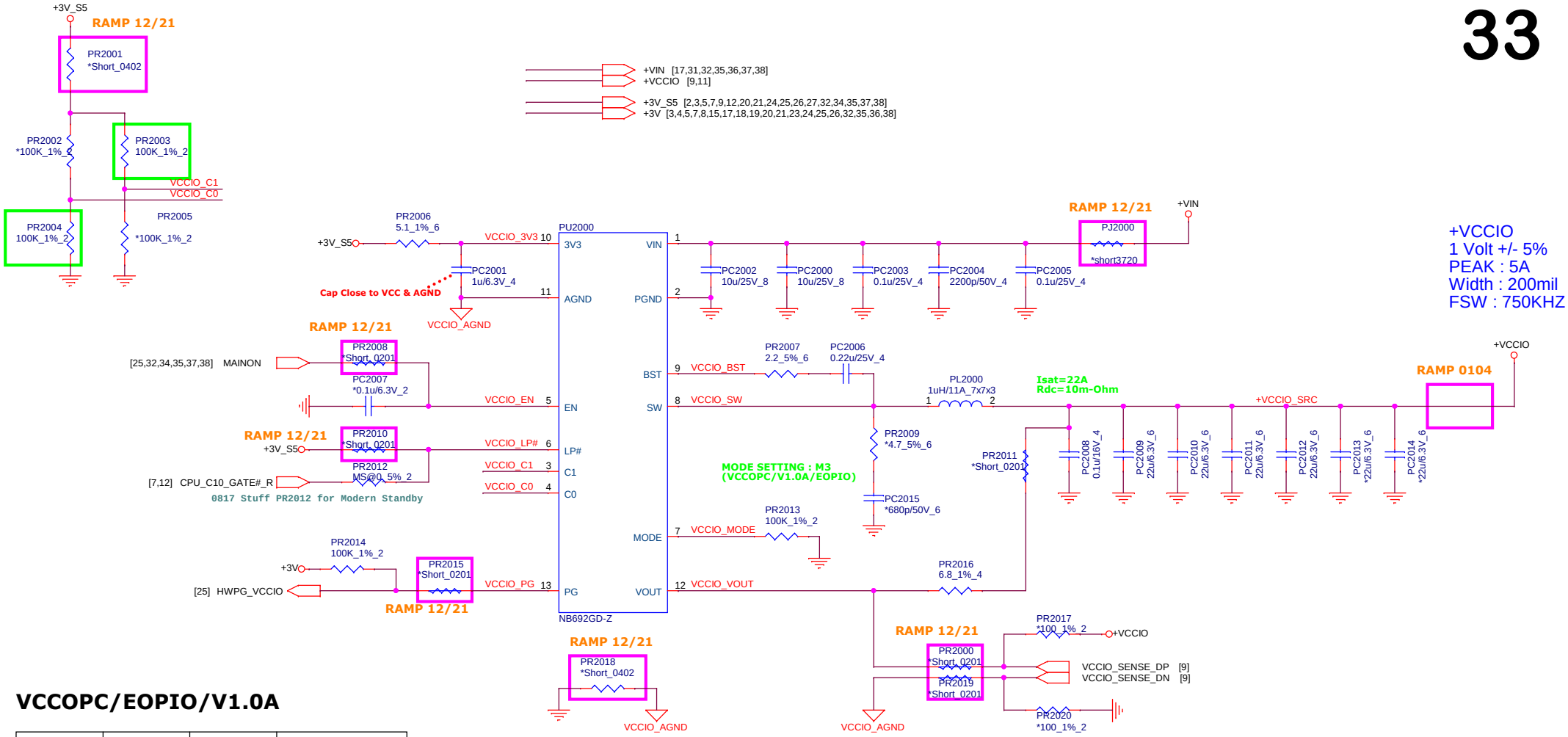
VCC=5V
(DON'T Connect to External Load)

TDC : 6A
PEAK : 6.6A
Width : 330mil

TDC : 1A
PEAK : 1.1A
Width : 60mil

PU6 JW7110DFNC_TRPBF

Quanta Computer Inc.			
PROJECT : Z8Y			
Size	Document Number		Rev
	SYSTEM 5V/3V (RT6256B/RT6258C)		1A
Date: Monday, January 04, 2021	Sheet 32 of 39		



VCCOPC/EOPIO/V1.0A

LP#	C1	C0	VOUT (V)
0	X	X	0V
1	0	0	0.8V
1	0	1	0.95V
1	1	0	1V
1	1	1	1.05V

Default Setting

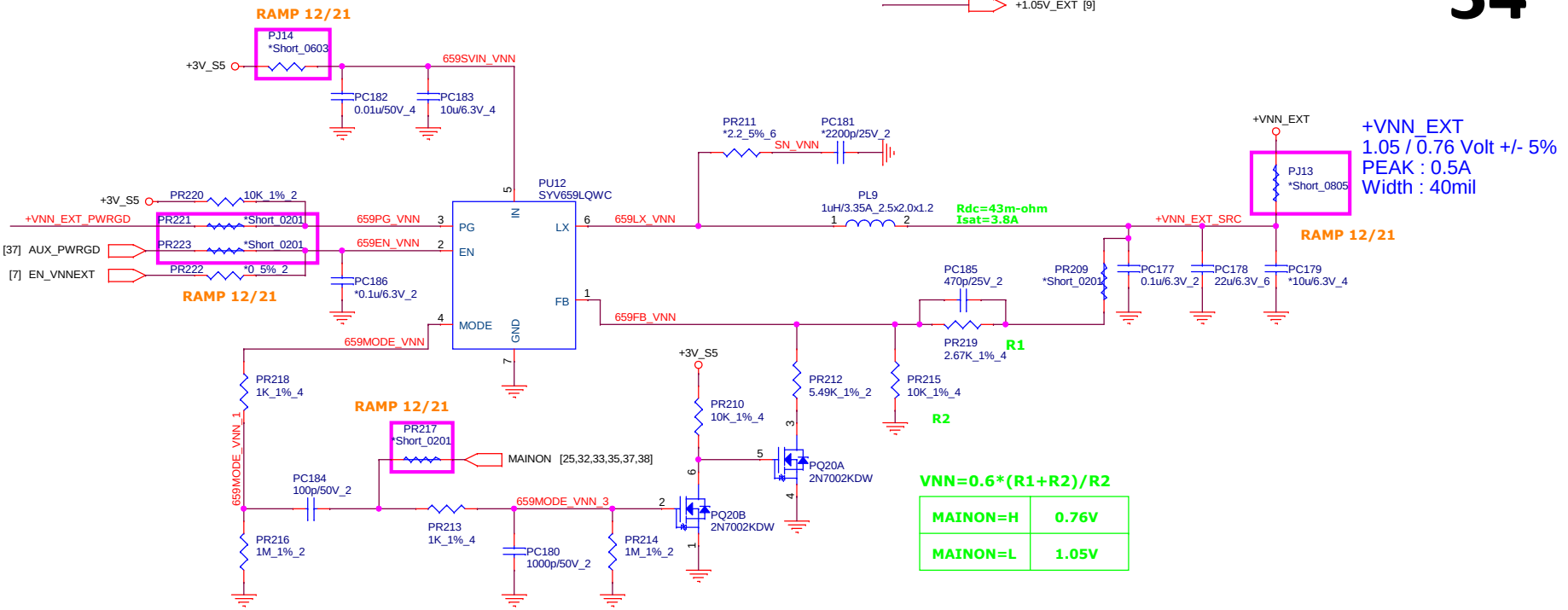
Quanta Computer Inc.

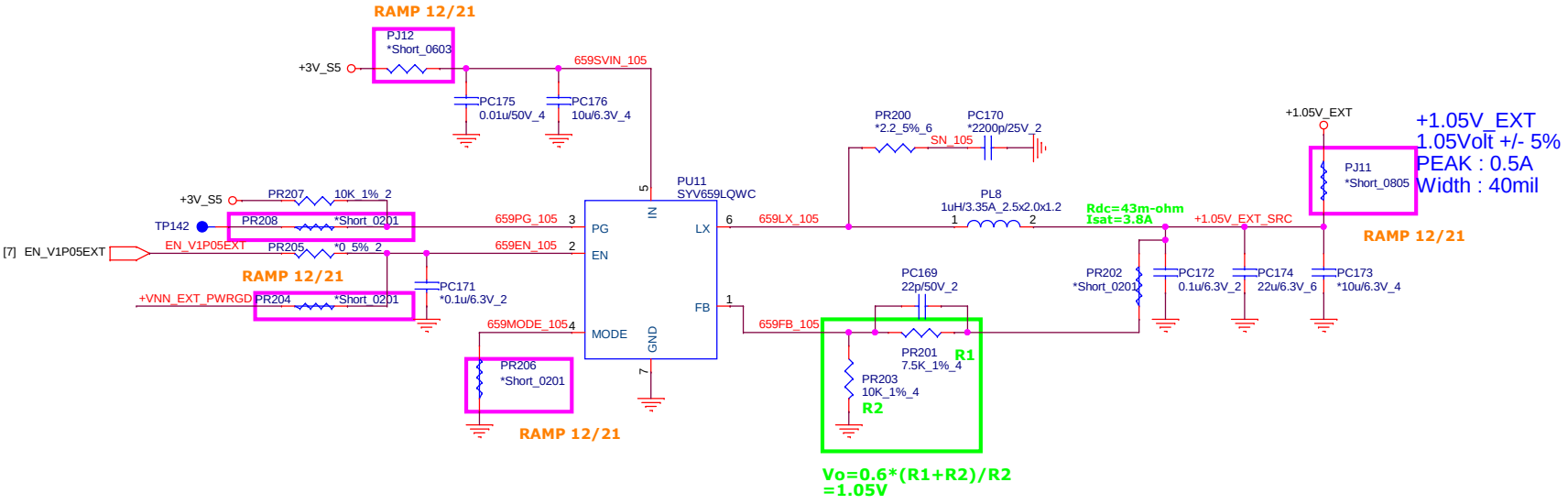
PROJECT : Z8Y

Size	Document Number	Rev
	+VCCIO (NB692GD-Z)	1A

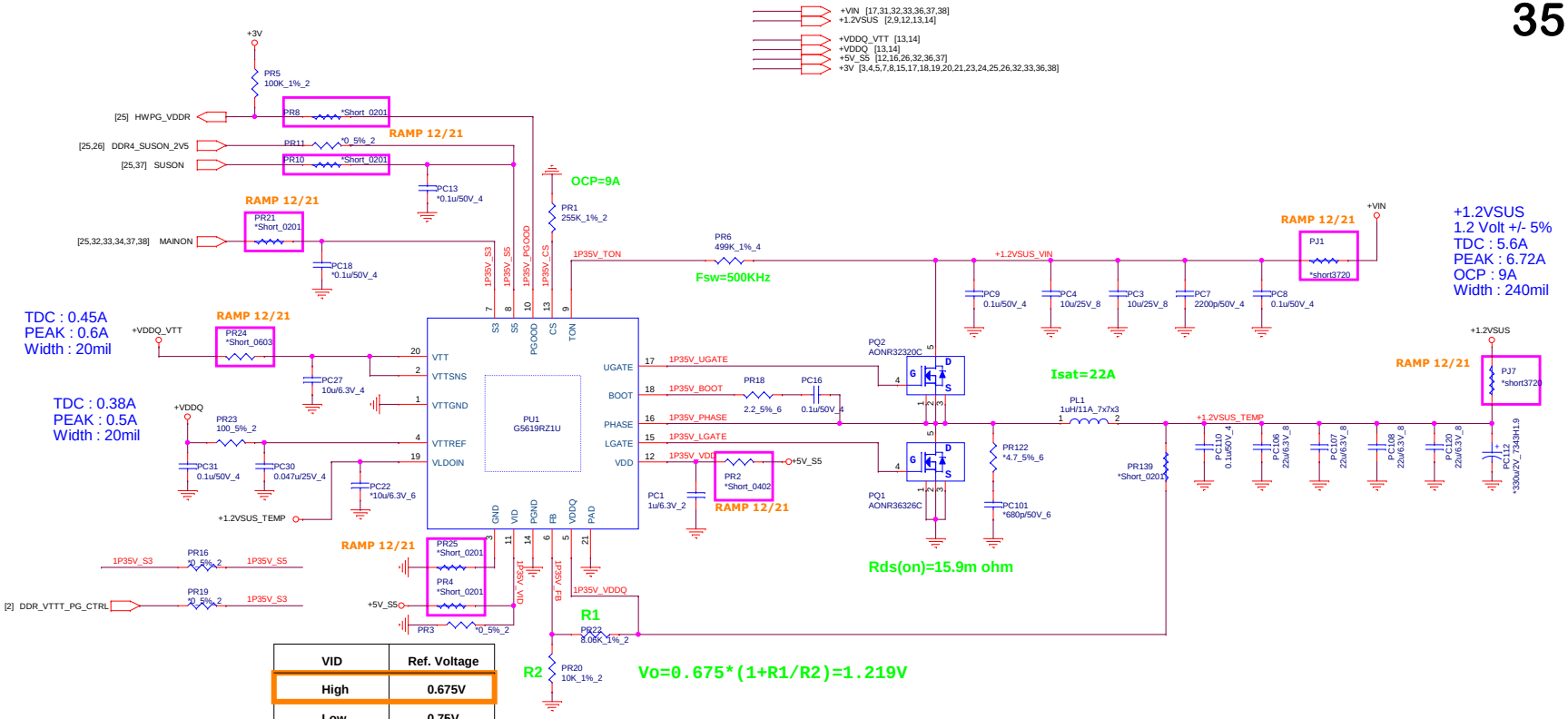
Date: Monday, January 04, 2021 Sheet 33 of 39

+3V_S5 [2,3,5,7,9,12,20,21,24,25,26,27,32,33,35,37,38]
+VNN_EXT [9]
+1.05V_EXT [9]





Quanta Computer Inc.	
PROJECT : Z8Y	
Size	Document Number: +VNN_EXT & +1.05V_EXT (SYV659LQWC) — Rev 1A
Date: Monday, January 04, 2021	Sheet 34 of 39



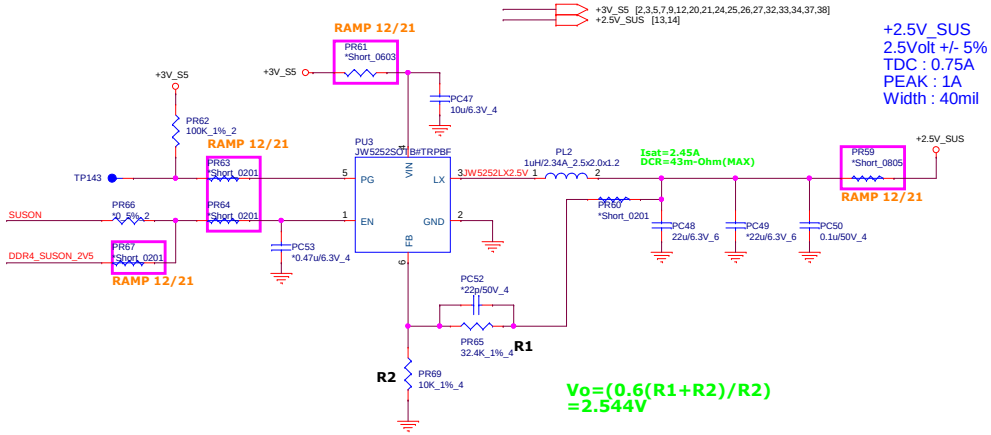
VID	Ref. Voltage
High	0.675V
Low	0.75V

OCP=9A
L ripple current
=(19-1.2)*1.2/(1u*500k*19)
=2.248A
Vtrip=[9-(2.248/2)]*15.9mohm
=125.228mV
Rlimit=125.228mV/5uA*10=250.456Kohm
=255kohm

DDR=1.219V
R1=8.06K/F_2
R2=10K/F_2

	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	ON	ON	ON
S3 (mainon off)	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

+2.5VSUS Power Rail For DDR4



Quanta Computer Inc.
PROJECT : Z8Y

Size	Document Number	Rev
	DDR4_+1.2VSUS (G5619RZ1U)	1A

Date: Monday, January 04, 2021 Sheet 35 of 39

+VIN [17,31,32,33,35,37,38]
+VCCIN [9]
+5V_S5 [12,16,26,32,35,37]
+3V [3,4,5,7,8,15,17,18,19,20,21,23,24,25,26,32,33,35,38]
+VCCST [7,9,11,12,31]

JSL_4 Core 10W

+VCCIN
TDC : 10A
ICCMAX : 35A
DC_LL = 2m
VBOOT = 1.8V
FSW = 600KHz

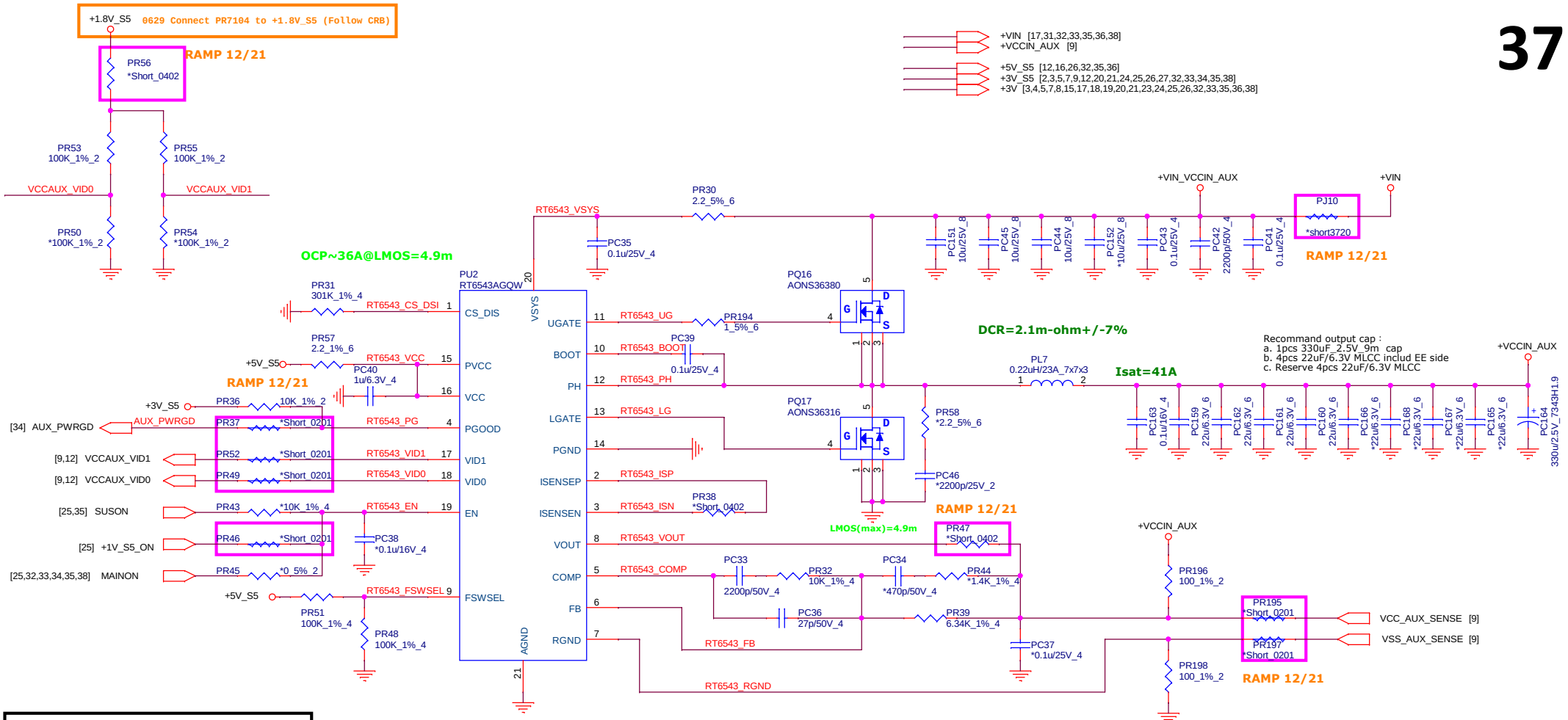
RAMP 1/4
RAMP 12/21
DCR=1.19m-ohm+/-5%
Isat=35A
Don't Connect Pin2 to Phase
Close to IC
Close to Phase1 Inductor
Close to Phase1 MOSFET
A to C 11/6
(1) uP9523Q : PSYS = 2.56V
(2) Double Check PMON Setting with charger (ISL9241)
Recommand output cap:
a. 1pcs 330uF/2.5V_9m cap
b. 13pcs 22uF/6.3V MLCC includ EE side
c. Reserve 4pcs 22uF/6.3V MLCC

PU6000 UP9523QQKI

PROG1 Dynamic VID Transition Boost = 30mV
PROG2 Iccmax = 35A
PROG3 Load Line = 2mΩ
PROG4 Switching Frequency = 600kHz

FSW=600KHz

Quanta Computer Inc.	
PROJECT :	
Size	Document Number: CPU VR IC (uP9523QQKI) — Rev 1A
Date: Monday, January 04, 2021	Sheet 36 of 39



+VCCIN_AUX
JSL_4 Core 10W

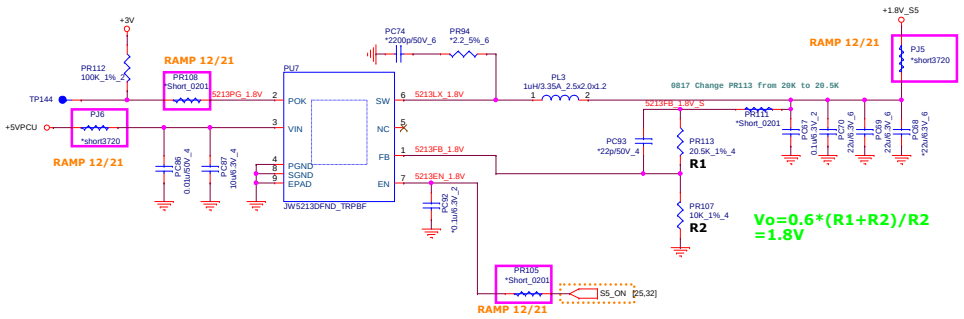
TDC : 4A
ICCMAX : 24A
LL = 0m
VBOOT = 1.8V

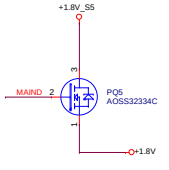
Quanta Computer Inc.		
PROJECT :		
Size	Document Number: VCCIN_AUX IC (RT6543AGQW)	Rev: 1A
Date: Monday, January 04, 2021	Sheet 37 of 39	

+5V_S5 [12,16,26,32,35,36,37]
+3V_S5 [2,3,5,7,9,12,20,21,24,25,26,27,32,33,34,35,37]
+1.8V_S5 [6,9,12,22,23,25,26,37]
+1.8V [15,18,25]
+1.2V_S5 [27]

VL [30,32]
+VIN [17,31,32,33,35,36,37]
+3V [3,4,5,7,8,15,17,18,19,20,21,23,24,25,26,32,33,35,36]
+5V [17,18,19,26,32]

+1.8V_S5
1.8Volt +/- 5%
TDC : 3A
PEAK : 4A
Width : 120mil

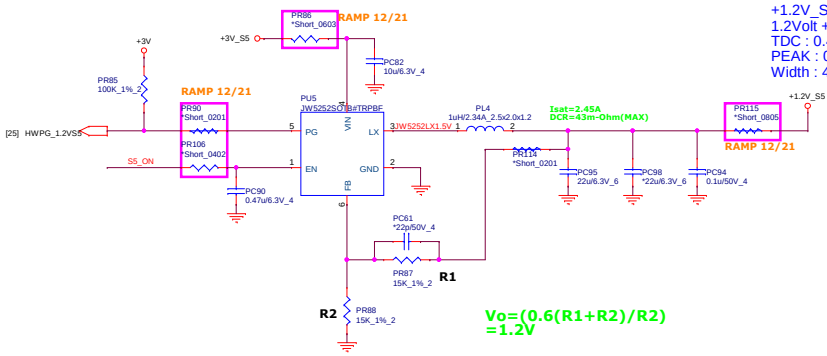




TDC : 0.6A
PEAK : 0.8A
Width : 40mil

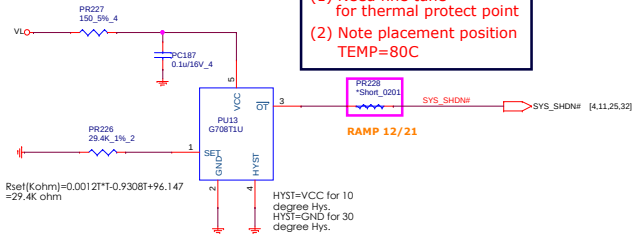
2020/9/2 Del +1.5V (Not Need to Co-layout Audio Codec ALC255)
2020/9/4 Change +1.5V to +1.2V_S5 (for Type-C MUX IC PS8762)

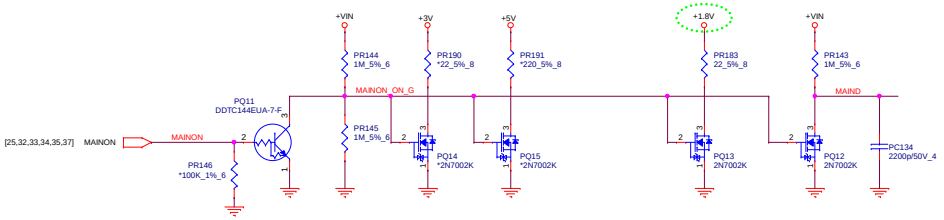
+1.2V_S5
1.2Volt +/- 5%
TDC : 0.4A
PEAK : 0.53A
Width : 40mil



Thermal protection

(1) Need fine tune
for thermal protect point
(2) Note placement position
TEMP=80C

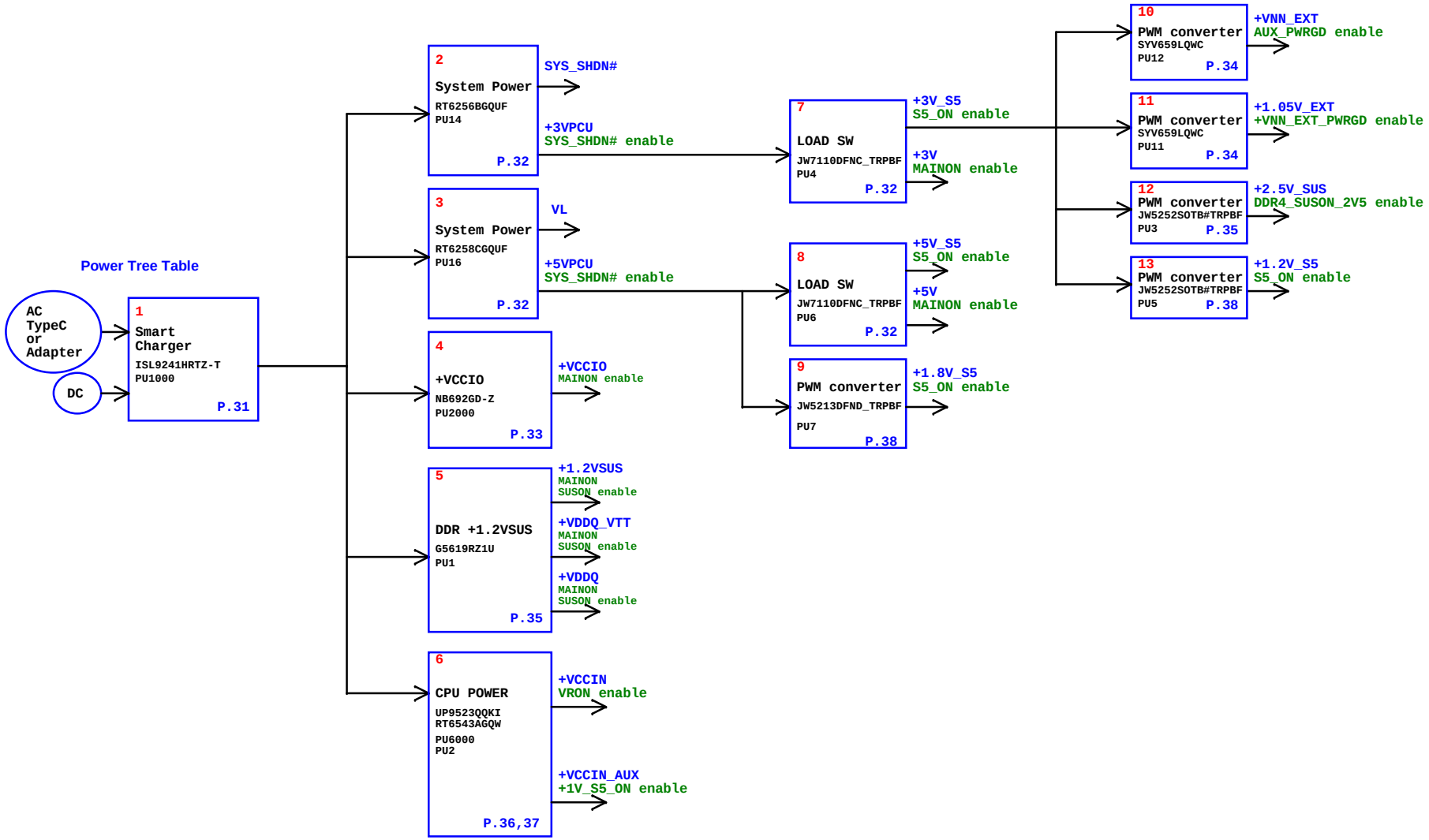




Quanta Computer Inc.
PROJECT : Z8Y

Size	Document Number	Rev
	+1.8V_S5 & +1.2V_S5 & THM	1A
Date: Monday, January 04, 2021	Sheet 38 of 39	

Power Tree Table



Quanta Computer Inc.
PROJECT : ZBK

Size	Document Number	Rev
	POWER TREE TABLE	1A

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