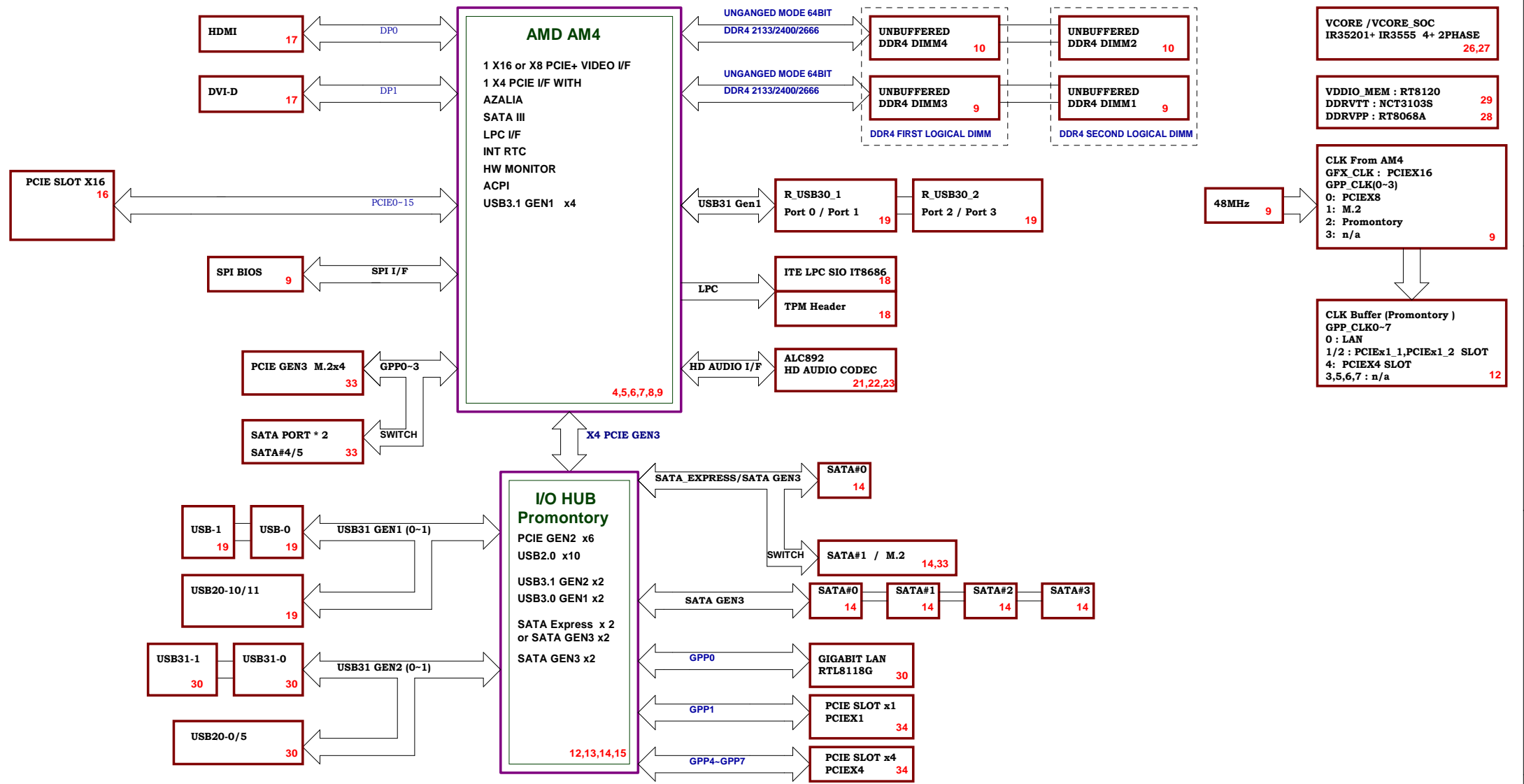
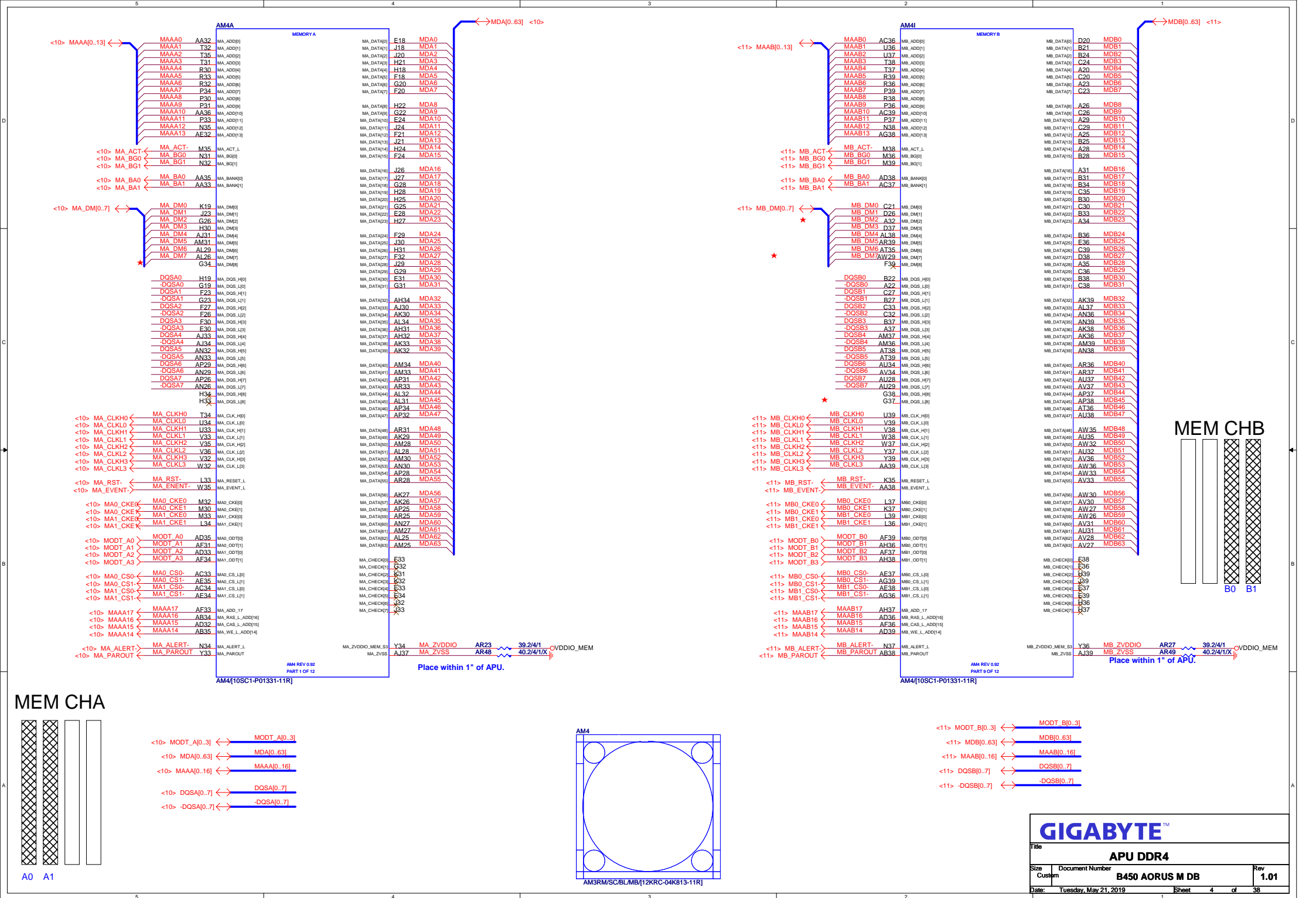


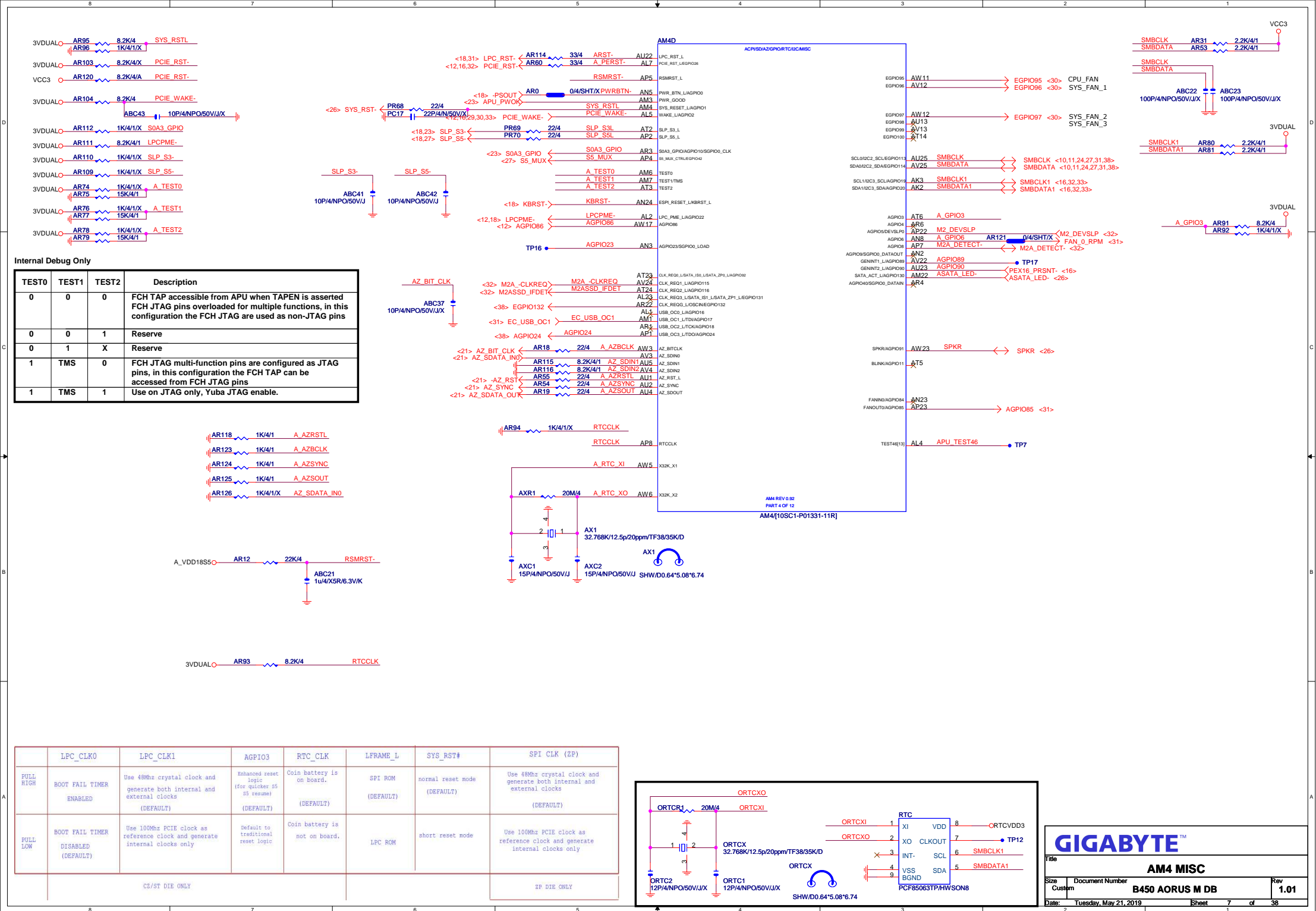
B450 AORUS M DB

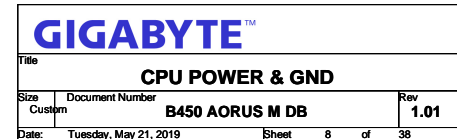
PAGE	TITLE	Revision : 1.01
01	COVER SHEET	
02	BOM & PCB MODIFY HISTORY	
03	BLOCK DIAGRAM	
04	CPU DDR4 MEMORY	
05	CPU CONTROL	
06	CPU GFX, GPP, SB, GND	
07	CPU ACPI/GPIO/USB/AUDIO	
08	CPU POWER & GND	
09	CPU CLK/SPI/USB	
10	DDR4 CHANNEL A	
11	DDR4 CHANNEL B	
12	PM CLK/GPIO/FAN	
13	PM USB	
14	PM UMI/GPP/SATA	
15	PM POWER & GND	
16	PCI EXPRESS x16	
17	HDMI , DVI	
18	IT8686CX , TPM	
19	F_USB30 , R_USB30 , F_USB20	
20	A_VDD1V8 / A_VDDPS5	
21	ALC892 CODEC	
22	AUDIO JACK	
23	AUDIO LED	
24	POWER SEQUENCE , A_VDDP	
25	PWM SL95712	

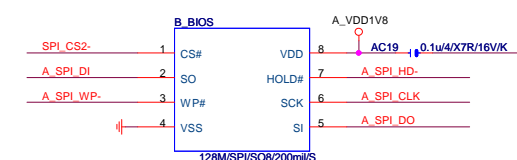
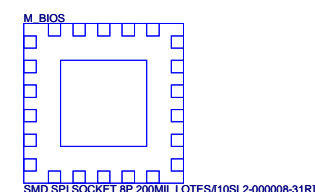
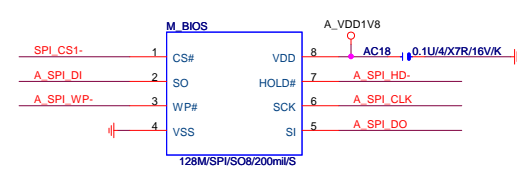
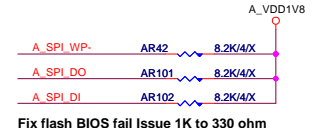
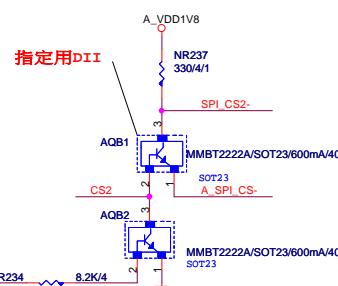
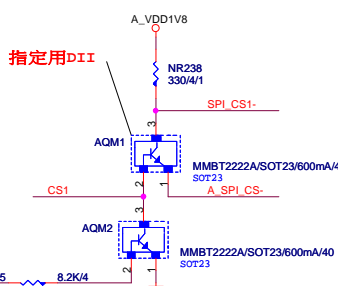
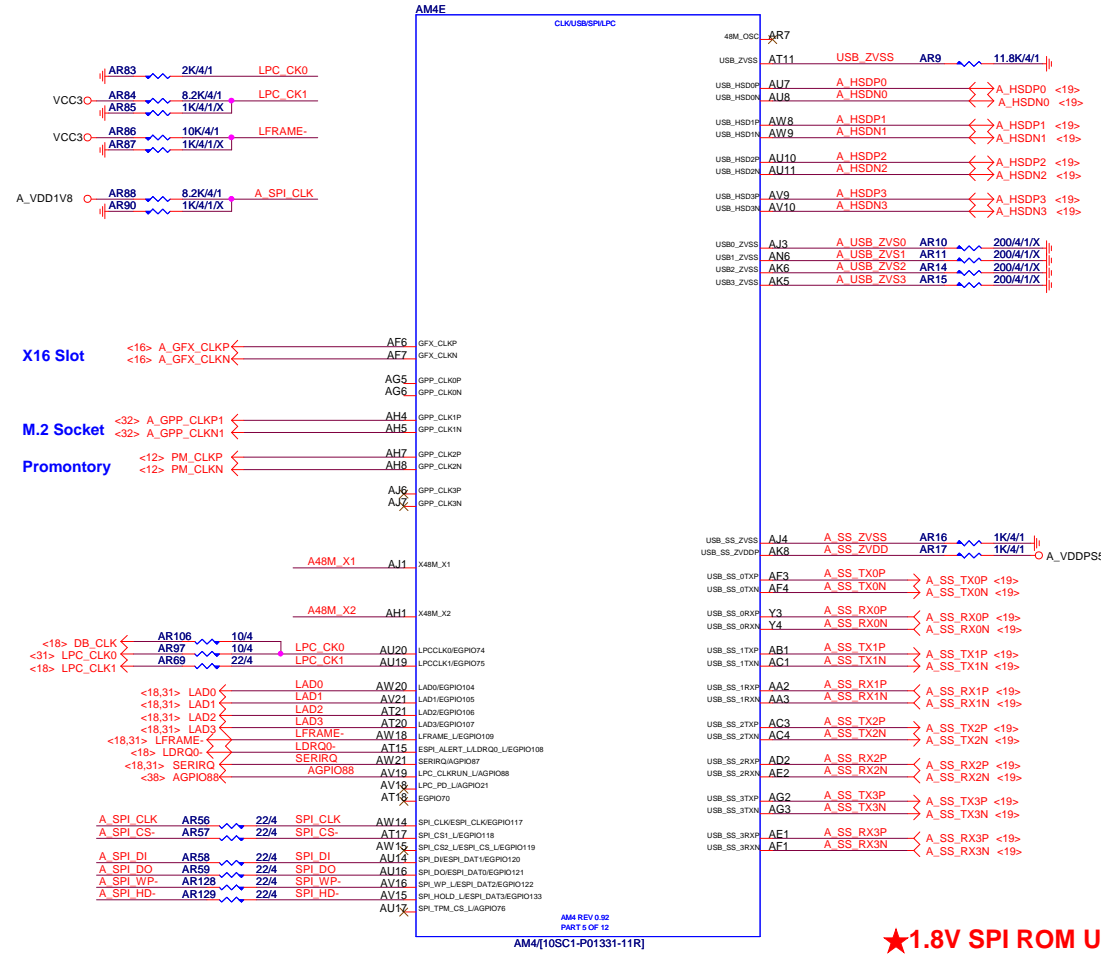
[illegible]











GIGABYTE™

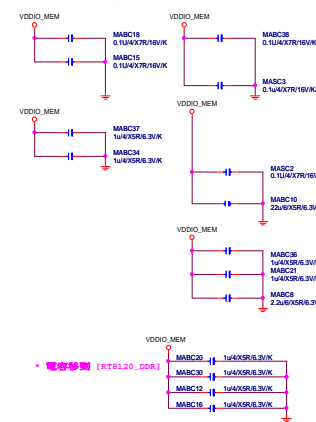
Title**DDR4 CHANNEL A**

Size**Custom**Document Number**B450 AORUS M DB**Rev**1.01**

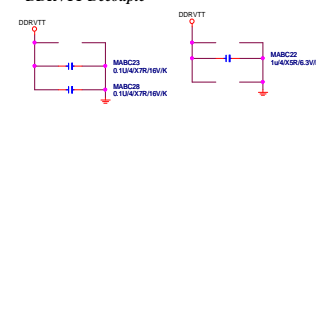
Date**Tuesday, May 21, 2019**Sheet**9** of **38**



DDR12V Decouple

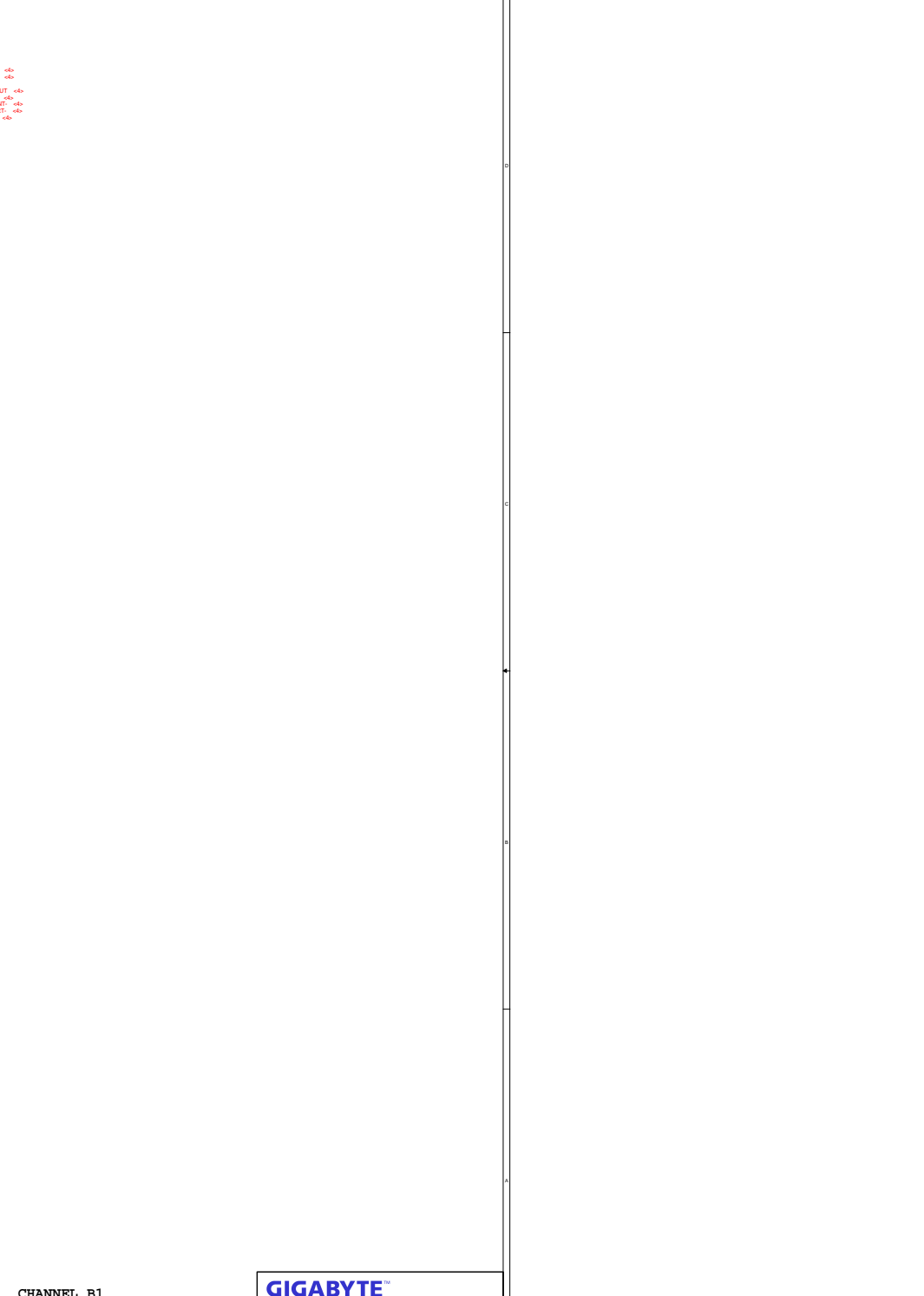


DDRVRTT Decouple

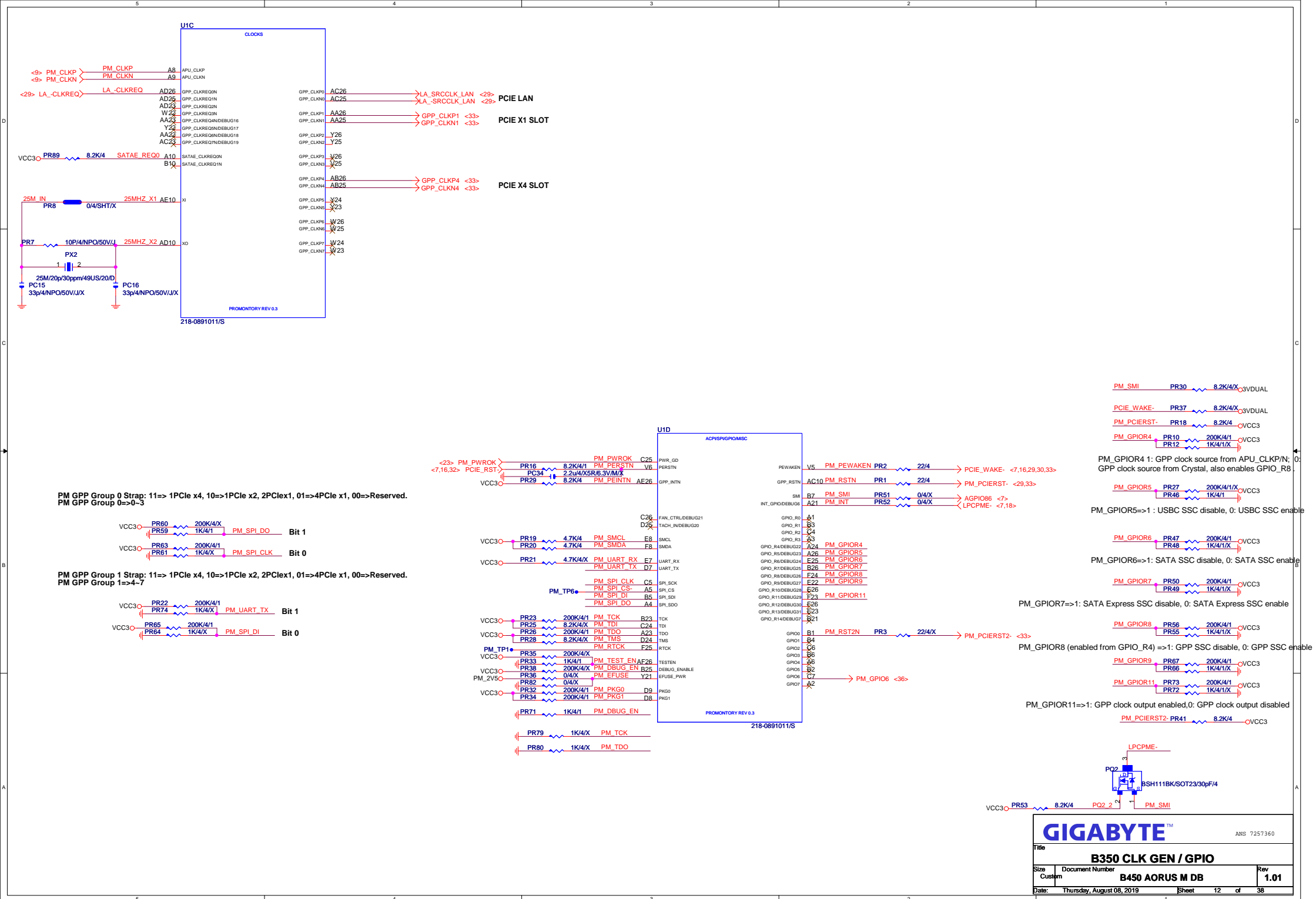


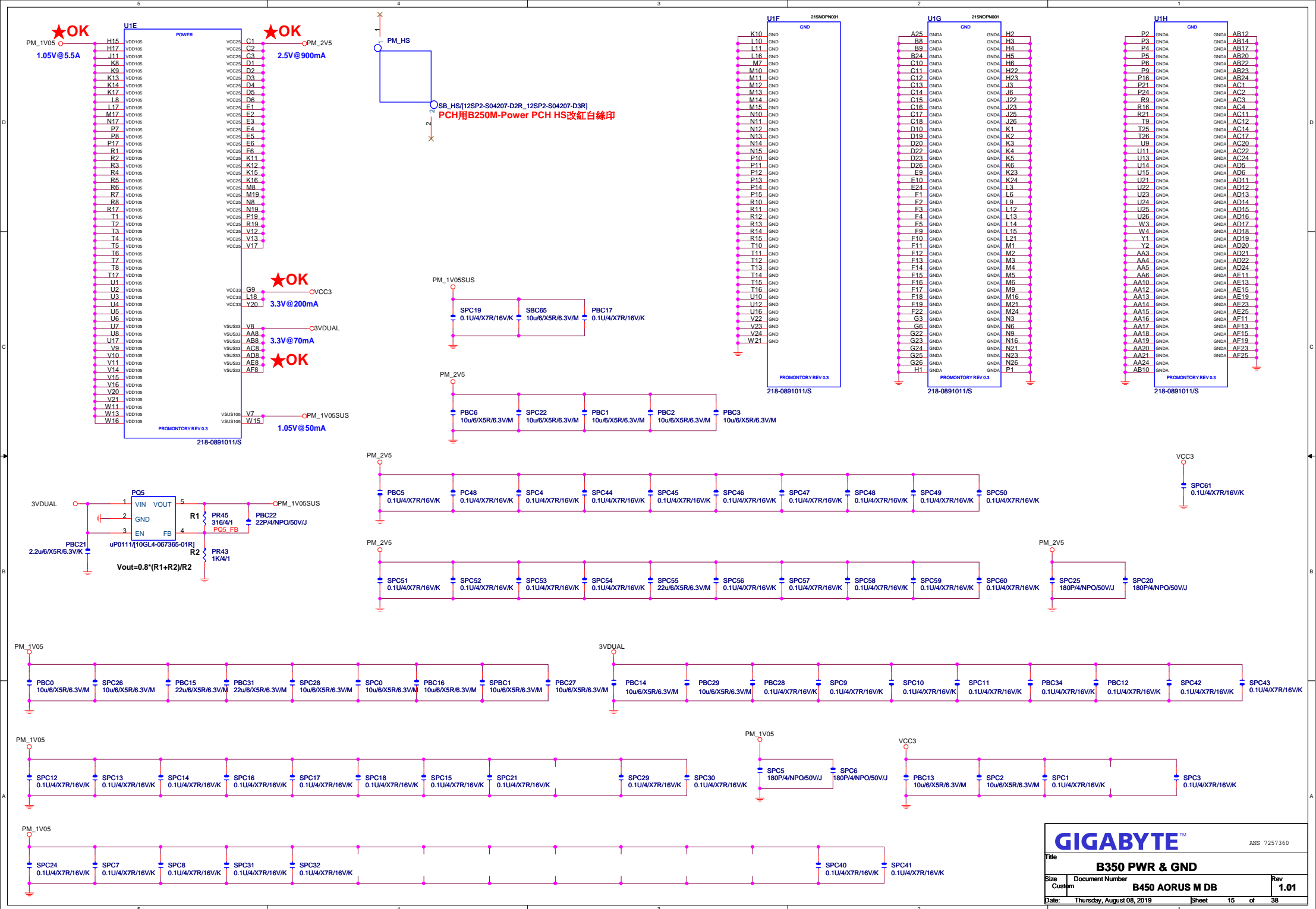


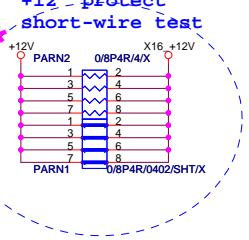
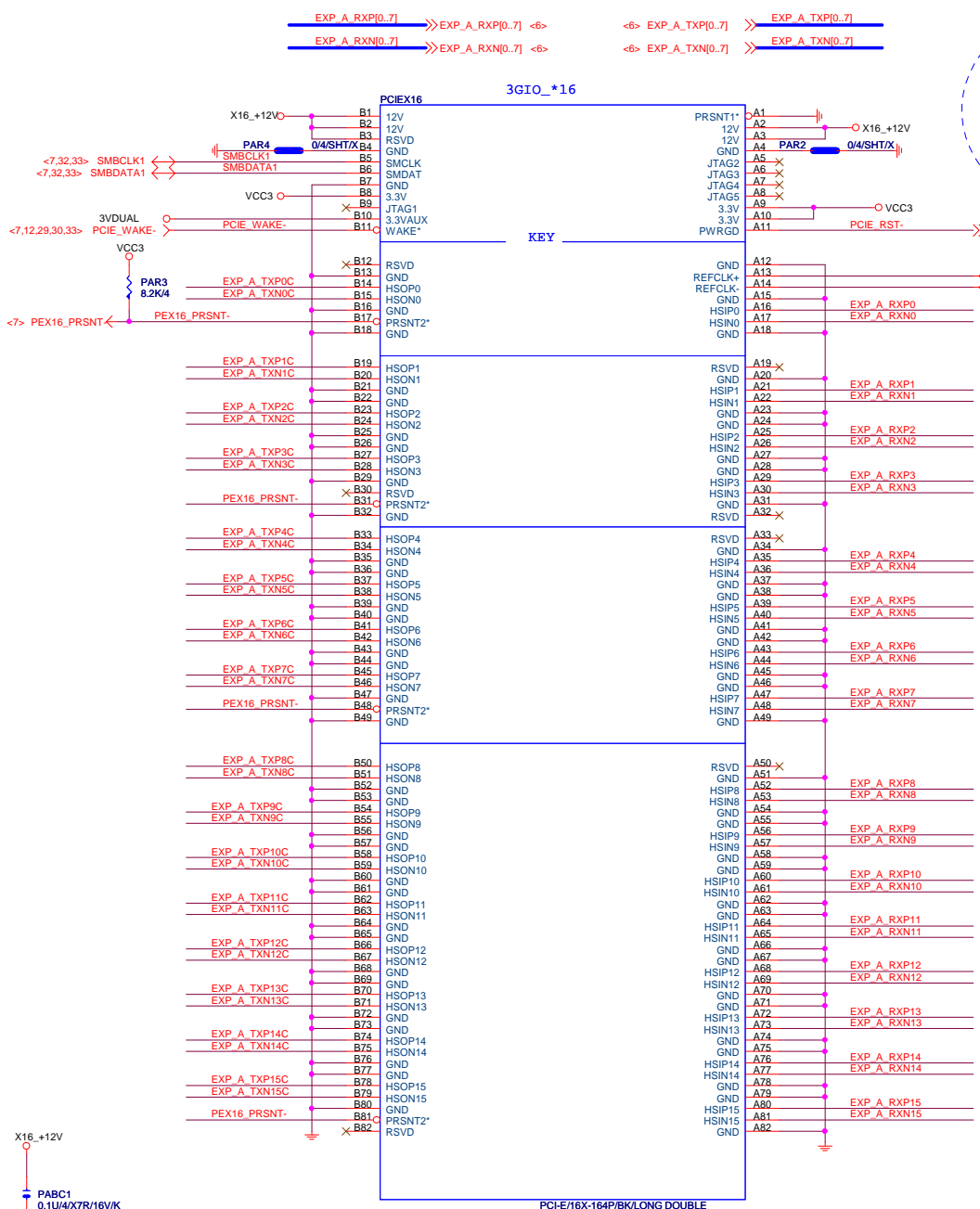
CHANNEL B0
SA2:1=001



CHANNEL B1
SA2:3=011

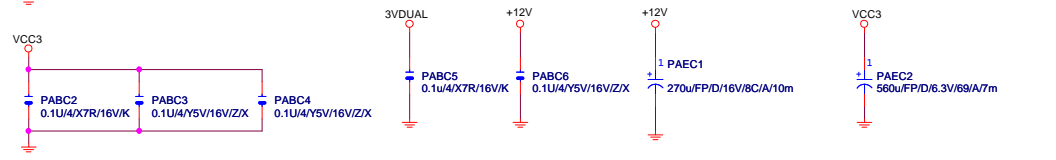






EXP A TXP0	PAC4	0.22u/4X5R6.3V/K	EXP A TXP0C
EXP A TXN0	PAC5	0.22u/4X5R6.3V/K	EXP A TXN0C
EXP A TXP1	PAC6	0.22u/4X5R6.3V/K	EXP A TXP1C
EXP A TXN1	PAC7	0.22u/4X5R6.3V/K	EXP A TXN1C
EXP A TXP2	PAC8	0.22u/4X5R6.3V/K	EXP A TXP2C
EXP A TXN2	PAC9	0.22u/4X5R6.3V/K	EXP A TXN2C
EXP A TXP3	PAC10	0.22u/4X5R6.3V/K	EXP A TXP3C
EXP A TXN3	PAC11	0.22u/4X5R6.3V/K	EXP A TXN3C
EXP A TXP4	PAC12	0.22u/4X5R6.3V/K	EXP A TXP4C
EXP A TXN4	PAC13	0.22u/4X5R6.3V/K	EXP A TXN4C
EXP A TXP5	PAC14	0.22u/4X5R6.3V/K	EXP A TXP5C
EXP A TXN5	PAC15	0.22u/4X5R6.3V/K	EXP A TXN5C
EXP A TXP6	PAC16	0.22u/4X5R6.3V/K	EXP A TXP6C
EXP A TXN6	PAC17	0.22u/4X5R6.3V/K	EXP A TXN6C
EXP A TXP7	PAC18	0.22u/4X5R6.3V/K	EXP A TXP7C
EXP A TXN7	PAC19	0.22u/4X5R6.3V/K	EXP A TXN7C
EXP A TXP8	PAC20	0.22u/4X5R6.3V/K	EXP A TXP8C
EXP A TXN8	PAC21	0.22u/4X5R6.3V/K	EXP A TXN8C
EXP A TXP9	PAC22	0.22u/4X5R6.3V/K	EXP A TXP9C
EXP A TXN9	PAC23	0.22u/4X5R6.3V/K	EXP A TXN9C
EXP A TXP10	PAC24	0.22u/4X5R6.3V/K	EXP A TXP10C
EXP A TXN10	PAC25	0.22u/4X5R6.3V/K	EXP A TXN10C
EXP A TXP11	PAC26	0.22u/4X5R6.3V/K	EXP A TXP11C
EXP A TXN11	PAC27	0.22u/4X5R6.3V/K	EXP A TXN11C
EXP A TXP12	PAC28	0.22u/4X5R6.3V/K	EXP A TXP12C
EXP A TXN12	PAC29	0.22u/4X5R6.3V/K	EXP A TXN12C
EXP A TXP13	PAC30	0.22u/4X5R6.3V/K	EXP A TXP13C
EXP A TXN13	PAC31	0.22u/4X5R6.3V/K	EXP A TXN13C
EXP A TXP14	PAC32	0.22u/4X5R6.3V/K	EXP A TXP14C
EXP A TXN14	PAC33	0.22u/4X5R6.3V/K	EXP A TXN14C
EXP A TXP15	PAC34	0.22u/4X5R6.3V/K	EXP A TXP15C
EXP A TXN15	PAC35	0.22u/4X5R6.3V/K	EXP A TXN15C

EXP A RXP[0.15]	>>>EXP_A_RXP[0.15] <-6>
EXP A RXN[0.15]	>>>EXP_A_RXN[0.15] <-6>
EXP A TXP[0.15]	>>>EXP_A_TXP[0.15] <-6>
EXP A TXN[0.15]	>>>EXP_A_TXN[0.15] <-6>



GIGABYTE™

Size

Custom

Date:

Tuesday, May 21, 2019

Title

PCIEx16

Document Number

B450 AORUS M DB

Rev

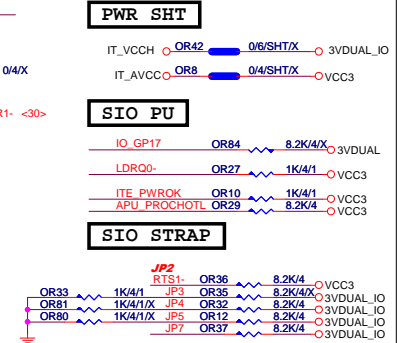
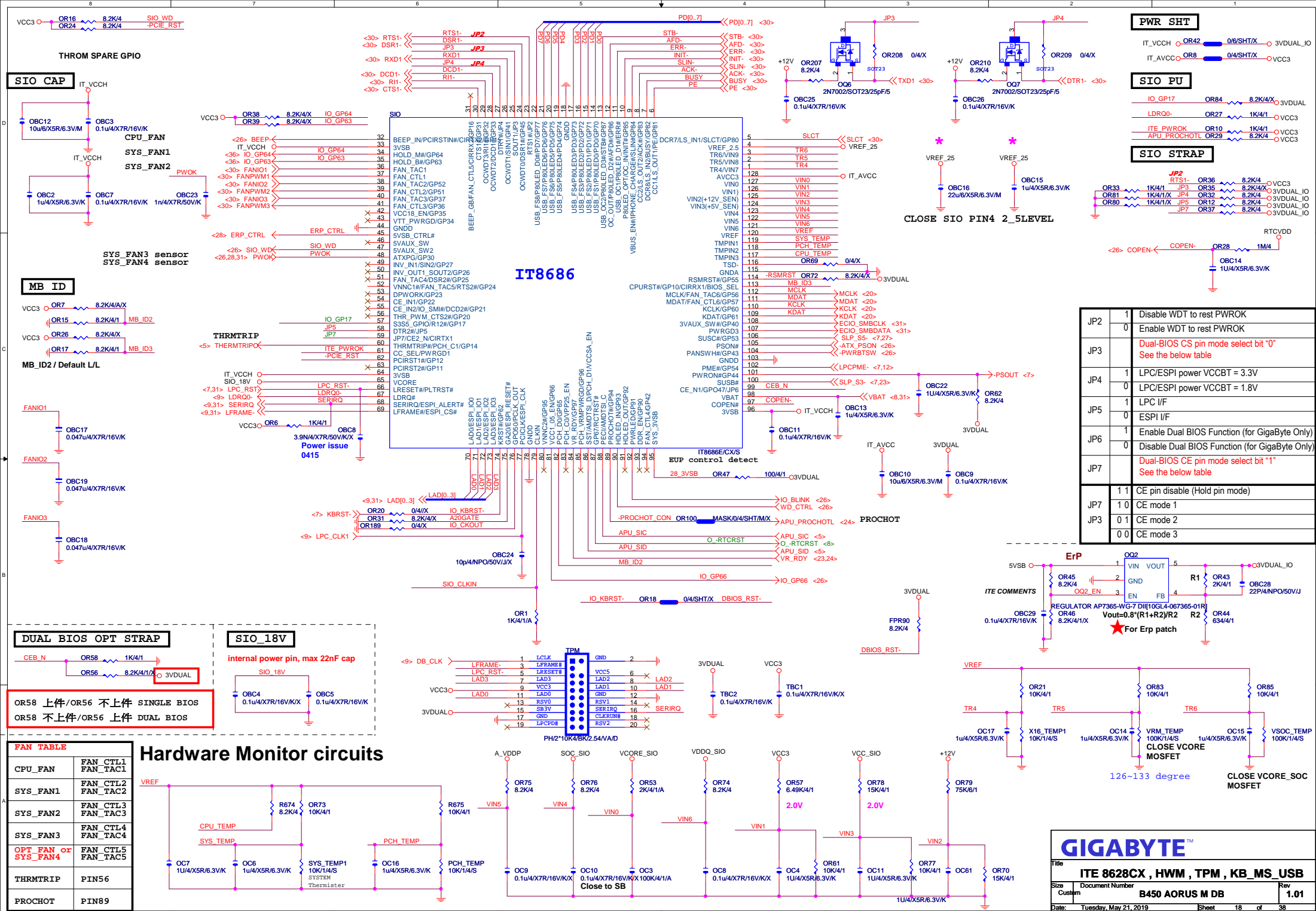
1.01

Sheet

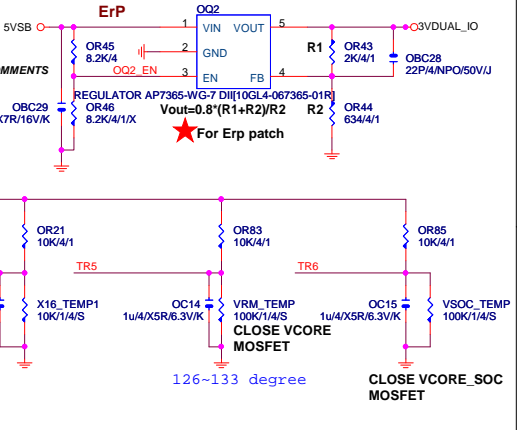
16

of

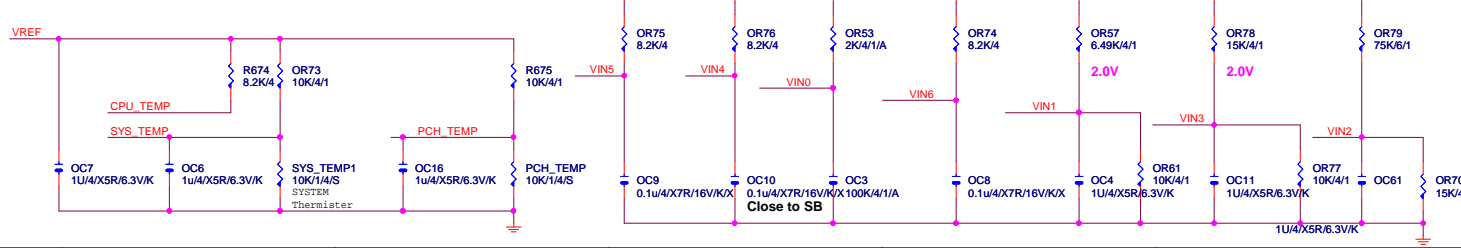
38



JP2	1	Disable WDT to rest PWROK
JP2	0	Enable WDT to rest PWROK
JP3		Dual-BIOS CS pin mode select bit "0" See the below table
JP4	1	LPC/ESPI power VCCBT = 3.3V
JP4	0	LPC/ESPI power VCCBT = 1.8V
JP5	1	LPC I/F
JP5	0	ESPI I/F
JP6	1	Enable Dual BIOS Function (for GigaByte Only)
JP6	0	Disable Dual BIOS Function (for GigaByte Only)
JP7		Dual-BIOS CE pin mode select bit "1" See the below table
JP7	1 1	CE pin disable (Hold pin mode)
JP7	1 0	CE mode 1
JP3	0 1	CE mode 2
JP3	0 0	CE mode 3



Hardware Monitor circuits



DUAL BIOS OPT STRAP

CEB_N OR58 1K/4/1 3VDUAL
OR56 8.2K/4/1

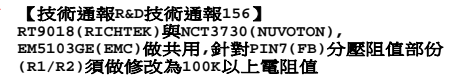
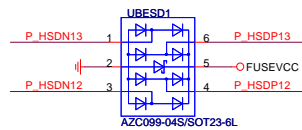
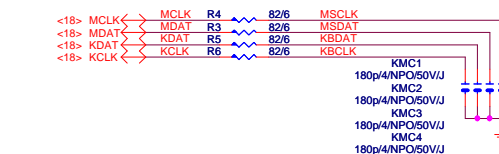
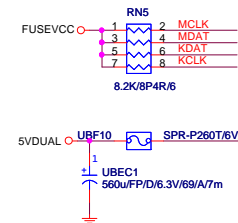
OR58 上件/OR56 不上件 SINGLE BIOS
OR58 不上件/OR56 上件 DUAL BIOS

SIO_18V

internal power pin, max 22nF cap

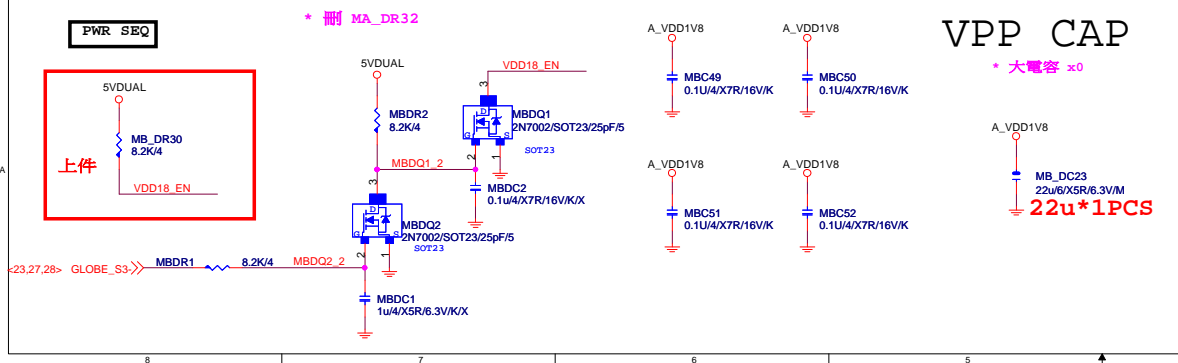
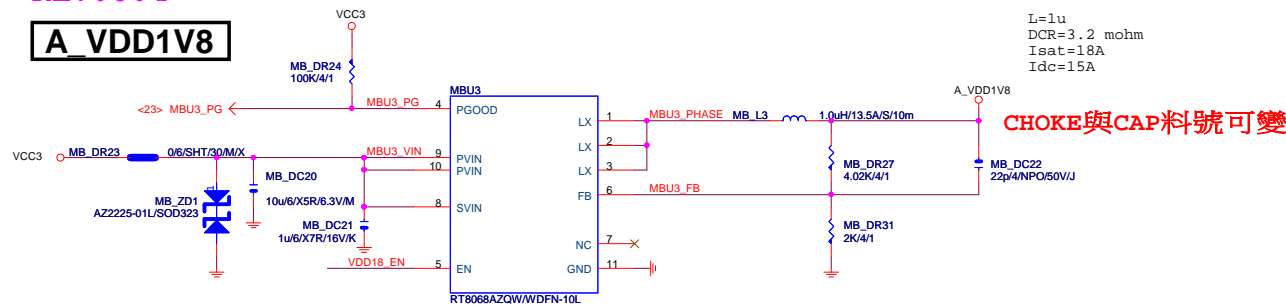
SIO_18V
OBC4 0.1u/4X7R/16V/KX
OBC5 0.1u/4X7R/16V/KX

FAN TABLE	
CPU_FAN	FAN_CTL1 FAN_TAC1
SYS_FAN1	FAN_CTL2 FAN_TAC2
SYS_FAN2	FAN_CTL3 FAN_TAC3
SYS_FAN3	FAN_CTL4 FAN_TAC4
OPT_FAN or SYS_FAN4	FAN_CTL5 FAN_TAC5
THRMTRIP	PIN56
PROCHOT	PIN89

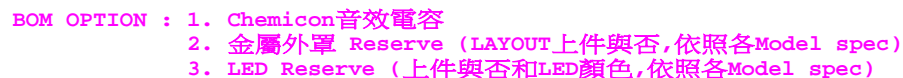


CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V

A_VDD1V8



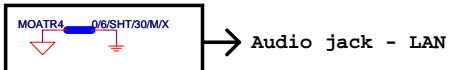
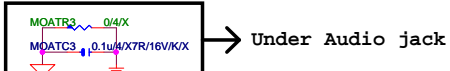
ALC892 六孔 AUDIO JACK



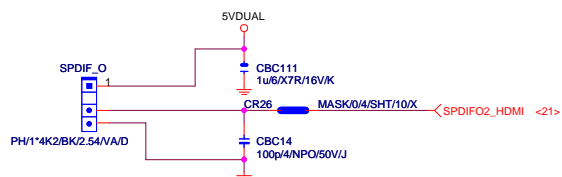
3. Codec下方,第二層必須參考GND



Rev 3.0

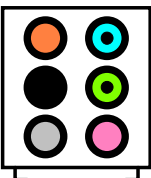


*量産前,0ohm改short pad



For HDMI SPDIF (依SPEC保留或移除)

AZALIA JACK



AZALIA JACK

BLUE

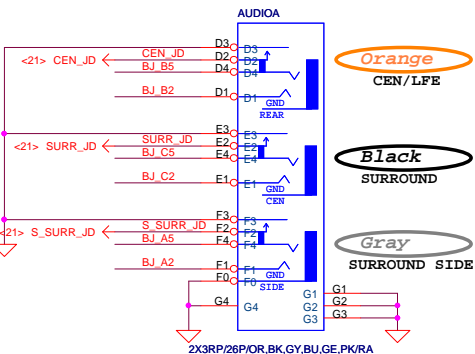
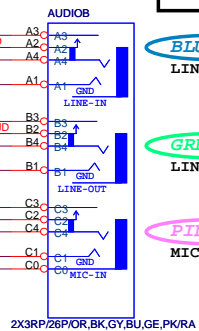
LINE-IN

GREEN

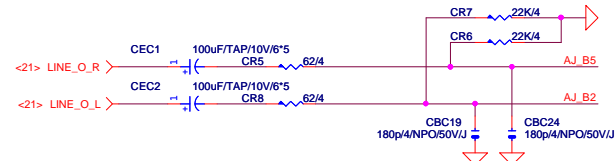
LINE-OUT

PINK

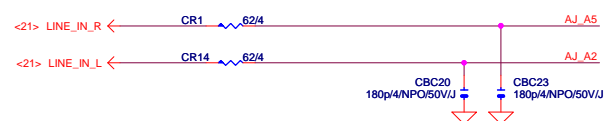
MIC-IN



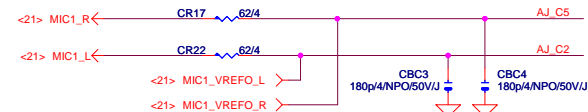
LINE-OUT



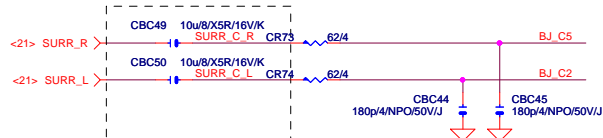
LINE-IN



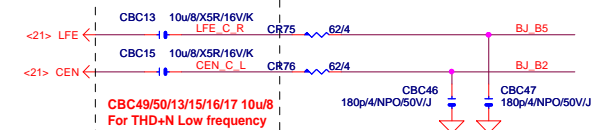
MIC-IN



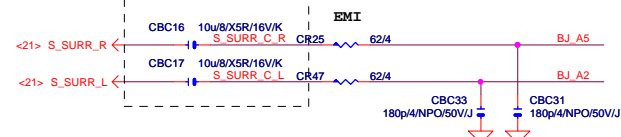
SURROUND



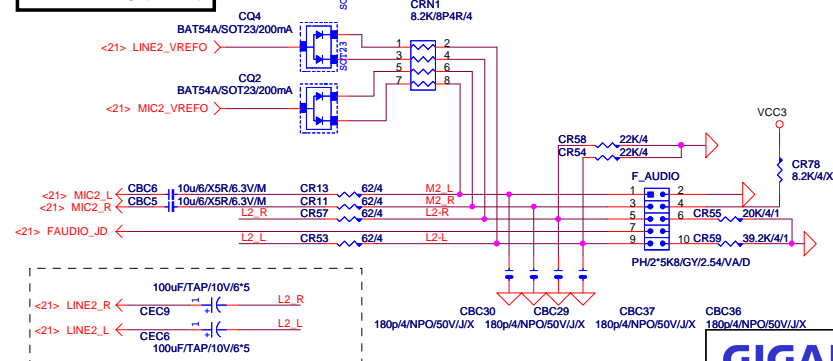
CEN/LFE



SURR BACK

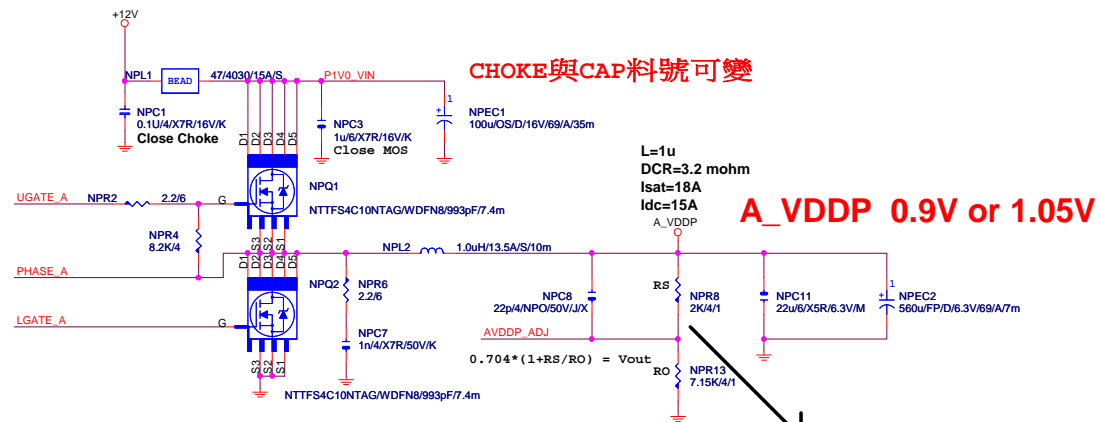
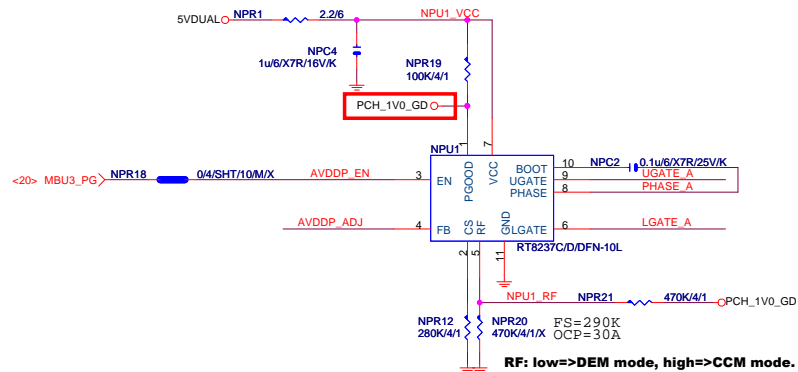


AZALIA FRONT PANEL

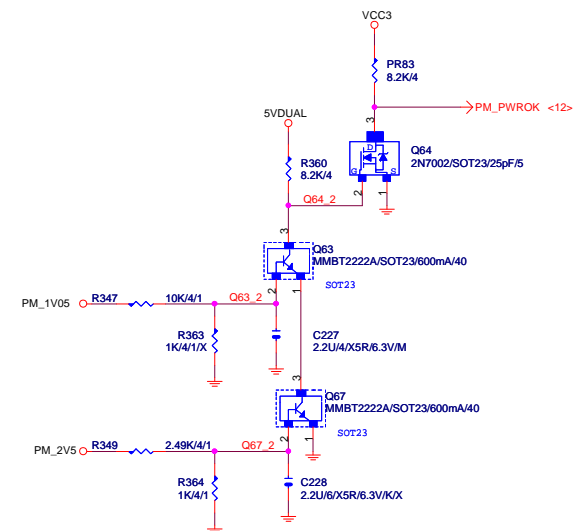
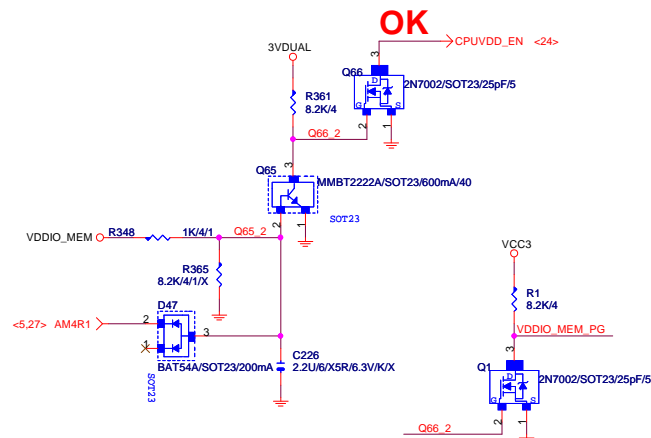
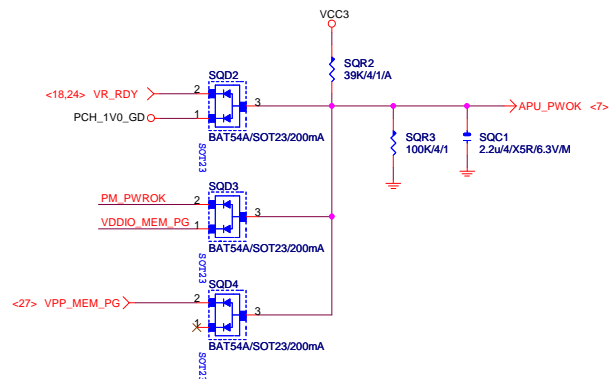
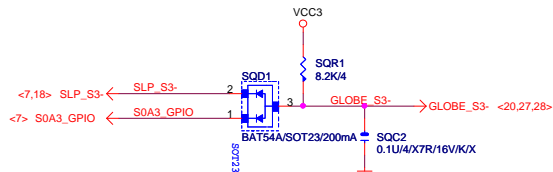


GIGABYTE™

Title		
AUDIO JACK		
Size	Document Number	Rev
Custom	B450 AORUS M DB	1.01
Date:	Tuesday, May 21, 2019	Sheet 22 of 38

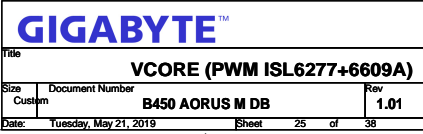


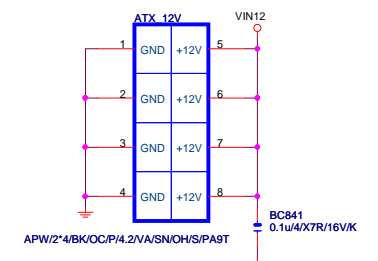
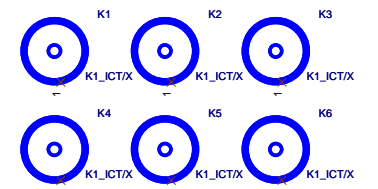
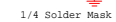
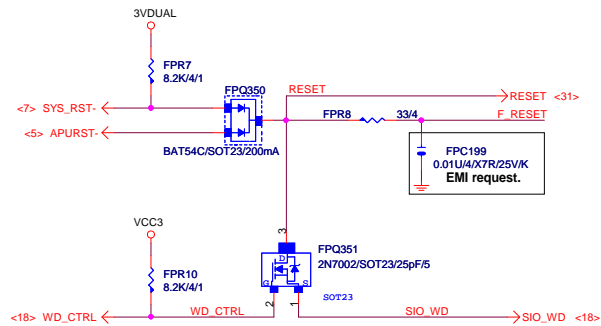
CORETYPE1	CORETYPE0	VPPD_ALW
1	X	0.9V
0	X	1.05V



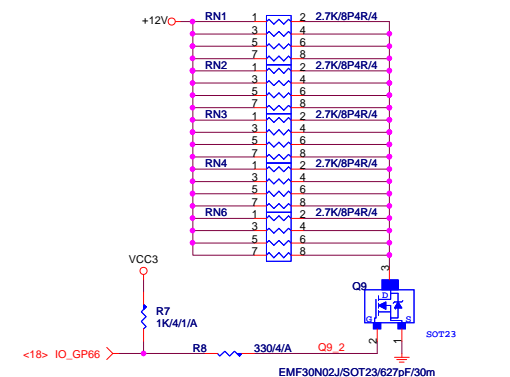
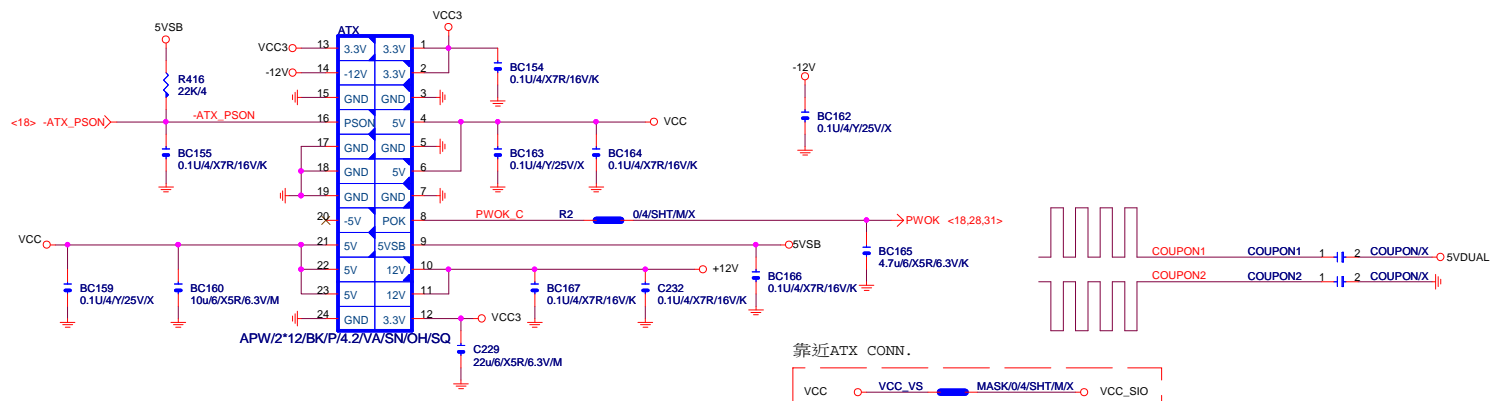
GIGABYTE™

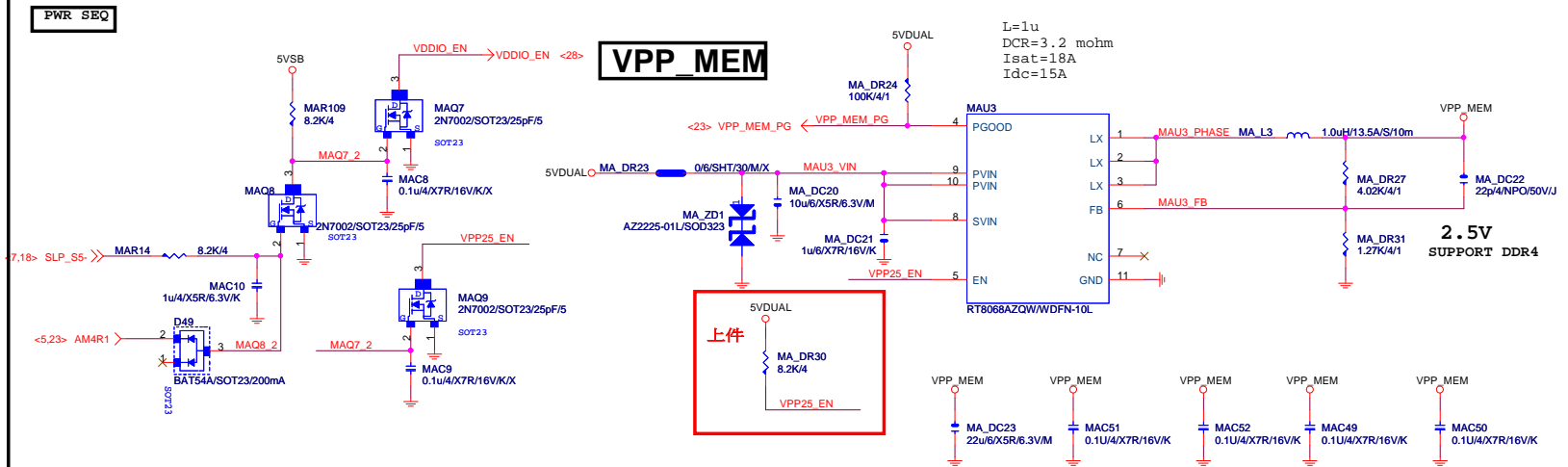
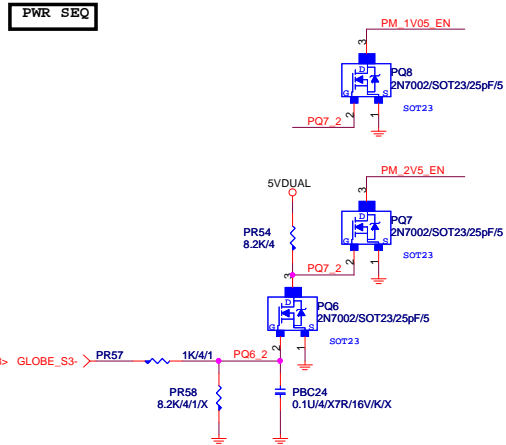
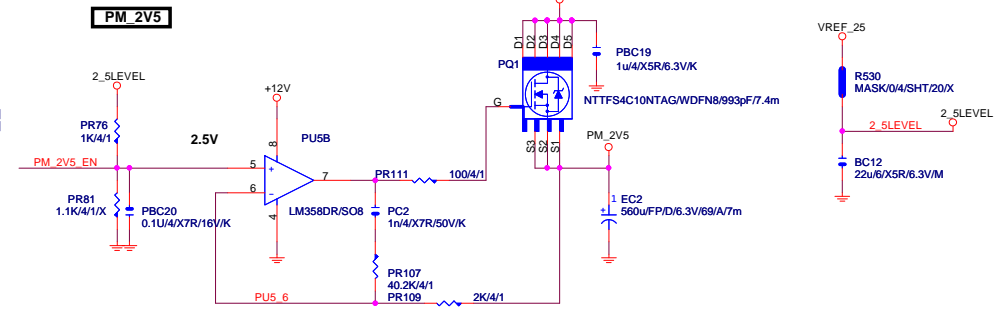
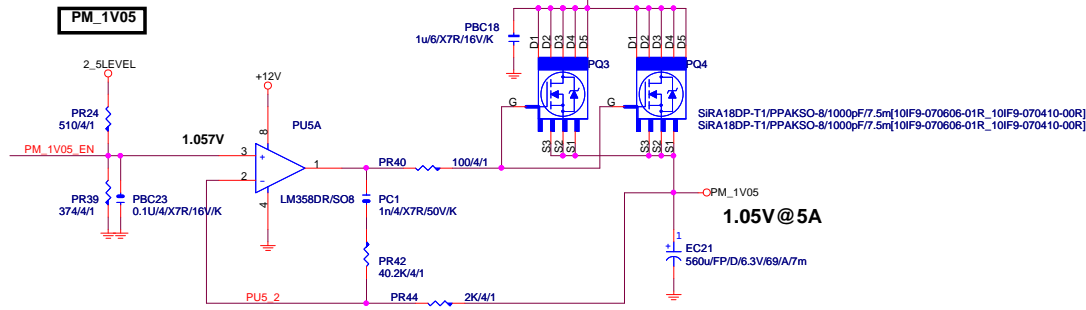
POWER SEQUENCE		
Title	Document Number	Rev
Size	Custom	1.01
Date:	Tuesday, May 21, 2019	Sheet 23 of 38



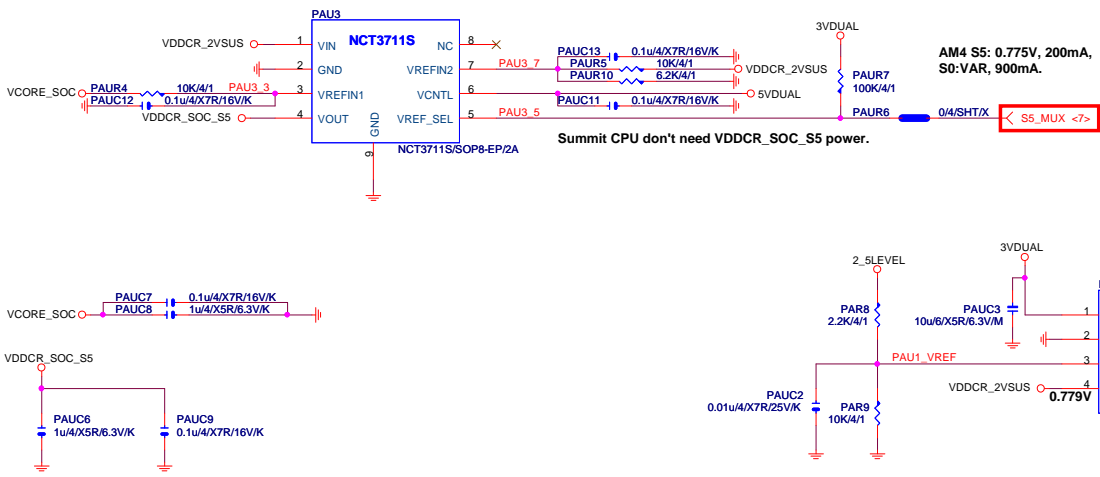


ATX POWER CONNECTOR

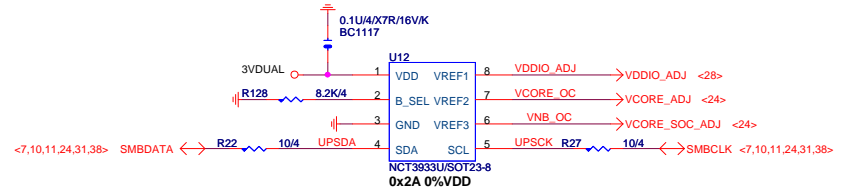




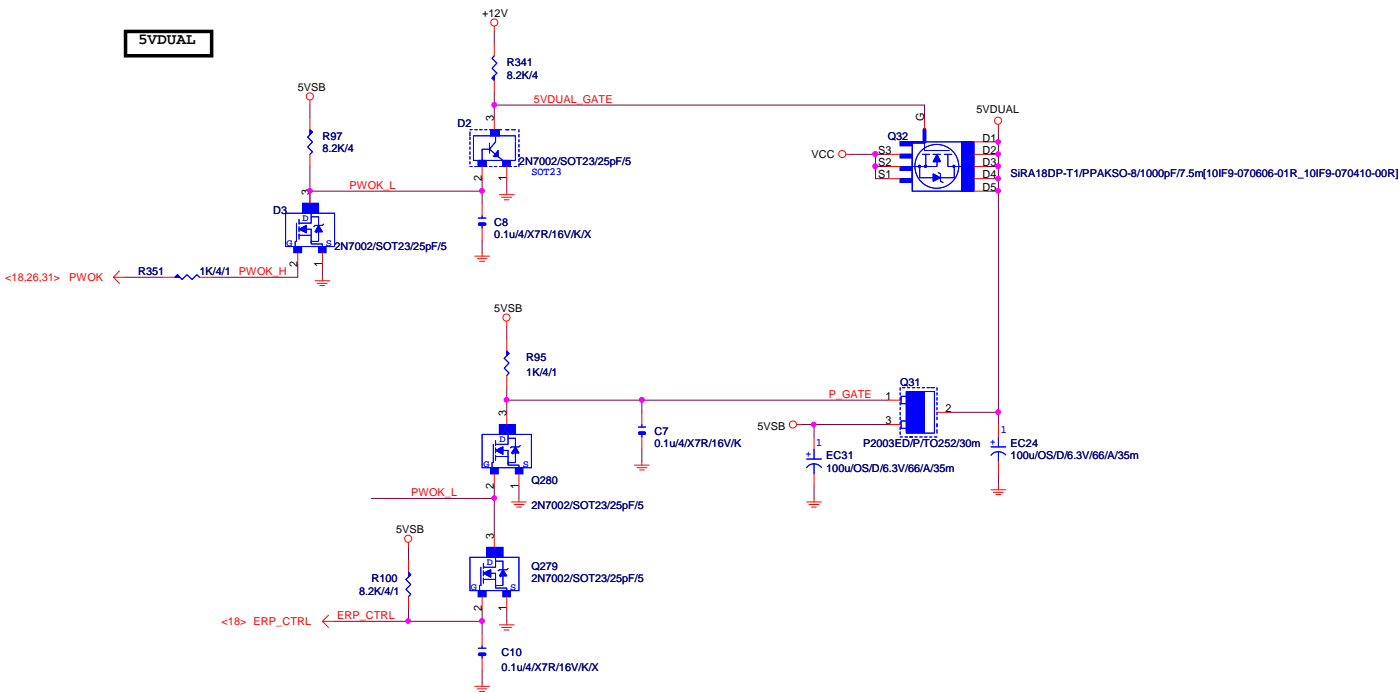
VDDCR SOC S5



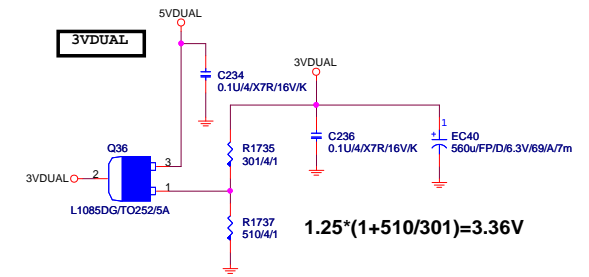
S5_MUX: S0-->High, S5-->Low
H: VDDCR_SOC_S5 will track VCORE_SOC.
L: If VCORE_SOC < 0.775V (OR 0.85V) , VDDCR_SOC_S5=0.775V.
If VCORE_SOC>=0.775V (OR 0.85V) , VDDCR_SOC_S5 will trace VCORE_SOC.



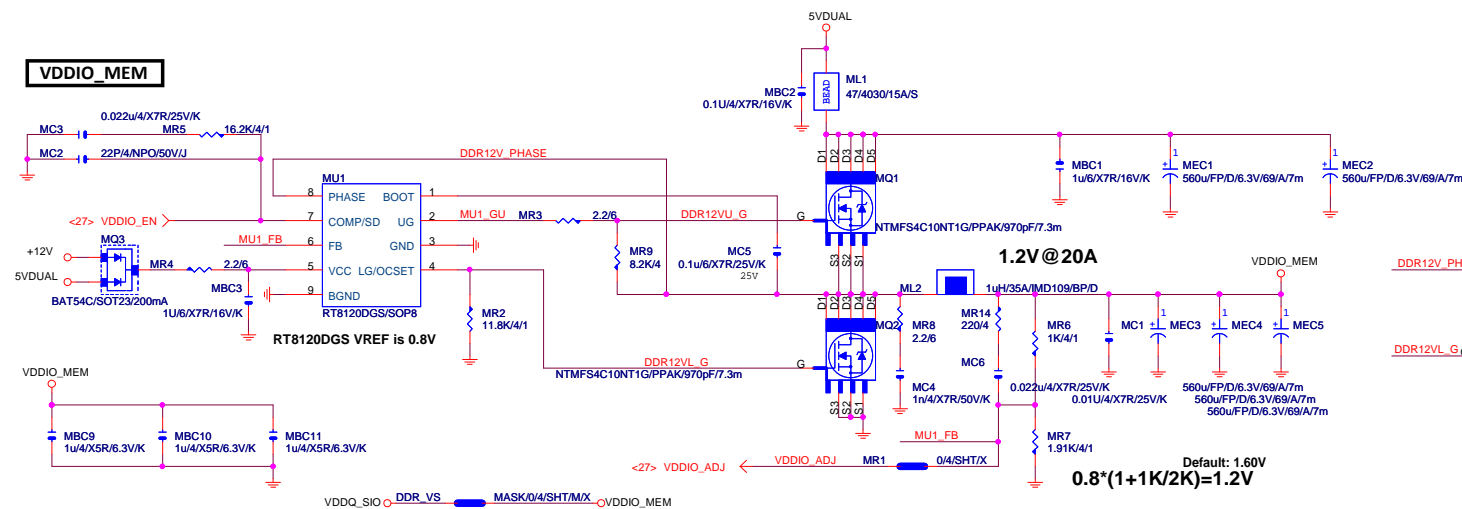
5VDUAL



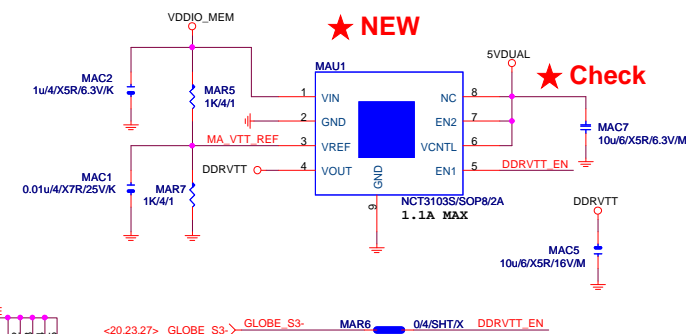
3VDUAL

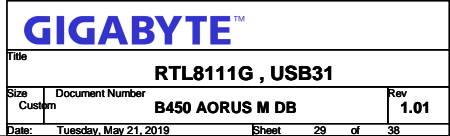


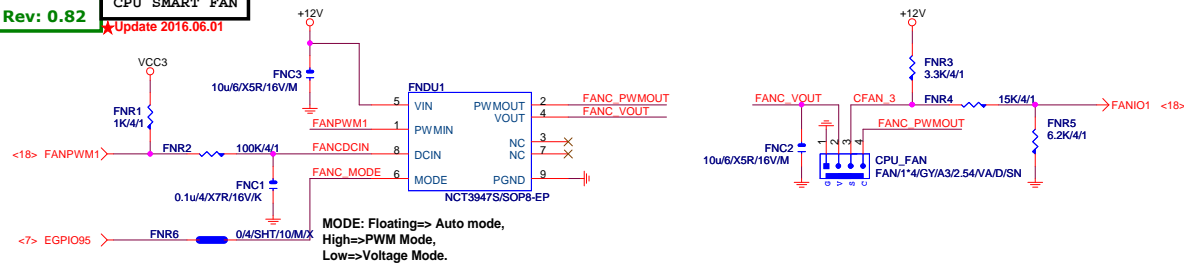
VDDIO_MEM



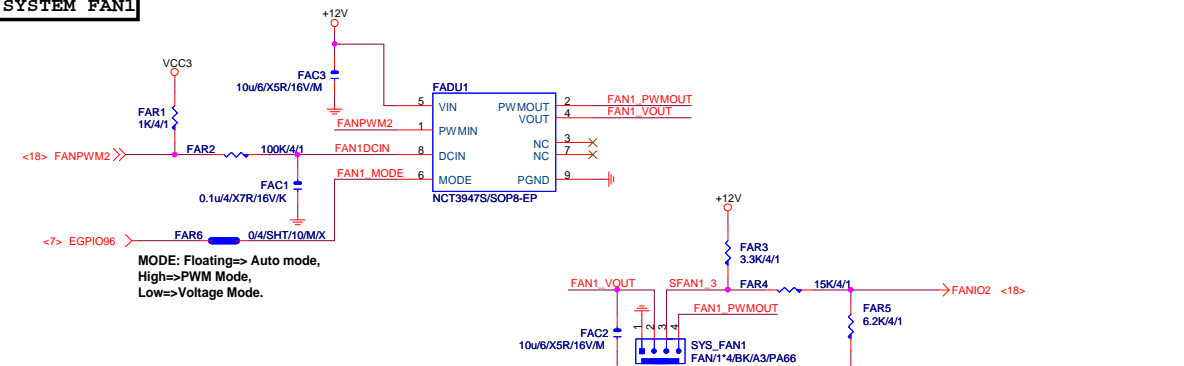
DDRVT



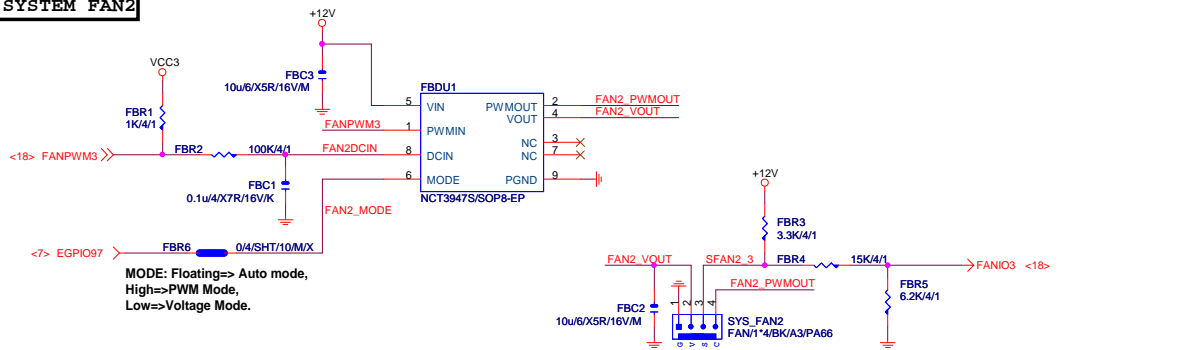




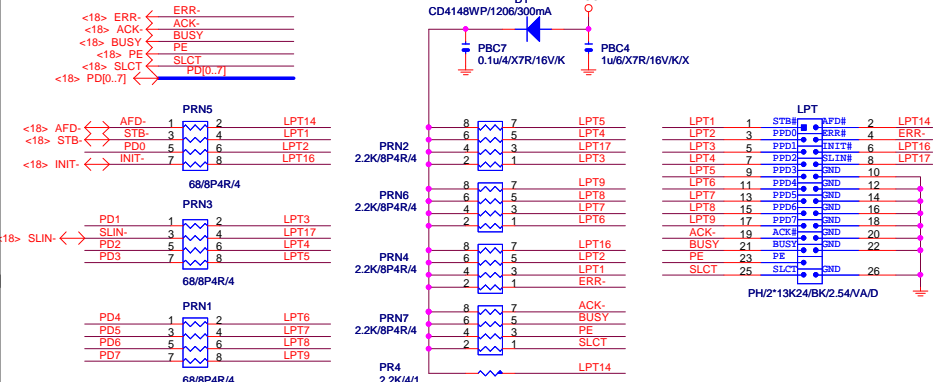
SYSTEM FAN1



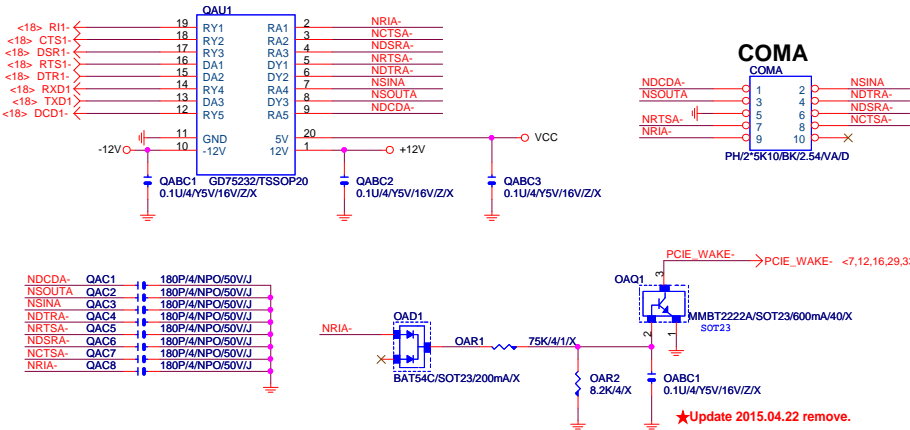
SYSTEM FAN2

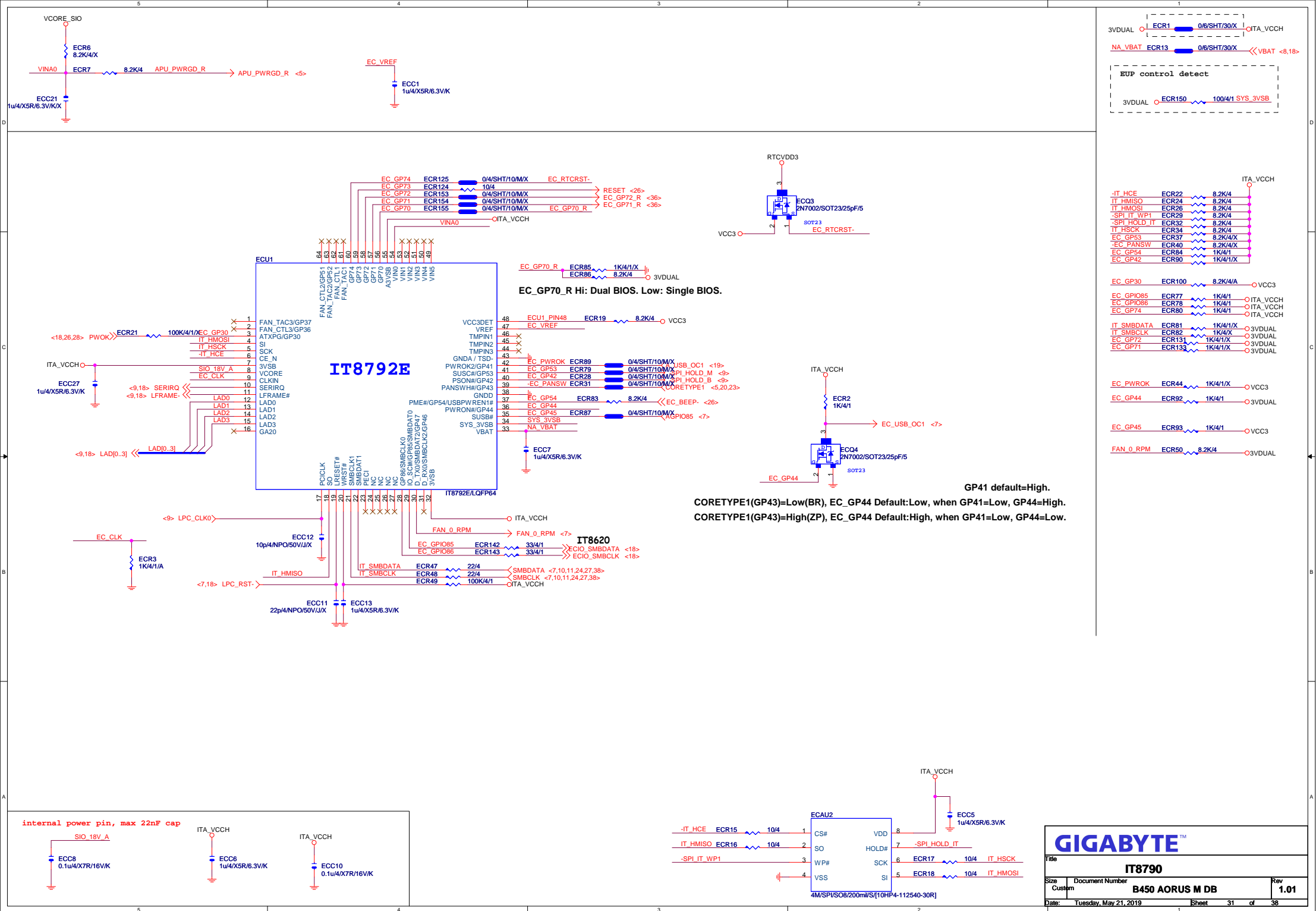


LPT PORT



COM PORT





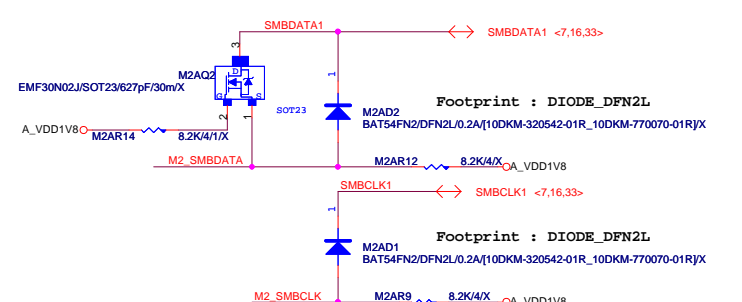
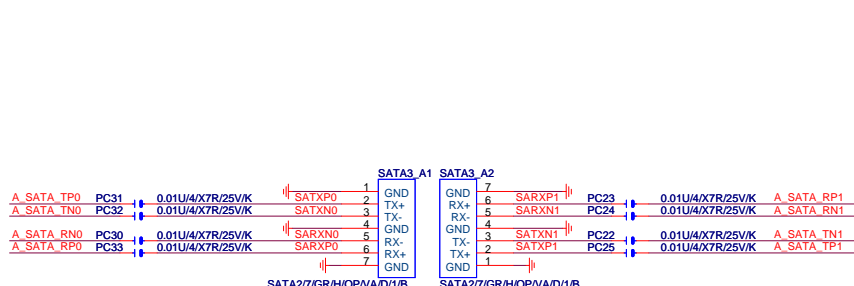
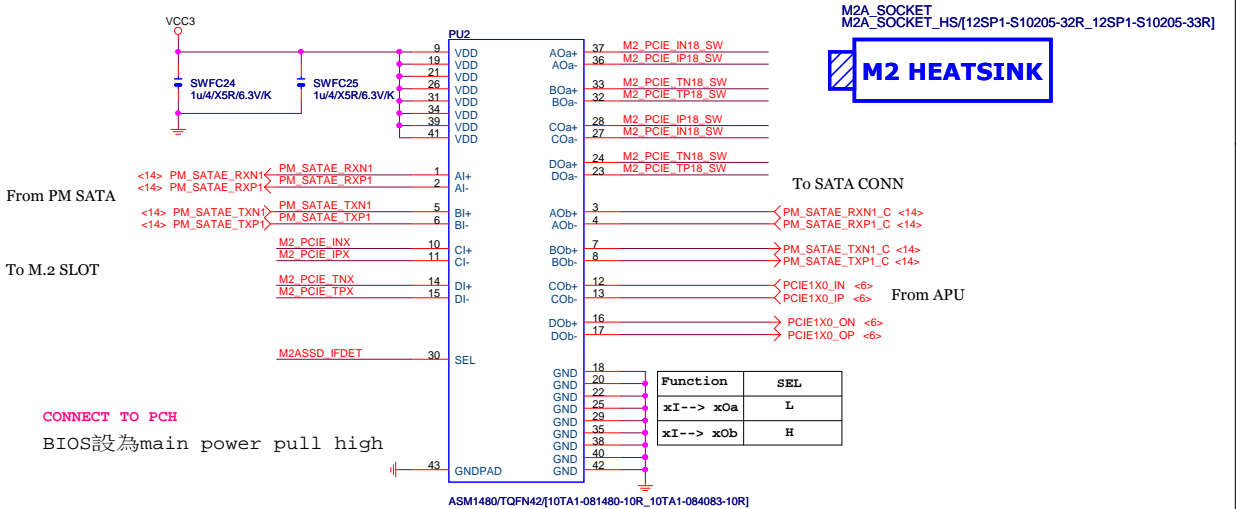
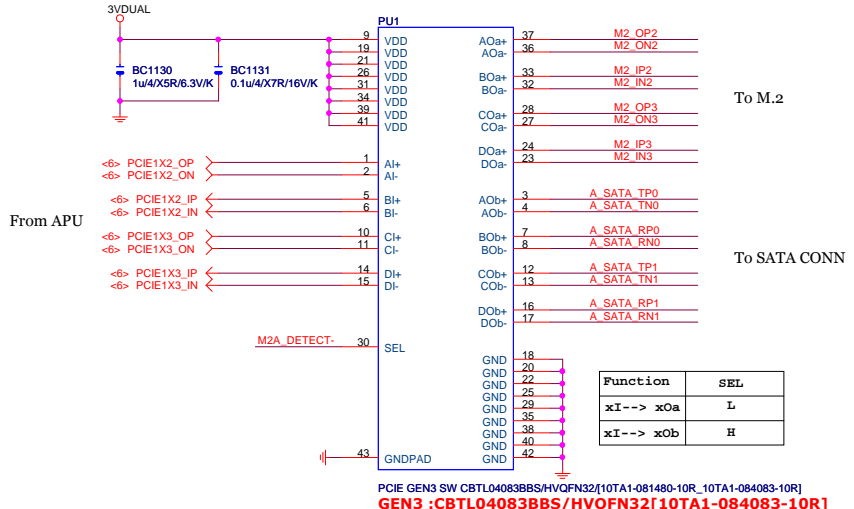
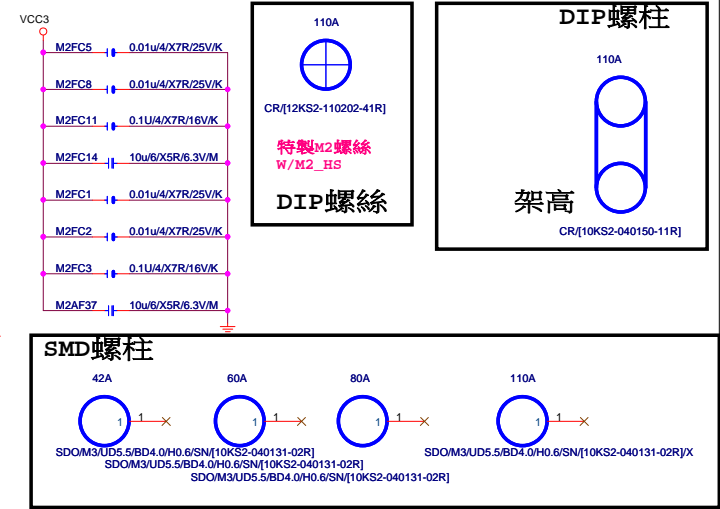
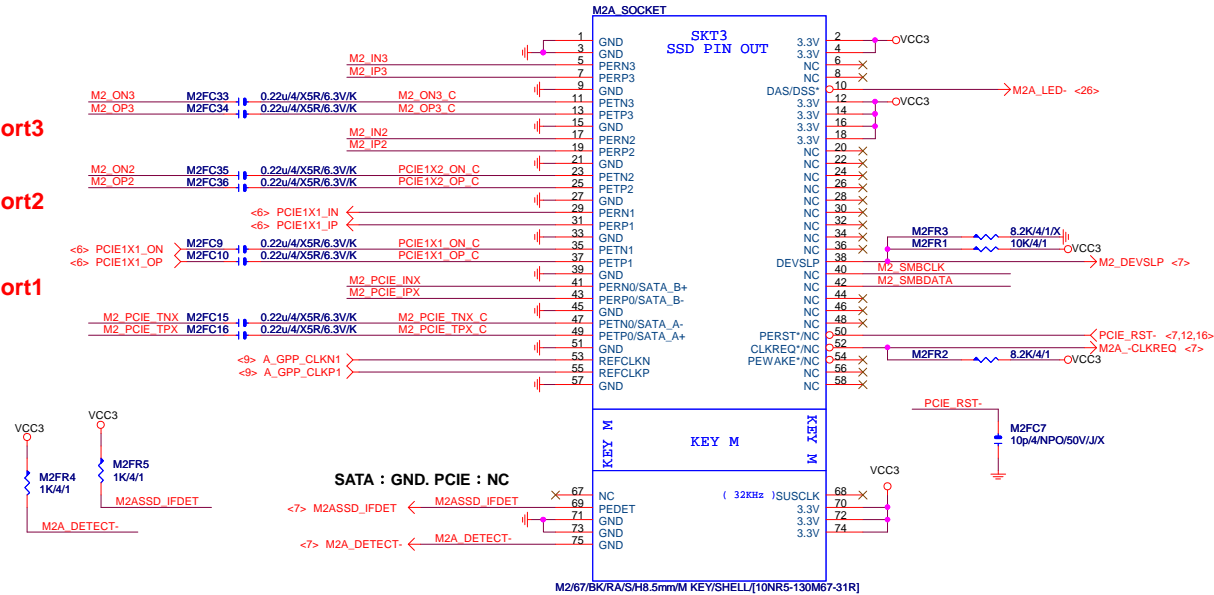
Rev 0.5

M.2 Lane4 from AM4 port3

M.2 Lane4 from AM4 port2

M.2 Lane4 from AM4 port1

by SWITCH Select



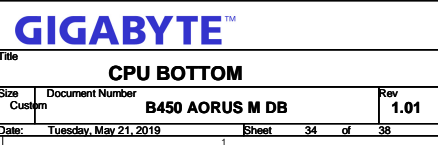
teknisi-indonesia.com

GIGABYTE™

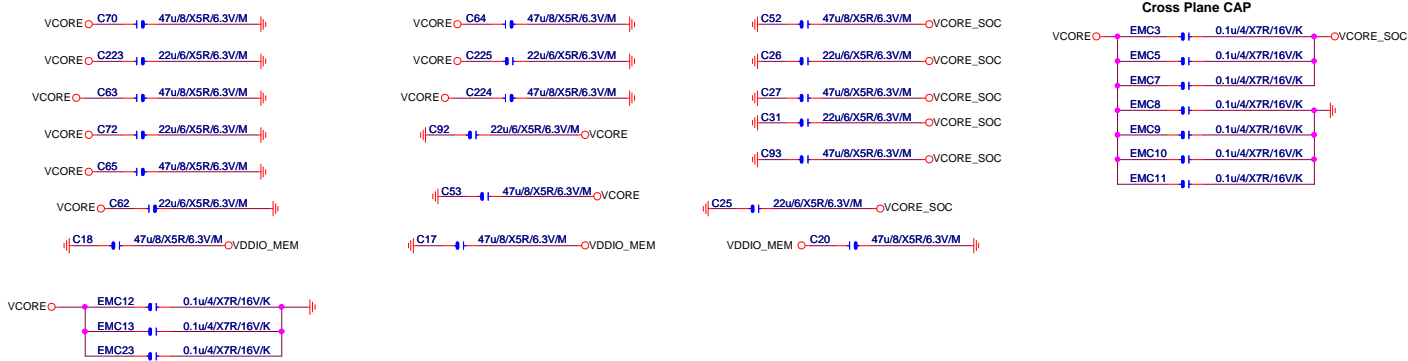
M.2 SWITCH

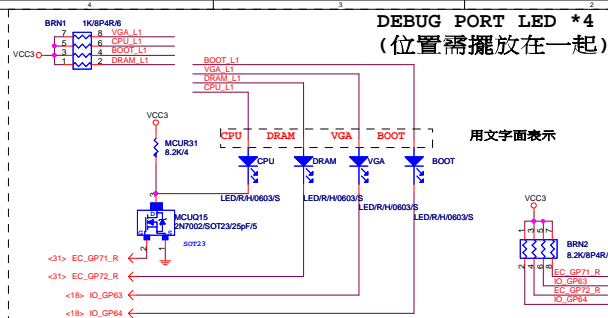
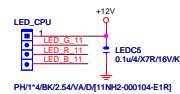
Size CustomDocument Number B450 AORUS M DBRev 1.01

Date: Tuesday, May 21, 2019Sheet 32 of 38



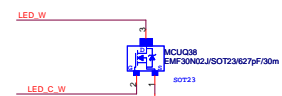
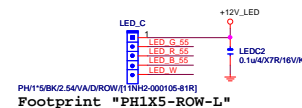
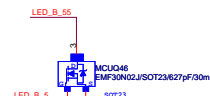
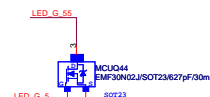
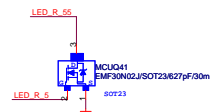
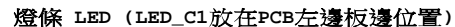
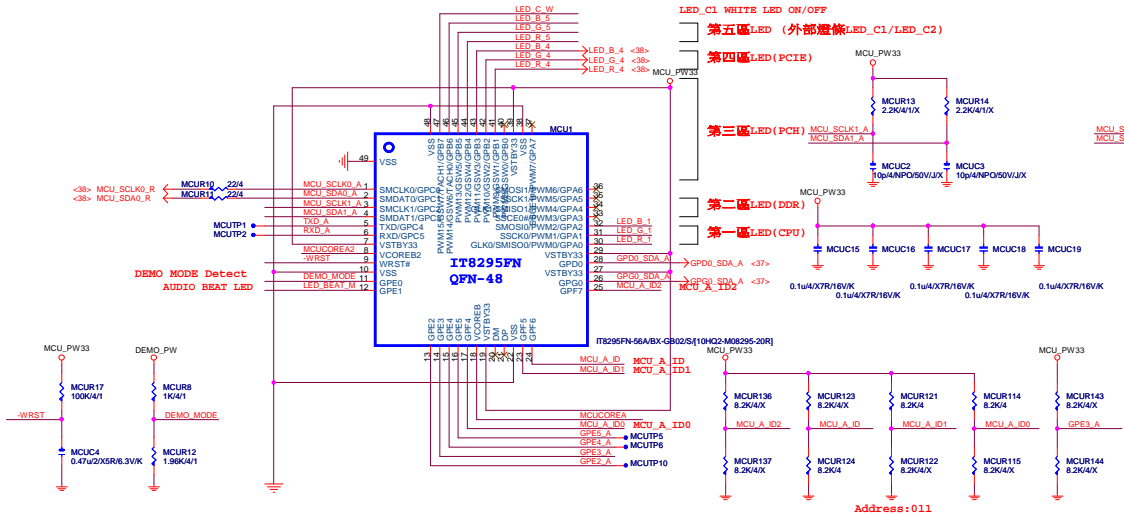
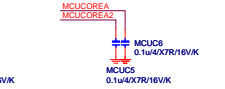
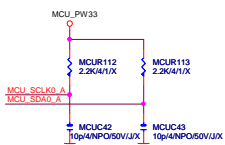
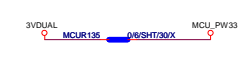
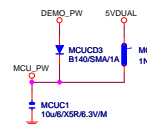
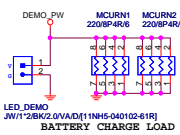
CPU TOP CAVITY



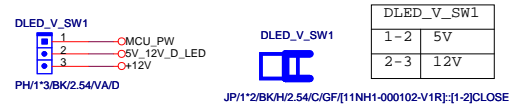


EC_GP71	CPU DEBUG
EC_GP72	DDR DEBUG
IO_GP63	VGA DEBUG
IO_GP64	BOOT DEVICE DEBUG
PM_GPIO6	software beat mode control
N_GPP_A22	
N_GPP_D12	

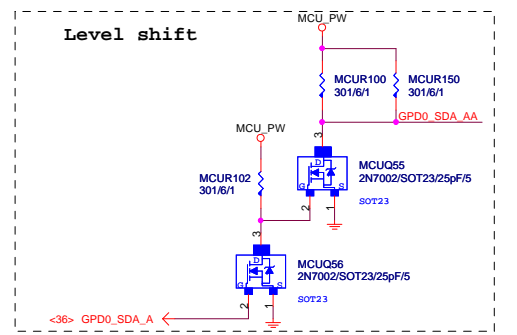
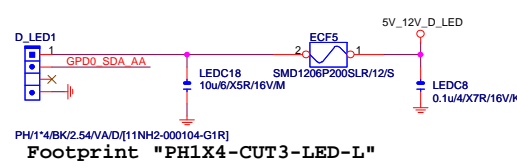
FOR DIMM 側發光 LED*12
(位置在DIMM兩側)

[illegible]

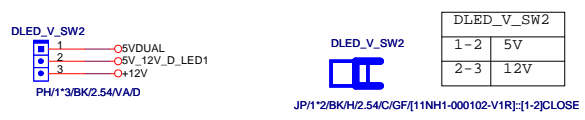
第六區 LED（靠近左上板邊位置）



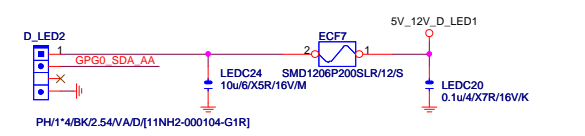
Digital LED Strip1



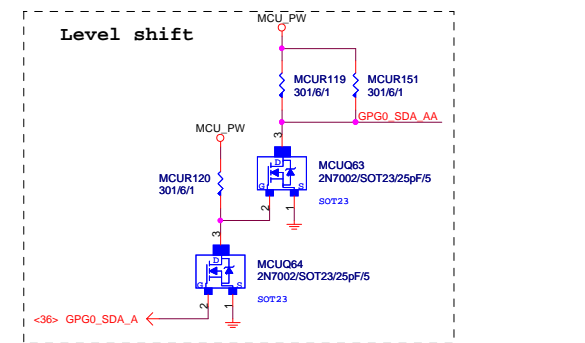
第七區 LED（靠近右下DDR板邊位置）



Digital LED Strip2



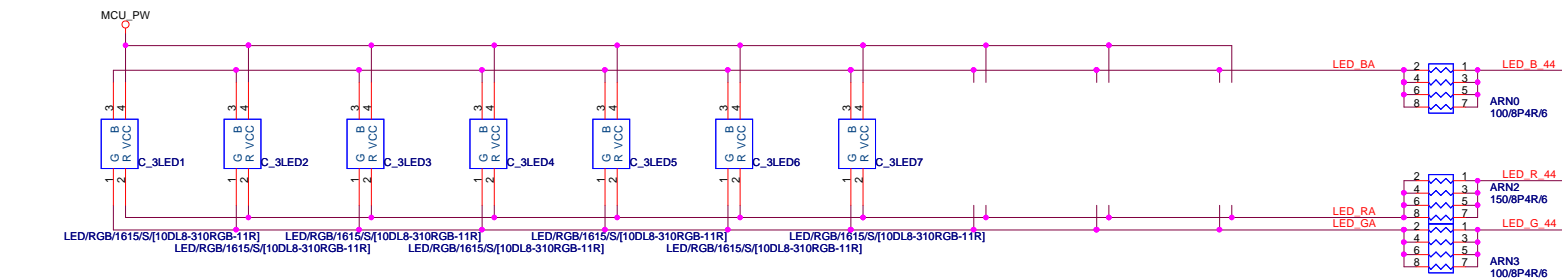
Footprint "PH1X4-CUT3-LED-L"
(for pin-name 與 model-name 同方向)



第三區 LED

第四區 LED

FOR AUDIO 正發光 LED*8 C_3LED1~8)

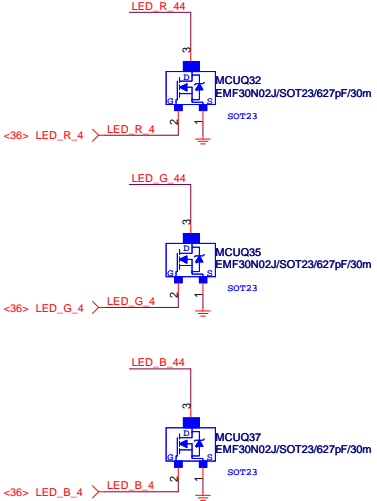


FOOTPRINT:LED-4P-RGB

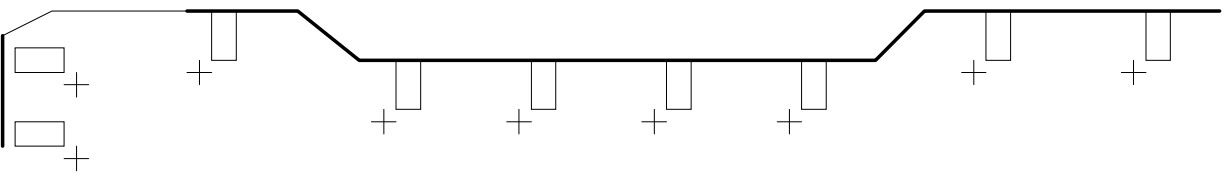
FOR PCIE16_1 側發光 LED*4
(位置在PCIE16_1 SLOT兩側各4顆)

FOR PCIE8 側發光 LED*4
(位置在PCIE8 SLOT兩側各4顆)

第四區 LED CONTROL



Audio Ground切割線+背面 RGB LED



RGB LED LAYOUT 注意事項 :

- 1. Debug LED (各LED依CPU/DRAM/VGA/BOOT個別位置擺放)
- 2. 背板 RGB LED 方向整板請統一如下
(整板正極可統一朝下或朝上)
- 3. 正板 RGB LED 統一方向即可
- 4. MCU_PW & MCU_PW33電源一律走20mils
- 5. ECF1,ECF2,ECF3,ECF5 兩端電源走80mils或用鋪銅方式加粗
- 6. MCU LED 出pin的走線4mils,如:LED_R_1,LED_G_1,LED_B_1
- 7. LED RGBW rule :W/S=10/5 mils 如:LED_R_11,LED_G_11,LED_B_11,LED_W.....
(包含從晶體到排阻到LED的net)
- 8. Digital LED NET rule W/S=4/8 mils
GPD0_SDA_B,GPD0_SDA_BB,GPD0_SDA_C,GPD0_SDA_CC

For AMD MCU update

