1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X2203/MLB

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0031723518	ENGINEERING RELEASED	2021-10-03

LAST_MODIFICATION=Sun Oct 3 21:59:49 2021

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61	152	USB-C: Support 1 ATC01	USBC	09/26/2021
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X2203GHUB = https://github.pie.apple.com/MobileMacIX/j413_hw/blob/master/j413/

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Apple Inc.

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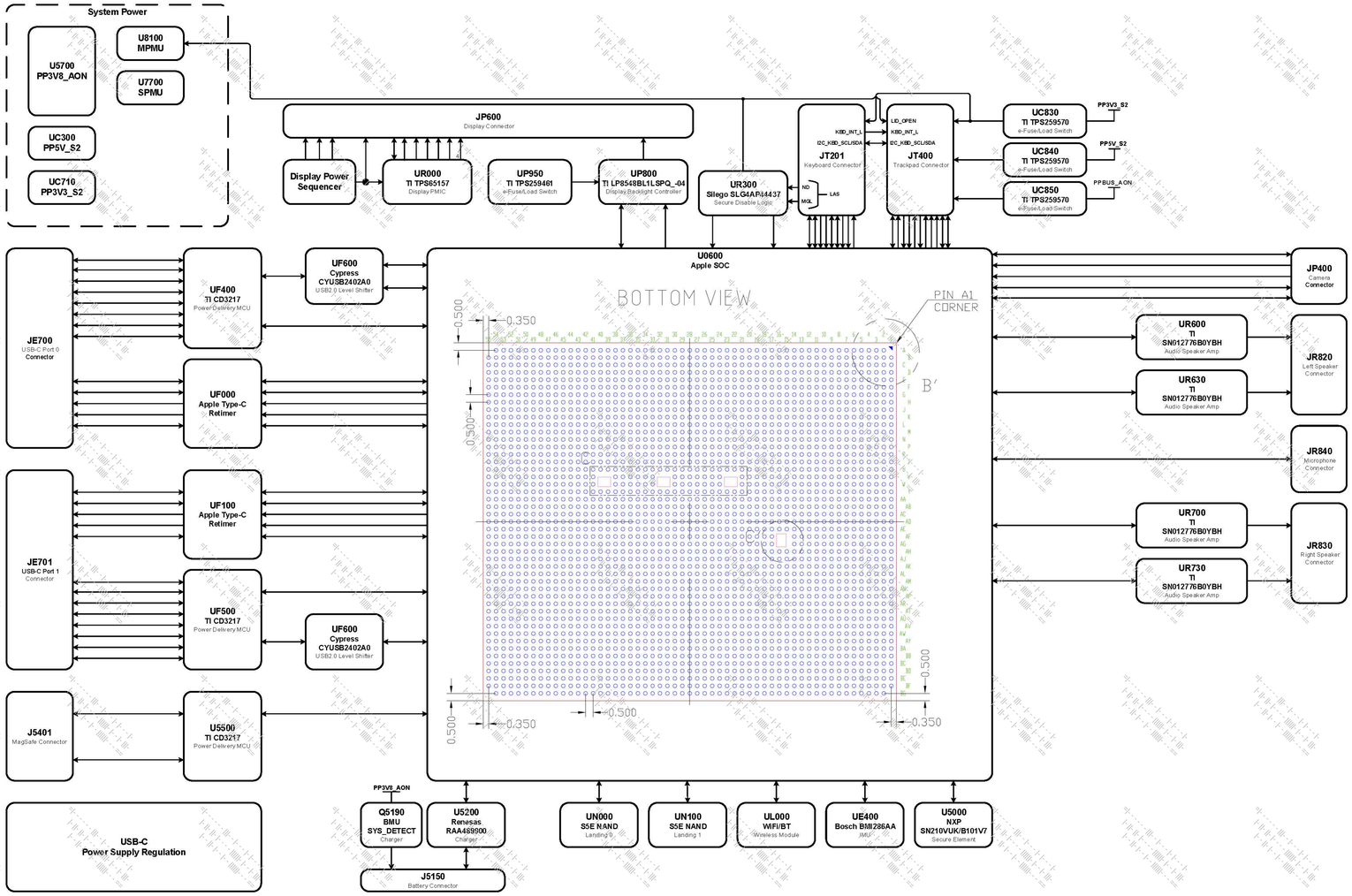
Block Diagram



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PAGE TITLE: PAGE_TITLE=Block Diagram

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A BOM Groups

BOM GROUP	BOM OPTIONS
MLB_COMMON	SCHEM,PCBF,COMMON,MLB_PROGPARTS,MLB_USBC,MLB_POWER,MLB_PMU,MLB_MECH,MLB_MISC,MLB_BLC,MLB_TCON,MLB_WIRELESS,EVT
MLB_USBC	ATCRTMR:B0,USBCPC:LAPTOP_B3,RT13_EFUSE:VDDIO,EUSB_LS:B0,ACE_WILL_BE_OTPED:YES,LFKA_TEST_MODE:YES
MLB_PROGPARTS	SOC_ROM:BLANK,RT13_ROM:BLANK,SE:DEV_SW_LN,UPC01_ROM:EVT,UPC5_ROM:EVT
MLB_POWER	P3V8AON_IC:A2_R170,P3V8AON_LPM,WHAMOLA:0A5-13V7,P5VS2PWREN_BYPASS:NO
MLB_PMU	MPMU_IC:A0_JPI,SPMU_IC:A0_JPI,PMU_BULK_VDDQL,PMU_32K_CLK:XOSC,PMU_FB:FF,BUCK6_BULK_REG
MLB_MECH	SHLD_CAN_MLB:EVT,BRKT_KBD:EVT
MLB_MISC	BOARD_ID,TPAD_32KCLK:NO,SYSDET:FET,BOOT_CFG_0,PMU_OUT32K:WLBT,SENSOR_IMU,MIPI_PWR:NO,REFIMU_IC:BMI284,QS360_DLY:YES,SOC_R9706:80HM,OCELOT_BYPASS:100NF
MLB_DEV	SENSORS:DEV,DEVELOPMENT,USBC_DBG,BTN_DBG
MLB_BLC	BLC_BEN_IC:V8,BLC_5V_CAP:4P7_UF,BLC_5V_SERIES:10_OHM,BLC_KBD_BOOST_USED:NO
MLB_TCON	PMIC_SDG_VBUCK1:NO,SDG_TI_PROG:X2203,SDG_TI
MLB_WIRELESS	RF-CONN

B Build Specific Groups

BOM GROUP	BOM OPTIONS	
BOARD_ID	BOARD_ID_3	Pull-ups: BOARD_ID[7:0] = 8'b0010_1000
PROTO0	BOARD_REV_3,BOARD_REV_2,BOARD_REV_1,BOARD_REV_0	Pull-downs: 4'b0000
PROTO1	BOARD_REV_3,BOARD_REV_2,BOARD_REV_1	Pull-downs: 4'b0001
PROTO1B	BOARD_REV_3,BOARD_REV_2,BOARD_REV_0	Pull-downs: 4'b0010
PROTO2	BOARD_REV_3,BOARD_REV_2	Pull-downs: 4'b0011
PROTO2B	BOARD_REV_3,BOARD_REV_1,BOARD_REV_0	Pull-downs: 4'b0100
EVT	BOARD_REV_3,BOARD_REV_1	Pull-downs: 4'b0101
DVT	BOARD_REV_3,BOARD_REV_0	Pull-downs: 4'b0110
PVT	BOARD_REV_3	Pull-downs: 4'b0111

C DC/DC BOM Groups

BOM GROUP	BOM OPTIONS
DCDC_COMMON	SCHEM,PCBF,COMMON,MLB_POWER,MLB_PMU,MLB_MECH,MLB_MISC,MLB_BLC,EVT

D RF BOM Groups

BOM GROUP	BOM OPTIONS
RF_COMMON	SCHEM,PCBF,RF-CONN

E Top-Level APNs

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-07020	1	SCHEM,MLB,X2203	SCHEM	CRITICAL	SCHEM
820-02536	1	PCBF,MLB,X2203	PCBF	CRITICAL	PCBF
685-00426	1	COMMON PARTS,MLB,X2203	CBOM	CRITICAL	CMN_PARTS_BOM
685-00427	1	NAND1,MLB,X2203	P1BOM	CRITICAL	PARTS_SSDNAND1
985-01536	1	DEV PARTS,MLB,X2203	DEV1	CRITICAL	DEV_PARTS_BOM

F Reference Design Pack Options

USB-C

PACK_OPTIONS TO INCLUDE IN NETLIST
USBC_SPI_UPC0
USBC_DEBUG_UPC0
USBC01_VR5V_LOCAL_NO
USBC_LAPTOP
PKGS:SMALL_PITCH
USBC_LAPTOP_CC_PRT
ACE2_SS_CAP
USBC_SPI_NO_2ND_ROM
USBC_SPI_UPC0_AND_NO_2ND_ROM
ACTIVE_READY:SMALL_PITCH:CHECK_WITH_DFW
INV:DPW

Iceman VR

PACK_OPTIONS TO INCLUDE IN NETLIST
3V8_AON_PBUS-18V
3V8_AON_I2C-DEV
3V8_INDUCTOR:1P5MM
3V8_AON_MLCC-LN

Wireless

PACK_OPTIONS TO INCLUDE IN NETLIST
SUNWAY
WLBT_D2R_TP_STATEN
WLBT_TP_0P2

Audio

PACK_OPTIONS TO INCLUDE IN NETLIST
SPKRAMP_A
SPKRAMP_B
SPKRAMP_D
SPKRAMP_E
SPKRAMP_ICC_GB

PP3V3_S2 VR

PACK_OPTIONS TO INCLUDE IN NETLIST
3V3_S2_PBUS-18V
3V3_S2_MLCC-LN
3V3_S2_VOUT-B12

Charger

PACK_OPTIONS TO INCLUDE IN NETLIST
CHGR_72W
CHGR_PBUS18V
CHGR_MLCC-LN

PP5V_S2 VR

PACK_OPTIONS TO INCLUDE IN NETLIST
5V_S2_PBUS18V
5V_S2_VOUT-B12
5V_S2_IND-15
5V_S2_MLCC-LN
5V_S2_THINSTNCL

Display Backlight

PACK_OPTIONS TO INCLUDE IN NETLIST
BLC_CBULK:0603
BLC_FET:OFF
BLC_IND:10UH
PANELPWR_MINNIE
BLC_FERRITE:YES

SOC

PACK_OPTIONS TO INCLUDE IN NETLIST
SOC_MIPI_ENABLE
SOC_MIPI_1SIDE
ONE_SIDED
PCIE_GP0
LPDP_INT_RCAL
LPDPRX0_RCAL
OCELOT_BYPASS:10UF

NAND

PACK_OPTIONS TO INCLUDE IN NETLIST
SSD_4_3UF_0402THIN

PMU

PACK_OPTIONS TO INCLUDE IN NETLIST
TPAD32K:PMU
PMU_32K_MEMS
PMU_32K_XOSC

IMU

PACK_OPTIONS TO INCLUDE IN NETLIST
REFIMU_VDD:LCFILT
REFIMU_TEST:NO

This is on purpose

SYNC_DATE=09/10/2021

PAGE TITLE: BOM Configuration

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DRAWING NUMBER: 051-07020 SIZE: D

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A Mounting Holes

SH0400
TH-NSP
1
SL-3.41X2.0-5.91X4.5
998-19374

SH0401
4.6R2.0-NSP
1
998-25030

SH0403
4.6X5.2R1.7X2.3-NSP
1
998-11114

SH0402
5.0R2.0-NSP
1
998-25031

B MDB Cowling Bosses

SH0440
2.7X1.8R-1.4ID-1.26H-SM
1
860-01964

C MagSafe/USB-C Cowling Bosses

SH0450
2.7X1.8R-1.4ID-1.16H-SM
1
860-01916

SH0451
2.7X1.8R-1.4ID-1.16H-SM
1
860-01916

SH0452
2.7X1.8R-1.4ID-1.16H-SM
1
860-01916

SH0453
2.7X1.8R-1.4ID-1.16H-SM
1
860-01916

D WiFi Module Cowling Boss

SH0470
1.8X2.7R-1.64H-SM
1
860-01957

E Right Speaker Cowling Boss

SH0480
6.12X1.8R-2HOLE-1.38H
1
860-01912

F MLB Shield Fence

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-32496	1	SHIELD,FENCE,THERMAL,MLB,P1,X2147	SHLD1	CRITICAL	SHLD_CAN_MLB:P2
806-35214	1	FENCE,MLB,EVT,X2147	SHLD1	CRITICAL	SHLD_CAN_MLB:EVT

SH0430
TH-NSP
1
SL-0.5X1.28-1.25X2.03
998-21458

SH0432
TH-NSP
1
SL-0.5X1.28-1.25X2.03
998-21458

SH0434
TH
1
SL-0.4X1.20
998-1681

SH0436
TH-NSP
1
SL-0.5X1.28-1.25X2.03
998-21458

SH0431
TH-NSP
1
SL-0.5X1.28-1.25X2.03
998-21458

SH0433
TH-NSP
1
SL-0.5X1.28-1.25X2.03
998-21458

SH0435
TH
1
SL-0.4X1.20
998-1681

SH0437
TH-NSP
1
SL-0.5X1.28-1.25X2.03
998-21458

G SOC Thermal Module Bosses

SH0490
STDOFF-3.8X2.5R-1.36H-SM
1
860-01913

SH0491
STDOFF-3.8X2.5R-1.36H-SM
1
860-01913

SH0492
STDOFF-3.8X2.5R-1.36H-SM
1
860-01913

SH0493
STDOFF-3.8X2.5R-1.36H-SM
1
860-01913

H Antenna Cowling Bosses

SH04A0
2.44X2.44SQ-1.15ID-1.044H-SM
1
860-02043

SH04A1
2.44X2.44SQ-1.15ID-1.044H-SM
1
860-02043

I Spacers

SH04B0
SPACER-MLB-X2147
SM
1
806-31591

SH04B2
SPACER-MLB-SMT-SML
SM
1
806-31120

SH04B1
SPACER-MLB-SMT
SM
1
806-31119

SH04B3
SPACER-MLB-SMT-LRG
SM
1
806-31121

J Keyboard Bracket

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-32523	1	BRKT,MLB,SMT,X2147	BRKT1	CRITICAL	BRKT_KBD:P2
806-35209	1	BRKT,MLB,EVT,X2147	BRKT1	CRITICAL	BRKT_KBD:EVT

BOM_COST_GROUP=MECHANICALS

SYNC_DATE=09/10/2021

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PD Parts

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REVISION 6.0.0
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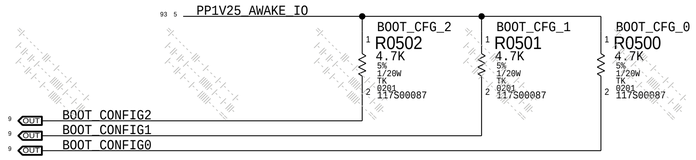
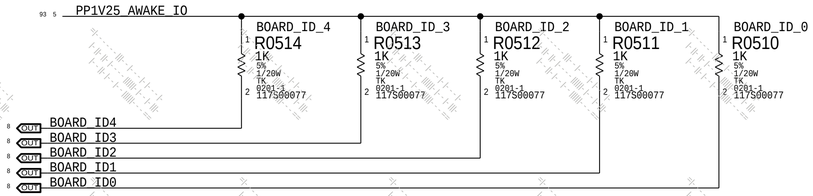
A BOOT CONFIG ID



STATEN BOOT AND POWER uARCH SPEC 2.1.5 (Section 2.2, Table 2.3):

BOOT_CFG[2:0]	MODE
000	NAND, 1.2V SPI0, 12MHZ, TESTMODE
001	NOR, 1.2V SPI1, 40MHZ
010	NAND, 1.2V SPI0, 12MHZ
011	NAND, 1.2V SPI0, 40MHZ
100	NOR, 1.2V SPI1, 12MHZ, TESTMODE
101	NOR, 1.2V SPI1, 40MHZ, TESTMODE
110	NOR, 1.2V SPI1, 6MHZ, TESTMODE
111	NOR, 1.2V SPI1, 12MHZ

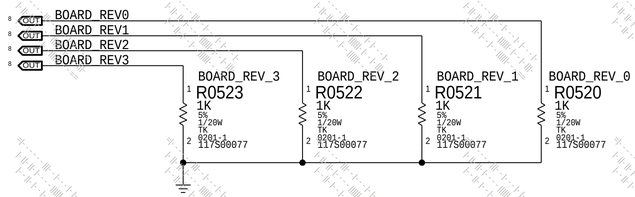
B BOARD ID



BoardID Wiki URL:

- BOARD_ID[7:0] assignments by product at link in QR Code.
- BOARD_ID[7:5] come from SOC
- BOARD_ID[4:0] are straps on MLB, sampled 100US after cold reset deassert.
- Staten Boot Power Micro Architecture Spec 2.1.3

C BOARD REV



- Stuffing the Resistor Results in a Logic Low (1'b0)

BOM_COST_GROUP=SOC

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE: SOC: CONFIG STRAPS

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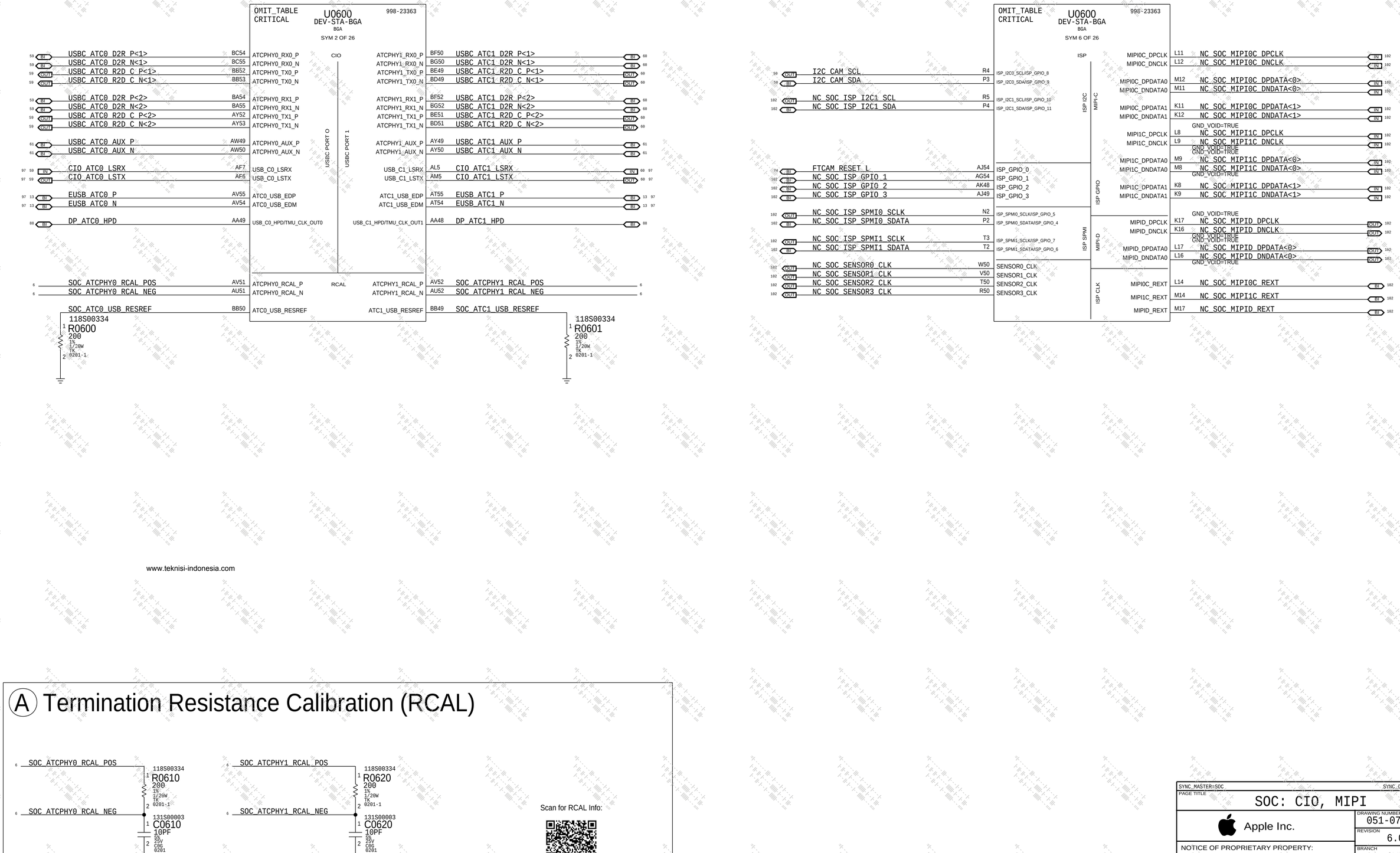

BOM_COST_GROUP=SOC

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE: SOC: CIO, MIPI

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DRAWING NUMBER: 051-07020 SIZE: D

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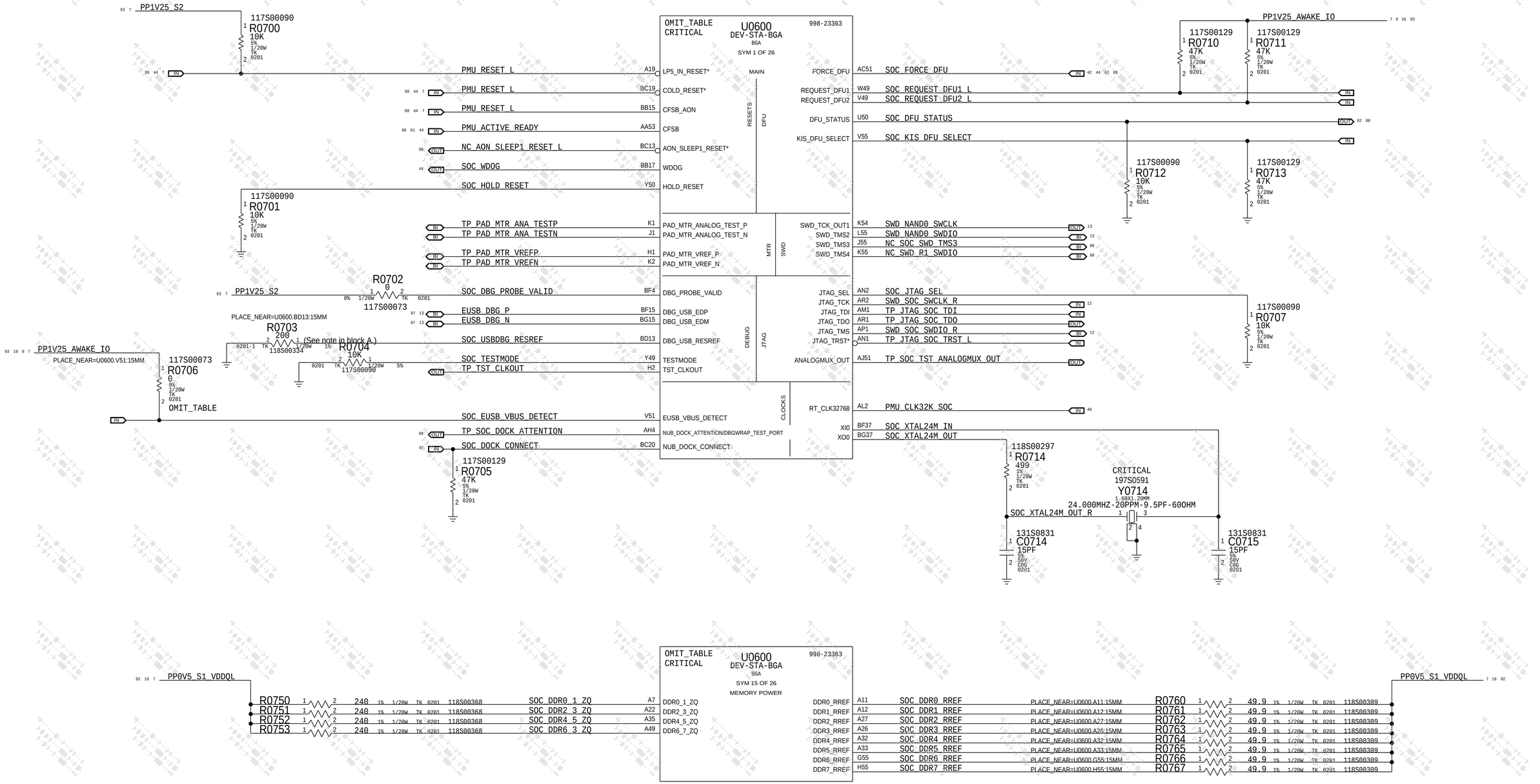

(A) RESREF Notes

- The RESREF node is sensitive to noise.
- 1-sided PCBs may be able to place R0703 less than 15mm from SOC pin on the perimeter of the SOC.
- 2-sided PCBs may be able to place R0703 less than 5mm from SOC pin.

(B) EUSB_VBUS_DETECT BOM Table

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S00090	1	RES,TK,10K OHM,5%,1/20W,0201	R0706	SOC_R0706:10K0HM
117S00073	1	RES,TK,0 OHM,1A MAX,1/20W,0201	R0706	SOC_R0706:0OHM

BOM_COST_GROUP=SOC

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE: SOC: RESETS, DEBUG, MISC

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AOP, NUB, SMC

Signal	Ball	Pin	Dir	Pull	Group
NC_AOP_FUNC0	U5	AOP_FUNC[0]	BI		AOP GPIO
NC_AOP_FUNC1	AB4	AOP_FUNC[1]	BI		AOP GPIO
NC_AOP_FUNC2	Y4	AOP_FUNC[2]	BI		AOP GPIO
NC_AOP_FUNC3	U4	AOP_FUNC[3]	BI	IPD	AOP GPIO
ALS_INT_L	AB5	AOP_FUNC[4]	BI	IPU	AOP GPIO
NC_SPI_DP2HDMI_HOLD_L	Y5	AOP_FUNC[5]	BI		AOP GPIO
SPI_GYRO_CS_L	AD6	AOP_FUNC[6]	BI		AOP GPIO
GYRO_INT	AC6	AOP_FUNC[7]	BI		AOP GPIO
GYRO_MOTION_INT	AA4	AOP_FUNC[8]	BI		AOP GPIO
NC_HDMI_CEC_AOP_TX	AC4	AOP_FUNC[9]	BI	IPD	AOP GPIO
NC_HDMI_CEC_AOP_RX	W5	AOP_FUNC[10]	BI		AOP GPIO
NC_AOP_FUNC11	AB6	AOP_FUNC[11]	BI		AOP GPIO
NC_AOP_FUNC12	AC5	AOP_FUNC[12]	BI		AOP GPIO
SPI_LAS_CS_L	AR3	AOP_FUNC[13]	BI	IPU	AOP GPIO
NC_HDMI_HDP_AOP	AD4	AOP_FUNC[14]	BI		AOP GPIO
I2C_AOP_ALS_SCL	AD7	AOP_I2CM0_SCL	OUT		AOP I2C
I2C_AOP_ALS_SDA	AE7	AOP_I2CM0_SDA	BI		AOP I2C
NC_SOC_AOP_I2CM1_SCL	AR6	AOP_I2CM1_SCL	OUT		AOP I2C
NC_SOC_AOP_I2CM1_SDA	AP6	AOP_I2CM1_SDA	BI		AOP I2C
NC_SOC_AOP_I2CM2_SCL	AE6	AOP_I2CM2_SCL	OUT		AOP I2C
NC_SOC_AOP_I2CM2_SDA	AE5	AOP_I2CM2_SDA	BI		AOP I2C
NC_AOP_I2S0_BCLK	AR7	AOP_I2S0_BCLK/AOP_PDM_IN_CLK6	OUT		AOP I2S
NC_AOP_I2S0_DIN	AT7	AOP_I2S0_DIN/AOP_PDM_IN_CLK5	IN		AOP I2S
NC_AOP_I2S0_DOUT	AT6	AOP_I2S0_DOUT/AOP_PDM_IN_CLK4	OUT		AOP I2S
NC_AOP_I2S0_LRCLK	AT5	AOP_I2S0_LRCK/AOP_PDM_IN_CLK3	OUT		AOP I2S
NC_PDM_DMIC_CLK2_R	AR5	AOP_I2S0_MCK/AOP_PDM_IN_CLK2	OUT		AOP I2S
PDM_DMIC_CLK1_R	AJ6	AOP_I2S1_BCLK/AOP_PDM_IN_CLK1	OUT		AOP I2S
NC_PDM_DMIC_DATA4	AH6	AOP_I2S1_DIN/AOP_PDM_IN_DATA4/AOP_PDM_IN_CLK8	IN		AOP I2S
PDM_DMIC_CLK7_R	AK6	AOP_I2S1_DOUT/AOP_PDM_IN_DATA3/AOP_PDM_IN_CLK7	OUT		AOP I2S
PDM_DMIC_DATA2	AL6	AOP_I2S1_LRCK/AOP_PDM_IN_DATA2	IN		AOP I2S
PDM_DMIC_DATA1	AH7	AOP_I2S1_MCK/AOP_PDM_IN_DATA1	IN		AOP I2S
SPI_AOP_GYRO_MISO	W4	AOP_SPI0_MISO	IN		AOP SPI
SPI_AOP_GYRO_MOSI_R	V4	AOP_SPI0_MOSI	OUT		AOP SPI
SPI_AOP_GYRO_CLK_R	U3	AOP_SPI0_SCLK	OUT		AOP SPI
SPI_AOP_SENSORS_MISO	AP7	AOP_SPI1_MISO	IN		AOP SPI
SPI_AOP_SENSORS_MOSI_R	AM6	AOP_SPI1_MOSI	OUT		AOP SPI
SPI_AOP_SENSORS_CLK_R	AN7	AOP_SPI1_SCLK	OUT		AOP SPI
NC_SOC_AOP_SPI1_CS_L	AN6	AOP_SPI1_SSIN	OUT		AOP SPI
SPMI_AOP_WLAN_HEB_CLK_R	AG7	AOP_SPMI0_SCLK	OUT		AOP SPMI
SPMI_AOP_WLAN_HEB_DATA_R	AG6	AOP_SPMI0_SDATA	BI		AOP SPMI
SPMI_AOP_SE_CLK_R	AL7	AOP_SPMI1_SCLK	OUT		AOP SPMI
SPMI_AOP_SE_DATA_R	AM7	AOP_SPMI1_SDATA	BI		AOP SPMI
NC_SOC_AOP_UART0_RXD	AH5	AOP_UART0_RXD	IN		AOP UART
NC_SOC_AOP_UART0_TXD	AJ5	AOP_UART0_TXD	OUT		AOP UART
NC_SOC_AOP_UART1_RXD	AJ7	AOP_UART1_RXD	IN		AOP UART
NC_SOC_AOP_UART1_TXD	AK7	AOP_UART1_TXD	OUT		AOP UART
NC_SOC_AOP_UART2_RXD	AN5	AOP_UART2_RXD	IN		AOP UART
NC_SOC_AOP_UART2_TXD	AR4	AOP_UART2_TXD	OUT		AOP UART
DMIC_DISABLE_L	AF4	MIC_DISABLE*	IN		
DMIC_DISABLE_WARN_L	AF5	MIC_DISABLE_WARN*	IN		

Signal	Ball	Pin	Dir	Pull	Group
NUB_CLK_OUT0	AB1	NUB_GPIO_0/AOP_FUNC15/NUB_CLK_OUT1	OUT		NUB GPIO
NC_SOC_NUB_CLK_OUT_0	AK4	NUB_GPIO_1/AOP_PDM_IN_CLK0	BI		NUB GPIO
NC_BKLT_PWR_ON	Y3	NUB_GPIO_2/AOP_PDM_IN_DATA0	BI		NUB GPIO
CODEC_RESET_L	BB14	NUB_GPIO_3/AOP_LEAP_MADI_IN	BI		NUB GPIO
SOC_SW_DBG	AA3	NUB_GPIO_4/AOP_LEAP_MADI_OUT	BI	IPU	NUB GPIO
TP_AOP_LEAP_MADI_IN	AB3	NUB_GPIO_5/AOP_PDM_OUT_CLK0	BI		NUB GPIO
TP_AOP_LEAP_MADI_OUT	U2	NUB_GPIO_6/AOP_PDM_OUT_DATA0/AOP_FUNC16	BI	IPU	NUB GPIO
SMC_FIXTURE_MODE_L	AJ4	NUB_GPIO_7/AOP_FUNC17	BI		NUB GPIO
CHGR_INT_L	AD3	NUB_GPIO_8/AOP_FUNC18	BI		NUB GPIO
NC_ENET_LOW_PWR	AE4	NUB_GPIO_9/AOP_FUNC19	BI		NUB GPIO
NC_LOM_PMU_RESET_EN	T4	NUB_GPIO_10/AOP_FUNC20	BI		NUB GPIO
NC_AOP_FUNC19	AP3	NUB_GPIO_11/KIS_GPIO0/AOP_FUNC21	BI		NUB GPIO
NC_AOP_FUNC20	AN3	NUB_GPIO_12/KIS_GPIO1/AOP_FUNC22	BI	IPU	NUB GPIO
IPD_SYS_AWAKE	Y2	NUB_SPMI0_SCLK	OUT		NUB SPMI
NC_SOC_NUB_GPIO_12	AT2	NUB_SPMI0_SDATA	BI		NUB SPMI
SPMI_NUB_MPMU_CLK_R	AT1	NUB_SPMI1_SCLK	OUT		NUB SPMI
SPMI_NUB_MPMU_DATA_R	AM4	NUB_SPMI1_SDATA	BI		NUB SPMI
SPMI_NUB_SPMU_CLK_R	AL4	NUB_SWD_TCK_OUT0	OUT		NUB SWD
SPMI_NUB_SPMU_DATA_R	AM3	NUB_SWD_TCK_OUT2	OUT		NUB SWD
SWD_NUB_PMU_SWCLK_R	AH3	NUB_SWD_TMS0	BI		NUB SWD
SWD_NUB_ATCRTMR_IPD_SWCLK	AK3	NUB_SWD_TMS1	BI		NUB SWD
SWD_NUB_PMU_SWDIO_R	AJ3	NUB_SWD_TMS5	BI		NUB SWD
SWD_IPD_SWDIO	AL3	SMC_I2CM0_SCL	OUT		SMC I2C
SWD_NUB_ATCRTMR_SWDIO_R	AC1	SMC_I2CM0_SDA	BI		SMC I2C
I2C_SMC_PWR_SCL	AD1	SMC_I2CM1_SCL/SMC_UART1_TXD	OUT		SMC I2C
I2C_SMC_PWR_SDA	AT4	SMC_I2CM1_SDA/SMC_UART1_RXD	BI		SMC I2C
I2C_SMC_UPC_SCL	AT3	SMC_I2CM2_SCL	OUT		SMC I2C
I2C_SMC_UPC_SDA	AP4	SMC_I2CM2_SDA	BI		SMC I2C
I2C_SMC_SNS1_SCL	AN4	SMC_I2CM3_SCL	OUT		SMC I2C
I2C_SMC_SNS1_SDA	W3	SMC_I2CM3_SDA	BI		SMC I2C
I2C_SMC_IPD_SCL	V3	SMC_I2CM4_SCL	OUT		SMC I2C
I2C_SMC_IPD_SDA	W1	SMC_I2CM4_SDA	BI		SMC I2C
NC_I2C_SMC_SNS0_SCL	V1	SMC_UART0_RXD	IN	IPD	SMC UART
NC_I2C_SMC_SNS0_SDA	AE2	SMC_UART0_TXD	OUT		SMC UART
UART_SMC_DEBUGPRT_D2R	AE3	SMC_GPIO0	BI	IPU	SMC GPIO
UART_SMC_DEBUGPRT_R2D	AC2	SMC_GPIO1	BI		SMC GPIO
UPC_SMC_I2C_INT_L	AB2	SMC_FPWM0	OUT		SMCFPWM
NC_SOC_SMC_GPIO_1	W6	SMC_FPWM1	IN		SMCFPWM
NC_SMC_FAN_0_PWM	AC3	SMC_FPWM2	OUT		SMCFPWM
NC_SMC_FAN_0_TACH	W2	SMC_FPWM3	IN		SMCFPWM
NC_SMC_FAN_1_PWM	Y6				
NC_SMC_FAN_1_TACH					

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Signal	Ball	Pin	Dir	Pull	Group
UPC_I2C_INT_L	G1	GPIO[0]	BI	IPU	GPIO
NC_SOC_AP_GPIO_1	AN55	GPIO[1]	BI		GPIO
SPKR_ID0	AL51	GPIO[2]	BI	IPU	GPIO
SPKR_ID1	AH53	GPIO[3]	BI	IPU	GPIO
SPKRAMP_RESET_L	BG8	GPIO[4]	BI		GPIO
SPKRAMP_INT_L	F1	GPIO[5]	BI	IPU	GPIO
CODEC_INT_L	AG51	GPIO[6]	BI	IPU	GPIO
SWD_UPC_SWCLK_R	R54	GPIO[7]	BI		GPIO
SWD_UPC_SWDIO0_R	R51	GPIO[8]	BI		GPIO
SWD_UPC_SWDIO1_R	R53	GPIO[9]	BI		GPIO
NC_CCG_I2C_INT	U55	GPIO[10]	BI		GPIO
BOARD_REV0	T55	GPIO[11]	BI		GPIO
BOARD_REV1	N55	GPIO[12]	BI		GPIO
BOARD_REV2	U52	GPIO[13]	BI		GPIO
BOARD_REV3	J2	GPIO[14]	BI		GPIO
NC_DMIC_ID	D54	GPIO[15]	BI		GPIO
NC_SOC_GPIO16	C54	GPIO[16]	BI		GPIO
NC_SOC_GPIO17	D53	GPIO[17]	BI		GPIO
NC_SOC_AP_GPIO_18	E54	GPIO[18]	BI		GPIO
NC_SOC_AP_GPIO_19	F54	GPIO[19]	BI		GPIO
NC_ENET_I2C_LOM_INT_L	T53	GPIO[20]	BI		GPIO
TOUCHID_INT	R52	GPIO[21]	BI	IPD	GPIO
TOUCHID_PWR_EN	V53	GPIO[22]	BI		GPIO
NC_SOC_AP_GPIO_23	T52	GPIO[23]	BI		GPIO
NC_SOC_AP_GPIO_24	V52	GPIO[24]	BI		GPIO
NC_ENET_SELECT_1G_H_10G_L	AC49	GPIO[25]	BI		GPIO
NC_SOC_AP_GPIO_26	AC50	GPIO[26]	BI	IPD	GPIO
BOARD_ID0	M1	BOARD_ID0/SOC_DEBUG1	IN		BOARD ID
BOARD_ID1	M2	BOARD_ID1/SOC_DEBUG2	IN		BOARD ID
BOARD_ID2	N1	BOARD_ID2/SOC_DEBUG3	IN		BOARD ID
BOARD_ID3	P1	BOARD_ID3/SPI0_SSIN	IN		BOARD ID
BOARD_ID4	U1	BOARD_ID4	IN		BOARD ID
UART_DEBUGPRT_D2R	Y52	UART0_RXD	IN	IPU	UART
UART_DEBUGPRT_R2D	W52	UART0_TXD	OUT		UART
NC_SOC_AP_UART1_CTS_L	G2	UART1_CTS*	IN		UART
NC_SOC_AP_UART1_RTS_L	D1	UART1_RTS*	OUT		UART
NC_SOC_AP_UART1_RXD	F2	UART1_RXD	IN		UART
NC_SOC_AP_UART1_TXD	E1	UART1_TXD	OUT		UART
NC_SOC_AP_UART2_CTS_L	D3	UART2_CTS*	IN	IPU	UART
NC_SOC_AP_UART2_RTS_L	E2	UART2_RTS*	OUT		UART
NC_SOC_AP_UART2_RXD	D2	UART2_RXD	IN	IPU	UART
NC_SOC_AP_UART2_TXD	C2	UART2_TXD	OUT		UART
NC_SOC_AP_UART3_CTS_L	Y54	UART3_CTS*	IN		UART
NC_SOC_AP_UART3_RTS_L	W53	UART3_RTS*	OUT		UART
NC_SOC_AP_UART3_RXD	Y53	UART3_RXD	IN		UART
NC_SOC_AP_UART3_TXD	V54	UART3_TXD	OUT		UART
NC_SOC_AP_UART4_RXD	U54	UART4_RXD	IN		UART
NC_SOC_AP_UART4_TXD	U53	UART4_TXD	OUT		UART
UART_TCON_D2R	AC52	UART6_RXD	IN	IPU	UART
NC_UART_TCON_R2D	AC53	UART6_TXD	OUT		UART
NC_UART_HDMI_D2R	P55	UART7_RXD	IN		UART
NC_UART_HDMI_R2D	R55	UART7_TXD	OUT		UART
NAND0_CLK24M0_R	AJ50	NAND_SYS_CLK0	OUT		NAND
NAND0_CLK24M1_R	AK50	NAND_SYS_CLK1	OUT		NAND
NAND_BFH	AL53	SSD_BFH	OUT		NAND
NAND0_RESET_L	AJ53	SSD_RESET*	OUT		NAND

BOM_COST_GROUP=SOC

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

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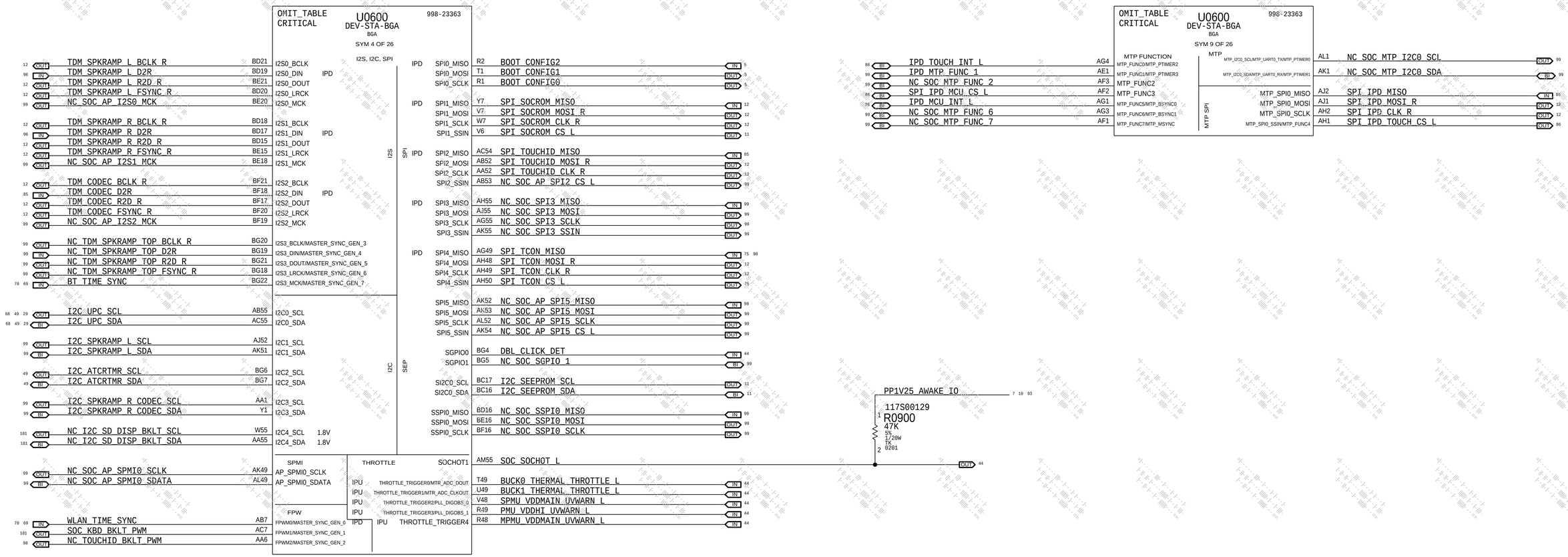

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LPDP FTCAM AUX C	AV7	LPDPRX_AUX_D0_P	LPDP RX	LPDP_TX0P / LPDP_TX0N	BG44 / BF44 LPDP INT DATA C P<0> / LPDP INT DATA C N<0>
NC SOC LPDP RX AUX D1	AW7	LPDPRX_AUX_D1_P		LPDP_TX1P / LPDP_TX1N	BG45 / BF45 LPDP INT DATA C P<1> / LPDP INT DATA C N<1>
NC SOC LPDP RX AUX D2	AY7	LPDPRX_AUX_D2_P		LPDP_TX2P / LPDP_TX2N	BG46 / BF46 LPDP INT DATA C P<2> / LPDP INT DATA C N<2>
NC SOC LPDP RX AUX D3	BB7	LPDPRX_AUX_D3_P		LPDP_TX3P / LPDP_TX3N	BG47 / BF47 LPDP INT DATA C P<3> / LPDP INT DATA C N<3>
NC SOC LPDP RX AUX D4	BC7	LPDPRX_AUX_D4_P		LPDP_AUX_P / LPDP_AUX_N	BD42 / BD41 LPDP INT AUX C P / LPDP INT AUX C N
NC SOC LPDP RX AUX D5	BD7	LPDPRX_AUX_D5_P		LPDP_RCAL_P / LPDP_RCAL_N	BC42 / BC41 SOC LPDP INT RCAL POS / SOC LPDP INT RCAL NEG
NC SOC LPDP RX AUX D6	AV8	LPDPRX_AUX_D6_P	LPDP EXT TX	LPDP_EXT_TX0P / LPDP_EXT_TX0N	BG10 / BF10 NC LPDP EXT DATA CP<0> / NC LPDP EXT DATA CN<0>
NC SOC LPDP RX AUX D7	AW8	LPDPRX_AUX_D7_P		LPDP_EXT_TX1P / LPDP_EXT_TX1N	BG11 / BF11 NC LPDP EXT DATA CP<1> / NC LPDP EXT DATA CN<1>
NC SOC LPDP RX AUX D8	AY8	LPDPRX_AUX_D8_P		LPDP_EXT_TX2P / LPDP_EXT_TX2N	BG12 / BF12 NC LPDP EXT DATA CP<2> / NC LPDP EXT DATA CN<2>
NC SOC LPDP RX AUX D9	BB8	LPDPRX_AUX_D9_P		LPDP_EXT_TX3P / LPDP_EXT_TX3N	BG13 / BF13 NC LPDP EXT DATA CP<3> / NC LPDP EXT DATA CN<3>
NC SOC LPDP RX AUX D10	BC8	LPDPRX_AUX_D10_P		LPDP_EXT_AUX_P / LPDP_EXT_AUX_N	BC12 / BC11 NC LPDP EXT AUX CP / NC LPDP EXT AUX CN
NC SOC LPDP RX AUX D11	BD8	LPDPRX_AUX_D11_P		LPDP_EXT_RCAL_P / LPDP_EXT_RCAL_N	BD12 / BD11 NC SOC LPDP DP2HDMI RCAL POS / NC SOC LPDP DP2HDMI RCAL NEG
LPDP FTCAM DATA P<0>	AV1	LPDPRX_RX_D0_P		DISP_HPD / DISP_EXT_HPD	BG17 / BG16 LPDP INT HPD / NC LPDP EXT HPD
LPDP FTCAM DATA N<0>	AV2	LPDPRX_RX_D0_N	DISPLAY	DISP_SPI_MISO/DISP_I2C_SCL	T6 I2C DISP BKLT SCL
NC SOC LPDP RX D1P	AW1	LPDPRX_RX_D1_P		DISP_SPI_MOSI/DISP_I2C_SDA	R6 I2C DISP BKLT SDA
NC SOC LPDP RX D1N	AW2	LPDPRX_RX_D1_N		DISP_SPI_SCLK/DWI_DO	U6 NC SPI DISP BKLT CLK R
NC SOC LPDP RX D2P	AY1	LPDPRX_RX_D2_P		DISP_SPI_SSIN/DWI_CLK	T5 NC SPI DISP BKLT CS L
NC SOC LPDP RX D2N	AY2	LPDPRX_RX_D2_N		DISP_SPMI_SCLK	L2 NC SPMI DISP BKLT CLK
NC SOC LPDP RX D3P	BB1	LPDPRX_RX_D3_P		DISP_SPMI_SDATA	L1 NC SPMI DISP BKLT DATA
NC SOC LPDP RX D3N	BB2	LPDPRX_RX_D3_N		DISP_POL	AG53 NC SOC DISP POL
NC SOC LPDP RX D4P	BC1	LPDPRX_RX_D4_P		DISP_FSYNC	AB50 NC DISP BKLT FSYNC
NC SOC LPDP RX D4N	BC2	LPDPRX_RX_D4_N		DISP_LSYNC	AA50 DISP BKLT LSYNC
NC SOC LPDP RX D5P	BD1	LPDPRX_RX_D5_P		DISP_TOUCH_BSYNC0	AG52 NC SOC DISP TOUCH BSYNC 0
NC SOC LPDP RX D5N	BD2	LPDPRX_RX_D5_N		DISP_TOUCH_BSYNC1	Y55 NC SOC DISP TOUCH BSYNC 1
NC SOC LPDP RX D6P	AV4	LPDPRX_RX_D6_P		DISP_TOUCH_EB	AA54 NC SOC DISP TOUCH EB
NC SOC LPDP RX D6N	AV5	LPDPRX_RX_D6_N		DFR_BSYNC/DISP_INT	AA51 NC BKLT BOOST THROTTLE L
NC SOC LPDP RX D7P	AW4	LPDPRX_RX_D7_P		DFR_DISP_TE	U51 NC SOC DFR DISP TE
NC SOC LPDP RX D7N	AW5	LPDPRX_RX_D7_N			
NC SOC LPDP RX D8P	AY4	LPDPRX_RX_D8_P			
NC SOC LPDP RX D8N	AY5	LPDPRX_RX_D8_N			
NC SOC LPDP RX D9P	BB4	LPDPRX_RX_D9_P			
NC SOC LPDP RX D9N	BB5	LPDPRX_RX_D9_N			
NC SOC LPDP RX D10P	BC4	LPDPRX_RX_D10_P			
NC SOC LPDP RX D10N	BC5	LPDPRX_RX_D10_N			
NC SOC LPDP RX D11P	BD4	LPDPRX_RX_D11_P			
NC SOC LPDP RX D11N	BD5	LPDPRX_RX_D11_N			
SOC LPDPRX RCAL POS	BA1	LPDPRX0_RCAL_P			
SOC LPDPRX RCAL NEG	BA2	LPDPRX0_RCAL_N			
NC SOC LPDP RX1 RCAL POS	BA5	LPDPRX1_RCAL_P			
NC SOC LPDP RX1 RCAL NEG	BA4	LPDPRX1_RCAL_N			

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U0600
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BGA
998-23363
SYM 7 OF 26

PCIE NAND0 D2R P<0>	BF24	ST_PCIE_RX0_P	PCIE, MTR	GP_PCIE_RX0_P	BF29 PCIE WLBT D2R P
PCIE NAND0 D2R N<0>	BG24	ST_PCIE_RX0_N		GP_PCIE_RX0_N	BG29 PCIE WLBT D2R N
PCIE NAND0 R2D C P<0>	BD23	ST_PCIE_TX0_P	PCIE ST0 / PCIE GP0	GP_PCIE_TX0_P	BD28 PCIE WLBT R2D C P
PCIE NAND0 R2D C N<0>	BE23	ST_PCIE_TX0_N		GP_PCIE_TX0_N	BE28 PCIE WLBT R2D C N
PCIE CLK100M NAND0 0 P	BC36	ST_PCIE_REF_CLK0_P		GP_PCIE_REF_CLK0_P	BF40 PCIE CLK100M WLBT P
PCIE CLK100M NAND0 0 N	BD36	ST_PCIE_REF_CLK0_N		GP_PCIE_REF_CLK0_N	BG40 PCIE CLK100M WLBT N
NAND0 CLKREQ0 L	AL55	ST_PCIE_CLKREQ0*		UID_MODE GP_PCIE_CLKREQ0*	J54 WLBT CLKREQ L
NAND0 PCIE RESET L	AG50	ST_PCIE_PERST0*		GP_PCIE_PERST0*	M55 WLBT RESET L
PCIE NAND0 D2R P<1>	BF26	ST_PCIE_RX1_P	PCIE ST1 / PCIE GP1	GP_PCIE_RX1_P	BF31 NC SOC GP PCIE RX1P
PCIE NAND0 D2R N<1>	BG26	ST_PCIE_RX1_N		GP_PCIE_RX1_N	BG31 NC SOC GP PCIE RX1N
PCIE NAND0 R2D C P<1>	BD25	ST_PCIE_TX1_P		GP_PCIE_TX1_P	BD30 NC SOC GP PCIE TX1P
PCIE NAND0 R2D C N<1>	BE25	ST_PCIE_TX1_N		GP_PCIE_TX1_N	BE30 NC SOC GP PCIE TX1N
PCIE CLK100M NAND0 1 P	BC37	ST_PCIE_REF_CLK1_P		GP_PCIE_REF_CLK1_P	BF41 NC SOC GP PCIE CLK1 100MP
PCIE CLK100M NAND0 1 N	BD37	ST_PCIE_REF_CLK1_N		GP_PCIE_REF_CLK1_N	BG41 NC SOC GP PCIE CLK1 100MN
NAND0 CLKREQ1 L	AP55	ST_PCIE_CLKREQ1*		GP_PCIE_CLKREQ1*	M54 NC SOC GP PCIE CLKREQ 1 L
NC SOC ST PCIE PERST 1 L	AH52	ST_PCIE_PERST1*		GP_PCIE_PERST1*	F55 NC SOC GP PCIE PERST 1 L
			PCIE GP2	GP_PCIE_RX2_P	BF33 NC SOC GP PCIE RX2P
				GP_PCIE_RX2_N	BG33 NC SOC GP PCIE RX2N
				GP_PCIE_TX2_P	BD32 NC SOC GP PCIE TX2P
				GP_PCIE_TX2_N	BE32 NC SOC GP PCIE TX2N
				GP_PCIE_REF_CLK2_P	BF39 NC SOC GP PCIE CLK2 100MP
				GP_PCIE_REF_CLK2_N	BG39 NC SOC GP PCIE CLK2 100MN
				GP_PCIE_CLKREQ2*	L54 NC SOC GP PCIE CLKREQ 2 L
				GP_PCIE_PERST2*	D55 NC SOC GP PCIE PERST 2 L
			PCIE GP3	GP_PCIE_RX3_P	BF35 NC SOC GP PCIE RX3P
				GP_PCIE_RX3_N	BG35 NC SOC GP PCIE RX3N
				GP_PCIE_TX3_P	BD34 NC SOC GP PCIE TX3P
				GP_PCIE_TX3_N	BE34 NC SOC GP PCIE TX3N
				GP_PCIE_REF_CLK3_P	BF42 NC SOC GP PCIE CLK3 100MP
				GP_PCIE_REF_CLK3_N	BG42 NC SOC GP PCIE CLK3 100MN
				GP_PCIE_CLKREQ3*	P54 NC SOC GP PCIE CLKREQ 3 L
				GP_PCIE_PERST3*	E55 NC SOC GP PCIE PERST 3 L
SOC ST PCIE RCAL POS	BB29	ST_PCIE_RCAL_P		GP_PCIE_RCAL_P	BB26 SOC GP PCIE RCAL POS
SOC ST PCIE RCAL NEG	BB28	ST_PCIE_RCAL_N		GP_PCIE_RCAL_N	BB27 SOC GP PCIE RCAL NEG

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A Termination Resistance Calibration (RCAL)

NC SOC LPDP RX1 RCAL POS (PACK_IGNORE=TRUE, PACK_OPTION=LPDPRX1_RCAL)	R1020 200 1% 1/20W TK 0201-1	SOC LPDPRX RCAL POS (PACK_OPTION=LPDPRX0_RCAL)	R1021 200 1% 1/20W TK 0201-1
NC SOC LPDP RX1 RCAL NEG (PACK_IGNORE=TRUE, PACK_OPTION=LPDPRX1_RCAL)	C1020 10PF 5% 25V C0G 0201	SOC LPDPRX RCAL NEG (PACK_OPTION=LPDPRX0_RCAL)	C1021 10PF 5% 25V C0G 0201
NC SOC LPDP DP2HDMI RCAL POS (PACK_IGNORE=TRUE, PACK_OPTION=LPDP_EXT_RCAL)	R1022 200 1% 1/20W TK 0201-1	SOC LPDP INT RCAL POS (PACK_OPTION=LPDP_INT_RCAL)	R1023 200 1% 1/20W TK 0201-1
NC SOC LPDP DP2HDMI RCAL NEG (PACK_IGNORE=TRUE, PACK_OPTION=LPDP_EXT_RCAL)	C1022 10PF 5% 25V C0G 0201	SOC LPDP INT RCAL NEG (PACK_OPTION=LPDP_INT_RCAL)	C1023 10PF 5% 25V C0G 0201
SOC ST PCIE RCAL POS	R1024 200 1% 1/20W TK 0201-1	SOC GP PCIE RCAL POS	R1025 200 1% 1/20W TK 0201-1
SOC ST PCIE RCAL NEG	C1024 10PF 5% 25V C0G 0201	SOC GP PCIE RCAL NEG	C1025 10PF 5% 25V C0G 0201

Scan for RCAL Info:

B PCIe CLKREQ/PERST Pull-Ups/Downs

PP1V25_AWAKE_IO

R1000	47K 5% 1/20W TK 0201 (117S00129)		WLBT CLKREQ L
R1001	47K 5% 1/20W TK 0201 (117S00129)	PACK_IGNORE=TRUE, PCIE_GP1	NC SOC GP PCIE CLKREQ 1 L
R1002	47K 5% 1/20W TK 0201 (117S00129)	PACK_IGNORE=TRUE, PCIE_GP2	NC SOC GP PCIE CLKREQ 2 L
R1003	47K 5% 1/20W TK 0201 (117S00129)	PACK_IGNORE=TRUE, PCIE_GP3	NC SOC GP PCIE CLKREQ 3 L
R1004	47K 5% 1/20W TK 0201 (117S00129)		NAND0 CLKREQ0 L
R1005	47K 5% 1/20W TK 0201 (117S00129)		NAND0 CLKREQ1 L
R1010	47K 5% 1/20W TK 0201 (117S00129)	PCIE_GP0	WLBT RESET L
R1011	47K 5% 1/20W TK 0201 (117S00129)	PACK_IGNORE=TRUE, PCIE_GP1	NC SOC GP PCIE PERST 1 L
R1012	47K 5% 1/20W TK 0201 (117S00129)	PACK_IGNORE=TRUE, PCIE_GP2	NC SOC GP PCIE PERST 2 L
R1013	47K 5% 1/20W TK 0201 (117S00129)	PACK_IGNORE=TRUE, PCIE_GP3	NC SOC GP PCIE PERST 3 L
R1014	47K 5% 1/20W TK 0201 (117S00129)		NAND0_PCIE_RESET_L

BOM_COST_GROUP=SOC

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE: SOC: LPDP, PCIE

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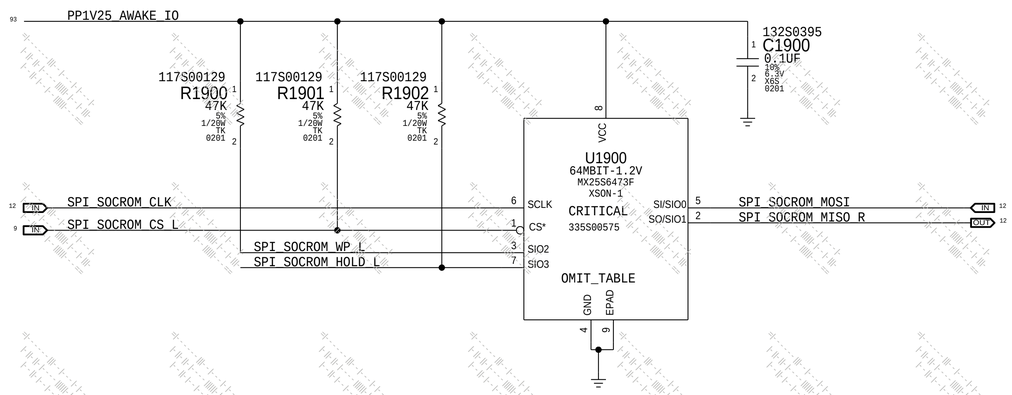
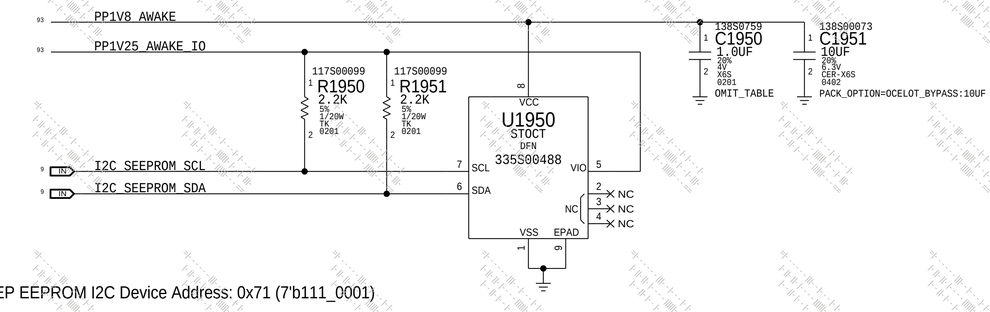
A SPI ROM



B SEP EEPROM



SEP EEPROM I2C Device Address: 0x71 (7'b111_0001)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0759	1	CAP,CER,1UF,20%,4V,X6S,0201	C1950		OCELOT_BYPASS:1UF
132S0395	1	CAP,CER,0.1UF,10%,6.3V,X6S,0201	C1950		OCELOT_BYPASS:100NF

BOM_COST_GROUP=SOC

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE
SOC: SPI NOR, SEP ROM

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A SOC ROM Source Terminations

R2000 20 1% 1/20W TK 0201 118S00467
SPI_SOCROM_MISO (OUT 9) → SPI_SOCROM_MISO_R (IN 11)
PLACE_NEAR=U0600.Y7:10MM

R2001 20 1% 1/20W TK 0201 118S00467
SPI_SOCROM_MOSI_R (IN 9) → SPI_SOCROM_MOSI (OUT 11)
PLACE_NEAR=U0600.V7:10MM

R2002 20 1% 1/20W TK 0201 118S00467
SPI_SOCROM_CLK_R (IN 9) → SPI_SOCROM_CLK (OUT 11)
PLACE_NEAR=U0600.W7:10MM

B TOUCHID Source Terminations

R2004 20 1% 1/20W TK 0201 118S00467
SPI_TOUCHID_MOSI_R (IN 9) → SPI_TOUCHID_MOSI (OUT 85)
PLACE_NEAR=U0600.AB52:10MM

R2005 20 1% 1/20W TK 0201 118S00467
SPI_TOUCHID_CLK_R (IN 9) → SPI_TOUCHID_CLK (OUT 85)
PLACE_NEAR=U0600.AA52:10MM

C IPD Source Terminations

R2006 20 1% 1/20W TK 0201 118S00467
SPI_IPD_MOSI_R (IN 9) → SPI_IPD_MOSI (OUT 86)
PLACE_NEAR=U0600.AJ1:10MM

R2007 20 1% 1/20W TK 0201 118S00467
SPI_IPD_CLK_R (IN 9) → SPI_IPD_CLK (OUT 86)
PLACE_NEAR=U0600.AH2:10MM

D TCON Source Terminations

R2090 20 1% 1/20W TK 0201 118S00467
SPI_TCON_MOSI_R (IN 9) → SPI_TCON_MOSI (OUT 75 90)
PLACE_NEAR=U0600.AH48:10MM

R2091 20 1% 1/20W TK 0201 118S00467
SPI_TCON_CLK_R (IN 9) → SPI_TCON_CLK (OUT 75 90)
PLACE_NEAR=U0600.AH49:10MM

E IMU Source Terminations

SENSOR_IMU
R2008 20 1% 1/20W TK 0201 118S00467
SPI_AOP_GYRO_MOSI_R (IN 8) → SPI_AOP_GYRO_MOSI (OUT 57)
PLACE_NEAR=U0600.V4:10MM

SENSOR_IMU
R2009 20 1% 1/20W TK 0201 118S00467
SPI_AOP_GYRO_CLK_R (IN 8) → SPI_AOP_GYRO_CLK (OUT 57)
PLACE_NEAR=U0600.U3:10MM

F SOC SWD Source Terminations

R2084 20 1% 1/20W TK 0201 118S00467
SWD_SOC_SWCLK_R (IN 7) → SWD_SOC_SWCLK (OUT 62)
PLACE_NEAR=U0600.AR2:10MM

R2085 20 1% 1/20W TK 0201 118S00467
SWD_SOC_SWDIO_R (IN 7) → SWD_SOC_SWDIO (OUT 62)
PLACE_NEAR=U0600.AP1:10MM

G SOC SPMI MPMU Source Terminations

R2060 33 1% 1/20W TK 0201 118S00377
SPMI_NUB_MPMU_CLK_R (IN 8) → SPMI_NUB_MPMU_CLK (OUT 41)
PLACE_NEAR=U0600.AT2:10MM

R2061 33 1% 1/20W TK 0201 118S00377
SPMI_NUB_MPMU_DATA_R (BI 8) → SPMI_NUB_MPMU_DATA (BI 41)
PLACE_NEAR=U0600.AT1:10MM

H SOC SPMI SPMU Source Terminations

R2062 33 1% 1/20W TK 0201 118S00377
SPMI_NUB_SPMU_CLK_R (IN 8) → SPMI_NUB_SPMU_CLK (OUT 35)
PLACE_NEAR=U0600.AM4:10MM

R2063 33 1% 1/20W TK 0201 118S00377
SPMI_NUB_SPMU_DATA_R (BI 8) → SPMI_NUB_SPMU_DATA (BI 35)
PLACE_NEAR=U0600.AL4:10MM

I PMU SWD Series R

R2072 15 1% 1/20W TK 0201 118S00465
SWD_NUB_PMU_SWCLK_R (IN 8) → SWD_NUB_PMU_SWCLK
PLACE_NEAR=U0600.AM3:10MM

R2070 49.9 1% 1/20W TK 0201 118S00309
SWD_NUB_PMU_SWCLK → SWD_NUB_SWCLK_SPMU (OUT 96)
PLACE_NEAR=R2071.1:10MM

R2071 49.9 1% 1/20W TK 0201 118S00309
SWD_NUB_PMU_SWCLK → SWD_NUB_SWCLK_MPMU (OUT 96)
PLACE_NEAR=R2070.1:10MM

R2075 15 1% 1/20W TK 0201 118S00465
SWD_NUB_PMU_SWDIO_R (BI 8) → SWD_NUB_PMU_SWDIO
PLACE_NEAR=U0600.AK3:10MM

R2073 49.9 1% 1/20W TK 0201 118S00309
SWD_NUB_PMU_SWDIO → SWD_NUB_SWDIO_SPMU (BI 96)
PLACE_NEAR=R2074.1:10MM

R2074 49.9 1% 1/20W TK 0201 118S00309
SWD_NUB_PMU_SWDIO → SWD_NUB_SWDIO_MPMU (BI 96)
PLACE_NEAR=R2073.1:10MM

J LAS Source Terminations

R2080 20 1% 1/20W TK 0201 118S00467
SPI_AOP_SENSORS_CLK_R (IN 8) → SPI_AOP_SENSORS_CLK (OUT 85)
PLACE_NEAR=U0600.AN7:10MM

R2081 20 1% 1/20W TK 0201 118S00467
SPI_AOP_SENSORS_MOSI_R (IN 8) → SPI_AOP_SENSORS_MOSI (OUT 85)
PLACE_NEAR=U0600.AM6:10MM

L TDM Source Terminations

R2010 20 1% 1/20W TK 0201 118S00467
TDM_SPKRAMP_L_BCLK_R (IN 9) → TDM_SPKRAMP_L_BCLK
MAKE_BASE=TRUE
PLACE_NEAR=U0600.BD21:10MM
TDM_SPKRAMP_L_BCLK (82)
TDM_SPKRAMP_L_BCLK (82)
TDM_SPKRAMP_L_BCLK (82)

R2011 20 1% 1/20W TK 0201 118S00467
TDM_SPKRAMP_L_R2D_R (IN 9) → TDM_SPKRAMP_L_R2D
MAKE_BASE=TRUE
PLACE_NEAR=U0600.BE21:10MM
TDM_SPKRAMP_L_R2D (82)
TDM_SPKRAMP_L_R2D (82)
TDM_SPKRAMP_L_R2D (82)

R2012 20 1% 1/20W TK 0201 118S00467
TDM_SPKRAMP_L_FSYNC_R (IN 9) → TDM_SPKRAMP_L_FSYNC
MAKE_BASE=TRUE
PLACE_NEAR=U0600.BD20:10MM
TDM_SPKRAMP_L_FSYNC (82)
TDM_SPKRAMP_L_FSYNC (82)
TDM_SPKRAMP_L_FSYNC (82)

R2020 20 1% 1/20W TK 0201 118S00467
TDM_SPKRAMP_R_BCLK_R (IN 9) → TDM_SPKRAMP_R_BCLK
MAKE_BASE=TRUE
PLACE_NEAR=U0600.BD18:10MM
TDM_SPKRAMP_R_BCLK (83)
TDM_SPKRAMP_R_BCLK (83)
TDM_SPKRAMP_R_BCLK (83)

R2021 20 1% 1/20W TK 0201 118S00467
TDM_SPKRAMP_R_R2D_R (IN 9) → TDM_SPKRAMP_R_R2D
MAKE_BASE=TRUE
PLACE_NEAR=U0600.BD15:10MM
TDM_SPKRAMP_R_R2D (83)
TDM_SPKRAMP_R_R2D (83)
TDM_SPKRAMP_R_R2D (83)

R2022 20 1% 1/20W TK 0201 118S00467
TDM_SPKRAMP_R_FSYNC_R (IN 9) → TDM_SPKRAMP_R_FSYNC
MAKE_BASE=TRUE
PLACE_NEAR=U0600.BE15:10MM
TDM_SPKRAMP_R_FSYNC (83)
TDM_SPKRAMP_R_FSYNC (83)
TDM_SPKRAMP_R_FSYNC (83)

R2030 20 1% 1/20W TK 0201 118S00467
TDM_CODEC_BCLK_R (IN 9) → TDM_CODEC_BCLK (OUT 85 90)
PLACE_NEAR=U0600.BF21:10MM

R2031 20 1% 1/20W TK 0201 118S00467
TDM_CODEC_R2D_R (IN 9) → TDM_CODEC_R2D (OUT 85)
PLACE_NEAR=U0600.BF17:10MM

R2032 20 1% 1/20W TK 0201 118S00467
TDM_CODEC_FSYNC_R (IN 9) → TDM_CODEC_FSYNC (OUT 85)
PLACE_NEAR=U0600.BF20:10MM

BOM_COST_GROUP=SOC

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PAGE TITLE: PAGE_TITLE=SOC: SOURCE TERMS

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BRANCH	evt-1
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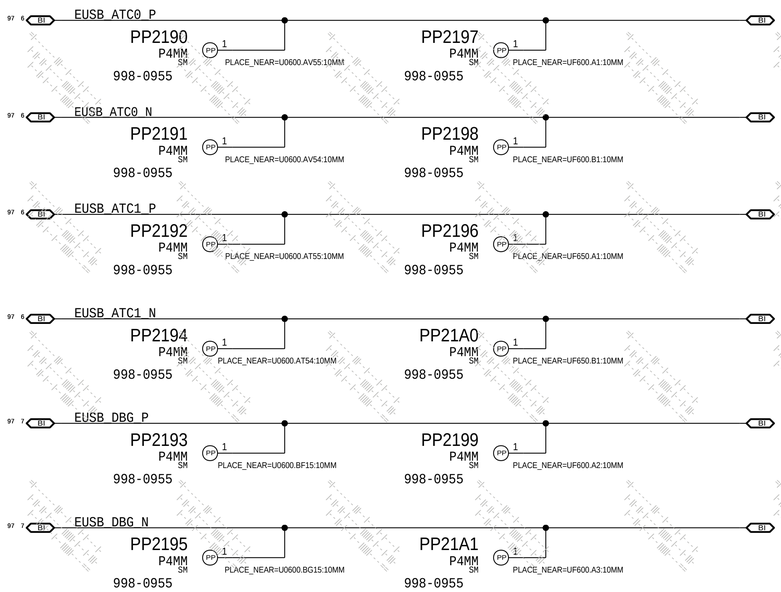
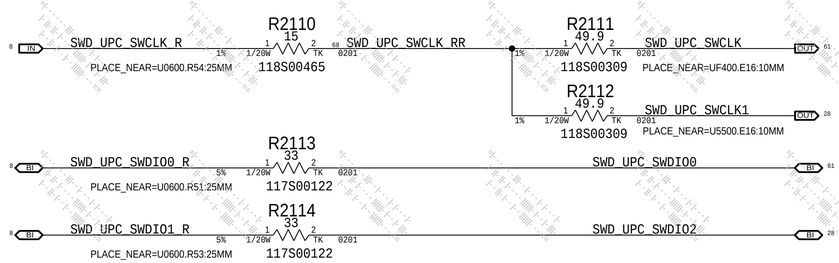
A EUSB Series Resistors & Test Points

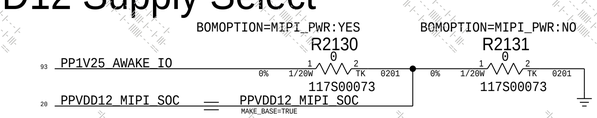


B DMIC Source Term

C UPC SWD Source Term

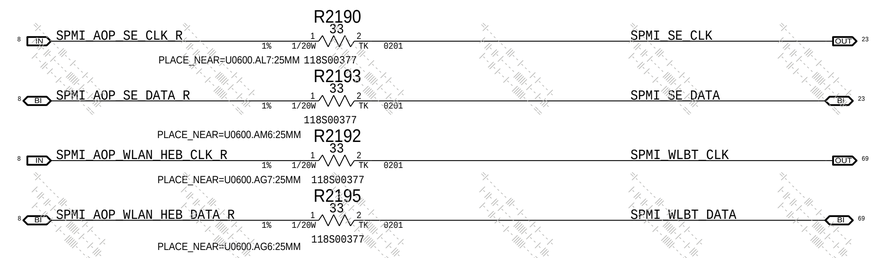


D MIPI PPVDD12 Supply Select

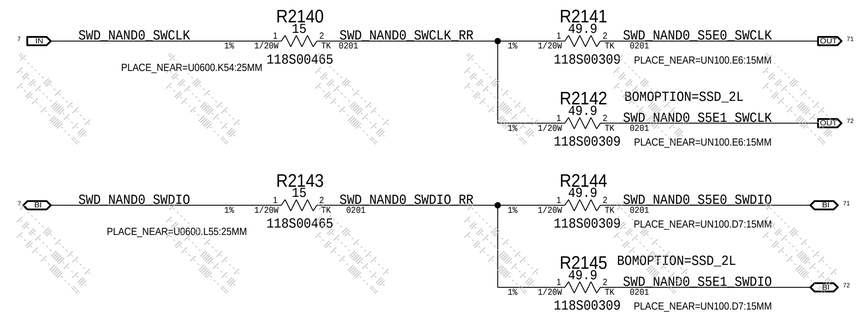


X2203 does not use the MIPI Interface on the SOC Interface
Per Moon Jung Kim (SEG Analog), VDD12_MIPIC and VDD12_MIPID can be tied to GND.

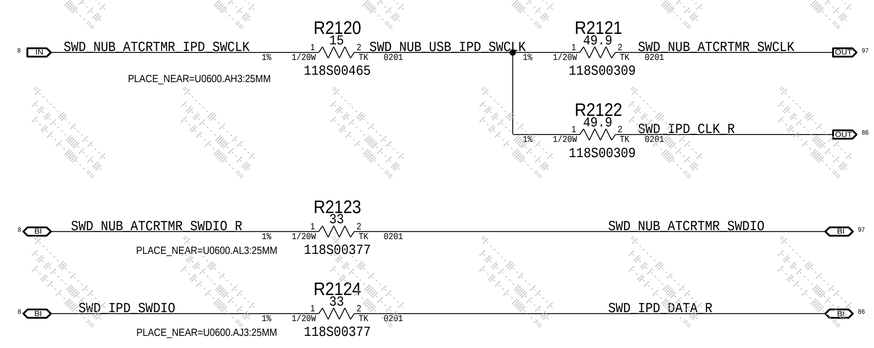
E Secure Element and WiFi SPMU Source Term



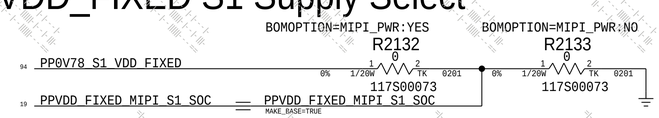
F NAND SWD Source Term



G IPD and ATC SWD Source Term

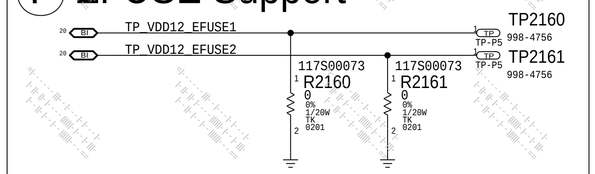


H MIPI PPVDD_FIXED S1 Supply Select



X2203 does not use the MIPI Interface on the SOC Interface
Per Moon Jung Kim (SEG Analog), VDD_FIXED_MIPIC_S1, VDD_FIXED_MIPID_PLL_S1, and VDD_FIXED_MIPID_S1 can be tied to GND.

I EFUSE Support



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PAGE TITLE	PAGE_TITLE=SOC: SOURCE TERMS
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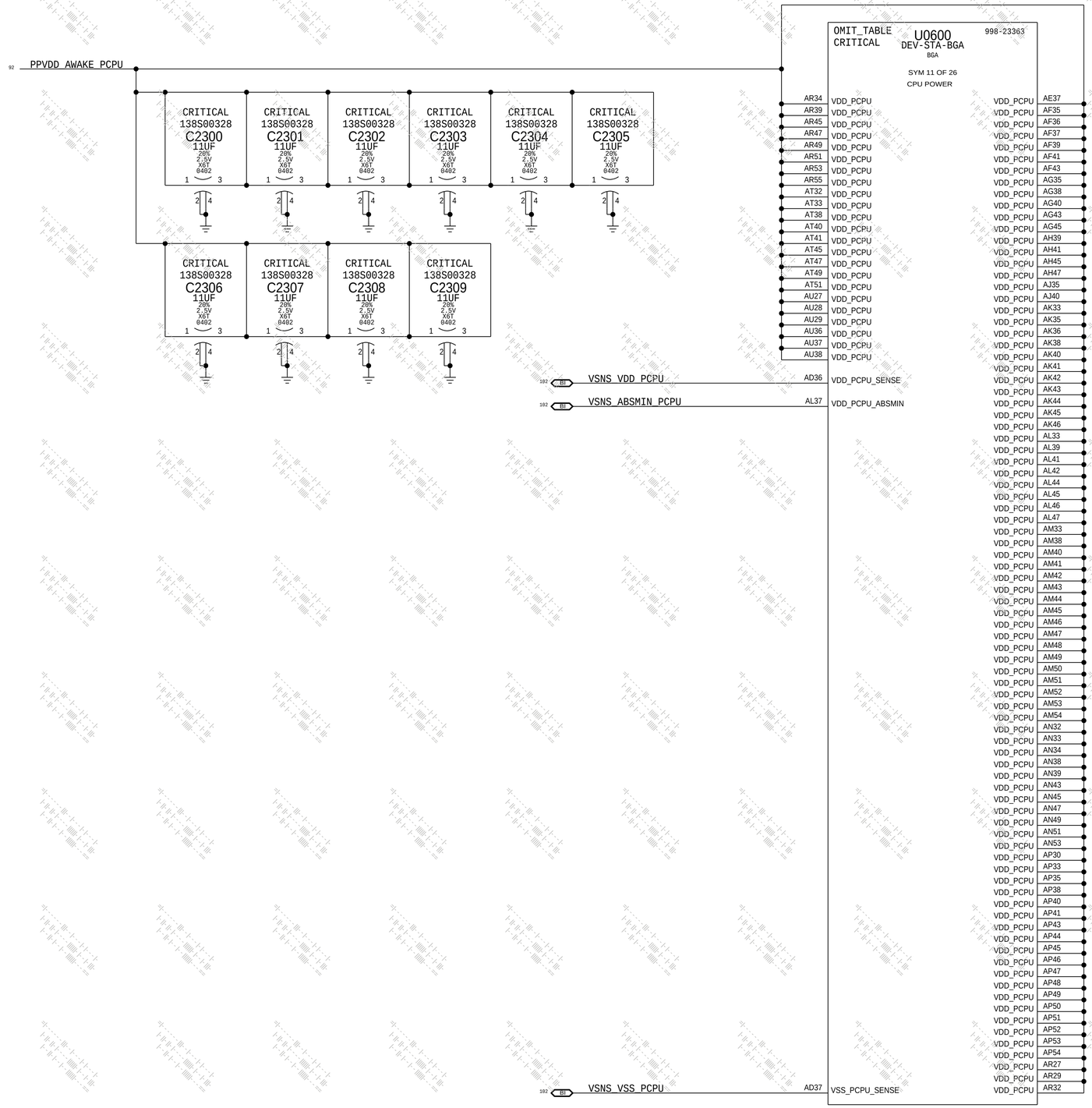
SYNC_DATE=09/28/2021



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SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE

SOC: POWER PCPU

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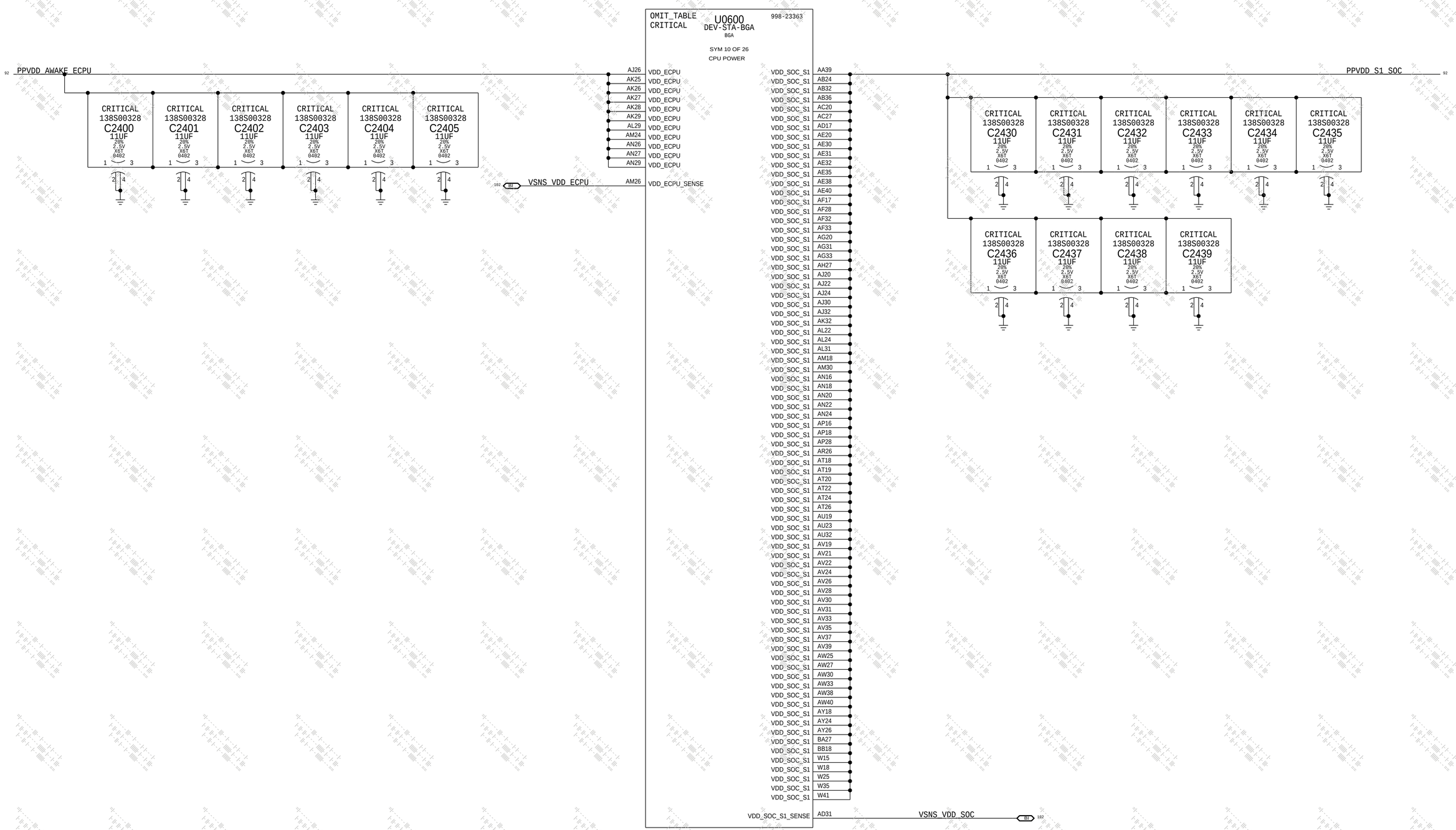

BOM_COST_GROUP=SOC

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE
SOC: POWER ECPU

Apple Inc.

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SHEET 15 OF 113

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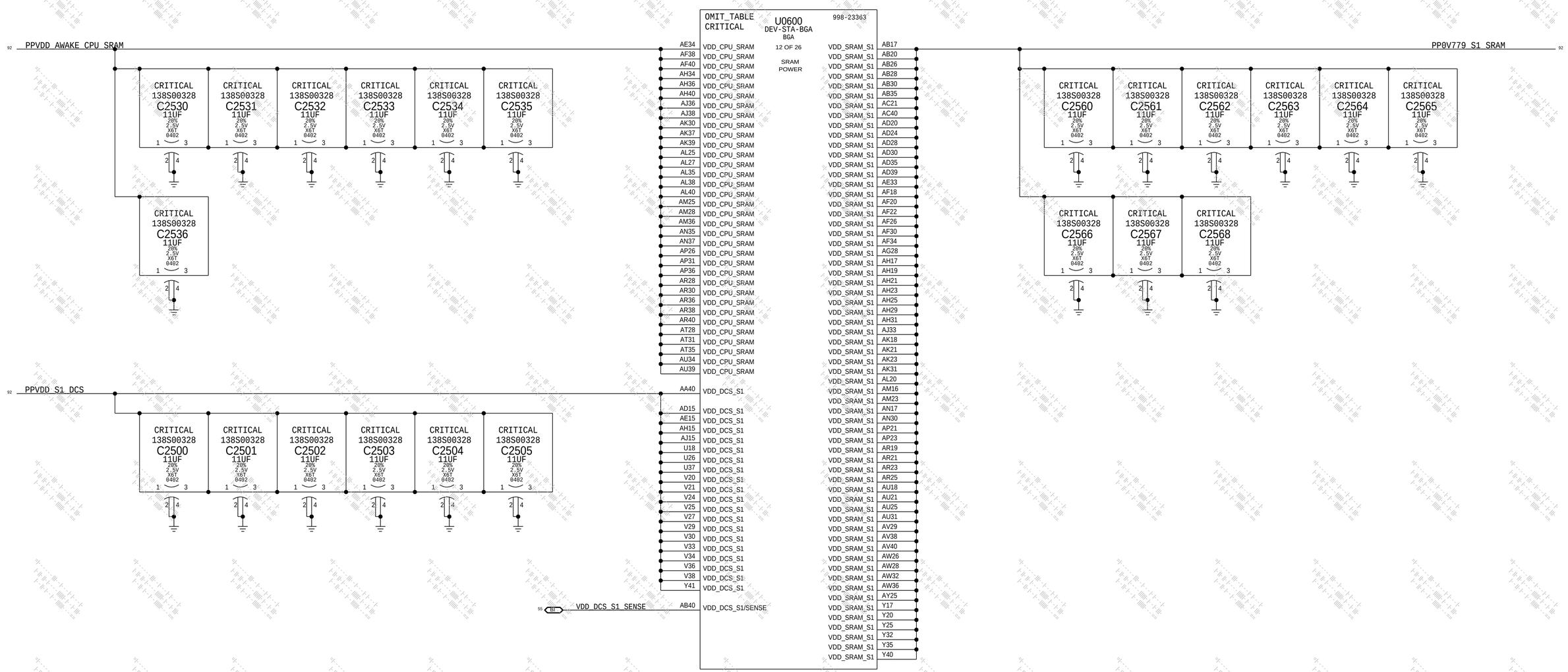

BOM_COST_GROUP=SOC

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE

SOC: POWER SRAM

Apple Inc.

DRAWING NUMBER 051-07020 SIZE D

REVISION 6.0.0

BRANCH evt-1

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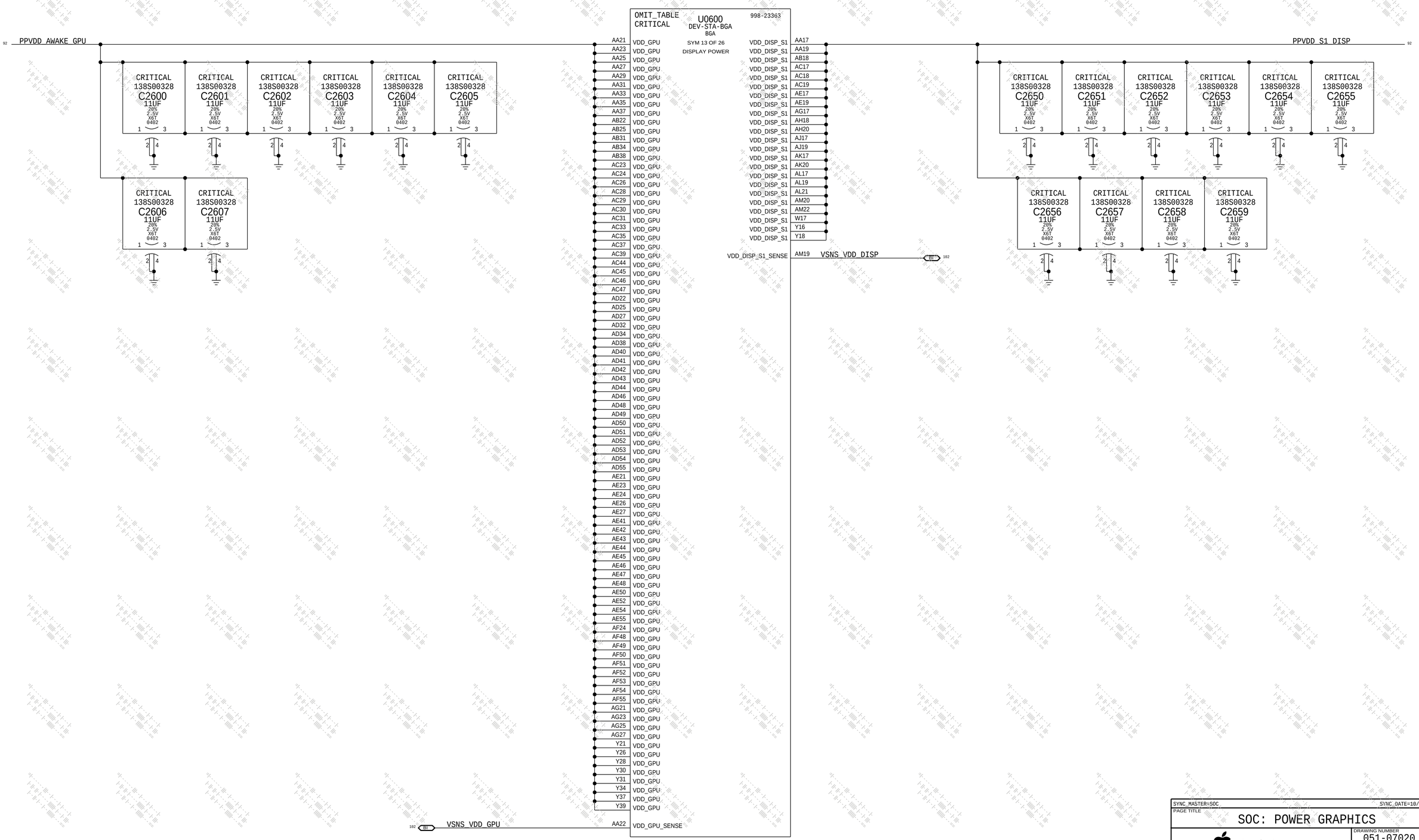

BOM_COST_GROUP=SOC

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE
SOC: POWER GRAPHICS

Apple Inc.

DRAWING NUMBER 051-07020 SIZE D

REVISION 6.0.0

BRANCH evt-1

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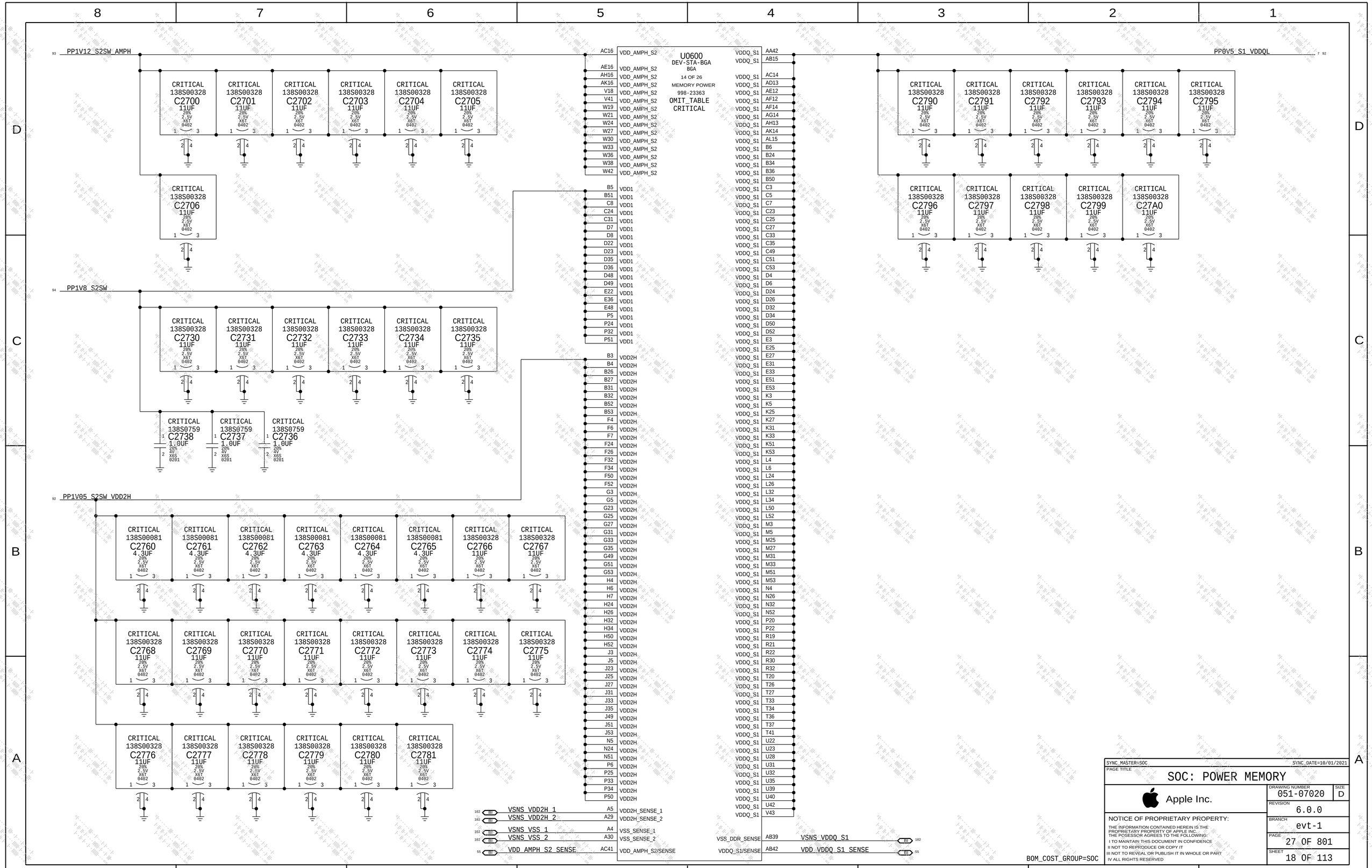
PP1V12_S2SW_AMPH
PP1V8_S2SW
PP1V05_S2SW_VDD2H
PP0V5_S1_VDDQL
U0600
DEV-STA-BGA
BGA
14 OF 26
MEMORY POWER
998-23363
OMIT_TABLE
CRITICAL
VSNS_VDD2H_1
VSNS_VDD2H_2
VSNS_VSS_1
VSNS_VSS_2
VDD_AMPH_S2_SENSE
VSNS_VDDQ_S1
VDD_VDDQ_S1_SENSE
BOM_COST_GROUP=SOC
SYNC_MASTER=SOC
SYNC_DATE=10/01/2021
PAGE TITLE
SOC: POWER MEMORY
Apple Inc.
DRAWING NUMBER
051-07020
SIZE
D
REVISION
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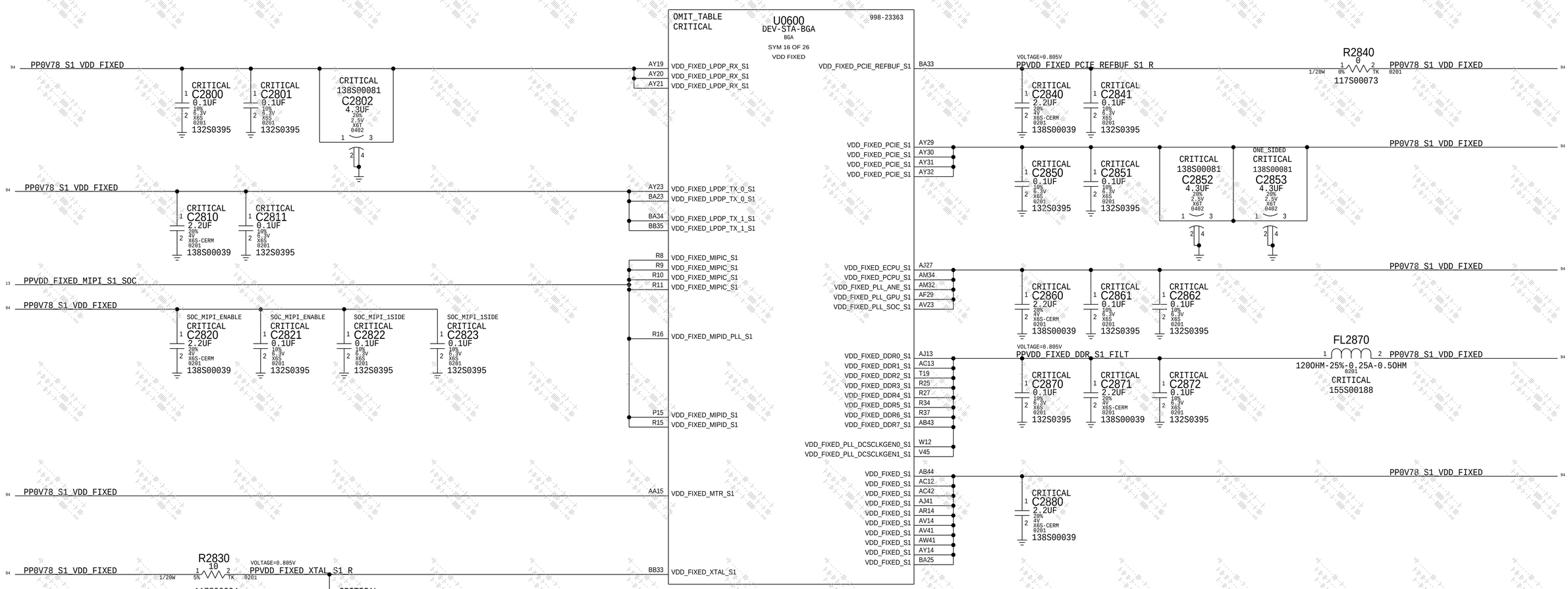

BOM_COST_GROUP=SOC

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE
SOC: POWER FIXED

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DRAWING NUMBER 051-07020 SIZE D

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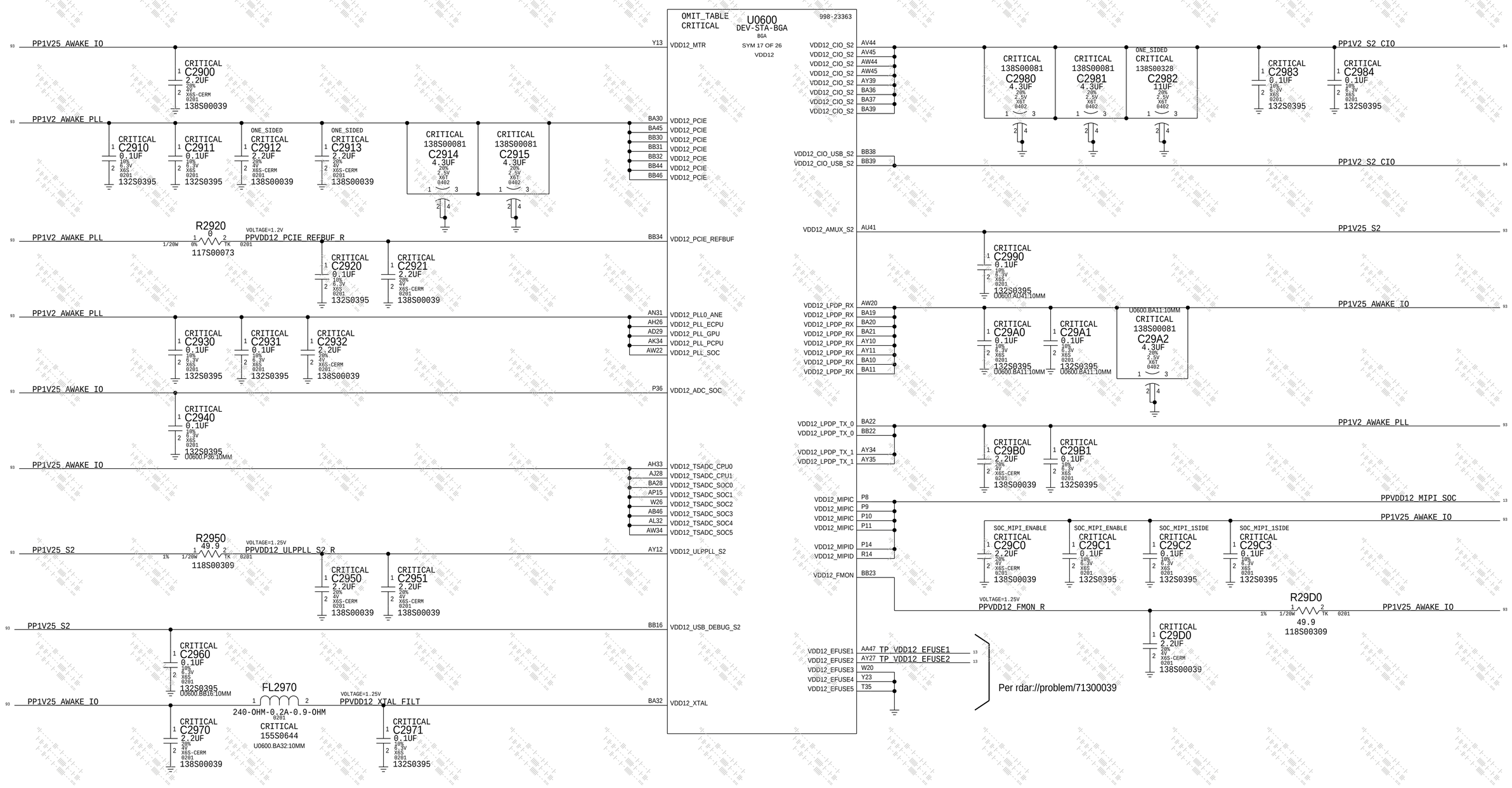

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE

SOC: POWER VDD12

Apple Inc.

DRAWING NUMBER 051-07020 SIZE D

REVISION 6.0.0

BRANCH evt-1

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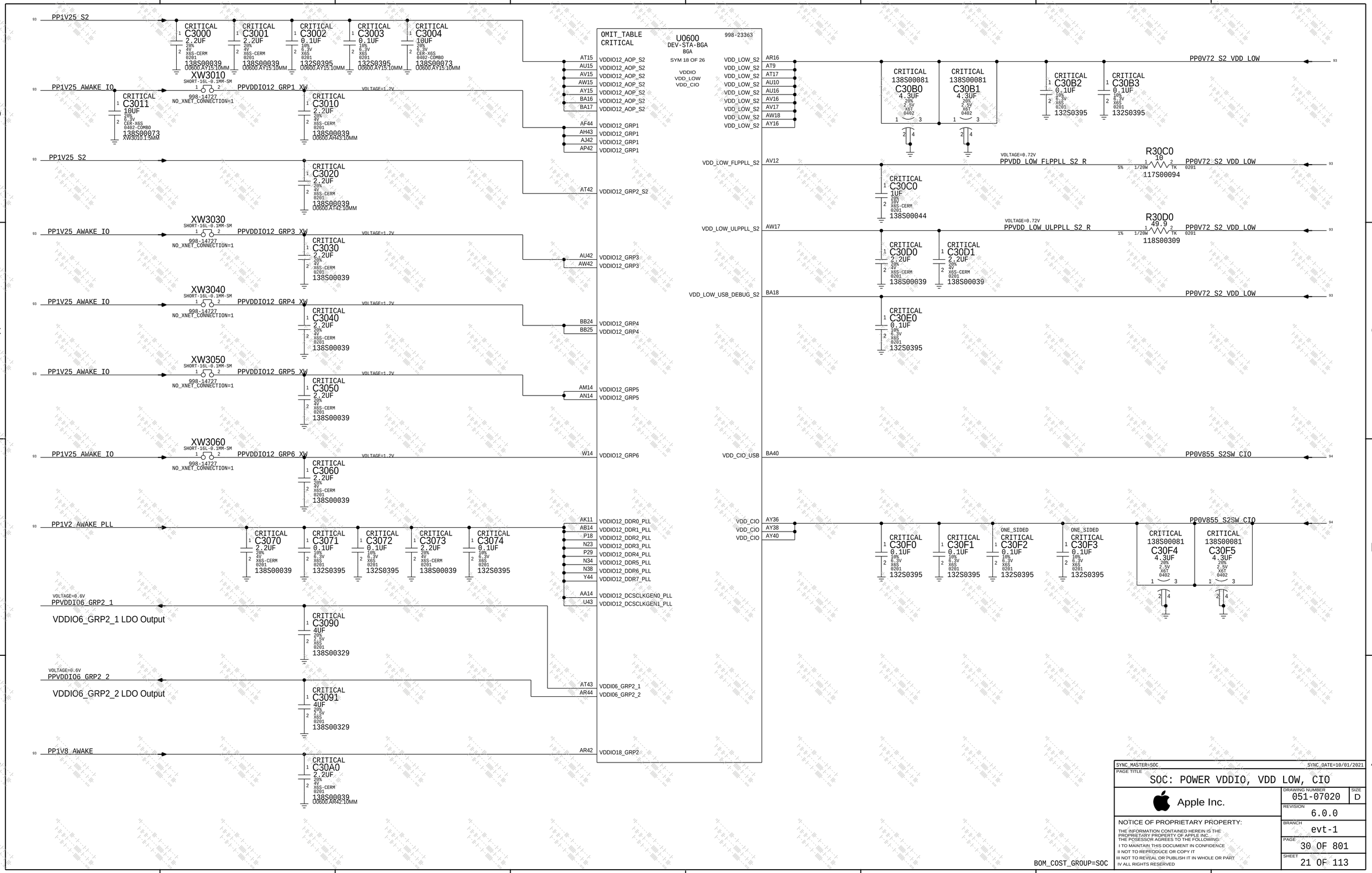
OMIT_TABLE
CRITICAL
U0600
DEV-STA-BGA
BGA
SYM 18 OF 26
998-23363
VDDIO
VDD_LOW
VDD_CIO
PP1V25_S2
PP1V25_AWAKE_IO
PP1V2_AWAKE_PLL
PP1V8_AWAKE
PPVDDIO12_GRP1_XW
PPVDDIO12_GRP3_XW
PPVDDIO12_GRP4_XW
PPVDDIO12_GRP5_XW
PPVDDIO12_GRP6_XW
PPVDDIO6_GRP2_1
PPVDDIO6_GRP2_2
VDDIO6_GRP2_1 LDO Output
VDDIO6_GRP2_2 LDO Output
VDD_LOW_FLPPLL_S2
VDD_LOW_ULPPLL_S2
VDD_LOW_USB_DEBUG_S2
VDD_CIO_USB
PPV72_S2_VDD_LOW
PPVDD_LOW_FLPPLL_S2_R
PPVDD_LOW_ULPPLL_S2_R
PP0V855_S2SW_CIO
R30C0
R30D0
BOM_COST_GROUP=SOC
SYNC_MASTER=SOC
SYNC_DATE=10/01/2021
PAGE TITLE
SOC: POWER VDDIO, VDD LOW, CIO
Apple Inc.
DRAWING NUMBER
051-07020
SIZE
D
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BOM_COST_GROUP=SOC

SYNC_MASTER=SOC SYNC_DATE=10/01/2021

PAGE TITLE

SOC: GND

Apple Inc.

DRAWING NUMBER 051-07020

SIZE D

REVISION 6.0.0

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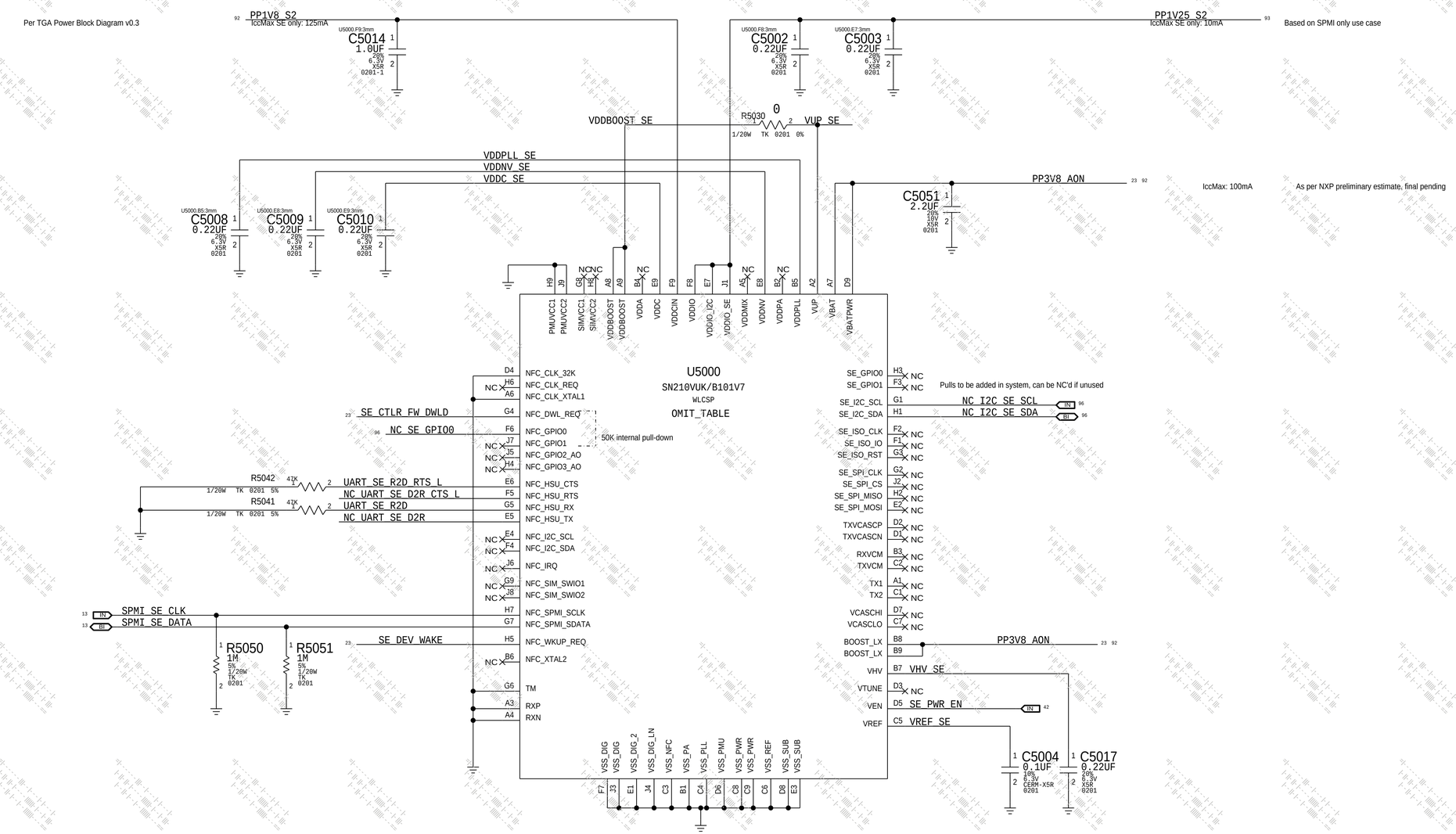
Timing Requirements:
- VBAT supply ramp time: 20ms

Ceres - Secure Element

*** OK2INTEGRATE ***



R5000 47K 1/20W TK 0201 5% — SE_CTLR_FW_DWLD
R5006 47K 1/20W TK 0201 5% — SE_DEV_WAKE

<rdar://problem/52067756> [SN200V] Wired Mode SE Only Reference Design Material
<rdar://problem/45108950> Mac - Venus Reference guide and De-coupling requirements

BOM_COST_GROUP=SECURE ELEMENT

SYNC_MASTER= SYNC_DATE=09/10/2021

PAGE TITLE: Secure Element

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D
REVISION: 6.0.0
BRANCH: evt-1
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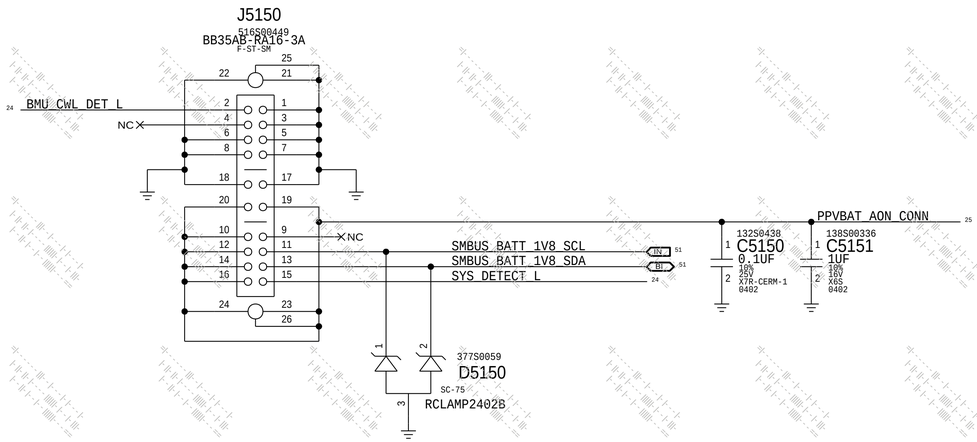
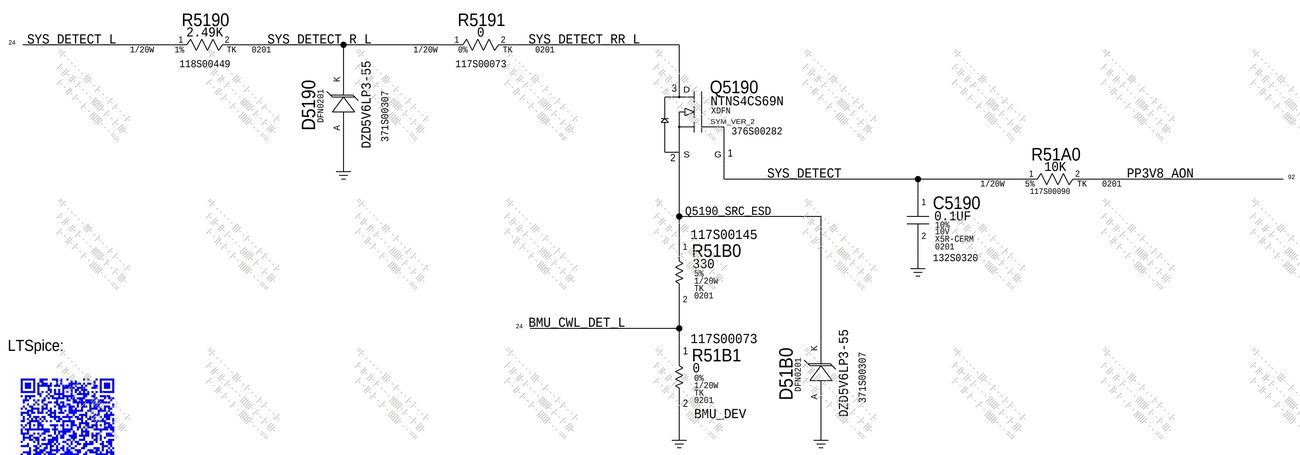
A BMU Connector



B BMU SYS_DETECT Circuit



LTSpice:

$X2203GHUB/mlb/sim/ltspice/bmu_sys_detect/bmu_sys_detect.asc

C BMU SYS_DETECT NOTES

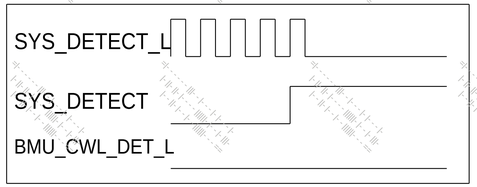
The BMU SYS_DETECT circuit relies on the system assembly in order to be properly enabled. During assembly, a metal gasket is placed between the cowling and the top-side of the BMU flex. The gasket is used to connect the BMU_CWL_DET_L signal, located between J5150.1 and Q5190.2, to GND. Once BMU_CWL_DET_L is tied to GND, then the SYS_DETECT circuit is ready to be enabled.

The BMU VBAT output will be enabled after the BMU flex and cowling are installed and power is supplied by connecting a power adapter to either the USB-C or MagSafe Connectors.

Thus the MLB remains in an unpowered state during system assembly.

Once the MLB is assembled into an enclosure, the BMU SYS_DETECT circuit output, SYS_DETECT_L, is continuously sampled by the Gas Gauge IC at a rate of once per second until it detects a logic low. During the once per second interval, an internal pull-up within the Gas Gauge IC is enabled for 4us to conserve battery charge. Once a logic low is detected, then the BMU enables the VBAT outptu voltage.

Below is an example waveform showing how the BMU SYS_DETECT circuit works.



In the event that the cowling needs to be removed while retaining power to the MLB, resistor R51B1 can be loaded.

BOM_COST_GROUP=BATTERY

PAGE TITLE	BMU Connector
Apple Inc.	DRAWING NUMBER 051-07020 SIZE D
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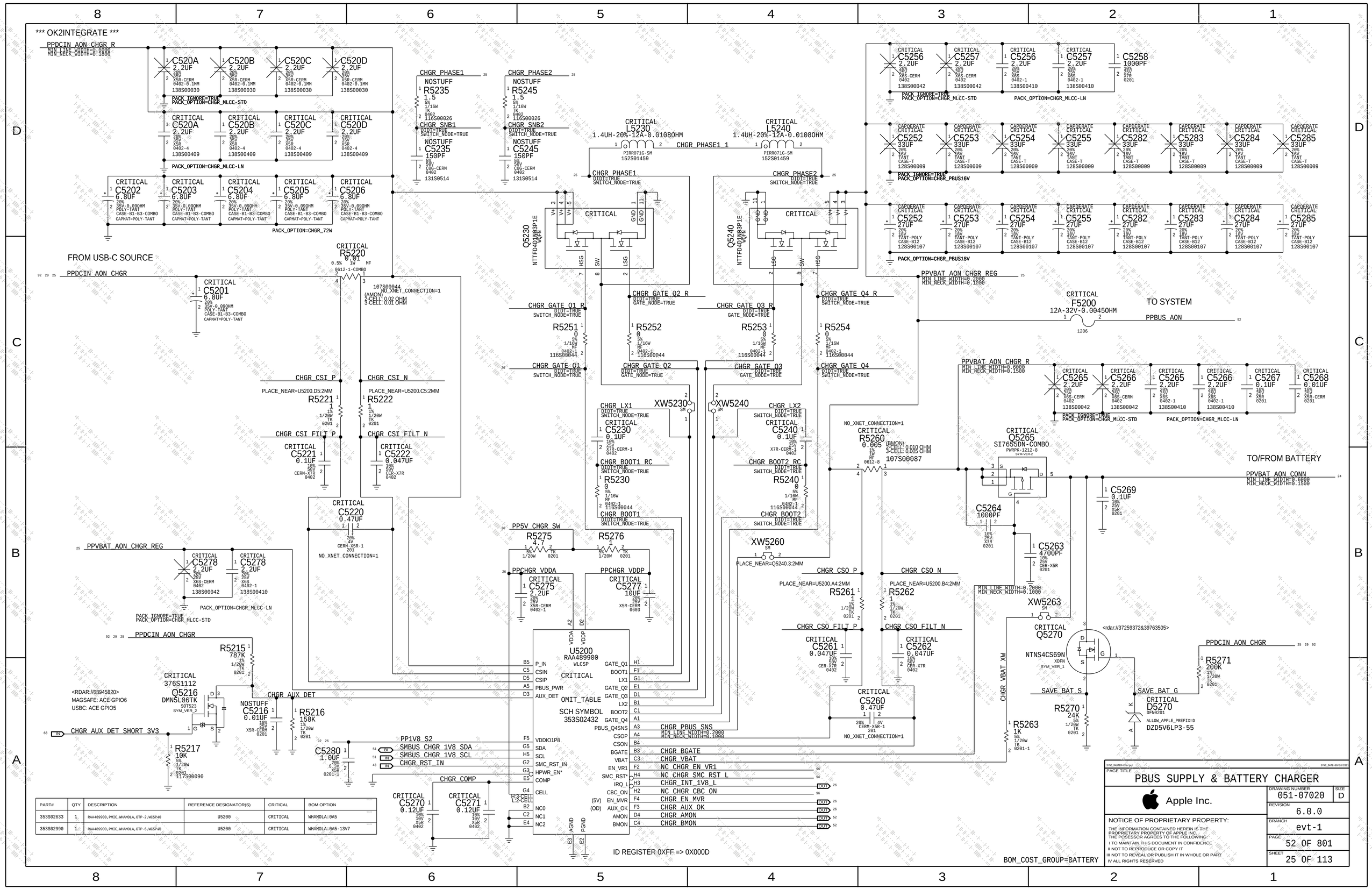


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02633	1	RAA489900,PMIC,WHAMOLA,OTP-2,WCSP40	U5200	CRITICAL	WHAMOLA:0A5
353S02990	1	RAA489900,PMIC,WHAMOLA,OTP-6,WCSP40	U5200	CRITICAL	WHAMOLA:0A5-13V7

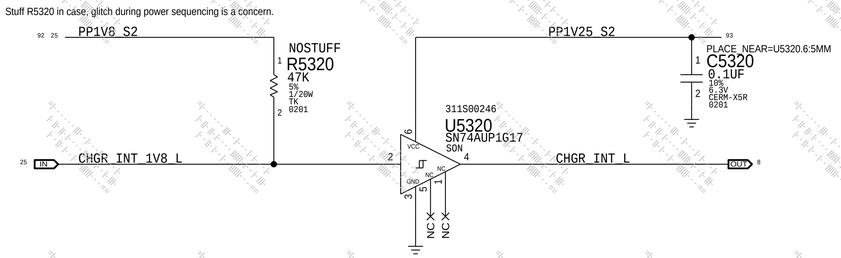
*** OK2INTEGRATE ***

CHGR I2C Level Translation

SMBUS_CHGR_1V8_[SCL/SDA]: Level translation circuit to be placed in project specific I2C page.

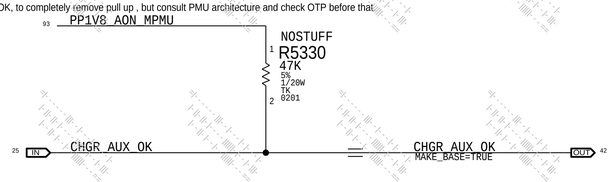
CHGR_INT_L Level Translation

Stuff R5320 in case, glitch during power sequencing is a concern.



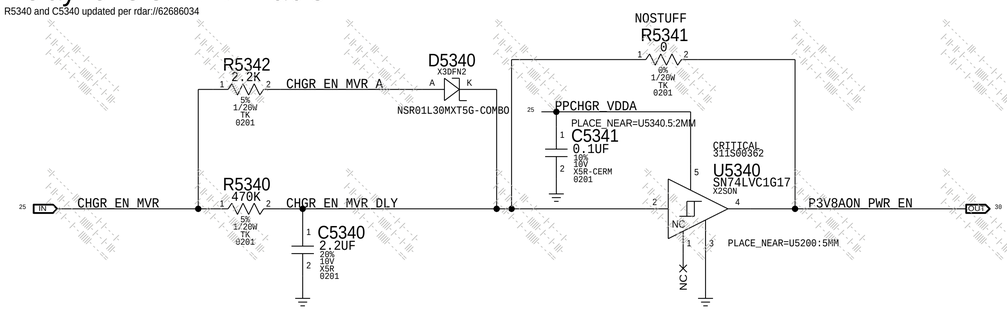
CHGR_AUX_OK Pull Up

Pull up to MPMU LDO9, or rely on MPMU internal pull up,
OK, to completely remove pull up , but consult PMU architecture and check OTP before that

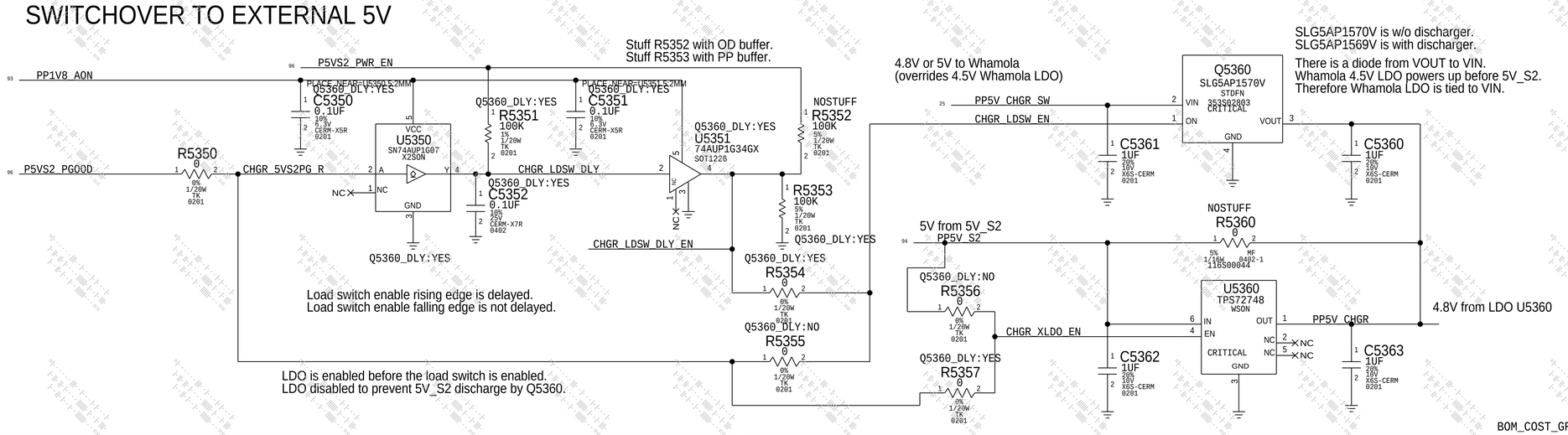


Delay for 3.8V VR Enable

R5340 and C5340 updated per rdar://62686034



SWITCHOVER TO EXTERNAL 5V



SLG5AP1570V is w/o discharger.
SLG5AP1569V is with discharger.

There is a diode from VOUT to VIN.
Whamola 4.5V LDO powers up before 5V_S2.
Therefore Whamola LDO is tied to VIN.

Probe points - bottom

BOM_COST_GROUP=BATTERY

PAGE TITLE	BATTERY CHARGER SUPPORT
Apple Inc.	DRAWING NUMBER 051-07020 SIZE D
	REVISION 6.0.0
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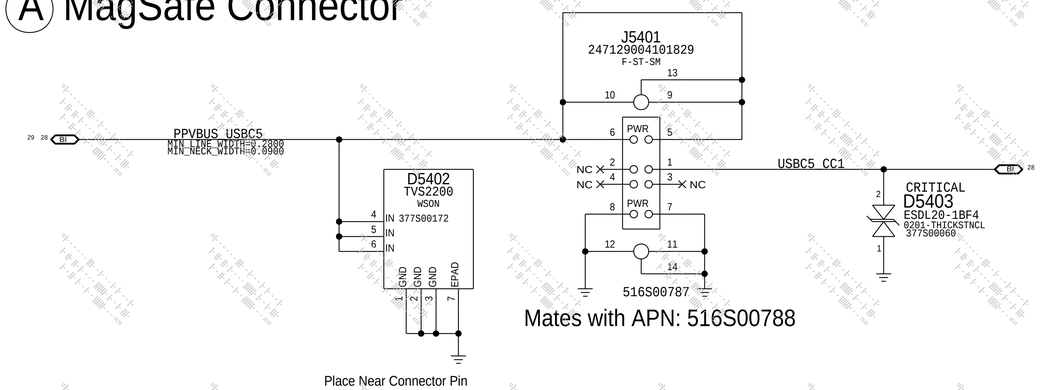
A MagSafe Connector



BOM_COST_GROUP=MAGSAFE

SYNC_MASTER= SYNC_DATE=09/18/2020

PAGE TITLE MAGSAFE: CONNECTOR

Apple Inc.

DRAWING NUMBER 051-07020 SIZE D

REVISION 6.0.0

BRANCH evt-1

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Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)

PPHV_INT5_AONSW

R5502 1/20W 5% 1K 0201-1 MAKE_BASE=TRUE

PD_ACE5_VCONN
PD_ACE5_VCONN

MAX 100uF TOTAL ON RAIL

PPVBUS_USBC5

PLACE_NEAR=U5500.G6:5MM
CRITICAL C5521 2200PF 10% 25V CER-X7R 0201 132500057

PLACE_NEAR=U5500.H5:5MM
CRITICAL C5522 2200PF 10% 25V CER-X7R 0201 132500057

PLACE_NEAR=U5500.J6:5MM
CRITICAL C5523 3300PF 10% 25V CER-X7R 0201 132500343

PLACE_NEAR=U5500.K5:5MM
CRITICAL C5524 3300PF 10% 25V CER-X7R 0201 132500343

PLACE_NEAR=U5500.L6:5MM
CRITICAL C5525 0.01UF 10% 25V X7R 0201 132500070

PLACE_NEAR=U5500.M5:5MM
CRITICAL C5526 0.01UF 10% 25V X7R 0201 132500070

CRITICAL D5501 SDM2U40CSP X3-WLB1608-1

C5501 1UF 10% 35V X5R 0402

PP3V3_UPC5_LDO

R5506 1/20W 5% 100K 0201

R5507 1/20W 5% 10K 0201 UPC5_GPIO2

R5534 1/20W 5% 100K 0201

R5531 1/20W 5% 100K 0201

R5573 1/20W 5% 100K 0201

R5572 1/20W 5% 100K 0201

R5574 1/20W 5% 100K 0201

R5575 1/20W 5% 100K 0201

ACE_WILL_BE_OTPED:NO
84.5k 0201 R5550 1/20W 1% UPC5_I2C_ADDR

R5503 1/20W 0.1% 15K 0201 CRITICAL

ACE_WILL_BE_OTPED:NO
R5510 1/20W 5% 1M 0201 I2C_UPC5_SDA

ACE_WILL_BE_OTPED:YES
R5508 1/20W 5% 1M 0201 CKPLUS_WAIVE=I2C_PULLUP I2C_UPC5_SDA

R5509 1/20W 5% 1M 0201 CKPLUS_WAIVE=I2C_PULLUP I2C_UPC5_SCL

NC_UPC5_RESET_L MAKE_BASE=TRUE

U5500
CD3217B12GACER
FCBGA

CRITICAL
OMIT_TABLE

Pin	Net	Function
B13	PD_UPC5_MRESET	HRESET
A14	NC_UPC5_RESET_L	MRESET
B17		RESET*
A2	UPC5_SER_DBG	GPIO0
B1		GPIO1
D1	UPC5_GPIO1	GPIO2
F1	UPC5_GPIO2	GPIO3
C2	UPC5_GPIO3	GPIO4
E2	UPC5_GPIO4	GPIO5
B3	UPC5_GPIO5	GPIO6
C4	UPC5_GPIO6	GPIO7
D3	UPC5_GPIO7	GPIO8
E4	UPC5_GPIO8	GPIO9
F3	UPC5_GPIO9	GPIO10
F7	UPC5_GPIO10	BUSPOWER
A18	GND	I2C_ADDR (IPU-BOOT)
M19	UPC5_I2C_ADDR	R_OSC
M21	UPC5_R_OSC	I2CM_SDA_CNFG
A16	I2C_UPC5_SDA	I2CM_SCL_CNFG
B15	I2C_UPC5_SCL	I2C_SDA1
B5	I2C_UPC_SDA	I2C_SCL1
A4	I2C_UPC_SCL	I2C_IRQ1*
D7	UPC_I2C_INT_L	I2C_SDA2
B7	I2C_SMC_UPC_SDA	I2C_SCL2
A6	I2C_SMC_UPC_SCL	I2C_IRQ2*
C8	UPC_SMC_I2C_INT_L	SPI_CLK
B9	SPI_UPC5_R_CLK	SPI_MOSI
B11	SPI_UPC5_R_MOSI	SPI_MISO
A10	SPI_UPC5_R_MISO	SPI_SSZ
A8	SPI_UPC5_R_CS_L	SWD_DATA (IPU)
E20	SWD_UPC_SWDIO2	SWD_CLK (IPU)
E16	SWD_UPC_SWCLK1	UART_RX
B19	UART_UPC5	UART_TX
A20	UART_UPC5	USB_RP1_P
H19	PD_UPC5_USB_RP	USB_RP1_N
H21	PD_UPC5_USB_RP	USB_RP2_P
G20	PD_UPC5_USB_RP	USB_RP2_N
G22	PD_UPC5_USB_RP	USB_RP3_P
F19	PD_UPC5_USB_RP	USB_RP3_N
F21	PD_UPC5_USB_RP	AUX_P
J12	PD_UPC5_PORT_MUX	AUX_N
H11	PD_UPC5_PORT_MUX	HPD
C12	ROM_UPC5_WP_L	DEBUG0
G12	PD_UPC5_DBG_R	DEBUG1
F11	PD_UPC5_DBG_R	DEBUG2
E8	PD_UPC5_DBG_R	DEBUG3
E12	PD_UPC5_DBG_R	DEBUG4
G16	PD_UPC5_DBG_R	DEBUG5
F15	PD_UPC5_DBG_R	DEBUG6
D15	PD_UPC5_DBG_R	DEBUG7
D19	PD_UPC5_DBG_R	

DIGITAL CORE I/O & CONTROL

TYPE-C

PORT_MUX

POWER

GND

Pin	Net	Function
C20	PP3V3_S2_LDO	VIN_3V3
A12	PP1V25_S2	VDDIO
D11	GND	VDDIO_CFG
C22, D21	PP3V3_UPC5_LDO	LDO_3V3
L20	UPC5_LV	VIN_LV
L18		VOUT_LV
C16		VRET
L22	UPC5_SS	SS
E22	PP1V5_UPC5_LDO_CORE	LDO_CORE
D5	PPVBUS_USBC5	VBUS_OPT
F5	PPHV_INT5_AONSW	PP_HV_OPT
M15	USBC5_CC1	C_CC1
N16		
M17	USBC5_CC2	C_CC2
N18		
L14	USBC5_CC1	RPD_G1
L16	GND	RPD_G2
K19	PD_UPC5_USB2	C_USB_TP
K21	PD_UPC5_USB2	C_USB_TN
J20	PD_UPC5_USB2	C_USB_BP
J22	PD_UPC5_USB2	C_USB_BN
J16	PD_UPC5_USB2	C_SBU1
H15	PD_UPC5_USB2	C_SBU2
C18	GND_OPT	
E18	GND_OPT	
D17	GND_OPT	
G18	GND_OPT	

MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.0850

R5501 1K 5% 1/20W 1K 0201-1

C5508 10UF 20% 6.3V CERM 0402

C5502 1.0UF 20% 6.3V X5R 0201-1

C5500 10UF 20% 6.3V CERM 0402

C5505 10UF 20% 6.3V CERM 0402

C5509 0.68UF 5% 6.3V X5S 0402

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

NOSTUFF C5514 220PF 5% 50V C0G 0201-1

C5513 220PF 5% 50V C0G 0201-1

R5579 100K 5% 1/20W 1K 0201

Configured as UPC5 (the 6th slot)

ACE_WILL_BE_OTPED:YES (POR)
If Ace can be OTPed
before installing bundle.
(ICT station is ready)

I2C_ADDR=Float
I2CM_SCL_CNFG=HIGH
I2CM_SDA_CNF=LOW

ACE_WILL_BE_OTPED:NO
Like in P0, Or EE bring up
Prevents I2C Conflict with
Other Aces before OTP

I2C_ADDR=84.5K PD
I2CM_SCL_CNFG=HIGH
I2CM_SDA_CNFG=HIGH

R5505 1/20W 5% 1M 0201 UART_UPC5

R5577 1/20W 5% 100K 0201

R5578 1/20W 5% 100K 0201

R5576 1/20W 5% 100K 0201

SPI ROM

PP3V3_UPC5_LDO

R5560 3.3K 1/20W 5% 0201

NOSTUFF R5561 3.3K 1/20W 5% 0201

R5563 3.3K 1/20W 5% 0201

R5562 3.3K 1/20W 5% 0201

C5560 1UF 10% 6.3V CERM 402

U5560
8MBIT-3.0V
W25Q80DVUXIE
USON
OMIT_TABLE
CRITICAL

VCC, CLK, CS*, WP*(IO2), HOLD*(IO3), DI(IO0), DO(IO1), GND, EPAD

R5564 3.3K 1/20W 5% 0201

R5565 15 1/20W 5% 0201 SPI_UPC5_R_MOSI

R5566 15 1/20W 5% 0201 SPI_UPC5_R_MISO

NOSTUFF R5567 47K 1/20W 5% 0201

DISABLING BOOTING FROM SPI

R5568 15 1/20W 5% 0201 SPI_UPC5_R_CLK

R5569 15 1/20W 5% 0201 SPI_UPC5_R_CS_L

AARDVARKANOID CONN

APN 516S00115

USBC_DBG

J5502
505070-1222
PACK_TYPE=M-ST-SM
PACK_IGNORE=TRUE
PACK_OPTION=MAGSAFE_ACE_UPC_DBG:SMALL

Pin	Net	Pin	Net
13		14	
1	PP1V25_S2	2	SPI_UPC5_CS_L
3	SWD_UPC_SWDIO2	4	SPI_UPC5_CLK
5	SWD_UPC_SWCLK1	6	SPI_UPC5_MOSI
7	SPI_UPC5_MISO	8	UPC5_SER_DBG
9	I2C_UPC01_3V3_SDA	10	NC_MAGSAFE_ACE_DEB_CON_10
11	I2C_UPC01_3V3_SCL	12	NC
15		16	

BOM_COST_GROUP=MAGSAFE

PAGE TITLE
MAGSAFE: PORT CONTROLLER

Apple Inc.

DRAWING NUMBER 051-07020
SIZE D
REVISION 6.0.0
BRANCH evt-1
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SHEET 28 OF 113

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A 20V Aliases

POWER ALIASES

28 BI PPVBUS_USBC5 — PPVBUS_USBC5 (MAKE_BASE=TRUE) BI 27 28

GPIOs

28 BI UPC5_GPIO1 — 100K 0201 1K 117S00095 2 1 5% 1/20W R5602

28 BI UPC5_GPIO5 — 100K 0201 1K 117S00095 2 1 5% 1/20W R5603

DEBUG PORT

28 BI NC_MAGSAFE_ACE_DEB_CON_10 — NC_MAGSAFE_ACE_DEB_CON_10 (MAKE_BASE=TRUE)

B Power/Fuse for UPC5

28 BI PPHV_INT5_AONSW — PPHV_INT5_AONSW (MAKE_BASE=TRUE) 0603-1 2 CRITICAL 6A-32V 1 F5601 740S00053 PPDCIN_AON_CHGR (PLACE_NEAR=U5500:5MM) BI 29

28 BI PPHV_INT5_AONSW

MAX 100uF TOTAL ON RAIL

C I2C Aliases

68 51 8 IN I2C_SMC_UPC_SCL — CKPLUS_WAIVE=I2C_PULLUP — MAKE_BASE=TRUE — I2C_SMC_UPC_SCL OUT 28

68 51 8 BI I2C_SMC_UPC_SDA — CKPLUS_WAIVE=I2C_PULLUP — MAKE_BASE=TRUE — I2C_SMC_UPC_SDA BI 28

68 49 9 IN I2C_UPC_SCL — CKPLUS_WAIVE=I2C_PULLUP — MAKE_BASE=TRUE — I2C_UPC_SCL OUT 28

68 49 9 BI I2C_UPC_SDA — CKPLUS_WAIVE=I2C_PULLUP — MAKE_BASE=TRUE — I2C_UPC_SDA BI 28

68 49 8 OUT UPC_I2C_INT_L — CKPLUS_WAIVE=I2C_PULLUP — MAKE_BASE=TRUE — UPC_I2C_INT_L IN 28

68 51 8 OUT UPC_SMC_I2C_INT_L — CKPLUS_WAIVE=I2C_PULLUP — MAKE_BASE=TRUE — UPC_SMC_I2C_INT_L IN 28

D Charger Aliases

92 25 BI PPDCIN_AON_CHGR — PPDCIN_AON_CHGR BI 29

BI PPDCIN_AON_CHGR — MAKE_BASE=TRUE

BOM_COST_GROUP=MAGSAFE

PAGE TITLE	MAGSAFE: CONTROLLER SUPPORT
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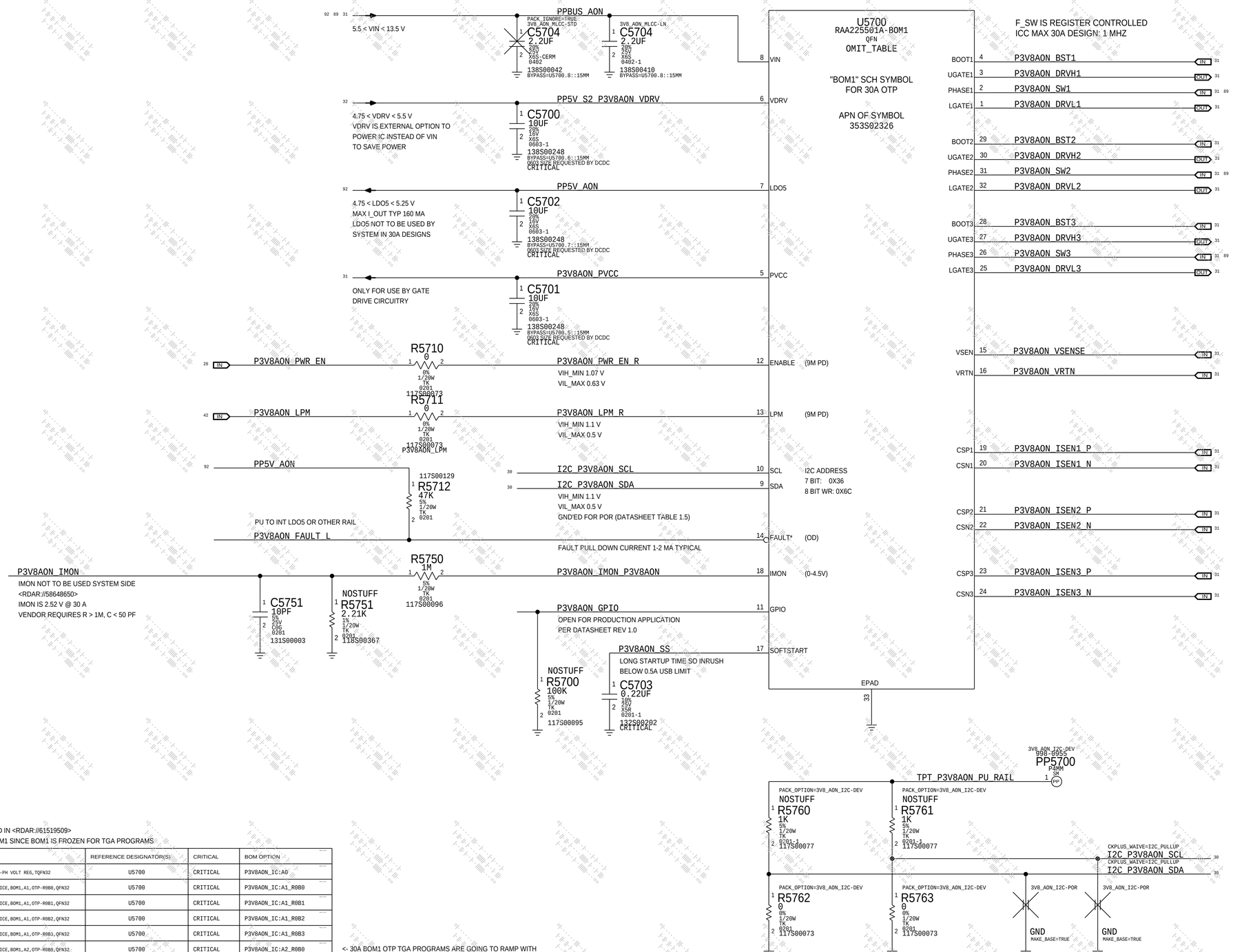
3V8 AON CONTROLLER
30A ICC MAX



30A OTP CHANGES DOCUMENTED IN <RDAR://61519509>

BOM5 IS A CONTINUATION OF BOM1 SINCE BOM1 IS FROZEN FOR TGA PROGRAMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
353S02326	1	IC,RAA225501,3-PH VOLT REG,TQFN32	U5700	CRITICAL	P3V8AON_IC:A0	
353S02472	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B0,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B0	
353S02544	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B1,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B1	
353S02560	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B2,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B2	
353S02576	1	IC,RAA225501B,ICE,BOM1,A1,OTP-R0B3,QFN32	U5700	CRITICAL	P3V8AON_IC:A1_R0B3	
353S02592	1	IC,RAA225501B,ICE,BOM1,A2,OTP-R0B0,QFN32	U5700	CRITICAL	P3V8AON_IC:A2_R0B0	<- 30A BOM1 OTP TGA PROGRAMS ARE GOING TO RAMP WITH
353S02645	1	IC,RAA225501C,ICE,BOM5,A2,OTP-R170,QFN32	U5700	CRITICAL	P3V8AON_IC:A2_R170	<- NEW BOM5 OTP FOR FUTURE PROGRAMS

SYNC_MASTER=MainVR SYNC_DATE=10/01/2021

PAGE TITLE: POWER: 3V8 AON (1/2)

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REVISION: 6.0.0

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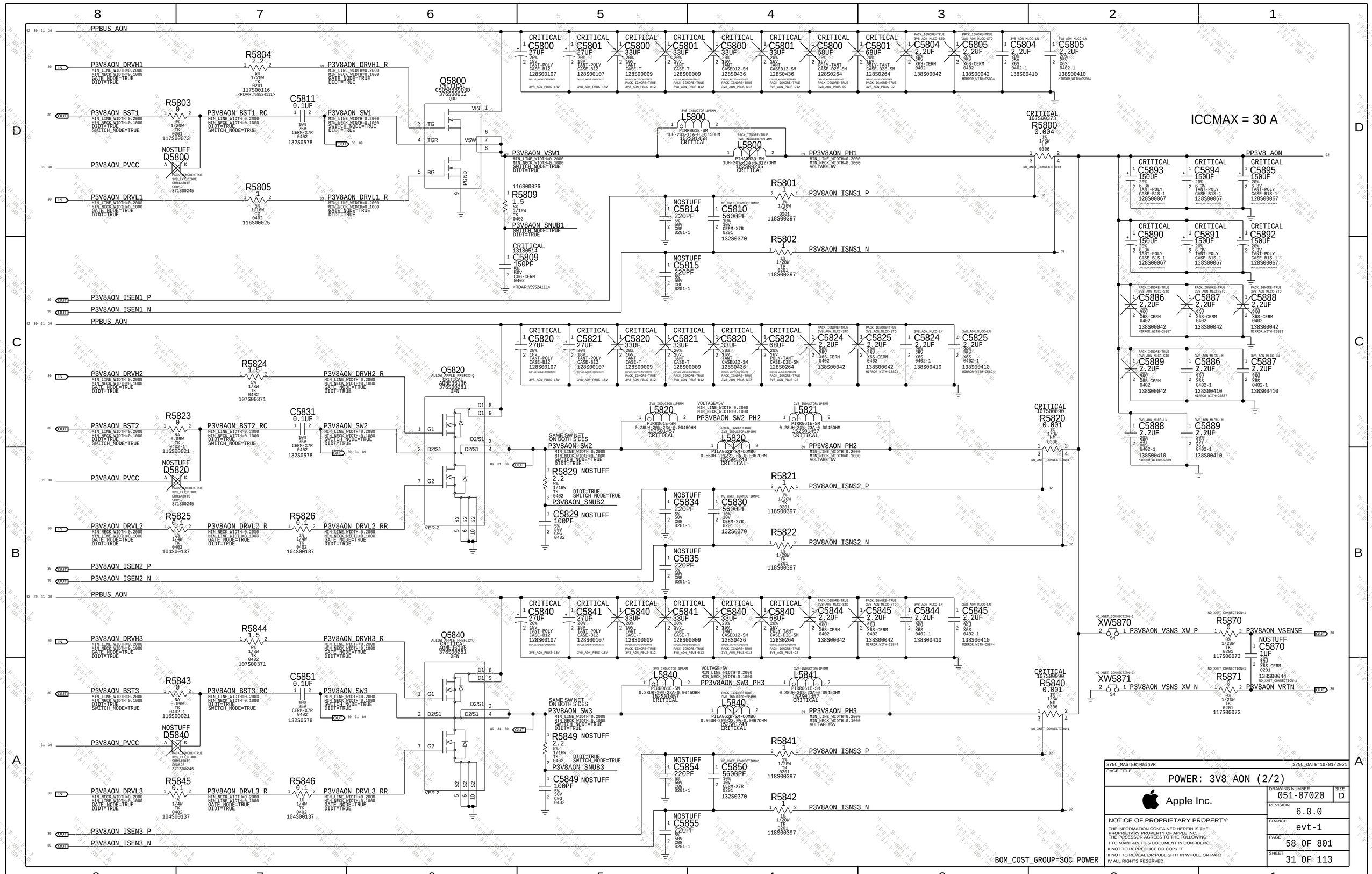

SYNC_MASTER=MainVR SYNC_DATE=10/01/2021

PAGE TITLE

POWER: 3V8 AON (2/2)

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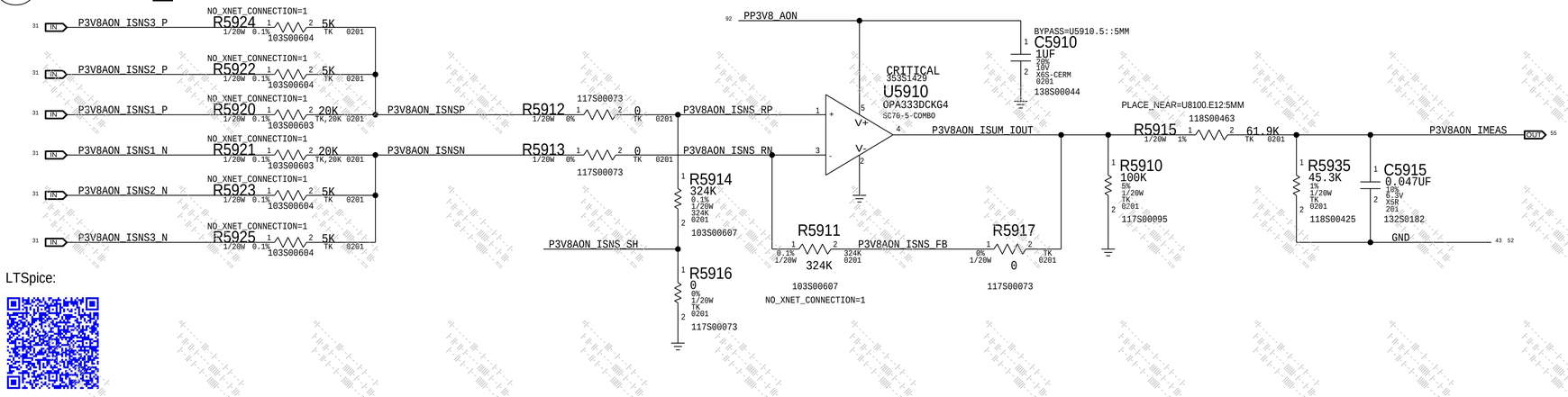
A PP3V8_AON Current Sense



LTSpice:

$X2203GHUB/mlb/sim/ltspice/pp3v8_aon_vddmain/pp3v8_aon_vddmain_current_sense.asc

B PP5V_S2 to PP3V8_AON VDRV Connection

BOM_COST_GROUP=SOC POWER

SYNC_MASTER=jawt50 SYNC_DATE=09/28/2021

PAGE TITLE: POWER: 3V8 AON SUPPORT

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*** OK2INTEGRATE ***

OMIT_TABLE
998-23585

U7700
VALE
CSP
SYM 1 OF 4

VOLTAGE INPUTS
SENSE
BUCK OUTPUTS

PP3V8_AON

PP0V779_S1_SRAM

PP2V58_AWAKE_NAND_VCC

PPVDD_S1_DISP

PP0V5_S1_VDDQL

PP0V88_S1

PP1V12_S2SW_AMPH

PP5V_SPMU_BSTLQ_XW

PP5V_SPMU_BSTLQ

BOM_COST_GROUP=SOC POWER

SYNC_MASTER=MPMU_SPMU SYNC_DATE=10/01/2021

PAGE TITLE
SPMU: INPUT PWR, BULK, BSTLQ

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OMIT_TABLE
998-23585

U7700
VALE
CSP
SYM 2 OF 4

92	PP3V8_AON	M8	VDD_CTRL_LDOG	VLDO4	P7	PP0V72_S2_VDD_LOW	93
92	PP3V8_AON	A1	VDD_BOOST_LDO	VLDO6	D3	NC_SPMU_VLDO6	93
		A2	VDD_BOOST_LDO				
		A3	VDD_BOOST_LDO	VLDO9	D1	PP1V8_AON_SPMU	94
92	PP3V8_AON	C1	VDD_MAIN_LDO	VLDO9B	B1	PP1V2_AON_SPMU	94
		C2	VDD_MAIN_LDO				
		C3	VDD_MAIN_LDO	VLDO12	P8	PP0V78_S1_VDD_FIXED	94
92	PP3V8_AON	A4	VDD_LDO15	VLDO15	B4	NC_SPMU_VLDO15	94
93 34	PP1V25_S2	N7	VDD_LDO4	VLDO17	B2	NC_SPMU_VLDO17	94
92	PP0V88_S1	N8	VDD_LDO12	VLDO18	B3	NC_SPMU_VLDO18	94
				VLDOINT	D2	PP1V5_LDOINT_SPMU	94
92 34	PP1V8_S2	M13	VDD_SW4	VSW4	M14	PP1V8_AWAKE_SPMU_GPIO	34 93
93 34	PP1V25_S2	P13	VDD_SW5	VSW5	N13	PP1V25_AWAKE_NAND_VCCQ	34 93
		P14	VDD_SW5	VSW5	N14		
92 34	PP0V88_S1	P12	VDD_SW6	VSW6	P11	PP0V88_AWAKE_NAND_VDD	34 93
92	PP0V88_S1	P10	VDD_SW7	VSW7	P9		

LDO INPUTS

LDO OUTPUTS

LOAD SWITCHES

LDO4	300MA MAX
LDO6	50MA MAX
LDO9	10MA MAX
LDO9B	10MA MAX
LDO12	850MA MAX
LDO15	100MA MAX
LDO17	250MA MAX
LDO18	250MA MAX
LDOINT	150MA MAX
VSW4	200MA MAX, 125MOHM MAX
VSW5	890MA MAX, 23MOHM MAX
VSW6	150MA MAX, 23MOHM MAX
VSW7	820MA MAX, 23MOHM MAX

VDD_LDO4
DECOUPLING SHARED WITH J10 (VDDIO_1V2)

PP1V25_S2
- CRITICAL 138S00073 C7820 10UF 20% 6.3V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C7821 10UF 20% 6.3V CER-X6S 0402-COMBO

VLDO4
PP0V72_S2_VDD_LOW
- CRITICAL 138S00073 C7840 10UF 20% 6.3V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C7841 10UF 20% 6.3V CER-X6S 0402-COMBO

VLDO12
PP0V78_S1_VDD_FIXED
- CRITICAL 138S00073 C78C0 10UF 20% 6.3V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C78C1 10UF 20% 6.3V CER-X6S 0402-COMBO

VDD_SW4
DECOUPLING SHARED WITH H10 (VDDIO_1V8)

PP1V8_S2
- CRITICAL 138S00073 C7830 10UF 20% 6.3V CER-X6S 0402-COMBO

VSW4
PP1V8_AWAKE_SPMU_GPIO
- CRITICAL 138S00044 C7850 1UF 20% 16V X6S-CERM 0201

VLDO9
PP1V8_AON_SPMU
- CRITICAL 138S00073 C7890 10UF 20% 6.3V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C7891 10UF 20% 6.3V CER-X6S 0402-COMBO

VLDOINT
PP1V5_LDOINT_SPMU
- CRITICAL 138S00073 C7810 10UF 20% 6.3V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C7811 10UF 20% 6.3V CER-X6S 0402-COMBO

VDD_SW5
DECOUPLING SHARED WITH J10 (VDDIO_1V2)

PP1V25_S2
- CRITICAL 138S00073 C7822 10UF 20% 6.3V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C7823 10UF 20% 6.3V CER-X6S 0402-COMBO

VSW5
PP1V25_AWAKE_NAND_VCCQ
- CRITICAL 138S00073 C7860 10UF 20% 6.3V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C7861 10UF 20% 6.3V CER-X6S 0402-COMBO

VLDO9B
PP1V2_AON_SPMU
- CRITICAL 138S00073 C78A0 10UF 20% 6.3V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C78A1 10UF 20% 6.3V CER-X6S 0402-COMBO

UN-UNUSED LDOS
LDO 6, 15, 17, 18

VDD_SW6/7
DECOUPLING SHARED VDD_LDO12

PP0V88_S1
- CRITICAL 138S00073 C7831 10UF 20% 6.3V CER-X6S 0402-COMBO

VSW6/7
PP0V88_AWAKE_NAND_VDD
- CRITICAL 138S00073 C7870 10UF 20% 6.3V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C7871 10UF 20% 6.3V CER-X6S 0402-COMBO
- CRITICAL 138S00073 C7872 10UF 20% 6.3V CER-X6S 0402-COMBO

BOM_COST_GROUP=SOC POWER

PAGE TITLE: SPMU: LDO, SW

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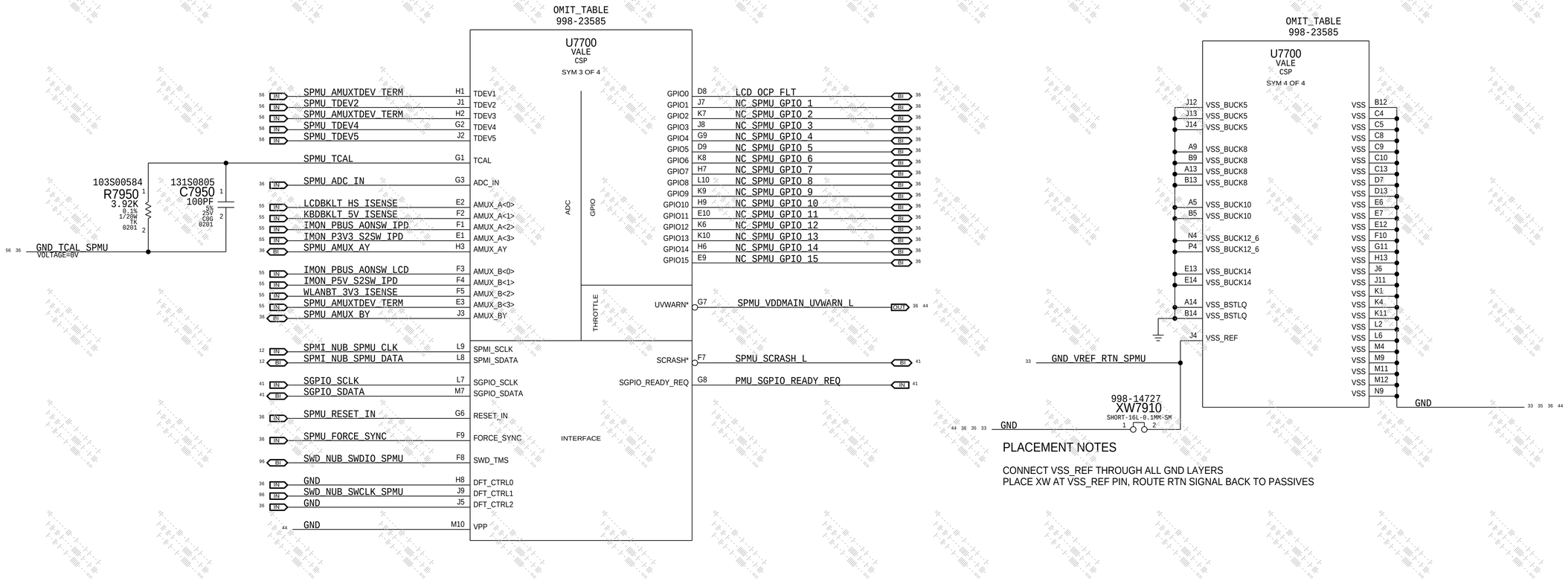

PLACEMENT NOTES

CONNECT VSS_REF THROUGH ALL GND LAYERS
PLACE XW AT VSS_REF PIN, ROUTE RTN SIGNAL BACK TO PASSIVES

BOM_COST_GROUP=SOC POWER

PAGE TITLE	PAGE_TITLE=SPMU: GPIO, VSS
Apple Inc.	DRAWING NUMBER 051-07020 SIZE D
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A SPMU GPIO

35	LCD_OCP_FLT	LCD_OCP_FLT (MAKE_BASE=TRUE)	78
35	NC_SPMU_GPIO_1	NC_SPMU_GPIO_1 (MAKE_BASE=TRUE)	
35	NC_SPMU_GPIO_2	NC_SPMU_GPIO_2 (MAKE_BASE=TRUE)	
35	NC_SPMU_GPIO_3	NC_SPMU_GPIO_3 (MAKE_BASE=TRUE)	
35	NC_SPMU_GPIO_4	NC_SPMU_GPIO_4 (MAKE_BASE=TRUE)	
35	NC_SPMU_GPIO_5	NC_SPMU_GPIO_5 (MAKE_BASE=TRUE)	
35	NC_SPMU_GPIO_6	NC_SPMU_GPIO_6 (MAKE_BASE=TRUE)	
35	NC_SPMU_GPIO_7	NC_SPMU_GPIO_7 (MAKE_BASE=TRUE)	
35	NC_SPMU_GPIO_8	NC_SPMU_GPIO_8 (MAKE_BASE=TRUE)	
35	NC_SPMU_GPIO_9	NC_SPMU_GPIO_9 (MAKE_BASE=TRUE)	
35	NC_SPMU_GPIO_10	NC_SPMU_GPIO_10 (MAKE_BASE=TRUE)	
35	NC_SPMU_GPIO_11	NC_SPMU_GPIO_11 (MAKE_BASE=TRUE)	
35	NC_SPMU_GPIO_12	NC_SPMU_GPIO_12 (MAKE_BASE=TRUE)	
35	NC_SPMU_GPIO_13	NC_SPMU_GPIO_13 (MAKE_BASE=TRUE)	
35	NC_SPMU_GPIO_14	NC_SPMU_GPIO_14 (MAKE_BASE=TRUE)	
35	NC_SPMU_GPIO_15	NC_SPMU_GPIO_15 (MAKE_BASE=TRUE)	
35	GND	GND (MAKE_BASE=TRUE)	33 35 36 44
35	GND	GND (MAKE_BASE=TRUE)	33 35 36 44

B Probe Points

35	BI SPMU_AMUX_AY	1	PP8000 P4MM SM
35	BI SPMU_AMUX_BY	1	PP8001 P4MM SM
33	IN BUCK5_LX0	1	PP8050 P4MM SM
33	IN BUCK5_LX1	1	PP8051 P4MM SM
33	IN BUCK6_LX	1	PP8060 P4MM SM
33	IN BUCK8_LX0	1	PP8080 P4MM SM
33	IN BUCK8_LX1	1	PP8081 P4MM SM
33	IN BUCK8_LX2	1	PP8082 P4MM SM
33	IN BUCK10_LX	1	PP80A0 P4MM SM
33	IN BUCK12_LX	1	PP80C0 P4MM SM
33	IN BUCK14_LX	1	PP80E0 P4MM SM
33	IN SPMU_BSTLQ_LX	1	PP80F0 P4MM SM

C SPMU Quiet GND Connections

44 36 35 33	GND	GND (MAKE_BASE=TRUE)	
55 54 53	GND	GND (MAKE_BASE=TRUE)	
56 35	GND_TCAL_SPMU	XW8030 SHORT-16L-0.1MM-SM 998-14727	GND (MAKE_BASE=TRUE)
33	GND_ADC_RTN_SPMU	XW8031 SHORT-16L-0.1MM-SM 998-14727	GND (MAKE_BASE=TRUE)

D SPMU Input Protection

35	SPMU_ADC_IN	R8010 1M 5% 1/20W TK 0201 117S00096	
35	SPMU_RESET_IN	R8011 100K 5% 1/20W TK 0201 117S00095	
35	SPMU_FORCE_SYNC	R8012 10K 5% 1/20W TK 0201 117S00090	

E SPMU/SOC Throttle Pull-Up

PP1V25_AWAKE_IO 42 93

117S00090
R8020
10K
5%
1/20W
TK
0201

SPMU_VDDMAIN_UVWARN_L

F SPMU Sense Connections

33	PPVDD_SPMU_VDD_MAIN_SNS	XW8020 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1	PP3V8_AON OUT 33 36 92
	PPVDD_SPMU_VDD_MAIN_SNS (MAKE_BASE=TRUE)		
33	PPVDD_SPMU_VDD_BOOST_SNS	XW8021 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1	PP3V8_AON OUT 33 36 92
	PPVDD_SPMU_VDD_BOOST_SNS (MAKE_BASE=TRUE)		

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BOM_COST_GROUP=SOC POWER

SYNC_MASTER= SYNC_DATE=09/10/2021

PAGE TITLE: SPMU: ALIASES, SUPPORT

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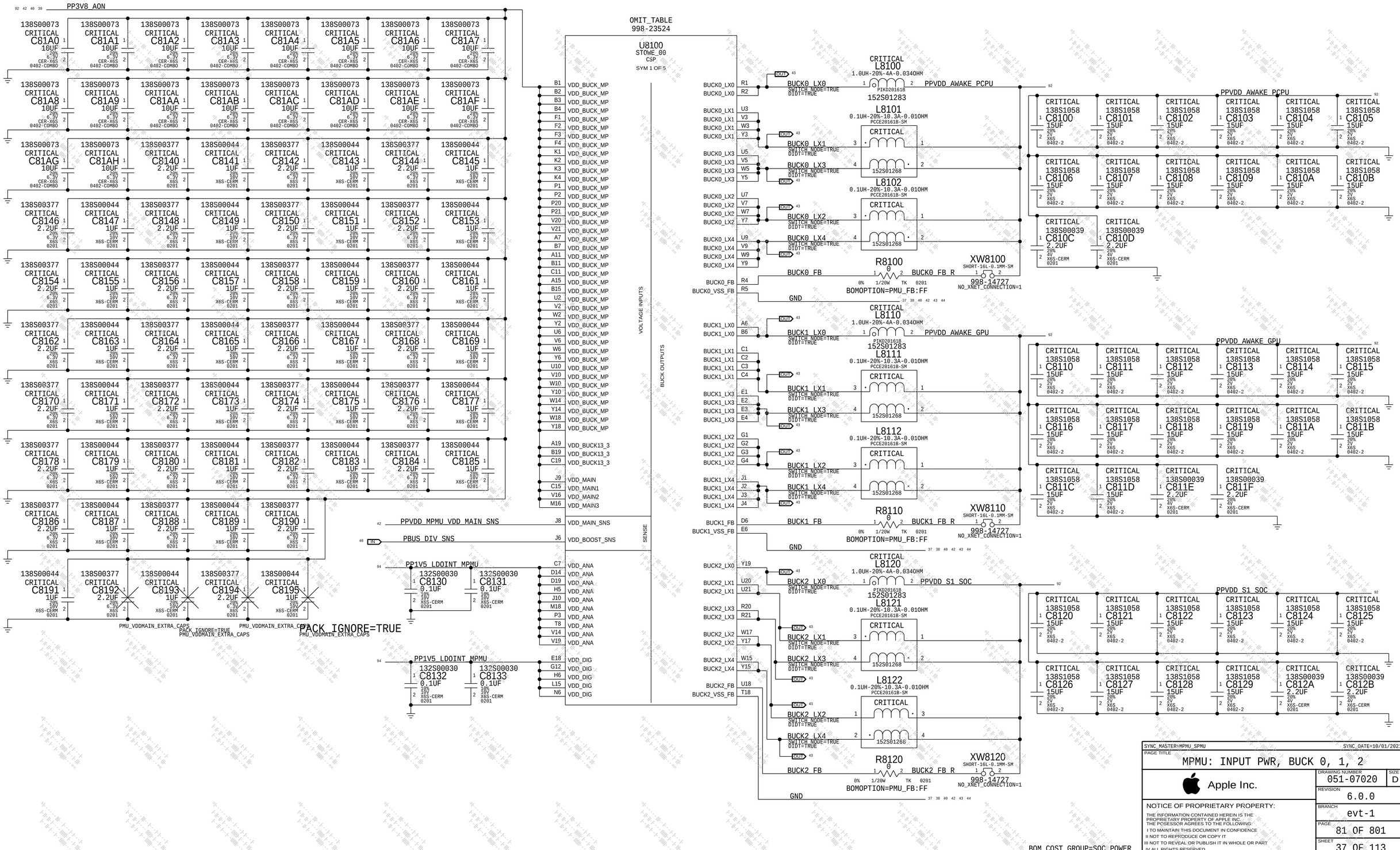

SYNC_MASTER=MPMU_SPMU SYNC_DATE=10/01/2021

PAGE TITLE

MPMU: INPUT PWR, BUCK 0, 1, 2

Apple Inc.

DRAWING NUMBER	051-07020
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OMIT_TABLE
998-23524

U8100
STOWE_00
CSP
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MPMU_BSTLQ_LX — T15 BSTLQ_LX
PP5V_MPMU_BSTLQ_XW — T16 BSTLQ_VOUT
PP5V_MPMU_BSTLQ — D17 VDD_HI_INT1, G7 VDD_HI_INT2, E21 VDD_HI_INT3, M19 VDD_HI_INT4, J15 VDD_HI_INT5
PP1V25_S2 — N13 VDDIO_1V2
PP1V8_S2 — P15 VDDIO_1V8
PP1V2_AON_MPMU — M13 VDDIO_1V2_1V8
PPVREF_MPMU — H11 VREF
PP1V5_MPMU_VREFADC — H7 VREF_ADC
GND_VREF_RTN_MPMU (VOLTAGE=0V)
GND_ADC_RTN_MPMU (VOLTAGE=0V)
H9 VBAT
H8 IBAT
MPMU_VBAT
MPMU_IBAT
NC_MPMU_XIN — M21 XIN
MPMU_XOUT — L21 XOUT
PMU_CLK32K_SOC_R — M7 SLEEP_32K
PMU_CLK32K_WLBT_IPD_R — M8 OUT_32K
PP1V8_S2 — N20 VDD_SW1
PP1V8_S2 — N16 VDD_SW2
PP1V25_S2 — N18 VDD_SW3
VSW1 N21
VSW2 N17
VSW3 N19

BUCK OUTPUTS
CLOCK
LOAD SWITCHES

138S00041 CRITICAL C8211 2.2UF 10% 10V X6S-CERM 0402
132S0406 CRITICAL C8210 0.22UF 20% 6.3V X6S-CERM 0201

BUCK3_LX A18, BUCK3_LX B18
BUCK3_FB D18, BUCK3_VSS_FB C18
BUCK4_LX0 A16
BUCK4_LX1 A14, BUCK4_LX1 B14
BUCK4_LX2 A12, BUCK4_LX2 B12
BUCK4_FB D16, BUCK4_VSS_FB C16
BUCK7_LX0 N1
BUCK7_LX1 L1, BUCK7_LX1 L2, BUCK7_LX1 L3
BUCK7_FB N4, BUCK7_VSS_FB N3
BUCK9_LX0 A8
BUCK9_LX1 A10, BUCK9_LX1 B10, BUCK9_LX1 C10
BUCK9_FB D8, BUCK9_VSS_FB C8
BUCK11_LX0 Y13
BUCK11_LX1 V11, BUCK11_LX1 W11, BUCK11_LX1 Y11
BUCK11_FB U13, BUCK11_VSS_FB V13
BUCK13_LX A20, BUCK13_LX B20, BUCK13_LX C20
BUCK13_FB E20, BUCK13_VSS_FB D20

CRITICAL L8230 0.47UH-20%-4A-0.024OHM PIKD20121B-SM 152S01263
BUCK3_LX — SWITCH_NODE=TRUE DIDT=TRUE
R8230 0 0% 1/20W TK 0201 — BUCK3_FB — BUCK3_FB_R
XW8230 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1 — PP1V8_S2

CRITICAL L8240 1.0UH-20%-4A-0.034OHM PIKD20161B 152S01283
BUCK4_LX0 — SWITCH_NODE=TRUE DIDT=TRUE
L8241 0.1UH-20%-10.3A-0.010HM PCE20161B-SM CRITICAL 152S01268
BUCK4_LX1, BUCK4_LX2 — SWITCH_NODE=TRUE DIDT=TRUE
R8240 0 0% 1/20W TK 0201 — BUCK4_FB — BUCK4_FB_R
BOMOPTION=PMU_FB:FF
XW8240 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1 — PP1V05_S2SW_VDD2H

CRITICAL L8270 1.0UH-20%-4A-0.034OHM PIKD20161B 152S01283
BUCK7_LX0 — SWITCH_NODE=TRUE DIDT=TRUE
CRITICAL L8271 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM 152S00204
BUCK7_LX1 — SWITCH_NODE=TRUE DIDT=TRUE
R8270 0 0% 1/20W TK 0201 — BUCK7_FB — BUCK7_FB_R
BOMOPTION=PMU_FB:FF
XW8270 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1 — PPVDD_AWAKE_CPU_SRAM

CRITICAL L8290 1.0UH-20%-4A-0.034OHM PIKD20161B 152S01283
BUCK9_LX0 — SWITCH_NODE=TRUE DIDT=TRUE — PPVDD_S1_DCS
CRITICAL L8291 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM 152S00204
BUCK9_LX1 — SWITCH_NODE=TRUE DIDT=TRUE
R8290 0 0% 1/20W TK 0201 — BUCK9_FB — BUCK9_FB_R
BOMOPTION=PMU_FB:FF
XW8290 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1

CRITICAL L82B0 1.0UH-20%-4A-0.034OHM PIKD20161B 152S01283
BUCK11_LX0 — SWITCH_NODE=TRUE DIDT=TRUE
CRITICAL L82B1 0.22UH-20%-6.7A-0.023OHM PINA20121T-SM 152S00204
BUCK11_LX1 — SWITCH_NODE=TRUE DIDT=TRUE
R82B0 0 0% 1/20W TK 0201 — BUCK11_FB — BUCK11_FB_R
BOMOPTION=PMU_FB:FF
XW82B0 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1 — PPVDD_AWAKE_ECPU

CRITICAL L82D0 0.47UH-20%-6.9A-0.022OHM MEMK2520-SM 152S01325
BUCK13_LX — SWITCH_NODE=TRUE DIDT=TRUE — PP1V25_S2
R82D0 0 0% 1/20W TK 0201 — BUCK13_FB — BUCK13_FB_R
XW82D0 SHORT-16L-0.1MM-SM 998-14727 NO_XNET_CONNECTION=1

GND

PP1V8_AWAKE
NC_PPVOUT_MPMU_SW2_REG
PP1V25_AWAKE_IO

VSW4 700MA MAX, 23MOHM MAX
VSW5 350MA MAX, 125MOHM MAX
VSW6 200MA MAX, 23MOHM MAX

PP1V8_S2: CRITICAL C8230 C8231 C8232 C8233 C8234 C8235 C8236 C8237 C8238 C8239 C823A C823B 10UF 20% 6.3V CER-X6S 0402-COMBO
PP1V05_S2SW_VDD2H: CRITICAL C8240 C8241 C8242 C8243 C8244 C8245 C8246 C8247 C8248 C8249 C824A C824B 15UF 20% 2V X6S 0402-2; C824C C824D 2.2UF 20% 4V X6S-CERM 0201
PPVDD_AWAKE_CPU_SRAM: CRITICAL C8270 C8271 C8272 C8273 C8274 C8275 C8276 C8277 15UF 20% 2V X6S 0402-2; C8278 C8279 2.2UF 20% 4V X6S-CERM 0201; C8298 C8299 2.2UF 20% 4V X6S-CERM 0201
PPVDD_S1_DCS: CRITICAL C8290 C8291 C8292 C8293 C8294 C8295 C8296 C8297 15UF 20% 2V X6S 0402-2 — NOSTUFF NOSTUFF
PPVDD_AWAKE_ECPU: CRITICAL C82B0 C82B1 C82B2 C82B3 C82B4 C82B5 C82B6 C82B7 15UF 20% 2V X6S 0402-2; C82B8 C82B9 2.2UF 20% 4V X6S-CERM 0201
PP1V25_S2: CRITICAL C82D0 C82D1 C82D2 C82D3 C82D4 C82D5 15UF 20% 2V X6S 0402-2

VDD_SW1 — PP1V8_S2 — CRITICAL C8200 10UF 20% 6.3V CER-X6S 0402-COMBO — PLACE_NEAR=U8100.N20:5MM
VDD_SW3 — PP1V25_S2 — CRITICAL C8201 10UF 20% 6.3V CER-X6S 0402-COMBO — PLACE_NEAR=U8100.N18:5MM
VSW1 — PP1V8_AWAKE — CRITICAL C8202 C8203 10UF 20% 6.3V CER-X6S 0402-COMBO
VSW3 — PP1V25_AWAKE_IO — CRITICAL C8204 C8205 10UF 20% 6.3V CER-X6S 0402-COMBO — BOM_COST_GROUP=SOC POWER

SYNC_MASTER=MPMU_SPMU SYNC_DATE=10/01/2021
PAGE TITLE: MPMU: BUCK 3, 4, 7, 9, 11, 13, SW
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LDO INPUTS

Signal	Pin
PP3V8_AON (VDDMAIN>>)	F15 VDD_CTRL_LDOG
PP3V8_AON	G17 VDD_BOOST_LDO
	G18 VDD_BOOST_LDO
	H17 VDD_BOOST_LDO
	H18 VDD_BOOST_LDO
	J18 VDD_BOOST_LDO
PP3V8_AON	J17 VDD_MAIN_LDO
	K17 VDD_MAIN_LDO
	K19 VDD_MAIN_LDO
PP3V8_AON	L18 VDD_RTC_ALT
BUCK3 OR BUCK13>> PPVDD_LDO20_14_8_3	F19 VDD_LDO20_14_8_3
	F20 VDD_LDO20_14_8_3
	G20 VDD_LDO20_14_8_3
	H20 VDD_LDO20_14_8_3
BUCK4>> PP1V05_S2SW_VDD2H	J20 VDD_LDO11
BUCK4>> PP1V05_S2SW_VDD2H	F16 VDD_LDO16
IN NC_MPMU_LDO1_EN	R13 LDO1_EN

LDO OUTPUTS

Pin	Signal	Output
VLDO1 G19	NC_MPMU_VLDO1	LDO1 300MA MAX
VLDO2 J16	PP1V8_AON	LDO2 50MA MAX
VLDO3 F18	NC_MPMU_VLDO3	LDO3 600MA MAX
VLDO5 G16	NC_MPMU_VLDO5	LDO5 250MA MAX
VLDO7 H19	PP3V3_S2_LDO	LDO7 250MA MAX
VLDO8 H21	PP1V2_AWAKE_PLL	LDO8 730MA MAX
VLDO9 K16	PP1V8_AON_MPMU	LDO9 10MA MAX
VLDO9B K18	PP1V2_AON_MPMU	LDO9B 10MA MAX
VLDO10 H16	PP3V3_AON	LDO10 250MA MAX
VLDO11 J21	PP0V855_S2SW_CIO	LDO11 1000MA MAX
VLDO13 J19	PP3V3_S2SW_SNS	LDO13 250MA MAX
VLDO14 F21	NC_MPMU_VLDO14	LDO14 300MA MAX
VLDO16 F17	NC_MPMU_VLDO16	LDO16 1500MA MAX
VLDO20 G21	PP1V2_S2_CIO	LDO20 400MA MAX
VLDOINT K20	PP1V5_LDOINT_MPMU	LDOINT 150MA MAX
VLDORTC L19	PP1V5_LDOINT_MPMU	
VLDORTC2 L20	GND	

VDD LDO 3/8/14/20

PPVDD_LDO20_14_8_3
- C8300 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073
- C8301 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073

LDO 2 DECOUPLING

PP1V8_AON
- C8320 4.7UF 6.3V X6S 0402 — CRITICAL 138S0750

LDO 9 DECOUPLING

PP1V8_AON_MPMU
- C8310 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073
- C8311 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073

LDO 11 DECOUPLING

PP0V855_S2SW_CIO
- C83B5 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073
- C83B6 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073

LDO INT DECOUPLING

PP1V5_LDOINT_MPMU
- C8380 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073
- C8381 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073

VDD LDO 11

PP1V05_S2SW_VDD2H
- C83B0 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073
- C83B1 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073

LDO 7 DECOUPLING

PP3V3_S2_LDO
- C8330 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073
- C8331 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073

LDO 9B DECOUPLING

PP1V2_AON_MPMU
- C8340 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073
- C8341 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073

LDO 13 DECOUPLING

PP3V3_S2SW_SNS
- C83D0 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073

UN-UNUSED LDOS

LDO 1, 3, 5, 14, 16

LDO RTC

(TIED TO LDOINT FOR PORTABLES)

LDO 8 DECOUPLING

PP1V2_AWAKE_PLL
- C8360 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073
- C8361 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073
- C8362 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073 — NOSTUFF

LDO 10 DECOUPLING

PP3V3_AON
- C83A0 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073

LDO 20 DECOUPLING

PP1V2_S2_CIO
- C8350 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073
- C8351 10UF 20% 6.3V CER-X6S 0402-COMBO — CRITICAL 138S00073

BOM_COST_GROUP=SOC POWER

SYNC_MASTER=MPMU_SPMU SYNC_DATE=10/01/2021

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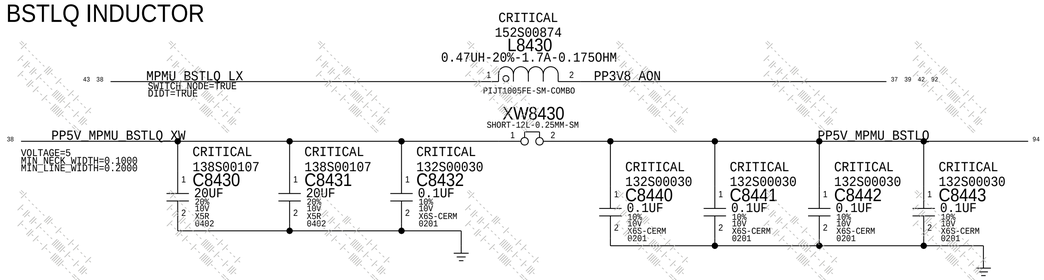
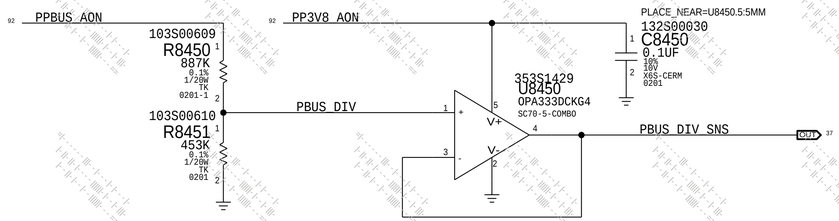
BSTLQ INDUCTOR



PBUS SENSE

POSSIBLE TO USE SMALLER FOOTPRINT OPAMP (TLV9051IDPW)



32K CLOCK XO (PACK_OPTION PMU_32K_OSC)

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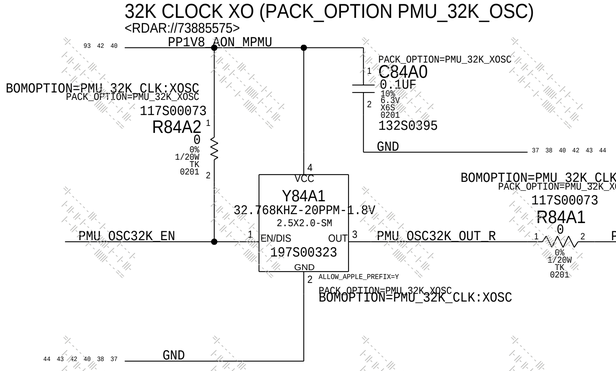
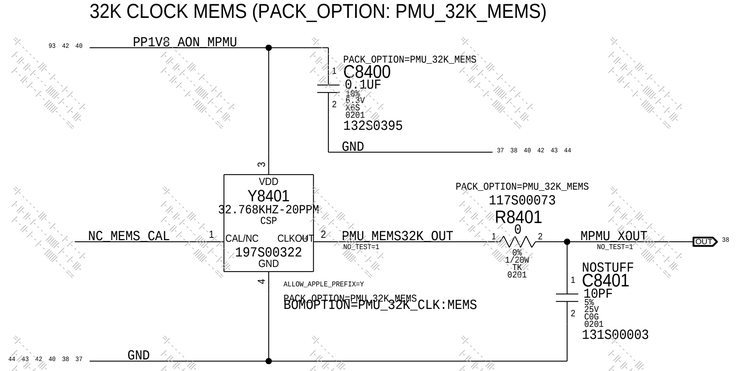
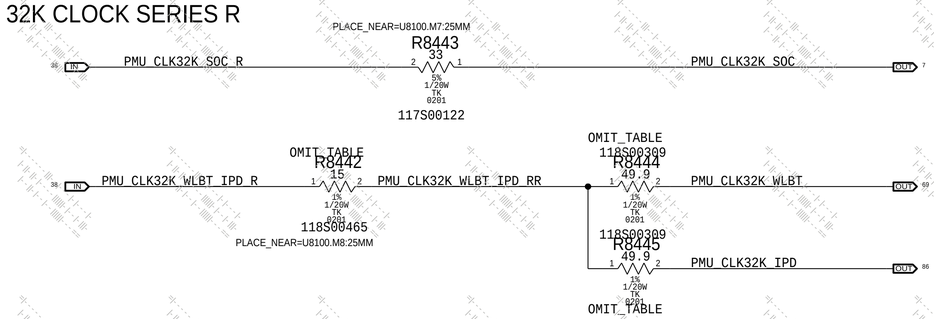
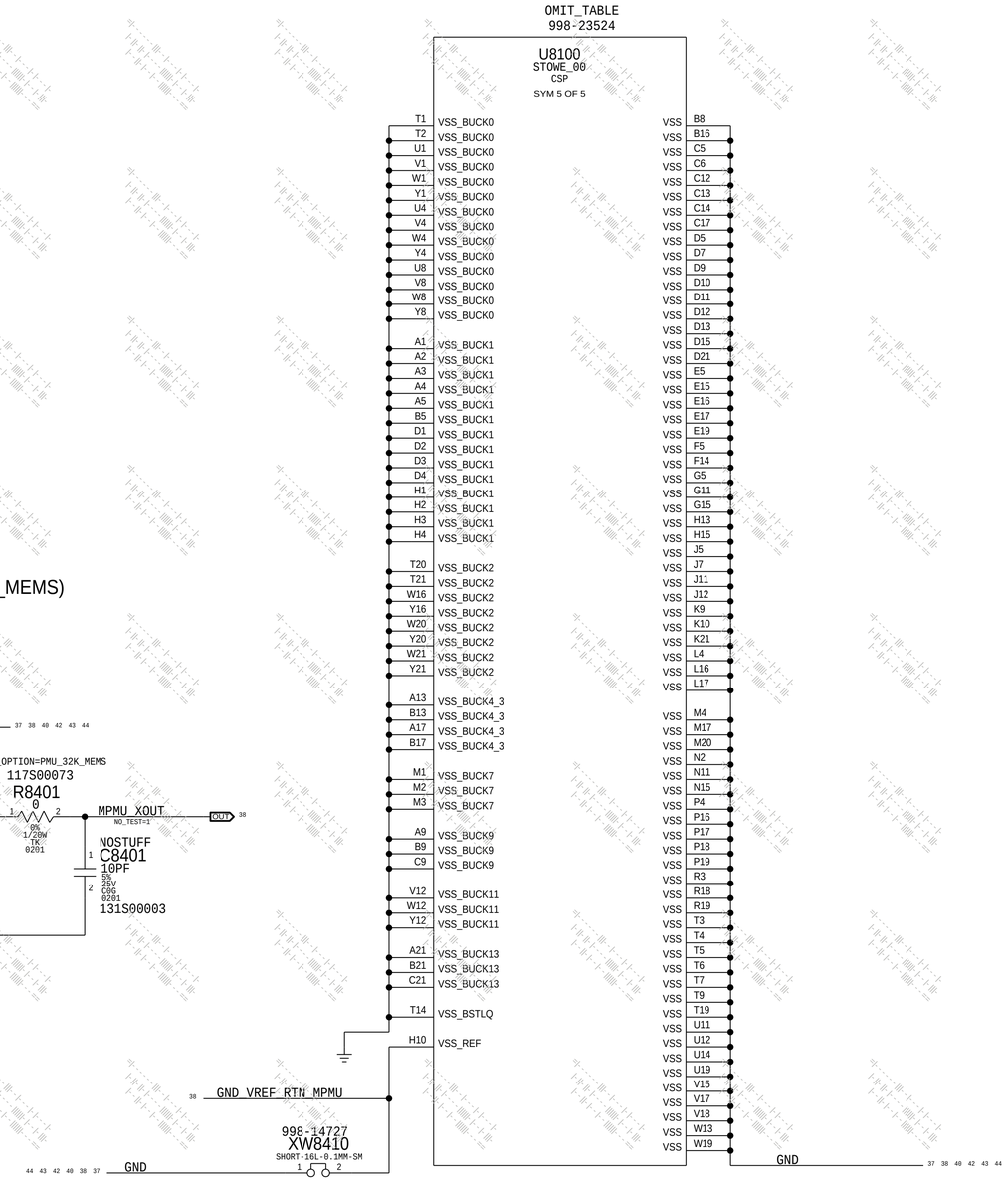


32K CLOCK MEMS (PACK_OPTION: PMU_32K_MEMS)



32K CLOCK SERIES R





PLACEMENT NOTES

CONNECT VSS_REF THROUGH ALL GND LAYERS
PLACE XW AT VSS_REF PIN, ROUTE RTN SIGNAL BACK TO PASSIVES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S00465	1	RES,TK,15 OHM,1%,1/20W,0201	R8442		PMU_OUT32K:TEE
117S00122	1	RES,TK,33 OHM,5%,1/20W,0201	R8442		PMU_OUT32K:WLBT
118S00309	2	RES,TK,49.9 OHM,1%,1/20W,0201	R8444,R8445		PMU_OUT32K:TEE
117S00073	1	RES,TK,0 OHM,1A MAX,1/20W,0201	R8444		PMU_OUT32K:WLBT

BOM_COST_GROUP=SOC POWER

PAGE_TITLE=MPMU: MISC CKT, VSS

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U8100
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Net	Pin	Function
MPMU_AMUXTDEV_TERM	F8	TDEV1
MPMU_TDEV2	F13	TDEV2
MPMU_TDEV3	F9	TDEV3
MPMU_TDEV4	F10	TDEV4
MPMU_TDEV5	F11	TDEV5
MPMU_TDEV6	F12	TDEV6
MPMU_TDEV7	G9	TDEV7
MPMU_TDEV8	G8	TDEV8
MPMU_TCAL	E14	TCAL
GND	E13	BRICK_ID1
GND	E9	BRICK_ID2
MPMU_ADC_IN	G14	ADC_IN
DCIN_VSENSE	E11	AMUX_A<0>
DCIN_ISENSE	E10	AMUX_A<1>
PBUS_VSENSE	E8	AMUX_A<2>
BMON_ISENSE	E7	AMUX_A<3>
MPMU_AMUX_AY	G13	AMUX_AY
P3V8AON_IMEAS	E12	AMUX_B<0>
P3V3S2_HS_ISENSE	F6	AMUX_B<1>
P5VS2_HS_ISENSE	F7	AMUX_B<2>
MPMU_AMUXTDEV_TERM	G6	AMUX_B<3>
MPMU_AMUX_BY	G10	AMUX_BY
PMU_ONOFF_L	N12	BUTTON1
PMU_RSLOC_RST_L	L13	BUTTON2
NC_MPMU_BUTTON3	K15	BUTTON3
NC_MPMU_BUTTON4	K13	BUTTON4
NC_MPMU_RESET_IN0	K7	RESET_IN0
SOC_WDOG	L9	RESET_IN1
UPC_PMU_RESET_1V8	K5	RESET_IN2
SOC_SOCHOT_L	M9	RESET_IN3
MPMU_SHDN	K11	SHDN
MPMU_REQUEST_DFU	L12	REQUEST_DFU
NC_MPMU_VBUS_DET	L11	VBUS_DETECT
SPMI_NUB_MPMU_CLK	M14	SPMI_SCLK
SPMI_NUB_MPMU_DATA	M15	SPMI_SDATA
SGPIO_SCLK_R	P14	SGPIO_SCLK
SGPIO_SDATA_R	N14	SGPIO_SDATA
PMU_SGPIO_READY_REQ	P13	SGPIO_READY_REQ
SWD_NUB_SWDIO_MPMU	K12	SWD_TMS
GND	J14	DFT_CTRL0
SWD_NUB_SWCLK_MPMU	J13	DFT_CTRL1
GND	H12	DFT_CTRL2
MPMU_OTP_SEL	N5	OTP_SEL
GND	K8	VPP

Net	Pin	Function
IPD_LID_OPEN_1V8	R12	GPIO0
CODEC_WAKE_L	R6	GPIO1
IPD_OCP_FLT	M11	GPIO2
NC_MPMU_GPIO_3	P9	GPIO3
CHGR_AUX_OK	M10	GPIO4 (HLD)
WLBT_WAKE	N9	GPIO5
IPD_PWR_EN	T10	GPIO6 (HLD)
NC_MPMU_GPIO_7	N10	GPIO7
IPD_TOUCH_RESET_L	T11	GPIO8 (SEQ)
NC_MPMU_GPIO_9	U15	GPIO9 (SEQ)
LCD_PWR_EN	U16	GPIO10 (SEQ)
P3V3S2_PWR_EN_MPMU	P11	GPIO11 (SEQ)
PVDD1_PWR_EN	P12	GPIO12 (SEQ)
WLBT_PWR_EN	R15	GPIO13 (SEQ)
TPAD_KBD_WAKE_L	P7	GPIO14 (SEQ)
SE_PWR_EN	P6	GPIO15 (SEQ)
NC_MPMU_GPIO_16	P5	GPIO16 (SEQ)
NAND0_LPB_L	R8	GPIO17 (SEQ)
BL_PWR_EN	R9	GPIO18 (SEQ)
P3V8AON_LPM	R7	GPIO19 (SEQ,HLD)
P5VS2TPS_PWR_EN	R10	GPIO20 (SEQ,HLD)
NC_MPMU_GPIO_21	P10	GPIO21 (SEQ)
NC_MPMU_GPIO_22	R11	GPIO22 (SEQ)
NC_MPMU_GPIO_23	T12	GPIO23 (SEQ)
IPD_MCU_RESET_L	T13	GPIO24 (SEQ)
NC_MPMU_GPIO_25	R16	GPIO25 (SEQ)
NC_MPMU_GPIO_26	R17	GPIO26 (SEQ,HV)
NC_MPMU_BUTTONO1	L14	BUTTONO1
NC_MPMU_BUTTONO2	K14	BUTTONO2
NC_MPMU_BUTTONO3	M12	BUTTONO3
DBL_CLICK_DET	T17	DBLCLICK_DET
PMU_RESET_L	L6	RESET*
MPMU_SOC_FORCE_DFU_R	H14	FORCE_DFU
NC_MPMU_WAKE2MS	R14	WAKE2MS
NC_MPMU_OFF_REQ	U17	OFF_REQ
PMU_SYS_ALIVE	K6	SYS_ALIVE
PMU_ACTIVE_READY	L10	ACTIVE_READY
PMU_CRASH_L	L8	CRASH*
MPMU_FAULT_OUT_L	L7	FAULT_OUT*
MPMU_SCRASH_L	M6	SCRASH*
BUCK0_THERMAL_THROTTLE_L	L5	THROTTLE0*
BUCK1_THERMAL_THROTTLE_L	N7	THROTTLE1*
TPT_MPMU_THROTTLE2_L	P8	THROTTLE2*
PMU_VDDHI_UVWARN_L	N8	THROTTLE3*
MPMU_VDDMAIN_UVWARN_L	M5	UVWARN*

ADC / GPIO / BUTTONS / STATE MACHINE / INTERFACE / THROTTLE

103S00584
R8550
3.92K
0.1% 1/20W TK 0201

131S0805
C8550
100PF
5% 25V C0G 0201

GND_TCAL_MPMU
VOLTAGE=0V

117S00113
R8540
20
5% 1/20W TK 0201

117S00113
R8541
20
5% 1/20W TK 0201

SGPIO_SCLK

SGPIO_SDATA

117S00099
R8562
2.2K
5% 1/20W TK 0201

SOC_FORCE_DFU

NOSTUFF
117S00090
R8561
10K
5% 1/20W TK 0201

PP1V8_AON_MPMU

>> IPU: LDO9
117S00077
R8560
1K
5% 1/20W TK 0201-1

SPMU_SCRASH_L

BOM_COST_GROUP=SOC POWER

SYNC_MASTER=MPMU_SPMU SYNC_DATE=10/01/2021

PAGE TITLE
MPMU: GPIO

Apple Inc.

DRAWING NUMBER 051-07020 SIZE D

REVISION 6.0.0

BRANCH evt-1

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A MPMU GPIO Aliases

IO OTP SETTINGS (WIP), IF NOT OTP IT WILL BE CONFIGURED AS SW OVERRIDE..
SUPPLY:LDO9 (1.8V AON), BUCK13 (1.25V S2), BUCK3 (1.8V S2), SLDO9B (1.2V AON)
IO TYPE: INPUT, OUTPUT OPEN DRAIN, OR OUTPUT PUSH PULL
PULLS: IPU, IPD, NONE

GPIO0: LDO9 IN IPD
GPIO1: LDO9 IN IPU
GPIO2: LDO9 IN IPD
GPIO3: BUCK13 IN IPD
GPIO4: -WIP- IN IPU
GPIO5: BUCK13 IN IPD
GPIO6: LDO9 PP NONE
GPIO7: LDO9 IN IPD
> NEEDS OVERRIDE?
GPIO8: LDO9 OD NONE
GPIO9: LDO9 IN IPD
> NEEDS OVERRIDE?
GPIO10: LDO9 PP NONE
GPIO11: LDO9 PP NONE
GPIO12: LDO9 OD NONE
GPIO13: -WIP- PP NONE
GPIO14: LDO9 IN NONE
GPIO15: LDO9 PP NONE
GPIO16: LDO9 IN IPD
> NEEDS OVERRIDE?
GPIO17: BUCK13 PP NONE
GPIO18: LDO9 PP NONE
GPIO19: LDO9 PP IPD
GPIO20: LDO9 PP NONE
GPIO21: LDO9 IN IPD
> NEEDS OVERRIDE?
GPIO22: LDO9 IN IPD
> NEEDS OVERRIDE?
GPIO23: LDO9 IN IPD
> NEEDS OVERRIDE?
GPIO24: LDO9 OD NONE
GPIO25: WIP PP NONE
GPIO26: LDO9 IN IPD
> NEEDS OVERRIDE?

41 BI	IPD_LID_OPEN_1V8	IPD_LID_OPEN_1V8 (MAKE_BASE=TRUE)	81 87
41 BI	CODEC_WAKE_L	CODEC_WAKE_L (MAKE_BASE=TRUE)	85
41 BI	IPD_OCP_FLT	IPD_OCP_FLT (MAKE_BASE=TRUE)	48
41 BI	NC_MPMU_GPIO_3	NC_MPMU_GPIO_3 (MAKE_BASE=TRUE)	
41 BI	CHGR_AUX_OK	CHGR_AUX_OK (MAKE_BASE=TRUE)	26
41 BI	WLBT_WAKE	WLBT_WAKE (MAKE_BASE=TRUE)	69 70
41 BI	IPD_PWR_EN	IPD_PWR_EN (MAKE_BASE=TRUE)	42 48
41 BI	NC_MPMU_GPIO_7	NC_MPMU_GPIO_7 (MAKE_BASE=TRUE)	
41 BI	IPD_TOUCH_RESET_L	IPD_TOUCH_RESET_L (MAKE_BASE=TRUE)	42 86
41 BI	NC_MPMU_GPIO_9	NC_MPMU_GPIO_9 (MAKE_BASE=TRUE)	
41 BI	LCD_PWR_EN	LCD_PWR_EN (MAKE_BASE=TRUE)	76
41 BI	P3V3S2_PWR_EN_MPMU	P3V3S2_PWR_EN_MPMU (MAKE_BASE=TRUE)	42 46
41 BI	PVDD1_PWR_EN	PVDD1_PWR_EN (MAKE_BASE=TRUE)	48
41 BI	WLBT_PWR_EN	WLBT_PWR_EN (MAKE_BASE=TRUE)	69 70
41 BI	TPAD_KBD_WAKE_L	TPAD_KBD_WAKE_L (MAKE_BASE=TRUE)	86
41 BI	SE_PWR_EN	SE_PWR_EN (MAKE_BASE=TRUE)	93
41 BI	NC_MPMU_GPIO_16	NC_MPMU_GPIO_16 (MAKE_BASE=TRUE)	
41 BI	NAND0_LPB_L	NAND0_LPB_L (MAKE_BASE=TRUE)	71 72
41 BI	BL_PWR_EN	BL_PWR_EN (MAKE_BASE=TRUE)	77
41 BI	P3V8AON_LPM	P3V8AON_LPM (MAKE_BASE=TRUE)	30 42
41 BI	P5VS2TPS_PWR_EN	P5VS2TPS_PWR_EN (MAKE_BASE=TRUE)	42 46
41 BI	NC_MPMU_GPIO_21	NC_MPMU_GPIO_21 (MAKE_BASE=TRUE)	
41 BI	NC_MPMU_GPIO_22	NC_MPMU_GPIO_22 (MAKE_BASE=TRUE)	
41 BI	NC_MPMU_GPIO_23	NC_MPMU_GPIO_23 (MAKE_BASE=TRUE)	
41 BI	IPD_MCU_RESET_L	IPD_MCU_RESET_L (MAKE_BASE=TRUE)	42 86
41 BI	NC_MPMU_GPIO_25	NC_MPMU_GPIO_25 (MAKE_BASE=TRUE)	
41 BI	NC_MPMU_GPIO_26	NC_MPMU_GPIO_26 (MAKE_BASE=TRUE)	

B MPMU Input Protection & Pull-Downs

42 30	P3V8AON_LPM	R8630 100K 5% 1/20W TK 0201	117S00095
46 42	P5VS2TPS_PWR_EN	R8631 100K 5% 1/20W TK 0201	117S00095
46 42	P3V3S2_PWR_EN_MPMU	R8632 100K 5% 1/20W TK 0201	117S00095
42 41	MPMU_OTP_SEL PD FOR PORTABLES	R8622 0 6% 1/20W TK 0201	117S00073
41	MPMU_ADC_IN	R8610 1M 5% 1/20W TK 0201	117S00096
38	MPMU_IBAT	R8611 1M 5% 1/20W TK 0201	117S00096
41	MPMU_REQUEST_DFU	R8612 10K 5% 1/20W TK 0201	117S00090
41	MPMU_SHDN	R8613 10K 5% 1/20W TK 0201	117S00090
38	MPMU_VBAT	R8614 1M 5% 1/20W TK 0201	117S00096
88 62 44 7	SOC_FORCE_DFU PMOS OD	R8615 47K 5% 1/20W TK 0201	117S00129
48 42	IPD_PWR_EN	R8616 100K 5% 1/20W TK 0201	117S00095

C MPMU Pull-Ups

PP1V8_AON_MPMU (40 93)

R8620	117S00090	10K 5% 1/20W TK 0201	PMU_CRASH_L (41 46)
R8621	117S00095	100K 5% 1/20W TK 0201	MPMU_FAULT_OUT_L (41)
R8623	117S00090	10K 5% 1/20W TK 0201	PMU_ONOFF_L (42 43 85 88)
R8624	117S00090	10K 5% 1/20W TK 0201	PMU_RSLOC_RST_L (43 44 85 88)
R8625	117S00095	100K 5% 1/20W TK 0201	IPD_TOUCH_RESET_L (42 86)
R8626	117S00095	100K 5% 1/20W TK 0201	IPD_MCU_RESET_L (42 86)

PP1V25_S2 (93)

R8640	117S00090	10K 5% 1/20W TK 0201	PMU_SYS_ALIVE (41 73 88 96)
	NOSTUFF		

PP1V25_AWAKE_IO (36 93)

R8651	117S00090	10K 5% 1/20W TK 0201	BUCK0_THERMAL_THROTTLE_L (41 44)
	NOSTUFF		
R8652	117S00090	10K 5% 1/20W TK 0201	BUCK1_THERMAL_THROTTLE_L (41 44)
	NOSTUFF		
R8653	117S00090	10K 5% 1/20W TK 0201	TPT_MPMU_THROTTLE2_L (41 44)
R8654	117S00090	10K 5% 1/20W TK 0201	PMU_VDDHI_UVWARN_L (41 44)
	NOSTUFF		
R8650	117S00090	10K 5% 1/20W TK 0201	MPMU_VDDMAIN_UVWARN_L (41 44)
	NOSTUFF		

D MPMU Misc Aliases

41	GND	GND (MAKE_BASE=TRUE) 37 38 40 42 43 44
41	GND	GND (MAKE_BASE=TRUE) 37 38 40 42 43 44
41	GND	GND (MAKE_BASE=TRUE) 37 38 40 42 43 44
41	GND	GND (MAKE_BASE=TRUE) 37 38 40 42 43 44
39	NC_MPMU_LDO1_EN	NC_MPMU_LDO1_EN (MAKE_BASE=TRUE)
41	NC_MPMU_OFF_REQ	NC_MPMU_OFF_REQ (MAKE_BASE=TRUE)
42 41	MPMU_OTP_SEL	MPMU_OTP_SEL (MAKE_BASE=TRUE) 41 42
41	NC_MPMU_WAKE2MS	NC_MPMU_WAKE2MS (MAKE_BASE=TRUE)

VLDORTC2 IS PLANNED FOR B0, AND CURRENTLY NOT IMPLEMENTED

39	GND	GND (MAKE_BASE=TRUE) 37 38 40 42 43 44

E MPMU VDD_MAIN Sense

XW8661
SHORT-16L-0.1MM-SM
998-14727
NO_XNET_CONNECTION=1

37	PPVDD_MPMU_VDD_MAIN_SNS	PP3V8_AON (OUT) 37 39 40 92
	PPVDD_MPMU_VDD_MAIN_SNS (MAKE_BASE=TRUE)	

F MPMU Button and Reset Aliases

41 OUT	PMU_ONOFF_L	PMU_ONOFF_L (MAKE_BASE=TRUE) 42 43 85 88
41	NC_MPMU_BUTTON3	NC_MPMU_BUTTON3 (MAKE_BASE=TRUE)
41	NC_MPMU_BUTTON4	NC_MPMU_BUTTON4 (MAKE_BASE=TRUE)
41	NC_MPMU_BUTTONO1	NC_MPMU_BUTTONO1 (MAKE_BASE=TRUE)
41	NC_MPMU_BUTTONO2	NC_MPMU_BUTTONO2 (MAKE_BASE=TRUE)
41	NC_MPMU_BUTTONO3	NC_MPMU_BUTTONO3 (MAKE_BASE=TRUE)
41	NC_MPMU_RESET_IN0	NC_MPMU_RESET_IN0 (MAKE_BASE=TRUE)
41	UPC_PMU_RESET_1V8	UPC_PMU_RESET_1V8 (MAKE_BASE=TRUE) 43

BOM_COST_GROUP=SOC POWER

PAGE TITLE: MPMU: ALIAS, PULLS

Apple Inc.

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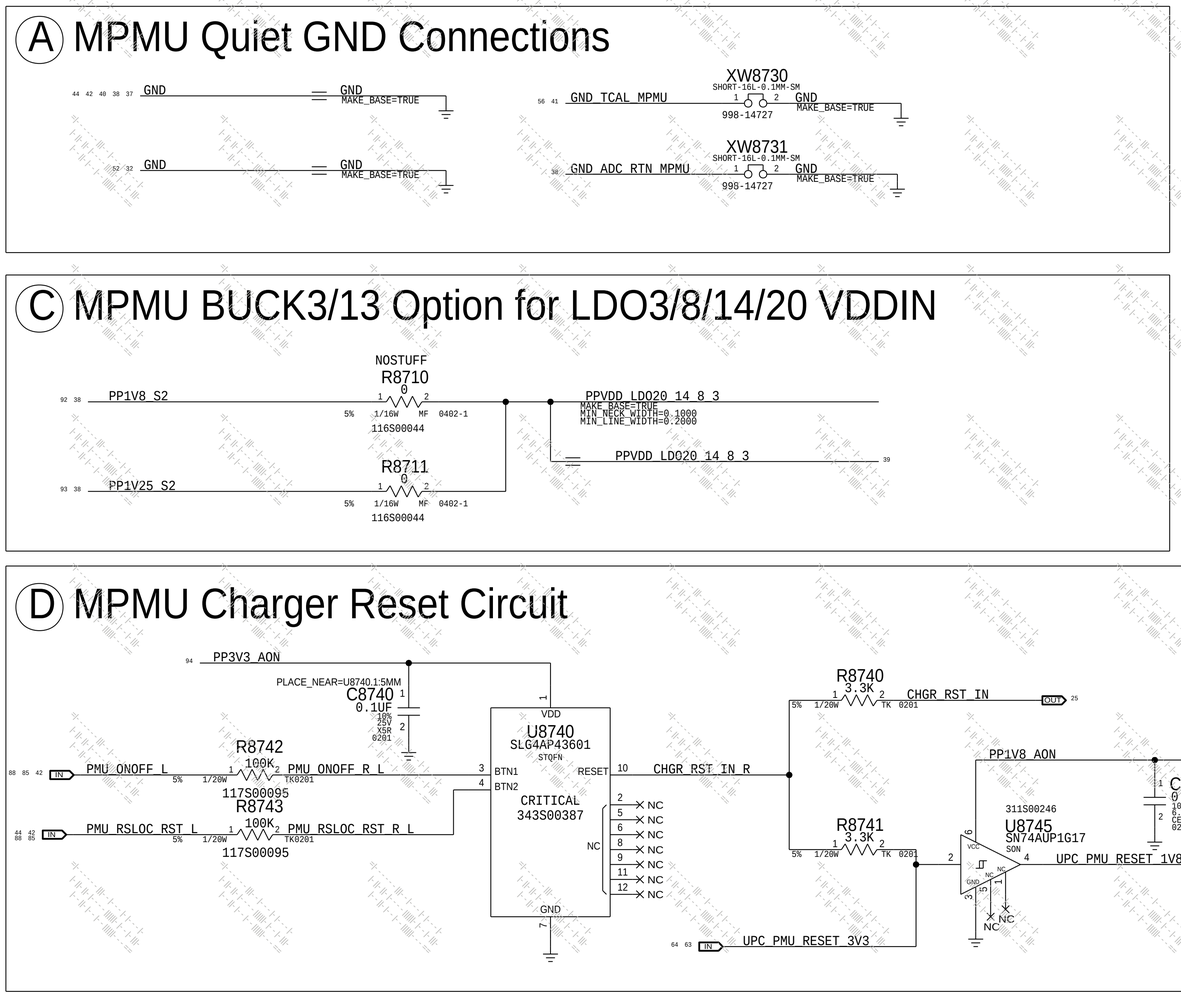

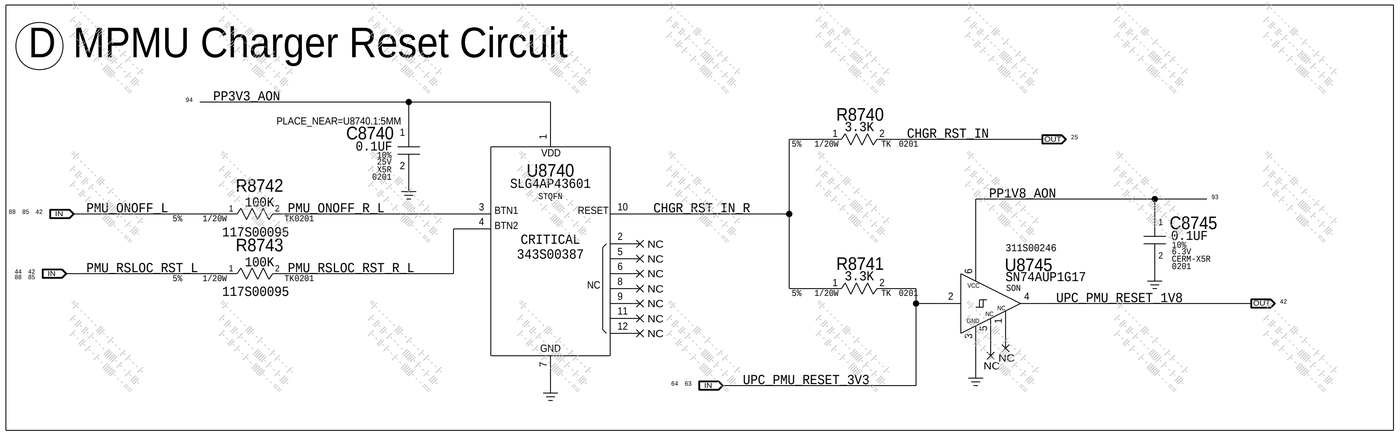

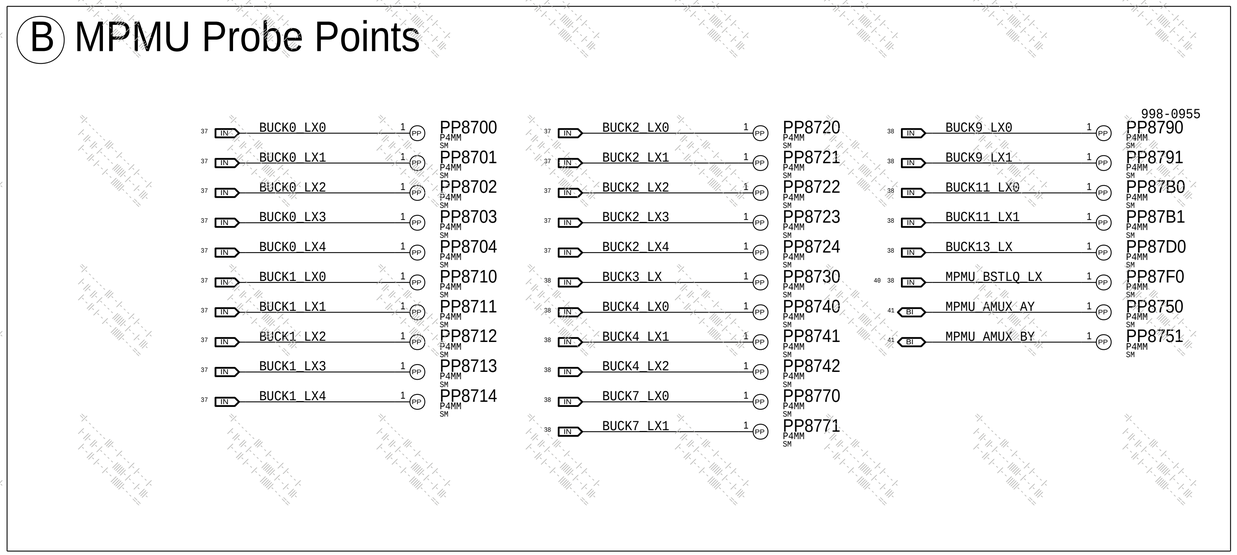

BOM_COST_GROUP=SOC POWER

SYNC_MASTER=jawebb SYNC_DATE=09/28/2021

PAGE TITLE: MPMU: SUPPORT

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D

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A MPMU Misc Aliases

41 OUT	PMU_RSLOC_RST_L	PMU_RSLOC_RST_L MAKE_BASE=TRUE	42 43 85 88
38	NC_MPMU_XIN	NC_MPMU_XIN MAKE_BASE=TRUE	
41	SOC_WDOG	SOC_WDOG MAKE_BASE=TRUE	7
41	SOC_SOCHOT_L	SOC_SOCHOT_L MAKE_BASE=TRUE	9
41	PMU_RESET_L	PMU_RESET_L MAKE_BASE=TRUE	7 88
41	PMU_ACTIVE_READY	PMU_ACTIVE_READY MAKE_BASE=TRUE	7 61 88
41	DBL_CLICK_DET	DBL_CLICK_DET MAKE_BASE=TRUE	9
41	SOC_FORCE_DFU	SOC_FORCE_DFU MAKE_BASE=TRUE	7 42 62 88
42 41	BUCK0_THERMAL_THROTTLE_L	BUCK0_THERMAL_THROTTLE_L MAKE_BASE=TRUE	9
42 41	BUCK1_THERMAL_THROTTLE_L	BUCK1_THERMAL_THROTTLE_L MAKE_BASE=TRUE	9
42 41	TPT_MPMU_THROTTLE2_L	TPT_MPMU_THROTTLE2_L MAKE_BASE=TRUE	
42 41	PMU_VDDHI_UVWARN_L	PMU_VDDHI_UVWARN_L MAKE_BASE=TRUE	9
42 41	MPMU_VDDMAIN_UVWARN_L	MPMU_VDDMAIN_UVWARN_L MAKE_BASE=TRUE	9
41	NC_MPMU_VBUS_DET	NC_MPMU_VBUS_DET MAKE_BASE=TRUE	
41	GND	GND MAKE_BASE=TRUE	37 38 40 42 43

B SPMU Misc Aliases

9	SPMU_VDDMAIN_UVWARN_L	SPMU_VDDMAIN_UVWARN_L MAKE_BASE=TRUE	44
36 35	SPMU_VDDMAIN_UVWARN_L	SPMU_VDDMAIN_UVWARN_L MAKE_BASE=TRUE	44
35	GND	GND MAKE_BASE=TRUE	33 35 36

C 32.768kHz Clock Aliases

40	PMU_MEMS32K_OUT	PMU_MEMS32K_OUT MAKE_BASE=TRUE	40

BOM_COST_GROUP=SOC POWER

SYNC_MASTER= SYNC_DATE=09/10/2021

PAGE TITLE: PMU: SUPPORT - FF

Apple Inc.

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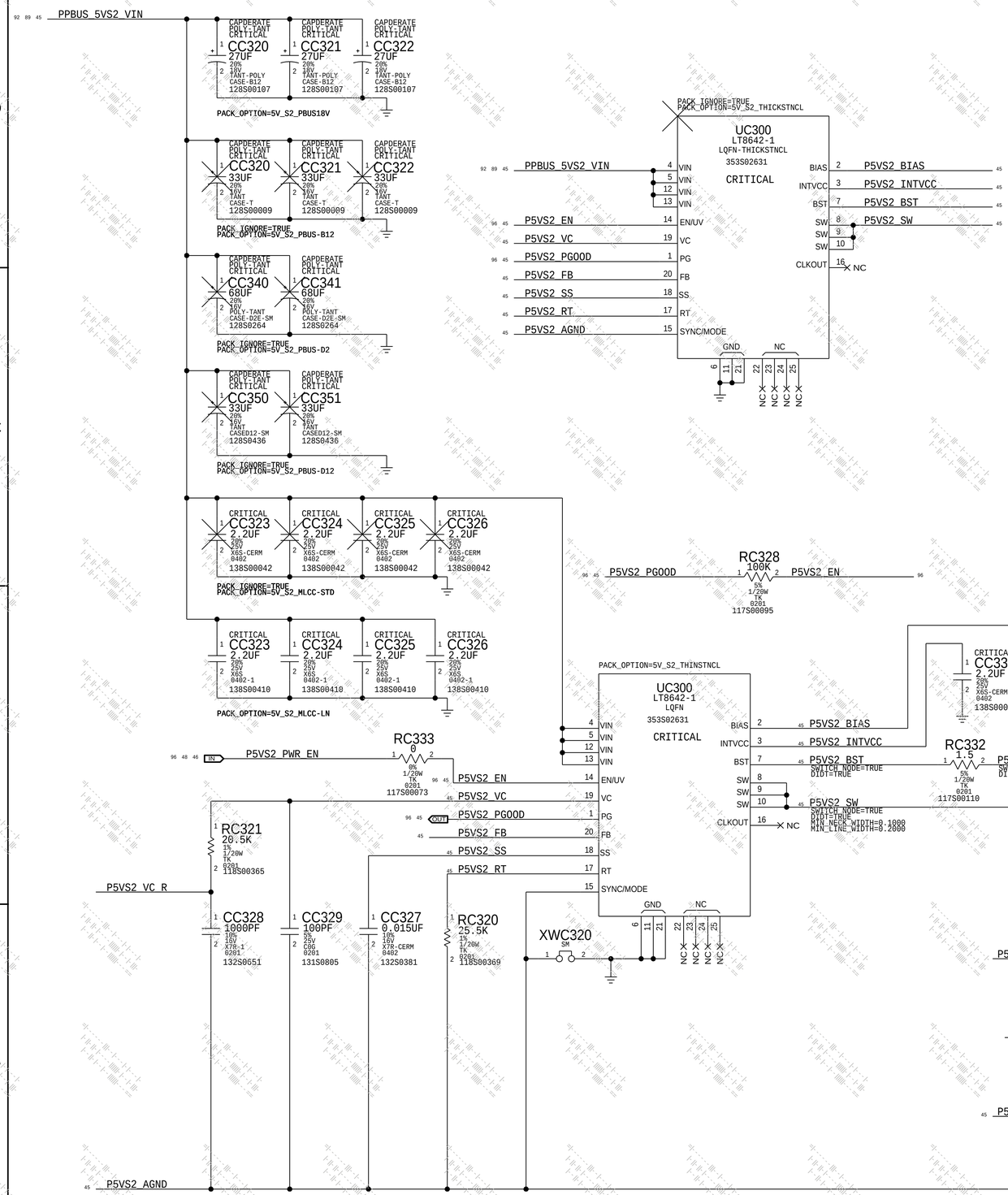
* OK2INTEGRATE *

5V_S2 Voltage Regulator



SET ONE OPTION FOR THE PBUS POLY CAPS

PACK_OPTION=5V_S2_PBUS-B12
PACK_OPTION=5V_S2_PBUS-D2
PACK_OPTION=5V_S2_PBUS-D12
PACK_OPTION=5V_S2_PBUS18V

SET ONE OPTION FOR THE OUTPUT CAPS

PACK_OPTION=5V_S2_VOUT-B2
PACK_OPTION=5V_S2_VOUT-B12

SET ONE OPTION FOR THE INDUCTOR

PACK_OPTION=5V_S2_IND-24
PACK_OPTION=5V_S2_IND-15

SET ONE OPTION FOR THE MLCC CAPS

PACK_OPTION=5V_S2_MLCC-STD
PACK_OPTION=5V_S2_MLCC-LN

SET ONE OPTION FOR UC300

PACK_OPTION=5V_S2_THINSTNCL
PACK_OPTION=5V_S2_THICKSTNCL

Startup time MIN/TYP/MAX 4.3/7.9/15.9 ms

Vout=5.15V
EDC=6.6A
F=1.5MHz

BOM_COST_GROUP=PLATFORM POWER

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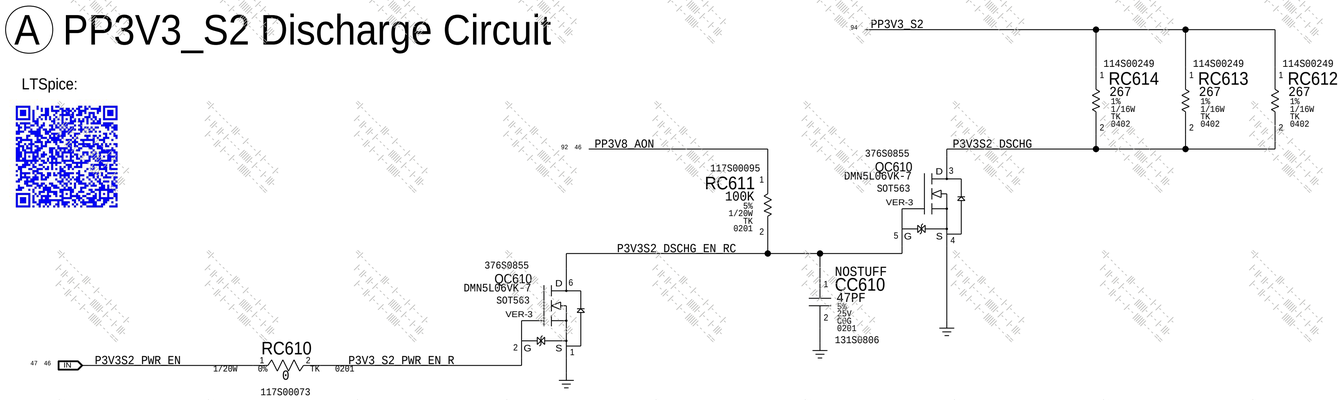
A PP3V3_S2 Discharge Circuit

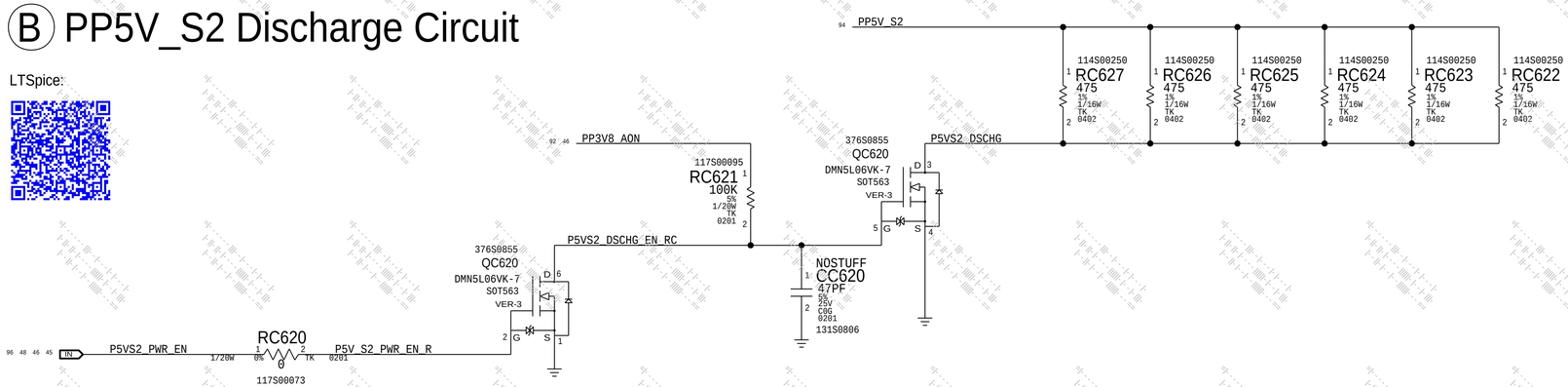
LTSpice:



$X2203GHUB/mlb/sim/ltspice/pp3v3_s2_discharge/pp3v3_s2_discharge_diodes_inc.asc

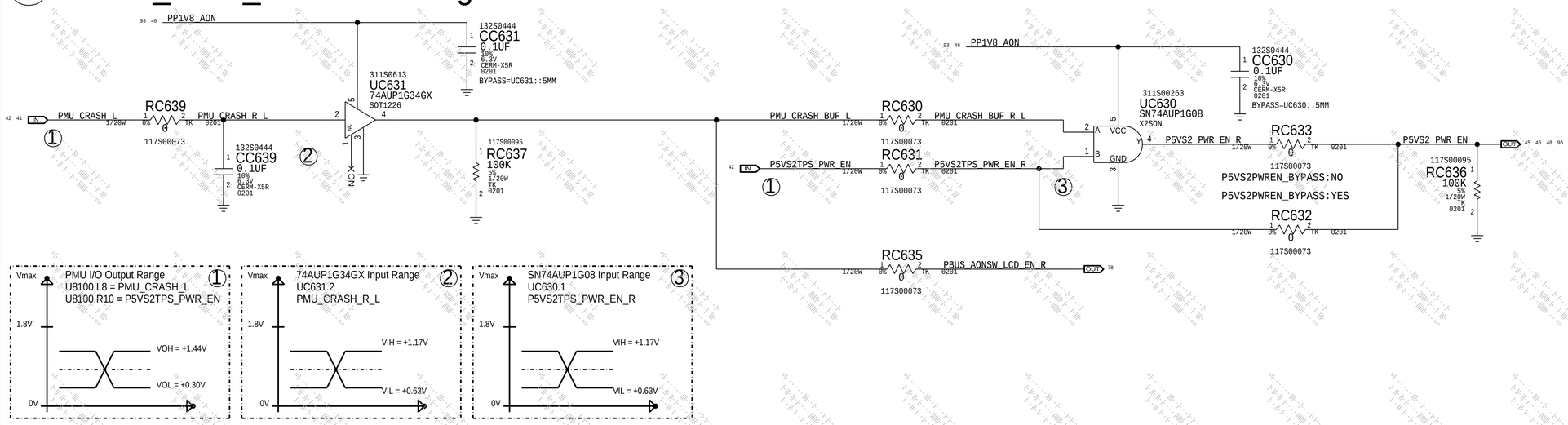
B PP5V_S2 Discharge Circuit

LTSpice:



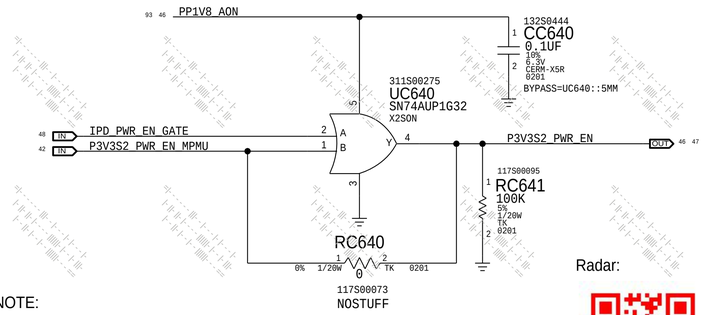
$X2203GHUB/mlb/sim/ltspice/pp5v_s2_discharge/pp5v_s2_discharge_diodes_inc.asc

C P5VS2_PWR_EN Control Logic



BOM_COST_GROUP=PLATFORM POWER

D P3V3S2_PWR_EN Control Logic



Radar:

NOTE:
Per Stowe PMU OTP, GPIO11 is OFF when the System is OFF.
A side-effect is that during the SIP_SMC->AWAKE transition the rail goes from ON->OFF->ON, which means we lose trackpad power during the OFF transition.
IPD_PWR_EN and PP5VS2_PWR_EN were moved to GPIOs that Stowe PMU can hold off.

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* OK2INTEGRATE *

3V3_S2 VR

SET ONE OPTION FOR PBUS CAPS

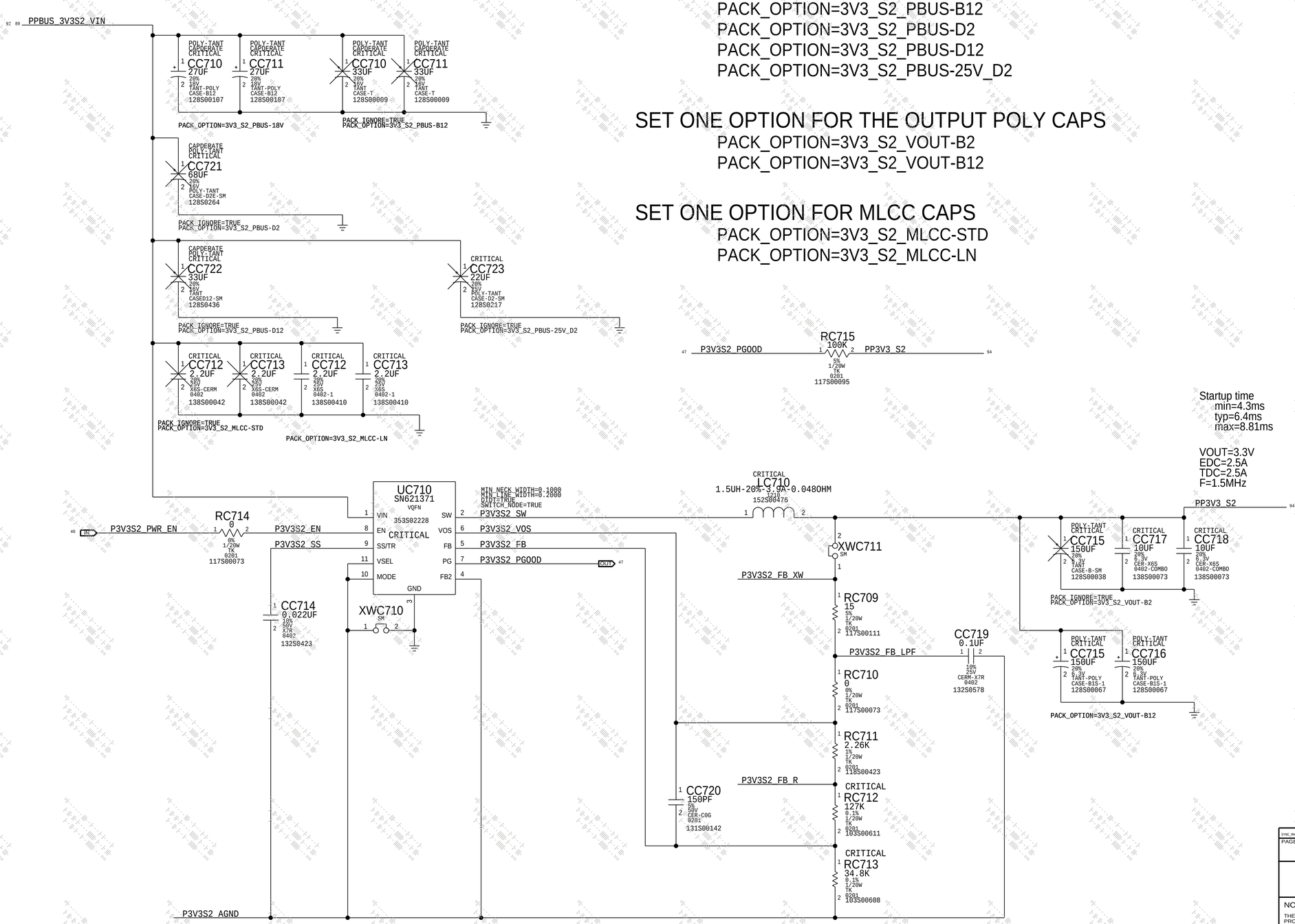
PACK_OPTION=3V3_S2_PBUS-18V
PACK_OPTION=3V3_S2_PBUS-B12
PACK_OPTION=3V3_S2_PBUS-D2
PACK_OPTION=3V3_S2_PBUS-D12
PACK_OPTION=3V3_S2_PBUS-25V_D2

SET ONE OPTION FOR THE OUTPUT POLY CAPS

PACK_OPTION=3V3_S2_VOUT-B2
PACK_OPTION=3V3_S2_VOUT-B12

SET ONE OPTION FOR MLCC CAPS

PACK_OPTION=3V3_S2_MLCC-STD
PACK_OPTION=3V3_S2_MLCC-LN



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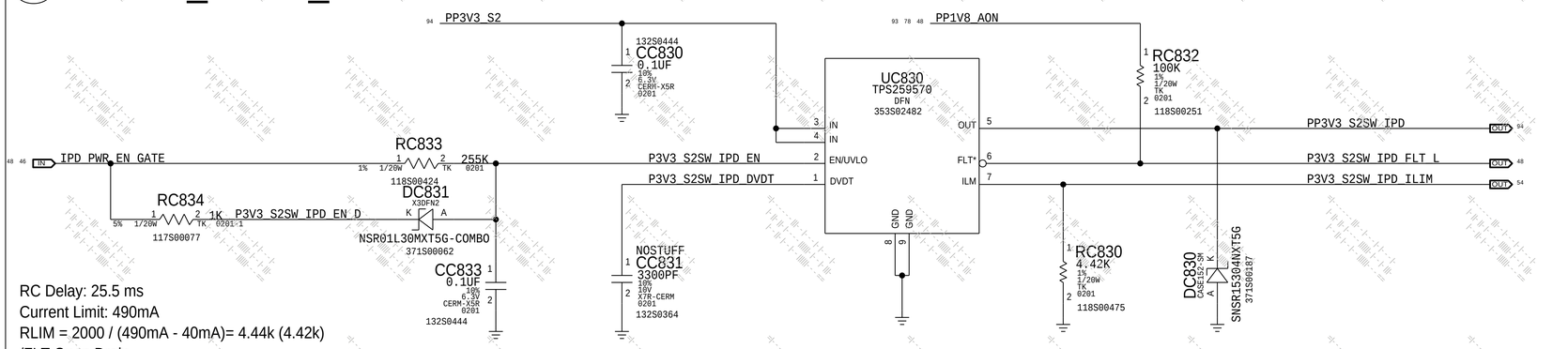
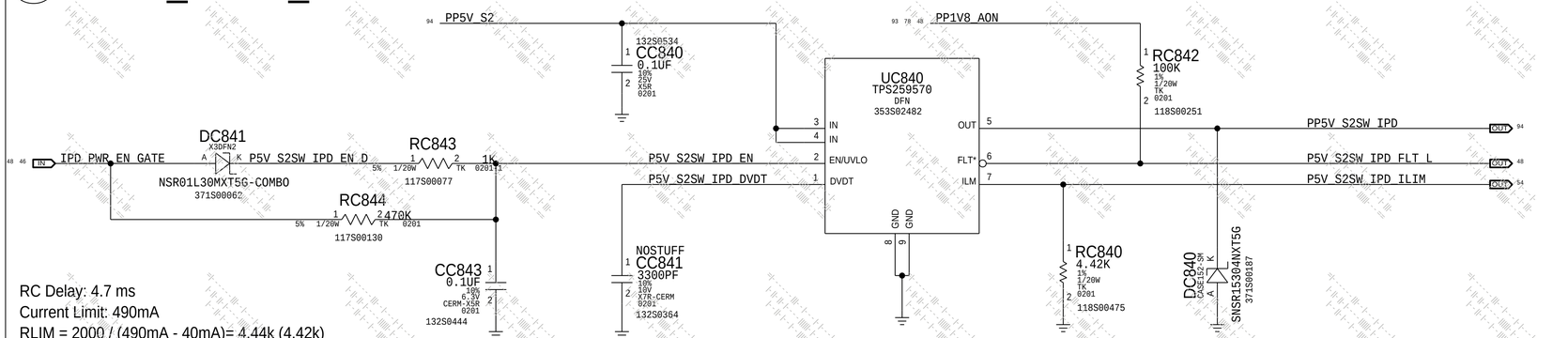
A PP3V3_S2SW_IPD Load Switch & e-Fuse



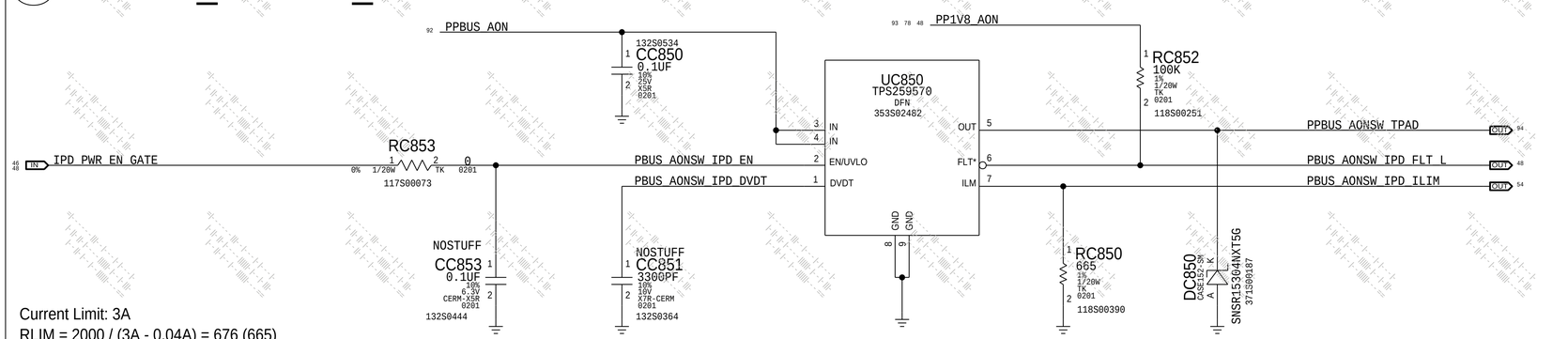
RC Delay: 25.5 ms
Current Limit: 490mA
RLIM = 2000 / (490mA - 40mA)= 4.44k (4.42k)
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))
$X2203GHUB/mlb/sim/ltspice/ocp_rc_filters/ocp_filters.asc

B PP5V_S2SW_IPD Load Switch & e-Fuse



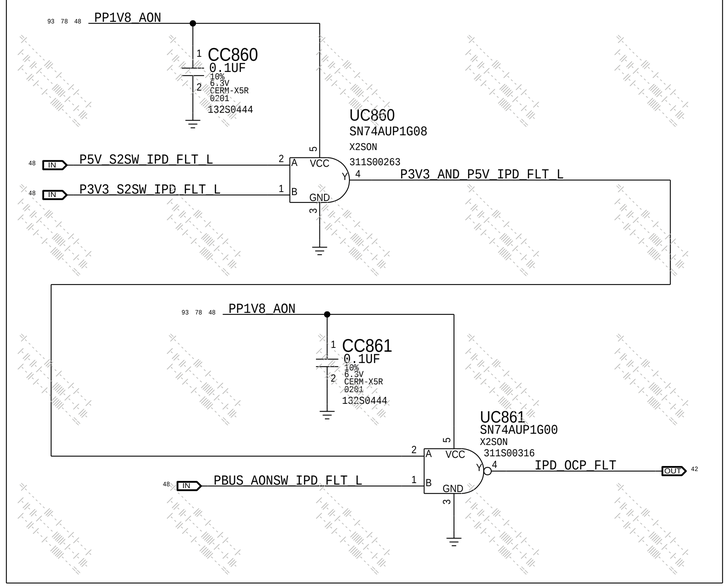
RC Delay: 4.7 ms
Current Limit: 490mA
RLIM = 2000 / (490mA - 40mA)= 4.44k (4.42k)
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))
$X2203GHUB/mlb/sim/ltspice/ocp_rc_filters/ocp_filters.asc

C PPBUS_AONSW_IPD Load Switch & e-Fuse

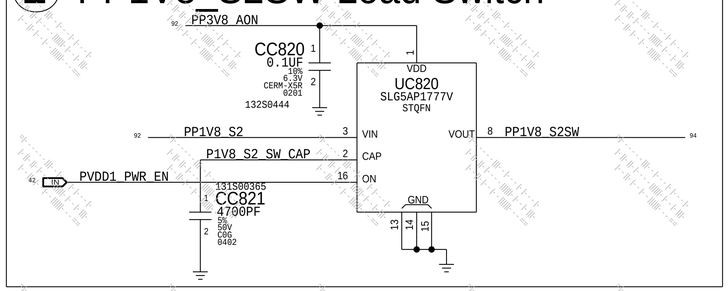


Current Limit: 3A
RLIM = 2000 / (3A - 0.04A) = 676 (665)
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))

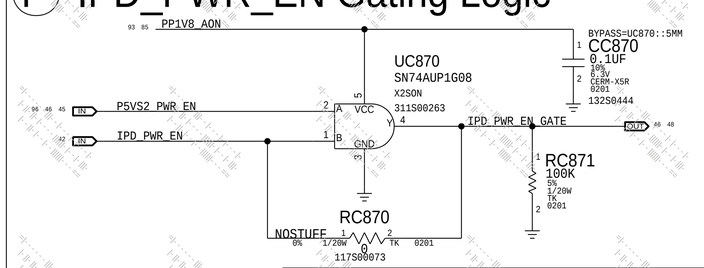
C IPD_OCP_FLT Control Logic



E PP1V8_S2SW Load Switch



F IPD_PWR_EN Gating Logic



BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: Power: Load Switches

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DRAWING NUMBER: 051-07020 SIZE: D
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BRANCH: evt-1
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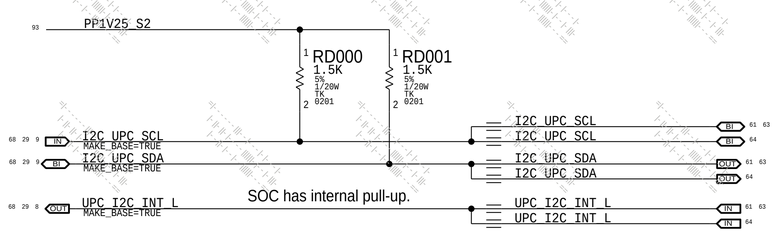
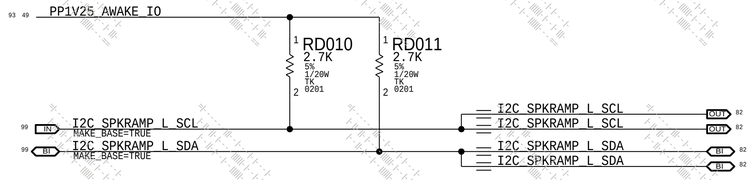
A AP_I2C0 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	0	400 kHZ	0X38	0X71	ACE2 - 0
AP	0	400 kHZ	0X3F	0X7F	ACE2 - 1
AP	0	400 kHZ	0X3A	0X75	ACE2 - MagSafe



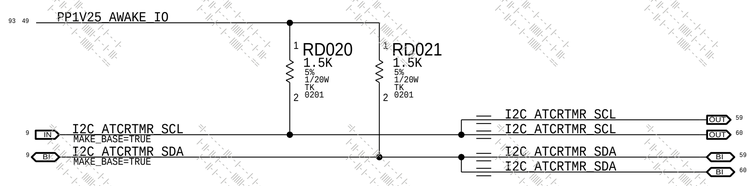
B AP_I2C1 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	1	400 kHZ	0X38	0X71	Left SpkrAmp A
AP	1	400 kHZ	0X39	0X73	Left SpkrAmp B



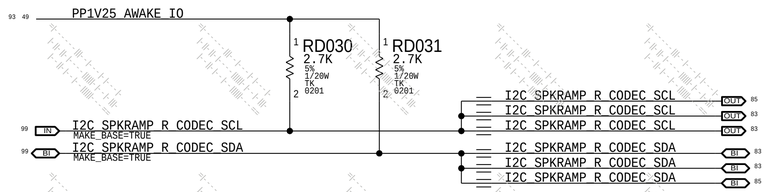
C AP_I2C2 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	2	100 kHZ/400 kHZ	0X18	0X31	RT13 Port 0
AP	2	100 kHZ/400 kHZ	0X19	0X33	RT13 Port 1



D AP_I2C3 - I2C Interface

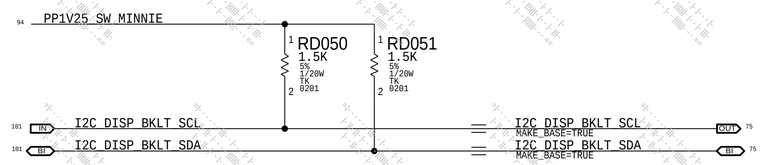
MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AP	3	400 kHZ	0X3B	0X77	Right SpkrAmp D
AP	3	400 kHZ	0X3C	0X79	Right SpkrAmp E
AP	3	400 kHZ	0X4B	0X97	CODEC



E AP_I2C4 - I2C Interface (Unused)

F DISP_I2C - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
DISP	0	100 kHZ	0X2F	0X5F	Minnie Bklt Drvr



BOM_COST_GROUP=SENSORS

SYNC_MASTER= SYNC_DATE=09/10/2021

PAGE TITLE: I2C: AP, DISP

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DRAWING NUMBER: 051-07020 SIZE: D

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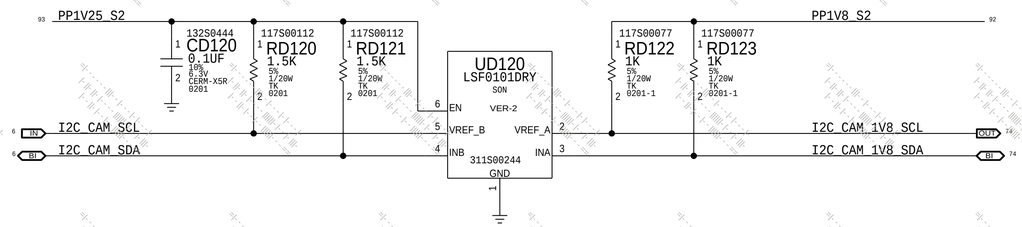
A ISP_I2C0 - I2C Interface

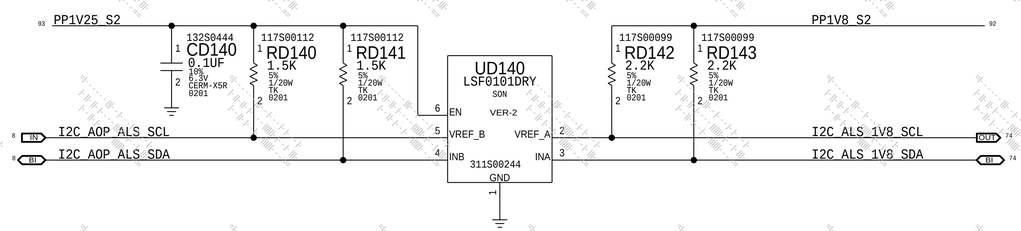
MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
ISP	0	400 kHz	0X10	0X21	Camera PMIC
ISP	0	400 kHz	0X36	0X6D	Image Sensor



B ISP_I2C1 - I2C Interface (Unused)

C AOP_I2CM0 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
AOP	0	400 kHz	0X48	0X91	TMP108
AOP	0	400 kHz	0X29	0X53	TETRA2 ALS



D AOP_I2CM1 - I2C Interface (Unused)

E AOP_I2CM2 - I2C Interface (Unused)

F SEP_I2C0 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SEP	0	400 kHz/1 MHz	0X71	0XE3	SEP Custom App
SEP	0	400 kHz/1 MHz	0X51	0XA3	SEP EEPROM App

I2C Pull-Ups at EEPROM (U1950)

BOM_COST_GROUP=SENSORS

SYNC_MASTER= SYNC_DATE=09/10/2021

PAGE TITLE: I2C: ISP, AOP, SEP

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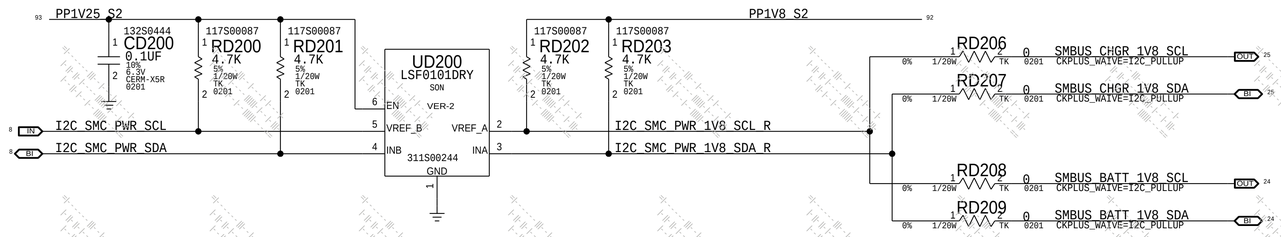
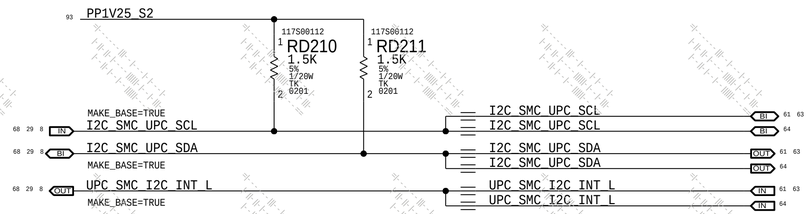
A SMC_I2C0 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	0	100 kHz	0X09	0X13	Whamola Charger
SMC	0	100 kHz	0X0B	0X16	Battery BMU
SMC	0	100 kHz	0X40	0X81	INA233 - U202
SMC	0	100 kHz	0X44	0X89	INA233 - U203
SMC	0	100 kHz	0X45	0X8B	INA233 - U201



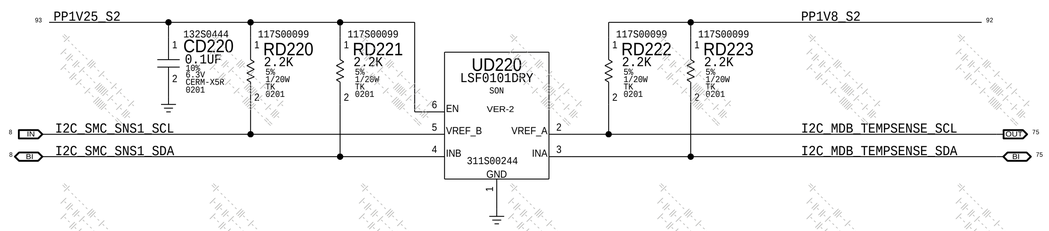
B SMC_I2C1 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	1	400 kHz	0X38	0X71	ACE2 - 0
SMC	1	400 kHz	0X3F	0X7F	ACE2 - 1
SMC	1	400 kHz	0X3A	0X75	ACE2 - MagSafe



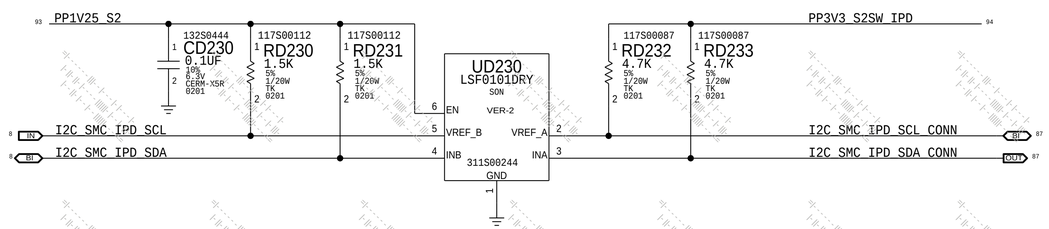
C SMC_I2C2 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	2	100 kHz	0X48	0X91	MDB - TMP468



D SMC_I2C3 - I2C Interface

MASTER	NUMBER	SPEED	7-BIT ADDR	8-BIT ADDR (R)	DEVICE
SMC	3	100 kHz	0X4C	0X99	PALM - TempSense



E SMC_I2C4 - I2C Interface (Unused)

BOM_COST_GROUP=SENSORS

SYNC_MASTER=jweb01 SYNC_DATE=09/28/2021

PAGE TITLE: I2C: SMC

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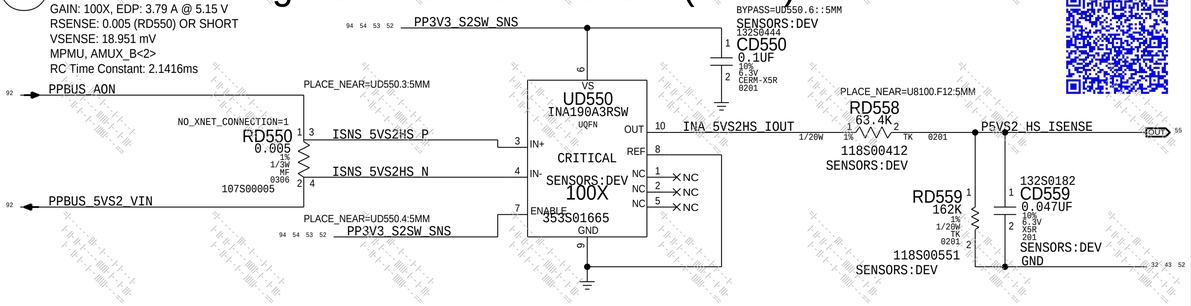
A 5V S2 VR High Side Current Sensor (IO5R)

GAIN: 100X, EDP: 3.79 A @ 5.15 V
RSENSE: 0.005 (RD550) OR SHORT
VSENSE: 18.951 mV
MPMU, AMUX_B<2>
RC Time Constant: 2.1416ms

LTSpice:

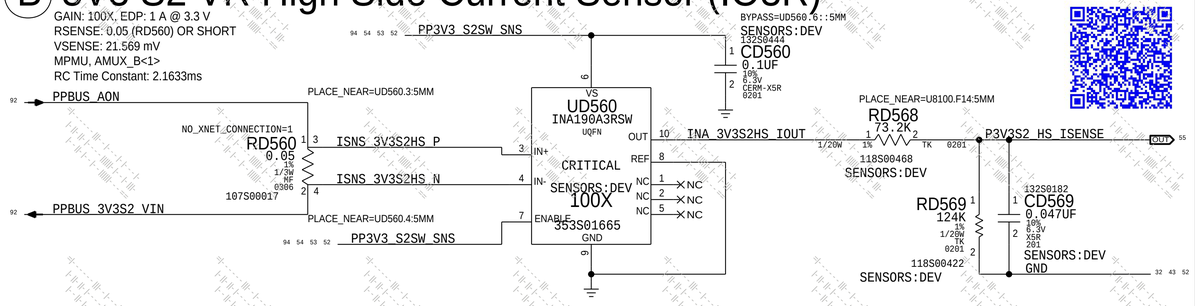


$X2203GHUB/mlb/sim/ltspice/io5r_p5vs2_hs_isense/io5r_p5vs2_hs_isense.asc

B 3V3 S2 VR High Side Current Sensor (IO3R)

GAIN: 100X, EDP: 1 A @ 3.3 V
RSENSE: 0.05 (RD560) OR SHORT
VSENSE: 21.569 mV
MPMU, AMUX_B<1>
RC Time Constant: 2.1633ms

LTSpice:

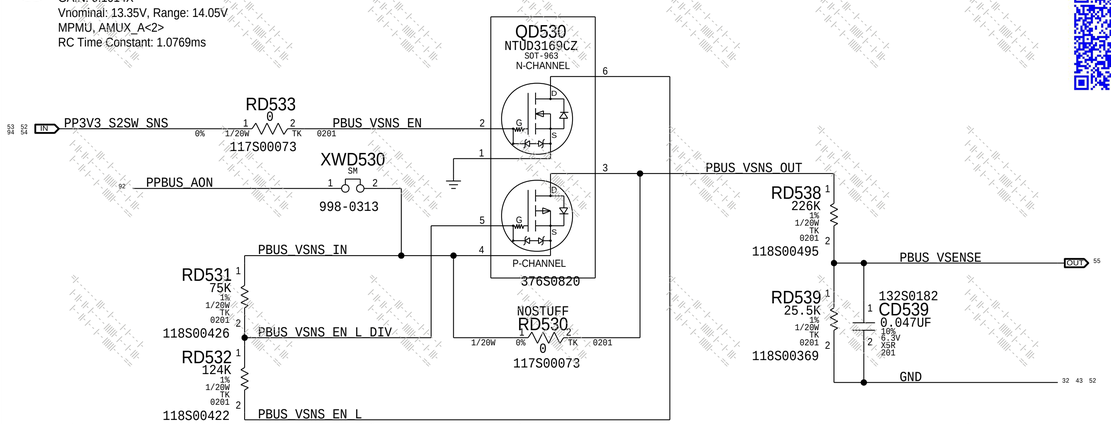


$X2203GHUB/mlb/sim/ltspice/io3r_p3v3s2_hs_isense/io3r_p3v3s2_hs_isense.asc

C PPBUS Voltage Sensor (VP0R)

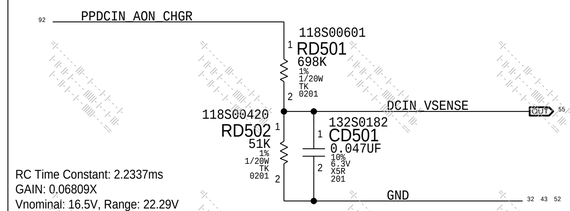
GAIN: 0.1014X
Vnominal: 13.35V, Range: 14.05V
MPMU, AMUX_A<2>
RC Time Constant: 1.0769ms

LTSpice:



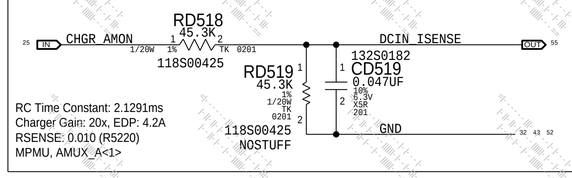
$X2203GHUB/mlb/sim/ltspice/vp0r_sense/vp0r_pbus_vsense_pulse_diodesinc.asc
$X2203GHUB/mlb/sim/ltspice/vp0r_sense/vp0r_pbus_vsense_pulse_onsemi.asc

D DCIN Voltage Sensor (VD0R)



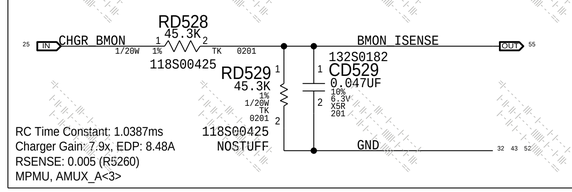
RC Time Constant: 2.2337ms
GAIN: 0.06809X
Vnominal: 16.5V, Range: 22.29V
MPMU, AMUX_A<0>

E DCIN Current Sensor (ID0R)



RC Time Constant: 2.1291ms
Charger Gain: 20x, EDP: 4.2A
RSENSE: 0.010 (R5220)
MPMU, AMUX_A<1>

F BMON Current Sensor (IPBR)



RC Time Constant: 1.0387ms
Charger Gain: 7.9x, EDP: 8.48A
RSENSE: 0.005 (R5260)
MPMU, AMUX_A<3>

G Production Sensor BOM Table

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00095	1	RES,TK,100K OHM,5%,,1/20W,0201	RD559		SENSORS:PROD
117S00095	1	RES,TK,100K OHM,5%,,1/20W,0201	RD569		SENSORS:PROD

BOM_COST_GROUP=SENSORS

PAGE TITLE: SENSORS: POWER HIGH SIDE (1/2)

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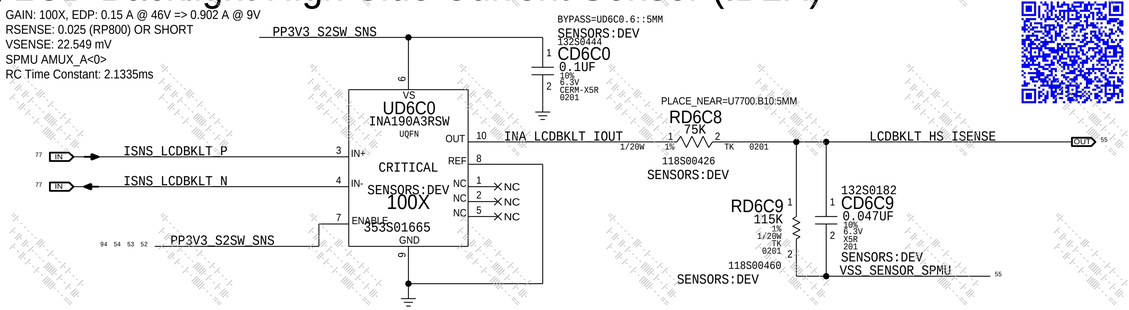
A LCD Backlight High Side Current Sensor (IBLR)

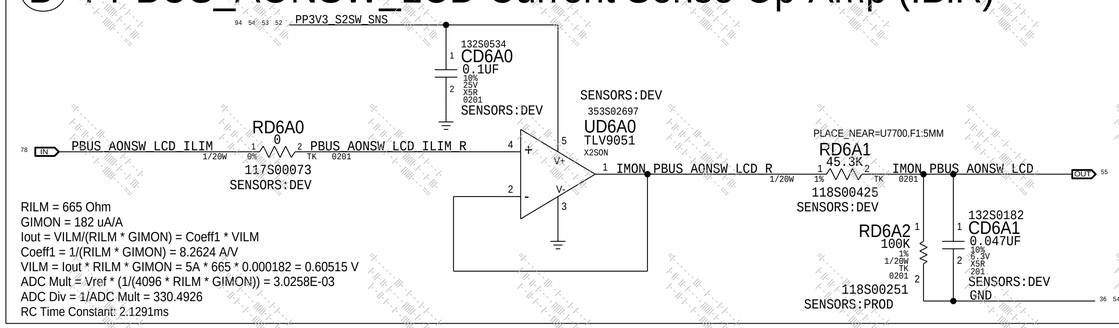
GAIN: 100X, EDP: 0.15 A @ 46V => 0.902 A @ 9V
RSENSE: 0.025 (RP800) OR SHORT
VSENSE: 22.549 mV
SPMU AMUX_A<0>
RC Time Constant: 2.1335ms

LTSpice:



$X2203GHUB/mlb/sim/ltspice/iblr_lcdbklt_hs_isense/iblr_lcdbklt_hs_isense.asc

B PPBUS_AONSW_LCD Current Sense Op-Amp (IBlR)



RILM = 665 Ohm
GIMON = 182 uA/A
Iout = VILM/(RILM * GIMON) = Coeff1 * VILM
Coeff1 = 1/(RILM * GIMON) = 8.2624 A/V
VILM = Iout * RILM * GIMON = 5A * 665 * 0.000182 = 0.60515 V
ADC Mult = Vref * (1/(4096 * RILM * GIMON)) = 3.0258E-03
ADC Div = 1/ADC Mult = 330.4926
RC Time Constant: 2.1291ms

C Production Sensor BOM Table

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00095	1	RES,TK,100K OHM,5%,,1/20W,0201	RD6C9		SENSORS:PROD

BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: POWER HIGH SIDE (2/2)

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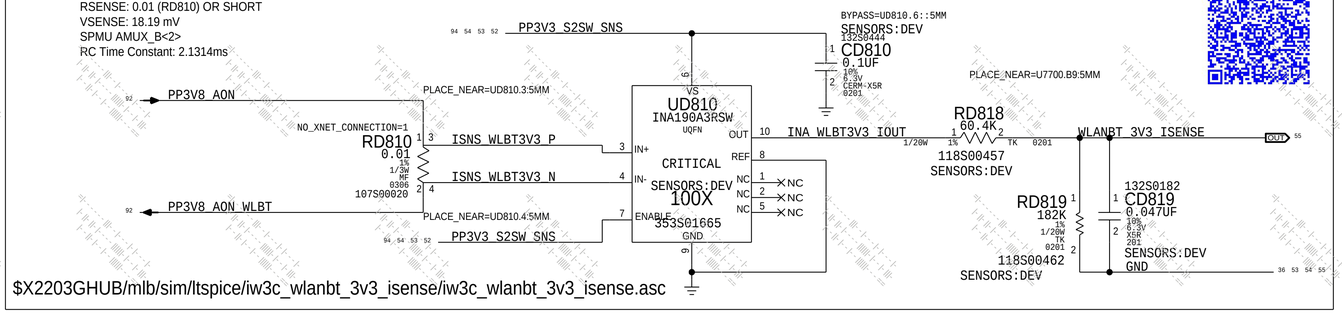
A WLAN BT 3V8 AON Current Sensor (IW3C)

GAIN: 100X, EDP: 1.819 A @ 3.8 V
RSENSE: 0.01 (RD810) OR SHORT
VSENSE: 18.19 mV
SPMU AMUX_B<2>
RC Time Constant: 2.1314ms

LTSpice:

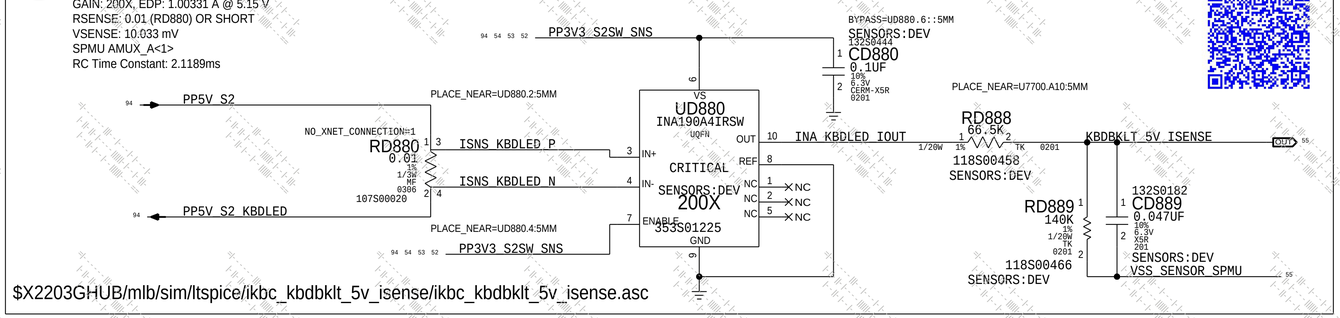


$X2203GHUB/mlb/sim/ltspice/iw3c_wlanbt_3v3_isense/iw3c_wlanbt_3v3_isense.asc

B Keyboard LED 5V Current Sensor (IKBC)

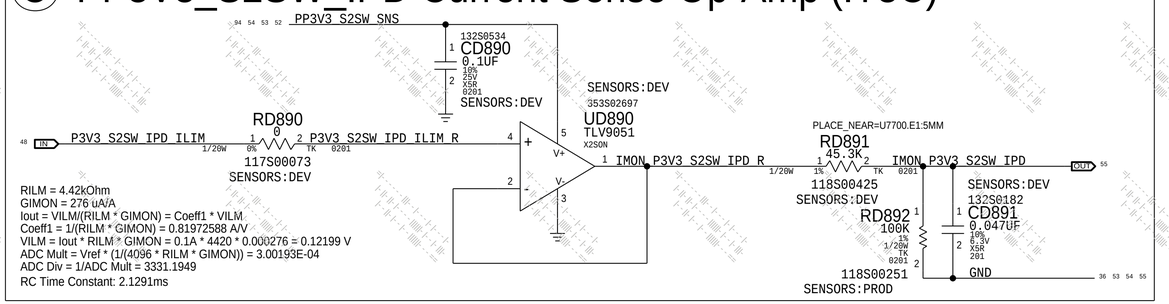
GAIN: 200X, EDP: 1.00331 A @ 5.15 V
RSENSE: 0.01 (RD880) OR SHORT
VSENSE: 10.033 mV
SPMU AMUX_A<1>
RC Time Constant: 2.1189ms

LTSpice:



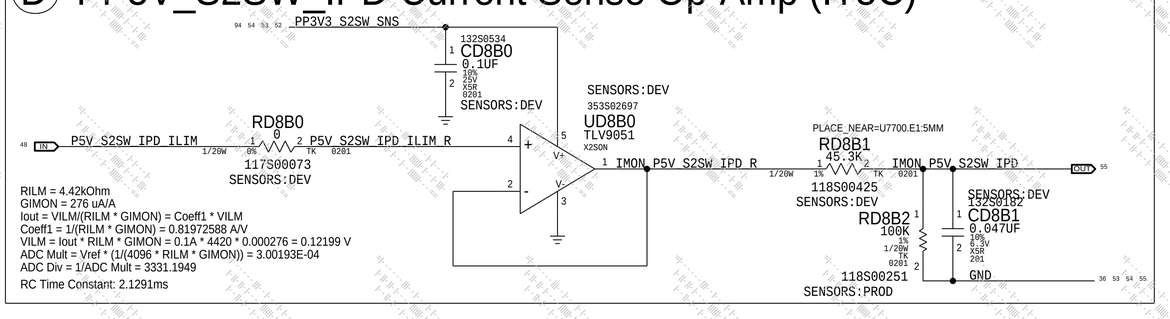
$X2203GHUB/mlb/sim/ltspice/ikbc_kbdbklt_5v_isense/ikbc_kbdbklt_5v_isense.asc

C PP3V3_S2SW_IPD Current Sense Op-Amp (IT3C)



RILM = 4.42kOhm
GIMON = 276 uA/A
Iout = VILM/(RILM * GIMON) = Coeff1 * VILM
Coeff1 = 1/(RILM * GIMON) = 0.81972588 A/V
VILM = Iout * RILM * GIMON = 0.1A * 4420 * 0.000276 = 0.12199 V
ADC Mult = Vref * (1/(4096 * RILM * GIMON)) = 3.00193E-04
ADC Div = 1/ADC Mult = 3331.1949
RC Time Constant: 2.1291ms

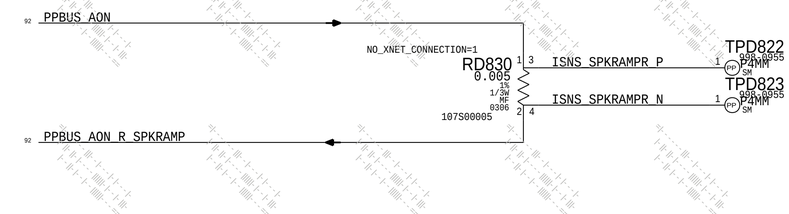
D PP5V_S2SW_IPD Current Sense Op-Amp (IT5C)



RILM = 4.42kOhm
GIMON = 276 uA/A
Iout = VILM/(RILM * GIMON) = Coeff1 * VILM
Coeff1 = 1/(RILM * GIMON) = 0.81972588 A/V
VILM = Iout * RILM * GIMON = 0.1A * 4420 * 0.000276 = 0.12199 V
ADC Mult = Vref * (1/(4096 * RILM * GIMON)) = 3.00193E-04
ADC Div = 1/ADC Mult = 3331.1949
RC Time Constant: 2.1291ms

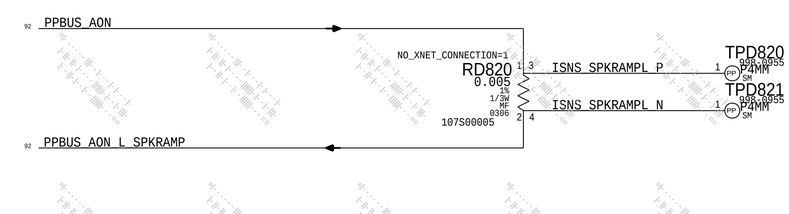
E Right Speaker Amplifier Current Sensor (Ixxx)

GAIN: 100X, EDP: 2.6 A
RSENSE: 0.005 (RD820) OR SHORT
VSENSE: 13 mV, RANGE: 3.3 A

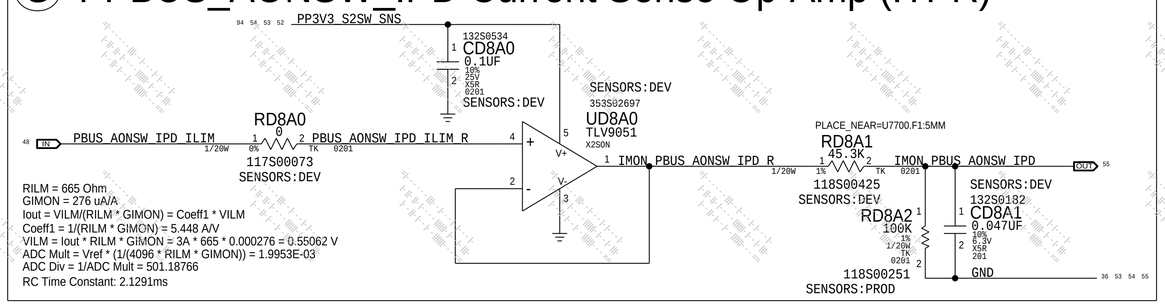


F Left Speaker Amplifier Current Sensor (Ixxx)

GAIN: 100X, EDP: 2.6 A
RSENSE: 0.005 (RD820) OR SHORT
VSENSE: 13 mV, RANGE: 3.3 A



G PPBUS_AONSW_IPD Current Sense Op-Amp (ITPR)



RILM = 665 Ohm
GIMON = 276 uA/A
Iout = VILM/(RILM * GIMON) = Coeff1 * VILM
Coeff1 = 1/(RILM * GIMON) = 5.448 A/V
VILM = Iout * RILM * GIMON = 3A * 665 * 0.000276 = 0.55062 V
ADC Mult = Vref * (1/(4096 * RILM * GIMON)) = 1.9953E-03
ADC Div = 1/ADC Mult = 501.18766
RC Time Constant: 2.1291ms

H Production Sensor BOM Table

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00095	1	RES,TK,100K OHM,5%,,1/20W,0201	RD819		SENSORS:PROD
117S00095	1	RES,TK,100K OHM,5%,,1/20W,0201	RD889		SENSORS:PROD

BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: POWER LOW SIDE (1/2)

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A ADC Input Aliases

MASTER PMU AMUX ALIAS

52	DCIN_VSENSE (MAKE_BASE=TRUE)	DCIN_VSENSE	41
52	DCIN_ISENSE (MAKE_BASE=TRUE)	DCIN_ISENSE	41
52	PBUS_VSENSE (MAKE_BASE=TRUE)	PBUS_VSENSE	41
52	BMON_ISENSE (MAKE_BASE=TRUE)	BMON_ISENSE	41
32	P3V8AON_IMEAS (MAKE_BASE=TRUE)	P3V8AON_IMEAS	41
52	P3V3S2_HS_ISENSE (MAKE_BASE=TRUE)	P3V3S2_HS_ISENSE	41
52	P5VS2_HS_ISENSE (MAKE_BASE=TRUE)	P5VS2_HS_ISENSE	41
55	MPMU_AMUXTDEV_TERM (MAKE_BASE=TRUE)	MPMU_AMUXTDEV_TERM	41

SLAVE PMU AMUX ALIAS

53	LCDBKLT_HS_ISENSE (MAKE_BASE=TRUE)	LCDBKLT_HS_ISENSE	35
56	KBDBKLT_5V_ISENSE (MAKE_BASE=TRUE)	KBDBKLT_5V_ISENSE	35
54	IMON_PBUS_AONSW_IPD (MAKE_BASE=TRUE)	IMON_PBUS_AONSW_IPD	35
54	IMON_P3V3_S2SW_IPD (MAKE_BASE=TRUE)	IMON_P3V3_S2SW_IPD	35
53	IMON_PBUS_AONSW_LCD (MAKE_BASE=TRUE)	IMON_PBUS_AONSW_LCD	35
56	IMON_P5V_S2SW_IPD (MAKE_BASE=TRUE)	IMON_P5V_S2SW_IPD	35
54	WLANBT_3V3_ISENSE (MAKE_BASE=TRUE)	WLANBT_3V3_ISENSE	35
55	SPMU_AMUXTDEV_TERM (MAKE_BASE=TRUE)	SPMU_AMUXTDEV_TERM	35

B SOC Sense Lines

102	VSNS_VDD_PCPU	PPE0A1 (P4MM SM)
102	VSNS_VSS_PCPU	PPE0A2 (P4MM SM)
102	VSNS_VDD_GPU	PPE0A3 (P4MM SM)
102	VSNS_VDD_SOC	PPE0A4 (P4MM SM)
102	VSNS_VDD_ECPU	PPE0A5 (P4MM SM)
102	VSNS_VDD_DISP	PPE0A6 (P4MM SM)
102	VSNS_ABSMIN_PCPU	PPE0A7 (P4MM SM)
102	VSNS_VSS_1	PPE0A8 (P4MM SM)
102	VSNS_VDD2H_1	PPE0A9 (P4MM SM)
102	VSNS_VSS_2	PPE0AA (P4MM SM)
102	VSNS_VDD2H_2	PPE0AB (P4MM SM)
102	VSNS_VDDQ_S1	PPE0AC (P4MM SM)
16	VDD_DCS_S1_SENSE	PPE0B0 (P4MM SM)
18	VDD_AMPH_S2_SENSE	PPE0B1 (P4MM SM)
18	VDD_VDDQ_S1_SENSE	PPE0B2 (P4MM SM)

PPE0AE (P4MM SM) — PLACE_NEAR=PPE0A3:2MM

PPE0AF (P4MM SM)

998-0955

C Unused MPMU AMUX/TDEV Termination

RECOMMENDED NOT TO LEAVE AMUX/TDEV FLOATING.

55 MPMU_AMUXTDEV_TERM
56 MPMU_AMUXTDEV_TERM
MPMU_AMUXTDEV_TERM (MAKE_BASE=TRUE)
RE010 100K 5% 1/20W TK 0201 117S00095

D Unused SPMU AMUX/TDEV Termination

RECOMMENDED NOT TO LEAVE AMUX/TDEV FLOATING.

55 SPMU_AMUXTDEV_TERM
56 SPMU_AMUXTDEV_TERM
56 SPMU_AMUXTDEV_TERM
SPMU_AMUXTDEV_TERM (MAKE_BASE=TRUE)
RE020 100K 5% 1/20W TK 0201 117S00095

E I/V Sensor Ground Reference Aliases

Slave PMU ADC Ground Alias

54 VSS_SENSOR_SPMU
53 VSS_SENSOR_SPMU
VSS_SENSOR_SPMU (MAKE_BASE=TRUE)
XWE020 (SM) 1 — 2 GND
36 53 54

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BOM_COST_GROUP=SENSORS

PAGE TITLE	SENSORS: POWER SUPPORT
Apple Inc.	DRAWING NUMBER 051-07020 — SIZE D
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A Master PMU TDEV1 (Txxx)

Location: TBD

55 MPMU_AMUXTDEV_TERM (MAKE_BASE=TRUE) = MPMU_AMUXTDEV_TERM OUT 41

B Master PMU TDEV2 (Tm0B)

Location: Ambient

THMSNS_MPMU2_P — 107S00460 RE121 10K-1% 0201-2 NO_XNET_CONNECTION=1 — PLACE_NEAR=XWE121.1:2MM 131S0805 CE121 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 — XWE121 SM 998-0313 NO_XNET_CONNECTION=1 PLACE_NEAR=U8100.F13:5MM — MPMU_TDEV2 OUT 41

THMSNS_MPMU2_N — XWE122 SM 998-0313 NO_XNET_CONNECTION=1 — THMSNS_MPMU_VSS 56

C Master PMU TDEV3 (TIOP)

Location: Thunderbolt Proximity

THMSNS_MPMU3_P — 107S00460 RE131 10K-1% 0201-2 NO_XNET_CONNECTION=1 — PLACE_NEAR=XWE131.1:2MM 131S0805 CE131 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 — XWE131 SM 998-0313 NO_XNET_CONNECTION=1 PLACE_NEAR=U8100.F9:5MM — MPMU_TDEV3 OUT 41

THMSNS_MPMU3_N — XWE132 SM 998-0313 NO_XNET_CONNECTION=1 — THMSNS_MPMU_VSS 56

D Master PMU TDEV4 (TW0P)

Location: Wireless Proximity

THMSNS_MPMU4_P — 107S00460 RE141 10K-1% 0201-2 NO_XNET_CONNECTION=1 — PLACE_NEAR=XWE141.1:2MM 131S0805 CE141 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 — XWE141 SM 998-0313 NO_XNET_CONNECTION=1 PLACE_NEAR=U8100.F10:5MM — MPMU_TDEV4 OUT 41

THMSNS_MPMU4_N — XWE142 SM 998-0313 NO_XNET_CONNECTION=1 — THMSNS_MPMU_VSS 56

E Master/Slave PMU VSS Connection

PLACE_NEAR=U8100.J11:5MM
XWE100 SM
56 THMSNS_MPMU_VSS — 1 — 2 — GND_TCAL_MPMU 41 43 56

PLACE_NEAR=U7700.C6:5MM
XWE1A0 SM
56 THMSNS_SPMU_VSS — 1 — 2 — GND_TCAL_SPMU 35 36

F Master PMU TDEV5 (TPMP)

Location: Master PMU Proximity

MPMU_TDEV5 OUT 41

107S00460 RE151 10K-1% 0201-2 NO_XNET_CONNECTION=1 — PLACE_NEAR=U8100.F11:5MM 131S0805 CE151 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1

GND_TCAL_MPMU 41 43 56

G Master PMU TDEV6 (T5SP)

Location: PP5V_S2 (UC300)

THMSNS_MPMU6_P — 107S00460 RE161 10K-1% 0201-2 NO_XNET_CONNECTION=1 — PLACE_NEAR=XWE161.1:2MM 131S0805 CE161 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 — XWE161 SM 998-0313 NO_XNET_CONNECTION=1 PLACE_NEAR=U8100.F12:5MM — MPMU_TDEV6 OUT 41

THMSNS_MPMU6_N — XWE162 SM 998-0313 NO_XNET_CONNECTION=1 — THMSNS_MPMU_VSS 56

H Master PMU TDEV7 (TCHP)

Location: Charger Proximity

THMSNS_MPMU7_P — 107S00460 RE171 10K-1% 0201-2 NO_XNET_CONNECTION=1 — PLACE_NEAR=XWE171.1:2MM 131S0805 CE171 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 — XWE171 SM 998-0313 NO_XNET_CONNECTION=1 PLACE_NEAR=U8100.G9:5MM — MPMU_TDEV7 OUT 41

THMSNS_MPMU7_N — XWE172 SM 998-0313 NO_XNET_CONNECTION=1 — THMSNS_MPMU_VSS 56

I Master PMU TDEV8 (TMVR)

Location: Main VR (PP3V8_AON_VDDMAIN)

THMSNS_MPMU8_P — 107S00460 RE181 10K-1% 0201-2 NO_XNET_CONNECTION=1 — PLACE_NEAR=XWE181.1:2MM 131S0805 CE181 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 — XWE181 SM 998-0313 NO_XNET_CONNECTION=1 PLACE_NEAR=U8100.G8:5MM — MPMU_TDEV8 OUT 41

THMSNS_MPMU8_N — XWE182 SM 998-0313 NO_XNET_CONNECTION=1 — THMSNS_MPMU_VSS 56

J Slave PMU TDEV1 (Txxx)

Location: TBD

55 SPMU_AMUXTDEV_TERM (MAKE_BASE=TRUE) = SPMU_AMUXTDEV_TERM OUT 35

K Slave PMU TDEV2 (TH0T)

Location: NAND Proximity

THMSNS_SPMU2_P — 107S00460 RE1C1 10K-1% 0201-2 NO_XNET_CONNECTION=1 — PLACE_NEAR=XWE1C1.1:2MM 131S0805 CE1C1 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 — XWE1C1 SM 998-0313 NO_XNET_CONNECTION=1 PLACE_NEAR=U7700.J1:5MM — SPMU_TDEV2 OUT 35

THMSNS_SPMU2_N — XWE1C2 SM 998-0313 NO_XNET_CONNECTION=1 — THMSNS_SPMU_VSS 56

L Slave PMU TDEV3 (Txxx)

Location: TBD

55 SPMU_AMUXTDEV_TERM (MAKE_BASE=TRUE) = SPMU_AMUXTDEV_TERM OUT 35

M Slave PMU TDEV4 (TSCD)

Location: SOC Proximity

THMSNS_SPMU4_P — 107S00460 RE1E1 10K-1% 0201-2 NO_XNET_CONNECTION=1 — PLACE_NEAR=XWE1E1.1:2MM 131S0805 CE1E1 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 — XWE1E1 SM 998-0313 NO_XNET_CONNECTION=1 PLACE_NEAR=U7700.G2:5MM — SPMU_TDEV4 OUT 35

THMSNS_SPMU4_N — XWE1E2 SM 998-0313 NO_XNET_CONNECTION=1 — THMSNS_SPMU_VSS 56

N Slave PMU TDEV5 (TPSP)

Location: Slave PMU Proximity

THMSNS_SPMU5_P — 107S00460 RE1F1 10K-1% 0201-2 NO_XNET_CONNECTION=1 — PLACE_NEAR=XWE1F1.1:2MM 131S0805 CE1F1 100PF 5% 25V C0G 0201 NO_XNET_CONNECTION=1 — XWE1F1 SM 998-0313 NO_XNET_CONNECTION=1 PLACE_NEAR=U7700.J2:5MM — SPMU_TDEV5 OUT 35

THMSNS_SPMU5_N — XWE1F2 SM 998-0313 NO_XNET_CONNECTION=1 — THMSNS_SPMU_VSS 56

BOM_COST_GROUP=SENSORS

SYNC_DATE=09/10/2021

PAGE TITLE: SENSORS: THERMAL

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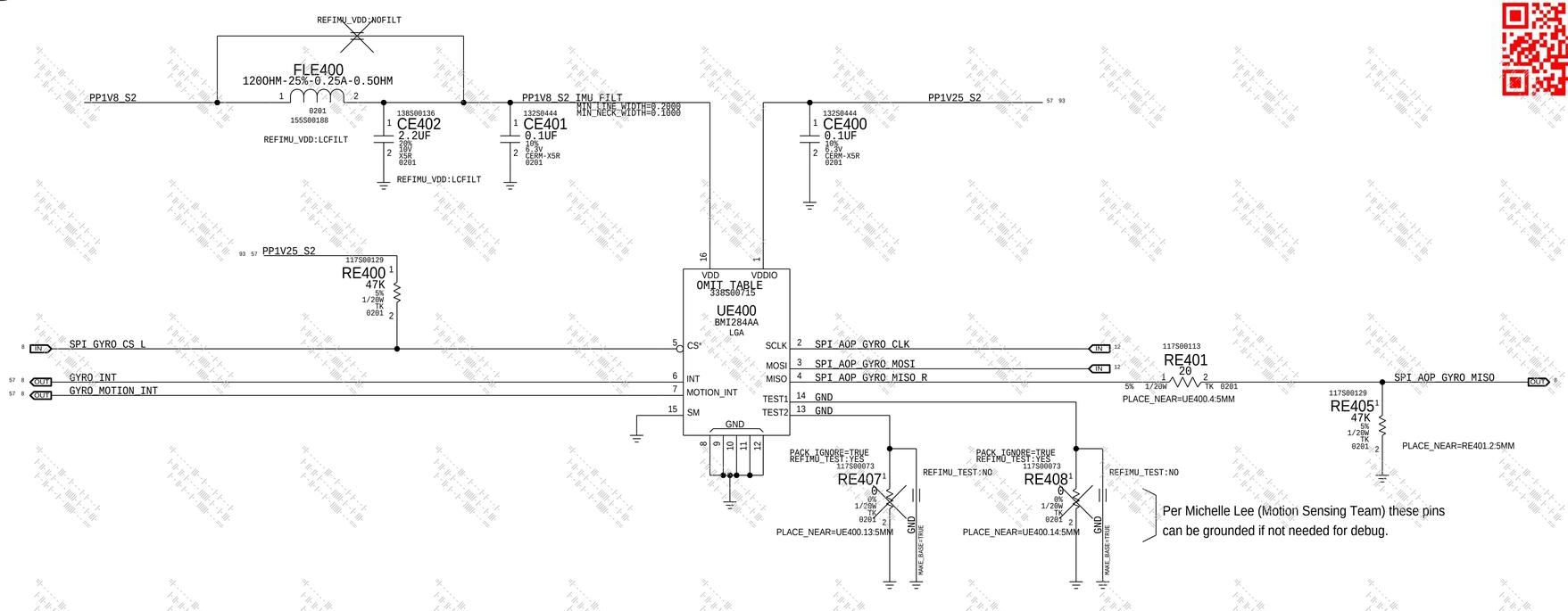
*** OK2INTEGRATE ***

A Sovereign Accelerometer and Gyroscope

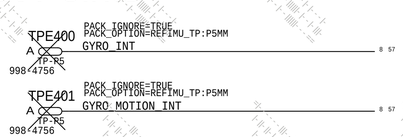
Datasheet Radar:



Per Michelle Lee (Motion Sensing Team) these pins can be grounded if not needed for debug.

MFG: Bosch
MPN: BMI284AA
APN: 338S00715
URL: https://www.bosch-sensortec.com/products/motion-sensors/imus/
Radar: rdar://61521702 (Sovereign: Datasheet)

B Test Points



C Sovereign BOM Options

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00715	1	IC,SOVEREIGN,BMI284,AA,LGA16	UE400	CRITICAL	REFIMU_IC:BMI284
338S00849	1	IC,SOVEREIGN2,BMI286,AA,LGA16	UE400	CRITICAL	REFIMU_IC:BMI286

BOM_COST_GROUP=SENSORS

PAGE TITLE
SENSORS: MOTION

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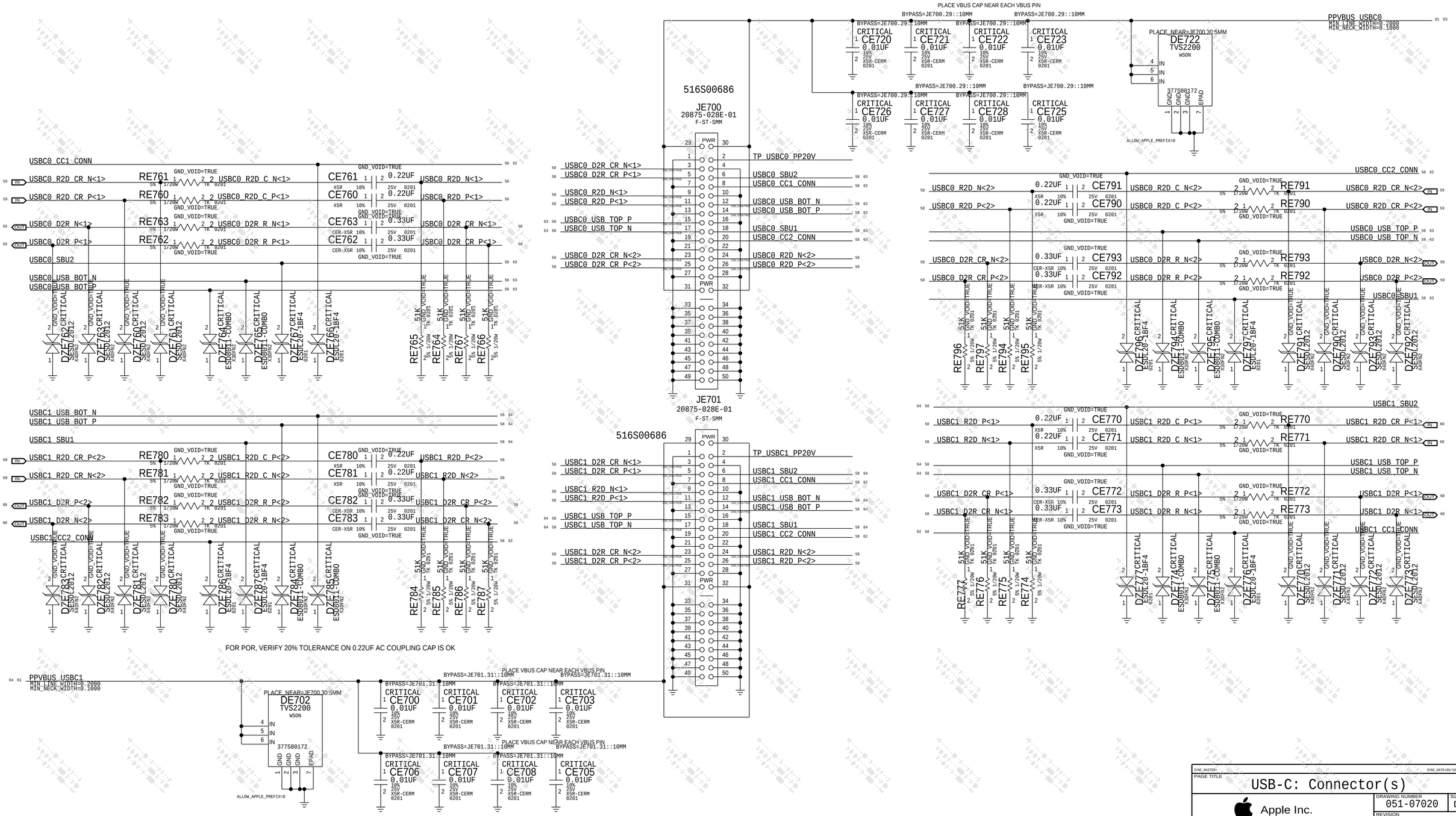
Left Rear Port



Left Front Port

BOM_COST_GROUP=USB-C

SYNC_MASTER= SYNC_DATE=05/10/2021

PAGE TITLE: USB-C: Connector(s)

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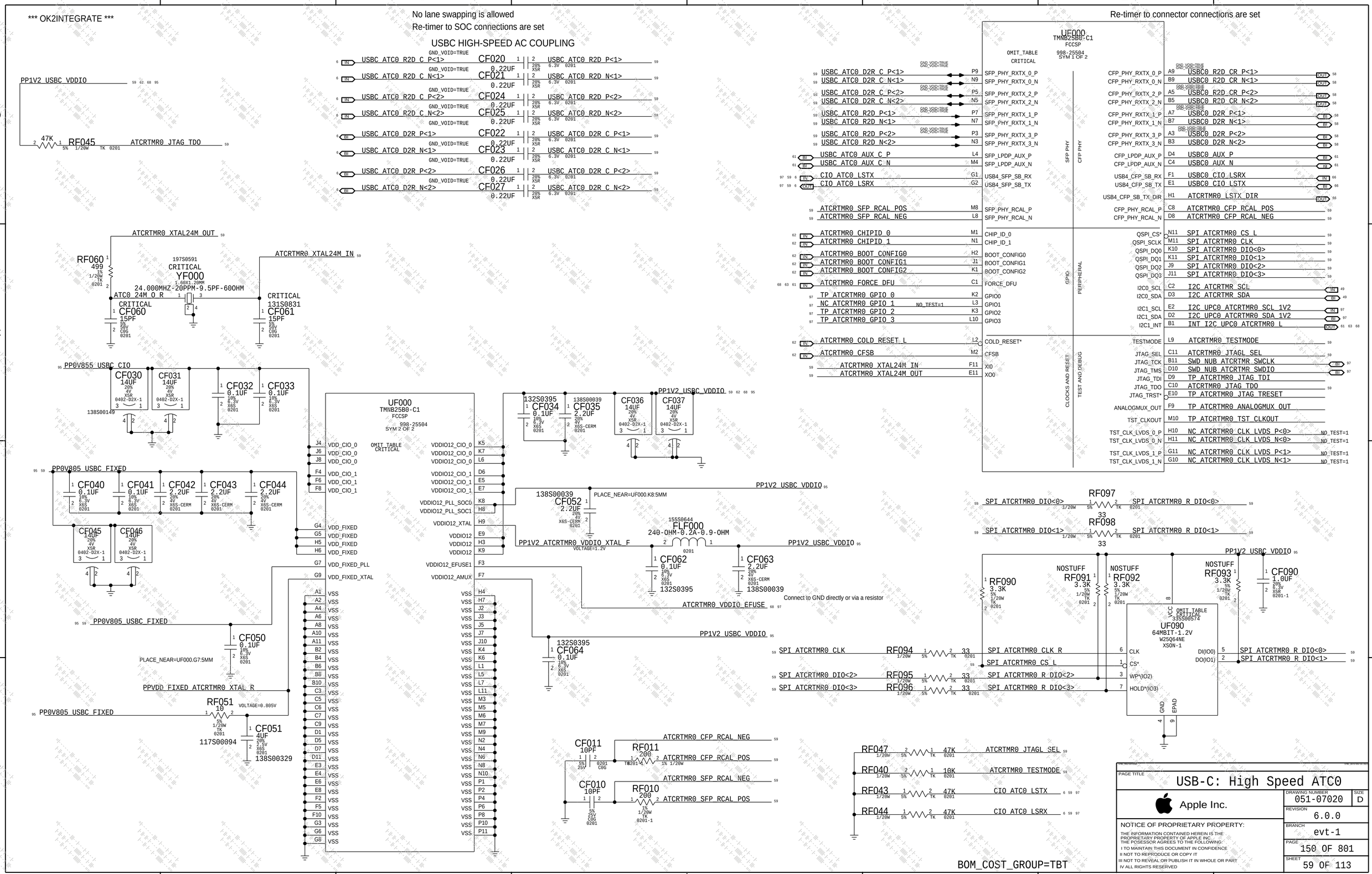
*** OK2INTEGRATE ***
No lane swapping is allowed
Re-timer to SOC connections are set
USBC HIGH-SPEED AC COUPLING
Re-timer to connector connections are set
PP1V2_USBC_VDDIO
RF045 47K
ATCRTMR0_JTAG_TDO
USBC_ATC0_R2D_C_P<1> CF020 0.22UF USBC_ATC0_R2D_P<1>
USBC_ATC0_R2D_C_N<1> CF021 0.22UF USBC_ATC0_R2D_N<1>
USBC_ATC0_R2D_C_P<2> CF024 0.22UF USBC_ATC0_R2D_P<2>
USBC_ATC0_R2D_C_N<2> CF025 0.22UF USBC_ATC0_R2D_N<2>
USBC_ATC0_D2R_P<1> CF022 0.22UF USBC_ATC0_D2R_C_P<1>
USBC_ATC0_D2R_N<1> CF023 0.22UF USBC_ATC0_D2R_C_N<1>
USBC_ATC0_D2R_P<2> CF026 0.22UF USBC_ATC0_D2R_C_P<2>
USBC_ATC0_D2R_N<2> CF027 0.22UF USBC_ATC0_D2R_C_N<2>
UF000 TMNB25B0-C1 FCCSP 998-25504 SYM 1 OF 2
OMIT_TABLE CRITICAL
USBC_ATC0_D2R_C_P<1> P9 SFP_PHY_RXTX_0_P
USBC_ATC0_D2R_C_N<1> N9 SFP_PHY_RXTX_0_N
USBC_ATC0_D2R_C_P<2> P5 SFP_PHY_RXTX_2_P
USBC_ATC0_D2R_C_N<2> N5 SFP_PHY_RXTX_2_N
USBC_ATC0_R2D_P<1> P7 SFP_PHY_RXTX_1_P
USBC_ATC0_R2D_N<1> N7 SFP_PHY_RXTX_1_N
USBC_ATC0_R2D_P<2> P3 SFP_PHY_RXTX_3_P
USBC_ATC0_R2D_N<2> N3 SFP_PHY_RXTX_3_N
USBC_ATC0_AUX_C_P L4 SFP_LPDP_AUX_P
USBC_ATC0_AUX_C_N M4 SFP_LPDP_AUX_N
CIO_ATC0_LSTX G1 USB4_SFP_SB_RX
CIO_ATC0_LSRX G2 USB4_SFP_SB_TX
ATCRTMR0_SFP_RCAL_POS M8 SFP_PHY_RCAL_P
ATCRTMR0_SFP_RCAL_NEG L8 SFP_PHY_RCAL_N
ATCRTMR0_CHIPID_0 M1 CHIP_ID_0
ATCRTMR0_CHIPID_1 N1 CHIP_ID_1
ATCRTMR0_BOOT_CONFIG0 H2 BOOT_CONFIG0
ATCRTMR0_BOOT_CONFIG1 J1 BOOT_CONFIG1
ATCRTMR0_BOOT_CONFIG2 K1 BOOT_CONFIG2
ATCRTMR0_FORCE_DFU C1 FORCE_DFU
TP_ATCRTMR0_GPIO_0 K2 GPIO0
NC_ATCRTMR0_GPIO_1 L3 GPIO1 NO_TEST=1
TP_ATCRTMR0_GPIO_2 K3 GPIO2
TP_ATCRTMR0_GPIO_3 L10 GPIO3
ATCRTMR0_COLD_RESET_L L2 COLD_RESET*
ATCRTMR0_CFSB M2 CFSB
ATCRTMR0_XTAL24M_IN F11 XI0
ATCRTMR0_XTAL24M_OUT E11 XO0
SFP PHY
GPIO
CLOCKS AND RESET
TEST AND DEBUG
CFP PHY
PERIPHERAL
CFP_PHY_RXTX_0_P A9 USBC0_R2D_CR_P<1>
CFP_PHY_RXTX_0_N B9 USBC0_R2D_CR_N<1>
CFP_PHY_RXTX_2_P A5 USBC0_R2D_CR_P<2>
CFP_PHY_RXTX_2_N B5 USBC0_R2D_CR_N<2>
CFP_PHY_RXTX_1_P A7 USBC0_D2R_P<1>
CFP_PHY_RXTX_1_N B7 USBC0_D2R_N<1>
CFP_PHY_RXTX_3_P A3 USBC0_D2R_P<2>
CFP_PHY_RXTX_3_N B3 USBC0_D2R_N<2>
CFP_LPDP_AUX_P D4 USBC0_AUX_P
CFP_LPDP_AUX_N C4 USBC0_AUX_N
USB4_CFP_SB_RX F1 USBC0_CIO_LSRX
USB4_CFP_SB_TX E1 USBC0_CIO_LSTX
USB4_CFP_SB_TX_DIR H1 ATCRTMR0_LSTX_DIR
CFP_PHY_RCAL_P C8 ATCRTMR0_CFP_RCAL_POS
CFP_PHY_RCAL_N D8 ATCRTMR0_CFP_RCAL_NEG
QSPI_CS* N11 SPI_ATCRTMR0_CS_L
QSPI_SCLK M11 SPI_ATCRTMR0_CLK
QSPI_DQ0 K10 SPI_ATCRTMR0_DIO<0>
QSPI_DQ1 K11 SPI_ATCRTMR0_DIO<1>
QSPI_DQ2 J9 SPI_ATCRTMR0_DIO<2>
QSPI_DQ3 J11 SPI_ATCRTMR0_DIO<3>
I2C0_SCL C2 I2C_ATCRTMR_SCL
I2C0_SDA D3 I2C_ATCRTMR_SDA
I2C1_SCL E2 I2C_UPC0_ATCRTMR0_SCL_1V2
I2C1_SDA D2 I2C_UPC0_ATCRTMR0_SDA_1V2
I2C1_INT B1 INT_I2C_UPC0_ATCRTMR0_L
TESTMODE L9 ATCRTMR0_TESTMODE
JTAG_SEL C11 ATCRTMR0_JTAGL_SEL
JTAG_TCK B11 SWD_NUB_ATCRTMR_SWCLK
JTAG_TMS D10 SWD_NUB_ATCRTMR_SWDIO
JTAG_TDI D9 TP_ATCRTMR0_JTAG_TDI
JTAG_TDO C10 ATCRTMR0_JTAG_TDO
JTAG_TRST* E10 TP_ATCRTMR0_JTAG_TRESET
ANALOGMUX_OUT F9 TP_ATCRTMR0_ANALOGMUX_OUT
TST_CLKOUT M10 TP_ATCRTMR0_TST_CLKOUT
TST_CLK_LVDS_0_P H10 NC_ATCRTMR0_CLK_LVDS_P<0> NO_TEST=1
TST_CLK_LVDS_0_N H11 NC_ATCRTMR0_CLK_LVDS_N<0> NO_TEST=1
TST_CLK_LVDS_1_P G11 NC_ATCRTMR0_CLK_LVDS_P<1> NO_TEST=1
TST_CLK_LVDS_1_N G10 NC_ATCRTMR0_CLK_LVDS_N<1> NO_TEST=1
ATCRTMR0_XTAL24M_OUT
ATCRTMR0_XTAL24M_IN
RF060 499 1% 1/20W TK 0201
197S0591 CRITICAL YF000 1.60X1.20MM 24.000MHZ-20PPM-9.5PF-60OHM
ATC0_24M_O_R
CRITICAL CF060 15PF 5% 50V C0G 0201
CRITICAL 131S0831 CF061 15PF 5% 50V C0G 0201
PP0V855_USBC_CIO
CF030 14UF 20% 4V X5R 0402-D2X-1 138S00149
CF031 14UF 20% 4V X5R 0402-D2X-1
CF032 0.1UF 10% 6.3V X6S 0201
CF033 0.1UF 10% 6.3V X6S 0201
UF000 TMNB25B0-C1 FCCSP 998-25504 SYM 2 OF 2
OMIT_TABLE CRITICAL
VDD_CIO_0 J4 J6 J8
VDD_CIO_1 F4 F6 F8
VDD_FIXED G4 G5 H5 H6
VDD_FIXED_PLL G7
VDD_FIXED_XTAL G9
VDDIO12_CIO_0 K5 K7 L6
VDDIO12_CIO_1 D6 E5 E7
VDDIO12_PLL_SOC0 K8
VDDIO12_PLL_SOC1 H8
VDDIO12_XTAL H9
VDDIO12 E9 H3 K9
VDDIO12_EFUSE1 F3
VDDIO12_AMUX F7
VSS
132S0395 CF034 0.1UF 10% 6.3V X6S 0201
138S00039 CF035 2.2UF 20% 4V X6S-CERM 0201
CF036 14UF 20% 4V X5R 0402-D2X-1
CF037 14UF 20% 4V X5R 0402-D2X-1
PP1V2_USBC_VDDIO
138S00039 CF052 2.2UF 20% 4V X6S-CERM 0201 PLACE_NEAR=UF000.K8:5MM
155S0644 FLF000 240-OHM-0.2A-0.9-OHM 0201
PP1V2_ATCRTMR0_VDDIO_XTAL_F VOLTAGE=1.2V
CF062 0.1UF 10% 6.3V X6S 0201 132S0395
CF063 2.2UF 20% 4V X6S-CERM 0201 138S00039
Connect to GND directly or via a resistor
ATCRTMR0_VDDIO_EFUSE
132S0395 CF064 0.1UF 10% 6.3V X6S 0201
PP0V805_USBC_FIXED
CF040 0.1UF 10% 6.3V X6S 0201
CF041 0.1UF 10% 6.3V X6S 0201
CF042 2.2UF 20% 4V X6S-CERM 0201
CF043 2.2UF 20% 4V X6S-CERM 0201
CF044 2.2UF 20% 4V X6S-CERM 0201
CF045 14UF 20% 4V X5R 0402-D2X-1
CF046 14UF 20% 4V X5R 0402-D2X-1
CF050 0.1UF 10% 6.3V X6S 0201
PLACE_NEAR=UF000.G7:5MM
PPVDD_FIXED_ATCRTMR0_XTAL_R
RF051 10 5% 1/20W TK 0201 VOLTAGE=0.805V
117S00094
CF051 4UF 20% 2.5V X6S 0201 138S00329
RF097 33 1/20W 5% TK 0201 SPI_ATCRTMR0_DIO<0> SPI_ATCRTMR0_R_DIO<0>
RF098 33 1/20W 5% TK 0201 SPI_ATCRTMR0_DIO<1> SPI_ATCRTMR0_R_DIO<1>
RF090 3.3K 5% 1/20W TK 0201
NOSTUFF RF091 3.3K 5% 1/20W TK 0201
NOSTUFF RF092 3.3K 5% 1/20W TK 0201
NOSTUFF RF093 3.3K 5% 1/20W TK 0201
CF090 1.0UF 20% 6.3V X5R 0201-1
UF090 64MBIT-1.2V W25Q64NE XSON-1 335S00574
OMIT_TABLE CRITICAL
SPI_ATCRTMR0_CLK RF094 33 SPI_ATCRTMR0_CLK_R
SPI_ATCRTMR0_CS_L
SPI_ATCRTMR0_DIO<2> RF095 33 SPI_ATCRTMR0_R_DIO<2>
SPI_ATCRTMR0_DIO<3> RF096 33 SPI_ATCRTMR0_R_DIO<3>
CLK CS* WP*(IO2) HOLD*(IO3) DI(IO0) DO(IO1) GND EPAD
SPI_ATCRTMR0_R_DIO<0> SPI_ATCRTMR0_R_DIO<1>
CF011 10PF 5% 25V C0G ATCRTMR0_CFP_RCAL_NEG
RF011 200 1% 1/20W TK 0201-1 ATCRTMR0_CFP_RCAL_POS
CF010 10PF 5% 25V C0G ATCRTMR0_SFP_RCAL_NEG
RF010 200 1% 1/20W TK 0201-1 ATCRTMR0_SFP_RCAL_POS
RF047 47K ATCRTMR0_JTAGL_SEL
RF040 10K ATCRTMR0_TESTMODE
RF043 47K CIO_ATC0_LSTX
RF044 47K CIO_ATC0_LSRX
BOM_COST_GROUP=TBT
PAGE TITLE USB-C: High Speed ATC0
Apple Inc.
DRAWING NUMBER 051-07020
SIZE D
REVISION 6.0.0
BRANCH evt-1
PAGE 150 OF 801
SHEET 59 OF 113
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*** OK2INTEGRATE ***

No lane swapping is allowed

Re-timer to SOC connections are set

Re-timer to connector connections are set

USBC HIGH-SPEED AC COUPLING

USBC_ATC1_R2D_C_P<1>	CF120 0.22UF	USBC_ATC1_R2D_P<1>		
USBC_ATC1_R2D_C_N<1>	CF121 0.22UF	USBC_ATC1_R2D_N<1>		
USBC_ATC1_R2D_C_P<2>	CF124 0.22UF	USBC_ATC1_R2D_P<2>		
USBC_ATC1_R2D_C_N<2>	CF125 0.22UF	USBC_ATC1_R2D_N<2>		
USBC_ATC1_D2R_P<1>	CF122 0.22UF	USBC_ATC1_D2R_C_P<1>		
USBC_ATC1_D2R_N<1>	CF123 0.22UF	USBC_ATC1_D2R_C_N<1>		
USBC_ATC1_D2R_P<2>	CF126 0.22UF	USBC_ATC1_D2R_C_P<2>		
USBC_ATC1_D2R_N<2>	CF127 0.22UF	USBC_ATC1_D2R_C_N<2>		

PP1V2_USBC_VDDIO — RF145 47K 5% 1/20W TK 0201 — ATCRTMR1_JTAG_TDO

ATCRTMR1_XTAL24M_OUT — RF160 499 1% 1/20W TK 0201 — ATCRTMR1_XTAL24M_IN

197S0591 CRITICAL YF100 1.00X1.20MM 24.000MHZ-20PPM-9.5PF-600HM

ATC1_24M_O_R — CRITICAL CF160 15PF 5% 50V C0G 0201 — CRITICAL 131S0831 CF161 15PF 5% 50V C0G 0201

PP0V855_USBC_CIO — CF130 14UF 20% 4V X5R 0402-D2X-1 (138S00149) — CF131 14UF 20% 4V X5R 0402-D2X-1 — CF132 0.1UF 10% 6.3V X6S 0201 — CF133 0.1UF 10% 6.3V X6S 0201

PP0V805_USBC_FIXED — CF140 0.1UF 10% 6.3V X6S 0201 — CF141 0.1UF 10% 6.3V X6S 0201 — CF142 2.2UF 20% 4V X6S-CERM 0201 — CF143 2.2UF 20% 4V X6S-CERM 0201 — CF144 2.2UF 20% 4V X6S-CERM 0201

CF145 14UF 20% 4V X5R 0402-D2X-1 — CF146 14UF 20% 4V X5R 0402-D2X-1

PP0V805_USBC_FIXED — CF150 0.1UF 10% 6.3V X6S 0201 — PLACE_NEAR=UF100.G7:5MM

PPVDD_FIXED_ATCRTMR1_XTAL_R — RF151 10 5% 1/20W TK 0201 (117S00094) — VOLTAGE=0.805V — CF151 4UF 20% 2.5V X6S 0201 (138S00329)

PP0V805_USBC_FIXED

UF100 TMNB25B0-C1 FCCSP 998-25504 SYM 2 OF 2

OMIT_TABLE CRITICAL

Pin	Net
J4	VDD_CIO_0
J6	VDD_CIO_0
J8	VDD_CIO_0
F4	VDD_CIO_1
F6	VDD_CIO_1
F8	VDD_CIO_1
G4	VDD_FIXED
G5	VDD_FIXED
H5	VDD_FIXED
H6	VDD_FIXED
G7	VDD_FIXED_PLL
G9	VDD_FIXED_XTAL
A1	VSS
A2	VSS
A4	VSS
A6	VSS
A8	VSS
A10	VSS
A11	VSS
B2	VSS
B4	VSS
B6	VSS
B8	VSS
B10	VSS
C3	VSS
C5	VSS
C6	VSS
C7	VSS
C9	VSS
D1	VSS
D5	VSS
D7	VSS
D11	VSS
E3	VSS
E4	VSS
E6	VSS
E8	VSS
F2	VSS
F5	VSS
F10	VSS
G3	VSS
G6	VSS
G8	VSS
K5	VDDIO12_CIO_0
K7	VDDIO12_CIO_0
L6	VDDIO12_CIO_0
D6	VDDIO12_CIO_1
E5	VDDIO12_CIO_1
E7	VDDIO12_CIO_1
K8	VDDIO12_PLL_SOC0
H8	VDDIO12_PLL_SOC1
H9	VDDIO12_XTAL
E9	VDDIO12
H3	VDDIO12
K9	VDDIO12
F3	VDDIO12_EFUSE1
F7	VDDIO12_AMUX
H4	VSS
H7	VSS
J2	VSS
J3	VSS
J5	VSS
J7	VSS
J10	VSS
K4	VSS
K6	VSS
L1	VSS
L5	VSS
L7	VSS
L11	VSS
M3	VSS
M5	VSS
M6	VSS
M7	VSS
M9	VSS
N2	VSS
N4	VSS
N6	VSS
N8	VSS
N10	VSS
P1	VSS
P2	VSS
P4	VSS
P6	VSS
P8	VSS
P10	VSS
P11	VSS

132S0395 CF134 0.1UF 10% 6.3V X6S 0201 — 138S00039 CF135 2.2UF 20% 4V X6S-CERM 0201 — CF136 14UF 20% 4V X5R 0402-D2X-1 — CF137 14UF 20% 4V X5R 0402-D2X-1 — PP1V2_USBC_VDDIO

138S00039 CF152 2.2UF 20% 4V X6S-CERM 0201 — PLACE_NEAR=UF100.K8:5MM — PP1V2_USBC_VDDIO

155S0644 FLF100 240-OHM-0.2A-0.9-OHM 0201

PP1V2_ATCRTMR1_VDDIO_XTAL_F (VOLTAGE=1.2V) — CF162 0.1UF 10% 6.3V X6S 0201 (132S0395) — PP1V2_USBC_VDDIO — CF163 2.2UF 20% 4V X6S-CERM 0201 (138S00039)

ATCRTMR1_VDDIO_EFUSE

Connect to GND directly or via a resistor

132S0395 CF164 0.1UF 10% 6.3V X6S 0201 — PP1V2_USBC_VDDIO

UF100 TMNB25B0-C1 FCCSP 998-25504 SYM 1 OF 2

OMIT_TABLE CRITICAL

Pin	Net	Group
P9	SFP_PHY_RXTX_0_P	SFP PHY
N9	SFP_PHY_RXTX_0_N	SFP PHY
P5	SFP_PHY_RXTX_2_P	SFP PHY
N5	SFP_PHY_RXTX_2_N	SFP PHY
P7	SFP_PHY_RXTX_1_P	SFP PHY
N7	SFP_PHY_RXTX_1_N	SFP PHY
P3	SFP_PHY_RXTX_3_P	SFP PHY
N3	SFP_PHY_RXTX_3_N	SFP PHY
L4	SFP_LPDP_AUX_P	SFP PHY
M4	SFP_LPDP_AUX_N	SFP PHY
G1	USB4_SFP_SB_RX	SFP PHY
G2	USB4_SFP_SB_TX	SFP PHY
M8	SFP_PHY_RCAL_P	SFP PHY
L8	SFP_PHY_RCAL_N	SFP PHY
M1	CHIP_ID_0	GPIO
N1	CHIP_ID_1	GPIO
H2	BOOT_CONFIG0	GPIO
J1	BOOT_CONFIG1	GPIO
K1	BOOT_CONFIG2	GPIO
C1	FORCE_DFU	GPIO
K2	GPIO0	GPIO
L3	GPIO1	GPIO
K3	GPIO2	GPIO
L10	GPIO3	GPIO
L2	COLD_RESET*	CLOCKS AND RESET
M2	CFSB	CLOCKS AND RESET
F11	XI0	CLOCKS AND RESET
E11	XO0	CLOCKS AND RESET
A9	CFP_PHY_RXTX_0_P	PERIPHERAL
B9	CFP_PHY_RXTX_0_N	PERIPHERAL
A5	CFP_PHY_RXTX_2_P	PERIPHERAL
B5	CFP_PHY_RXTX_2_N	PERIPHERAL
A7	CFP_PHY_RXTX_1_P	PERIPHERAL
B7	CFP_PHY_RXTX_1_N	PERIPHERAL
A3	CFP_PHY_RXTX_3_P	PERIPHERAL
B3	CFP_PHY_RXTX_3_N	PERIPHERAL
D4	CFP_LPDP_AUX_P	PERIPHERAL
C4	CFP_LPDP_AUX_N	PERIPHERAL
F1	USB4_CFP_SB_RX	PERIPHERAL
E1	USB4_CFP_SB_TX	PERIPHERAL
H1	USB4_CFP_SB_TX_DIR	PERIPHERAL
C8	CFP_PHY_RCAL_P	PERIPHERAL
D8	CFP_PHY_RCAL_N	PERIPHERAL
N11	QSPI_CS*	PERIPHERAL
M11	QSPI_SCLK	PERIPHERAL
K10	QSPI_DQ0	PERIPHERAL
K11	QSPI_DQ1	PERIPHERAL
J9	QSPI_DQ2	PERIPHERAL
J11	QSPI_DQ3	PERIPHERAL
C2	I2C0_SCL	PERIPHERAL
D3	I2C0_SDA	PERIPHERAL
E2	I2C1_SCL	PERIPHERAL
D2	I2C1_SDA	PERIPHERAL
B1	I2C1_INT	PERIPHERAL
L9	TESTMODE	TEST AND DEBUG
C11	JTAG_SEL	TEST AND DEBUG
B11	JTAG_TCK	TEST AND DEBUG
D10	JTAG_TMS	TEST AND DEBUG
D9	JTAG_TDI	TEST AND DEBUG
C10	JTAG_TDO	TEST AND DEBUG
E10	JTAG_TRST*	TEST AND DEBUG
F9	ANALOGMUX_OUT	TEST AND DEBUG
M10	TST_CLKOUT	TEST AND DEBUG
H10	TST_CLK_LVDS_0_P	TEST AND DEBUG
H11	TST_CLK_LVDS_0_N	TEST AND DEBUG
G11	TST_CLK_LVDS_1_P	TEST AND DEBUG
G10	TST_CLK_LVDS_1_N	TEST AND DEBUG

USBC_ATC1_D2R_C_P<1> — USBC_ATC1_D2R_C_N<1> — USBC_ATC1_D2R_C_P<2> — USBC_ATC1_D2R_C_N<2> — USBC_ATC1_R2D_P<1> — USBC_ATC1_R2D_N<1> — USBC_ATC1_R2D_P<2> — USBC_ATC1_R2D_N<2> — USBC_ATC1_AUX_C_P — USBC_ATC1_AUX_C_N — CIO_ATC1_LSTX — CIO_ATC1_LSRX — ATCRTMR1_SFP_RCAL_POS — ATCRTMR1_SFP_RCAL_NEG — ATCRTMR1_CHIPID_0 — ATCRTMR1_CHIPID_1 — ATCRTMR1_BOOT_CONFIG0 — ATCRTMR1_BOOT_CONFIG1 — ATCRTMR1_BOOT_CONFIG2 — ATCRTMR1_FORCE_DFU — TP_ATCRTMR1_GPIO_0 — NC_ATCRTMR1_GPIO_1 (NO_TEST=1) — TP_ATCRTMR1_GPIO_2 — TP_ATCRTMR1_GPIO_3 — ATCRTMR1_COLD_RESET_L — ATCRTMR1_CFSB — ATCRTMR1_XTAL24M_IN — ATCRTMR1_XTAL24M_OUT

USBC_ATC1_R2D_CR_P<1> — USBC_ATC1_R2D_CR_N<1> — USBC_ATC1_R2D_CR_P<2> — USBC_ATC1_R2D_CR_N<2> — USBC_ATC1_D2R_P<1> — USBC_ATC1_D2R_N<1> — USBC_ATC1_D2R_P<2> — USBC_ATC1_D2R_N<2> — USBC_ATC1_AUX_P — USBC_ATC1_AUX_N — CIO_ATC1_LSRX — CIO_ATC1_LSTX — ATCRTMR1_LSTX_DIR — ATCRTMR1_CFP_RCAL_POS — ATCRTMR1_CFP_RCAL_NEG — SPI_ATCRTMR1_CS_L — SPI_ATCRTMR1_CLK — SPI_ATCRTMR1_DIO<0> — SPI_ATCRTMR1_DIO<1> — SPI_ATCRTMR1_DIO<2> — SPI_ATCRTMR1_DIO<3> — I2C_ATCRTMR_SCL — I2C_ATCRTMR_SDA — I2C_UPC1_ATCRTMR1_SCL_1V2 — I2C_UPC1_ATCRTMR1_SDA_1V2 — INT_I2C_UPC1_ATCRTMR1_L — ATCRTMR1_TESTMODE — ATCRTMR1_JTAGL_SEL — SWD_NUB_ATCRTMR_SWCLK — SWD_NUB_ATCRTMR_SWDIO — TP_ATCRTMR1_JTAG_TDI — ATCRTMR1_JTAG_TDO — TP_ATCRTMR1_JTAG_TRESET — TP_ATCRTMR1_ANALOGMUX_OUT — TP_ATCRTMR1_TST_CLKOUT — NC_ATCRTMR1_CLK_LVDS_P<0> (NO_TEST=1) — NC_ATCRTMR1_CLK_LVDS_N<0> (NO_TEST=1) — NC_ATCRTMR1_CLK_LVDS_P<1> (NO_TEST=1) — NC_ATCRTMR1_CLK_LVDS_N<1> (NO_TEST=1)

SPI_ATCRTMR1_DIO<0> — RF197 33 1/20W 5% TK 0201 — SPI_ATCRTMR1_R_DIO<0>

SPI_ATCRTMR1_DIO<1> — RF198 33 1/20W 5% TK 0201 — SPI_ATCRTMR1_R_DIO<1>

PP1V2_USBC_VDDIO

RF190 3.3K 5% 1/20W TK 0201 — NOSTUFF RF191 3.3K 5% 1/20W TK 0201 — NOSTUFF RF192 3.3K 5% 1/20W TK 0201 — NOSTUFF RF193 3.3K 5% 1/20W TK 0201 — CF190 1.0UF 20% 6.3V X5R 0201-1

UF190 64MBIT-1.2V W25Q64NE XSON-1

OMIT_TABLE CRITICAL 335S00574

Pin	Net
6	CLK
1	CS*
3	WP*(IO2)
7	HOLD*(IO3)
5	DI(IO0)
2	DO(IO1)
8	VCC
4	GND
9	EPAD

SPI_ATCRTMR1_CLK — RF194 33 1/20W 5% TK 0201 — SPI_ATCRTMR1_CLK_R

SPI_ATCRTMR1_CS_L

SPI_ATCRTMR1_DIO<2> — RF195 33 1/20W 5% TK 0201 — SPI_ATCRTMR1_R_DIO<2>

SPI_ATCRTMR1_DIO<3> — RF196 33 1/20W 5% TK 0201 — SPI_ATCRTMR1_R_DIO<3>

SPI_ATCRTMR1_R_DIO<0> — SPI_ATCRTMR1_R_DIO<1>

CF111 10PF 5% 25V C0G 0201 — RF111 200 1% 1/20W TK 0201-1 — ATCRTMR1_CFP_RCAL_NEG — ATCRTMR1_CFP_RCAL_POS

CF110 10PF 5% 25V C0G 0201 — RF110 200 1% 1/20W TK 0201-1 — ATCRTMR1_SFP_RCAL_NEG — ATCRTMR1_SFP_RCAL_POS

RF147 47K 1/20W 5% TK 0201 — ATCRTMR1_JTAGL_SEL

RF140 10K 1/20W 5% TK 0201 — ATCRTMR1_TESTMODE

RF143 47K 1/20W 5% TK 0201 — CIO_ATC1_LSTX

RF144 47K 1/20W 5% TK 0201 — CIO_ATC1_LSRX

BOM_COST_GROUP=TBT

PAGE TITLE	USB-C: High Speed ATC1
	Apple Inc.
DRAWING NUMBER	051-07020
SIZE	D
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SPI Master Ace

UF260 8MBIT-3.0V W25Q80DVUXIE USON — OMIT_TABLE CRITICAL 335S00133

PP3V3_UPC0_LDO

RF260 3.3K 5% 1/20W TK 0201

RF261 3.3K 5% 1/20W TK 0201

RF263 3.3K 5% 1/20W TK 0201

RF262 3.3K 5% 1/20W TK 0201

CF260 1UF 10% 6.3V CERM 402

ROM_UPC01_WP_L

ROM_UPC01_HOLD_L

NOSTUFF RF264 3.3K 5% 1/20W TK 0201

SPI_UPC01_MOSI	RF289 15 5% 1/20W TK 0201	SPI_UPC01_R_MOSI
SPI_UPC01_MISO	RF288 15 5% 1/20W TK 0201	SPI_UPC01_R_MISO
NO_XNET_CONNECTION=1	RF284 100 5% 1/20W TK 0201	SPI_UPC01_CLK_DBG
SPI_UPC01_CLK	RF285 15 5% 1/20W TK 0201	SPI_UPC01_R_CLK
SPI_UPC01_CS_L	RF287 15 5% 1/20W TK 0201	SPI_UPC01_R_CS_L

SPI Secondary Ace

PACK_IGNORE=TRUE PACK_OPTION=USBC_SPI_2ND_ROM

UF250 8MBIT-3.0V W25Q80DVUXIE USON — OMIT_TABLE CRITICAL 335S00133

PP3V3_UPC1_LDO

RF250 3.3K 5% 1/20W TK 0201

NOSTUFF RF251 3.3K 5% 1/20W TK 0201

RF253 3.3K 5% 1/20W TK 0201

RF252 3.3K 5% 1/20W TK 0201

CF250 1UF 10% 6.3V CERM 402

RF259 3.3K 5% 1/20W TK 0201

RF254 15 5% 1/20W TK 0201	GND
RF255 15 5% 1/20W TK 0201	GND
RF257 15 5% 1/20W TK 0201	GND
RF258 15 5% 1/20W TK 0201	GND

Ace 0 is SPI Ace?

USBC_ATC1_AUX_P	CF236 0.1UF 10% 6.3V CERM-X5R 0201	USBC_ATC1_AUX_C_P
USBC_ATC1_AUX_N	CF237 0.1UF 10% 6.3V CERM-X5R 0201	USBC_ATC1_AUX_C_N

Ace 1 is SPI Ace?

USBC_ATC0_AUX_P	CF275 0.1UF 10% 6.3V CERM-X5R 0201	USBC_ATC0_AUX_C_P
USBC_ATC0_AUX_N	CF276 0.1UF 10% 6.3V CERM-X5R 0201	USBC_ATC0_AUX_C_N

Ace 1 is UART Ace?

PACK_OPTION=USBC_SPI_UPC0 — PACK_OPTION=USBC_SPI_UPC1

SPI_UPC01_R_CLK	MAKE_BASE=TRUE	SPI_UPC01_R_CLK
SPI_UPC01_R_CS_L	MAKE_BASE=TRUE	SPI_UPC01_R_CS_L
SPI_UPC01_R_MOSI	MAKE_BASE=TRUE	SPI_UPC01_R_MOSI
SPI_UPC01_R_MISO	MAKE_BASE=TRUE	SPI_UPC01_R_MISO
SWD_UPC_SWCLK	MAKE_BASE=TRUE	SWD_UPC_SWCLK
SWD_UPC_SWDIO0	MAKE_BASE=TRUE	SWD_UPC_SWDIO0
PP3V3_UPC0_LDO	MAKE_BASE=TRUE	PP3V3_UPC0_LDO

GND / GND / GND / GND — SWD_UPC01_UART_CLK / SWD_UPC01_UART_DATA / PP3V3_UPC1_LDO (MAKE_BASE=TRUE)

Ace 0 is UART Ace?

PACK_OPTION=USBC_SPI_UPC0_AND_NO_2ND_ROM

GND / GND / GND / GND (MAKE_BASE=TRUE)

PACK_OPTION=USBC_SPI_UPC1 — MAKE_BASE=TRUE

SPI_UPC01_R_CLK / SPI_UPC01_R_CS_L / SPI_UPC01_R_MOSI / SPI_UPC01_R_MISO / SWD_UPC_SWCLK / SWD_UPC_SWDIO0

SWD_UPC01_UART_CLK	MAKE_BASE=TRUE	SWD_UPC01_UART_CLK
SWD_UPC01_UART_DATA	MAKE_BASE=TRUE	SWD_UPC01_UART_DATA

PACK_OPTION=USBC_SPI_UPC0

RF273 100K 5% 1/20W TK 0201 — PD_UPC1_HPD

RF274 100K 5% 1/20W TK 0201 — PD_UPC0_HPD

SPI Ace		UART Ace
UART_UPC01_TX	MAKE_BASE=TRUE	UART_UPC01_TX
UART_UPC01_RX	MAKE_BASE=TRUE	UART_UPC01_RX

SPI Ace		UART Ace
UART_UPC01_RX		UART_UPC01_RX
UART_UPC01_TX		UART_UPC01_TX

ACE ARKANOID CONN

JF200 505070-1222 M-ST-SM — USBC_DBG — PACK_IGNORE=TRUE PACK_OPTION=KEEP_SMALL_ARKANOID_CONN

SMC		SOC
ATCRTMR0_FORCE_DFU		UPC_I2C_INT_L
I2C_SMC_UPC_SCL		I2C_UPC_SDA
I2C_SMC_UPC_SDA		I2C_UPC_SCL
UPC_SMC_I2C_INT_L		UPC0_SER_DBG
SPI_UPC01_CLK_DBG		UPC1_SER_DBG
UART_UPC01_TX (SPI Ace)		UART_UPC01_RX (SPI Ace)

BRIDGE ARKANOID CONN

JF201 505070-1222 M-ST-SM — USBC_DBG — PACK_IGNORE=TRUE PACK_OPTION=KEEP_SMALL_ARKANOID_CONN

ATCRTMR0_RESET_L	INT_I2C_UPC0_ATCRTMR0_L
UPC0_ATCRTMR01_PWR_EN	I2C_UPC0_ATCRTMR0_SCL
PP1V2_USBC_VDDIO	I2C_UPC0_ATCRTMR0_SDA
PP0V855_USBC_CIO	UPC1_ATCRTMR01_PWR_EN
ATCRTMR1_RESET_L	INT_I2C_UPC1_ATCRTMR1_L
I2C_UPC1_ATCRTMR1_SDA	I2C_UPC1_ATCRTMR1_SCL

USBC_DBG

RF280 200K 1% 1/20W TK 0201 — VREFB_ARDV01 — PP3V3_S2_LDO

PP1V25_S2

CF281 0.1UF 10% 6.3V CERM-X5R 0201

CF280 0.1UF 10% 6.3V CERM-X5R 0201

RF282 5.1K 5% 1/20W TK 0201

RF283 5.1K 5% 1/20W TK 0201

PACK_OPTION=PKGS:SMALL:PITCH

UF280 LSF0102 X2SON-COMBO 311S00234 — VREF_A, VREF_B, A1, A2, EN, B1, B2, GND

I2C_UPC_SCL — I2C_UPC01_3V3_SCL

I2C_UPC_SDA — I2C_UPC01_3V3_SDA

PACK_IGNORE=TRUE PACK_OPTION=PKGS:LARGER_PITCH

UF280 LSF0102 VSSOP 311S00257 — VREF_A, VREF_B, A1, A2, EN, B1, B2, GND

AARDVARKANOID CONN

JF202 505070-1222 M-ST-SM — USBC_DBG — PACK_IGNORE=TRUE PACK_OPTION=KEEP_SMALL_ARKANOID_CONN

SPI ACE		UART ACE
PP1V25_S2		SPI_UPC01_CS_L
SWD_UPC_SWDIO0_CONN		SPI_UPC01_CLK
SWD_UPC_SWCLK_CONN		SPI_UPC01_MOSI
SPI_UPC01_MISO		SWD_UPC01_UART_CLK
I2C_UPC01_3V3_SDA		SWD_UPC01_UART_DATA
I2C_UPC01_3V3_SCL		PP1V25_S2

BOM_COST_GROUP=USB-C

PP1V25_S2 / PP3V3_S2_LDO

CF230 0.1UF 10% 6.3V CERM-X5R 0201

UF230 SN74AXC1T45-S SOT-5X3 — VCCA, VCCB, DIR, A, B, GND

CF231 0.1UF 10% 6.3V CERM-X5R 0201

PMU_ACTIVE_READY — ATCRTMR01_ACTIVE_READY_3V3

PACK_IGNORE=TRUE PACK_OPTION=ACTIVE_READY:LARGE_PITCH

UF230 SN74AXC1T45 X2SON 311S00212 — VCCA, VCCB, DIR, A, B, GND

PACK_OPTION=ACTIVE_READY:SMALL_PITCH_CHECK_WITH_DFM

PP1V25_S2

RF212 1.5K 5% 1/20W TK 0201

RF213 1.5K 5% 1/20W TK 0201

INT_I2C_EUSBLS0_L	RF211 0 0% 1/20W TK 0201	INT_I2C_UPC0_ATCRTMR0_L
INT_I2C_EUSBLS1_L	RF216 0 0% 1/20W TK 0201	INT_I2C_UPC1_ATCRTMR1_L

ATCRTMR01_ACTIVE_READY_3V3 — NO_XNET_CONNECTION=1

RF290 100K 5% 1/20W TK 0201

USBC0_AUX_N	CF290 0.1UF 10% 6.3V CERM-X5R 0201	USBC0_AUX_C_N
USBC0_AUX_P	CF291 0.1UF 10% 6.3V CERM-X5R 0201	USBC0_AUX_C_P

RF292 33K 5% 1/20W TK 0201 — RF293 33K 5% 1/20W TK 0201 — RF291 100K 5% 1/20W TK 0201

ATCRTMR01_ACTIVE_READY_3V3 — NO_XNET_CONNECTION=1

RF298 100K 5% 1/20W TK 0201

USBC1_AUX_N	CF292 0.1UF 10% 6.3V CERM-X5R 0201	USBC1_AUX_C_N
USBC1_AUX_P	CF293 0.1UF 10% 6.3V CERM-X5R 0201	USBC1_AUX_C_P

RF296 33K 5% 1/20W TK 0201 — RF297 33K 5% 1/20W TK 0201 — RF299 100K 5% 1/20W TK 0201

HV POWER ALIASES

Fuses for laptop charging.

PACK_OPTION=USBC_LAPTOP

Desktops only need connection for programming OTP.

PACK_IGNORE=TRUE PACK_OPTION=USBC_DESKTOP

CRITICAL 0603-1 FF200 6A-32V 740S00053 — PPDCIN_AON_CHGR — PPHV_INT0_AONSW — MAKE_BASE=TRUE VOLTAGE=20V — PLACE_NEAR=UF400:5MM

RF200 0 0% 1/20W TK 0201 — PPHV_INT0_AONSW

CRITICAL 0603-1 FF201 6A-32V 740S00053 — PPHV_INT1_AONSW — MAKE_BASE=TRUE VOLTAGE=20V — PLACE_NEAR=UF500:5MM

RF201 0 0% 1/20W TK 0201 — PPHV_INT1_AONSW

PPVBUS_USBC0	MAKE_BASE=TRUE	PPVBUS_USBC0
PPVBUS_USBC1	MAKE_BASE=TRUE	PPVBUS_USBC1

SYNC_MASTER=USBC SYNC_DATE=09/26/2022

PAGE TITLE: USB-C: Support 1 ATC01

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*** OK2INTEGRATE ***

Ace 0 is Debug Port?

PACK_OPTION=USBC_DEBUG_UPC0 — ATC0 / UPC0 / RTMR0

UART DEBUGPRT_R2D	=	UART DEBUGPRT_R2D
UART DEBUGPRT_D2R	=	UART DEBUGPRT_D2R
SWD_SOC_SWCLK	=	SWD_SOC_SWCLK
SWD_SOC_SWDIO	=	SWD_SOC_SWDIO
UART_SMC_DEBUGPRT_R2D	=	UART_SMC_DEBUGPRT_R2D
UART_SMC_DEBUGPRT_D2R	=	UART_SMC_DEBUGPRT_D2R
USB_DBG_LS_P	=	USB_DBG_LS_P
USB_DBG_LS_N	=	USB_DBG_LS_N
SOC_DOCK_CONNECT	=	SOC_DOCK_CONNECT
SOC_DFU_STATUS	=	SOC_DFU_STATUS
SOC_FORCE_DFU	=	SOC_FORCE_DFU

PACK_OPTION=USBC_DEBUG_UPC0

Ace 1 is Debug Port?

PACK_OPTION=USBC_DEBUG_UPC1 — ATC1 / UPC1 / RTMR1

PD_UPC1_DBG0_R	=	PD_UPC1_DBG0_R
PD_UPC1_DBG1_R	=	PD_UPC1_DBG1_R
PD_UPC1_DBG2_R	=	PD_UPC1_DBG2_R
PD_UPC1_DBG3_R	=	PD_UPC1_DBG3_R
PD_UPC1_DBG4_R	=	PD_UPC1_DBG4_R
PD_UPC1_DBG5_R	=	PD_UPC1_DBG5_R
PD_UPC1_USBP2_RP	=	PD_UPC1_USBP2_RP
PD_UPC1_USBP2_RN	=	PD_UPC1_USBP2_RN
PD_UPC1_GPIO7	=	PD_UPC1_GPIO7
PD_UPC1_GPIO9	=	PD_UPC1_GPIO9
PD_UPC1_GPIO10	=	PD_UPC1_GPIO10

Main Debug Port

Ace2 GPIOs

Non-debug Port

Ace 1 is non-debug Port?

ATC1 / UPC1 / RTMR1

RF320	100K	PD_UPC1_DBG0_R	= PD_UPC1_DBG0_R
RF321	100K	PD_UPC1_DBG1_R	= PD_UPC1_DBG1_R
RF322	100K	PD_UPC1_DBG2_R	= PD_UPC1_DBG2_R
RF323	100K	PD_UPC1_DBG3_R	= PD_UPC1_DBG3_R
RF324	100K	PD_UPC1_DBG4_R	= PD_UPC1_DBG4_R
RF325	100K	PD_UPC1_DBG5_R	= PD_UPC1_DBG5_R
RF328	100K	PD_UPC1_USBP2_RP	= PD_UPC1_USBP2_RP
RF329	100K	PD_UPC1_USBP2_RN	= PD_UPC1_USBP2_RN

Ace2 GPIOs

RF373	100K	PD_UPC1_GPIO7	= PD_UPC1_GPIO7
RF374	100K	PD_UPC1_GPIO9	= PD_UPC1_GPIO9
RF375	100K	PD_UPC1_GPIO10	= PD_UPC1_GPIO10

CKPLUS_WAIVE=SINGLE_NODENET — on all nets above.

Ace 0 is non-debug Port?

PACK_IGNORE=TRUE
PACK_OPTION=USBC_DEBUG_UPC1 — ATC0 / UPC0 / RTMR0

RF310	100K	PD_UPC0_DBG0_R	UART_DEBUGPRT_R2D
RF311	100K	PD_UPC0_DBG1_R	UART_DEBUGPRT_D2R
RF312	100K	PD_UPC0_DBG2_R	SWD_SOC_SWCLK
RF313	100K	PD_UPC0_DBG3_R	SWD_SOC_SWDIO
RF314	100K	PD_UPC0_DBG4_R	UART_SMC_DEBUGPRT_R2D
RF315	100K	PD_UPC0_DBG5_R	UART_SMC_DEBUGPRT_D2R
RF318	100K	PD_UPC0_USBP2_RP	USB_DBG_LS_P
RF319	100K	PD_UPC0_USBP2_RN	USB_DBG_LS_N

Ace2 GPIOs

RF363	100K	PD_UPC0_GPIO7	SOC_DOCK_CONNECT
RF364	100K	PD_UPC0_GPIO9	SOC_DFU_STATUS
RF365	100K	PD_UPC0_GPIO10	SOC_FORCE_DFU

CKPLUS_WAIVE=SINGLE_NODENET — on all nets above.

GND, GND, GND — MAKE_BASE=TRUE — PACK_OPTION=USBC_SPI_NO_2ND_ROM — GND, GND, GND

Unused ports

RF397	100K	PD_UPC0_GPIO1	PD_UPC0_GPIO1
RF398	100K	PD_UPC0_GPIO6	PD_UPC0_GPIO6
RF31A	100K	PD_UPC0_USBP3_RP	PD_UPC0_USBP3_RP
RF31B	100K	PD_UPC0_USBP3_RN	PD_UPC0_USBP3_RN

Secondary ACE ROM Options

RF396	100K	PD_UPC1_GPIO1	PD_UPC1_GPIO1
RF399	100K	PD_UPC1_GPIO6	PD_UPC1_GPIO6
RF32A	100K	PD_UPC1_USBP3_RP	PD_UPC1_USBP3_RP
RF32B	100K	PD_UPC1_USBP3_RN	PD_UPC1_USBP3_RN

Connections for Laptops (USBC power in) — PACK_OPTION=USBC_LAPTOP
Connections for Desktops (No USBC power in) — PACK_OPTION=USBC_DESKTOP

PP3V3_UPC0_LDO	=	PP3V3_UPC0_LDO
USBC0_CC1	=	USBC0_CC1
USBC0_CC2	=	USBC0_CC2

Connections for Laptops (USBC power in) — PACK_OPTION=USBC_LAPTOP
Connections for Desktops (No USBC power in) — PACK_OPTION=USBC_DESKTOP

PP3V3_UPC1_LDO	=	PP3V3_UPC1_LDO
USBC1_CC1	=	USBC1_CC1
USBC1_CC2	=	USBC1_CC2

USBC0 PP_CABLE Protection

PP3V3_UPC0_LDO — USBC0_VBIAS_PRT — MIN_LINE_WIDTH=0.0990 MIN_NECK_WIDTH=0.0990

CF300 1UF 10% 6.3V CERM 402
CF301 0.1UF 10% 50V CERM-X7R 0402

UF300 TPD4S311A BGA — VPWR, VBIAS, FLT*, SBU1, SBU2, CC1, CC2, C_SBU1, C_SBU2, C_CC1, C_CC2, RPD_G1, RPD_G2, GND, GND, GND — 338S00753

NC_USBC0_CC_FLT_L (NO_TEST=1)
USBC0_CC1, USBC0_CC2
USBC0_CC1_CONN, USBC0_CC2_CONN — MAKE_BASE=TRUE — PACK_OPTION=USBC_DESKTOP
PACK_OPTION=USBC_LAPTOP_CC_PRT — pack option for all component

USBC1 PP_CABLE Protection

PP3V3_UPC1_LDO — USBC1_VBIAS_PRT — MIN_LINE_WIDTH=0.0990 MIN_NECK_WIDTH=0.0990

CF350 1UF 10% 6.3V CERM 402
CF351 0.1UF 10% 50V CERM-X7R 0402

UF350 TPD4S311A BGA — VPWR, VBIAS, FLT*, SBU1, SBU2, CC1, CC2, C_SBU1, C_SBU2, C_CC1, C_CC2, RPD_G1, RPD_G2, GND, GND, GND — 338S00753

NC_USBC1_CC_FLT_L (NO_TEST=1)
USBC1_CC1, USBC1_CC2
USBC1_CC1_CONN, USBC1_CC2_CONN — MAKE_BASE=TRUE — PACK_OPTION=USBC_DESKTOP
PACK_OPTION=USBC_LAPTOP_CC_PRT — pack option for all component

ATC0: I2C_ADDR=GND, i2CM_*_CNFG=1M\u03a9 3V3_LDO_X pull-ups
ATC1: I2C_ADDR=Float, i2CM_*_CNFG=1M\u03a9 3V3_LDO_X pull-ups
ATC2: I2C_ADDR=GND, i2CM_*_CNFG=1M\u03a9 pull-downs
ATC3: I2C_ADDR=Float, i2CM_*_CNFG=1M\u03a9 pull-downs

GND, NC_UPC1_I2C_ADDR — MAKE_BASE=TRUE — NC_UPC1_I2C_ADDR (NO_TEST=1)

Configure to enable VDDIO and use it for SWD.
GND, GND — MAKE_BASE=TRUE

Is UPCx_5V_EN being used?

UPC0_5V_EN	RF350	100K
UPC1_5V_EN	RF351	100K

PACK_OPTION=USBC01_VR5V_LOCAL_NO
BOM_COST_GROUP=USB-C

ATCRTMR Boot Config

[2:0] = [011] 30Mhz QSPI and Test Mode Enabled
POR config should be [010] Test Mode Disabed

RF380	10K	ATCRTMR0_BOOT_CONFIG2	
RF381	10K	ATCRTMR0_BOOT_CONFIG1	NOSTUFF
RF382	10K	ATCRTMR0_BOOT_CONFIG0	LFKA_TEST_MODE:NO
RF383	10K	ATCRTMR1_BOOT_CONFIG2	
RF384	10K	ATCRTMR1_BOOT_CONFIG1	NOSTUFF
RF385	10K	ATCRTMR1_BOOT_CONFIG0	LFKA_TEST_MODE:NO

LFKA_TEST_MODE:YES — RF386 10K — RF387 10K — PP1V2_USBC_VDDIO — RF388 10K NOSTUFF — ATCRTMR0_BOOT_CONFIG2, ATCRTMR0_BOOT_CONFIG1, ATCRTMR0_BOOT_CONFIG0

LFKA_TEST_MODE:YES — RF389 10K — RF390 10K — PP1V2_USBC_VDDIO — RF391 10K NOSTUFF — ATCRTMR1_BOOT_CONFIG2, ATCRTMR1_BOOT_CONFIG1, ATCRTMR1_BOOT_CONFIG0

ATCRTMR0 CHIP 0X00

RF392	10K	ATCRTMR0_CHIPID_0
RF393	10K	ATCRTMR0_CHIPID_1

ATCRTMR1 CHIP 0X01

PP1V2_USBC_VDDIO — RF395 47K — ATCRTMR1_CHIPID_0

RF394 10K — ATCRTMR1_CHIPID_1

ATCRTMR0_RESET_1V2_L	RF330	0	ATCRTMR0_COLD_RESET_L
	RF331	0	ATCRTMR0_CFSB
P1V2_ATC01_PGOOD	RF332	0	NOSTUFF
ATCRTMR1_RESET_1V2_L	RF333	0	ATCRTMR1_COLD_RESET_L
	RF334	0	ATCRTMR1_CFSB
P1V2_ATC01_PGOOD	RF335	0	NOSTUFF

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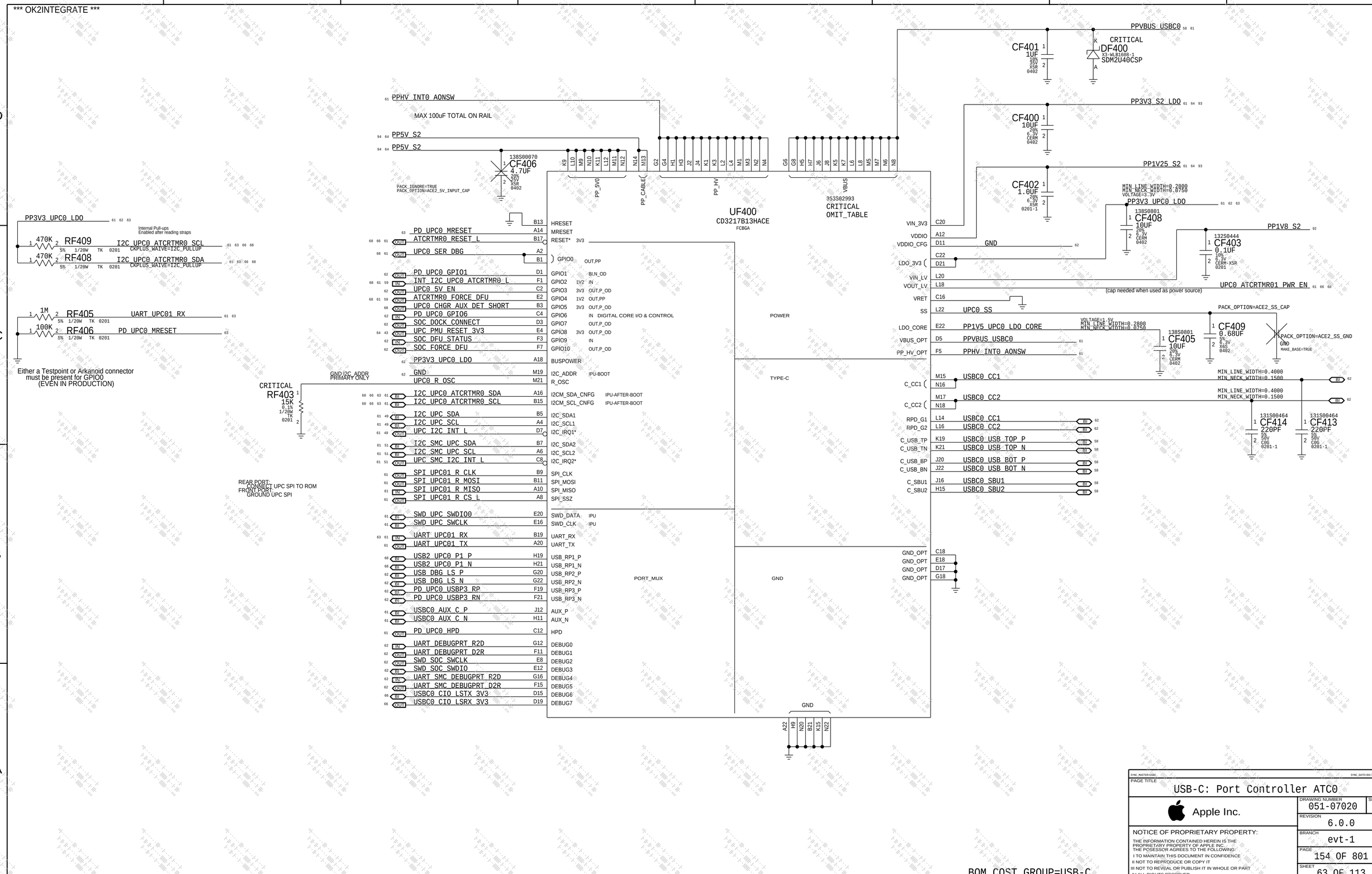
*** OK2INTEGRATE ***



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*** OK2INTEGRATE ***

PPHV_INT1_AONSW

MAX 100uF TOTAL ON RAIL

PP5V_S2

PP5V_S2

138S00070 CF506 4.7UF 20% 25V X5R 0402

PACK_IGNORE=TRUE
PACK_OPTION=ACE2_5V_INPUT_CAP

PP3V3_UPC1_LDO

470K RF509 5% 1/20W TK 0201 — I2C_UPC1_ATCRTMR1_SCL — CKPLUS_WAIVE=I2C_PULLUP

470K RF508 5% 1/20W TK 0201 — I2C_UPC1_ATCRTMR1_SDA — CKPLUS_WAIVE=I2C_PULLUP

1M RF505 5% 1/20W TK 0201 — UART_UPC01_TX

100K RF506 5% 1/20W TK 0201 — PD_UPC1_MRESET

Either a Testpoint or Arkanoid connector
must be present for GPIO0
(EVEN IN PRODUCTION)

CRITICAL RF503 15K 0.1% 1/20W TK 0201

GND_I2C_ADDR
PRIMARY ONLY

REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI

UF500
CD3217B13HACE
FCBGA

PP_5V0: K9, L10, M9, N10, K11, L12, M11, N12
PP_CABLE: N14, M13
PP_HV: G2, G4, H1, H3, J2, J4, K1, K3, L2, L4, M1, M3, N2, N4
VBUS: G6, G8, H5, H7, J6, J8, K5, K7, L6, L8, M5, M7, N6, N8

353S02993
CRITICAL
OMIT_TABLE

Pin	Net	Dir	Function
B13	HRESET		HRESET
A14	MRESET		MRESET
B17	RESET*	3V3	RESET*
A2	GPIO0		OUT,PP
B1			
D1	GPIO1		BI,N_OD
F1	GPIO2	1V2	IN
C2	GPIO3	3V3	OUT,P_OD
E2	GPIO4	1V2	OUT,PP
B3	GPIO5	3v3	OUT,P_OD
C4	GPIO6		IN DIGITAL CORE I/O & CONTROL
D3	GPIO7		OUT,P_OD
E4	GPIO8	3v3	OUT,P_OD
F3	GPIO9		IN
F7	GPIO10		OUT,P_OD
A18	BUSPOWER		
M19	I2C_ADDR		IPU-BOOT
M21	R_OSC		
A16	I2CM_SDA_CNFG		IPU-AFTER-BOOT
B15	I2CM_SCL_CNFG		IPU-AFTER-BOOT
B5	I2C_SDA1		
A4	I2C_SCL1		
D7	I2C_IRQ1*		
B7	I2C_SDA2		
A6	I2C_SCL2		
C8	I2C_IRQ2*		
B9	SPI_CLK		
B11	SPI_MOSI		
A10	SPI_MISO		
A8	SPI_SSZ		
E20	SWD_DATA		IPU
E16	SWD_CLK		IPU
B19	UART_RX		
A20	UART_TX		
H19	USB_RP1_P		
H21	USB_RP1_N		
G20	USB_RP2_P		
G22	USB_RP2_N		
F19	USB_RP3_P		
F21	USB_RP3_N		
J12	AUX_P		
H11	AUX_N		
C12	HPD		
G12	DEBUG0		
F11	DEBUG1		
E8	DEBUG2		
E12	DEBUG3		
G16	DEBUG4		
F15	DEBUG5		
D15	DEBUG6		
D19	DEBUG7		

PD_UPC1_MRESET
ATCRTMR1_RESET_L
UPC1_SER_DBG
PD_UPC1_GPIO1
INT_I2C_UPC1_ATCRTMR1_L
UPC1_5V_EN
ATCRTMR1_FORCE_DFU
UPC1_CHGR_AUX_DET_SHORT
PD_UPC1_GPIO6
PD_UPC1_GPIO7
UPC_PMU_RESET_3V3
PD_UPC1_GPIO9
PD_UPC1_GPIO10
PP3V3_UPC1_LDO
NC_UPC1_I2C_ADDR
UPC1_R_OSC
I2C_UPC1_ATCRTMR1_SDA
I2C_UPC1_ATCRTMR1_SCL
I2C_UPC_SDA
I2C_UPC_SCL
UPC_I2C_INT_L
I2C_SMC_UPC_SDA
I2C_SMC_UPC_SCL
UPC_SMC_I2C_INT_L
GND
GND
GND
GND
SWD_UPC01_UART_DATA
SWD_UPC01_UART_CLK
UART_UPC01_TX
UART_UPC01_RX
USB2_UPC1_P1_P
USB2_UPC1_P1_N
PD_UPC1_USBP2_RP
PD_UPC1_USBP2_RN
PD_UPC1_USBP3_RP
PD_UPC1_USBP3_RN
USBC1_AUX_C_P
USBC1_AUX_C_N
PD_UPC1_HPD
PD_UPC1_DBG0_R
PD_UPC1_DBG1_R
PD_UPC1_DBG2_R
PD_UPC1_DBG3_R
PD_UPC1_DBG4_R
PD_UPC1_DBG5_R
USBC1_CIO_LSTX_3V3
USBC1_CIO_LSRX_3V3

POWER

TYPE-C

PORT_MUX

GND

Pin	Net
C20	VIN_3V3
A12	VDDIO
D11	VDDIO_CFG — GND
C22	LDO_3V3
D21	
L20	VIN_LV
L18	VOUT_LV
C16	VRET
L22	SS — UPC1_SS
E22	LDO_CORE — PP1V5_UPC1_LDO_CORE
D5	VBUS_OPT — PPVBUS_USBC1
F5	PP_HV_OPT — PPHV_INT1_AONSW
M15	C_CC1 — USBC1_CC1
N16	
M17	C_CC2 — USBC1_CC2
N18	
L14	RPD_G1 — USBC1_CC1
L16	RPD_G2 — USBC1_CC2
K19	C_USB_TP — USBC1_USB_TOP_P
K21	C_USB_TN — USBC1_USB_TOP_N
J20	C_USB_BP — USBC1_USB_BOT_P
J22	C_USB_BN — USBC1_USB_BOT_N
J16	C_SBU1 — USBC1_SBU1
H15	C_SBU2 — USBC1_SBU2

GND_OPT: C18, E18, D17, G18

GND: A22, H9, N20, B21, K15, N22

PPVBUS_USBC1

CF501 1UF 20% 35V X5R 0402

CRITICAL DF500 X3-WLB1608-1 SDM2U40CSP

138S0801 CF500 10UF 20% 6.3V CERM 0402

PP3V3_S2_LDO

PP1V25_S2

CF502 1.0UF 20% 6.3V X5R 0201-1

MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.0750
VOLTAGE=3.3V

PP3V3_UPC1_LDO

138S0801 CF508 10UF 20% 6.3V CERM 0402

PP1V8_S2

132S0444 CF503 0.1UF 10% 6.3V CERM-X5R 0201

UPC1_ATCRTMR01_PWR_EN

(cap needed when used as power source)

PACK_OPTION=ACE2_SS_CAP

VOLTAGE=1.5V
MIN_LINE_WIDTH=0.2800
MIN_NECK_WIDTH=0.0750

138S0801 CF505 10UF 20% 6.3V CERM 0402

CF509 0.68UF 5% 6.3V X6S 0402

PACK_OPTION=ACE2_SS_GND
GND
MAKE_BASE=TRUE

MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.1500

131S00464 CF514 220PF 5% 50V C0G 0201-1

131S00464 CF513 220PF 5% 50V C0G 0201-1

BOM_COST_GROUP=USB-C

PAGE TITLE	USB-C: Port Controller ATC1
	Apple Inc.
DRAWING NUMBER	051-07020
SIZE	D
REVISION	6.0.0
BRANCH	evt-1
PAGE	155 OF 801
SHEET	64 OF 113

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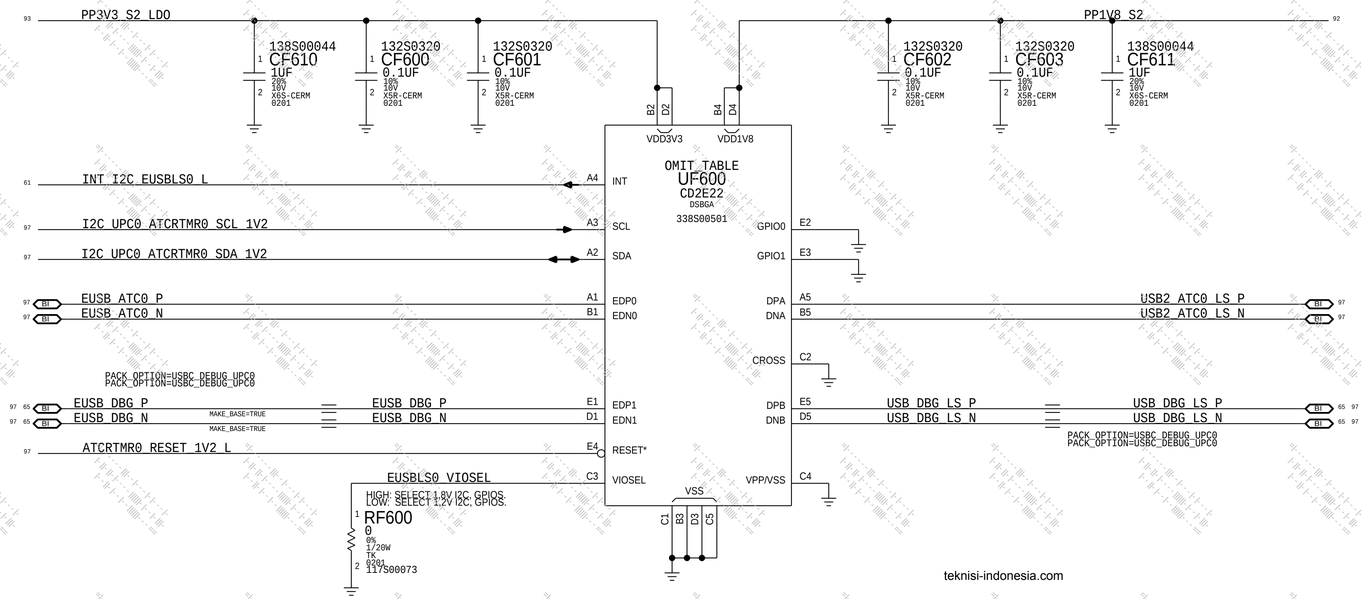
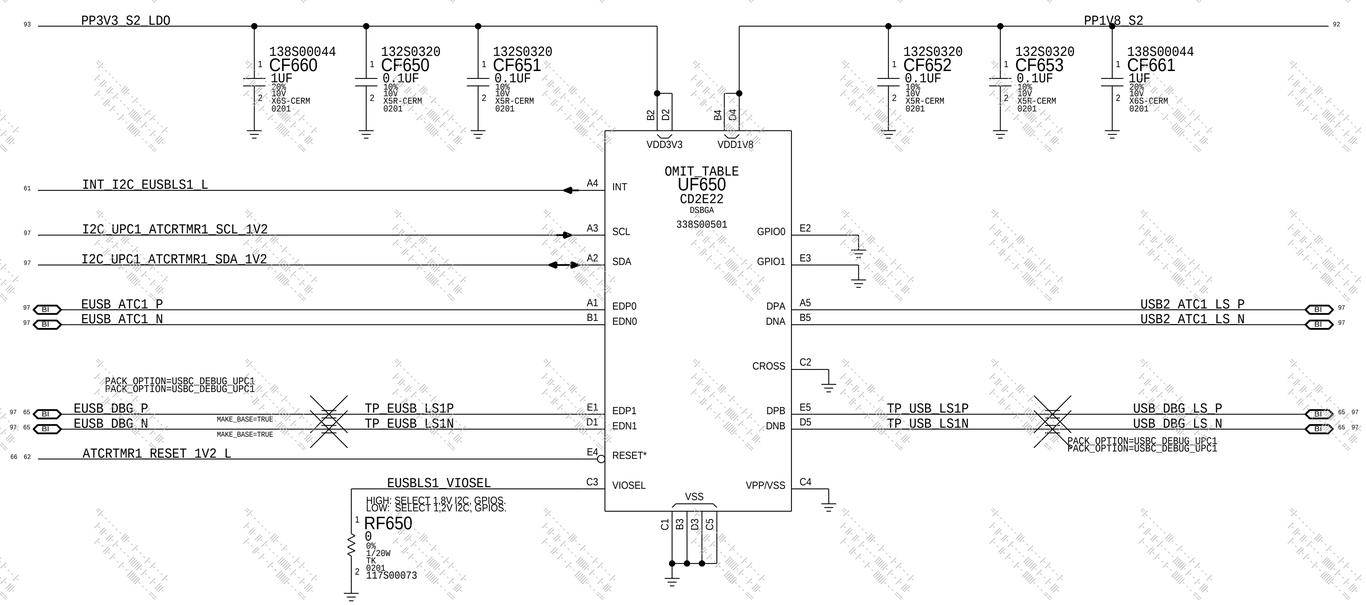
*** OK2INTEGRATE ***





teknisi-indonesia.com

BOM_COST_GROUP=USB-C

SYNC_MASTER=USBC SYNC_DATE=09/26/2021

PAGE TITLE

USB-C: USB2 RPT

Apple Inc.

DRAWING NUMBER 051-07020 SIZE D

REVISION 6.0.0

BRANCH evt-1

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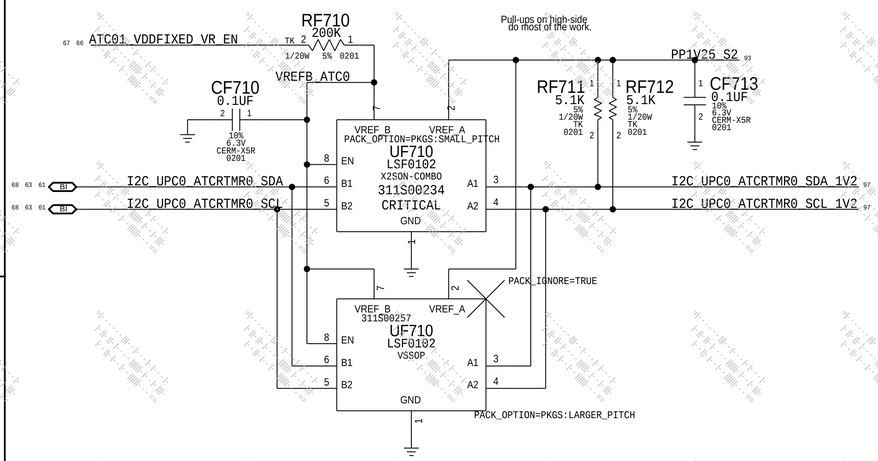
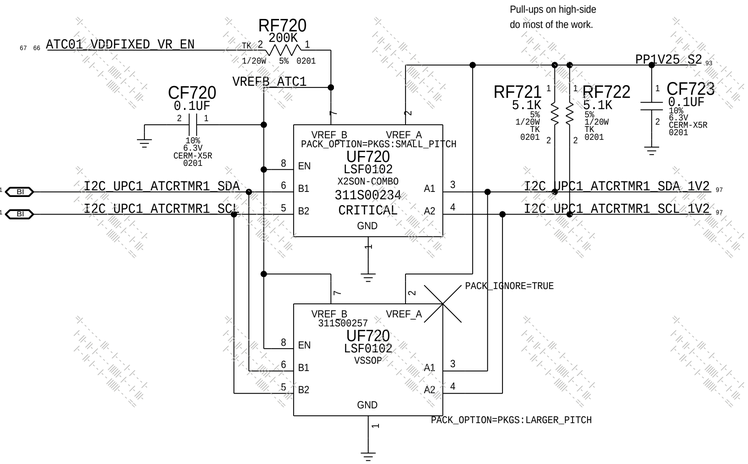
*** OK2INTEGRATE ***

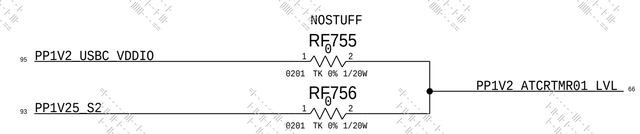
Sequencing Requirements: 3.3V to UF790 --> system 1.2V (UF710,UF720) same time or before system 1.8V (UF400&UF500 VIN_LV pin)

ATC0 RE-TIMER I2C LEVEL SHIFTERS

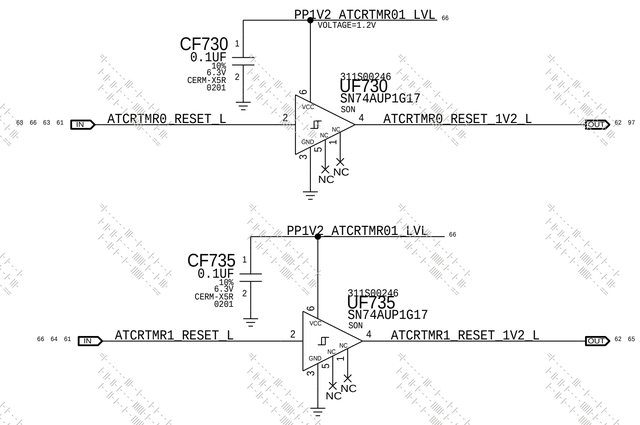


ATC1 RE-TIMER I2C LEVEL SHIFTERS

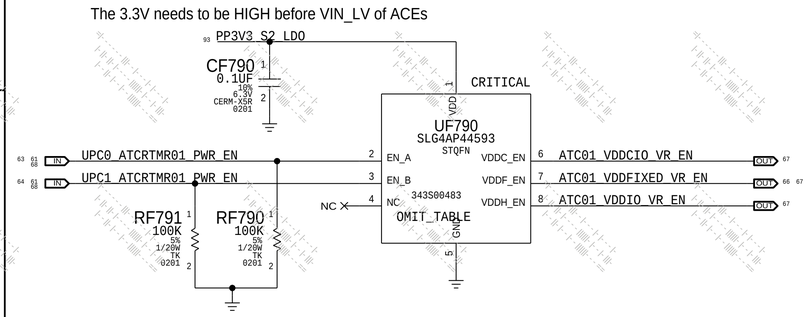


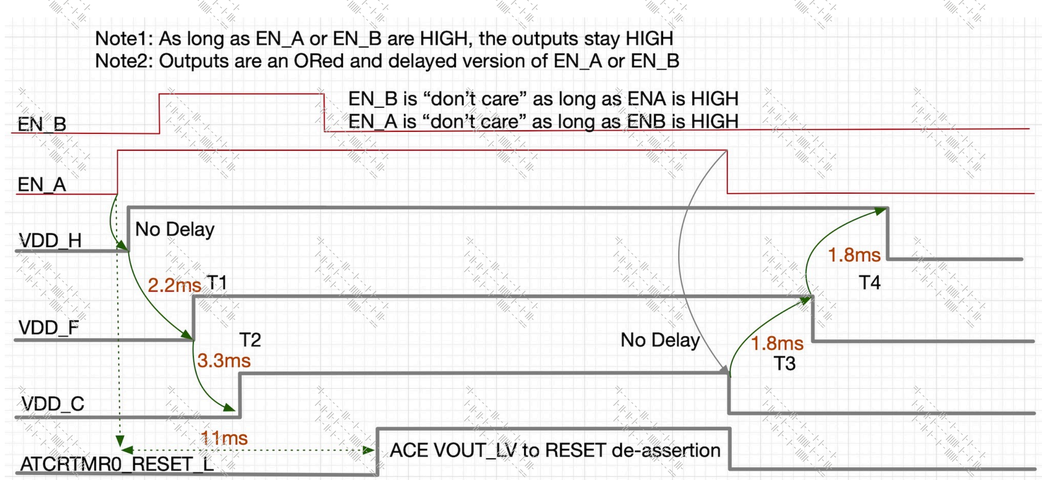


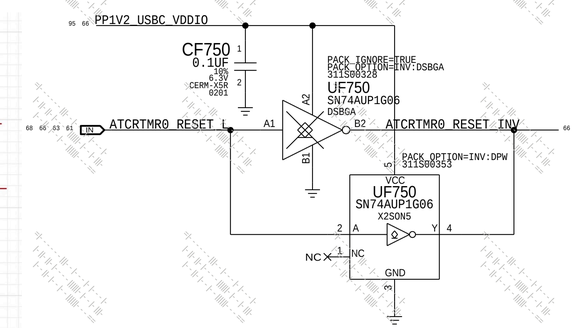
ATC0/1 AND eUSB0/1 RESET LEVEL SHIFTERS

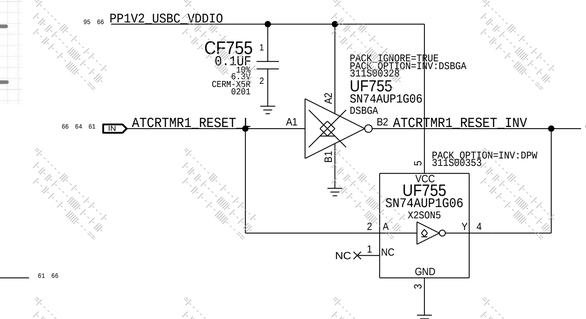


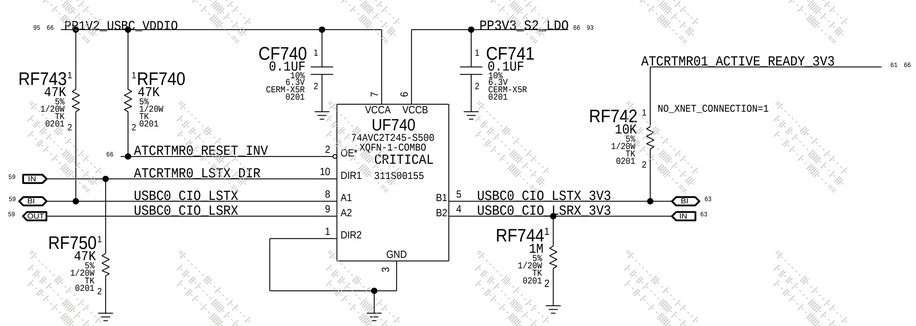
The 3.3V needs to be HIGH before VIN_LV of ACEs

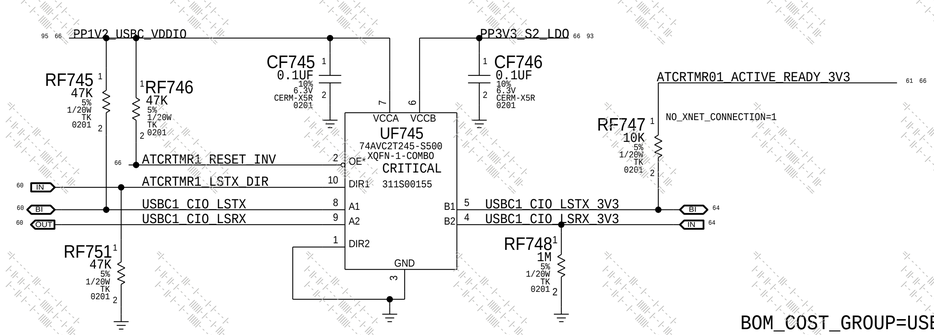












BOM_COST_GROUP=USB-C

PAGE TITLE: USB-C: HS Level Shifters

Apple Inc.

DRAWING NUMBER: 051-07020 | SIZE: D

REVISION: 6.0.0

BRANCH: evt-1

PAGE: 157 OF 801

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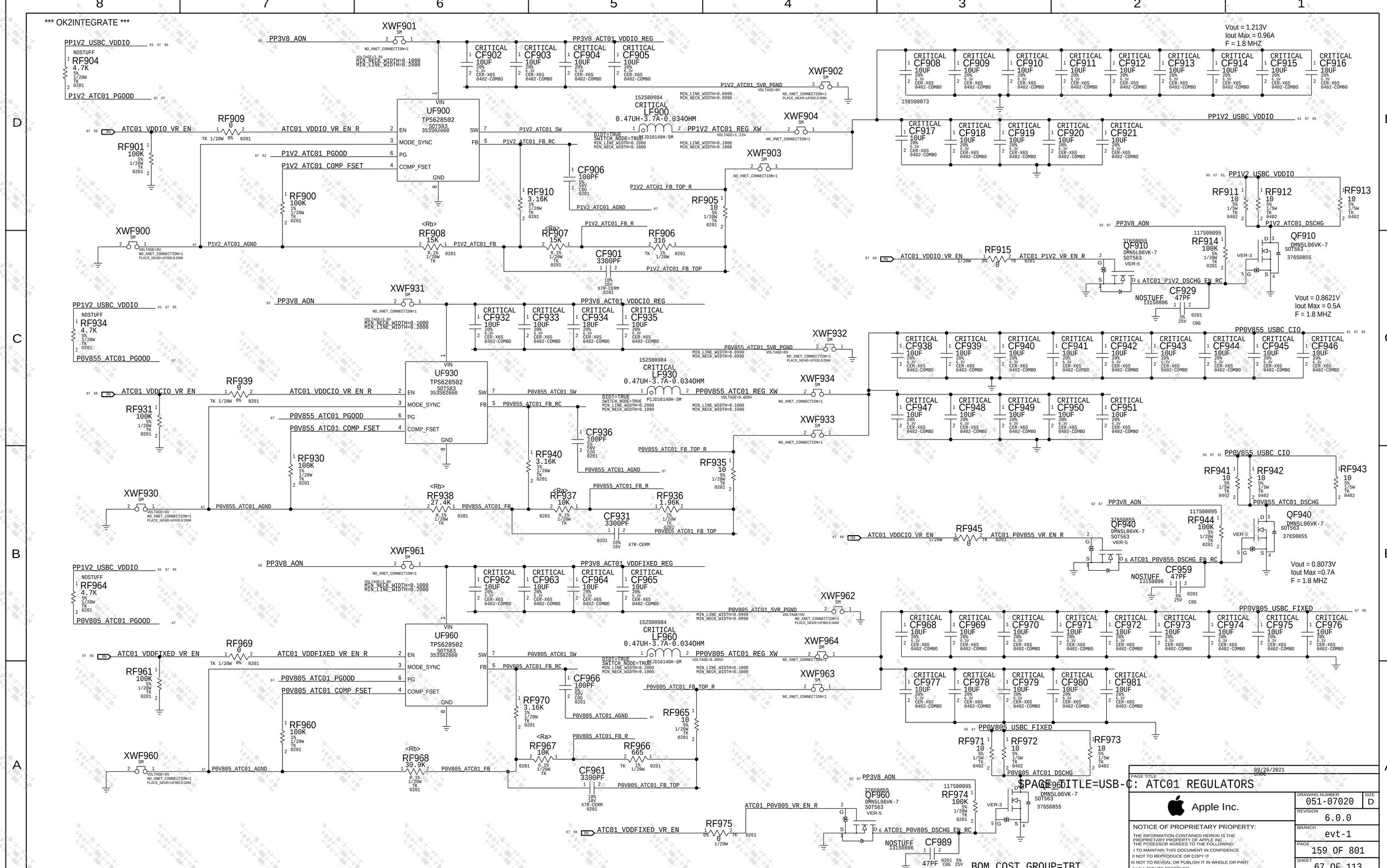
*** OK2INTEGRATE ***
Vout = 1.213V
Iout Max = 0.96A
F = 1.8 MHZ
Vout = 0.8621V
Iout Max = 0.5A
F = 1.8 MHZ
Vout = 0.8073V
Iout Max =0.7A
F = 1.8 MHZ
UF900 TPS628502
UF930 TPS628502
UF960 TPS628502
LF900 0.47UH-3.7A-0.0340HM
LF930 0.47UH-3.7A-0.0340HM
LF960 0.47UH-3.7A-0.0340HM
ATC01 VDDIO VR EN
ATC01 VDDIO VR EN R
ATC01 VDDCIO VR EN
ATC01 VDDCIO VR EN R
ATC01 VDDFIXED VR EN
ATC01 VDDFIXED VR EN R
ATC01 P1V2 VR EN R
ATC01 P0V855 VR EN R
ATC01 P0V805 VR EN R
ATC01 P1V2 DSCHG EN RC
ATC01 P0V855 DSCHG EN RC
ATC01 P0V805 DSCHG EN RC
PP1V2 USBC VDDIO
PP0V855 USBC CIO
PP0V805 USBC FIXED
PP3V8 AON
PP3V8 ACT01 VDDIO REG
PP3V8 ACT01 VDDCIO REG
PP3V8 ACT01 VDDFIXED REG
P1V2 ATC01 DSCHG
P0V855 ATC01 DSCHG
P0V805 ATC01 DSCHG
$PAGE_TITLE=USB-C: ATC01 REGULATORS
BOM_COST_GROUP=TBT
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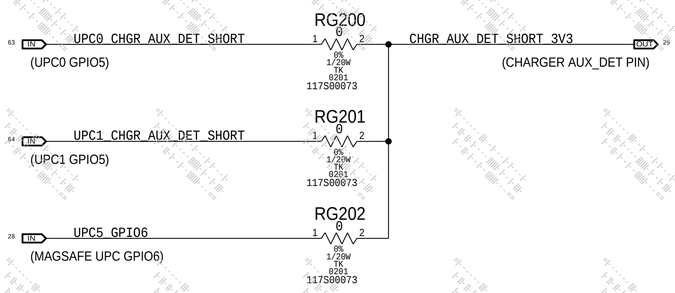
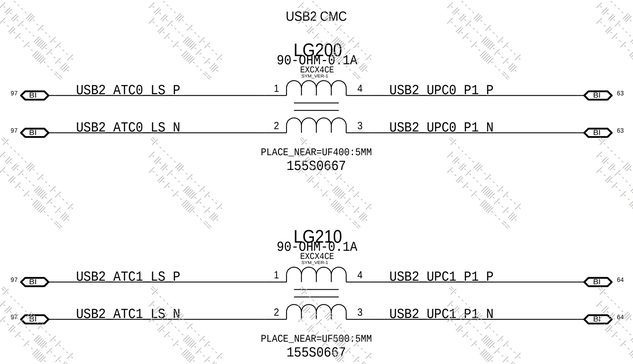
A Charger AUX_DET Connections

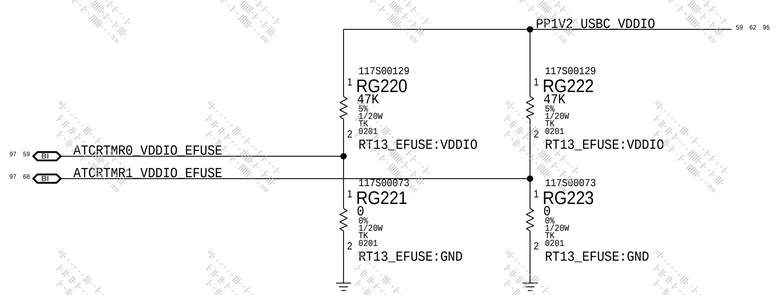
CHARGER AUX DET CONNECTIONS
<RDAR://70072178>
ALLOW ACE TO SEND A SIGNAL TO CHARGER
TO BLOCK SYSTEM CURRENT THROUGH ACE2 FETS DURING ACE2 SOFT START



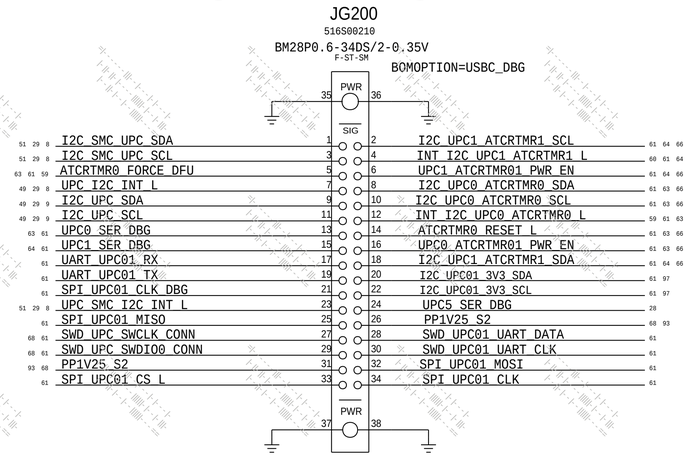
B USB 2.0 Common Mode Choke



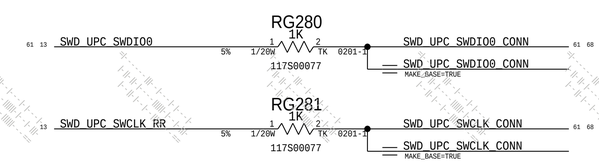
C RT13 VDDIO_EFUSE Selection



D USB-C/MagSafe Debug Connector



E USB-C SWDIO Aliases



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PAGE TITLE
USB-C: PROJECT SUPPORT

Apple Inc.

DRAWING NUMBER 051-07020
SIZE D
REVISION 6.0.0
BRANCH evt-1
PAGE 162 OF 801
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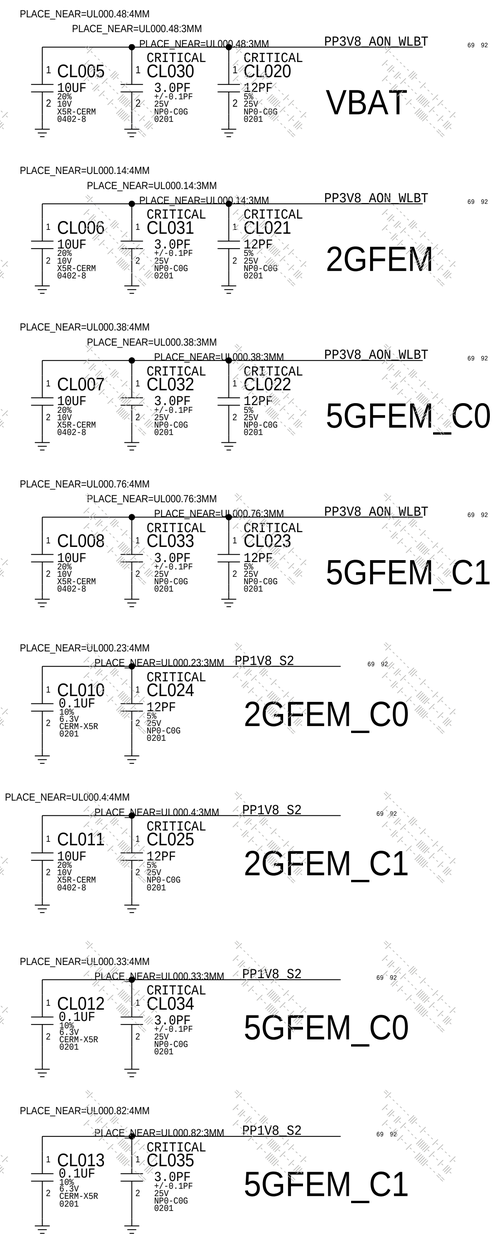
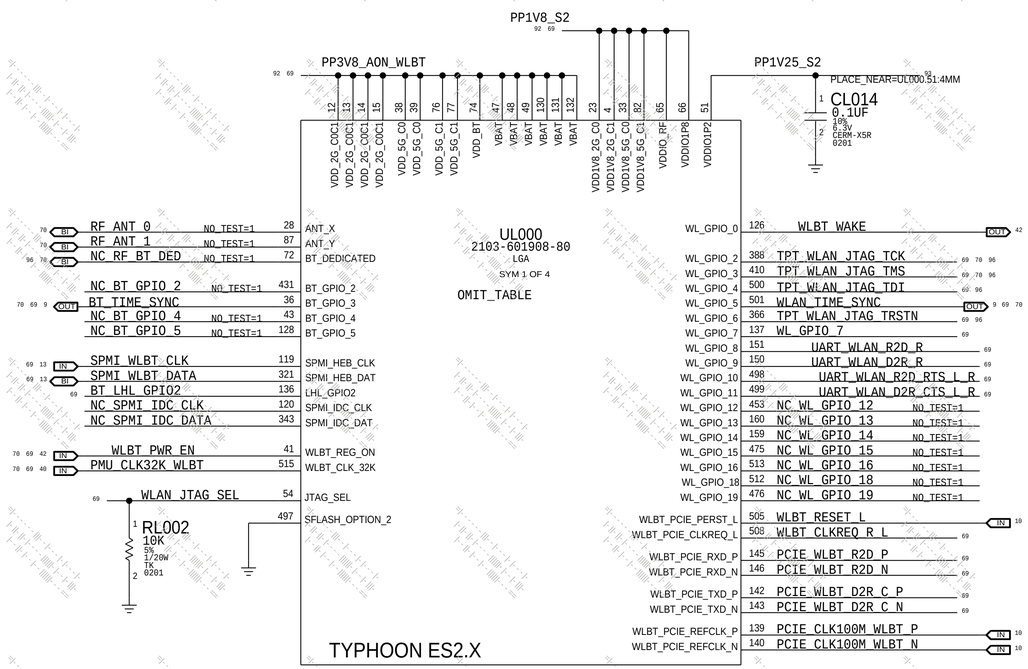
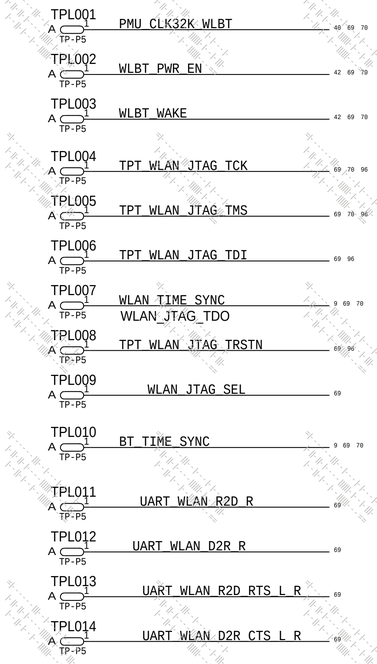
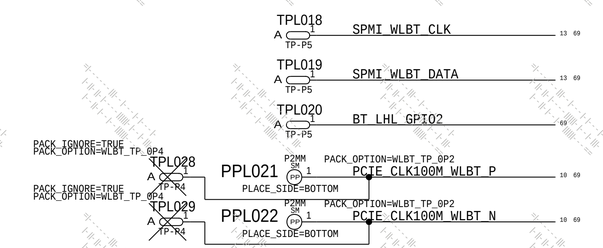
FOR SYSTEM INTEGRATION INFORMATION REFER TO
RDAR://PROBLEM/59047597

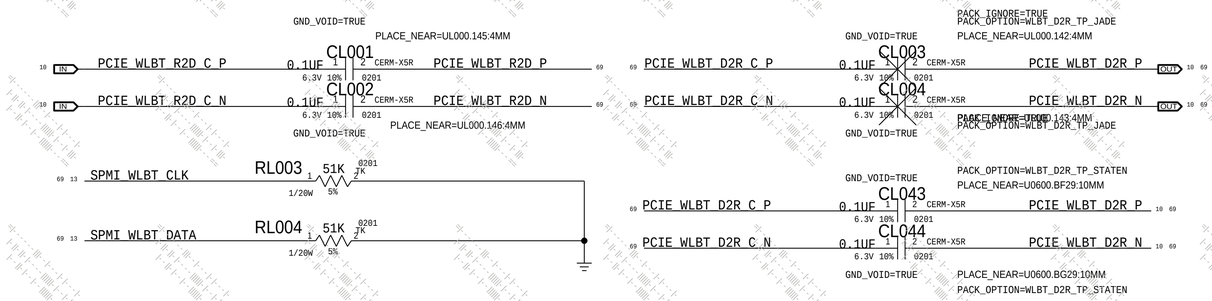
TYPHOON WIFI/BT MODULE

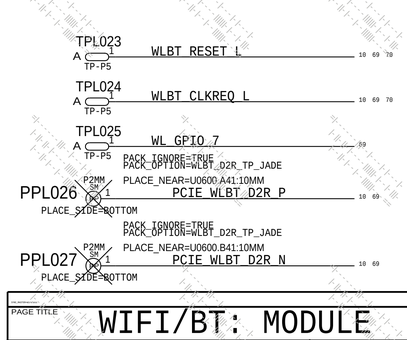












TYPHOON BOM TABLE:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S00912	1	MODULE,WLAN/BT,TYPHOON, ES4.7	UL000	CRITICAL	

BOM_COST_GROUP=WIRELESS

PAGE TITLE: WIFI/BT: MODULE

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D
REVISION: 6.0.0
BRANCH: evt-1
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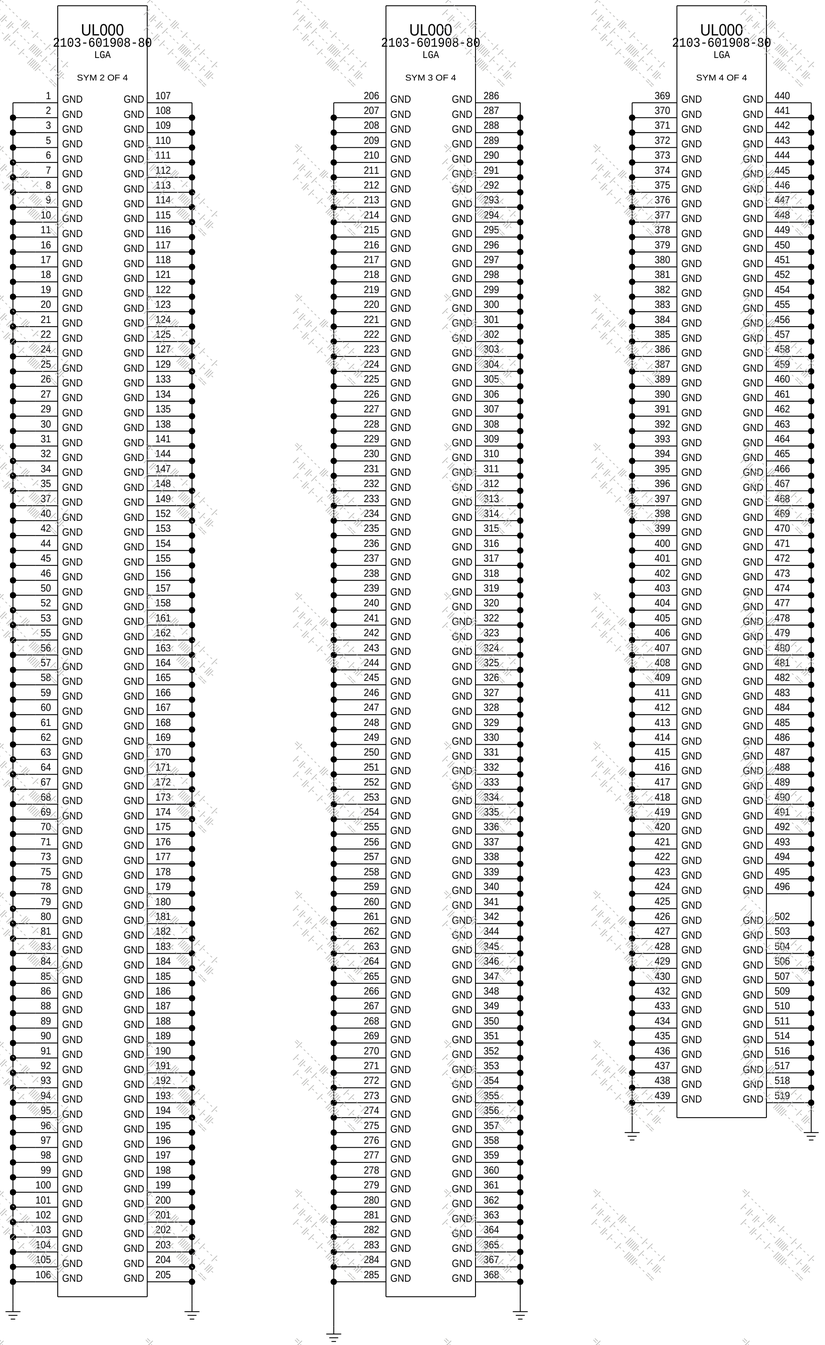
TYPHOON WIFI/BT MODULE GND



ANTENNA CONNECTORS

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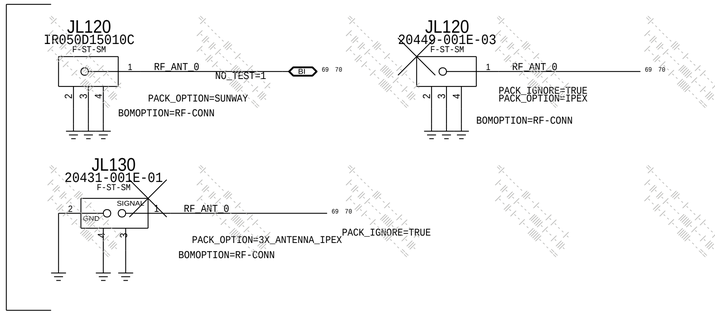
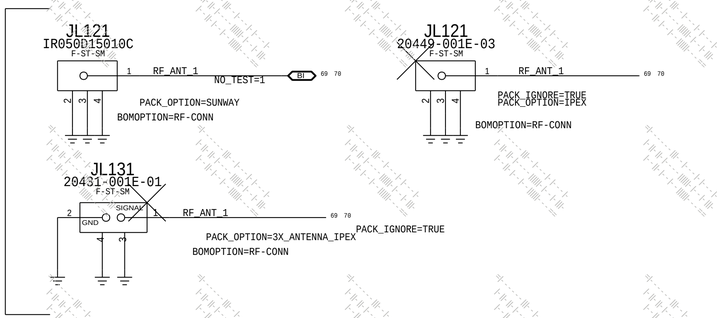
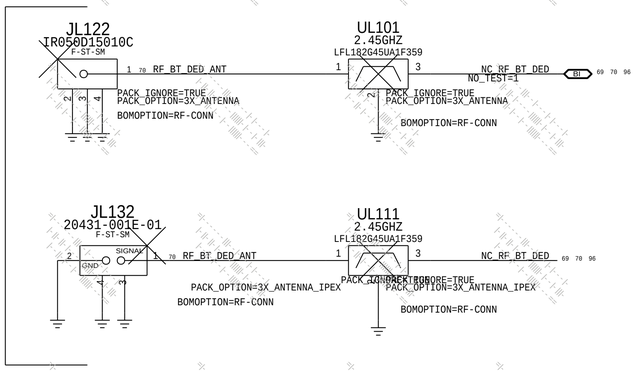
5G_C0
BT_C0



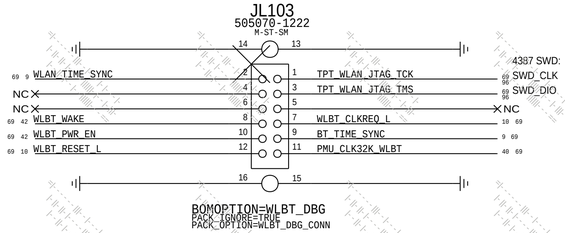
2G_C1
5G_C1
BT_C1



BT_C1_DED



WLBT DEBUG CONNECTOR



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PAGE TITLE
WIFI/BT: ANTENNA and GND

Apple Inc.

DRAWING NUMBER	051-07020
SIZE	D
REVISION	6.0.0
BRANCH	evt-1
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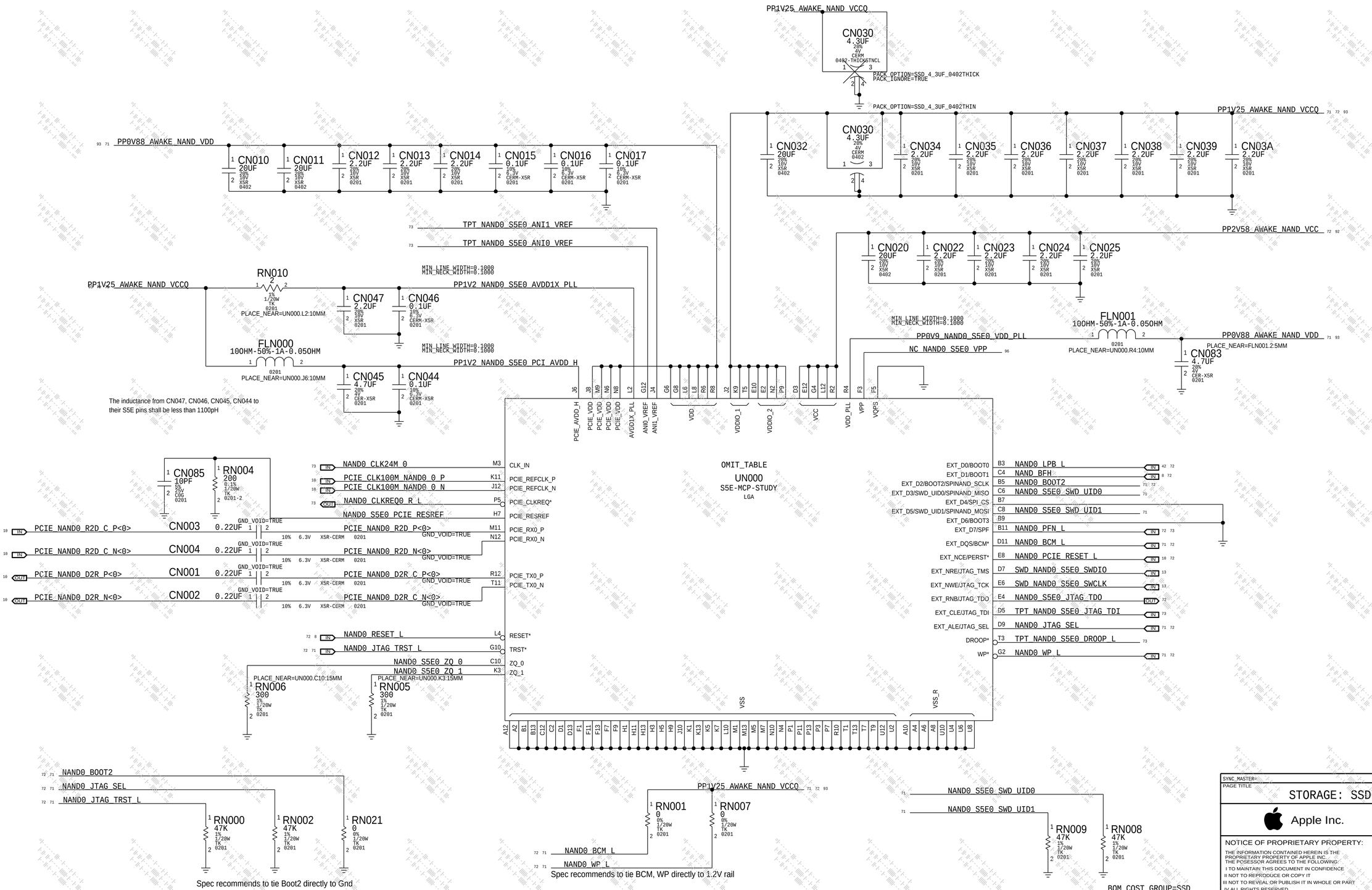
*** OK2INTEGRATE ***

NAND0 S5E0



SYNC_MASTER=
SYNC_DATE=09/10/2021

PAGE TITLE: STORAGE: SSD0 S5E <0>

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D

REVISION: 6.0.0

BRANCH: evt-1

PAGE: 220 OF 801

SHEET: 71 OF 113

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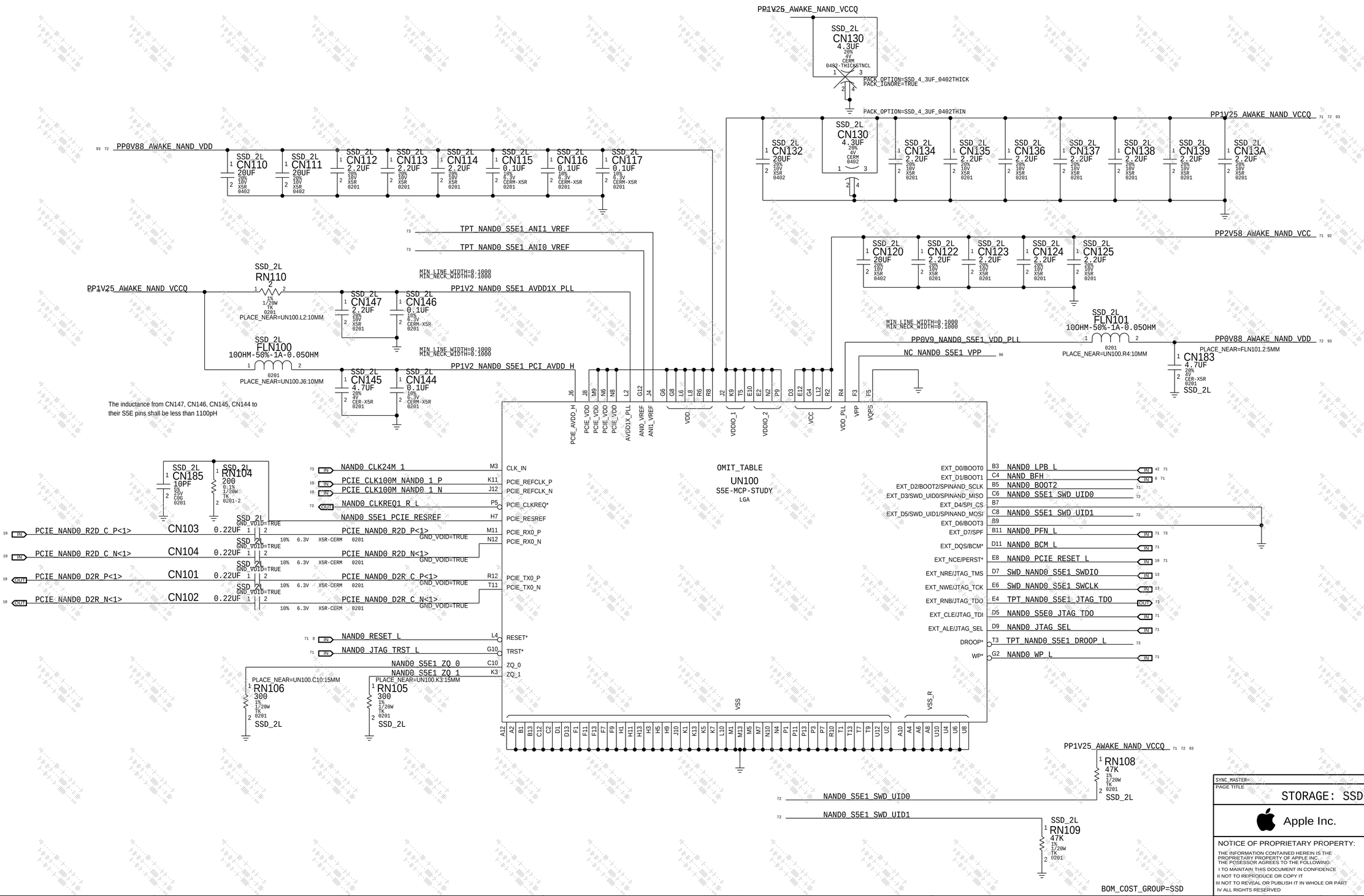
*** OK2INTEGRATE ***

NAND0 S5E1



SYNC_MASTER= SYNC_DATE=09/10/2021

PAGE TITLE

STORAGE: SSD0 S5E <1>

Apple Inc.

DRAWING NUMBER 051-07020 SIZE D

REVISION 6.0.0

BRANCH evt-1

PAGE 221 OF 801

SHEET 72 OF 113

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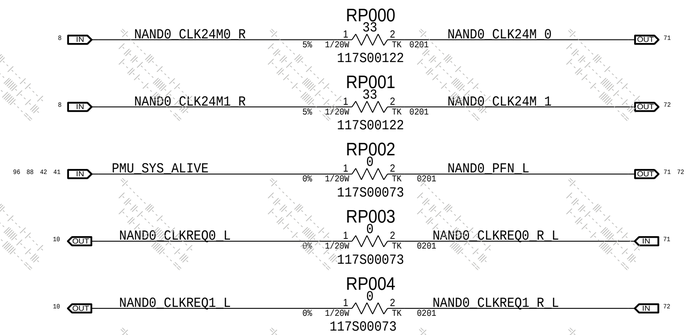
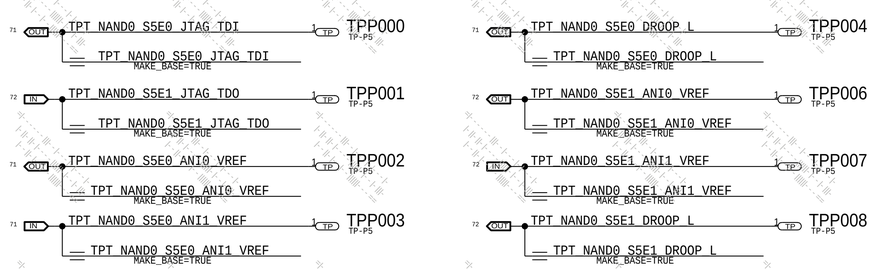
A SSD Termination Resistors



B S5E Test Points



BOM_COST_GROUP=SSD

SYNC_MASTER= SYNC_DATE=09/10/2021

PAGE TITLE: STORAGE: SSD Support

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D

REVISION: 6.0.0

BRANCH: evt-1

PAGE: 230 OF 801

SHEET: 73 OF 113

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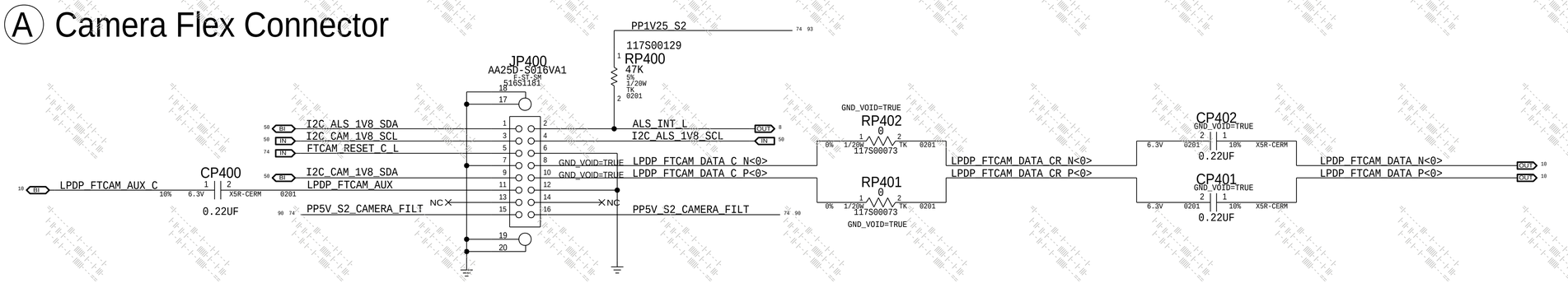
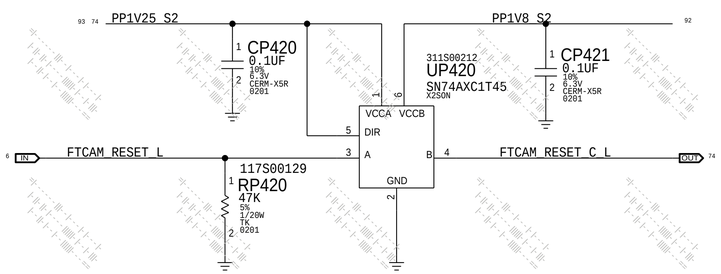
A Camera Flex Connector

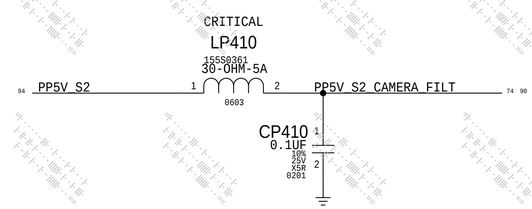


CAM TAIL FLEX CONNECTOR APN 516S1180

B Camera Reset Level Shifter



C Camera Power Filter(s)



BOM_COST_GROUP=CAMERA

PAGE TITLE	CAMERA: FLEX CONNECTOR
Apple Inc.	DRAWING NUMBER 051-07020 SIZE D
	REVISION 6.0.0
	BRANCH evt-1
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	SHEET 74 OF 113

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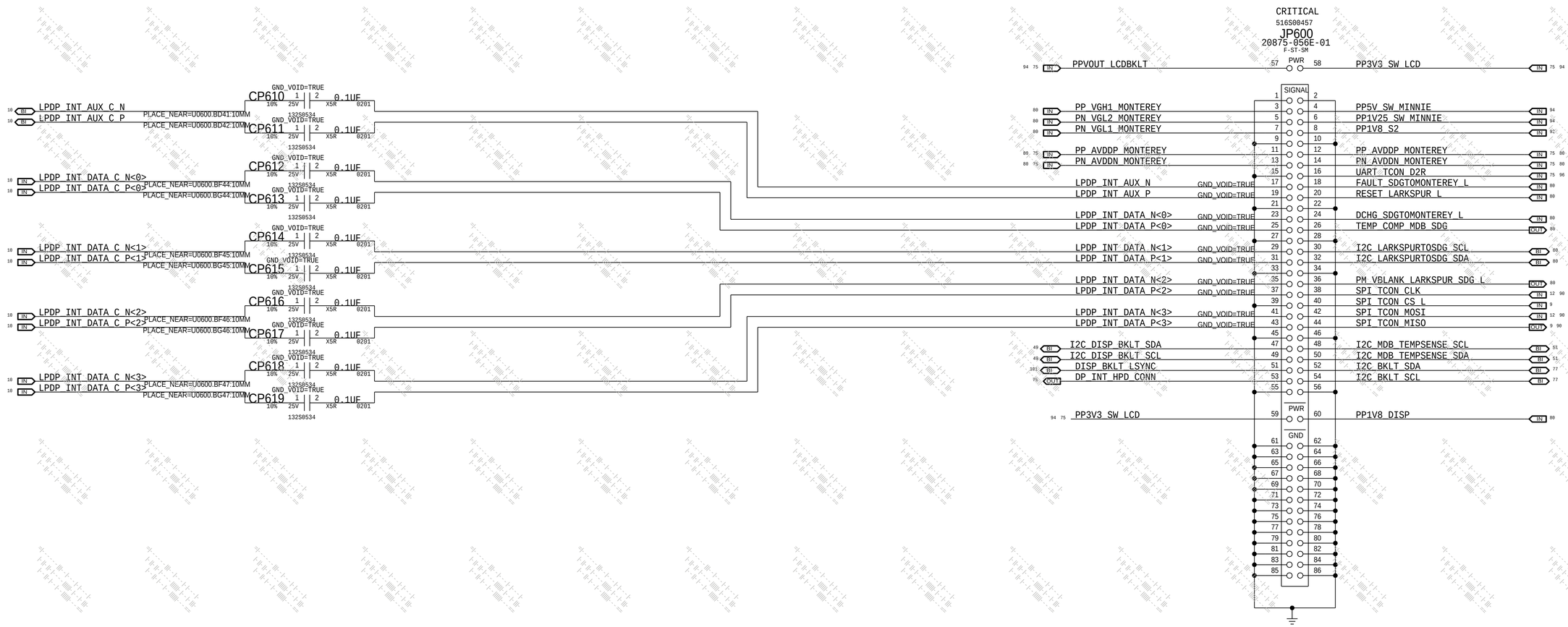
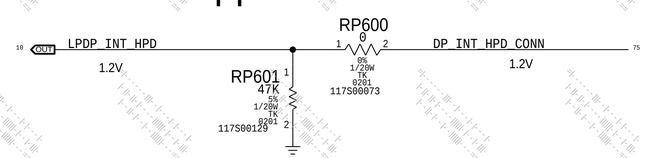
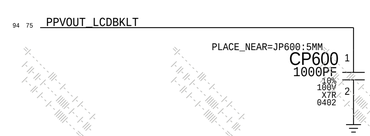
A LCD Panel Interface



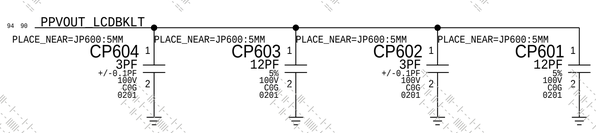
B LCD Panel Support



D LCD Panel Bypass



C LCD Panel Desense



E UART PULLDOWN

teknisi-indonesia.com

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=	SYNC_DATE=09/10/2021
PAGE TITLE	eDP Display Connector
Apple Inc.	DRAWING NUMBER 051-07020 SIZE D
	REVISION 6.0.0
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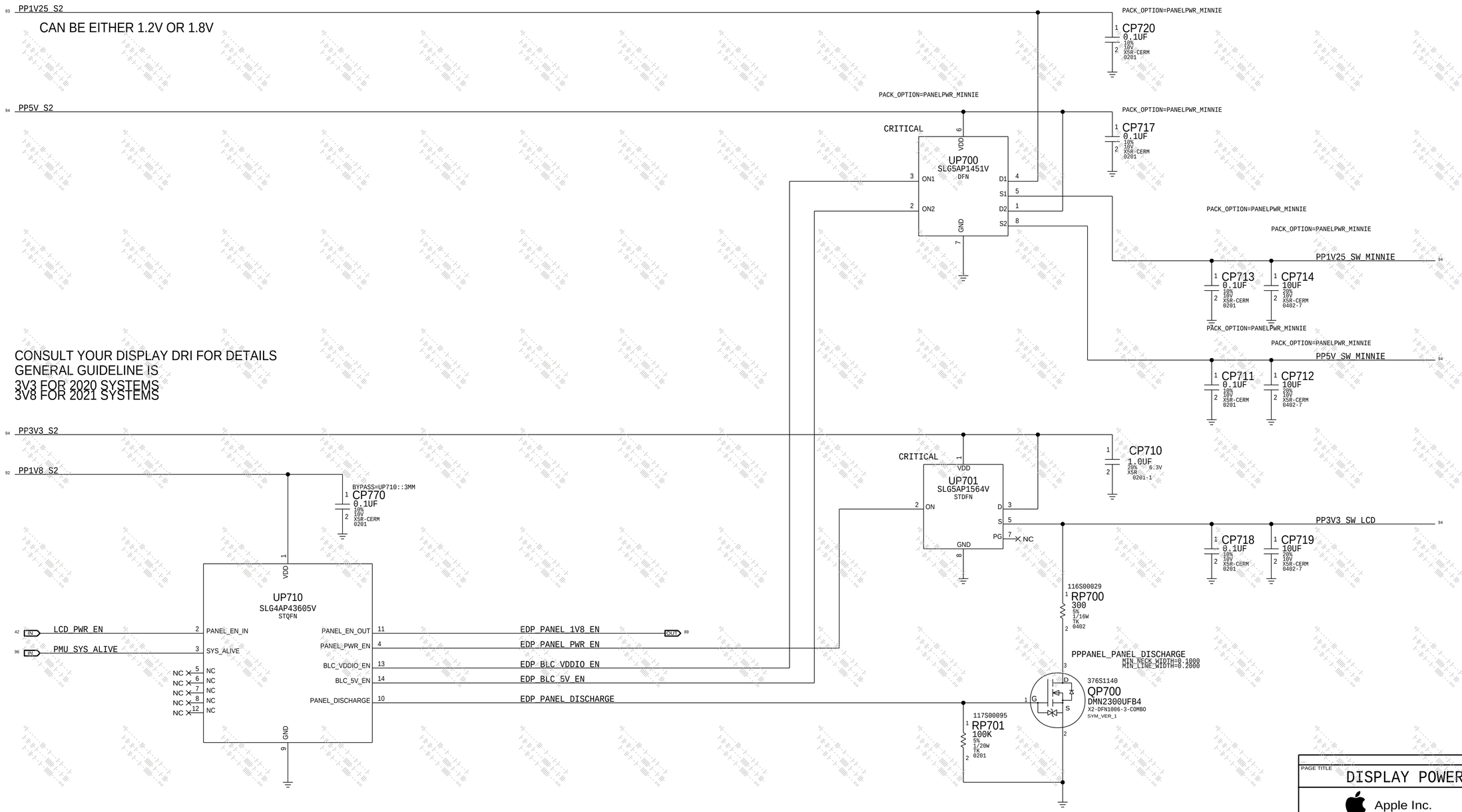
	PAGE 236 OF 801
	SHEET 75 OF 113

*** OK2INTEGRATE ***



BOM_COST_GROUP=DISPLAY

PAGE TITLE	DISPLAY POWER SEQUENCER
	Apple Inc.
DRAWING NUMBER	051-07020
SIZE	D
REVISION	6.0.0
BRANCH	evt-1
PAGE	237 OF 801
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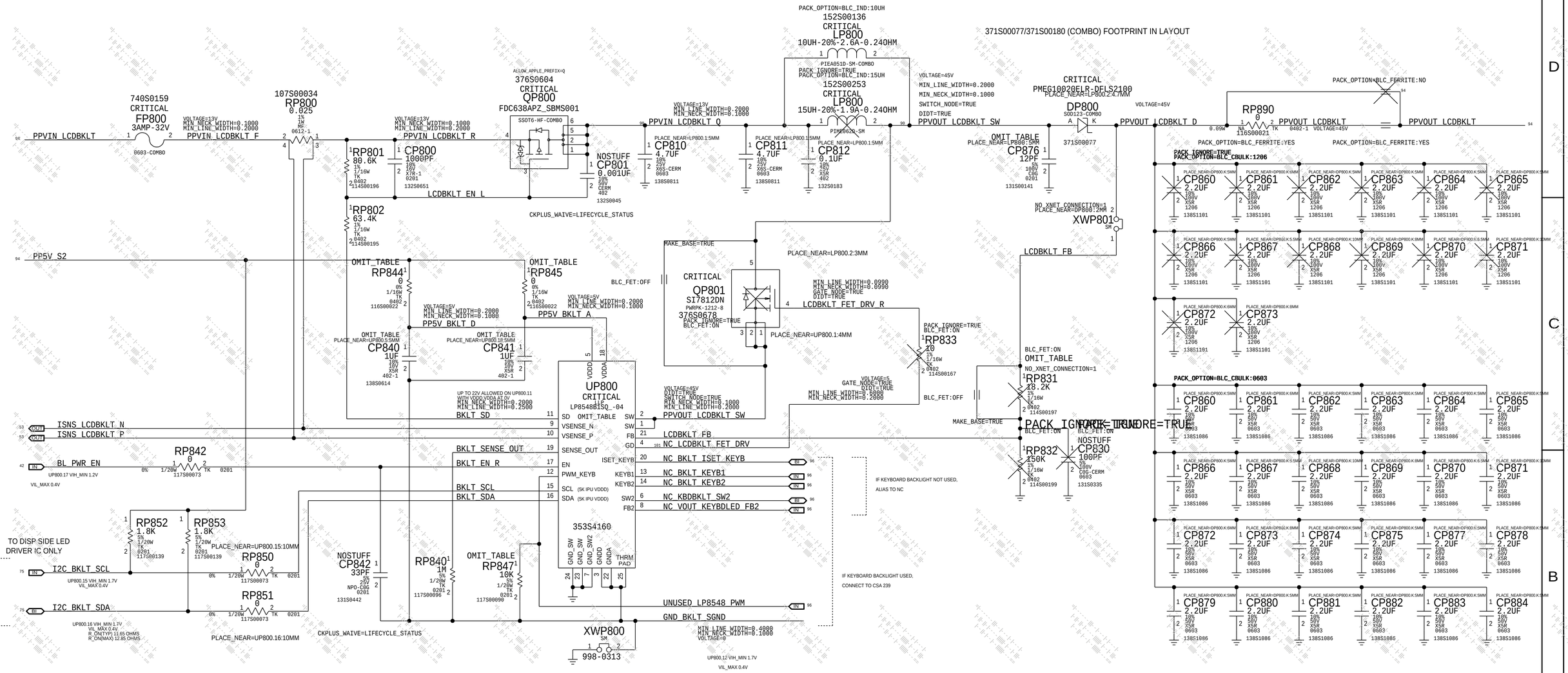
*** OK2INTEGRATE ***

BEN IC: DISPLAY/KBD BACKLIGHT BOOST CONVERTER



BEN IC VERSION TO MATCH VERSION OF JERRY/MINNIE IC IS ON THE PANEL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S4160	1	IC,LP854881-04,DC/DC CVTR,BOOST,QFN-24	UP800		BLC_BEN_IC:V4
353S02256	1	IC,LP854881A-07,DC/DC BOOST CVTR,QFN24	UP800		BLC_BEN_IC:V7
353S02616	1	IC,LP854881A-08,DC/DC BOOST CVTR,QFN24	UP800		BLC_BEN_IC:V8

BACKLIGHT SWITCH NODE DESENSE OPTION

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S00141	1	CAP,C0G,12PF,5%,100V,0201	CP876		BLC_SW_NODE_DESENSE

10K IF KEYBOARD PWM INPUT IS NOT PRESENT (X941. X1536)
100K IF KEYBOARD PWM INPUT IS PRESENT (X1538)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
117S00090	1	RES,TK,10K OHM,5%,1/20W,0201	RP847		BLC_KBD_BOOST_USED:NO
118S00251	1	RES,TK,100K OHM,1%,1/20W,0201	RP847		BLC_KBD_BOOST_USED:YES

BACKLIGHT BOOST VOLTAGE LEVEL BASED ON NUMBER OF LEDS PER STRING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S00197	1	RES,TK,18.2KOHM,1%,1/16W,0402	RP831		BLC_LEDS_PER_STRING:16
114S00198	1	RES,TK,28.7KOHM,1%,1/16W,0402	RP831		BLC_LEDS_PER_STRING:18

BOM OPTION FOR BLC 5V RC FILTER, BASED ON PER PROJECT 5V RIPPLE CHARACTERIZATION
AS COMPARED TO BLC TEAM'S 50 MV RIPPLE SPEC FOR VDDD & VDDA. SEE <RDAR://50682542>

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S00022	2	RES,TK,0 OHM,2A MAX,1/16W,0402	RP844,RP845		BLC_5V_SERIES:0_OHM
114S00167	2	RES,TK,10 OHM,1%,1/16W,0402	RP844,RP845		BLC_5V_SERIES:10_OHM
138S0614	2	CAP,CER,X5R,1UF,10%,10V,0402	CP840,CP841		BLC_5V_CAP:1_UF
138S00070	2	CAP,CER,X5R,4.7UF,20%,25V,0402	CP840,CP841		BLC_5V_CAP:4P7_UF

BOM_COST_GROUP=DISPLAY

SYNC_MASTER=DisplayBacklight SYNC_DATE=09/26/2021

PAGE TITLE
BEN: CONTROLLER

Apple Inc.

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REVISION 6.0.0
BRANCH evt-1
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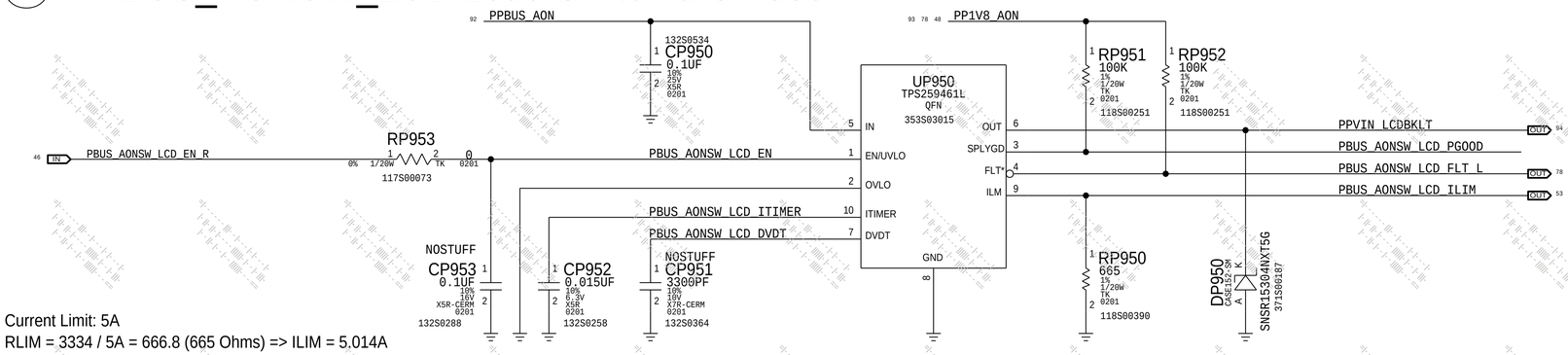
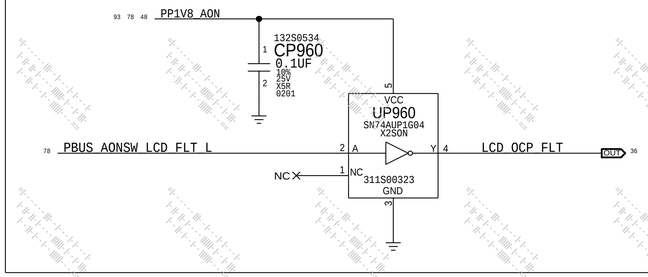
A PPBUS_AONSW_LCD Load Switch & e-Fuse



Current Limit: 5A
RLIM = 3334 / 5A = 666.8 (665 Ohms) => ILIM = 5.014A
/FLT Open Drain
Host-Controlled (EN = MPMU GPIO6, 1.8V LVCMOS (PP1V8_AON))

B LCD_OCP_FLT Control Logic



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER= SYNC_DATE=09/10/2021
PAGE TITLE
BEN: PBUS E-Fuse

Apple Inc.

DRAWING NUMBER 051-07020
SIZE D
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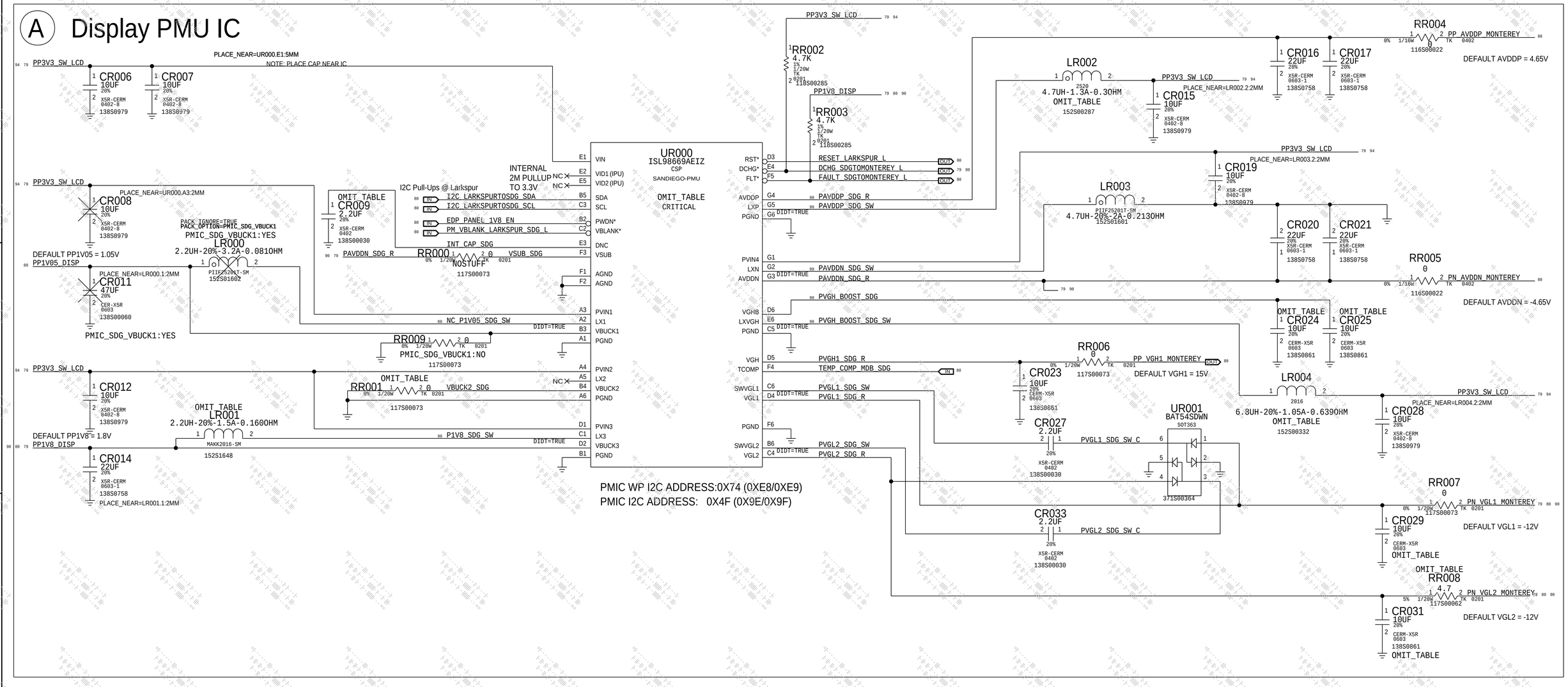
*** OK2INTEGRATE ***

A Display PMU IC



B BOMOPTIONs: TI vs. Intersil

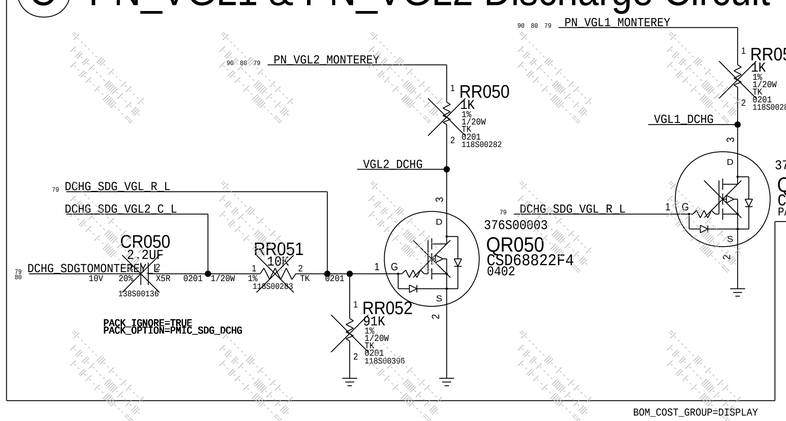
Texas Instruments Option Table

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S00844	1	IC,TPS65157B0E2,PMU,SAN DIEGO,BGA42	UR000	SDG_TI_PROG:X2203
338S00185	1	IC,TPS65157,SAN DIEGO,A1,DSBGA42	UR000	SDG_TI_PROG:BLANK
152S00289	2	IND,4.7UH,2016,PIYA2016T-4R7MDR	LR001	SDG_TI
152S01601	1	IND,MLD,4.7UH,20%,2A,0.213OHM,2520	LR002	SDG_TI
152S00332	1	IND,6.8UH,2016,PISA20161T6R8-013	LR004	SDG_TI
138S0861	2	CAP,CER,10UF.20%,35V,X5R,0603	CR029,CR031	SDG_TI
138S0861	2	CAP,CER,10UF.20%,35V,X5R,0603	CR024,CR025	SDG_TI
138S00030	1	CAP,CER,2.2UF.20%,35V,X5R,0402	CR009	SDG_TI
117S00073	1	RES,TK,0 OHM,1A MAX,1/20W,0201	RR008	SDG_TI

Intersil Option Table

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S00183	1	IC,ISL98669,SAN DIEGO,A1,CSP42	UR000	SDG_ISL
152S1648	2	IND,2.2UH,2016,MAKK2016T2R2M	LR001	SDG_ISL
152S00286	1	IND,2.2UH,2520,VLS252010HBX-2R2M	LR002	SDG_ISL
152S00483	1	IND,10UH,2016,LQE2MEN00MG0	LR004	SDG_ISL
138S0709	2	CAP,CER,4.7UF.10%,35V,X5R,0603	CR029,CR031	SDG_ISL
138S0709	2	CAP,CER,4.7UF.10%,35V,X5R,0603	CR024,CR025	SDG_ISL
116S00022	1	RES,0 OHM,1A,0402	CR009	SDG_ISL
117S00062	1	RES,TK,4.7 OHM,5%,1/20W,0201	RR008	SDG_ISL
117S00073	1	RES,TK,0 OHM,1A MAX,1/20W,0201	RR001	SDG_ISL

C PN_VGL1 & PN_VGL2 Discharge Circuit



SYNC_MASTER=DisplayPMIC SYNC_DATE=09/10/2021

PAGE TITLE

PMU: SAN DIEGO

Apple Inc.

DRAWING NUMBER	051-07020
SIZE	D
REVISION	6.0.0
BRANCH	evt-1
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A Power Connections Alias

75	PP1V8_DISP (MAKE_BASE=TRUE)	=	PP1V8_DISP	79 90
	PP1V05_DISP (MAKE_BASE=TRUE)	=	PP1V05_DISP	79
75	PN_VGL1_MONTEREY (MAKE_BASE=TRUE)	=	PN_VGL1_MONTEREY	79 90
75	PN_VGL2_MONTEREY (MAKE_BASE=TRUE)	=	PN_VGL2_MONTEREY	79 90
75	PP_AVDDP_MONTEREY (MAKE_BASE=TRUE)	=	PP_AVDDP_MONTEREY	79
75	PN_AVDDN_MONTEREY (MAKE_BASE=TRUE)	=	PN_AVDDN_MONTEREY	79
75	PP_VGH1_MONTEREY (MAKE_BASE=TRUE)	=	PP_VGH1_MONTEREY	79
	NC_P1V05_SDG_SW (MAKE_BASE=TRUE)	=	NC_P1V05_SDG_SW	79

B Signal Connections Alias

75	I2C_LARKSPURTOSDG_SDA (MAKE_BASE=TRUE CKPLUS_WAIVE=I2C_PULLUP)	=	I2C_LARKSPURTOSDG_SDA	79
	I2C Pull-Up @ Larkspur			
75	I2C_LARKSPURTOSDG_SCL (MAKE_BASE=TRUE CKPLUS_WAIVE=I2C_PULLUP)	=	I2C_LARKSPURTOSDG_SCL	79
	I2C Pull-Up @ Larkspur			
76	EDP_PANEL_1V8_EN (MAKE_BASE=TRUE)	=	EDP_PANEL_1V8_EN	79
75	PM_VBLANK_LARKSPUR_SDG_L (MAKE_BASE=TRUE)	=	PM_VBLANK_LARKSPUR_SDG_L	79
75	RESET_LARKSPUR_L (MAKE_BASE=TRUE)	=	RESET_LARKSPUR_L	79
75	DCHG_SDGTOMONTEREY_L (MAKE_BASE=TRUE)	=	DCHG_SDGTOMONTEREY_L	79
75	FAULT_SDGTOMONTEREY_L (MAKE_BASE=TRUE)	=	FAULT_SDGTOMONTEREY_L	79
75	TEMP_COMP_MDB_SDG (MAKE_BASE=TRUE)	=	TEMP_COMP_MDB_SDG	79

SYNC_DATE=09/10/2021

PAGE TITLE: PMU: SAN DIEGO SUPPORT

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D

REVISION: 6.0.0

BRANCH: evt-1

PAGE: 241 OF 801

SHEET: 80 OF 113

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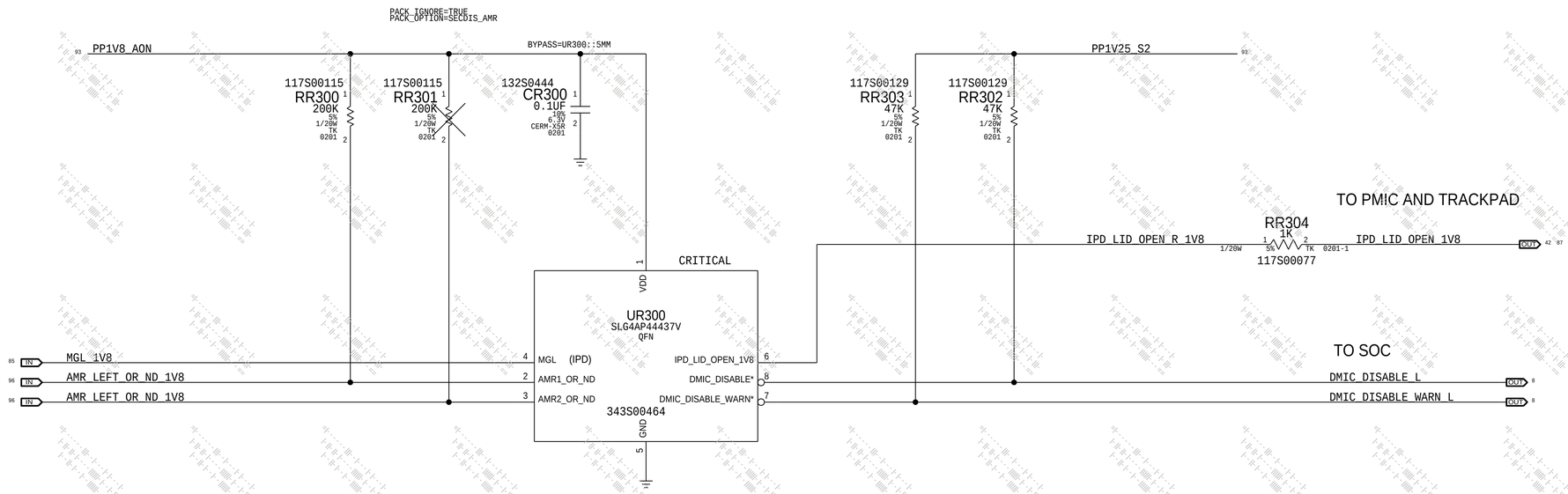
*** OK2INTEGRATE ***

LID SECDIS LOGIC



BOM_COST_GROUP=SOC

PAGE TITLE	SECDIS: SAK
Apple Inc.	DRAWING NUMBER 051-07020 / SIZE D
	REVISION 6.0.0
	BRANCH evt-1
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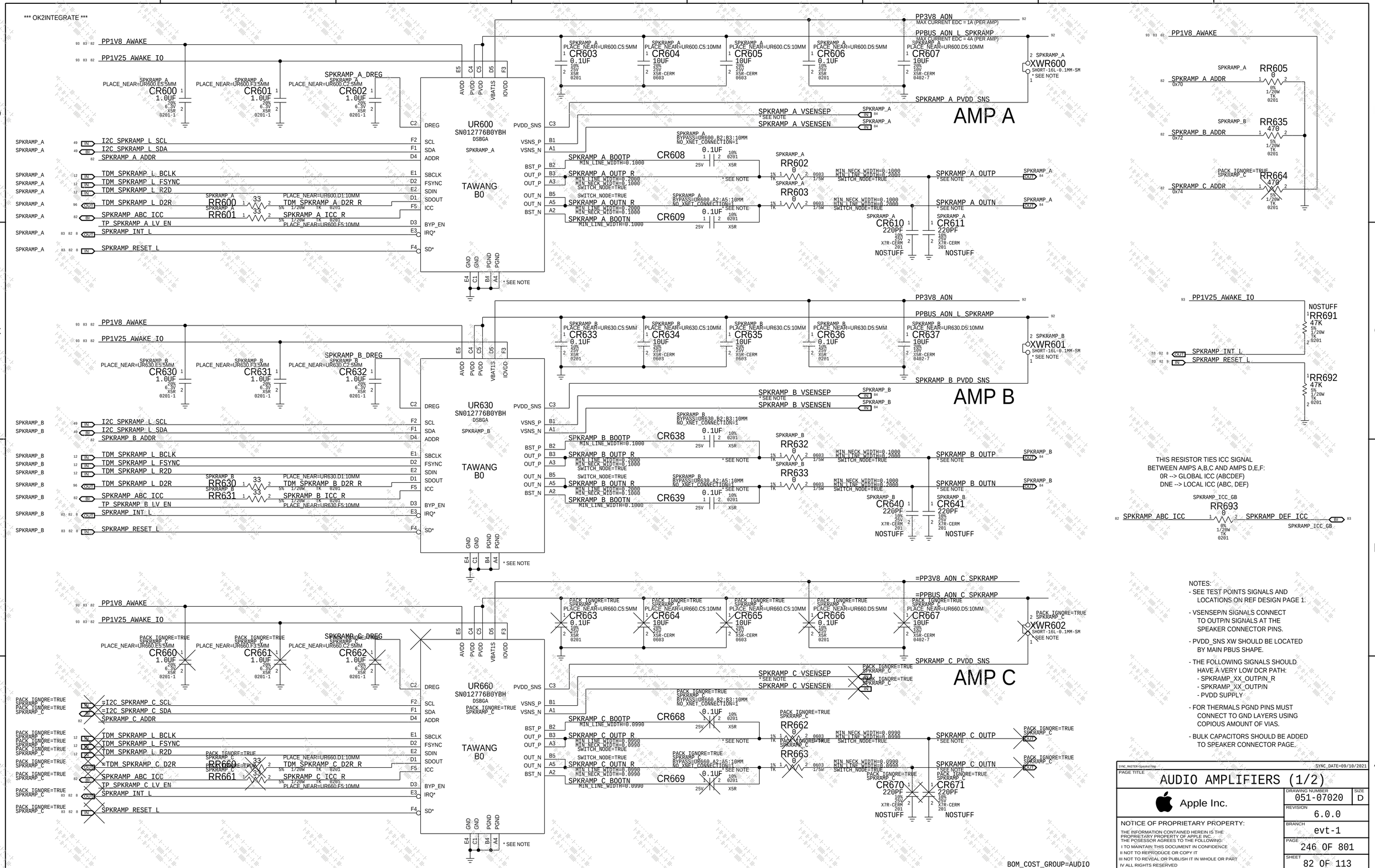
*** OK2INTEGRATE ***
AMP A
AMP B
AMP C
UR600
UR630
UR660
SN012776B0YBH
TAWANG B0
PP3V8_AON
PPBUS_AON_L_SPKRAMP
PP1V8_AWAKE
PP1V25_AWAKE_IO
SPKRAMP_A_PVDD_SNS
SPKRAMP_B_PVDD_SNS
SPKRAMP_C_PVDD_SNS
=PP3V8_AON_C_SPKRAMP
=PPBUS_AON_C_SPKRAMP
SPKRAMP_A_VSENSEP
SPKRAMP_A_VSENSEN
SPKRAMP_B_VSENSEP
SPKRAMP_B_VSENSEN
SPKRAMP_C_VSENSEP
SPKRAMP_C_VSENSEN
SPKRAMP_A_OUTP
SPKRAMP_A_OUTN
SPKRAMP_B_OUTP
SPKRAMP_B_OUTN
SPKRAMP_C_OUTP
SPKRAMP_C_OUTN
SPKRAMP_INT_L
SPKRAMP_RESET_L
SPKRAMP_ABC_ICC
SPKRAMP_ICC_GB
THIS RESISTOR TIES ICC SIGNAL
BETWEEN AMPS A,B,C AND AMPS D,E,F:
0R --> GLOBAL ICC (ABCDEF)
DNE --> LOCAL ICC (ABC, DEF)
NOTES:
- SEE TEST POINTS SIGNALS AND LOCATIONS ON REF DESIGN PAGE 1.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- PVDD_SNS XW SHOULD BE LOCATED BY MAIN PBUS SHAPE.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
- SPKRAMP_XX_OUTP/N_R
- SPKRAMP_XX_OUTP/N
- PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.
- BULK CAPACITORS SHOULD BE ADDED TO SPEAKER CONNECTOR PAGE.
BOM_COST_GROUP=AUDIO
PAGE TITLE
AUDIO AMPLIFIERS (1/2)
Apple Inc.
DRAWING NUMBER 051-07020
SIZE D
REVISION 6.0.0
BRANCH evt-1
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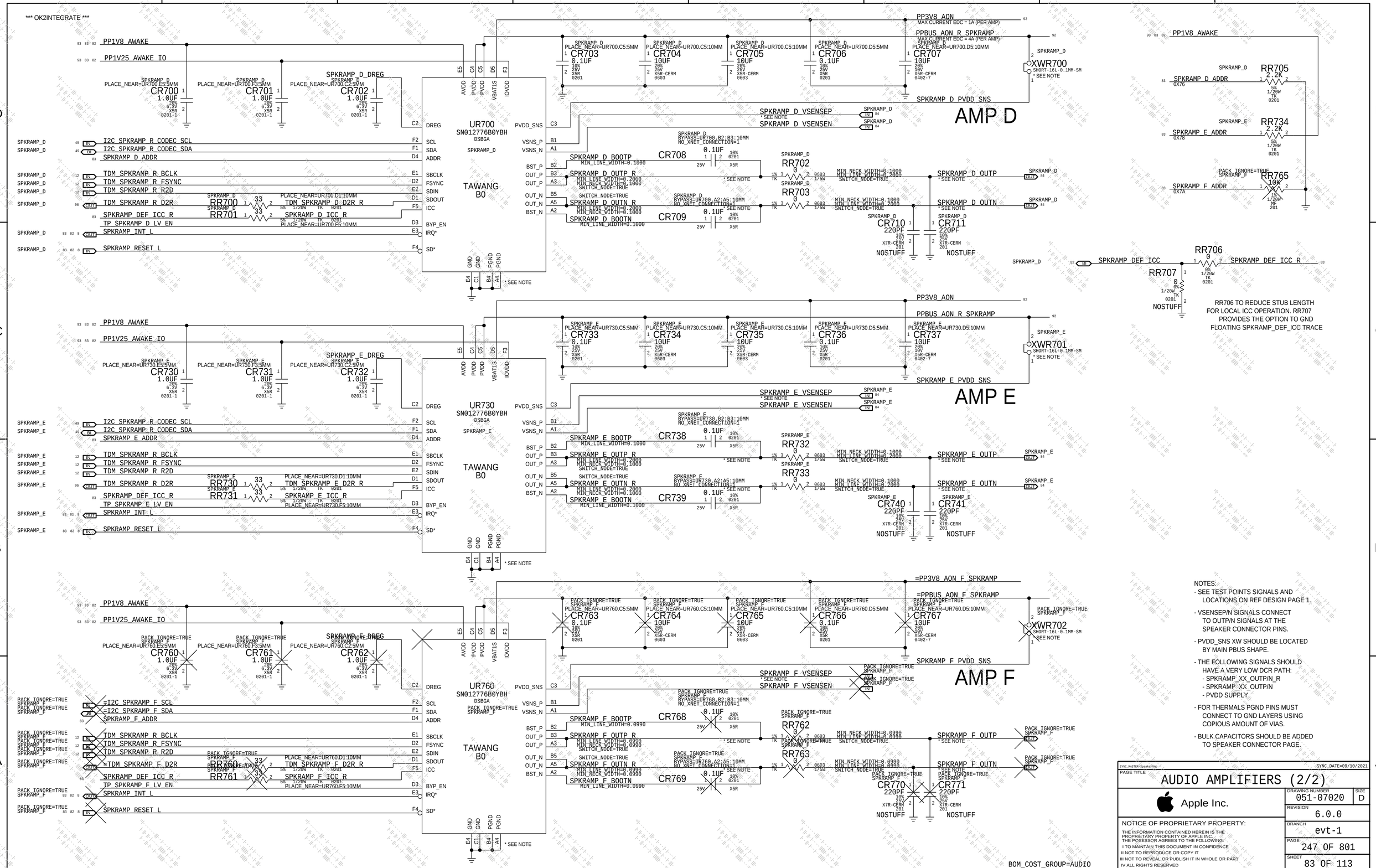

NOTES:
- SEE TEST POINTS SIGNALS AND LOCATIONS ON REF DESIGN PAGE 1.
- VSENSEP/N SIGNALS CONNECT TO OUTP/N SIGNALS AT THE SPEAKER CONNECTOR PINS.
- PVDD_SNS XW SHOULD BE LOCATED BY MAIN PBUS SHAPE.
- THE FOLLOWING SIGNALS SHOULD HAVE A VERY LOW DCR PATH:
  - SPKRAMP_XX_OUTP/N_R
  - SPKRAMP_XX_OUTP/N
  - PVDD SUPPLY
- FOR THERMALS PGND PINS MUST CONNECT TO GND LAYERS USING COPIOUS AMOUNT OF VIAS.
- BULK CAPACITORS SHOULD BE ADDED TO SPEAKER CONNECTOR PAGE.

SYNC_MASTER=Speaker1 SYNC_DATE=09/10/2021

PAGE TITLE: AUDIO AMPLIFIERS (2/2)

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D

REVISION: 6.0.0

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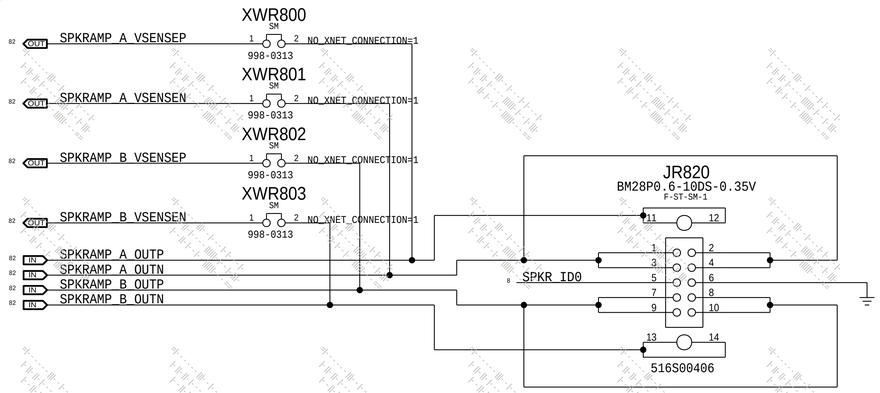
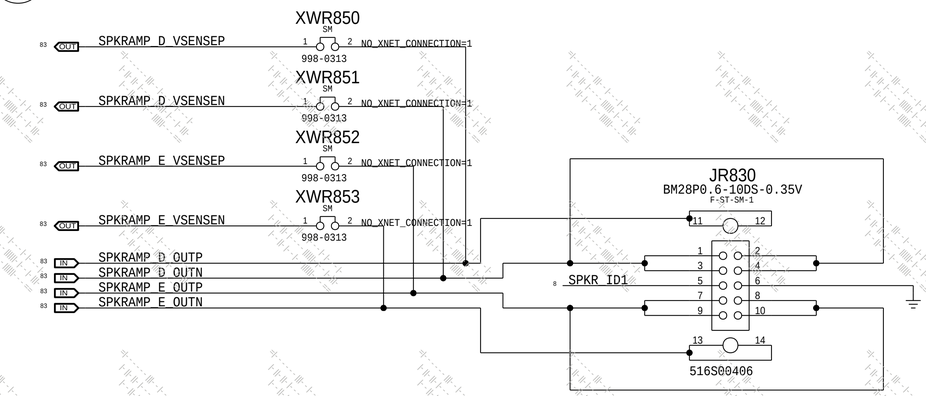
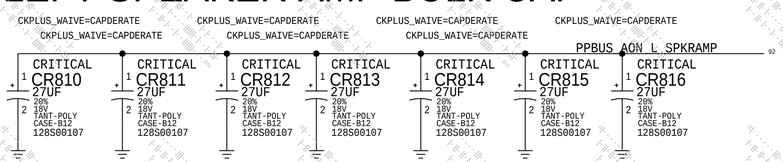
A LEFT SPEAKER CONNECTOR



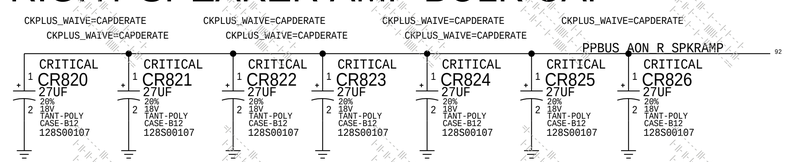
B RIGHT SPEAKER CONNECTOR



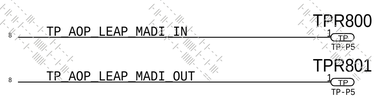
C LEFT SPEAKER AMP BULK CAP



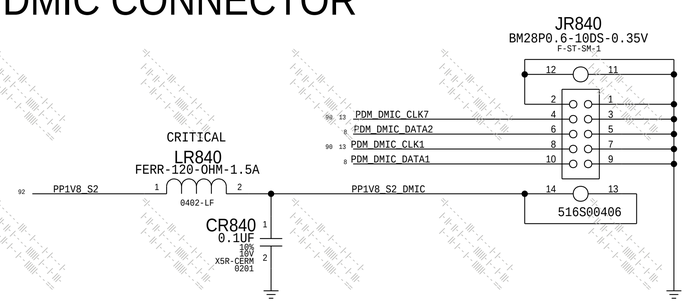
D RIGHT SPEAKER AMP BULK CAP



E MADI TEST POINT



F DMIC CONNECTOR



BOM_COST_GROUP=AUDIO

DESIGN: T651/MLB
LAST CHANGE: Fri Oct 11 18:06:02 2019

PAGE TITLE: Audio Connectors

Apple Inc.

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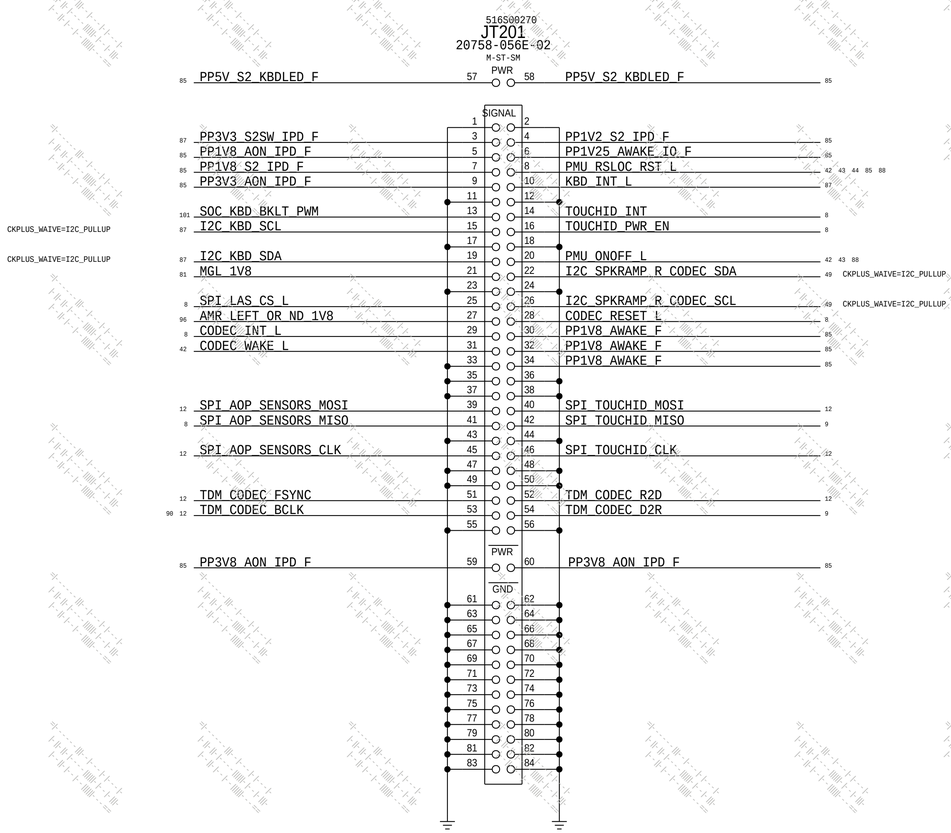
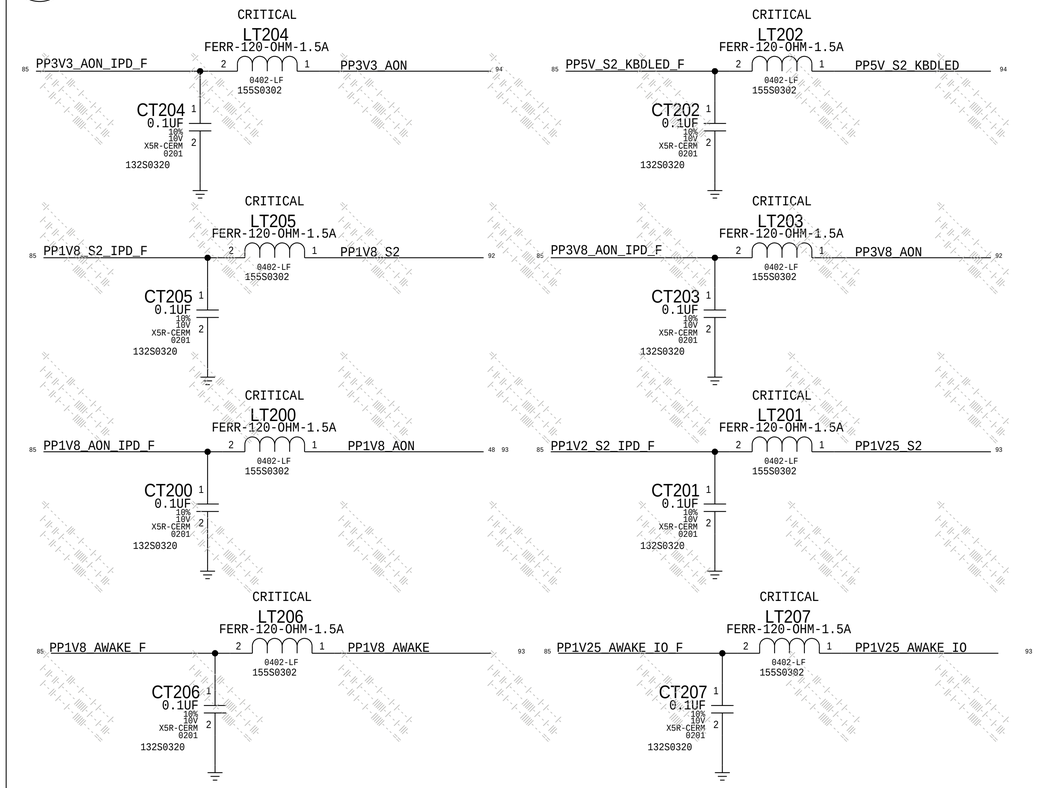
A KBD B2B CONNECTOR

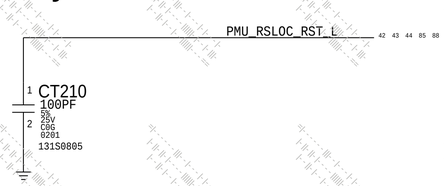


KBD Flex Receptacle APN 516S00457

B KBD PWR FILTER



C Keyboard Control



BOM_COST_GROUP=KEYBOARD

PAGE TITLE	Keyboard Connector
Apple Inc.	DRAWING NUMBER 051-07020 SIZE D
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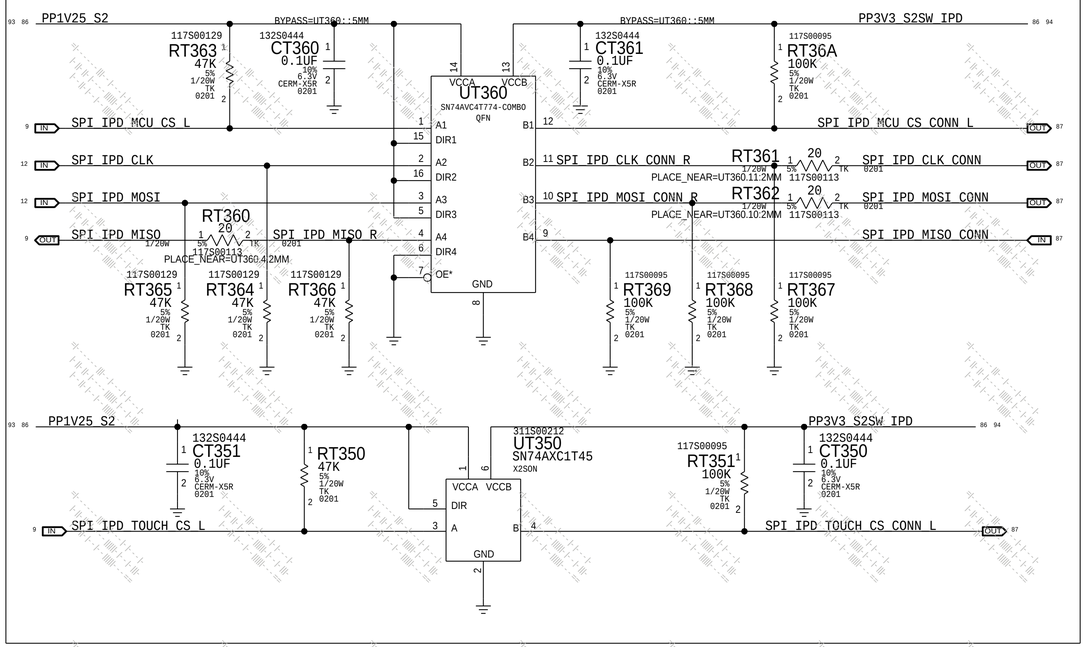
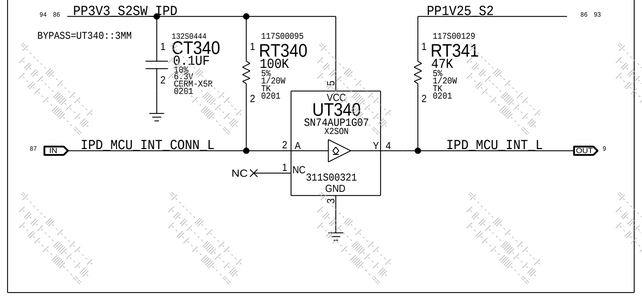
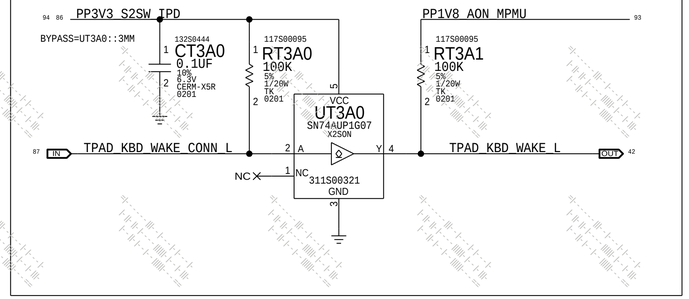
A Trackpad SPI Bus Level Shifter



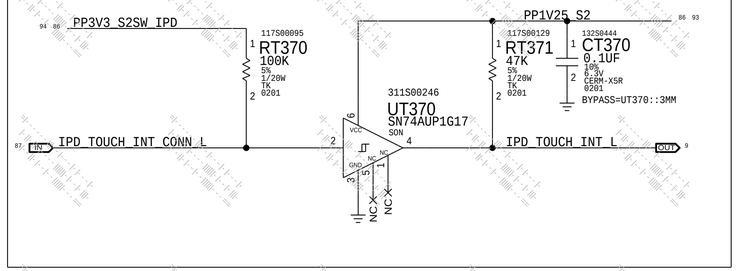
B Trackpad MCU_INT_L LS



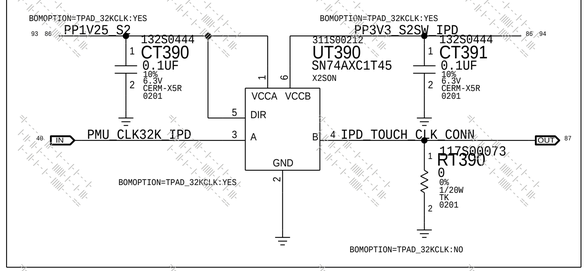
C Trackpad WAKE_L LS



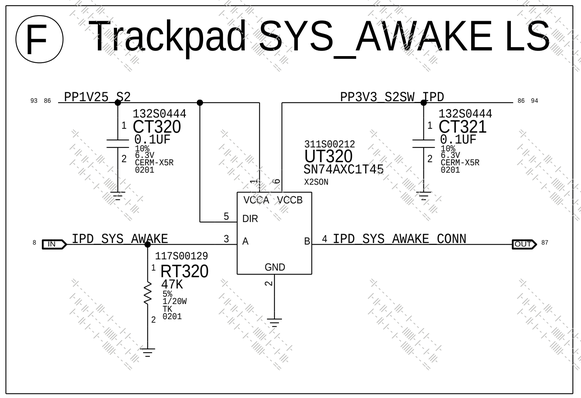
D Trackpad TOUCH_INT_L LS



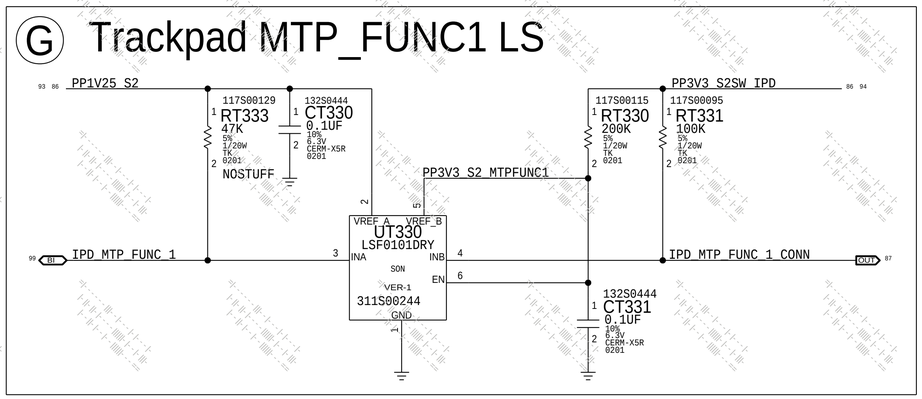
E Trackpad 32kHz Clock LS



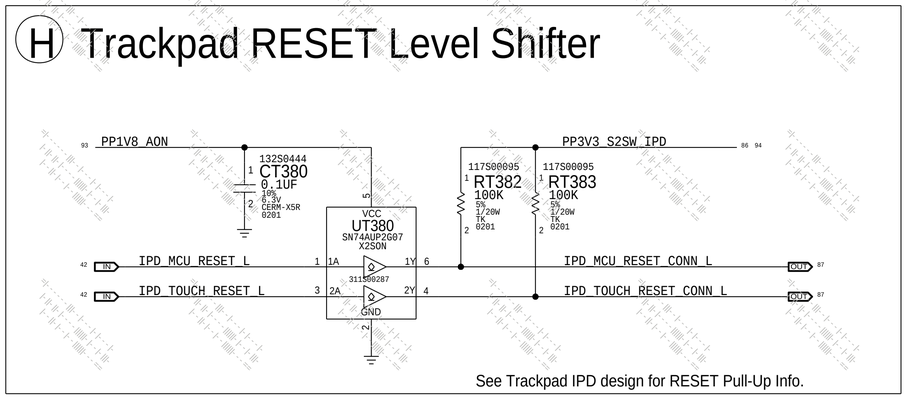
F Trackpad SYS_AWAKE LS



G Trackpad MTP_FUNC1 LS

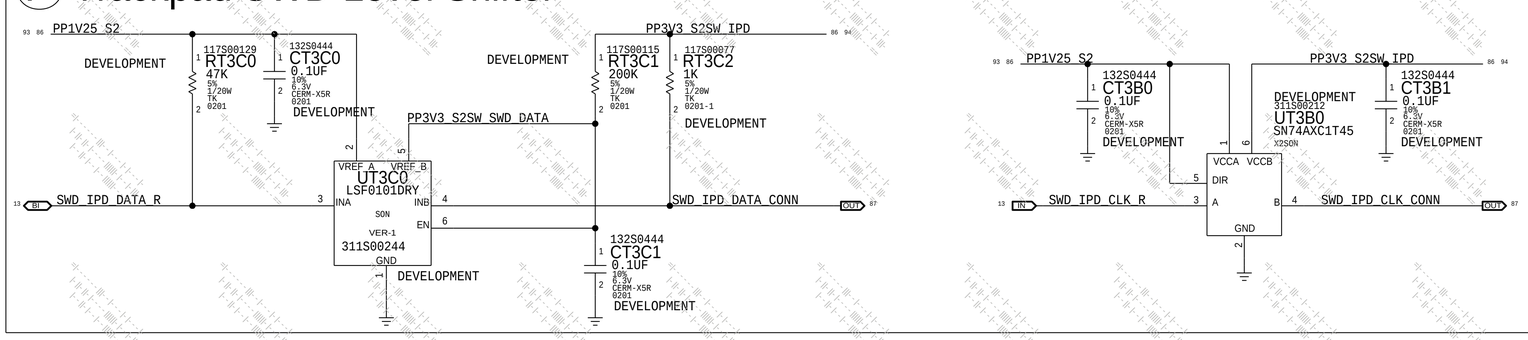


H Trackpad RESET Level Shifter



See Trackpad IPD design for RESET Pull-Up Info.

I Trackpad SWD Level Shifter



BOM_COST_GROUP=TRACKPAD

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Apple Inc.	DRAWING NUMBER 051-07020 SIZE D
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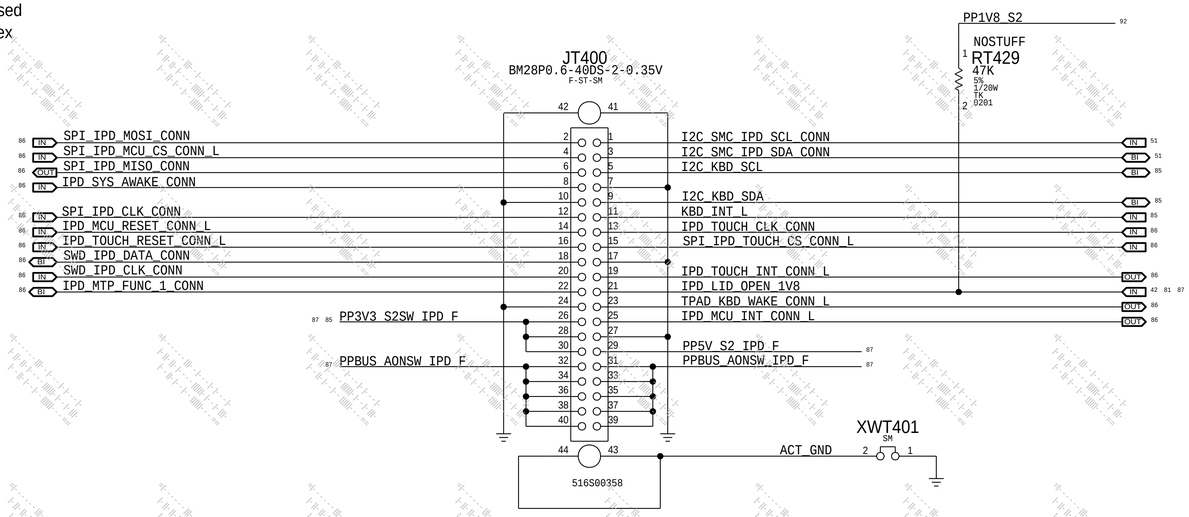
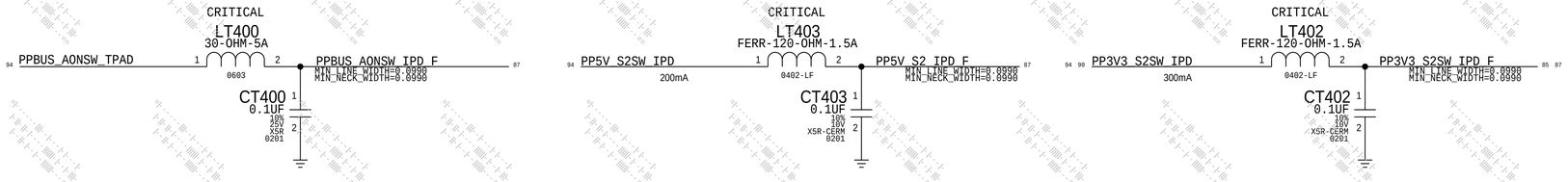
A Trackpad Connector

Bottom side contacts used
Pinout reversed from flex



C Trackpad Control

B Trackpad Power Supply Filters



BOM_COST_GROUP=TRACKPAD

SYNC_MASTER= SYNC_DATE=09/10/2021

PAGE TITLE: Trackpad Connector

Apple Inc.

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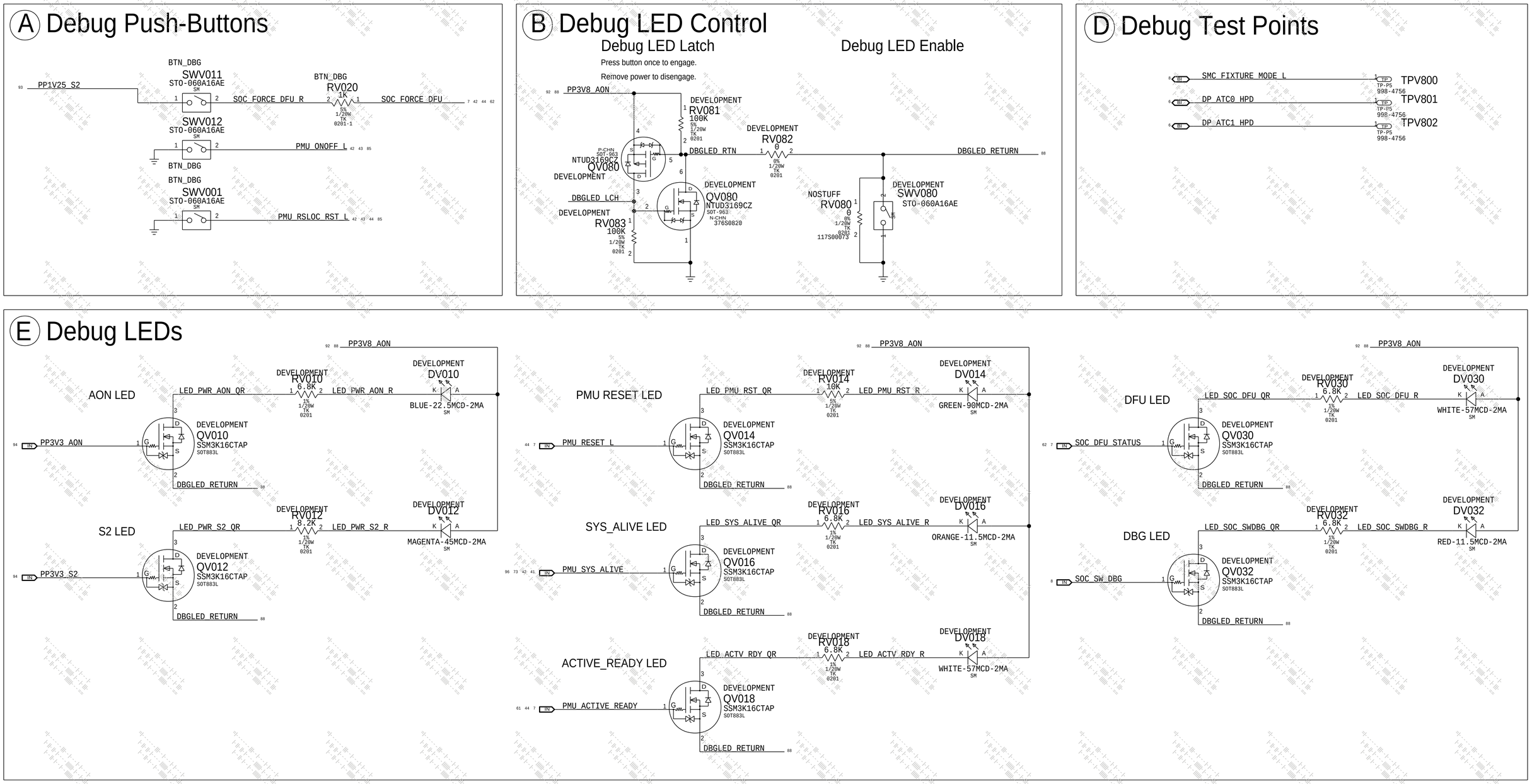

BOM_COST_GROUP=DEBUG

SYNC_MASTER=jawe65 SYNC_DATE=09/28/2021

PAGE TITLE: DEBUG

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D

REVISION: 6.0.0

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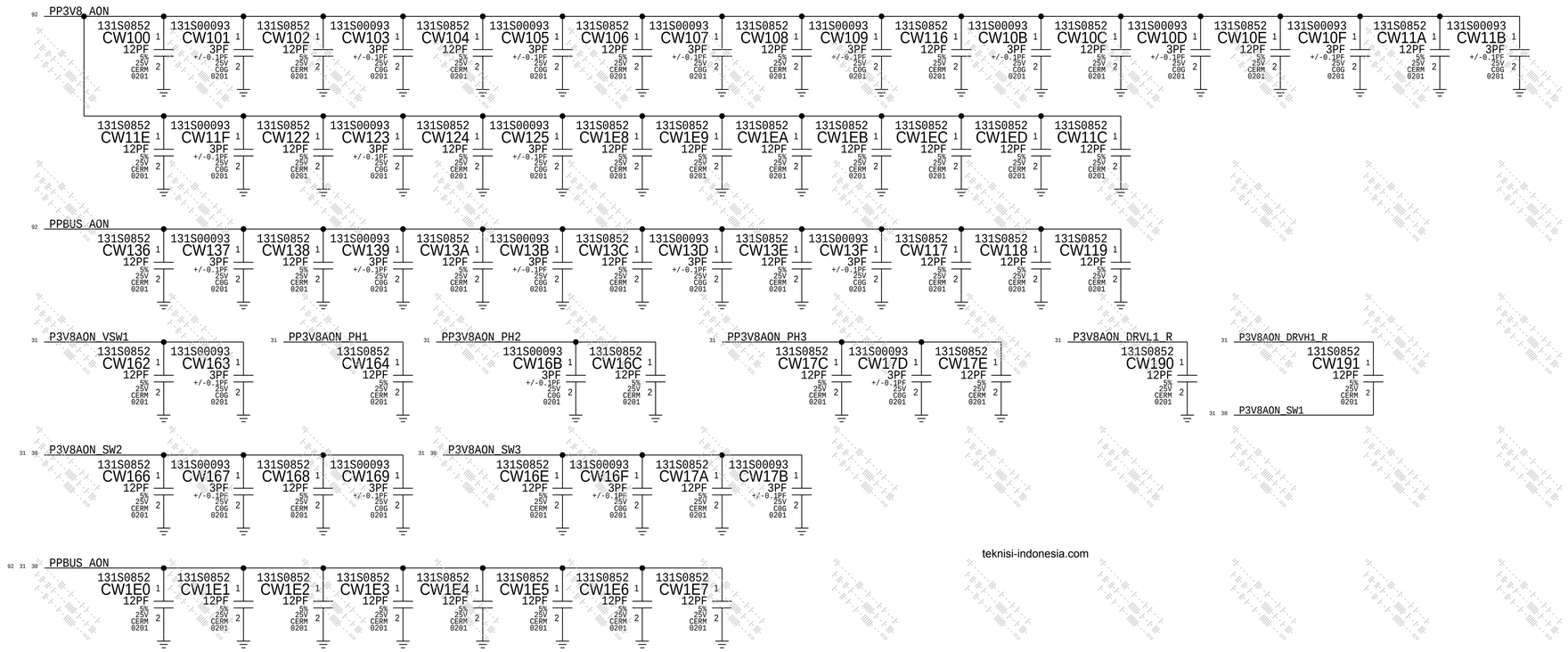
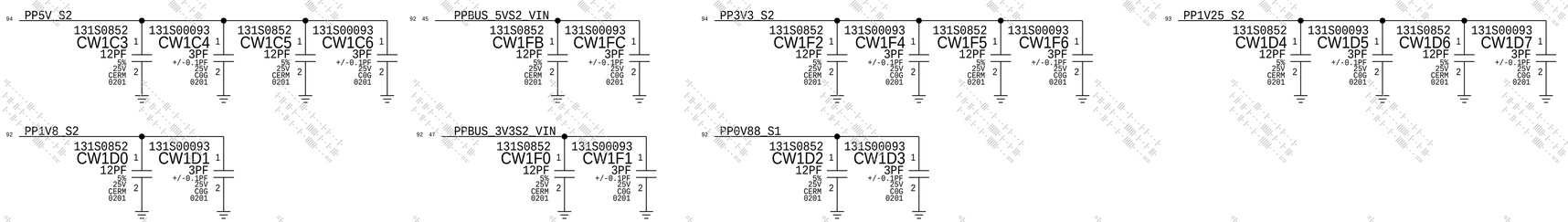
A ICEMAN Desense



teknisi-indonesia.com

B BUCK POWER Desense



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09/10/2021

PAGE TITLE: Desense 1

Apple Inc.

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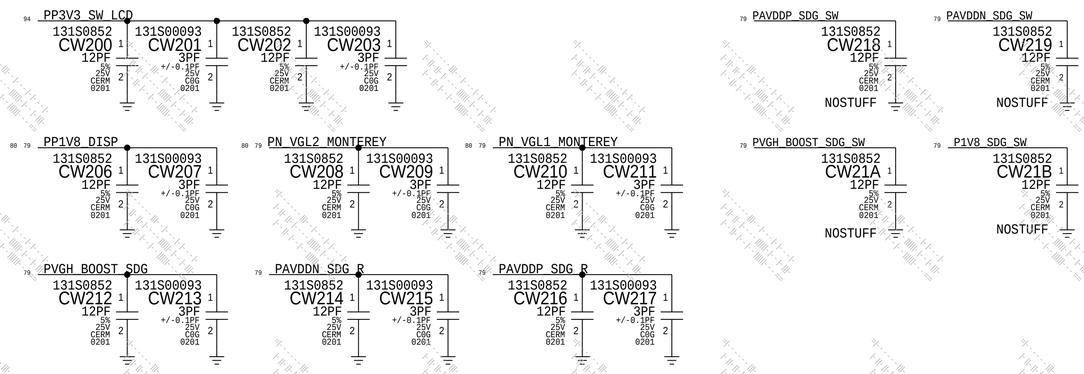
A Display PMIC Desense



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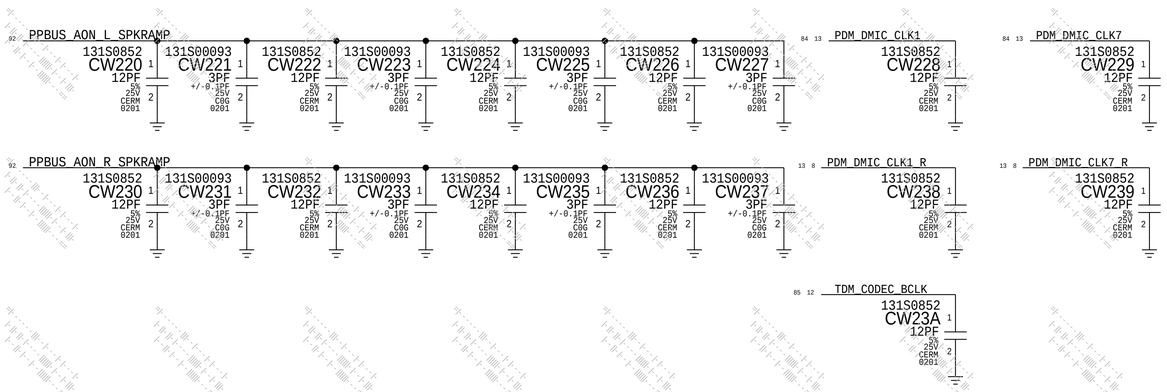
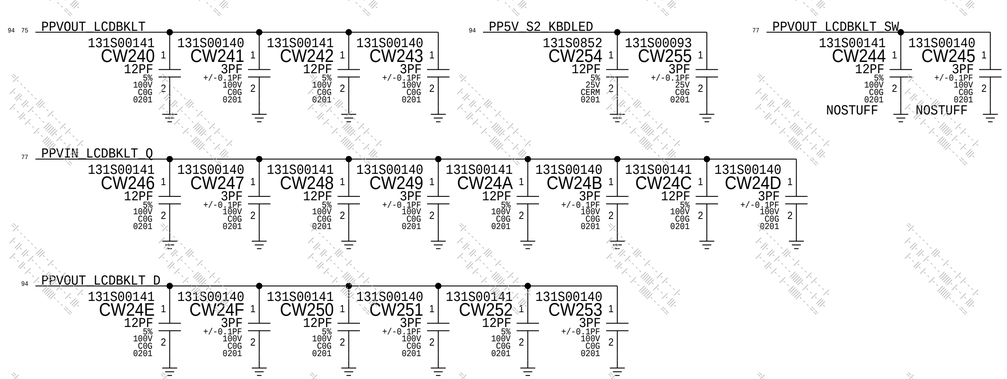


C Display and Keyboard Backlight Desense



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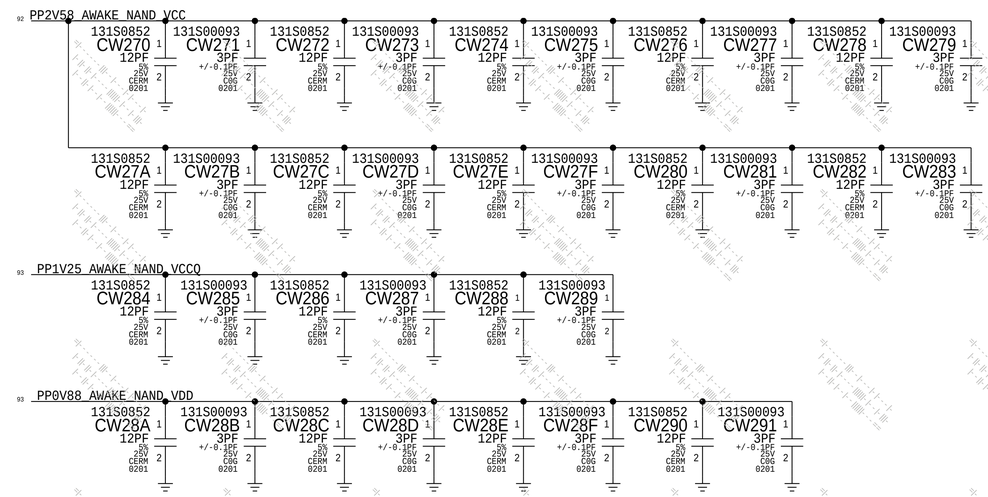
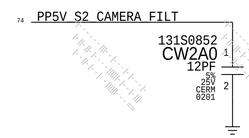
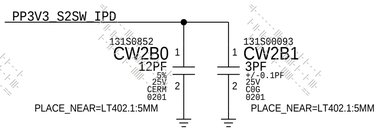


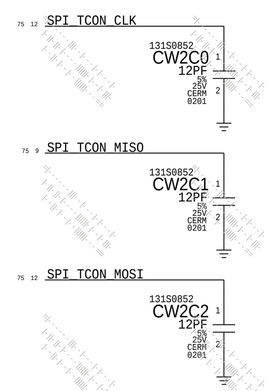
E Camera Desense



F Trackpad Desense



G Display TCON Desense



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	Apple Inc.
DRAWING NUMBER	051-07020
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A SOC Desense

Net	Pin 1	Pin 2
92 91 PPVDD_AWAKE_PCPU	CW300 131S0852 12PF 5% 25V CERM 0201	CW301 131S00093 3PF +/-0.1PF 25V C0G 0201
92 91 PPVDD_AWAKE_PCPU	CW302 131S0852 12PF 5% 25V CERM 0201	CW303 131S00093 3PF +/-0.1PF 25V C0G 0201
92 91 PPVDD_AWAKE_CPU_SRAM	CW304 131S0852 12PF 5% 25V CERM 0201	CW305 131S00093 3PF +/-0.1PF 25V C0G 0201
92 91 PPVDD_AWAKE_CPU_SRAM	CW306 131S0852 12PF 5% 25V CERM 0201	CW307 131S00093 3PF +/-0.1PF 25V C0G 0201
92 91 PPVDD_S1_SOC	CW308 131S0852 12PF 5% 25V CERM 0201	CW309 131S00093 3PF +/-0.1PF 25V C0G 0201
92 91 PPVDD_S1_SOC	CW310 131S0852 12PF 5% 25V CERM 0201	CW311 131S00093 3PF +/-0.1PF 25V C0G 0201
92 91 PPVDD_S1_DCS	CW312 131S0852 12PF 5% 25V CERM 0201	CW313 131S00093 3PF +/-0.1PF 25V C0G 0201
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92 91 PP0V779_S1_SRAM	CW316 131S0852 12PF 5% 25V CERM 0201	CW317 131S00093 3PF +/-0.1PF 25V C0G 0201
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92 91 PPVDD_S1_DISP	CW322 131S0852 12PF 5% 25V CERM 0201	CW323 131S00093 3PF +/-0.1PF 25V C0G 0201
92 91 PPVDD_AWAKE_GPU	CW324 131S0852 12PF 5% 25V CERM 0201	CW325 131S00093 3PF +/-0.1PF 25V C0G 0201
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92 91 PP1V05_S2SW_VDD2H	CW328 131S0852 12PF 5% 25V CERM 0201	CW329 131S00093 3PF +/-0.1PF 25V C0G 0201
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93 91 PP1V12_S2SW_AMPH	CW334 131S0852 12PF 5% 25V CERM 0201	CW335 131S00093 3PF +/-0.1PF 25V C0G 0201
92 91 PPVDD_AWAKE_ECPU	CW336 131S0852 12PF 5% 25V CERM 0201	CW337 131S00093 3PF +/-0.1PF 25V C0G 0201
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92 PP0V72_S2_VDD_LOW	CW33C 131S0852 12PF 5% 25V CERM 0201	CW33D 131S00093 3PF +/-0.1PF 25V C0G 0201
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	CW355 131S0852 12PF 5% 25V CERM 0201	CW356 131S00093 3PF +/-0.1PF 25V C0G 0201
	CW357 131S0852 12PF 5% 25V CERM 0201	CW358 131S00093 3PF +/-0.1PF 25V C0G 0201
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BOM_COST_GROUP=DESENSE

09/10/2021

PAGE TITLE: Desense 3

Apple Inc.

DRAWING NUMBER: 051-07020 SIZE: D

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USBC DCIN

61 PPDCIN_AON_CHGR

PPDCIN_AON_CHGR
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PPDCIN_AON_CHGR 25 29
PPDCIN_AON_CHGR 52

PBUS

25 PPBUS_AON

PPBUS_AON
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MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.0970

PPBUS_AON 54
PPBUS_AON 54
PPBUS_AON 78
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PPBUS_AON 52
PPBUS_AON 89

52 PPBUS_5VS2_VIN

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MIN_NECK_WIDTH=0.1000
MAKE_BASE=TRUE

PPBUS_5VS2_VIN 45 89

52 PPBUS_3V3S2_VIN

PPBUS_3V3S2_VIN
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MIN_NECK_WIDTH=0.1000
MAKE_BASE=TRUE

PPBUS_3V3S2_VIN 47 89

54 PPBUS_AON_L_SPKRAMP

PPBUS_AON_L_SPKRAMP
MIN_LINE_WIDTH=0.0970
MIN_NECK_WIDTH=0.1000
MAKE_BASE=TRUE

PPBUS_AON_L_SPKRAMP 84
PPBUS_AON_L_SPKRAMP 82
PPBUS_AON_L_SPKRAMP 82
PPBUS_AON_L_SPKRAMP 90

54 PPBUS_AON_R_SPKRAMP

PPBUS_AON_R_SPKRAMP
MIN_LINE_WIDTH=0.0970
MIN_NECK_WIDTH=0.1000
MAKE_BASE=TRUE

PPBUS_AON_R_SPKRAMP 84
PPBUS_AON_R_SPKRAMP 83
PPBUS_AON_R_SPKRAMP 83
PPBUS_AON_R_SPKRAMP 90

P3V8 VDD_MAIN

31 PP3V8_AON

PP3V8_AON
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V8_AON 49
PP3V8_AON 88
PP3V8_AON 23
PP3V8_AON 54
PP3V8_AON 37 39 40 42
PP3V8_AON 39
PP3V8_AON 40
PP3V8_AON 33 36
PP3V8_AON 34
PP3V8_AON 34
PP3V8_AON 34
PP3V8_AON 34
PP3V8_AON 48
PP3V8_AON 24
PP3V8_AON 39
PP3V8_AON 82
PP3V8_AON 82
PP3V8_AON 83
PP3V8_AON 83
PP3V8_AON 32
PP3V8_AON 46
PP3V8_AON 67
PP3V8_AON 67
PP3V8_AON 67
PP3V8_AON 67
PP3V8_AON 85

P3V8 VDD_MAIN WLBT

54 PP3V8_AON_WLBT

PP3V8_AON_WLBT
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V8_AON_WLBT 69

MPMU BUCK 0

37 PPVDD_AWAKE_PCPU

PPVDD_AWAKE_PCPU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PPVDD_AWAKE_PCPU 14
PPVDD_AWAKE_PCPU 91
PPVDD_AWAKE_PCPU 37

MPMU BUCK 1

37 PPVDD_AWAKE_GPU

PPVDD_AWAKE_GPU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PPVDD_AWAKE_GPU 17
PPVDD_AWAKE_GPU 91
PPVDD_AWAKE_GPU 37

MPMU BUCK 2

37 PPVDD_S1_SOC

PPVDD_S1_SOC
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PPVDD_S1_SOC 15
PPVDD_S1_SOC 37
PPVDD_S1_SOC 91

MPMU BUCK 3

43 38 PP1V8_S2

PP1V8_S2
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V8_S2 84
PP1V8_S2 38
PP1V8_S2 89
PP1V8_S2 38
PP1V8_S2 38
PP1V8_S2 38
PP1V8_S2 34
PP1V8_S2 33
PP1V8_S2 48
PP1V8_S2 76
PP1V8_S2 85
PP1V8_S2 87
PP1V8_S2 23
PP1V8_S2 57
PP1V8_S2 74
PP1V8_S2 69
PP1V8_S2 25 26
PP1V8_S2 75
PP1V8_S2 50
PP1V8_S2 50
PP1V8_S2 51
PP1V8_S2 51
PP1V8_S2 63
PP1V8_S2 64
PP1V8_S2 65
PP1V8_S2 65

MPMU BUCK 4

38 PP1V05_S2SW_VDD2H

PP1V05_S2SW_VDD2H
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.5000

PP1V05_S2SW_VDD2H 18
PP1V05_S2SW_VDD2H 39
PP1V05_S2SW_VDD2H 39 Powers Unused MPMU LDO16
PP1V05_S2SW_VDD2H 38
PP1V05_S2SW_VDD2H 91

SPMU BUCK 5

33 PP0V779_S1_SRAM

PP0V779_S1_SRAM
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP0V779_S1_SRAM 16
PP0V779_S1_SRAM 33
PP0V779_S1_SRAM 91

SPMU BUCK 6

33 PP2V58_AWAKE_NAND_VCC

PP2V58_AWAKE_NAND_VCC
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP2V58_AWAKE_NAND_VCC 71 72
PP2V58_AWAKE_NAND_VCC 90
PP2V58_AWAKE_NAND_VCC 33

MPMU BUCK 7

38 PPVDD_AWAKE_CPU_SRAM

PPVDD_AWAKE_CPU_SRAM
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.0990
MIN_LINE_WIDTH=0.2000

PPVDD_AWAKE_CPU_SRAM 16
PPVDD_AWAKE_CPU_SRAM 91
PPVDD_AWAKE_CPU_SRAM 38

SPMU BUCK 8

33 PPVDD_S1_DISP

PPVDD_S1_DISP
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PPVDD_S1_DISP 17
PPVDD_S1_DISP 91
PPVDD_S1_DISP 33

MPMU BUCK 9

38 PPVDD_S1_DCS

PPVDD_S1_DCS
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PPVDD_S1_DCS 16
PPVDD_S1_DCS 91
PPVDD_S1_DCS 38

SPMU BUCK 10

33 PP0V5_S1_VDDQL

PP0V5_S1_VDDQL
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP0V5_S1_VDDQL 7 18
PP0V5_S1_VDDQL 91
PP0V5_S1_VDDQL 33

MPMU BUCK 11

38 PPVDD_AWAKE_ECPU

PPVDD_AWAKE_ECPU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PPVDD_AWAKE_ECPU 19
PPVDD_AWAKE_ECPU 91
PPVDD_AWAKE_ECPU 38

SPMU BUCK 12

33 PP0V88_S1

PP0V88_S1
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.0990
MIN_LINE_WIDTH=0.2000

PP0V88_S1 34
PP0V88_S1 34
PP0V88_S1 34
PP0V88_S1 33
PP0V88_S1 89

P5V LDO5

30 PP5V_AON

PP5V_AON
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP5V_AON
GDS_LDO_Active 30

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MPMU BUCK 13

43 38 PP1V25_S2 — PP1V25_S2
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V25_S2 — 88
PP1V25_S2 — 38
PP1V25_S2 — 89
PP1V25_S2 — 36
PP1V25_S2 — 38
PP1V25_S2 — 33
PP1V25_S2 — 34
PP1V25_S2 — 34
PP1V25_S2 — 42
PP1V25_S2 — 20
PP1V25_S2 — 21
PP1V25_S2 — 21
PP1V25_S2 — 26
PP1V25_S2 — 26
PP1V25_S2 — 7
PP1V25_S2 — 50
PP1V25_S2 — 51
PP1V25_S2 — 51
PP1V25_S2 — 51
PP1V25_S2 — 51
PP1V25_S2 — 50
PP1V25_S2 — 49
PP1V25_S2 — 81
PP1V25_S2 — 21
PP1V25_S2 — 69
PP1V25_S2 — 57
PP1V25_S2 — 26
PP1V25_S2 — 28
PP1V25_S2 — 61 63 64
PP1V25_S2 — 74
PP1V25_S2 — 85
PP1V25_S2 — 66
PP1V25_S2 — 66
PP1V25_S2 — 66
PP1V25_S2 — 68
PP1V25_S2 — 76
PP1V25_S2 — 86

SPMU BUCK 14

33 PP1V12_S2SW_AMPH — PP1V12_S2SW_AMPH
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V12_S2SW_AMPH — 18
PP1V12_S2SW_AMPH — 33
PP1V12_S2SW_AMPH — 91

MPMU BUCK 3 SW 1

38 PP1V8_AWAKE — PP1V8_AWAKE
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V8_AWAKE — 21
PP1V8_AWAKE — 11
PP1V8_AWAKE — 85
PP1V8_AWAKE — 82 83

MPMU BUCK 3 SW 2

38 NC_PPVOUT_MPMU_SW2_REG — NC_PPVOUT_MPMU_SW2_REG
MAKE_BASE=TRUE

MPMU BUCK 13 SW 3

38 PP1V25_AWAKE_IO — PP1V25_AWAKE_IO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V25_AWAKE_IO — 21
PP1V25_AWAKE_IO — 21
PP1V25_AWAKE_IO — 21
PP1V25_AWAKE_IO — 21
PP1V25_AWAKE_IO — 21
PP1V25_AWAKE_IO — 20
PP1V25_AWAKE_IO — 20
PP1V25_AWAKE_IO — 20
PP1V25_AWAKE_IO — 20
PP1V25_AWAKE_IO — 20
PP1V25_AWAKE_IO — 20
PP1V25_AWAKE_IO — 20
PP1V25_AWAKE_IO — 13
PP1V25_AWAKE_IO — 11
PP1V25_AWAKE_IO — 11
PP1V25_AWAKE_IO — 5
PP1V25_AWAKE_IO — 7 9 10
PP1V25_AWAKE_IO — 49
PP1V25_AWAKE_IO — 36 42
PP1V25_AWAKE_IO — 82
PP1V25_AWAKE_IO — 85
PP1V25_AWAKE_IO — 82 83

SPMU BUCK 3 SW 4

34 PP1V8_AWAKE_SPMU_GPIO — PP1V8_AWAKE_SPMU_GPIO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

SPMU BUCK 13 SW 5

34 PP1V25_AWAKE_NAND_VCCQ — PP1V25_AWAKE_NAND_VCCQ
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V25_AWAKE_NAND_VCCQ — 71 72
PP1V25_AWAKE_NAND_VCCQ — 90

SPMU BUCK 12 SW 6/7

34 PP0V88_AWAKE_NAND_VDD — PP0V88_AWAKE_NAND_VDD
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP0V88_AWAKE_NAND_VDD — 71
PP0V88_AWAKE_NAND_VDD — 72
PP0V88_AWAKE_NAND_VDD — 90

SPMU BUCK 12 SW 7

TIED TO SW6

MPMU LDO 1

39 NC_MPMU_VLDO1 — NC_MPMU_VLDO1
MAKE_BASE=TRUE

MPMU LDO 2

39 PP1V8_AON — PP1V8_AON
MAKE_BASE=TRUE

PP1V8_AON — 39
PP1V8_AON — 43
PP1V8_AON — 81
PP1V8_AON — 48 78
PP1V8_AON — 48 85
PP1V8_AON — 86
PP1V8_AON — 46
PP1V8_AON — 26

MPMU LDO 3

39 NC_MPMU_VLDO3 — NC_MPMU_VLDO3
MAKE_BASE=TRUE

SPMU LDO 4

34 PP0V72_S2_VDD_LOW — PP0V72_S2_VDD_LOW
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP0V72_S2_VDD_LOW — 34
PP0V72_S2_VDD_LOW — 21
PP0V72_S2_VDD_LOW — 21
PP0V72_S2_VDD_LOW — 21
PP0V72_S2_VDD_LOW — 21
PP0V72_S2_VDD_LOW — 91

MPMU LDO 5

39 NC_MPMU_VLDO5 — NC_MPMU_VLDO5
MAKE_BASE=TRUE

SPMU LDO 6

34 NC_SPMU_VLDO6 — NC_SPMU_VLDO6
MAKE_BASE=TRUE

MPMU LDO 7

39 PP3V3_S2_LDO — PP3V3_S2_LDO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP3V3_S2_LDO — 39
PP3V3_S2_LDO — 61 63 64
PP3V3_S2_LDO — 28
PP3V3_S2_LDO — 66
PP3V3_S2_LDO — 65
PP3V3_S2_LDO — 65
PP3V3_S2_LDO — 66

MPMU LDO 8

39 PP1V2_AWAKE_PLL — PP1V2_AWAKE_PLL
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.5000

PP1V2_AWAKE_PLL — 39
PP1V2_AWAKE_PLL — 20
PP1V2_AWAKE_PLL — 20
PP1V2_AWAKE_PLL — 20
PP1V2_AWAKE_PLL — 20
PP1V2_AWAKE_PLL — 21
PP1V2_AWAKE_PLL — 91

MPMU LDO 9

39 PP1V8_AON_MPMU — PP1V8_AON_MPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.0990
MIN_LINE_WIDTH=0.2000

PP1V8_AON_MPMU — 39 41
PP1V8_AON_MPMU — 40 42
PP1V8_AON_MPMU — 26
PP1V8_AON_MPMU — 86

MPMU LDO 9B

39 PP1V2_AON_MPMU — PP1V2_AON_MPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.0990
MIN_LINE_WIDTH=0.0990

PP1V2_AON_MPMU — 39
PP1V2_AON_MPMU — 38

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SPMU LDO 9

34 PP1V8_AON_SPMU

PP1V8_AON_SPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V8_AON_SPMU 34

SPMU LDO 9B

34 PP1V2_AON_SPMU

PP1V2_AON_SPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V2_AON_SPMU 34
PP1V2_AON_SPMU 33

MPMU LDO 10

39 PP3V3_AON

PP3V3_AON
MAKE_BASE=TRUE

PP3V3_AON 39
PP3V3_AON 43
PP3V3_AON 85
PP3V3_AON 88

MPMU LDO 11

39 PP0V855_S2SW_CIO

PP0V855_S2SW_CIO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.5000

PP0V855_S2SW_CIO 21
PP0V855_S2SW_CIO 21
PP0V855_S2SW_CIO 39

SPMU LDO12

34 PP0V78_S1_VDD_FIXED

PP0V78_S1_VDD_FIXED
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP0V78_S1_VDD_FIXED 34
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 13
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 19
PP0V78_S1_VDD_FIXED 91

UC710 - 3V3_S2

47 PP3V3_S2

Sourced from PBus
Enabled by P3V3S2_PWR_EN

PP3V3_S2
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
MAKE_BASE=TRUE

PP3V3_S2 47
PP3V3_S2 46
PP3V3_S2 89
PP3V3_S2 48
PP3V3_S2 76
PP3V3_S2 88

UC300 - 5V S2

45 PP5V_S2

Sourced from PBus
Enabled by P5VS2_PWR_EN

PP5V_S2
MIN_LINE_WIDTH=0.0990
MIN_NECK_WIDTH=0.0990
MAKE_BASE=TRUE

PP5V_S2 89

PP5V_S2 46
PP5V_S2 32
PP5V_S2 77
PP5V_S2 76
PP5V_S2 54
PP5V_S2 48
PP5V_S2 74
PP5V_S2 63 64
PP5V_S2 63 64
PP5V_S2 26

Trackpad - 5V S2

48 PP5V_S2SW_IPD

PP5V_S2SW_IPD
MIN_LINE_WIDTH=0.0970
MIN_NECK_WIDTH=0.1000
MAKE_BASE=TRUE

PP5V_S2SW_IPD 87

MPMU LDO13

39 PP3V3_S2SW_SNS

PP3V3_S2SW_SNS
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.0970
MIN_NECK_WIDTH=0.1000

PP3V3_S2SW_SNS 39
PP3V3_S2SW_SNS 52 53 54

MPMU LDO14

39 NC_MPMU_VLDO14

NC_MPMU_VLDO14
MAKE_BASE=TRUE

SPMU LDO15

34 NC_SPMU_VLDO15

NC_SPMU_VLDO15
MAKE_BASE=TRUE

MPMU LDO16

39 NC_MPMU_VLDO16

NC_MPMU_VLDO16
MAKE_BASE=TRUE

SPMU LDO17

34 NC_SPMU_VLDO17

NC_SPMU_VLDO17
MAKE_BASE=TRUE

SPMU LDO18

34 NC_SPMU_VLDO18

NC_SPMU_VLDO18
MAKE_BASE=TRUE

48 PP3V3_S2SW_IPD

PP3V3_S2SW_IPD
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.0970
MIN_NECK_WIDTH=0.1000

PP3V3_S2SW_IPD 87 90
PP3V3_S2SW_IPD 86
PP3V3_S2SW_IPD 51

76 PP3V3_SW_LCD

PP3V3_SW_LCD
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

PP3V3_SW_LCD 75
PP3V3_SW_LCD 90
PP3V3_SW_LCD 79

76 PP5V_SW_MINNIE

PP5V_SW_MINNIE
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000

PP5V_SW_MINNIE 75

76 PP1V25_SW_MINNIE

PP1V25_SW_MINNIE
MAKE_BASE=TRUE

PP1V25_SW_MINNIE 75
PP1V25_SW_MINNIE 49

48 PP1V8_S2SW

PP1V8_S2SW
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000

PP1V8_S2SW 18
PP1V8_S2SW 91

Keyboard Backlight - 5V S2

54 PP5V_S2_KBDLED

PP5V_S2_KBDLED
MIN_LINE_WIDTH=0.0970
MIN_NECK_WIDTH=0.1000
MAKE_BASE=TRUE

PP5V_S2_KBDLED 85
PP5V_S2_KBDLED 90

48 PPBUS_AONSW_TPAD

PPBUS_AONSW_TPAD
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.0990
MIN_NECK_WIDTH=0.0990

PPBUS_AONSW_TPAD 87

Digital Ground

GND
MIN_LINE_WIDTH=0.1000
MIN_NECK_WIDTH=0.0900

MPMU LDO19

(NOT USED)

MPMU LDO20

39 PP1V2_S2_CIO

PP1V2_S2_CIO
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.5000

PP1V2_S2_CIO 39
PP1V2_S2_CIO 20
PP1V2_S2_CIO 20
PP1V2_S2_CIO 91

MPMU LDOINT

39 PP1V5_LDOINT_MPMU

PP1V5_LDOINT_MPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V5_LDOINT_MPMU 39
PP1V5_LDOINT_MPMU 37
PP1V5_LDOINT_MPMU 37
PP1V5_LDOINT_MPMU 39

SPMU LDOINT

34 PP1V5_LDOINT_SPMU

PP1V5_LDOINT_SPMU
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP1V5_LDOINT_SPMU 34
PP1V5_LDOINT_SPMU 33
PP1V5_LDOINT_SPMU 33

MPMU VDD BOOST

40 PP5V_MPMU_BSTLQ

PP5V_MPMU_BSTLQ
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP5V_MPMU_BSTLQ 38

SPMU VDD BOOST

33 PP5V_SPMU_BSTLQ

PP5V_SPMU_BSTLQ
MAKE_BASE=TRUE
MIN_NECK_WIDTH=0.1000
MIN_LINE_WIDTH=0.2000

PP5V_SPMU_BSTLQ 33

MPMU LDO RTC

SHORTED TO MPMU LDOINT FOR PORTABLES

Display Backlight Rails

77 PPVOUT_LCDBKLT

PPVOUT_LCDBKLT
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.1000

PPVOUT_LCDBKLT 75
PPVOUT_LCDBKLT 75 90

78 PPVIN_LCDBKLT

PPVIN_LCDBKLT
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.1000

PPVIN_LCDBKLT 77

98 PPVOUT_LCDBKLT_D

PPVOUT_LCDBKLT_D
MAKE_BASE=TRUE
MIN_LINE_WIDTH=0.5000
MIN_NECK_WIDTH=0.1000

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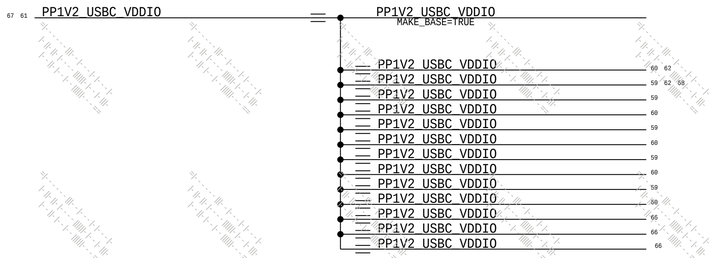
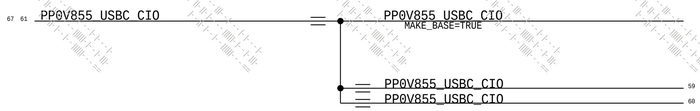
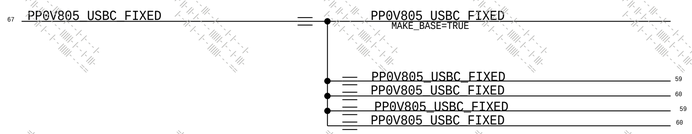
USB 1V2 VDDIO



USB 0V855 CIO



USB 0V805 Fixed



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POWER ALIASES 4

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A Lid Angle Sensor Aliases

85	AMR LEFT OR ND 1V8	MAKE_BASE=TRUE	AMR LEFT OR ND 1V8	81
			AMR LEFT OR ND 1V8	81

B Speaker Amplifier Aliases

9 IN	TDM SPKRAMP L D2R	MAKE_BASE=TRUE	TDM SPKRAMP L D2R	82
			TDM SPKRAMP L D2R	82
9 IN	TDM SPKRAMP R D2R	MAKE_BASE=TRUE	TDM SPKRAMP R D2R	83
			TDM SPKRAMP R D2R	83

C PMU Aliases

35	SWD NUB SWCLK SPMU	MAKE_BASE=TRUE	SWD NUB SWCLK SPMU	12
35	SWD NUB SWDIO SPMU	MAKE_BASE=TRUE	SWD NUB SWDIO SPMU	12
41	SWD NUB SWCLK MPMU	MAKE_BASE=TRUE	SWD NUB SWCLK MPMU	12
41	SWD NUB SWDIO MPMU	MAKE_BASE=TRUE	SWD NUB SWDIO MPMU	12
76	PMU SYS ALIVE	MAKE_BASE=TRUE	PMU SYS ALIVE	41 42 73 88

D Charger Aliases

26	P5VS2 PGOOD	MAKE_BASE=TRUE	P5VS2 PGOOD	45
25	NC CHGR CBC ON	MAKE_BASE=TRUE	NC CHGR CBC ON	
25	NC CHGR EN VR1	MAKE_BASE=TRUE	NC CHGR EN VR1	
25	NC CHGR SMC RST L	MAKE_BASE=TRUE	NC CHGR SMC RST L	

E PP5V_S2 Aliases

26	P5VS2 PWR EN	MAKE_BASE=TRUE	P5VS2 PWR EN	45 46 48
45	P5VS2 EN	MAKE_BASE=TRUE	P5VS2 EN	45

F Display Aliases

75	UART TCON D2R	MAKE_BASE=TRUE	UART TCON D2R	8
77	NC BKLT ISET KEYB	MAKE_BASE=TRUE	NC BKLT ISET KEYB	
77	NC BKLT KEYB1	MAKE_BASE=TRUE	NC BKLT KEYB1	
77	NC BKLT KEYB2	MAKE_BASE=TRUE	NC BKLT KEYB2	
77	NC KBDBKLT SW2	MAKE_BASE=TRUE	NC KBDBKLT SW2	
77	NC VOUT KEYBDLED FB2	MAKE_BASE=TRUE	NC VOUT KEYBDLED FB2	
77	UNUSED LP8548 PWM	MAKE_BASE=TRUE	UNUSED LP8548 PWM	

G Secure Element Aliases

23	NC SE GPIO0	MAKE_BASE=TRUE	NC SE GPIO0
23	NC I2C SE SCL	MAKE_BASE=TRUE	NC I2C SE SCL
23	NC I2C SE SDA	MAKE_BASE=TRUE	NC I2C SE SDA

H NAND Aliases

71	NC NAND0 S5E0 VPP	MAKE_BASE=TRUE	NC NAND0 S5E0 VPP
72	NC NAND0 S5E1 VPP	MAKE_BASE=TRUE	NC NAND0 S5E1 VPP

I Wireless Module Aliases

70 69	NC RF BT DED	MAKE_BASE=TRUE	NC RF BT DED	
	TPT WLAN JTAG TCK	MAKE_BASE=TRUE	TPT WLAN JTAG TCK	69 70
	TPT WLAN JTAG TMS	MAKE_BASE=TRUE	TPT WLAN JTAG TMS	69 70
	TPT WLAN JTAG TRSTN	MAKE_BASE=TRUE	TPT WLAN JTAG TRSTN	69
	TPT WLAN JTAG TDI	MAKE_BASE=TRUE	TPT WLAN JTAG TDI	69

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A USB-C Aliases: USB 2.0 I/F

65	USB2_ATC0_LS_P	MAKE_BASE=TRUE	USB2_ATC0_LS_P 68
65	USB2_ATC0_LS_N	MAKE_BASE=TRUE	USB2_ATC0_LS_N 68
65	USB2_ATC1_LS_P	MAKE_BASE=TRUE	USB2_ATC1_LS_P 68
65	USB2_ATC1_LS_N	MAKE_BASE=TRUE	USB2_ATC1_LS_N 68
65	USB_DBG_LS_P	MAKE_BASE=TRUE	USB_DBG_LS_P 62
65	USB_DBG_LS_N	MAKE_BASE=TRUE	USB_DBG_LS_N 62

B USB-C Aliases: CIO Debug I/F

CIO_ATC0_LSRX	MAKE_BASE=TRUE	CIO_ATC0_LSRX	6 59
CIO_ATC0_LSTX	MAKE_BASE=TRUE	CIO_ATC0_LSTX	6 59
CIO_ATC1_LSRX	MAKE_BASE=TRUE	CIO_ATC1_LSRX	6 60
CIO_ATC1_LSTX	MAKE_BASE=TRUE	CIO_ATC1_LSTX	6 60

C USB-C Aliases: EUSB I/F

65	EUSB_ATC0_P	MAKE_BASE=TRUE	EUSB_ATC0_P 6 13
65	EUSB_ATC0_N	MAKE_BASE=TRUE	EUSB_ATC0_N 6 13
65	EUSB_ATC1_P	MAKE_BASE=TRUE	EUSB_ATC1_P 6 13
65	EUSB_ATC1_N	MAKE_BASE=TRUE	EUSB_ATC1_N 6 13
13 7	EUSB_DBG_P	MAKE_BASE=TRUE	EUSB_DBG_P 65
13 7	EUSB_DBG_N	MAKE_BASE=TRUE	EUSB_DBG_N 65
65	ATCRTMR0_RESET_1V2_L	MAKE_BASE=TRUE	ATCRTMR0_RESET_1V2_L 62 66

D USB-C Aliases: I2C I/F

59 BI	I2C_UPC0_ATCRTMR0_SDA_1V2	MAKE_BASE=TRUE	I2C_UPC0_ATCRTMR0_SDA_1V2 BI 66
65 BI	I2C_UPC0_ATCRTMR0_SDA_1V2		
59 BI	I2C_UPC0_ATCRTMR0_SCL_1V2	MAKE_BASE=TRUE	I2C_UPC0_ATCRTMR0_SCL_1V2 BI 66
65 BI	I2C_UPC0_ATCRTMR0_SCL_1V2		
60 BI	I2C_UPC1_ATCRTMR1_SDA_1V2	MAKE_BASE=TRUE	I2C_UPC1_ATCRTMR1_SDA_1V2 BI 66
65 BI	I2C_UPC1_ATCRTMR1_SDA_1V2		
60 BI	I2C_UPC1_ATCRTMR1_SCL_1V2	MAKE_BASE=TRUE	I2C_UPC1_ATCRTMR1_SCL_1V2 BI 66
65 BI	I2C_UPC1_ATCRTMR1_SCL_1V2		

E USB-C Aliases: SWD I/F

59	SWD_NUB_ATCRTMR_SWCLK	MAKE_BASE=TRUE	SWD_NUB_ATCRTMR_SWCLK 13
60	SWD_NUB_ATCRTMR_SWCLK		
59	SWD_NUB_ATCRTMR_SWDIO	MAKE_BASE=TRUE	SWD_NUB_ATCRTMR_SWDIO 13
60	SWD_NUB_ATCRTMR_SWDIO		

F USB-C Aliases: CC I/F

97 62	NC_USBC0_CC_FLT_L	MAKE_BASE=TRUE	NC_USBC0_CC_FLT_L 62 97
97 62	NC_USBC1_CC_FLT_L	MAKE_BASE=TRUE	NC_USBC1_CC_FLT_L 62 97

G USB-C Aliases: GPIO

59	TP_ATCRTMR0_GPIO_0	MAKE_BASE=TRUE	TP_ATCRTMR0_GPIO_0
59	NC_ATCRTMR0_GPIO_1	MAKE_BASE=TRUE	NC_ATCRTMR0_GPIO_1
59	TP_ATCRTMR0_GPIO_2	MAKE_BASE=TRUE	TP_ATCRTMR0_GPIO_2
59	TP_ATCRTMR0_GPIO_3	MAKE_BASE=TRUE	TP_ATCRTMR0_GPIO_3
60	TP_ATCRTMR1_GPIO_0	MAKE_BASE=TRUE	TP_ATCRTMR1_GPIO_0
60	NC_ATCRTMR1_GPIO_1	MAKE_BASE=TRUE	NC_ATCRTMR1_GPIO_1
60	TP_ATCRTMR1_GPIO_2	MAKE_BASE=TRUE	TP_ATCRTMR1_GPIO_2
60	TP_ATCRTMR1_GPIO_3	MAKE_BASE=TRUE	TP_ATCRTMR1_GPIO_3

Leave these as TP, so that RT13 debug modes can be enabled.

H USB-C Aliases: VDD I/O Fuse I/F

68 59	ATCRTMR0_VDDIO_EFUSE	MAKE_BASE=TRUE	ATCRTMR0_VDDIO_EFUSE
68 60	ATCRTMR1_VDDIO_EFUSE	MAKE_BASE=TRUE	ATCRTMR1_VDDIO_EFUSE

I USB-C Aliases: SOC Dock Connect

62	SOC_DOCK_CONNECT	MAKE_BASE=TRUE	SOC_DOCK_CONNECT 7

J USB-C Aliases: UPC I2C

28	I2C_UPC01_3V3_SDA	MAKE_BASE=TRUE	I2C_UPC01_3V3_SDA 61 68
28	I2C_UPC01_3V3_SCL	MAKE_BASE=TRUE	I2C_UPC01_3V3_SCL 61 68

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A GPIO AOP ALIAS

8	NC_SOC_AOP_I2CM1_SCL	NC_SOC_AOP_I2CM1_SCL	MAKE_BASE=TRUE
8	NC_SOC_AOP_I2CM1_SDA	NC_SOC_AOP_I2CM1_SDA	MAKE_BASE=TRUE
8	NC_SOC_AOP_I2CM2_SCL	NC_SOC_AOP_I2CM2_SCL	MAKE_BASE=TRUE
8	NC_SOC_AOP_I2CM2_SDA	NC_SOC_AOP_I2CM2_SDA	MAKE_BASE=TRUE
98 8	NC_AOP_I2S0_LRCLK	NC_AOP_I2S0_LRCLK 98	MAKE_BASE=TRUE
98 8	NC_AOP_I2S0_LRCLK	NC_AOP_I2S0_LRCLK 98	MAKE_BASE=TRUE
8	NC_SOC_AOP_UART0_RXD	NC_SOC_AOP_UART0_RXD	MAKE_BASE=TRUE
8	NC_SOC_AOP_UART0_TXD	NC_SOC_AOP_UART0_TXD	MAKE_BASE=TRUE
8	NC_SOC_AOP_UART1_RXD	NC_SOC_AOP_UART1_RXD	MAKE_BASE=TRUE
8	NC_SOC_AOP_UART1_TXD	NC_SOC_AOP_UART1_TXD	MAKE_BASE=TRUE
8	NC_SOC_AOP_UART2_RXD	NC_SOC_AOP_UART2_RXD	MAKE_BASE=TRUE
8	NC_SOC_AOP_UART2_TXD	NC_SOC_AOP_UART2_TXD	MAKE_BASE=TRUE
8	NC_AOP_FUNC0	NC_AOP_FUNC0	MAKE_BASE=TRUE
8	NC_AOP_FUNC1	NC_AOP_FUNC1	MAKE_BASE=TRUE
8	NC_AOP_FUNC2	NC_AOP_FUNC2	MAKE_BASE=TRUE
8	NC_AOP_FUNC3	NC_AOP_FUNC3	MAKE_BASE=TRUE
8	NC_AOP_FUNC11	NC_AOP_FUNC11	MAKE_BASE=TRUE
8	NC_AOP_FUNC12	NC_AOP_FUNC12	MAKE_BASE=TRUE
8	NC_AOP_FUNC20	NC_AOP_FUNC20	MAKE_BASE=TRUE
8	NC_HDMI_CEC_AOP_TX	NC_HDMI_CEC_AOP_TX	MAKE_BASE=TRUE
8	NC_HDMI_CEC_AOP_RX	NC_HDMI_CEC_AOP_RX	MAKE_BASE=TRUE
8	NC_HDMI_HDP_AOP	NC_HDMI_HDP_AOP	MAKE_BASE=TRUE
7	TP_SOC_DOCK_ATTENTION	TP_SOC_DOCK_ATTENTION	MAKE_BASE=TRUE
8	NC_AOP_FUNC19	NC_AOP_FUNC19	MAKE_BASE=TRUE
9	NC_TOUCHID_BKLT_PWM	NC_TOUCHID_BKLT_PWM	MAKE_BASE=TRUE

B GPIO AP ALIAS

8	NC_BKLT_PWR_ON	NC_BKLT_PWR_ON	MAKE_BASE=TRUE
8	NC_SOC_AP_GPIO_1	NC_SOC_AP_GPIO_1	MAKE_BASE=TRUE
8	NC_CCG_I2C_INT	NC_CCG_I2C_INT	MAKE_BASE=TRUE
8	NC_DMIC_ID	NC_DMIC_ID	MAKE_BASE=TRUE
8	NC_SOC_AP_GPIO_18	NC_SOC_AP_GPIO_18	MAKE_BASE=TRUE
8	NC_SOC_AP_GPIO_19	NC_SOC_AP_GPIO_19	MAKE_BASE=TRUE
8	NC_ENET_I2C_LOM_INT_L	NC_ENET_I2C_LOM_INT_L	MAKE_BASE=TRUE
8	NC_SOC_AP_GPIO_23	NC_SOC_AP_GPIO_23	MAKE_BASE=TRUE
8	NC_SOC_AP_GPIO_24	NC_SOC_AP_GPIO_24	MAKE_BASE=TRUE
8	NC_ENET_SELECT_1G_H_10G_L	NC_ENET_SELECT_1G_H_10G_L	MAKE_BASE=TRUE
8	NC_SOC_AP_GPIO_26	NC_SOC_AP_GPIO_26	MAKE_BASE=TRUE
8	NC_SOC_AP_UART1_CTS_L	NC_SOC_AP_UART1_CTS_L	MAKE_BASE=TRUE
8	NC_SOC_AP_UART1_RTS_L	NC_SOC_AP_UART1_RTS_L	MAKE_BASE=TRUE
8	NC_SOC_AP_UART1_RXD	NC_SOC_AP_UART1_RXD	MAKE_BASE=TRUE
8	NC_SOC_AP_UART1_TXD	NC_SOC_AP_UART1_TXD	MAKE_BASE=TRUE
8	NC_SOC_AP_UART3_CTS_L	NC_SOC_AP_UART3_CTS_L	MAKE_BASE=TRUE
8	NC_SOC_AP_UART3_RTS_L	NC_SOC_AP_UART3_RTS_L	MAKE_BASE=TRUE
8	NC_SOC_AP_UART3_RXD	NC_SOC_AP_UART3_RXD	MAKE_BASE=TRUE
8	NC_SOC_AP_UART3_TXD	NC_SOC_AP_UART3_TXD	MAKE_BASE=TRUE
8	NC_SOC_AP_UART4_RXD	NC_SOC_AP_UART4_RXD	MAKE_BASE=TRUE
8	NC_SOC_AP_UART4_TXD	NC_SOC_AP_UART4_TXD	MAKE_BASE=TRUE
8	NC_UART_TCON_R2D	NC_UART_TCON_R2D	MAKE_BASE=TRUE
8	NC_UART_HDMI_D2R	NC_UART_HDMI_D2R	MAKE_BASE=TRUE
8	NC_UART_HDMI_R2D	NC_UART_HDMI_R2D	MAKE_BASE=TRUE
8	NC_SOC_AP_UART2_RXD	NC_SOC_AP_UART2_RXD	MAKE_BASE=TRUE
8	NC_SOC_AP_UART2_TXD	NC_SOC_AP_UART2_TXD	MAKE_BASE=TRUE
8	NC_SOC_AP_UART2_CTS_L	NC_SOC_AP_UART2_CTS_L	MAKE_BASE=TRUE
8	NC_SOC_AP_UART2_RTS_L	NC_SOC_AP_UART2_RTS_L	MAKE_BASE=TRUE

C DEBUG ALIAS

7	NC_AON_SLEEP1_RESET_L	NC_AON_SLEEP1_RESET_L	MAKE_BASE=TRUE
7	NC_SOC_SWD_TMS3	NC_SOC_SWD_TMS3	MAKE_BASE=TRUE
3	NC_SWD_R1_SWDIO	NC_SWD_R1_SWDIO	MAKE_BASE=TRUE

D GND ALIAS

The DUT_GND_DETECT signal is for dev only,
and should be tied to GND.

GND — GND — IN 22
MAKE_BASE=TRUE

SYNC_MASTER=jwelsb SYNC_DATE=09/28/2021

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SOC: ALIASES GPIO

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A SPI & I2S ALIAS

9	NC_TDM_SPKRAMP_TOP_BCLK_R	NC_TDM_SPKRAMP_TOP_BCLK_R (MAKE_BASE=TRUE)	
9	NC_TDM_SPKRAMP_TOP_D2R	NC_TDM_SPKRAMP_TOP_D2R (MAKE_BASE=TRUE)	
9	NC_TDM_SPKRAMP_TOP_R2D_R	NC_TDM_SPKRAMP_TOP_R2D_R (MAKE_BASE=TRUE)	
9	NC_TDM_SPKRAMP_TOP_FSYNC_R	NC_TDM_SPKRAMP_TOP_FSYNC_R (MAKE_BASE=TRUE)	
9	NC_SOC_AP_SPMI0_SCLK	NC_SOC_AP_SPMI0_SCLK (MAKE_BASE=TRUE)	
9	NC_SOC_AP_SPMI0_SDATA	NC_SOC_AP_SPMI0_SDATA (MAKE_BASE=TRUE)	
9	NC_SOC_AP_SPI5_MISO	NC_SOC_AP_SPI5_MISO (MAKE_BASE=TRUE)	
9	NC_SOC_AP_SPI5_MOSI	NC_SOC_AP_SPI5_MOSI (MAKE_BASE=TRUE)	
9	NC_SOC_AP_SPI5_SCLK	NC_SOC_AP_SPI5_SCLK (MAKE_BASE=TRUE)	
9	NC_SOC_AP_SPI5_CS_L	NC_SOC_AP_SPI5_CS_L (MAKE_BASE=TRUE)	
9	NC_SOC_SSPI0_MISO	NC_SOC_SSPI0_MISO (MAKE_BASE=TRUE)	
9	NC_SOC_SSPI0_MOSI	NC_SOC_SSPI0_MOSI (MAKE_BASE=TRUE)	
9	NC_SOC_SSPI0_SCLK	NC_SOC_SSPI0_SCLK (MAKE_BASE=TRUE)	
9	NC_SOC_SGPIO_1	NC_SOC_SGPIO_1 (MAKE_BASE=TRUE)	
9	NC_SOC_AP_SPI2_CS_L	NC_SOC_AP_SPI2_CS_L (MAKE_BASE=TRUE)	
99 9	NC_SOC_AP_I2S0_MCK	NC_SOC_AP_I2S0_MCK (MAKE_BASE=TRUE)	99
99 9	NC_SOC_AP_I2S1_MCK	NC_SOC_AP_I2S1_MCK (MAKE_BASE=TRUE)	99
99 9	NC_SOC_AP_I2S2_MCK	NC_SOC_AP_I2S2_MCK (MAKE_BASE=TRUE)	99
8	NC_PDM_DMIC_DATA4	NC_PDM_DMIC_DATA4 (MAKE_BASE=TRUE)	
8	NC_PDM_DMIC_CLK2_R	NC_PDM_DMIC_CLK2_R (MAKE_BASE=TRUE)	
8	NC_AOP_I2S0_BCLK	NC_AOP_I2S0_BCLK (MAKE_BASE=TRUE)	
8	NC_AOP_I2S0_DIN	NC_AOP_I2S0_DIN (MAKE_BASE=TRUE)	
8	NC_AOP_I2S0_DOUT	NC_AOP_I2S0_DOUT (MAKE_BASE=TRUE)	
8	NC_SOC_AOP_SPI1_CS_L	NC_SOC_AOP_SPI1_CS_L (MAKE_BASE=TRUE)	
99 8	NC_SPI_DP2HDMI_HOLD_L	NC_SPI_DP2HDMI_HOLD_L (MAKE_BASE=TRUE)	99
99 9	NC_SOC_AP_I2S0_MCK	NC_SOC_AP_I2S0_MCK (MAKE_BASE=TRUE)	99
99 9	NC_SOC_AP_I2S1_MCK	NC_SOC_AP_I2S1_MCK (MAKE_BASE=TRUE)	99
99 9	NC_SOC_AP_I2S2_MCK	NC_SOC_AP_I2S2_MCK (MAKE_BASE=TRUE)	99
99 8	NC_SPI_DP2HDMI_HOLD_L	NC_SPI_DP2HDMI_HOLD_L (MAKE_BASE=TRUE)	99
9	NC_SOC_SPI3_MOSI	NC_SOC_SPI3_MOSI (MAKE_BASE=TRUE)	
9	NC_SOC_SPI3_MISO	NC_SOC_SPI3_MISO (MAKE_BASE=TRUE)	
9	NC_SOC_SPI3_SCLK	NC_SOC_SPI3_SCLK (MAKE_BASE=TRUE)	
9	NC_SOC_SPI3_SSIN	NC_SOC_SPI3_SSIN (MAKE_BASE=TRUE)	
8	NC_SOC_GPIO16	NC_SOC_GPIO16 (MAKE_BASE=TRUE)	
8	NC_SOC_GPIO17	NC_SOC_GPIO17 (MAKE_BASE=TRUE)	

B GPIO MTP ALIAS

9	NC_SOC_MTP_I2C0_SCL	NC_SOC_MTP_I2C0_SCL (MAKE_BASE=TRUE)	
9	NC_SOC_MTP_I2C0_SDA	NC_SOC_MTP_I2C0_SDA (MAKE_BASE=TRUE)	
9	NC_SOC_MTP_FUNC_6	NC_SOC_MTP_FUNC_6 (MAKE_BASE=TRUE)	
9	NC_SOC_MTP_FUNC_7	NC_SOC_MTP_FUNC_7 (MAKE_BASE=TRUE)	
9	IPD_MTP_FUNC_1	IPD_MTP_FUNC_1 (MAKE_BASE=TRUE)	86
9	NC_SOC_MTP_FUNC_2	NC_SOC_MTP_FUNC_2 (MAKE_BASE=TRUE)	

C AUDIO I2C

9	I2C_SPKRAMP_L_SDA	I2C_SPKRAMP_L_SDA (MAKE_BASE=TRUE)	49
9	I2C_SPKRAMP_L_SCL	I2C_SPKRAMP_L_SCL (MAKE_BASE=TRUE)	49
9	I2C_SPKRAMP_R_CODEC_SDA	I2C_SPKRAMP_R_CODEC_SDA (MAKE_BASE=TRUE)	49
9	I2C_SPKRAMP_R_CODEC_SCL	I2C_SPKRAMP_R_CODEC_SCL (MAKE_BASE=TRUE)	49

SYNC_MASTER= SYNC_DATE=09/10/2021

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(A) LPDP ALIAS

NC_SOC_LPDP_RX_AUX_D1	=	NC_SOC_LPDP_RX_AUX_D1 MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D2	=	NC_SOC_LPDP_RX_AUX_D2 MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D3	=	NC_SOC_LPDP_RX_AUX_D3 MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D4	=	NC_SOC_LPDP_RX_AUX_D4 MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D5	=	NC_SOC_LPDP_RX_AUX_D5 MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D6	=	NC_SOC_LPDP_RX_AUX_D6 MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D7	=	NC_SOC_LPDP_RX_AUX_D7 MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D8	=	NC_SOC_LPDP_RX_AUX_D8 MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D9	=	NC_SOC_LPDP_RX_AUX_D9 MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D10	=	NC_SOC_LPDP_RX_AUX_D10 MAKE_BASE=TRUE
NC_SOC_LPDP_RX_AUX_D11	=	NC_SOC_LPDP_RX_AUX_D11 MAKE_BASE=TRUE
NC_SOC_ST_PCIE_PERST_1_L	=	NC_SOC_ST_PCIE_PERST_1_L MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D1P	=	NC_SOC_LPDP_RX_D1P MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D1N	=	NC_SOC_LPDP_RX_D1N MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D2P	=	NC_SOC_LPDP_RX_D2P MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D2N	=	NC_SOC_LPDP_RX_D2N MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D3P	=	NC_SOC_LPDP_RX_D3P MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D3N	=	NC_SOC_LPDP_RX_D3N MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D4P	=	NC_SOC_LPDP_RX_D4P MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D4N	=	NC_SOC_LPDP_RX_D4N MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D5P	=	NC_SOC_LPDP_RX_D5P MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D5N	=	NC_SOC_LPDP_RX_D5N MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D6P	=	NC_SOC_LPDP_RX_D6P MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D6N	=	NC_SOC_LPDP_RX_D6N MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D7P	=	NC_SOC_LPDP_RX_D7P MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D7N	=	NC_SOC_LPDP_RX_D7N MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D8P	=	NC_SOC_LPDP_RX_D8P MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D8N	=	NC_SOC_LPDP_RX_D8N MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D9P	=	NC_SOC_LPDP_RX_D9P MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D9N	=	NC_SOC_LPDP_RX_D9N MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D10P	=	NC_SOC_LPDP_RX_D10P MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D10N	=	NC_SOC_LPDP_RX_D10N MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D11P	=	NC_SOC_LPDP_RX_D11P MAKE_BASE=TRUE
NC_SOC_LPDP_RX_D11N	=	NC_SOC_LPDP_RX_D11N MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CP<0>	=	NC_LPDP_EXT_DATA_CP<0> MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CN<0>	=	NC_LPDP_EXT_DATA_CN<0> MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CP<1>	=	NC_LPDP_EXT_DATA_CP<1> MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CN<1>	=	NC_LPDP_EXT_DATA_CN<1> MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CP<2>	=	NC_LPDP_EXT_DATA_CP<2> MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CN<2>	=	NC_LPDP_EXT_DATA_CN<2> MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CP<3>	=	NC_LPDP_EXT_DATA_CP<3> MAKE_BASE=TRUE
NC_LPDP_EXT_DATA_CN<3>	=	NC_LPDP_EXT_DATA_CN<3> MAKE_BASE=TRUE
NC_LPDP_EXT_AUX_CP	=	NC_LPDP_EXT_AUX_CP MAKE_BASE=TRUE
NC_LPDP_EXT_AUX_CN	=	NC_LPDP_EXT_AUX_CN MAKE_BASE=TRUE
NC_LPDP_EXT_HPD	=	NC_LPDP_EXT_HPD MAKE_BASE=TRUE
NC_SOC_LPDP_RX1_RCAL_POS	=	NC_SOC_LPDP_RX1_RCAL_POS MAKE_BASE=TRUE
NC_SOC_LPDP_RX1_RCAL_NEG	=	NC_SOC_LPDP_RX1_RCAL_NEG MAKE_BASE=TRUE

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SOC: ALIASES LPDP RX

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A PCIe ALIAS

10	NC_SOC_GP_PCIE_RX1P	NC_SOC_GP_PCIE_RX1P	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_RX1N	NC_SOC_GP_PCIE_RX1N	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_TX1P	NC_SOC_GP_PCIE_TX1P	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_TX1N	NC_SOC_GP_PCIE_TX1N	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLK1_100MP	NC_SOC_GP_PCIE_CLK1_100MP	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLK1_100MN	NC_SOC_GP_PCIE_CLK1_100MN	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLKREQ_1_L	NC_SOC_GP_PCIE_CLKREQ_1_L	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_PERST_1_L	NC_SOC_GP_PCIE_PERST_1_L	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_RX2P	NC_SOC_GP_PCIE_RX2P	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_RX2N	NC_SOC_GP_PCIE_RX2N	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_TX2P	NC_SOC_GP_PCIE_TX2P	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_TX2N	NC_SOC_GP_PCIE_TX2N	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLK2_100MP	NC_SOC_GP_PCIE_CLK2_100MP	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLK2_100MN	NC_SOC_GP_PCIE_CLK2_100MN	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLKREQ_2_L	NC_SOC_GP_PCIE_CLKREQ_2_L	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_PERST_2_L	NC_SOC_GP_PCIE_PERST_2_L	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_RX3P	NC_SOC_GP_PCIE_RX3P	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_RX3N	NC_SOC_GP_PCIE_RX3N	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_TX3P	NC_SOC_GP_PCIE_TX3P	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_TX3N	NC_SOC_GP_PCIE_TX3N	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLK3_100MP	NC_SOC_GP_PCIE_CLK3_100MP	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLK3_100MN	NC_SOC_GP_PCIE_CLK3_100MN	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_CLKREQ_3_L	NC_SOC_GP_PCIE_CLKREQ_3_L	MAKE_BASE=TRUE
10	NC_SOC_GP_PCIE_PERST_3_L	NC_SOC_GP_PCIE_PERST_3_L	MAKE_BASE=TRUE

B DISP ALIAS

9	NC_I2C_SD_DISP_BKLT_SCL	NC_I2C_SD_DISP_BKLT_SCL	MAKE_BASE=TRUE
9	NC_I2C_SD_DISP_BKLT_SDA	NC_I2C_SD_DISP_BKLT_SDA	MAKE_BASE=TRUE
10	I2C_DISP_BKLT_SCL	I2C_DISP_BKLT_SCL 49	MAKE_BASE=TRUE
10	I2C_DISP_BKLT_SDA	I2C_DISP_BKLT_SDA 49	MAKE_BASE=TRUE
10	NC_SPI_DISP_BKLT_CLK_R	NC_SPI_DISP_BKLT_CLK_R	MAKE_BASE=TRUE
10	NC_SPI_DISP_BKLT_CS_L	NC_SPI_DISP_BKLT_CS_L	MAKE_BASE=TRUE
10	NC_SPMI_DISP_BKLT_CLK	NC_SPMI_DISP_BKLT_CLK	MAKE_BASE=TRUE
10	NC_SPMI_DISP_BKLT_DATA	NC_SPMI_DISP_BKLT_DATA	MAKE_BASE=TRUE
10	NC_SOC_DISP_POL	NC_SOC_DISP_POL	MAKE_BASE=TRUE
10	NC_DISP_BKLT_FSYNC	NC_DISP_BKLT_FSYNC	MAKE_BASE=TRUE
75	DISP_BKLT_LSYNC	DISP_BKLT_LSYNC 10	MAKE_BASE=TRUE
10	NC_SOC_DISP_TOUCH_BSYNC_0	NC_SOC_DISP_TOUCH_BSYNC_0	MAKE_BASE=TRUE
10	NC_SOC_DISP_TOUCH_BSYNC_1	NC_SOC_DISP_TOUCH_BSYNC_1	MAKE_BASE=TRUE
10	NC_SOC_DISP_TOUCH_EB	NC_SOC_DISP_TOUCH_EB	MAKE_BASE=TRUE
10	NC_BKLT_BOOST_THROTTLE_L	NC_BKLT_BOOST_THROTTLE_L	MAKE_BASE=TRUE
10	NC_SOC_DFR_DISP_TE	NC_SOC_DFR_DISP_TE	MAKE_BASE=TRUE
77	NC_LCDBKLT_FET_DRV	NC_LCDBKLT_FET_DRV	MAKE_BASE=TRUE

D LPDP Aliases

10	NC_SOC_LPDP_DP2HDMI_RCAL_POS	NC_SOC_LPDP_DP2HDMI_RCAL_POS	MAKE_BASE=TRUE
10	NC_SOC_LPDP_DP2HDMI_RCAL_NEG	NC_SOC_LPDP_DP2HDMI_RCAL_NEG	MAKE_BASE=TRUE

C Keyboard Backlight

9	SOC_KBD_BKLT_PWM	SOC_KBD_BKLT_PWM	MAKE_BASE=TRUE
85	SOC_KBD_BKLT_PWM		

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SOC: ALIASES PCIE, LPDP TX

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A SMC & NUB ALIAS

8	NC_SOC_SMC_GPIO_1	NC_SOC_SMC_GPIO_1	MAKE_BASE=TRUE
8	NC_SMC_FAN_0_PWM	NC_SMC_FAN_0_PWM	MAKE_BASE=TRUE
8	NC_SMC_FAN_0_TACH	NC_SMC_FAN_0_TACH	MAKE_BASE=TRUE
8	NC_SMC_FAN_1_PWM	NC_SMC_FAN_1_PWM	MAKE_BASE=TRUE
8	NC_SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE
8	NC_SOC_NUB_CLK_OUT_0	NC_SOC_NUB_CLK_OUT_0	MAKE_BASE=TRUE
8	NC_SOC_NUB_GPIO_12	NC_SOC_NUB_GPIO_12	MAKE_BASE=TRUE
8	NC_ENET_LOW_PWR	NC_ENET_LOW_PWR	MAKE_BASE=TRUE
8	NC_LOM_PMU_RESET_EN	NC_LOM_PMU_RESET_EN	MAKE_BASE=TRUE

B SENSE ALIAS

14	VSNS_VDD_PCPU	VSNS_VDD_PCPU	MAKE_BASE=TRUE	55
14	VSNS_VSS_PCPU	VSNS_VSS_PCPU	MAKE_BASE=TRUE	55
14	VSNS_ABSMIN_PCPU	VSNS_ABSMIN_PCPU	MAKE_BASE=TRUE	55
15	VSNS_VDD_ECPU	VSNS_VDD_ECPU	MAKE_BASE=TRUE	55
17	VSNS_VDD_GPU	VSNS_VDD_GPU	MAKE_BASE=TRUE	55
15	VSNS_VDD_SOC	VSNS_VDD_SOC	MAKE_BASE=TRUE	55
17	VSNS_VDD_DISP	VSNS_VDD_DISP	MAKE_BASE=TRUE	55
18	VSNS_VDD2H_1	VSNS_VDD2H_1	MAKE_BASE=TRUE	55
18	VSNS_VSS_1	VSNS_VSS_1	MAKE_BASE=TRUE	55
18	VSNS_VDD2H_2	VSNS_VDD2H_2	MAKE_BASE=TRUE	55
18	VSNS_VSS_2	VSNS_VSS_2	MAKE_BASE=TRUE	55
18	VSNS_VDDQ_S1	VSNS_VDDQ_S1	MAKE_BASE=TRUE	55

C ISP ALIAS

6	NC_SOC_ISP_GPIO_1	NC_SOC_ISP_GPIO_1	MAKE_BASE=TRUE
6	NC_SOC_ISP_GPIO_2	NC_SOC_ISP_GPIO_2	MAKE_BASE=TRUE
6	NC_SOC_ISP_GPIO_3	NC_SOC_ISP_GPIO_3	MAKE_BASE=TRUE
6	NC_SOC_ISP_SPMI0_SCLK	NC_SOC_ISP_SPMI0_SCLK	MAKE_BASE=TRUE
6	NC_SOC_ISP_SPMI0_SDATA	NC_SOC_ISP_SPMI0_SDATA	MAKE_BASE=TRUE
6	NC_SOC_ISP_SPMI1_SCLK	NC_SOC_ISP_SPMI1_SCLK	MAKE_BASE=TRUE
6	NC_SOC_ISP_SPMI1_SDATA	NC_SOC_ISP_SPMI1_SDATA	MAKE_BASE=TRUE
6	NC_SOC_ISP_I2C1_SCL	NC_SOC_ISP_I2C1_SCL	MAKE_BASE=TRUE
6	NC_SOC_ISP_I2C1_SDA	NC_SOC_ISP_I2C1_SDA	MAKE_BASE=TRUE
6	NC_SOC_SENSOR0_CLK	NC_SOC_SENSOR0_CLK	MAKE_BASE=TRUE
6	NC_SOC_SENSOR1_CLK	NC_SOC_SENSOR1_CLK	MAKE_BASE=TRUE
6	NC_SOC_SENSOR2_CLK	NC_SOC_SENSOR2_CLK	MAKE_BASE=TRUE
6	NC_SOC_SENSOR3_CLK	NC_SOC_SENSOR3_CLK	MAKE_BASE=TRUE

D MIPI Aliases

6	NC_SOC_MIPI0C_DPCLK	NC_SOC_MIPI0C_DPCLK	MAKE_BASE=TRUE
6	NC_SOC_MIPI0C_DNCLK	NC_SOC_MIPI0C_DNCLK	MAKE_BASE=TRUE
6	NC_SOC_MIPI0C_DPDATA<0>	NC_SOC_MIPI0C_DPDATA<0>	MAKE_BASE=TRUE
6	NC_SOC_MIPI0C_DNDATA<0>	NC_SOC_MIPI0C_DNDATA<0>	MAKE_BASE=TRUE
6	NC_SOC_MIPI0C_DPDATA<1>	NC_SOC_MIPI0C_DPDATA<1>	MAKE_BASE=TRUE
6	NC_SOC_MIPI0C_DNDATA<1>	NC_SOC_MIPI0C_DNDATA<1>	MAKE_BASE=TRUE
6	NC_SOC_MIPI1C_DPCLK	NC_SOC_MIPI1C_DPCLK	MAKE_BASE=TRUE
6	NC_SOC_MIPI1C_DNCLK	NC_SOC_MIPI1C_DNCLK	MAKE_BASE=TRUE
6	NC_SOC_MIPI1C_DPDATA<0>	NC_SOC_MIPI1C_DPDATA<0>	MAKE_BASE=TRUE
6	NC_SOC_MIPI1C_DNDATA<0>	NC_SOC_MIPI1C_DNDATA<0>	MAKE_BASE=TRUE
6	NC_SOC_MIPI1C_DPDATA<1>	NC_SOC_MIPI1C_DPDATA<1>	MAKE_BASE=TRUE
6	NC_SOC_MIPI1C_DNDATA<1>	NC_SOC_MIPI1C_DNDATA<1>	MAKE_BASE=TRUE
6	NC_SOC_MIPID_DPCLK	NC_SOC_MIPID_DPCLK	MAKE_BASE=TRUE
6	NC_SOC_MIPID_DNCLK	NC_SOC_MIPID_DNCLK	MAKE_BASE=TRUE
6	NC_SOC_MIPID_DPDATA<0>	NC_SOC_MIPID_DPDATA<0>	MAKE_BASE=TRUE
6	NC_SOC_MIPID_DNDATA<0>	NC_SOC_MIPID_DNDATA<0>	MAKE_BASE=TRUE
6	NC_SOC_MIPI0C_REXT	NC_SOC_MIPI0C_REXT	MAKE_BASE=TRUE
6	NC_SOC_MIPI1C_REXT	NC_SOC_MIPI1C_REXT	MAKE_BASE=TRUE
6	NC_SOC_MIPID_REXT	NC_SOC_MIPID_REXT	MAKE_BASE=TRUE

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SOC: ALIASES CAMERA, USB, MISC

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SCSET RULES

DIELECTRIC BASED SPACING RULES	
RULE DEFINITION	LIST OF VALUES
A_DIELECTRIC_(N)X Calculates dielectric distance from stackup, shorted distance is used unless L is defined	EXAMPLE: 2,3,5,7,9,10,12,14,16 2-10
A_DIELECTRIC_(N)XD:XV,XVL,X Calculates dielectric distance from Hybrid Table and stackup, shorted distance is used unless L defined	EXAMPLE: 2,3D,3D:5V,5VL,7 PLEASE USE HYBRID TABLE
A_DIELECTRIC_(N)XIN_(N)XOUT Calculates dielectric distance from stackup, shorted distance is used unless L is defined	EXAMPLE: 2_5,3L_3L

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17.4 RULES

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PHYSICAL CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR WARNING
CLASS NAME	DDR ***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
I2C	P	A_45_OHM_SE	*SMB*SCL*,*SMB*SDA*,*I2C*SCL*,*I2C*SDA*,*I2C*INT*	Y
SPI	P	A_45_OHM_SE	*SPI*MISO*,*SPI*MOSI*,*SPI*CLK*,*SPI*CS*	Y
SPMI	P	A_45_OHM_SE	*SPMI*	Y
SWD	P	A_45_OHM_SE	SWD_NAND*,SWD_NUB*	Y
JTAG	P	A_45_OHM_SE	*JTAG*SEL,*JTAG*TCK,*JTAG*TDI,*JTAG*TDO,*JTAG*TMS	Y
CLOCK_24M	P	A_45_OHM_SE	SOC_XTAL24M*,SOC_24M_O_R,NAND0_CLK24M*	Y
CLOCK_32K	P	A_45_OHM_SE	PMU_CLK32K*	Y
TDM_LEFT	P	A_45_OHM_SE	TDM_SPKRAMP_L*	Y
TDM_RIGHT	P	A_45_OHM_SE	TDM_SPKRAMP_R*	Y
TDM_CODEC	P	A_45_OHM_SE	TDM_CODEC*	Y
SPKR_ICC	P	A_45_OHM_SE	SPKRAMP_ICC,SPKRAMP_*_ICC_R	Y
UART	P	A_45_OHM_SE	UART_*	Y
RESETS	P	A_45_OHM_SE	*RST*,*RESET*,*PERST*	Y
WDOG	P	A_45_OHM_SE	SOC_WDOG	Y
SOCHOT	P	A_45_OHM_SE	SOC_SOCHOT_L	Y
POWER_BUTTON	P	A_45_OHM_SE	*PMU_ONOFF*	Y
FAULT	P	A_45_OHM_SE	*FAULT*	Y
DMIC_PDM	P	A_45_OHM_SE	PDM_DMIC_DATA*,DMIC_DATA*,PDM_DMIC_CLK*,DMIC_CLK*	Y
CIO_D2R	P	A_85_OHM_DIFF	DP:DP_USBC*_D2R*	Y
CIO_R2D	P	A_85_OHM_DIFF	DP:DP_USBC*_R2D*	Y
PCIE_NAND_D2R	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND*_D2R*	Y
PCIE_NAND_R2D	P	A_85_OHM_DIFF	DP:DP_PCIE_NAND*_R2D*	Y
PCIE_WLBT_D2R	P	A_85_OHM_DIFF	DP:DP_PCIE_WLBT*_R2D*	Y
PCIE_WLBT_R2D	P	A_85_OHM_DIFF	DP:DP_PCIE_WLBT*_D2R*	Y
LPDP	P	A_85_OHM_DIFF	DP:DP_LPDP_INT_DATA*	Y
LPDP_FTCAM	P	A_85_OHM_DIFF	DP:DP_LPDP_FTCAM_DATA*	Y
PCIE_CLK	P	A_85_OHM_DIFF	DP:DP_PCIE_CLK100M*	Y
PCIE_CLKREQ	P	A_45_OHM_SE	*CLKREQ*	Y
EUSB	P	A_85_OHM_DIFF	DP:DP_EUSB*	Y
GROUND	P	DEFAULT	GND	Y
POWER	P	POWER	PP*,PN*	Y

PHYSICAL CONSTRAINT SET, NET ASSIGNMENT

DOMAIN (P,P,D)	NET RULE ASSIGNMENT	
	CONSTRAINT SET	COMMA SEPARATED NET NAMES (WILDCARD SUPPORT EX: DDR*)

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17.4 PHYSICAL CSETS

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SPACING CONSTRAINT SET, CLASS ASSIGNMENT

CLASS DEFINITIONS			COMMA SEPARATED WITH WILDCARD SUPPORT: NET NAMES EX: DDR*	CLEAR WARNING
CLASS NAME	***** ***	CONSTRAINT SET	DP NAMES EX: DP:DP_AA*,DP_BB* (LINE STARTS WITH FLAG DP:)	Y/N
CLOCK_24M	S	A_DIELECTRIC_3X	=	Y
CLOCK_32K	S	A_DIELECTRIC_3X	=	Y
CIO_D2R	S	A_DIELECTRIC_9X	=	Y
CIO_R2D	S	A_DIELECTRIC_9X	=	Y
PCIE_NAND_D2R	S	A_DIELECTRIC_9X	=	Y
PCIE_NAND_R2D	S	A_DIELECTRIC_9X	=	Y
PCIE_WLBT_D2R	S	A_DIELECTRIC_7X	=	Y
PCIE_WLBT_R2D	S	A_DIELECTRIC_7X	=	Y
PCIE_CLK	S	A_DIELECTRIC_6X	=	Y
LPDP	S	A_DIELECTRIC_6X	=	Y
LPDP_FTCAM	S	A_DIELECTRIC_5X	=	Y
EUSB	S	A_DIELECTRIC_5X	=	Y
GROUND	S	DEFAULT	=	Y
POWER	S	DEFAULT	=	Y

RF	S	RF	RF_ANT*	Y

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17.4 SPACING CSETS, ISO

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SPACING CONSTRAINT SET ASSIGNMENT, CLASS-CLASS

CLASS TO CLASS SPACING		
CLASS NAME	CLASS NAME	CONSTRAINT SET
CIO_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
CIO_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
LPDP	GROUND	DEFAULT_WITH_4X_TO_SHAPE
LPDP_FTCAM	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_CLK	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_D2R	GROUND	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_R2D	GROUND	DEFAULT_WITH_4X_TO_SHAPE
CIO_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
CIO_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
LPDP	POWER	DEFAULT_WITH_4X_TO_SHAPE
LPDP_FTCAM	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_CLK	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_NAND_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_D2R	POWER	DEFAULT_WITH_4X_TO_SHAPE
PCIE_WLBT_R2D	POWER	DEFAULT_WITH_4X_TO_SHAPE
CIO_D2R	CIO_D2R	A_DIELECTRIC_4X
CIO_D2R	PCIE_NAND_D2R	A_DIELECTRIC_4X
CIO_D2R	PCIE_WLBT_D2R	A_DIELECTRIC_4X
CIO_D2R	LPDP_FTCAM	A_DIELECTRIC_4X
CIO_D2R	CIO_R2D	A_DIELECTRIC_7X
PCIE_NAND_D2R	PCIE_NAND_D2R	A_DIELECTRIC_4X
PCIE_NAND_D2R	PCIE_WLBT_D2R	A_DIELECTRIC_4X
PCIE_NAND_D2R	LPDP_FTCAM	A_DIELECTRIC_4X
PCIE_NAND_D2R	PCIE_NAND_R2D	A_DIELECTRIC_7X
PCIE_WLBT_D2R	PCIE_WLBT_R2D	A_DIELECTRIC_4X
PCIE_WLBT_D2R	LPDP_FTCAM	A_DIELECTRIC_4X
CIO_R2D	CIO_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_NAND_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_WLBT_R2D	A_DIELECTRIC_4X
CIO_R2D	PCIE_CLK	A_DIELECTRIC_4X
CIO_R2D	LPDP	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_NAND_R2D	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_WLBT_R2D	A_DIELECTRIC_4X
PCIE_NAND_R2D	PCIE_CLK	A_DIELECTRIC_4X
PCIE_NAND_R2D	LPDP	A_DIELECTRIC_4X
PCIE_WLBT_R2D	PCIE_CLK	A_DIELECTRIC_4X
PCIE_WLBT_R2D	LPDP	A_DIELECTRIC_4X
PCIE_CLK	PCIE_CLK	A_DIELECTRIC_4X
PCIE_CLK	LPDP	A_DIELECTRIC_4X
LPDP	LPDP	A_DIELECTRIC_3X
LPDP_FTCAM	LPDP_FTCAM	A_DIELECTRIC_3X

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SOC

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
939-11077	1	PCBA,CORBETT,X2203	U0600	CRITICAL	CPU:INTERPOSER
998-23363	1	IC,DEV,STA,BGA	U0600	CRITICAL	CPU:DEV

B0 BEST

998-26981	1	SOC,STA B0+8G,1Y,10FSTP,LP,BX,H,M2565			U0600	CRITICAL	CPU:SOC_8GB_BEST
	998-26978	998-26981	ALT_CMN	ALL	Micron ATK/SCK/ASE		
998-26982	1	SOC,STA B0+16G,1Y,10FSTP,LP,BX,H,M2565			U0600	CRITICAL	CPU: SOC_16GB_BEST
	998-26979	998-26982	ALT_CMN	ALL	Micron ATK/SCK/ASE		
998-26984	1	SOC,STA B0+24G,1Z,10FSTP,LP,BX,H,M2565			U0600	CRITICAL	CPU: SOC_24GB_BEST
	998-26980	998-26984	ALT_CMN	ALL	Micron ATK/SCK/ASE		

B0 GOOD

998-26988	1	SOC,STA B0+8G,1Y,9FSTP,AP,BX,H,M2565			U0600	CRITICAL	CPU: SOC_8GB_GOOD
	998-26985	998-26988	ALT_CMN	ALL	Micron ATK/SCK/ASE		
	998-26981	998-26988	ALT_CMN	ALL	Hynix ATK/SCK/ASE - BEST		
	998-26978	998-26988	ALT_CMN	ALL	Micron ATK/SCK/ASE - BEST		
998-26989	1	SOC,STA B0+16G,1Y,9FSTP,AP,BX,H,M2565			U0600	CRITICAL	CPU:SOC_16GB_GOOD
	998-26986	998-26989	ALT_CMN	ALL	Micron ATK/SCK/ASE		
	998-26982	998-26989	ALT_CMN	ALL	Hynix ATK/SCK/ASE - BEST		
	998-26979	998-26989	ALT_CMN	ALL	Micron ATK/SCK/ASE - BEST		
998-26990	1	SOC,STA B0+24G,1Z,9FSTP,AP,BX,H,M2565			U0600	CRITICAL	CPU:SOC_24GB_GOOD
	998-26987	998-26990	ALT_CMN	ALL	Micron ATK/SCK/ASE		

A1 BEST

998-25075	1	SOC,STA A0+8G,1Y,10C,DEV,BX,H,ATK,M2565			U0600	CRITICAL	CPU:SOC_8GB_BEST_A1
	998-25074	998-25075	ALT_CMN	ALL	Hynix SCK		
	998-25076	998-25075	ALT_CMN	ALL	Hynix ASE		
	998-25077	998-25075	ALT_CMN	ALL	Micron SCK		
	998-25078	998-25075	ALT_CMN	ALL	Micron ATK		
	998-25079	998-25075	ALT_CMN	ALL	Micron ASE		
998-25081	1	SOC,STA A0+16G,1Y,10C,DEV,BX,H,ATK,M2565			U0600	CRITICAL	CPU: SOC_16GB_BEST_A1
	998-25080	998-25081	ALT_CMN	ALL	Hynix SCK		
	998-25082	998-25081	ALT_CMN	ALL	Hynix ASE		
	998-25083	998-25081	ALT_CMN	ALL	Micron SCK		
	998-25084	998-25081	ALT_CMN	ALL	Micron ATK		
	998-25085	998-25081	ALT_CMN	ALL	Micron ASE		

A1 GOOD

998-25087	1	SOC,STA A0+8G,1Y,9C,DEV,BX,H,ATK,M2565			U0600	CRITICAL	CPU: SOC_8GB_GOOD_A1
	998-25086	998-25087	ALT_CMN	ALL	Hynix SCK		
	998-25088	998-25087	ALT_CMN	ALL	Hynix ASE		
	998-25089	998-25087	ALT_CMN	ALL	Micron SCK		
	998-25090	998-25087	ALT_CMN	ALL	Micron ATK		
	998-25091	998-25087	ALT_CMN	ALL	Micron ASE		
	998-25075	998-25087	ALT_CMN	ALL	Hynix ATK - BEST		
	998-25074	998-25087	ALT_CMN	ALL	Hynix SCK - BEST		
	998-25076	998-25087	ALT_CMN	ALL	Hynix ASE - BEST		
	998-25077	998-25087	ALT_CMN	ALL	Micron SCK - BEST		
	998-25078	998-25087	ALT_CMN	ALL	Micron ATK - BEST		
	998-25079	998-25087	ALT_CMN	ALL	Micron ASE - BEST		
998-25093	1	SOC,STA A0+16G,1Y,9C,DEV,BX,H,ATK,M2565			U0600	CRITICAL	CPU:SOC_16GB_GOOD_A1
	998-25092	998-25093	ALT_CMN	ALL	Hynix SCK		
	998-25094	998-25093	ALT_CMN	ALL	Hynix ASE		
	998-25095	998-25093	ALT_CMN	ALL	Micron SCK		
	998-25096	998-25093	ALT_CMN	ALL	Micron ATK		
	998-25097	998-25093	ALT_CMN	ALL	Micron ASE		
	998-25081	998-25093	ALT_CMN	ALL	Hynix ATK - BEST		
	998-25080	998-25093	ALT_CMN	ALL	Hynix SCK - BEST		
	998-25082	998-25093	ALT_CMN	ALL	Hynix ASE - BEST		
	998-25083	998-25093	ALT_CMN	ALL	Micron SCK - BEST		
	998-25084	998-25093	ALT_CMN	ALL	Micron ATK - BEST		
	998-25085	998-25093	ALT_CMN	ALL	Micron ASE - BEST		

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NAND BOM GROUPS

BOM GROUP	BOM OPTIONS
NANDCFG:ITLC_S5E_128G_TO	NAND_L0:ITLC_128G_TO
NANDCFG:ITLC_S5E_128G_SD	NAND_L0:ITLC_128G_SD
NANDCFG:ITLC_S5E_256G_HY	NAND_L0:ITLC_256G_HY
NANDCFG:ITLC_S5E_256G_SD	NAND_L0:ITLC_256G_SD
NANDCFG:ITLC_S5E_256G_TO	NAND_L0:ITLC_256G_TO
NANDCFG:ITLC_S5E_512G_SD	NAND_L0:ITLC_512G_SD,NAND_L1:ITLC_512G_SD,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_512G_TO	NAND_L0:ITLC_512G_TO,NAND_L1:ITLC_512G_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_512G_HY	NAND_L0:ITLC_512G_HY,NAND_L1:ITLC_512G_HY,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_1P0T_HY	NAND_L0:ITLC_1P0T_HY,NAND_L1:ITLC_1P0T_HY,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_1P0T_TO	NAND_L0:ITLC_1P0T_TO,NAND_L1:ITLC_1P0T_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_2P0T_TO	NAND_L0:ITLC_2P0T_TO,NAND_L1:ITLC_2P0T_TO,PARTS_SSDNAND1
NANDCFG:ITLC_S5E_2P0T_HY	NAND_L0:ITLC_2P0T_HY,NAND_L1:ITLC_2P0T_HY,PARTS_SSDNAND1
NANDCFG:INTERPOSER	NAND_L0:INTERPOSER,NAND_L1:INTERPOSER,PARTS_SSDNAND1
NANDCFG:NONE	NAND_L0:OFF,NAND_L1:OFF,PARTS_SSDNAND1

NAND Landing 0

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-18368	1	IC,NAND,S5E MCP ROUTING STUDY,LGA110	UN000	CRITICAL	NAND_L0:S5E_STUDY
335S00462	1	NAND,3DV4,128GBT,XXX,S5E,256G,T,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_128G_TO
335S00470	1	NAND,3DV4,128GBT,XXX,S5E,256G,SD,SLGA110	UN000	CRITICAL	NAND_L0:ITLC_128G_SD
335S00504	1	NAND,3DV6T,256GB,S5E,XX.X,512G,H,LGA110	UN000	CRITICAL	NAND_L0:ITLC_256G_HY
335S00531	1	NAND,BICS5T,256GB,S5E,XX.X,512G,W,LGA110	UN000	CRITICAL	NAND_L0:ITLC_256G_SD
335S00517	1	NAND,BICS5T,256GB,S5E,XX.X,512G,K,LGA110	UN000	CRITICAL	NAND_L0:ITLC_256G_TO
335S00532	1	NAND,BICS5T,320GB,S5E,XX.X,512G,W,LGA110	UN000	CRITICAL	NAND_L0:ITLC_512G_SD
335S00518	1	NAND,BICS5T,320GB,S5E,XX.X,512G,K,LGA110	UN000	CRITICAL	NAND_L0:ITLC_512G_TO
335S00504	1	NAND,3D6T,256GB,S5E,XX.X,512G,H,LGA110	UN000	CRITICAL	NAND_L0:ITLC_512G_HY
335S00506	1	NAND,3DV6T,512GB,S5E,XX.X,512G,H,LGA110	UN000	CRITICAL	NAND_L0:ITLC_1P0T_HY
335S00519	1	NAND,BICS5T,512GB,S5E,XX.X,512G,K,LGA110	UN000	CRITICAL	NAND_L0:ITLC_1P0T_TO
335S00521	1	NAND,BICS5T,1TB,S5E,XX.X,512G,K,LGA110	UN000	CRITICAL	NAND_L0:ITLC_2P0T_TO
335S00508	1	NAND,3DV6T,1TB,S5E,XX.X,512G,H,LGA110	UN000	CRITICAL	NAND_L0:ITLC_2P0T_HY
939-08815	1	PCBA,BANDIPUR,X1711	UN000	CRITICAL	NAND_L0:INTERPOSER

NAND Landing 1

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-18368	1	IC,NAND,S5E MCP ROUTING STUDY,LGA110	UN100	CRITICAL	NAND_L1:S5E_STUDY
335S00531	1	NAND,BICS5T,256GB,S5E,XX.X,512G,W,LGA110	UN100	CRITICAL	NAND_L1:ITLC_512G_SD
335S00517	1	NAND,BICS5T,256GB,S5E,XX.X,512G,K,LGA110	UN100	CRITICAL	NAND_L1:ITLC_512G_TO
335S00504	1	NAND,3D6T,256GB,S5E,XX.X,512G,H,LGA110	UN100	CRITICAL	NAND_L1:ITLC_512G_HY
335S00506	1	NAND,3DV6T,512GB,S5E,XX.X,512G,H,LGA110	UN100	CRITICAL	NAND_L1:ITLC_1P0T_HY
335S00519	1	NAND,BICS5T,512GB,S5E,XX.X,512G,K,LGA110	UN100	CRITICAL	NAND_L1:ITLC_1P0T_TO
335S00521	1	NAND,BICS5T,1TB,S5E,XX.X,512G,K,LGA110	UN100	CRITICAL	NAND_L1:ITLC_2P0T_TO
335S00508	1	NAND,3DV6T,1TB,S5E,XX.X,512G,H,LGA110	UN100	CRITICAL	NAND_L1:ITLC_2P0T_HY
939-08815	1	PCBA,BANDIPUR,X1711	UN100	CRITICAL	NAND_L1:INTERPOSER

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A Module Parts

RT13 Retimer

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-21959	2	IC,LIFUKA,A0,USB-C RETIMER,FCCSP154	UF000,UF100	CRITICAL	ATCRTMR:A0
998-25504	2	IC,LIFUKA,B0,USB-C RETIMER,DEV,CSP154	UF000,UF100	CRITICAL	ATCRTMR:B0

Ace2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S02158	3	IC,CD3217,ACE2,B2,USB PWR SW W/HV,BGA123	UF400,UF500,U5500	CRITICAL	USBCPC:LAPTOP_B2_PPO
353S02742	3	IC,CD3217,ACE2,B2,USB PWR SW W/HV,BGA123	UF400,UF500,U5500	CRITICAL	USBCPC:LAPTOP_B2
353S02993	3	IC,ACE2,B3,USB PWR SW W/HV,RGM3,BGA123	UF400,UF500,U5500	CRITICAL	USBCPC:LAPTOP_B3

eUSB Level Shifter

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00628	2	IC,PARROT,CD2E226B,B0 LSB1,OTP-6,CSP25	UF600,UF650	CRITICAL	EUSB_LS:B0

Re-timer Sequencer

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S00483	2	IC,SLG4AP44593,PWR RAIL SEQUENCER,QFN8	UF790	CRITICAL	

SECURE ELEMENT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S00629	1	IC,SN210V,B1,CERES,DEV,VER=LN,WLCSP81	U5000	CRITICAL	SE:DEV_SW_LN
338S00630	1	IC,SN210V,B1,CERES,PROD,VER=MU,WLCSP81	U5000	CRITICAL	SE:PROD_SW_MU

B Programmable Parts

USBC ACE2 ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	UF260	CRITICAL	UPC01_ROM:BLANK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00537	335S00133	UPC01_ROM:BLANK	UF260	rdar://80303180
335S00570	335S00133	UPC01_ROM:BLANK	UF260	rdar://80303180
335S00571	335S00133	UPC01_ROM:BLANK	UF260	rdar://80303180

341S01912	1	ROM,ACE-P01 (V2.112.0.5) PROTO-0,X2203	UF260	CRITICAL	UPC01_ROM:P0
341S01998	1	ROM,ACE-P01 (V2.116.0.5) PROTO-2,X2203	UF260	CRITICAL	UPC01_ROM:P2
341S02052	1	Description: ROM,ACE-P01 (V2.131.3.6) EVT,X2203	UF260	CRITICAL	UPC01_ROM:EVT

MagSafe ACE2 ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00133	1	IC,SPI SERIAL FLASH,8MBITS,3.0V,USON8	U5560	CRITICAL	UPC5_ROM:BLANK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00537	335S00133	UPC5_ROM:BLANK	U5560	rdar://80303078
335S00570	335S00133	UPC5_ROM:BLANK	U5560	rdar://80303078
335S00571	335S00133	UPC5_ROM:BLANK	U5560	rdar://80303078

341S01913	1	ROM,ACE-P5 (V2.112.0.3) PROTO-0,X2203	U5560	CRITICAL	UPC5_ROM:P0
341S01999	1	ROM,ACE-P5 (V2.116.0.3) PROTO-2,X2203	U5560	CRITICAL	UPC5_ROM:P2
341S02053	1	ROM,ACE-P5 (V2.131.3.6) EVT,X2203	U5560	CRITICAL	UPC5_ROM:EVT

SOC ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-22994	1	IC,FLASH,64MBIT,1.2V,QE=1,M,4X4MM,SON8	U1900	CRITICAL	SOC_ROM:BLANK_P1
335S00575	1	IC,FLASH,64MBIT,1.2V,QE=1,M,4X4MM,SON8	U1900	CRITICAL	SOC_ROM:BLANK

RT13 ROM(s)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
998-22993	2	IC,FLASH,64MBIT,1.2V,QE=1,M,4X4MM,SON8	UF090,UF190	CRITICAL	RT13_ROM:BLANK_P1
335S00574	2	IC,FLASH,64MBIT,1.2V,QE=1,M,4X4MM,SON8	UF090,UF190	CRITICAL	RT13_ROM:BLANK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S00575	335S00574	RT13_ROM:BLANK	UF090,UF190	rdar://76779010

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SPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-23585	1	IC,PMU,VALE,CSP196	U7700	CRITICAL	SPMU_IC:DEV
998-24583	1	IC,PMU,VALE,A0,OTP-JPC,CSP196	U7700	CRITICAL	SPMU_IC:A0_JPC
998-25434	1	IC,PMU,VALE,A0,OTP-JPD,WLCSP196	U7700	CRITICAL	SPMU_IC:A0_JPD
998-26179	1	IC,PMU,VALE,A0,OTP-JPE,WLCSP196	U7700	CRITICAL	SPMU_IC:A0_JPE
998-26198	1	IC,PMU,VALE,A0,OTP-JPF,WLCSP196	U7700	CRITICAL	SPMU_IC:A0_JPF
998-26683	1	IC,PMU,VALE,A0,OTP-JPG,WLCSP196	U7700	CRITICAL	SPMU_IC:A0_JPG
998-26878	1	IC,PMU,VALE,A0,OTP-JPH,WLCSP196	U7700	CRITICAL	SPMU_IC:A0_JPH
998-27502	1	IC,PMU,VALE,A0,OTP-JPI,WLCSP196	U7700	CRITICAL	SPMU_IC:A0_JPI

MPMU

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
998-23524	1	IC,PMU,STOWE,CSP420	U8100	CRITICAL	MPMU_IC:DEV
998-24581	1	IC,PMU,STOWE,A0,OTP-JPC,CSP420	U8100	CRITICAL	MPMU_IC:A0_JPC
998-25433	1	IC,PMU,STOWE,A0,OTP-JPD,WLCSP420	U8100	CRITICAL	MPMU_IC:A0_JPD
998-26178	1	IC,PMU,STOWE,A0,OTP-JPE,WLCSP420	U8100	CRITICAL	MPMU_IC:A0_JPE
998-26197	1	IC,PMU,STOWE,A0,OTP-JPF,WLCSP420	U8100	CRITICAL	MPMU_IC:A0_JPF
998-26682	1	IC,PMU,STOWE,A0,OTP-JPG,WLCSP420	U8100	CRITICAL	MPMU_IC:A0_JPG
998-26877	1	IC,PMU,STOWE,A0,OTP-JPH,WLCSP420	U8100	CRITICAL	MPMU_IC:A0_JPH
998-27501	1	IC,PMU,STOWE,A0,OTP-JPI,WLCSP420	U8100	CRITICAL	MPMU_IC:A0_JPI

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Alternates

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	Alternate Vendor	Primary Vendor
138S0846	138S0811	ALT_CMN	ALL	rdar://problem/59474499	Samsung	Murata
376S1053	376S0604	ALT_CMN	ALL	rdar://problem/59475163	Diodes Inc	Fairchild
740S00041	740S0159	ALT_CMN	ALL	rdar://problem/59438907	Bourns	LittelFuse
107S00033	107S00034	ALT_CMN	ALL	rdar://problem/59471007	TFT	Cyntec
376S0948	376S00076	ALT_CMN	ALL	rdar://problem/59134310	Diodes Inc	Toshiba
128S00031	128S00011	ALT_CMN	ALL	rdar://problem/73938832	ROHM CORP	Kemet
128S00026	128S00011	ALT_CMN	ALL	rdar://problem/73938832	NEC	Kemet
128S00087	128S00011	ALT_CMN	ALL	rdar://problem/73938832	Panasonic	Kemet
376S00228	376S1179	ALT_CMN	ALL	rdar://problem/73939839	Fairchild	Vishay
376S00007	376S1179	ALT_CMN	ALL	rdar://problem/73939839	AOS	Vishay
376S1147	376S00281	ALT_CMN	ALL	rdar://problem/73949207	On Semi	AOS
107S00029	107S00087	ALT_CMN	ALL	rdar://problem/73982640	TFT	Yageo
138S00332	138S00328	ALT_CMN	ALL	rdar://problem/74145755	Kyocera	Murata
138S0863	138S1058	ALT_CMN	ALL	rdar://problem/74148337	Taiyo	Murata
138S00229	138S00107	ALT_CMN	ALL	rdar://problem/74148104	Kyocera	Murata
138S00022	138S0801	ALT_CMN	ALL	rdar://problem/74146716	Taiyo	Murata/Samsung
152S00398	152S00204	ALT_CMN	ALL	rdar://problem/73959393	Taiyo	Cyntec
152S01317	152S01268	ALT_CMN	ALL	rdar://problem/73958701	Taiyo	Cyntec
152S00997	152S00476	ALT_CMN	ALL	rdar://problem/73957803	Chilisin	Murata
107S00055	107S00090	ALT_CMN	ALL	rdar://problem/73982769	Cyntec	TFT
138S00181	138S0835	ALT_CMN	ALL	rdar://problem/74150148	Samsung	Murata
138S00291	138S0835	ALT_CMN	ALL	rdar://problem/74150148	Kyocera	Murata
377S00166	377S00160	ALT_CMN	ALL	rdar://problem/59407974	Semtech	On Semi
138S00330	138S00081	ALT_CMN	ALL	rdar://problem/74146122	SEMCO	Murata
377S00123	377S00031	ALT_CMN	ALL	rdar://problem/59407768	Semtech	On Semi
377S00186	377S00060	ALT_CMN	ALL	rdar://problem/59407847	Semtech	ST Micro
311S00230	311S00212	ALT_CMN	ALL	rdar://problem/71866385	Nexperia	TI
138S0771	138S00336	ALT_CMN	ALL	rdar://problem/71832350	Taiyo	Murata
138S00343	138S00329	ALT_CMN	ALL	rdar://problem/71832255	Kyocera	Murata
107S00076	107S00044	ALT_CMN	ALL	rdar://problem/71831138	Yageo	Cyntec
138S00151	138S00149	ALT_CMN	ALL	rdar://problem/71832189	Taiyo	Murata
138S00150	138S00149	ALT_CMN	ALL	rdar://problem/71832189	SEMCO	Murata
138S00148	138S00149	ALT_CMN	ALL	rdar://problem/71832189	Kyocera	Murata
107S00365	107S00373	ALT_CMN	ALL	rdar://problem/71831414	Cyntec	TFT
132S00176	132S0640	ALT_CMN	ALL	rdar://problem/71831575	Yageo	Murata
138S00164	138S00138	ALT_CMN	ALL	rdar://problem/71831667	Taiyo	Kyocera
138S00280	138S00138	ALT_CMN	ALL	rdar://problem/71831667	Samsung	Kyocera
138S00139	138S00138	ALT_CMN	ALL	rdar://problem/71831667	Murata	Kyocera
138S00047	138S00073	ALT_CMN	ALL	rdar://problem/71831776	Taiyo	Murata
138S00097	138S0750	ALT_CMN	ALL	rdar://problem/74149037	Taiyo Yuden	Murata
155S00007	155S0667	ALT_CMN	ALL	rdar://problem/73218092	Taiyo	Pansonic
740S00081	740S00053	ALT_CMN	ALL	rdar://problem/73218321	Bourns	AEM
377S00210	377S00172	ALT_CMN	ALL	rdar://problem/73218476	Semtech	TI
376S00292	376S1140	ALT_CMN	ALL	rdar://problem/73218568	Nexperia	Diodes Inc
376S00303	376S00012	ALT_CMN	ALL	rdar://problem/73218339	Diodes Inc	TI
128S00106	128S00107	ALT_CMN	ALL	rdar://problem/73938270	Tokin	Kemet
128S00110	128S00107	ALT_CMN	ALL	rdar://problem/73938270	Samsung	Kemet
371S00220	371S00307	ALT_CMN	ALL	rdar://problem/73940785	On Semi	Diodes Inc
152S00991	152S00984	ALT_CMN	ALL	rdar://problem/73958066	Taiyo	Cyntec
152S01378	152S01283	ALT_CMN	ALL	rdar://problem/80602206	Microgate	Cyntec
152S01494	152S01263	ALT_CMN	ALL	rdar://problem/73957626	Taiyo	Cyntec
152S00979	152S00874	ALT_CMN	ALL	rdar://problem/73960389	Taiyo	Cyntec
311S00322	311S00321	ALT_CMN	ALL	rdar://problem/72334560	Nexperia	TI
335S00232	335S00133	ALT_CMN	ALL	rdar://problem/73953460	Macronix	Winbond
138S00197	138S00409	ALT_CMN	ALL	rdar://problem/75264457	Murata	Taiyo
138S00413	138S00410	ALT_CMN	ALL	rdar://problem/75264676	Murata	Taiyo
376S00521	376S00519	ALT_CMN	ALL	rdar://problem/74496873	Vishay	On Semi
197S00318	197S00323	ALT_CMN	ALL	rdar://problem/75588335	NDK	TXC
197S00335	197S00323	ALT_CMN	ALL	rdar://problem/75588335	Kyocera	TXC

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	Alternate Vendor	Primary Vendor
371S00085	371S00190	ALT_CMN	ALL	rdar://problem/59404601	On Semi	Diodes Inc
311S00156	311S00129	ALT_CMN	ALL	rdar://problem/59489090	Nexperia	TI
376S1080	376S0820	ALT_CMN	ALL	rdar://problem/59489026	Diodes Inc	On Semi
311S00269	311S00234	ALT_CMN	ALL	rdar://problem/59489341	Nexperia	TI
376S1128	376S00282	ALT_CMN	ALL	rdar://problem/73941008	Diodes Inc	On Semi
376S00224	376S00282	ALT_CMN	ALL	rdar://problem/73941008	Nexperia	On Semi
107S00101	107S00005	ALT_CMN	ALL	TBD	Yageo	Cyntec
107S00102	107S00017	ALT_CMN	ALL	TBD	Yageo	Cyntec
107S0276	107S00020	ALT_CMN	ALL	TBD	Cyntec	TFT
107S00370	107S00371	ALT_CMN	ALL	TBD	Yageo	Cyntec/Yageo
107S00372	107S00371	ALT_CMN	ALL	TBD	Vishay	Cyntec/Yageo
107S00298	107S00460	ALT_CMN	ALL	TBD	TDK	Murata
107S0150	107S00460	ALT_CMN	ALL	TBD	Panasonic	Murata
138S00284	138S00136	ALT_CMN	ALL	rdar://problem/74149755	Kyocera	Murata
138S0852	138S0818	ALT_CMN	ALL	TBD	Samsung	Murata
155S0275	155S00188	ALT_CMN	ALL	TBD	Taiyo Yuden	Murata
155S0706	155S0302	ALT_CMN	ALL	TBD	Taiyo Yuden	Murata
155S0741	155S0361	ALT_CMN	ALL	TBD	Murata	TDK
155S0823	155S0644	ALT_CMN	ALL	TBD	TDK/Taiyo	Murata
311S00267	311S00244	ALT_CMN	ALL	TBD	Nexperia	TI
311S00268	311S00246	ALT_CMN	ALL	TBD	Nexperia	TI
152S01163	152S00136	ALT_CMN	ALL	Per Louisa Zhang	Chilisin	Cyntec
138S00031	138S0861	ALT_CMN	ALL	rdar://73954319	Murata/Taiyo	Murata
152S00810	152S01601	ALT_CMN	ALL	TBD	Taiyo Yuden	Cyntec
152S00809	152S00332	ALT_CMN	ALL	TBD	Taiyo Yuden	Cyntec
740S0118	740S00028	ALT_CMN	ALL	rdar://problem/74350704	Polytronics	Bussmann
740S0144	740S00028	ALT_CMN	ALL	rdar://problem/74350704	LittelFuse	Bussman
128S00094	128S00067	ALT_CMN	ALL	rdar://problem/73939352	Tokin/Kemet	Panasonic
128S00069	128S00067	ALT_CMN	ALL	rdar://problem/73939352	Rohm	Panasonic
138S00385	138S00377	ALT_CMN	ALL	rdar://problem/73954116	Kyocera	Murata
152S01521	152S01459	ALT_CMN	ALL	rdar://problem/74521339	Chilisin	Cyntec
152S01520	152S01458	ALT_CMN	ALL	rdar://problem/74521392	Chilisin	Cyntec
152S01519	152S01457	ALT_CMN	ALL	rdar://problem/74521425	Chilisin	Cyntec
311S00317	311S00316	ALT_CMN	ALL	TBD	Nexperia	TI
311S00272	311S00287	ALT_CMN	ALL	TBD	Nexperia	TI
311S00336	311S0613	ALT_CMN	ALL	TBD	TI	NXP/Diodes
138S00416	138S00328	ALT_CMN	ALL	rdar://problem/74145755	Taiyo Yuden	Murata
138S00087	138S1086	ALT_CMN	ALL	TBD	Taiyo Yuden	Murata
376S00332	376S0855	ALT_CMN	ALL	rdar://problem/75989879	Nexperia	Diodes Inc
376S00074	376S0855	ALT_CMN	ALL	rdar://problem/75989879	Toshiba	Diodes Inc
197S0590	197S0591	ALT_CMN	ALL	rdar://problem/73953315	EPSON	NDK
197S0588	197S0591	ALT_CMN	ALL	rdar://problem/73953315	TXC	NDK
311S0612	311S00263	ALT_CMN	ALL	rdar://problem/76165274	NXP	TI
311S00057	311S00263	ALT_CMN	ALL	rdar://problem/76165274	Diodes Inc	TI
152S01548	152S00289	ALT_CMN	ALL	rdar://problem/76165749	Murata	Cyntec
353S02402	353S1429	ALT_CMN	ALL	rdar://problem/76165876	On Semi	TI
371S00284	371S00187	ALT_CMN	ALL	rdar://problem/76171510	NXP	On Semi
371S00240	371S00364	ALT_CMN	ALL	rdar://problem/76171942	NXP	Diodes Inc.
376S00516	376S1112	ALT_CMN	ALL	rdar://problem/74046107	On Semi.	Diodes Inc.
152S00343	152S01325	ALT_CMN	ALL	rdar://problem/78474169	Murata	Taiyo Yuden
107S00479	107S00478	ALT_CMN	ALL	rdar://problem/80035462	Yageo	Cyntec
311S00352	311S00353	ALT_CMN	ALL	rdar://problem/80101244	Nexperia	TI
138S1065	138S1058	ALT_CMN	ALL	rdar://problem/80325043	Taiyo Yuden	Murata
371S00205	371S00077	ALT_CMN	ALL	rdar://problem/80305372	Vishay	Nexperia
107S00474	107S00017	ALT_CMN	ALL	rdar://problem/80289091	TFT	Cyntec
107S00475	107S00044	ALT_CMN	ALL	rdar://problem/71831138	Yageo	Cyntec
107S00443	107S00005	ALT_CMN	ALL	rdar://80470921	TFT	Cyntec

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	Alternate Vendor	Primary Vendor
311S00078	311S00275	ALT_CMN	ALL	rdar://80479617	Nexperia	Ti
311S00006	311S00323	ALT_CMN	ALL	rdar://72334608	Nexperia	Ti
152S01461	152S01283	ALT_CMN	ALL	rdar://80602206	Sunlord	Cyntec
104S00138	104S00135	ALT_CMN	ALL	rdar://80471945	TFT	Cyntec/Yageo
371S00370	371S00062	ALT_CMN	ALL	rdar://80501286	Diodes	On Semi
311S00361	311S00362	ALT_CMN	ALL	rdar://81349317	Diodes	Ti
311S00360	311S00362	ALT_CMN	ALL	rdar://81349317	Nexperia	Ti
116S00014	116S00044	ALT_CMN	ALL	rdar://80606250	Cyntec/ROHM	TFT
311S00335	311S00155	ALT_CMN	ALL	rdar://82988239	Ti	Nexperia
376S0725	376S0604	ALT_CMN	ALL	rdar://82961072	Vishay	Fairchild

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EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
	685-00426	COMMON PARTS,MLB,X2203	MLB_COMMON,ALTERNATE:PART,ALT_CMN
	685-00427	PARTS,SSD NAND1,MLB,X2203	SSD_2L,ALTERNATE:PART,ALT_CMN
0VRW	939-10926	PCBA,MLB,DCDC,X2203	MLB_COMMON,DEV_PARTS_BOM,NANDCFG:INTERPOSER,CPU:INTERPOSER,ALTERNATE:PART,ALT_CMN
1620	939-11657	PCBA,MLB,RF-CHAR,X2203	RF_COMMON
	985-01536	DEV PARTS,MLB,X2203	MLB_DEV,ALTERNATE:PART,ALT_CMN

SOC (BEST), Hynix and Micron 8GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
0W89	639-15199	PCBA,MLB,BEST,SOC,M-8G,SD-128G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_S5E_128G_SD
0W8C	639-15200	PCBA,MLB,BEST,SOC,M-8G,TO-128G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_S5E_128G_TO
0W8H	639-15203	PCBA,MLB,BEST,SOC,M-8G,HY-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_S5E_256G_HY
0W8J	639-15204	PCBA,MLB,BEST,SOC,M-8G,SD-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_S5E_256G_SD
0W8K	639-15205	PCBA,MLB,BEST,SOC,M-8G,TO-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_S5E_256G_TO
0W8P	639-15209	PCBA,MLB,BEST,SOC,M-8G,SD-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_S5E_512G_SD
0W8Q	639-15210	PCBA,MLB,BEST,SOC,M-8G,TO-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_S5E_512G_TO
1JQJ	639-16109	PCBA,MLB,BEST,SOC,M-8G,HY-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_S5E_512G_HY
0W8V	639-15213	PCBA,MLB,BEST,SOC,M-8G,HY-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_S5E_1P0T_HY
0W8W	639-15214	PCBA,MLB,BEST,SOC,M-8G,TO-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_S5E_1P0T_TO
0W90	639-15217	PCBA,MLB,BEST,SOC,M-8G,HY-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_S5E_2P0T_HY
0W91	639-15218	PCBA,MLB,BEST,SOC,M-8G,TO-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_BEST,NANDCFG:ITLC_S5E_2P0T_TO

SOC (GOOD), Hynix and Micron 8GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
Q2D9	639-15221	PCBA,MLB,GOOD,SOC,M-8G,SD-128G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_S5E_128G_SD
Q2DC	639-15222	PCBA,MLB,GOOD,SOC,M-8G,TO-128G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_S5E_128G_TO
Q2DD	639-15225	PCBA,MLB,GOOD,SOC,M-8G,HY-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_S5E_256G_HY
Q2DF	639-15226	PCBA,MLB,GOOD,SOC,M-8G,SD-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_S5E_256G_SD
Q2DG	639-15227	PCBA,MLB,GOOD,SOC,M-8G,TO-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_S5E_256G_TO
Q2DH	639-15231	PCBA,MLB,GOOD,SOC,M-8G,SD-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_S5E_512G_SD
Q2DJ	639-15232	PCBA,MLB,GOOD,SOC,M-8G,TO-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_S5E_512G_TO
1JQK	639-16110	PCBA,MLB,GOOD,SOC,M-8G,HY-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_S5E_512G_HY
Q2DK	639-15235	PCBA,MLB,GOOD,SOC,M-8G,HY-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_S5E_1P0T_HY
Q2DL	639-15236	PCBA,MLB,GOOD,SOC,M-8G,TO-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_S5E_1P0T_TO
Q2DM	639-15239	PCBA,MLB,GOOD,SOC,M-8G,HY-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_S5E_2P0T_HY
Q2DN	639-15240	PCBA,MLB,GOOD,SOC,M-8G,TO-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_8GB_GOOD,NANDCFG:ITLC_S5E_2P0T_TO

SOC (BEST), Hynix and Micron 16GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
0W8F	639-15201	PCBA,MLB,BEST,SOC,M-16G,SD-128G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_S5E_128G_SD
0W8G	639-15202	PCBA,MLB,BEST,SOC,M-16G,TO-128G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_S5E_128G_TO
0W8L	639-15206	PCBA,MLB,BEST,SOC,M-16G,HY-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_S5E_256G_HY
0W8M	639-15207	PCBA,MLB,BEST,SOC,M-16G,SD-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_S5E_256G_SD
0W8N	639-15208	PCBA,MLB,BEST,SOC,M-16G,TO-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_S5E_256G_TO
0W8R	639-15211	PCBA,MLB,BEST,SOC,M-16G,SD-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_S5E_512G_SD
0W8T	639-15212	PCBA,MLB,BEST,SOC,M-16G,TO-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_S5E_512G_TO
1JQL	639-16111	PCBA,MLB,BEST,SOC,M-16G,HY-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_S5E_512G_HY
0W8X	639-15215	PCBA,MLB,BEST,SOC,M-16G,HY-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_S5E_1P0T_HY
0W8Y	639-15216	PCBA,MLB,BEST,SOC,M-16G,TO-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_S5E_1P0T_TO
0W92	639-15219	PCBA,MLB,BEST,SOC,M-16G,HY-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_S5E_2P0T_HY
0W93	639-15220	PCBA,MLB,BEST,SOC,M-16G,TO-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_BEST,NANDCFG:ITLC_S5E_2P0T_TO

SOC (GOOD), Hynix and Micron 16GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
0W96	639-15223	PCBA,MLB,GOOD,SOC,M-16G,SD-128G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_S5E_128G_SD
0W97	639-15224	PCBA,MLB,GOOD,SOC,M-16G,TO-128G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_S5E_128G_TO
0W9D	639-15228	PCBA,MLB,GOOD,SOC,M-16G,HY-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_S5E_256G_HY
0W9F	639-15229	PCBA,MLB,GOOD,SOC,M-16G,SD-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_S5E_256G_SD
0W9G	639-15230	PCBA,MLB,GOOD,SOC,M-16G,TO-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_S5E_256G_TO
0W9K	639-15233	PCBA,MLB,GOOD,SOC,M-16G,SD-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_S5E_512G_SD
0W9L	639-15234	PCBA,MLB,GOOD,SOC,M-16G,TO-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_S5E_512G_TO
1JQM	639-16112	PCBA,MLB,GOOD,SOC,M-16G,HY-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_S5E_512G_HY
0W9P	639-15237	PCBA,MLB,GOOD,SOC,M-16G,HY-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_S5E_1P0T_HY
0W9Q	639-15238	PCBA,MLB,GOOD,SOC,M-16G,TO-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_S5E_1P0T_TO
0W9V	639-15241	PCBA,MLB,GOOD,SOC,M-16G,HY-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_S5E_2P0T_HY
0W9W	639-15242	PCBA,MLB,GOOD,SOC,M-16G,TO-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_16GB_GOOD,NANDCFG:ITLC_S5E_2P0T_TO

SOC (BEST), Hynix and Micron 24GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
1MNQ	639-16519	PCBA,MLB,BEST,SOC,M-24G,HY-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_S5E_256G_HY
1MNP	639-16518	PCBA,MLB,BEST,SOC,M-24G,SD-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_S5E_256G_SD
1MPJ	639-16537	PCBA,MLB,BEST,SOC,M-24G,TO-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_S5E_256G_TO
1MNT	639-16521	PCBA,MLB,BEST,SOC,M-24G,SD-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_S5E_512G_SD
1MNV	639-16522	PCBA,MLB,BEST,SOC,M-24G,TO-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_S5E_512G_TO
1MNR	639-16520	PCBA,MLB,BEST,SOC,M-24G,HY-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_S5E_512G_HY
1MNW	639-16523	PCBA,MLB,BEST,SOC,M-24G,HY-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_S5E_1P0T_HY
1MNX	639-16524	PCBA,MLB,BEST,SOC,M-24G,TO-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_S5E_1P0T_TO
1MNY	639-16525	PCBA,MLB,BEST,SOC,M-24G,HY-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_S5E_2P0T_HY
1MP0	639-16526	PCBA,MLB,BEST,SOC,M-24G,TO-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_BEST,NANDCFG:ITLC_S5E_2P0T_TO

SOC (GOOD), Hynix and Micron 24GB

EEEE	BOM NUMBER	BOM NAME	BOM OPTIONS
1MP1	639-16527	PCBA,MLB,GOOD,SOC,M-24G,HY-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_S5E_256G_HY
1MP2	639-16528	PCBA,MLB,GOOD,SOC,M-24G,SD-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_S5E_256G_SD
1MP3	639-16529	PCBA,MLB,GOOD,SOC,M-24G,TO-256G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_S5E_256G_TO
1MP4	639-16530	PCBA,MLB,GOOD,SOC,M-24G,SD-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_S5E_512G_SD
1MP5	639-16531	PCBA,MLB,GOOD,SOC,M-24G,TO-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_S5E_512G_TO
1MP6	639-16532	PCBA,MLB,GOOD,SOC,M-24G,HY-512G,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_S5E_512G_HY
1MP7	639-16533	PCBA,MLB,GOOD,SOC,M-24G,HY-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_S5E_1P0T_HY
1MP8	639-16534	PCBA,MLB,GOOD,SOC,M-24G,TO-1P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_S5E_1P0T_TO
1MP9	639-16535	PCBA,MLB,GOOD,SOC,M-24G,HY-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_S5E_2P0T_HY
1MPC	639-16536	PCBA,MLB,GOOD,SOC,M-24G,TO-2P0T,X2203	CMN_PARTS_BOM,DEV_PARTS_BOM,ALTERNATE:PART,ALT_CMN,CPU:SOC_24GB_GOOD,NANDCFG:ITLC_S5E_2P0T_TO

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