Hadley15" Schematics Document

Haswell ULT

2013-06-21
REV : A00

DY : None Installed
UMA: UMA only installed
OPS: Optimus solution installed.
eDP: Support eDP Panel installed.
LVDS: Support LVDS Panel installed.

<Core Design>

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Title	Cover Page	
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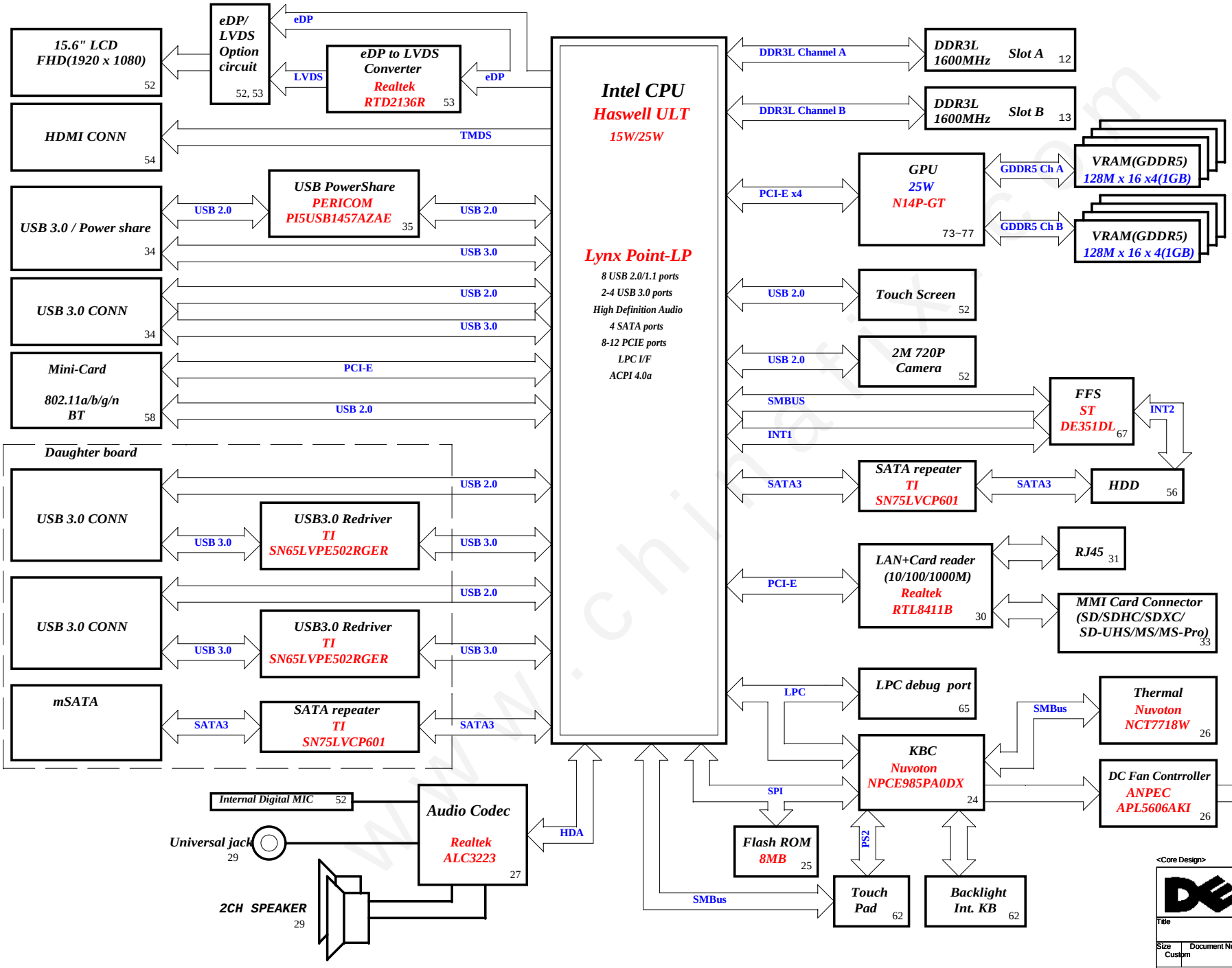
Hadly15 Block Diagram

Project code : 91.47L01.001
PCB P/N : 12311-1
Revision : A00



CHARGER BQ24717 44	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC TPS51225 45	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_CHARGER 3D3V_PWR

CPU DC/DC TPS51622 46~47	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51363 48	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0

SYSTEM DC/DC TPS51216 49	
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0

SYSTEM DC/DC NCP81172 82	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

Switches 36, 83	
INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_S5	3D3V_S0
3D3V_S0	3D3V_VGA_S0
1D05V_S0	1D05V_VGA_S0
1D35V_S3	1D35V_VGA_S0

LDO TLV70215DBVR 51	
INPUTS	OUTPUTS
3D3V_S5	

PCB LAYER
L1 : TOP
L2 : GND
L3 : Signal
L4 : Signal
L5 : VCC
L6 : Signal
L7 : GND
L8 : Bottom

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Title: *(Reserved)*

Size	Document Number	Rev
A3	*Hadley 15"*	*X02*

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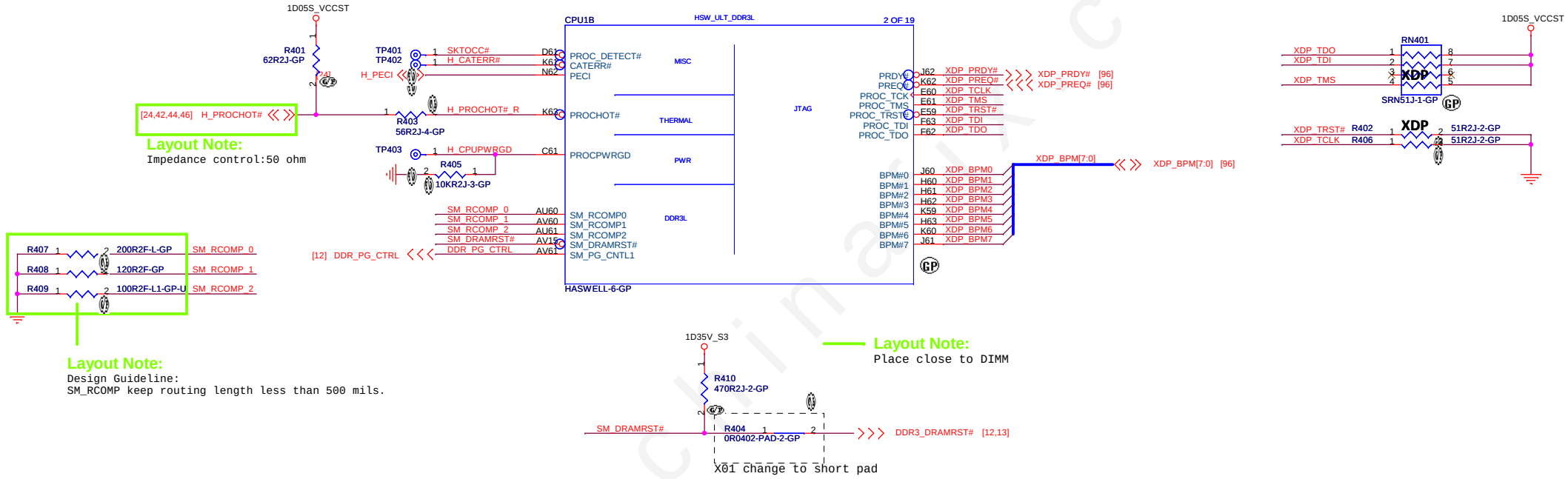
SSID = CPU



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Title: CPU (THERMAL/CLOCK)

Size	Document Number	Rev
A3	Hadley 15"	X02

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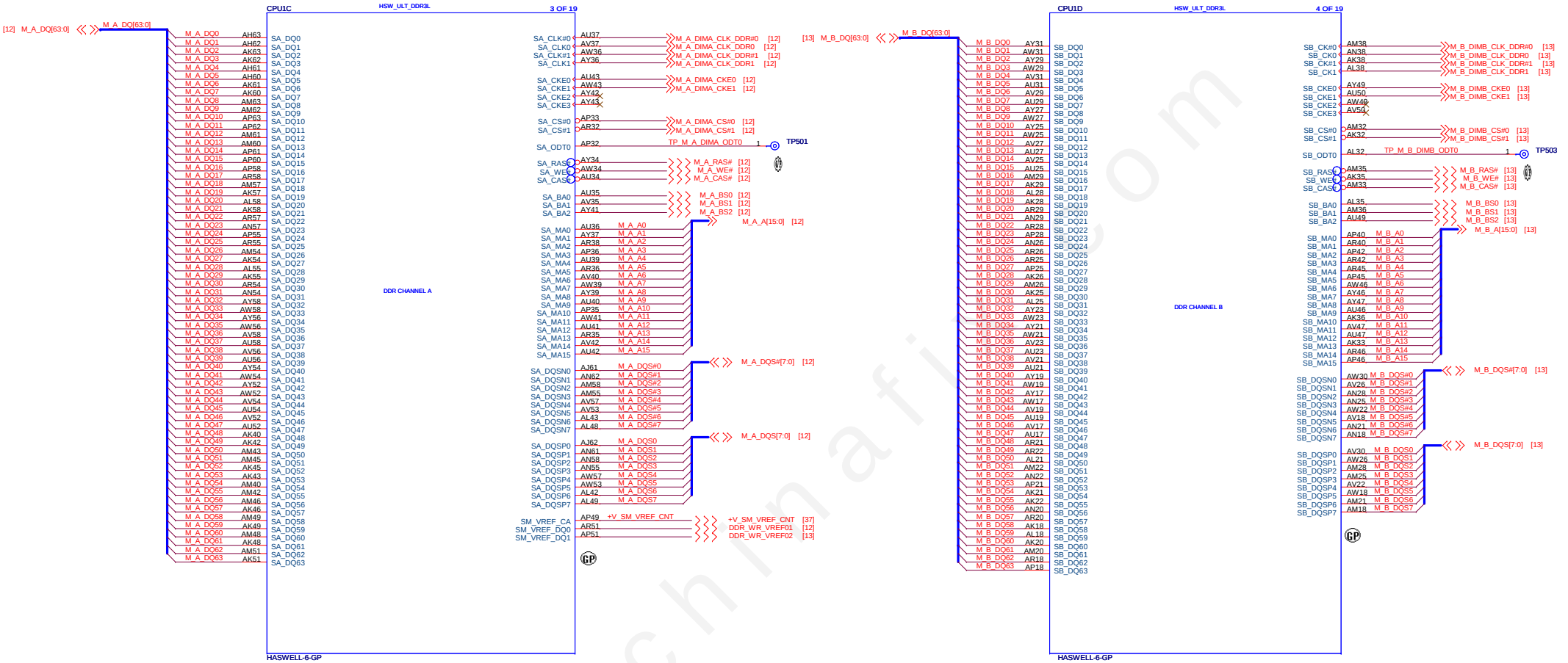
SSID = CPU



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Title: CPU (DDR)

Size: Custom | Document Number: Hadley 15" | Rev: X02

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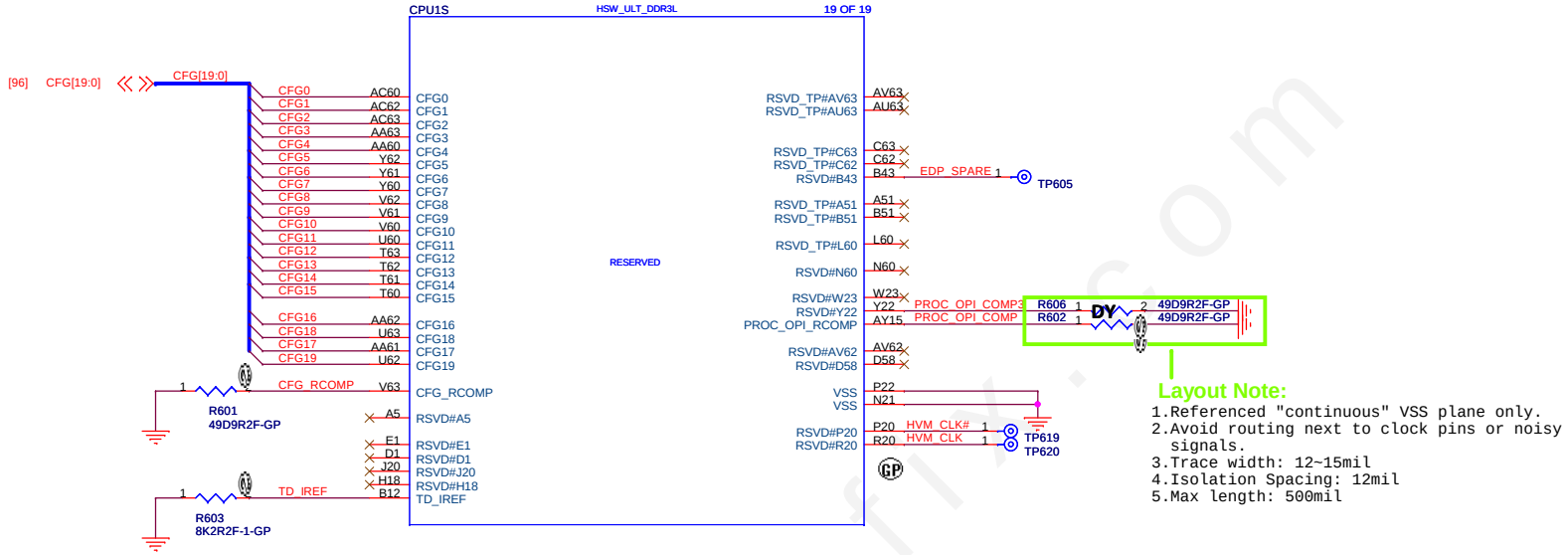
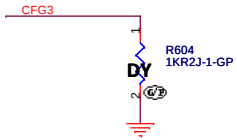
SSID = CPU

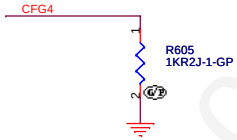


Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1 : DISABLED



DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT 1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

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Title: CPU (RESERVED)

Size: A3 | Document Number: Hadley 15" | Rev: X02

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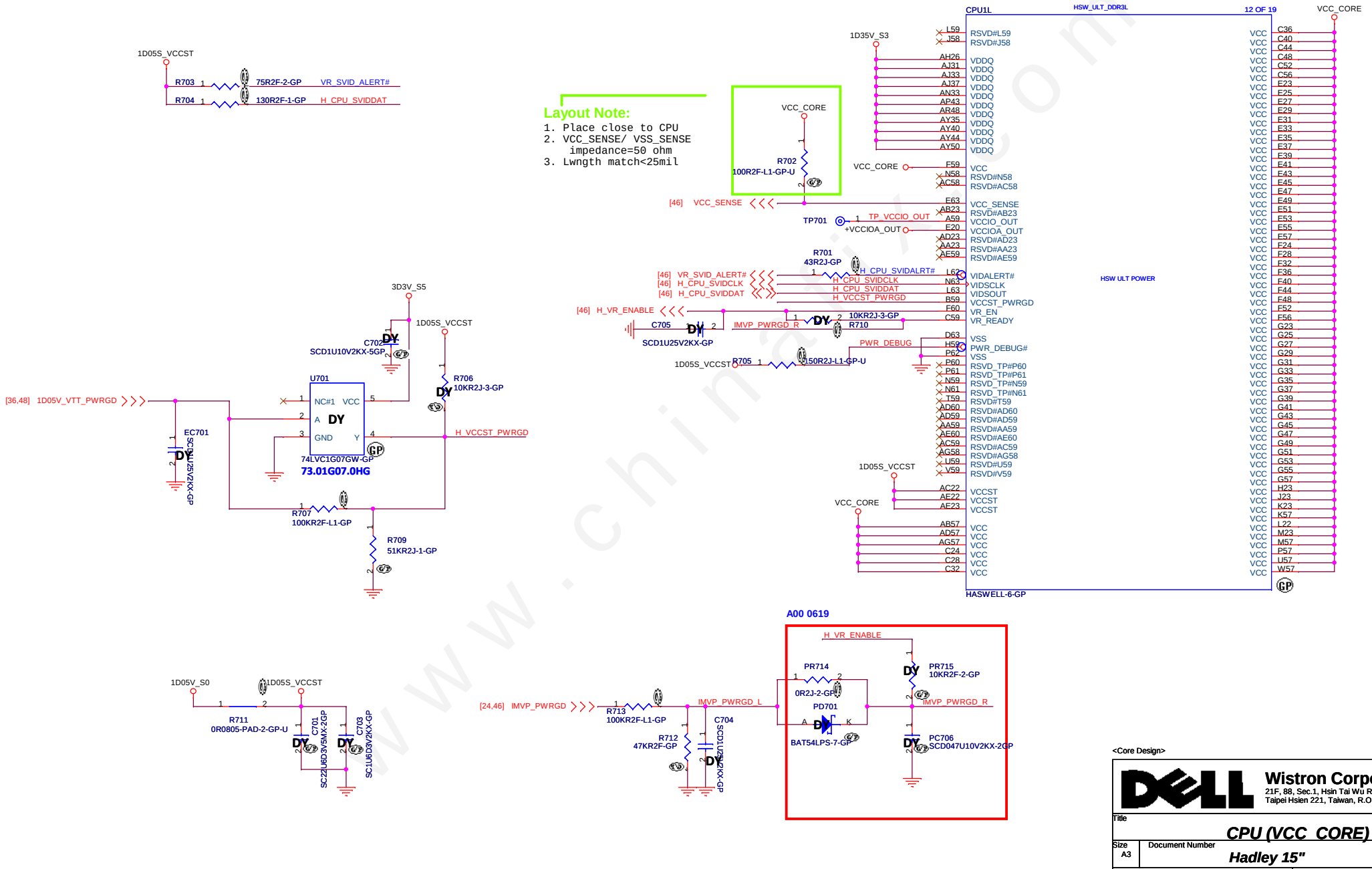
SSID = CPU



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Title: CPU (VCC_CORE)

Size: A3 | Document Number: Hadley 15" | Rev: X02

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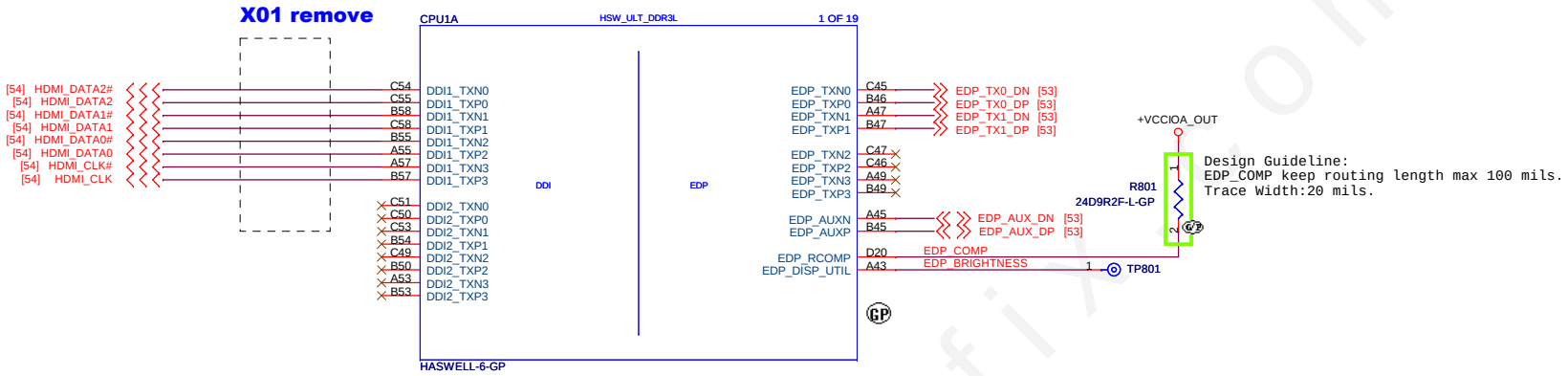
SSID = CPU

HDMI



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Title: CPU (DDI/EDP)

Size: A3 | Document Number: Hadley 15" | Rev: X02

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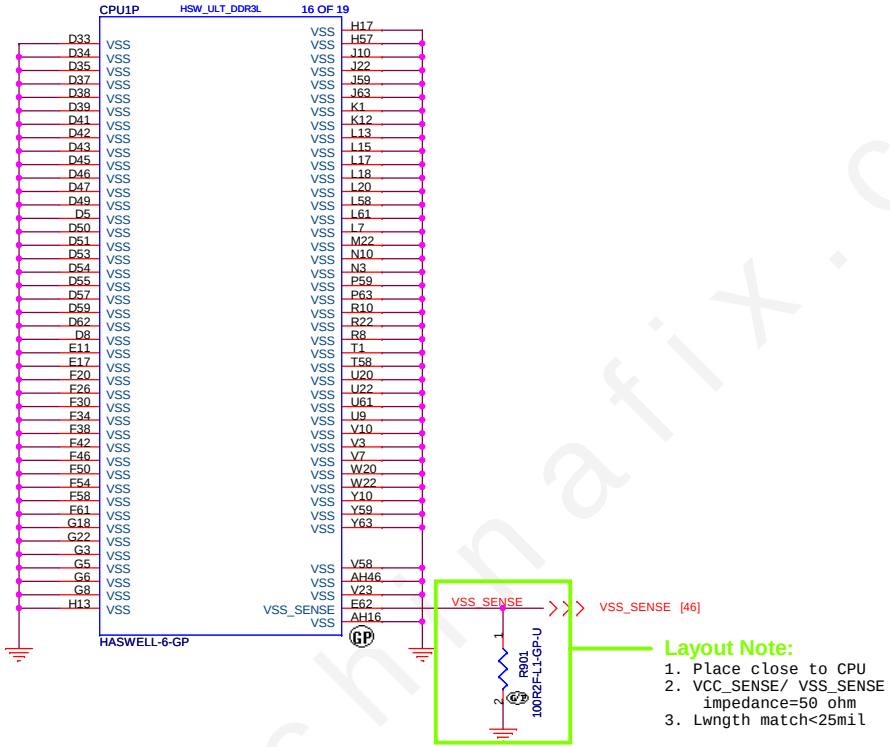
SSID = CPU



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Title: CPU (VSS)

Size: A3 | Document Number: Hadley 15" | Rev: X02

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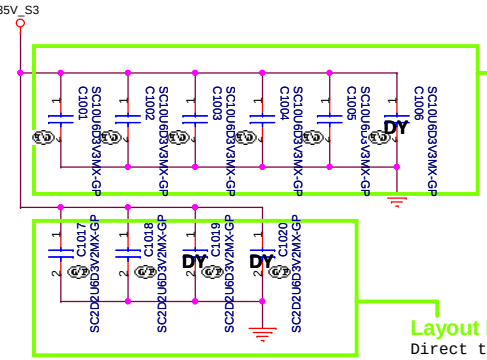
SSID = CPU



Layout Note:
As close to CPU as possible

Layout Note:
Direct tie to CPU VccIn/Vss balls

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Title	CPU(Power CAP1)	
Size: A3	Document Number: Hadley 15"	Rev: X02
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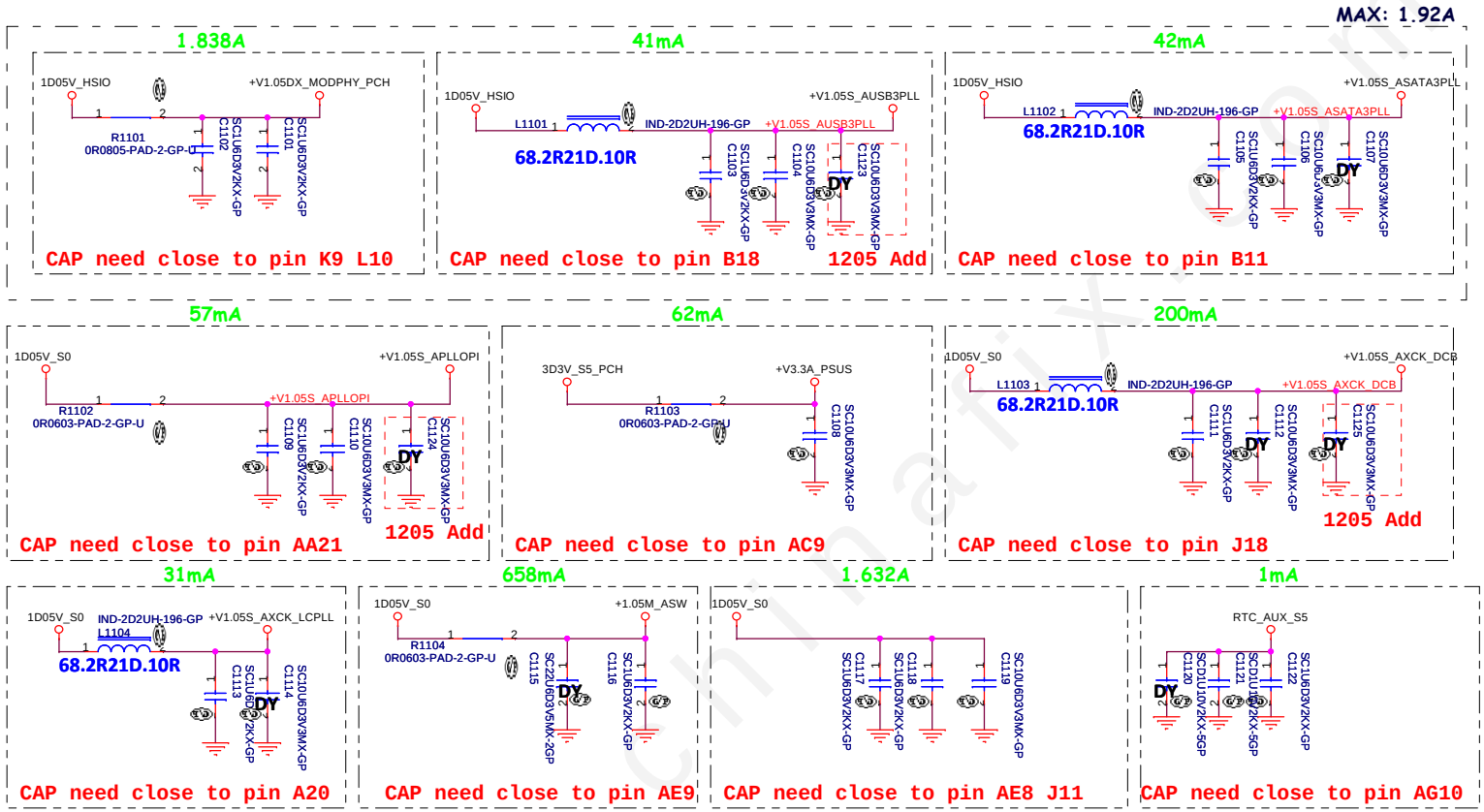
SSID = CPU



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Title: CPU(Power CAP2)

Size: A3 | Document Number: Hadley 15" | Rev: X02

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SSID = MEMORY

Note:
SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

DM1

[5] M_A_A[15:0]
M_A_A0 M_A_A1 M_A_A2 M_A_A3 M_A_A4 M_A_A5 M_A_A6 M_A_A7 M_A_A8 M_A_A9 M_A_A10 M_A_A11 M_A_A12 M_A_A13 M_A_A14 M_A_A15
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10/AP A11 A12 A13 A14 A15 A16/BA2

[5] M_A_BS2
[5] M_A_BS0
[5] M_A_BS1
[5] M_A_DQ[63:0]
BA0 BA1

M_A_DQ13 M_A_DQ8 M_A_DQ14 M_A_DQ10 M_A_DQ9 M_A_DQ12 M_A_DQ15 M_A_DQ11 M_A_DQ29 M_A_DQ28 M_A_DQ30 M_A_DQ31 M_A_DQ25 M_A_DQ24 M_A_DQ27 M_A_DQ26 M_A_DQ44 M_A_DQ41 M_A_DQ43 M_A_DQ47 M_A_DQ45 M_A_DQ40 M_A_DQ42 M_A_DQ46 M_A_DQ51 M_A_DQ50 M_A_DQ49 M_A_DQ48 M_A_DQ52 M_A_DQ53 M_A_DQ54 M_A_DQ55 M_A_DQ0 M_A_DQ1 M_A_DQ2 M_A_DQ6 M_A_DQ5 M_A_DQ4 M_A_DQ3 M_A_DQ7 M_A_DQ21 M_A_DQ20 M_A_DQ17 M_A_DQ16 M_A_DQ18 M_A_DQ19 M_A_DQ22 M_A_DQ23 M_A_DQ36 M_A_DQ33 M_A_DQ34 M_A_DQ38 M_A_DQ37 M_A_DQ32 M_A_DQ35 M_A_DQ39 M_A_DQ62 M_A_DQ58 M_A_DQ60 M_A_DQ61 M_A_DQ63 M_A_DQ59 M_A_DQ56 M_A_DQ57
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15 DQ16 DQ17 DQ18 DQ19 DQ20 DQ21 DQ22 DQ23 DQ24 DQ25 DQ26 DQ27 DQ28 DQ29 DQ30 DQ31 DQ32 DQ33 DQ34 DQ35 DQ36 DQ37 DQ38 DQ39 DQ40 DQ41 DQ42 DQ43 DQ44 DQ45 DQ46 DQ47 DQ48 DQ49 DQ50 DQ51 DQ52 DQ53 DQ54 DQ55 DQ56 DQ57 DQ58 DQ59 DQ60 DQ61 DQ62 DQ63

M_A_DQS#1 M_A_DQS#3 M_A_DQS#5 M_A_DQS#6 M_A_DQS#0 M_A_DQS#2 M_A_DQS#4 M_A_DQS#7
DQS0# DQS1# DQS2# DQS3# DQS4# DQS5# DQS6# DQS7#

M_A_DQS1 M_A_DQS3 M_A_DQS5 M_A_DQS6 M_A_DQS0 M_A_DQS2 M_A_DQS4 M_A_DQS7
DQS0 DQS1 DQS2 DQS3 DQS4 DQS5 DQS6 DQS7

[5] M_A_DQS#[7:0]
[5] M_A_DQS[7:0]

M_A_DIMA_ODT0 M_A_DIMA_ODT1
ODT0 ODT1

VREF_CA VREF_DQ
RESET#
VTT1 VTT2

NP1 NP2
RAS# WE# CAS#
CS0# CS1#
CKE0 CKE1
CK0 CK0# CK1 CK1#
DM0 DM1 DM2 DM3 DM4 DM5 DM6 DM7
SDA SCL
EVENT#
VDDSPD
SA0 SA1
NC#1 NC#2 NC#/TEST
VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18
VSS

SKT_DDR 204P SMD
DDR3-204P-122-GP-U1
62.10017.Z51

M_A_RAS# [5]
M_A_WE# [5]
M_A_CAS# [5]
M_A_DIMA_CS#0 [5]
M_A_DIMA_CS#1 [5]
M_A_DIMA_CKE0 [5]
M_A_DIMA_CKE1 [5]
M_A_DIMA_CLK_DDR0 [5]
M_A_DIMA_CLK_DDR#0 [5]
M_A_DIMA_CLK_DDR1 [5]
M_A_DIMA_CLK_DDR#1 [5]
PCH_SMBDATA [13,18,58,62,67]
PCH_SMBCLK [13,18,58,62,67]
SA0_DIMA
SA1_DIMA
3D3V_S0
1D35V_S3
0D675V_S0
M_VREF_CA_DIMMA
M_VREF_DQ_DIMMA
[4] DDR_PG_CTRL
[4,13] DDR3_DRAMRST#

R1202 0R0402-PAD-2-GP
R1201 0R0402-PAD-2-GP

C1203 SCD1U10V2KX-5GP

M_VREF_CA_DIMMA
C1201 SCD1U10V2KX-5GP
C1218 SCD1U10V2KX-5GP
C1202 SCD1U10V2KX-5GP

Layout Note:
Place these caps close to VREF_CA

M_VREF_DQ_DIMMA
C1204 SCD1U10V2KX-5GP
C1205 SC22D2U63V2MX-GP
C1206 SCD1U10V2KX-5GP

Layout Note:
Place these caps close to VREF_DQ

0D675V_S0
C1214 SCU6D3V2KX-GP
C1215 SCU6D3V2KX-GP
C1216 SCU6D3V2KX-GP

Layout Note:
Place these caps close to VTT1 and VTT2.

C1217 SCD1U10V2KX-5GP
close to dimm

Layout Note:
All VREF traces should have width=20mil; spacing=20 mil

C1220 SCD1U10V2KX-5GP
C1208 SC10D6J3V3MX-GP
C1209 SC10D6J3V3MX-GP
C1120 SC10D6J3V3MX-GP
C1121 SCD1U10V2KX-5GP
C1122 SCD1U10V2KX-5GP
C1210 SCD1U10V2KX-5GP
C1211 SCD1U10V2KX-5GP
C1212 SC1U6D3V2KX-GP
C1213 SC1U6D3V2KX-GP

Layout Note:
Place these Caps near SO-DIMMA.

Layout Note:
Place Close SO-DIMMA.

[5] DDR_WR_VREF01
0D675V_VTTREF
R1215 0R2J-2-GP
R1211 1K8R2F-GP
2R2F-GP R1210
M_VREF_DQ_DIMMA
C1219 SCD022U16V2JX-GP
+V_VREF_PATH1
R1213 1K8R2F-GP
R1212 24D9R2F-L-GP

X01 change to short pad
R1205 0R0402-PAD-2-GP
DDR_PG_CTRL_R
Q1201 DMN5L06K-7-GP
Q1201 Need check Vth=1V
84.05067.031

5V_S5
R1208 220KR2J-L2-GP
R1204 2MR2-GP
DDR_VTT_PG_CTRL
DDR_VTT_PG_CTRL [49]

Q1202 2N7002K-2-GP
84.2N702.J31
2ND = 84.2N702.031
M_A_B_DIMM_ODT

R1206 66D5R2F-GP M_A_DIMA_ODT0
R1207 66D5R2F-GP M_A_DIMA_ODT1
R1203 66D5R2F-GP M_B_DIMB_ODT0 [13]
R1209 66D5R2F-GP M_B_DIMB_ODT1 [13]

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Title: DDR3L-SODIMM1
Size: Custom | Document Number: Hadley 15" | Rev: X02
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SSID = MEMORY

DM2

M_B_A[15:0] [5]

M_B_A0 M_B_A1 M_B_A2 M_B_A3 M_B_A4 M_B_A5 M_B_A6 M_B_A7 M_B_A8 M_B_A9 M_B_A10 M_B_A11 M_B_A12 M_B_A13 M_B_A14 M_B_A15

[5] M_B_BS2
[5] M_B_BS0
[5] M_B_BS1
[5] M_B_DQ[63:0]

M_B_DQ8 M_B_DQ14 M_B_DQ10 M_B_DQ11 M_B_DQ12 M_B_DQ9 M_B_DQ13 M_B_DQ15 M_B_DQ28 M_B_DQ29 M_B_DQ26 M_B_DQ27 M_B_DQ25 M_B_DQ24 M_B_DQ30 M_B_DQ31 M_B_DQ40 M_B_DQ41 M_B_DQ46 M_B_DQ42 M_B_DQ45 M_B_DQ44 M_B_DQ47 M_B_DQ43 M_B_DQ56 M_B_DQ57 M_B_DQ59 M_B_DQ58 M_B_DQ61 M_B_DQ60 M_B_DQ63 M_B_DQ62 M_B_DQ4 M_B_DQ1 M_B_DQ3 M_B_DQ7 M_B_DQ5 M_B_DQ0 M_B_DQ2 M_B_DQ6 M_B_DQ21 M_B_DQ20 M_B_DQ22 M_B_DQ23 M_B_DQ16 M_B_DQ17 M_B_DQ19 M_B_DQ18 M_B_DQ36 M_B_DQ33 M_B_DQ35 M_B_DQ39 M_B_DQ37 M_B_DQ32 M_B_DQ34 M_B_DQ38 M_B_DQ52 M_B_DQ49 M_B_DQ48 M_B_DQ53 M_B_DQ51 M_B_DQ55 M_B_DQ54 M_B_DQ50

M_B_DQS#[7:0] [5]
M_B_DQS[7:0] [5]

M_B_DQS#1 M_B_DQS#3 M_B_DQS#5 M_B_DQS#7 M_B_DQS#0 M_B_DQS#2 M_B_DQS#4 M_B_DQS#6

M_B_DQS1 M_B_DQS3 M_B_DQS5 M_B_DQS7 M_B_DQS0 M_B_DQS2 M_B_DQS4 M_B_DQS6

[12] M_B_DIMB_ODT0
[12] M_B_DIMB_ODT1

M_VREF_CA_DIMMB
M_VREF_DQ_DIMMB

[4,12] DDR3_DRAMRST#

0D675V_S0

SKT_DDR 204P SMD
DDR3-204P-122-GP-U1
62.10017.Z51

M_B_RAS# [5]
M_B_WE# [5]
M_B_CAS# [5]

M_B_DIMB_CS#0 [5]
M_B_DIMB_CS#1 [5]

M_B_DIMB_CKE0 [5]
M_B_DIMB_CKE1 [5]

M_B_DIMB_CLK_DDR0 [5]
M_B_DIMB_CLK_DDR#0 [5]

M_B_DIMB_CLK_DDR1 [5]
M_B_DIMB_CLK_DDR#1 [5]

PCH_SMBDATA [12,18,58,62,67]
PCH_SMBCLK [12,18,58,62,67]

3D3V_S0

SA0_DIMB
SA1_DIMB

1D35V_S3

Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

M_VREF_CA_DIMMB

C1301 SCD1U10V2KX-5GP
EC1302 SCD1U10V2KX-5GP
C1302 SCD1U10V2KX-5GP

Layout Note:
Place these caps close to VREF_CA

M_VREF_DQ_DIMMB

C1305 SC2D2U6D3V2MX-GP
C1304 SCD1U10V2KX-5GP
C1306 SCD1U10V2KX-5GP

Layout Note:
Place these caps close to VREF_DQ

0D675V_S0

C1316 SC1U6D3V2KX-GP
C1317 SC1U6D3V2KX-GP
C1318 SC1U6D3V2KX-GP

Layout Note:
Place these caps close to VTT1 and VTT2.

C1319 SCD1U10V2KX-5GP

close to dimm

Layout Note:
All VREF traces should have width=20mil; spacing=20 mil

C1303 SCD1U10V2KX-5GP

R1301 10KR2J-3-GP
R1302 0R0402-PAD-2-GP

C1312 SC1U6D3V3MX-GP
C1311 SC1U6D3V3MX-GP
C1310 SC1U6D3V3MX-GP
C1309 SC1U6D3V3MX-GP
C1308 SC1U6D3V3MX-GP
C1307 SC1U6D3V3MX-GP

C1313 SCD1U10V2KX-5GP
C1314 SCD1U10V2KX-5GP
C1315 SCD1U10V2KX-5GP
C1301 SCD1U10V2KX-5GP

Layout Note:
Place these Caps near SO-DIMMA.

Layout Note:
Place Close SO-DIMMA.

[5] DDR_WR_VREF02

0D675V_VTTREF 1D35V_S3

R1308 0R2J-2-GP
R1306 1K8R2F-GP
2R2F-GP R1304
R1303 1K8R2F-GP
C1320 SCD022U16V2JX-GP
+V_VREF_PATH2
R1307 24D9R2F-L-GP

M_VREF_DQ_DIMMB

<Core Design>

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Title: DDR3L-SODIMM2

Size: Custom | Document Number: Hadley 15" | Rev: X02

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<Core Design>

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Title: M1&M3

Size: A3 | Document Number: Hadley 15" | Rev: X02

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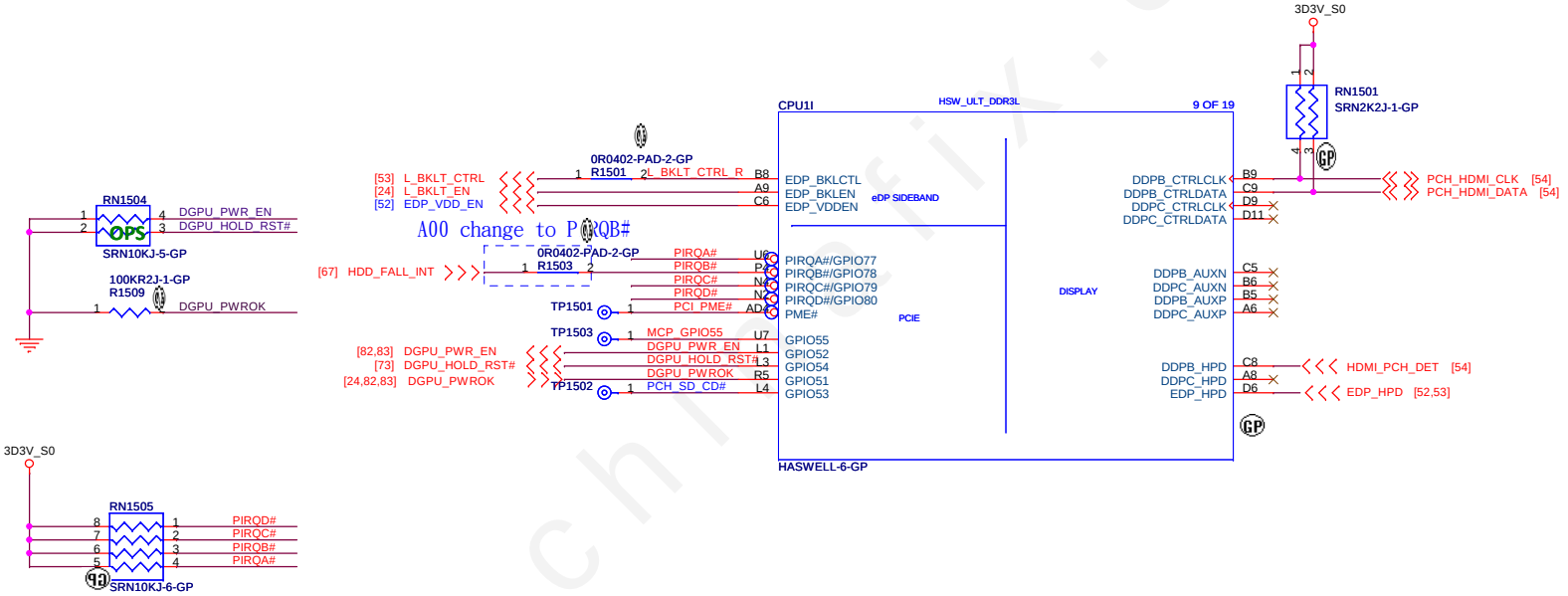
SSID = CPU



<Core Design>

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Title: CPU (EDP SIDEBAND/GPIO/DDI)

Size	Document Number	Rev
A3	Hadley 15"	X02

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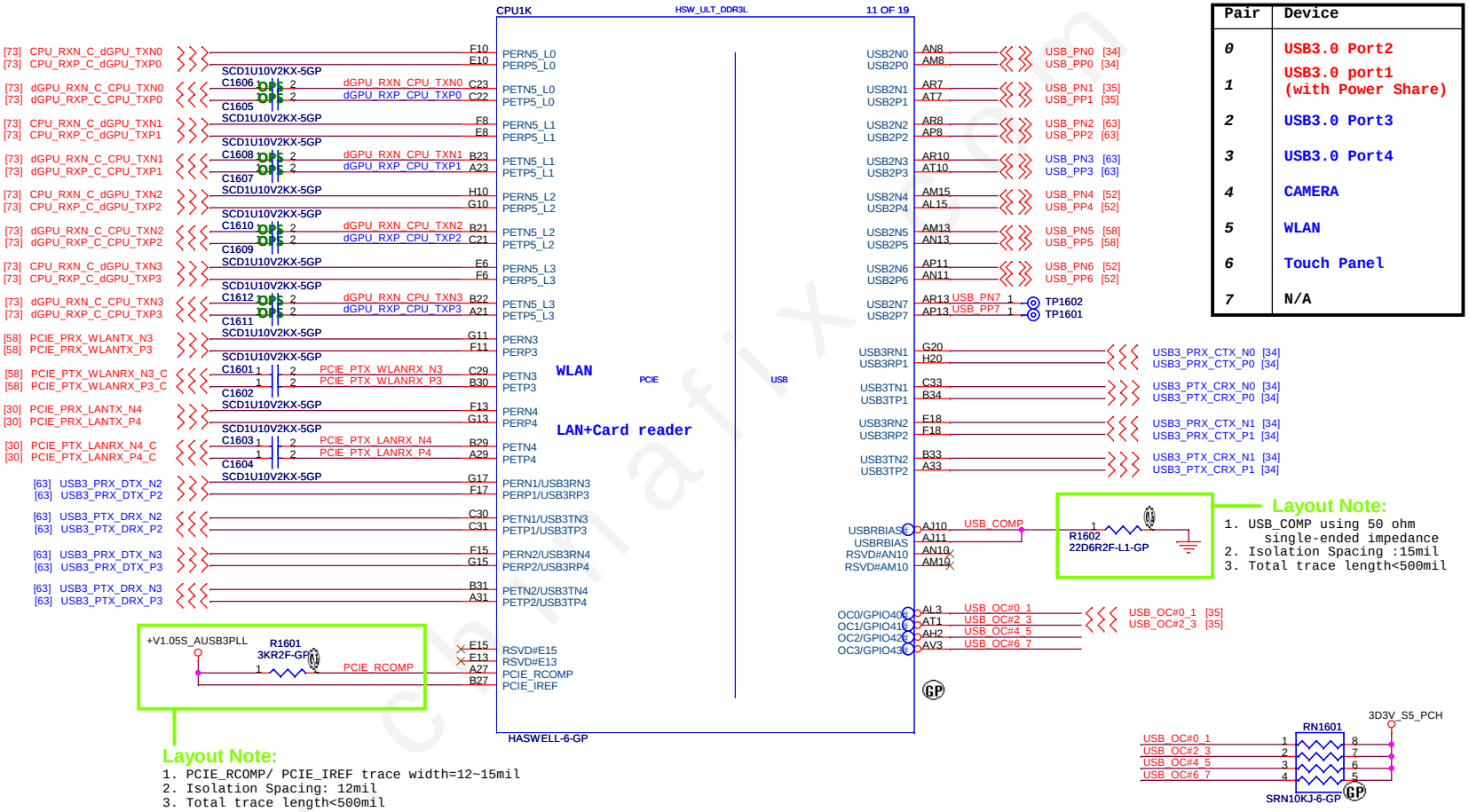
SSID = CPU

PCIE Table

Port	Device	Share BUS
1	N/A	USB3.0_3
2	N/A	USB3.0_4
3	WLAN	
4	LAN+ Card reader	
5(4lane)	GPU	
6(4lane)	N/A	SATA0~3



Layout Note:

1. PCIE_RCOMP/ PCIE_IREF trace width=12~15mil
2. Isolation Spacing: 12mil
3. Total trace length<500mil

USB 2.0 Table

Pair	Device
0	USB3.0 Port2
1	USB3.0 port1 (with Power Share)
2	USB3.0 Port3
3	USB3.0 Port4
4	CAMERA
5	WLAN
6	Touch Panel
7	N/A

Layout Note:

1. USB_COMP using 50 ohm single-ended impedance
2. Isolation Spacing :15mil
3. Total trace length<500mil

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PCIE/USB)

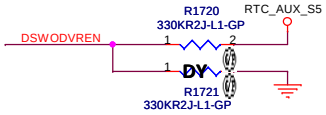
Size: A3 | Document Number: Hadley 15" | Rev: X02

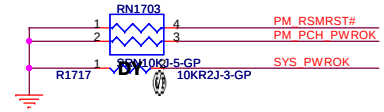
Date: Friday, June 21, 2013 | Sheet 16 of 101

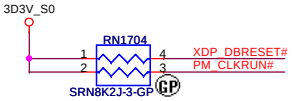
SSID = CPU

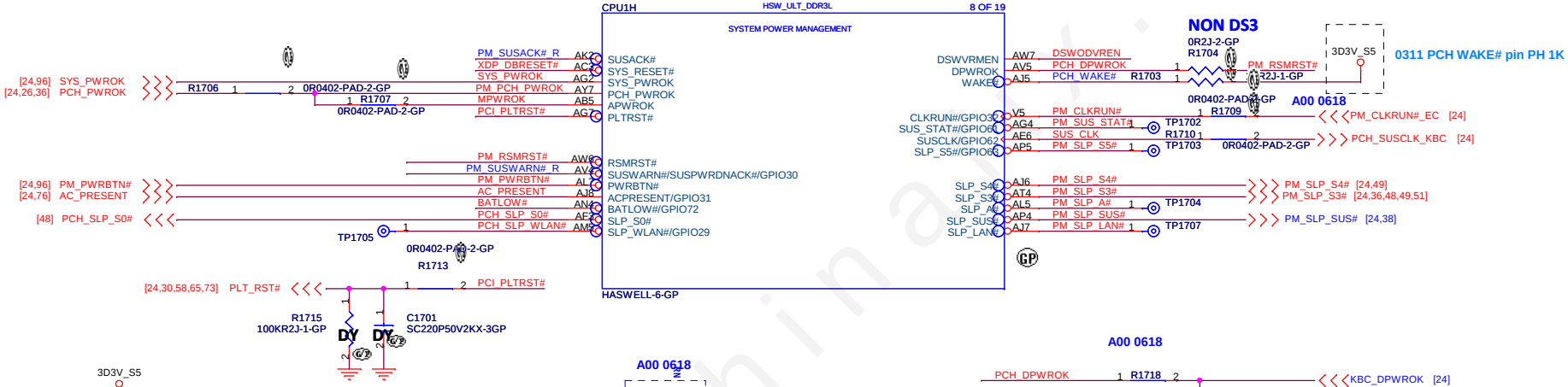
PCH strap pin:

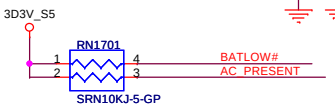
On Die DSW VR Enable	
DSWODVREN	Low = Disable High = Enable (default) *

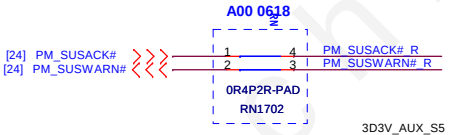


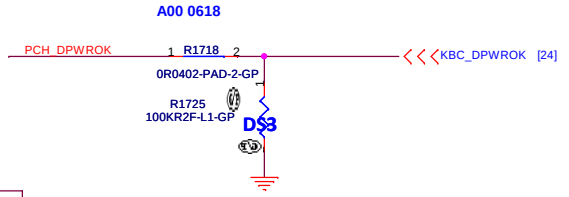


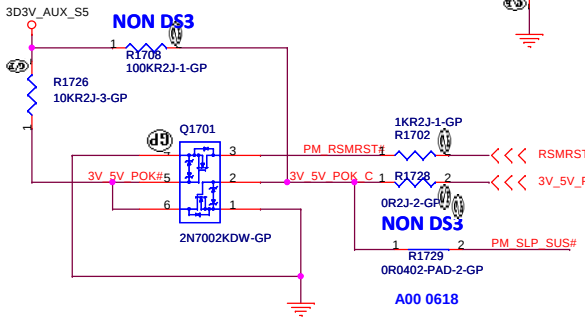


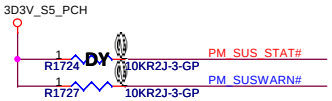












<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PM)

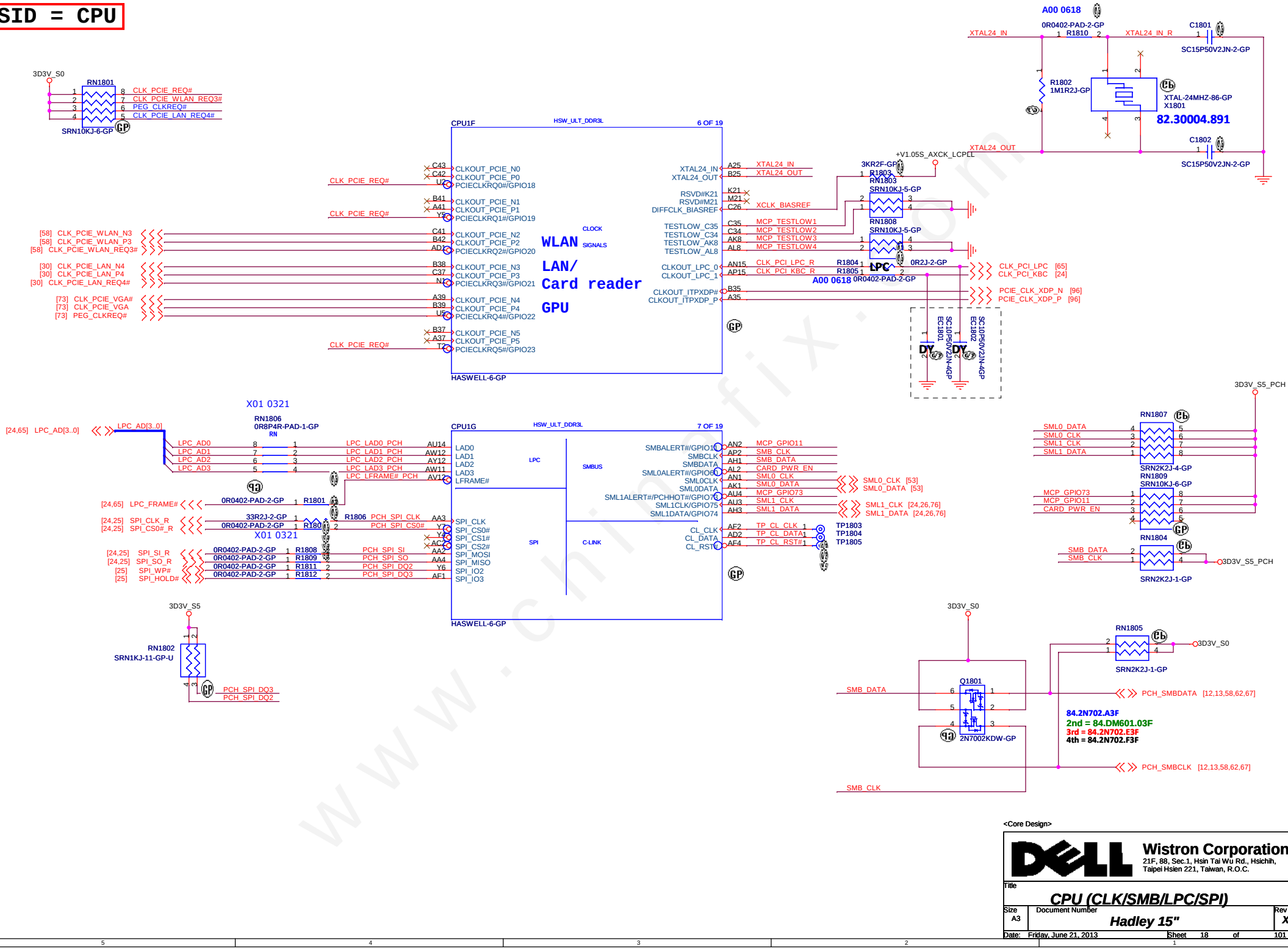
Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 21, 2013 | Sheet 17 of 101

SSID = CPU

A00 0618

X01 0321



<Core Design>

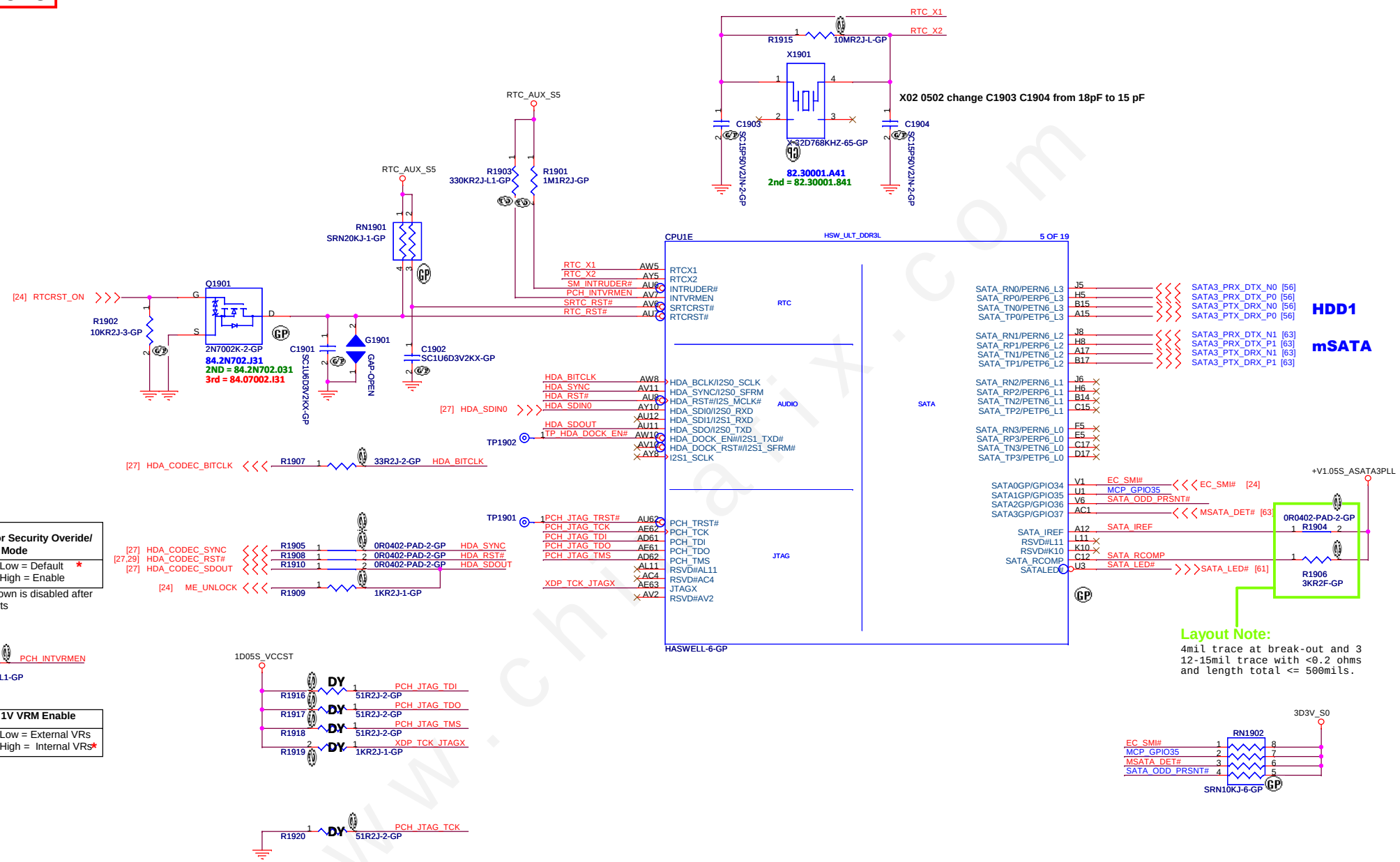
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (CLK/SMB/LPC/SPI)**

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 21, 2013 Sheet 18 of 101

SSID = CPU



Flash Descriptor Security Overide/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default * High = Enable

The internal pull-down is disabled after PLTRST# deasserts

Integrated SUS 1V VRM Enable	
INTVRMEN	Low = External VRs High = Internal VRs*

<Core Design>

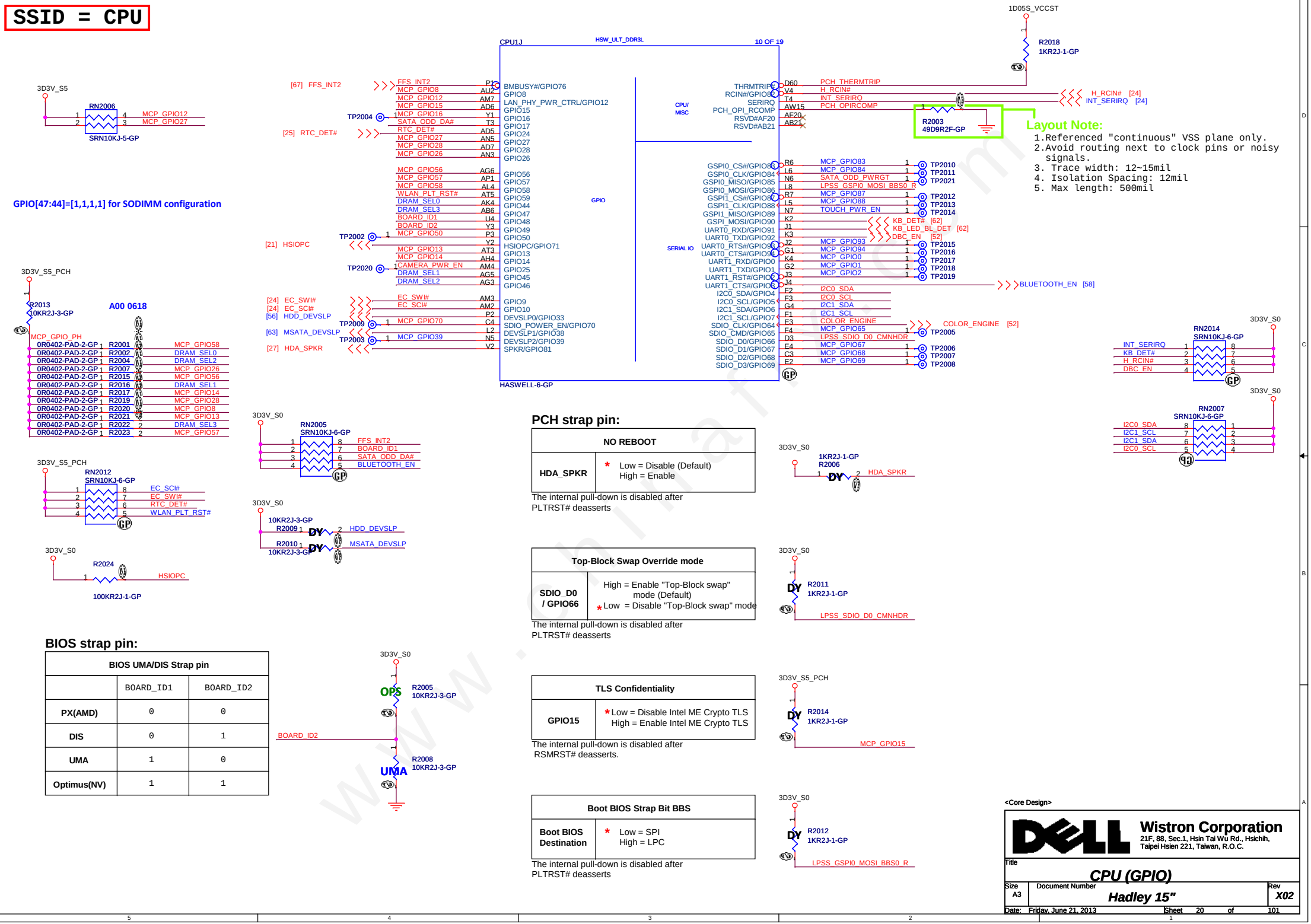
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RTC/SATA/HDA/JTAG)

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 21, 2013 Sheet 19 of 101

SSID = CPU



GPIO[47:44]=[1,1,1,1] for SODIMM configuration

Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

PCH strap pin:

NO REBOOT	
HDA_SPKR	* Low = Disable (Default) High = Enable

The internal pull-down is disabled after PLTRST# deasserts

Top-Block Swap Override mode	
SDIO_D0 / GPIO66	High = Enable "Top-Block swap" mode (Default) * Low = Disable "Top-Block swap" mode

The internal pull-down is disabled after PLTRST# deasserts

TLS Confidentiality	
GPIO15	* Low = Disable Intel ME Crypto TLS High = Enable Intel ME Crypto TLS

The internal pull-down is disabled after RSMRST# deasserts.

Boot BIOS Strap Bit BBS	
Boot BIOS Destination	* Low = SPI High = LPC

The internal pull-down is disabled after PLTRST# deasserts

BIOS strap pin:

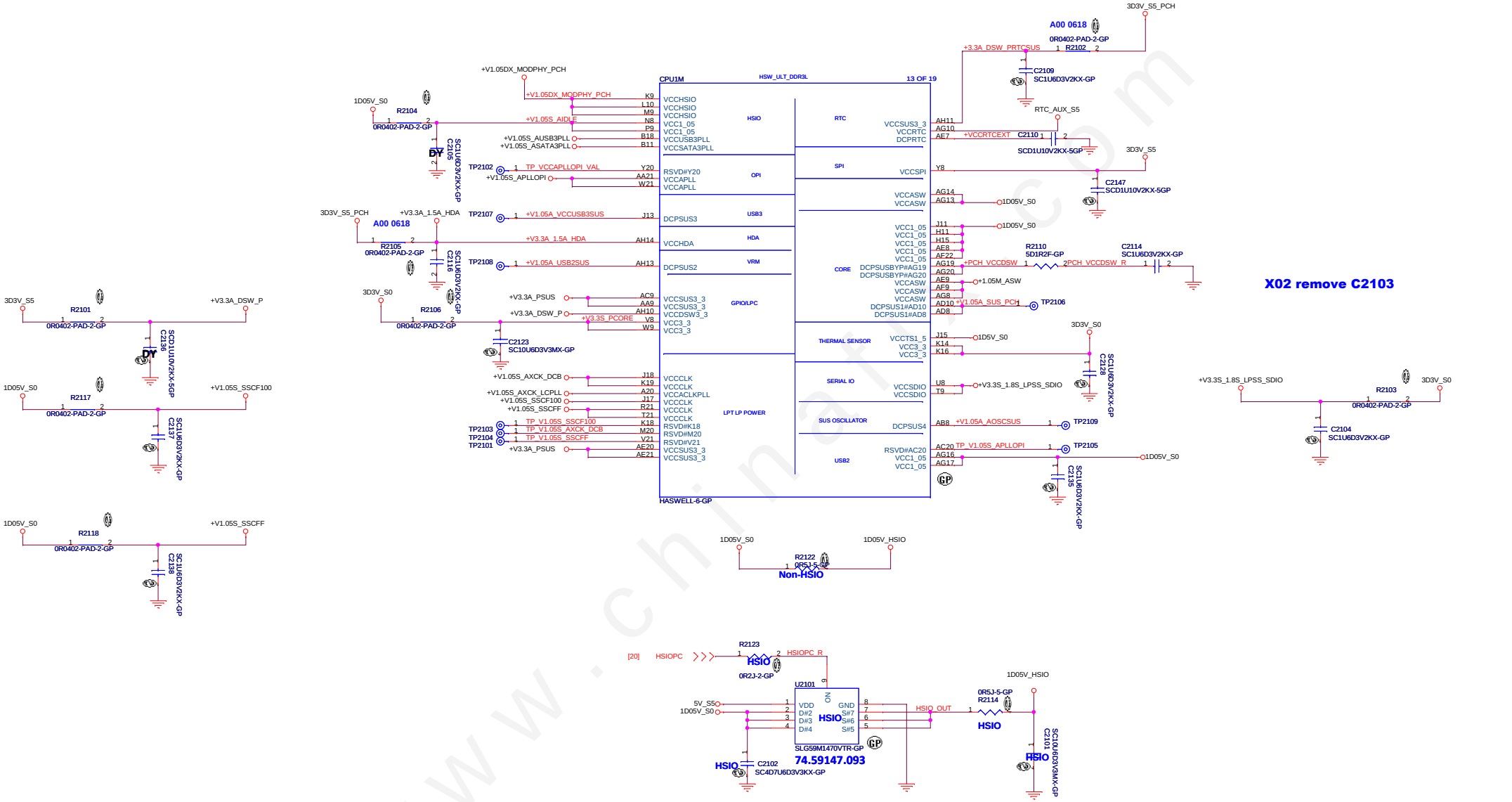
BIOS UMA/DIS Strap pin		
	BOARD_ID1	BOARD_ID2
PX(AMD)	0	0
DIS	0	1
UMA	1	0
Optimus(NV)	1	1

<Core Design>

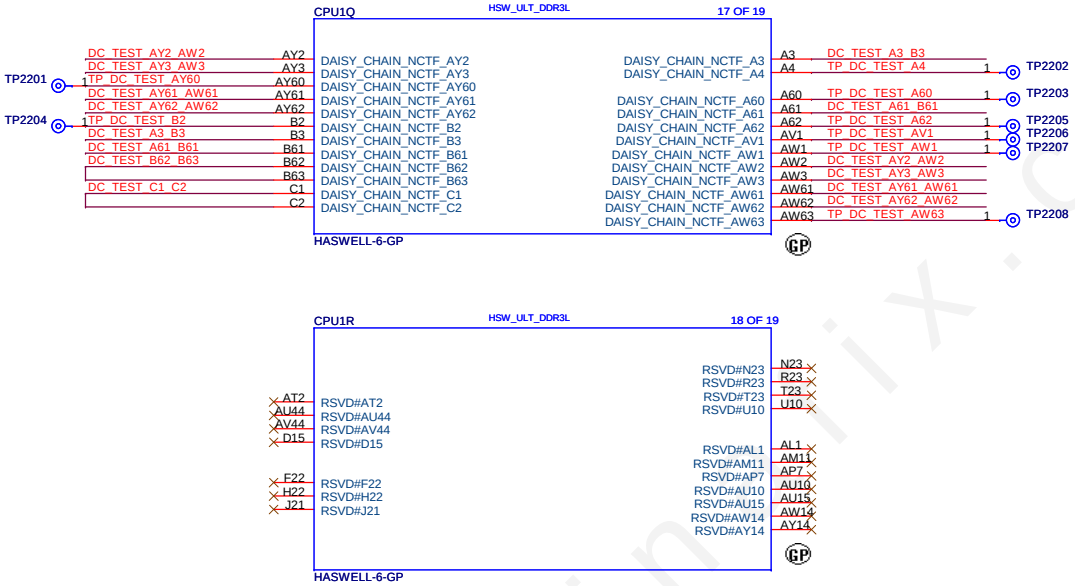
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (GPIO)
Size: A3
Document Number: Hadley 15"
Rev: X02
Date: Friday, June 21, 2013
Sheet 20 of 101

SSID = CPU



SSID = CPU



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RSVD

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 21, 2013 | Sheet 22 of 101

SSID = CPU

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (VSS)

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 21, 2013 Sheet 23 of 101

SSID = KBC

PCB VERSION A/D(PIN98)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
(DOH70)UMA	100.0K	10.0K(64.10025.6DL)	3.0V
(DOH50)UMA/eDP	100.0K	13.7K(64.13725.6DL)	2.902V
TBD	100.0K	17.8K(64.17825.6DL)	2.801V
(DOH70)DIS	100.0K	22.1K(64.22125.6DL)	2.702V
TBD	100.0K	27.0K(64.27025.6DL)	2.598V
TBD	100.0K	32.4K(64.32425.6DL)	2.492V
TBD	100.0K	37.4K(64.37425.6DL)	2.402V
TBD	100.0K	43.2K(64.43225.6DL)	2.304V
(DOH50)UMA/LVDS	100.0K	49.9K(64.49925.6DL)	2.201V
(DOH50)DIS/eDP	100.0K	57.6K(64.57625.6DL)	2.093V
TBD	100.0K	64.9K(64.64925.6DL)	2.001V
TBD	100.0K	73.2K(64.73225.6DL)	1.905V
TBD	100.0K	82.5K(64.82525.6DL)	1.808V
TBD	100.0K	93.1K(64.93125.6DL)	1.709V
TBD	100.0K	107K(64.10735.6DL)	1.594V
TBD	100.0K	120K(64.12035.6DL)	1.499V
TBD	100.0K	137K(64.13735.6DL)	1.392V
TBD	100.0K	154K(64.15435.6DL)	1.299V
TBD	100.0K	200K(64.20035.6DL)	1.099V
TBD	100.0K	232K(64.23236.6DL)	0.994V

Layout Note:
Need very close to EC

Don't PD

ALL_SYS_PWRGD assert, delay 10ms;
PCH_PWROK assert.

ALL_SYS_PWRGD assert, delay 100ms;
SYS_PWROK assert.

LVDS backlight Control from PS8625

eDP backlight Control from PCH

Backlight Control from LVDS Converter

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC
C2422 PDG is 47p

Layout Note:
Connect GND and AGND planes via either
0R resistor or connect directly.

AOAC Ambient temperature detect

EC_GPIO47 High Active

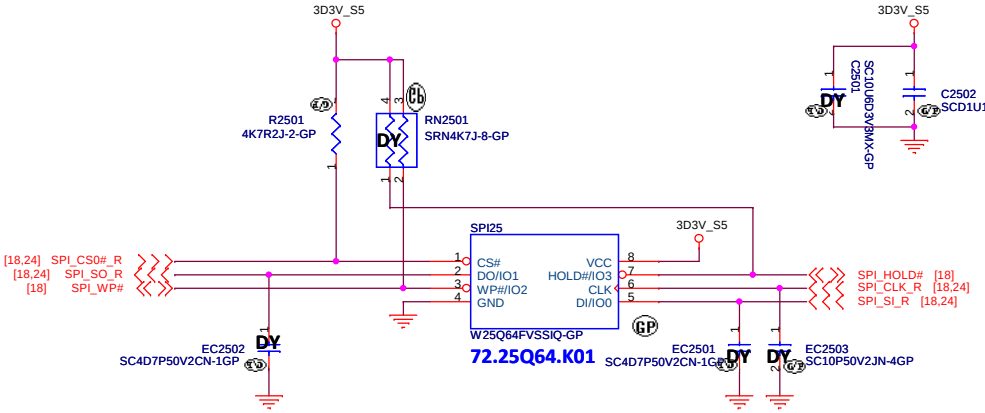
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

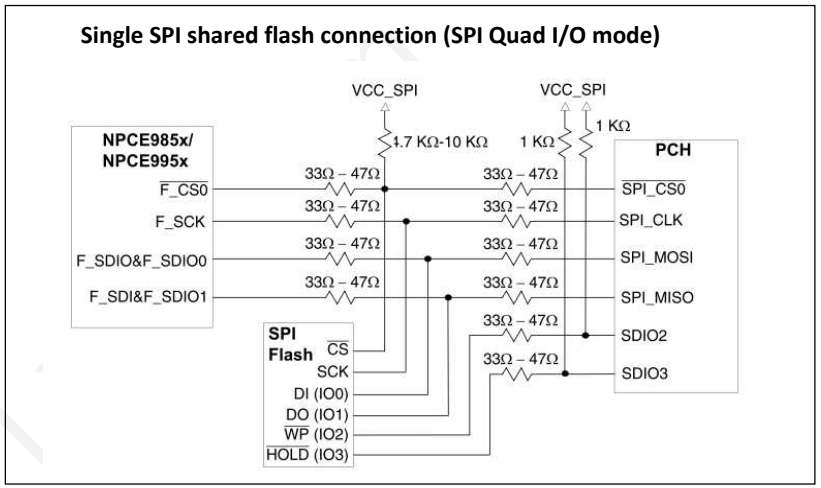
Title: KBC Nuvoton NPCE985
Size: A2 | Document Number: Hadley 15" | Rev: X02
Date: Friday, June 21, 2013 | Sheet 24 of 101

SSID = Flash.ROM

SPI Flash ROM(8M) for PCH

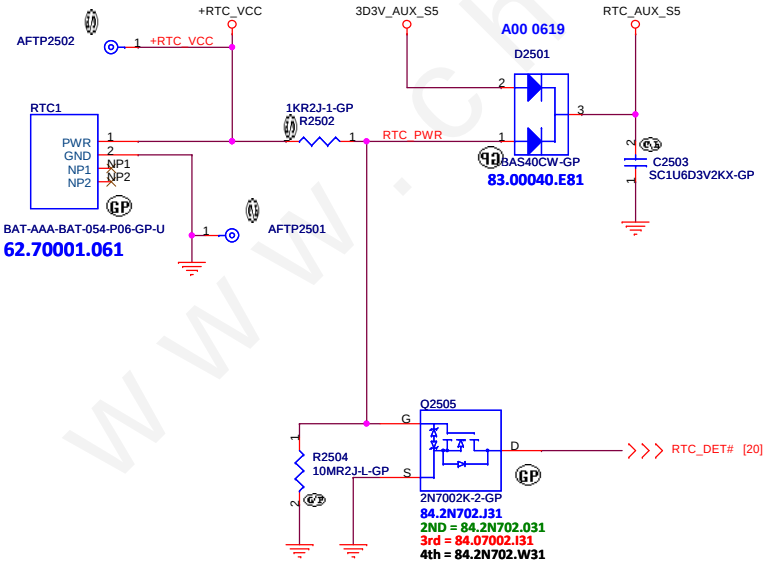


Source	QUAD/DUAL fast read	DUAL fast read
72.25Q64.K01	O	O
72.25647.00A	O	O



Refer to "NCPE985x/ NPCE995x board design reference guide"

SSID = RBATT



<Core Design>

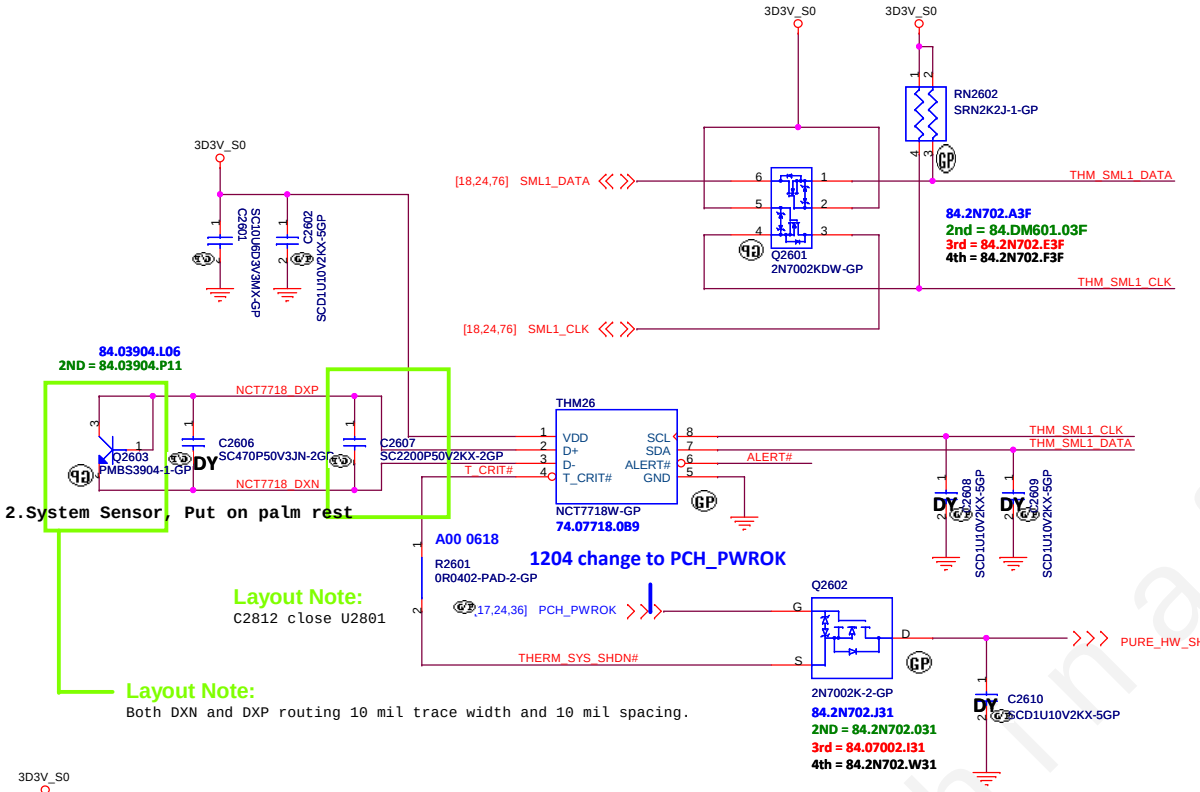
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

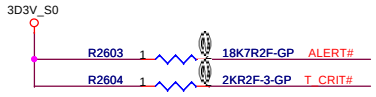
Title: Flash/RTC

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 21, 2013 | Sheet 25 of 101

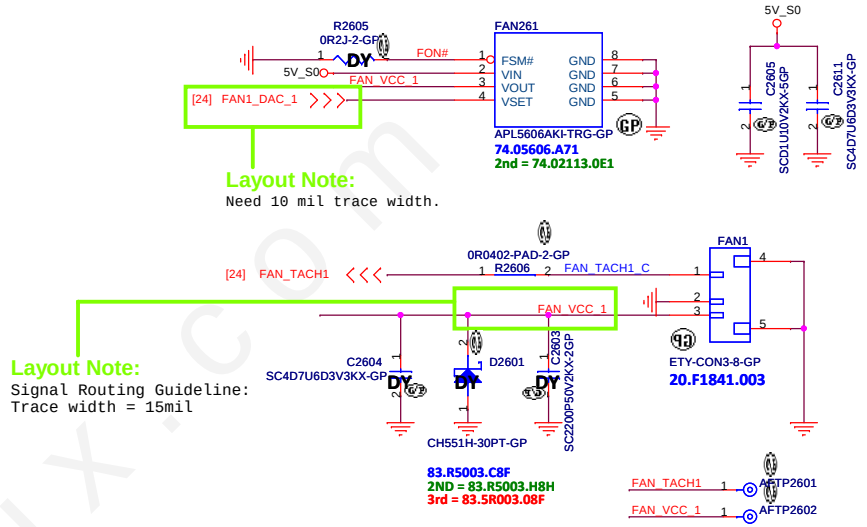
SSID = Thermal





TEMPERATURE (℃)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

Fan controller1



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal NCT7718W/Fan

Size: A3 | Document Number: Hadley 15" | Rev: X02

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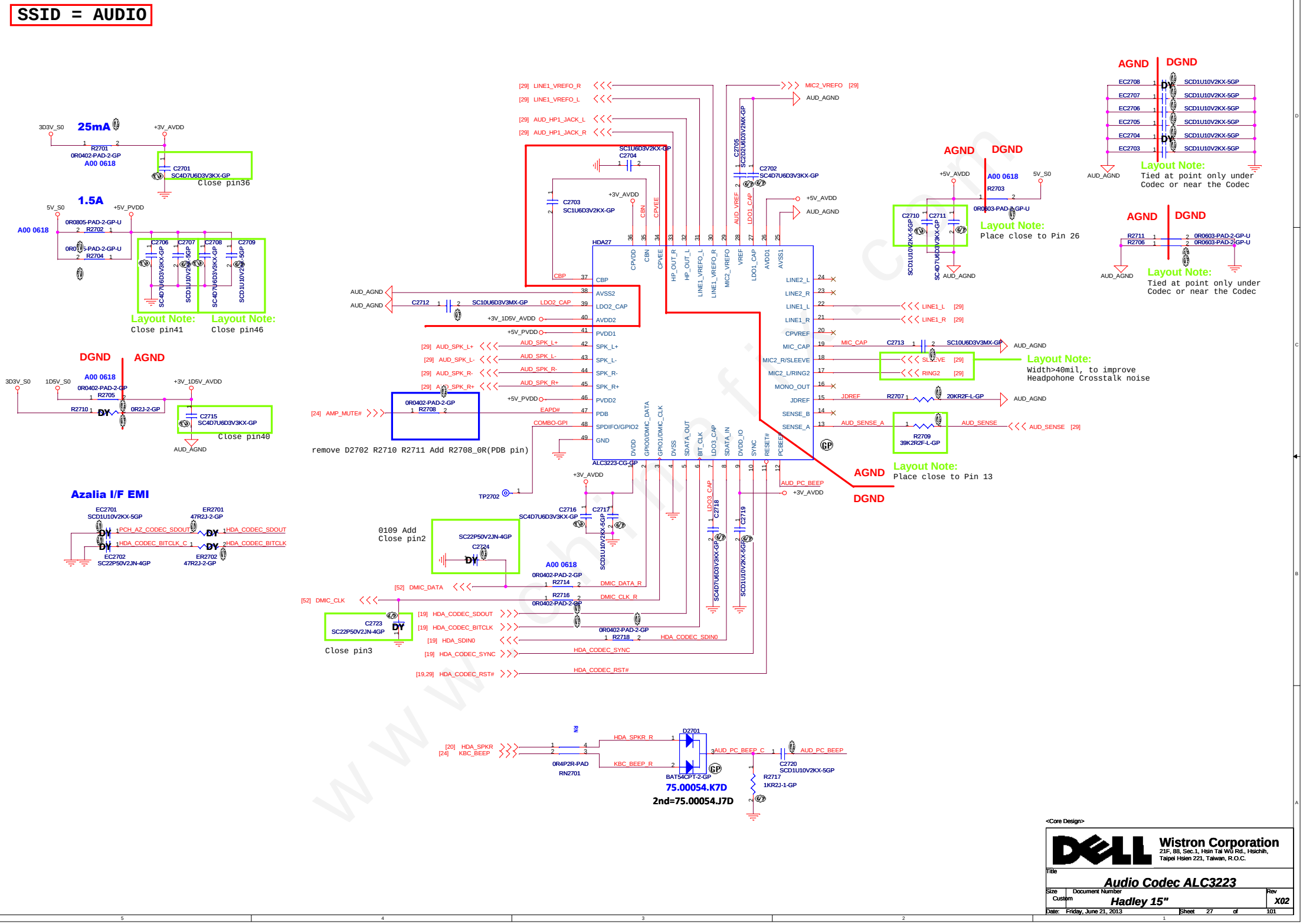
SSID = AUDIO



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Audio Codec ALC3223

Size	Document Number	Rev
Custom	Hadley 15"	X02

Date: Friday, June 21, 2013 Sheet 27 of 101

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

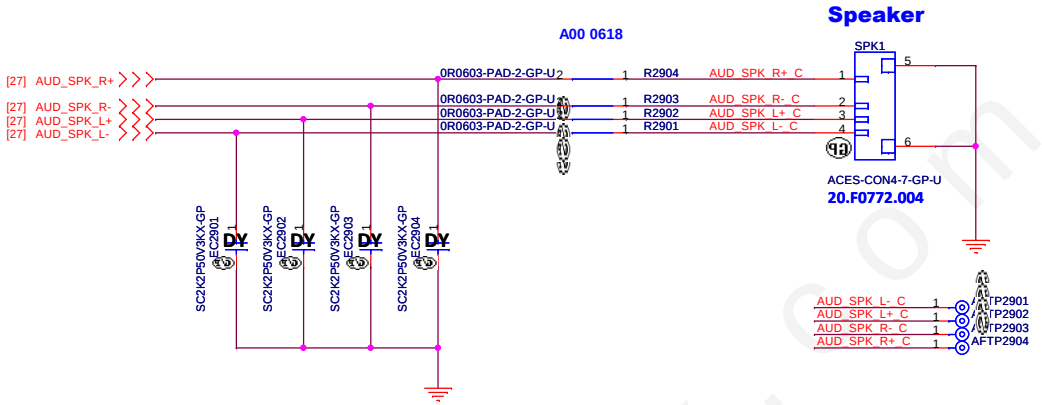
Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 21, 2013 | Sheet 28 of 101

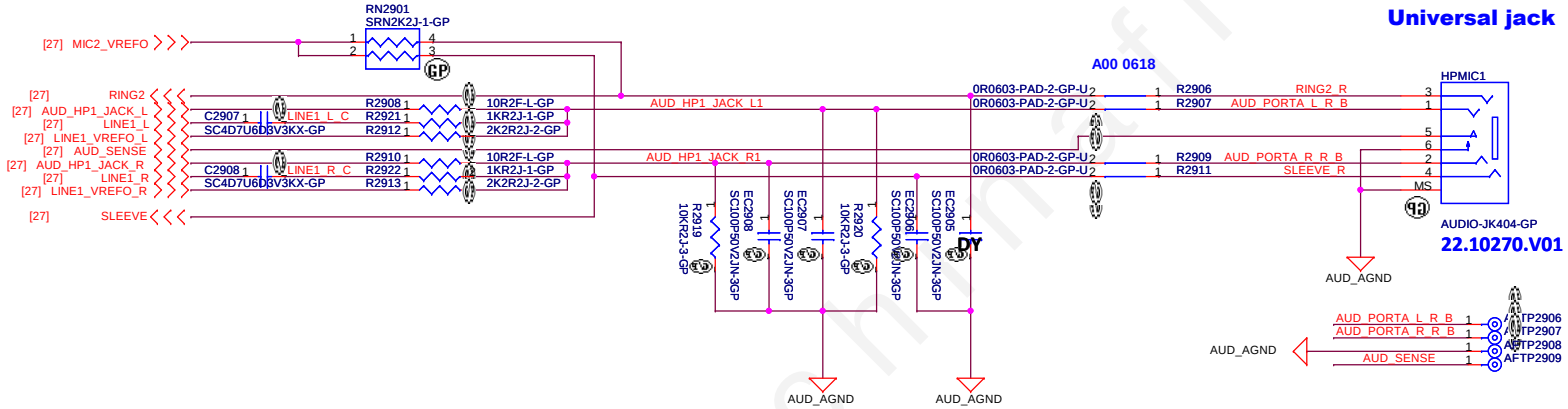
SSID = AUDIO

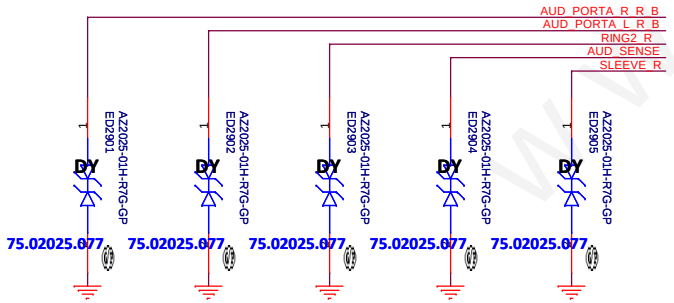
Speaker

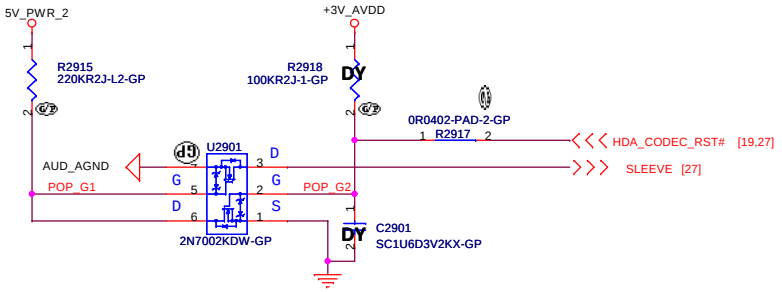


CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L_

Universal jack







<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Speaker/HPMIC CONN

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 21, 2013 | Sheet 29 of 101

SSID = LOM

main: 84.00102.031
2nd: 84.03403.031

0311 modify power rail

0110 add CAP
need close to chip

Pin12 Pull VCC33 (3D3V_S0)
Supported RTD3

Close To Pin 13

Close To Pin 27

A00 0618

X5R

68.4R71E.10G

RTL8411B-CGT-GP

71.08411.D03

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

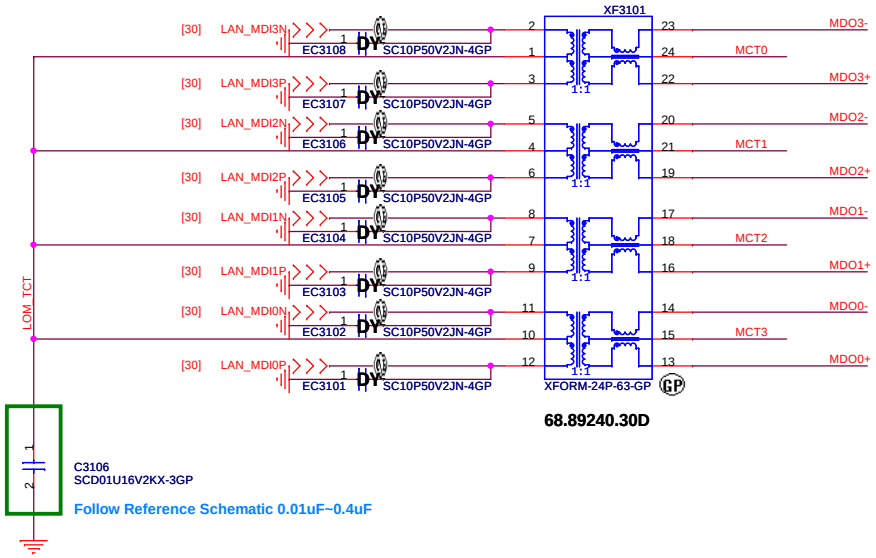
Title: LOM(RTL8411B)

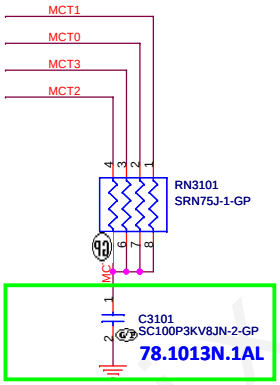
Size: A3 | Document Number: Hadley 15" | Rev: X02

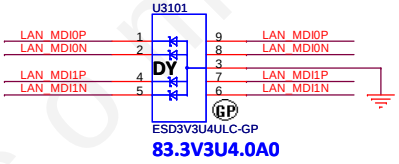
Date: Friday, June 21, 2013 | Sheet 30 of 101

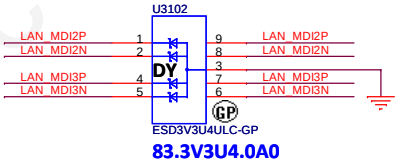
SSID = LOM

GIGA LAN TransFormer

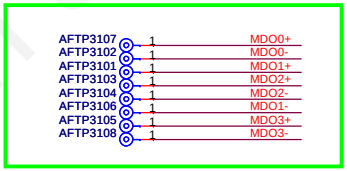


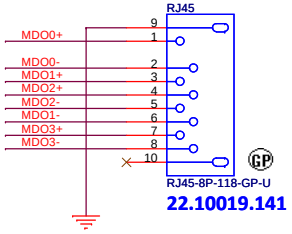






Layout:
Place near RJ45





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RJ45+Transformer

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 21, 2013 | Sheet 31 of 101

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<Core Design>

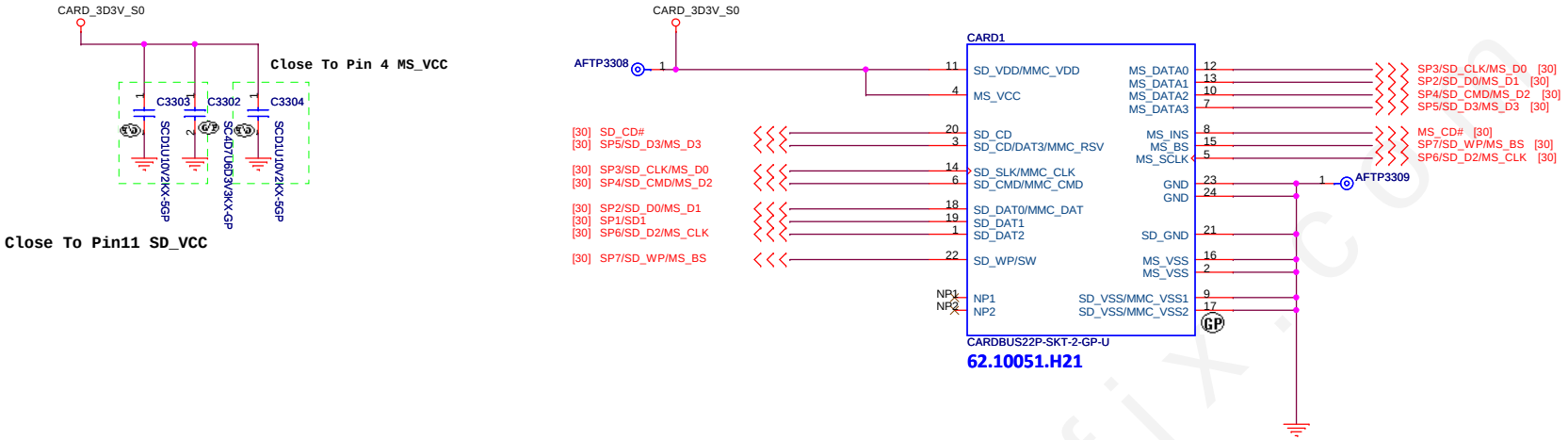
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

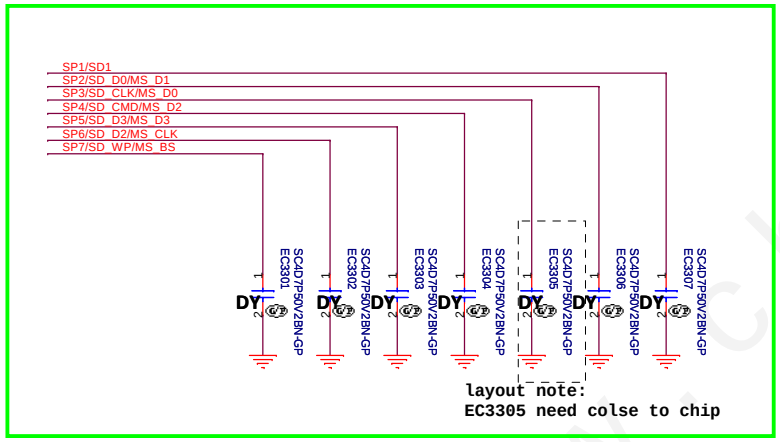
Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

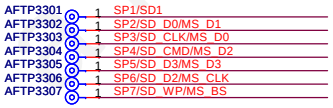
Date: Friday, June 21, 2013 | Sheet 32 of 101

SSID = SDIO



Reserve EMI Cap, 0107 CLK Cap DY





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

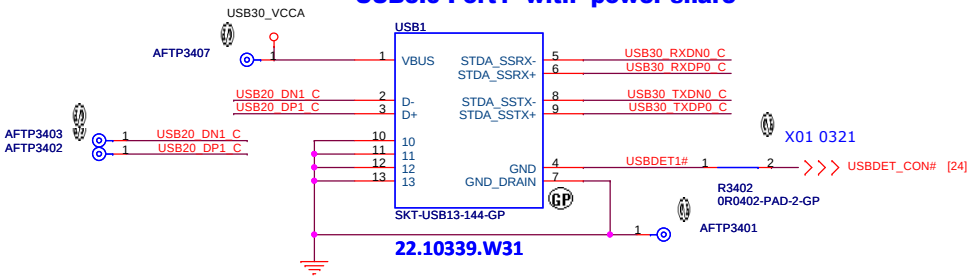
Title: Card Reader CONN

Size: A3 | Document Number: Hadley 15" | Rev: X02

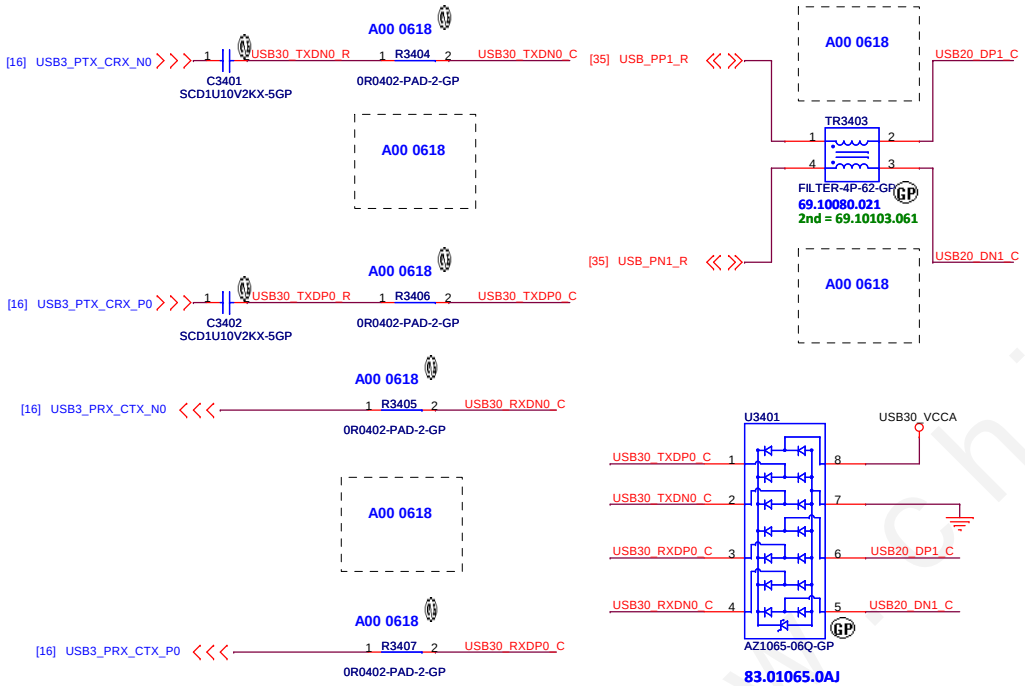
Date: Friday, June 21, 2013 | Sheet 33 of 101

SSID = USB

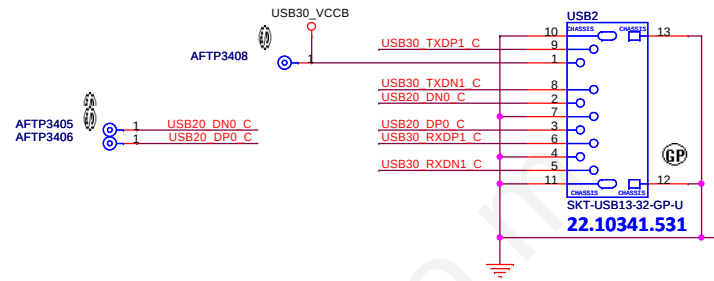
USB3.0 Port1 with power share



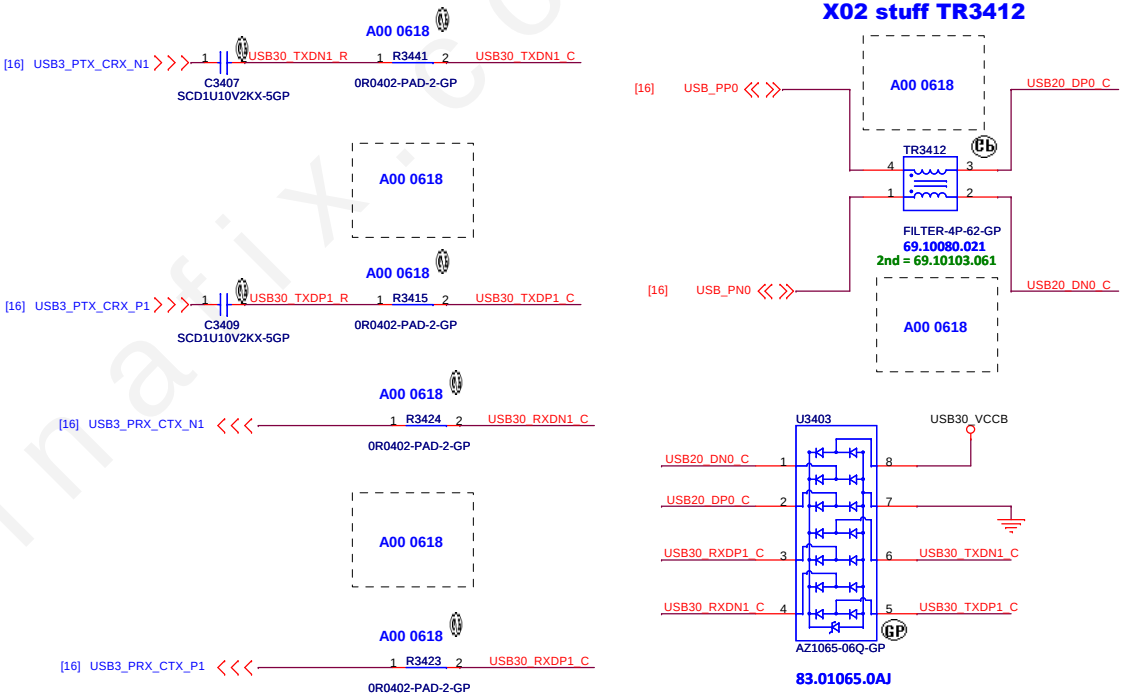
X02 stuff TR3403



USB3.0 Port2



X02 stuff TR3412

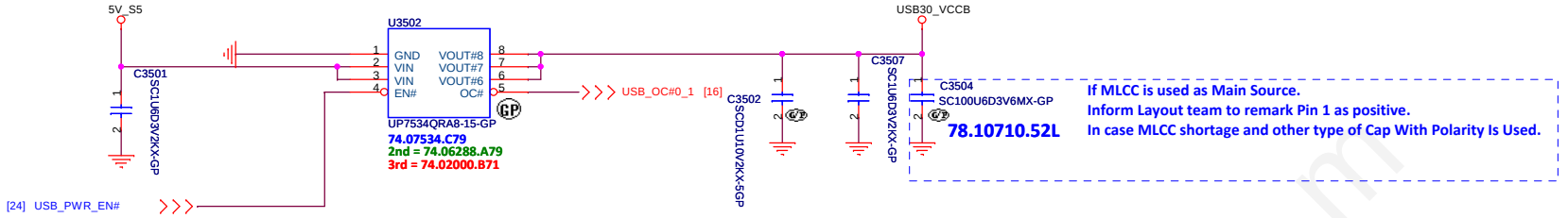


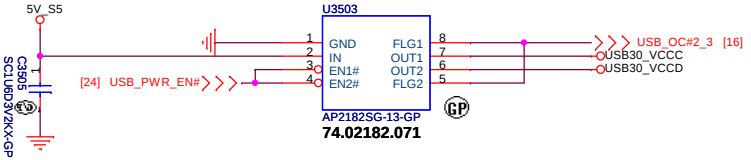
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB3.0(1)	
Size: A3	Document Number: Hadley 15"	Rev: X02
Date: Friday, June 21, 2013	Sheet 34 of 101	

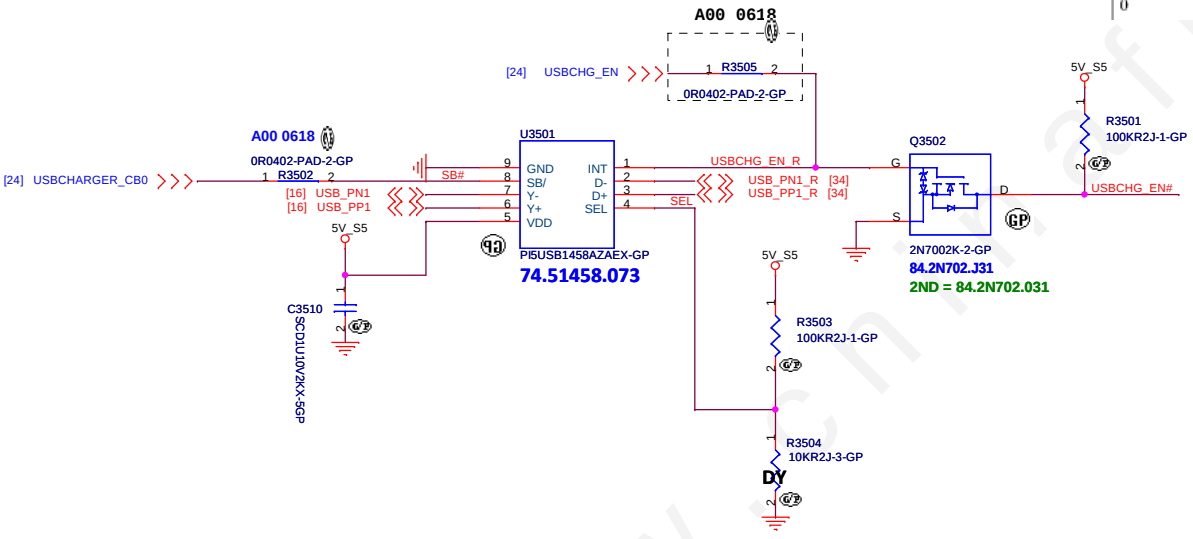
SSID = USB

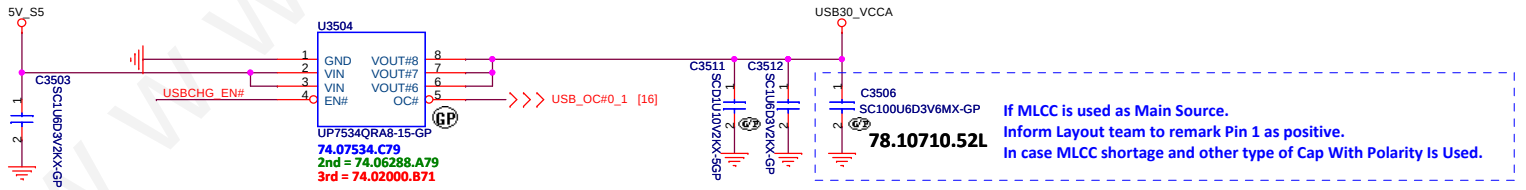




SB/ (pin 8)	SEL(pin 4)	Feature	pin 1 role (INT or INT/)
0	0	Auto S & C without mouse/keyboard pass through	INT or INT/
0	1	Auto S & C with mouse/keyboard pass through	INT or INT/
1	0	S0 charging with SDP only	INT or INT/
1	1	S0 charging with CDP or SDP only (depending on external device)	INT or INT/
0	M= (1/2)*V_{DD}	Test Mode, M = $V_{DD/2}$ = (1/2)*V_{DD}	

0319 modify USB Charger circuit





USB Power SW (U3504)

Vendor	Vendor P/N	Wistron P/N	Priority
Silergy	SY6288DCAC	74.06288.A79	1ST
DII (Diodes)	AP2301MPG-13	74.02301.071	2ND
GMT	G547I2P81U	74.00547.F79	3RD

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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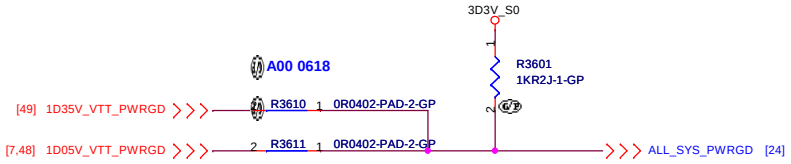
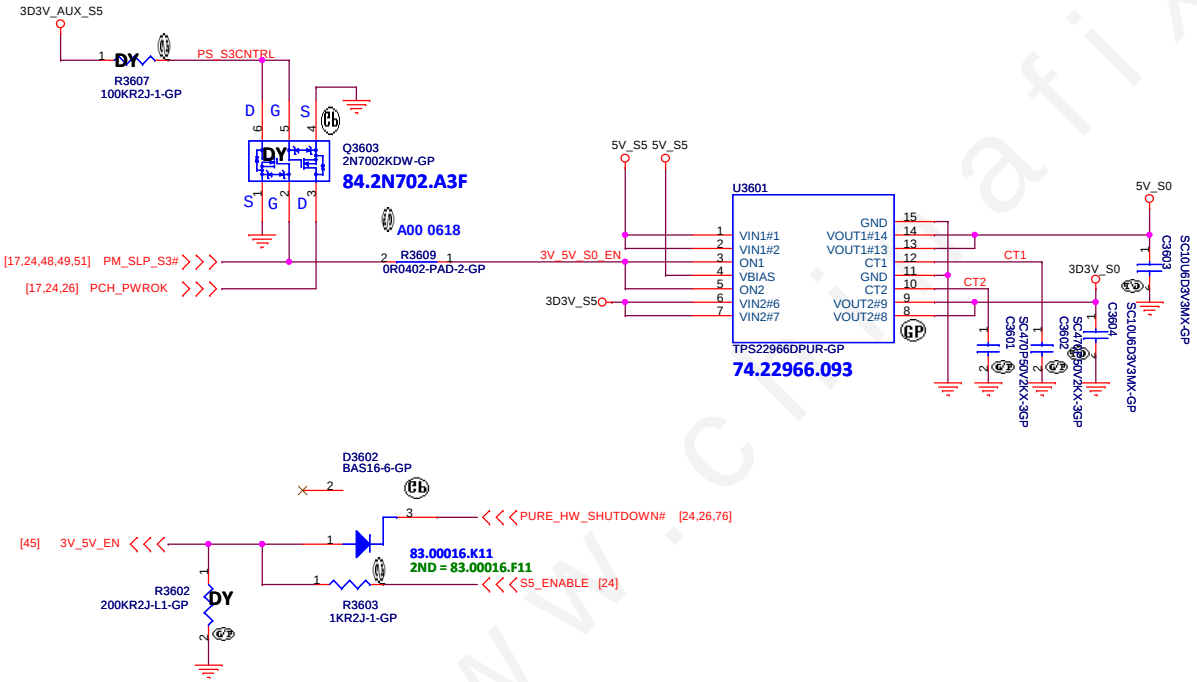
Title: USB Power SW
Size: | Document Number: Hadley 15" | Rev: X02
Date: Friday, June 21, 2013 | Sheet 35 of 101

SSID = Reset.Suspend

Power Good



ROSA Run Power



5V_S0

5V_S0 Comsumption
Peak current 4.033A

3D3V_S0

3D3V_S0 Comsumption
Peak current 3A

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

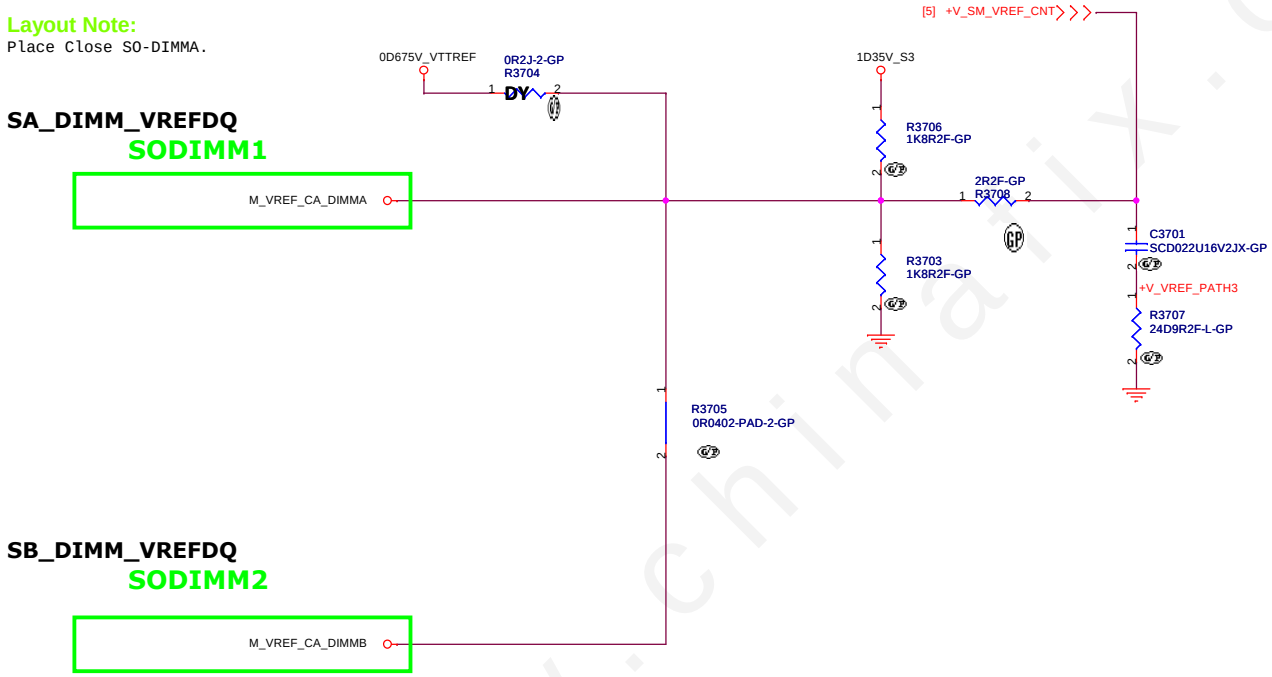
Title: *Power Plane Enable*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 21, 2013 | Sheet 36 of 101

SSID = Reset.Suspend

Layout Note:
Place Close SO-DIMMA.



Close to DIMM
S3 Power Reduction Circuit PM_DRAM_PWRGD

<Core Design>

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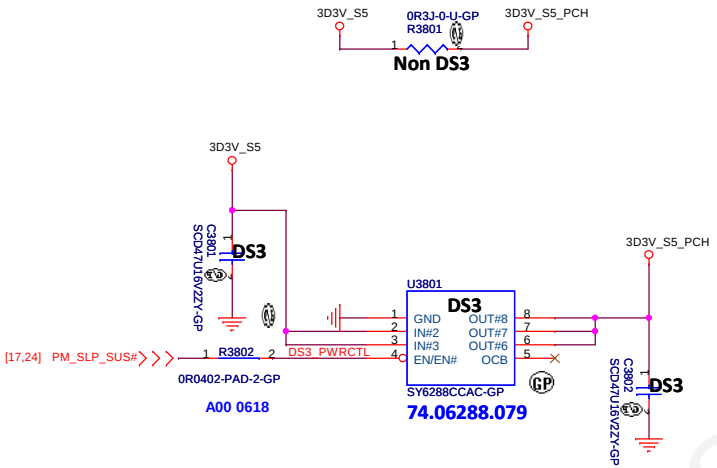
Title: S3 Power Reduction
Size: A3 | Document Number: Hadley 15" | Rev: X02
Date: Friday, June 21, 2013 | Sheet 37 of 101

SSID = Reset.Suspend



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
DSW		
Size: A3	Document Number: Hadley 15"	Rev: X02
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(Blanking)

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 21, 2013 | Sheet 39 of 101

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size	Document Number	Rev
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Date: Friday, June 21, 2013 Sheet 40 of 101

(Blanking)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 21, 2013 |

SSID = PWR.Support

0103 Add EC4203
ndde close to EL4202

Layout Note:
PSID Layout width > 25mil

A00 0618

A00 0619

DCIN1
ACES-CON5-27-GP
20.F2182.005

EC4203 SCD1U50V5JX-1-GP DY
EL4202 PAD-2P-4516-GP-U
AFTP4203
AFTP4204
AFTP4205
EC4201 SC10U25V5KX-GP DY
EC4202 SCD1U25V2KX-GP
EL4201 PAD-2P-4516-GP-U
EL4203 PAD-2P-4516-GP-U
JGND

PR4219 0R0603-PAD-2-GP-U
PS_ID_R
PS_ID_R2
PS_ID
PD4204 PESD24VS2UT-GP DY

PQ4201 FDV301N-NL-GP
84.00301.A31
2nd = 84.3K329.031

PR4202 15KR2F-GP
PR4211 100KR2J-1-GP
PQ3802_1
PMBS3904-1-GP PQ4202
84.03904.L06
2nd = 84.03904.P11
PR4203 10KR2J-3-GP
PSID_DISABLE#_R_C
PR4208 33R2J-2-GP DY
PR4207 33R2J-2-GP

5V_S5
3D3V_S5
PD4203 BAV99-12-GP
75.00099.E7D
2nd = 75.03101.07D
PR4206 2K2R2J-2-GP
PSID_EC [24]

PR4216 3K3R6J-GP
PQ4206_3
PR4214 100KR2J-1-GP
PQ4206 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
3rd = 84.2N702.E3F
4th = 84.2N702.F3F
AC_IN#_G
PR4215 100KR2J-1-GP
PR4212 1KR2J-1-GP
[24] AC_IN_KBC#
[24] PWR_CHG_AD_OFF

PD4201 1SMB22AT3G-GP-U1
83.22R03.03G
PQ4204 PDTC124EU-GP
84.00124.H1K
2nd = 84.05124.011
PQ4205 PDTA124EU-1-GP
84.00124.K1K
2nd = 84.05124.A11
AD_OFF_L
AD_OFF_R
PC4202 SCD1U25V3KX-GP
PR4210 47KR3J-L-GP

+DC_IN
PU4201 SI7121DN-T1-GE3-GP
AD+
PC4201 SC1U25V5KX-1GP
PR4209 240KR3-GP
PC4205 SCD01U50V2KX-1GP
PC4206 SC10U25V5KX-GP

Id=-9.6A
Qg=-25nC
Rdson=18~30mohm

DT MODE
PWR_CHG_AD_OFF_R

PC4208 SC1U25V3KX-1-GP DY
PQ4208 2N7002K-2-GP
84.2N702.J31
PQ3808D
PQ3808G
PR4217 1KR2J-1-GP DY
PC4209 SCD01U50V2KX-1GP DY

PR4213 10KR2J-3-GP DY
PQ4203 DMN66D0LDW-7-GP
PR4218 100KR2J-1-GP DY
PQ3807D DY
PC4207 SC1U6D3V2ZY-GP
[4,24,44,46] H_PROCHOT#
BAT_IN#
BAT_IN# [24,43,44]

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: DCIN
Size: A3
Document Number: Hadley 15"
Rev: X02
Date: Friday, June 21, 2013
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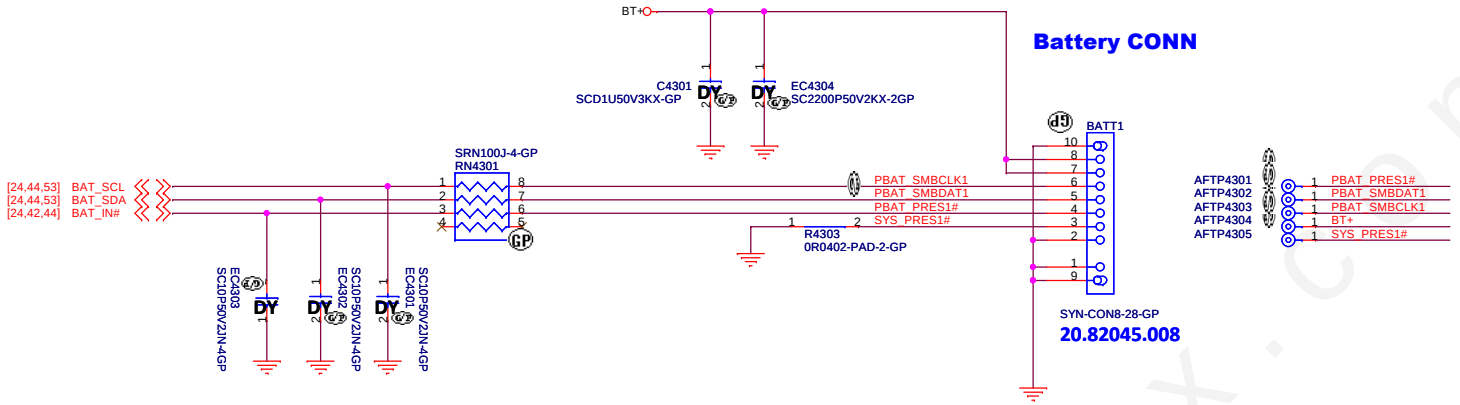
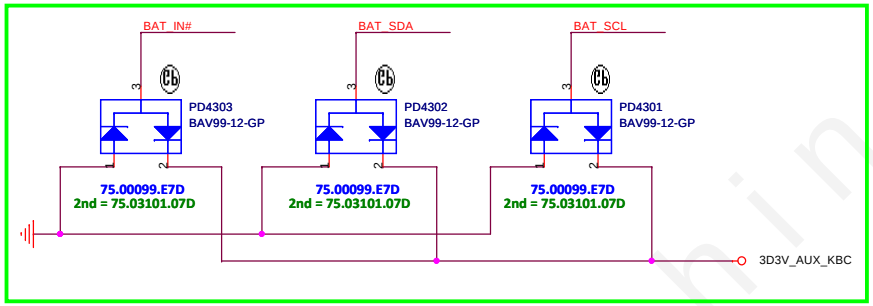
SSID = PWR.Support



0109 DY PD4301~4303



Layout Note:
Place near Battery CONN

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: BATT CONN

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 21, 2013 Sheet 43 of 101

SSID = Charger

KBC FOR DT MODE
CHECK EE PULL HIGH

VacDET=2.4V
Acok setting=2.4*((PR4444+PR4411)/PR4411)
Setting=18.178v

PU4406 and PU4407:
main source: 84.03660.037

ZZ.00215.037

DIS_DTM:
H= cell is plus to GND. (reset charger ic)
L=nornal

Follow custormer circuits

ACAV_IN
H=ACIN
L=UNAC

Follow custormer circuits

Close PR4443

PWR_CHG_ACOK:
PWR_CHG_REGN=6V
V+=6*(PR4404/(PR4410+PR4404))=3.27V

PWR_CHG_CMPIN:
V-=3.3*(PR4402/(PR4428+PR4402))=1.1099V

CHECK EE

CHECK PM BATTERY TYPE
CHECK CELL for DT mode

BATTERY MON

CHECK PM ADAPTER TYPE
And setting adapter type

DIS_DTM_HW:
PWR_CHG_REGN=6V
V+=6*(PR4440/(PR4441+PR4440))=3.27V
Setting=3.27*((PR4442+PR4447)/PR4447)=9V

(AD_IA_HW)

(AD_IA_HW_2)

ADAPTER TYPE	AD_IA_HW	AD_IA_HW_2	SETTING
90W	L	L	1.099V
65W	H	L	0.862329V
45W	L	H	0.659648V

CHECK EE
follow custormer circuits.

<Core Design>

Wistron Corporation
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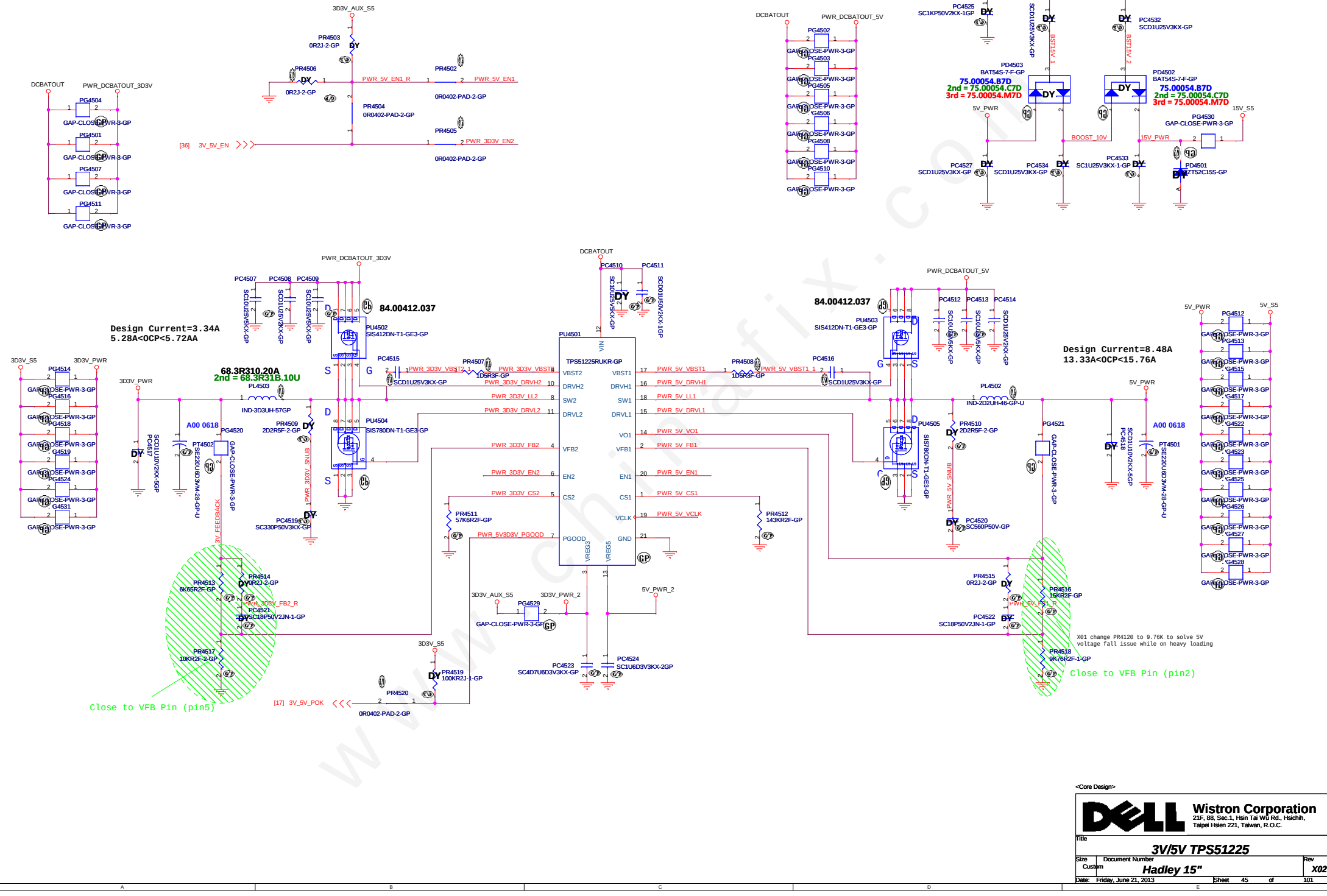
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGE(BQ24715)

Size: Custom | Document Number | Rev: X02

Date: Friday, June 21, 2013 | Sheet 44 of 101

SSID = PWR.Plane.Regulator_5v3p3v



<Core Design>

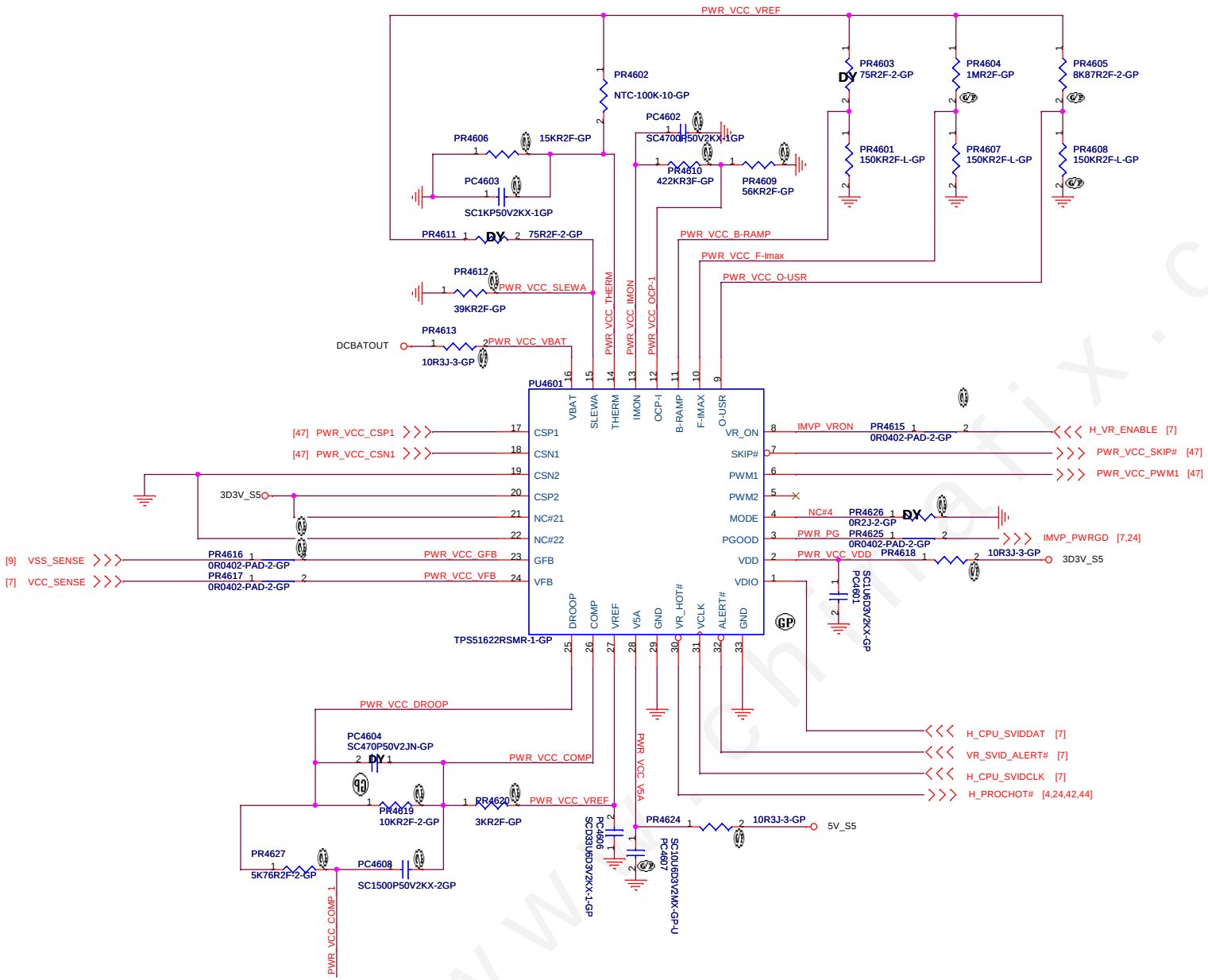
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

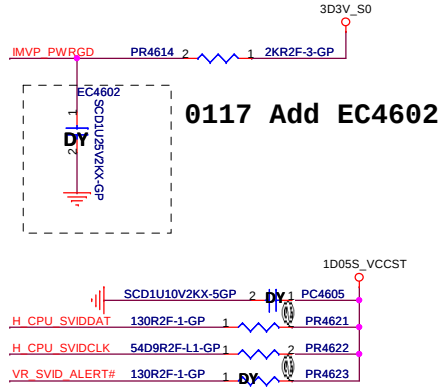
Title: 3V/5V TPS51225

Size: Custom | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 21, 2013 | Sheet 45 of 101

SSID = CPU.Regulator





		28W	15W
Fsw	PR4604	392K	1M
Fsw	PR4607	75K	150K
OCP	PR4609	150k	75K
IMON	PR4610	680K	422K
Load line	PR4620	2.8K	3K

<Core Design>

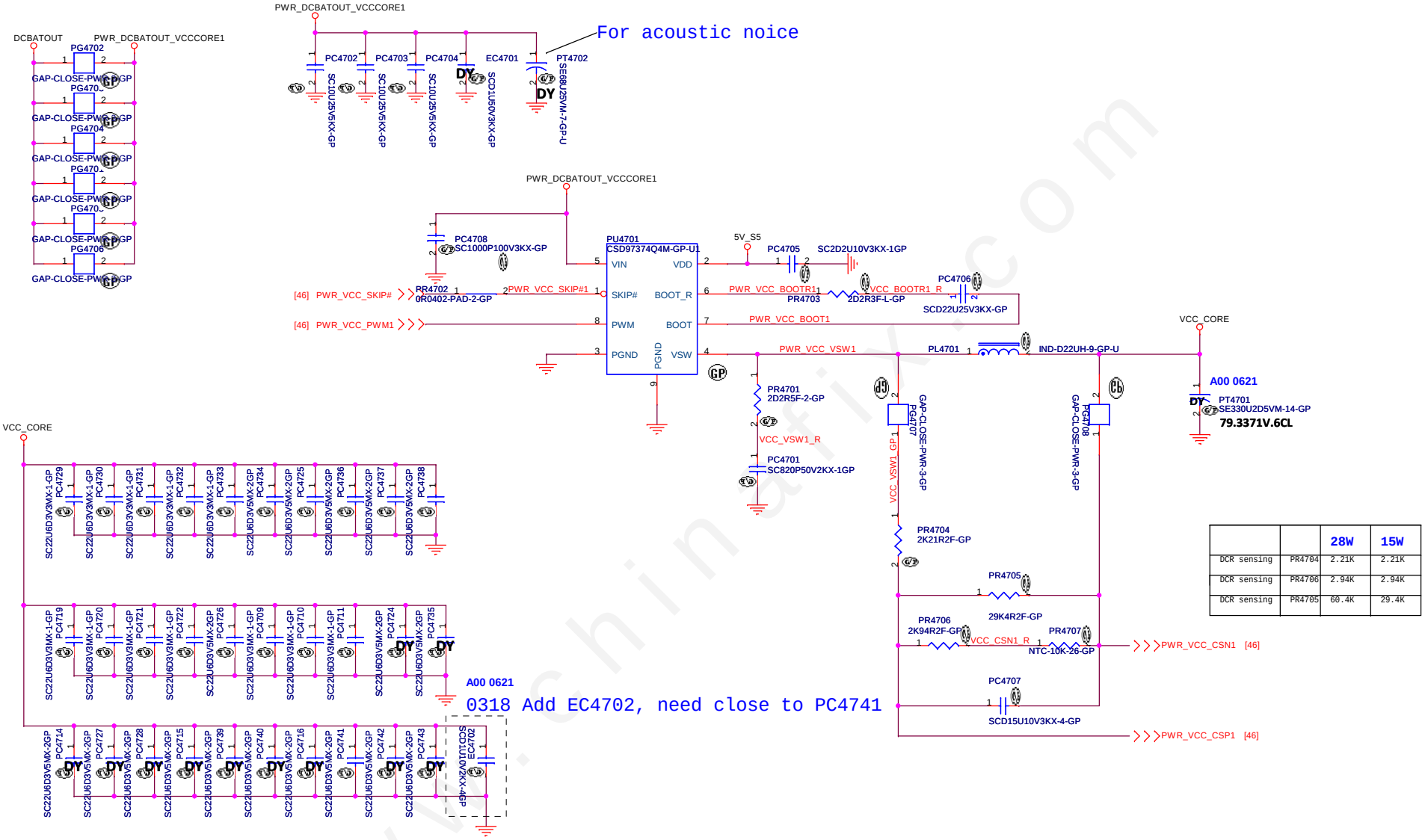
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51622 CPUCORE(1/2)

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 21, 2013 | Sheet 46 of 101

SSID = CPU.Regulator



		28W	15W
DCR sensing	PR4704	2.21K	2.21K
DCR sensing	PR4706	2.94K	2.94K
DCR sensing	PR4705	60.4K	29.4K

<Core Design>

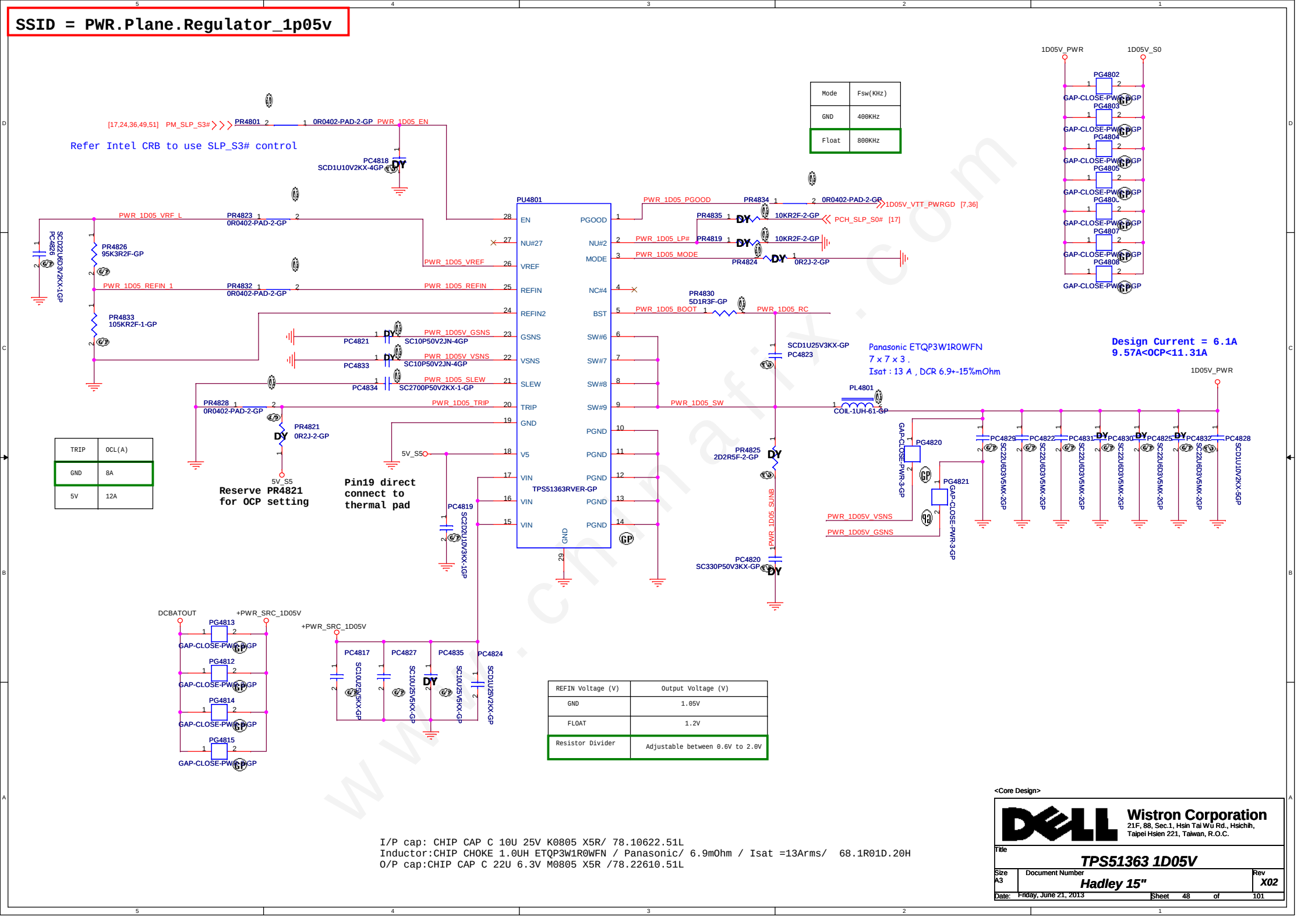
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51622 CPUCORE(2/2)

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 21, 2013 | Sheet 47 of 101

SSID = PWR.Plane.Regulator_1p05v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor:CHIP CHOKE 1.0UH ETQP3W1R0WFN / Panasonic/ 6.9mOhm / Isat =13Arms/ 68.1R01D.20H
O/P cap:CHIP CAP C 22U 6.3V M0805 X5R /78.22610.51L

<Core Design>

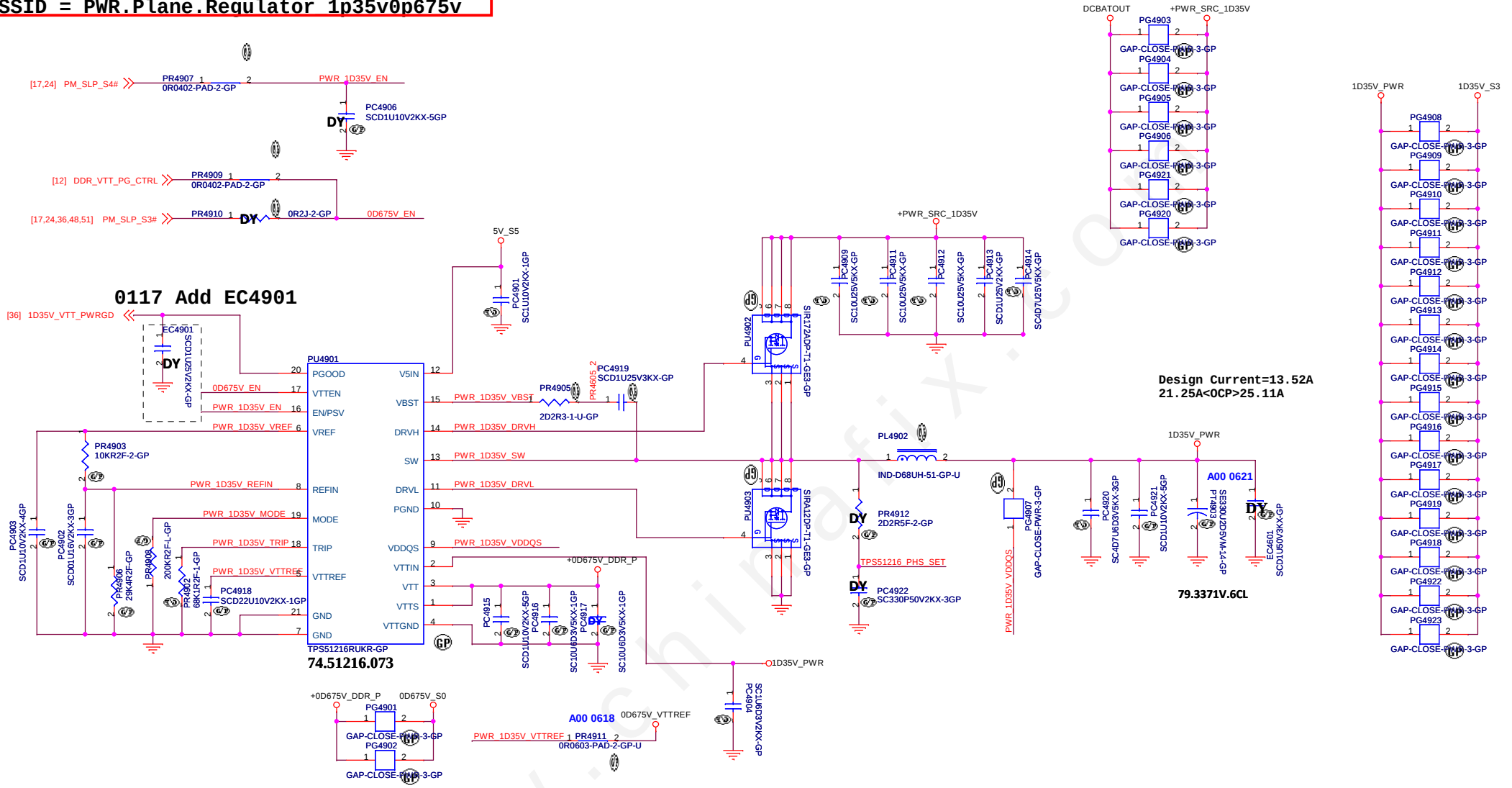
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51363 1D05V

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 21, 2013 Sheet 48 of 101

SSID = PWR.Plane.Regulator_1p35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE

PR4608	Frequency	Discharge Mode
200k ohm	400kHz	Tracking Discharge
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 1.0UH PCMB104T-1R0M/ 3.3mohm/ Isat =28A rms /68.1R01C.10Q
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S: SIR172ADP-T1-GE3 / 8.5mohm/10.5mOhm@4.5Vgs/ 84.00172.A37
L/S: SIRA12DP-T1-GE3 / 4.4mohm/6mOhm@4.5Vgs/ 84.SRA12.037

M14 DIS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51216_+1.35V_SUS

Size	Document Number	Rev
A3	Hadley 15"	X02

Date: Friday, June 21, 2013 Sheet 49 of 101

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

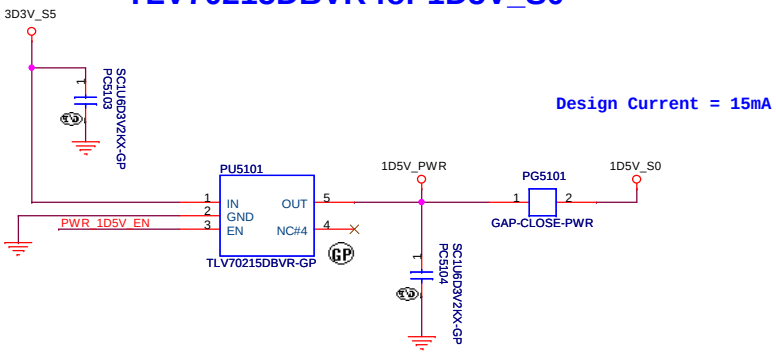
Title: *(Reserved)TPS51312 1D8V*

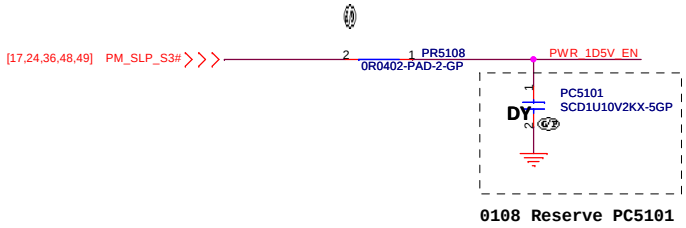
Size	Document Number	Rev
A3	*Hadley 15"*	*X02*

Date: Friday, June 21, 2013 Sheet 50 of 101

SSID = PWR.Plane.Regulator_1p5v

TLV70215DBVR for 1D5V_S0





0108 Reserve PC5101

<Core Design>

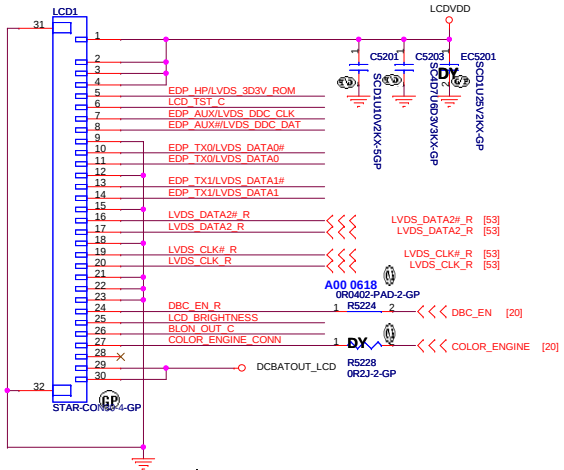
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *RT9198-15PU5R_1D5V*

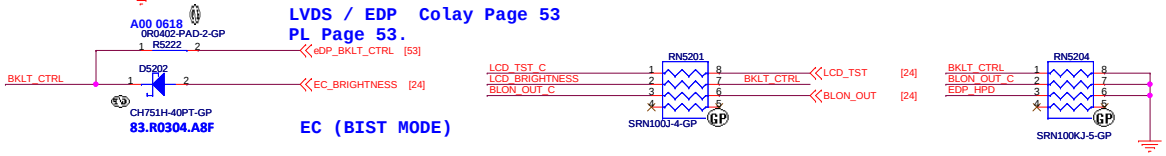
Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 21, 2013 | Sheet 51 of 101

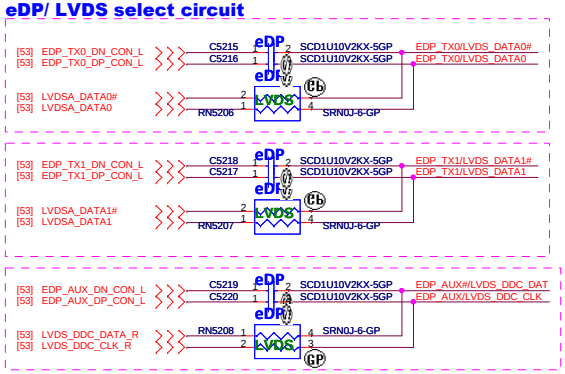
SSID = VIDEO



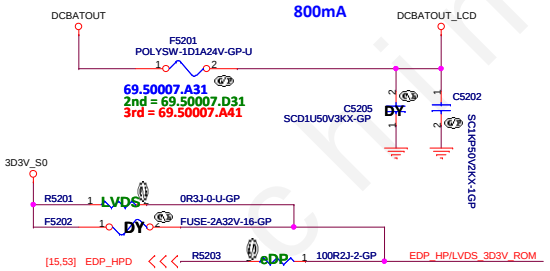
Pin	eDP	LVDS	Pin	eDP	LVDS
1	LCDVDD	LCDVDD	16	NC	LVDS_DATA2#
2	LCDVDD	LCDVDD	17	NC	LVDS_DATA2
3	LCDVDD	LCDVDD	18	GND	GND
4	LCDVDD	LCDVDD	19	NC	LVDS_CLK#_R
5	EDP_HP	3D3V_ROM	20	NC	LVDS_CLK_R
6	LCD_TST_C	LCD_TST_C	21	GND	GND
7	EDP_AUX	LVDS_DDC_CLK	22	GND	GND
8	EDP_AUX#	LVDS_DDC_DAT	23	GND	GND
9	GND	GND	24	DBC_EN	DBC_EN
10	EDP_TX0N	LVDS_DATA0#	25	BRIGHTNESS	BRIGHTNESS
11	EDP_TX0P	LVDS_DATA0	26	BLON_OUT	BLON_OUT
12	GND	GND	27	Color_Engine	Color_Engine
13	EDP_TX1N	LVDS_DATA1#	28	NC	NC
14	EDP_TX1P	LVDS_DATA1	29	DCBATOUT_LCD	DCBATOUT_LCD
15	GND	GND	30	DCBATOUT_LCD	DCBATOUT_LCD



eDP/ LVDS select circuit

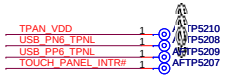


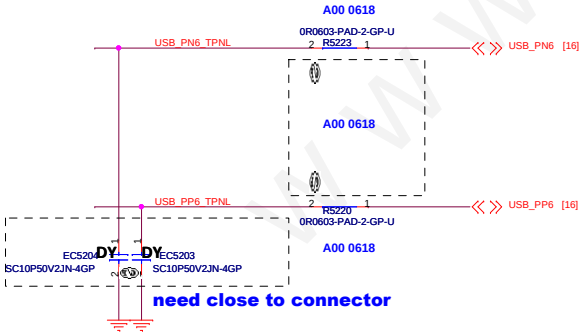
INVERTER POWER



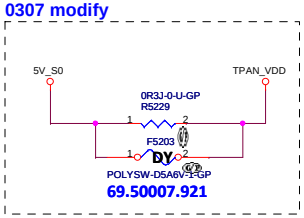
Touch panel

X02 remove TPNL1

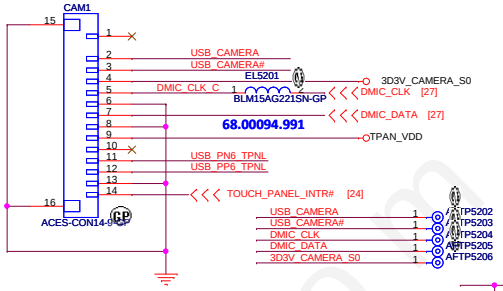




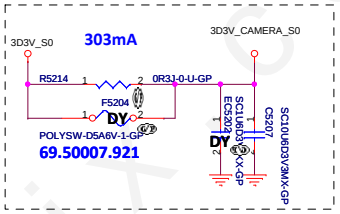
0307 modify



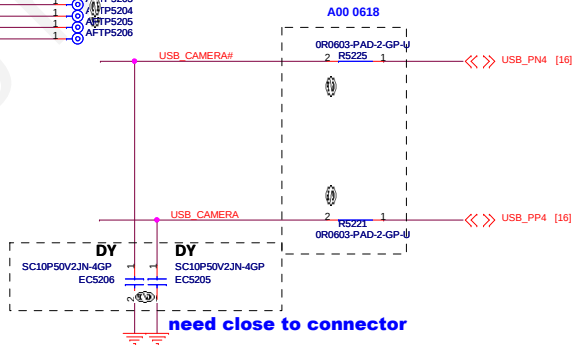
X02 change CAM1 connector



Camera Power

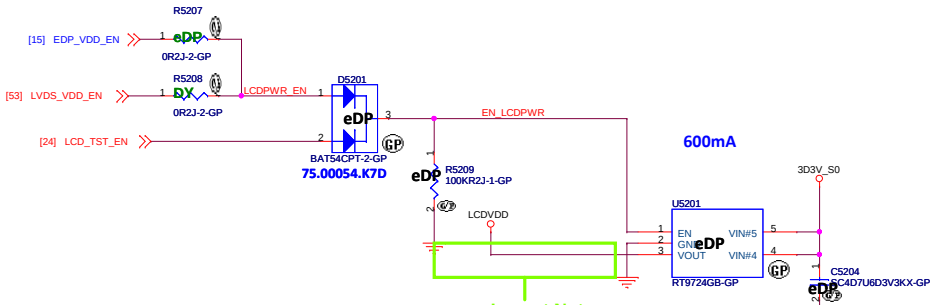


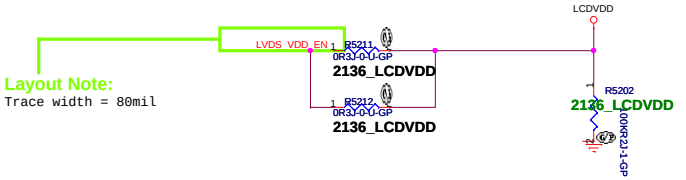
CAMERA



LCDVDD

LCD Power





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LCD Connector

Size	Document Number	Rev
Custom	Hadley 15"	X02

Date: Friday, June 21, 2013 Sheet 52 of 101

SSID = VIDEO

LVDS & EDP Colay

Layout Note:
Place near U5301

[8] EDP_TX1_DN
[8] EDP_TX1_DP
C5209 SCD1U10V2KX-5GP EDP_TX1_DN_RTS2136
C5210 SCD1U10V2KX-5GP EDP_TX1_DP_RTS2136
RN5303 SRN0J-6-GP
EDP_TX1_DN_CON_L
EDP_TX1_DP_CON_L
EDP_TX1_DN_CON_L [52]
EDP_TX1_DP_CON_L [52]

[8] EDP_TX0_DN
[8] EDP_TX0_DP
C5211 SCD1U10V2KX-5GP EDP_TX0_DN_RTS2136
C5212 SCD1U10V2KX-5GP EDP_TX0_DP_RTS2136
RN5301 SRN0J-6-GP
EDP_TX0_DN_CON_L
EDP_TX0_DP_CON_L
EDP_TX0_DN_CON_L [52]
EDP_TX0_DP_CON_L [52]

[8] EDP_AUX_DN
[8] EDP_AUX_DP
C5213 SCD1U10V2KX-5GP EDP_AUX_DN_RTS2136
C5214 SCD1U10V2KX-5GP EDP_AUX_DP_RTS2136
RN5304 SRN0J-6-GP
EDP_AUX_DN_CON_L
EDP_AUX_DP_CON_L
EDP_AUX_DN_CON_L [52]
EDP_AUX_DP_CON_L [52]

Brightness

[15] L_BKLT_CTRL
R5319 0R2J-2-GP 2136_PWM_IN
R5320 0R2J-2-GP eDP_BKLT_CTRL
eDP_BKLT_CTRL [52]
R5302 1KR2J-1-GP
[15,52] EDP_HPD
EDP_HPD_RTS2136

3D3V_S0
L5301 MPZ1608S600AT-GP 68.00212.011
DP_AVCC33
C5312 SCD1U10V2KX-5GP
C5302 SC10U6D3V3MX-GP
C5303 SCD1U10V2KX-5GP

3D3V_S0
L5302 MPZ1608S600AT-GP 68.00212.011
DP_DVCC33
C5317 SCD1U10V2KX-5GP
C5302 SC10U6D3V3MX-GP
C5313 SCD1U10V2KX-5GP

L5303 IND-4D7UH-300-GP
SWR_LX
SWR_V12
2136_SW
A00 0618
0R0603-PAD-2-GP-U
R5314
C5305 SC10U6D3V3MX-GP
C5306 SCD1U10V2KX-5GP

X02 change to 4P2R

RN5306 SRN100KJ-6-GP
TEST_MODE
2136_PWM_IN

SWR_V12
C5311 SCD1U10V2KX-5GP
[24] LVDS_R2136_BKLT_EN
[52] LVDS_DDC_DATA_R
[52] LVDS_DDC_CLK_R
LVDS_DDC_DATA_R
LVDS_DDC_CLK_R
EEPROM_SDA0
EEPROM_SCL0

LVDSA_DATA0# [52]
LVDSA_DATA0 [52]
LVDSA_DATA1# [52]
LVDSA_DATA1 [52]
LVDS_DATA2#_R [52]
LVDS_DATA2_R [52]

U5301 RTD2136R-CGT-GP 71.02136.B03

GND	49
MODE_CFG1	48
MODE_CFG0	47
MISCSCL	46
MISCSDA	45
BL_EN	44
VCCK	43
TXO0-	42
TXO0+	41
TXO1-	40
TXO1+	39
TXO2-	38
TXO2+	37
HPD	1
TEST	2
AUX_N	3
AUX_P	4
DP_V33	5
DP_GND	6
LANE0_P	7
LANE0_N	8
LANE1_P	9
LANE1_N	10
DP_V12	11
DP_REXT	12
TXOC-	36
TXOC+	35
TXO3-	34
TXO3+	33
TXE0-	32
TXE0+	31
TXE1-	30
TXE1+	29
TXE2-	28
TXE2+	27
TXEC-	26
TXEC+	25
CIICSCL	13
CIICSDA	14
SWR_VCCK	15
SWR_GND	16
SWR_LX	17
SWR_VDD	18
PWM_OUT	19
PANEL_VCC	20
PWM_IN	21
PVCC	22
TXE3+	23
TXE3-	24

LVDS_CLK#_R [52]
LVDS_CLK_R [52]

EDP_HPD_RTS2136
TEST_MODE
EDP_AUX_DN_RTS2136
EDP_AUX_DP_RTS2136
DP_AVCC33
EDP_TX0_DP_RTS2136
EDP_TX0_DN_RTS2136
EDP_TX1_DP_RTS2136
EDP_TX1_DN_RTS2136
SWR_V12
DP_REXT
R5301 12KR2F-L-GP
C5310 SCD1U10V2KX-5GP

Close to PIN5

DP_AVCC33
C5316 SCD1U10V2KX-5GP

CIICSCL1
CIICSDA1
SWR_V12
SWR_LX
DP_DVCC33
C5309 SCD1U10V2KX-5GP
[52] eDP_BKLT_CTRL
[52] LVDS_VDD_EN
2136_PWM_IN

DP_DVCC33
C5308 SCD1U10V2KX-5GP
C5307 SC10U6D3V3MX-GP

Close to PIN13

3D3V_S0
R5306 4K7R2J-2-GP
R5317 4K7R2J-2-GP
EEPROM_SCL0
EEPROM_SDA0
R5318 4K7R2J-2-GP
R5307 4K7R2J-2-GP

Operation Mode Table

		PIN47	
		0	1
PIN48	0	X	EP Mode
	1	ROM	EEPOOM

RN5301 SRN4K7J-10-GP
LVDS_DDC_DATA_R
LVDS_DDC_CLK_R
3D3V_S0
CIICSDA1
CIICSCL1
Q5301 2N7002KDW-GP
84.2N702.A3F
2nd = 84.DM601.03F
3rd = 84.2N702.E3F
4th = 84.2N702.F3F
CIICSDA
CIICSCL
RN5307 SRN0J-6-GP
SML0_DATA [18]
SML0_CLK [18]
PCH
PCH
RN5305 SRN0J-6-GP
BAT_SDA [24,43,44]
BAT_SCL [24,43,44]
KBC
KBC

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LVDS_Switch
Size: Custom
Document Number: Hadley 15"
Rev: X02
Date: Friday, June 21, 2013
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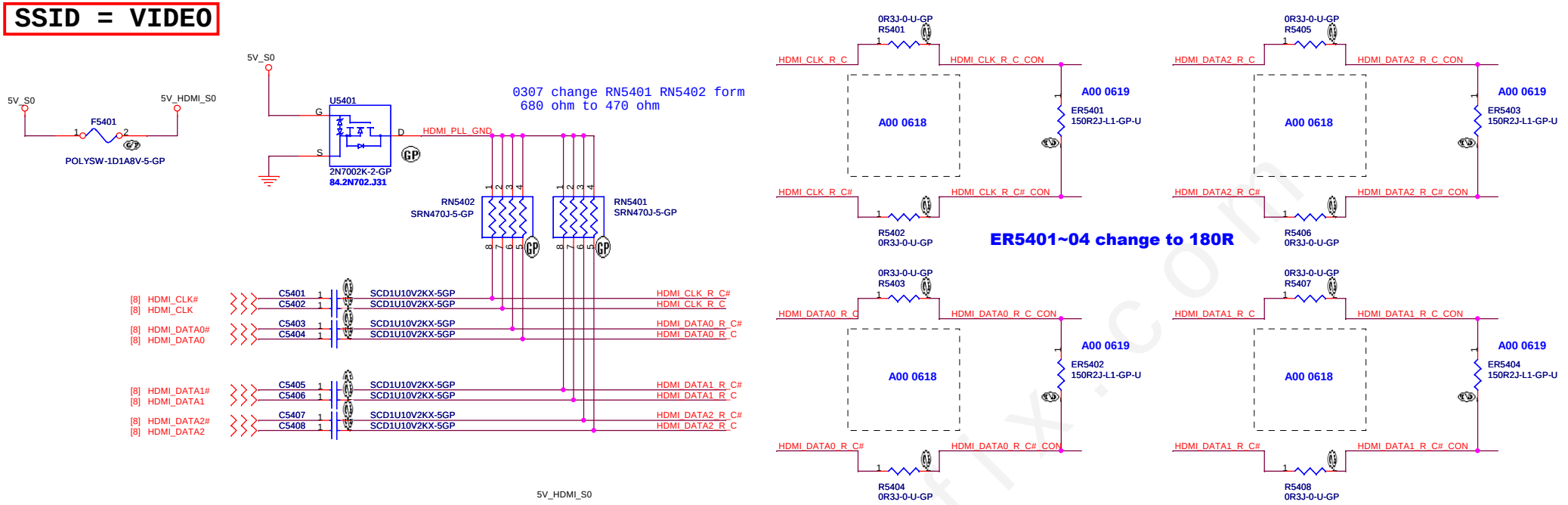
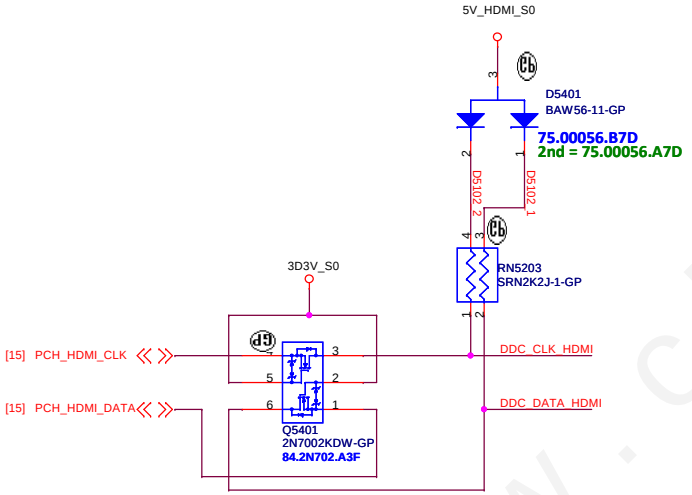
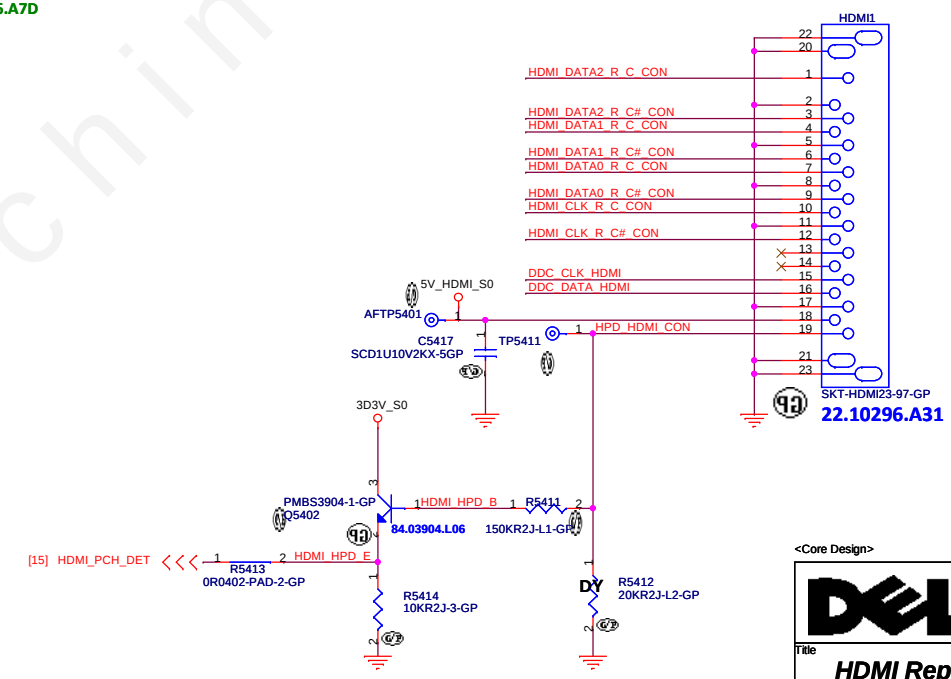
SSID = VIDEO



ER5401~04 change to 180R



HDMI CONN



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDMI Repeater/Connector

Size	Document Number	Rev
A3	Hadley 15"	X02

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<Core Design>

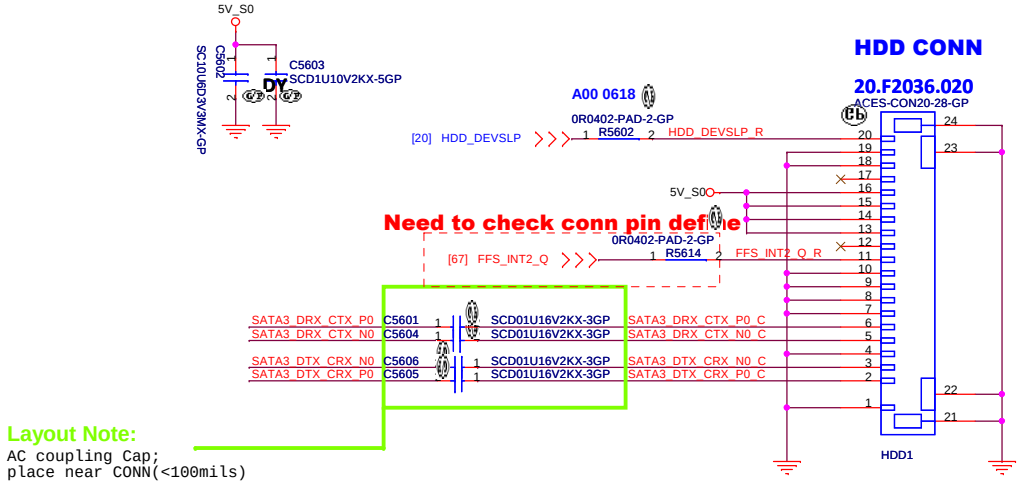
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 21, 2013 | Sheet 55 of 101

SSID = SATA



Layout Note:

AC coupling Cap;
place near CONN(<100mils)

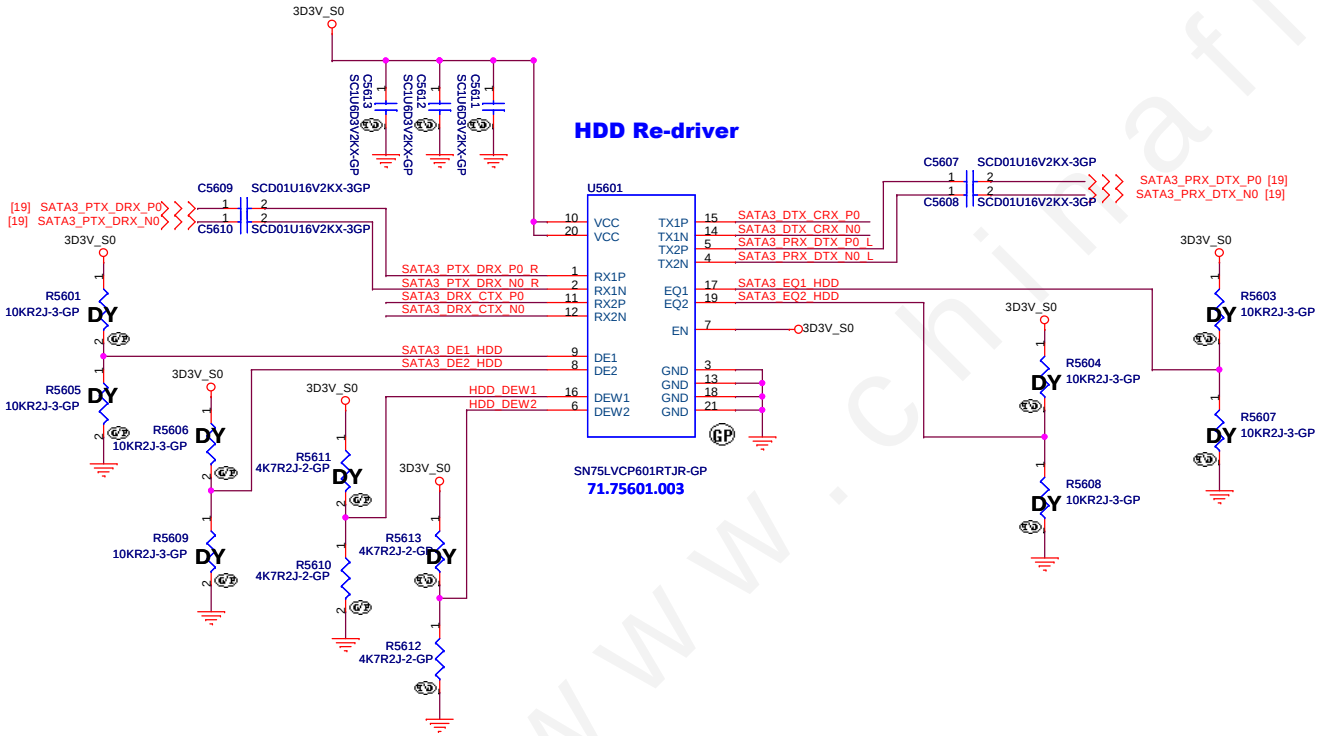


Table 1: Tx/Rx EQ & DE Pulse Width Settings

DE1/DE2	CH1/CH2De-Emphasis dB(@6Gbps
NC (*default*)	-6
0	0
1	-3

EQ1/EQ2	CH1/CH2Equalization dB (@6Gbps)
NC (*default*)	0
0	7
1	14

DEW1/DEW2	Device Function→ DE Width for CH1/CH2
0	De-Emphasis Pulse Width Short (recommended setting when link operates at SATA 1.5/3.0/6.0 Gbps)
1 (*default*)	De-Emphasis Pulse Width Long (recommended setting when link operates at SATA 1.5/3.0 Gbps speed only)

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *HDD*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 21, 2013 | Sheet 56 of 101

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<Core Design>

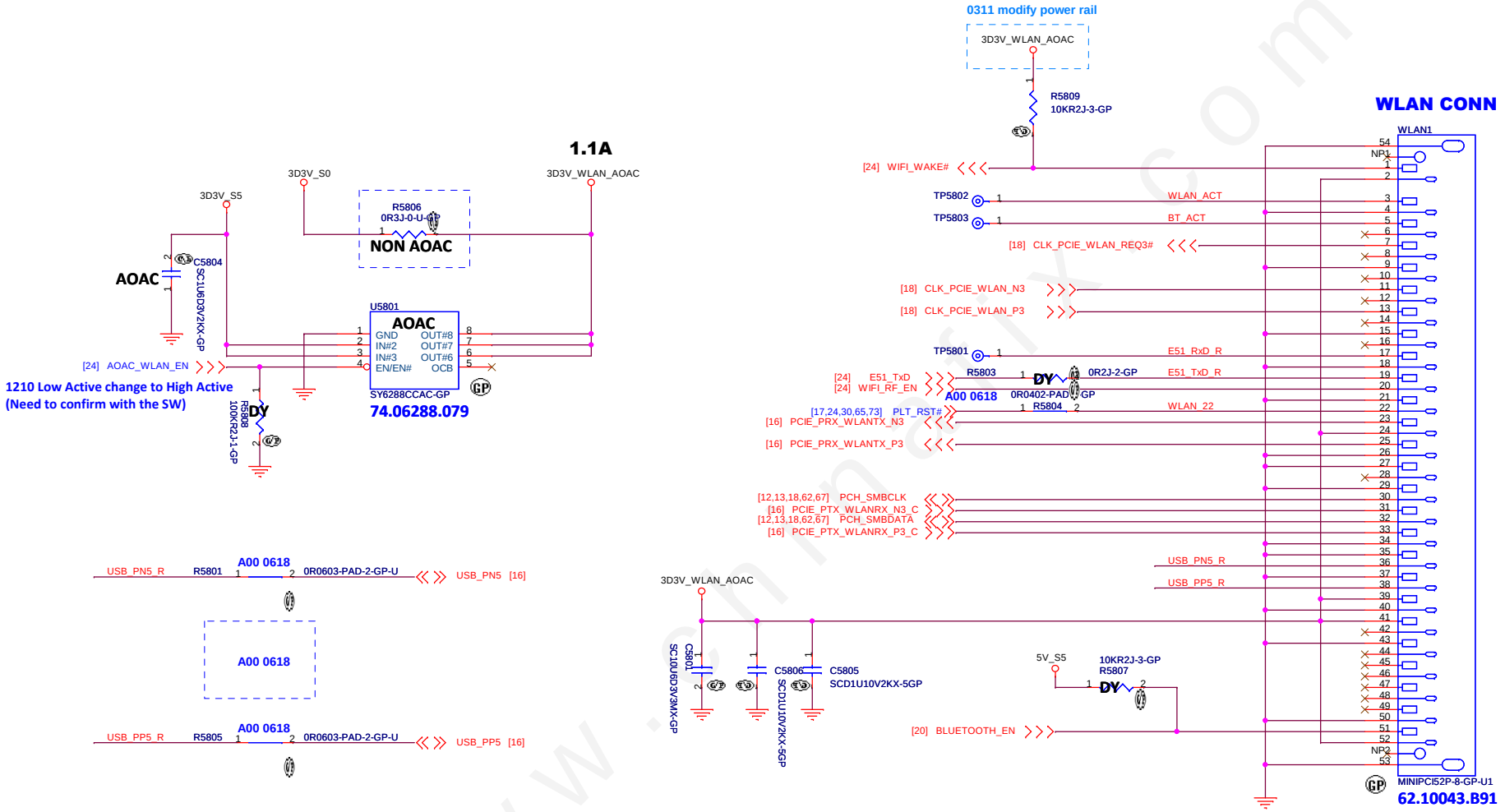
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 21, 2013 | Sheet 57 of 101

SSID = Wireless



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: WLAN/BT

Size	Document Number	Rev
A3	Hadley 15"	X02

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 21, 2013 | Sheet 59 of 101

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

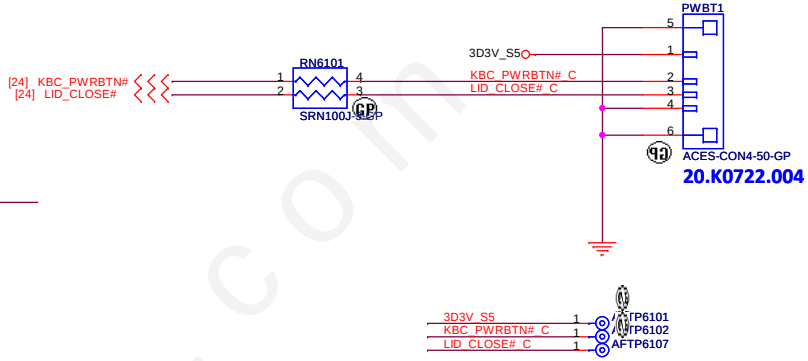
Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 21, 2013 | Sheet 60 of 101

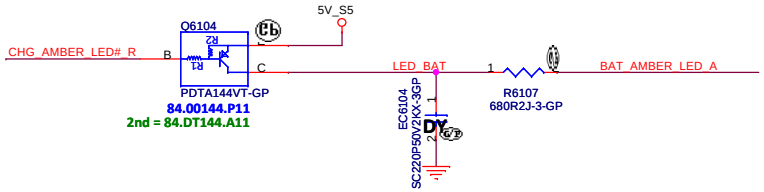
SSID = User.Interface

PWRBTN CONN



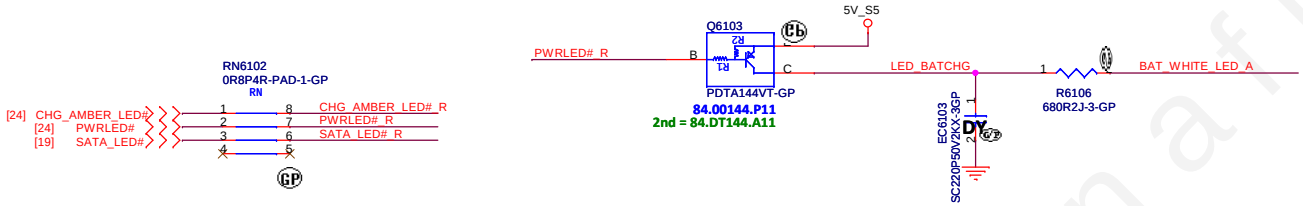
Battery LED1(Amber_LED)

LOW actived from KBC GPIO

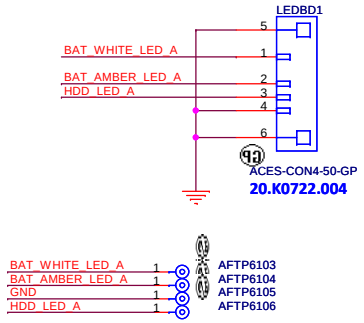


Power & Battery LED2(White_LED)

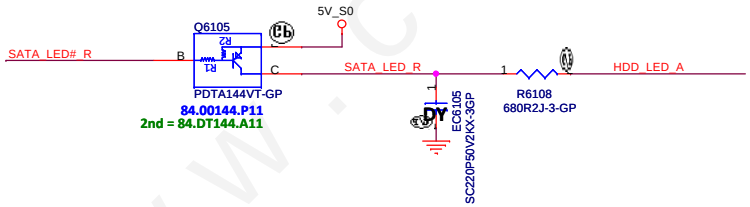
LOW actived from KBC GPIO



LED board CONN



SATA HDD LED



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

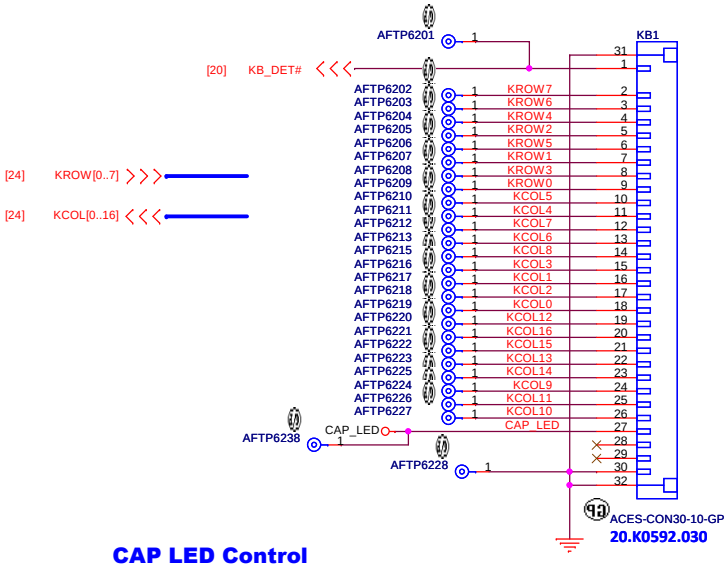
Title: LED Bar/Power Button

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 21, 2013 | Sheet 61 of 101

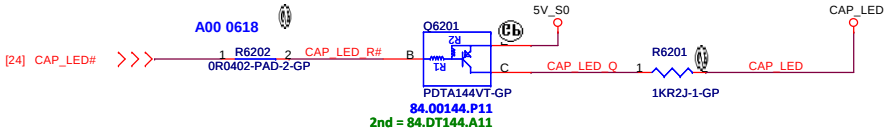
SSID = KBC

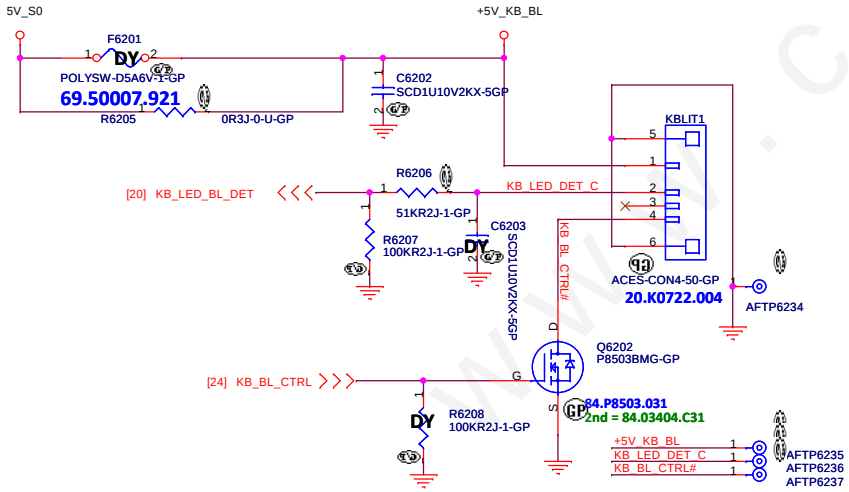
Internal Keyboard Connector



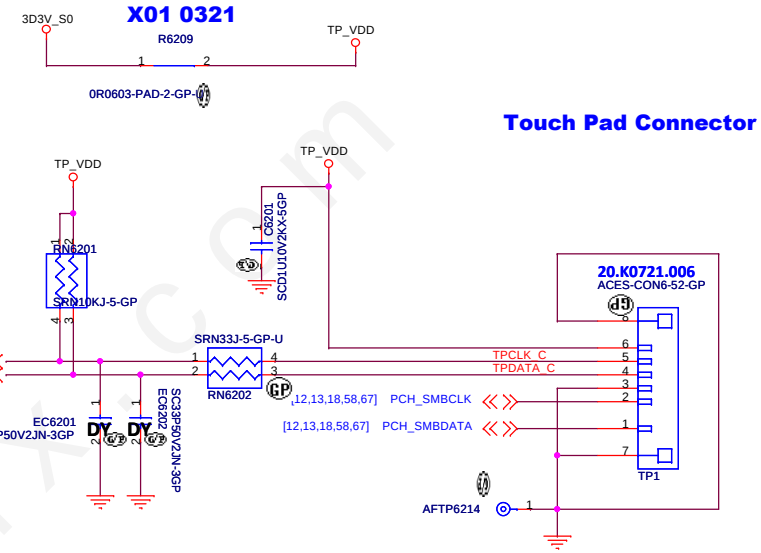
CAP LED Control

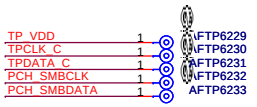
LOW actived from KBC GPIO





SSID = Touch.Pad





<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	Reserved	
Size: A3	Document Number: Hadley 15"	Rev: X02
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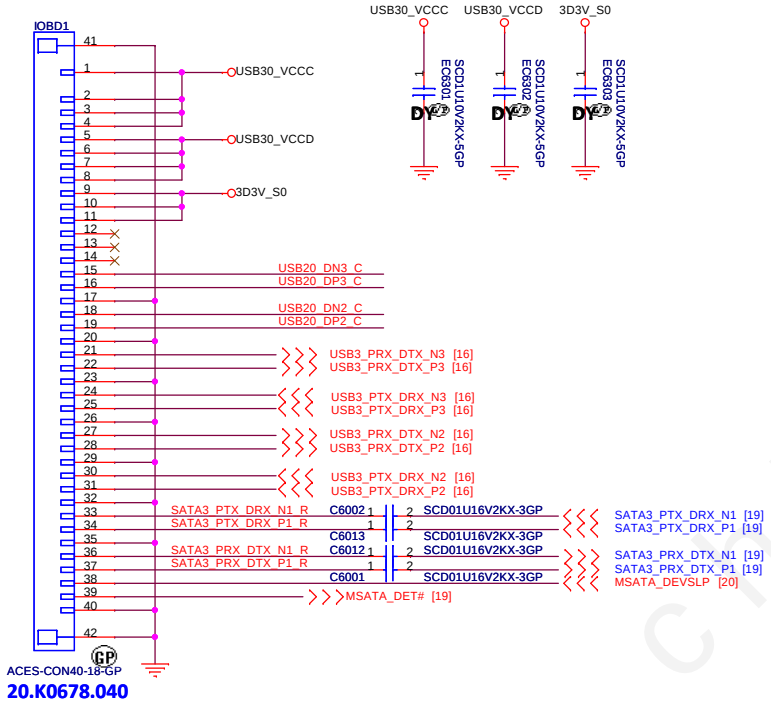
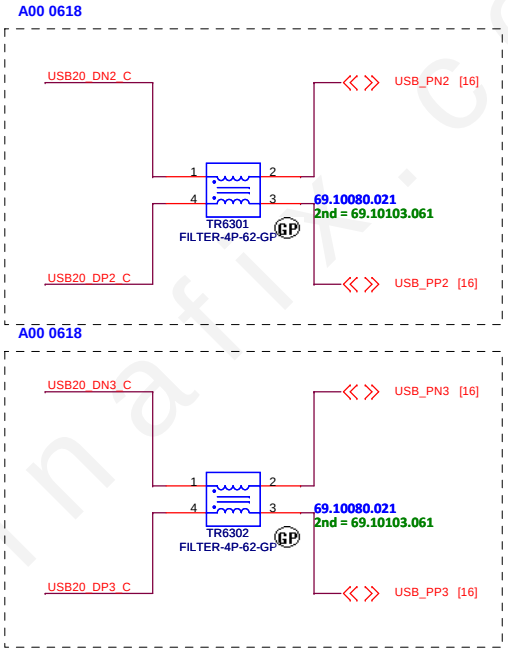
SSID = User.Interface





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: IO Board Connector

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 21, 2013 | Sheet 63 of 101

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

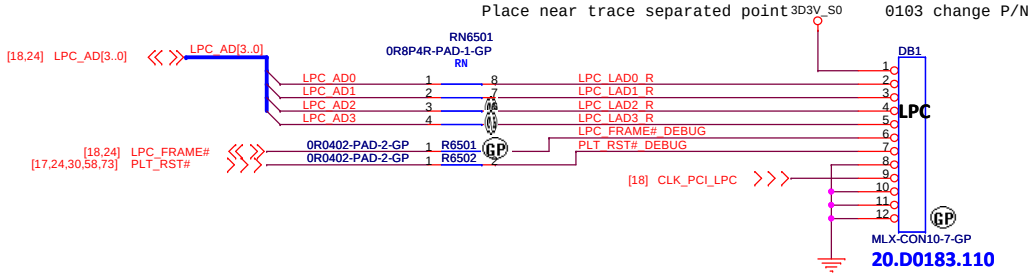
Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 21, 2013 | Sheet 64 of 101

SSID = DEBUG PORT

Debug Connector



<Core Design>

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Title: *Dubug connector*		
Size: A3	Document Number: *Hadley 15"*	Rev: *X02*
Date: Friday, June 21, 2013	Sheet 65 of 101	

(Blanking)

<Core Design>

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Title

Reserved

Size	Document Number	Rev
A4	Hadley 15"	X02

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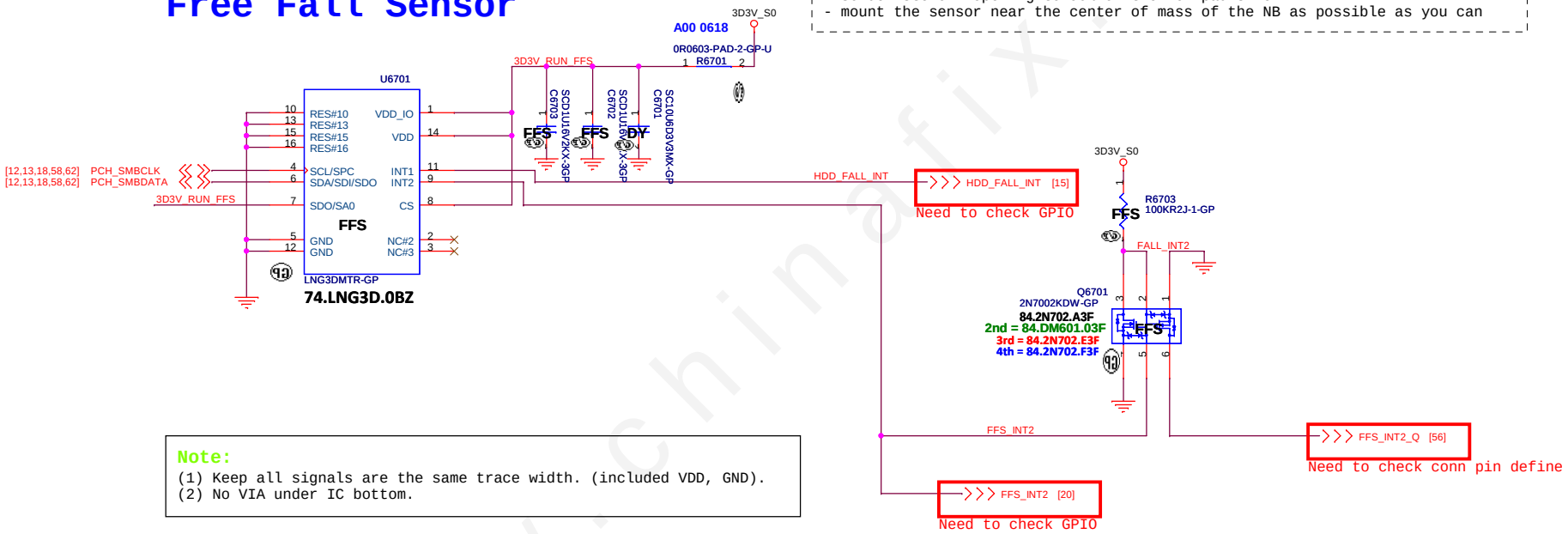
SSID = User.Interface

Free Fall Sensor

Note:
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note:
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

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Title: FFS		
Size: A3	Document Number: Hadley 15"	Rev: X02
Date: Friday, June 21, 2013	Sheet 67 of 101	

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Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 21, 2013 | Sheet 68 of 101

(Blanking)

<Core Design>

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Title: Reserved

Size: A3 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 21, 2013 | Sheet 69 of 101

(Blanking)

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Title: *Reserved*

Size: A3 | Document Number: *Hadley 15"* | Rev: *X02*

Date: Friday, June 21, 2013 | Sheet 70 of 101

(Blanking)

<Core Design>

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Title: *Reserved*

Size	Document Number	Rev
A3	*Hadley 15"*	*X02*

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(Blanking)

<Core Design>

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Title: *Reserved*

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SSID = VIDEO

dGPU Reset

D7301 1SS400GPT-GP
83.00400.C1F
2ND = 83.27101.01F
3RD = 83.01426.01F
A00 0618
0R0402-PAD-2-GP

[17,24,30,58,65] PLT_RST#
[15] DGPU_HOLD_RST#
R7304
VGA_RST# [76]

3D3V_VGA_S0
Q7301 2N7002K-2-GP 84.2N702.J31
R7308 10KR2J-3-GP
R7305 0R2J-2-GP
[18] PEG_CLKREQ#

GPU1A 1 OF 17
1/17 PCI_EXPRESS
GK107/GF108 GK208/GF117

PEX_WAKE#	NC
PEX_RST#	VGA_RST#
PEX_CLKREQ#	GPU_CLKREQ#
PEX_REFCLK	[18] CLK_PCIE_VGA
PEX_REFCLK#	[18] CLK_PCIE_VGA#

PEX_TX0 / PEX_TX0# — C7301 / C7302 SCD22U10V2KX-1GP — dGPU_TXP_CPU_RXP0 / dGPU_TXN_CPU_RXN0 — [16] CPU_RXP_C_dGPU_TXP0 / [16] CPU_RXN_C_dGPU_TXN0
PEX_RX0 / PEX_RX0# — [16] dGPU_RXP_C_CPU_TXP0 / [16] dGPU_RXN_C_CPU_TXN0
PEX_TX1 / PEX_TX1# — C7303 / C7304 SCD22U10V2KX-1GP — dGPU_TXP_CPU_RXP1 / dGPU_TXN_CPU_RXN1 — [16] CPU_RXP_C_dGPU_TXP1 / [16] CPU_RXN_C_dGPU_TXN1
PEX_RX1 / PEX_RX1# — [16] dGPU_RXP_C_CPU_TXP1 / [16] dGPU_RXN_C_CPU_TXN1
PEX_TX2 / PEX_TX2# — C7305 / C7306 SCD22U10V2KX-1GP — dGPU_TXP_CPU_RXP2 / dGPU_TXN_CPU_RXN2 — [16] CPU_RXP_C_dGPU_TXP2 / [16] CPU_RXN_C_dGPU_TXN2
PEX_RX2 / PEX_RX2# — [16] dGPU_RXP_C_CPU_TXP2 / [16] dGPU_RXN_C_CPU_TXN2
PEX_TX3 / PEX_TX3# — C7307 / C7308 SCD22U10V2KX-1GP — dGPU_TXP_CPU_RXP3 / dGPU_TXN_CPU_RXN3 — [16] CPU_RXP_C_dGPU_TXP3 / [16] CPU_RXN_C_dGPU_TXN3
PEX_RX3 / PEX_RX3#
PEX_TX4 / PEX_TX4#
PEX_RX4 / PEX_RX4#
PEX_TX5 / PEX_TX5#
PEX_RX5 / PEX_RX5#
PEX_TX6 / PEX_TX6#
PEX_RX6 / PEX_RX6#
PEX_TX7 / PEX_TX7#
PEX_RX7 / PEX_RX7#
PEX_TX8 / PEX_TX8#
PEX_RX8 / PEX_RX8#
PEX_TX9 / PEX_TX9#
PEX_RX9 / PEX_RX9#
PEX_TX10 / PEX_TX10#
PEX_RX10 / PEX_RX10#
PEX_TX11 / PEX_TX11#
PEX_RX11 / PEX_RX11#
PEX_TX12 / PEX_TX12#
PEX_RX12 / PEX_RX12#
PEX_TX13 / PEX_TX13#
PEX_RX13 / PEX_RX13#
PEX_TX14 / PEX_TX14#
PEX_RX14 / PEX_RX14#
PEX_TX15 / PEX_TX15#
PEX_RX15 / PEX_RX15#
PEX LANES 8 TO 15 NC FOR GF117/GK208

GF108	GK208/GK107/GF117
NC	PEX_PLL_HVDD
	PEX_SVDD_3V3

PEX_IOVDD_1..6 — 1D05V_VGA_S0 — C7323 C7310 C7322 C7312 C7313 C7325 C7326 — SC10U6D3V2MX-GP / SC10U6D3V2KX-GP

1.05V +/- 30mV
3.3A

PEX_IOVDDQ_1..14 — 1D05V_VGA_S0 — C7320 C7321 C7309 C7311 C7314 C7327 C7328 — SC10U6D3V3MX-GP / SC4D7U6D3V3KX-GP

3.3V +/- 5%
210mA

PEX_PLL_HVDD, PEX_SVDD_3V3 — 3D3V_VGA_S0 — C7316 C7315 C7324 — SC1U10V2KX-5GP / SC4D7U6D3V3KX-GP

X7R, Under GPU.

POWER IC

VDD_SENSE — L4 — VGA_SENSE [82]
GND_SENSE — L5 — GND_SENSE [82]
NC_3V3AUX — P8
PEX_TSTCLK_OUT / PEX_TSTCLK_OUT# — R7303 200R2F-L-GP — AJ26 PEXTSTCLK_OUT / AK26 PEXTSTCLK_OUT#

1.05V +/- 30mV
150mA

PEX_PLLVDD — AG26 — 1D05V_VGA_S0 — C7318 C7317 C7319 — SC1U10V2KX-5GP / SC4D7U6D3V3KX-GP / SC10U6D3V2KX-GP

0102 remove R7307

TESTMODE — AK11 TESTMODE — R7302 10KR2J-3-GP
PEX_TERMP — AP29 PEX_TERMP — R7301 2K49R2F-GP

OPS

N14P-GS-A1-GP
71.0N14P.00U

<Core Design>

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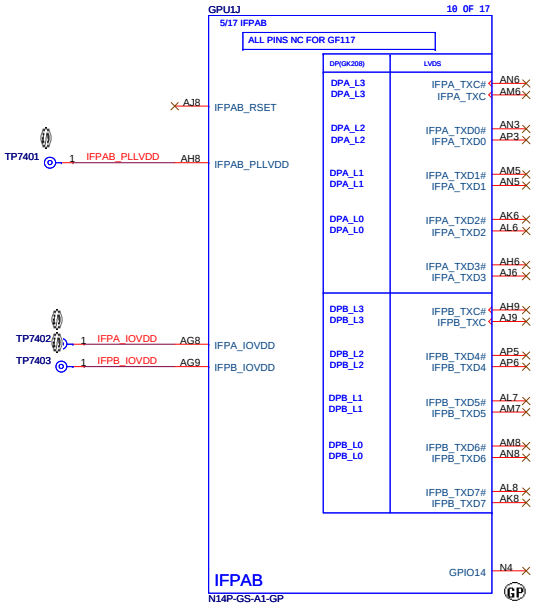
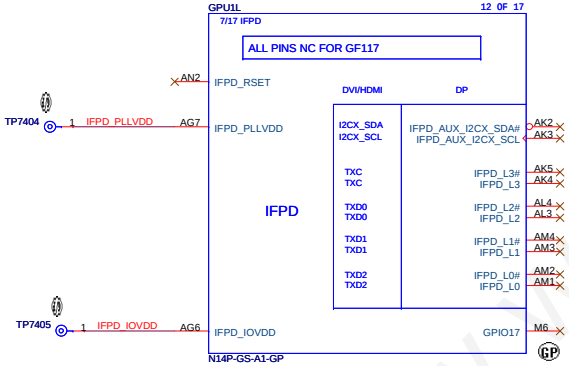
Title: GPU_PCIE/STRAPPING(1/5)
Size: Custom | Document Number: Hadley 15" | Rev: X02
Date: Friday, June 21, 2013 | Sheet 73 of 101

SSID = VIDEO



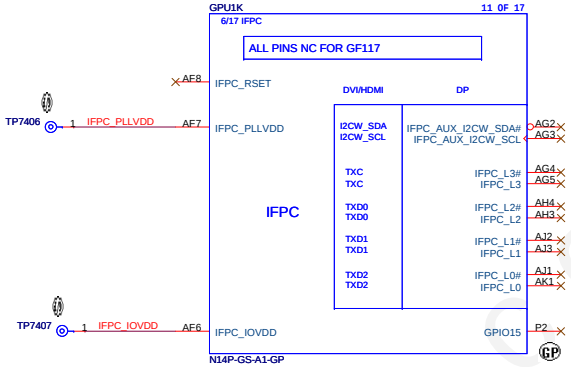
71.0N14P.00U

OPS



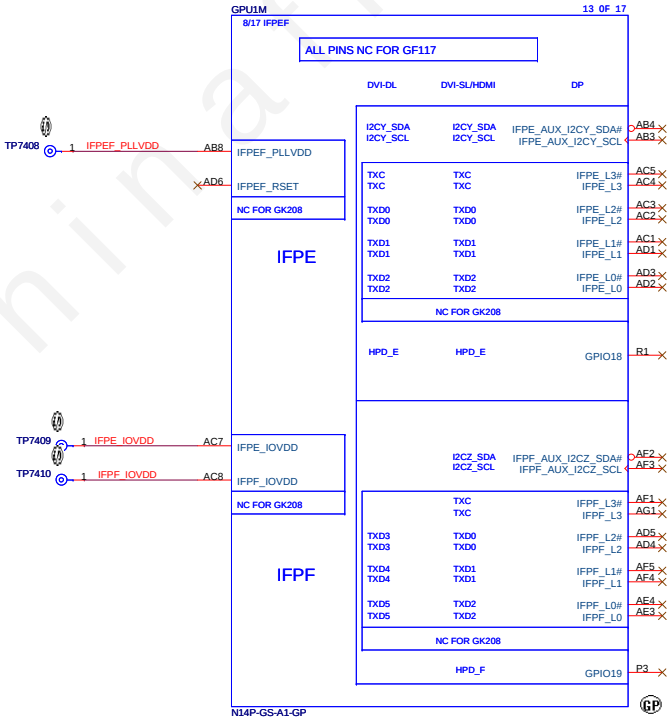
71.0N14P.00U

OPS



71.0N14P.00U

OPS



71.0N14P.00U

OPS

<Core Design>

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Title: GPU Memory(2/5)

Size	Document Number	Rev
Custom	Hadley 15"	X02

Date: Friday, June 21, 2013 Sheet 74 of 101

SSID = VIDEO

A00 0618

0102 remove L7502
change K27 pin net name

Layout note:FBA_PLL_AVDD=16mil
Place close to Ball

0102 remove L7503
change C7506 to 0603 package

Place under GPU near

DA-05691-001_V05 P7

THE FBA_WCKBxx PINS ARE USED ONLY ON GK107 THEY ARE NC FOR GK208/GF108 /GF117

THE FBB_WCKBxx PINS ARE USED ONLY ON GK107 THEY ARE NC FOR GF108

ALL PINS NC FOR GF117/GK208

1.35V +/- 3%
4.88A

GPU FBVDDQ Decoupling
PLACE CLOSE TO GPU BALLS

PLACE CLOSE TO GPU BALLS

71.0N14P.00U

OPS

<Core Design>

Wistron Corporation
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Title: GPU_DP/LVDS/CRT/GPIO(3/5)

Size: A2 | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 21, 2013 | Sheet 75 of 101

SSID = VIDEO

30ohm@100MHz
DCR=0.04 ohm
Max current = 3000mA

52mA

112mA

180ohm@100MHz
DCR=0.3 ohm
Max current = 300mA

NV request to need to be keeped

Resistor Values	Pull-up to VDD33	Pull-down to GND
4.99 k	1000	0000
10.0 k	1001	0001
15.0 k	1010	0010
20.0 k	1011	0011
24.9 k	1100	0100
30.1 k	1101	0101
34.8 k	1110	0110
45.3 k	1111	0111

GPU Product Name	N14P-GT
NV-Internal Chip Part# (used on labels of packaging bag/box materials)	GK107-750
Device ID	0x0FE4
Memory interface	GDDR5
Package	GB4-128

Configuration	Vendor	Strap	FBVDD/ FBVDDQ	Manufacturer Part Number	Max Speed WCK (MHz)	Memory Date Code Minimum	Status
128Mx16 GDDR5	Hynix	0x6	1.35V/ 1.35V	H5GQ2H24AFR-T2C	2000	N/A	Production candidate
	Samsung	0x7	1.35V/ 1.35V	K4G20325FD-FC04	2000	1219	Post-production candidate

0102 remove 0R

	Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
15K PD	ROM_SCLK	0	0	1	0
Hynix 35K PD	PCI_DEVID[4]	0	SUB_VENDOR	PCI_DEVID[5]	PEX_PLL_EN_TERM
Samsung 45K PD	ROM_SI	0	1	1	0
5K PH		0	1	1	1
45K PH	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]	
5K PD	ROM_SO	1	0	0	0
25K PD	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE	
5K PD	STRAP0	1	1	1	1
45K PD	USER[3]	USER[2]	USER[1]	USER[0]	
	STRAP1	0	0	0	0
	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	
	STRAP2	0	1	0	0
	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	
	STRAP3	0	0	0	0
	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	
	STRAP4	0	1	1	1
	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V	

DA-05691-001_V05 P15
GPIO20/21 NC : for ALL

DA-05691-001_V05 P6
NC : N13P-GS

EA40-HW SC

N14P-GT

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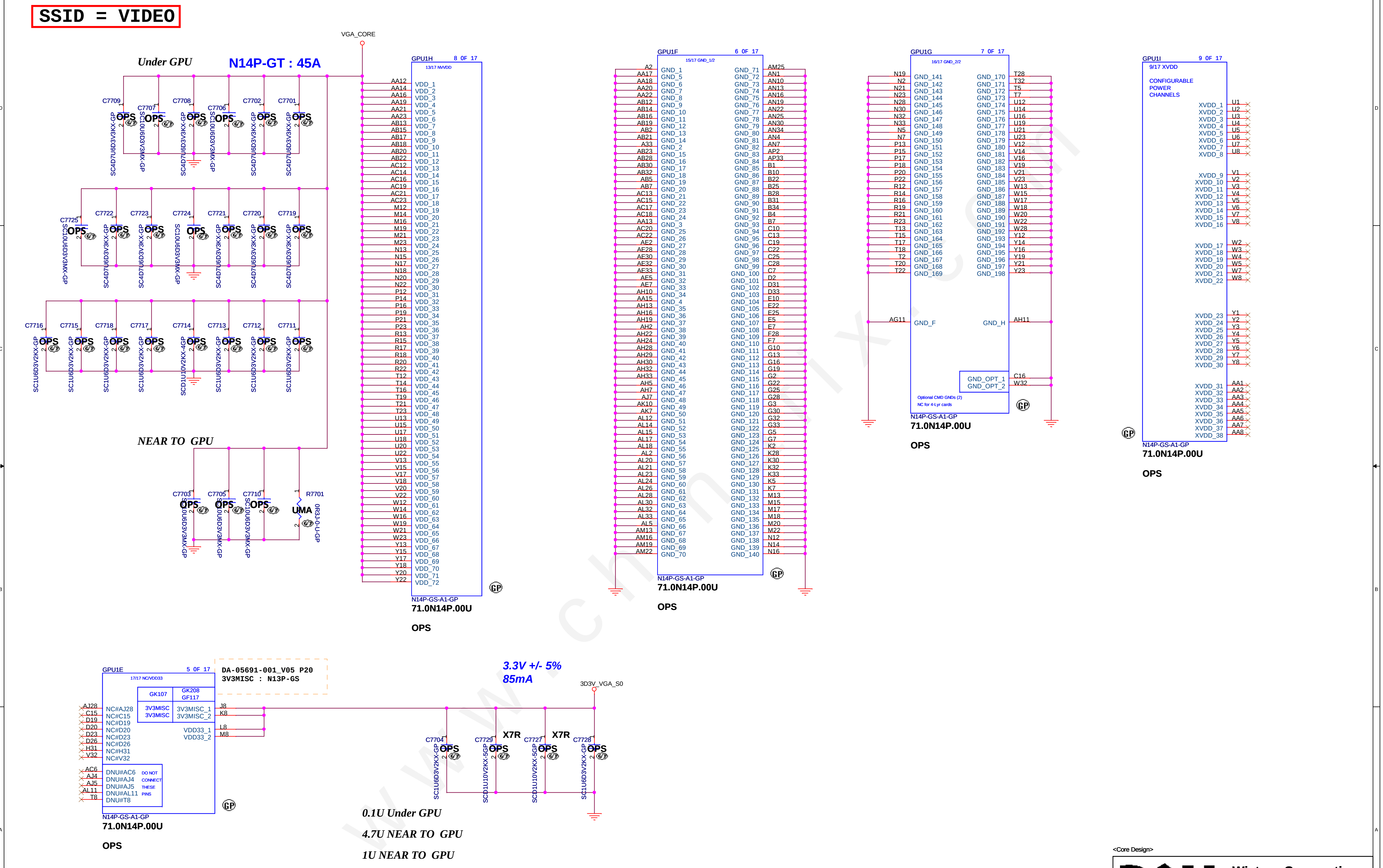
Title: Reserved

Size: Custom | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 21, 2013 | Sheet 76 of 101


SSID = VIDEO
VGA_CORE
Under GPU
N14P-GT : 45A
NEAR TO GPU
GPU1H 8 0F 17
13/17 NVVDD
GPU1F 6 0F 17
15/17 GND_1/2
GPU1G 7 0F 17
16/17 GND_2/2
GND_F
GND_H
GND_OPT_1
GND_OPT_2
Optional CMD GNDs (2)
NC for 4-Lyr cards
GPU1I 9 0F 17
9/17 XVDD
CONFIGURABLE
POWER
CHANNELS
N14P-GS-A1-GP
71.0N14P.00U
OPS
C7709 C7707 C7708 C7706 C7702 C7701
C7725 C7722 C7723 C7724 C7721 C7720 C7719
C7716 C7715 C7718 C7717 C7714 C7713 C7712 C7711
C7703 C7705 C7710
R7701
UMA
0R3J-0-U-GP
SC4D7U6D3V3KX-GP
SC10U6D3V3MX-GP
SC1U6D3V2KX-GP
SCD1U10V2KX-4GP
GPU1E 5 0F 17
17/17 NC/VDD33
GK107
GK208
GF117
3V3MISC
3V3MISC_1
3V3MISC_2
VDD33_1
VDD33_2
NC#AJ28
NC#C15
NC#D19
NC#D20
NC#D23
NC#D26
NC#H31
NC#V32
DNU#AC6
DNU#AJ4
DNU#AJ5
DNU#AL11
DNU#T8
DO NOT CONNECT THESE PINS
DA-05691-001_V05 P20
3V3MISC : N13P-GS
3.3V +/- 5%
85mA
3D3V_VGA_S0
C7704 C7729 C7727 C7728
X7R
SC1U6D3V2KX-GP
SCD1U10V2KX-5GP
0.1U Under GPU
4.7U NEAR TO GPU
1U NEAR TO GPU

<Core Design>

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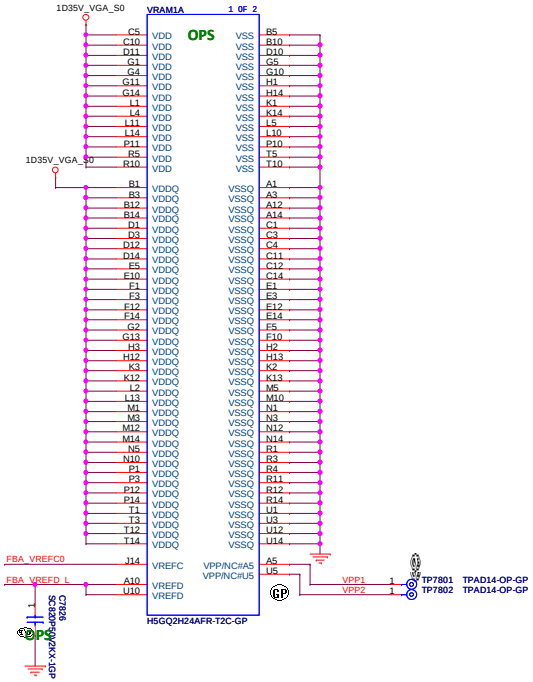
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU POWER(4/5)

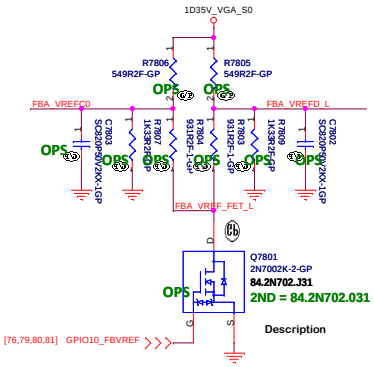
Size: Custom | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 21, 2013 | Sheet 77 of 101

SSID = VIDEO

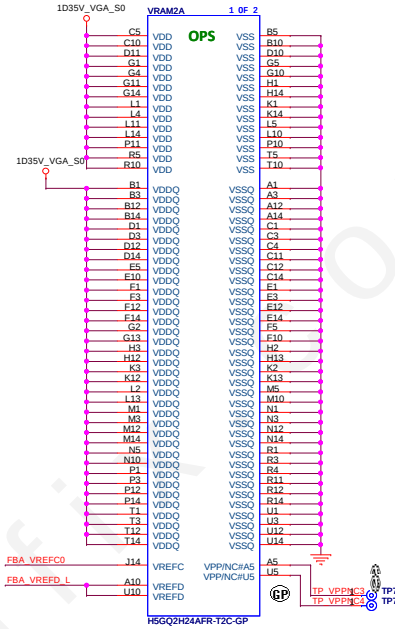


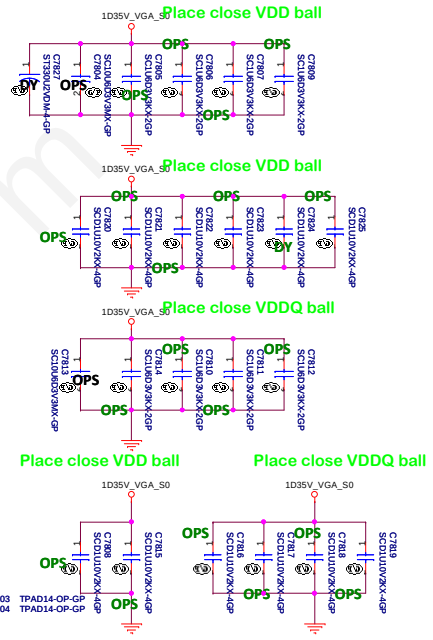
Frame Buffer Patition A-Lower Half



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

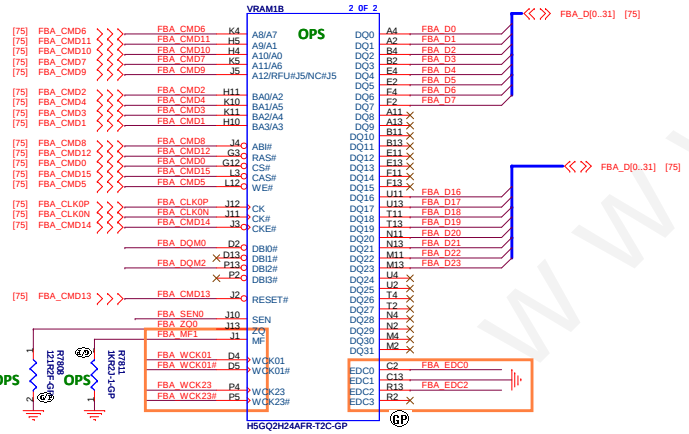




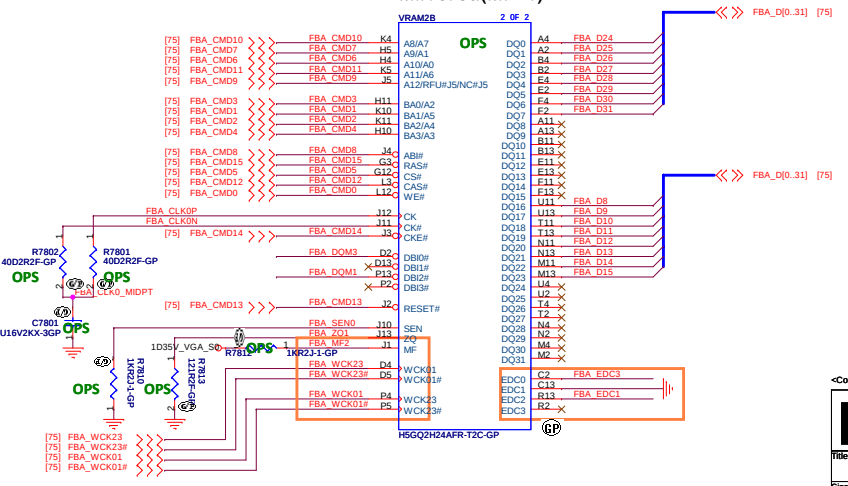
[75] FBA_EDC[0..3] — FBA_EDC0, FBA_EDC1, FBA_EDC2, FBA_EDC3

FBA_DQM0, FBA_DQM1, FBA_DQM2, FBA_DQM3 — FBA_DQM[0..3] [75]

Normal(MF=0)



Mirrored(MF=1)



<Core Design>

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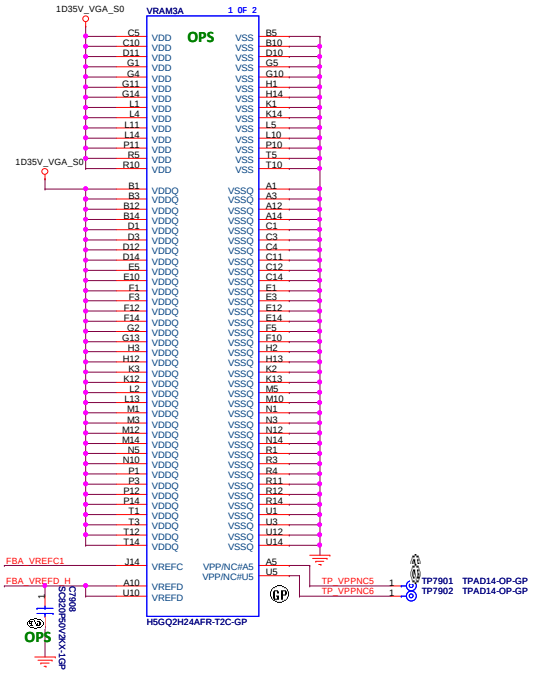
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM1,2 (1/4)

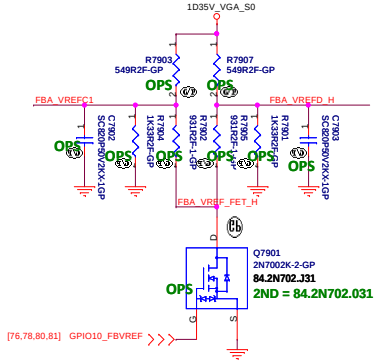
Size: Custom | Document Number: Hadley 15" | Rev: X02

Date: Friday, June 21, 2013 | Sheet 78 of 101

SSID = VIDEO

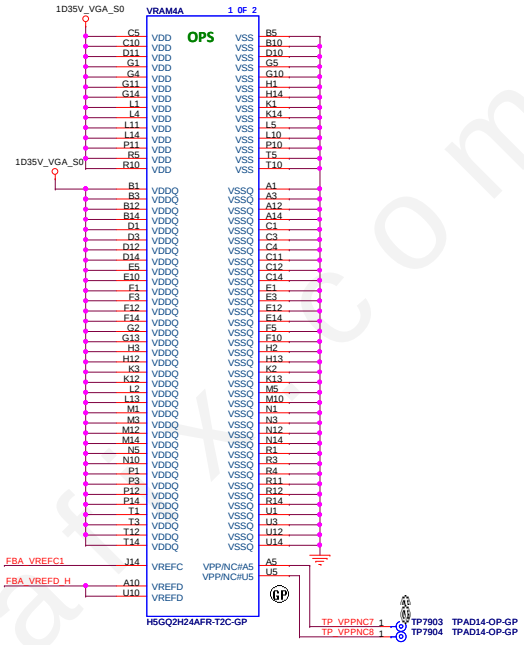


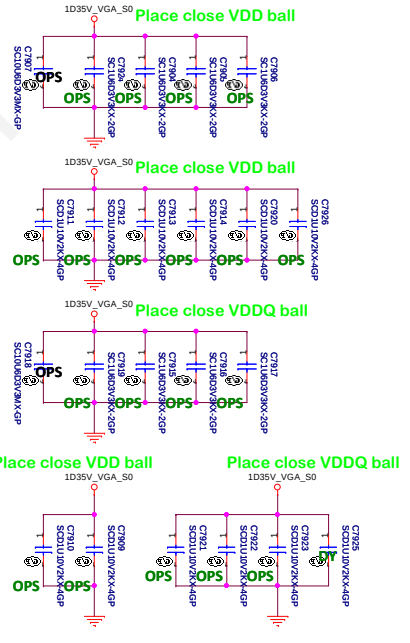
Frame Buffer Patition A-Upper Half

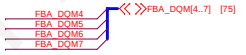


FBVREF Termination

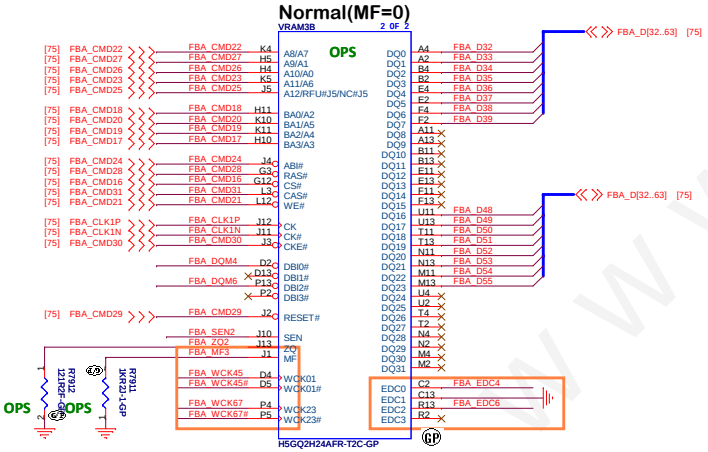
Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



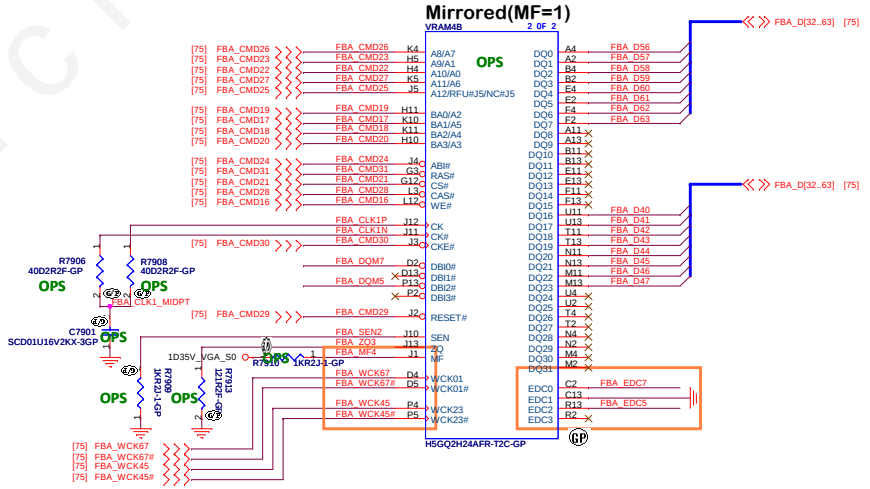




Normal(MF=0)



Mirrored(MF=1)



<Core Design>

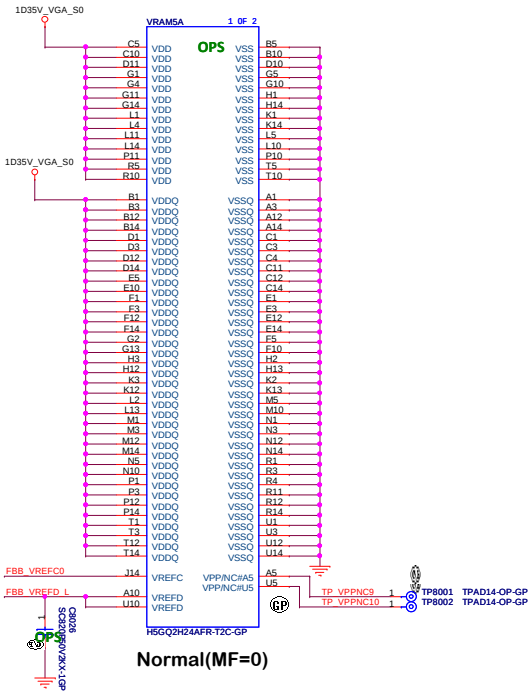
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GPU-VRAM3,4 (2/4)

Size: Custom | Document Number: Hadley 15" | Rev: X02

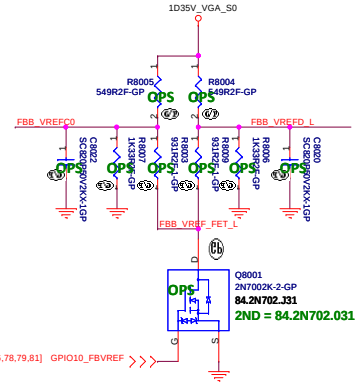
Date: Friday, June 21, 2013 | Sheet 79 of 101

SSID = VIDEO



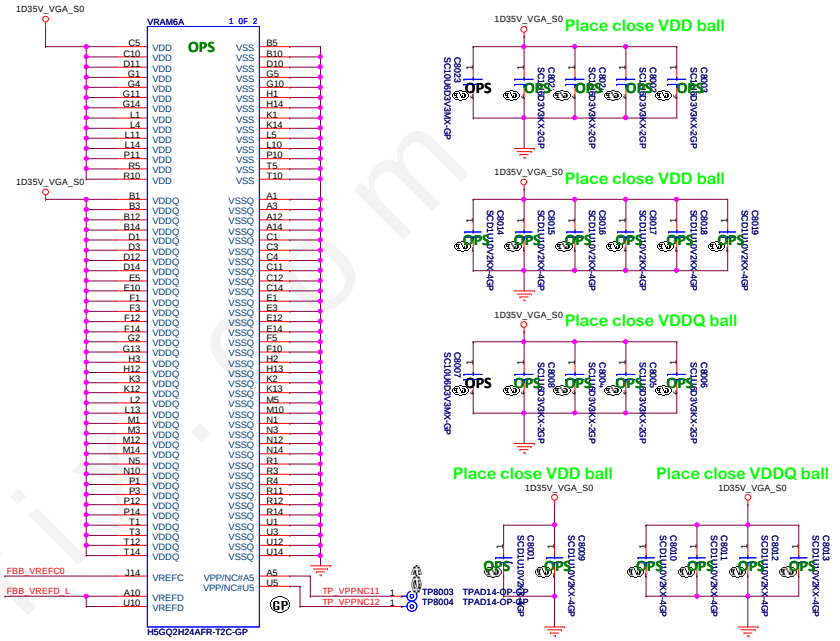
Normal(MF=0)

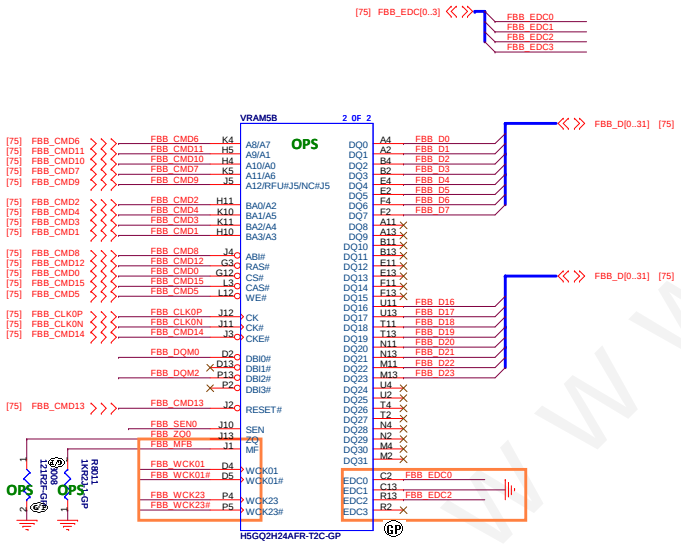
Frame Buffer Patition B-Lower Half



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low





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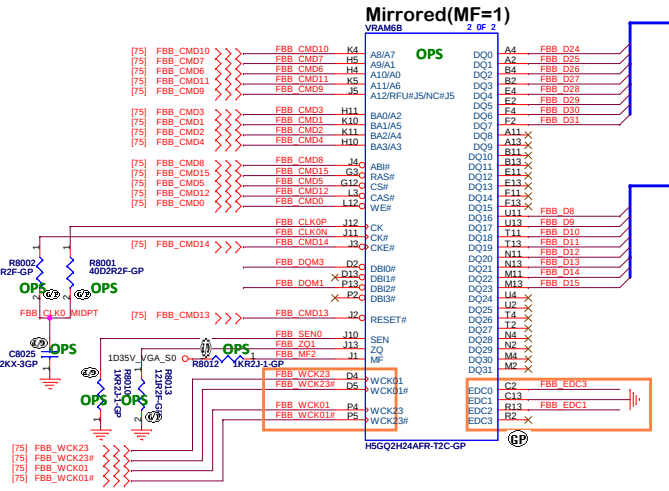

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Title: GPU-VRAM5,6 (3/4)

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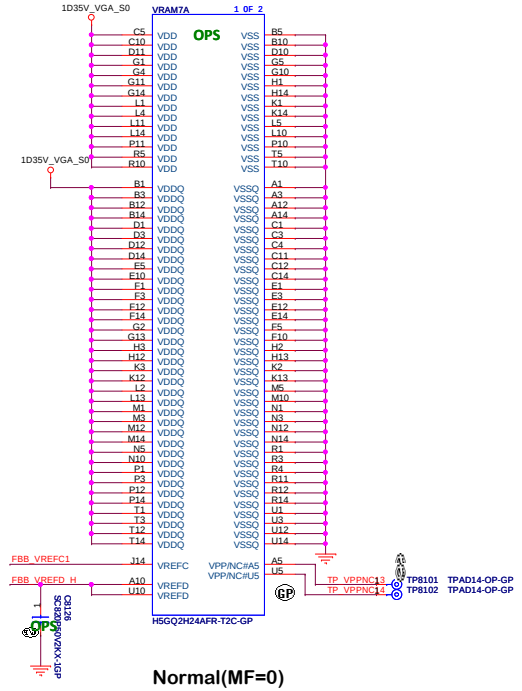
SSID = VIDEO



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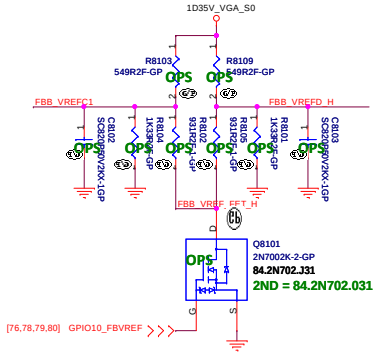
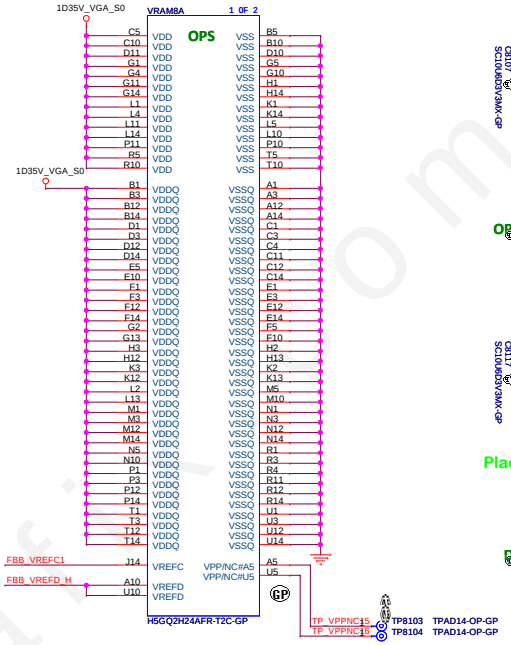
Frame Buffer Patition B-Upper Half



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low



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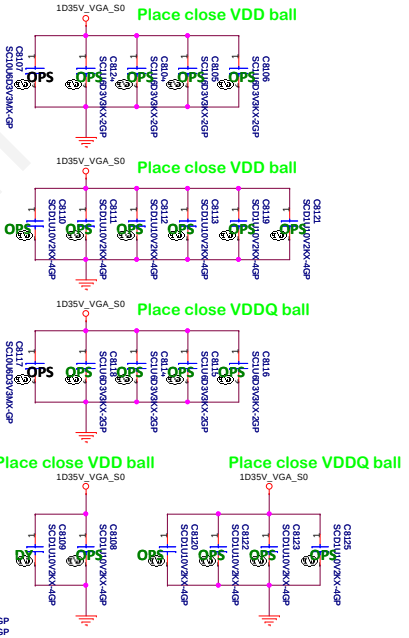

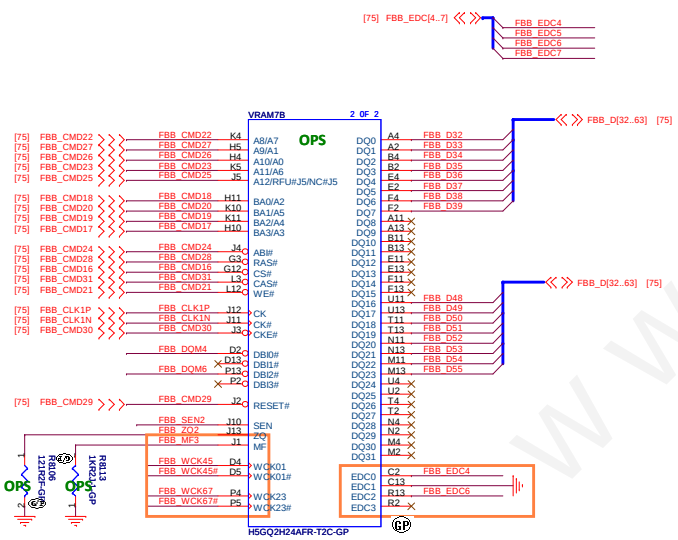

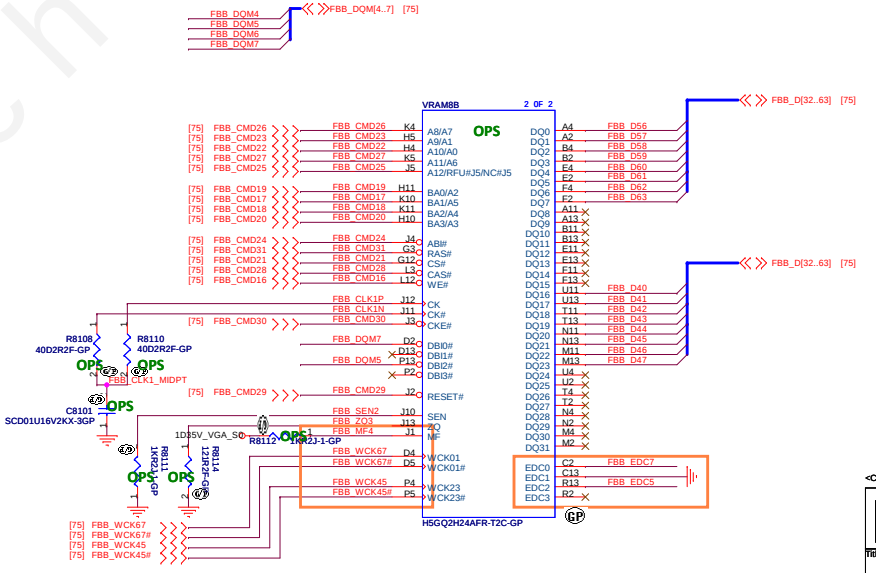

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Title: GPU-VRAM7,8 (4/4)

Size: Custom | Document Number: Hadley 15" | Rev: X02

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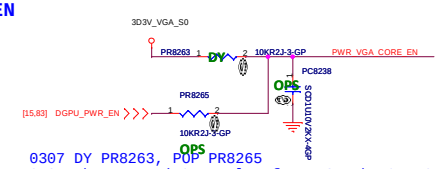
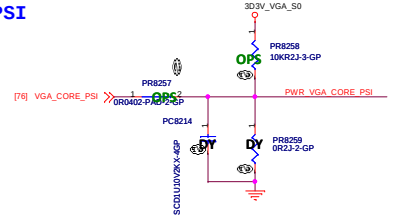
SSID = PWR.Plane.Regulator_vga_core

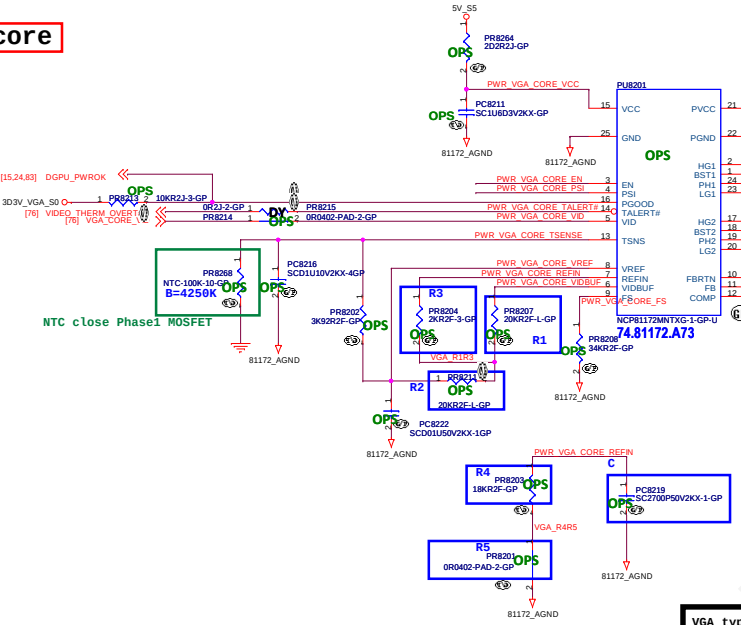
EN



0307 DY PR8263, POP PR8265
0521 change resistor value from 12K ohm to 10K

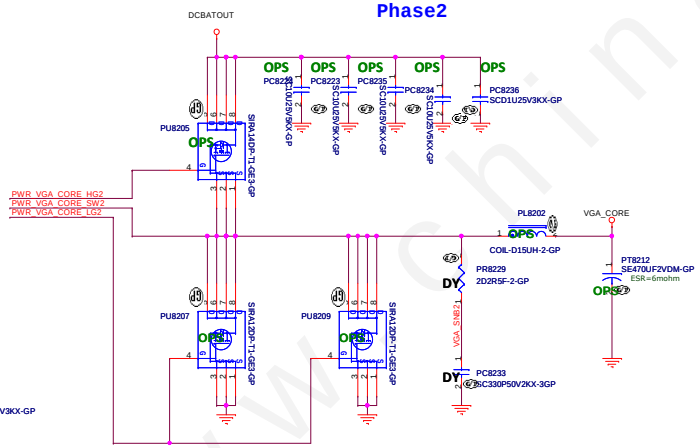
PSI



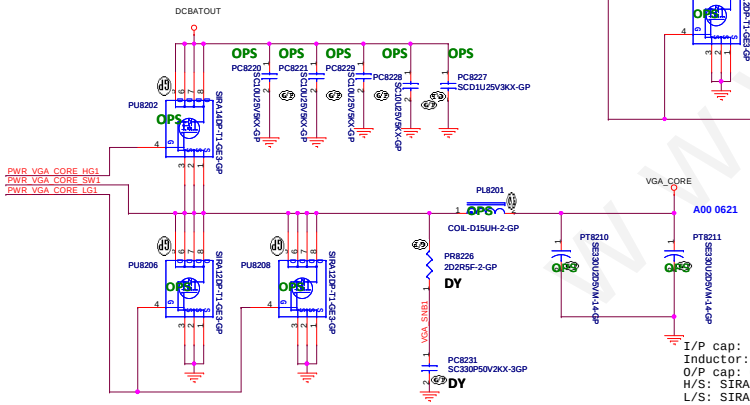


N14P-GT iis ConfigB

Phase2



Phase1



I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 0.22UH M PCMC063T-R22MN/ 2.8mohm/ Isat =40A rms /68.R2210_10V
O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
H/S: SIRA14DP-T1-GE3 / 6.8mohm/8.5mOhm@4.5Vgs/ 84.A14DP.037
L/S: SIRA12DP-T1-GE3 / 4.4mohm/6mOhm@4.5Vgs/ 84.SRA12.037

VGA type	Config	Design Current	EDP-peak	OCP	R1/PR8207	R2/PR8211	R3/PR8204	R4/PR8203	R5/PR8201	C/PC8219
N14P-LP	B	25A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GE	B	27A	40A	44A<OCP<52A	20K	20K	2K	18K	0	2.7nF
N14P-GS	B	38A	60A	66A<OCP<78A	20K	20K	2K	18K	0	2.7nF
N14P-GT	B	45A	75A	82.5A<OCP<97.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV	B	24A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14P-GV2	B	32A	55A	60.5A<OCP<71.5A	20K	20K	2K	18K	0	2.7nF
N14M-GS	B	26A	45A	49.5A<OCP<58.5A	20K	20K	2K	18K	0	2.7nF
N14M-LP	B	22A	35A	38.5A<OCP<45.5A	20K	20K	2K	18K	0	2.7nF
N14M-GL	C	24.33A	35.42A	38.96A<OCP<46.04A	39K	30K	3K	24K	3K	1.8nF
N14M-GE	C	35A	40.89A	44.98A<OCP<53.16A	39K	30K	3K	24K	3K	1.8nF
N14E-GTX	A	95A	125A	137.5A<OCP<162.5A	39K	39K	1.5K	30K	1.5K	1.5nF
N14E-GS	B	65.16A	87.87A	96.66A<OCP<114.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE-B	B	65.37A	98.6A	108.5A<OCP<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GE	B	65.37A	98.6A	108.5A<OCP<128.2A	20K	20K	2K	18K	0	2.7nF
N14E-GL	B	46.35A	71.83A	79.01A<OCP<93.98A	20K	20K	2K	18K	0	2.7nF

Table 1. PWM-VID Spec and Component Values

PWM-VID Spec				
		Config A	Config B	Config C
Vmin	V	0.6	0.6	0.65
Vmax	V	1.2	1.2	1.15
Vboot	V	0.875	0.9	0.9
Voltage Step Vstep	mV	6.25	6.25	25
Number of Voltage Levels N	level	96	96	20
PWM Frequency F_{PWM}	MHz	1.125	1.125	0.676
PWM Minimum Pulse Width T_{DMIN}	ns	9.26	9.26	74
VID Transient Time T	us	<100	<100	<100
Component Value				
R1 (1%)	KΩ	39	20	39
R2 (1%)	KΩ	39	20	30
R3 (1%)	KΩ	1.5	2	3
R4 (1%)	KΩ	30	18	24
R5 (1%)	KΩ	1.5	0	3
C	nF	1.5	2.7	1.8

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Title: NCP81172_VGA_CORE
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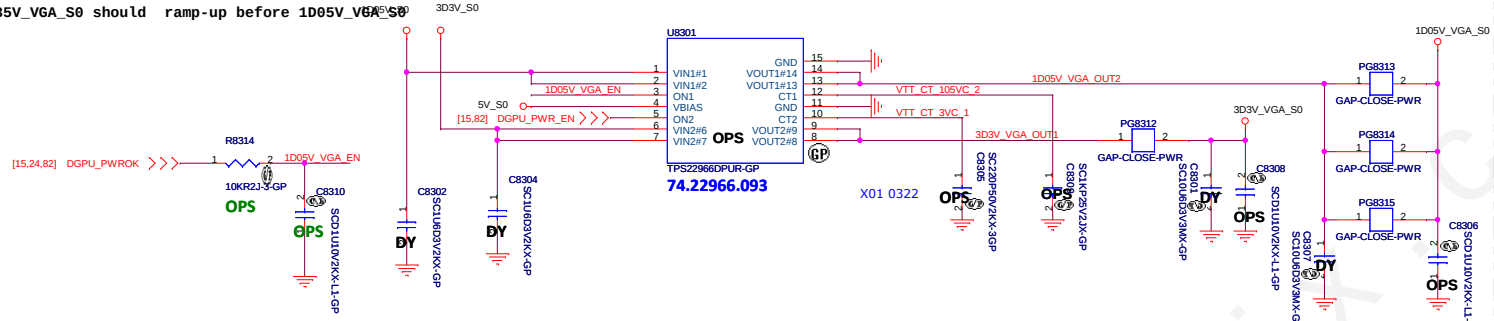
SSID = PWR.Plane.Regulator_3p3v_vga, 1p35v_vga, 1p05v_vga

3D3V_VGA_S0

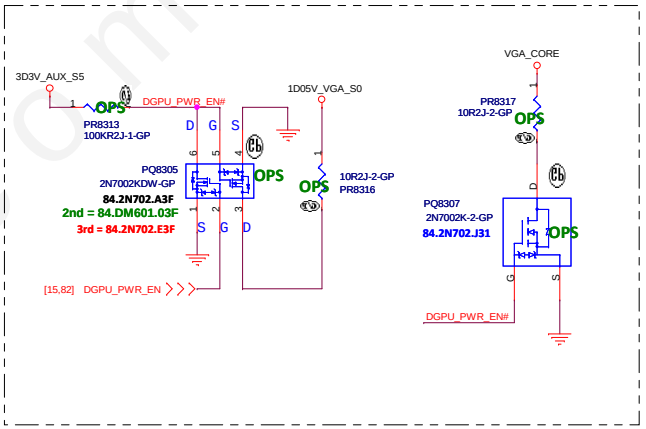
1D05V_VGA_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D5V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0

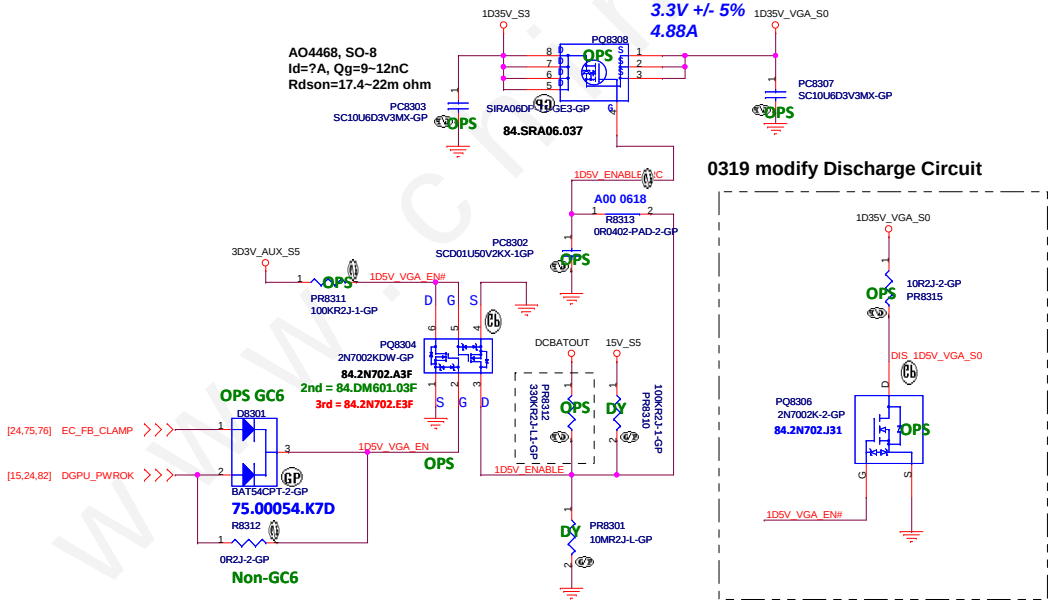
3D3V_S0 to 3D3V_VGA_S0
1D05V_S0 to 1D05V_VGA_S0



0307 Add Discharge Circuit



1D35V_VGA_S0



0319 modify Discharge Circuit

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SSID = User.Interface

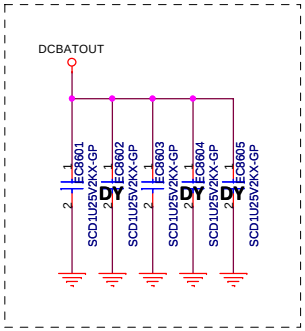
SO1 OPS — STF217R128H83-2-GP — 34.4Y702.301
SO2 OPS — STF217R128H83-2-GP — 34.4Y702.301
SO3 OPS — STF217R128H83-2-GP — 34.4Y702.301

S1 — SPRING-52-GP — 34.4T025.001
S2 — SPRING-52-GP — 34.4T025.001
S3 — SPRING-52-GP — 34.4T025.001
S4 — SPRING-52-GP — 34.4T025.001

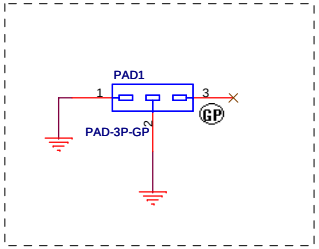
H2 — HOLET256B315R111-GP — ZZ.00PAD.M01
H3 — HT85BE85R29-U-5-GP — ZZ.00PAD.D41
H4 — HOLET256B315R111-GP — ZZ.00PAD.M01

C1 HOLE197R166-1-GP — ZZ.00PAD.V71
C2 HOLE197R166-1-GP — ZZ.00PAD.V71
C3 HOLE197R166-1-GP — ZZ.00PAD.V71

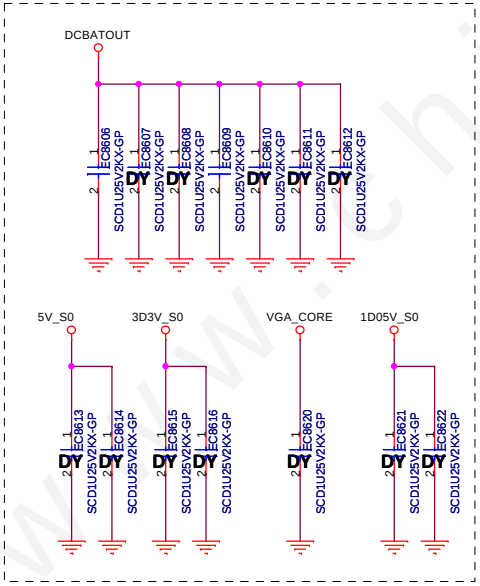
0116 Add RF CAP



0528 Add NPTH hole



0117 Add EMC CAP



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Title: UNUSED PARTS/EMI Capacitors
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Title: *Reserved*

Size | Document Number: *Hadley 15"* | Rev: *X02*

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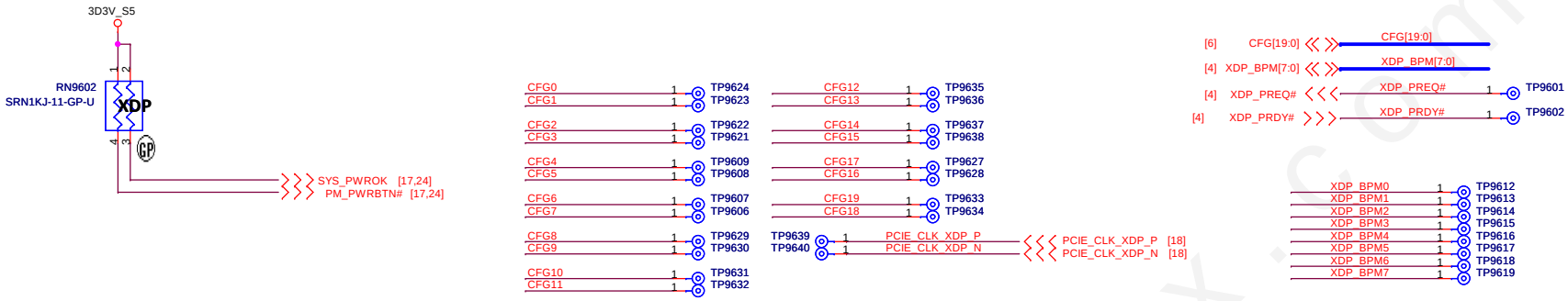
SSID = XDP

CPU XDP



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Title: CPU XDP

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PCH Strapping

Name	Schematics Notes

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value

Voltage Rails

POWER PLANE	VOLTAGE	ACTIVE IN	DESCRIPTION

SMBus ADDRESSES

I²C / SMBus Addresses	CHIEF RIVER ORB	
Device	Address	Bus
EC SMBus 1		
Battery 0	0x16	BAT_SCL/BAT_SDA
CHARGER	0x12	BAT_SCL/BAT_SDA
PS8122(HDMI Switch) (Bottom Dock)	0x9E	BAT_SCL/BAT_SDA
USB3.0 redriver PS8710 (Bottom Dock)	0x40	BAT_SCL/BAT_SDA
EC SMBus 2		
Battery 1	0x16	SML1_CLK/SML1_DATA
PCH	0x96 & 0x94	SML1_CLK/SML1_DATA
Discrete VGA Thermal	0x9C or 0x9E	SML1_CLK/SML1_DATA
PS8321 HDMI level shifter	0x96 & 0X97	SML1_CLK/SML1_DATA
NCT7718W	0x98 or 0x99	SML1_CLK/SML1_DATA
EC SMBus 3		SMB2_CLK/SMB2_DATA
NCT5605Y-0	0x30	SMB2_CLK/SMB2_DATA
NCT5605Y-1	0x32	SMB2_CLK/SMB2_DATA
PCH SMBus		
SO-DIMMA		PCH_SMBDATA/PCH_SMBCLK
SO-DIMMB		PCH_SMBDATA/PCH_SMBCLK
Intel LAN 82579		PCH_SMBDATA/PCH_SMBCLK
G-Sensor		PCH_SMBDATA/PCH_SMBCLK
MINI WWAN		PCH_SMBDATA/PCH_SMBCLK
INTEL LAN82579		PCH_SMBDATA/PCH_SMBCLK

PCIE Routing

LANE1	X
LANE2	X
LANE3	Mini Card1(WLAN)
LANE4	X
LANE5	X
LANE6	X
LANE7	X
LANE8	X

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	
3	
4	
5	

USB Table

Pair	Device
0	USB port 1,with Power Share
1	USB 2.0 HDMI
2	USB port2 (usb redriver)
3	X
4	Touch Panel
5	Card Reader
6	BLUETOOTH
7	CAMERA

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Title: Table of Content

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Title
Change History

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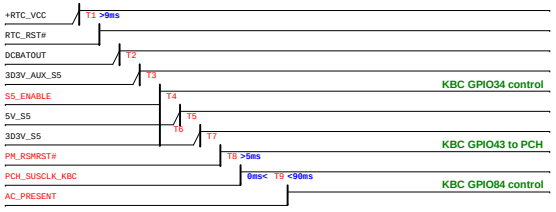
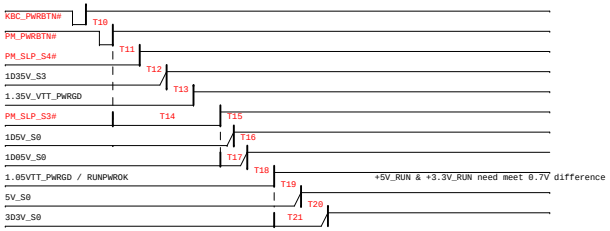
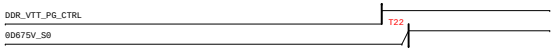
Intel-Power Up Sequence

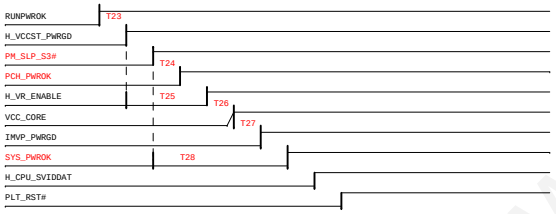
(AC mode)

Red printings:KBC GPIO involved



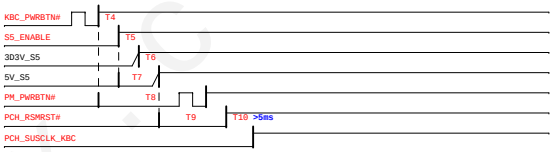


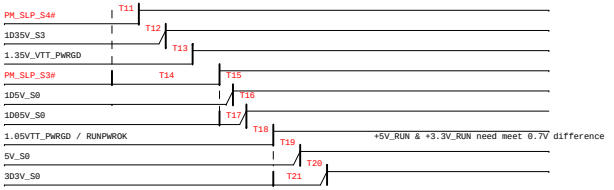


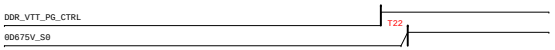


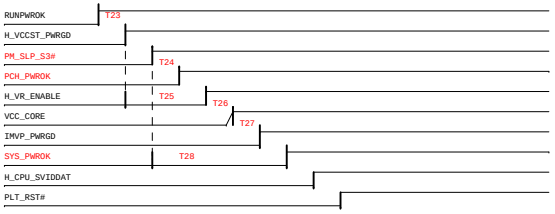
(DC mode)

Red printings:KBC GPIO involved









<Core Design>

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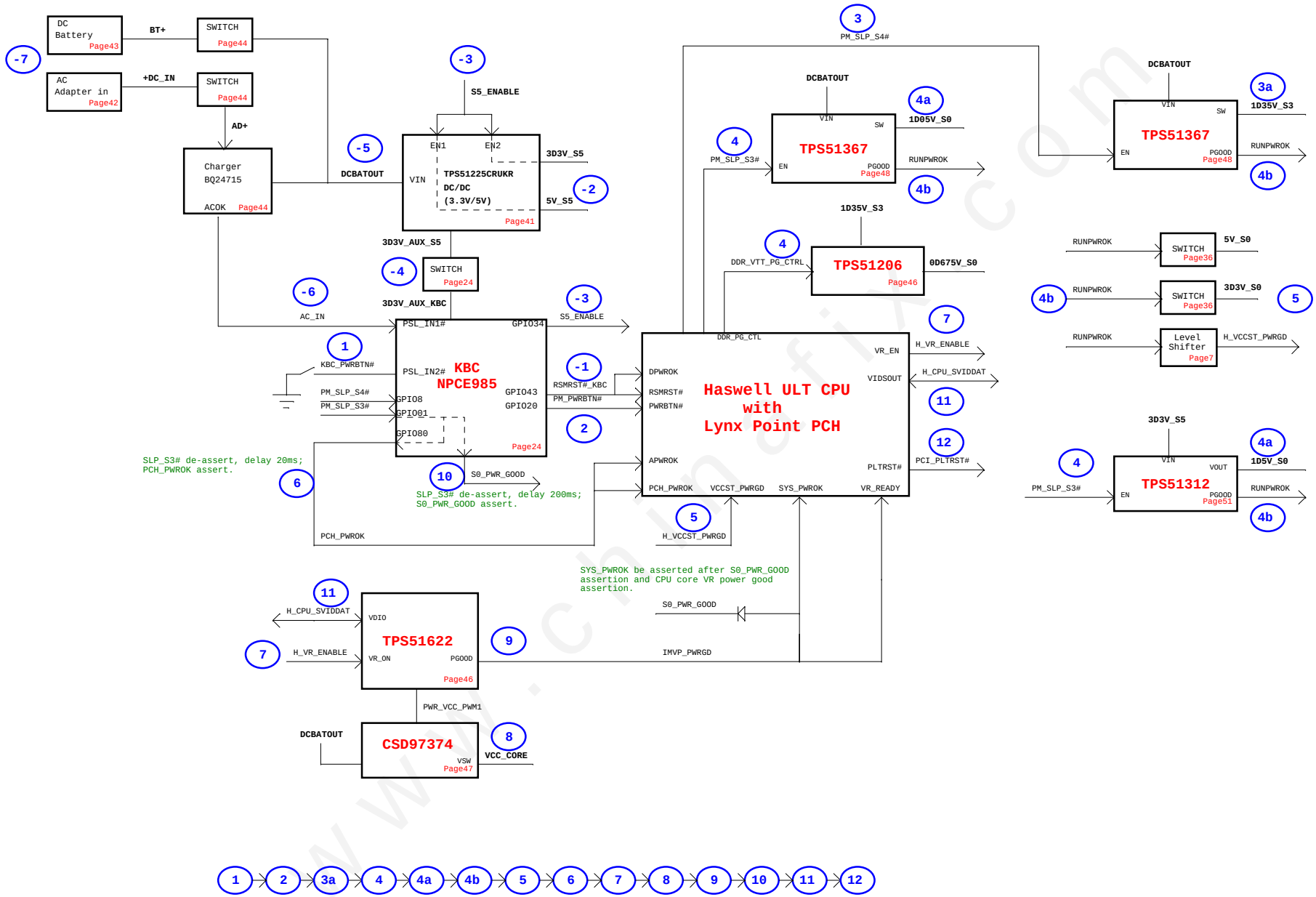
Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM



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Title: Power Block Diagram

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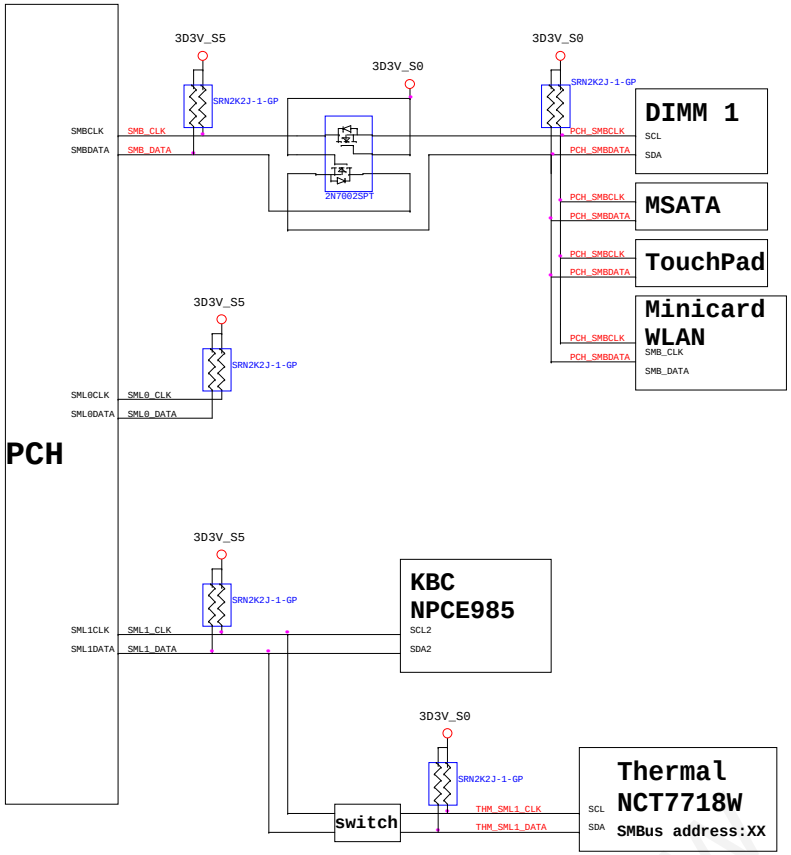
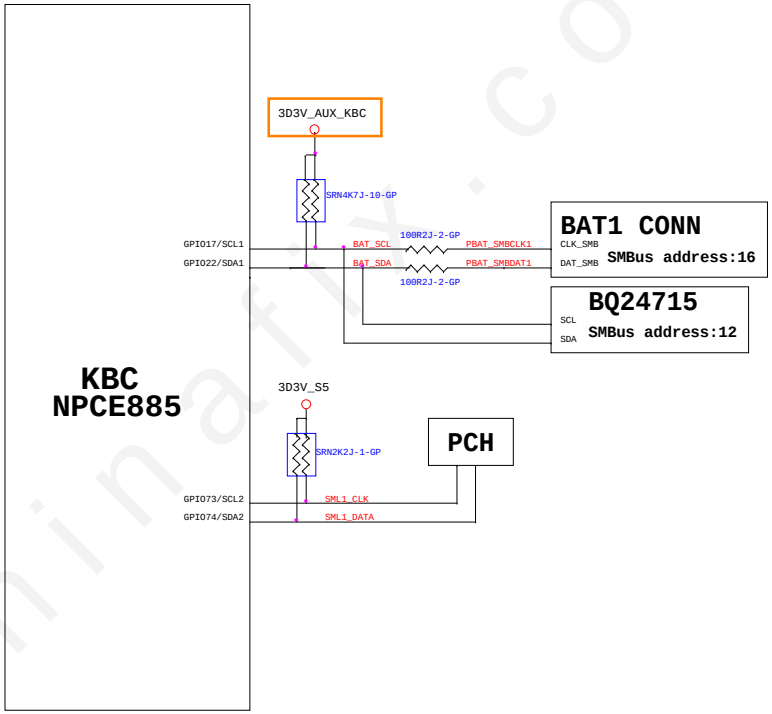
PCH SMBus Block Diagram



KBC SMBus Block Diagram



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Title: SMBUS Block Diagram

Size | Document Number: Hadley 15" | Rev: X02

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