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Lenovo - BIDDING BOX(M710e)

SCHEMATIC INDEX

PROJECT INFORMATION

PHASE: SVT 2017/11/28
BOM: 0.2
SVID: 17AA
SSID: 313C

BOM DISTRIBUTION RULE

BIDDING BOX
(BOM)

PCB Fab Note

Layer	Layer Name	Min/Typical/Max Layer Thickness (mil)	Dielectric Constant	Remark
	Solder Mask	0.4 / 0.65 / 1.8	3.40	
L1	Signal	1.4 / 1.90 / 2.4	NA	1.5 oz.(With Plating)
	Prepreg	2.2 / 2.75 / 3.2	3.90	
L2	Power/Gnd	1.0 / 1.20 / 1.4	NA	1. oz.
	Core	NA / 49.0 / NA	4.125	
L3	Power/Gnd	1.0 / 1.20 / 1.4	NA	1. oz.
	Prepreg	2.2 / 2.75 / 3.2	3.90	
L4	Signal	1.4 / 1.90 / 2.4	NA	1.5 oz.(With Plating)
	Solder Mask	0.4 / 0.65 / 1.8	3.40	

PCB / SILKSCREEN COLOR

PHASE	PCB	SILKSCREEN
	BIDDING BOX	BIDDING BOX
ET	RED	YELLOW
SDV	Blue	WHITE
SIT/SIT-R/SVT	GREEN	WHITE

BOM DEFINITION:

MARKING	DESCRIPTION
I	INSTALL
NI	NOT INSTALL
MP	PRODUCTION PART ONLY
PROTO	NOT FOR PRODUCTION PART
CCL	CRITICAL COMPONENT LIST

BIOS Licence Label

LBL1
BIOS_LICENCE

Note:
AMI uEFI

PCB For BIDDING BOX

PCB1
Printed Circuit Board
PCB_B250_ET
CCL=Y
4-Layer PCB,Color With Green Soldermask,White Silkscreen,11.179X7.874inch,Rev:V1.0,ROHS
0101FF203-491-G

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System BLOCK Diagram

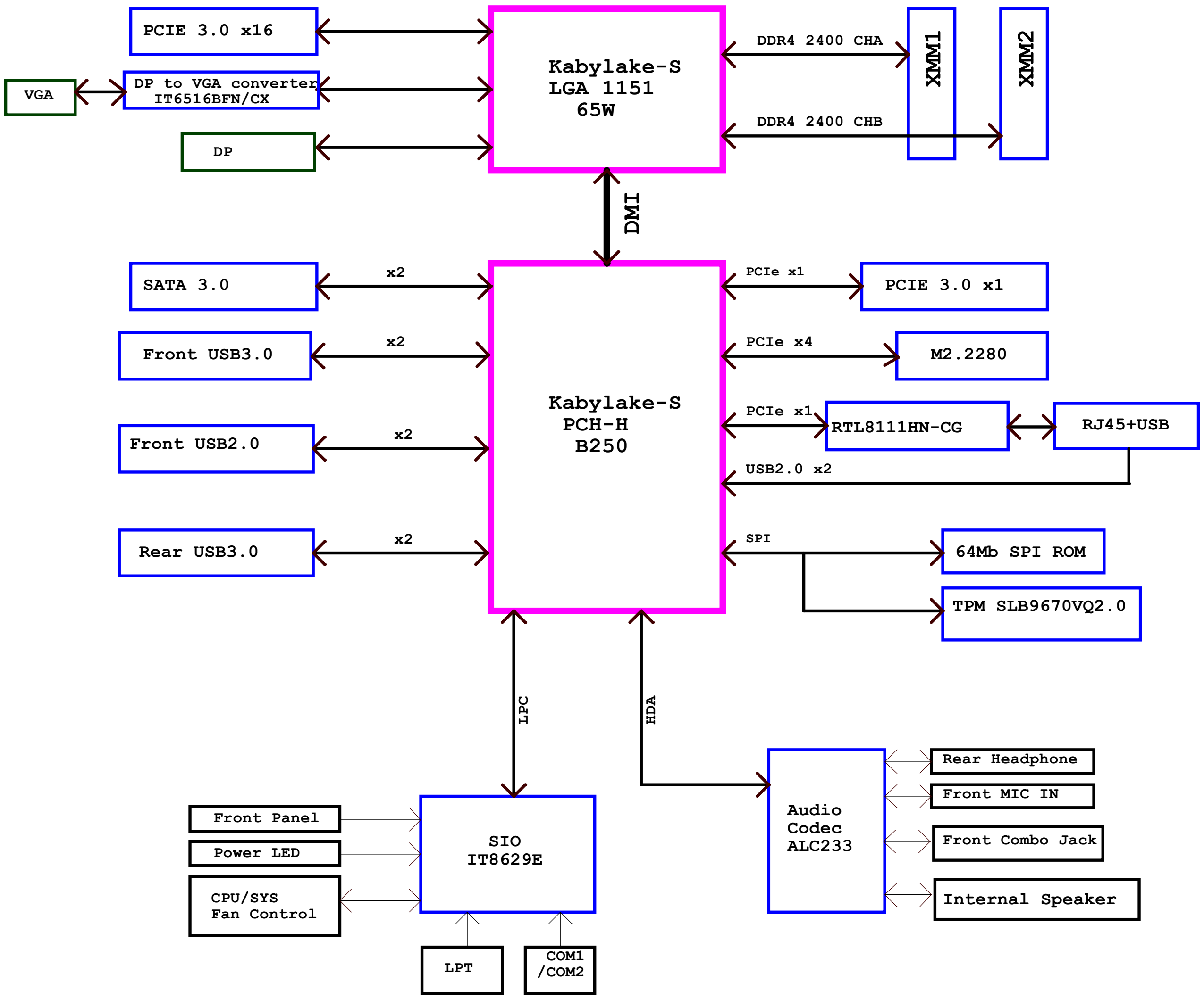

Table 4-1: Power Supply Rail Requirements

Power Rail	10 W Slot	25 W Slot	75 W Slot
+3.3V			
Voltage tolerance	± 9% (max)	± 9% (max)	± 9% (max)
Supply Current	3.0 A (max)	3.0 A (max)	3.0 A (max)
Capacitive Load	1000 μF (max)	1000 μF (max)	1000 μF (max)
+12V			
Voltage tolerance	± 8%	± 8%	± 8%
Supply Current	0.5 A	2.1 A (max)	5.5 A (max)
Capacitive Load	300 μF (max)	1000 μF (max)	2000 μF (max)

Power Rail	10 W Slot	25 W Slot	75 W Slot
+3.3Vaux			
Voltage tolerance	± 9% (max)	± 9% (max)	± 9% (max)
Supply Current			
Wakeup Enabled	375 mA (max)	375 mA (max)	375 mA (max)
Non-wakeup Enabled	20 mA (max)	20 mA (max)	20 mA (max)
Capacitive Load	150 μF (max)	150 μF (max)	150 μF (max)

Table 4-2: Add-in Card Power Dissipation

	X1		x4/x8	x16	
Standard height	10 W[1] (max)	25 W[1] (max)	25 W (max)	25 W[2] (max)	75 W[2, 4] (max)
Low profile card[3]	10 W (max)		25 W (max)	25 W (max)	

Notes:

1. A standard height x1 add-in card intended for desktop applications is limited in length to a half-length add-in card and 10 W maximum power dissipation. A standard height x1 add-in card intended for server I/O applications with 25 W maximum power dissipation must be greater than or equal to 177.80 mm (7.0 inches) in length, but must not exceed a full-length add-in card. See Table 6-1 for add-in card size definitions. The same server I/O add-in card must, at initial power-up, not exceed 10 W of power dissipation, until configured as a high power device, at which time it must not exceed 25 W of power dissipation. Refer to Chapter 6 of the *PCI Express Base Specification, Revision 1.1* for information on the power configuration mechanism.

Table 6-1: Add-in Card Sizes

Link Width		Height	Length
x1	Standard height, half length card	111.15 mm (4.376 inches) maximum	167.65 mm (6.600 inches) maximum
x1, x4, x8, x16	Standard height, full length cards	111.15 mm (4.376 inches) maximum	312.00 mm (12.283 inches) maximum
	Low profile cards	68.90 mm (2.731 inches) maximum	167.65 mm (6.600 inches) maximum

4.3.4.1. Power Requirements

All PCI connectors require four power rails: +5V, +3.3V, +12V, and -12V. Systems that provide PCI connectors are required to provide all four rails in every system with the current budget specified in Table 4-10. Systems may optionally supply 3.3Vaux power, as specified in the *PCI Bus Power Management Interface Specification*. Systems that do not support PCI bus power management must treat the 3.3Vaux pin as reserved.

Current requirements per connector for the two 12V rails are provided in Table 4-10. There are no specific system requirements for current per connector on the 3.3V and 5V rails; this is system dependent. Note that Section 4.4.2.2. requires that an add-in card must limit its total power consumption to 25 watts (from all power rails). The system provides a total power budget for add-in cards that can be distributed between connectors in an arbitrary way. The **PRSNTn#** pins on the connector allow the system to optionally assess the power demand of each add-in card and determine if the installed configuration will run within the total power budget. Refer to Section 4.4.1. for further details.

Table 4-10 specifies the tolerances of supply rails. Note that these tolerances are to be guaranteed at the components not the supply.

Table 4-10: Power Supply Rail Tolerances

Power Rail	Add-in Cards (Short and Long)
3.3 V ±0.3 V	7.6 A max. (system dependent)
5 V ± 5 %	5 A max. (system dependent)
12 V ±5%	500 mA max.
-12 V ±10%	100 mA max.

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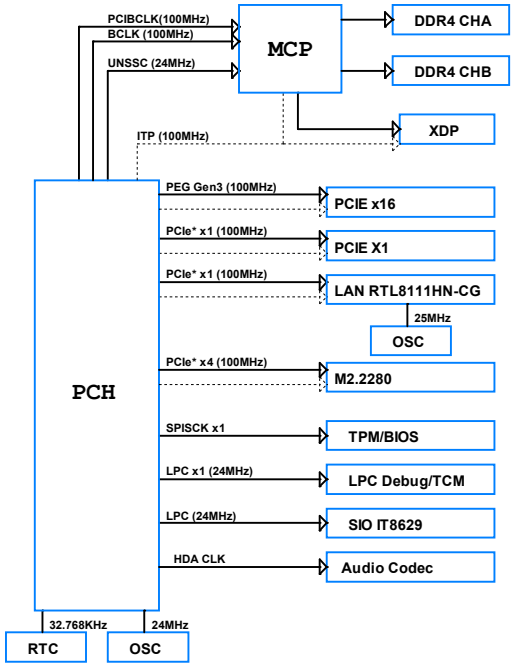
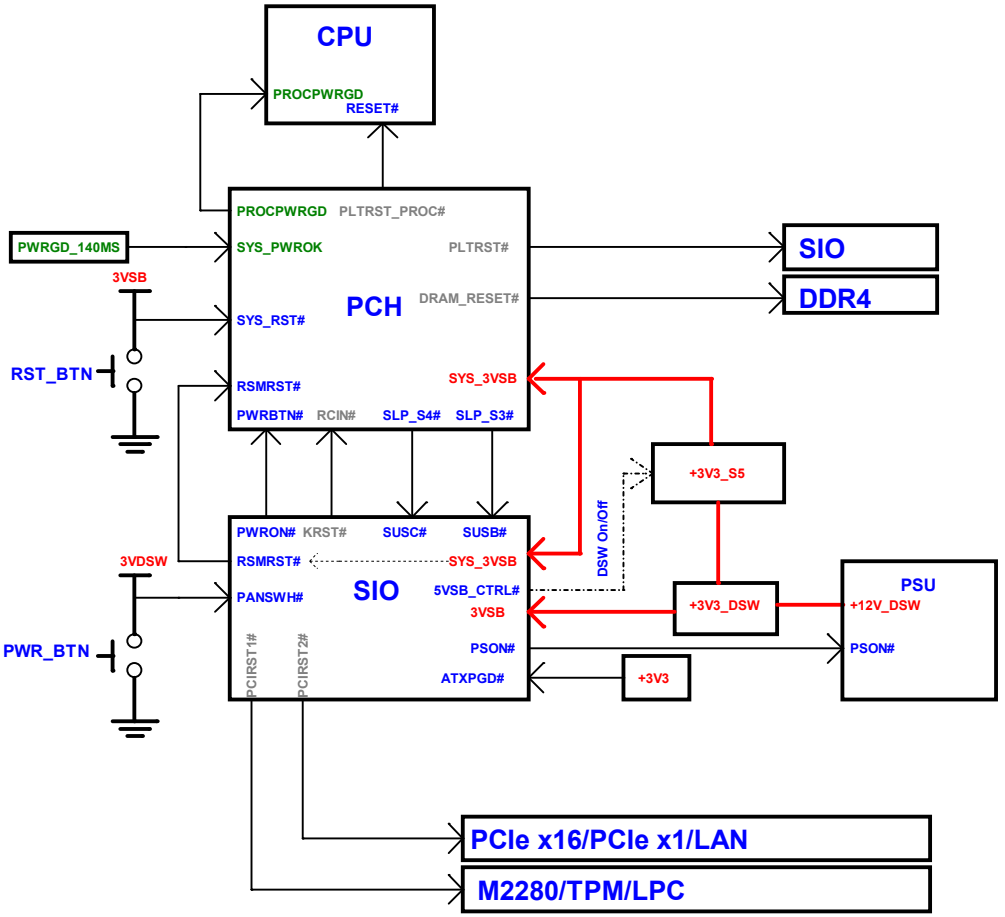
Clock Diagram



RESSET & POWER GOOD DIAGRAM



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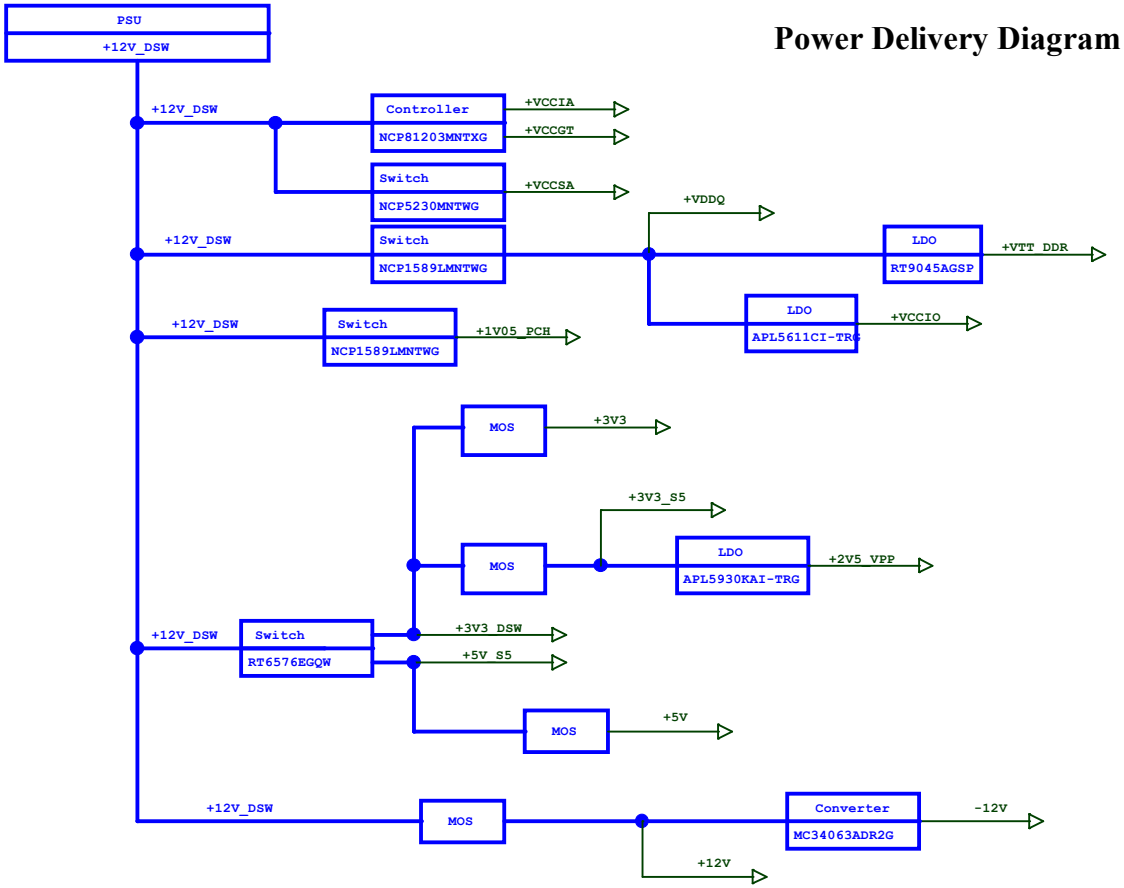
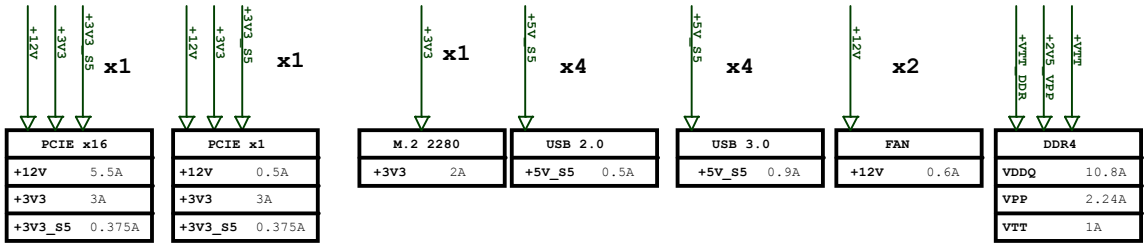
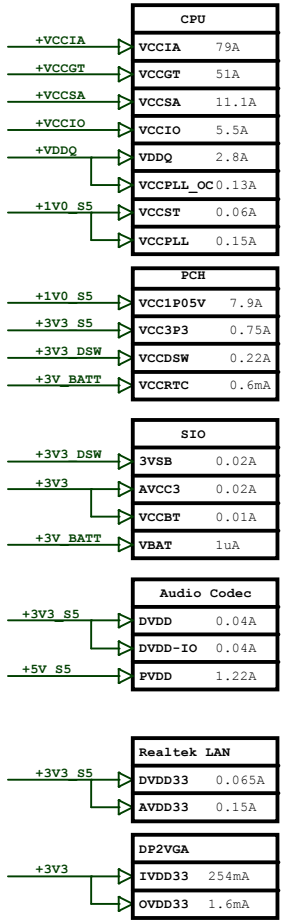
Power Delivery Diagram







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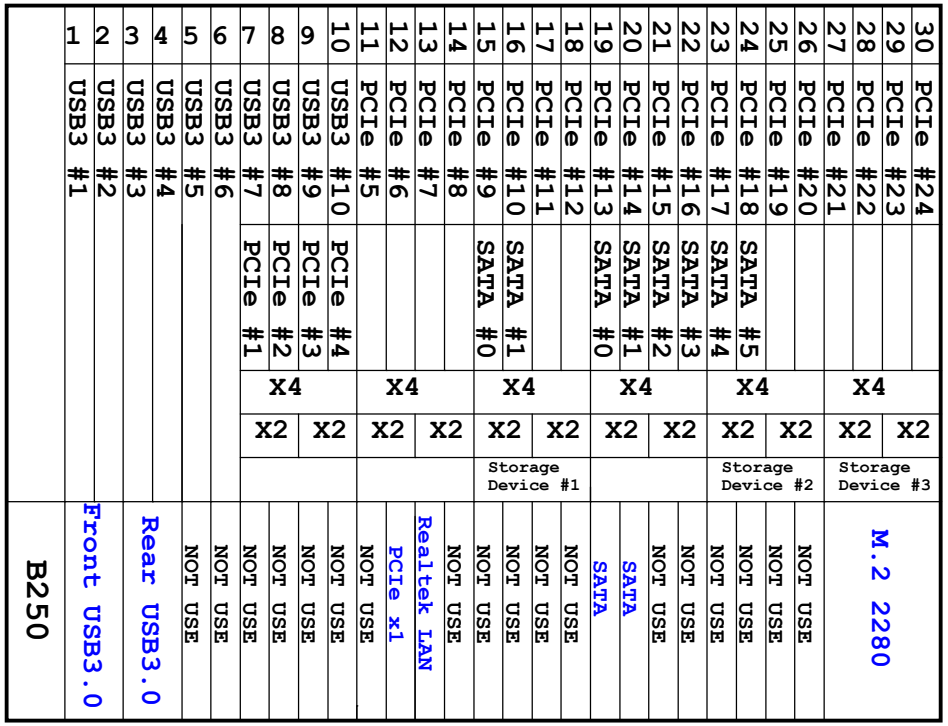
HSIO MAPPING



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PCH & SIO GPIO TABLE

PCH GPIO GPP A&B

GPIO Pin name	Power Well	Default Voltage	Native Fuanction	Default Status	Actual Power Well	Actual Voltage	Usage (BIOS CHECK)	Native or GPIO(Note1)	BootSet (BIOS Check)	Pad Reset Config (PADRSTCFG)(Note2)	Note
GPP_A0	S5	1.8V or 3.3V	LPC Mode: RCIN#(1st) eSPI Mode:ESPI_ALERT1#(3rd) (HEDT/WS Only)	Native RCIN#	PU 10K to S5	+3V3_S5	Reserve SIO_KBRST#	Native	NA		
GPP_A1	S5	1.8V or 3.3V	LPC mode: LAD0(1st) eSPImode:ESPI_IO0(3rd)	Native LAD0	NA	NA	LPC_AD0	Native	NA		
GPP_A2	S5	1.8V or 3.3V	LPC mode: LAD1(1st) eSPI mode:ESPI_IO1(3rd)	Native LAD1	NA	NA	LPC_AD1	Native	NA		
GPP_A3	S5	1.8V or 3.3V	LPC mode: LAD2()1st eSPI mode:ESPI_IO2(3rd)	Native LAD2	NA	NA	LPC_AD2	Native	NA		
GPP_A4	S5	1.8V or 3.3V	LPC mode: LAD3(1st) eSPI mode:ESPI_IO3(3rd)	Native LAD3	NA	NA	LPC_AD3	Native	NA		
GPP_A5	S5	1.8V or 3.3V	LPC mode:LFRAME#(1st) eSPI mode:ESPI_CS#(3rd)	Native LFRAME#	NA	NA	LPC_FRAME#	Native	NA		
GPP_A6	S5	1.8V or 3.3V	LPC Mode: SERIRQ(1st) eSPI Mode:ESPI_CS#1(3rd) (HEDT/WS Only)	Native SERIRQ	PU 10K to S0	+3V3	SER_IRQ	Native	NA		
GPP_A7	S5	1.8V or 3.3V	LPC Mode: PIRQA#(1st) eSPI Mode:ESPI_ALERT0#(3rd) (HEDT/WS Only)	Native PIRQA#	PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_A8	S5	1.8V or 3.3V	LPC Mode:CLKRUN# eSPI Mode: None	Native CLKRUN#	PU 10K to S5	+3V3_S5	CLKRUN#_PCH	NA	NA		
GPP_A9	S5	1.8V or 3.3V	LPC mode:CLKOUT_LPC0(1st) eSPI mode:ESPI_CLK(3rd)	Native CLKOUT_LPC0	NA	NA	CK_P_24M_SIO	Native	NA		
GPP_A10	S5	1.8V or 3.3V	LPC Mode:CLKOUT_LPC1 eSPI Mode: None	Native CLKOUT_LPC1	NA	NA	CLKOUT_LPC	Native	NA		
GPP_A11	S5	1.8V or 3.3V	LPC mode: PME# eSPI mode: None	Native PME#	PU 10K to S5	+3V3_S5	SIO_PME#	Native	NA		
GPP_A12	S5	1.8V or 3.3V	BM_BUSY#(1st)/ISH_GP6(2nd) SX_EXIT_HOLDOFF#(3rd)	GPI	PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_A13	S5	1.8V or 3.3V	LPC mode:SUSWARN#/SUSPWRDNACK eSPI mode: None	Native SUSWARN#	NA	NA	SUS_WARN#	Native	NA		
GPP_A14	S5	1.8V or 3.3V	LPC mode:SUS_STAT#(1st) eSPI mode:ESPI_RESET#(3rd)	Native SUS_STAT#	NA	NA	SUS_STAT#	Native	NA		
GPP_A15	S5	1.8V or 3.3V	LPC mode:SUS_ACK# eSPI mode: None	Native SUS_ACK#	PU 10K to S5	+3V3_S5	SUS_PWR_ACK#	Native	NA		
GPP_A16	S5	1.8V or 3.3V	CLKOUT_48(1st) (HEDT SKU Only)	Native or GPI	NA	NA	NA	NA	NA		Default depends on soft strap
GPP_A17	S5	1.8V or 3.3V	ISH_GP7	GPI	NA	NA	NA	NA	NA		
GPP_A18	S5	1.8V or 3.3V	ISH_GP0	GPI	NA	NA	NA	NA	NA		
GPP_A19	S5	1.8V or 3.3V	ISH_GP1	GPI	NA	NA	NA	NA	NA		
GPP_A20	S5	1.8V or 3.3V	ISH_GP2	GPI	NA	NA	NA	NA	NA		
GPP_A21	S5	1.8V or 3.3V	ISH_GP3	GPI	NA	NA	NA	NA	NA		
GPP_A22	S5	1.8V or 3.3V	ISH_GP4	GPI	NA	NA	NA	NA	NA		
GPP_A23	S5	1.8V or 3.3V	ISH_GP5	GPI	NA	NA	NA	NA	NA		
GPP_B0	S5	1.8V or 3.3V	None	GPO	NA	NA	NA	NA	NA		As GPIO,the signal defaults to'0'
GPP_B1	S5	1.8V or 3.3V	None	GPO	NA	NA	NA	NA	NA		As GPO,the signal default to "0"
GPP_B2	S5	1.8V or 3.3V	VRALERT#	GPI	PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_B3	S5	1.8V or 3.3V	CPU_GP2	GPI	NA	NA	NA	NA	NA		
GPP_B4	S5	1.8V or 3.3V	CPU_GP3	GPI	NA	NA	NA	NA	NA		
GPP_B5	S5	1.8V or 3.3V	SRCCLKREQ0#	GPI	NA	NA	NA	NA	NA		
GPP_B6	S5	1.8V or 3.3V	SRCCLKREQ1#	GPI	NA	NA	NA	NA	NA		
GPP_B7	S5	1.8V or 3.3V	SRCCLKREQ2#	GPI	NA	NA	NA	NA	NA		
GPP_B8	S5	1.8V or 3.3V	SRCCLKREQ3#	GPI	NA	NA	NA	NA	NA		
GPP_B9	S5	1.8V or 3.3V	SRCCLKREQ4#	GPI	PU 10K to S0	+3V3	PCIEX16_CLKREQ#	Native	NA		Map to CLKOUT PCIE P/N [5] and PCIeX16
GPP_B10	S5	1.8V or 3.3V	SRCCLKREQ5#	GPI	NA	NA	NA	NA	NA		
GPP_B11	S5	1.8V or 3.3V	None	GPO	NA	NA	NA	NA	NA		As GPO,the signal default to "0"
GPP_B12	S5	1.8V or 3.3V	SLP_S0#	Native SLP_S0#	Reserve PU 10K to S5	+3V3_S5	SLP_S0#	Native	NA		
GPP_B13	S5	1.8V or 3.3V	PLTRST#	Native PLTRST#	NA	NA	PLTRST_N	Native	NA		
GPP_B14	S5	1.8V or 3.3V	SPKR	GPO	NA	NA	SPKR	Native	NA		SMI#/NMI, starp, As GPIO,the signal defaults to'0'
GPP_B15	S5	1.8V or 3.3V	GSPI0_CS#	GPI	NA	NA	+	GPO	High:Control switch connect USB signal Low:Control switch connect COM signal	00=RSMRST#	
GPP_B16	S5	1.8V or 3.3V	GSPI0_CLK	GPI	NA	NA	NA	NA	NA		
GPP_B17	S5	1.8V or 3.3V	GSPI0_MISO	GPI	NA	NA	NA	NA	NA		
GPP_B18	S5	1.8V or 3.3V	GSPI0_MOSI	GPO	Reserve PU 1K to S5 Reserve PD 1K	+3V3_S5	PCH_STRAP_GPP_B18	NA	NA		Starp,As GPIO,the signal defaults to'0'
GPP_B19	S5	1.8V or 3.3V	GSPI1_CS#	GPI	NA	NA	NA	NA	NA		
GPP_B20	S5	1.8V or 3.3V	GSPI1_CLK	GPI	NA	NA	NA	NA	NA		[redacted]
GPP_B21	S5	1.8V or 3.3V	GSPI1_MISO	GPI	PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_B22	S5	1.8V or 3.3V	GSPI1_MOSI	GPO	Reserve PU 1K to S5 PD 10K	+3V3_S5	PCH_STRAP_BBS	NA	NA		Starp,As GPIO,the signal defaults to'0'
GPP_B23	S5	1.8V or 3.3V	SML1ALERT#(1st)/ PCHHOT#(2nd)	GPO	PU 150K to S5	+3V3_S5	PCH_STRAP_EXI_N	NA	NA		SMI#/NMI, starp, As GPIO,the signal defaults to'0'

PCH GPIO GPP C&D

GPIO Pin name	Power Well	Default Voltage	Native Fuanction	Default Status	Actual Power Well	Actual Voltage	Usage (BIOS CHECK)	Native or GPIO(Note1)	BootSet (BIOS Check)	Pad Reset Config (PADRSTCFG)(Note2)	Note
GPP_C0	S5	1.8V or 3.3V	SMBCLK	Native SMBCLK	PU 2.2K to S5	+3V3_S5	SMBCLK	Native	NA		
GPP_C1	S5	1.8V or 3.3V	SMBDATA	Native SMBDATA	PU 2.2K to S5	+3V3_S5	SMBDATA	Native	NA		
GPP_C2	S5	1.8V or 3.3V	SMBALERT#	GPO	PU 1K to S5 Reserve PD 10K	+3V3_S5	PCH_STRAP_TLS	NA	NA		Strap
GPP_C3	S5	1.8V or 3.3V	SML0CLK	Native SML0CLK	NA	NA	NA	NA	NA		
GPP_C4	S5	1.8V or 3.3V	SML0DATA	Native SML0DATA	NA	NA	NA	NA	NA		
GPP_C5	S5	1.8V or 3.3V	SML0ALERT#	GPO	Reserve PU 1K to S5 PD 10K	+3V3_S5	PCH_STRAP_ESPI_EN	NA	NA		Strap
GPP_C6	S5	1.8V or 3.3V	SML1CLK	GPI	Reserve PU 2.2K to S5	+3V3_S5	SML1_CLK	Native	NA		
GPP_C7	S5	1.8V or 3.3V	SML1DATA	GPI	Reserve PU 2.2K to S5	+3V3_S5	SML1_DAT	Native	NA		
GPP_C8	S5	1.8V or 3.3V	UART0_RXD	GPI	NA	NA	NA	NA	NA		
GPP_C9	S5	1.8V or 3.3V	UART0_TXD	GPI	NA	NA	NA	NA	NA		
GPP_C10	S5	1.8V or 3.3V	UART0_RTS#	GPI	NA	NA	NA	NA	NA		
GPP_C11	S5	1.8V or 3.3V	UART0_CTS#	GPI	NA	NA	NA	NA	NA		
GPP_C12	S5	1.8V or 3.3V	UART1_RXD(1st)/ ISH_UART1_RXD(2nd)	GPI	NA	NA	NA	NA	NA		
GPP_C13	S5	1.8V or 3.3V	UART1_TXD (1st)/ ISH_UART1_TXD(2nd)	GPI	NA	NA	NA	NA	NA		
GPP_C14	S5	1.8V or 3.3V	UART1_RTS#(1st)/ ISH_UART1_RTS#(2nd)	GPI	NA	NA	NA	NA	NA		
GPP_C15	S5	1.8V or 3.3V	UART1_CTS#(1st)/ ISH_UART1_CTS#(2nd)	GPI	NA	NA	NA	NA	NA		
GPP_C16	S5	1.8V or 3.3V	I2C0_SDA	GPI	Reserve PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_C17	S5	1.8V or 3.3V	I2C0_SCL	GPI	Reserve PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_C18	S5	1.8V or 3.3V	I2C1_SDA	GPI	Reserve PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_C19	S5	1.8V or 3.3V	I2C1_SCL	GPI	Reserve PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_C20	S5	1.8V or 3.3V	UART2_RXD	GPI	NA	NA	NA	NA	NA		
GPP_C21	S5	1.8V or 3.3V	UART2_TXD	GPI	NA	NA	NA	NA	NA		
GPP_C22	S5	1.8V or 3.3V	UART2_RTS#	GPI	NA	NA	LPC_SMI#	GPI	High:No SMI Interrupt Low:SMI interrupt	00 = RSMRST#	SMI#/NMI,This SMI used for LPC debug header
GPP_C23	S5	1.8V or 3.3V	UART2_CTS#	GPI	PU 10K to S5	+3V3_S5	SIO2PCH_SMI#	GPI	High:No SMI Interrupt Low:SMI interrupt	00 = RSMRST#	SMI#/NMI,This SMI used for SIO
GPP_D0	S5	1.8V or 3.3V	None	GPI	NA	NA	NA	NA	NA		[redacted]
GPP_D1	S5	1.8V or 3.3V	None	GPI	NA	NA	NA	NA	NA		[redacted]
GPP_D2	S5	1.8V or 3.3V	None	GPI	NA	NA	NA	NA	NA		[redacted]
GPP_D3	S5	1.8V or 3.3V	None	GPI	NA	NA	NA	NA	NA		[redacted]
GPP_D4	S5	1.8V or 3.3V	ISH_I2C2_SDA(1st)/ I2C3_SDA(2nd)	GPI	Reserve PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_D5	S5	1.8V or 3.3V	I2S0_SFRM	GPI	NA	NA	NA	NA	NA		
GPP_D6	S5	1.8V or 3.3V	I2S0_TXD	GPI	NA	NA	NA	NA	NA		
GPP_D7	S5	1.8V or 3.3V	I2S0_RXD	GPI	NA	NA	NA	NA	NA		
GPP_D8	S5	1.8V or 3.3V	I2S0_SCLK	GPI	NA	NA	NA	NA	NA		
GPP_D9	S5	1.8V or 3.3V	None	GPI	NA	NA	NA	NA	NA		
GPP_D10	S5	1.8V or 3.3V	None	GPI	NA	NA	NA	NA	NA		
GPP_D11	S5	1.8V or 3.3V	None	GPI	NA	NA	NA	NA	NA		
GPP_D12	S5	1.8V or 3.3V	None	GPI	NA	NA	NA	NA	NA		
GPP_D13	S5	1.8V or 3.3V	ISH_UART0_RXD(1st) /I2C_SDA(3rd)	GPI	Reserve PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_D14	S5	1.8V or 3.3V	ISH_UART0_TXD(1st) /I2C2_SCL(3rd)	GPI	Reserve PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_D15	S5	1.8V or 3.3V	ISH_UART0_RTS#	GPI	NA	NA	NA	NA	NA		
GPP_D16	S5	1.8V or 3.3V	ISH_UART0_CTS#	GPI	NA	NA	NA	NA	NA		
GPP_D17	S5	1.8V or 3.3V	DMIC_CLK1	GPI	NA	NA	NA	NA	NA		
GPP_D18	S5	1.8V or 3.3V	DMIC_DATA1	GPI	NA	NA	NA	NA	NA		
GPP_D19	S5	1.8V or 3.3V	DMIC_CLK0	GPI	NA	NA	NA	NA	NA		
GPP_D20	S5	1.8V or 3.3V	DMIC_DATA0	GPI	NA	NA	NA	NA	NA		
GPP_D21	S5	1.8V or 3.3V	None	GPI	NA	NA	NA	NA	NA		
GPP_D22	S5	1.8V or 3.3V	None	GPI	NA	NA	NA	NA	NA		
GPP_D23	S5	1.8V or 3.3V	ISH_I2C2_SCL(1st)/ I2C3_SCL(2nd)	GPI	Reserve PU 10K to S5	+3V3_S5	NA	NA	NA		

PCH GPIO GPP E&F

GPIO Pin name	Power Well	Default Voltage	Native Fuanction	Default Status	Actual Power Well	Actual Voltage	Usage (BIOS CHECK)	Native or GPIO(Note1)	BootSet (BIOS Check)	Pad Reset Config (PADRSTCFG)(Note2)	Note
GPP_E0	S5	1.8V or 3.3V	SATAXPCIE0(1st)/ SATAGP0(2nd)	Native SATAXPCIE0	NA	NA	NA	NA	NA		SMI#NMI.Default SATAXPCIEX is set by a soft strap. Default is GPI before soft straps are loaded
GPP_E1	S5	1.8V or 3.3V	SATAXPCIE1(1st)/ SATAGP1(2nd)	Native SATAXPCIE1	NA	NA	NA	NA	NA		
GPP_E2	S5	1.8V or 3.3V	SATAXPCIE2(1st) /SATAGP2(2nd)	Native SATAXPCIE2	NA	NA	NA	NA	NA		
GPP_E3	S5	1.8V or 3.3V	CPU_GP0	GPI	NA	NA	NA	NA	NA		[redacted]
GPP_E4	S5	1.8V or 3.3V	SATA_DEVSLP0	GPI	NA	NA	NA	NA	NA		[redacted]
GPP_E5	S5	1.8V or 3.3V	SATA_DEVSLP1	GPI	NA	NA	NA	NA	NA		[redacted]
GPP_E6	S5	1.8V or 3.3V	SATA_DEVSLP2	GPI	NA	NA	NA	NA	NA		[redacted]
GPP_E7	S5	1.8V or 3.3V	CPU_GP1	GPI	NA	NA	NA	NA	NA		[redacted]
GPP_E8	S5	1.8V or 3.3V	SATA_LED#	GPI	PU 10K to S0	+3V3	SATA_LED#	Native	NA		[redacted]
GPP_E9	S5	1.8V or 3.3V	USB_OC0#	GPI	PU 10K to S5	3.3V_S5	USB_OC_LAN# USB2:port1 /port2	Native	NA		
GPP_E10	S5	1.8V or 3.3V	USB_OC1#	GPI	PU 10K to S5	3.3V_S5	USB3.0_OC_BACK# USB2:port3/port4 USB3:port3/port4	Native	NA		
GPP_E11	S5	1.8V or 3.3V	USB_OC2#	GPI	PU 10K to S5	3.3V_S5	NA	NA	NA		
GPP_E12	S5	1.8V or 3.3V	USB_OC3#	GPI	PU 10K to S5	3.3V_S5	USB_OC_FRONT1# USB2:port7/port8 USB3:port1/port2	Native	NA		
GPP_F0	S5	1.8V or 3.3V	SATAXPCIE3(1st) /SATAGP3(2nd)	Native SATAXPCIE3	NA	NA	NA	NA	NA		Default SATAXPCIEX is set by a soft strap. Default is GPI before soft straps are loaded
GPP_F1	S5	1.8V or 3.3V	SATAXPCIE4(1st) /SATAGP4(2nd)	Native SATAXPCIE4	NA	NA	NA	NA	NA		
GPP_F2	S5	1.8V or 3.3V	SATAXPCIE5(1st) /SATAGP5(2nd)	Native SATAXPCIE5	NA	NA	NA	NA	NA		
GPP_F3	S5	1.8V or 3.3V	SATAXPCIE6(1st)/SATAGP6(2nd)(HEDT/WS Only)	Native SATAXPCIE6	Rerverse PU 10K to S0	+3V3	M2_SSD2_DET#	GPI	High:M2.2280 device Not detect Low:M2.2280 device detect	10 = PLTRET#	
GPP_F4	S5	1.8V or 3.3V	SATAXPCIE7(1st)/SATAGP7(2nd)(HEDT/WS Only)	Native SATAXPCIE7	NA	NA	NA	NA	NA		
GPP_F5	S5	1.8V or 3.3V	SATA_DEVSLP3	GPI	NA	NA	NA	NA	NA		
GPP_F6	S5	1.8V or 3.3V	SATA_DEVSLP4	GPI	NA	NA	NA	NA	NA		
GPP_F7	S5	1.8V or 3.3V	SATA_DEVSLP5	GPI	NA	NA	NA	NA	NA		
GPP_F8	S5	1.8V or 3.3V	SATA_DEVSLP6(HEDT /WS Only)	GPI	NA	NA	NA	NA	NA		
GPP_F9	S5	1.8V or 3.3V	SATA_DEVSLP7(HEDT /WS Only)	GPI	NA	NA	NA	NA	NA		
GPP_F10	S5	1.8V or 3.3V	SCLOCK	GPI	Reserve PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_F11	S5	1.8V or 3.3V	SLOAD	GPI	Reserve PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_F12	S5	1.8V or 3.3V	SDATAOUT1	GPI	Reserve PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_F13	S5	1.8V or 3.3V	SDATAOUT2	GPI	Reserve PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_F14	S5	1.8V or 3.3V	None	GPI	PU 10K to S5	+3V3_S5	H_SKTOCC#	GPI	High:CPU Not detect Low:CPU Not detect	00 = RSMRST#	
GPP_F15	S5	1.8V or 3.3V	USB_OC4#	GPI	PU 10K to S5	+3V3_S5	USB_OC_FRONT2# USB2:port5/port6	Native	NA		
GPP_F16	S5	1.8V or 3.3V	USB_OC5#	GPI	PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_F17	S5	1.8V or 3.3V	USB_OC6#	GPI	PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_F18	S5	1.8V or 3.3V	USB_OC7#	GPI	PU 10K to S5	+3V3_S5	NA	NA	NA		
GPP_F19	S5	1.8V or 3.3V	eDP_VDDEN	GPI	NA	NA	NA	NA	NA		
GPP_F20	S5	1.8V or 3.3V	eDP_BKLTEN	GPI	NA	NA	NA	NA	NA		
GPP_F21	S5	1.8V or 3.3V	eDP_BKLTCTL	GPI	NA	NA	NA	NA	NA		
GPP_F22	S5	1.8V or 3.3V	None	GPI	NA	NA	NA	NA	NA		
GPP_F23	S5	1.8V or 3.3V	None	GPI	NA	NA	NA	NA	NA		

PCH GPIO GPP G&H

GPIO Pin name	Power Well	Default Voltage	Native Fuanction	Default Status	Actual Power Well	Actual Voltage	Usage (BIOS CHECK)	Native or GPIO(Note1)	BootSet (BIOS Check)	Pad Reset Config (PADRSTCFG)(Note2)	Note
GPP_G0	S5	1.8V or 3.3V	FAN_TACH_0 (HEDT Only)	GPI	Reserve PU 10k to S0 PD 10K	+3V3	BRD_ID0	GPI	High:Set BRD_ID0 as 1 Low:Set BRD_ID0 as 0	10 = PLTRST#	
GPP_G1	S5	1.8V or 3.3V	FAN_TACH_1 (HEDT Only)	GPI	PU 10k to S0 Reserve PD 10K	+3V3	BRD_ID1	GPI	High:Set BRD_ID1 as 1 Low:Set BRD_ID1 as 0	10 = PLTRST#	
GPP_G2	S5	1.8V or 3.3V	FAN_TACH_2 (HEDT Only)	GPI	PU 10k to S0 Reserve PD 10K	+3V3	BRD_ID2	GPI	High:Set BRD_ID2 as 1 Low:Set BRD_ID2 as 0	10 = PLTRST#	To be used for future
GPP_G3	S5	1.8V or 3.3V	FAN_TACH_3 (HEDT Only)	GPI	PU 10k to S0 Reserve PD 10K	+3V3	BRD_ID3	GPI	High:Set BRD_ID3 as 1 Low:Set BRD_ID3 as 0	10 = PLTRST#	
GPP_G4	S5	1.8V or 3.3V	FAN_TACH_4 (HEDT Only)	GPI	PU 10k to S0 Reserve PD 10K	+3V3	BRD_ID4	GPI	High:Set BRD_ID4 as 1 Low:Set BRD_ID4 as 0	10 = PLTRST#	
GPP_G5	S5	1.8V or 3.3V	FAN_TACH_5 (HEDT Only)	GPI	PU 10k to S0 Reserve PD 10K	+3V3	BRD_ID5	GPI	High:Set BRD_ID5 as 1 Low:Set BRD_ID5 as 0	10 = PLTRST#	
GPP_G6	S5	1.8V or 3.3V	FAN_TACH_6 (HEDT Only)	GPI	PU 10k to S0	+3V3	CLR_CMOS	GPI	High:Not Clear CMOS Low:Clear CMOS	10 = PLTRST#	
GPP_G7	S5	1.8V or 3.3V	FAN_TACH_7 (HEDT Only)	GPI	NA	NA	NA	NA	NA		
GPP_G8	S5	1.8V or 3.3V	FAN_PWM_0 (HEDT Only)	Native	NA	NA	NA	NA	NA		
GPP_G9	S5	1.8V or 3.3V	FAN_PWM_1 (HEDT Only)	Native	NA	NA	NA	NA	NA		
GPP_G10	S5	1.8V or 3.3V	FAN_PWM_2 (HEDT Only)	Native	NA	NA	NA	NA	NA		
GPP_G11	S5	1.8V or 3.3V	FAN_PWM_3 (HEDT Only)	Native	NA	NA	NA	NA	NA		
GPP_G12	S5	1.8V or 3.3V	GSXDOUT	GPI	PU 10k to S0	+3V3	FRONT_USB3_DET#	GPI	High:Front USB2.0 not detect Low:Front USB2.0 detect	10 = PLTRST#	
GPP_G13	S5	1.8V or 3.3V	GSXSLOAD	GPI	Reserve PU 10k to S0	+3V3	FRONT_USB2_DET#	GPI	High:Front USB3.0 not detect Low:Front USB3.0 detect	10 = PLTRST#	
GPP_G14	S5	1.8V or 3.3V	GSXDIN	GPI	NA	NA	PCH_USB_UART_EN	GPO&GPI	High:Select USB port Low:Select UART	00 = RSMRST#	
GPP_G15	S5	1.8V or 3.3V	GSXRESET#	GPI	NA	NA	NA	NA	NA		
GPP_G16	S5	1.8V or 3.3V	GSXCLK	GPI	PU 10k to S0	+3V3	F_AUDIO_DET#	GPI	High:F_Audio not detect Low:F_audio detect	10 = PLTRST#	The function is reserved
GPP_G17	S5	1.8V or 3.3V	ADR_COMPLETE	GPI	PU 10k to S5	+3V3_DUAL_S5	FRONTLED_GPIO_1	GPO	High: Light Front LED Low: Shut Front LED	00 = RSMRST#	
GPP_G18	S5	1.8V or 3.3V	NMI#	GPI	PU 10k to S5	+3V3_DUAL_S5	FRONTLED_GPIO_2	GPO	High: Light Front LED Low: Shut Front LED	00 = RSMRST#	
GPP_G19	S5	1.8V or 3.3V	SMI#	GPI	PU 10k to S5	+3V3_DUAL_S5	FRONTLED_GPIO_3	GPO	High: Light Front LED Low: Shut Front LED	00 = RSMRST#	
GPP_G20	S5	1.8V or 3.3V	None	GPI	PU 10k to S5	+3V3_DUAL_S5	REARLED_GPIO_4	GPO	High: Light Front LED Low: Shut Front LED	00 = RSMRST#	
GPP_G21	S5	1.8V or 3.3V	None	GPI	PU 10k to S5	+3V3_DUAL_S5	REARLED_GPIO_5	GPO	High: Light Front LED Low: Shut Front LED	00 = RSMRST#	
GPP_G22	S5	1.8V or 3.3V	None	GPI	PU 10k to S5	+3V3_DUAL_S5	REARLED_GPIO_6	GPO	High: Light Front LED Low: Shut Front LED	00 = RSMRST#	
GPP_G23	S5	1.8V or 3.3V	None	GPI	NA	NA	JDUSTY2_GPIO	GPO	High:JDUSTY2 detect Low: JDUSTY2 not detect	10 = PLTRST#	
GPP_H0	S5	1.8V or 3.3V	SRCCLKREQ6#	GPI	PU 10k to S0	+3V3	PCIE_RTL_CLKREQ6#	NA	NA		
GPP_H1	S5	1.8V or 3.3V	SRCCLKREQ7#	GPI	PU 10k to S0	+3V3	PCIE_RTL_CLKREQ7#	NA	NA		
GPP_H2	S5	1.8V or 3.3V	SRCCLKREQ8#	GPI	PU 10k to S0	+3V3	PCIE_RTL_CLKREQ8#	NA	NA		
GPP_H3	S5	1.8V or 3.3V	SRCCLKREQ9#	GPI	NA	NA	NA	Native	NA		
GPP_H4	S5	1.8V or 3.3V	SRCCLKREQ10#	GPI	ReservePU 10k to S0	+3V3	PCIE_RTL_CLKREQ10#	Native	NA		
GPP_H5	S5	1.8V or 3.3V	SRCCLKREQ11#	GPI	PU 10k to S0	+3V3_VDD_LAN_KILLER	PCIE_RIVT_CLKREQ11#	NA	NA		
GPP_H6	S5	1.8V or 3.3V	SRCCLKREQ12#	GPI	PU 10k to S0	+3V3	PCIE_RIVT_CLKREQ12#	Native	NA		
GPP_H7	S5	1.8V or 3.3V	SRCCLKREQ13#	GPI	PU 10k to S0	+3V3	CHASSIS_ID1	GPI	High:Set CHASSIS_ID1 as 1 Low:Set CHASSIS_ID1 as 0	10 = PLTRST#	For Fan curve
GPP_H8	S5	1.8V or 3.3V	SRCCLKREQ14#	GPI	PU 10k to S0	+3V3	CHASSIS_ID2	GPI	High:Set CHASSIS_ID2 as 1 Low:Set CHASSIS_ID2 as 0	10 = PLTRST#	
GPP_H9	S5	1.8V or 3.3V	SRCCLKREQ15#	GPI	PU 10k to S0	+3V3	COMM_B_DETECT#	GPI	High: COM not detect Low: COM detect	10 = PLTRST#	
GPP_H10	S5	1.8V or 3.3V	SML2CLK (HEDT Only)	GPI	NA	NA	NA	NA	NA		
GPP_H11	S5	1.8V or 3.3V	SML2DATA (HEDT Only)	GPI	NA	NA	NA	NA	NA		
GPP_H12	S5	1.8V or 3.3V	SML2ALERT# (HEDT/WS Only)	GPO	Reserve PU 10k to S5	+3V3_DUAL_S5	NA	NA	NA		Strap
GPP_H13	S5	1.8V or 3.3V	SML3CLK (HEDT Only)	GPI	NA	NA	NA	NA	NA		
GPP_H14	S5	1.8V or 3.3V	SML3DATA (HEDT Only)	GPI	NA	NA	NA	NA	NA		
GPP_H15	S5	1.8V or 3.3V	SML3ALERT# (HEDT Only)	GPI	NA	NA	NA	NA	NA		
GPP_H16	S5	1.8V or 3.3V	SML4CLK (HEDT Only)	GPI	NA	NA	NA	NA	NA		
GPP_H17	S5	1.8V or 3.3V	SML4DATA (HEDT Only)	GPI	NA	NA	NA	NA	NA		
GPP_H18	S5	1.8V or 3.3V	SML4ALERT# (HEDT Only)	GPI	NA	NA	NA	NA	NA		
GPP_H19	S5	1.8V or 3.3V	ISH_I2C0_SDA	GPI	NA	NA	NA	NA	NA		
GPP_H20	S5	1.8V or 3.3V	ISH_I2C0_SCL	GPI	NA	NA	NA	NA	NA		
GPP_H21	S5	1.8V or 3.3V	ISH_I2C1_SDA	GPI	NA	NA	NA	NA	NA		
GPP_H22	S5	1.8V or 3.3V	ISH_I2C1_SCL	GPI	NA	NA	NA	NA	NA		
GPP_H23	S5	1.8V or 3.3V	None	GPI	PU 8.2k to S5	+3V3_DUAL_S5	RING#	GPI wake	High:Not Wake system by com port Low:Wake system by com port	00 = RSMRST#	

Note1:Must keep the related registers of un-used pins(default is native or GPIO) as chipset default value.
Note2:Pad Reset Config(PADRSTCFG) registers must be well programmed follow this table, or HW curent leakage may occur.

PCH GPIO GPP I & GPD

GPIO Pin name	Power Well	Default Voltage	Native Fuanction	Default Status	Actual Power Well	Actual Voltage	Usage (BIOS CHECK)	Native or GPIO	BootSet (BIOS Check)	Note
GPP_I0	S5	3.3V	DDSP_HPD0	GPI	NA	NA	NA	NA	NA	
GPP_I1	S5	3.3V	DDSP_HPD1	GPI	NA	NA	NA	NA	NA	
GPP_I2	S5	3.3V	DDSP_HPD2	GPI	PU 1M to S0	+3V3	DPD_HPD_R	Native	NA	
GPP_I3	S5	3.3V	DDSP_HPD3	GPI	NA	NA	NA	NA	NA	
GPP_I4	S5	3.3V	EDP_HPD	GPI	PD 100k	NA	NA	NA	NA	
GPP_I5	S5	3.3V	DDPB_CTRLCLK	GPI	NA	NA	NA	NA	NA	
GPP_I6	S5	3.3V	DDPB_CTRLDATA	GPO	NA	NA	NA	NA	NA	
GPP_I7	S5	3.3V	DDPC_CTRLCLK	GPI	NA	NA	NA	Native	NA	
GPP_I8	S5	3.3V	DDPC_CTRLDATA	GPO	NA	NA	NA	Native	NA	
GPP_I9	S5	3.3V	DDPD_CTRLCLK	GPI	PU 2.2K to S0	+3V3V	DDPD_CTRLCLK	Native	NA	
GPP_I10	S5	3.3V	DDPD_CTRLDATA	GPO	PU 2.2K to S0	+3V3V	DDPD_CTRLDATA	Native	NA	
GPD0	DSW	3.3V	BATLOW#	Native	PU 10k to DSW	+3V3_DSW	NA	NA	NA	
GPD1	DSW	3.3V	ACPRESENT	Native	PU 10k to DSW	+3V3_DSW	NA	NA	NA	
GPD2	DSW	3.3V	LAN_WAKE#	Native	PU 10k to DSW	+3V3_DSW	LAN_WAKE#	Native	NA	
GPD3	DSW	3.3V	PWRBTN#	Native	PU 4.7k to DSW	+3V3_DSW	PWRBTN_OUT#	Native	NA	
GPD4	DSW	3.3V	SLP_S3#	Native	NA	NA	SLP_S3#	Native	NA	
GPD5	DSW	3.3V	SLP_S4#	Native	NA	NA	SLP_S4#	Native	NA	
GPD6	DSW	3.3V	SLP_A#	Native	NA	NA	NA	NA	NA	
GPD7	DSW	3.3V	Reserved Functionality	Native	NA	NA	NA	NA	NA	
GPD8	DSW	3.3V	SUSCLK	Native	NA	NA	SUSCLK_PCH	Native	NA	
GPD9	DSW	3.3V	SLP_WLAN#	Native	NA	NA	NA	NA	NA	
GPD10	DSW	3.3V	SLP_S5#	Native	NA	NA	NA	NA	NA	
GPD11	DSW	3.3V	LANPHYPC	Native	NA	NA	NA	NA	NA	

Strapping

Signal	Usage	When Sampled	Comment
SMBALERT#/ GPP_C2	TLS CONFIDENTIALITY 0: DISABLE 1: ENABLE (DEFAULT)	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). 1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality).
GSPI0_MOSI/ GPP_B18	NO REBOOT 0: DISABLE (DEFAULT) 1: ENABLE	Rising edge of PCH_PWROK	The signal has a weak internal pull-down. 0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.
SML0ALERT#/ GPP_C5	ESPI ENABLE STRAP 0: LPC 1: ESPI	Rising edge of RSMRST#	This signal has a weak internal pull-down. 0 = LPC Is selected for EC. (Default) 1 = eSPI Is selected for EC.
GSPI1_MOSI/ GPP_B22	BOOT BIOS STRAP 0: SPI 1: ESPI/LPC	Rising edge of PCH_PWROK	This Signal has a weak internal pull-down. This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Bus0, Device31, Function0, offset BCh, bit 6). Bit 6 Boot BIOS Destination 0 SPI (Default) 1 LPC
SML1ALERT#/ PCHHOT#/ GPP_B23	EXI BOOT STALLBYPASS STRAP 0: DISABLE (DEFAULT) 1: ENABLE	Rising edge of RSMRST#	This signal has an internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
GPP_H12	ESPI FLASH SHARING MODE STRAP 0: DISABLE (DEFAULT) 1: SLAVE ATTACHED FLASH SHARING	Rising edge of RSMRST#	This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MISO	JTAG ODT DISABLE STRAP(DFX) 0: DISABLE 1: ENABLE	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_MOSI	BOOT HALF STRAP(DFX) 0: ENABLE 1: DISABLE (PCH INT PULL-UP)	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2	CONSENT STRAP(DXF) 0: ENABLE 1: DISABLE	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	PERSONALITY STRAP(DXF) 0: ENABLE 1: DISABLE	Rising edge of RSMRST#	This signal has an internal pull-up. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

SIO GPIO

GPIO Pin name	Power Well	Default Voltage	Native Fuanction	Default Status	Actual Power Well	Actual Voltage	Usage (BIOS CHECK)	Native or GPIO	BootSet (BIOS Check)	Note
GP10	AVCC3	3.3V	PCIRST3#/CIRRX1	CIRRX1	1K PU to +3.3V_S5	+3.3V_S5	FP_GRNLED	GPO	NA	
GP11	AVCC3	3.3V	PCIRST2#	PCIRST2#	10K PU to +3V3	+3V3	SIO_PCIRST2#	Native	NA	
GP12	AVCC3	3.3V	PCIRST1#/PCH_C0A	PCIRST1#	NA	NA	SIO_PCIRST1#	Native	NA	
GP13	AVCC3	3.3V	SLP_SUS_FET/5VSB_CTRL#	SLP_SUS_FET	10K PU to +5V_DSW	+5V_DSW	+5V_S5_EN#	Native	NA	
GP14	AVCC3	3.3V	CHARGP14	CHARGP14	10K PU to +3V3_S5	+3V3_S5	SIO2PCH_SMI#	GPO	NA	
GP15	AVCC3	3.3V	FAN_CTL4/ PCIRSTIN#/CIRTX2	FAN_CTL4	10K PU to +3V3	+3V3	SIO_PCIRST_IN	Native	NA	
GP16	AVCC3	3.3V	CIRRX2 /FAN_TAC4	FAN_TAC4	NA	NA	NA	NA	NA	
GP17	AVCC3	3.3V	RI2#	RI2#	10K PU to +3V3_DSW	+3V3_DSW	RI2#	Native	NA	
GP20	3VSB	3.3V	CTS2#	GP20	NA	NA	CTS2#	Native	NA	
GP21	3VSB	3.3V	DCD2#	GP21	NA	NA	DCD2#	Native	NA	
GP22	3VSB	3.3V	PCH_D0B	PCH_D0B	1K PU to +3V3	+3V3	FP_YLWLED	GPO	NA	
GP23	3VSB	3.3V	DPWROK	DPWROK	1K PU to 3V3_DSW	+3V3_DSW	PCH_DPWROK	Native	NA	
GP24	3VSB	3.3V	RST2#	GP24	NA	NA	RST2#	Native	NA	
GP25	3VSB	3.3V	DSR2#	GP25	NA	NA	DSR2#	Native	NA	
GP26	3VSB	3.3V	SOUT2	GP26	NA	NA	TXD2	Native	NA	
GP27	3VSB	3.3V	SIN2	GP27	NA	NA	RXD2	Native	NA	
GP30	AVCC3	3.3V	ATXPG	ATXPG	10K PU to +3V3	+3V3V	PWROK_PS	Native	NA	
GP31	AVCC3	3.3V	CTS1#/FAN_TAC5	CTS1#	NA	NA	CTS1#	Native	NA	
GP32	AVCC3	3.3V	RI1#	RI1#	8.2K PU to +3V3_S5	+3V3V_S5	RI1#	Native	NA	
GP33	AVCC3	3.3V	DCD1#/FAN_CTL5	DCD#	NA	NA	DCD1#	Native	NA	
GP34	AVCC3	3.3V	RSTCONIN	RSTCONIN	4.7K PU to +3V3_DSW	+3V3_DSW	SIO_RSTCONIN	Native	NA	
GP35	AVCC3	3.3V	RSTCONOUT	RSTCONOUT	NA	NA	NA	NA	NA	
GP36	AVCC3	3.3V	FAN_CTL3	FAN_CTL3	NA	NA	NA	NA	NA	
GP37	AVCC3	3.3V	FAN_TAC3	FAN_TAC3	NA	NA	NA	NA	NA	
GP40	AVCC3	3.3V	3VSBSW#/SCL0	3VSBSW#	NA	NA	3VSBSW3	Native	NA	
GP41	AVCC3	3.3V	SIN1	SIN1	NA	NA	RXD1	Native	NA	
GP42	AVCC3	3.3V	VCORE_EN/PCH_C0B /SUSWARN#	PCH_C0B	NA	NA	SUS_WARN#	Native	NA	
GP43	AVCC3	3.3V	SST/AMDTSI_D/PCH_D1	Ext sensor	2.2K PU to +3.3V_S5	+3.3V_S5	SML1_DATA	Native	NA	
GP44	AVCC3	3.3V	PECI/AMDTSI_C1	Ext sensor	NA	NA	H_PECI	Native	NA	
GP45	AVCC3	3.3V	DSR1#/PCH_D0A	DSR1#	NA	NA	DSR1#	Native	NA	
GP47	AVCC3	3.3V	NA	NA	NA	NA	NA	NA	NA	
GP050	AVCC3	3.3V	JP1	NA	NA	NA	SIO_JP1	Native	NA	
GP51	AVCC3	3.3V	FAN_CTL2	FAN_CTL2	NA	NA	SYS_FAN_PWM2	Native	NA	
GP52	AVCC3	3.3V	FAN_TAC2	FAN_TAC2	NA	NA	SYS_FAN_TACH2	Native	NA	
GP53	AVCC3	3.3V	SUSC#	SUSC#	NA	NA	SLP_S4#	Native	NA	
GP54	AVCC3	3.3V	PME#	PME#	10K PU to +3V3_S5	+3V3_S5	SIO_PME#	Native	NA	
GP55	AVCC3	3.3V	RSMRST#	RSMRST#	10K PU to +3V3_S5	+3V3_S5	SIO_RSMRST#	Native	NA	
GP56	AVCC3	3.3V	MCLK	MCLK	4.7k PU to +5V_DUAL_S3	+5V_DUAL_S3	MSCLK	Native	NA	
GP57	AVCC3	3.3V	MDAT	MDAT	4.7K PU to +5V_DUAL_S3	+5V_DUAL_S3	MADATA	Native	NA	
GP60	AVCC3	3.3V	KCLK	KCLK	4.7K PU to +5V_DUAL_S3	+5V_DUAL_S3	KBDCLK	Native	NA	
GP61	AVCC3	3.3V	KDAT	KDAT	4.7K PU to +5V_DUAL_S3	+5V_DUAL_S3	KBDDATA	Native	NA	
GP62	AVCC3	3.3V	KRST#	KRST#	NA	NA	SIO_KBRST#	Native	NA	
GP63	3VSB	3.3V	SLP_SUS3	SLP_SUS3	NA	NA	SLP_SUS#	Native	NA	
GP64	3VSB	3.3V	NA	GP64	NA	NA	NA	NA	NA	
GP65	3VSB	3.3V	VLDT_EN	GP65	NA	NA	NA	NA	NA	
GP66	3VSB	3.3V	SCL_1	GP66	NA	NA	NA	NA	NA	
GP67	3VSB	3.3V	SDA1	GP67	NA	NA	NA	NA	NA	
GP70	AVCC3	3.3V	PD0	PD0	NA	NA	XPD0	Native	NA	
GP71	AVCC3	3.3V	PD1	PD1	NA	NA	XPD1	Native	NA	
GP72	AVCC3	3.3V	PD2	PD2	NA	NA	XPD2	Native	NA	
GP73	AVCC3	3.3V	PD3	PD3	NA	NA	XPD3	Native	NA	
GP74	AVCC3	3.3V	PD4	PD4	NA	NA	XPD4	Native	NA	
GP75	AVCC3	3.3V	PD5	PD5	NA	NA	XPD5	Native	NA	
GP76	AVCC3	3.3V	PD6	PD6	NA	NA	XPD6	Native	NA	
GP77	AVCC3	3.3V	PD7/DIG0	PD7	NA	NA	XPD7	Native	NA	
GP80	AVCC3	3.3V	SLCT	SLCT#	NA	NA	SLCT	Native	NA	
GP81	AVCC3	3.3V	PE	PE#	NA	NA	PE	Native	NA	
GP82	AVCC3	3.3V	BUSY/DIG3	BUSY#	NA	NA	BUSY	Native	NA	
GP83	AVCC3	3.3V	ACK#/DIG2	ACK#	NA	NA	ACK#	Native	NA	
GP84	AVCC3	3.3V	SMBD_R1/SLIN#	SMBD_R	NA	NA	XSLIN#	Native	NA	
GP85	AVCC3	3.3V	SMBD_M1/INIT#	SMBD_M	NA	NA	XINIT#	Native	NA	
GP86	AVCC3	3.3V	SMBC_R1/AFD#	SMBC_R	NA	NA	XAFD#	Native	NA	
GP87	AVCC3	3.3V	SMBC_M1/STB#	SMBC_M	NA	NA	XSTB#	Native	NA	
GP90	3VSB	3.3V	FAN_CTL6	GP90	NA	NA	NA	NA	NA	
GP91	3VSB	3.3V	FAN_TAC6	GP91	NA	NA	NA	NA	NA	
GP92	3VSB	3.3V	NA	GP92	NA	NA	NA	NA	NA	
GP93	3VSB	3.3V	NA	GP93	10K PU to +3.3V_S5	+3V3_S5	H_SKTOCC#	GPI	NA	
GP94	3VSB	3.3V	NA	NA	NA	NA	NA	NA	NA	
GP95	3VSB	3.3V	NA	NA	NA	NA	NA	NA	NA	
GPA0	3VSB	3.3V	JP6	NA	8.2K PD to GND	NA	SIO_JP6	Native	NA	
GPA1	3VSB	3.3V	NA	NA	NA	NA	NA	NA	NA	
GPA2	3VSB	3.3V	PCH_C1	NA	2.2K PU to +3.3V_S5	+3V3_S5	SML1_CLK	Native	NA	
GPA3	3VSB	3.3V	AMDTSI_C2		NA	NA	NA	NA	NA	

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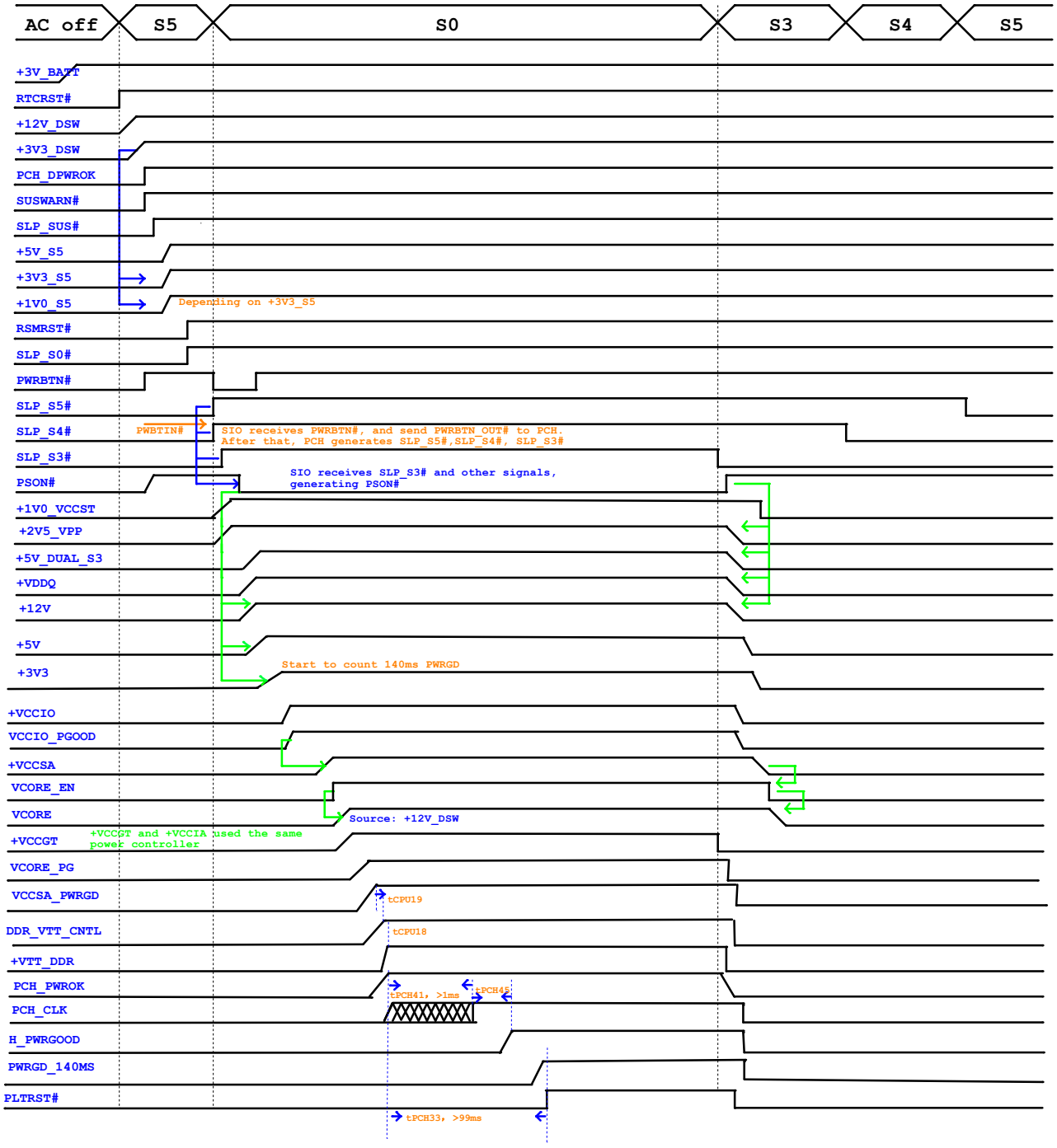
POWER SEQUENCE DIAGRAM



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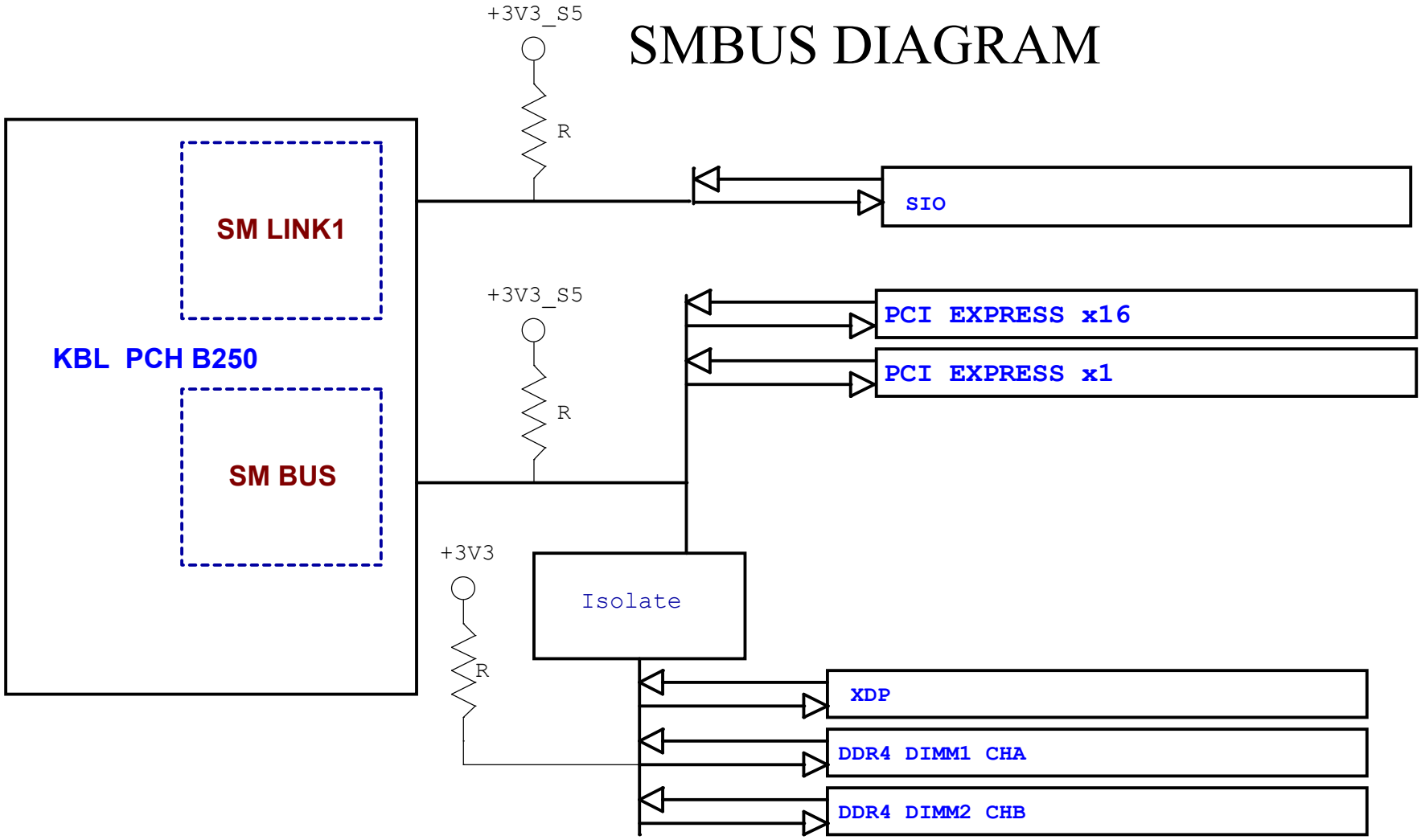
SMBUS DIAGRAM



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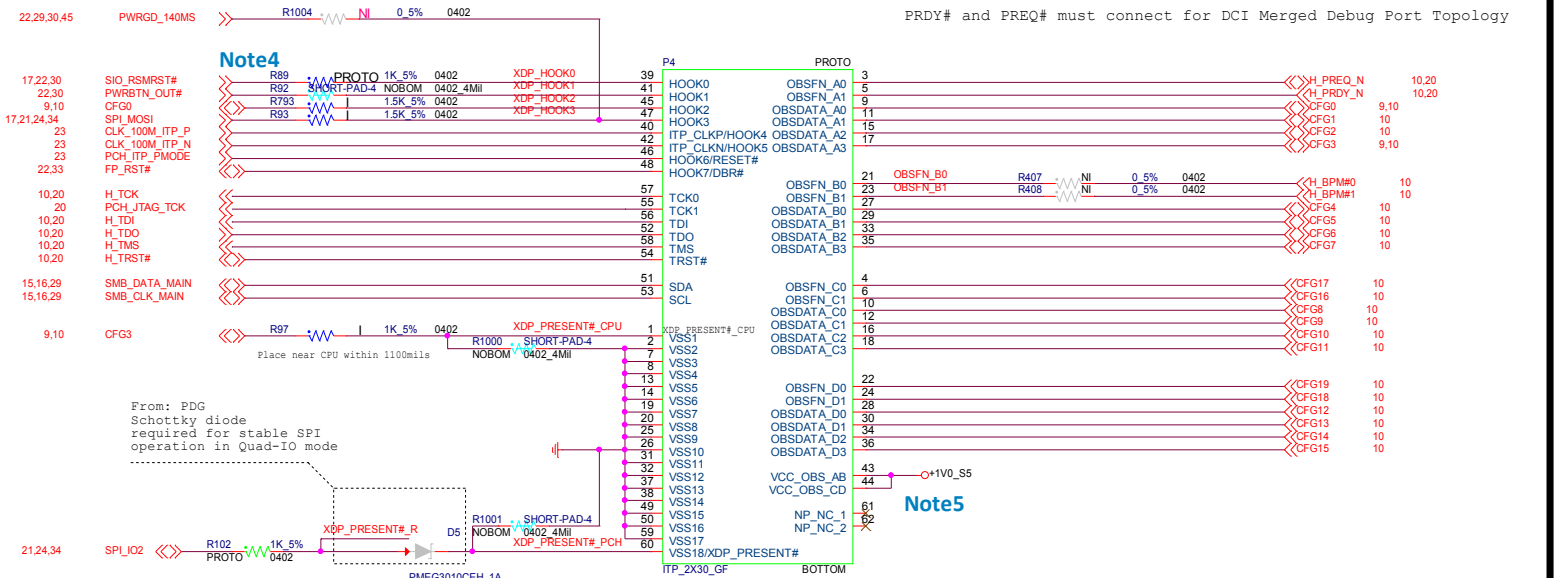
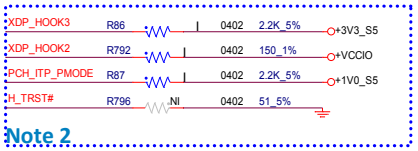
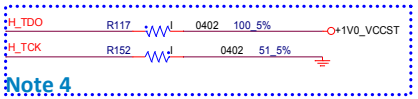
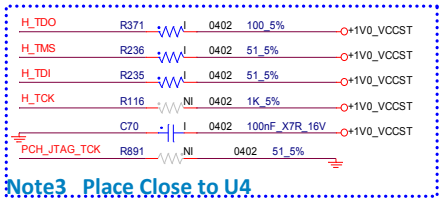
Intel MCP XDP Debug Connector



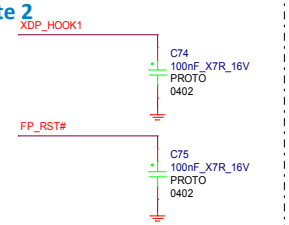
HW PU/PD Configuration







DeCoupling CAP



CFG Connection

Design Note

Note 1: XDP Connector Footprint

- NPI
- HMS2X30CZ
- MVB
- HMS2X30CZ_MVB_NP

Note 2

- C74 Place close to P4 Connector
- C75 Place close to P4 Connector
- R792 Place close to P4 Connector
- R86 Place close to P4 Connector
- R87 Place close to P4 Connector
- R796 Close P4

Note3

- R891 Place Close to U4 Within 1.1"
- R116 Place Close to U4 Within 1.1"
- R235 Place Close to U4 Within 1.5"
- R236 Place Close to U4 Within 1.5"
- R371 Place Close to U4 Within 1.5"
- C70 Place Close to R235, R236, R371

Note4

- R793 Place close to T Point
- R89 Place close to T Point
- R102 near PCH within 500mils (SPI_IO2)
- R93 Close to T-Point of SPI_MOSI < 1100mils
- R152 Place Close to CPU Within 1.5"
- R117 Place Close to CPU Within 1.5"

Note5

- P4.43 and P4.44 Power trace width = 10mils

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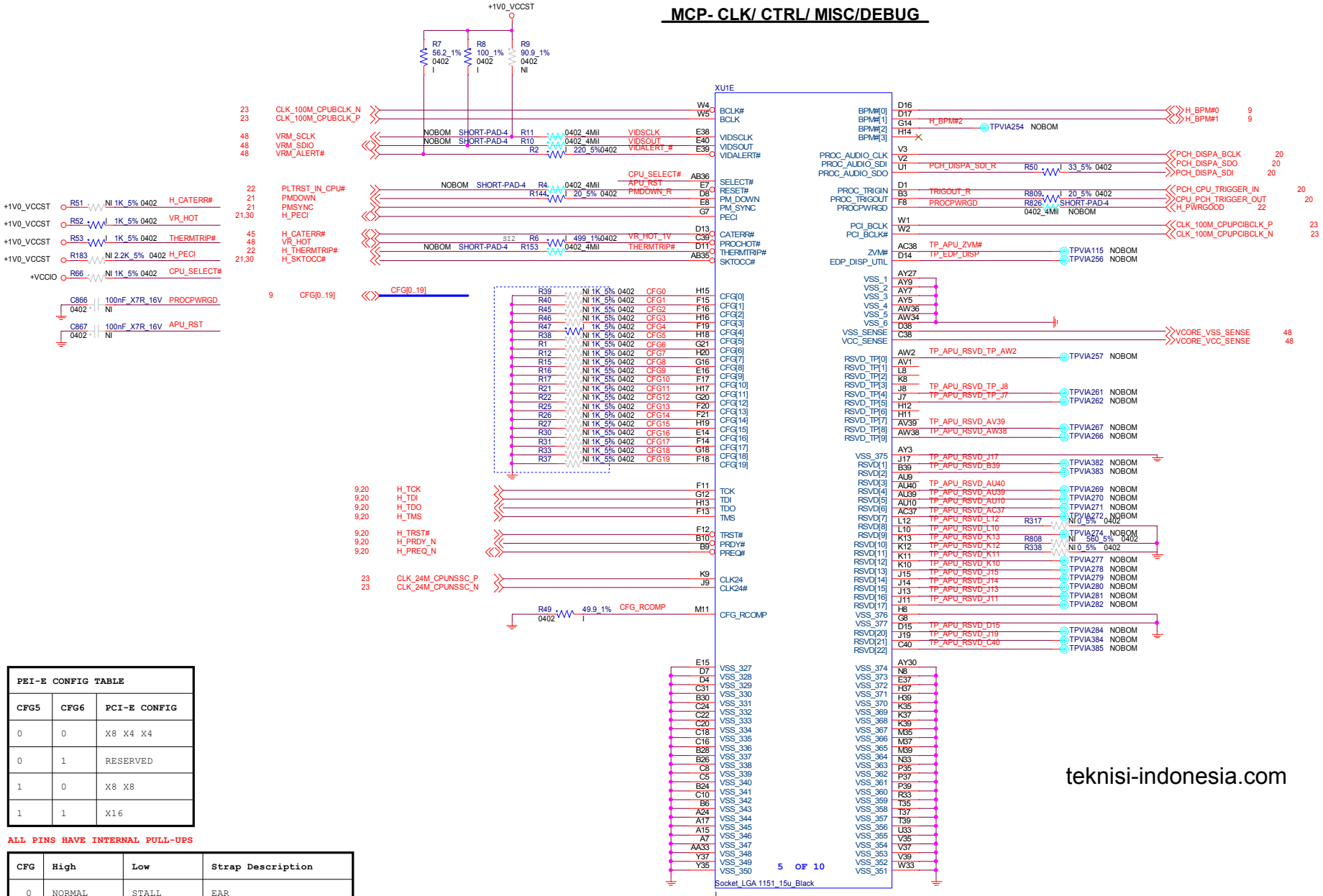
MCP- CLK/ CTRL/ MISC/DEBUG



PEI-E CONFIG TABLE		
CFG5	CFG6	PCI-E CONFIG
0	0	X8 X4 X4
0	1	RESERVED
1	0	X8 X8
1	1	X16

ALL PINS HAVE INTERNAL PULL-UPS

CFG	High	Low	Strap Description
0	NORMAL	STALL	EAR
1			RESERVED
2	NORMAL	REVERSE	PEG_LANE_REVERSAL
3			RESERVED
4	DISABLE	ENABLE "0"	eDP enable
5	see table above		PEG0CFGSEL[0] x16
6	see table above		PEG0CFGSEL[1] x16
7	RESET_N	BIOS REQ	PEG_DEFER_TRAINING
8-19			RESERVED

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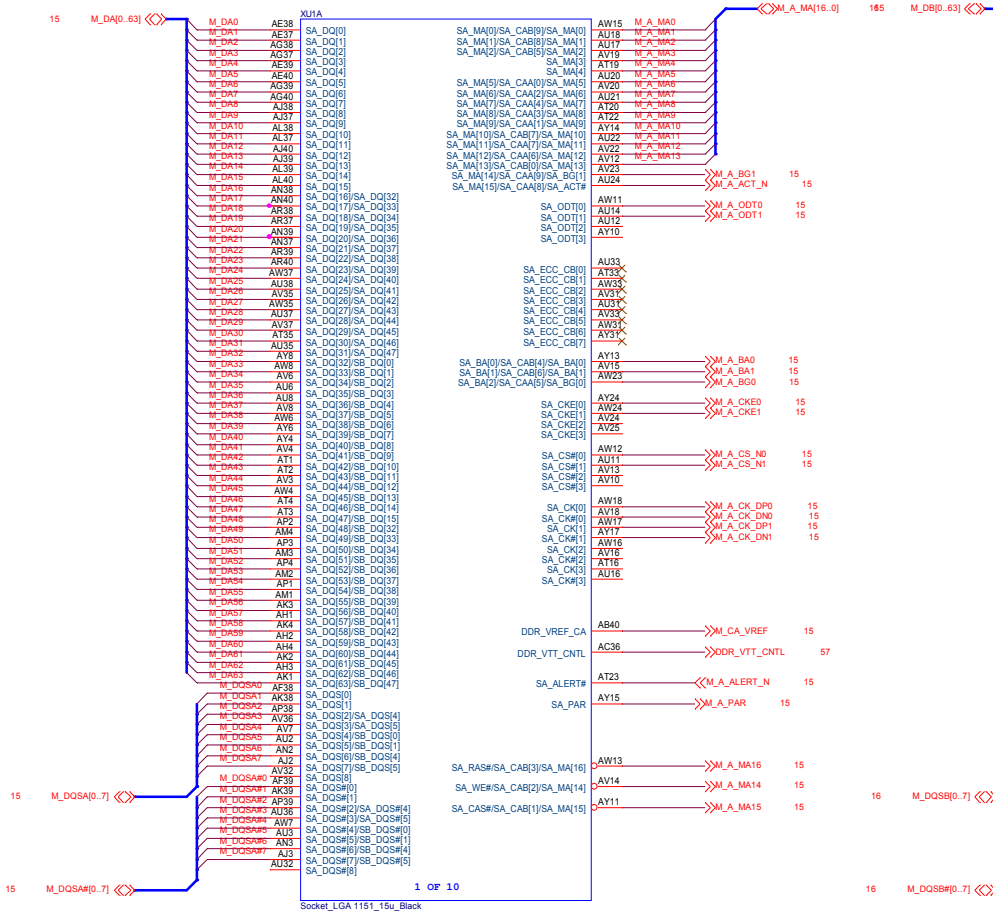
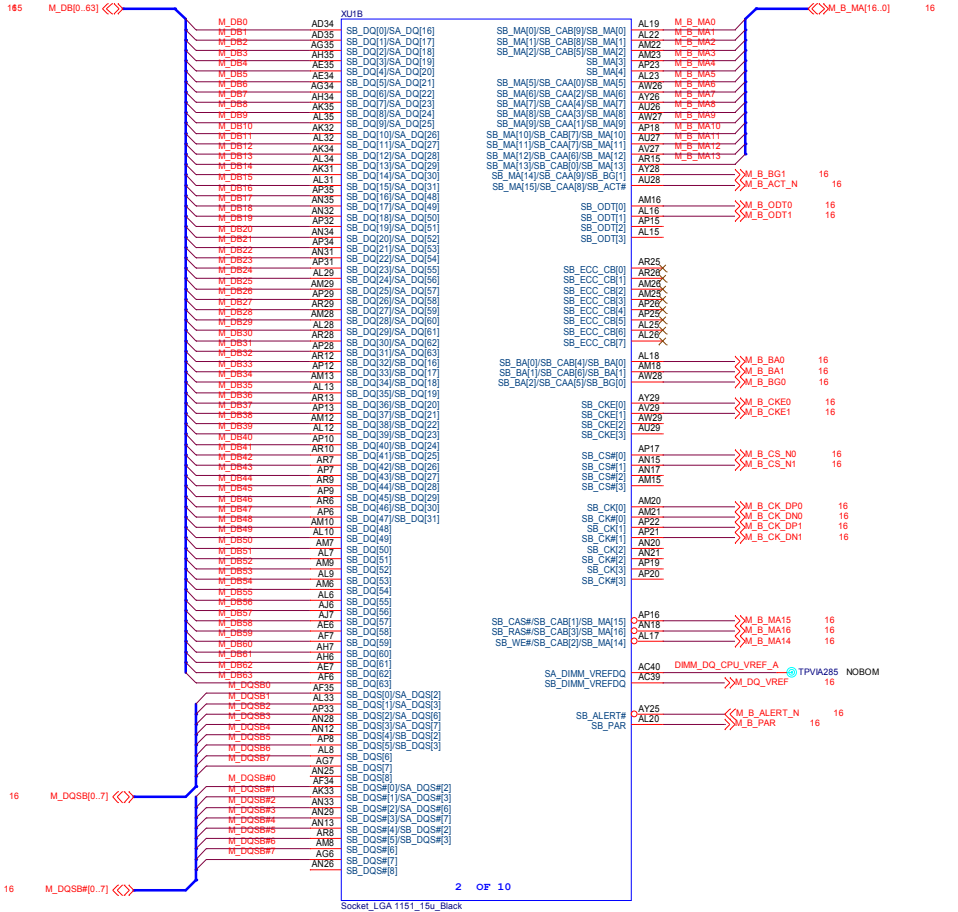
DDR4 CH-A

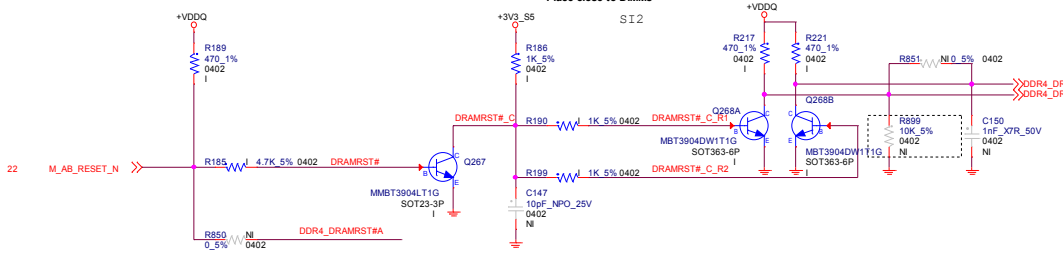


DDR4 CH-B



DDR4 DRAMRST# BUFFER CIRCUIT

Place close to DIMMs



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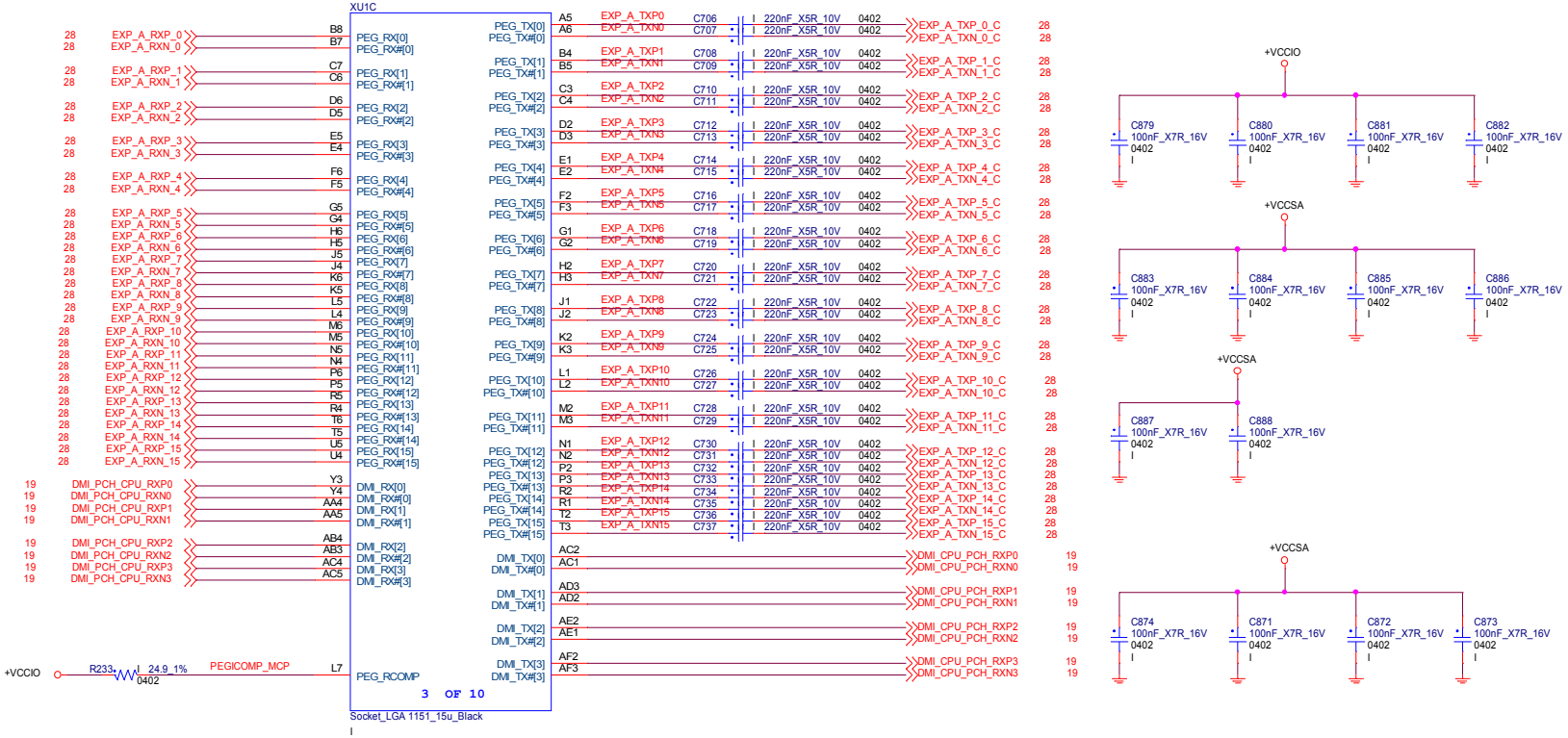
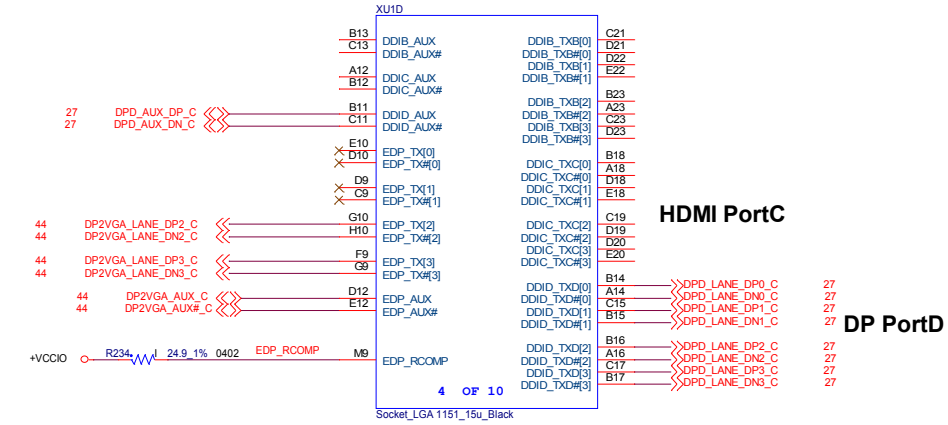
MCP - PCIE,DMI,FDI,DDI





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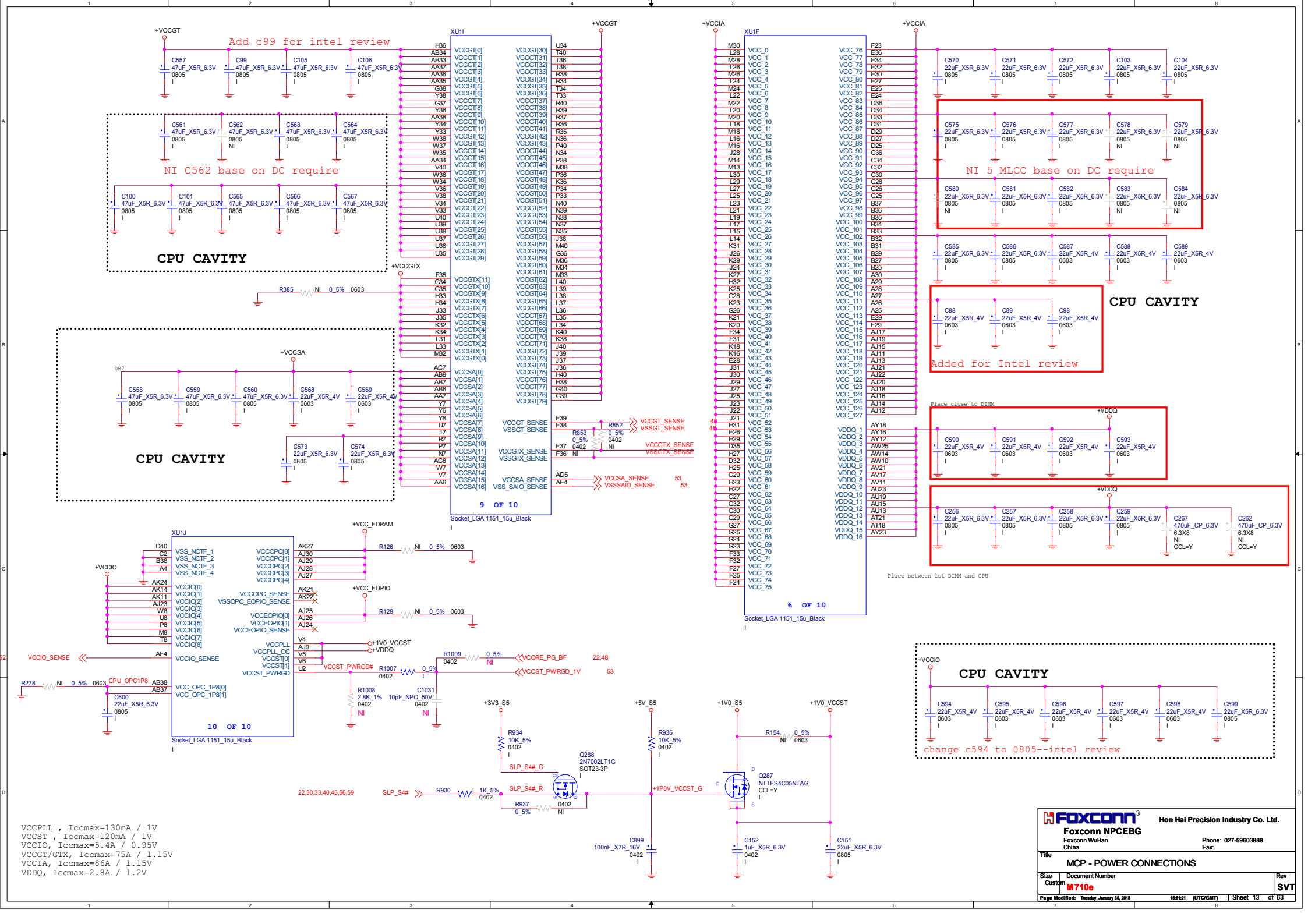

VCCPLL , Iccmax=130mA / 1V
VCCST , Iccmax=120mA / 1V
VCCIO, Iccmax=5.4A / 0.95V
VCCGT/GTX, Iccmax=75A / 1.15V
VCCIA, Iccmax=86A / 1.15V
VDDQ, Iccmax=2.8A / 1.2V

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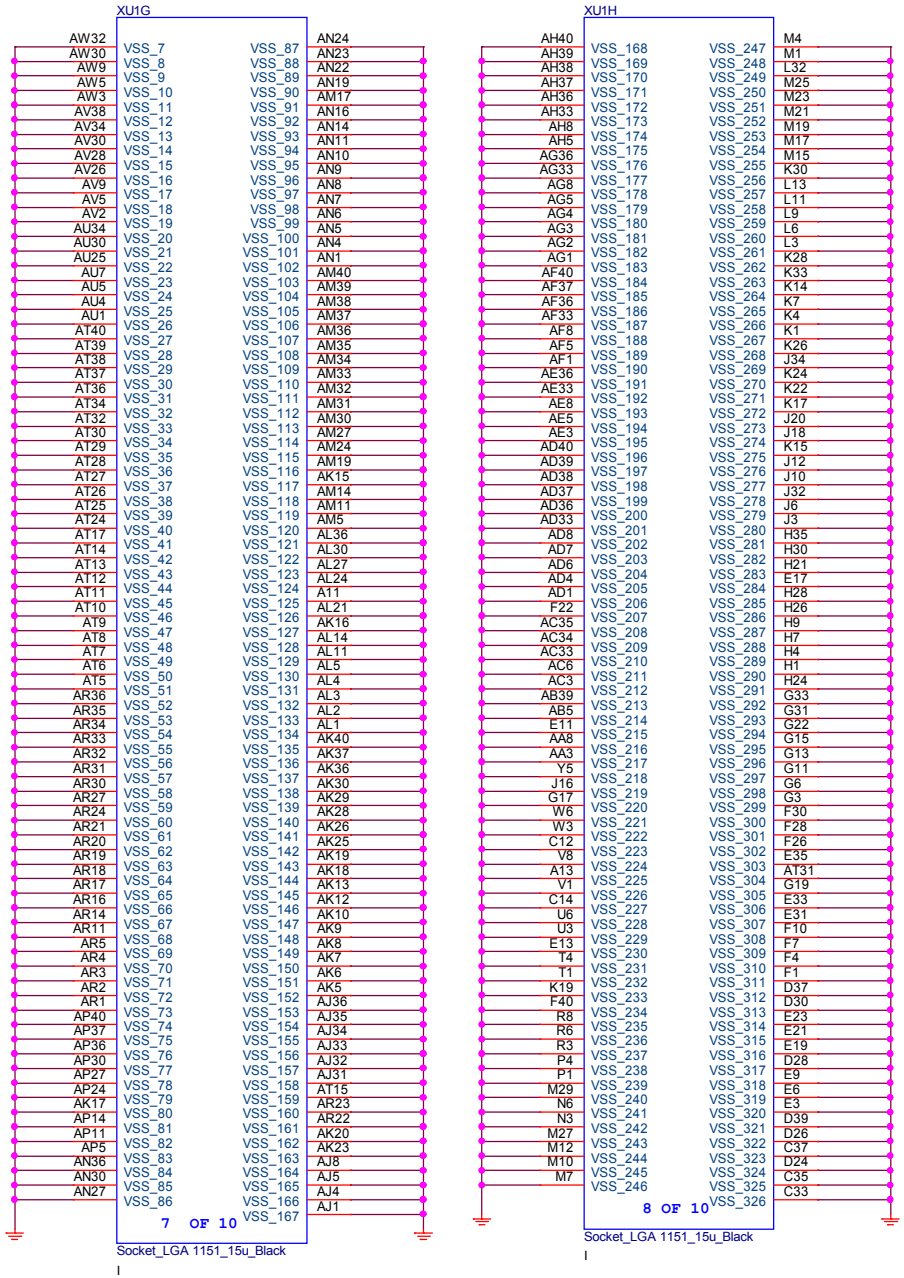

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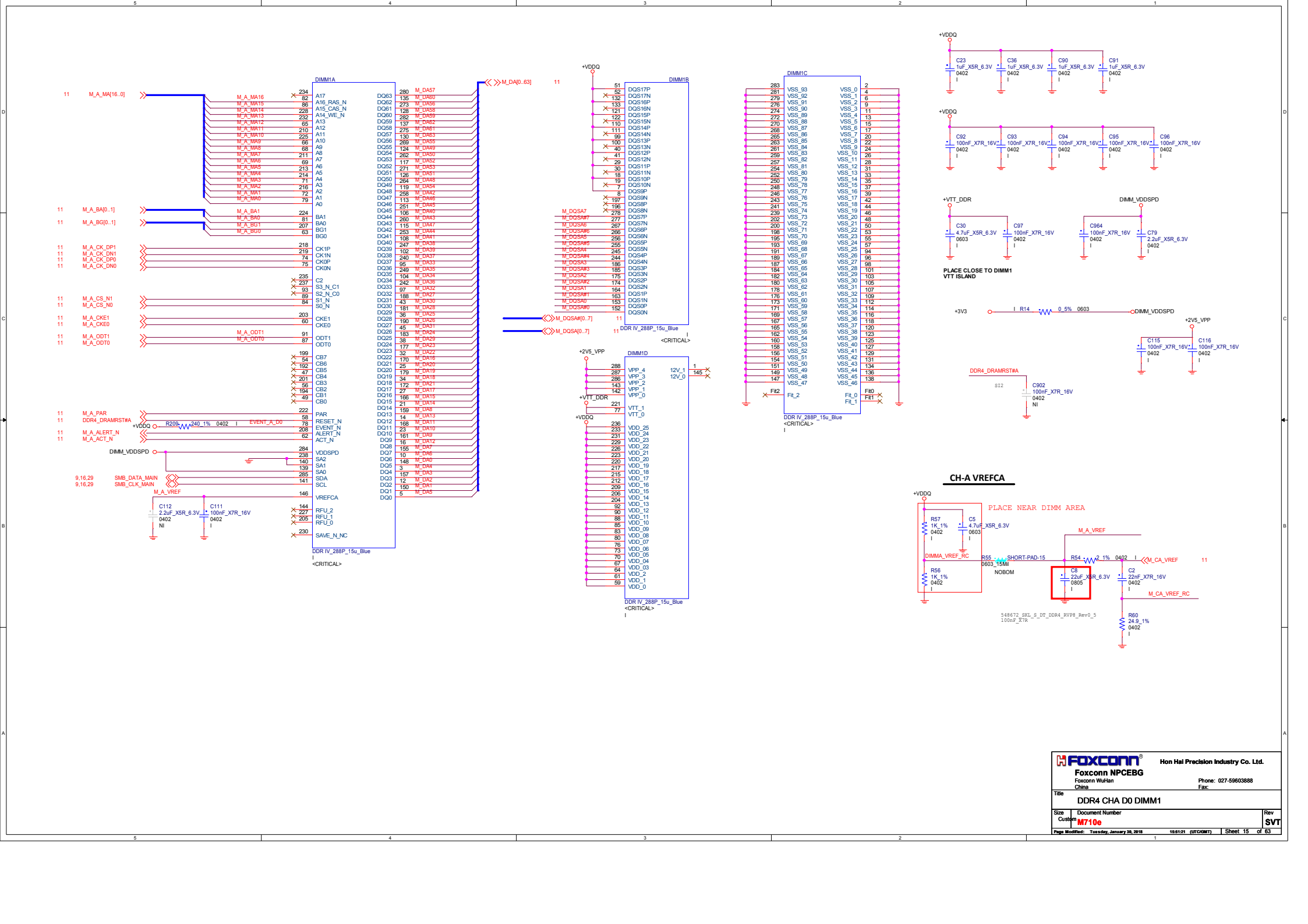

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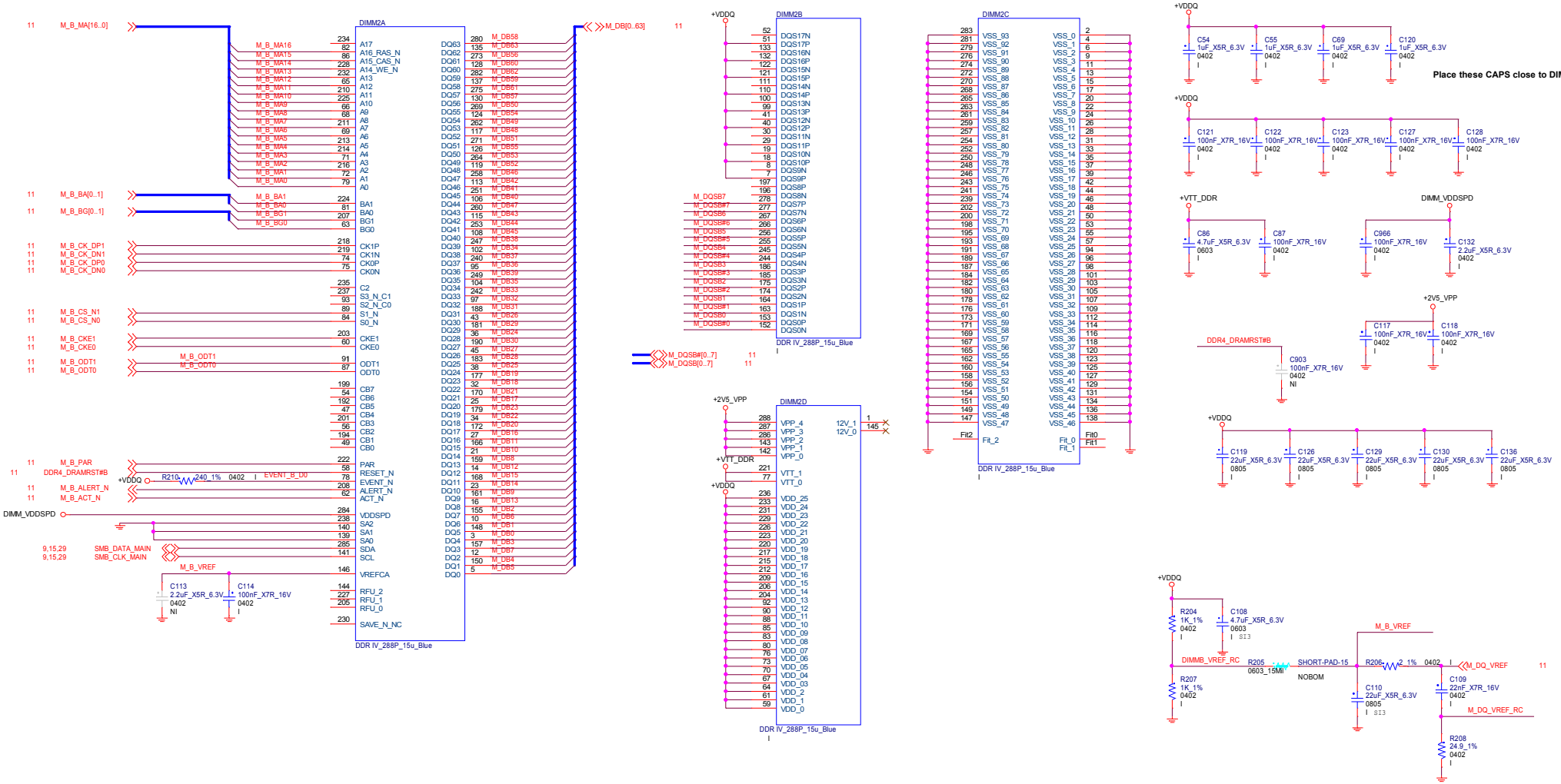

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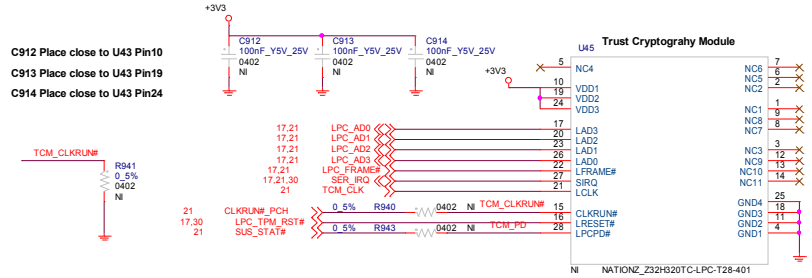
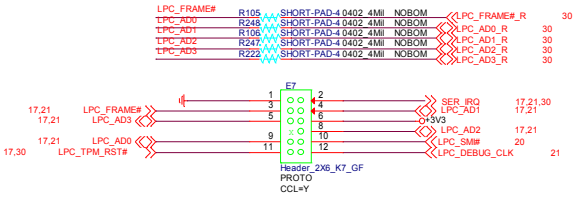
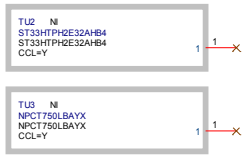






TPM-SPI Interface

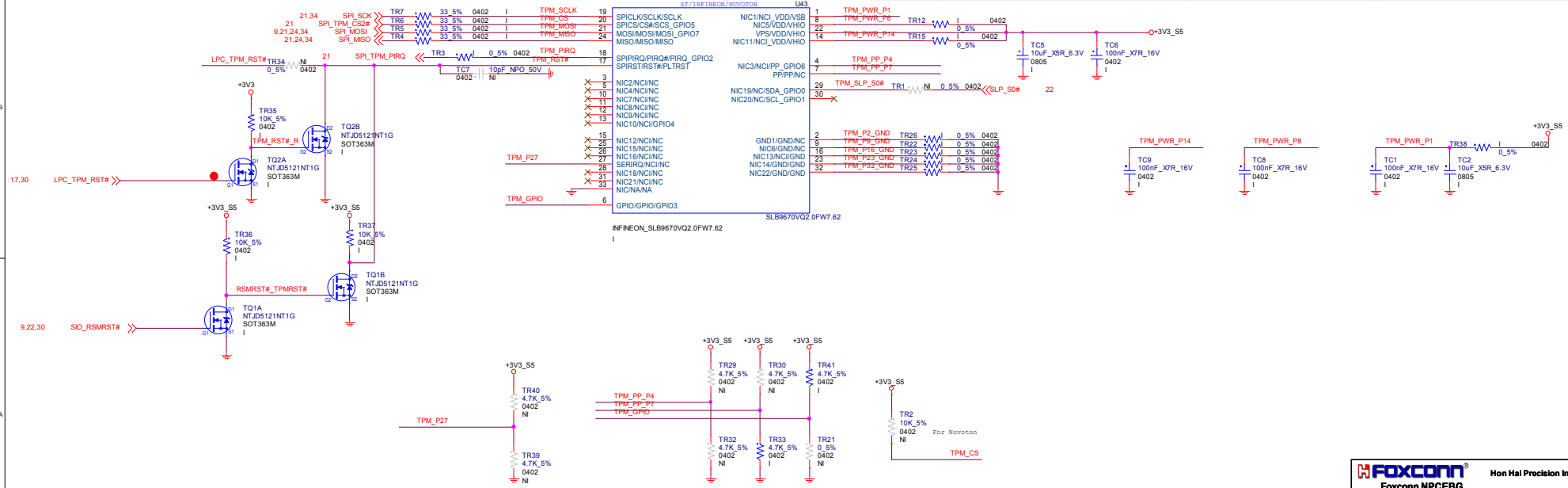
TPM

ST & NCT & Infineon co-lay

NPCT750LBAYX
ST33HTPH2E32AHB4
SLB9670VQ2.0FW7.62

PIN	SLB9670VQ2.0FW7.62	NPCT750	ST33HTPH2E32AHB4
1	TR38/TC1/TC2	TR38/TC1/TC2	NI
2	TR26	NI	TR26
7	TR33	NI	NI
8	TR12/TC8	TR12/TC8	NI
9	TR22	TR22	NI
14	TR15/TC9	TR15/TC9	NI
16	TR23	TR23	NI
23	TR24	TR24	NI
27	NI	TR39	NI
29	NI	TR1	NI
32	TR25	TR25	NI

Use 7.61 FW for ET phase since 7.62 not ready



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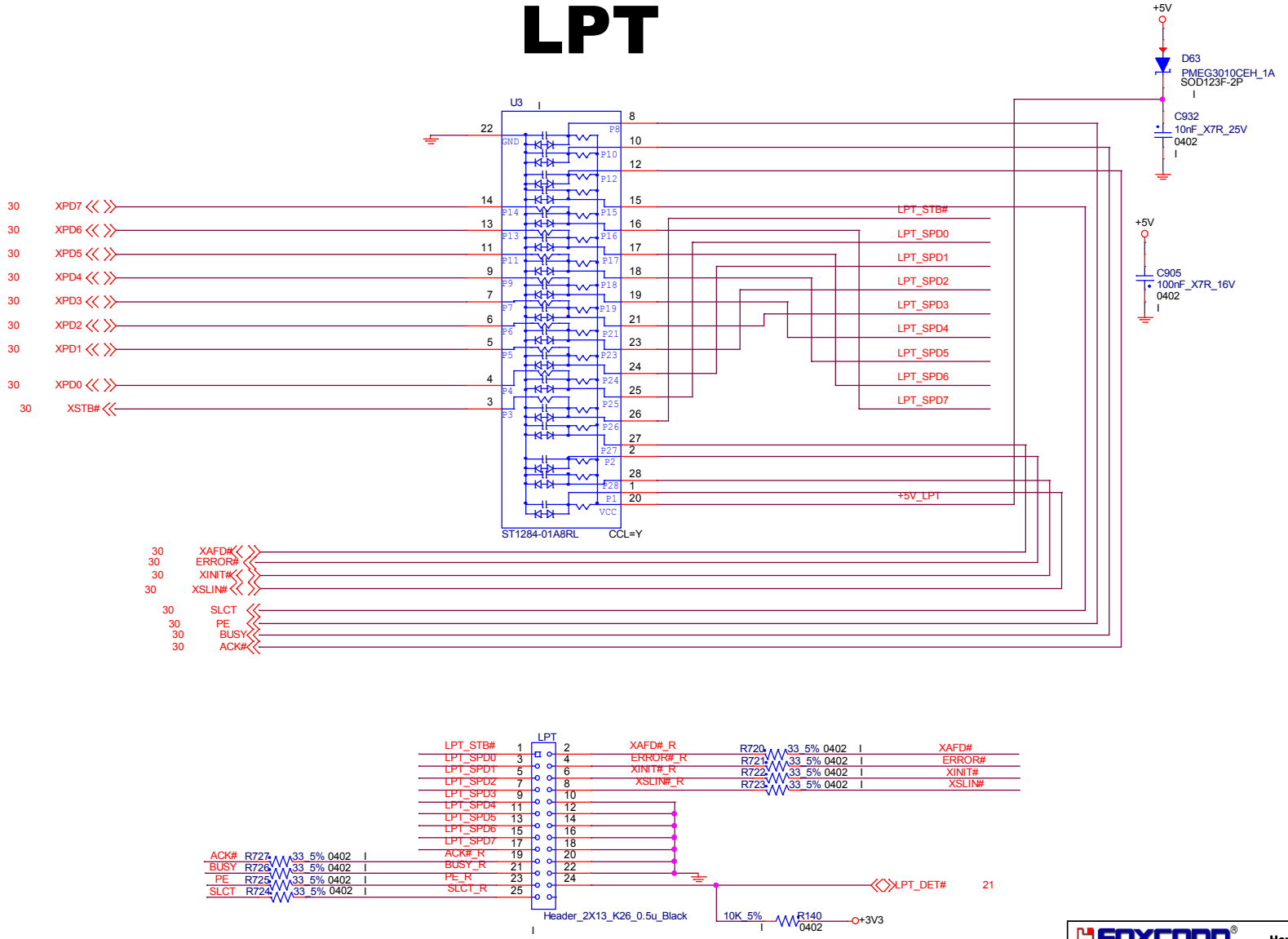

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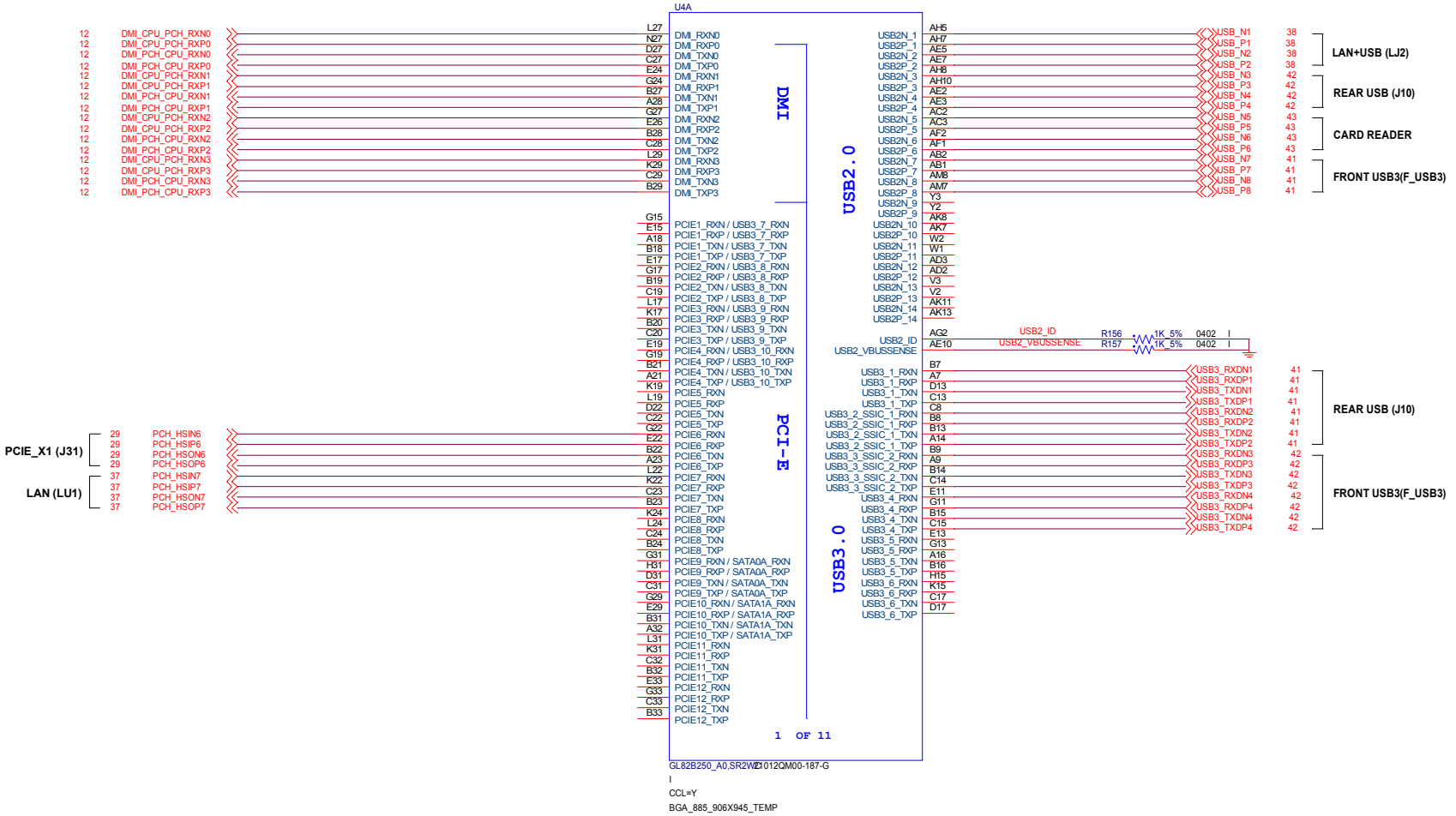
Title: LPT		
Size: B	Document Number: M710e	Rev: SVT
Page Modified: Tuesday, January 30, 2018 15:51:21 (UTC/GMT)		Sheet 18 of 63



Foxconn NPCEBG
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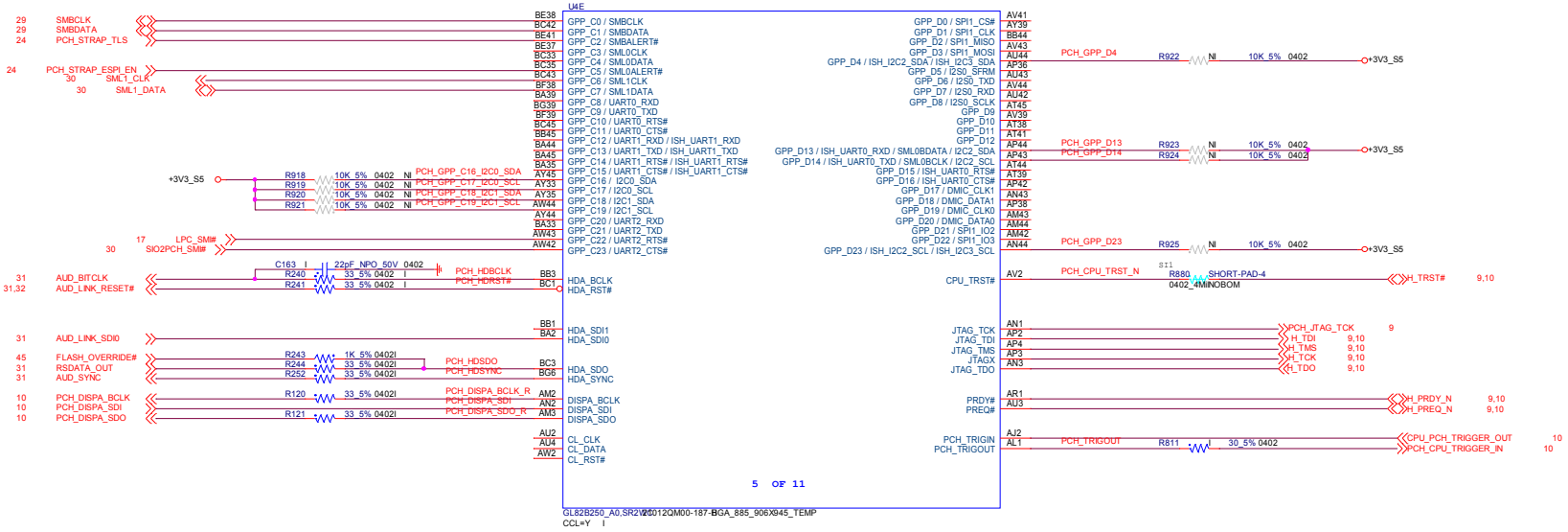
Foxconn WuHan
China
Phone: 027-59603888
Fax:

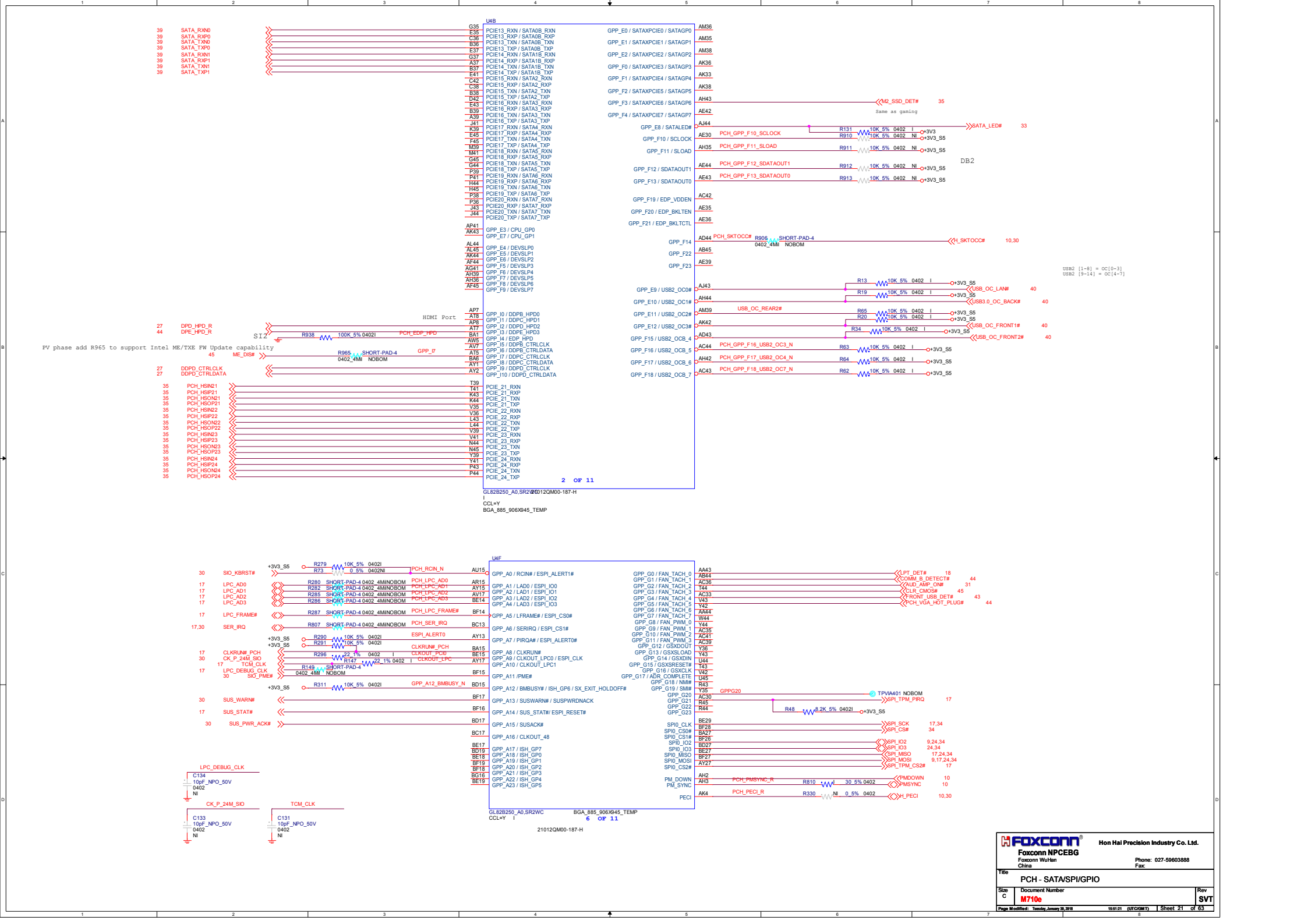
Title: PCH - DMI/PCIE/USB2-3

Size: Custom | Document Number: M710e | Rev: SVT

Page Modified: Tuesday, January 30, 2018 15:51:21 (UTC/GMT) | Sheet 19 of 63



FOXCONN	Hon Hai Precision Industry Co. Ltd.	
Foxconn NPCEBG Foxconn WuHan China	Phone: 027-59603888 Fax:	
Title: PCH - SMBUS/HDA/GPIO/JTAG		
Size: C	Document Number: M710e	Rev: SVT
Page Modified: Tuesday, January 30, 2018 15:51:21 (UTC/GMT)		Sheet 20 of 63


U4B
PCIE13_RXN / SATA0B_RXN
PCIE13_RXP / SATA0B_RXP
PCIE13_TXN / SATA0B_TXN
PCIE13_TXP / SATA0B_TXP
PCIE14_RXN / SATA1B_RXN
PCIE14_RXP / SATA1B_RXP
PCIE14_TXN / SATA1B_TXN
PCIE14_TXP / SATA1B_TXP
PCIE15_RXN / SATA2_RXN
PCIE15_RXP / SATA2_RXP
PCIE15_TXN / SATA2_TXN
PCIE15_TXP / SATA2_TXP
PCIE16_RXN / SATA3_RXN
PCIE16_RXP / SATA3_RXP
PCIE16_TXN / SATA3_TXN
PCIE16_TXP / SATA3_TXP
PCIE17_RXN / SATA4_RXN
PCIE17_RXP / SATA4_RXP
PCIE17_TXN / SATA4_TXN
PCIE17_TXP / SATA4_TXP
PCIE18_RXN / SATA5_RXN
PCIE18_RXP / SATA5_RXP
PCIE18_TXN / SATA5_TXN
PCIE18_TXP / SATA5_TXP
PCIE19_RXN / SATA6_RXN
PCIE19_RXP / SATA6_RXP
PCIE19_TXN / SATA6_TXN
PCIE19_TXP / SATA6_TXP
PCIE20_RXN / SATA7_RXN
PCIE20_RXP / SATA7_RXP
PCIE20_TXN / SATA7_TXN
PCIE20_TXP / SATA7_TXP
GPP_E3 / CPU_GP0
GPP_E7 / CPU_GP1
GPP_E4 / DEVSLP0
GPP_E5 / DEVSLP1
GPP_E6 / DEVSLP2
GPP_F5 / DEVSLP3
GPP_F6 / DEVSLP4
GPP_F7 / DEVSLP5
GPP_F8 / DEVSLP6
GPP_F9 / DEVSLP7
GPP_I0 / DDPB_HPD0
GPP_I1 / DDPC_HPD1
GPP_I2 / DDPD_HPD2
GPP_I3 / DDPE_HPD3
GPP_I4 / EDP_HPD
GPP_I5 / DDPB_CTRLCLK
GPP_I6 / DDPB_CTRLDATA
GPP_I7 / DDPC_CTRLCLK
GPP_I8 / DDPC_CTRLDATA
GPP_I9 / DDPD_CTRLCLK
GPP_I10 / DDPD_CTRLDATA
PCIE_21_RXN
PCIE_21_RXP
PCIE_21_TXN
PCIE_21_TXP
PCIE_22_RXN
PCIE_22_RXP
PCIE_22_TXN
PCIE_22_TXP
PCIE_23_RXN
PCIE_23_RXP
PCIE_23_TXN
PCIE_23_TXP
PCIE_24_RXN
PCIE_24_RXP
PCIE_24_TXN
PCIE_24_TXP
2 OF 11
GL82B250_A0,SR2WC
21012QM00-187-H
CCL=Y
BGA_885_906X945_TEMP
GPP_E0 / SATAXPCIE0 / SATAGP0
GPP_E1 / SATAXPCIE1 / SATAGP1
GPP_E2 / SATAXPCIE2 / SATAGP2
GPP_F0 / SATAXPCIE3 / SATAGP3
GPP_F1 / SATAXPCIE4 / SATAGP4
GPP_F2 / SATAXPCIE5 / SATAGP5
GPP_F3 / SATAXPCIE6 / SATAGP6
GPP_F4 / SATAXPCIE7 / SATAGP7
GPP_E8 / SATALED#
GPP_F10 / SCLOCK
GPP_F11 / SLOAD
GPP_F12 / SDATAOUT1
GPP_F13 / SDATAOUT0
GPP_F19 / EDP_VDDEN
GPP_F20 / EDP_BKLTEN
GPP_F21 / EDP_BKLTCTL
GPP_F14
GPP_F22
GPP_F23
GPP_E9 / USB2_OC0#
GPP_E10 / USB2_OC1#
GPP_E11 / USB2_OC2#
GPP_E12 / USB2_OC3#
GPP_F15 / USB2_OCB_4
GPP_F16 / USB2_OCB_5
GPP_F17 / USB2_OCB_6
GPP_F18 / USB2_OCB_7
M2_SSD_DET#
Same as gaming
SATA_LED#
PCH_GPP_F10_SCLOCK
PCH_GPP_F11_SLOAD
PCH_GPP_F12_SDATAOUT1
PCH_GPP_F13_SDATAOUT0
PCH_SKTOCC#
H_SKTOCC#
USB_OC_REAR2#
PCH_GPP_F16_USB2_OC3_N
PCH_GPP_F17_USB2_OC4_N
PCH_GPP_F18_USB2_OC7_N
USB_OC_LAN#
USB3.0_OC_BACK#
USB_OC_FRONT1#
USB_OC_FRONT2#
DB2
USB2 [1-8] = OC[0-3]
USB2 [9-14] = OC[4-7]
HDMI Port
DPD_HPD_R
DPE_HPD_R
PCH_EDP_HPD
ME_DIS#
GPP_I7
DDPD_CTRLCLK
DDPD_CTRLDATA
PCH_HSIN21
PCH_HSIP21
PCH_HSON21
PCH_HSOP21
PCH_HSIN22
PCH_HSIP22
PCH_HSON22
PCH_HSOP22
PCH_HSIN23
PCH_HSIP23
PCH_HSON23
PCH_HSOP23
PCH_HSIN24
PCH_HSIP24
PCH_HSON24
PCH_HSOP24
PV phase add R965 to support Intel ME/TXE FW Update capability
U4F
GPP_A0 / RCIN# / ESPI_ALERT1#
GPP_A1 / LAD0 / ESPI_IO0
GPP_A2 / LAD1 / ESPI_IO1
GPP_A3 / LAD2 / ESPI_IO2
GPP_A4 / LAD3 / ESPI_IO3
GPP_A5 / LFRAME# / ESPI_CS0#
GPP_A6 / SERIRQ / ESPI_CS1#
GPP_A7 / PIRQA# / ESPI_ALERT0#
GPP_A8 / CLKRUN#
GPP_A9 / CLKOUT_LPC0 / ESPI_CLK
GPP_A10 / CLKOUT_LPC1
GPP_A11 /PME#
GPP_A12 / BMBUSY# / ISH_GP6 / SX_EXIT_HOLDOFF#
GPP_A13 / SUSWARN# / SUSPWRDNACK
GPP_A14 / SUS_STAT#/ ESPI_RESET#
GPP_A15 / SUSACK#
GPP_A16 / CLKOUT_48
GPP_A17 / ISH_GP7
GPP_A18 / ISH_GP0
GPP_A19 / ISH_GP1
GPP_A20 / ISH_GP2
GPP_A21 / ISH_GP3
GPP_A22 / ISH_GP4
GPP_A23 / ISH_GP5
6 OF 11
GL82B250_A0,SR2WC
BGA_885_906X945_TEMP
CCL=Y
21012QM00-187-H
GPP_G0 / FAN_TACH_0
GPP_G1 / FAN_TACH_1
GPP_G2 / FAN_TACH_2
GPP_G3 / FAN_TACH_3
GPP_G4 / FAN_TACH_4
GPP_G5 / FAN_TACH_5
GPP_G6 / FAN_TACH_6
GPP_G7 / FAN_TACH_7
GPP_G8 / FAN_PWM_0
GPP_G9 / FAN_PWM_1
GPP_G10 / FAN_PWM_2
GPP_G11 / FAN_PWM_3
GPP_G12 / GSXDOUT
GPP_G13 / GSXSLOAD
GPP_G14 / GSXDIN
GPP_G15 / GSXSRESET#
GPP_G16 / GSXCLK
GPP_G17 / ADR_COMPLETE
GPP_G18 / NMI#
GPP_G19 / SMI#
GPP_G20
GPP_G21
GPP_G22
GPP_G23
SPI0_CLK
SPI0_CS0#
SPI0_CS1#
SPI0_IO2
SPI0_IO3
SPI0_MISO
SPI0_MOSI
SPI0_CS2#
PM_DOWN
PM_SYNC
PECI
LPT_DET#
COMM_B_DETECT#
AUD_AMP_ON#
CLR_CMOS#
FRONT_USB_DET#
PCH_VGA_HOT_PLUG#
SPI_TPM_PIRQ
SPI_SCK
SPI_CS#
SPI_IO2
SPI_IO3
SPI_MISO
SPI_MOSI
SPI_TPM_CS2#
PMDOWN
PMSYNC
H_PECI
SIO_KBRST#
LPC_AD0
LPC_AD1
LPC_AD2
LPC_AD3
LPC_FRAME#
SER_IRQ
CLKRUN#_PCH
CK_P_24M_SIO
TCM_CLK
LPC_DEBUG_CLK
SIO_PME#
SUS_WARN#
SUS_STAT#
SUS_PWR_ACK#
PCH_RCIN_N
PCH_LPC_AD0
PCH_LPC_AD1
PCH_LPC_AD2
PCH_LPC_AD3
PCH_LPC_FRAME#
PCH_SER_IRQ
ESPI_ALERT0
CLKRUN#_PCH
CLKOUT_PCI0
CLKOUT_LPC
GPP_A12_BMBUSY_N
LPC_DEBUG_CLK
CK_P_24M_SIO
TCM_CLK
PCH_PMSYNC_R
PCH_PECI_R
GPPG20
TPVIA401 NOBOM
Foxconn NPCEBG
Foxconn WuHan
China
Hon Hai Precision Industry Co. Ltd.
Phone: 027-59603888
Fax:
Title
PCH - SATA/SPI/GPIO
Size
C
Document Number
M710e
Rev
SVT
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15:31:21 (UTC/GMT)
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From EDS
1. SRCCLKREQ#[7:0] can be mapped to any of the CLKOUT_PCIE_P/N[7:0]
2. SRCCLKREQ#[15:8] can be mapped to any of the CLKOUT_PCIE_P/N[15:8] pairs

U4D

GPP_B0 / GPP_B1 / GPP_B2 / VRALERT# / GPP_B3 / CPU_GP2 / GPP_B4 / CPU_GP3 / GPP_B5 / SRCCLKREQ0# / GPP_B6 / SRCCLKREQ1# / GPP_B7 / SRCCLKREQ2# / GPP_B8 / SRCCLKREQ3# / GPP_B9 / SRCCLKREQ4# / GPP_B10 / SRCCLKREQ5# / GPP_B11 / GPP_B12 / SLP_S0# / GPP_B13 / PLTRST# / GPP_B14 / SPKR / GPP_B15 / GSPI0_CS# / GPP_B16 / GSPI0_CLK / GPP_B17 / GSPI0_MISO / GPP_B18 / GSPI0_MOSI / GPP_B19 / GSPI1_CS# / GPP_B20 / GSPI1_CLK / GPP_B21 / GSPI1_MISO / GPP_B22 / GSPI1_MOSI / GPP_B23 / SML1ALERT# / PCHHOT#

GPP_H0 / GPP_H1 / GPP_H2 / GPP_H3 / GPP_H4 / GPP_H5 / GPP_H6 / GPP_H7 / GPP_H8 / GPP_H9 / GPP_H10 / GPP_H11 / GPP_H12 / GPP_H13 / GPP_H14 / GPP_H15 / GPP_H16 / GPP_H17 / GPP_H18 / GPP_H19 / GPP_H20 / GPP_H21 / GPP_H22 / GPP_H23

4 OF 11

GL82B250_A0,SR2WC 21012QM00-187-H
CCL=Y
I
BGA_885_906X945_TEMP

PROCPWRGD, PLTRST_PROC#, RSMRST#, DRAM_RESET#, DSW_PWROK, PCH_PWROK, SLP_LAN#, SLP_SUS#, SRTCRST#, SYS_PWROK, SYS_RESET#, WAKE#, INTRUDER#, THRMTRIP#, GPD0 / BATLOW#, GPD1 / ACPRESENT, GPD2 / LAN_WAKE#, GPD3 / PWRBTN#, GPD4 / SLP_S3#, GPD5 / SLP_S4#, GPD6 / SLP_A#, GPD7 / RSVD, GPD8 / SUSCLK, GPD9 / SLP_WLAN#, GPD10 / SLP_S5#, GPD11 / LANPHYPC

AL2	H_PWRGOOD_R	R959 10_5% 0402 I	H_PWRGOOD	10
AK3	PLTRST_IN_CPU_R	R960 10_5% 0402 I	PLTRST_IN_CPU#	10
BG5	PCH_RSMRST#	C218 22nF_X7R_16V 0402 NI; R336 33_5% 0402 I; R200 10K_5% 0402 NI	SIO_RSMRST#	9,17,30
BD10			M_AB_RESET_N	11
BD4		R203 100K_5% 0402 NI	PCH_DPWROK	30
BE4	PCH_PWROK	X3 R901 10_5% 0402 I; R902 0_5% 0402 NI; VCORE_PG_BF; PWRGD_140MS		
AV11	SLP_LAN_N	TP4 NOBOM; R201 33_5% 0402 I	SLP_SUS#	30,54
BF10	SLP_SUS#_R			
BF8	SRTCRST#_PCH	R159 20K_1% 0402 I; C154 1uF_X5R_6.3V 0402; +3V_BATT	SRTCRST#_PCH	23
AW3	SYS_PWROK	X3 R618 10_5% 0402 NI; R903 0_5% 0402 I; R340 10K_5% 0402 NI	VCORE_PG_BF; PWRGD_140MS	13,48; 9,29,30,45
AV3		R342 10K_5% 0402 I	FP_RST#	9,33
BE9		R964 10K_5% 0402 I	PCI_EXP_WAKE#	28,29,35,37
BF9	INTRDUER_N_PCH	R993 SHORT-PAD-4 0402_4MI NOBOM	INTRUDER#	45
AH4		R345 390_1% 0402 NI +1V0_S5	H_THERMTRIP#	10
BF11	BATLOW#_PCH	C155 680pF_X7R_50V; R349 10K_5% 0402 I		
BD13	ACPRESENT	R350 10K_5% 0402 I		
BE10	LAN_WAKE_N	R364 10K_5% 0402 I		
BC5		R365 8.2K_5% 0402 I	PWRBTN_OUT#	9,30
BA11	PCH_SLP_S3#	R228 22_5% 0402 I	SLP_S3#	30,38,45,53,57
BF13	PCH_SLP_S4#	R229 33_5% 0402 I	SLP_S4#	13,30,33,40,45,56,59
BE13	SLP_A#	TP319 NOBOM		
BG11	WAKEOUT_N	TP316 NOBOM		
AV13	SUSCLK_PCH	R366 30_5% 0402 I	SUSCLK_M2280	35
BA9	SLP_WAN_N	TP317 NOBOM		
BB7	PCH_SLP_S5#	R302 SHORT-PAD-4 0402_4MI NOBOM	SLP_S5#	45
BC11	GPD11	TP2 NOBOM		

+3V3_S5 +3V3_S5
R787 10K_5% 0402 NI
R332 10K_5% 0402 I
GPP_B2_PCH

28 PCIEX16_CLKREQ#
17 SLP_S0#
30 PLTRST_N
31,45 SPKR
38 PCH_USB_UART_EN
SLP_S0#
R114 33_5% 0402 I GPP_B14_SPKR

24 PCH_STRAP_GPP_B18

+3V3_S5 R333 10K_5% 0402 I GPP_B21_GSPI1_MISO
24 PCH_STRAP_BBS
24 PCH_STRAP_EXI_N

NOBOM TP318 GPP_H0
35 M2_2280_CLKREQ#
37 LAN_CLKREQ#
29 PCIEX1_CLKREQ#

24 PCH_STRAP_GPP_H12

BRD_ID0
BRD_ID1
BRD_ID2
BRD_ID3
BRD_ID4
BRD_ID5

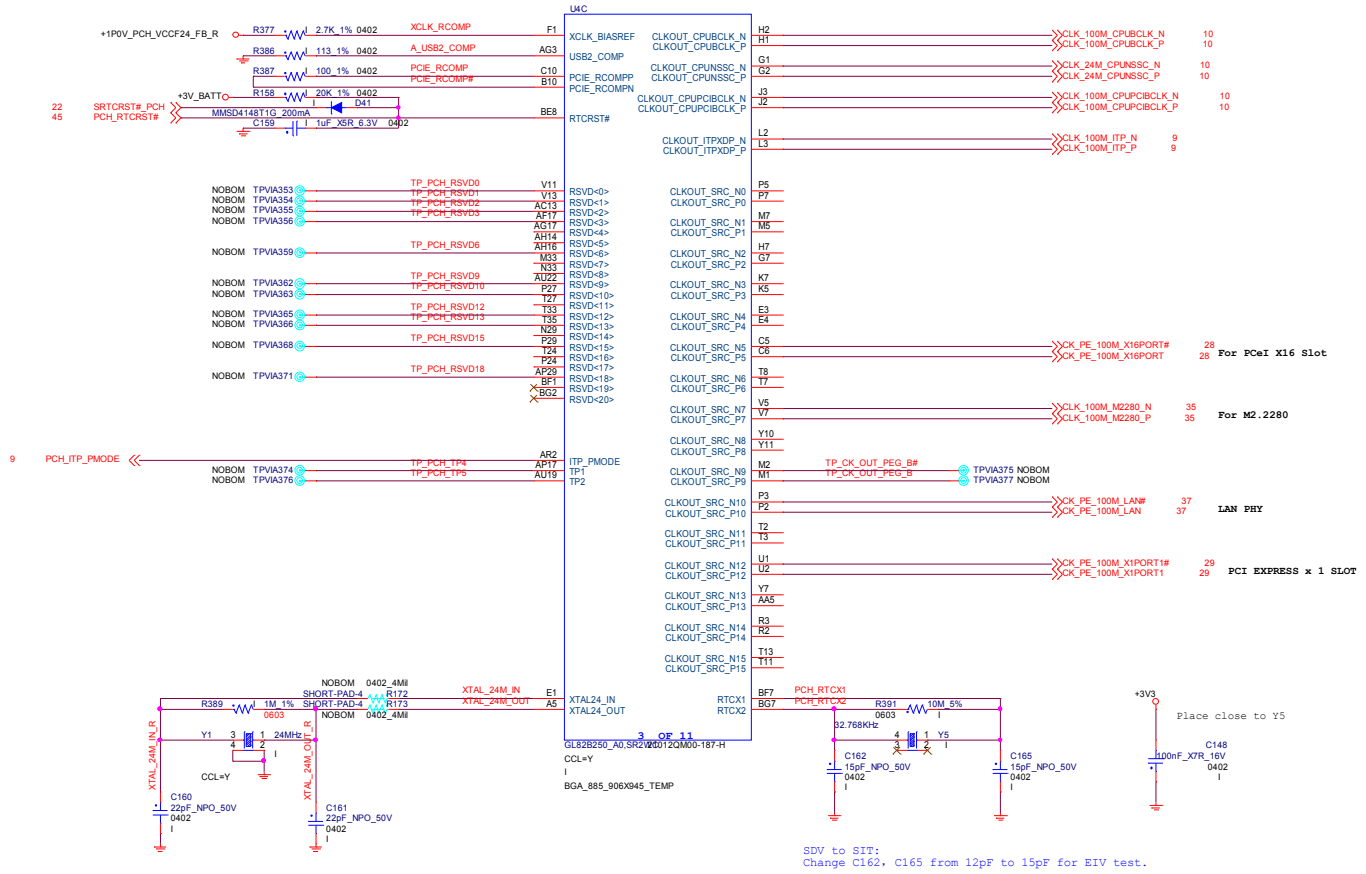
+3V3_S5
R160 10K_5% NI 0402
R162 10K_5% NI 0402
R168 10K_5% NI 0402
R174 10K_5% NI 0402
R193 10K_5% NI 0402
R191 10K_5% NI 0402
BRD_ID0
BRD_ID1
BRD_ID2
BRD_ID3
BRD_ID4
BRD_ID5
R194 10K_5% I 0402
R195 10K_5% I 0402
R196 10K_5% I 0402
R197 10K_5% I 0402
R198 10K_5% I 0402
R192 10K_5% I 0402

BATTERY

DO NOT exceed 3.2V
+3V_BATT
C228 1uF_X5R_16V 0603 I
D1 BAT54C_200mA SOT23-3P I
BATT_LPS
BATT_R_2
R376 1K_5% 0603 I
BATT1
XBT1 Battery Holder_H I CCL=Y
C766 100nF_X7R_16V 0402 I
+3V3_DSW
R363 1.5K_1% 0402 I
R380 45.3K_1% 0402 I
@XBT1 Battery_3V_225mAh I

Hon Hai Precision Industry Co. Ltd.		
Foxconn NPCEBG		
Foxconn WuHan China	Phone: 027-59603888 Fax:	
Title: PCH - GPIO/MISC		
Size: Custom	Document Number: M710e	Rev: SVT
Page Modified: Tuesday, January 30, 2018 18:51:21 (UTC/GMT)		Sheet 22 of 63

PCH - CLOCK DISTRIBUTION



FOXCONN	Hon Hai Precision Industry Co. Ltd.	
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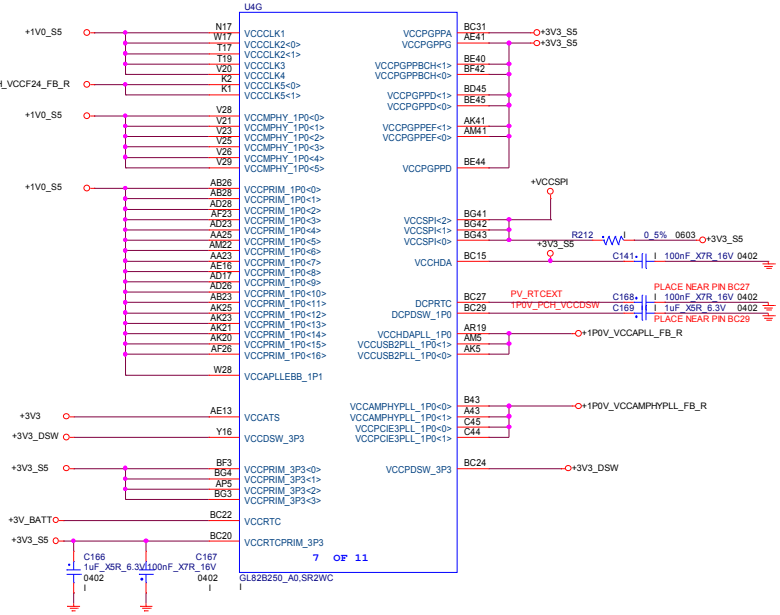
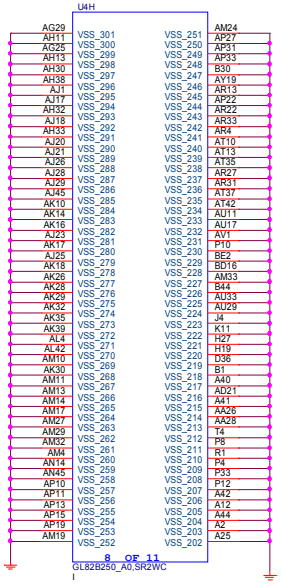
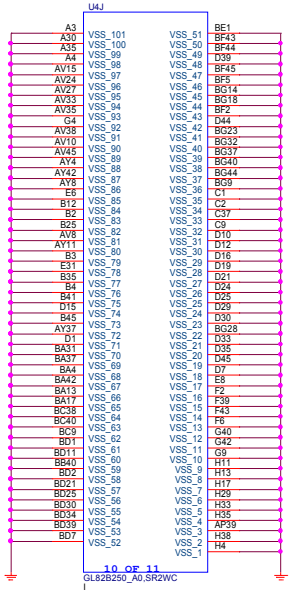
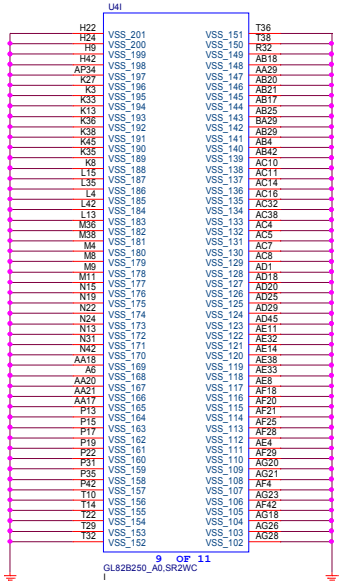
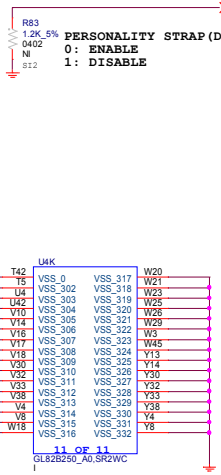
Foxconn WuHan China	Fax:	
Title: PCH - CLOCK		
Size: C	Document Number: M710e	Rev: SVT
Page Modified: Tuesday, January 30, 2018 15:51:21 (UTC/GMT)	Sheet 23 of 63	







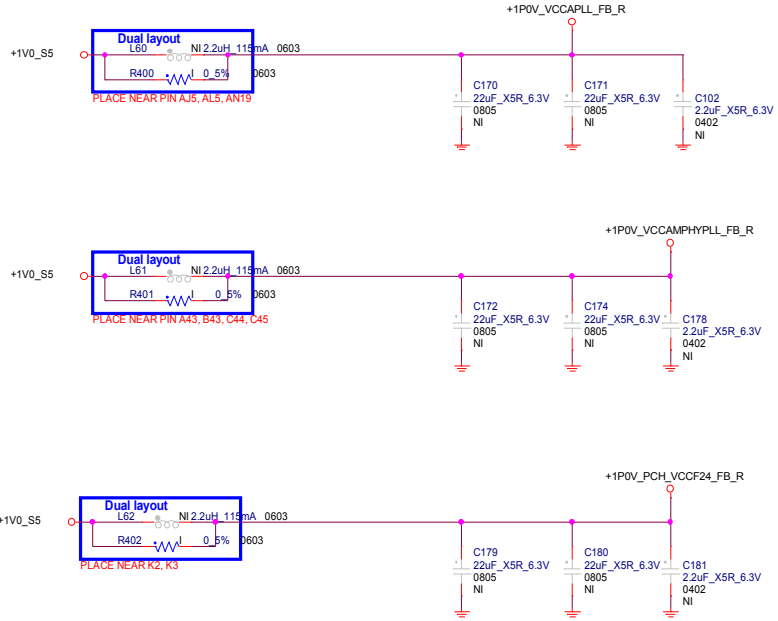




FOXCONN®	Hon Hai Precision Industry Co. Ltd.	
Foxconn NPCEBG		
Foxconn WuHan China	Phone: 027-59603888 Fax:	
Title: PCH - PWR/STRAP		
Size: C	Document Number: M710e	Rev: SVT
Page Modified: Tuesday, January 30, 2018 15:51:21 (UTC/GMT)		Sheet 24 of 63

FILTER

SKYLAKE Decoupling & filter

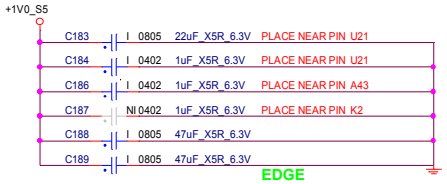


Power Plane Isolation

Need to update for KBL

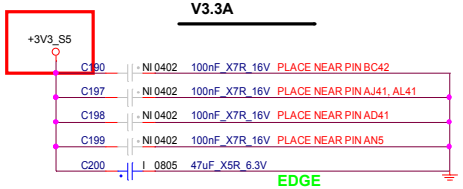
Voltage	Interface	PCH Pins sharing power rail
VCC_PCH 1.05V	Core	U26, U25, U23, U21, V26,
	PCIe/SATA/ USB3	T19, T20, P22, P23, P25, P26, P28, P14, P16, P17
	GPIO/LPC	AC12
	FDI	M14
	DIFFCLK	U12, V14
		W14
		AB2
	SSC	T16, V16
		AA16, W16
	USB2	AF19, AF20, AF22, AF23, AP22
PCH 3.3V Standby	SUS	AM33, AN33
	USB2	AH18, AH20, AH22, AJ20, AK20
	AZALIA	AW26
	USB3	P20
	RTC	AP35
PCH 3.3V	CLK	AM7, AM9, AP5, AP7, AR4, AT5, AV4, AW4, AW9, AG12, AK11,
	HVCMOS	AG1
	PCIe	AV3, AW3
	Core	U30, W30
	Fuse	AF26

V1.0A

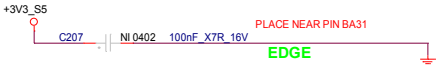


V3.3 DSW

V3.3A

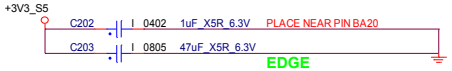


VccPGPPA

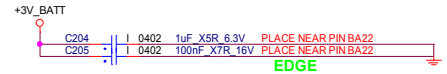


V1.8A / V1.8S / V3.3S

V3.3A



VCCRTC



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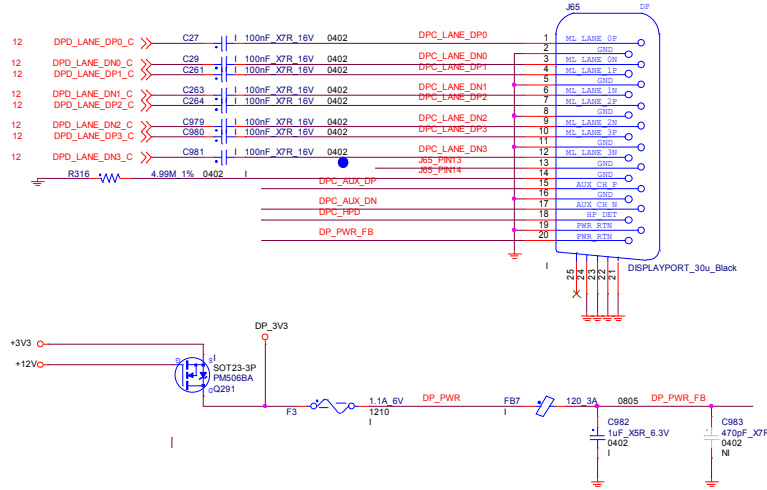
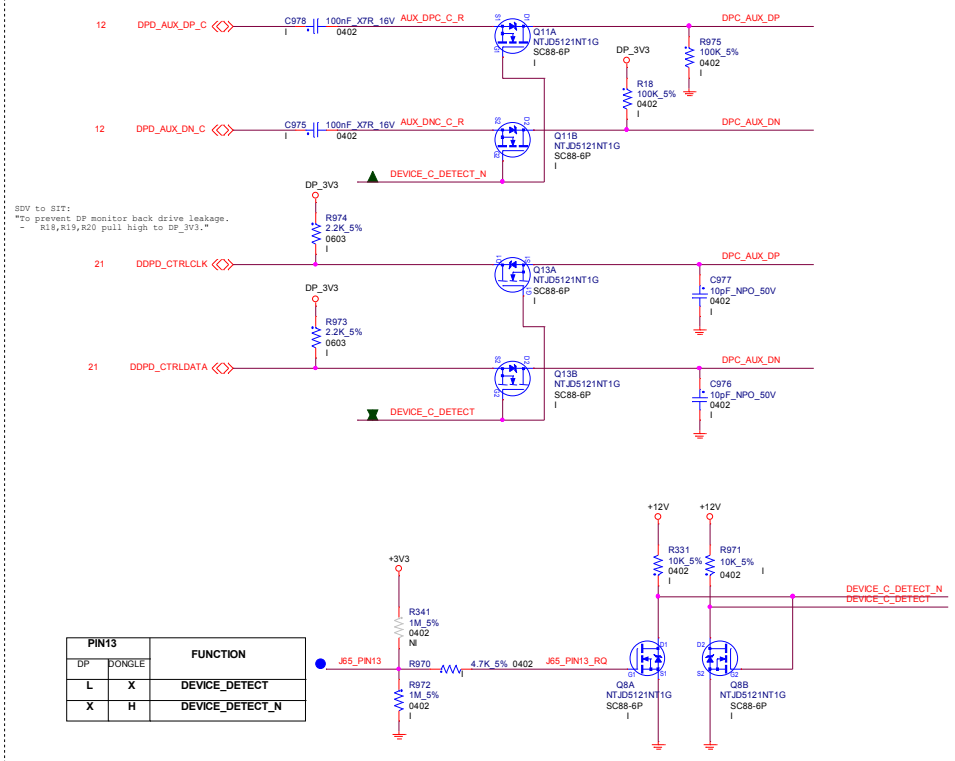
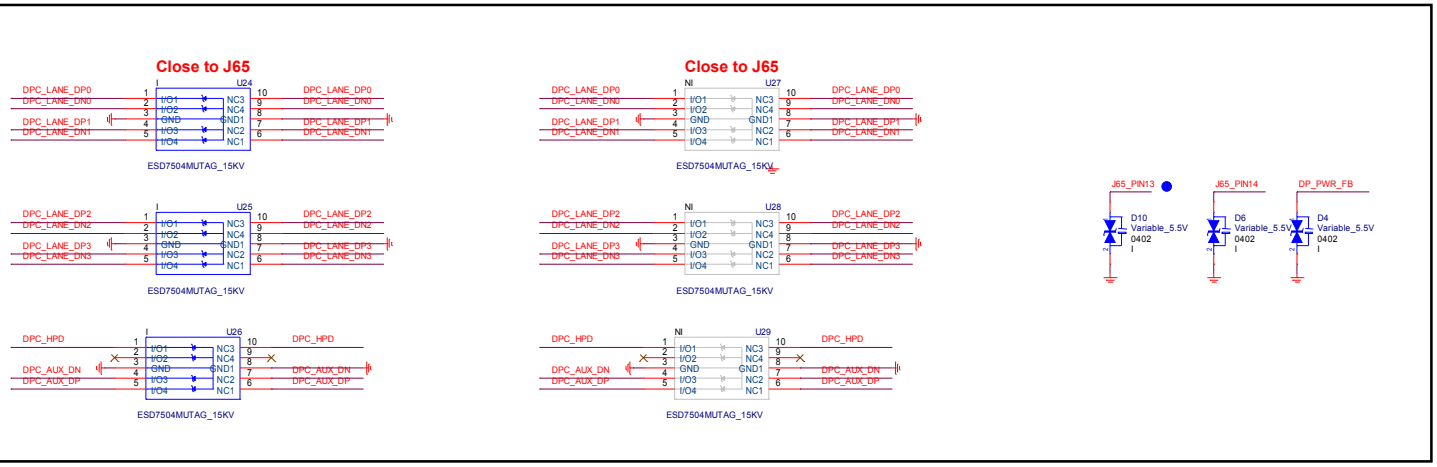
DP-PortD





PIN13		FUNCTION
DP	DONGLE	
L	X	DEVICE_DETECT
X	H	DEVICE_DETECT_N

ESD suppressor



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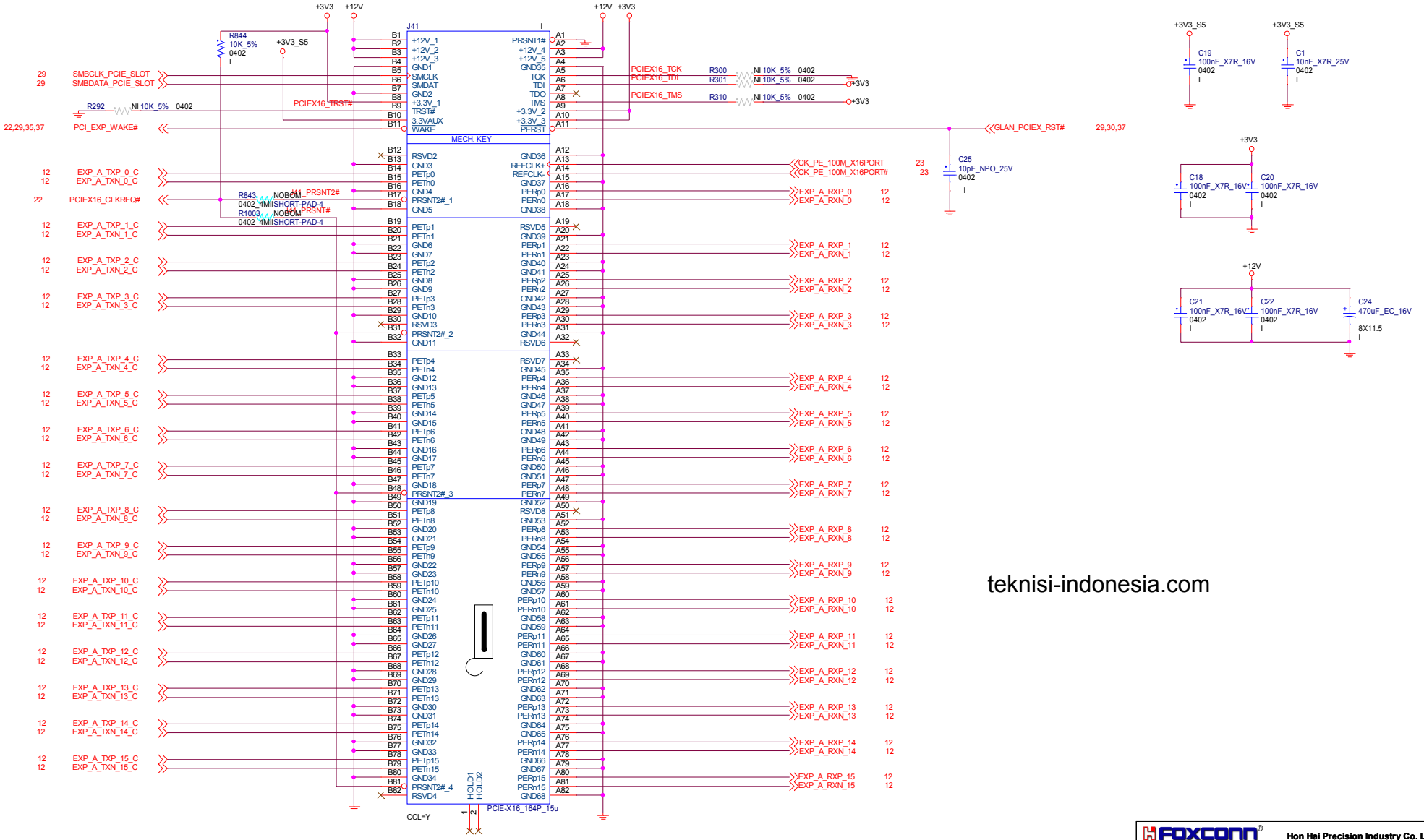
PCI EXPRESS x16 SLOT



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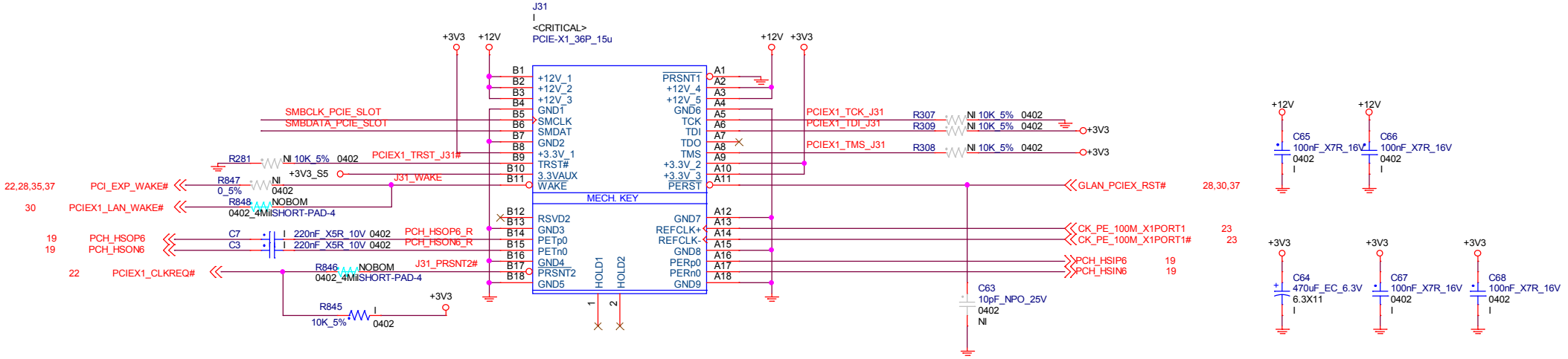
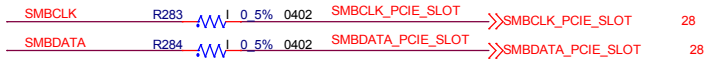
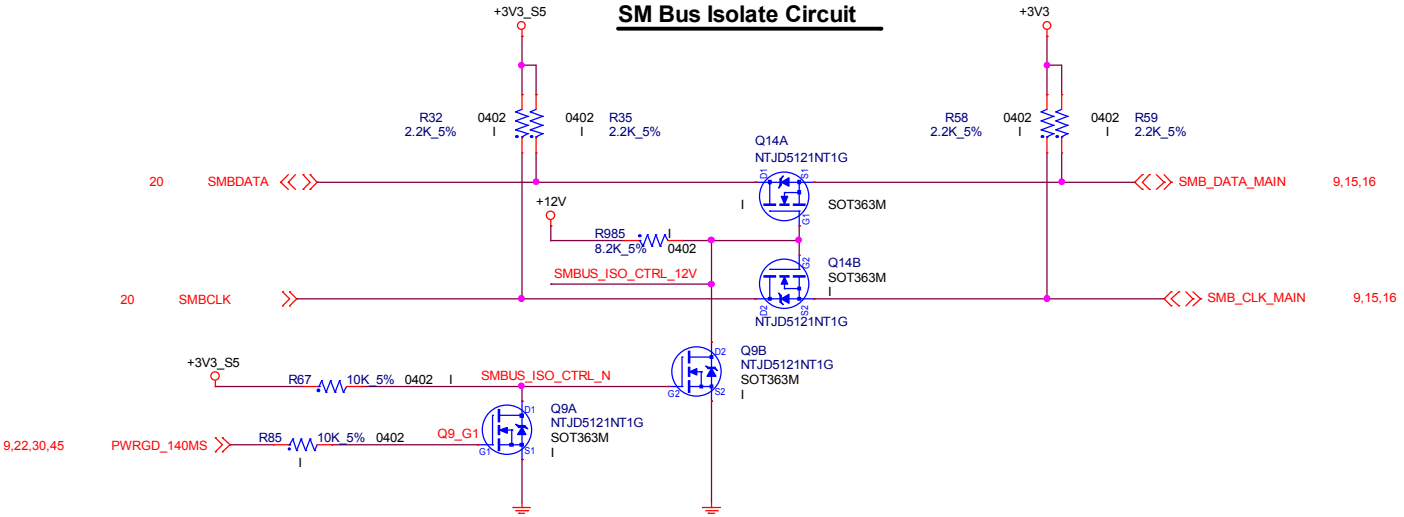
PCI EXPRESS X1 SLOT1(Support Gen3)



For Monotonic improve use



SM Bus Isolate Circuit



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IT8629E Power On Strapping Options

Power-On Strapping

	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	**EUP**
Pin-45		0	DSW
JP2	WDT_EN	1	**Disable WDT to reset PWROK**
Pin-119		0	Enable WDT to reset PWROK
JP3	FAN_CTL_SEL	1	**EC Index 63h/73h/7Bh/A3 is 80h**
Pin-121		0	EC Index 63h/73h/7Bh/A3 is 00h
JP4	K8PWR_EN	1	**Disable K8 Power Sequence**
Pin-123		0	Enable K8 Power Sequence
JP5	UOVMODE_SEL	1	Notice Mode (Default)
Pin-26	OV/UV	0	Force Mode
JP6	VIH/VIL_SEL	1	BAY-TRAIL PLATFORM
Pin-46		0	NOT BAY-TRAIL PLATFORM

FAN_CTRL2 not supported by JP3 FAN_CTL_SEL(EC index 6Bh default value always 80h)

ITE +3V3 Bleed off

RI2# used for LAN G3 to S5 WOL

Voltage detect

Thermal Sensor

SQ1 closer to CPU VRM

SC193/SC194/SC88 Close SIO pin 96

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Title	SIO IT8629E
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change from +5V_S5 to +5V 2017/9/28

change from +3V3_S5 to +3V3 2017/9/28

change from +3V3_S5 to +3V3 2017/9/28

AC11 /AC12 close AU1 pin 1

AC14 /AC15 close AU1 pin 9

change from +3V3_S5 to +3V3 2017/9/28

change from +3V3_S5 to +3V3 2017/9/28

Add AR97 pull high to +3V3_DSW.and dummy AR10. 2017/9/29

change from +3V3_S5 to +3V3 2017/9/28

Use Speaker 8 Ohm /1W=> 20 mils for this project

Vout =0.8 * (1+PR101/PR102)
=1.509V

AMP ENABLE CIRCUIT

change from +3V3_S5 to +3V3 2017/9/28

Place near AJ1

Place near AJ2

Place near AJ3

Place near AU1

Place near AU1.

Place near AJ1

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Size	C
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change 2017/9/28

ESD component shall close AJ1

ESD component shall close AJ3

ESD component shall close AJ2

Front MIC IN

REAR LINE OUT

HeadPhone_OUT

Audio Jack

Combo Jack connector

PCB trace width of SLEEVE & RING2 are required at least 40 mil and its length should be as short as possible.

AFB8/AFB11 should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk

Darlington circuit

Control by software driver and Codec GPIO.
GPIO#0 driver low at:
1).Initial state
2).Suspend to S1~S3
3).Resume from S~S3.

ANALOG

DIGITAL

To solve the background noise while combojack connecting to an active speaker and system entry into S3/S4/S5 without analog power.

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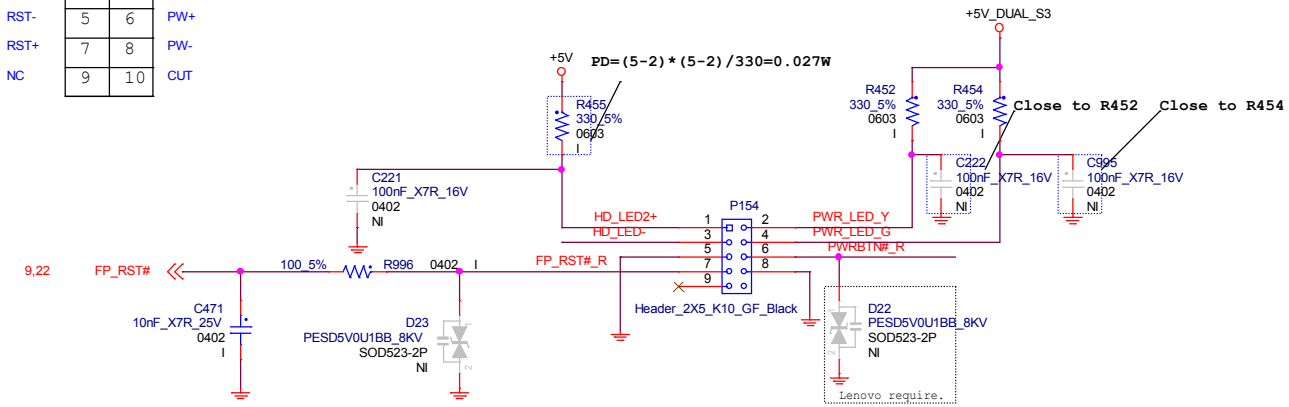
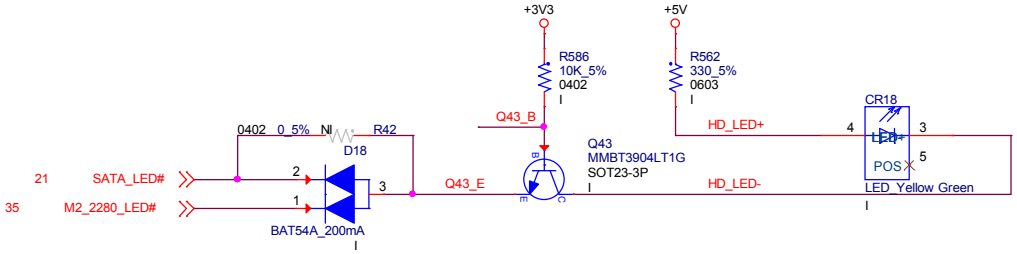
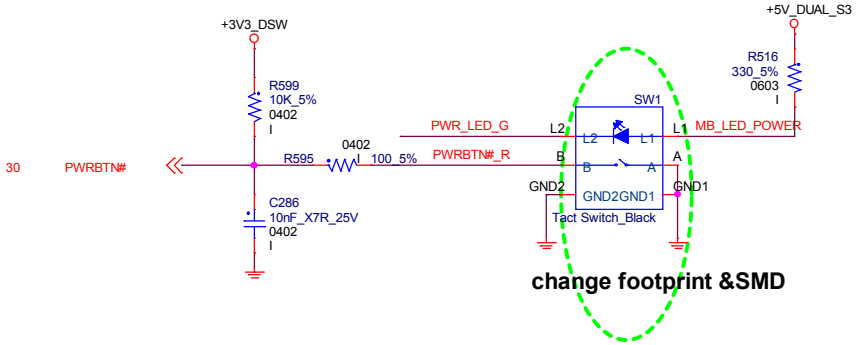
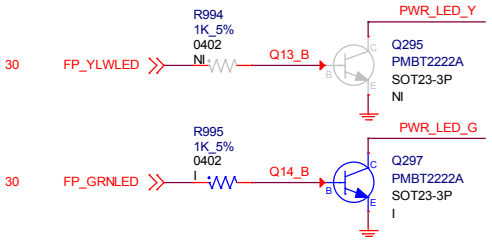
FRONT PANEL

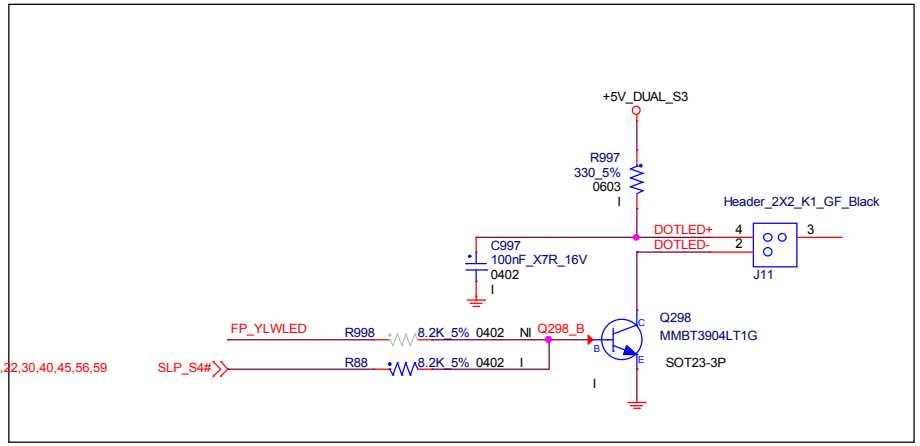
HD+	1	2	PWRLED(Yellow)
HD-	3	4	PWRLED(Green)
RST-	5	6	PW+
RST+	7	8	PW-
NC	9	10	CUT











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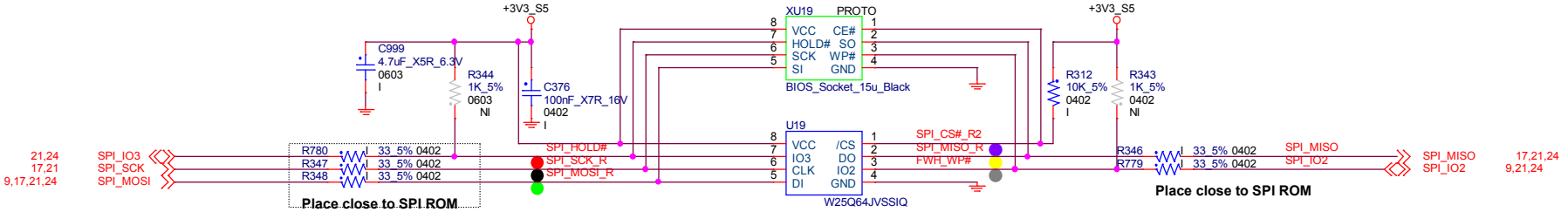
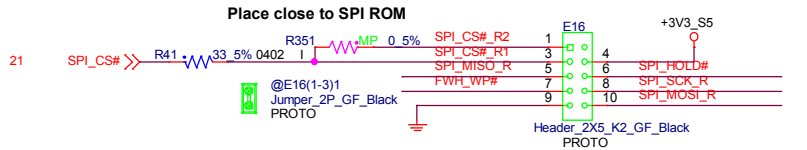
SPI ROM



LENOVO SPI ROM DEBUG HEADER



2x5_K2 Pitch = 1.27mm

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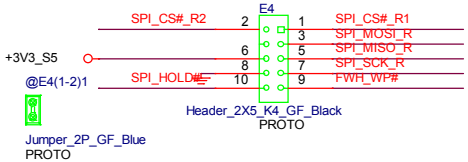
FOXCONN SPI ROM DEBUG HEADER

The header traces should be daisy-chain through the header with no stubs.



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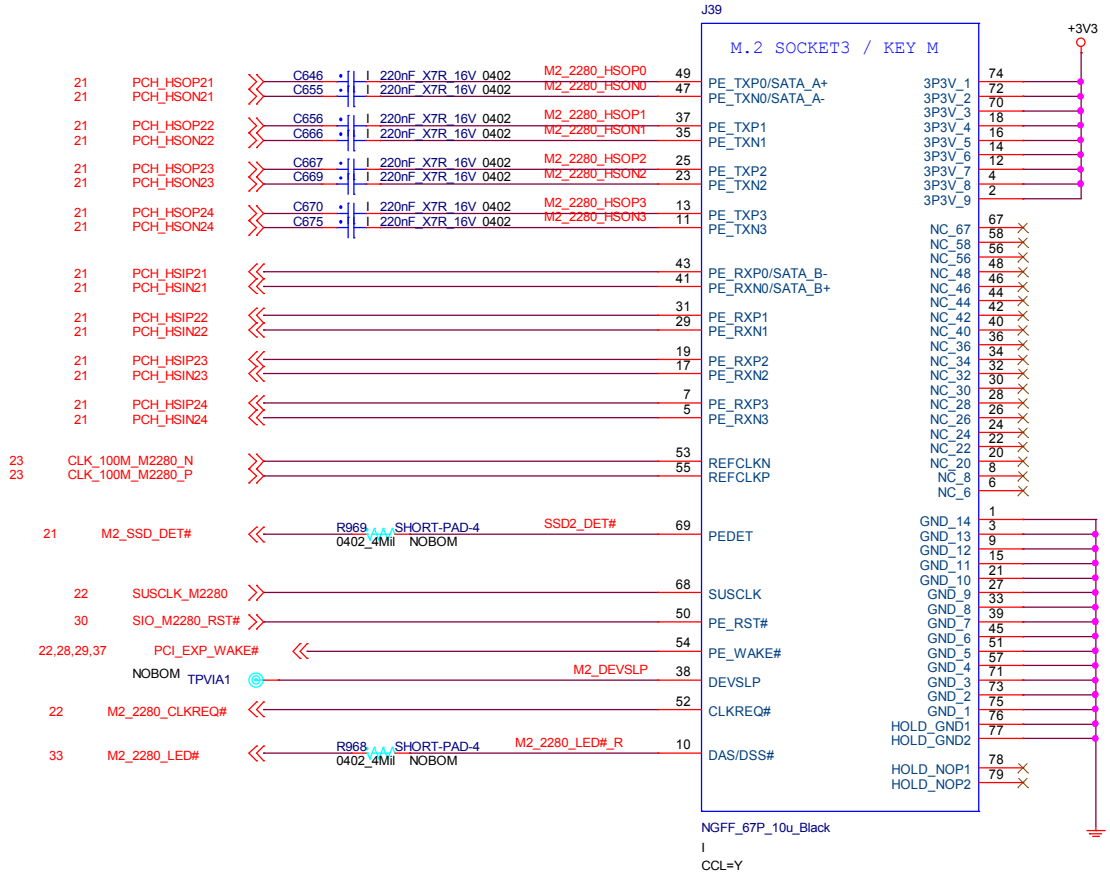
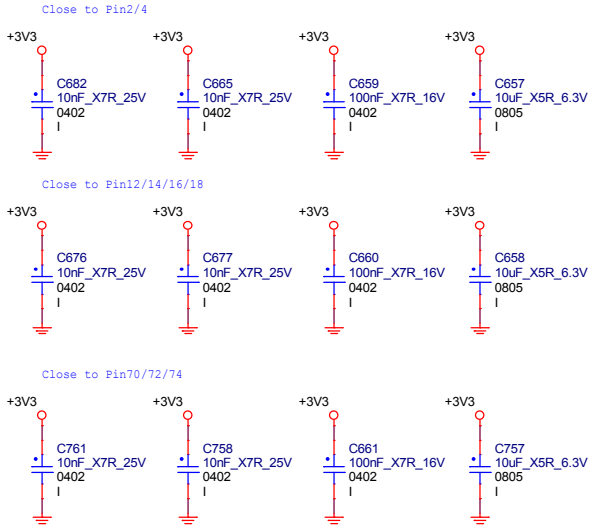
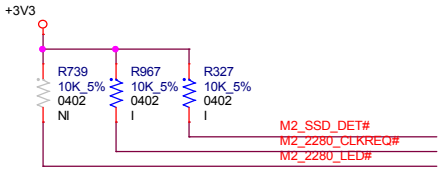
M.2 2280-3M



Decoupling CAP (J39)



M.2 SSD PU/PD Config



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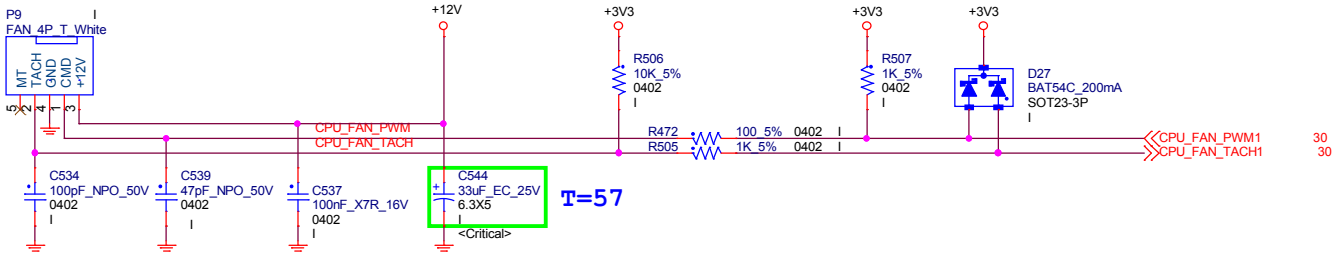
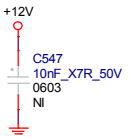
CPU FAN

Color: White



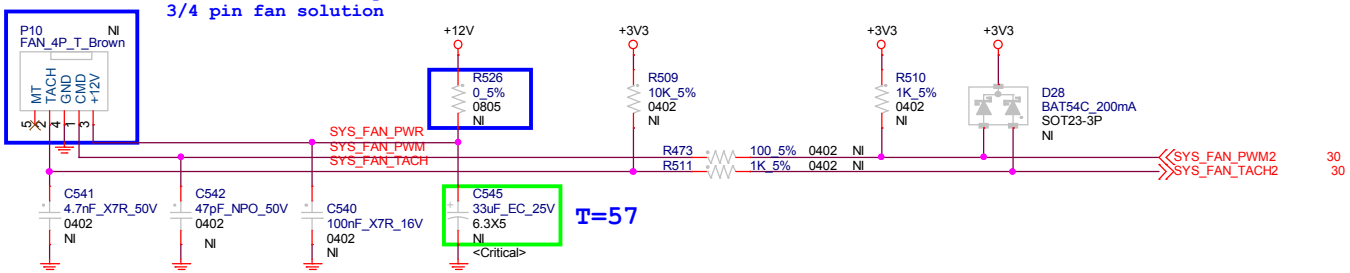
For EMI

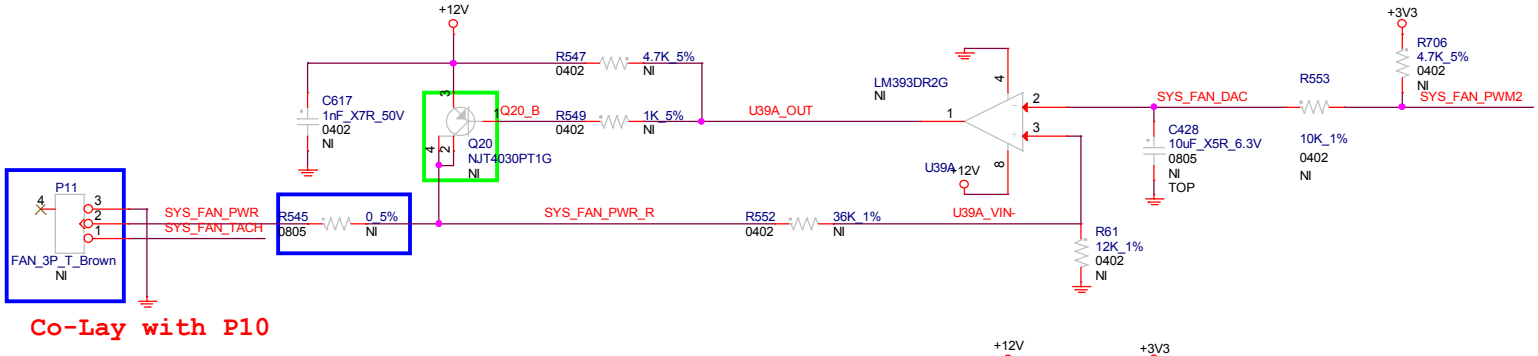


No need SYSTEM FAN

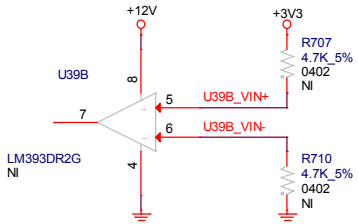
Color: Brown

R526/R473/R545 is optional for 3/4 pin fan solution





Co-Lay with P10



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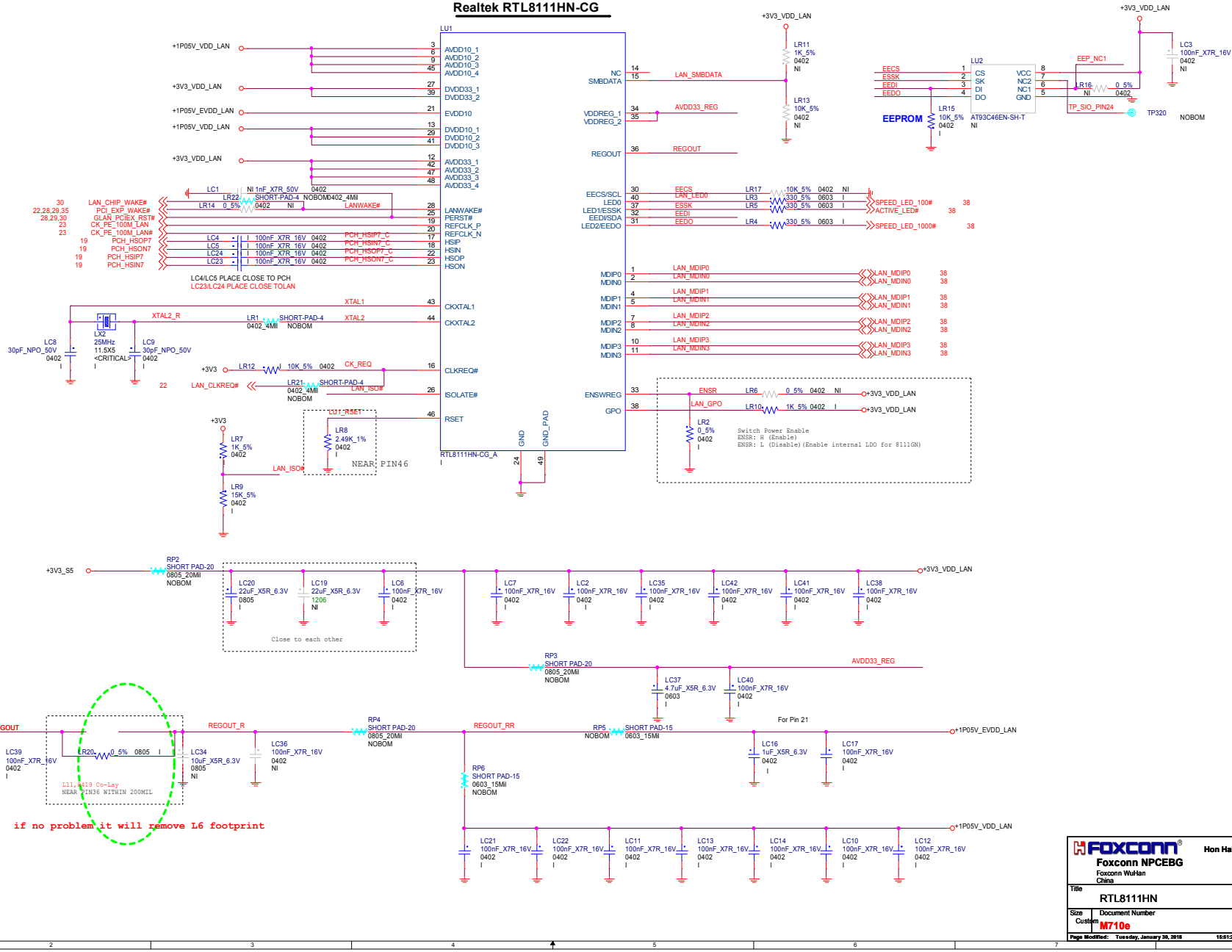
Realtek RTL8111HN-CG



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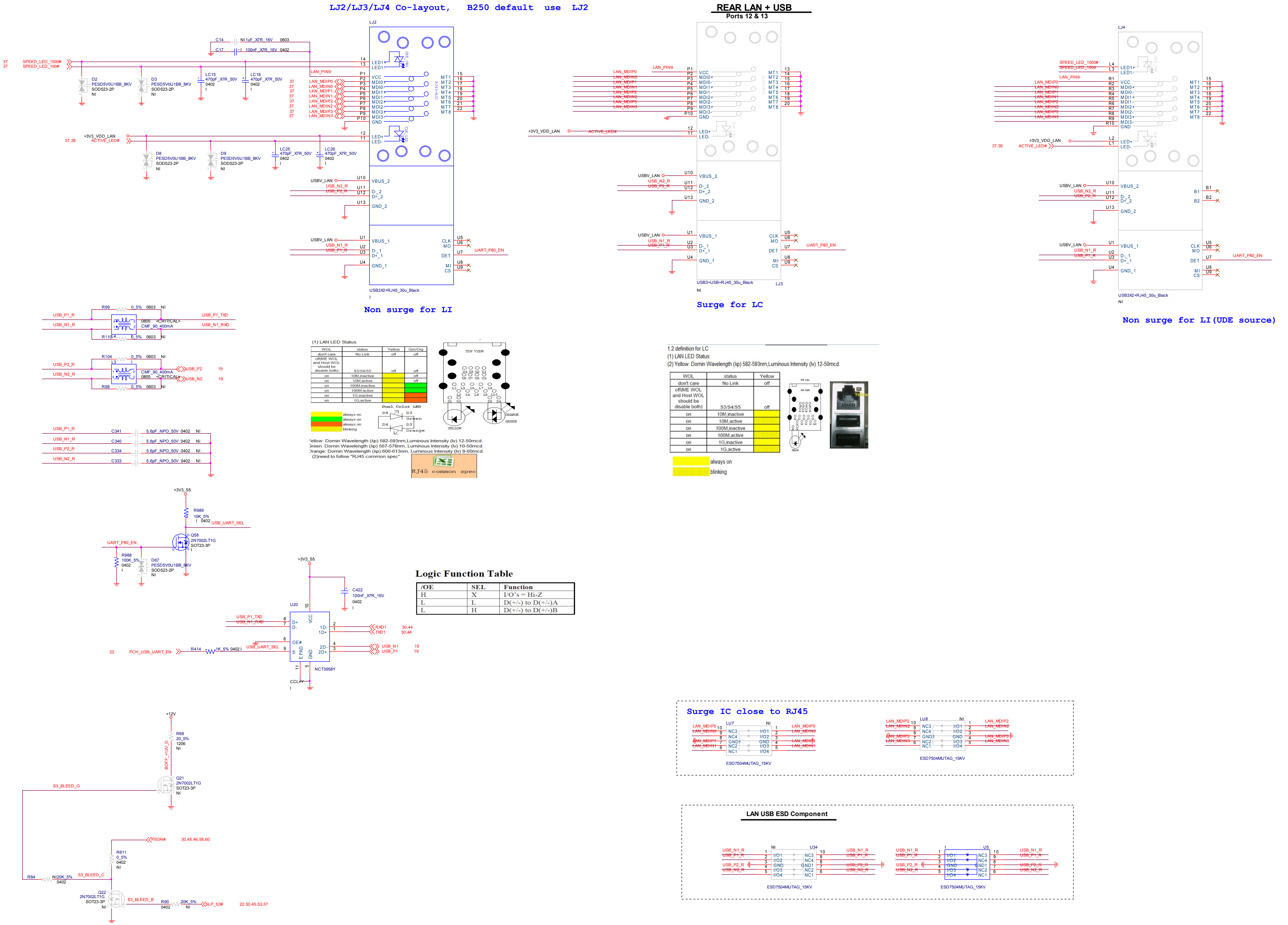

(1) LAN LED Status

WOL	status	Yellow	Grn/Org
don't care	No Link	off	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off	off
on	10M,inactive		off
on	10M,active		off
on	100M,inactive		
on	100M,active		
on	1G,inactive		
on	1G,active		

always on
always on
always on
blinking

Yellow: Domin Wavelength (λp) 582-593nm,Luminous Intensity (Iv) 12-50mcd.
Green: Domin Wavelength (λp) 567-578nm, Luminous Intensity (Iv) 10-50mcd.
Orange: Domin Wavelength (λp) 600-613nm, Luminous Intensity (Iv) 9-60mcd.
(2)need to follow "RJ45 common spec"

1.2 definition for LC
(1) LAN LED Status
(2) Yellow: Domin Wavelength (λp) 582-593nm,Luminous Intensity (Iv) 12-50mcd.

WOL	status	Yellow
don't care	No Link	off
off(ME WOL and Host WOL should be disable both)	S3/S4/S5	off
on	10M,inactive	
on	10M,active	
on	100M,inactive	
on	100M,active	
on	1G,inactive	
on	1G,active	

always on
blinking

Logic Function Table

/OE	SEL	Function
H	X	I/O's = Hi-Z
L	L	D(+/-) to D(+/-)A
L	H	D(+/-) to D(+/-)B

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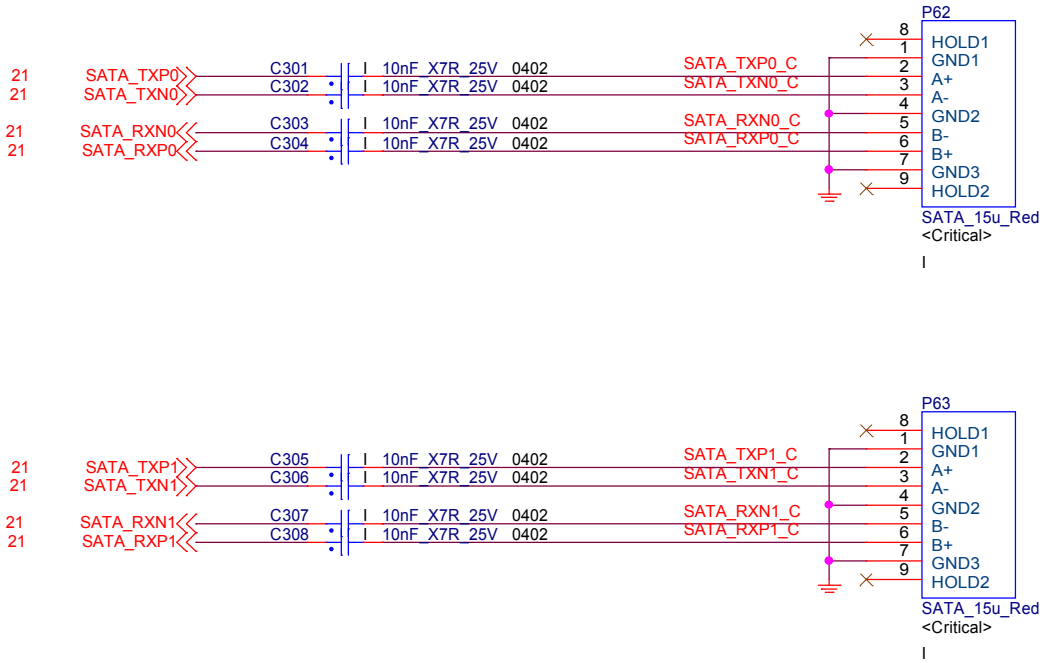
SATA 3.0 Port0,1



SATA GEN3.0

RED

SATA GEN3.0

RED

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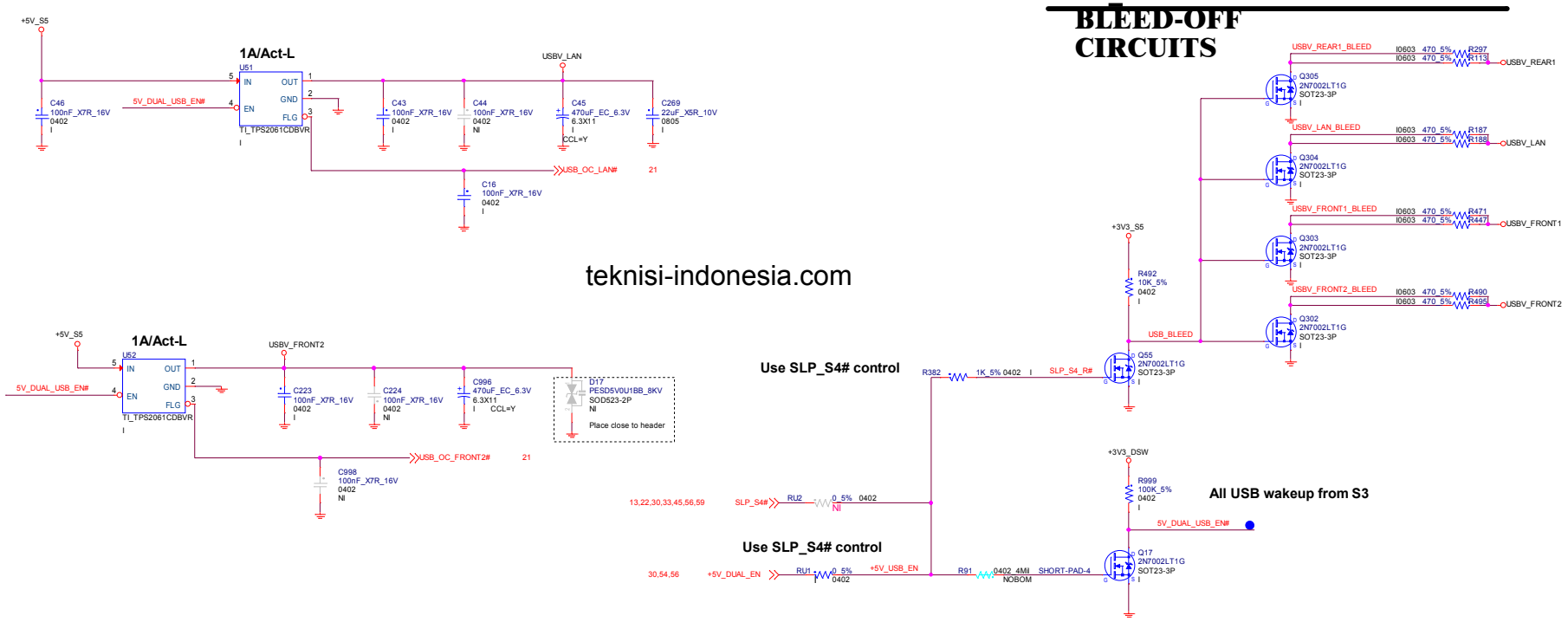
5V_USB BLEED-OFF CIRCUITS



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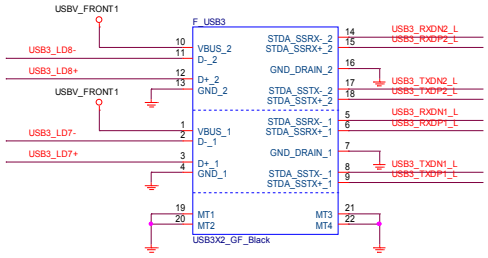
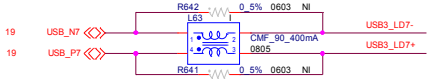
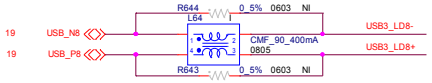
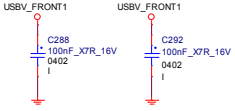
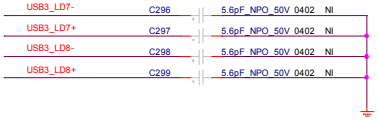
Front USB3.0X2

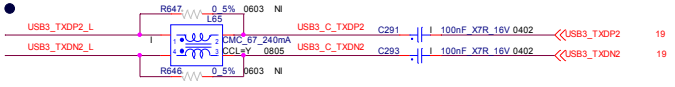




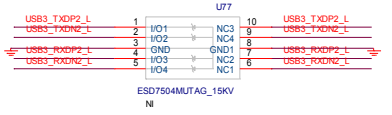


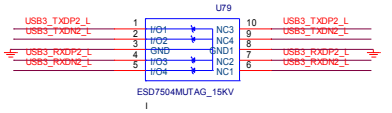


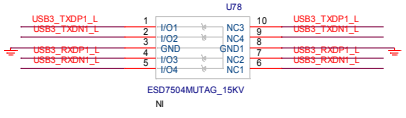


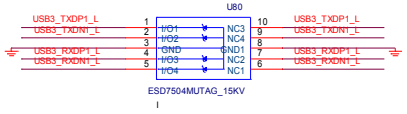


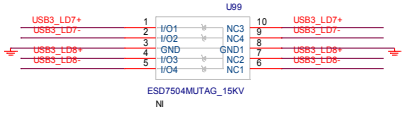
ESD suppressor

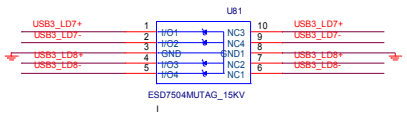












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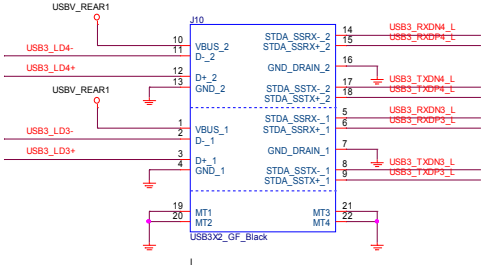
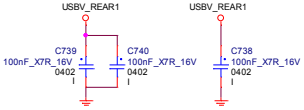
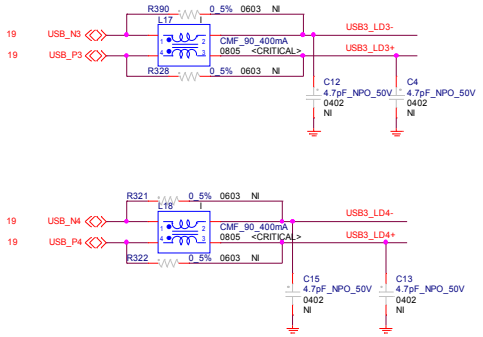
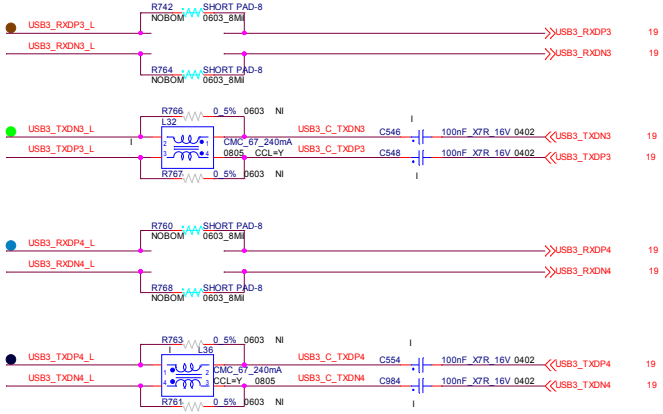
REAR USB3.0X2

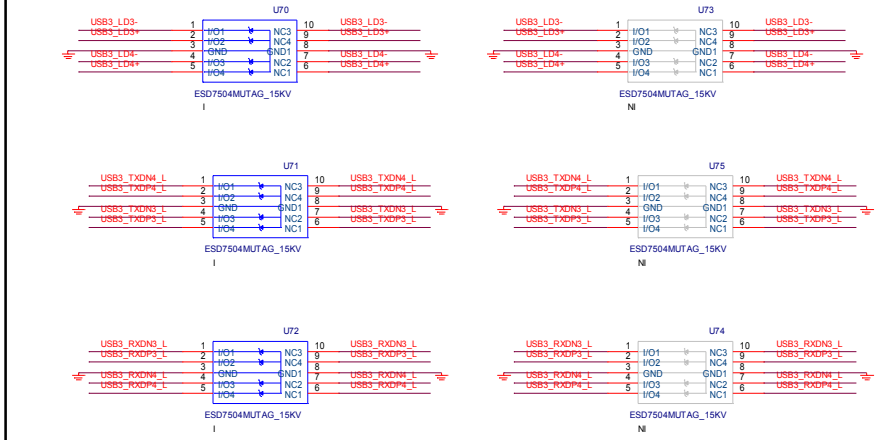








ESD suppressor



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Title: REAR USB3.0 X2		
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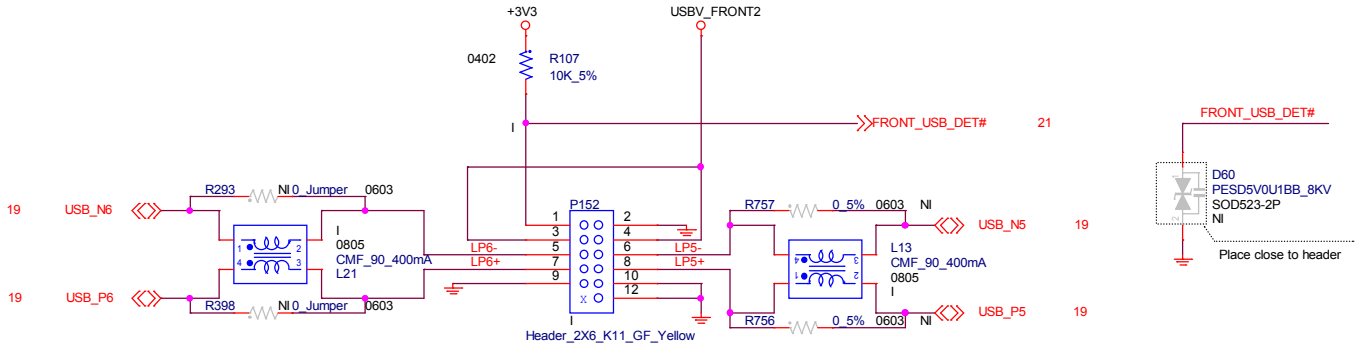
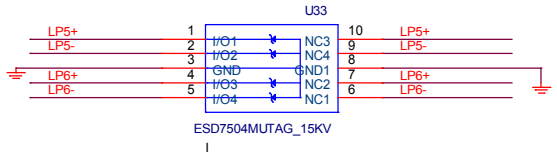


ESD suppressor



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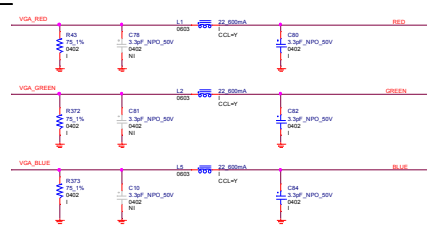
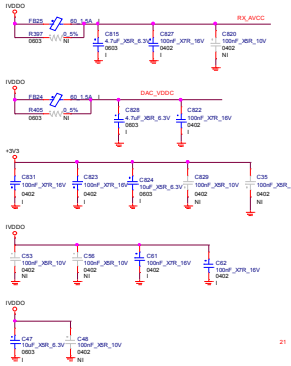
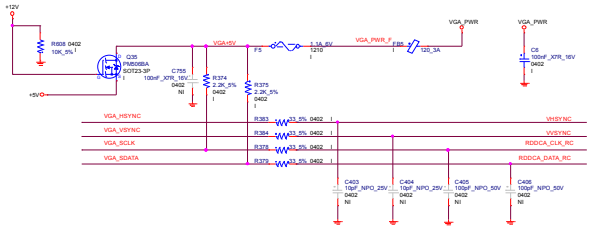
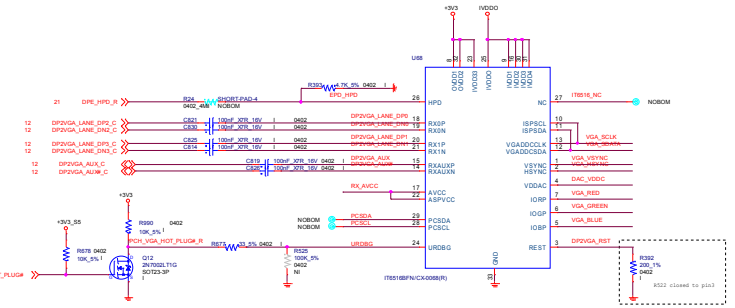
VGA





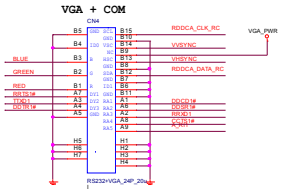


DP to VGA_IT6516B

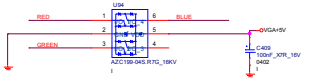


Pin24 [URDBG]	Pin26 [HPD]	VGA Device
HIGH	HIGH	Plug in or Un-Plug
LOW	HIGH	Plug in
LOW	LOW	Un-Plug

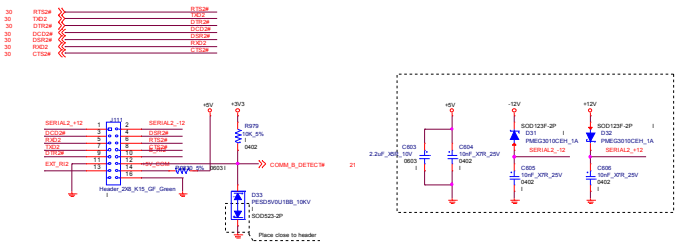
VGA + COM

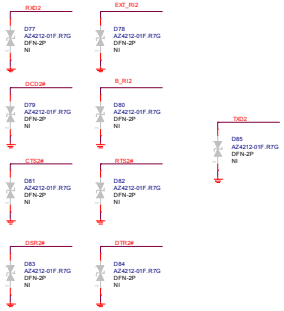


ESD pads are as close as possible to I/O connector pins.
capacitor pads are as close as possible to the ESD diode.

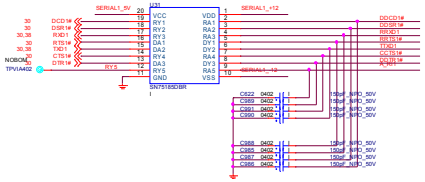


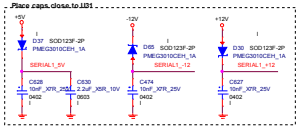
COM2 on Header



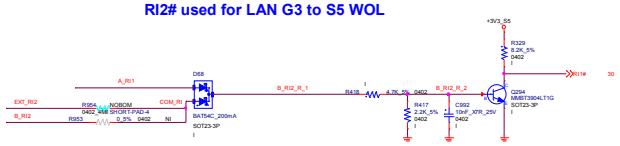


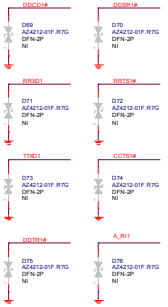
COM1 on board





COM1/COM2 both use RI1# RI2# used for LAN G3 to S5 WOL





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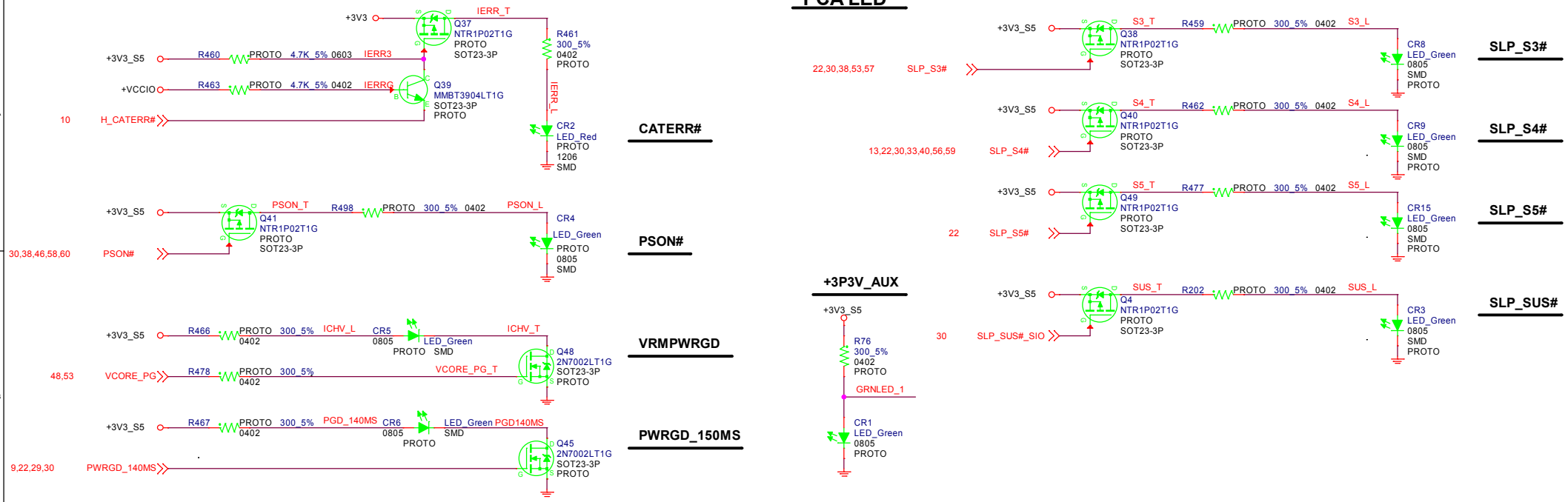
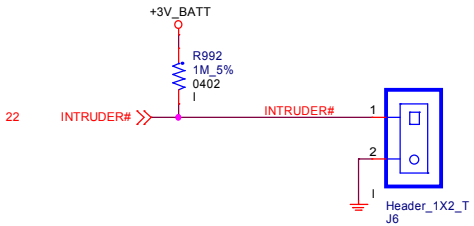
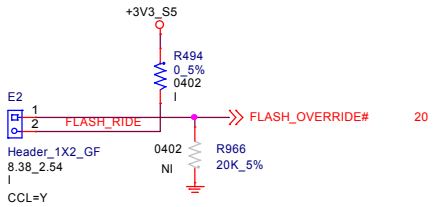
PCA LED



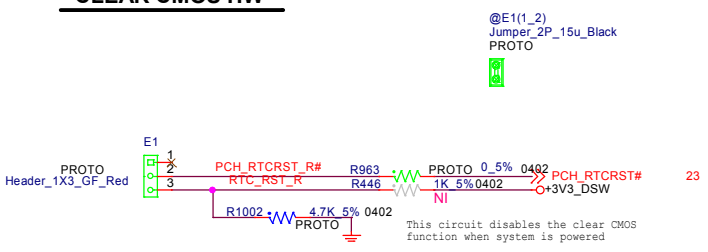
Case Open



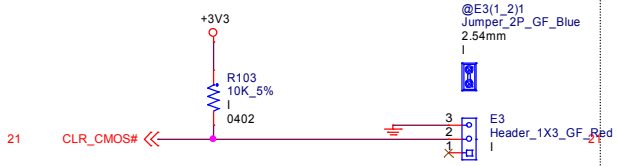
FLASH OVERRIDE(ME Disable)



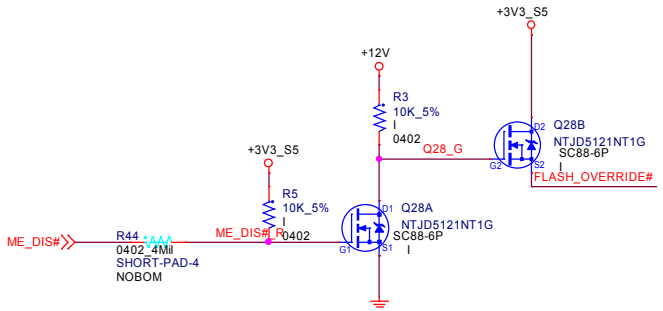
CLEAR CMOS HW



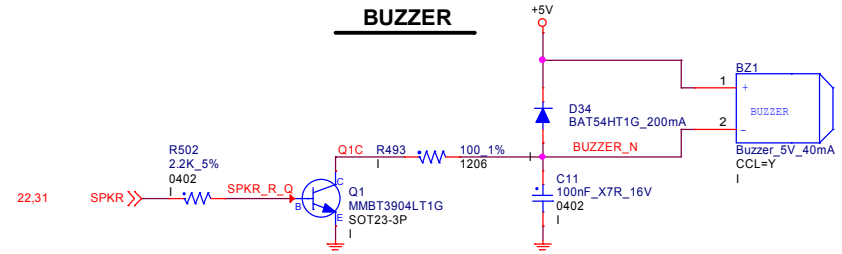
CLR CMOS SW



SW FLASH OVERRIDE



BUZZER



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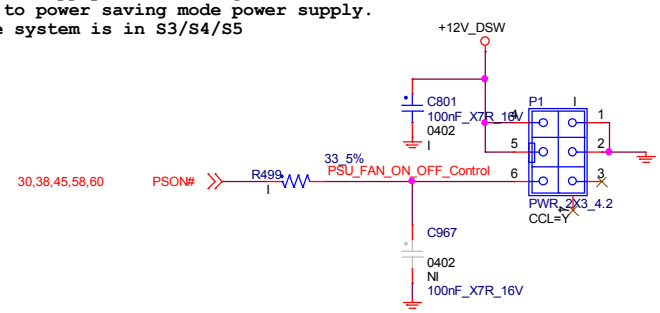
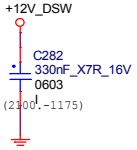
Power Input Connector

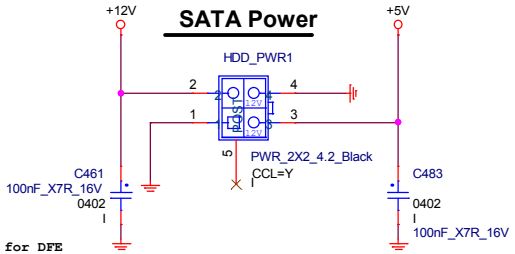
PSON# is an active low that allows the power supply fan and trig the PSU to go down to power saving mode power supply. when the system is in S3/S4/S5



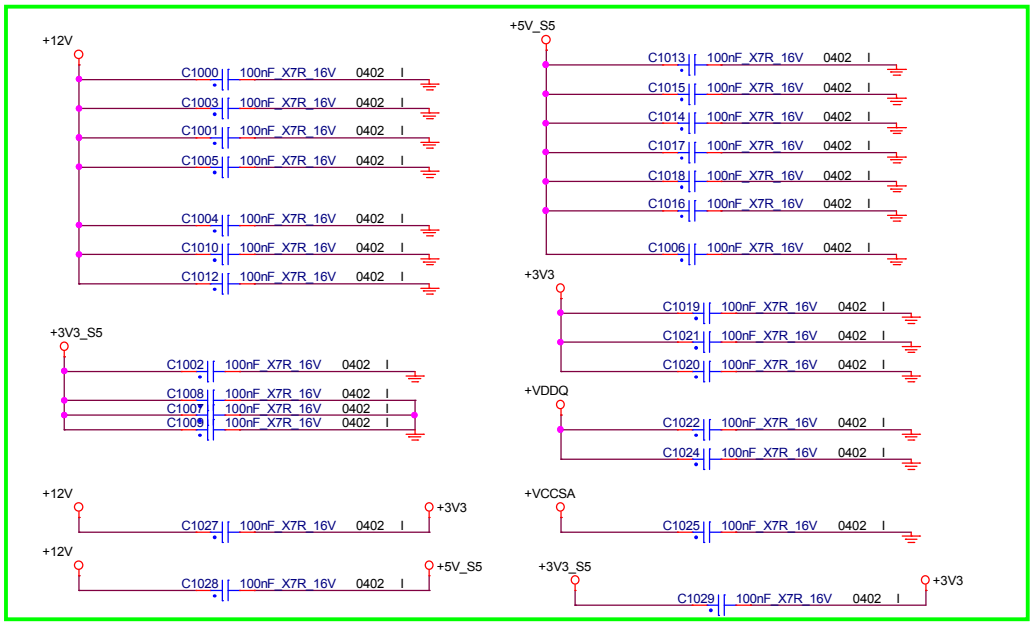
For EMI surge issue



SATA Power



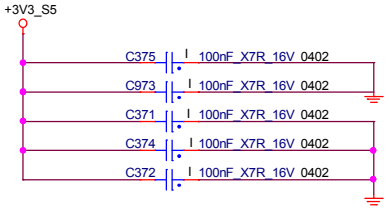
8/14: Layout request for DFE

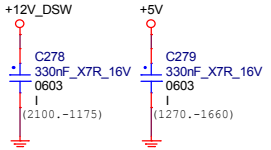


EMI CAP

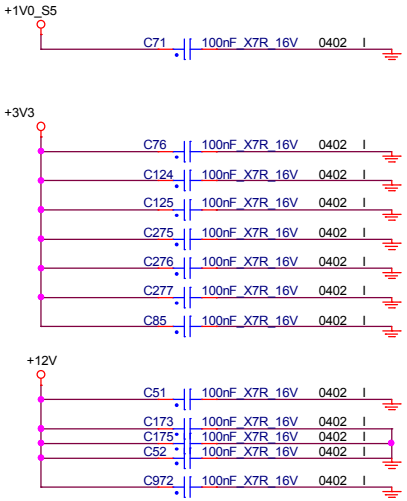
FXN EMI SUGGESTED PLACEMENT

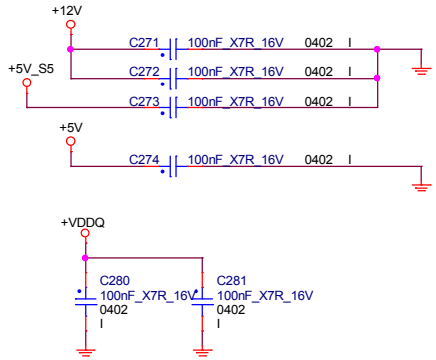
Stitching caps





Stich CAP





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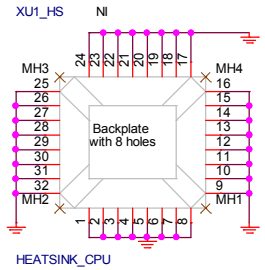

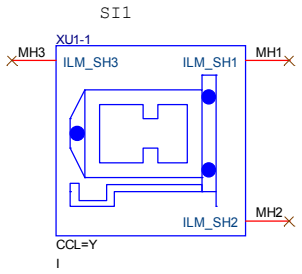

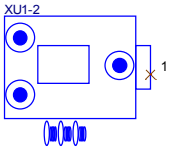

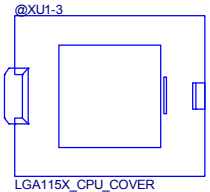

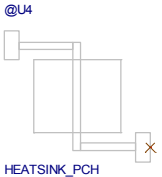

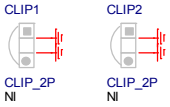

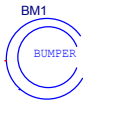

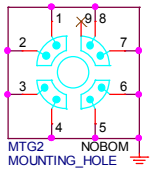

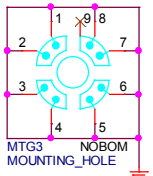

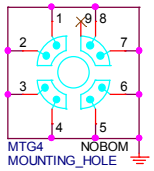

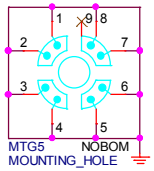

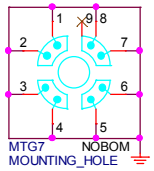

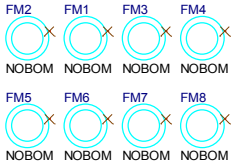

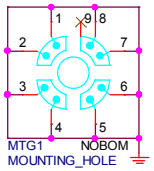

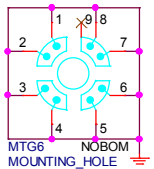

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B	M710e	SVT

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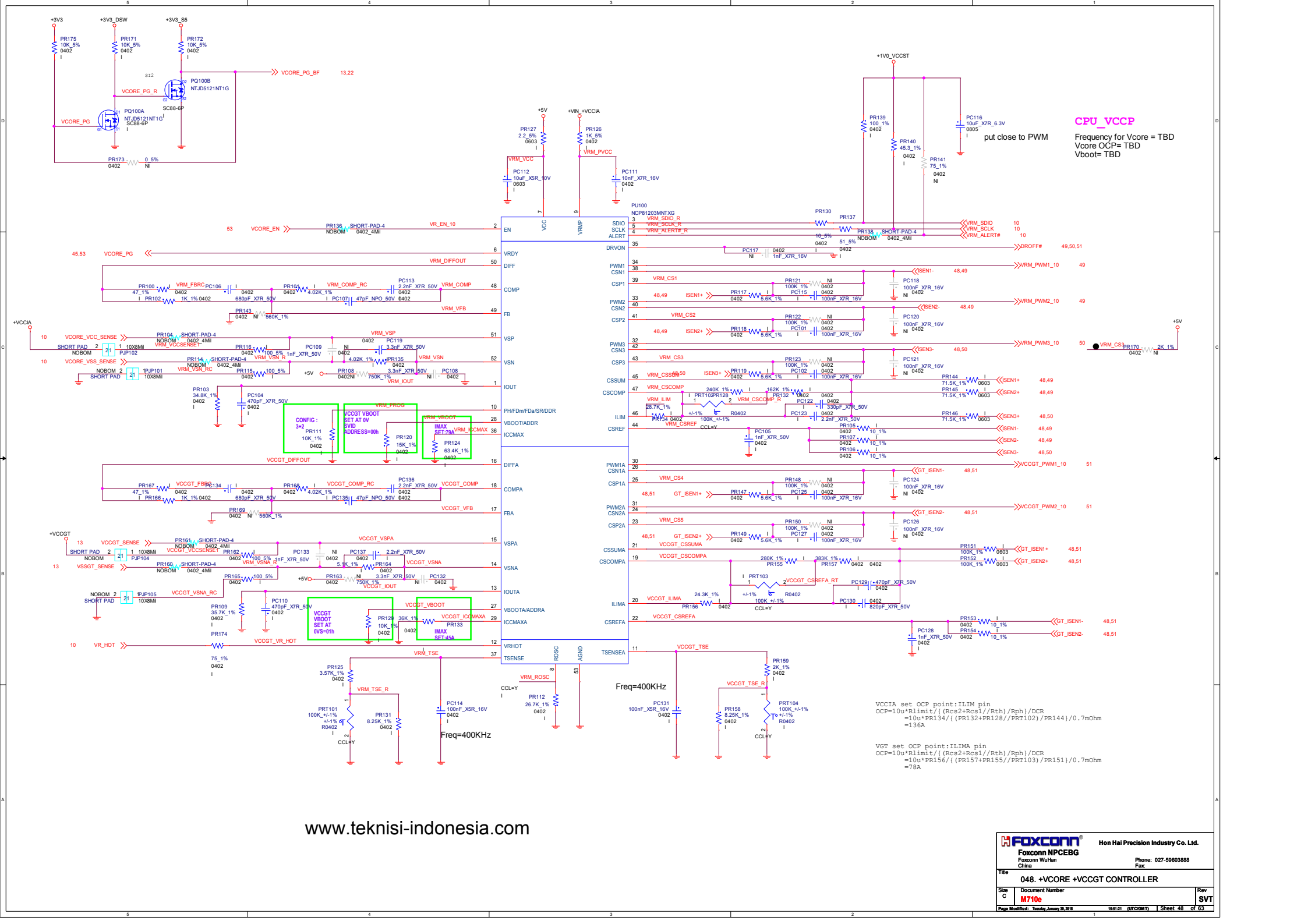

Foxconn NPCEBG	Hon Hai Precision Industry Co. Ltd.
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Title	048. +VCORE +VCCGT CONTROLLER
Size C	Document Number M710e
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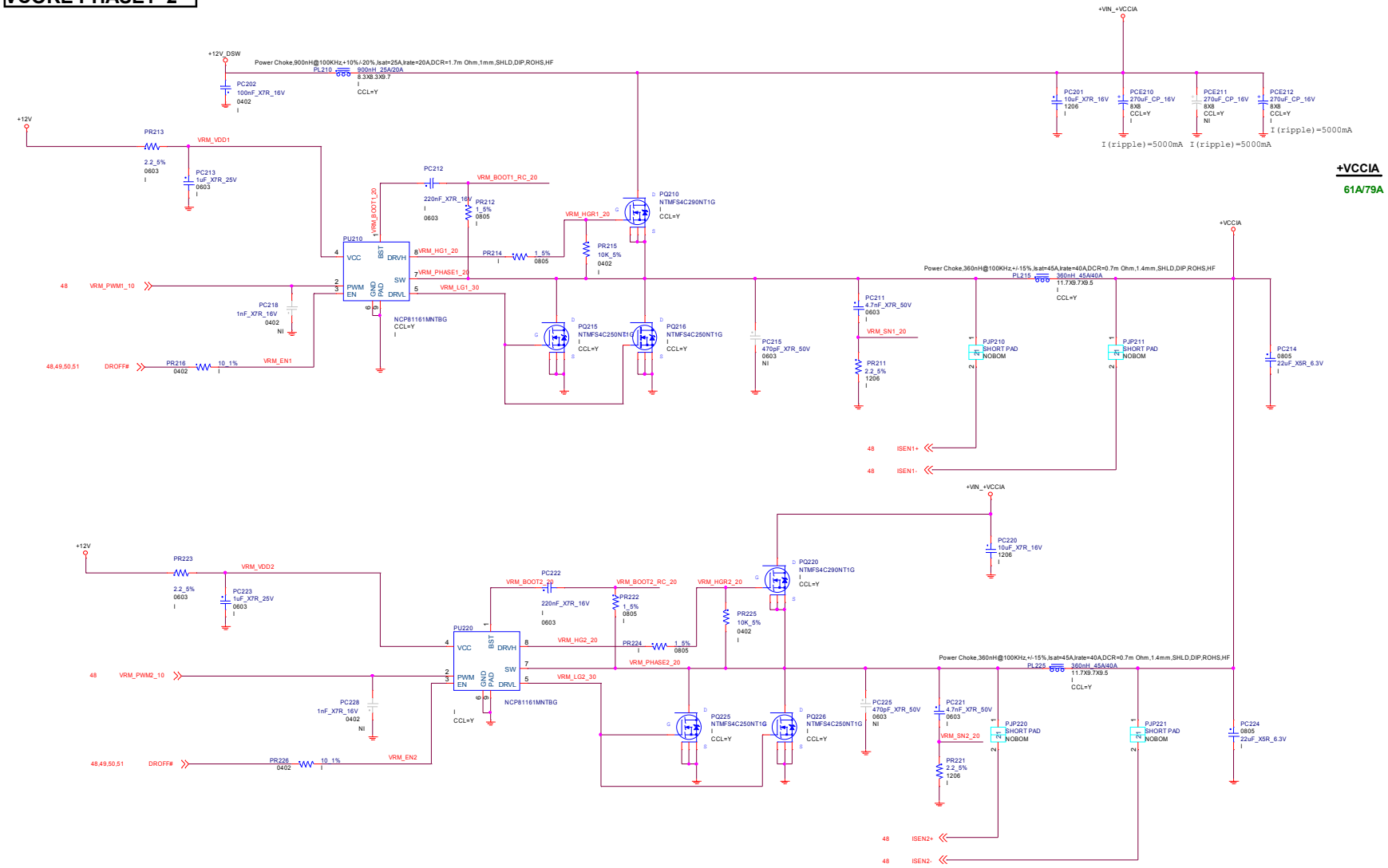
VCORE PHASE1~2



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Title	049. +VCORE PHASE 1 & 2
Size: Custom	Document Number: M710e
Rev	SVT
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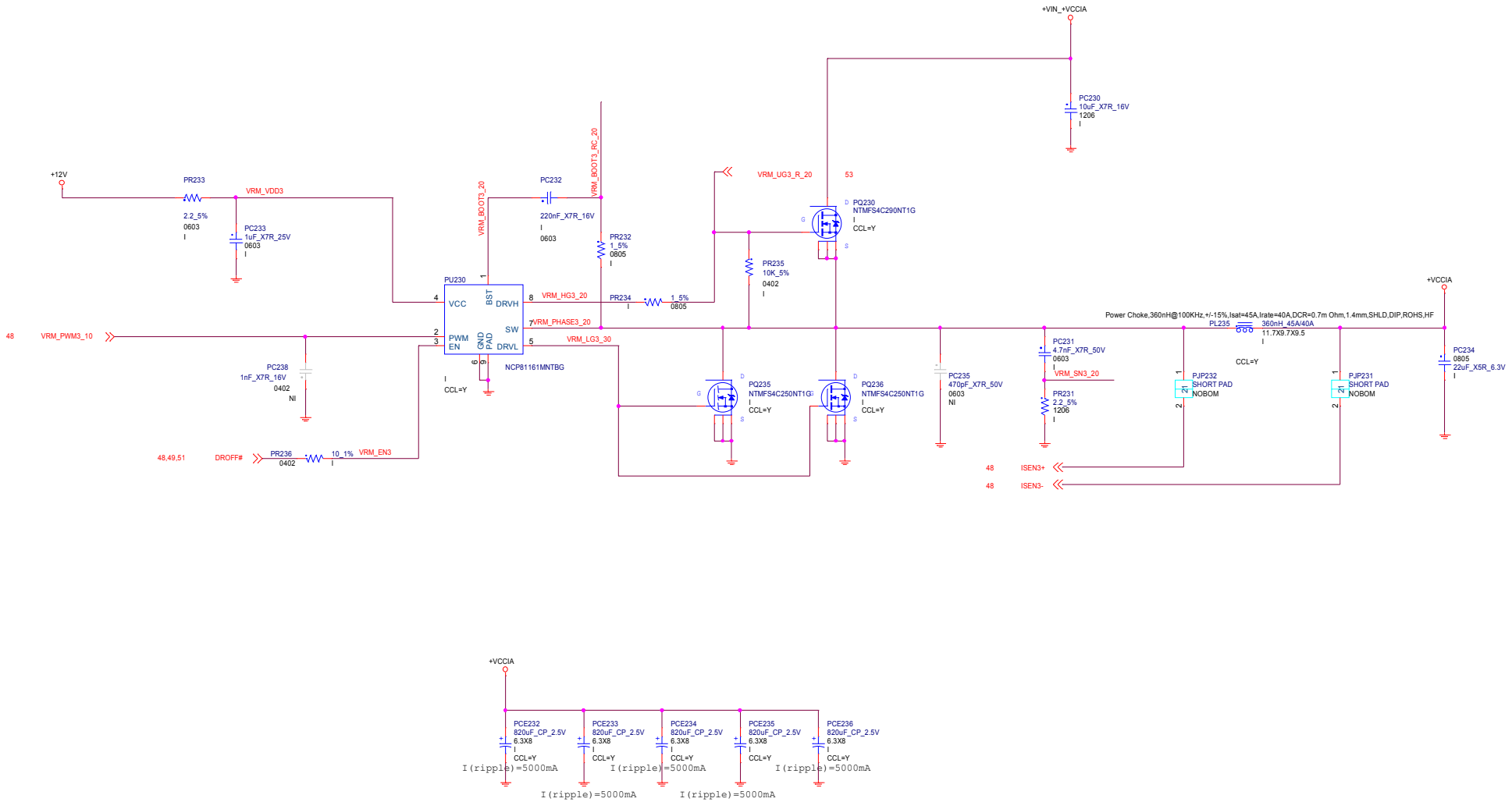
VCORE PHASE3



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Title: 050. +VCORE PHASE 3

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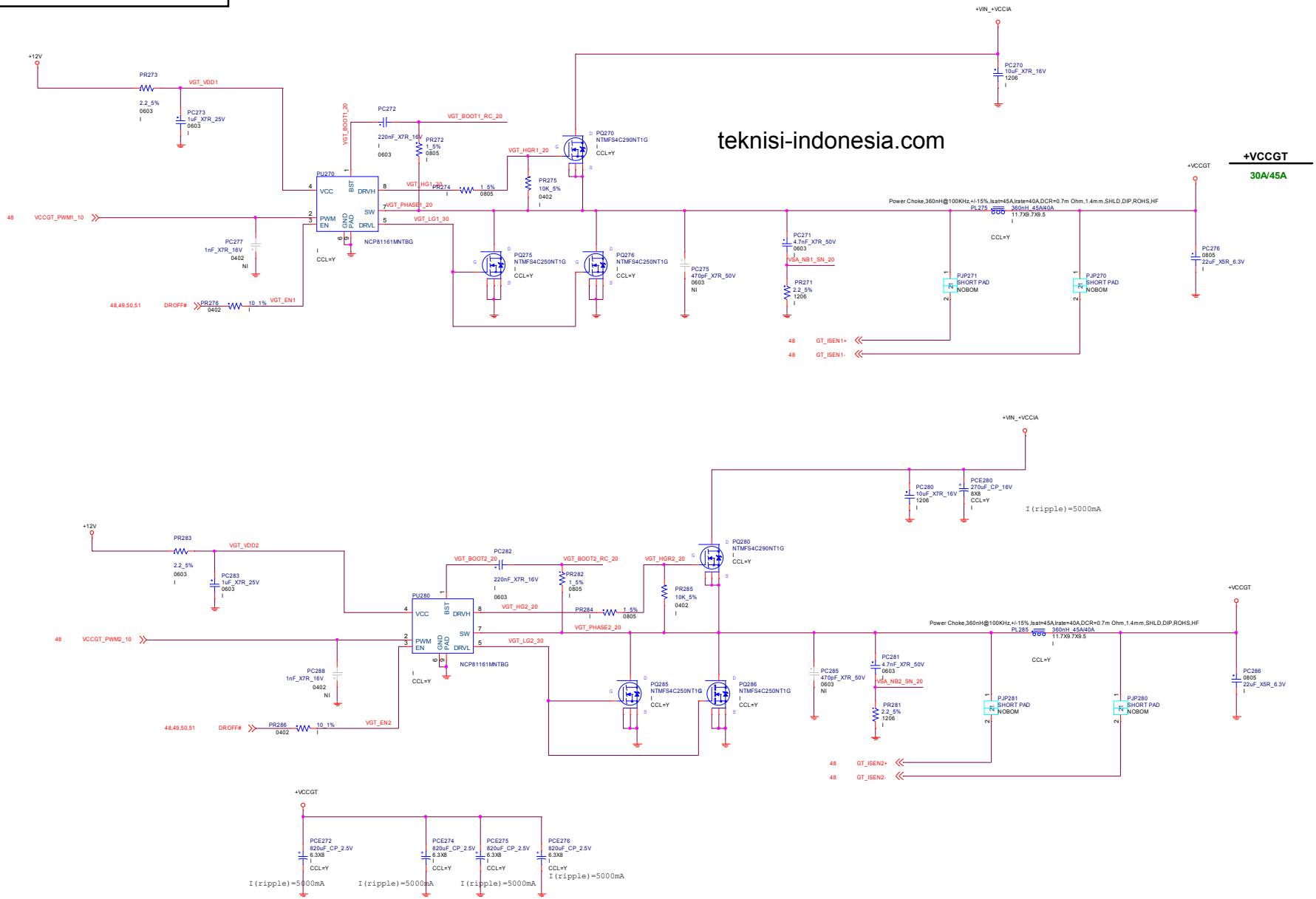
VGT PHASE1~2



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Title	051. +VCCGT Phase 1 & 2
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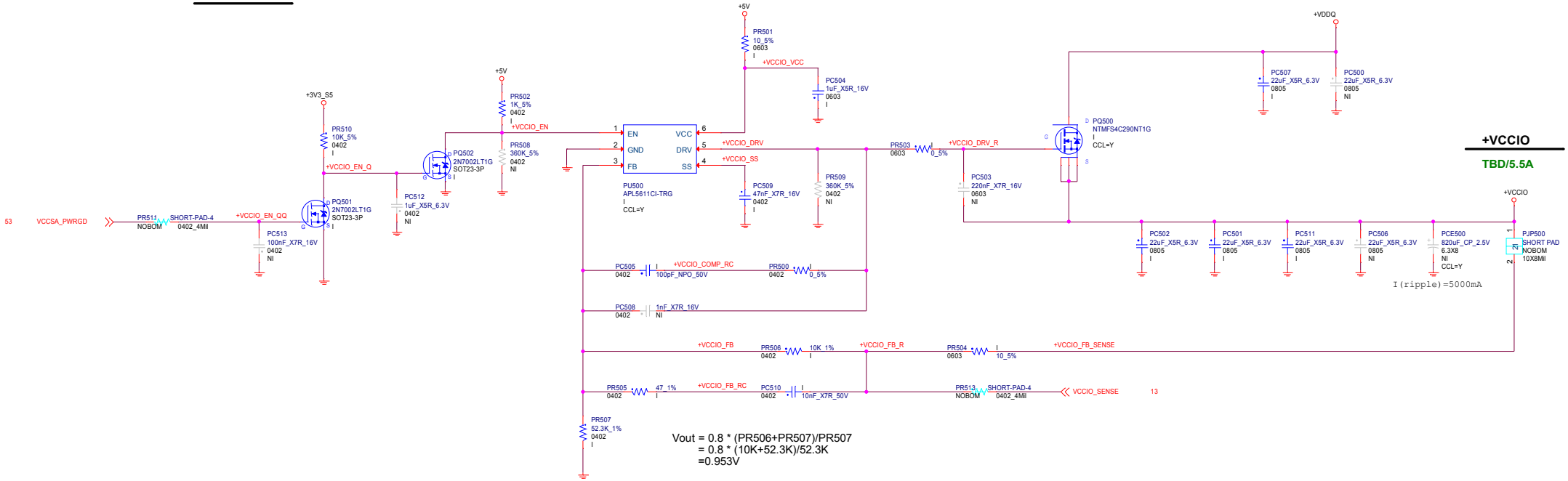
+VCCIO



Vout = 0.8 * (PR506+PR507)/PR507
= 0.8 * (10K+52.3K)/52.3K
=0.953V

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Title	052. +VCCIO
Size: Custom	Document Number: M710e
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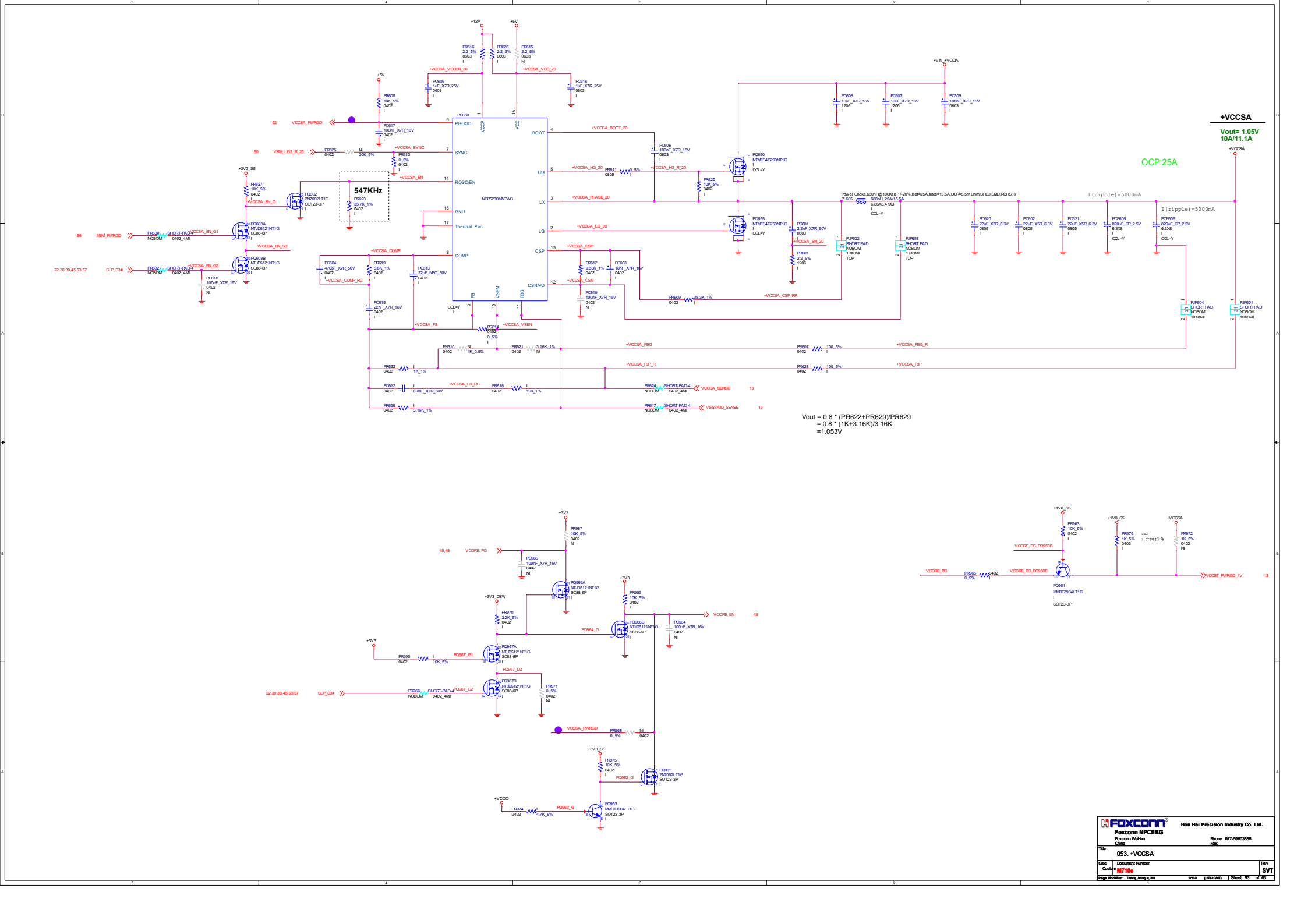
+VCCSA
Vout= 1.05V
10A/11.1A
OCP:25A
547KHz
NCP5230MNTWG
PGOOD
SYNC
ROSC/EN
GND
Thermal Pad
COMP
BOOT
UG
LX
LG
CSP
CSN/VO
VCC
VCCP
FB
VSEN
FBG
Power Choke,680nH@100KHz,+/-20%,Isat=25A,Irate=15.5A,DCR=5.5m Ohm,SHLD,SMD,ROHS,HF
I(ripple)=5000mA
I(ripple)=5000mA
Vout = 0.8 * (PR622+PR629)/PR629
= 0.8 * (1K+3.16K)/3.16K
=1.053V
+VCCSA
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053. +VCCSA
Size
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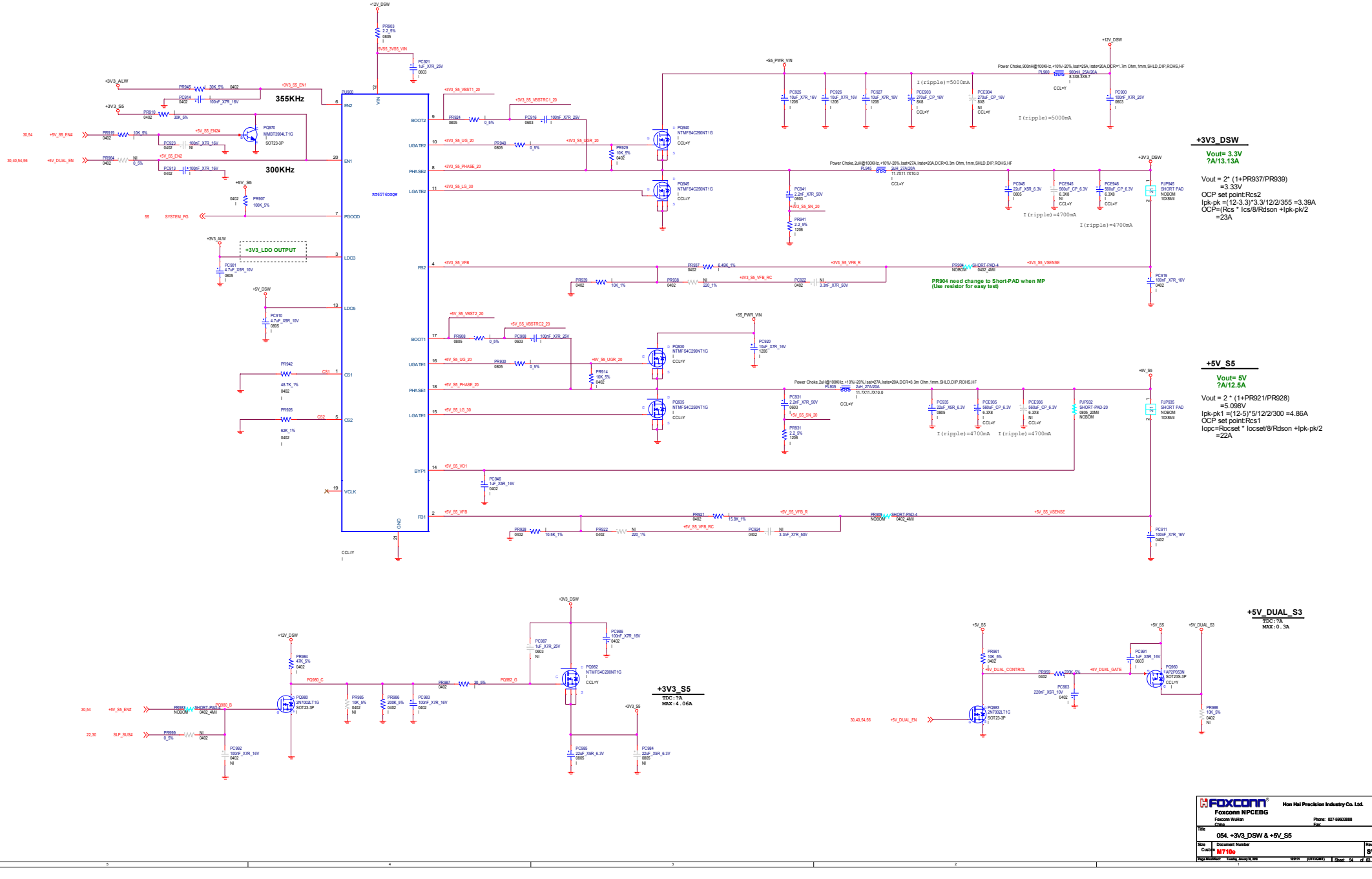
355KHz
300KHz
+3V_LDO OUTPUT
RT8567DGQW
+3V_DSW
Vout= 3.3V
?A/13.13A
Vout = 2* (1+PR937/PR939)
=3.33V
OCP set point:Rcs2
Ipk-pk =(12-3.3)*3.3/12/2/355 =3.39A
OCP=(Rcs * Ics/8/Rdson +Ipk-pk/2
=23A
PR904 need change to Short-PAD when MP
(Use resistor for easy test)
+5V_S5
Vout= 5V
?A/12.5A
Vout = 2 * (1+PR921/PR928)
=5.098V
Ipk-pk1 =(12-5)*5/12/2/300 =4.86A
OCP set point:Rcs1
Iopc=Rocset * Iocset/8/Rdson +Ipk-pk/2
=22A
+3V3_S5
TDC:?A
MAX:4.06A
+5V_DUAL_S3
TDC:?A
MAX:0.3A
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Title
054. +3V3_DSW & +5V_S5
Size
Custom
Document Number
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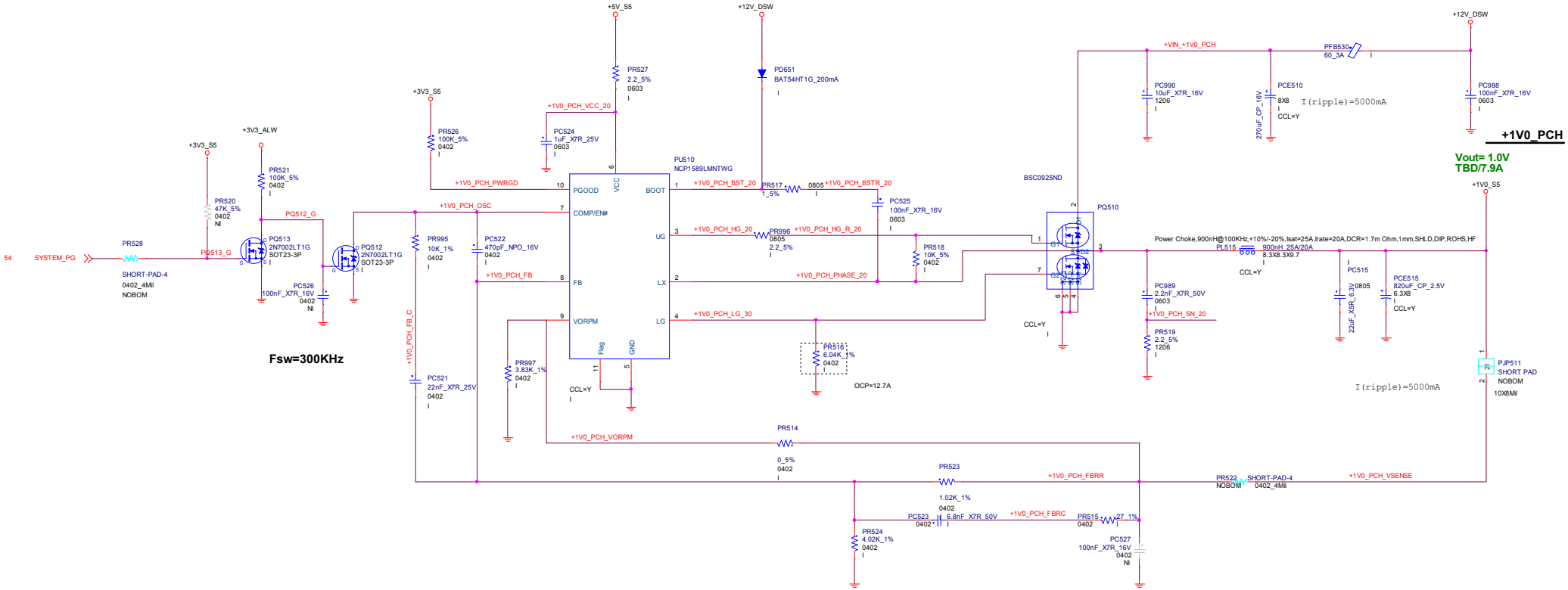

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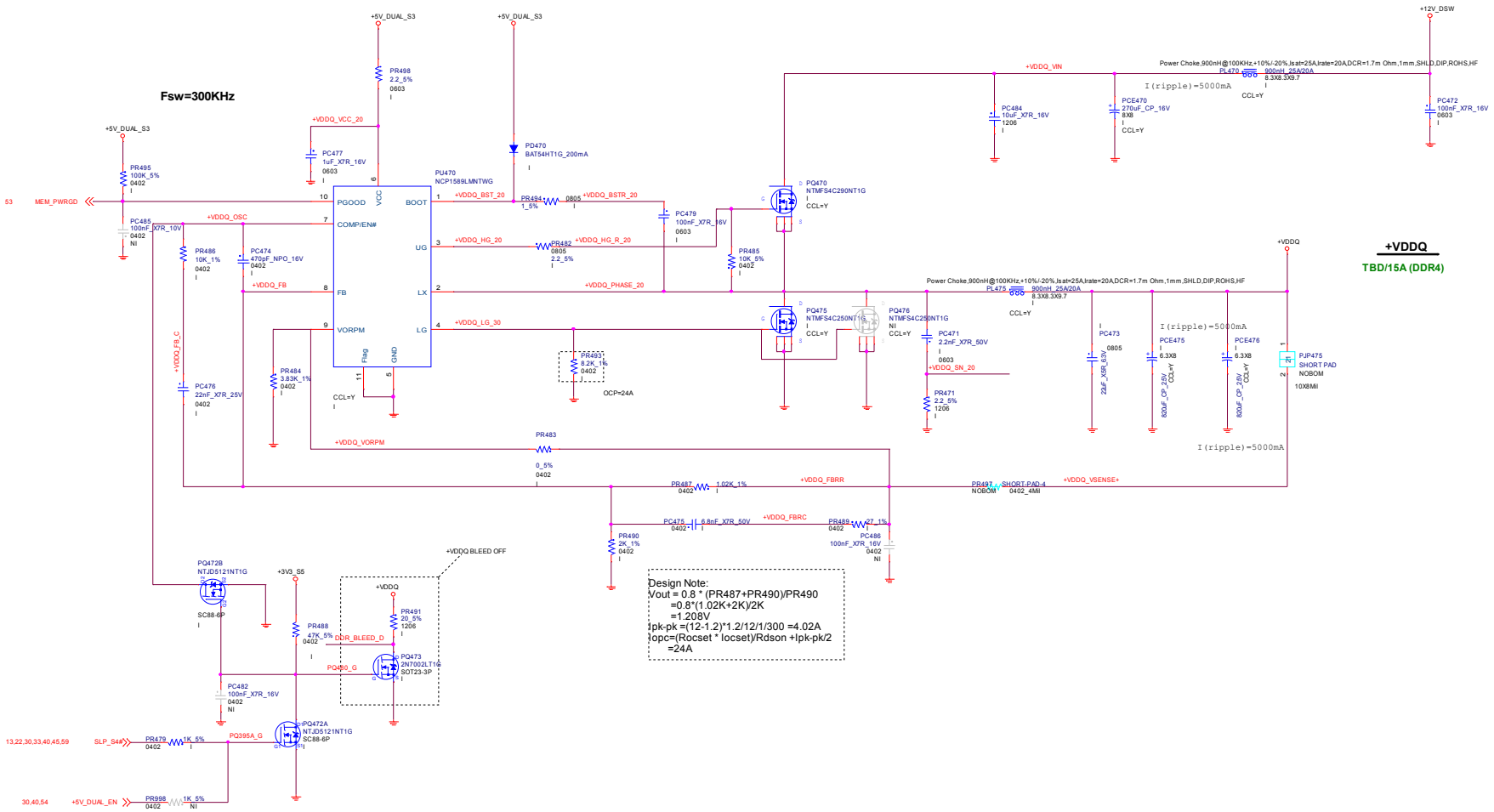
+VDDQ

Note: net-name:+VDDQ



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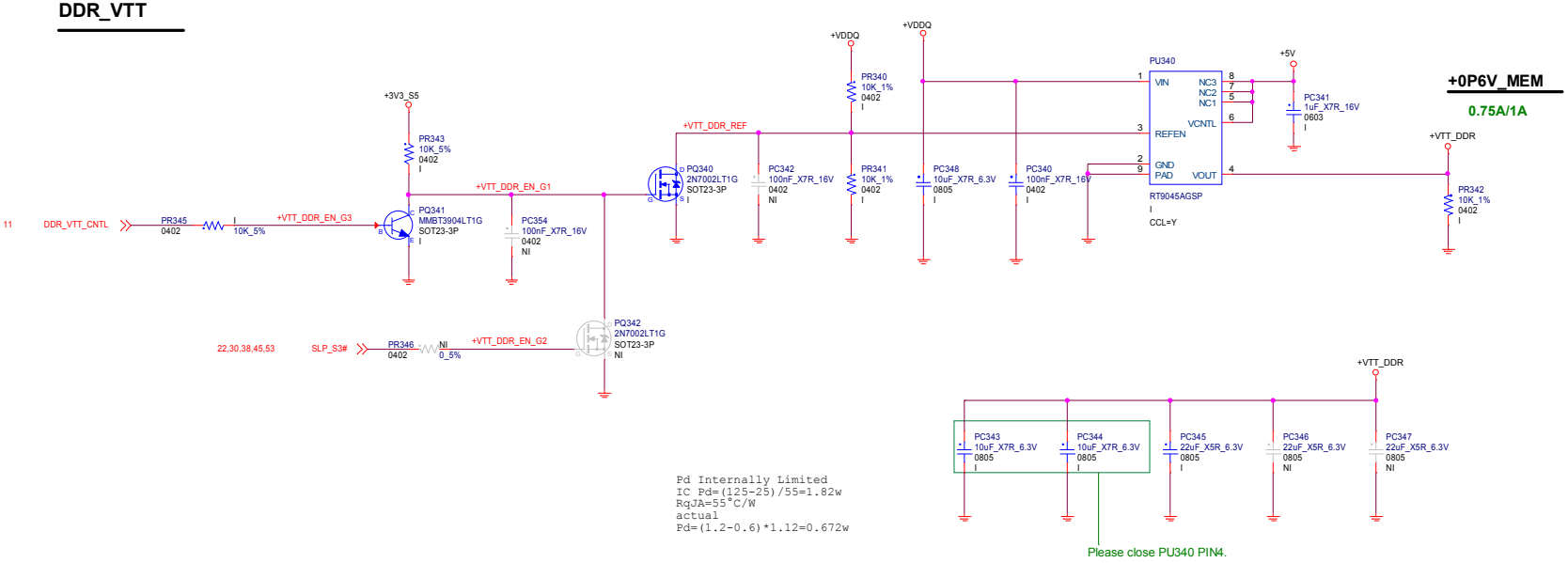
DDR_VTT



Pd Internally Limited
IC Pd=(125-25)/55=1.82w
RqJA=55°C/W
actual
Pd=(1.2-0.6)*1.12=0.672w

Please close PU340 PIN4.

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Title: 057. +VTT_DDR		
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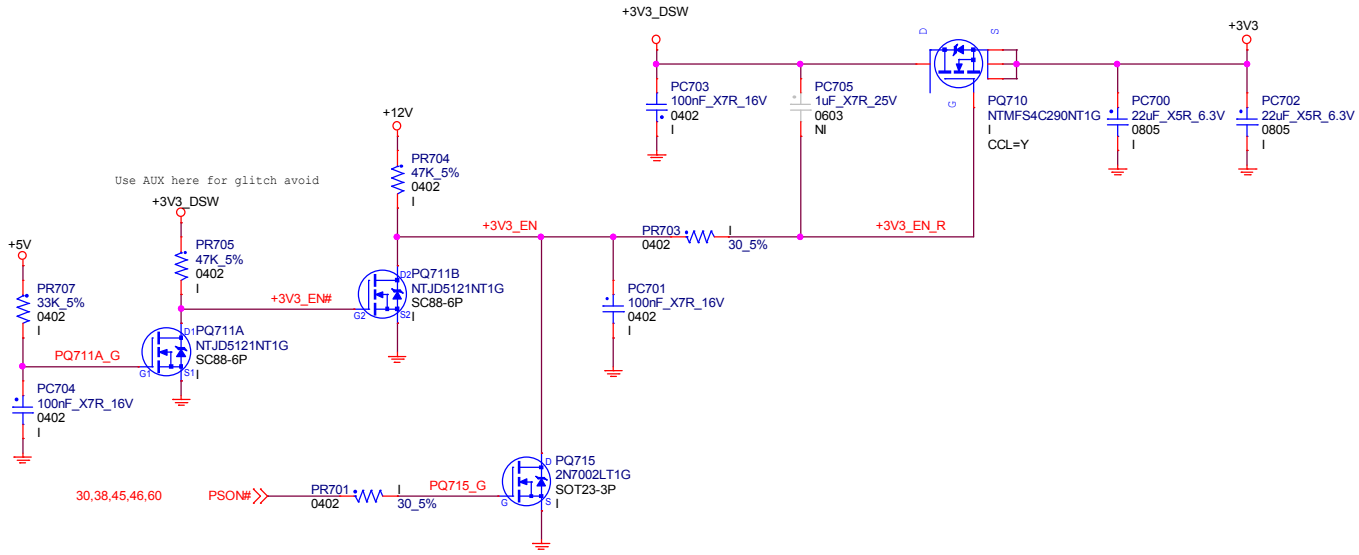
+3V3 (S0)

TBD/8.83A

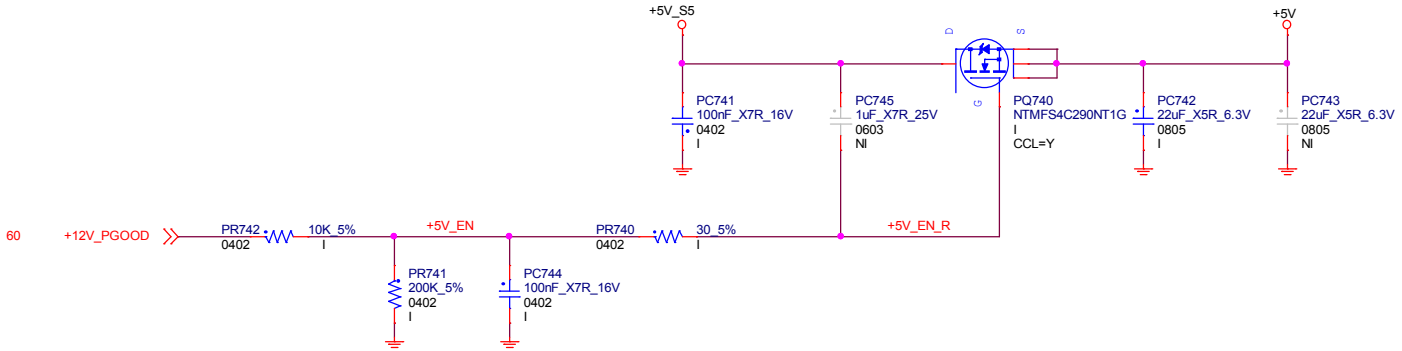
(S0-S5)



+5V (S0)

TBD/2.26A

(S0-S5)



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Title: 058. +5V & +3V3		
Size: Custom	Document Number: M710e	Rev: SVT
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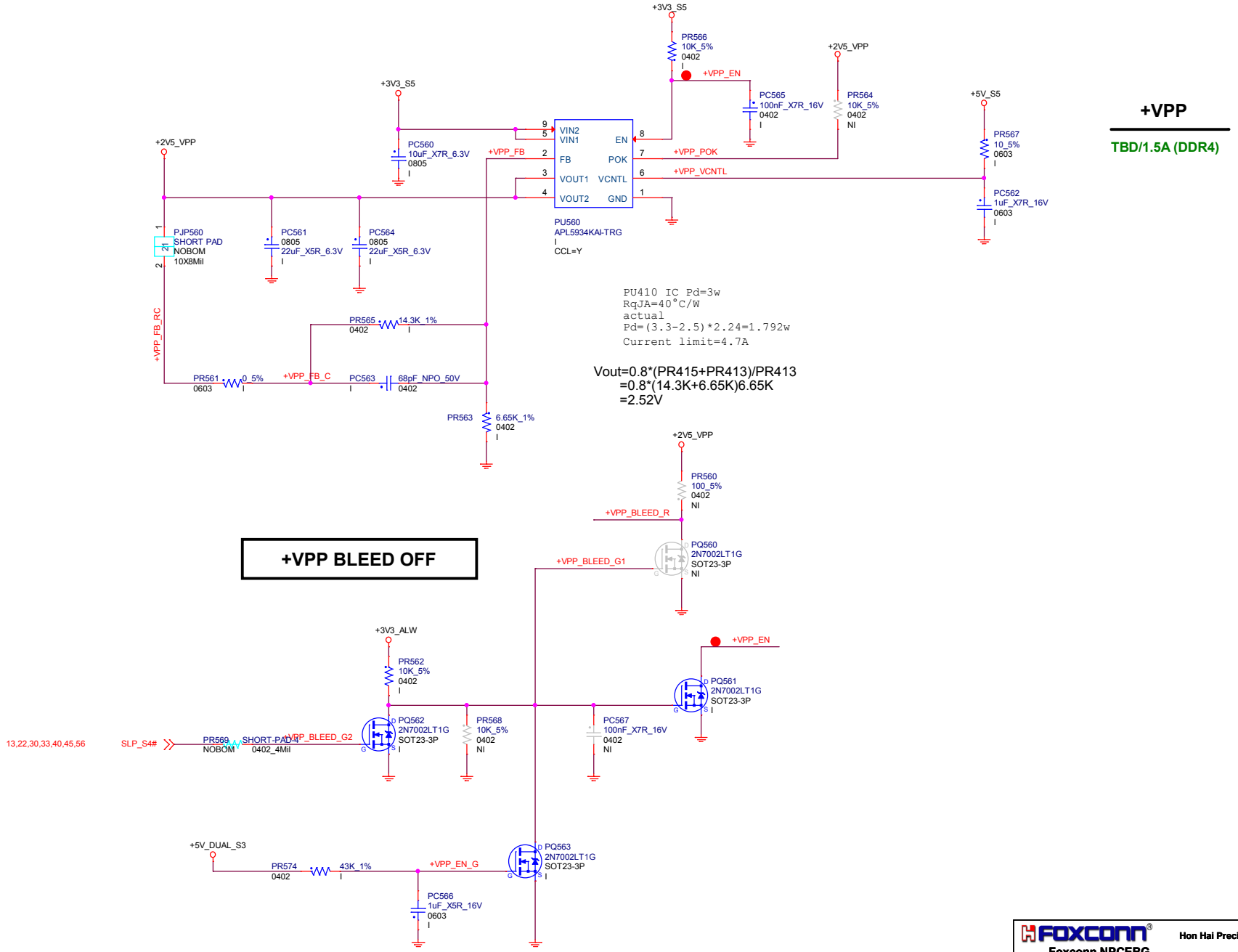

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Foxconn WuHan, China	Phone: 027-59603888, Fax:
Title	059. +2V5_VPP
Size A3	Document Number M710e
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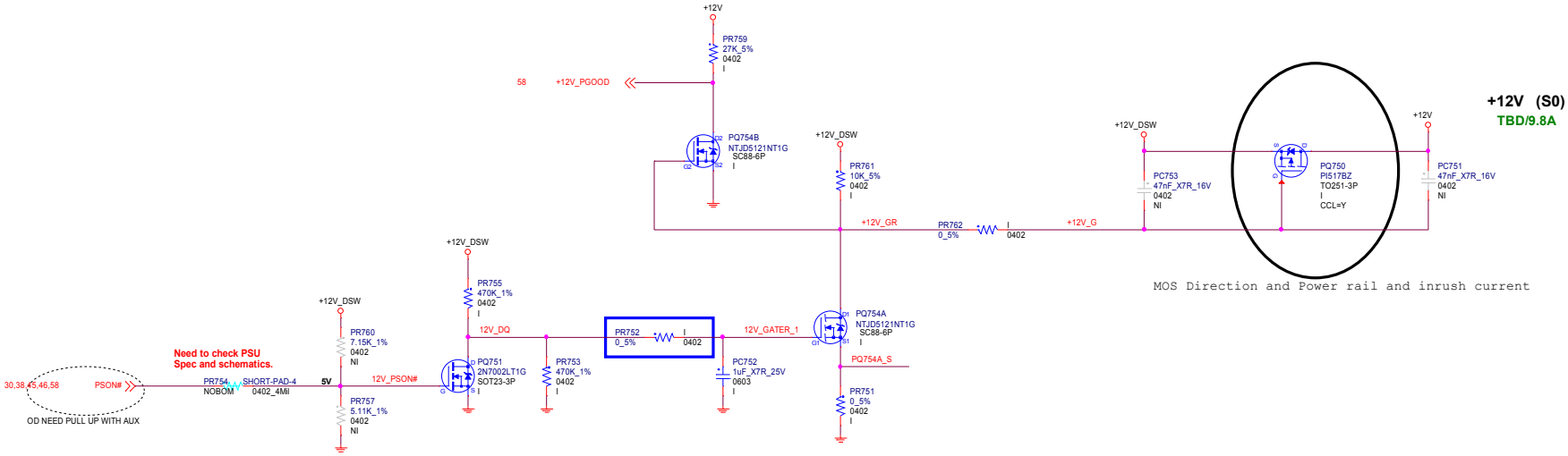
+12V



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Title: 060. +12V		
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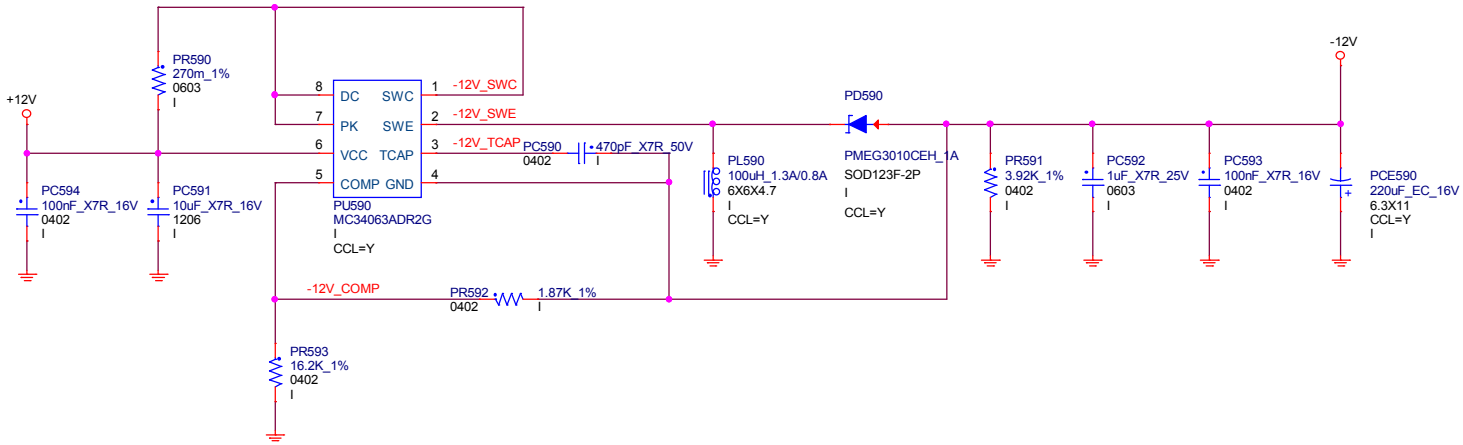
-12V

Vout= -12V
TBD/0.1A



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Title: 061. -12V		
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ET phase change List(DC Part)

20170801
1. Page 52: Delete PR512,PQ501A,PQ501B
Add PQ501
SLP_S3# change to VCCSA_PWRGD
2. Page 53: Delete PQ603 PR602 and net VCCIO
Add PQ603A PQ603B PR630 PR602 and net MEM_PWRGD SLP_S3#
Delete PQ693 PC991 PR974 and net VCCSA_PWRGD
Add PQ963 PR974 and net VCCIO

20170804
1. Page 54: PCE945 change from I to NI
PCE946 change from NI to I close to +3V3_S5 Vsense
PC946 change from NI to I for +3V3_DSW jitter fail
Delete net SYSTEM_PG
2. Page 61: PCE590 change from CHEMICON_EKY-160ETD221MF111 to CHEMICON_EKY-160EC3221MF111

20180818
1. Page54：PR959 change from 10K to 220K and add PC991 for power sequence TPLT16 issue

20180831
1. Page54：PQ900 change from RT6576EGQW to RT6576DGQW

SDV phase change List(DC Part)

20170912
1. Page 55: NCP1589L VCC change from +12V_DSW to +5V_S5 and PC526 change from NI to I for +1V_PCH overshoot

20170920
1. Page 52: PC509 change from 100nF to 47nF for VCCIO rise time fail
2. Page 60:PQ750 change from APEC_ AP6679BGJB-HF to NIKO_PI517BZ

20170929
1. Page 54: PR926 change from 57.6K to 71.5K for +3V3_DSW OCP fail
2. Page 59:PU560 change from ANPEC_ APL5930KAI-TRGIY to ANPEC_APL5934KAI-TRGIY

20171018
1. Page 56: PR493 change from 12K to 11.8K for VDDQ OCP test

SIT phase change List(DC Part)

20171127
1. Page 54: PR926 change to 62K for +3V3_DSW OCP fail,PR942 change to 48.7K for +5V_S5 OCP fail
2. Page 56:PR493 change to 8.2K for VDDQ OCP test

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Title: 62. Changelist-DC

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ET phase to SDV phase change List(EE Part)

20170801
1.Page29/30：Change RN1,RN2 RN12 from RESA to single resistor to meet Lenovo ECSL rule.
2.Page 34：Correct E16 PIN1/Pin3 wrong connection.
3.Page 43：Add R998 for Dot LED since SDV phase PCA spec change
4.Page 4：Add SW ME disable circuit follow S510

20170804
1.Page33：Change SW1 PN since lenovo SDV phase power switch need LED.
2.Page 47：Add one bumper BM1 since SID request
3.Page 16/18：Change DIMM reference from XMM2/XMM1 to DIMM1/DIMM2 to meet Lenovo Rule
4.Page 44：COM2 header add ESD （NI ）since EMC request
5.Page 30：Change SR12/SR8/SR9/SR10/SR11 from I to NI according ITE confirm

20170809
1.Page31：Change AC10 from I to NI to fix ET phase internal speaker can not work issue.
2.Page31：Change AR20/AR81/AR45 from I to NI to fix ET phase Rear IO headphone have noise issue.
3.Page 30：Change Change SR22 pull high voltage from +5V_S5 to +5V_DUAL_S3 to fix system can not go to deep S5 issue
4.Page 30：+5V_DUAL_EN add 10K pull high SR60 and pull high to +3V3_S5 to fix s ystem can not resume from S3 issue

20170814
1.Page46：Add 27pcs EMI Cap for Layout DFE request
2.Page19：Change LPT from FOXCONN_HC5213F-B3(EOL) to FOXCONN_HBF1131-L101D-EH
3.Page32：Change AQ8 from ON_MBT3904DW1T1G to AQ8/ AQ9 NEXPERIA_PBSS4320T

20170825
1.Page1：Update PCB1 description

SDV phase to SIT phase change List(EE Part)

20170905-AM1030
1.Page47：Change Mtg1,Mtg6 from 3.5mm to 3.96mm.

20170920-AM1830
1.Page48~62: Update DC SCH:
L_BIDDING_SDV_SCH_2017_0919_AM0811_PWR .DSN
2.Page32: AR65,AR66,AR67,AR68,AQ8,AQ9 change from NI to I. --For Pop noise issue.

20170922-AM0850
1.Page44: D33 change from NXP_PESD5V0U1BB to NEXPERIA_PESD5V0U1BB. Need Link CIS. 已经link CIS 20171121
2.Page33: Update SW1 PN. Need Link CIS, only for make BOM. 已经link CIS 20171107

20170922-PM1445
1.Page30: SQ8,SQ10,SR249,SR250 change from I to NI.
2.Page43: L13 change from 720401100-092-H to 720400M00-059-H. ---For BOM source
2.Page22: C228 change from 620102M03-015-H to 620102M02-015-H. ---For BOM source

20170925_AM0940 PM1950
1.Page30: SQ11,SR268 change from I to NI.
2.Page48~62: Update DC SCH:
L_BIDDING_SIT_SCH_2017_0925_AM0830.DSN
3.Page34: U19 change from W25Q64FVSSIQ to W25Q64JVSSIQ. Need Link CIS. 已经link CIS 20171121
4.Page27: Q291 change from NIKO_P8503BMG to NIKO_PM506BA.
5.Page44: Q35 change from NIKO_P8503BMG to NIKO_PM506BA.
20170925_PM1950
1.Page30: SU2,SC209,SR267,SR266 change from PROTO to NI. Not use
2.Page9: Change D5 from PROTO to NI, and add R1000,R1001 for XDP hot-plug.

20170928_PM1920--- Change part 1
1.Page34: Change DP2VGA IC U68 from ITE_IT6516BFN/CX to ITE_IT6516BFN/CX-0068(R).
Need Link CIS. Only for BOM. 已经link CIS 20171107

20170928_PM1920--- Change part 2
Page31:
1.+5V_PVDD power change from +5V_S5 to +5V supply.
2.+3V3_DVDD power change from +3V3_S5 to +3V3 supply.
3.+1V5_VDD power change from +3V3_S5 to +3V3 supply.
(AR13 pin1,AU4 pin3)
4.AR64,AR28,AR6 pull high power change from +3V3_S5 to +3V3 supply.
Page32:
5.Rear Audio connector AJ1 Pin6,pin7 add AR96 to GND,and add AR95 to AGND.
6.AR97 change from ON_MBT3904DW1T1G to NEXPERIA_PBSS4320T.Add AQ11.
20170929_AM0920
1.Page31:
Change AR10 pull high power from +3V_BATT to +3V3_DSW.
20170929_AM1000
1.Page48~62: Update DC SCH:
L_BIDDING_SIT_SCH_2017_0929_AM0800.DSN
20170929_PM1215
1.Page48~62: Update DC SCH:
L_BIDDING_SIT_SCH_2017_0929_AM1038.DSN
2.Page31:
Add AR97 pull high to +3V3_DSW.and dummy AR10 pull high +3V_BATT.

20170930_PM1605
1.Page47: Change BM1 from PINGOOD_R1005D-YAB to SPEEDGOLD_SG428.
---Follow SS Jessie suggestion change.

20171011_PM1430
1.Page45: Add R1002 to GND,change R446 from I to NI.

20171011_PM1920
1.Page30: SQ8,SQ10,SR249,SR250,SR61 change from NI to I.
Follow SIO vendor debug Dot LED power on issue.
2.Page30: Dummy C153 for PLTRST_N SI Rest test issue.
3.Page23:Change C162，C165 from 12pF to 15pF for EIV test.
Change from WALSIN_0402N120J500LT to WALSIN_0402N150J500LT.

20171012_AM1000
1.Page30: SR248 change from I to NI. And add SR270,Q306 connect to PSON#.
Debug Dot LED lighting issue.
2.Page28: Add R1003 connect to PRSNT#. Follow PCIE X16 design.
3.Page30: Add net name SQ10B_D between SR61 and SQ10B.

20171012_PM1900
1.Page40: Add RU1,RU2 for USB power enable.add net name +5V_USB_EN.
2.Page32: AR95 change to NI,AR96 change to I, for pop noise.

20171013_AM0930
1.Page40: RU1 change to I,RU2 change to NI.
2.All page: TitleBlock5 Foxconn change Rev from SDV to SIT.
3.Page9: R89，R92，R793，R93，R97，R1000，R1001，R86，R792，R87 change from Proto to I.

20171014_AM1130
1.Page24: Add RP44(NI) pull high for BOOT HALF STRAP.
2.Page9: Add R1004(NI) for XDP.

20171014_PM1530
1.Page11: Add R1005,R1006,C1030 for DDR.

20171016_PM1800
1.Page11: Delete R1005,R1006,C1030 for DDR.
2.Page13: Add R1007,R1008,R1009,C1031 follow CRB design.
L_BIDDING_SIT_SCH_2017_1018_AM0800_PWR.DSN

20171018_AM0850-----Gerber SCH
1.Page48~62:Change DC SCH:
L_BIDDING_SIT_SCH_2017_1018_AM0800_PWR.DSN
2.Page22: Add C218 for PLT19 sequence.

20171019_AM0950-----BOM SCH
1.Page22: Change C218 to I,and change to 22nF.
2.Page1: Update PCB1 PN.
3.Update DC SCH:L_BIDDING_SIT_SCH_2017_1018_AM1533_PWR.DSN

20171023_AM0820-----BOM SCH
1.Page22: Change C218 to NI.
2.Page30: Change Q306 to NI for not auto power on after clear RTC.

SIT phase to SVT phase change List(EE Part)

20171107_AM0910
1.Page33: Change J11 from FOXCONN HBC1021-L1A4D-EH to PINREX 210-92-02GB02. Need apply CIS.已经link CIS 20171121
2.Page33: P154 change from FOXCONN_HC11051-P5 to PINREX_210-92-05GB02. Need apply CIS.已经link CIS 20171122
3.Page32: AJ2 change from DIP to SMD follow HMD request.
4.Page:30: SR266,SR267,SU2,SC209 change from PROTO to NI.
20171108_PM1910-----SVT 0.1 BOM SCH
1.Update DC SCH:
L_BIDDING_SIT_SCH_2017_1106_AM1830_PWR.DSN
2.Page1: Change PCB1 PN for SVT phase.
3.Page34: U19 change from DIP to SMD for SVT phase.
20171113_PM1650
1.Page33: Change P154 from I to PROTO.
2.Page33: SW1 change from DIP to SMD for HMD.
3.Page31: AC9,AC56 change from MURATA_GRM21BR71A475KA73L to MURATA_GRM21BR61A475KA73L.
4.DC SCH update:
L_BIDDING_SVT_SCH_2017_1113_AM1030_PWR.DSN
5.Change 0-Ohm to ShortPad:
AR5,AR18,LR1,LR21,LR22,SR3,SR5,SR18,SR259,SR261,SR262,SR270,R4,R10,R11,R153,R826,R24,R44,R92,R880,R1000,R1001,R105,
R106,R222,R247,R248,R149,R172,R173,R280,R282,R285,R286,R287,R302,R807,R906,R965,R993,R846,R848,R843,R1003,R954,R968,R969,
6.Page37: Remove L6.
20171115_PM1646
1.Page17: Change TPM from INFINEON_SLB9670VQ2.0FW7.61 to INFINEON_SLB9670VQ2.0FW7.62. ----Need link CIS

20171121_PM1635
1.Page44: D33 link CIS,update footprint.
2.Page32: AJ2 link CIS.
3.Page33: SW1 change from MLC-63GQRF to MLC-63GQR. Link CIS.
4.Page33: J11 Link CIS,update footprint.
5.Page34: U19 SPI Rom link CIS.

20171122_PM1420
1.Page17: U43 TPM link CIS.
2.Page33: P154 link CIS.update footprint.
3.Page1: PCB1 update CCL to Y.

20171123_AM0930
1.Page41/42:
Change 0-Ohm to ShortPad(0603):
R742,R764,R760,R768,R648,R649,R645,R652,
Remove:L30,L37,L67,L66 footprint

20171123_PM1505 1124_AM0920
1.Page9:
XDP P4 footprint change from HMS2X30CZ to HMS2X30CZ_MVB_NP.

20171124_AM0920
1.Page48~62:
Update DC SCH:L_BIDDING_SVT_SCH_2017_1124_AM0900_PWR.DSN
2.All Page: Change Sev to SVT.

20171128_AM0915 ---V0.2 BOM
1.Page48~62:
Update DC SCH:
DC SCH update
1.Page54:change PR926 to 62K
change PR942 to 48.7K
L_BIDDING_SVT_SCH_2017_1127_AM1447_PWR.DSN
2.Page1: Change Sev to SVT.

20171130_PM1658
1.Page32: AD59 change from NI to I. Follow EMC request. 2017/11/30 Vivian
2.Page48~62: Change TitleBlock Rev from SDV to SVT.

20171201_PM1218 ---Gerber
1.Page46: change C1006 net from +12V to +5V_S5 for Layout .

20171204_PM1550
1.Page48~62:
Update DC SCH:
L_BIDDING_SVT_SCH_2017_1204_PM0824.DSN

20171205_AM0830
1.Page9:Change R89 to PROTO.
2.Page45:Change R1002 to PROTO.

2017206_PM1536
1.Page27,44:F3,F5 change TE MICROSMD110F-2 to LITTELFUSE MICROSMD110F-2.

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