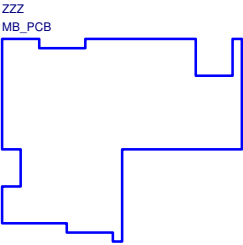


MODEL NAME : *APRFDV2000*
PCB NO : *LA-J321P*
BOM P/N : *451AK531L01/02/03/04/05/06/07/09/10/12/13/14/15/16/17/19*



Dell/Compal Confidential

Schematic Document

Augusta MLK Comet Lake U

BOM Structure

@ : Nopop Component
RF@ : RF Component
@RF@ : RF Nopop Component
EMC@ : EMI Component
@EMC@ : EMI Nopop Component
ST@ : ST TPM
@750@ : Nuvoton TPM
@NRTD3@ : non RTD3 support
RTD3@ : RTD3 support
XDP@ : XDP Component
DB@ : Debug Component
BreakDown@ : Breakdown Component
U22@ : CPU U22 identify for Power
U42@ : CPU U42 identify for Power
Auth_Dis_D4@ : Auth disabled for MEC5107
Auth_En_D4@ : Auth enabled for MEC5107
IR@ : IR component
@IR@ : IR Nopop component

VPro@ : support VPro
nVPro@ : support non VPro
NDS3@ : non Deep sleep Support
@DS3@ : Support Deep sleep
G3@ : EC G3 sharing mode
@MAF@ : Master Attached Flash sharing mode
TPS79801QDGNR@ : Camera sensor AVDD 2nd LDO
TPS7A1601DGNR@ : Camera sensor AVDD Main LDO
TPS79801QDGNR_IR@ : IR Camera sensor AVDD 2nd LDO
TPS7A1601DGNR_IR@ : IR Camera sensor AVDD Main LDO
@TGSSD@ : support Intel Teton Glacier SSD
WINBOND@ : BIOS ROM Option
XMC@ : BIOS ROM Option GD@ : BIOS ROM Option

2019-10-17

Rev: 0.2 (X01)
DVT1

U62U22EC@ : CPU U62 U22 identify for EC
U42EC@ : CPU U42 identify for EC
I7EC@ : CPU I7 identify for EC
I5I3EC@ : CPU I5I3 identify for EC
U62U22PCH@ : CPU U62U22 identify for BIOS
U42PCH@ : CPU U42 identify for BIOS
I7PCH@ : CPU I7 identify for PCH
I5I3PCH@ : CPU I5I3 identify for PCH

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				Date	Thursday, October 17, 2019
				Sheet	1 of 100
				Rev	0.2

Board ID Table

Vcc	3.3V +/- 5%	C	REV	
Board ID	0	240K +/- 5%	4700p	EVTT1
1	130K +/- 5%	4700p		DVT1
2	62K +/- 5%	4700p		DVT2
3	33K +/- 5%	4700p		
4	8.2K +/- 5%	4700p		
5	4.3K +/- 5%	4700p		PVT
6	2K +/- 5%	4700p		
7	NC			

Board ID Option									
RES	RES	RES	RES	RES	RES	RES	RES	RES	RES
0	130K	4700p	4700p	4700p	4700p	4700p	4700p	4700p	4700p
1	130K	4700p	4700p	4700p	4700p	4700p	4700p	4700p	4700p
2	130K	4700p	4700p	4700p	4700p	4700p	4700p	4700p	4700p
3	130K	4700p	4700p	4700p	4700p	4700p	4700p	4700p	4700p
4	130K	4700p	4700p	4700p	4700p	4700p	4700p	4700p	4700p
5	130K	4700p	4700p	4700p	4700p	4700p	4700p	4700p	4700p
6	130K	4700p	4700p	4700p	4700p	4700p	4700p	4700p	4700p
7	130K	4700p	4700p	4700p	4700p	4700p	4700p	4700p	4700p

USB 2.0

USB 2.0 PORT#	DESTINATION
1	TBT1
2	TBT2
3	USB Type-A
4	Dock
5	IR Camera
6	UF Camera
7	WWAN
8	USH
9	FPR
10	BT

Displayport

DDI	DDI PORT#	DESTINATION
	1	TBT Titan Ridge
eDP	1	FHD

Board ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	1.0
6	
7	

Symbol Note :

@ : means de-pop

⏏ : means Digital Ground

⏏ : means Analog Ground

USB 3.0

Flexible I/O	Interface	DESTINATION
1	PCI-E#1 / USB 3.0#1	
2	PCI-E#2 / USB 3.0#2	WF Camera
3	PCI-E#3 / USB 3.0#3	USB3.0 Type-A
4	PCI-E#4 / USB 3.0#4	NGFF (WWAN)
5	PCI-E#5 / USB 3.0#5	
6	PCI-E#6 / USB 3.0#6	TBT Titan Ridge
7	PCI-E #7	
8	PCI-E #8	
9	PCI-E #9	Card reader
10	PCI-E #10	WLAN PCIe Gen2
11	PCI-E #11 / SATA #0	
12	PCI-E #12 / SATA #1A	WWAN
13	PCI-E #13	
14	PCI-E #14	
15	PCI-E #15 / SATA #1B	Main SSD (2230)
16	PCI-E #16 / SATA #2	

CLK

CLK	DIFFERENTIAL	DESTINATION
	CLKOUT_PCIE0	TBT TR
	CLKOUT_PCIE1	Main SSD
	CLKOUT_PCIE2	WWAN
	CLKOUT_PCIE3	WLAN PCIe Gen2
	CLKOUT_PCIE4	Card Reader
	CLKOUT_PCIE5	N/A

SMBUS / I2C Control Table

	SOURCE	EC MECS107	Touch Screen	BASE	Gyro+ACC E-Compass	SAR sensor	USH	PD1	PS8811 Re-driver	Battery Charger	ALS	IMVP	WWAN
SMB01_DATA	SMB01-SMB01A	PCB_SMBus	V										
I2C0_SDA	I2C0_SCL	PCB_I2C		V									
ISH_I2C2_SDA	ISH_I2C2_SCL	PCB_ISH											V
ISH_I2C0_SDA	ISH_I2C0_SCL	PCB_ISH			V								
ISH_I2C1_SDA	ISH_I2C1_SCL	PCB_ISH									V		
SMB00_DATA	SMB00_CLK	EC_SMBus											
SMB01_DATA	SMB01_CLK	EC_SMBus				V	V						
SMB02_DATA	SMB02_CLK	EC_SMBus		V									
SMB04_DATA	SMB04_CLK	EC_SMBus					V						
SMB05_DATA	SMB05_CLK	EC_SMBus					V					V	
SMB10_DATA	SMB10_CLK	EC_SMBus							V				

Voltage Rails

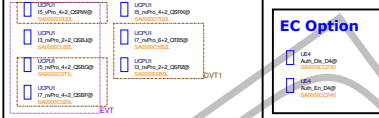
Power Plane	Description	S0	Soix	S4/S5
+VBUS1/2_PD_20V	Adapter power supply	N/A	N/A	N/A
+BATT	Battery power supply	N/A	N/A	N/A
B%	AC or battery power rail for System	N/A	N/A	N/A
+RTCVCC	RTC power	ON	ON	ON
+5VD	+5VD power	ON	ON	ON*
+5VALW	System +5V always on power rail	ON	ON	ON*
+3VALW	System +3V always on power rail	ON	ON	ON*
+3V_PCH	+3VALW power for PCH rails	ON	ON	ON*
+1.0V_PCHM_CORE	System +1.0V always on power rail	ON	ON	ON*
+1.8VDD	LPDDR3 +1.8V power rail	ON	ON	ON*
+0.6VS	DDR +0.6VS power rail for DDR terminator	ON	ON	ON*
+1.2V_DDR	LPDDR3 +1.2V power rail	ON	ON	ON*
+1.8VA	System +1.8V always on power rail	ON	ON	OFF
+1.0V_VCCST	+1.05 VCCST power rail	ON	OFF	OFF
+1.0V_VCCSTG	+1.05 VCCSTG power rail	ON	OFF	OFF
+1.0VS_VCCIO	+1.05 VCCIO power rail	ON	OFF	OFF
+VCC_CORE	Core voltage for CPU	ON	OFF	OFF
+VCC_GT	Silicon graphics power rail	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+5VS	System +5VS power rail	ON	OFF	OFF
+3VS	System +3VS power rail	ON	OFF	OFF
+1.8VS	System +1.8VS power rail	ON	OFF	OFF
+1.2V_USB	System +1.2V USB redriver power rail	ON	OFF	OFF
		ON	OFF	OFF
		ON	OFF	OFF
		ON	OFF	OFF

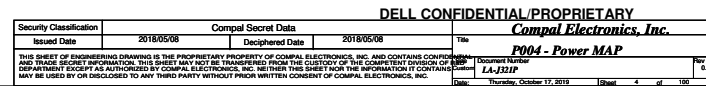
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF

POWER STATES

State	Signal	SLP S3#	SLP S4#	SLP S5#	SLP A#	ALWAYS PLANE	M PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON	ON
Soix/Moff		LOW	HIGH	HIGH	HIGH	ON	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3		LOW	LOW	LOW	HIGH	ON	ON	OFF	OFF	OFF
Soix (Suspend to RAM) / M-OFF		LOW	HIGH	HIGH	LOW	ON	OFF	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF		LOW	LOW	HIGH	LOW	ON	OFF	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF	OFF

EC Option





[AC in] (remove RTC)

[Battery only, AC absent] (remove RTC)

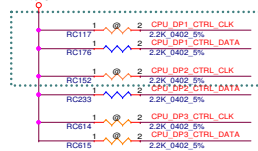




All VREF traces should have 10 mil trace width

COMPENSATION PU FOR eDP
CAD Note:
Trace width=5 mils
Isolation Spacing=25mil,
Max length=100 mils.

8/29 Modify by Kettle
Follow Riverside, CPU_DP1/DP2_CTRL_CLK PU change to decomp
+3VS

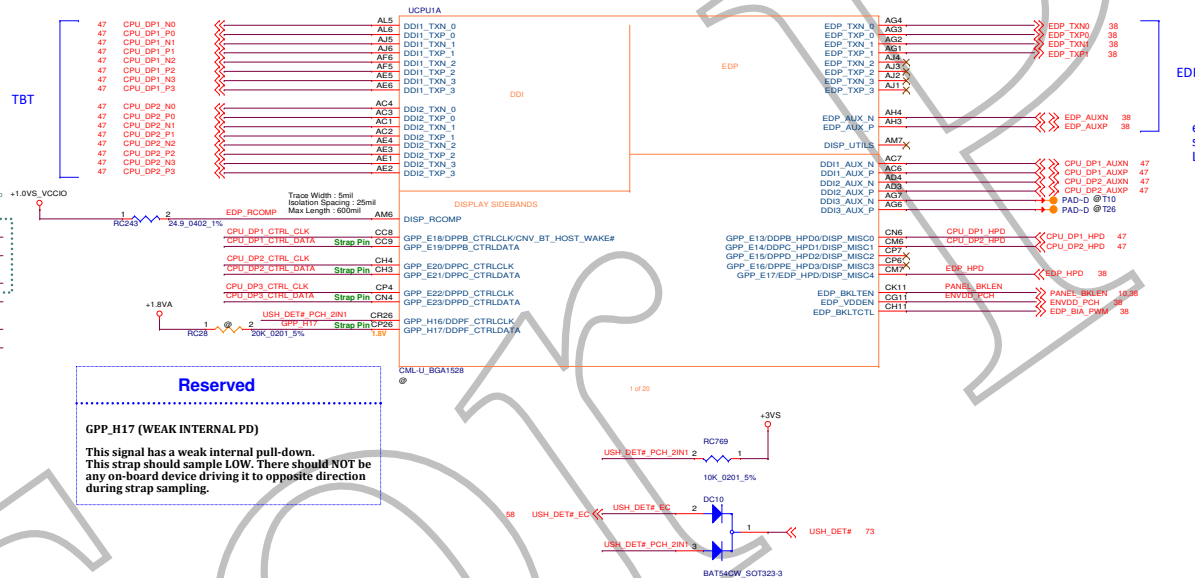


0 = DisplayPort not detected. (Default)
1 = DisplayPort is detected.

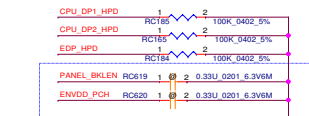
Reserved

GPP_H17 (WEAK INTERNAL PD)

This signal has a weak internal pull-down.
This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.

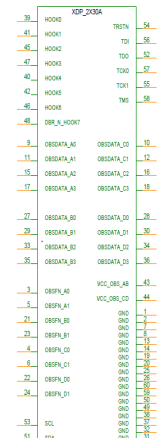
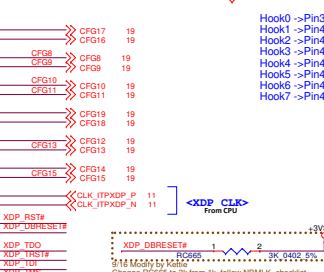
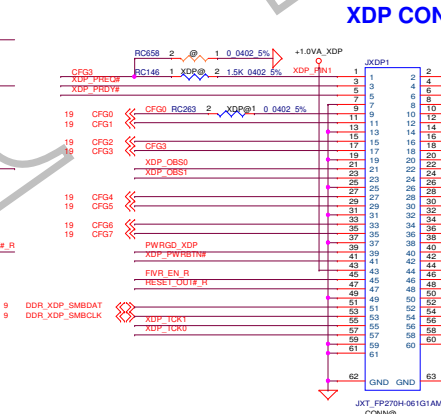
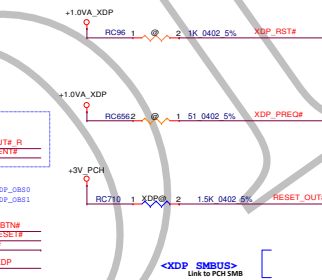
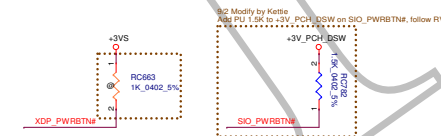
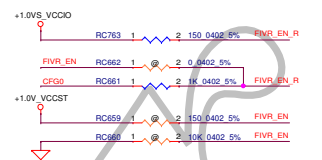
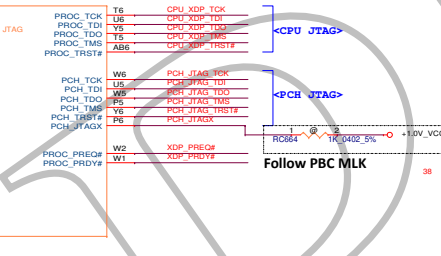
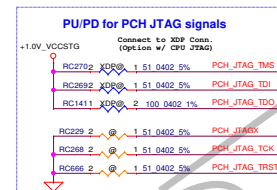


embedded DisplayPort Utility. Output control signal used for brightness correction of embedded LCD displays with backlight modulation.

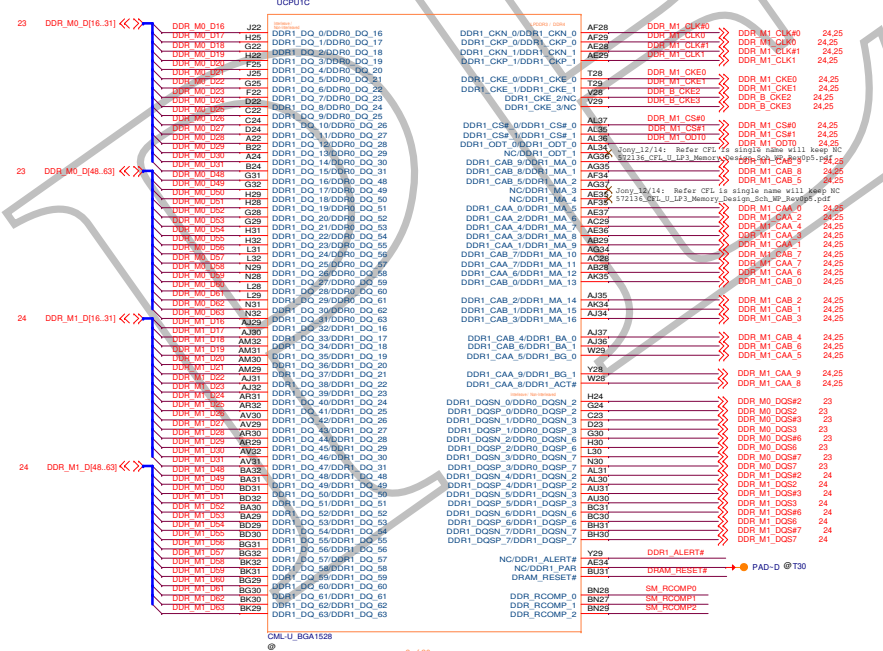
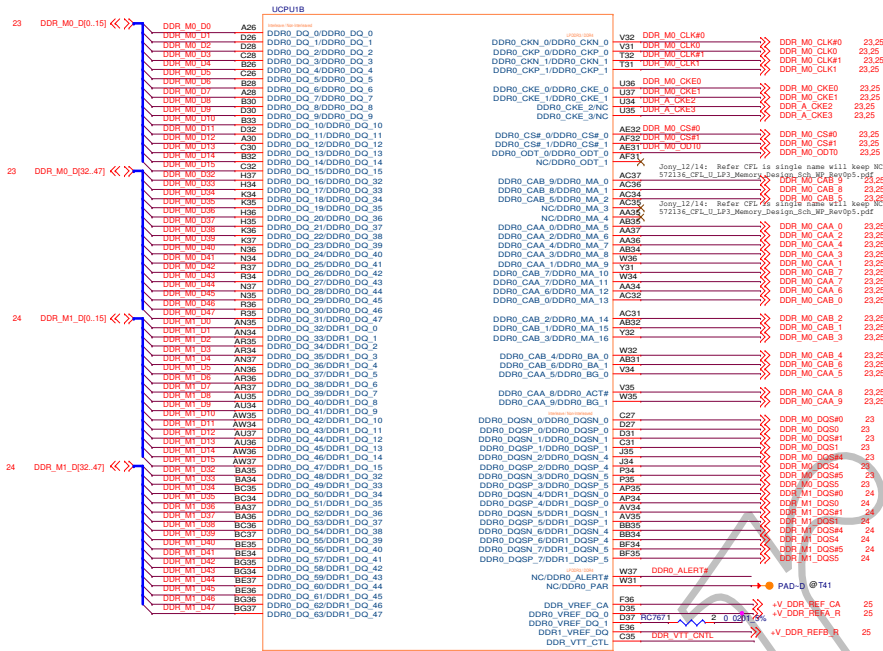


PCH GLITCH ISSUE MITIGATION(PDG p.130)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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				Date	Thursday, October 17, 2019
				Sheet	6 of 100
				Rev	0.2



LPDDR3, Ballout for side by side(Non-Interleave)



3.1 RCOMP

The RCOMP needed for the various I/Os are summarized in the tables below.

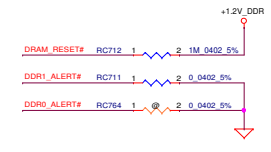
Table 8. RCOMP Recommendation for CML

Interface	Pin Name	Board Rterm (Ohm)	Board Rdc (Ohm)	Note
DDR - LP4	DDR_RCOMP[0]	121.0 ±1% on pkg to VSS	N/A	
	DDR_RCOMP[1]	80.6 Ω ±1% on pkg to VSS	N/A	
	DDR_RCOMP[2]	125.0 ±1% on pkg to VSS	N/A	
DDR - LP3	DDR_RCOMP[0]	300.0 ±1% on pkg to VSS	N/A	
	DDR_RCOMP[1]	80.6 Ω ±1% on pkg to VSS	N/A	
	DDR_RCOMP[2]	163.0 ±1% on pkg to VSS	N/A	
DDR - DR4 SODIMM	DDR_RCOMP[0]	121.0 ±1% on pkg to VSS	N/A	
	DDR_RCOMP[1]	80.6 Ω ±1% on pkg to VSS	N/A	
	DDR_RCOMP[2]	100.0 ±1% on pkg to VSS	N/A	

LPDDR3 COMPENSATION SIGNALS

SM_RCOMP0 RC2241 2 200.0402 1%
SM_RCOMP1 RC2481 2 80.6.0402 1%
SM_RCOMP2 RC2581 2 162.0402 1%

CAD Note:
Trace width=15 mils, Spacing=25 mils(Within Group 20mils)
Max trace length= 500 mils



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Date:	Thursday, October 17, 2019	Sheet	8	of	100	

BOOT HALT

SPI0_MOSI(WEAK INTERNAL PU)

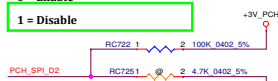
0 = Enable
1 = Disable



CONSENT STRAP

SPI0_I02(WEAK INTERNAL PU)

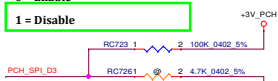
0 = Enable
1 = Disable



A0 PERSONALITY STRAP

SPI0_I03(WEAK INTERNAL PU)

0 = Enable
1 = Disable



TLS CONFIDENTIALITY

GPP_C2/SMBALERT#(INTERNAL PD 20K)

0 = TLS CONFIDENTIALITY DISABLE
1 = TLS CONFIDENTIALITY ENABLE



eSPI OR LPC

GPP_C5 / SML0ALERT#(WEAK INTERNAL PD)

0 = LPC is selected (for EC, Default)
1 = eSPI is selected (for EC)



Intel DCI-OOB

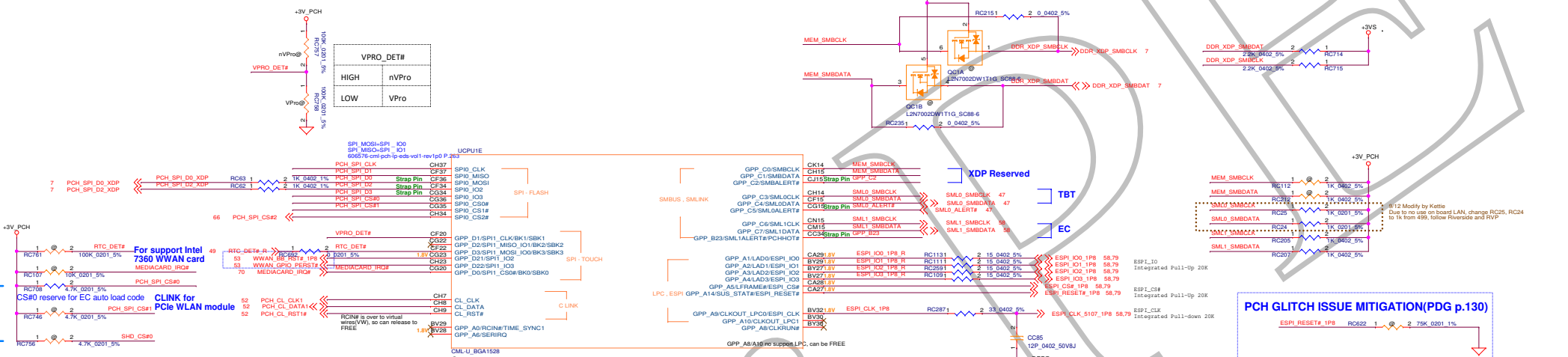
GPP_B23(Internal 20 K internal Pull Down)

0 = Disable IntelR DCI-OOB (Default)
1 = Enable IntelR DCI-OOB



606576-cml-pch-lp-eds-vol1-rev1p0
External pull-up is required. Recommend 100kohm if pulled up to 3.3V or 75kohm if pulled up to 1.8V.
This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

Intel Mee Crypto (TLS) Transport Layer Security to support Intel Active Management (AMT) with TLS.



PCH GLITCH ISSUE MITIGATION(PDG p.130)

9/12 Modify by Kettle
9/16 Modify by Kettle
Need to distinguish 5107 ES/MP, add BIOS ROM option

BIOS ROM Option

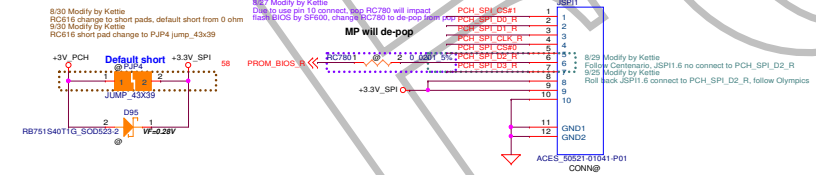
UC9 WINBOND® W25Q256JVEIQ_WSON8_8X6	MEC5107	EC chip	EC code	BIOS ROM source	BIOS file name
UC9 GD® S4000B60A00 GD25Q256VYIQ WSON 8P	ES	5107	RTOS	WINBOND, XMC	
UC9 XMC® S4000CW300 XM25Q256BXKXOTF WSON 8P	MP	5107	RTOS	GD	

9/10 Modify by Kettle
Add BIOS ROM option, GD for 2nd source, XMC for 3rd source

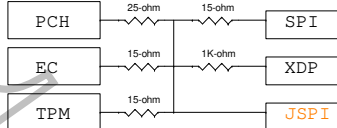
SPI ROM (32 MByte)
ROM is Quad SPI

Follow Pebble Creek MLK
SPI (BIOS)
JSPI DEBUG Conn.

D2 do not connect to JSPI1 or RC780 depop

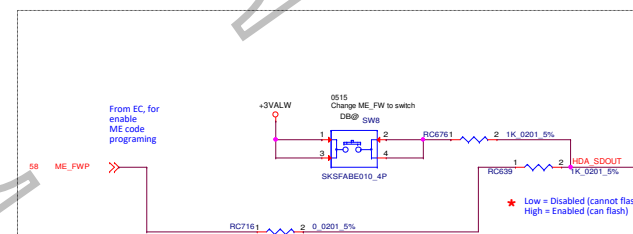
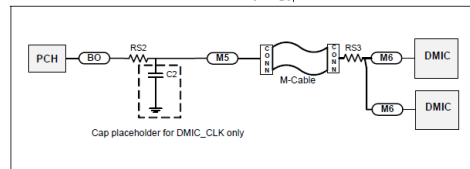
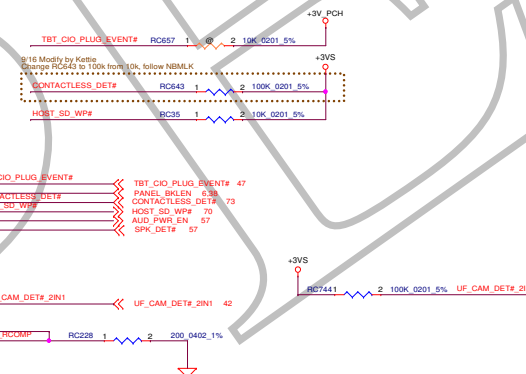
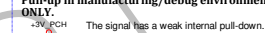
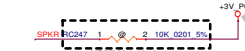
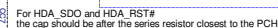
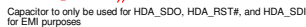
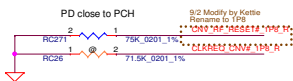


MEC5107 G3 Sharing Topology



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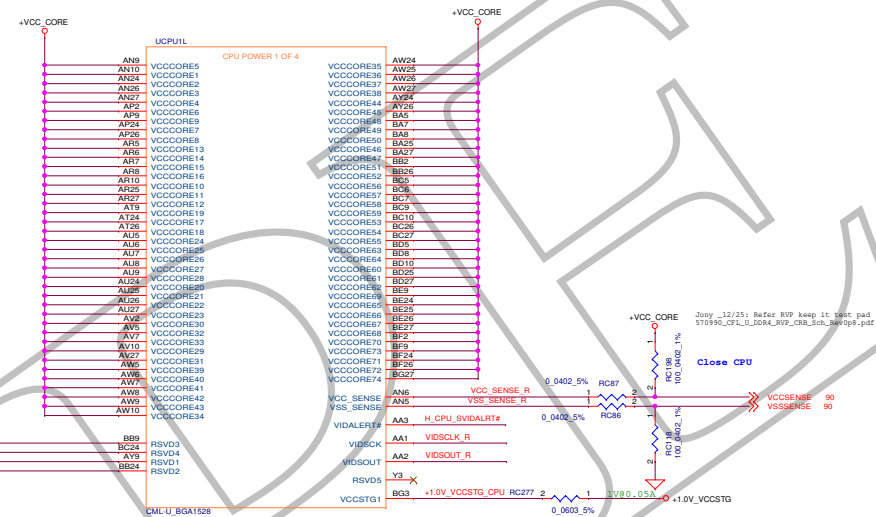
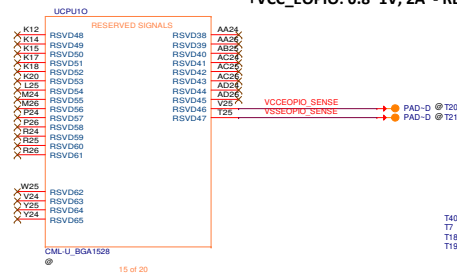
Pin Number	CFL U43e	WHL U42 QS/Production	CNL U22/WHL U42 ES0/1
AH26	ZV#	RSVD	RSVD
T25	VSS_EOPIO_SENSE	RSVD	RSVD
V25	VCC_EOPIO_SENSE	RSVD	RSVD
AA24	VCC_EOPIO	RSVD	RSVD
AA26	VCC_EOPIO	RSVD	RSVD
AB25	VCC_EOPIO	RSVD	RSVD
AC24	VCC_EOPIO	RSVD	RSVD
AC25	VCC_EOPIO	RSVD	RSVD
AC26	VCC_EOPIO	RSVD	RSVD
AD24	VCC_EOPIO	RSVD	RSVD
AD26	VCC_EOPIO	RSVD	RSVD
K12	VCCOPC	RSVD	RSVD
K14	VCCOPC	RSVD	RSVD
K15	VCCOPC	RSVD	RSVD
K17	VCCOPC	RSVD	RSVD
K18	VCCOPC	RSVD	RSVD
K20	VCCOPC	RSVD	RSVD
L25	VCCOPC	RSVD	RSVD
M24	VCCOPC	RSVD	RSVD
M26	VCCOPC	RSVD	RSVD
P24	VCCOPC	RSVD	RSVD
P26	VCCOPC	RSVD	RSVD
R24	VCCOPC	RSVD	RSVD
R25	VCCOPC	RSVD	RSVD
R26	VCCOPC	RSVD	RSVD
T24	VCCOPC	RSVD	RSVD
T25	VCCOPC	RSVD	RSVD
T26	VCCOPC	RSVD	RSVD
V24	VCC_OPC_1P8	RSVD	RSVD
V25	VCC_OPC_1P8	RSVD	RSVD
W25	VCC_OPC_1P8	RSVD	RSVD
AJ27	MSM#	RSVD	RSVD
G4	VSS	RSVD	RSVD
G3	VSS	RSVD	RSVD
C34	VSS	RSVD	RSVD

PSC(Primary side cap) : Place as close to the package as possible
BSC(Backside cap) : Place on secondary side, underneath the package

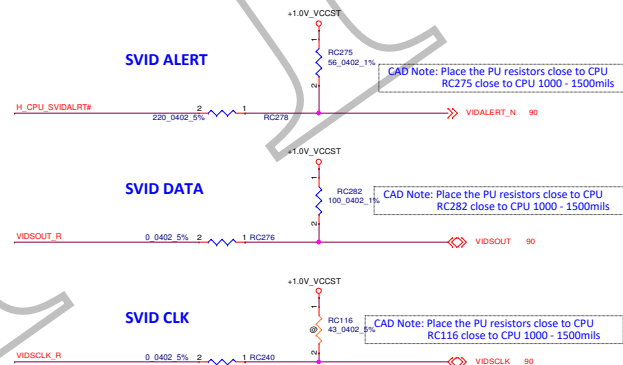
Component placement order:
Package edge > 0402 caps > 0805 caps > Bulk caps > Power source

+VCC_CORE: 0.55~1.5V, 29A
+VCC_EDRAM: 1V, 2.5A

+V1.8S_EDRAM: 1.8V, 50mA - REMOVE
+VCC_EOPIO: 0.8~1V, 2A - REMOVE

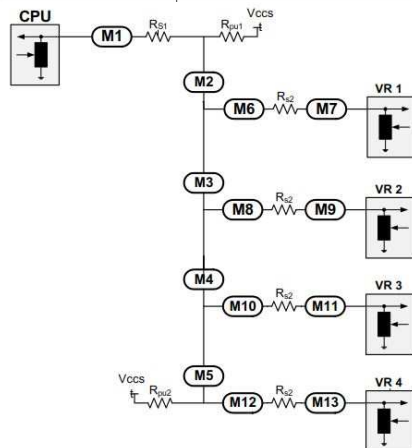


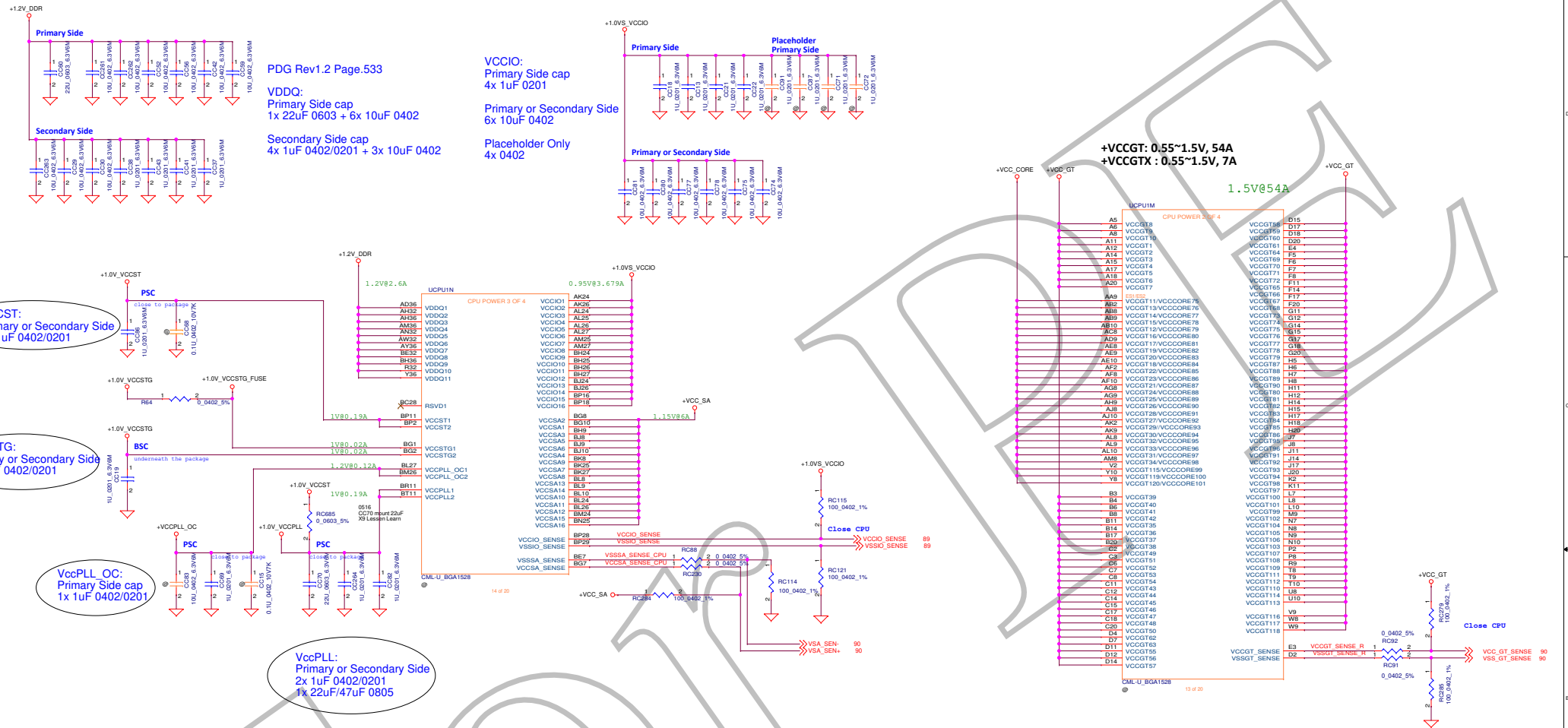
VCCOPC,VCCOPC_1P8,VCC_EOPIO for SKYLAKE-U 2+3e
(w/ on package cache)



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VIDSOUT platform resistors	Rpu1=100Ω, Rpu2=100Ω, Rs1=0Ω, Rs2=10Ω
VIDSCK platform resistors	Rpu1=Empty, Rpu2=45Ω, Rs1=0Ω, Rs2=49.9Ω
VIDSALERT# platform resistors	Rpu1=56Ω, Rpu2=Empty, Rs1=220Ω, Rs2=0Ω





Note1: VCCPRIM_CORE Implementation with PCH CORE_VID Recommendation

UCPU1R		
CR34	VSS, 1	BL7
BT5	VSS, 2	AE25
CP35	VSS, 3	BM33
CM37	VSS, 4	CM5
CM37	VSS, 5	AE27
CM37	VSS, 6	CM9
CM1	VSS, 7	AE30
BM6	VSS, 8	BM36
AV4	VSS, 9	CM13
BM4	VSS, 10	AE7
E36	VSS, 11	BM9
AE24	VSS, 12	CM17
AE26	VSS, 13	AE27
AE26	VSS, 14	BM36
AE26	VSS, 15	CM17
AG24	VSS, 16	AE27
AG26	VSS, 17	BM36
AG24	VSS, 18	CM17
AG26	VSS, 19	AE27
AG24	VSS, 20	BM36
AG26	VSS, 21	CM17
AG24	VSS, 22	AE27
AG26	VSS, 23	BM36
AG24	VSS, 24	CM17
AG26	VSS, 25	AE27
AG24	VSS, 26	BM36
AG26	VSS, 27	CM17
AG24	VSS, 28	AE27
AG26	VSS, 29	BM36
AG24	VSS, 30	CM17
AG26	VSS, 31	AE27
AG24	VSS, 32	BM36
AG26	VSS, 33	CM17
AG24	VSS, 34	AE27
AG26	VSS, 35	BM36
AG24	VSS, 36	CM17
AG26	VSS, 37	AE27
AG24	VSS, 38	BM36
AG26	VSS, 39	CM17
AG24	VSS, 40	AE27
AG26	VSS, 41	BM36
AG24	VSS, 42	CM17
AG26	VSS, 43	AE27
AG24	VSS, 44	BM36
AG26	VSS, 45	CM17
AG24	VSS, 46	AE27
AG26	VSS, 47	BM36
AG24	VSS, 48	CM17
AG26	VSS, 49	AE27
AG24	VSS, 50	BM36
AG26	VSS, 51	CM17
AG24	VSS, 52	AE27
AG26	VSS, 53	BM36
AG24	VSS, 54	CM17
AG26	VSS, 55	AE27
AG24	VSS, 56	BM36
AG26	VSS, 57	CM17
AG24	VSS, 58	AE27
AG26	VSS, 59	BM36
AG24	VSS, 60	CM17
AG26	VSS, 61	AE27
AG24	VSS, 62	BM36
AG26	VSS, 63	CM17
AG24	VSS, 64	AE27
AG26	VSS, 65	BM36
AG24	VSS, 66	CM17
AG26	VSS, 67	AE27
AG24	VSS, 68	BM36
AG26	VSS, 69	CM17
AG24	VSS, 70	AE27
AG26	VSS, 71	BM36
AG24	VSS, 72	CM17

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UCPU1S		
BT35	VSS, 145	BY25
DE	VSS, 146	J18
BT35	VSS, 147	BY25
BT35	VSS, 148	BY25
BT35	VSS, 149	BY25
BT35	VSS, 150	BY25
BT35	VSS, 151	BY25
BT35	VSS, 152	BY25
BT35	VSS, 153	BY25
BT35	VSS, 154	BY25
BT35	VSS, 155	BY25
BT35	VSS, 156	BY25
BT35	VSS, 157	BY25
BT35	VSS, 158	BY25
BT35	VSS, 159	BY25
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BT35	VSS, 162	BY25
BT35	VSS, 163	BY25
BT35	VSS, 164	BY25
BT35	VSS, 165	BY25
BT35	VSS, 166	BY25
BT35	VSS, 167	BY25
BT35	VSS, 168	BY25
BT35	VSS, 169	BY25
BT35	VSS, 170	BY25
BT35	VSS, 171	BY25
BT35	VSS, 172	BY25
BT35	VSS, 173	BY25
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BT35	VSS, 210	BY25
BT35	VSS, 211	BY25
BT35	VSS, 212	BY25
BT35	VSS, 213	BY25
BT35	VSS, 214	BY25
BT35	VSS, 215	BY25
BT35	VSS, 216	BY25

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UCPU1T		
NE	VSS, 290	CF23
BT3	VSS, 291	V4
BT3	VSS, 292	BE30
BT3	VSS, 293	VSS, 364
BT3	VSS, 294	CF23
BT3	VSS, 295	W10
BT3	VSS, 296	BE31
BT3	VSS, 297	VSS, 367
BT3	VSS, 298	VSS, 368
BT3	VSS, 299	VSS, 369
BT3	VSS, 300	VSS, 370
BT3	VSS, 301	VSS, 371
BT3	VSS, 302	VSS, 372
BT3	VSS, 303	VSS, 373
BT3	VSS, 304	VSS, 374
BT3	VSS, 305	VSS, 375
BT3	VSS, 306	VSS, 376
BT3	VSS, 307	VSS, 377
BT3	VSS, 308	VSS, 378
BT3	VSS, 309	VSS, 379
BT3	VSS, 310	VSS, 380
BT3	VSS, 311	VSS, 381
BT3	VSS, 312	VSS, 382
BT3	VSS, 313	VSS, 383
BT3	VSS, 314	VSS, 384
BT3	VSS, 315	VSS, 385
BT3	VSS, 316	VSS, 386
BT3	VSS, 317	VSS, 387
BT3	VSS, 318	VSS, 388
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BT3	VSS, 350	VSS, 420
BT3	VSS, 351	VSS, 421
BT3	VSS, 352	VSS, 422
BT3	VSS, 353	VSS, 423
BT3	VSS, 354	VSS, 424
BT3	VSS, 355	VSS, 425
BT3	VSS, 356	VSS, 426
BT3	VSS, 357	VSS, 427
BT3	VSS, 358	VSS, 428
BT3	VSS, 359	VSS, 429
BT3	VSS, 360	VSS, 430
BT3	VSS, 361	VSS, 431
BT3	VSS, 362	VSS, 432
BT3	VSS, 363	VSS, 433

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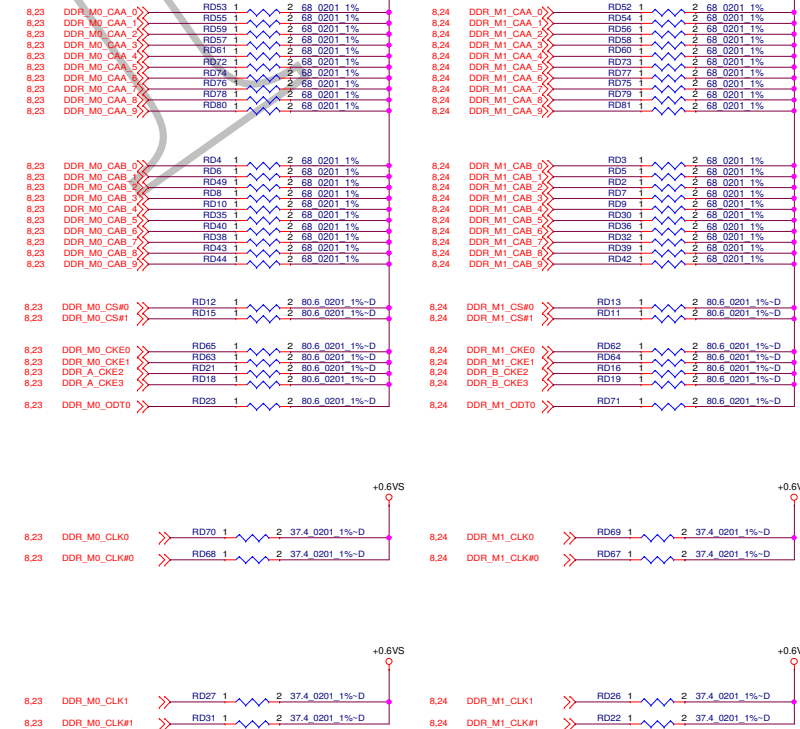
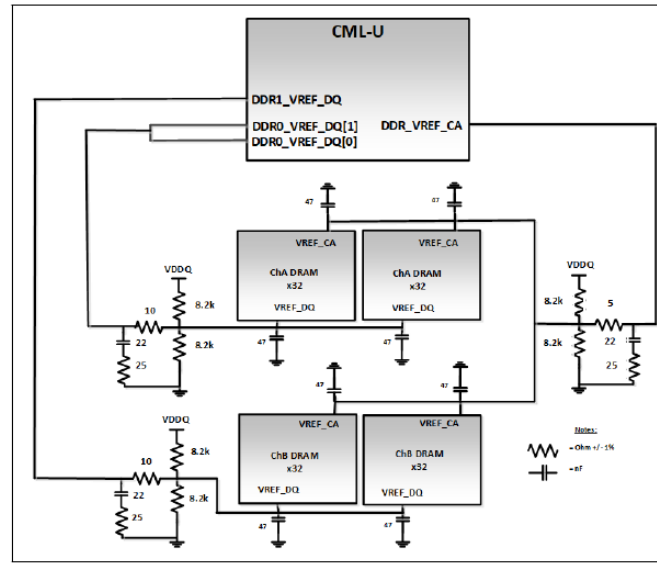
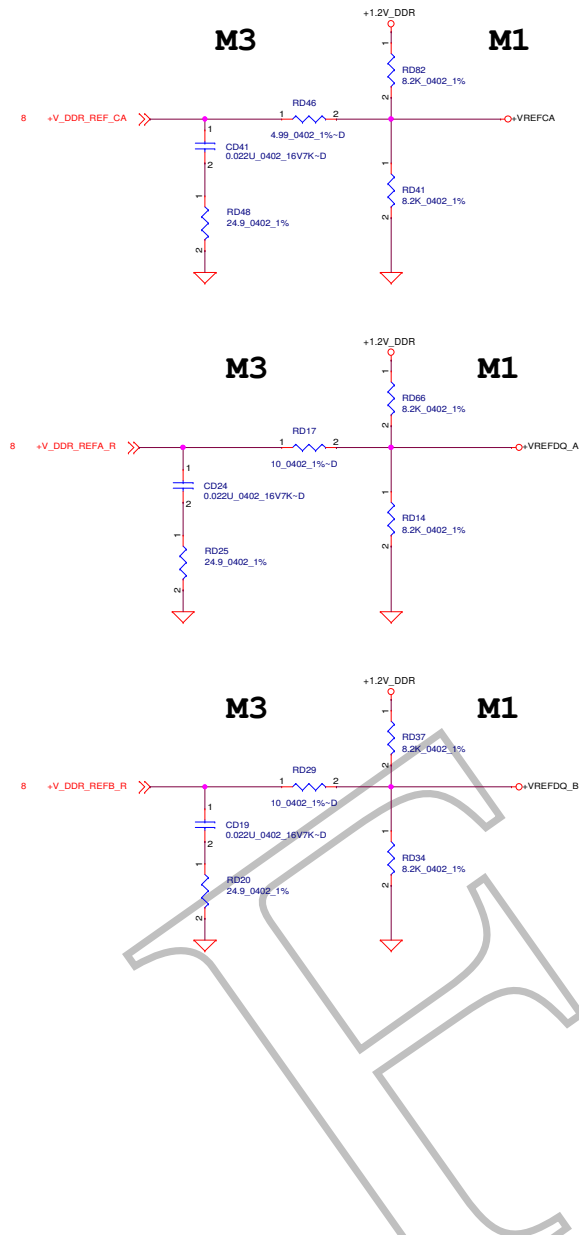
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VREF traces should be at least 20 mils wide with 20 mils spacing to other signals/planes.

Figure 60. LPDDR3 x32 Memory Down VREF-DQ and VREF-CA Overview



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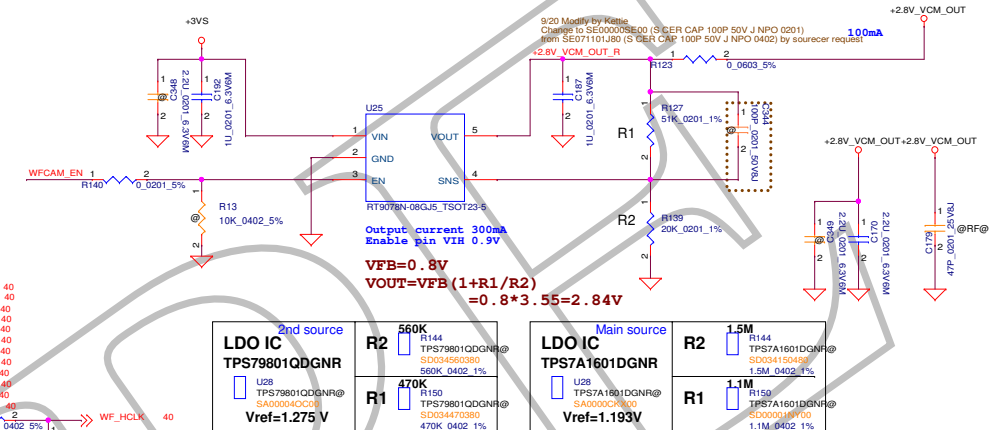
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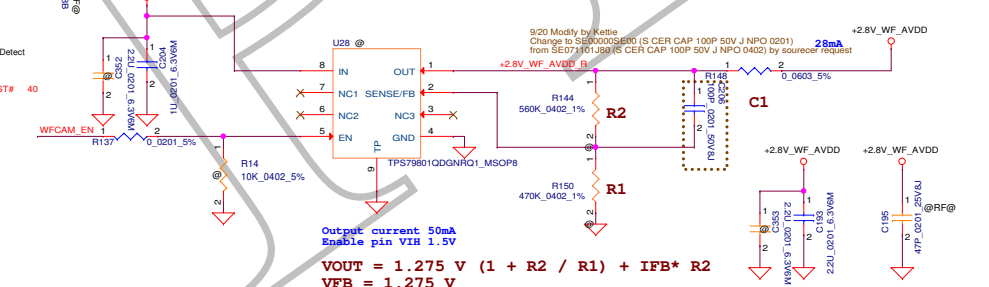
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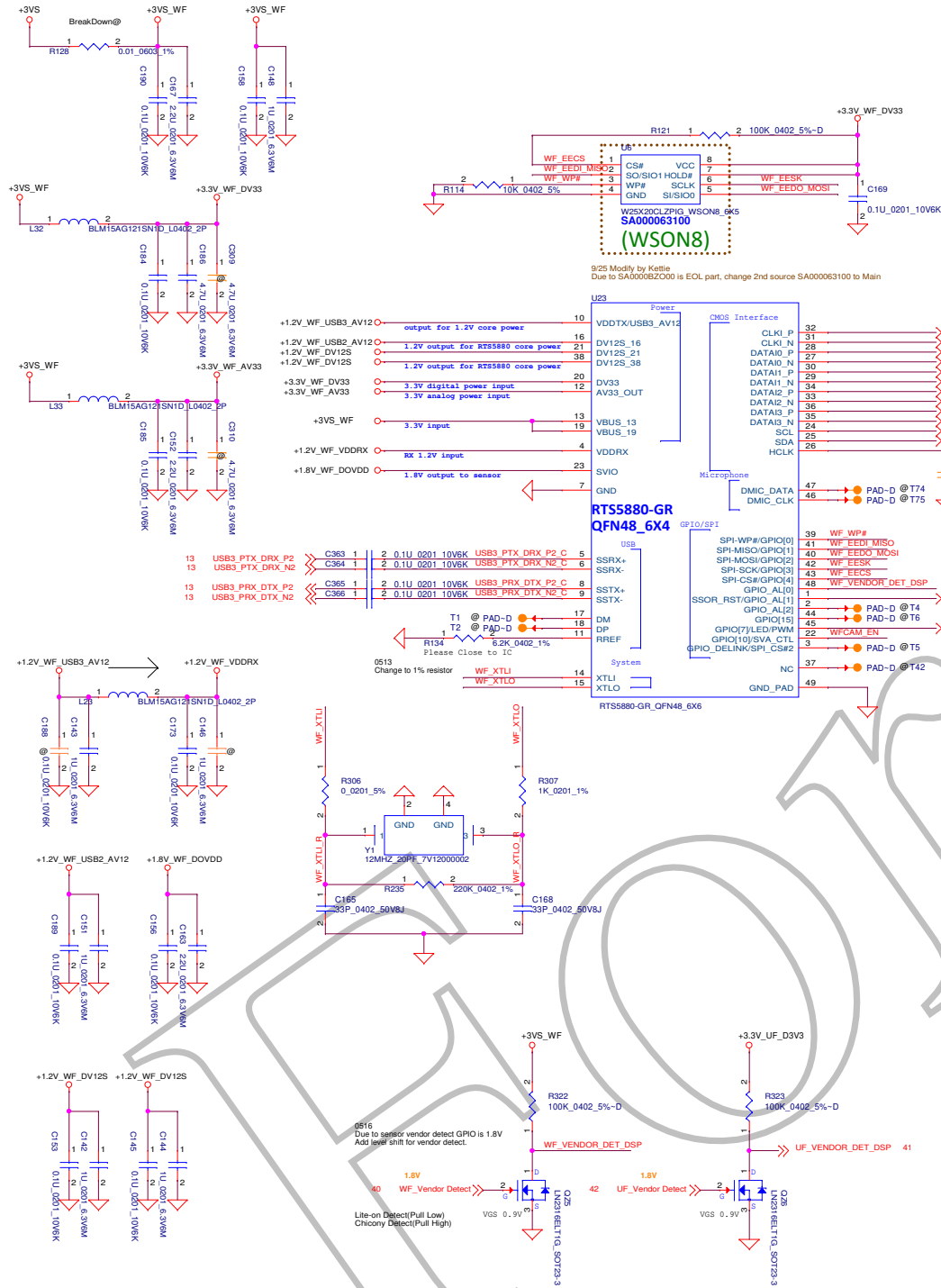
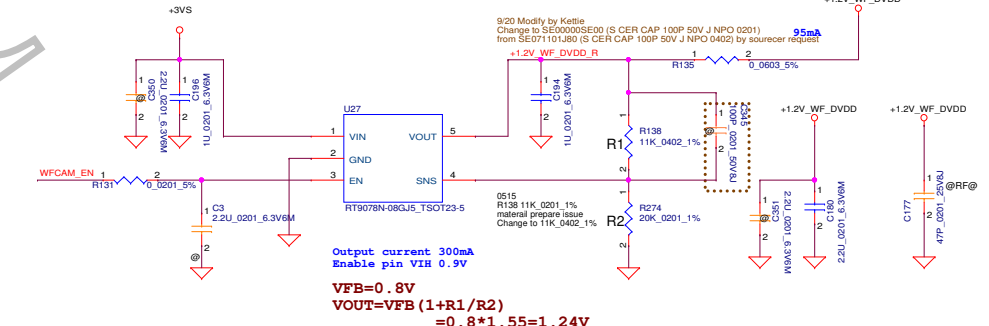
(+2.8V_VCM_OUT) For Rear Camera VCM

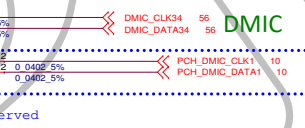
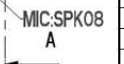
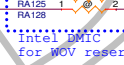
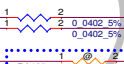
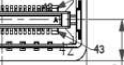
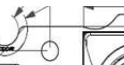
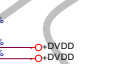
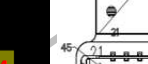
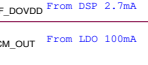
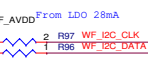
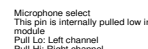
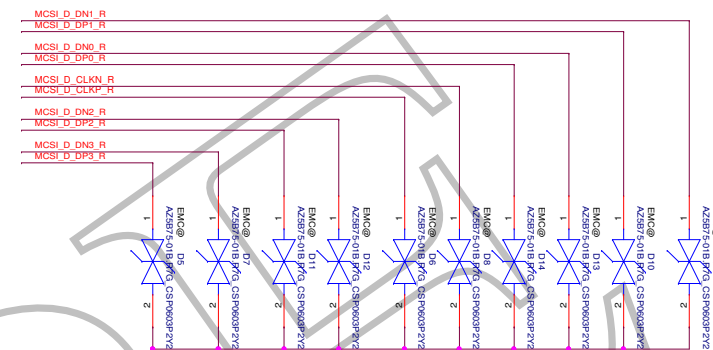
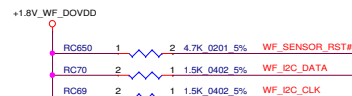
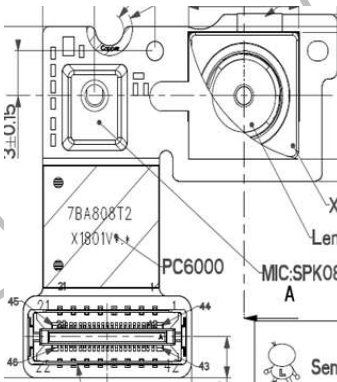
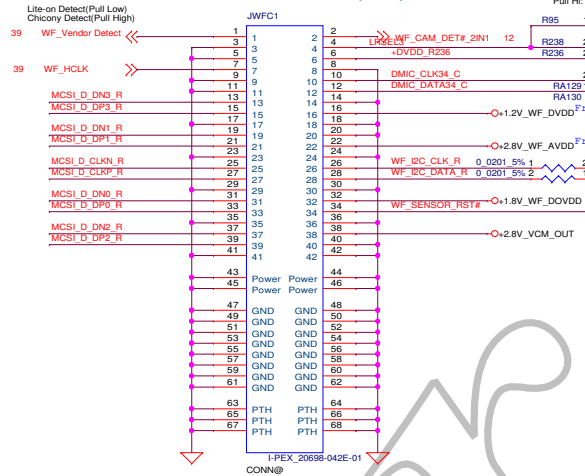
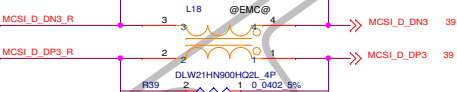
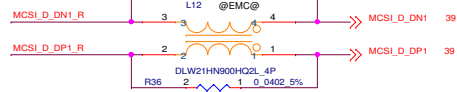


(+2.8V_WF_AVDD) For Rear Camera

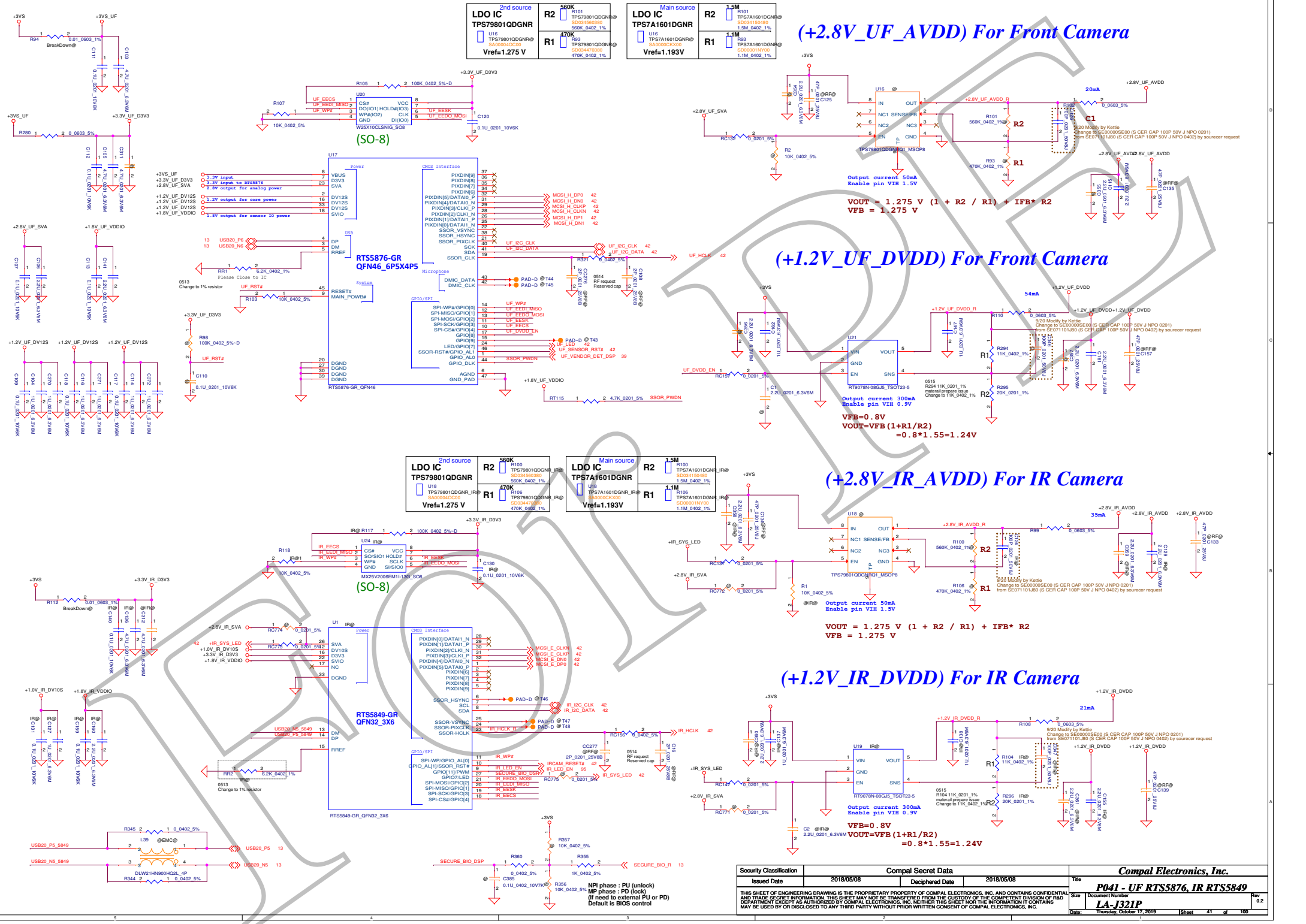


(+1.2V_WF_DVDD) For Rear Camera

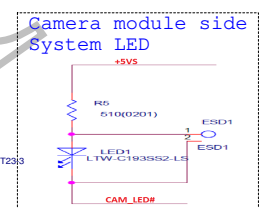
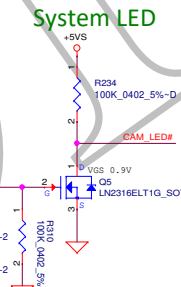
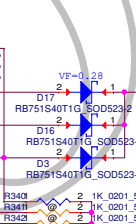
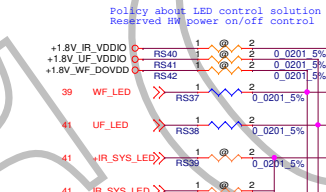
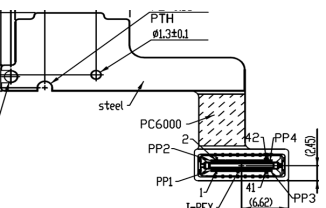
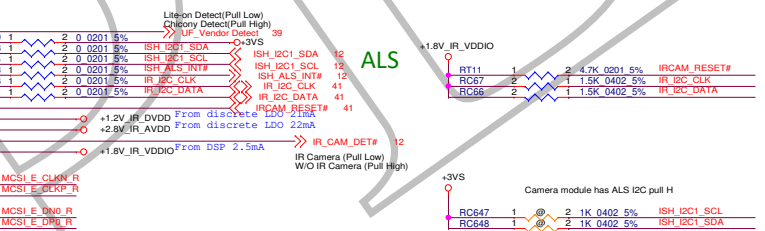
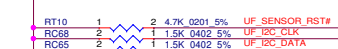
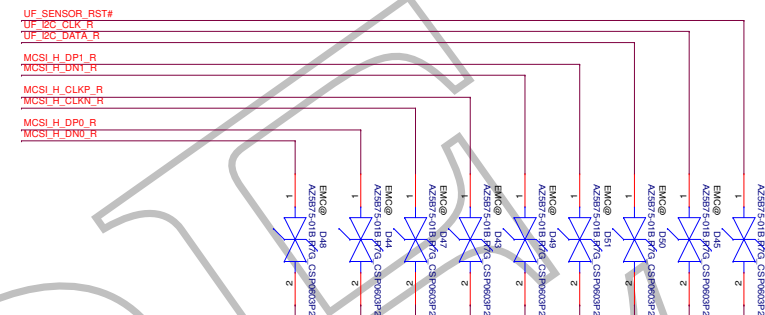
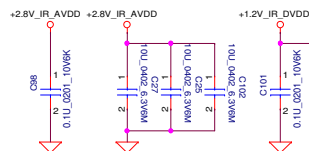




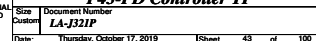
Module CONN Pin NO	M/B CON Pin define	Pin define	Module CONN Pin NO	M/B CON Pin define	Pin define
21	1	Lite-on det (Pull Low) Chicony det(Pull High)	22	2	DGND
20	3	DGND	23	4	MIC_select
19	5	DGND	24	6	MIC_3V3
18	7	MCLK	25	8	MIC_GND
17	9	DGND	26	10	MIC_CLK
16	11	DGND	27	12	MIC_DATA
15	13	DATA3_N	28	14	DGND
14	15	DATA3_P	29	16	DVDD
13	17	DGND	30	18	DGND
12	19	DATA1_N	31	20	AGND
11	21	DATA1_P	32	22	AVDD
10	23	DGND	33	24	DGND
9	25	CLK_N	34	26	SCL
8	27	CLK_P	35	28	SDA
7	29	DGND	36	30	DGND
6	31	DATA0_N	37	32	DOVDD
5	33	DATA0_P	38	34	PWDN
4	35	DGND	39	36	DGND
3	37	DATA2_N	40	38	VCM_VDD28
2	39	DATA2_P	41	40	VCM_GND
1	41	DGND	42	42	DGND
43	46	DGND	44	45	DGND
45	43	DGND	46	44	DGND

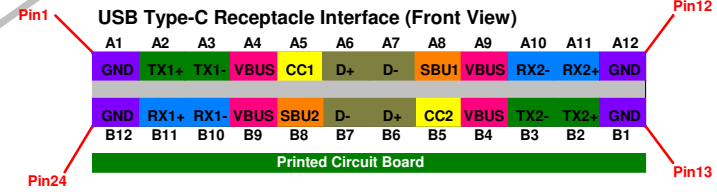
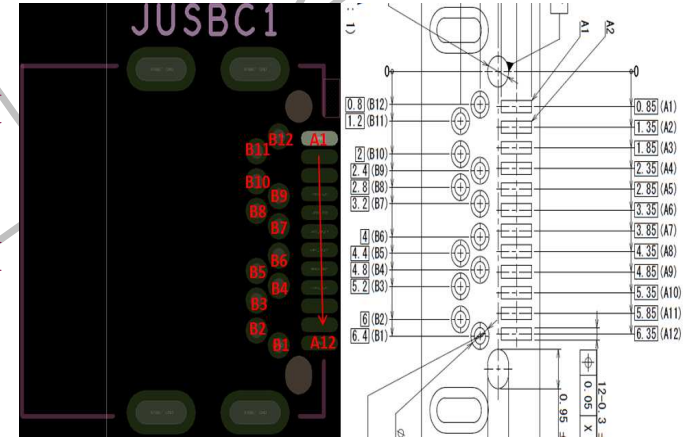
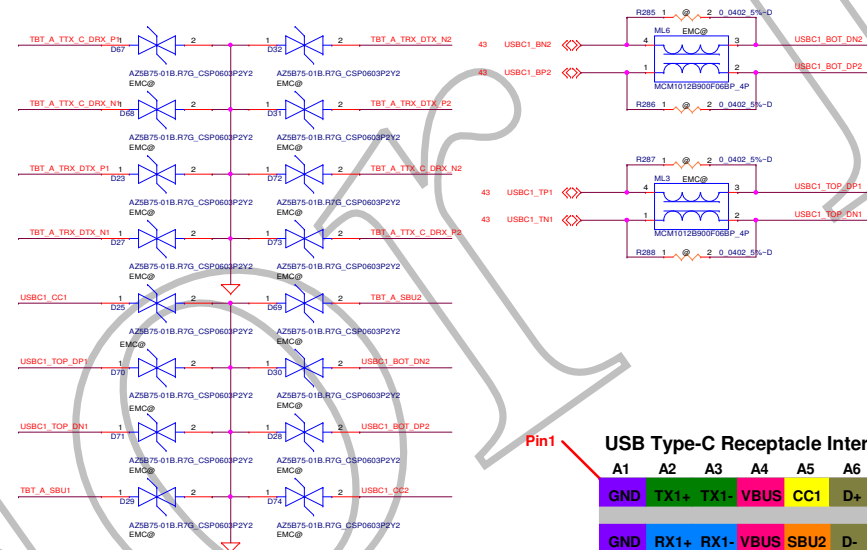
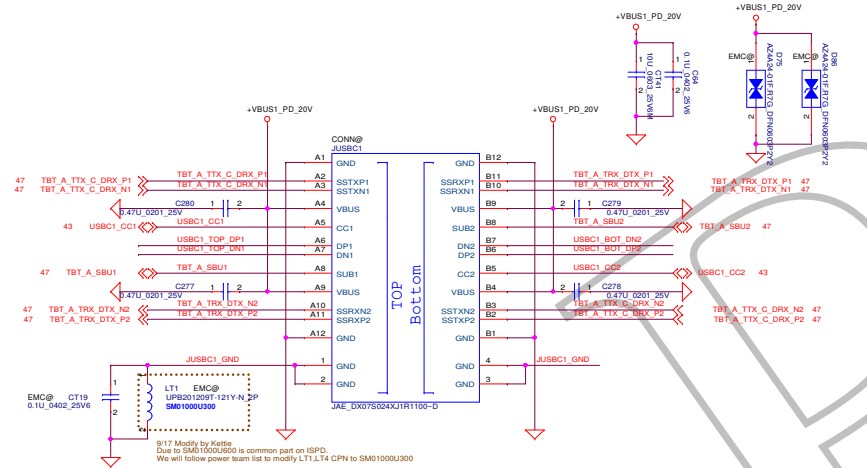


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Date		Thursday, October 17, 2019		Sheet	
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Module CONN Pin NO	M/B CONN Pin define	Pin Define	Module CONN Pin NO	M/B CONN Pin define	Pin Define
41	1	DGND	42	2	Lite-on det (Pull Low) Chicony det (Pull High)
39	3	LED_PWR	40	4	ALS_3V
37	5	LED_GND	38	6	ALS_SDA
35	7	5M_RESET	36	8	ALS_SCL
33	9	5M_SDA	34	10	ALS_INT
31	11	5M_SCL	32	12	IR_SCL
29	13	5M_VDDIO	30	14	IR_SDA
27	15	5M_DVDD	28	16	IR_RESET
25	17	5M_AGND	26	18	IR_DVDD
23	19	5M_AVDD	24	20	IR_AVDD
21	21	DGND	22	22	IR_AGND
19	23	5M_MCLK	20	24	IR_VDDIO
17	25	DGND	18	26	DGND
15	27	5M_MDP0	16	28	DGND
13	29	5M_MDN0	14	30	IR_MCN
11	31	DGND	12	32	IR_MCP
9	33	5M_MCP	10	34	DGND
7	35	5M_MCN	8	36	IR_MDN
5	37	DGND	6	38	IR_MDP
3	39	5M_MDP1	4	40	DGND
1	41	5M_MDN1	2	42	IR_MCLK
PP3	43	IR_LED+	PP4	44	IR_LED-
PP1	45	DGND	PP2	46	DGND



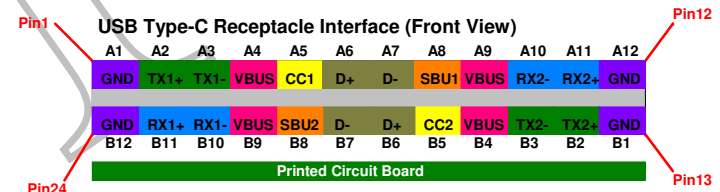
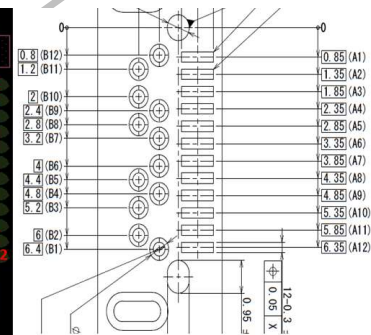
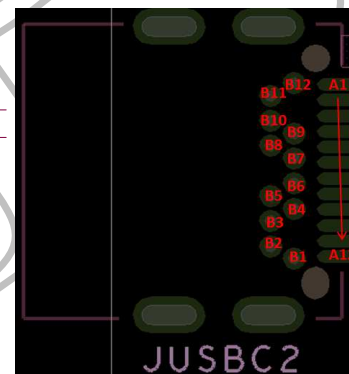
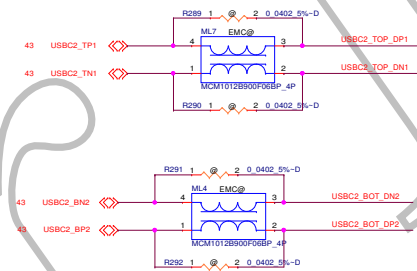
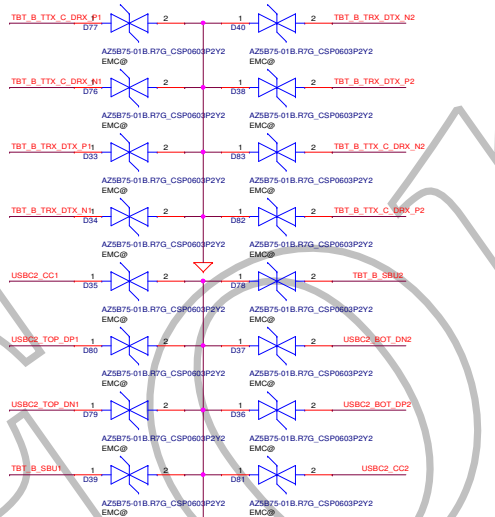
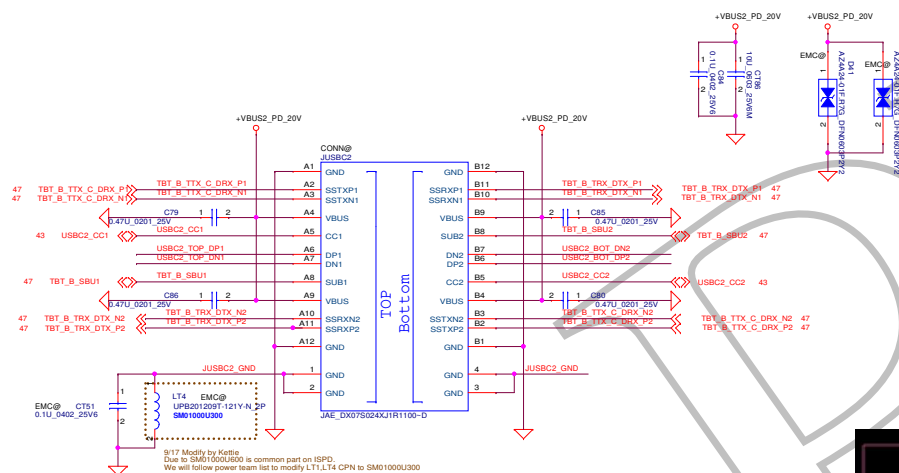


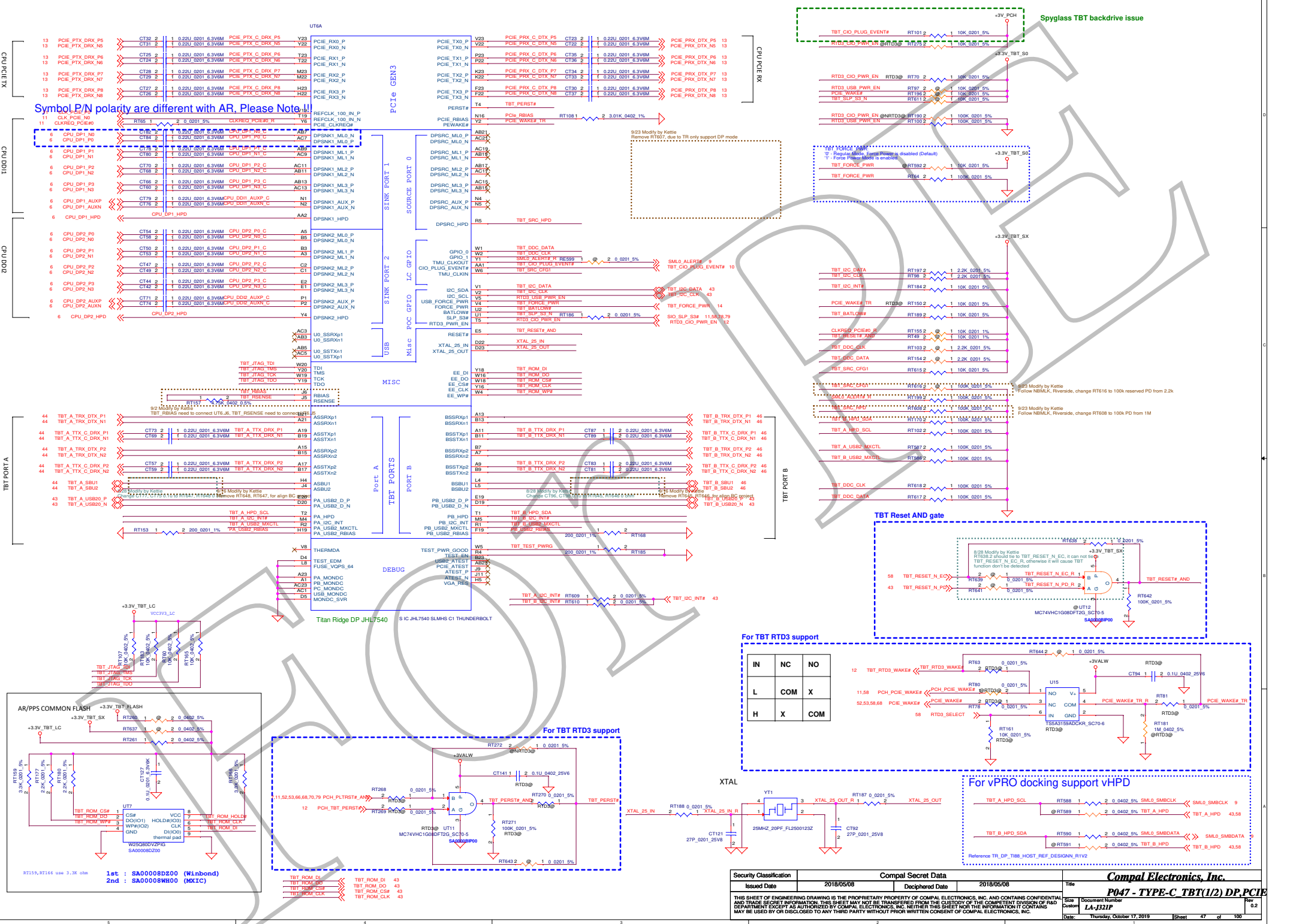
5/21 Modify by Kettie
Remove CT359-CT382, LT16-LT19, because no need
4/30 Modify by Kettie
Alignment with SA, change EMI component to depop

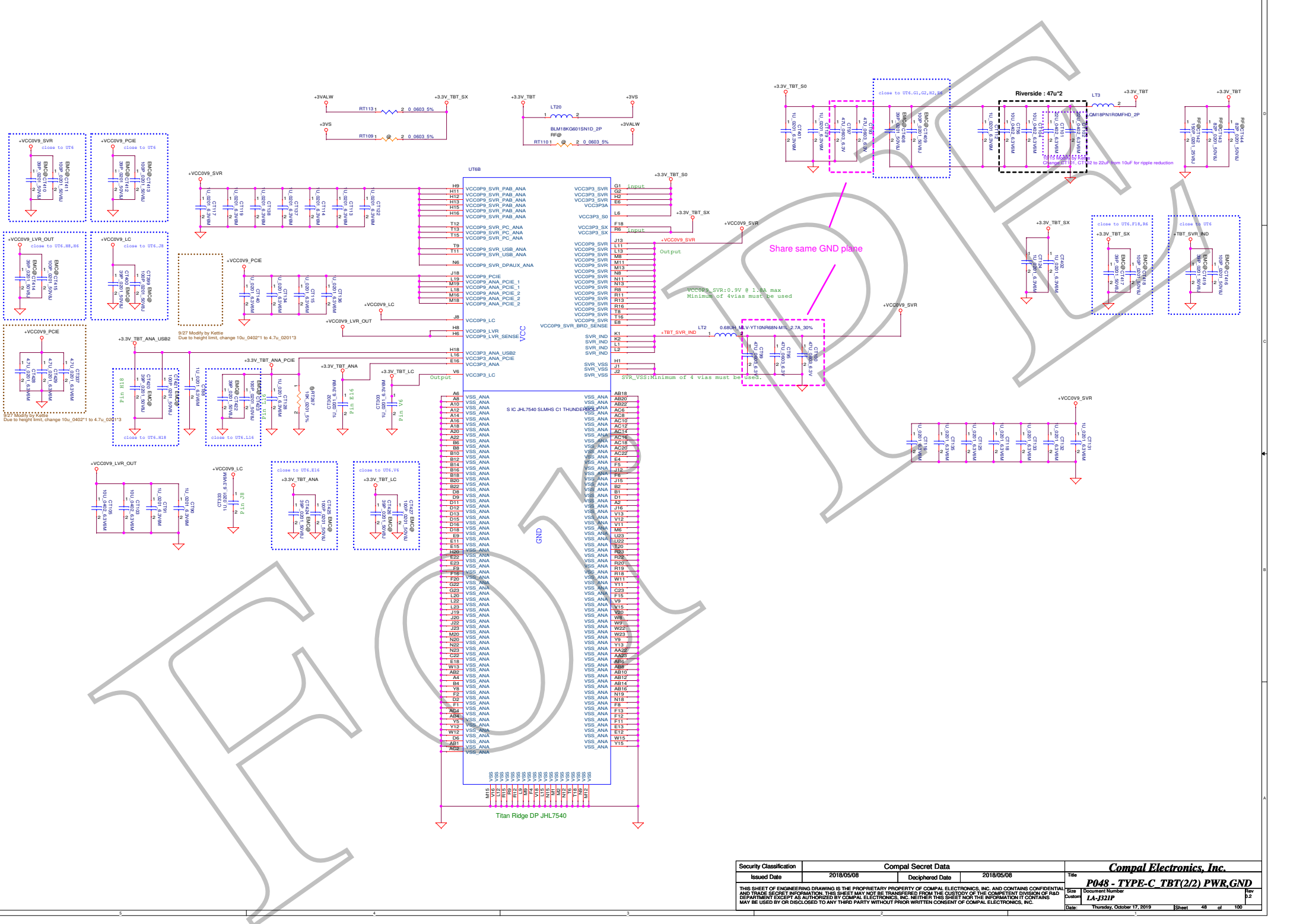


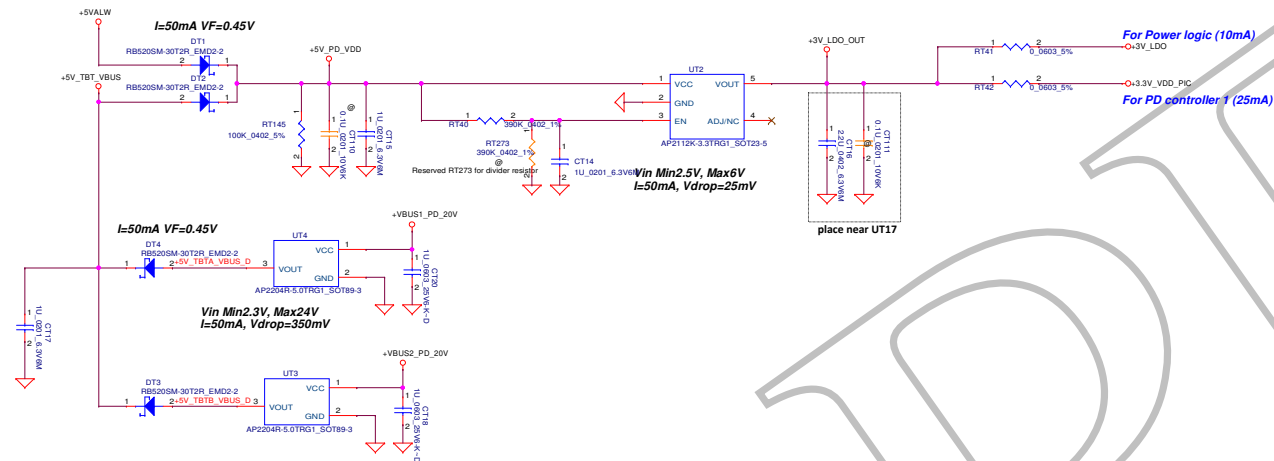
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				Thursday, October 17, 2019	0.2
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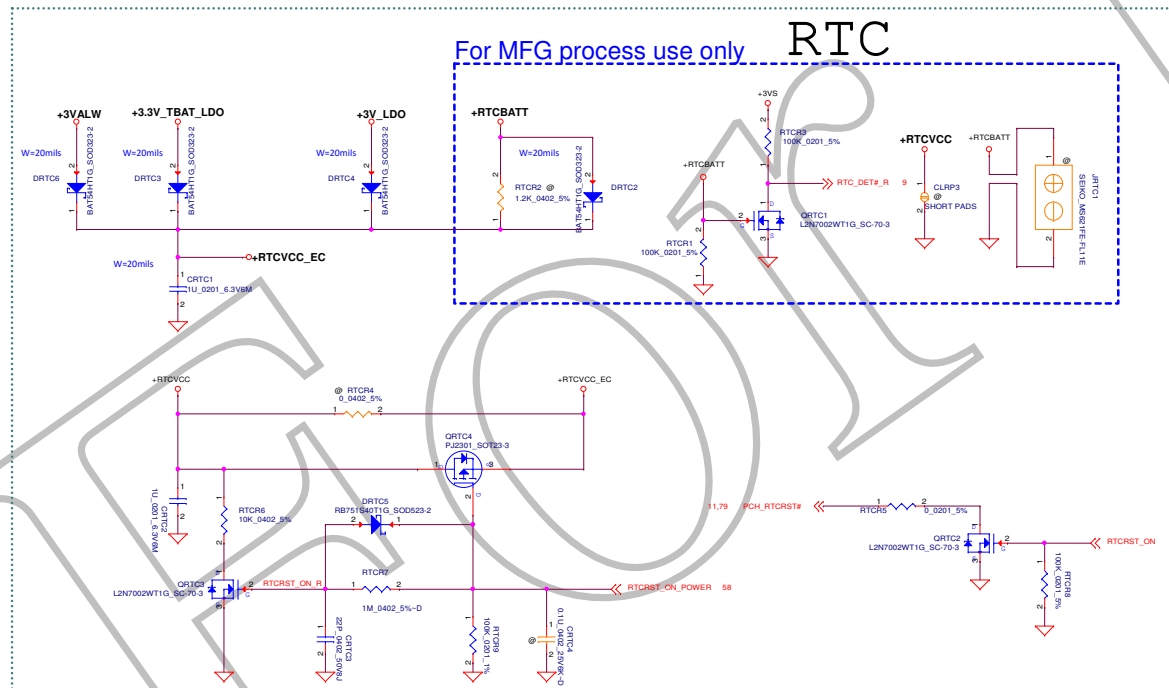








8/22 Modify by Kettie
 For layout simulation request, modify location, RTC22-RTC24 to RTC22-RTC23, RTC21-RTC24 to RTC21-RTC23, RTC1-RTC4 to RTC1-RTC4, RTC1 to RTC1



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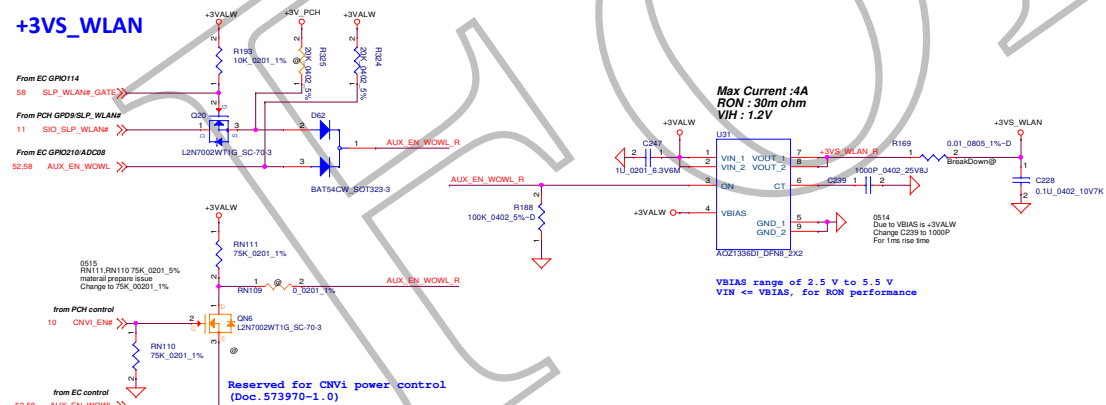
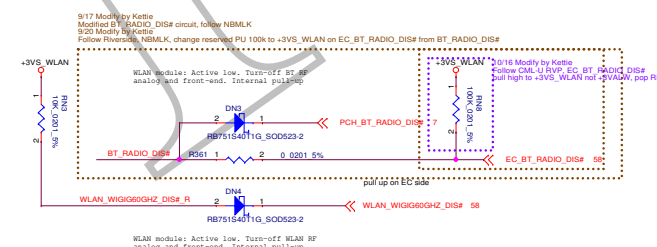
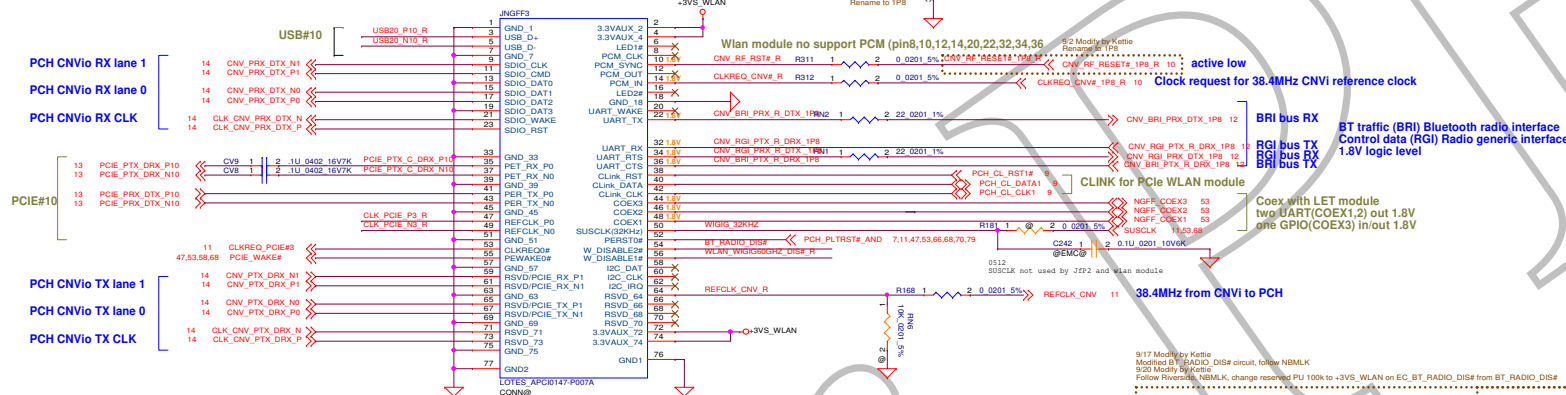
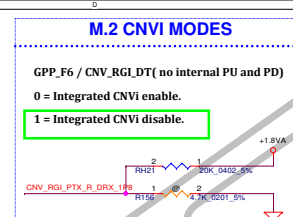
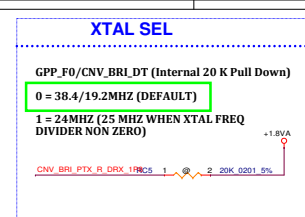
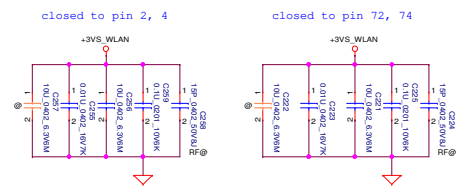
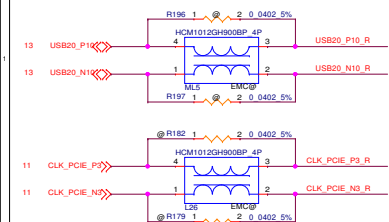
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				LA-J321P	
				Date:	Thursday, October 17, 2019
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3		2			

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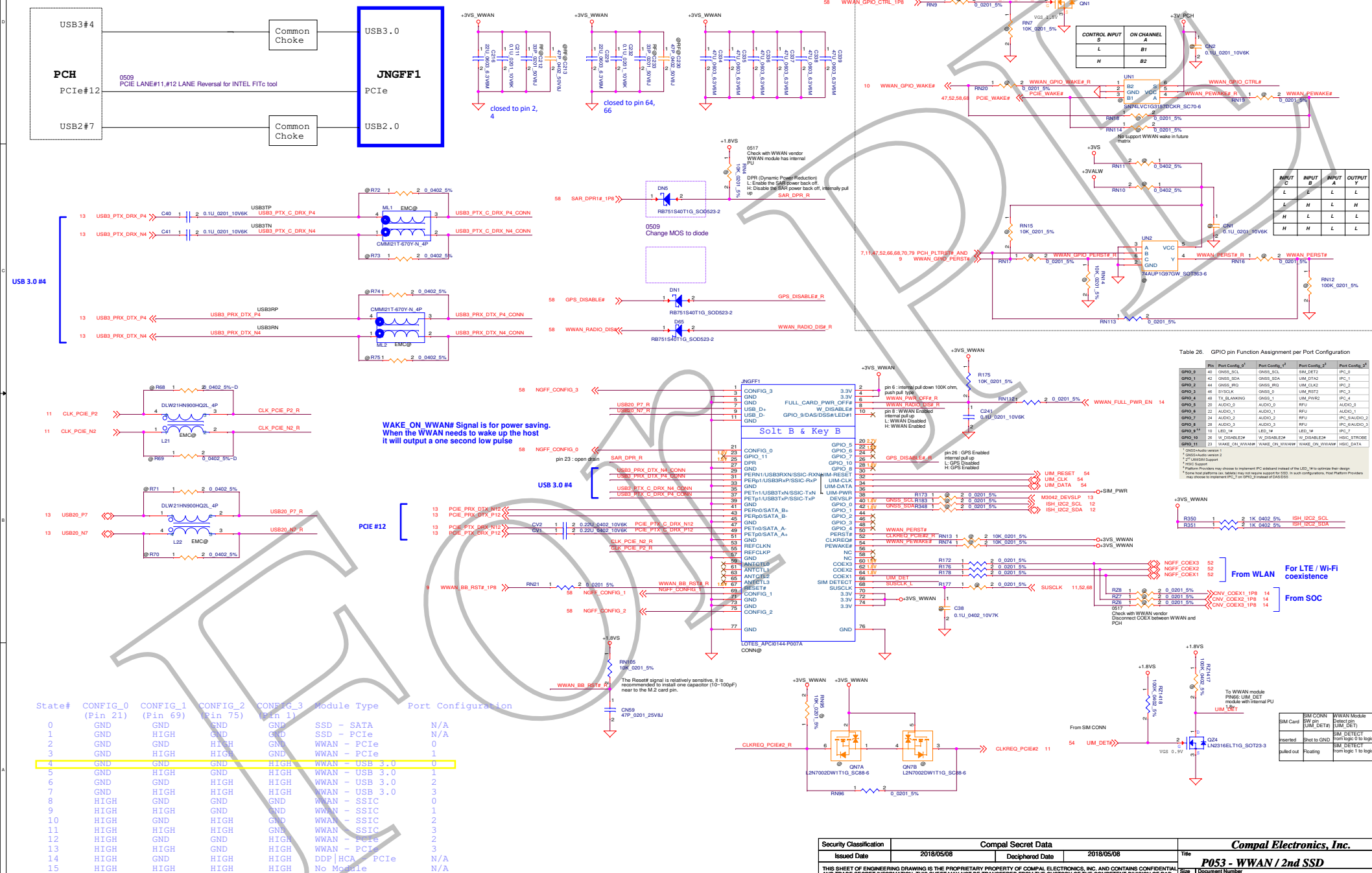
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				LA-J321P	
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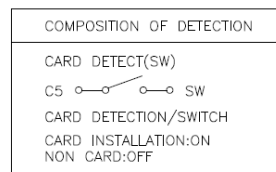
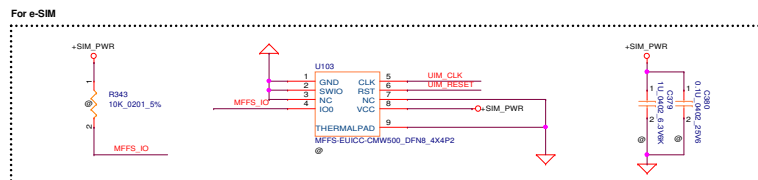
WLAN/BT/CNVi/PCIe
M.2 2230 Key-E



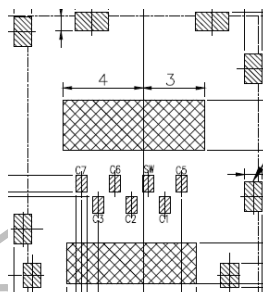
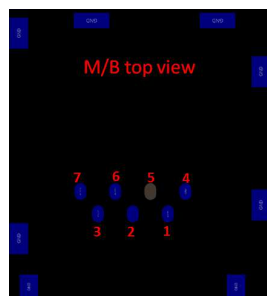
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WWAN USB
M.2 3042 Key-B



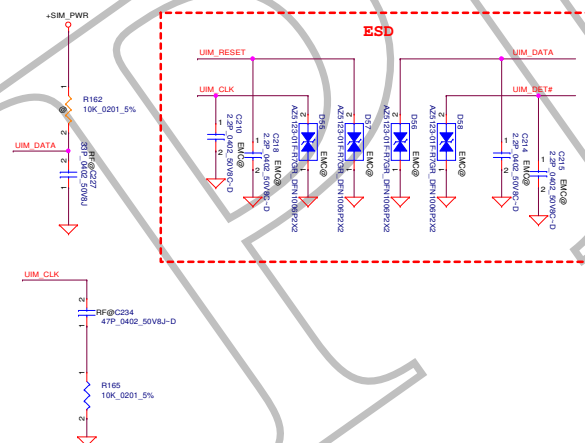


NANO SIM normal Open CONN.
No Card: SW floating
Card install: SW shot to GND(C5)



SIM Card Pin Assignments

NANO SIM CARD	
C1	Vcc
C2	RST
C3	CLK
C5	GND
SW	CD/SW
C6	Vpp
C7	DATA

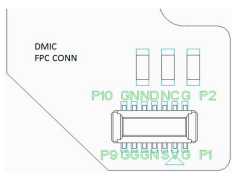
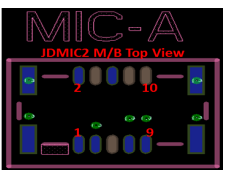
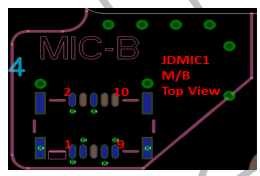
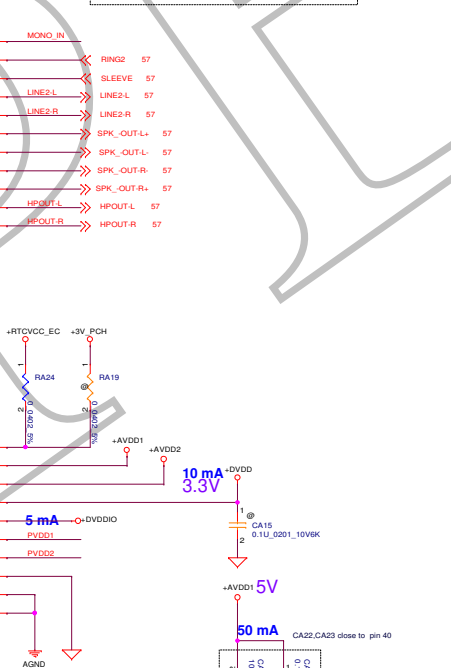
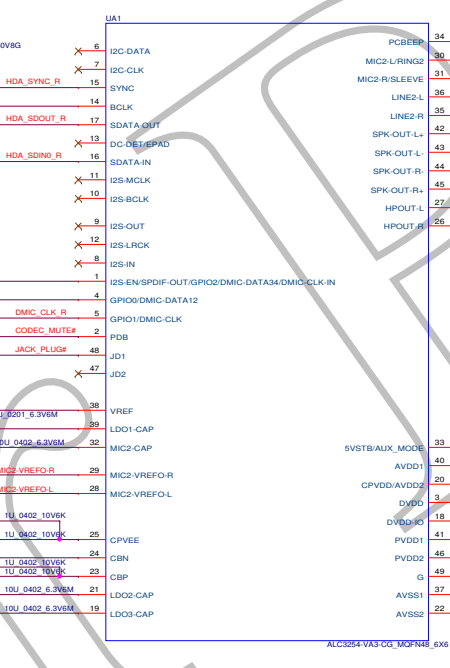
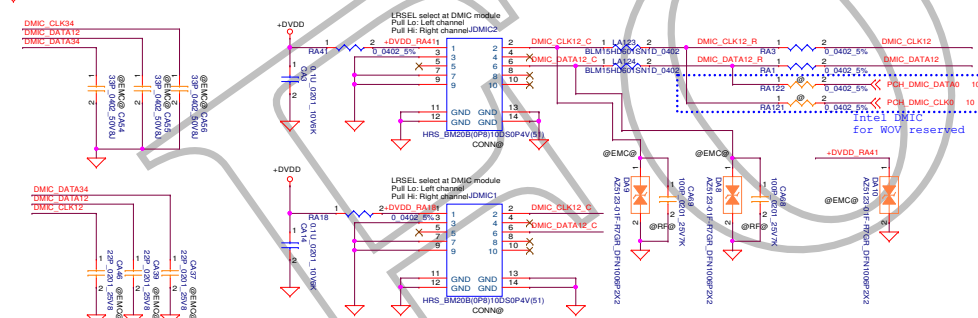
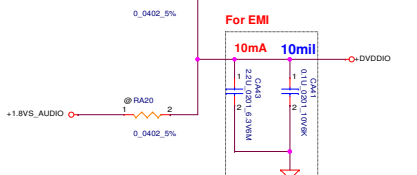
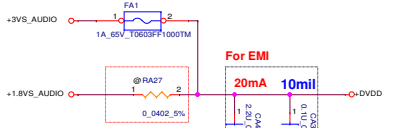
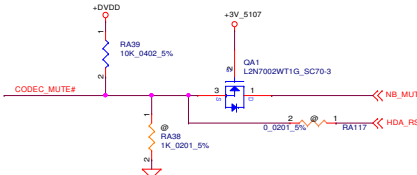
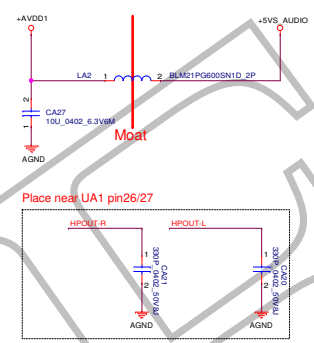
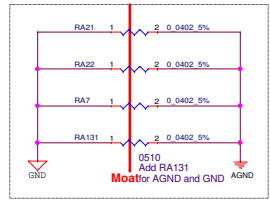
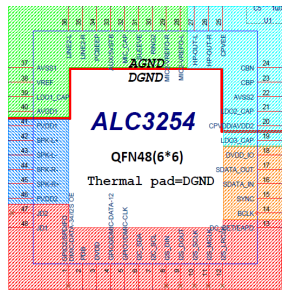
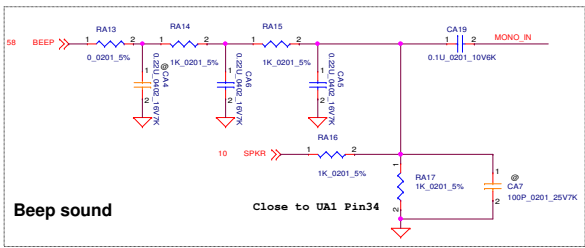


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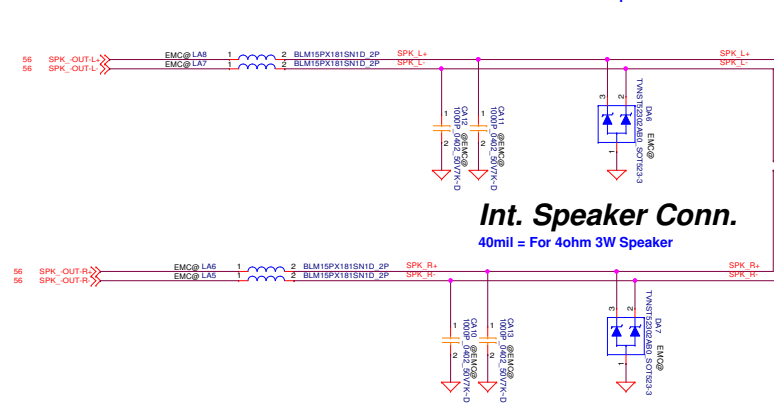
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Issued Date		2018/05/08	Deciphered Date	2018/05/08	
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				P055 - Reserve	
				Size	Rev
				Document Number	0.2
				LA-J321P	
				Date:	Thursday, October 17, 2019
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Date:		Thursday, October 17, 2019		Sheet 56 of 100	
P056 - Audio ALC3254		LA-J321P		Rev 0.2	

Int. Speaker Conn.

40mil = For 4ohm 3W Speaker



Int. Speaker Conn.

40mil = For 4ohm 3W Speaker

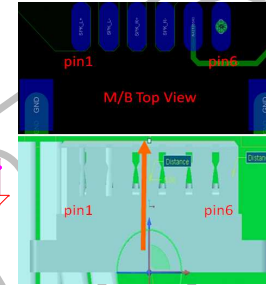
SPK_DET# (SPK_ID)	Speaker Vendor
High	FG
Low	YC

FG

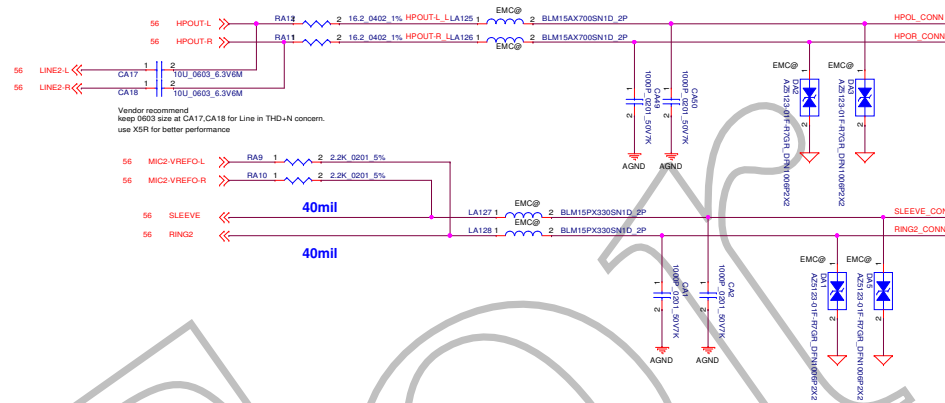
Conn Pin	Net name	Cable color
Pin 6	N/A	N/A
Pin 5	N/A	N/A
Pin 4	SPK R-	Black
Pin 3	SPK R+	Red
Pin 2	SPK L-	Blue
Pin 1	SPK L+	White

YC

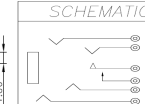
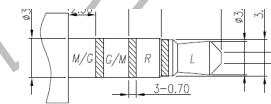
Conn Pin	Net name	Cable color
Pin 6	Loop with 5	Green
Pin 5	Loop with 6	Green
Pin 4	SPK R-	Black
Pin 3	SPK R+	Red
Pin 2	SPK L-	Blue
Pin 1	SPK L+	White



Universal Audio Jack

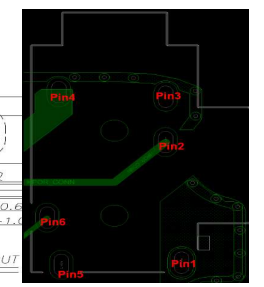
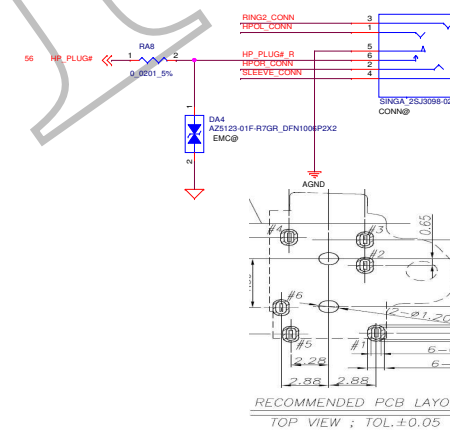


Universal Audio Jack CONN

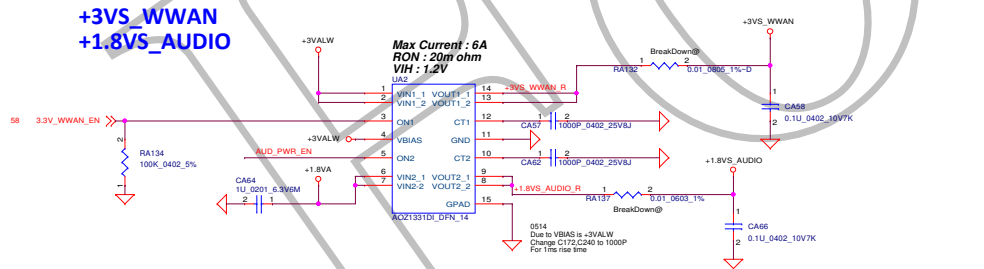


SINGATRON ENTERPRISE CO., LTD.	
信音企業股份有限公司	
TITLE: #3.50 AUDIO JACK	
DATE: 09/09/2019	PART NO: 2S3098-027111F
CHG: Bruce	SCALE: 4:1 UNIT: mm
APPR: Loo	SIZE: A3 SHEET: 1 OF 1
CUSTOMER COPY	

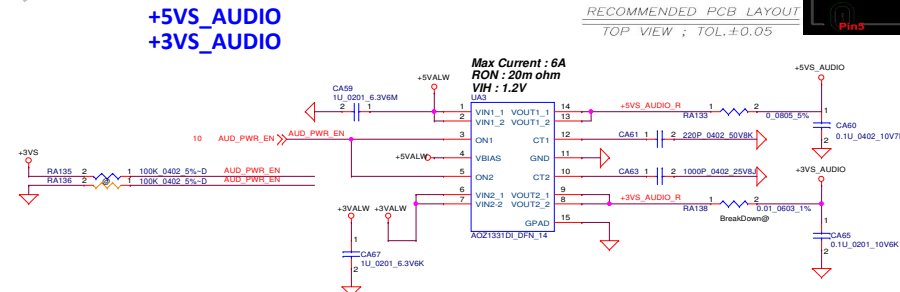
Audio Signal	Audio CONN Pin
RING2 CONN	#3 G/M
HPOL CONN	#1 L/R
HPOR CONN	#2 R/L
SLEEVE CONN	#4 M/G
HP_PLUG# R	#6
AGND	#5

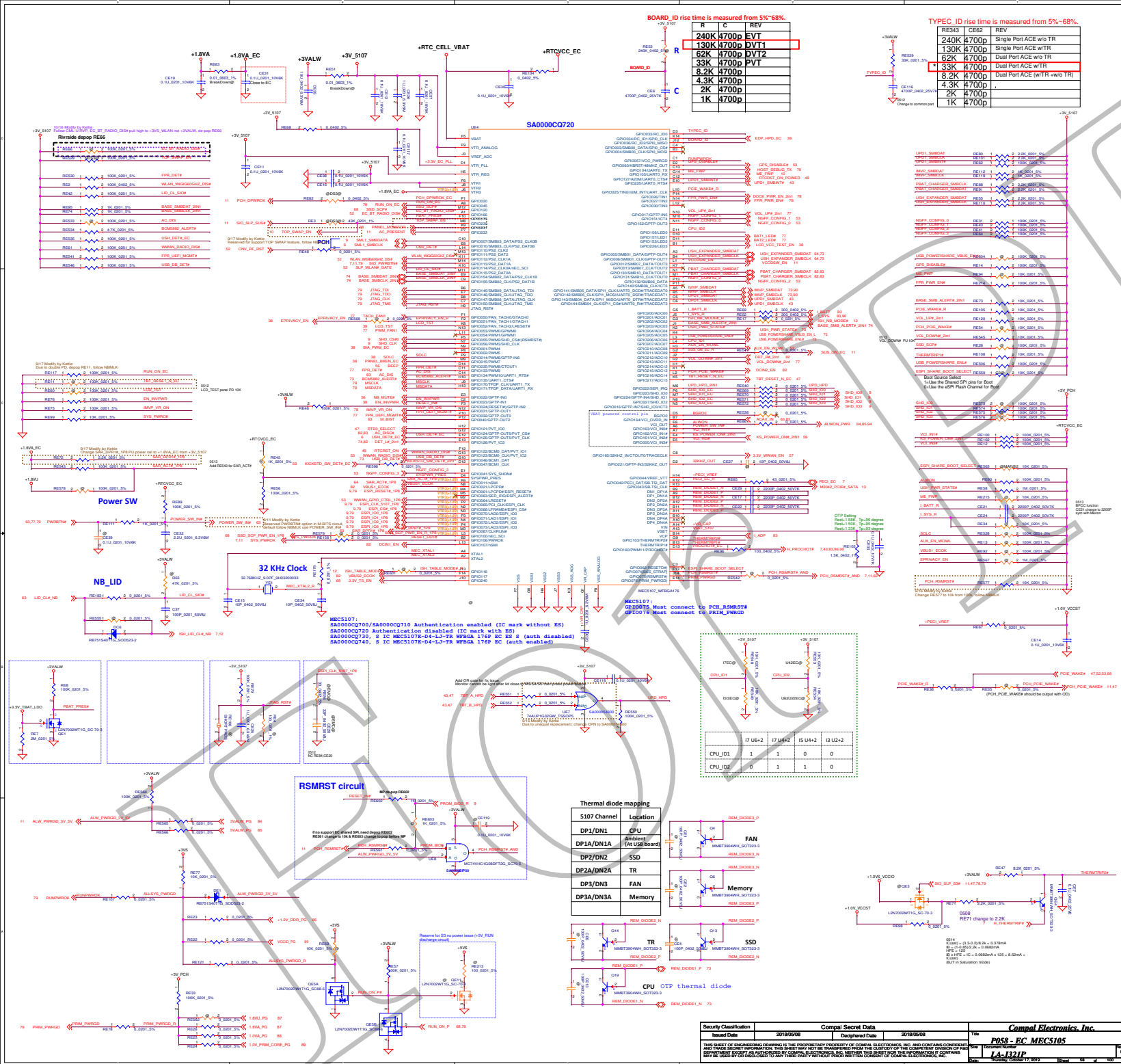


+3VS_WWAN
+1.8VS_AUDIO

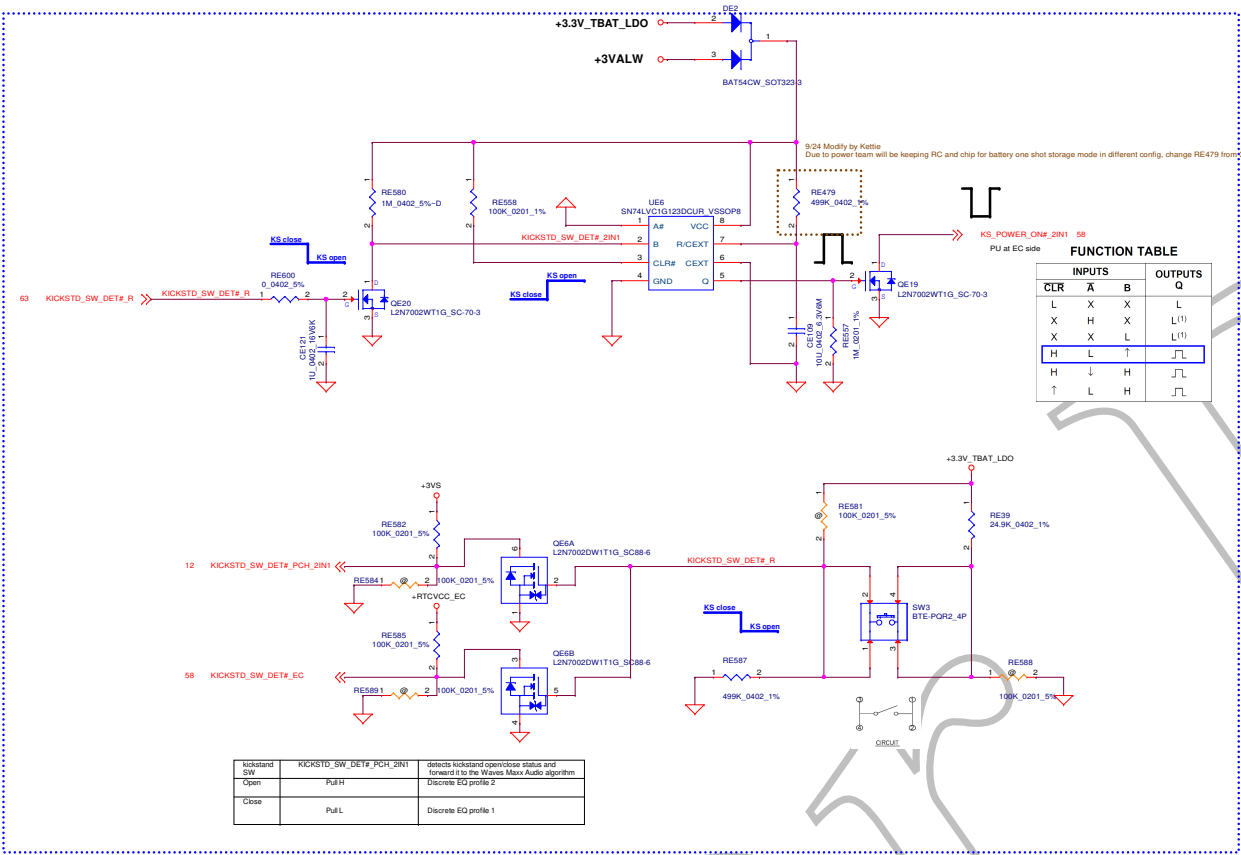


+5VS_AUDIO
+3VS_AUDIO

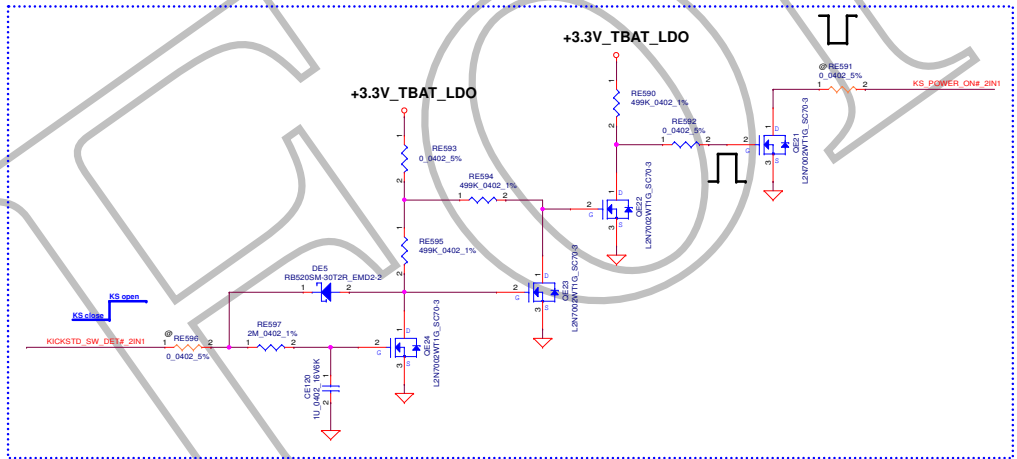




S5 LID OPEN POWER ON
Storage mode wake up circuit

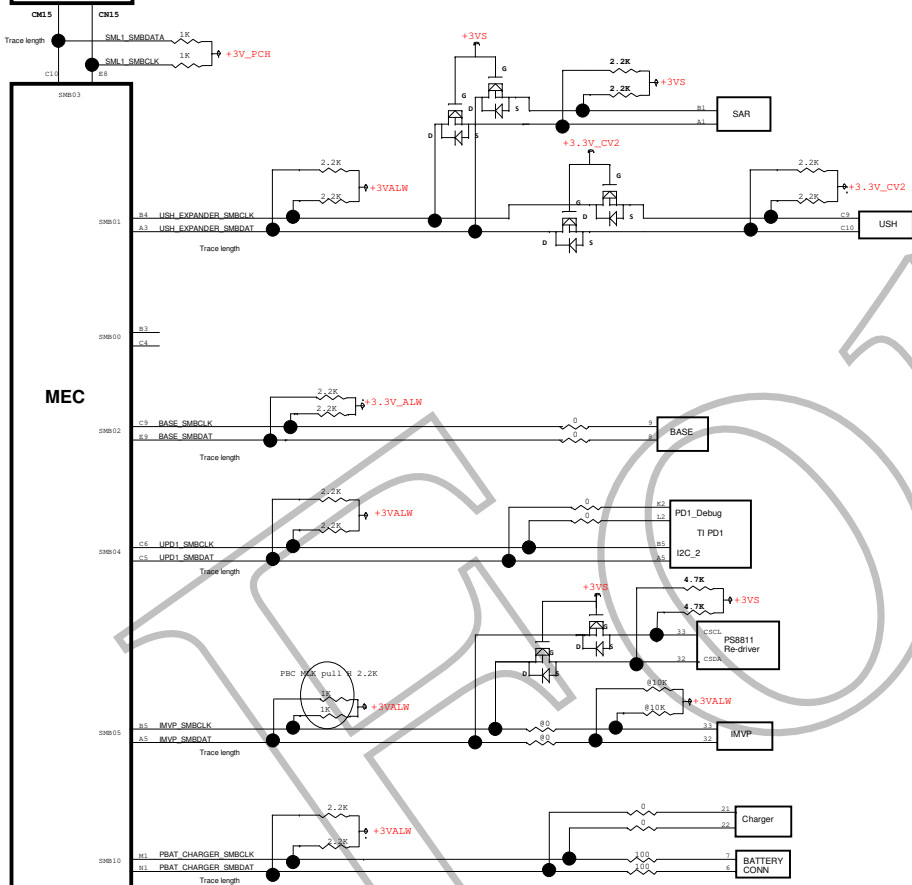
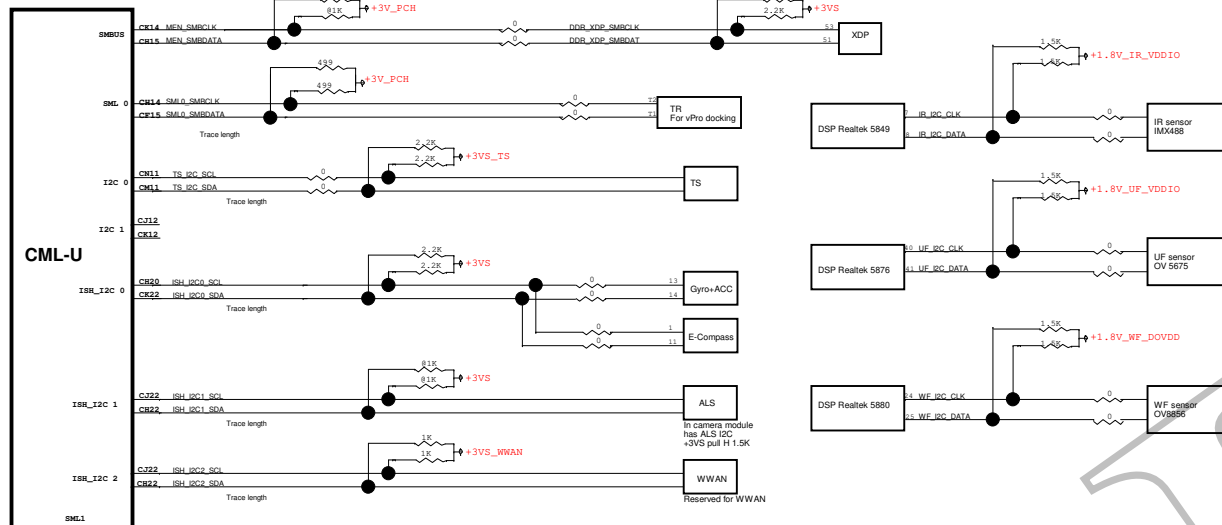


One shoot (Reserved)



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Size		Document Number			Rev
Date:		Thursday, October 17, 2019			0.2
Sheet		60		of	100

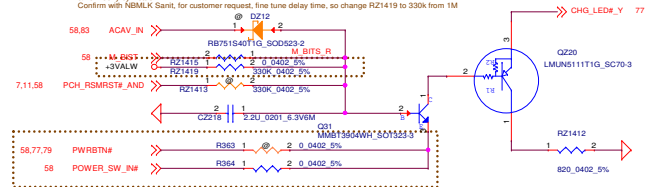


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				Size	Document Number
				LA-J321P	
				Date:	Thursday, October 17, 2019
		Sheet	62	of	100

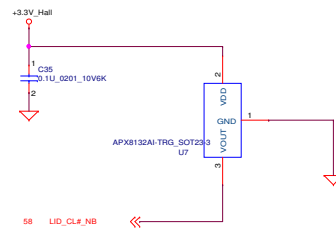
M-BITS

9/16 Modify by Kettie
Confirm with NBMLK Sanit, for customer request, fine tune delay time, so change RZ1419 to 330k from 1M



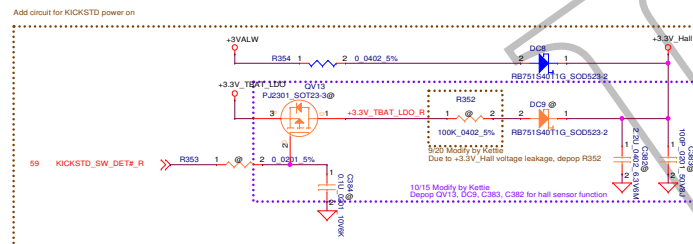
9/11 Modify by Kettle
Reserved PWRBTN# option in M-BITS circuit, default follow NBMLK use POWER_SW_IN#

Hall sensor



Output is P.P. type

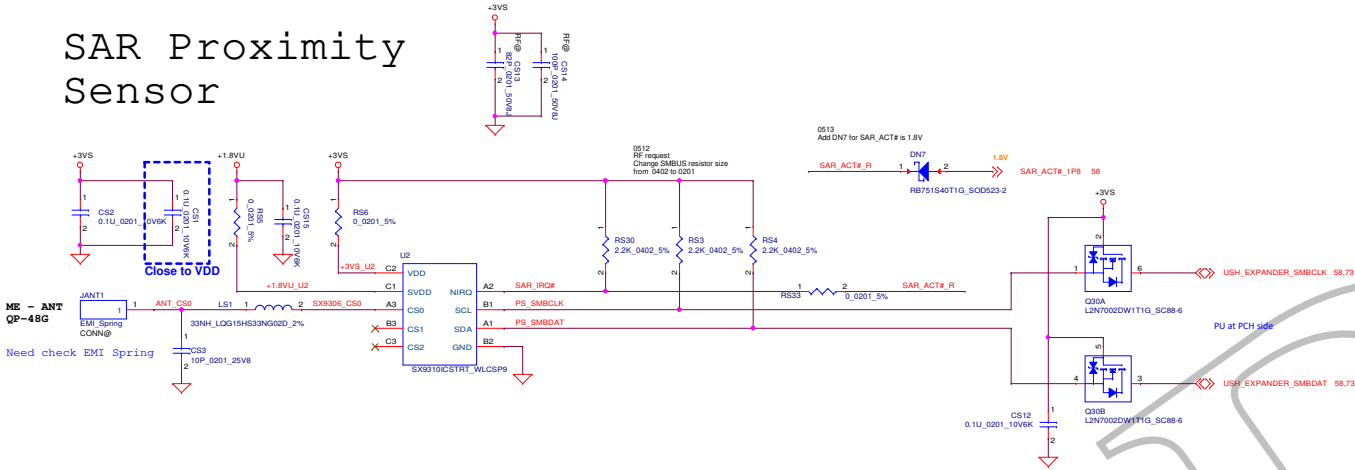
Mmagnetic field enters the hall sensor, output turns on (output is low).
Magnetic field release point, output turns off (output is high).



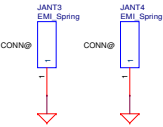
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Security Classification		Compel Secret Data		Title	
Issued Date		Deciphered Date		Compel Electronics, Inc. P063 - LED MBITS / LID	
2018/05/08		2018/05/08		Docuement Number LA-1321P	
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				Date:	10.2
				Thursday, October 17, 2019	Sheet 63 of 30

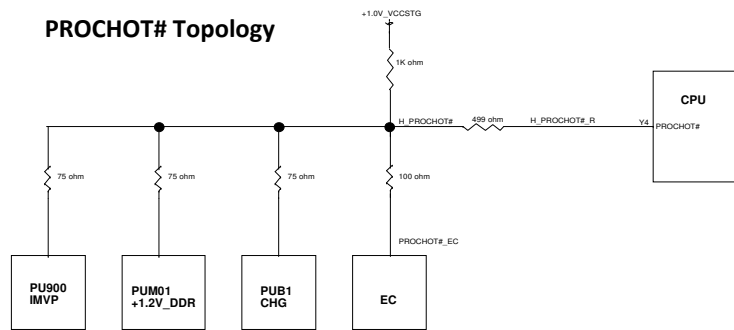
SAR Proximity Sensor



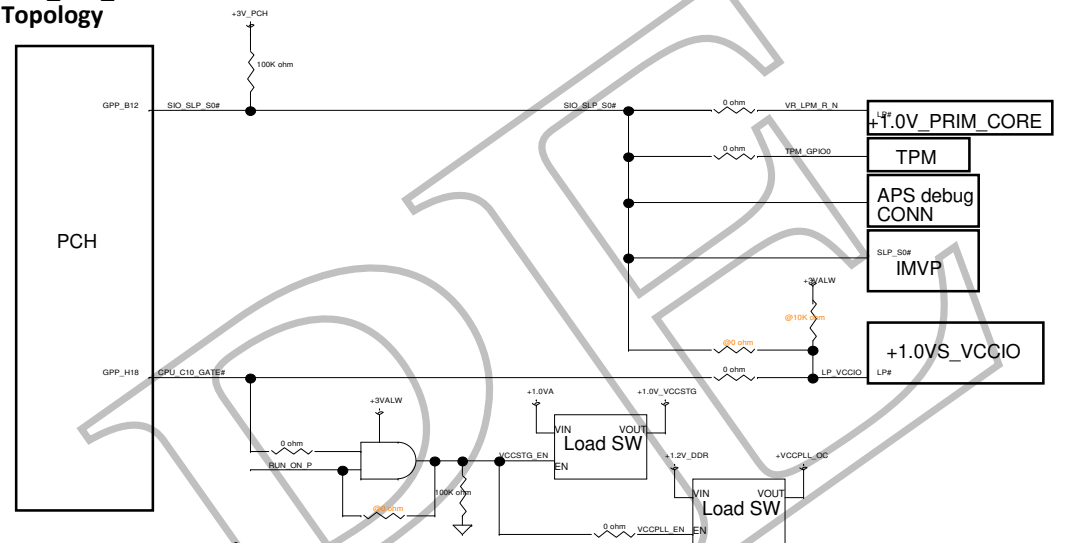
Tunable IC



PROCHOT# Topology

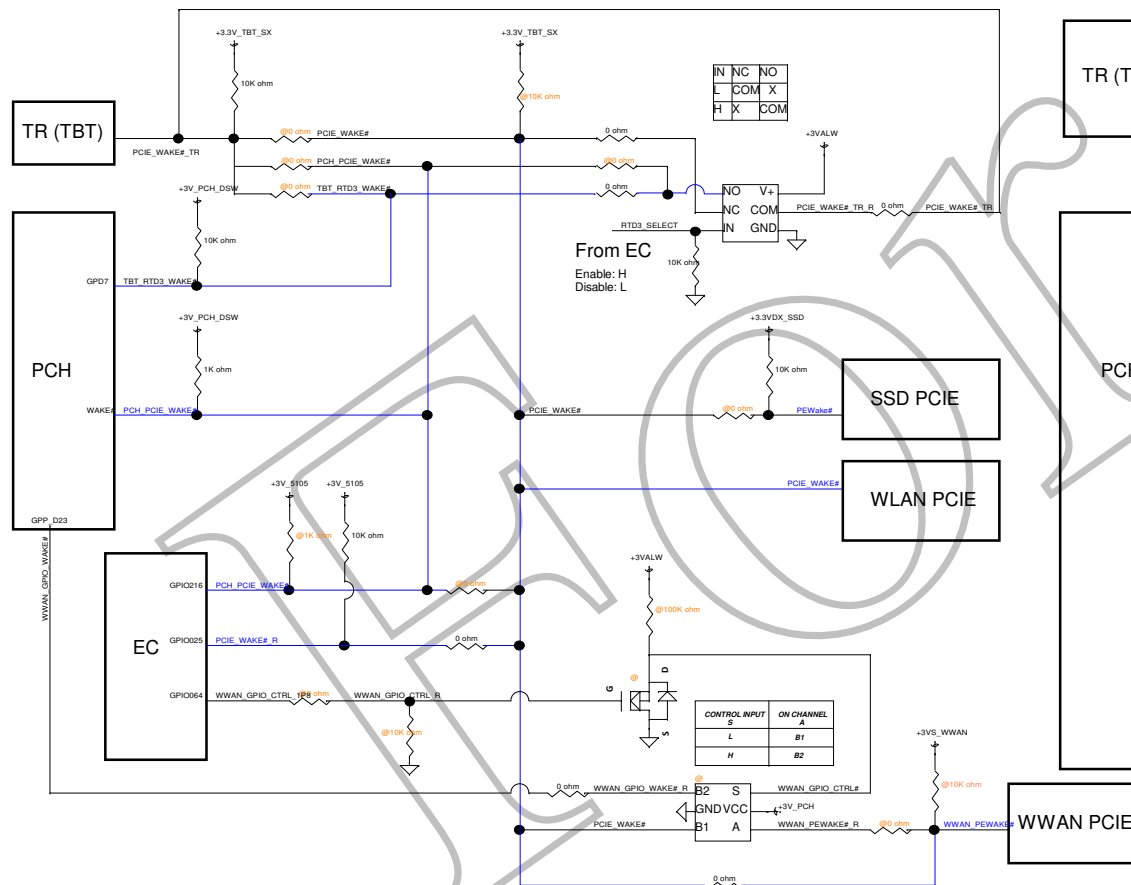


SIO_SLP_S0#
CPU_C10_GATE#
Topology

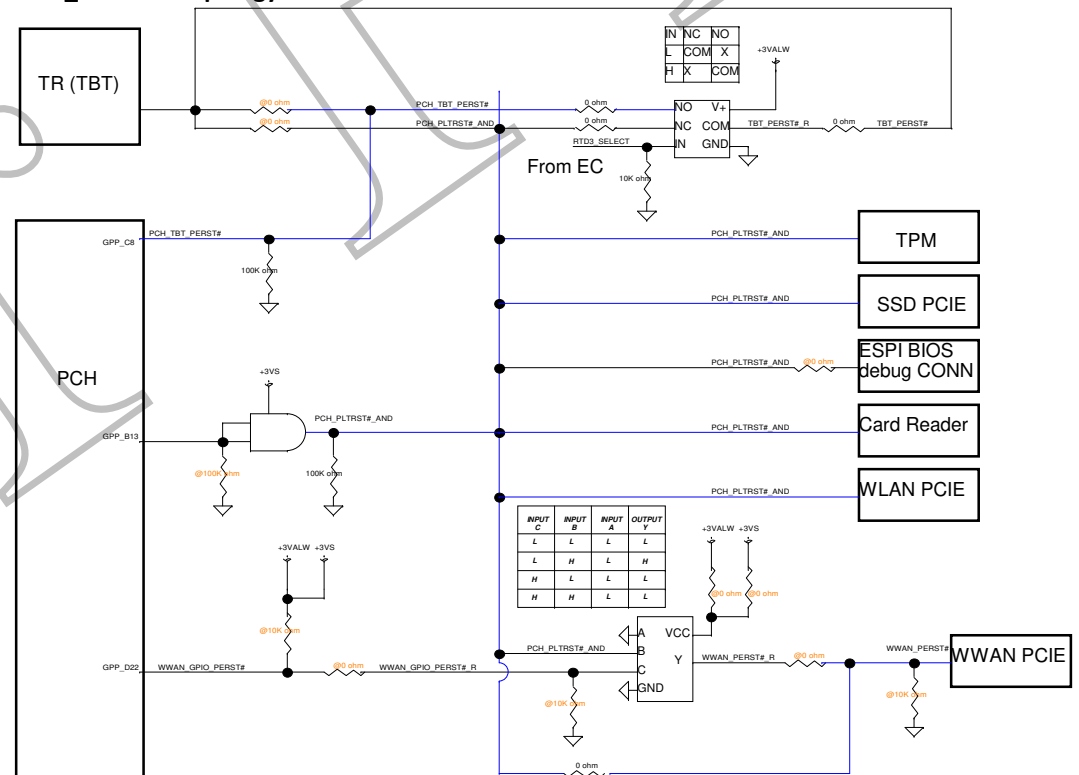


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PCH_PCIE_WAKE# Topology

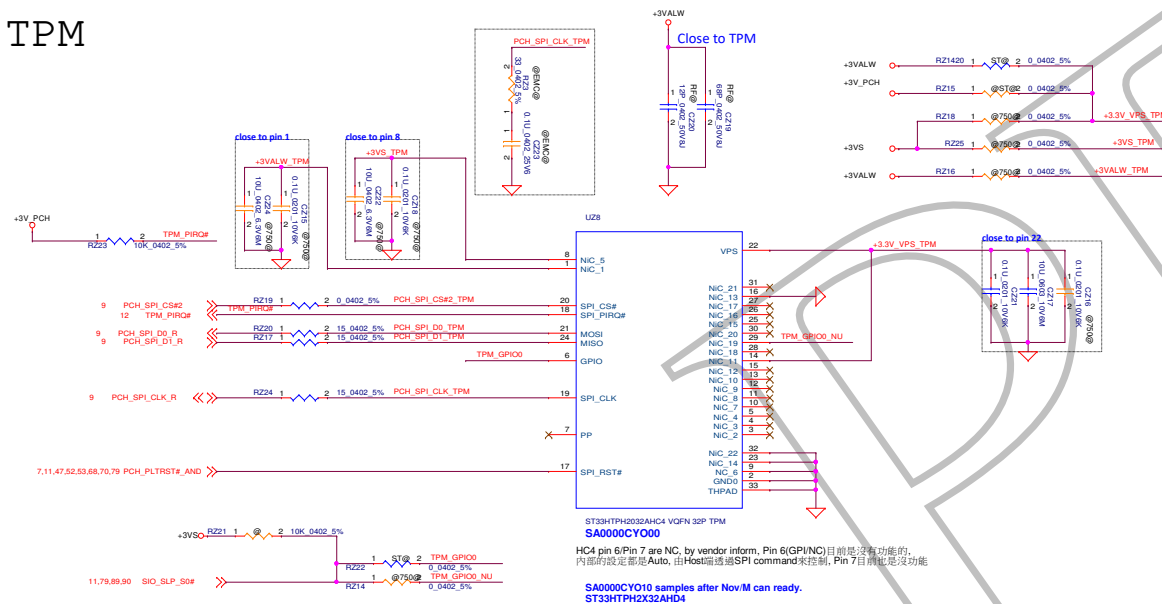


PCH_PLTRST# Topology

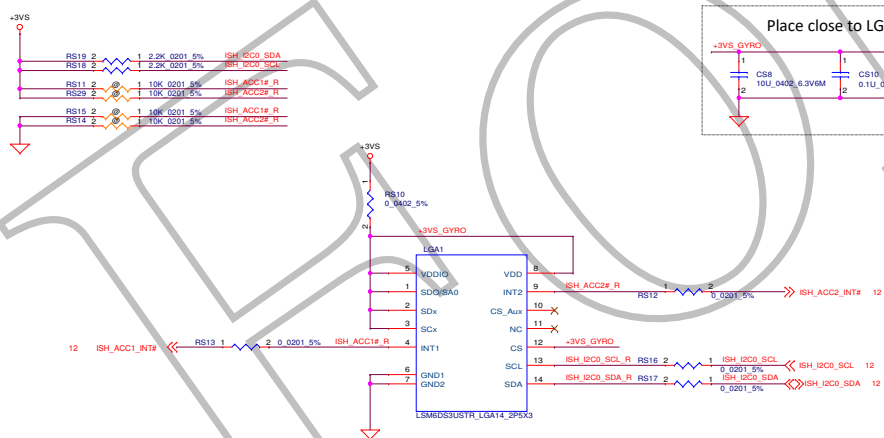


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					LA-J321P (Revised 17 2018)
				Drawn	Rev 0/2

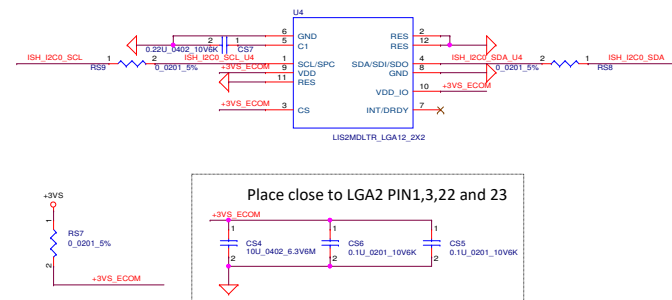
TPM



3D accelerometer and 3D gyroscope



E-Compass



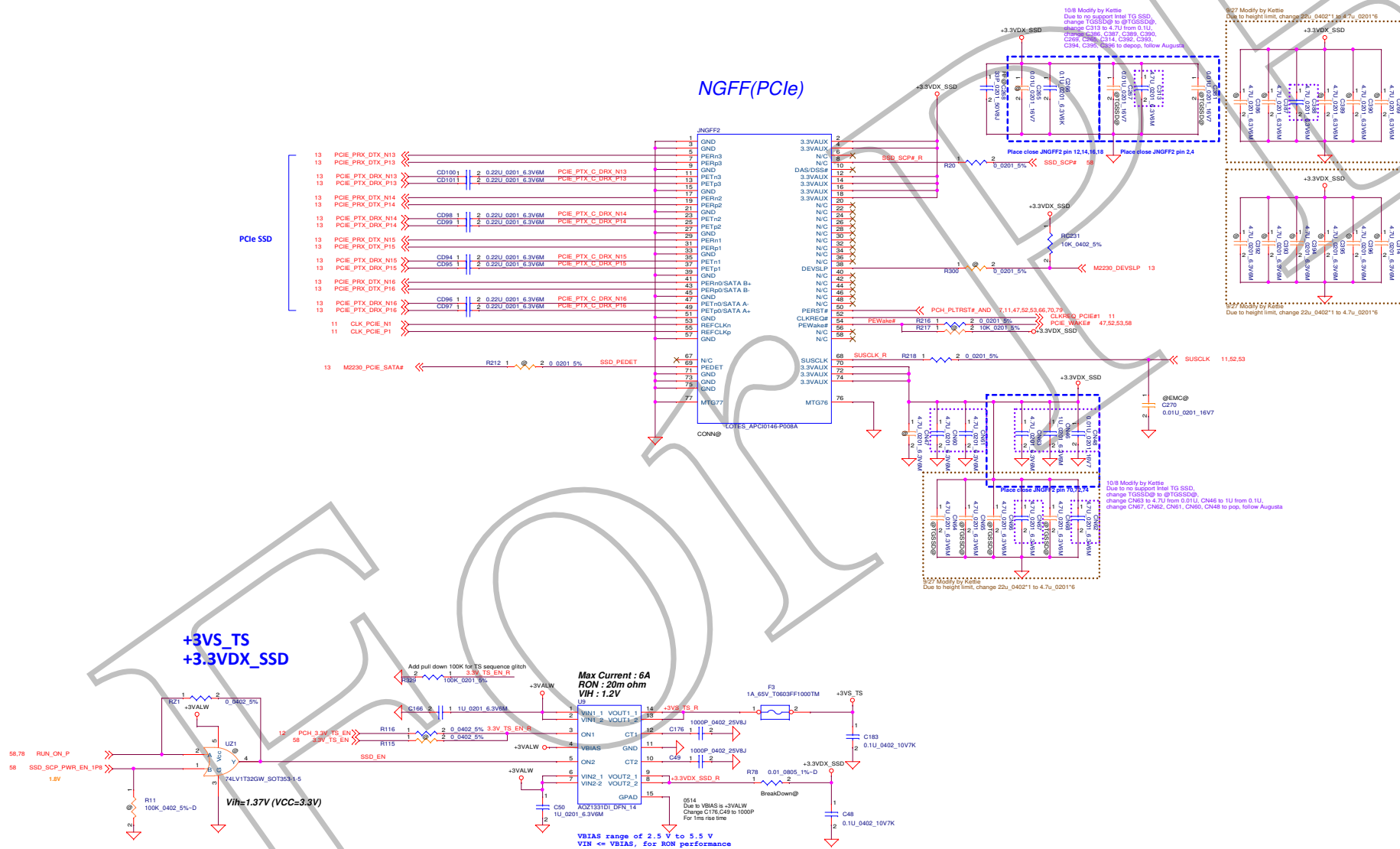
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Date: Thursday, October 17, 2019				Sheet 66 of 100

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				P067 - Reserve	
				Size	Rev
				Document Number	0.2
				LA-J321P	
				Date:	Thursday, October 17, 2019
				Sheet	67 of 100

SSD PCIe
M.2 2230 Key-M



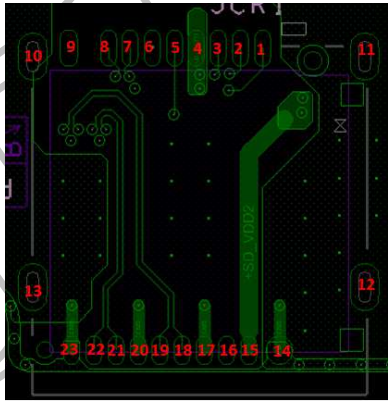
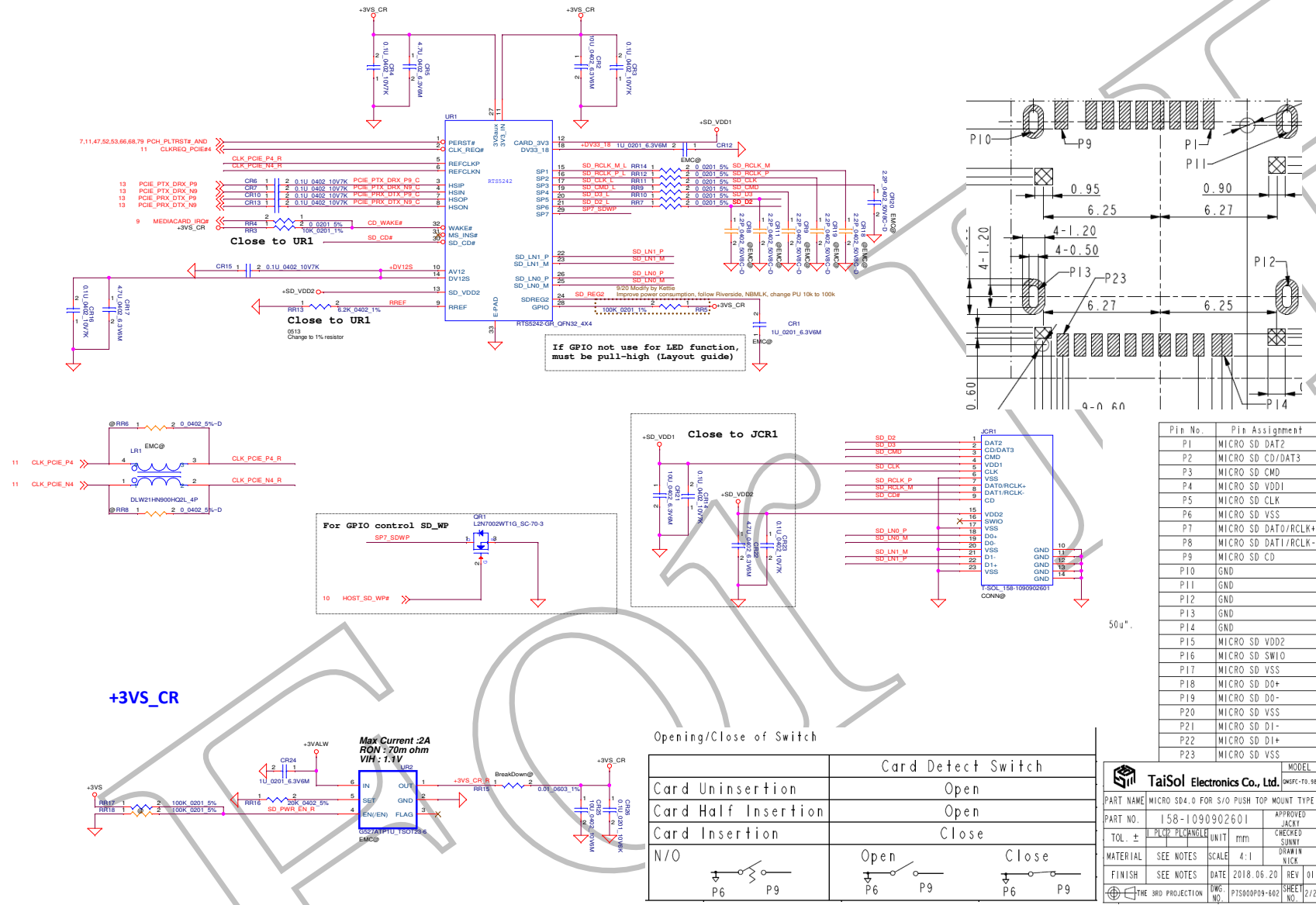
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Issued Date	2018/05/08	Deciphered Date	2018/05/08	Title	
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				LA-J321P (Revised)	Rev 0.2
				Date: 2018/05/17 2018	1 Sheet 68 of 100

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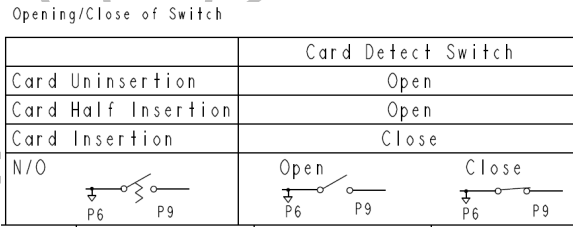
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				P069 - Reserve	
				Size	Rev
				Document Number	0.2
				LA-J321P	
				Date:	Thursday, October 17, 2019
				Sheet	69 of 100

Card Reader

- 1)Placing the RTS5242 chip and flash card socket locate to suit trace routing for SI / EMI / ESD.
- 2)Keep bulk and de-coupling capacitors as close as possible to the RTS5242 chip and flash card socket.
 - Bulk capacitor for Card_3V3 place closed to flash card socket.
 - Bulk capacitor for 3V3_IN / 3V3aux / DV128 place closed to RTS5242 chip.
- 3)Keep damping resistor (ex. for SD CLK / MS CLK) as close as possible to the RTS5242 chip.
- 4)Keep these capacitors for SD card / MS card signals as close as possible to flash card socket.



Pin No.	Pin Assignment
P1	MICRO SD DAT2
P2	MICRO SD CD/DAT3
P3	MICRO SD CMD
P4	MICRO SD VDD1
P5	MICRO SD CLK
P6	MICRO SD VSS
P7	MICRO SD DAT0/RCLK+
P8	MICRO SD DAT1/RCLK-
P9	MICRO SD CD
P10	GND
P11	GND
P12	GND
P13	GND
P14	GND
P15	MICRO SD VDD2
P16	MICRO SD SWIO
P17	MICRO SD VSS
P18	MICRO SD DO+
P19	MICRO SD DO-
P20	MICRO SD VSS
P21	MICRO SD DI-
P22	MICRO SD DI+
P23	MICRO SD VSS



TaiSol Electronics Co., Ltd.
PART NAME MICRO SD4.0 FOR S/O PUSH TOP MOUNT TYPE
PART NO. 158-1090902601
TOL. ± 0.1mm
MATERIAL SEE NOTES
FINISH SEE NOTES
DATE 2018.06.20
DWG. NO. P7500DP09-502

MODEL
DWGFC-TO-50
APPROVED JACY
CHECKED SUNNY
DRAWN NICE
REV 01
SHEET 2/2

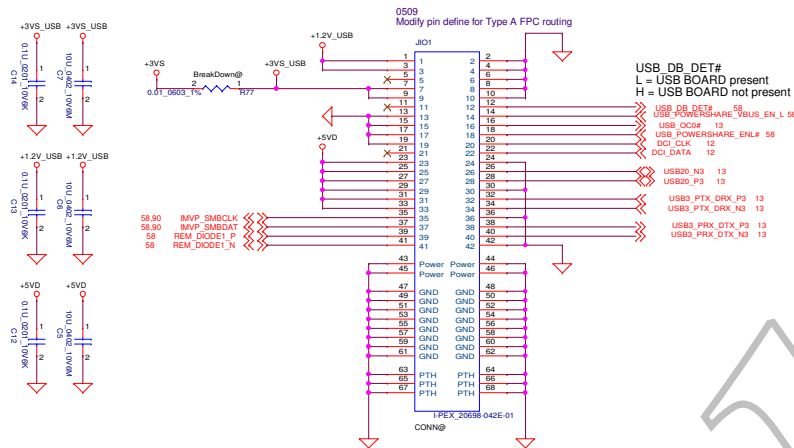
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				P071 - Reserve	
				Size	Rev
				Document Number	0.2
				LA-J321P	
				Date:	Thursday, October 17, 2019
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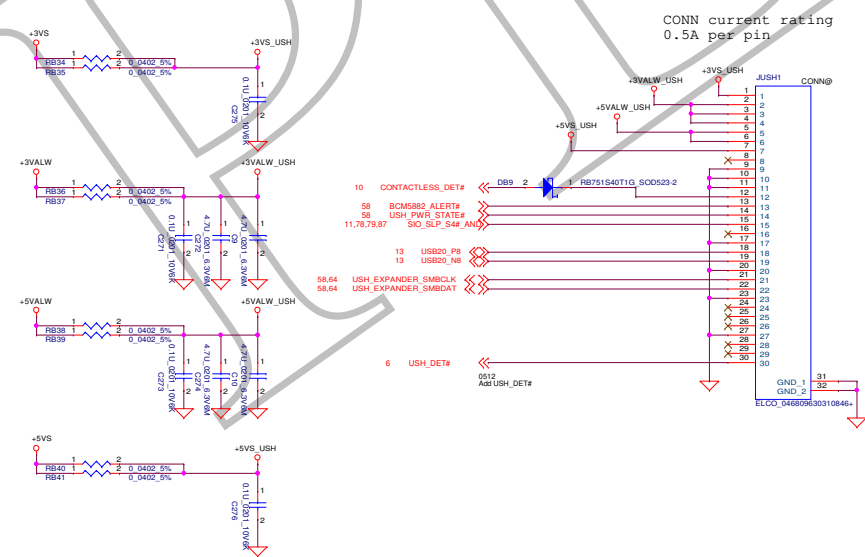
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				P072 - Reserve	
				Size	Document Number
				LA-J321P	
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3		2			

USB Board CONN



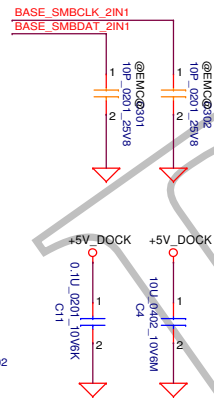
USH CONN.



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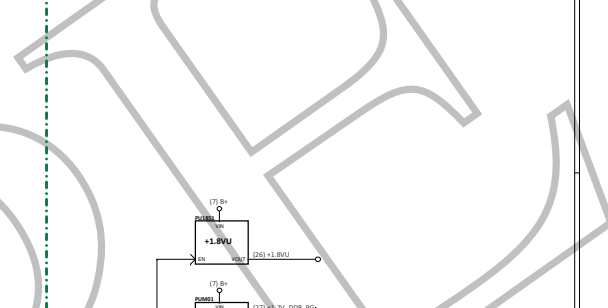
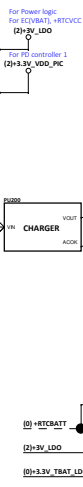
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Date: Thursday, October 17, 2019				Sheet 73 of 100

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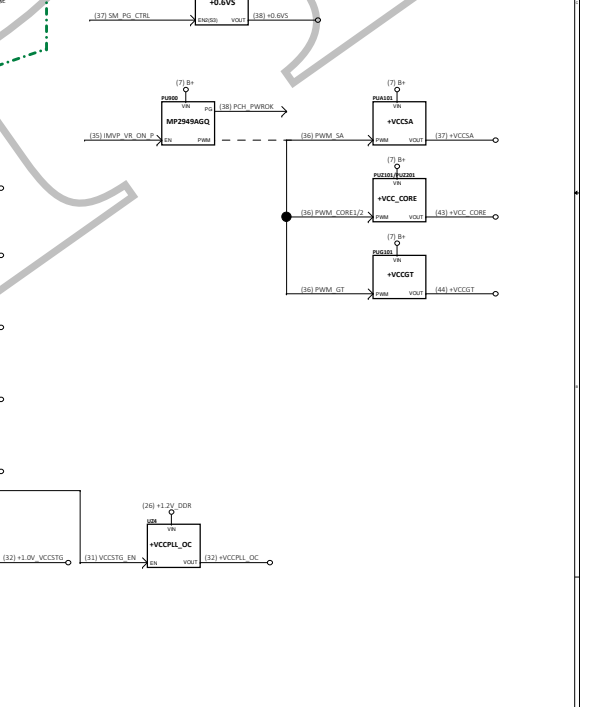
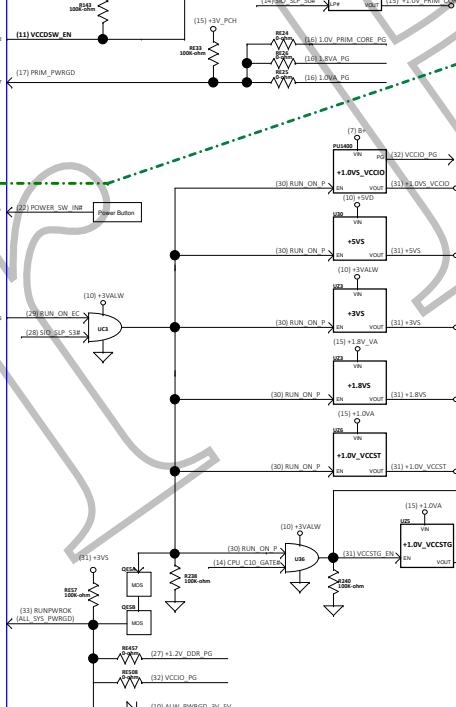


Compal Electronics, Inc.

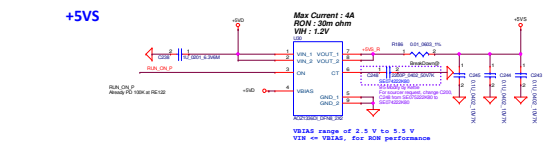
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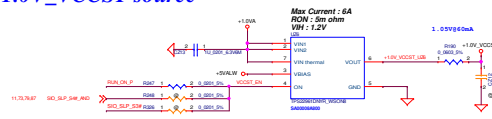
**S5 to S0
(22)~(42)**



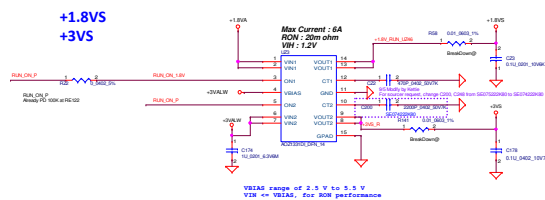
+5VS



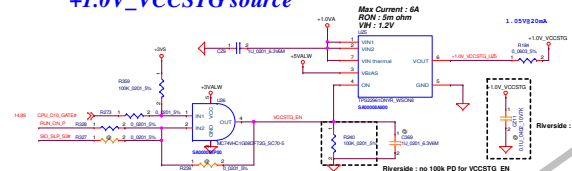
+1.0V_VCCST source



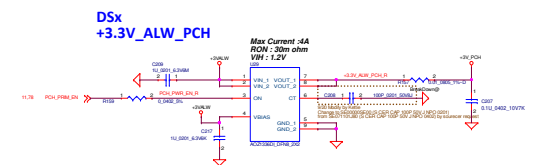
+1.8VS
+3VS



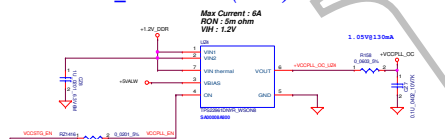
+1.0V_VCCSTG source



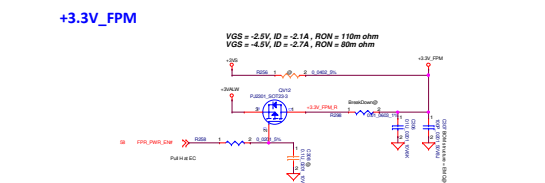
D5x
+3.3V_ALW_PCH



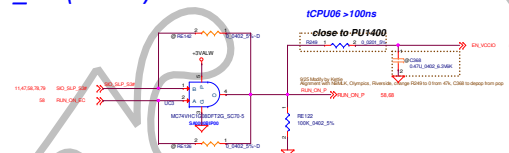
+VCCPLL_OC source (1.2V)



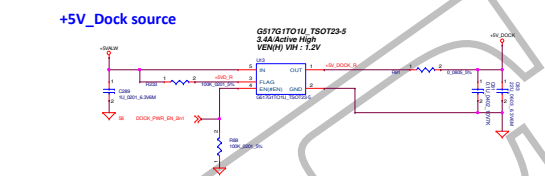
+3.3V_FPM



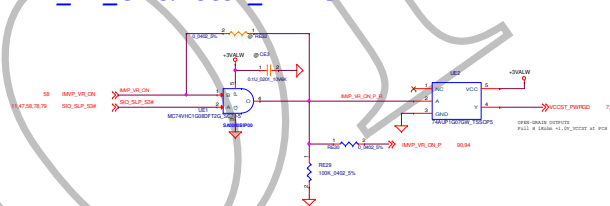
RUN_ON(VS EN)



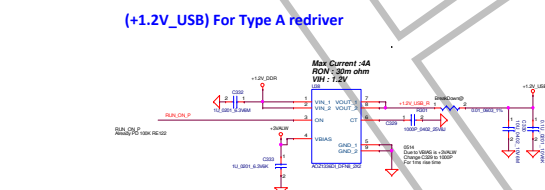
+5V_Dock source



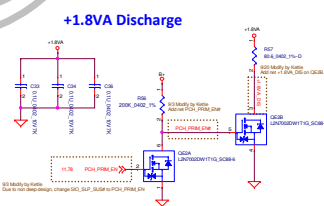
IMVP_VR_ON&VCCST_PWRGD



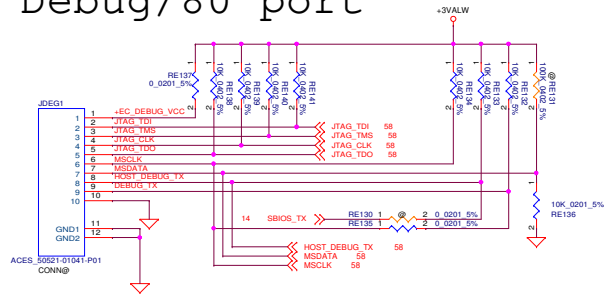
(+1.2V_USB) For Type A redriver



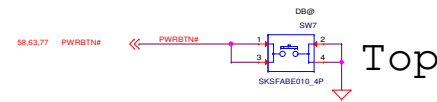
+1.8VA Discharge



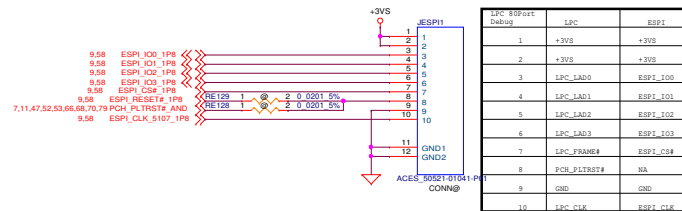
EC UART Debug/80 port



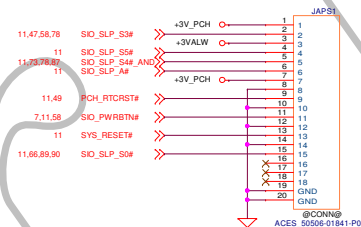
Test Power Button



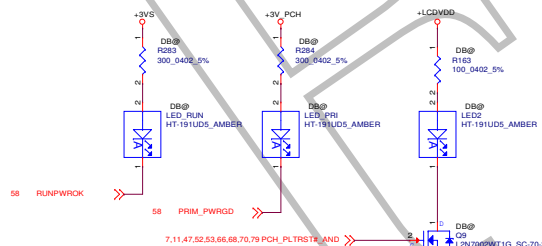
ESPI BIOS debug

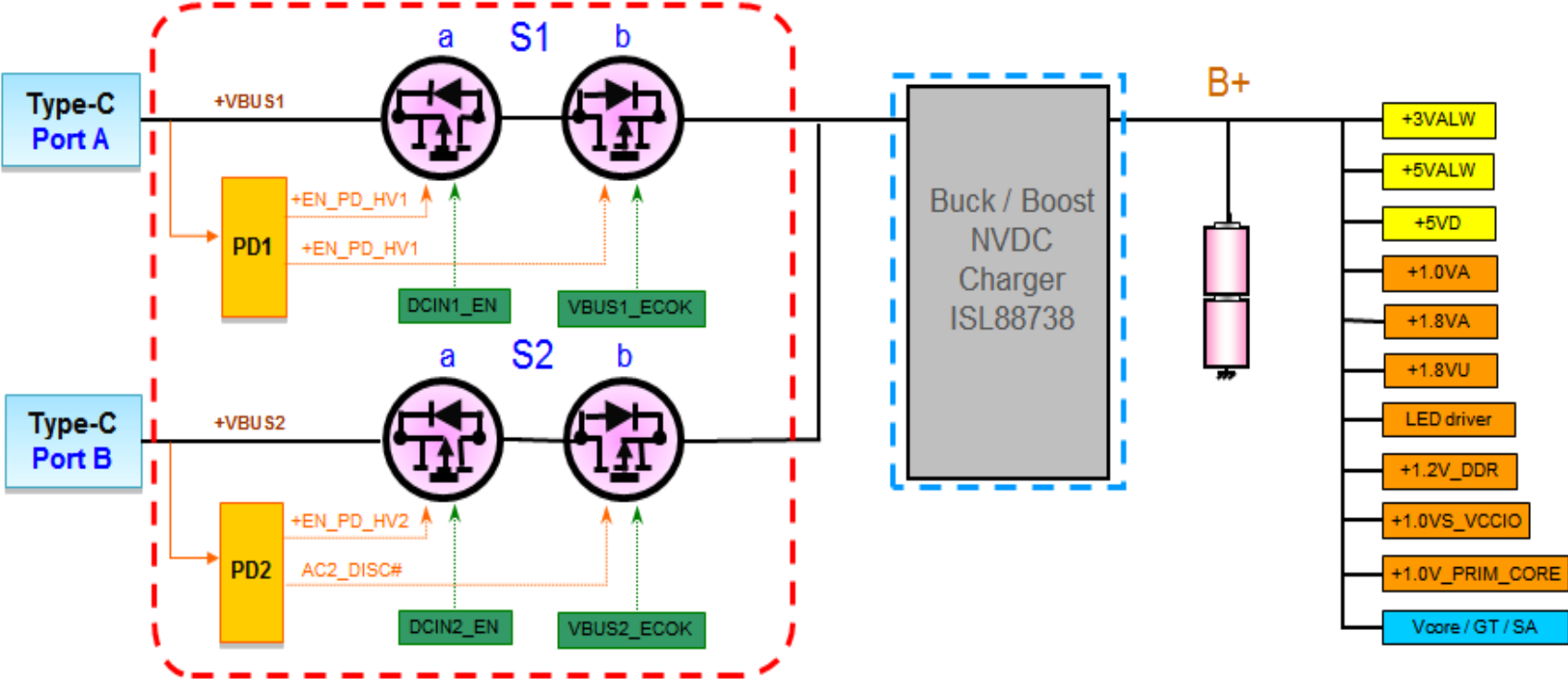


APS CONN



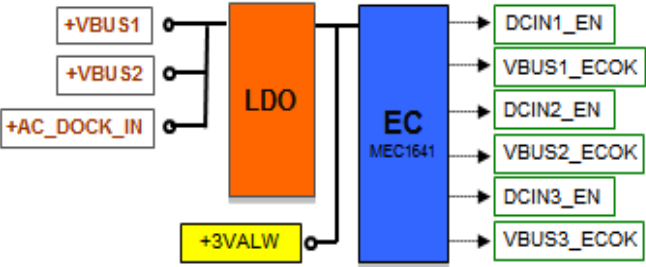
DEBUG LED





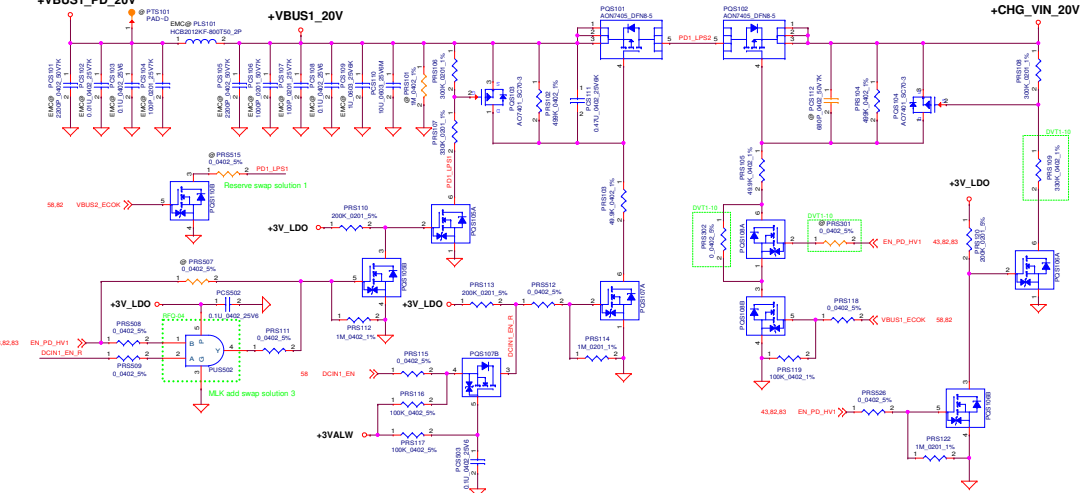
Tablet

--- Power Path Loop
--- Buck-Boost Charger

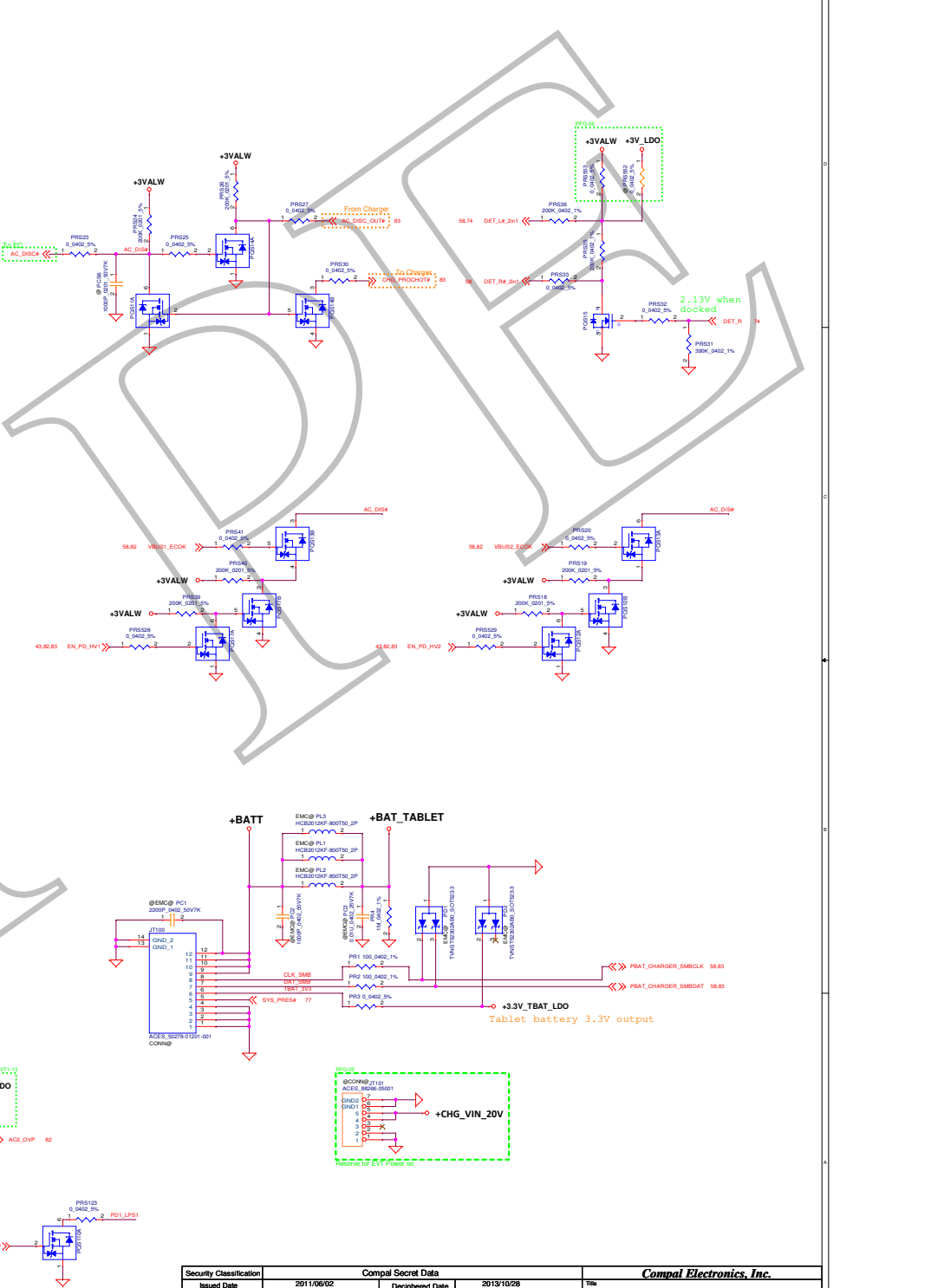
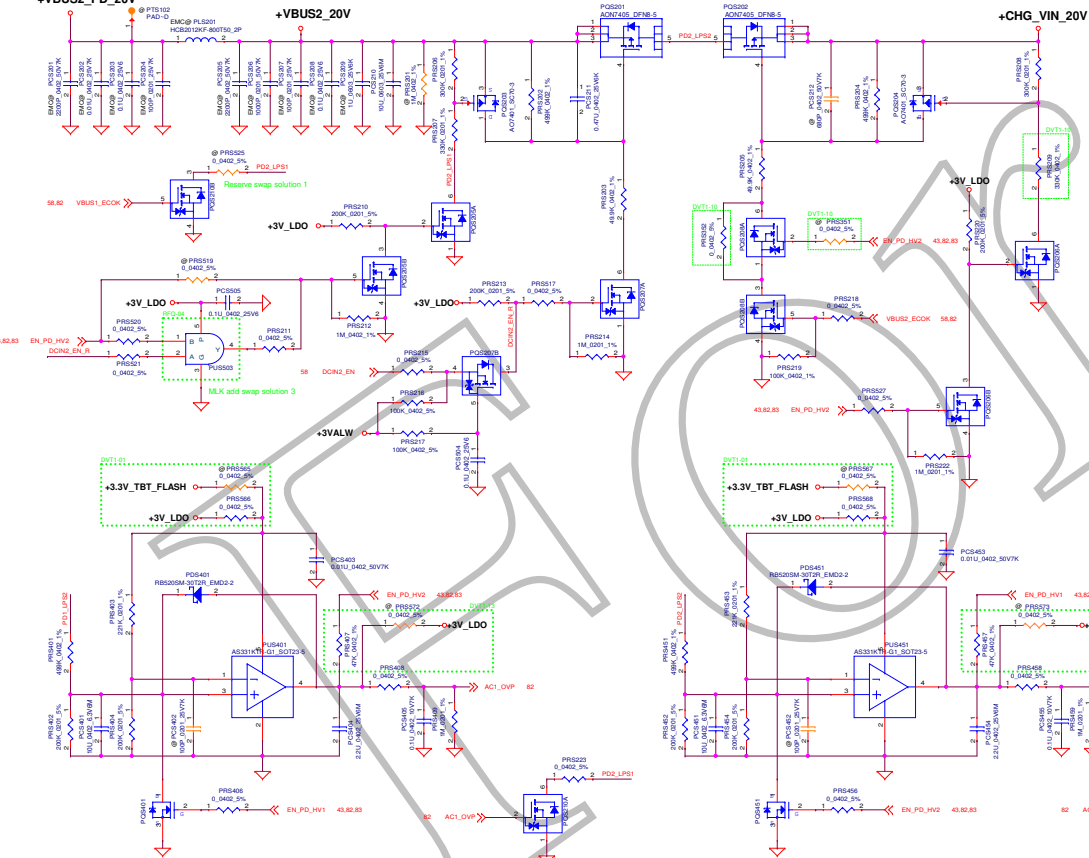


Function feild:
Rest of support elements (37.1), EMC Part (47.1)

Type C adapter input_1

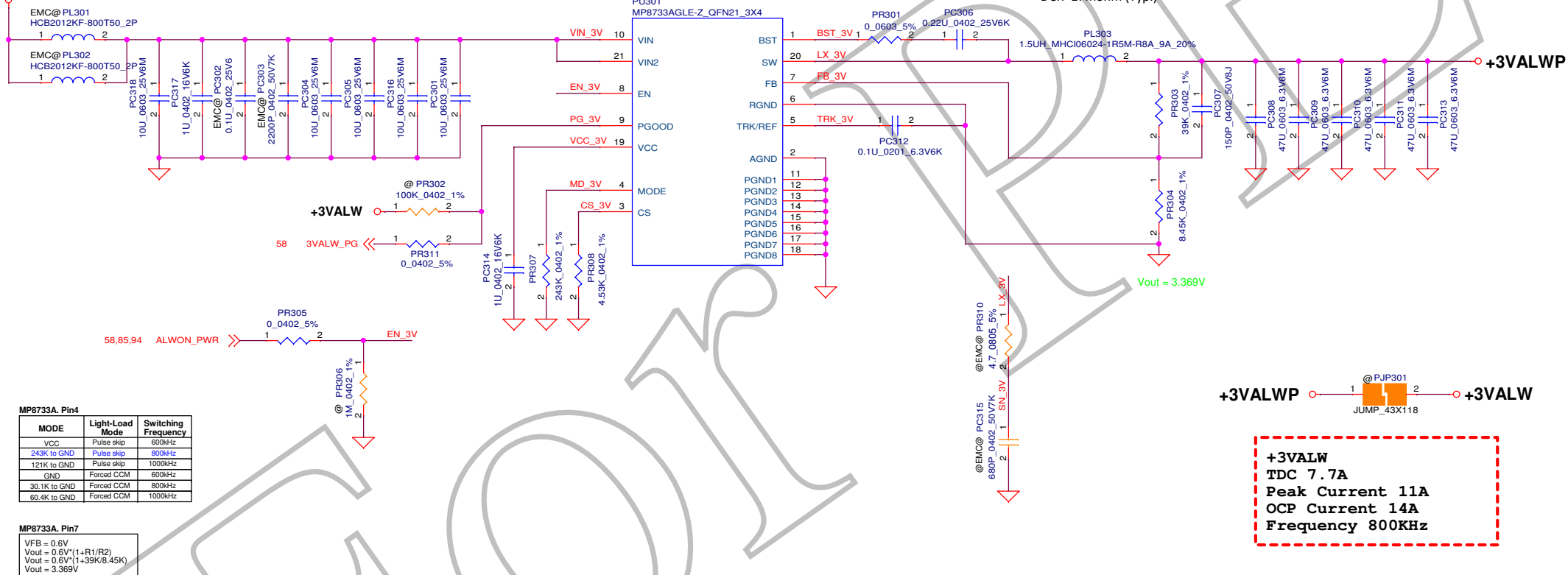


Type C adapter input_2



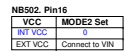
+3VALW controller(35.1), Support component(35.2)

B+



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VR_B+

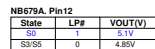


CLM	Resistor to GND
7A	0
10A	90K
13A	150K
16.5A	>230K or float

State	VOUT	Fs	Resistor to GND
M1	V<3V	700kHz	0
M2	V<3V	1000kHz	90K
M3	V>=3V	1000kHz	150K
M4	V>=3V	700kHz	>230K or float

NB502. Pin13

$VREF = 1.8V$ $R1 = 1/[VREF/(VOUT - VREF) - R2/R4] \cdot R2$ $VOUT = [R1 \cdot R4 \cdot VREF / (R4 \cdot R2 + R1 \cdot R2)] + VREF$ $VOUT = 5.09V$
--

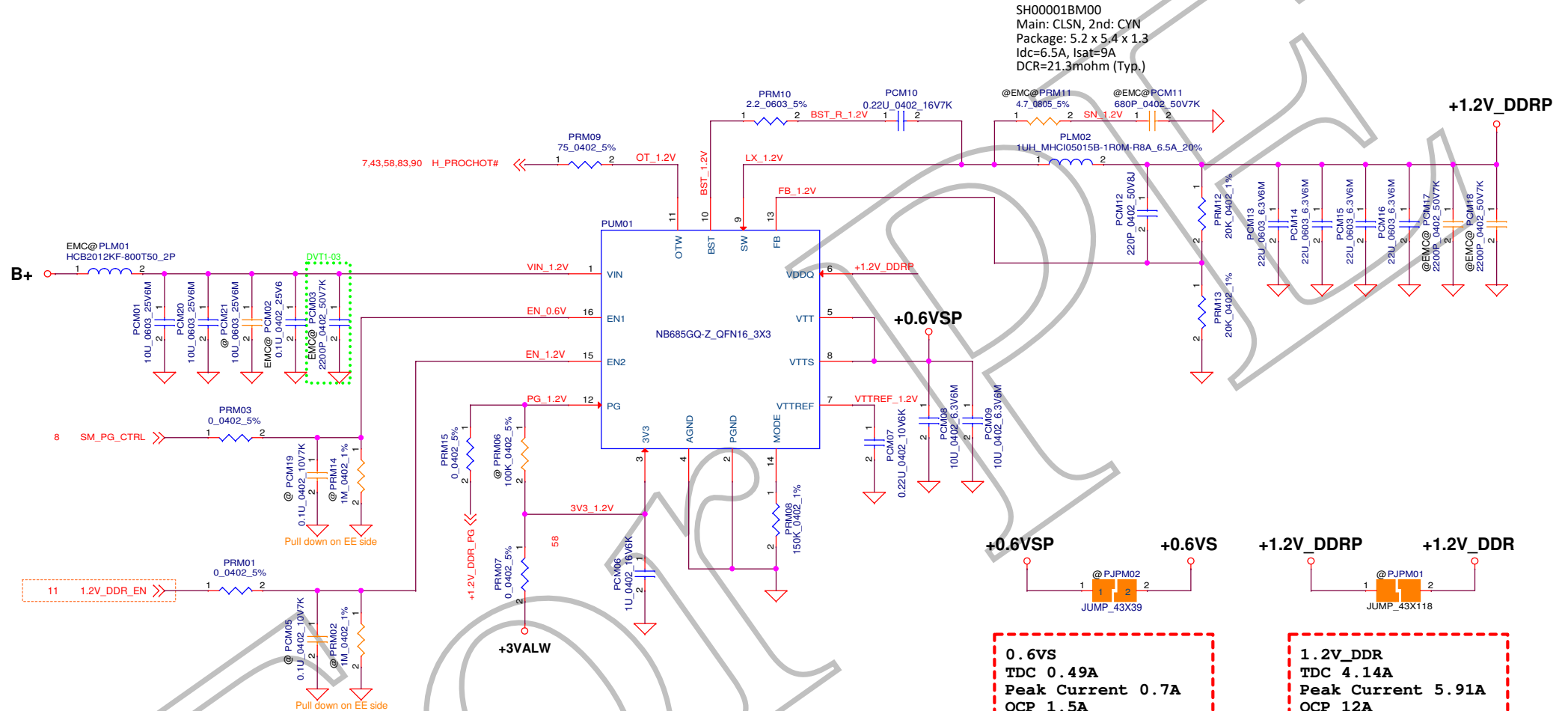


State	LP#	VOUT(V)
S0	1	5.1V
S3/S5	0	4.85V

+5VDP  **+5VD**

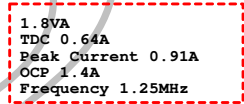
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title			
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+1.2V_DDR controller(35.3), Support component(35.4)

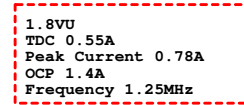


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+1.8VS controller(35.13), Support component(35.14)



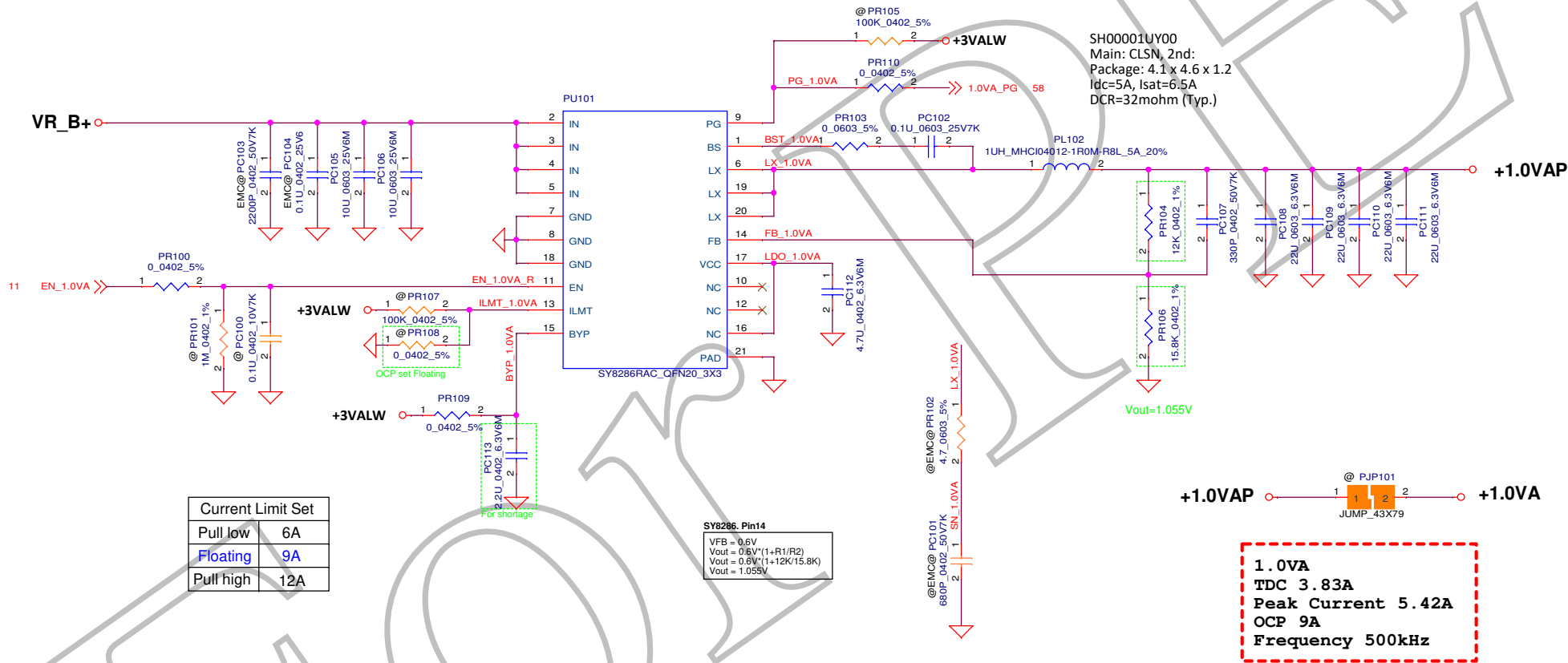
+1.8VU controller(35.13), Support component(35.14)



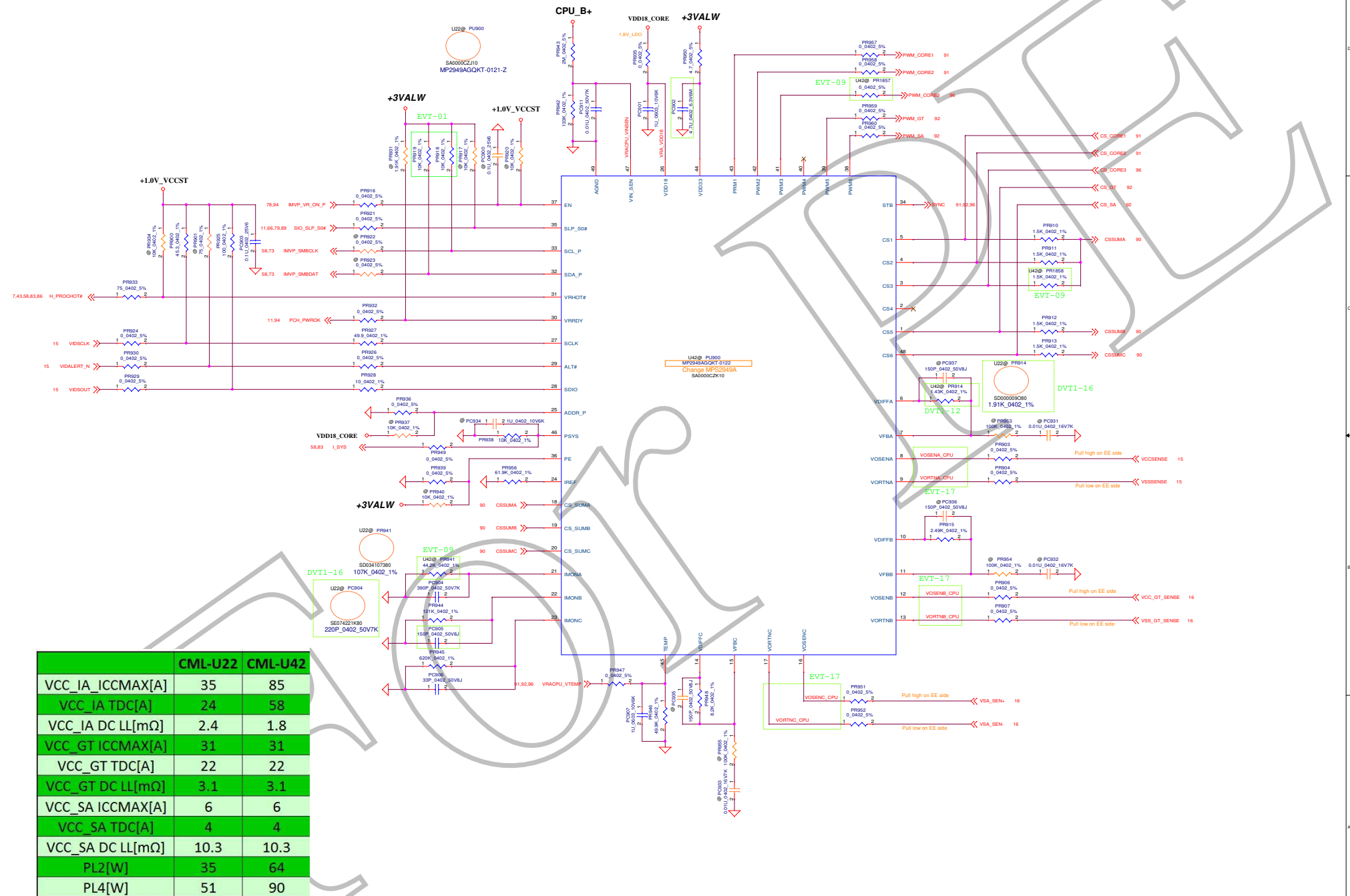
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Module Design

+1.0VA controller(35.5), Support component(35.6)

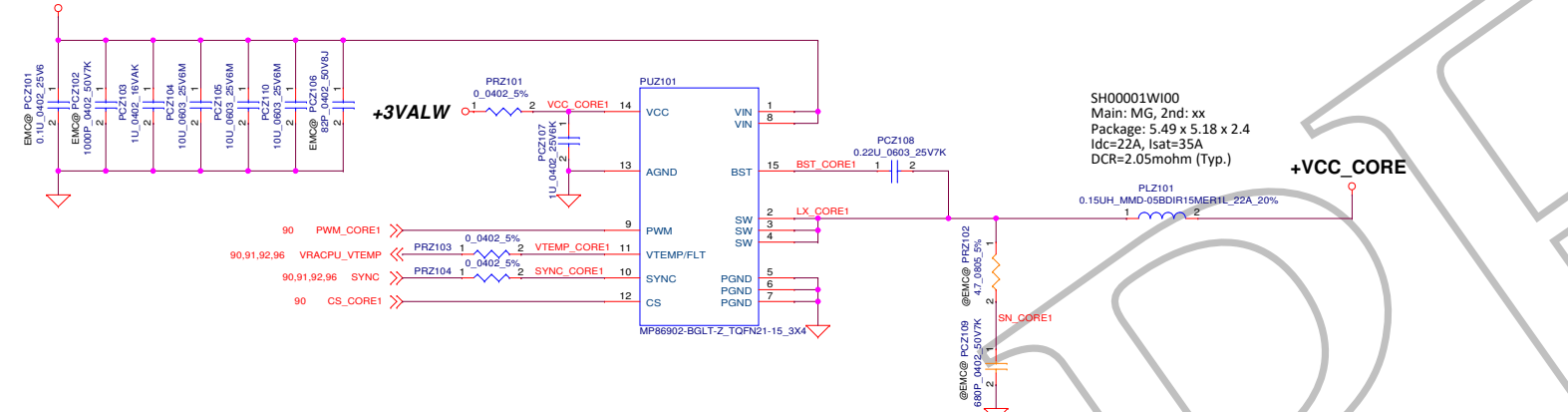


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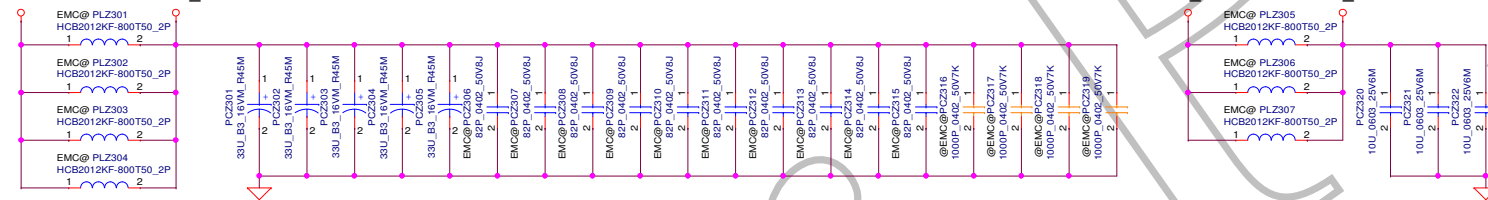
VCC_CORE Dr. MOS (36.2), Support component(36.3)

CPU_B+

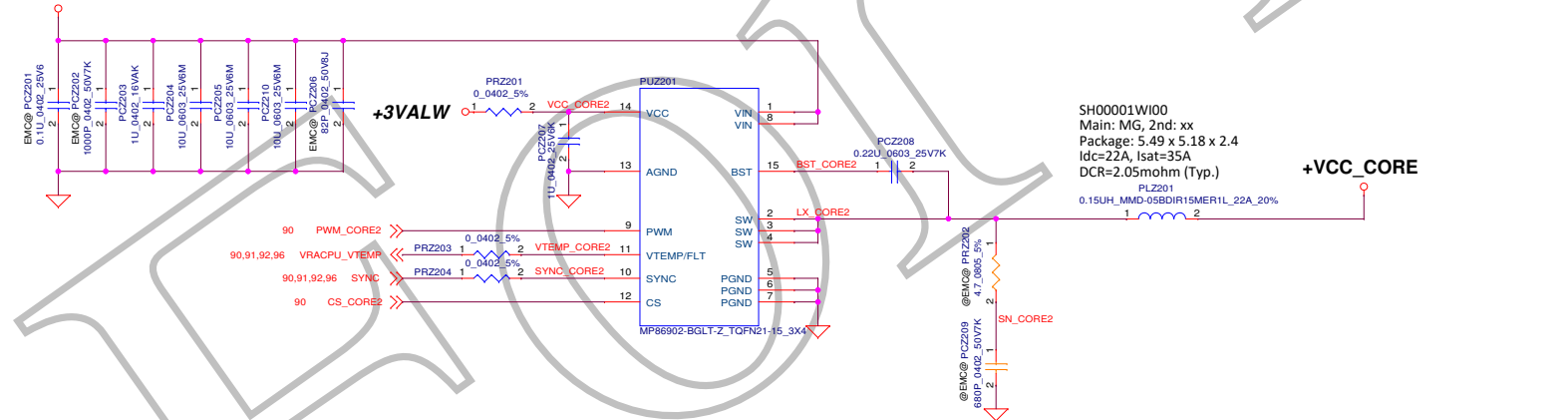


B+

CPU_B+



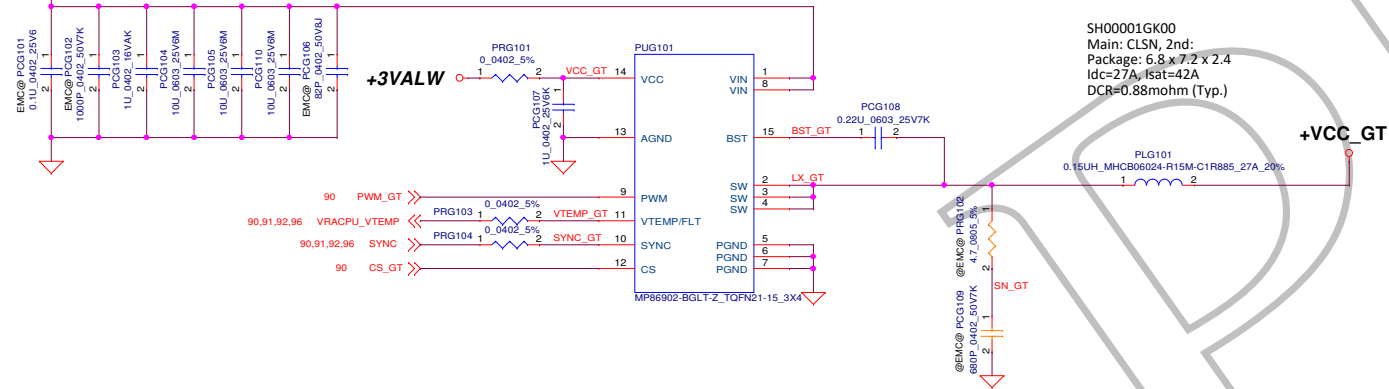
CPU_B+



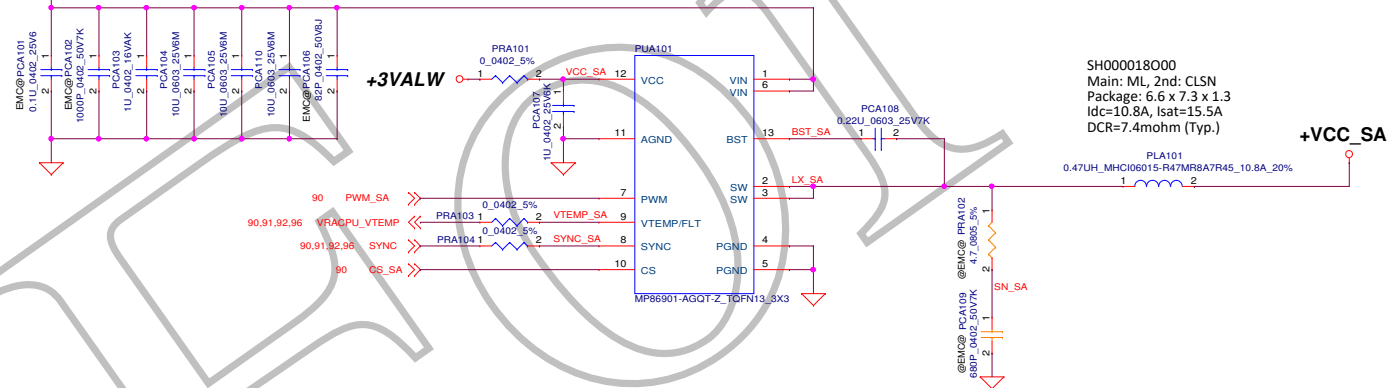
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VCC_GT/SA Dr. MOS (36.2), Support component(36.3)

CPU_B+



CPU_B+



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VCC_CORE output cap(36.4), VCC_GT output cap(36.5), VCC_SA output cap(36.6)

+VCC_CORE

Cap	SIZE	POP	INC
330uF	B2	3	1
47uF	0603	9	15
22uF	0603	4	0
10uF	0402	0	0
1uF	0201	14	0

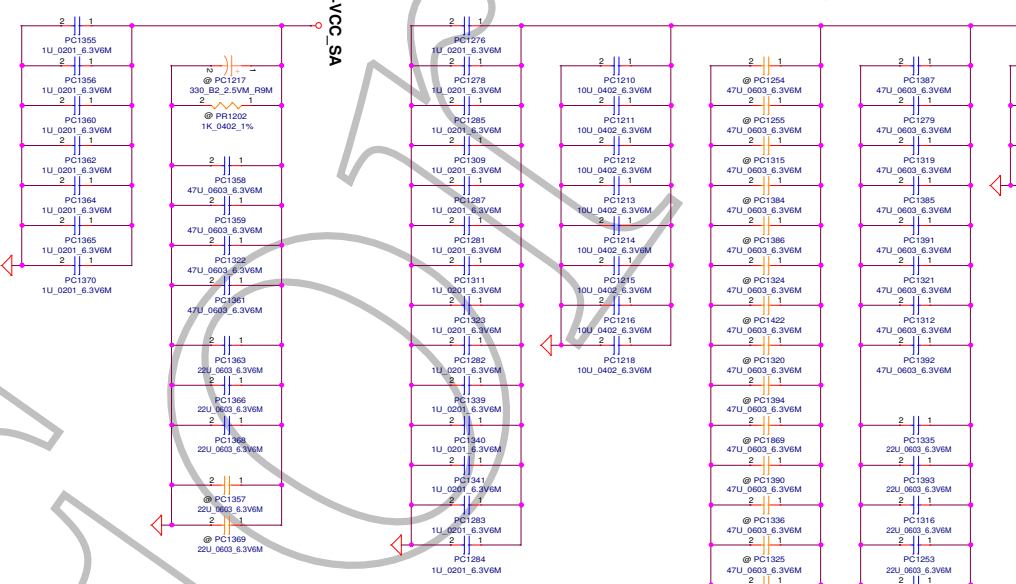


+VCC_GT

Cap	SIZE	POP	INC
330uF	B2	2	1
47uF	0603	8	17
22uF	0603	7	0
10uF	0402	0	0
1uF	0201	14	0

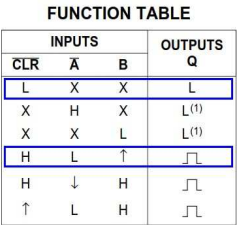
+VCC_SA




Cap	SIZE	POP	INC
330uF	B2	0	1
47uF	0603	4	0
22uF	0603	3	2
1uF	0201	7	0



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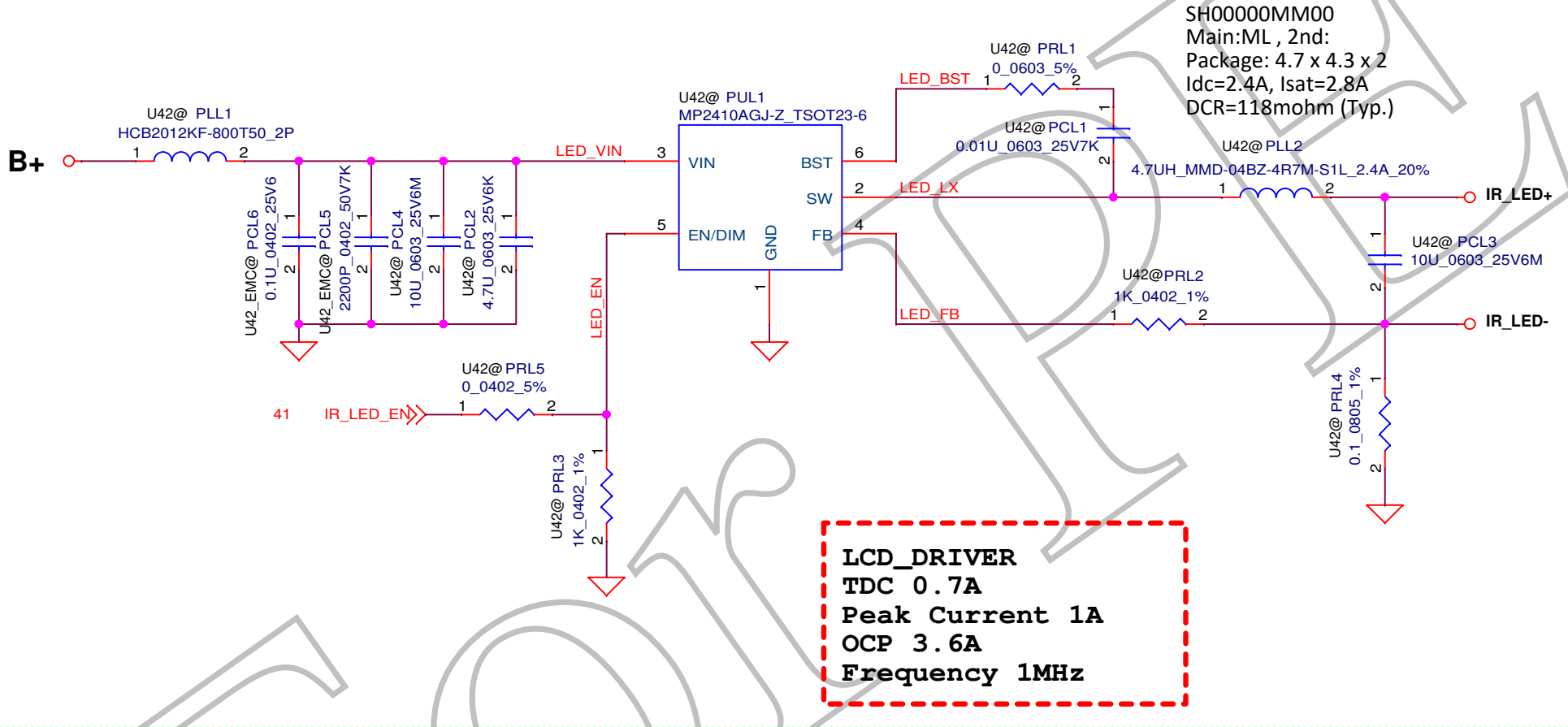
Vcore OVP



INPUTS			OUTPUTS Q
CLR	\bar{A}	B	
L	X	X	L
X	H	X	L ⁽¹⁾
X	X	L	L ⁽¹⁾
H	L	\uparrow	
H	\downarrow	H	
\uparrow	L	H	

LED driver controller(42.1), Support component(42.2)

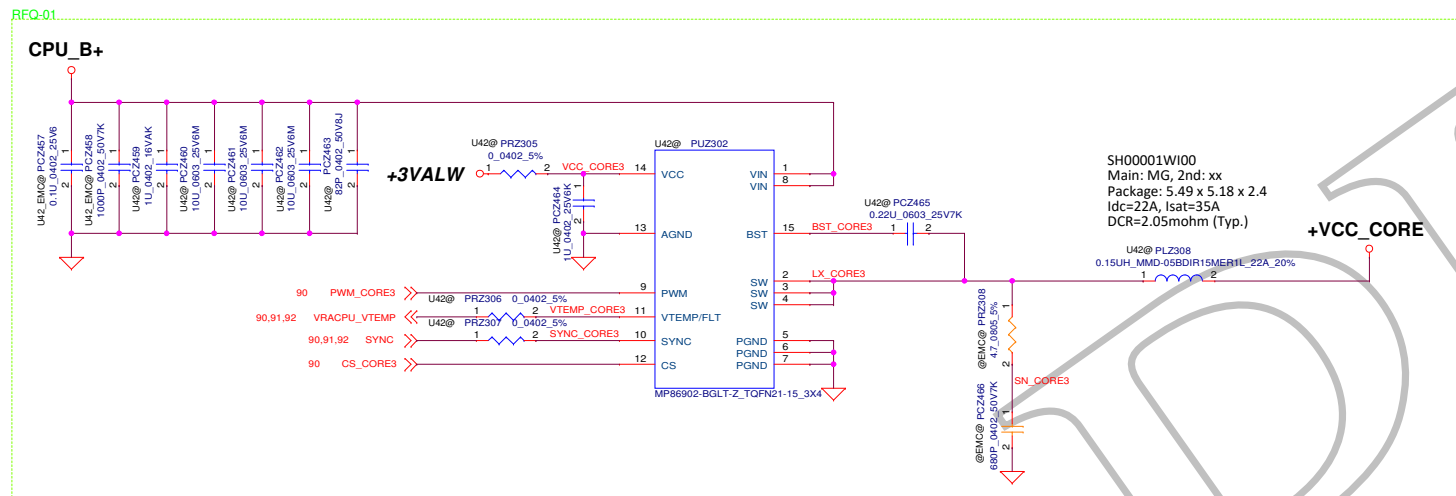
RFQ-01



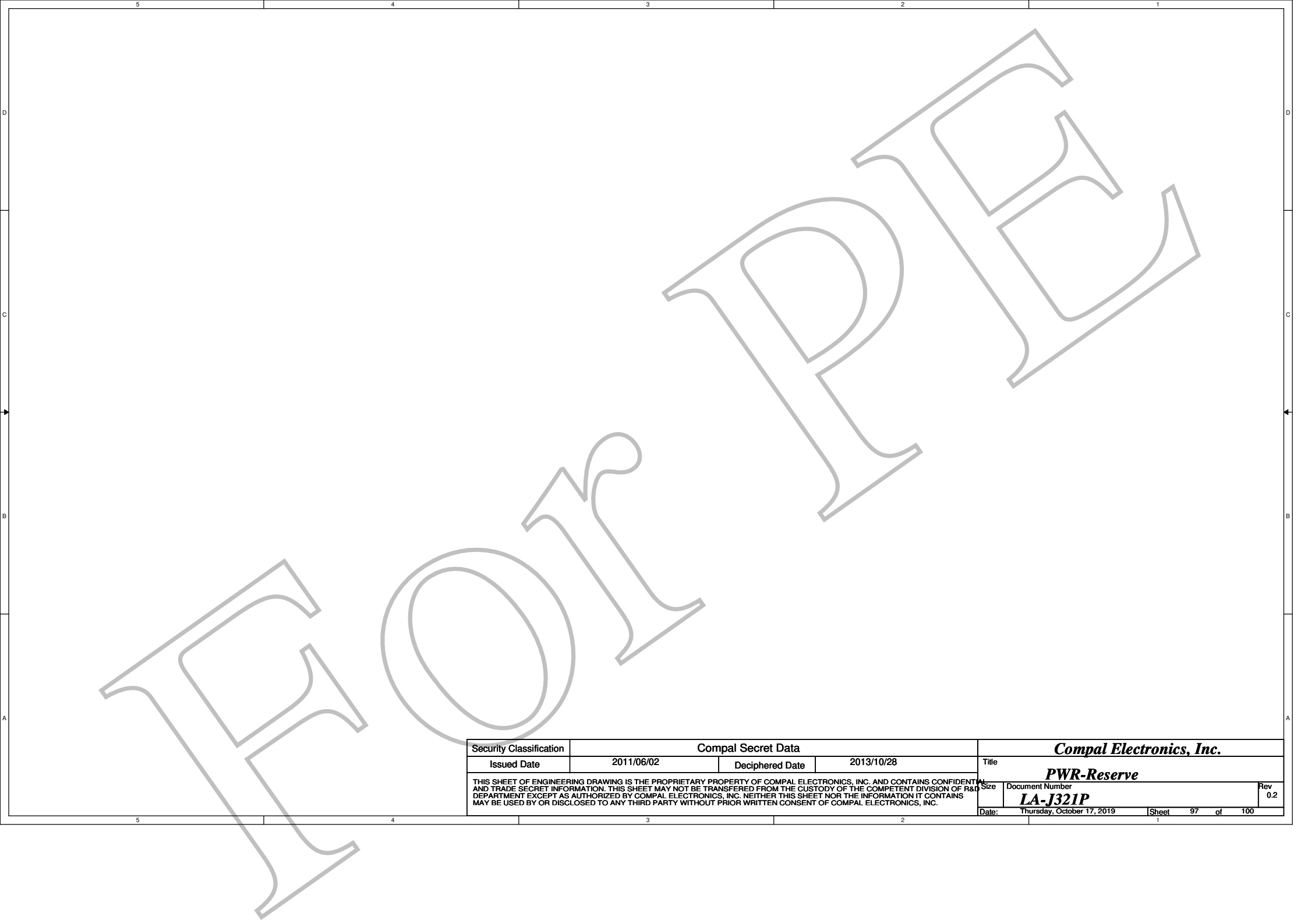
LCD_DRIVER
TDC 0.7A
Peak Current 1A
OCP 3.6A
Frequency 1MHz

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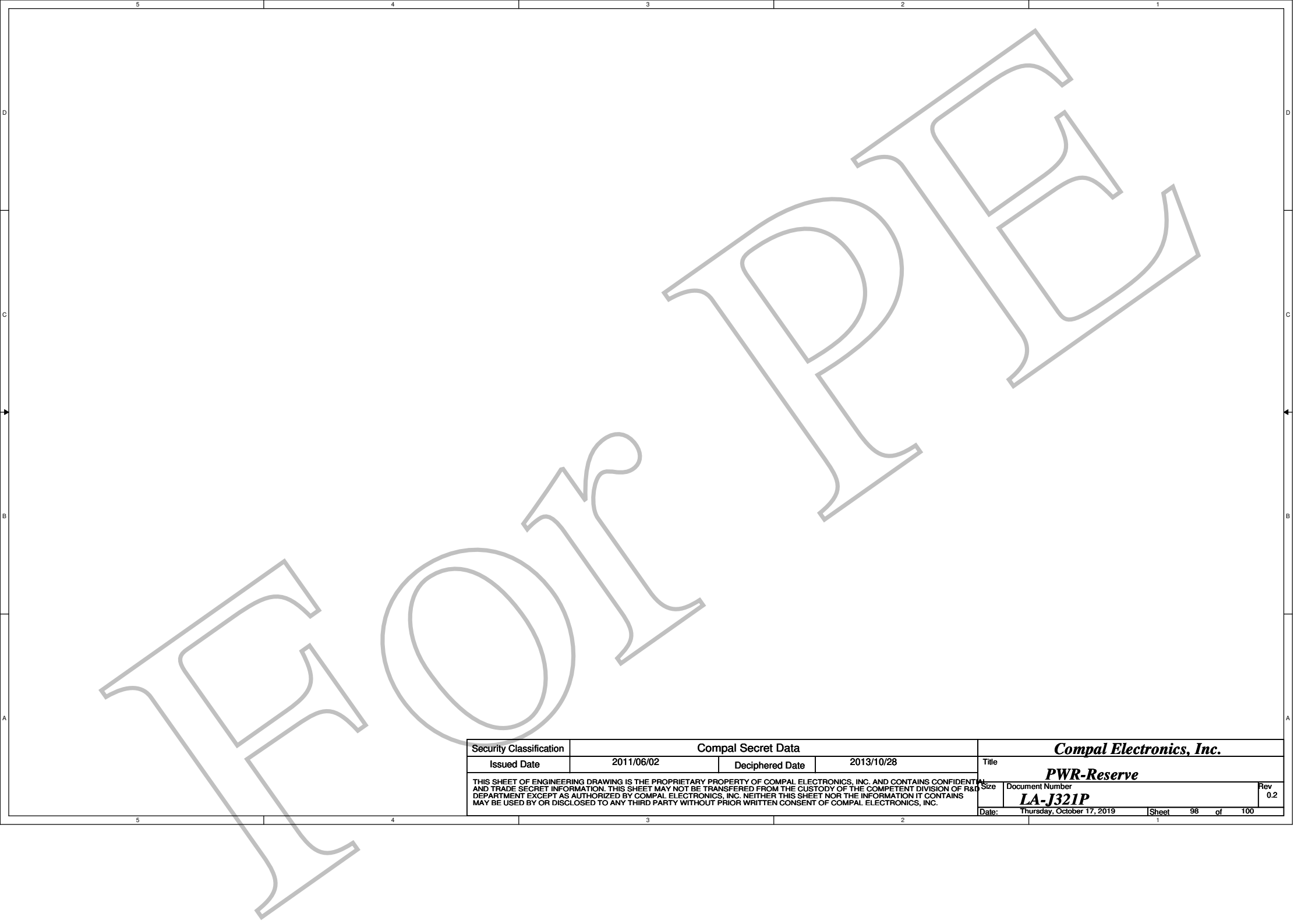
VCC_CORE Dr. MOS (36.2), Support component(36.3)



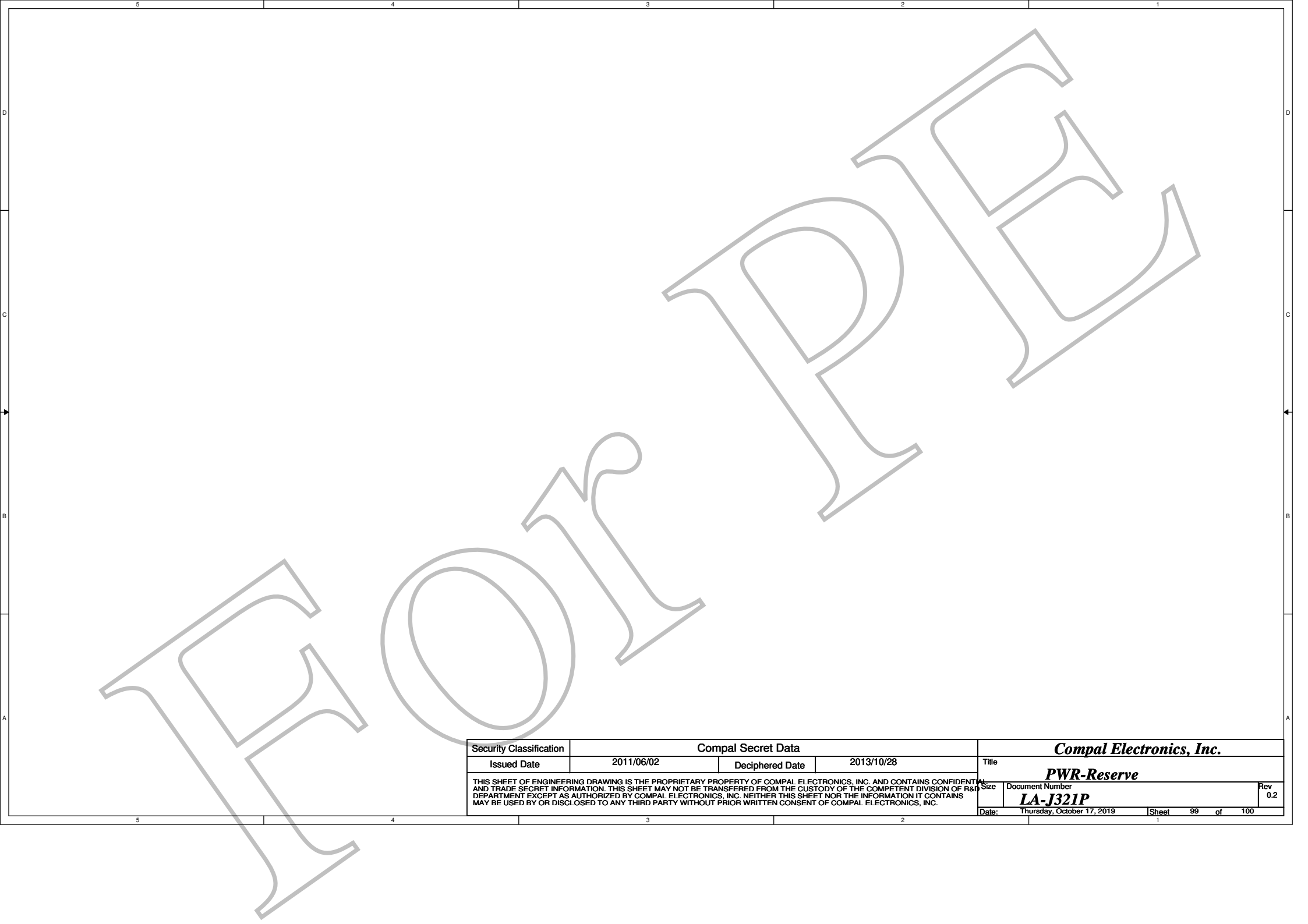
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								Size	Document Number		Rev		
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								Date:	Thursday, October 17, 2019		Sheet	96	of



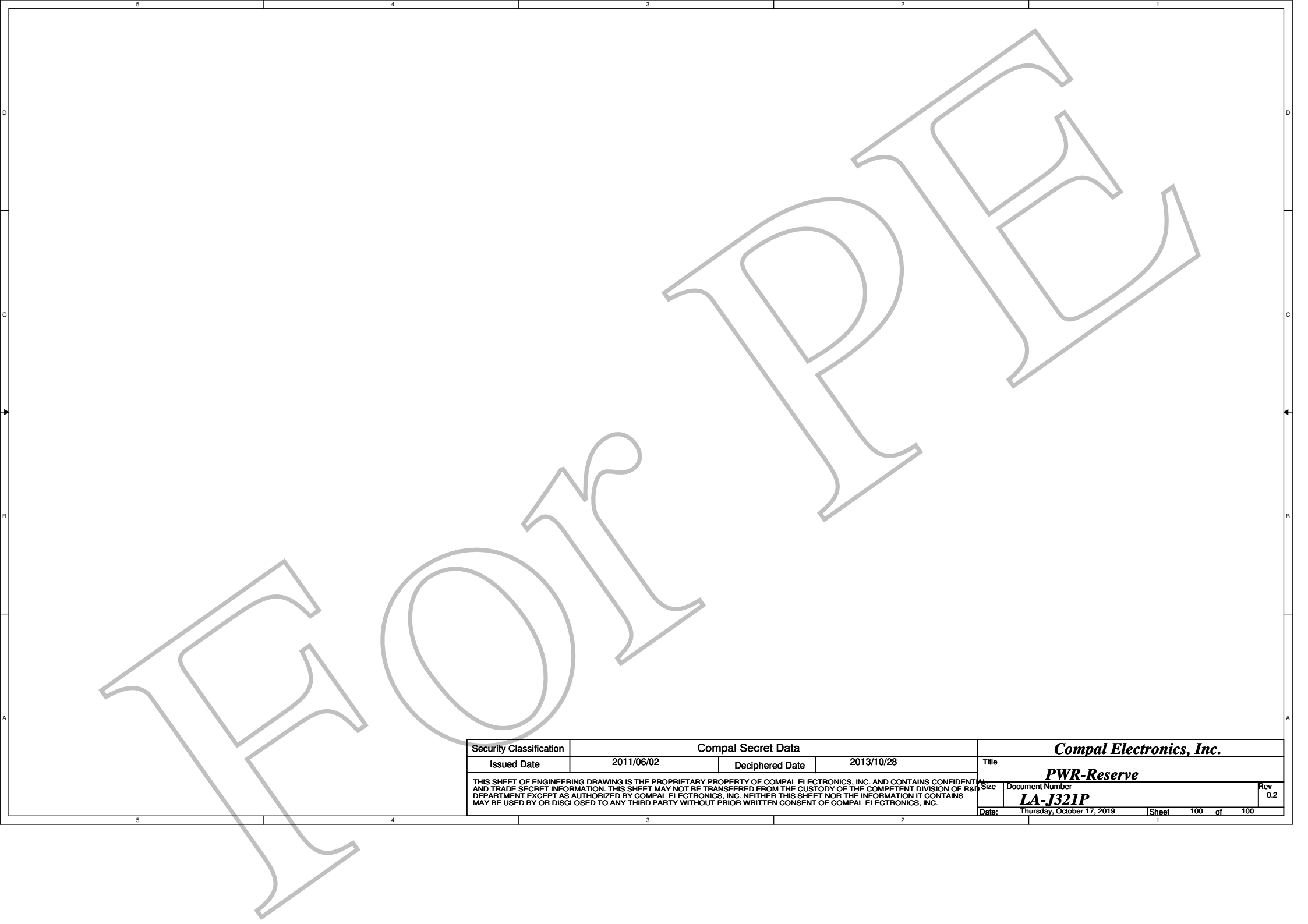
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								Date: Thursday, October 17, 2019		Sheet 100 of 100