

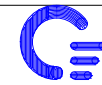
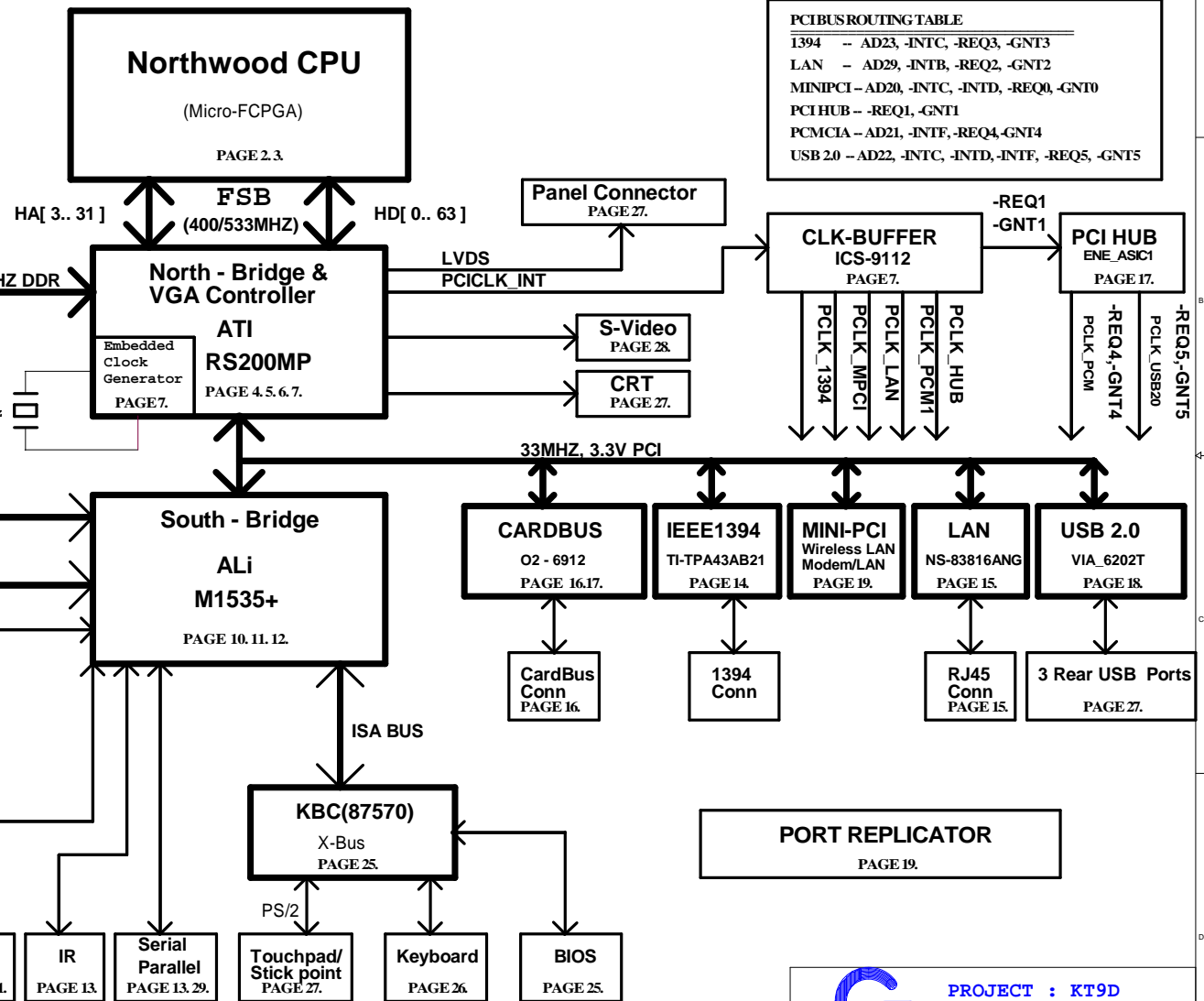
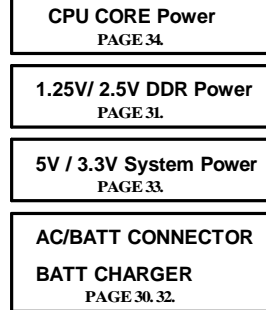
# KT9I

P/N: DAKT9DMB6A0

## STACK LAYERS

L1 : TOP  
L2 : VCC  
L3 : IN1 ( Hig Speed )  
L4 : GND  
L5 : IN2 ( High Speed )  
L6 : BOT

## Power - Source Control



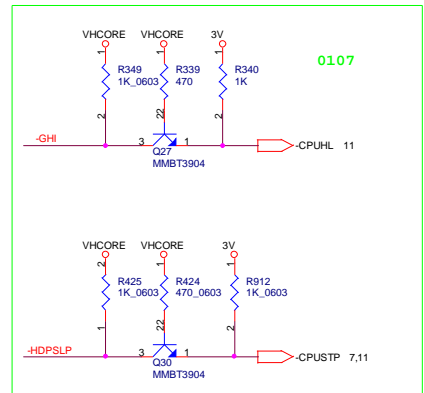
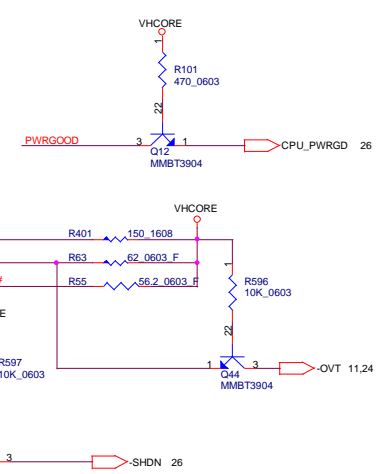
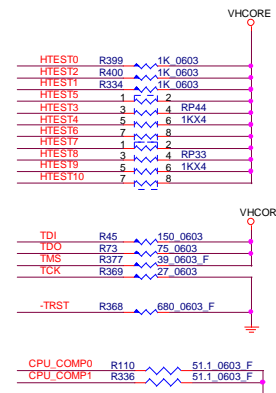
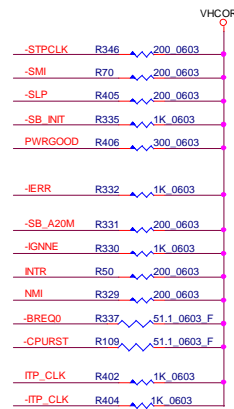
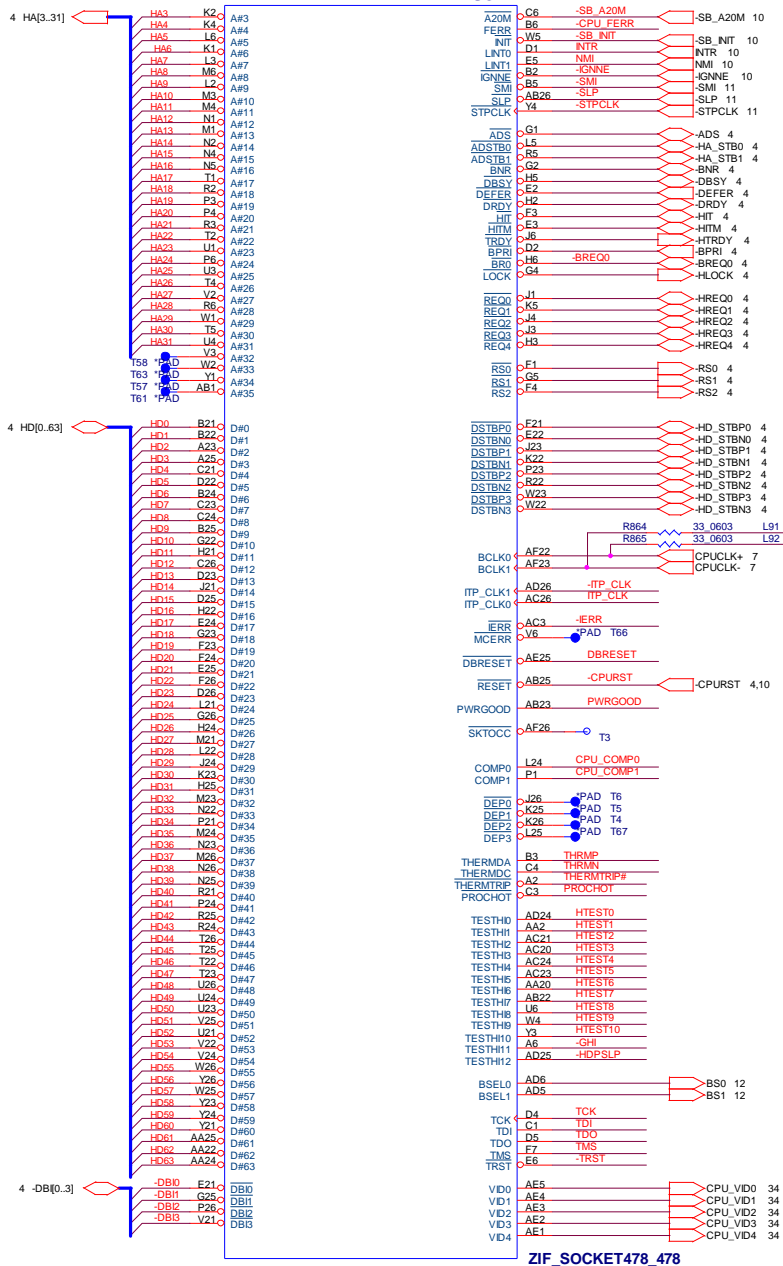
PROJECT : KT9D  
Quanta Computer Inc.

Size: Document Number  
BLOCK DIAGRAM  
Date: Monday, July 14, 2003 Sheet 1 of 34 Rev 1A

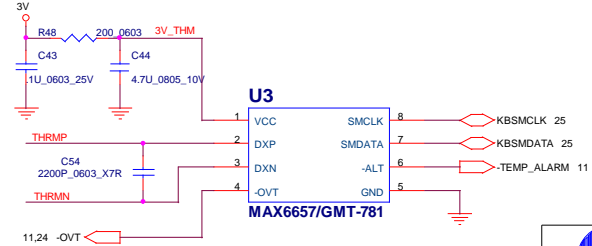
# NORTHWOOD CPU -A

02

## U8A



## H/W MONITOR



**PROJECT : KT9D**

**Quanta Computer Inc.**

Size: Document Number

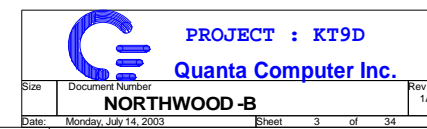
Date: Monday, July 14, 2003

**NORTHWOOD CPU -A**

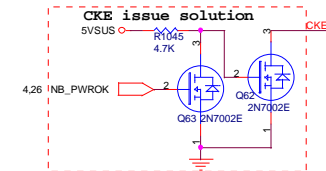
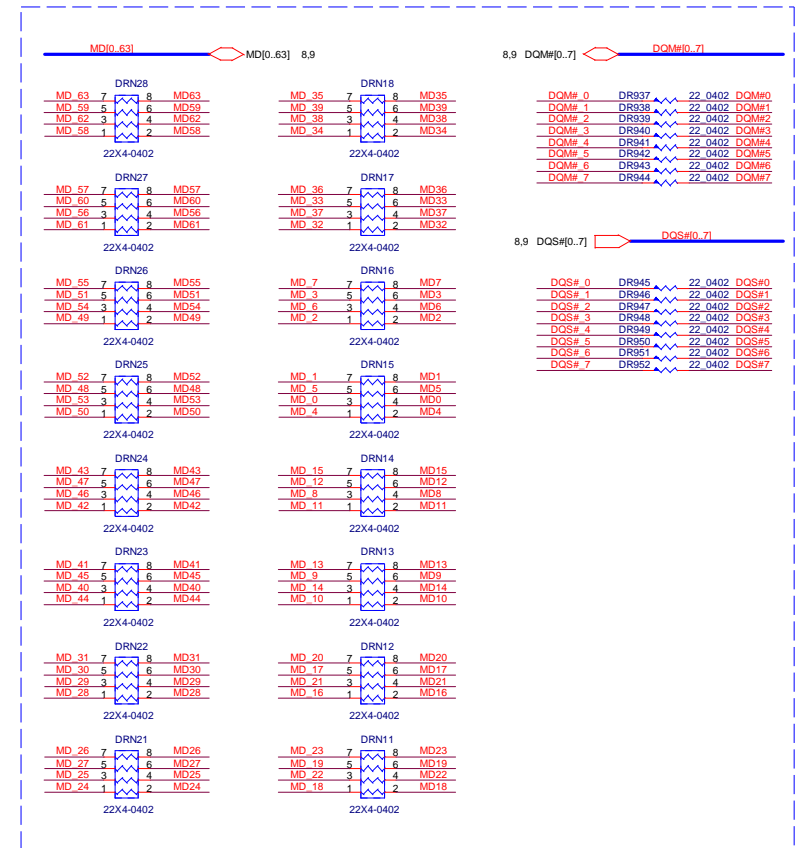
Sheet 2 of 34

Rev 1A

## 03





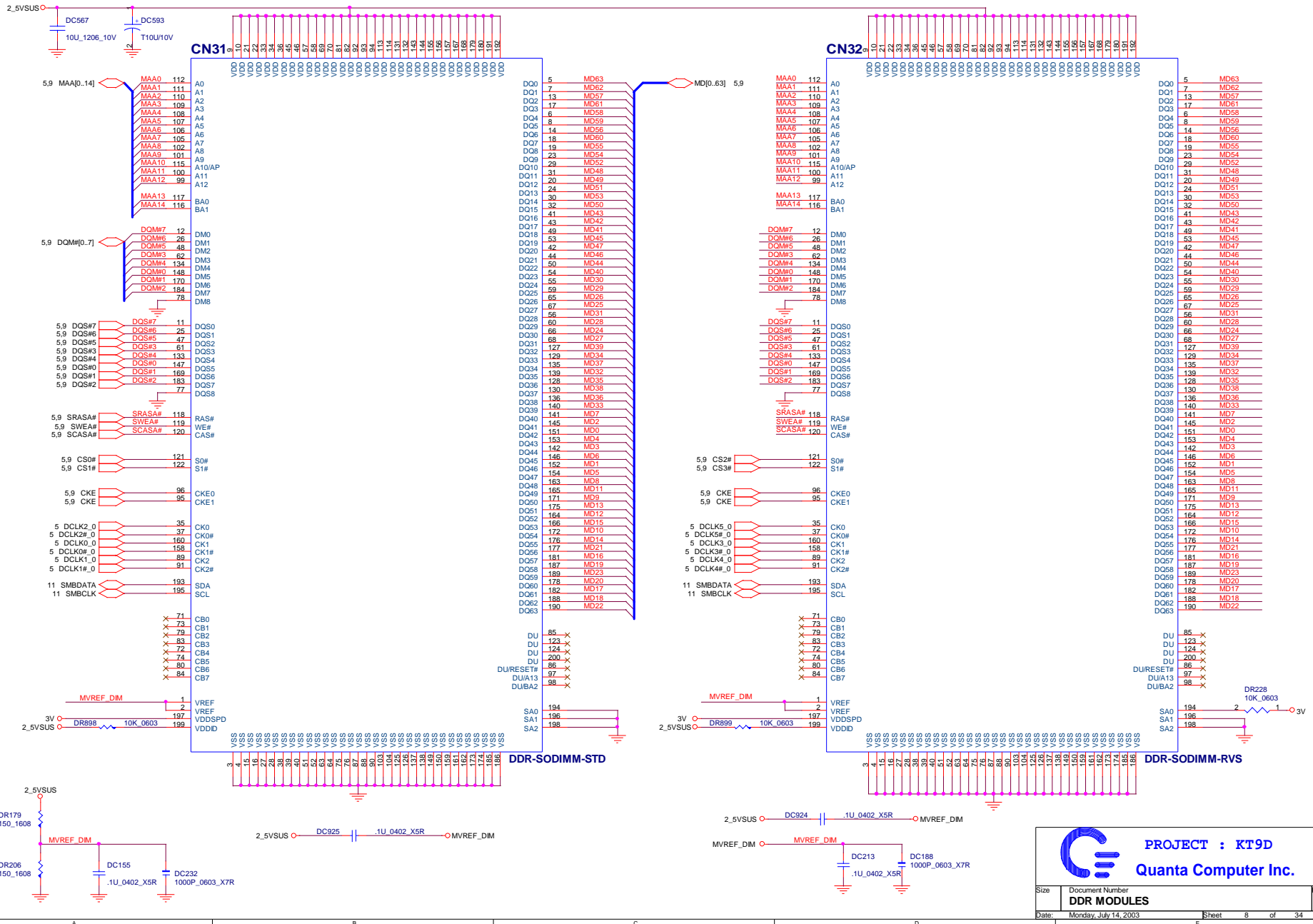


## 06









**PROJECT : KT9D**  
**Quanta Computer Inc.**

Size: Document Number  
**DDR MODULES**

Date: Monday, July 14, 2003 Sheet 8 of 34 Rev 1A



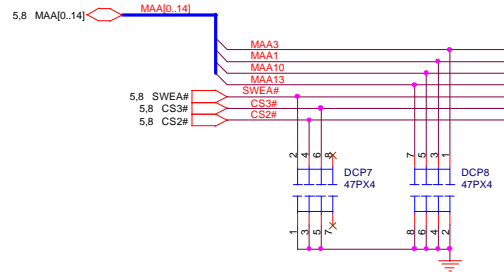
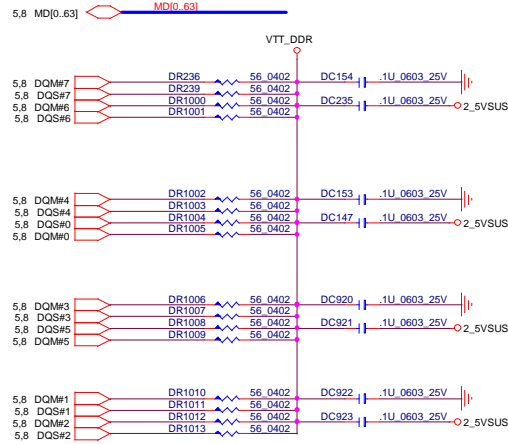
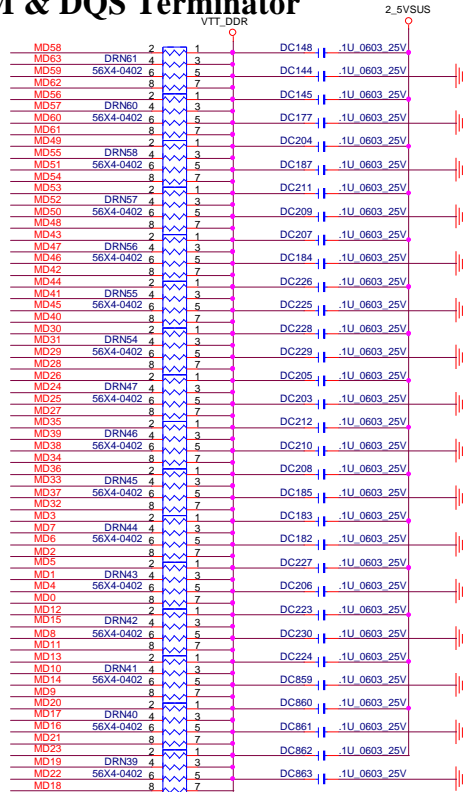
# DDR TERMINATOR



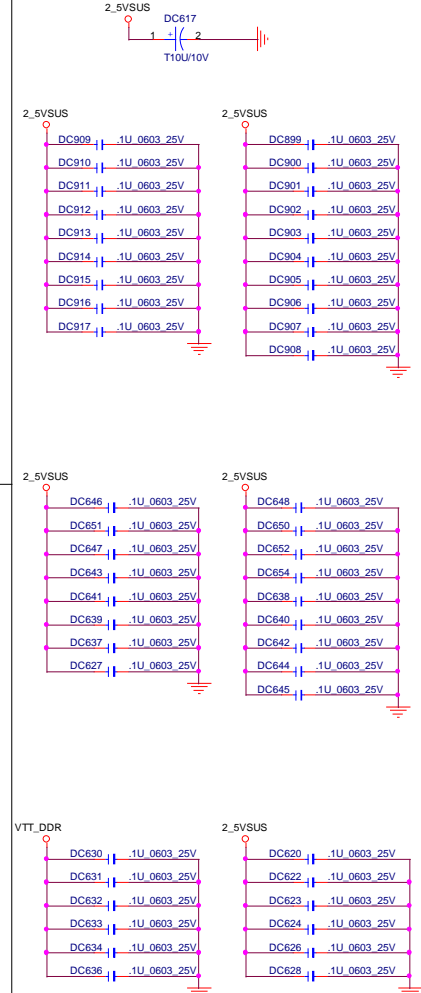
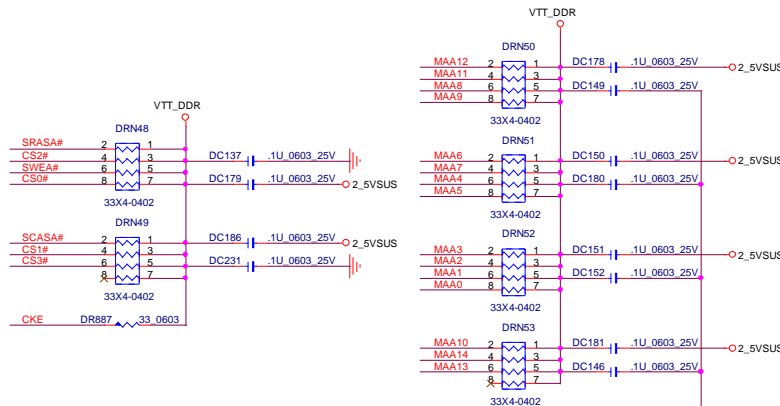
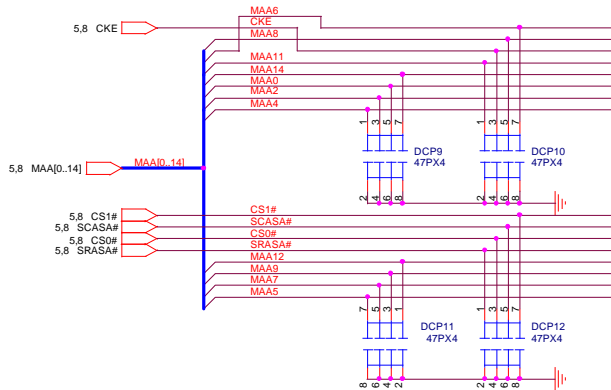
Could swap pin for layout .

09

## MD & DQM & DQS Terminator



## MA Terminator

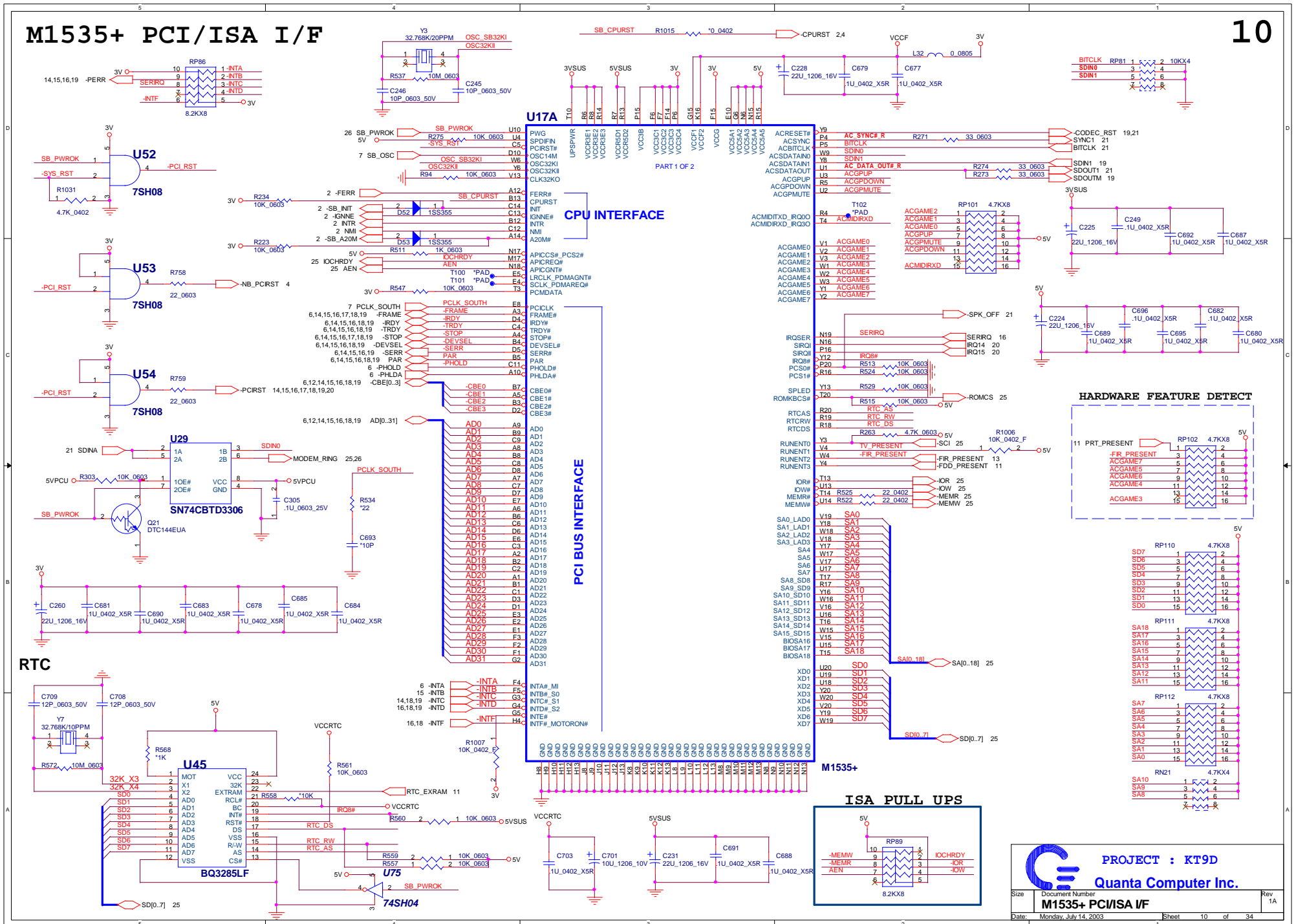


PROJECT : KT9D  
Quanta Computer Inc.

Size	Document Number	Rev
	DDR TERMINATOR	1A
Date:	Monday, July 14, 2003	Sheet 9 of 34

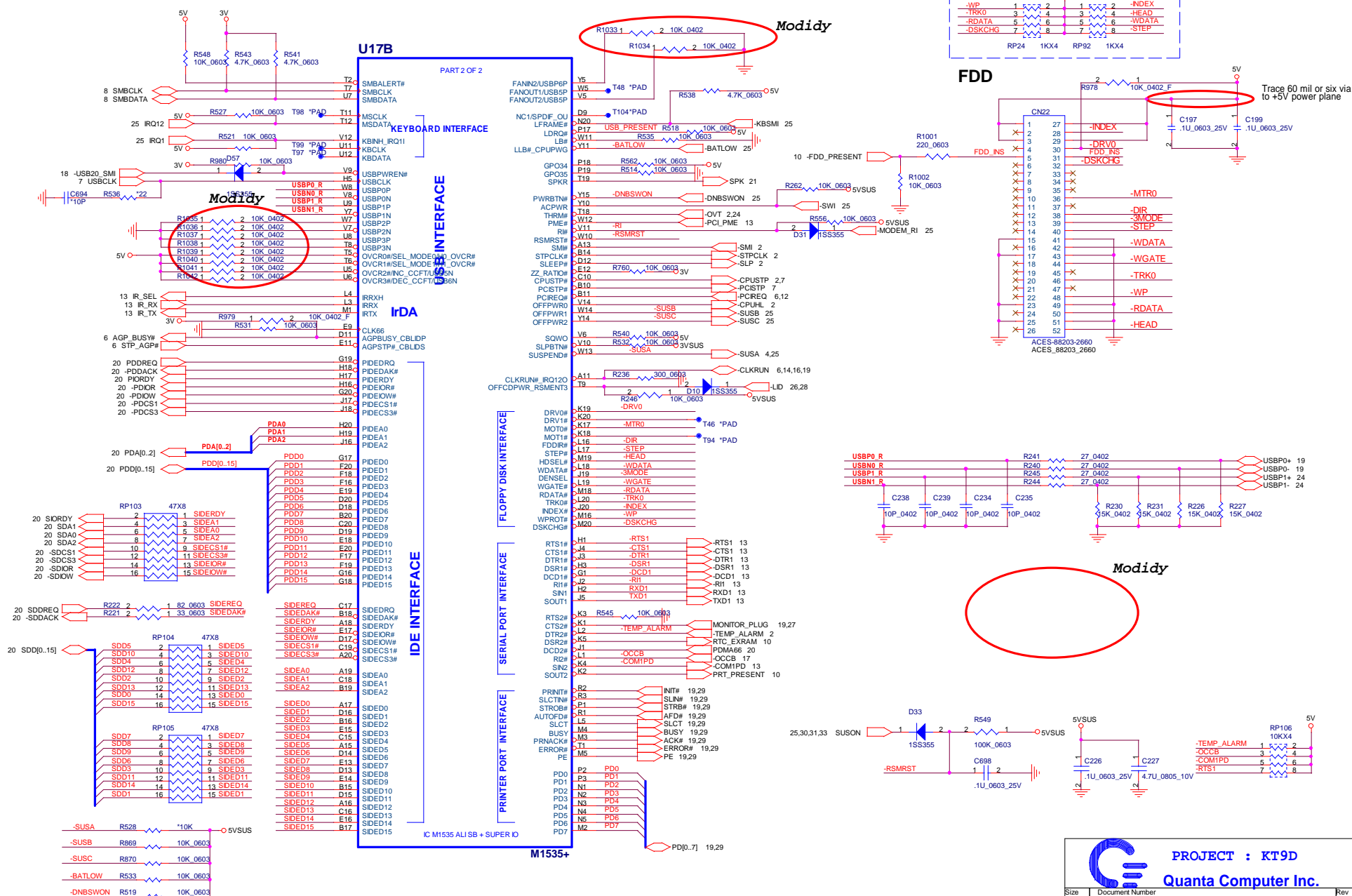
# M1535+ PCI/ISA I/F

10



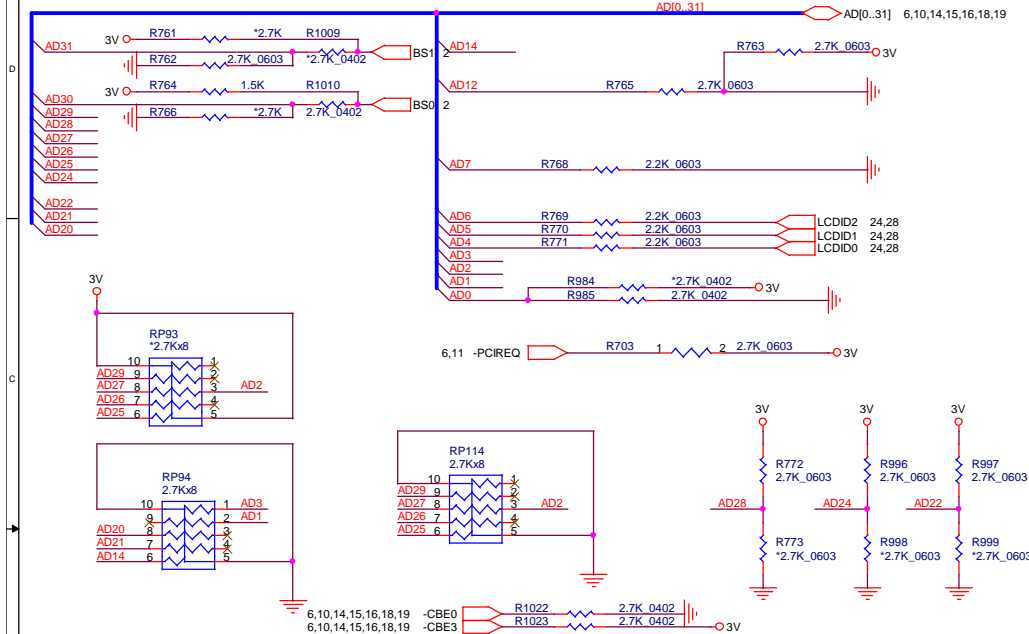
**PROJECT : KT9D**  
**Quanta Computer Inc.**  
 Size: 10 of 34  
 Date: Monday, July 14, 2003  
 Sheet: 10 of 34  
 Rev: 1A

## 11



# N.B & S.B H/W STRAPPING

## NORTH BRIDGE H/W STRAPPING



AD[31..30] : CLK SPEED DEFAULT: 00	00: 100 MHz 01: 133 MHz 10: 166MHz 11: 66 MHz	AD15 : RESERVED
AD29: RS200M FULL CONFIGURATION DEFAULT: 0	0: FULL CONFIGURATION 1: USES DEFAULT VALUES	AD14 : AGTL+ VDDQ DEFAULT: 0 0: 1.2V MOBILE PART 1: 1.7V DESKTOP PART
AD28: SPREAD SPECTRUM ENABLE DEFAULT: 0	0: DISABLE 1: ENABLE	AD13: RESERVED
AD27: MCERR OBSERVATION DEFAULT: 0	0: DISABLE 1: ENABLE	AD[12] : FLAT PANEL ID MSB
AD26: QUICK START SELECT DEFAULT: 0	0: DISABLE 1: ENABLE	AD10 : RESERVED
AD25: INIT OBSERVATION DEFAULT: 0	0: DISABLE 1: ENABLE	AD09 : RESERVED
AD24: IOQ ENABLE DEFAULT: 1	0: DISABLE 1: ENABLE	AD[7..4] : FLAT PANEL ID
AD23 : RESERVED		AD3: PC166 MODE DEFAULT: 0 0: 33MHz 1: 66MHz
AD22: 27MHz/33 MHz CLOCK SELECTION DEFAULT: 1	0: 33 MHz CLOCK OUTPUT 1: 27 MHz CLOCK INPUT	AD2: CAL DEFAULTS FOR CPU DEFAULT: 0 (FOR BRING UP) 0: DISABLE 1: ENABLE
AD21 : RESERVED	0: PLL Bypass mode disable( Normal mode) 1: PLL Bypass mode enable(Debug only)	AD1: FrcShortReset DEFAULT: 0 0: DISABLE 1: ENABLE
AD20 : PCICLK EXPANSION DEFAULT: 0	1: PCI_REQ#3, PCI_GNT#3 USED AS PCICLK 0: PCI_REQ#3, PCI_GNT#3 USED AS REQ/GNT	AD0: PC1AGP CONFIG. DEFAULT: 0 0: 33 MHz 1: 66 MHz
CBE#3: PROD TEST DEFAULT: 1	0: SHORT TIMERS 1: NORMAL OPERATION	-PCI_REQ: INTERNAL CLOCK GEN. DEFAULT: 1 0: DISABLE 1: ENABLE

12

## SOUTH BRIDGE H/W STRAPPING

	DTR2#	RTS2#	RTS1#	CLK320	SPLED	SQWO
PULL HIGH	INTERNAL KEYBOARD PS2 MODE DEFAULT	ENABLE INTERNAL KEYBOARD	SIO BASE ADDRESS 0X3F0h	32K CLOCK TEST MODE ENABLE	AT POWER MODE	PENTIUM II MODE DEFAULT
PULL LOW	INTERNAL KEYBOARD AT MODE	DISABLE INTERNAL KEYBOARD DEFAULT	SIO BASE ADDRESS 0X370h DEFAULT	32K CLOCK TEST MODE DISABLE DEFAULT	ATX POWER MODE DEFAULT	PENTIUM / K7 MODE

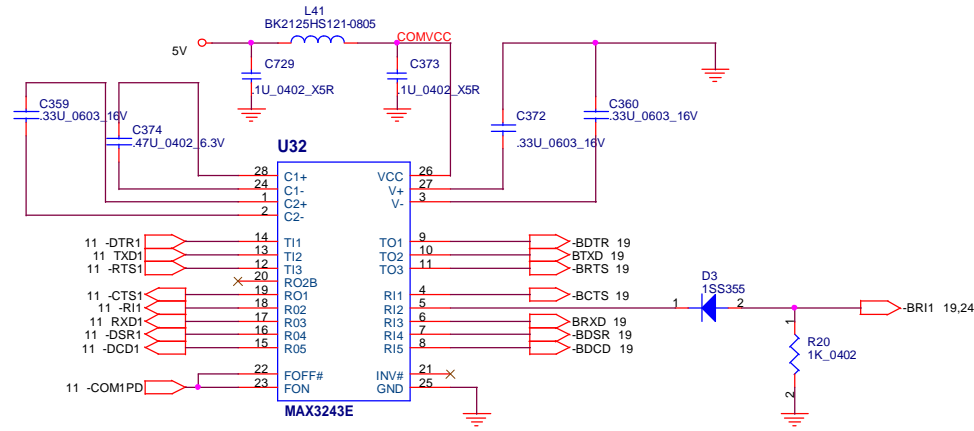
PCS1#	PCS0#	GPO34	LB#	GPO30[AEN]	GPO29	ROMCS#	GPO35
GPI24 & GPO30 FUNCTIONS	DISABLE 4MB FLASH ROM MODE	CHIP TEST MODE DISABLE DEFAULT	ACTIVE HIGH TO POWER OFF	L,L - USB TEST MODE L,H - AUDIO/MODEM TEST MODE H,L - SUPER IO TEST MODE H,H - NORMAL OPERATION		FLASH ROM MODE SELECTION L,L - RESERVED L,H - ENABLE 8Mb Flash ROM SIZE H,L - DISABLE ALL FUNC. IN THIS CONFIG. H,H - ENABLE LPC FLASH ROM	
IOCHRDY & AEN FUNCTIONS	ENABLE 4MB FLASH ROM MODE	CHIP TEST MODE ENABLE	ACTIVE LOW TO POWER OFF	DEFAULT: H, H		DEFAULT: H, L	



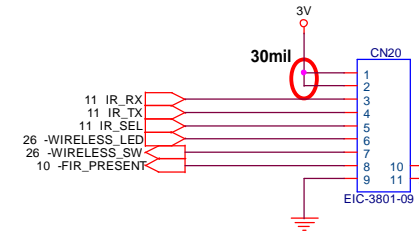
PROJECT : KT9D  
Quanta Computer Inc.

Size	Document Number	Rev
	N.B & S.B H/W STRAPPING	1A
Date: Monday, July 14, 2003	Sheet	12 of 34

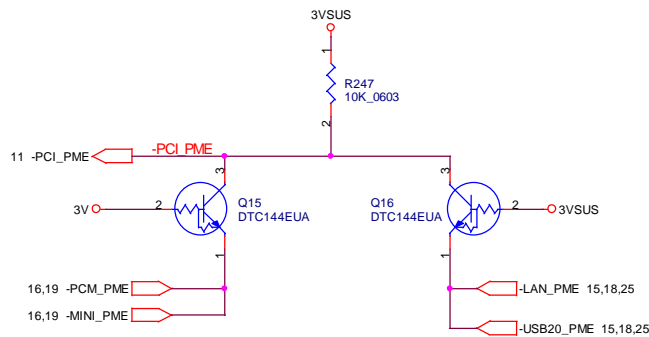
## SERIAL PORT



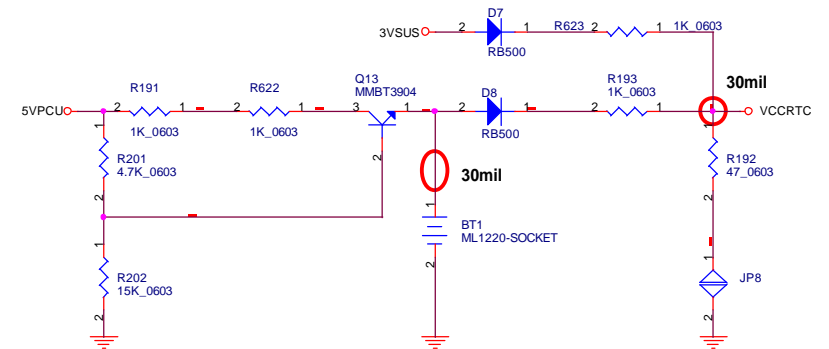
## FIR CON




## PME CONTROL



## RTC POWER CIRCUIT





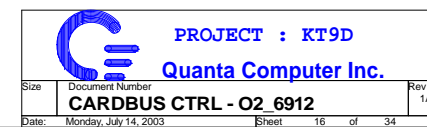
**PROJECT : KT9D**  
**Quanta Computer Inc.**

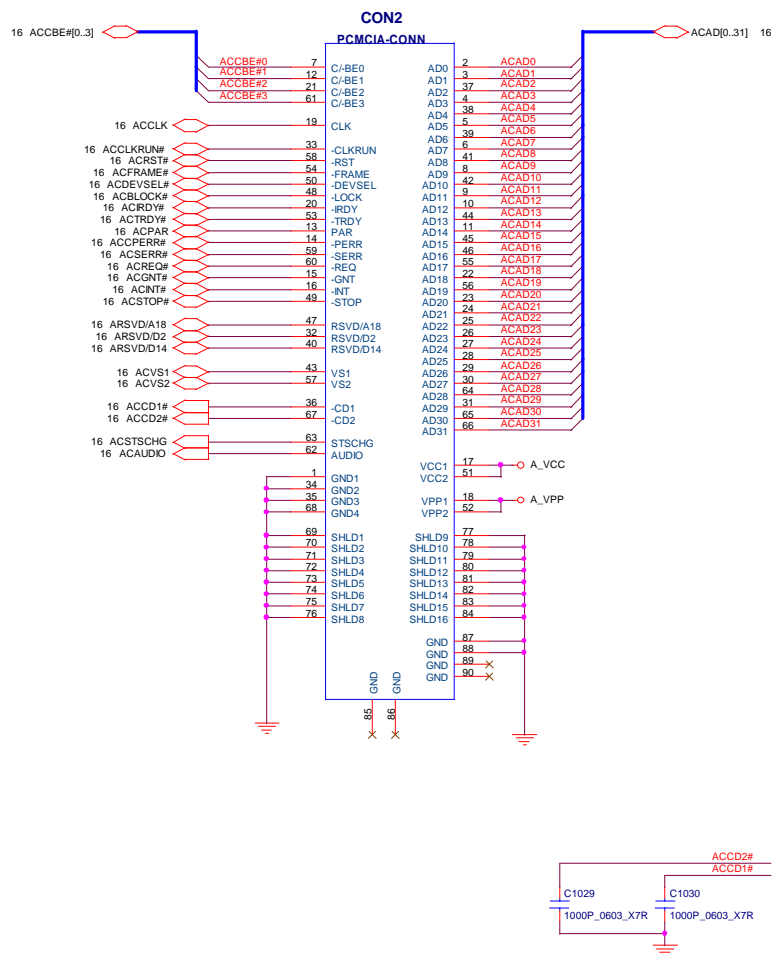
Size	Document Number	Rev
	<b>SERIAL PORT&amp;RTC&amp;FIR CON</b>	<b>1A</b>
Date: Monday, July 14, 2003		Sheet 13 of 34

## 14

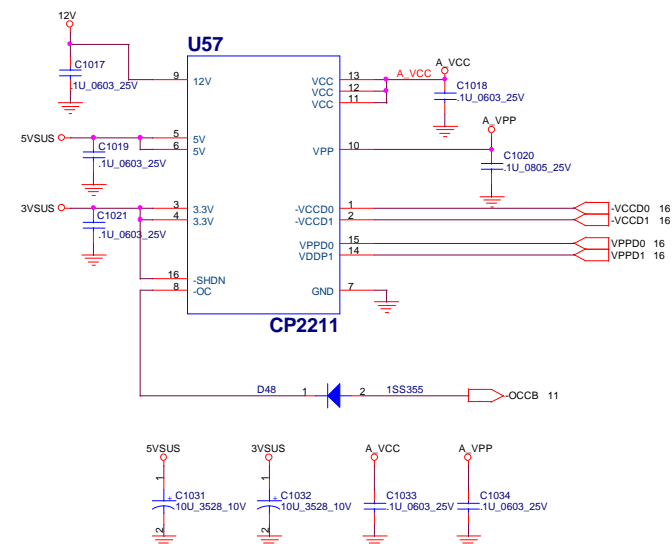




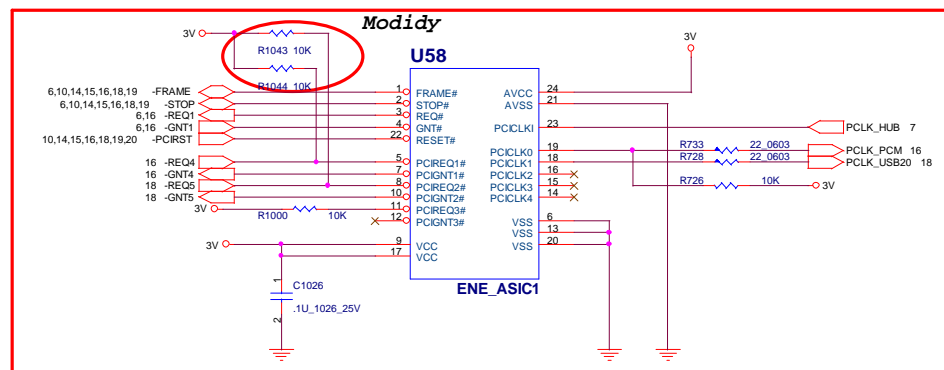




## CARDBUS POWER SWITCH

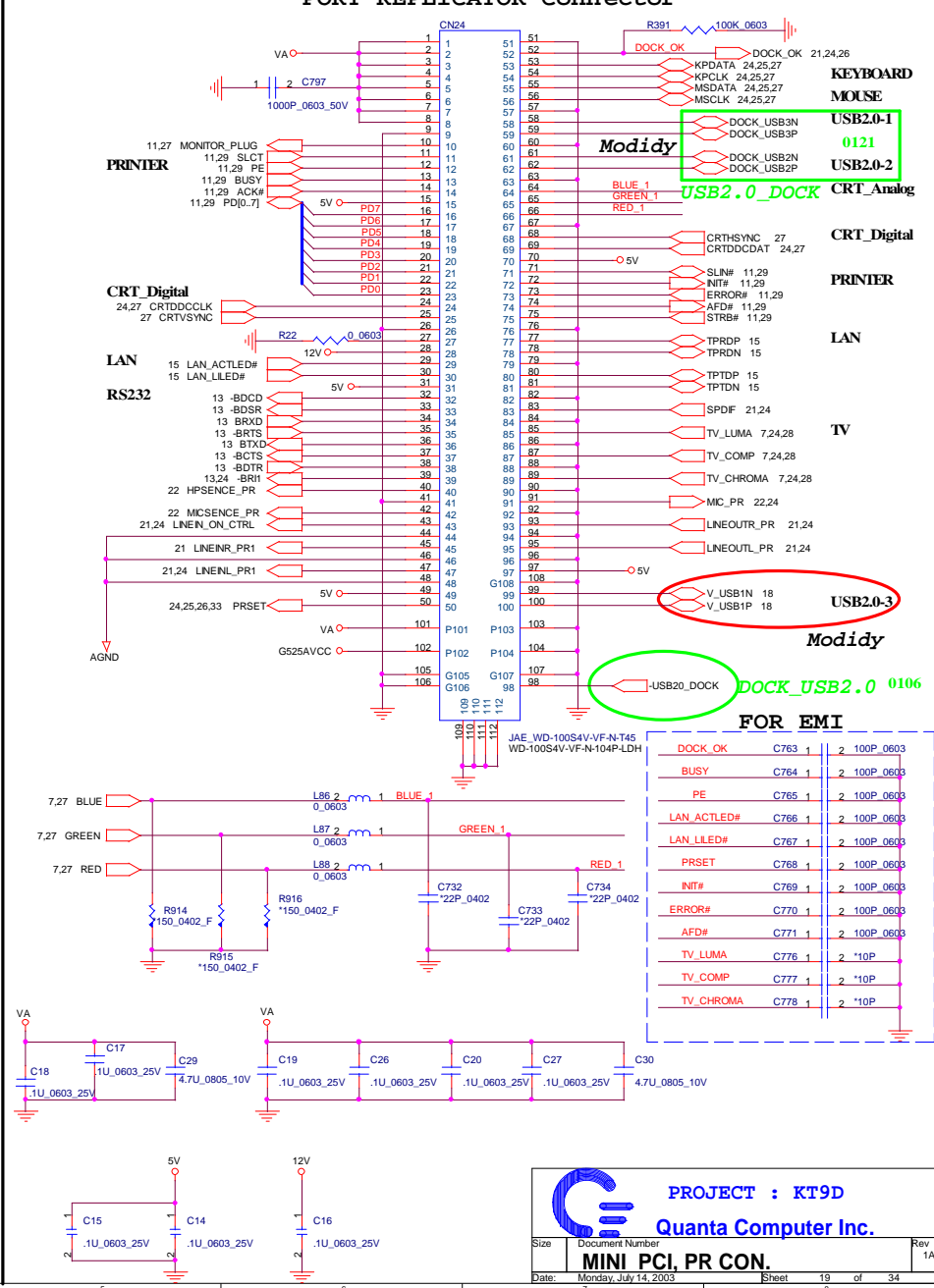


## PCI HUB\_ENE-ASIC1



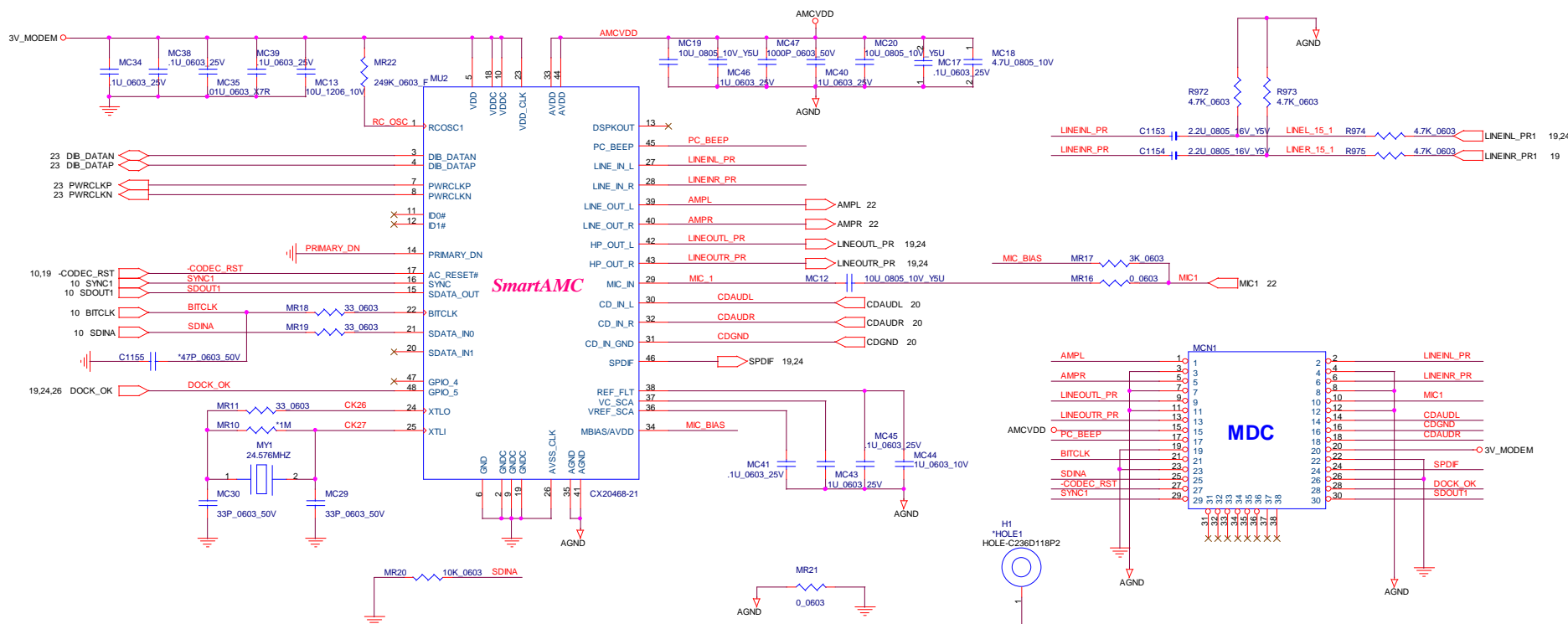


TYPE III MINI PCI SOCKET

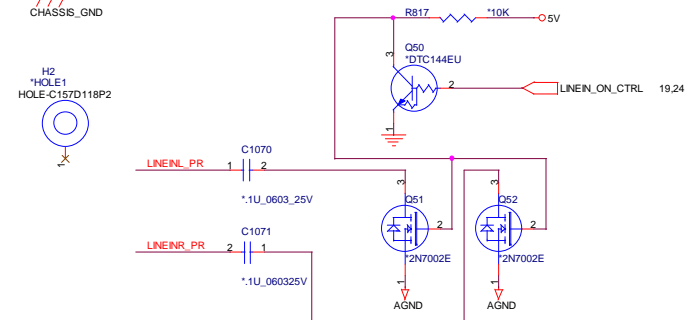
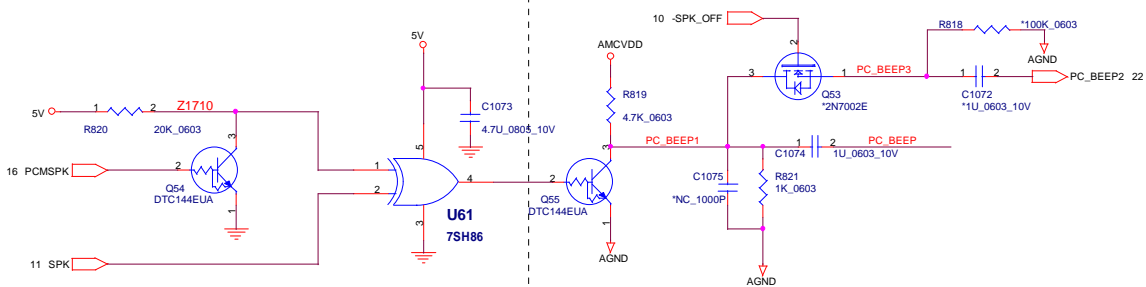





The AMC20493-001 modem is used for mother board family MBAMC20493-006.



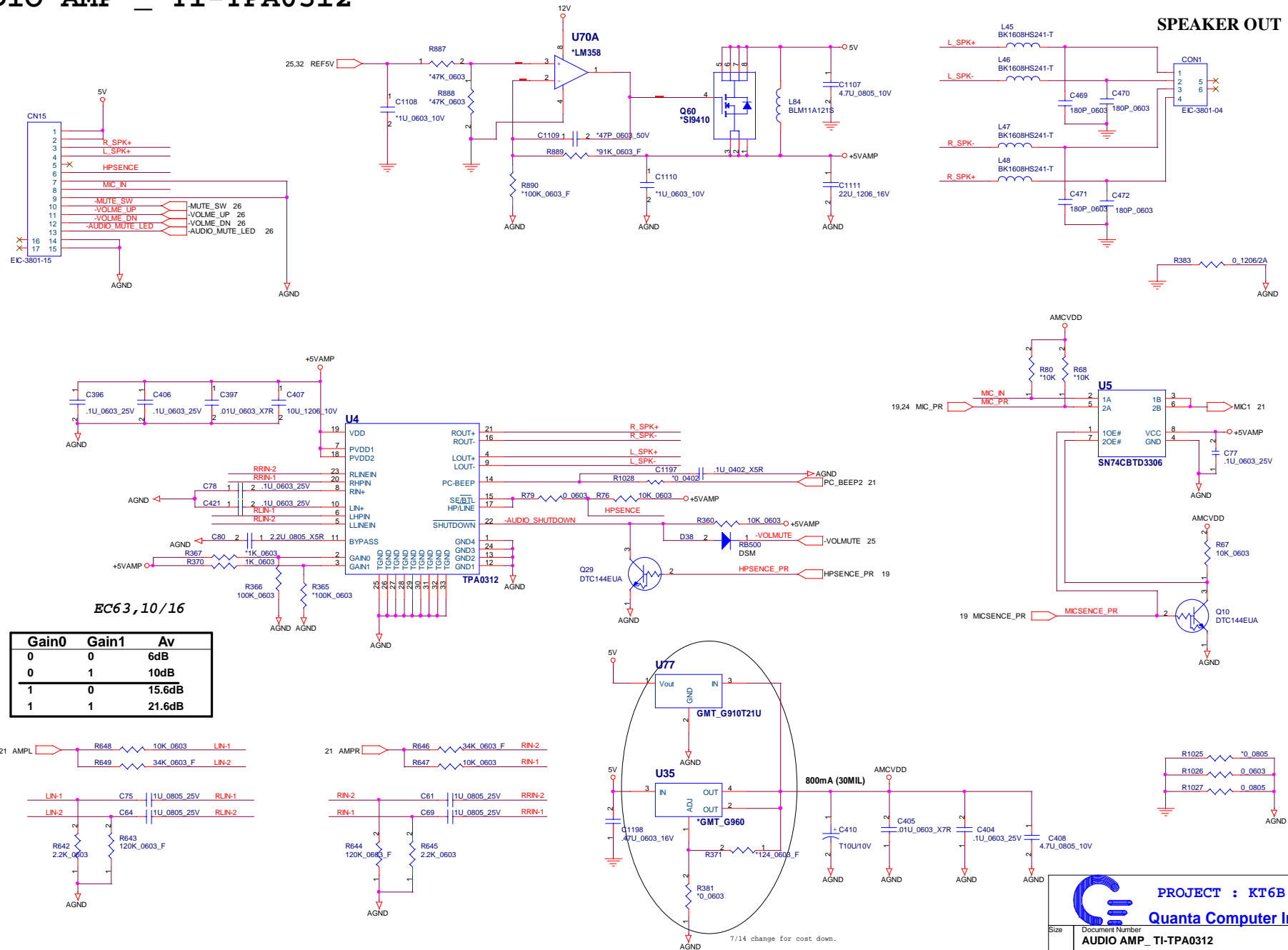
## PC SPEAKER



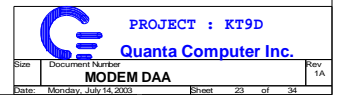


**PROJECT : KT9D**  
**Quanta Computer Inc.**

Size	Document Number	Rev	1A
<b>AMC97 CODEC</b>			
Date:	Monday, July 14, 2003	Sheet	21 of 34



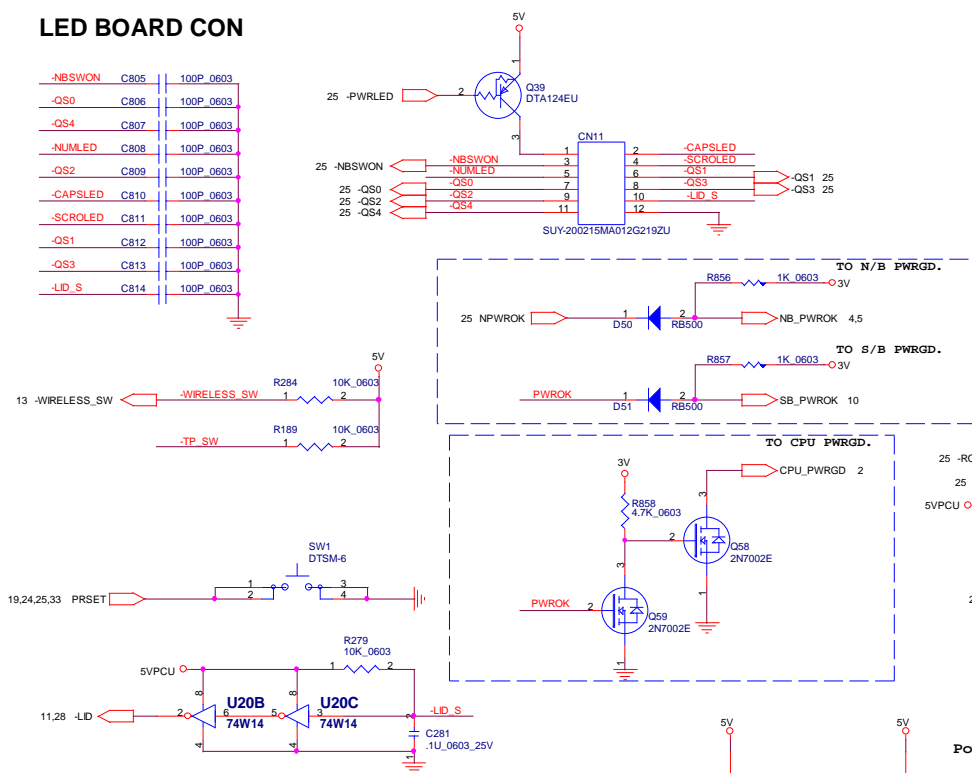




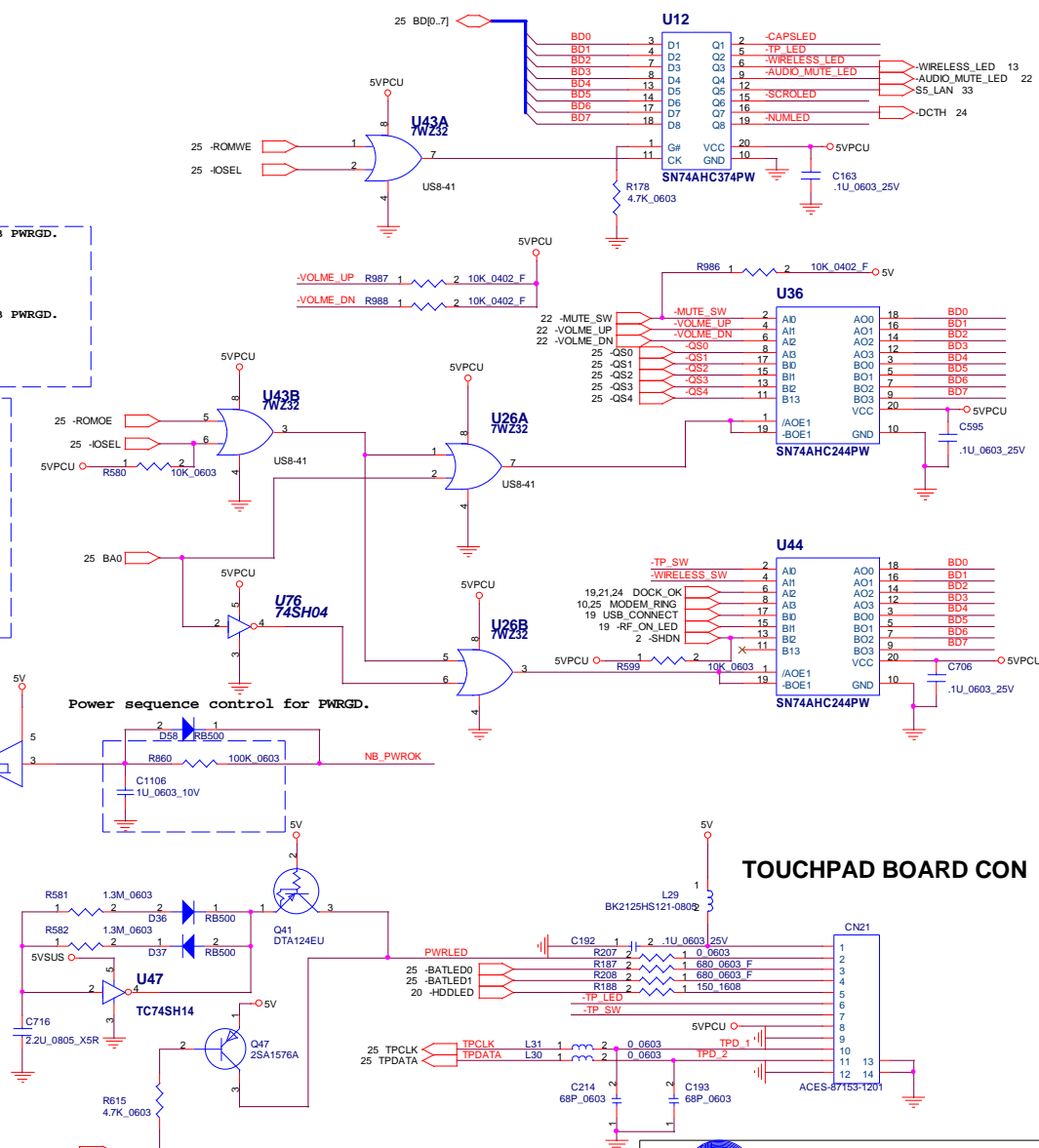
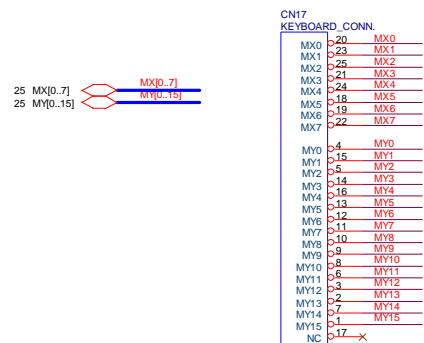




-NBSWON	C805	100P_0603
-QS0	C806	100P_0603
-QS4	C807	100P_0603
-NUMLED	C808	100P_0603
-QS2	C809	100P_0603
-CAPSLED	C810	100P_0603
-SCROLED	C811	100P_0603
-QS1	C812	100P_0603
-QS3	C813	100P_0603
-LIB_S	C814	100P_0603



**For ATI PWG function**



## TOUCHPAD BOARD CON

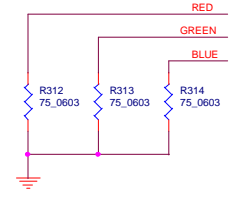
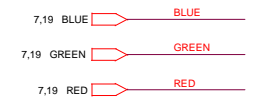
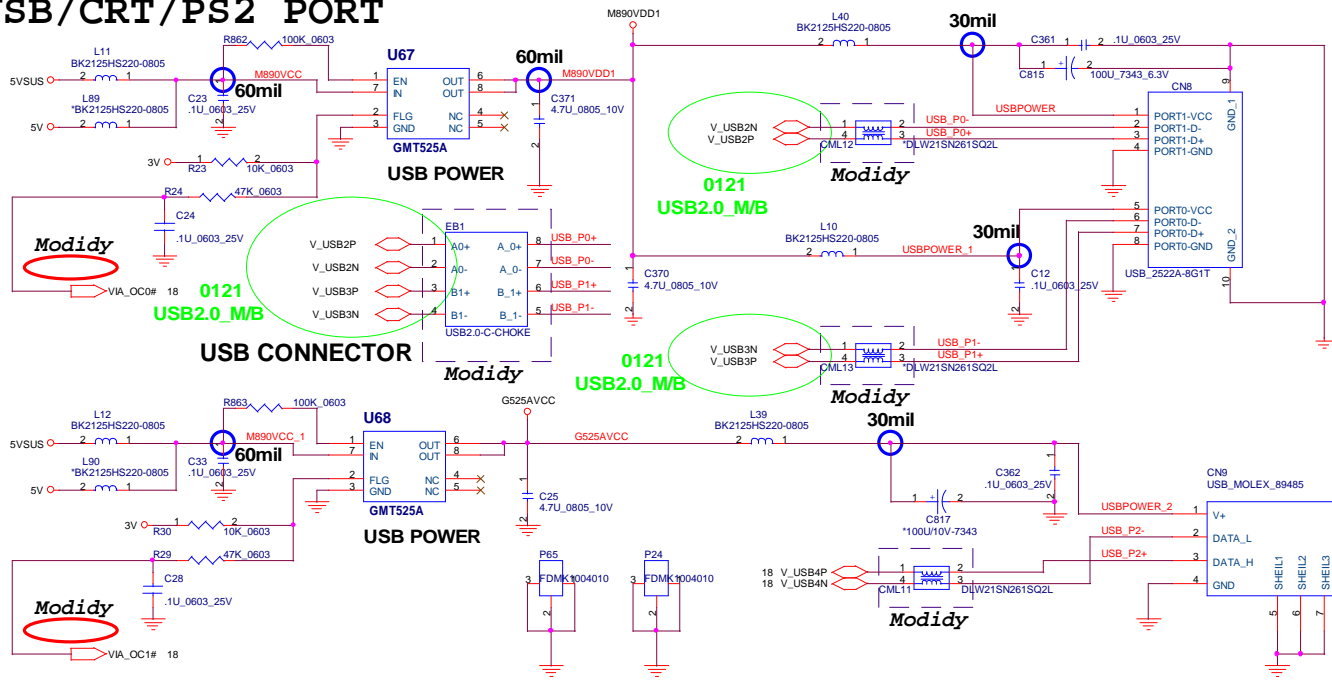


**Quanta Computer Inc.**

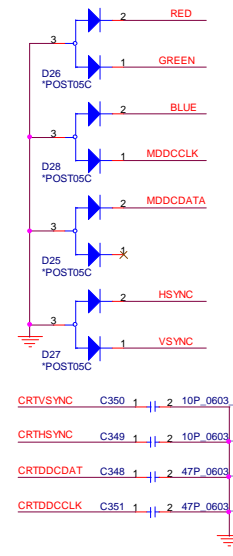
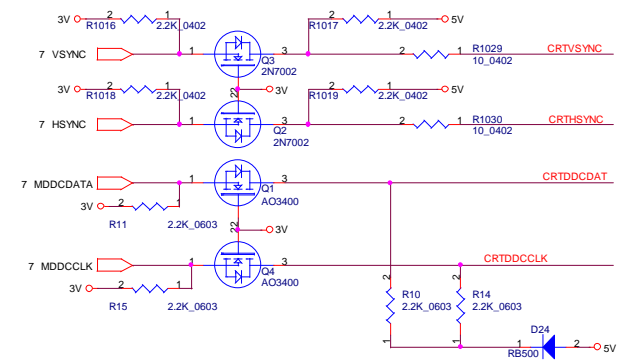
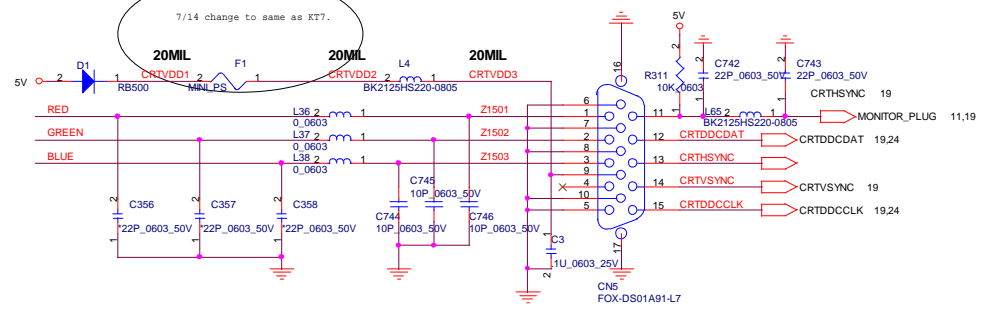
Rev	1A
-----	----

# USB/CRT/PS2 PORT

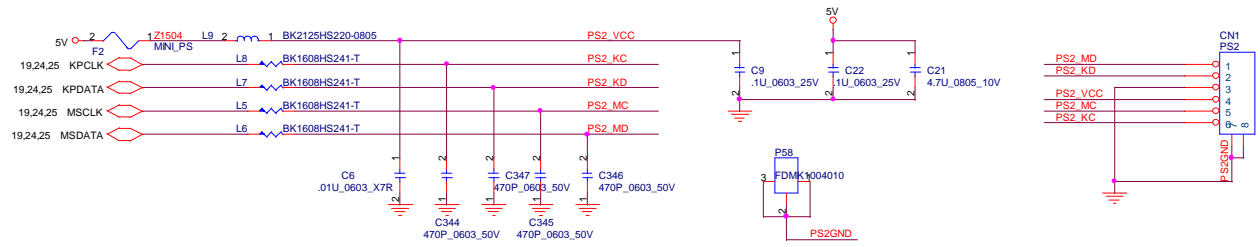
27



## CRT PORT



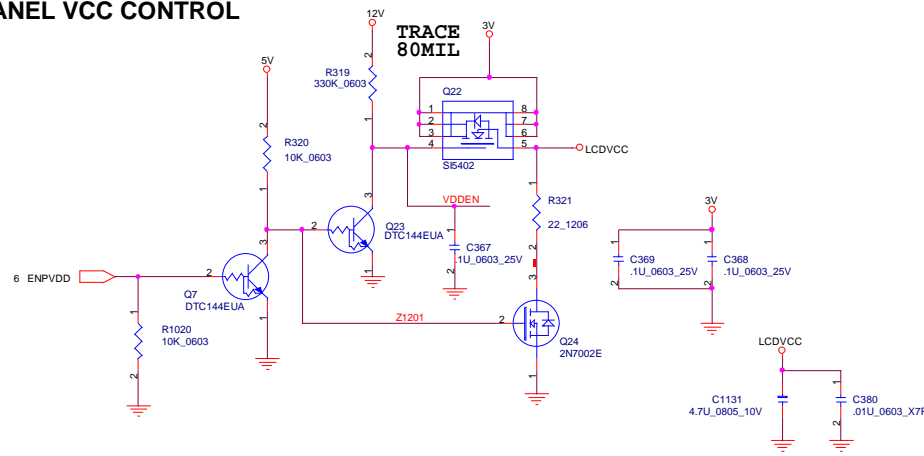
## PS/2 PORT



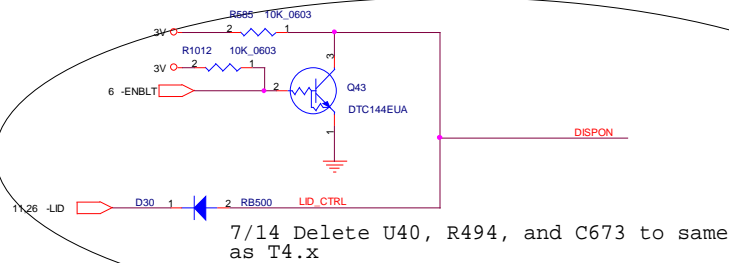
PROJECT : KT9D  
Quanta Computer Inc.

Size	Document Number	Rev
	USB/CRT/PS2 PORT	1A
Date:	Monday, July 14, 2003	Sheet 27 of 34

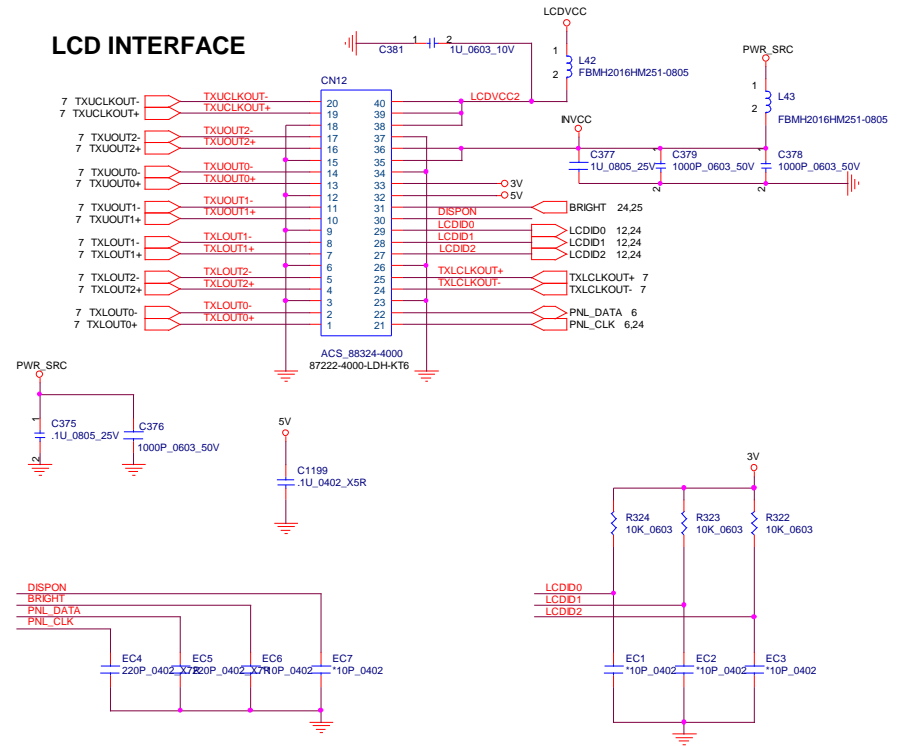
## PANEL VCC CONTROL



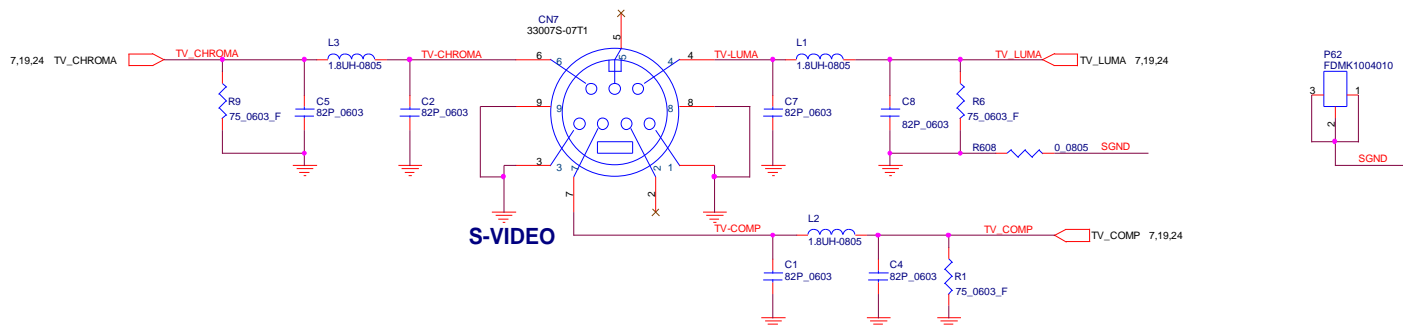
## BACKLIGHT POWER CONTROL



## LCD INTERFACE

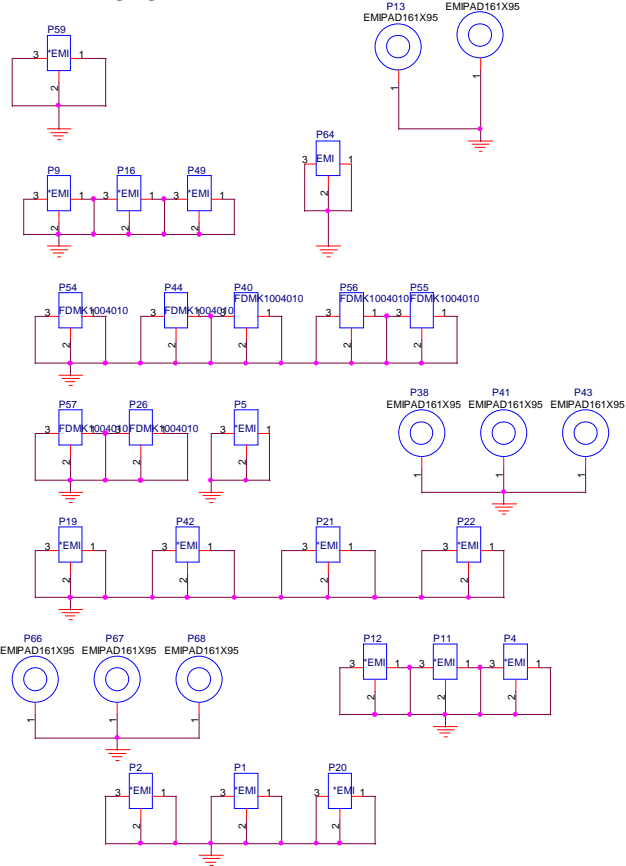


## S - TERMINAL CONNTER

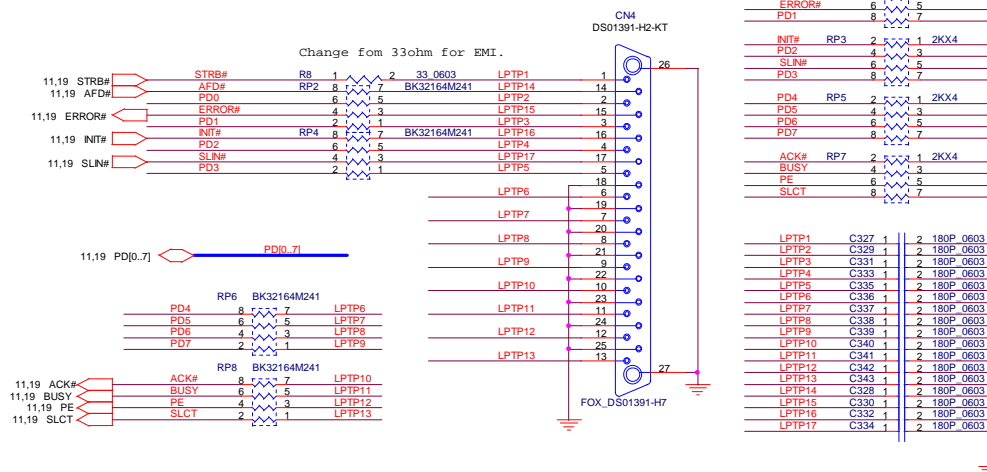


		<b>PROJECT : KT9D</b> <b>Quanta Computer Inc.</b>	Rev 1A
Size	Document Number	LCD INTERFACE & S-TERMIANL	
Date:	Monday, July 14, 2003	Sheet	28 of 34

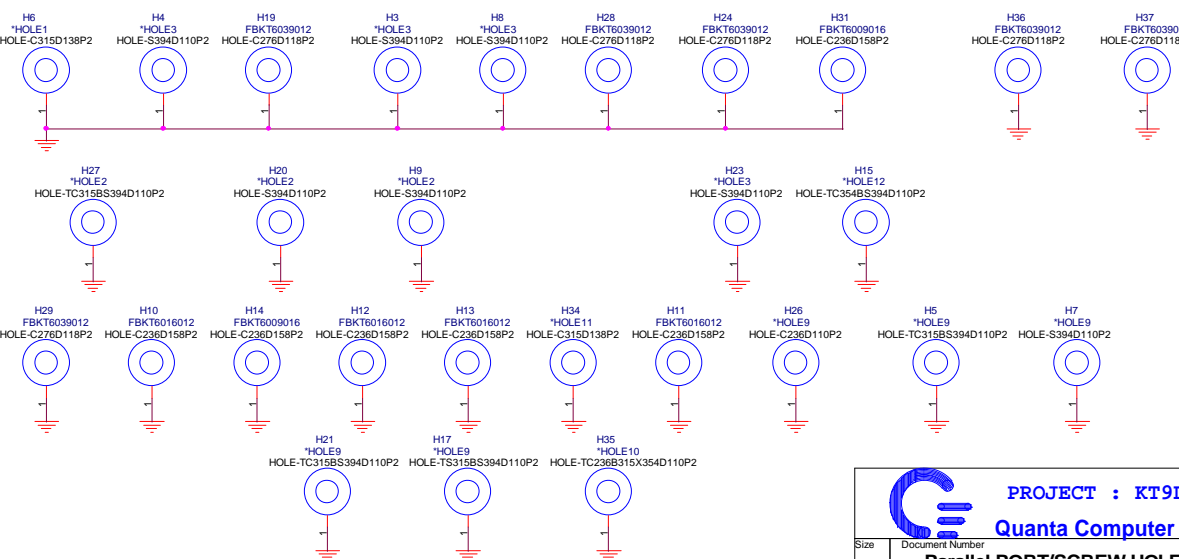
## EMI FENSES




Change fom 33ohm for EMI.



## SCREW HOLES

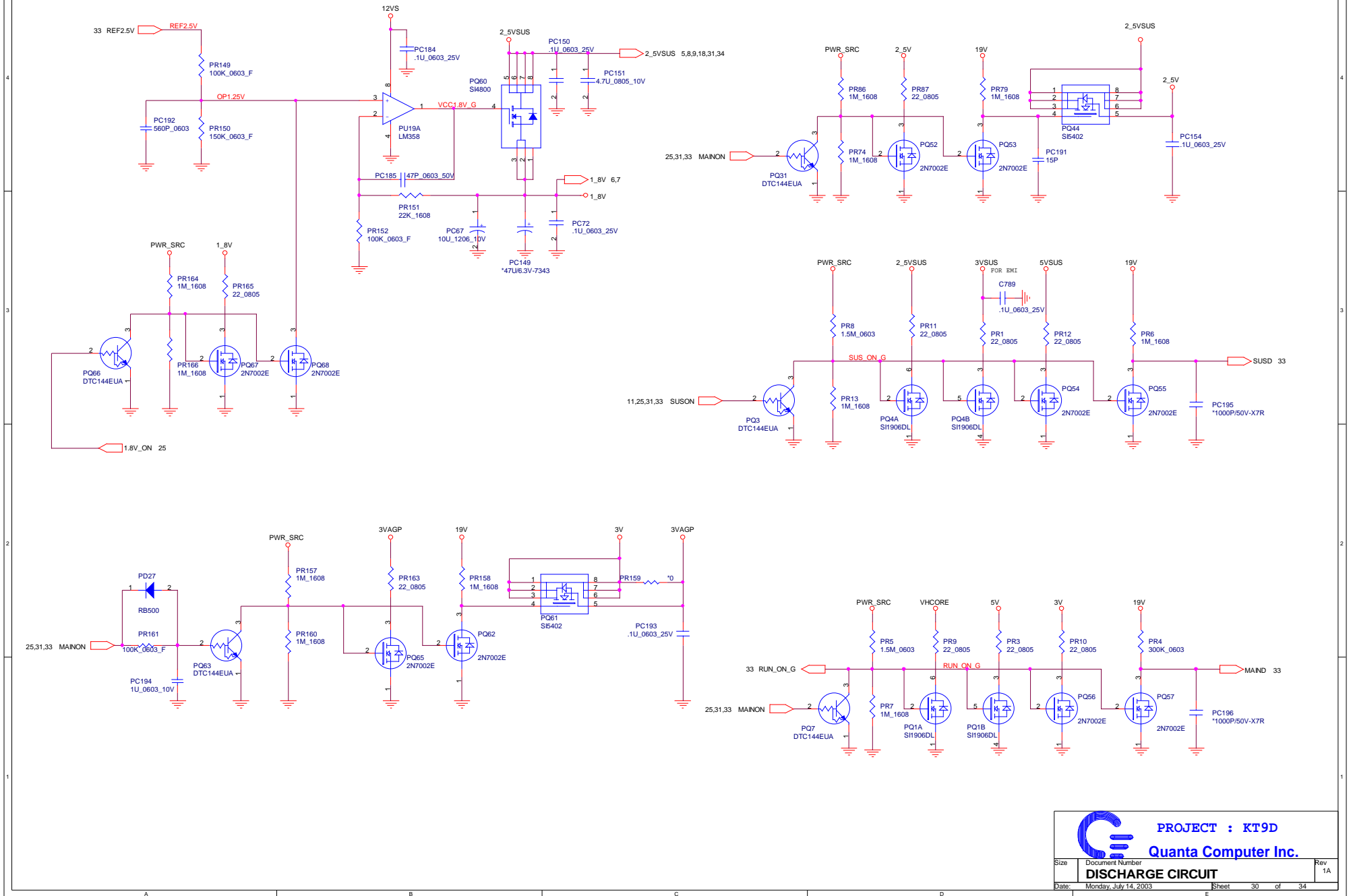



		<b>PROJECT : KT9D</b> <b>Quanta Computer Inc.</b>	
Size	Document Number	<b>Parallel PORT/SCREW HOLE</b>	Rev
			1A
Date:	Monday, July 14, 2003	Sheet	29 of 34



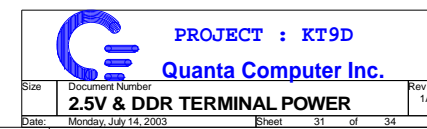
# DISCHARGE CIRCUIT

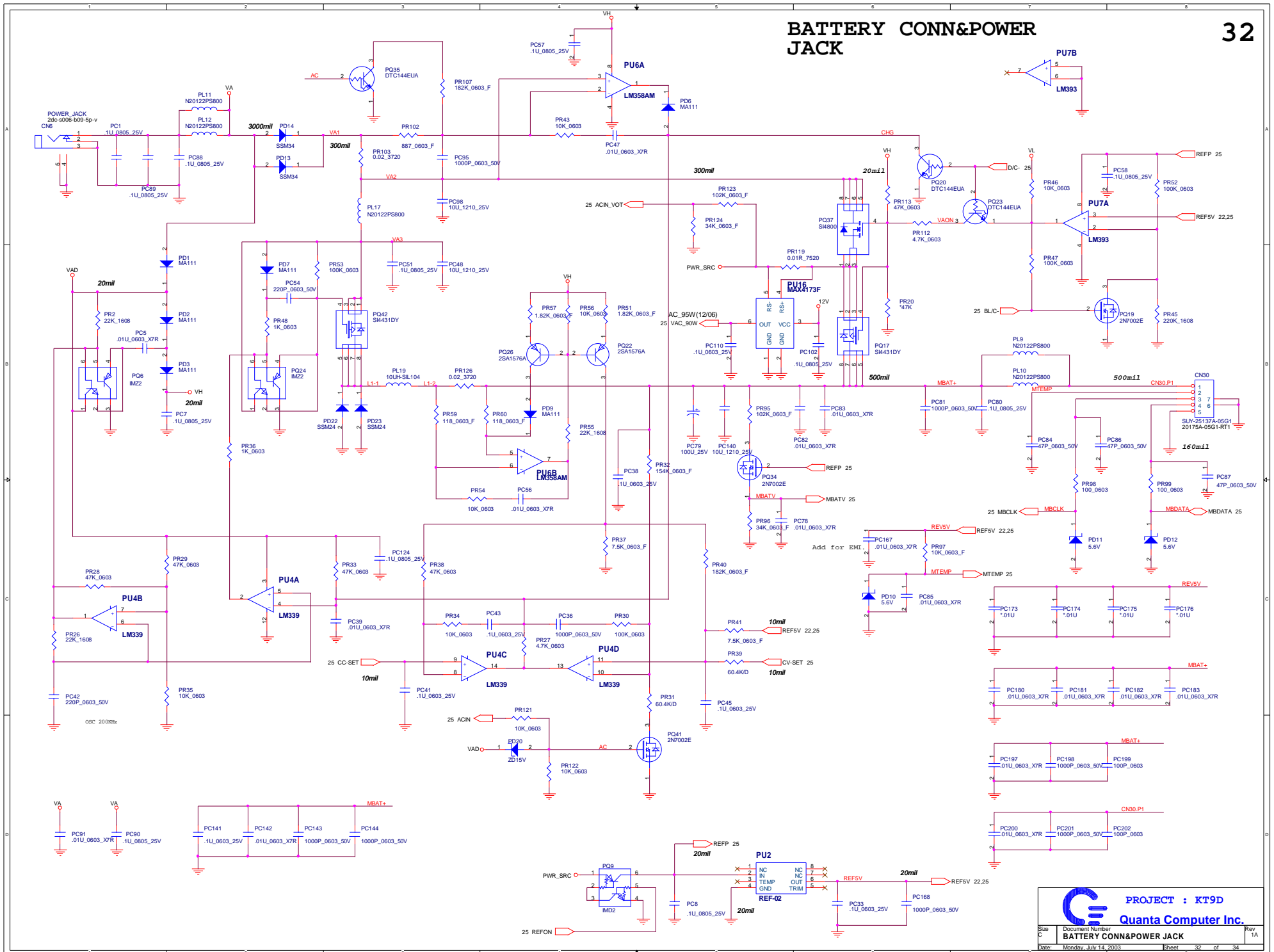
30



 <b>PROJECT : KT9D</b> <b>Quanta Computer Inc.</b>		Rev
		1A
<b>DISCHARGE CIRCUIT</b>		
Date:	Monday, July 14, 2003	Sheet 30 of 34

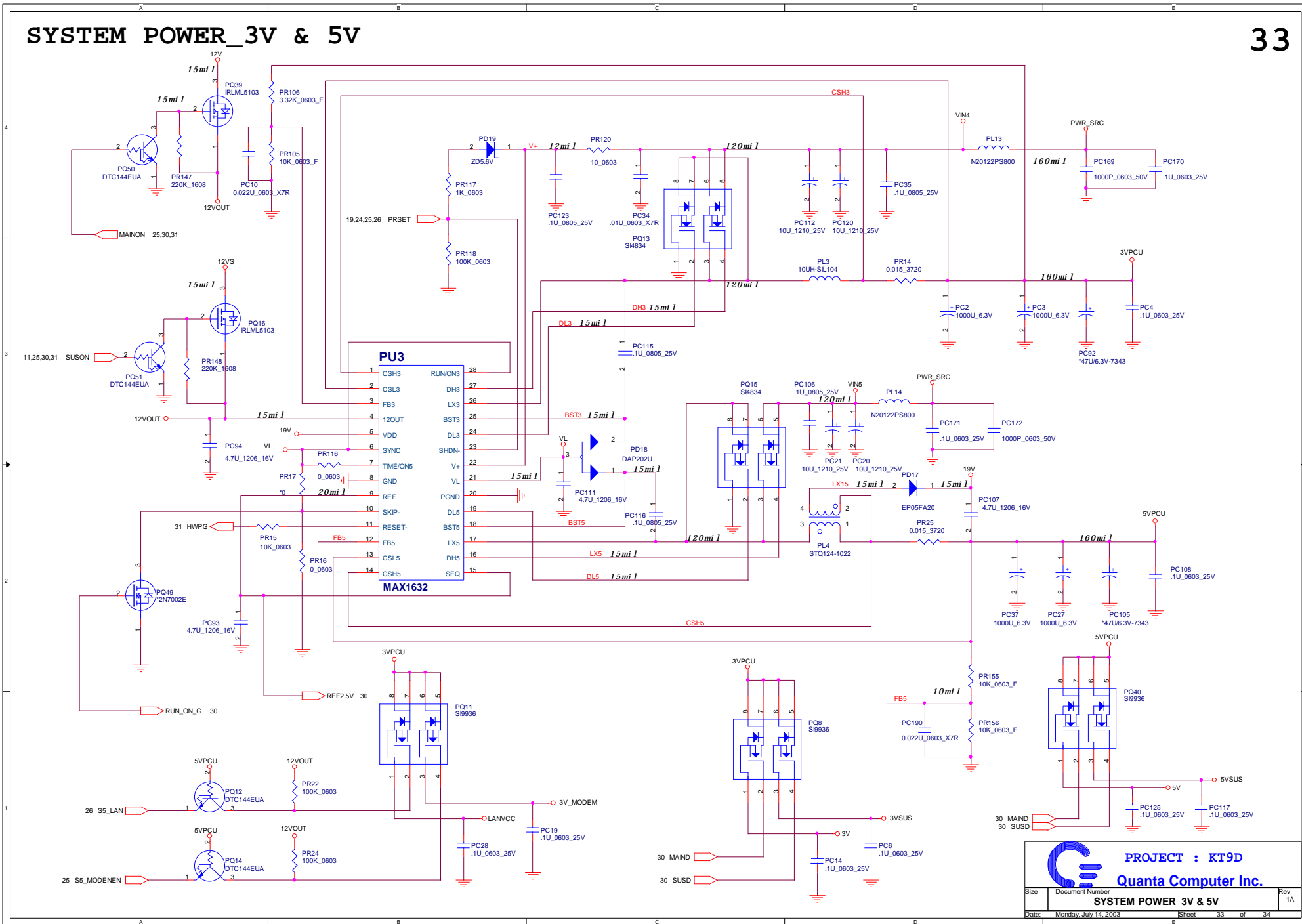
31



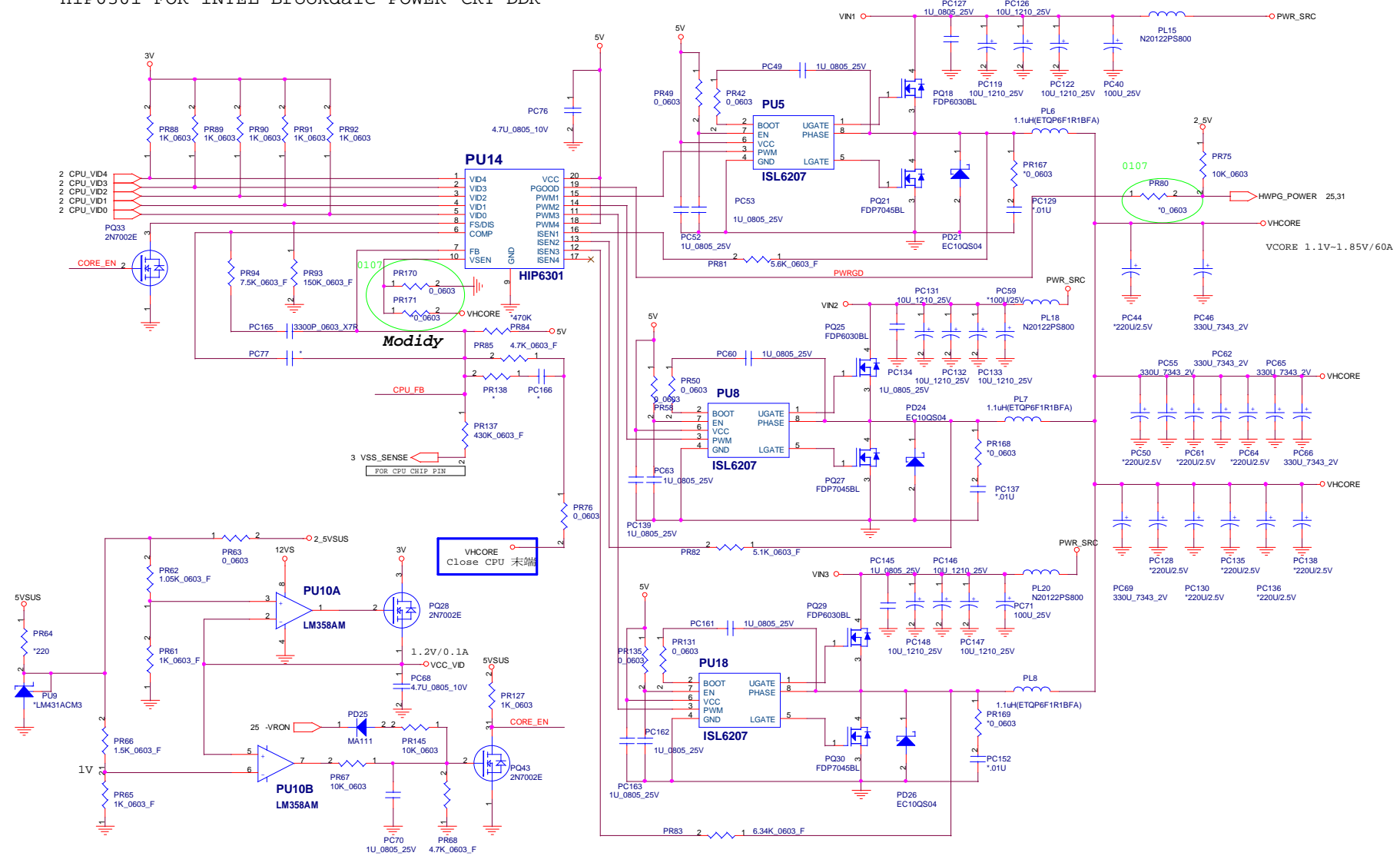



## SYSTEM POWER 3V & 5V

33



HIP6301 FOR INTEL Brookdale POWER CKT-DDR



				PROJECT : KT9D	
				Quanta Computer Inc.	
Size	Document Number	SYS POWER_VCORE- HIP6301			Rev 1A
Date:	Monday, July 14, 2003	Sheet	34	of	34