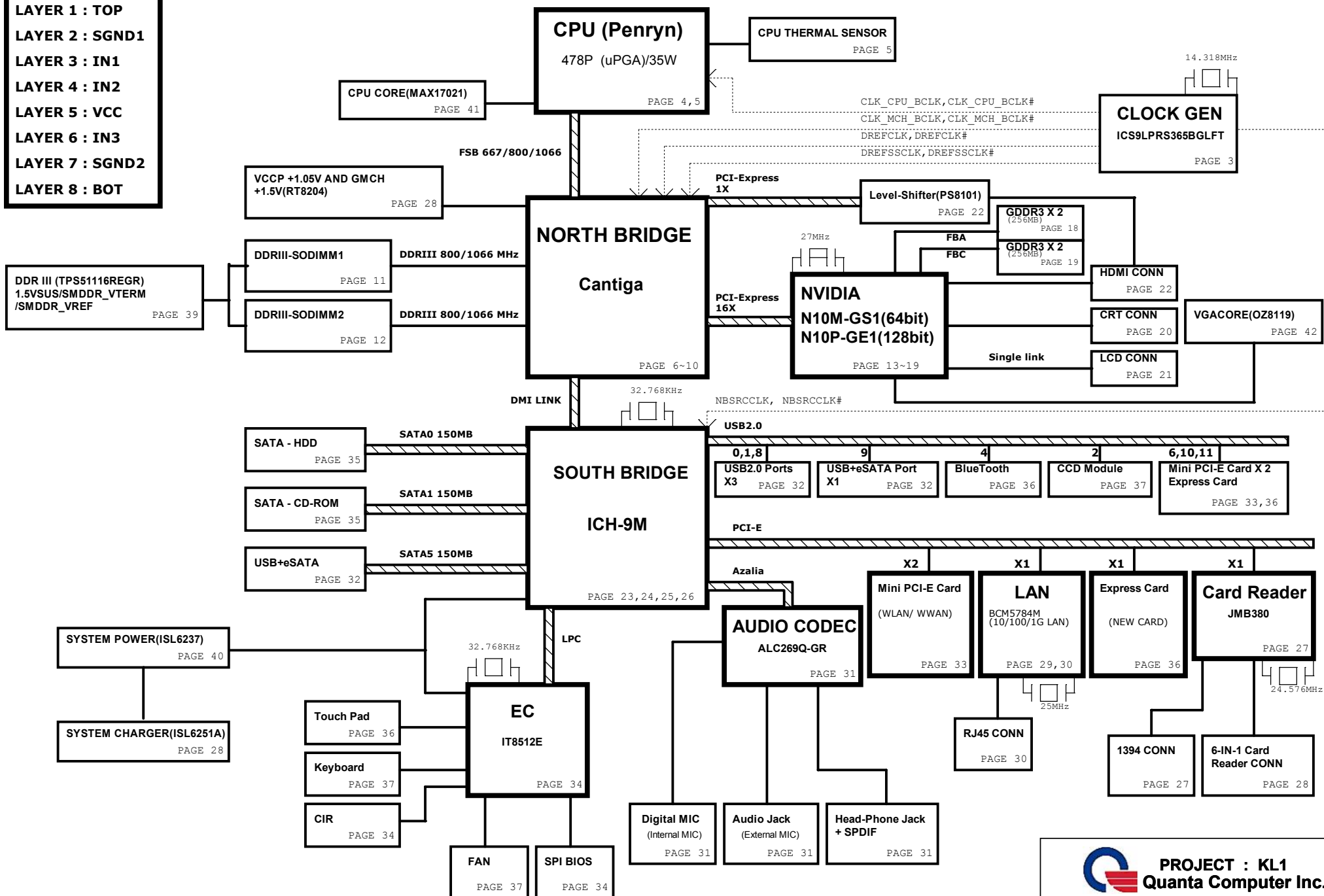


LAYER 1 : TOP  
 LAYER 2 : SGND1  
 LAYER 3 : IN1  
 LAYER 4 : IN2  
 LAYER 5 : VCC  
 LAYER 6 : IN3  
 LAYER 7 : SGND2  
 LAYER 8 : BOT

## KL1 BLOCK DIAGRAM

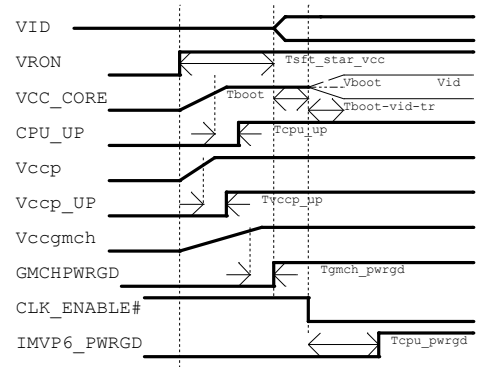


**PROJECT : KL1**  
**Quanta Computer Inc.**

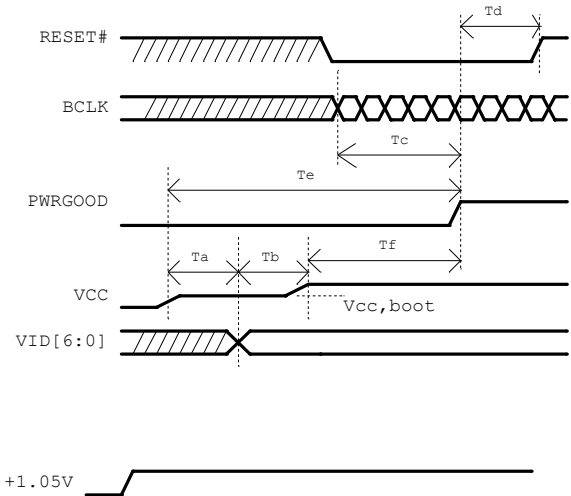
PCB Layers

Layer 1		TOP
Layer 2		GND
Layer 3		IN1
Layer 4		IN2
Layer 5		SVCC
Layer 6		IN3
Layer 7		GND
Layer 8		BOTTOM

Power On Sequencing Timing Diagram



Penryn Power-up Timing Specifications

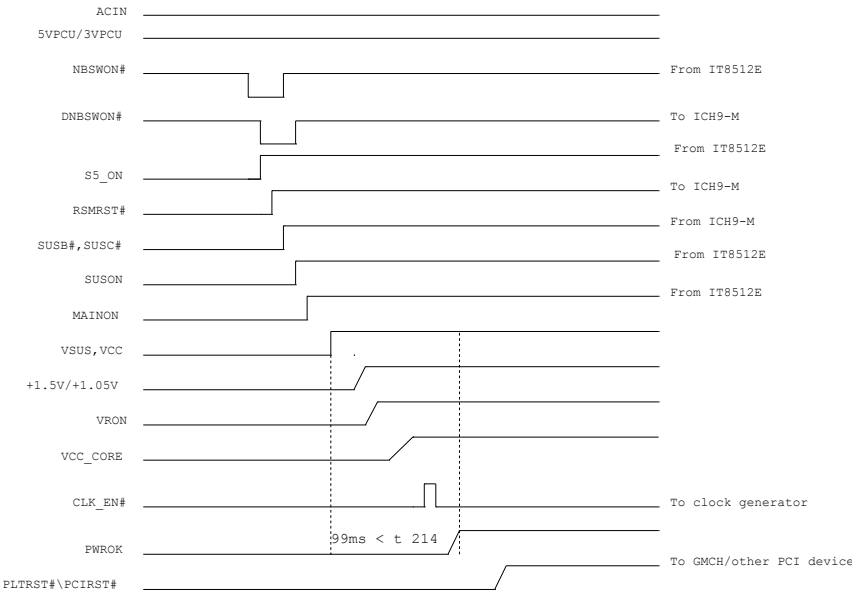



Ta=VCC and VCCP asseration to VID[6:0] vaild  
Tb=VID[6:0] stable to VCC vaild  
Tc=BCLK stable to PWRGOOD asseration  
Td=PWRGOOD to RESET# de-assertion time  
Te=Vcc,boot vaild to PWRGOOD asseration time

Voltage Rails

Voltage Rails	ON S0~S2	ON S3	ON S4	ON S5	Control signal
VCC_CORE	V				VRON
+1.5V	V				MAINON
+1.05V	V				MAINON
5V_S5/3V_S5	V	V	V	V	S5_ON
5VSUS/3VSUS/1.5VSUS	V	V			SUSON
SMDDR_VTERM/+3V/+5V/+15V/+1.8V	V				MAINON
+VGACORE/+VGA1.1V	V				MAINON
LANVCC	V	V			LAN_ON
3VPCU	V	V	V	V	VL
5VPCU	V	V	V	V	VL

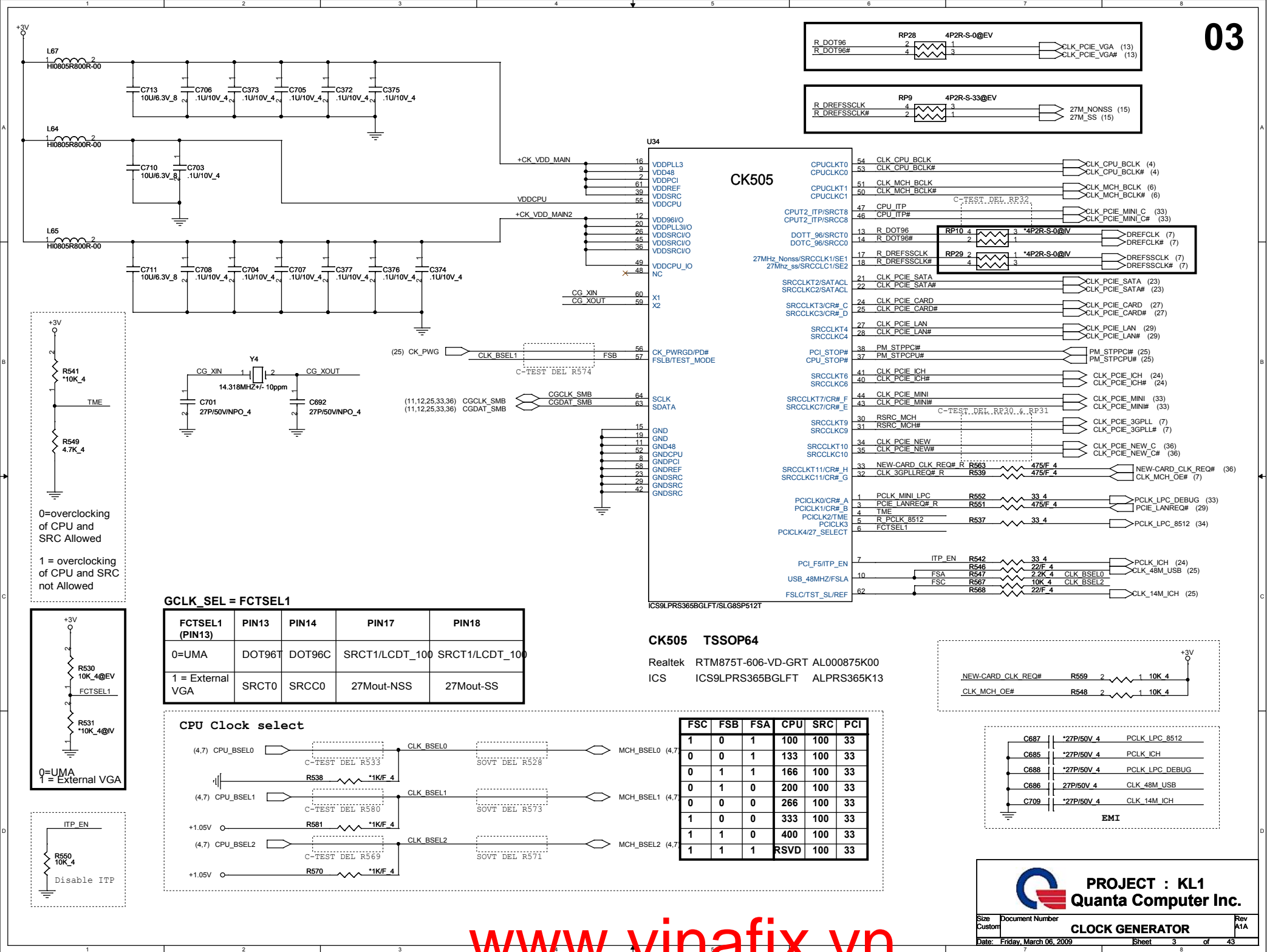
ACIN POWER ON TIMING

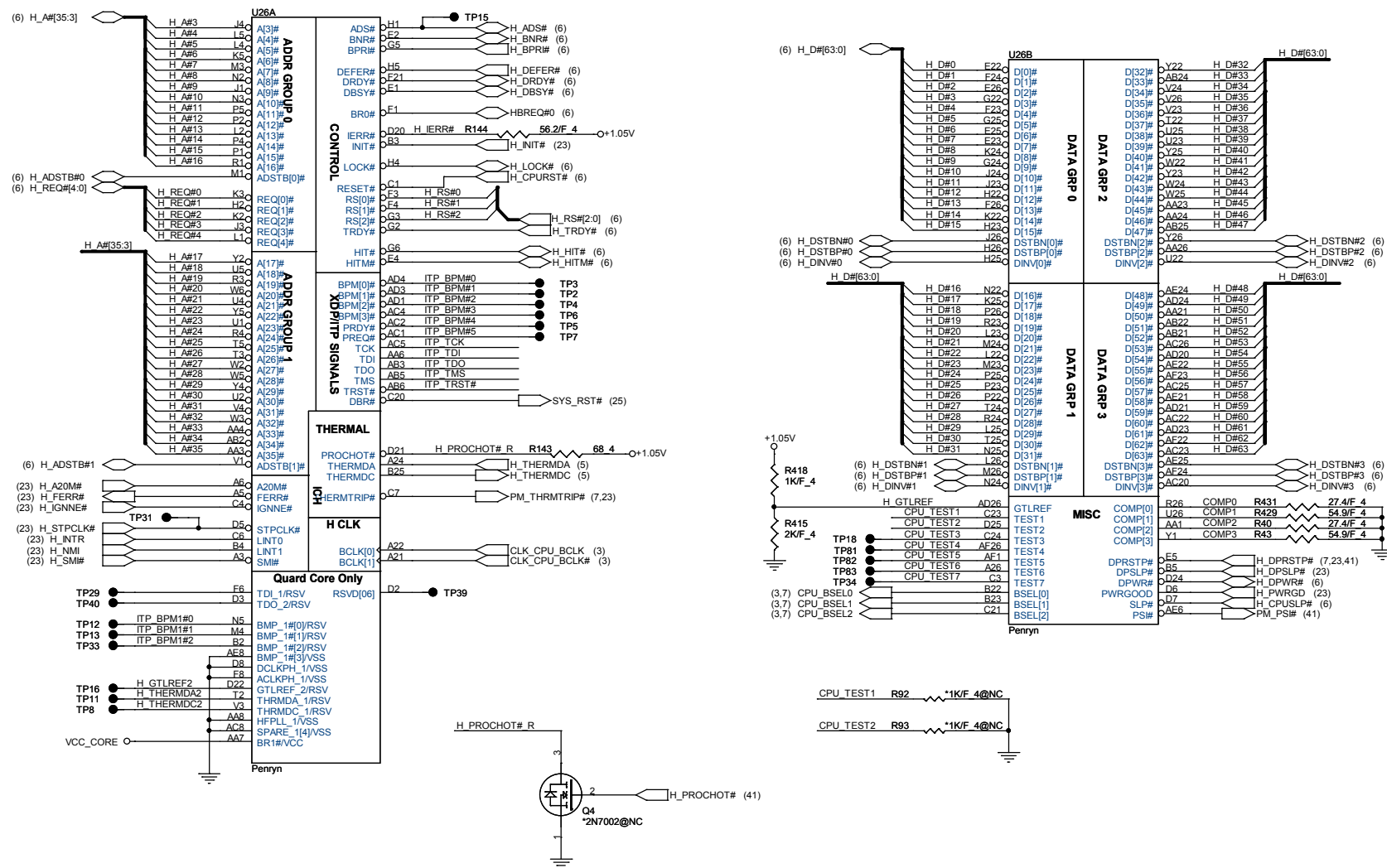




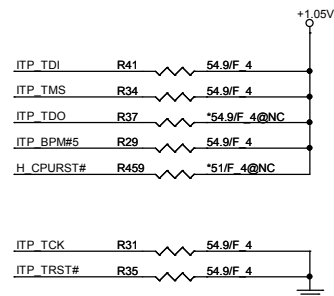
PROJECT : KL1  
Quanta Computer Inc.

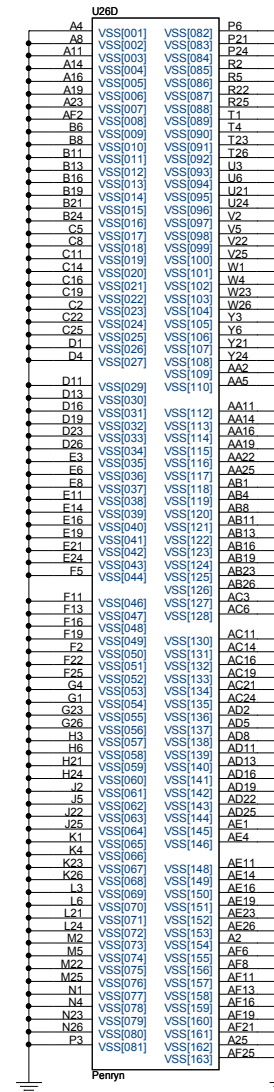
Size Custom	Document Number	SYSTEM INFORMATION	Rev A1A
Date: Friday, March 06, 2009	Sheet 2 of 43		

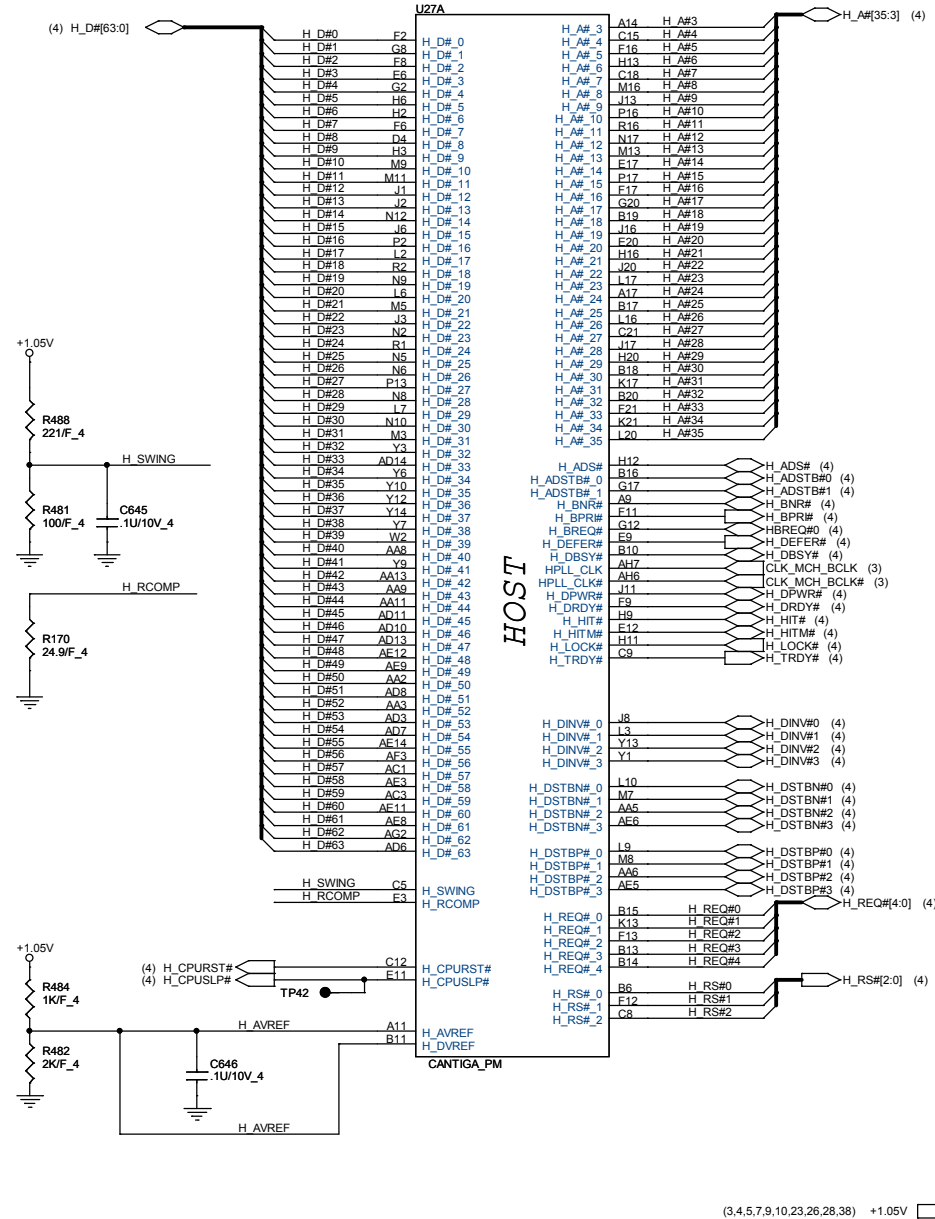




## Populate ITP700Flex for bringup

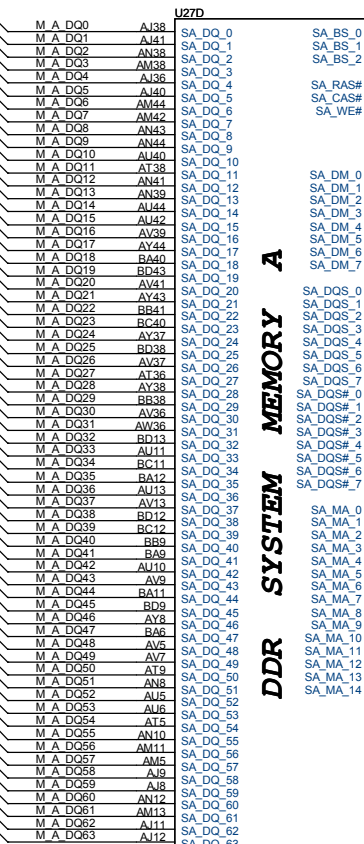




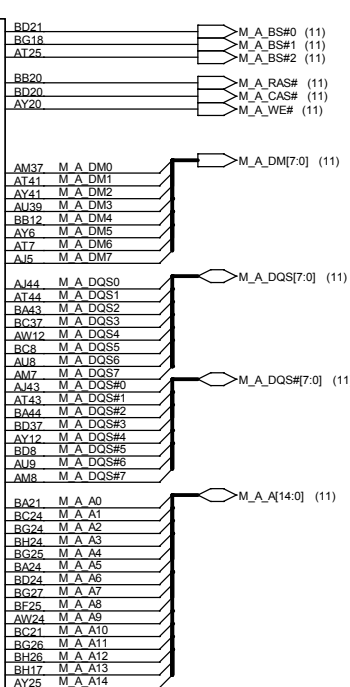




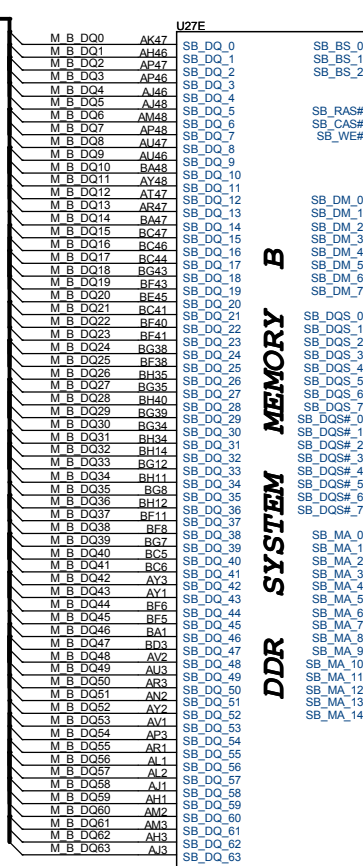
(11) M\_A\_DQ[63:0]



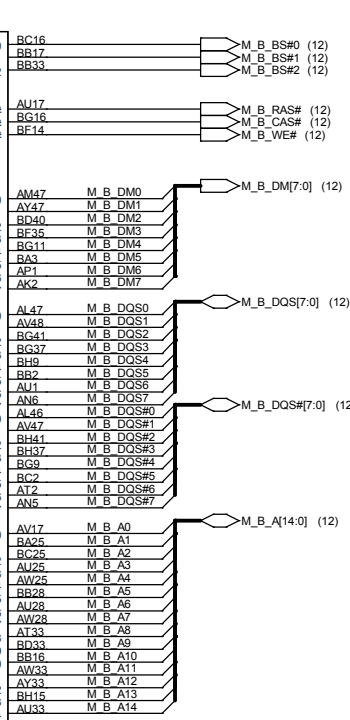
CANTIGA\_PM



(12) M\_B\_DQ[63:0]



CANTIGA\_PM

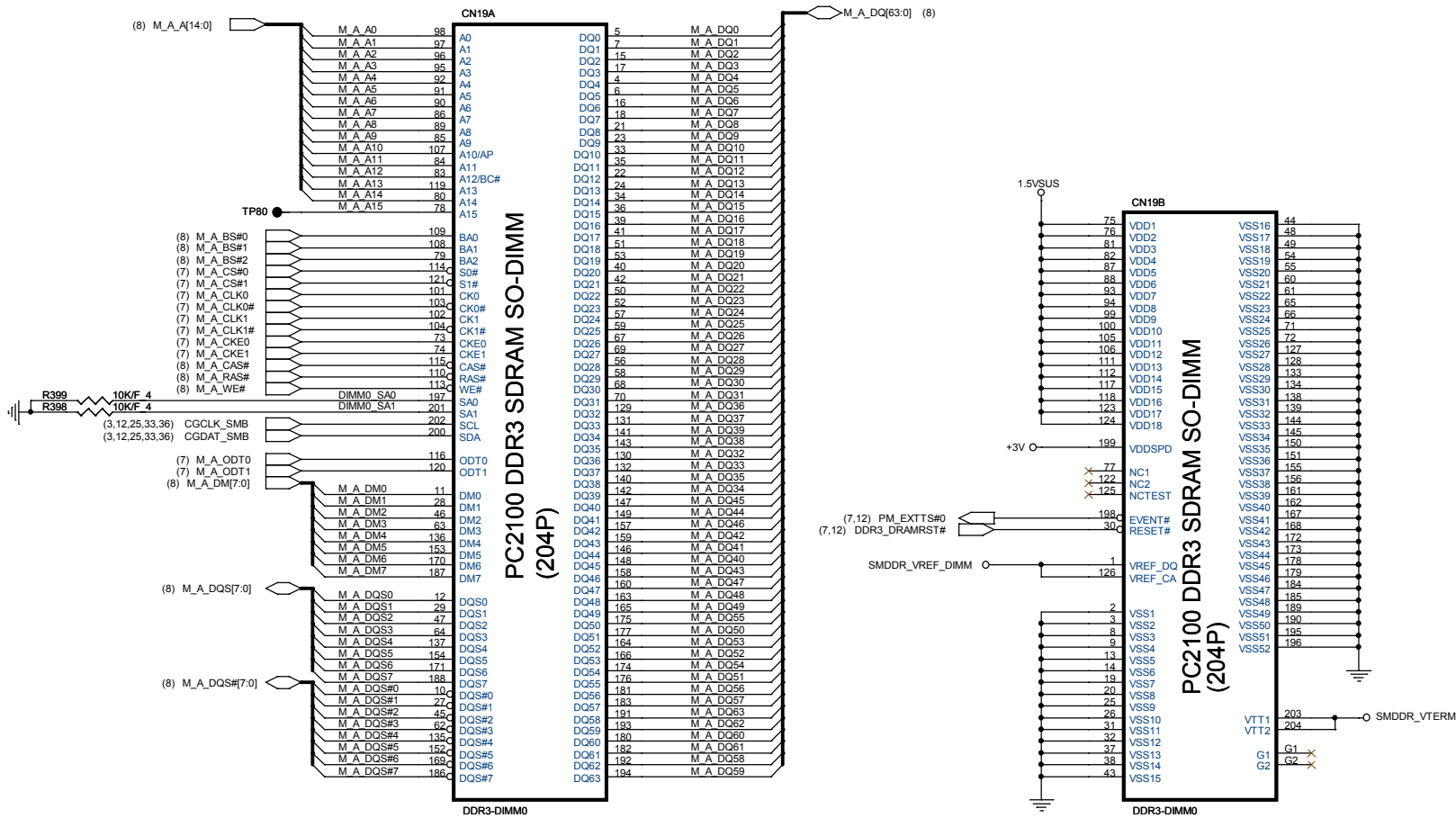


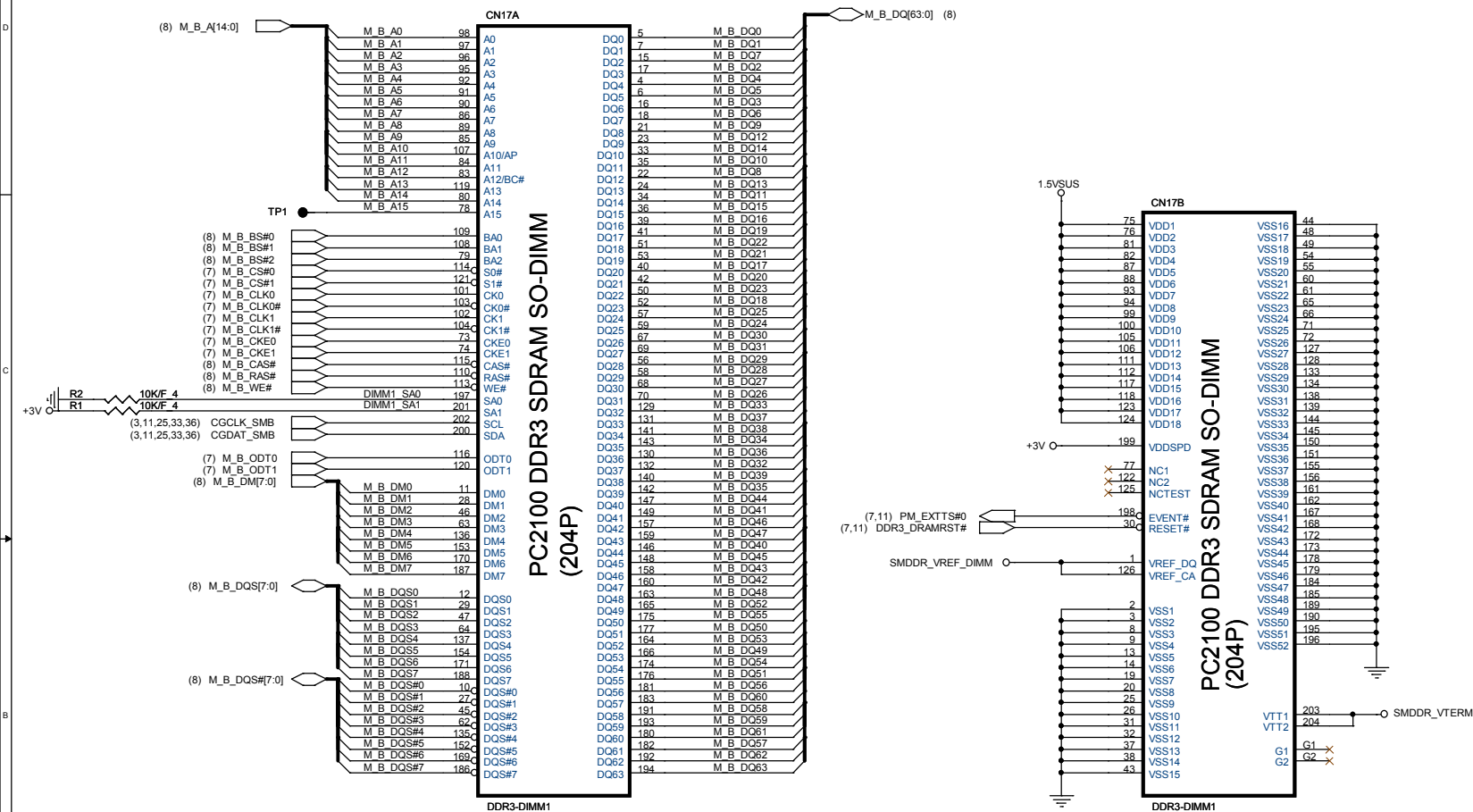
**PROJECT : KL1**  
**Quanta Computer Inc.**

Size Custom Document Number Cantiga DDR3 3/5 Rev A1A  
Date: Friday, March 06, 2009 Sheet 8 of 43

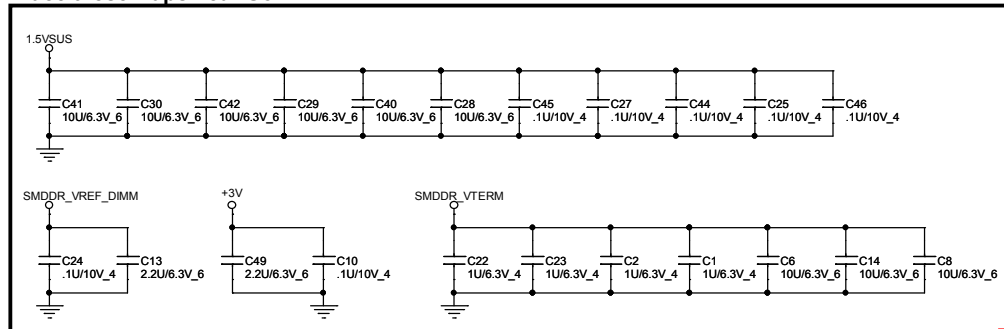








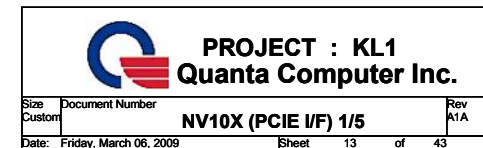
## Place these Caps near So-Dimm1

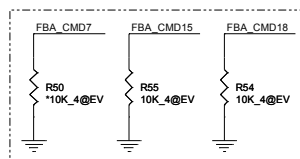
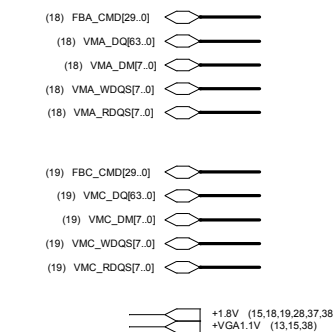
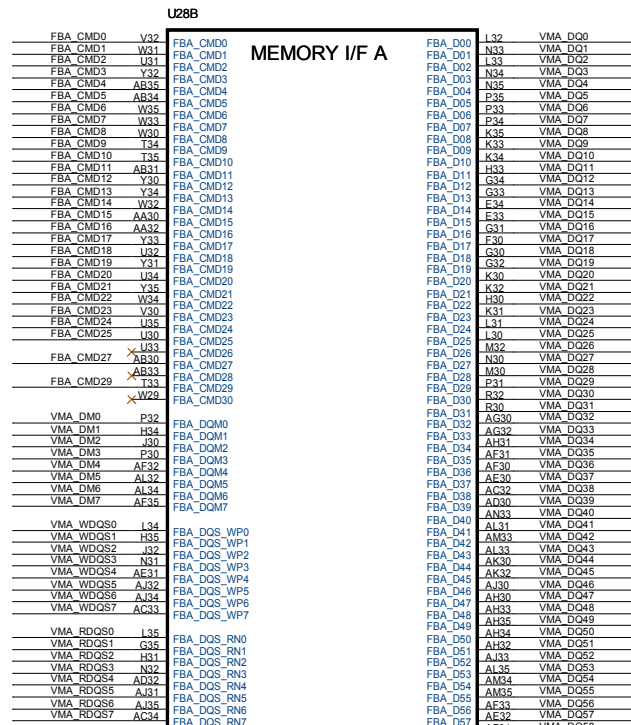


**PROJECT : KL1**  
**Quanta Computer Inc.**

Size: Custom  
 Document Number: **DDR3 DIMM-1(H=9.2)**  
 Date: Friday, March 07, 2020  
 Sheet: 12 of 43

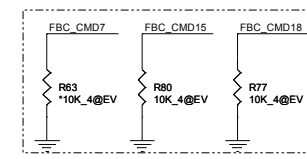
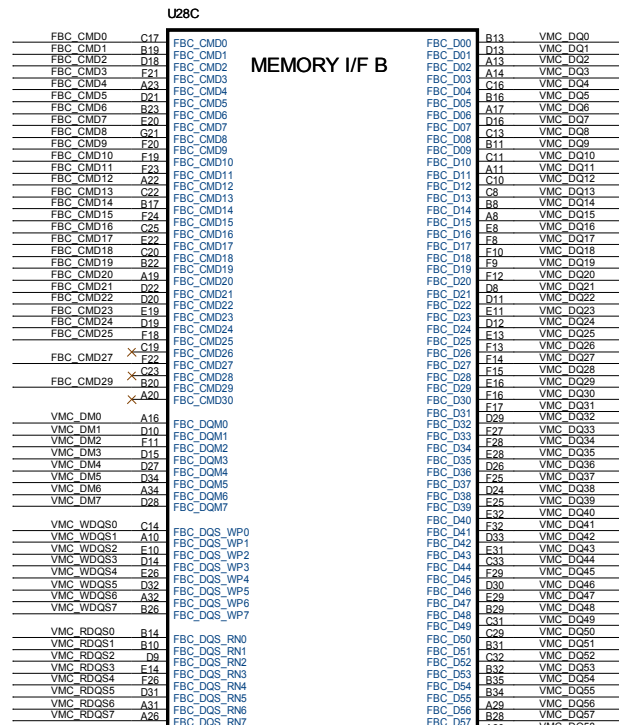
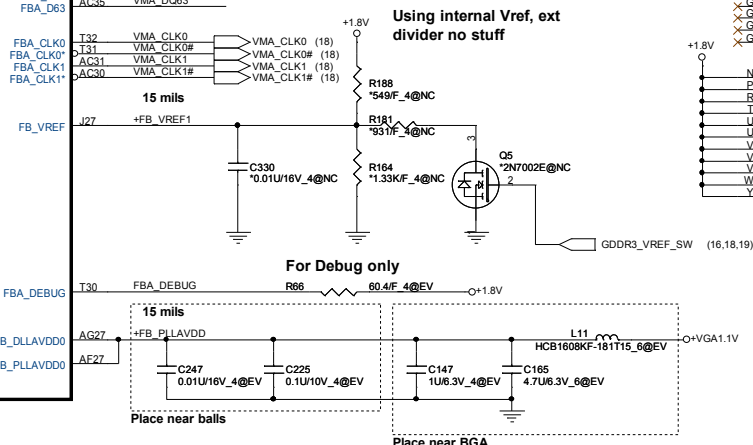
Rev: A1A





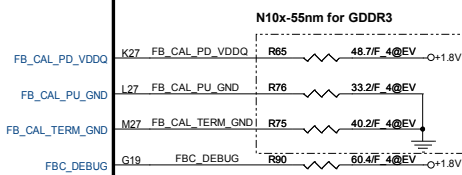
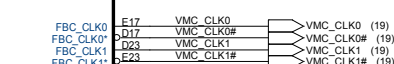
**N10x     55nm / 40nm**

R50	NC	10K
R55	10K	10K
R54	10K	10K

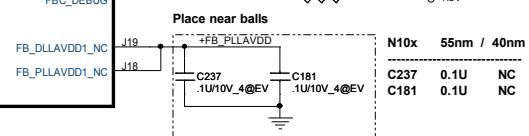


**N10x    55nm / 40nm**

R63	NC	10K
R80	10K	10K
R77	10K	10K



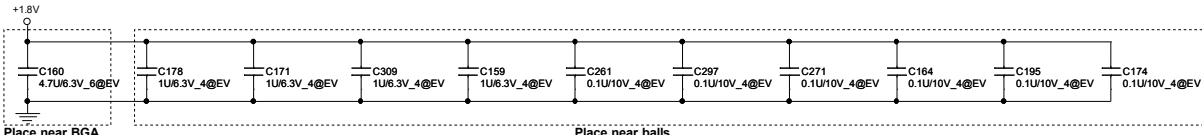
**N10x-55nm for GDDR3**

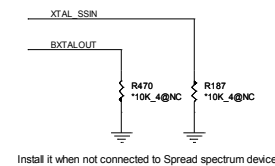
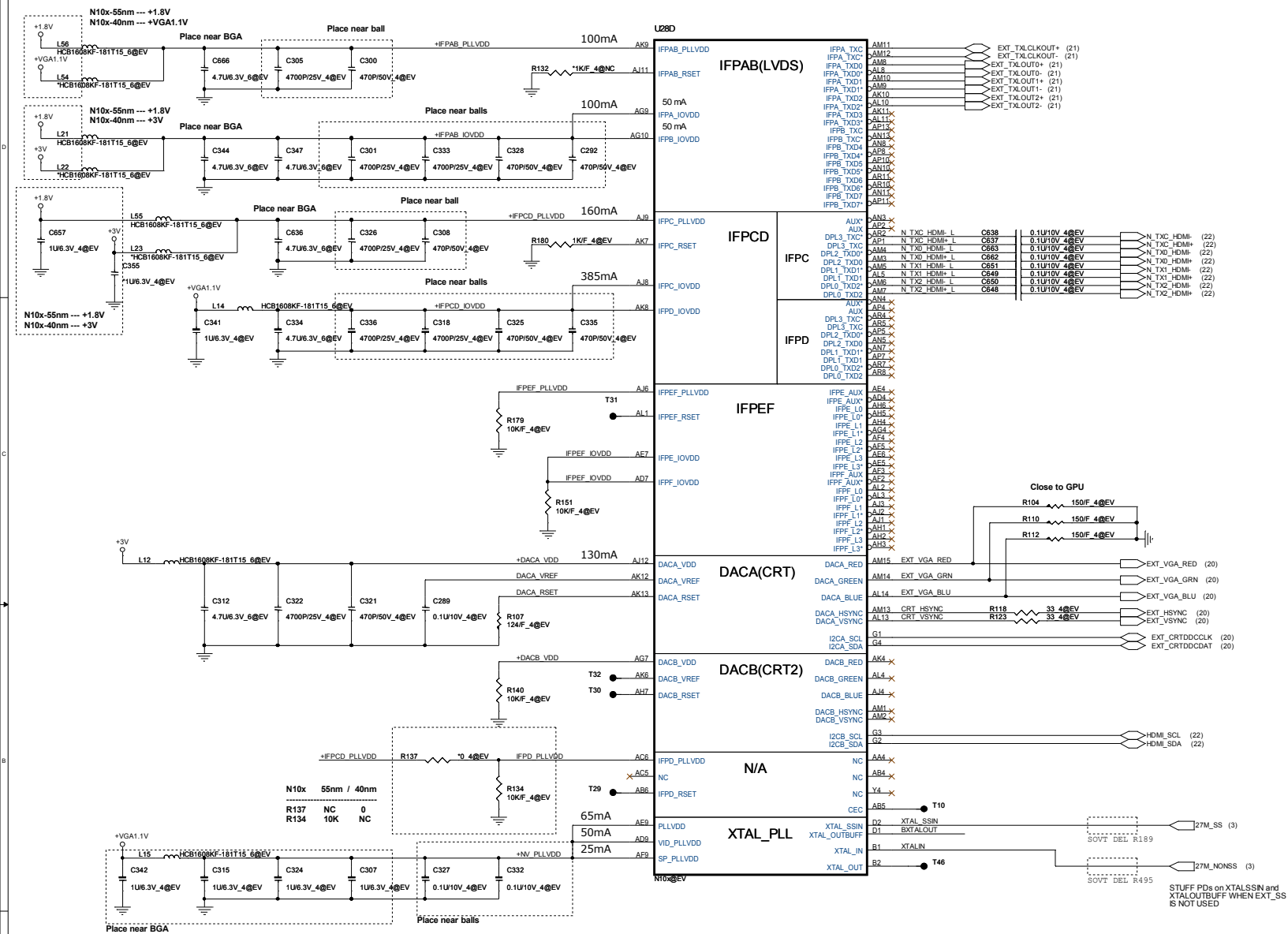


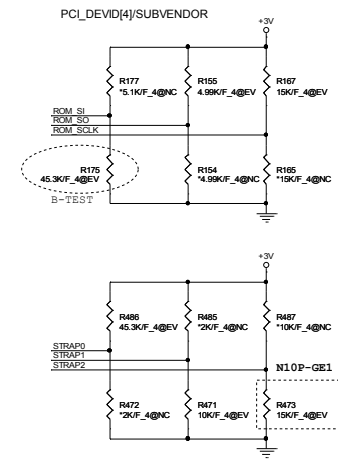
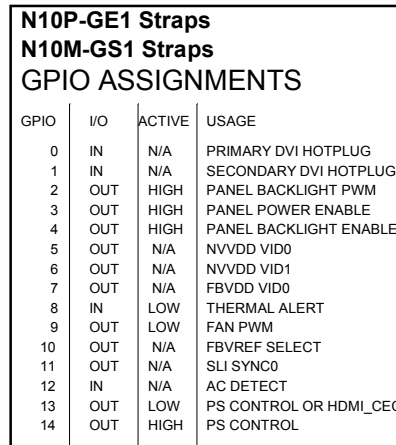
N10x 55nm / 40nm

N10x	55nm / 40nm
C237	0.1U NC
C124	0.1U NC

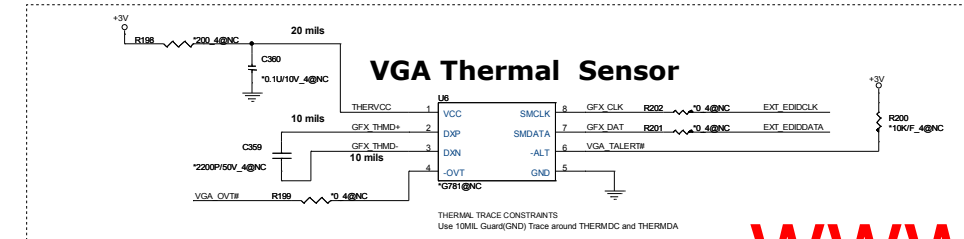
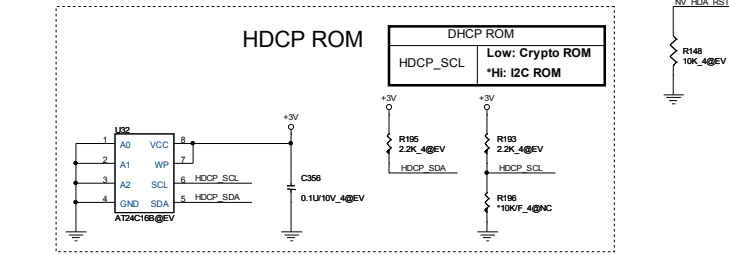
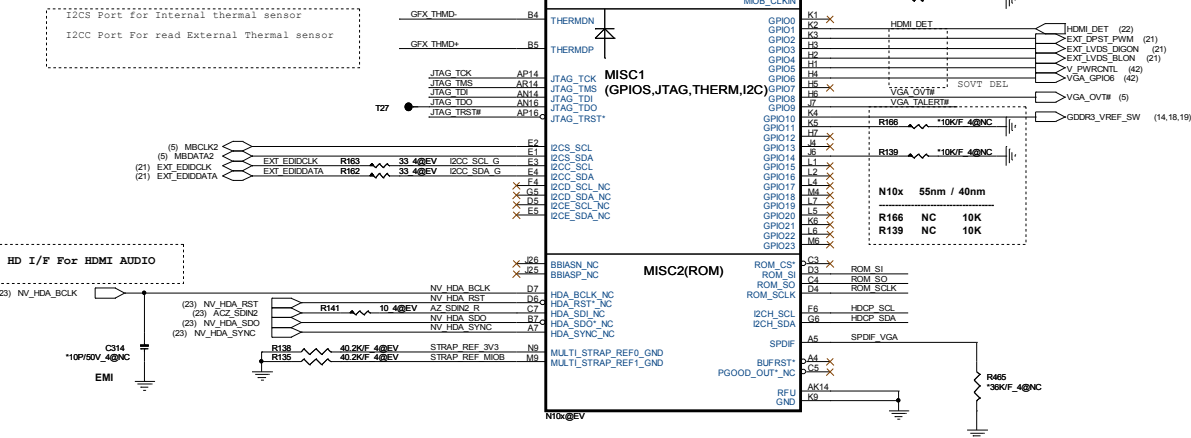
	N10M-55nm N10P-55nm	N10M-40nm N10P-40nm
Signal Name	GDDR3	GDDR3
FBCAL_PD_VDDQ	48.7 ohm	
FBCAL_PU_GND	33.2 ohm	
FBCAL_TERM_GND	40.2 ohm	







N10P-GE1 55nm / 40nm		N10M-GS1 55nm / 40nm	
R167	15K/F	R167	15K/F
R165	NC	R165	NC
R487	NC	R487	NC
R473	15K/F	R473	10K/F

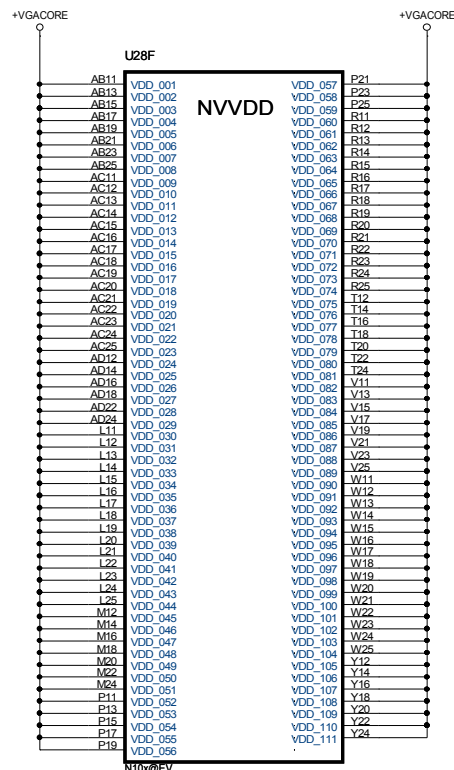


```
STRAP TABLE
STRAP0: USER[3:0]
STRAP1: 3GIO PADCFG[3:0]
STRAP2: PCI DEVID[3:0]
ROM SC1LK: PCI DEVID EXT, SUB VENDOR, SLOT CLK CFG, PEX PLL EN TERM
ROM SI: RAMCFG[3:0]
ROM SO: XCLK 417, FB 0 BAR SIZE, SMB ALT ADDR, VGA DEVICE
```

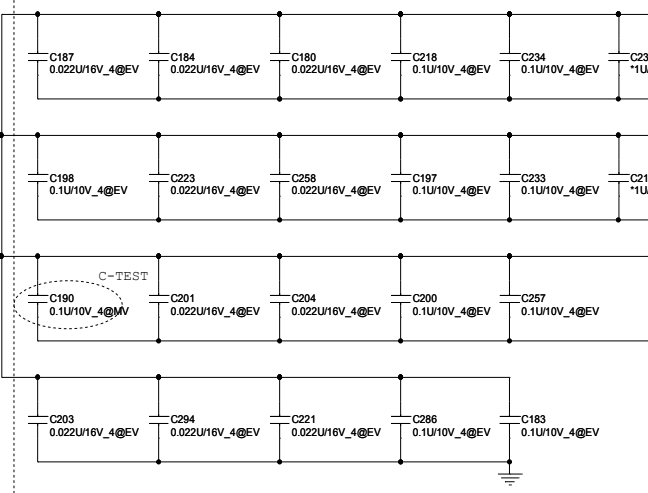
```
KL1 STRAP FUNCTION MAPPING
USER[3:0]: 1111
3GIO PADCFG[3:0]: 0001 NoteBook
PCI DEVID[3:0]: 0001
SUB VENDOR: 0 No Vedio BIOS ROM
SLOT CLK CLG: 1 GPU AND MCH USE COMMON REF CLOCK
PEX PLL EN TERM: 0 DISABLE PEX PLL TERMINATION
RAMCFG[3:0]: 0000 AND 0001
XCLK 417: 1 USING 27MHZ
FB 0 BAR SIZE:
SMB ALT ADDR:
VGA DEVICE:
```

ROM SI	RAMCFG LSIT:	
PD_R175:45K/F	0111	SAMSUNG K4J10324QD-HC12 32M32b * 4PCS
PD_R175:30K/F	0101	QIMONDA HYB18H1G321AF-11 32M32b * 2PCS

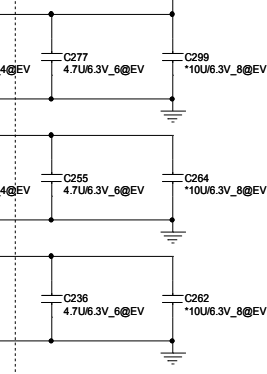
# NVVDD Decoupling



Place near balls



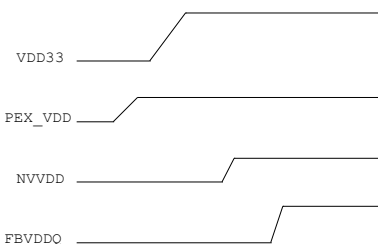
Place near BGA



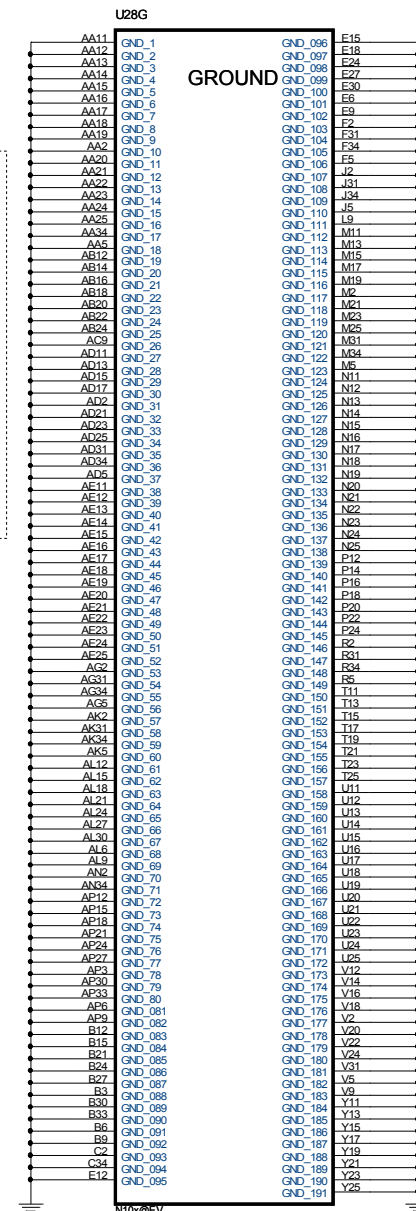
N10x	55nm	40nm
C187	0.022U	0.01U
C198	0.1U	0.01U
C190	0.1U	0.01U
C235	NC	1U
C217	NC	1U
C277	4.7U	1U
C255	4.7U	4.7U
C236	4.7U	NC
C299	NC	10U
C264	NC	10U
C262	NC	10U

N10P-GE1: +VGACORE +0.90V (Normal)

power up sequence



+VGACORE (37,38,42)



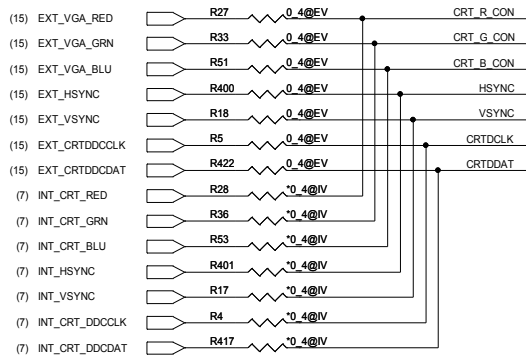
PROJECT : KL1  
Quanta Computer Inc.

Size Custom Document Number  
Date: Friday, March 06, 2009 Sheet 17 of 43  
Rev A1A

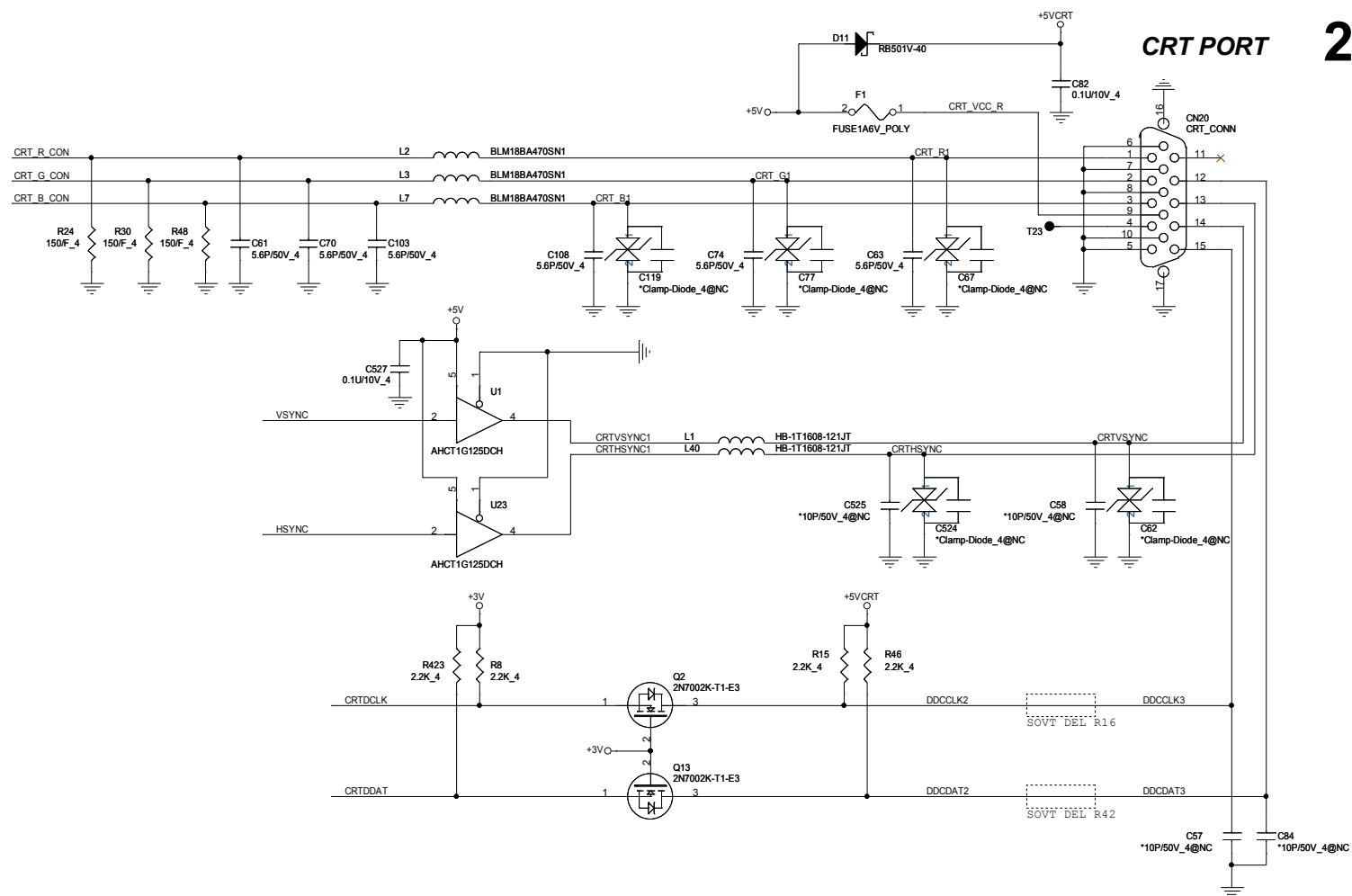




## CRT SWITCH

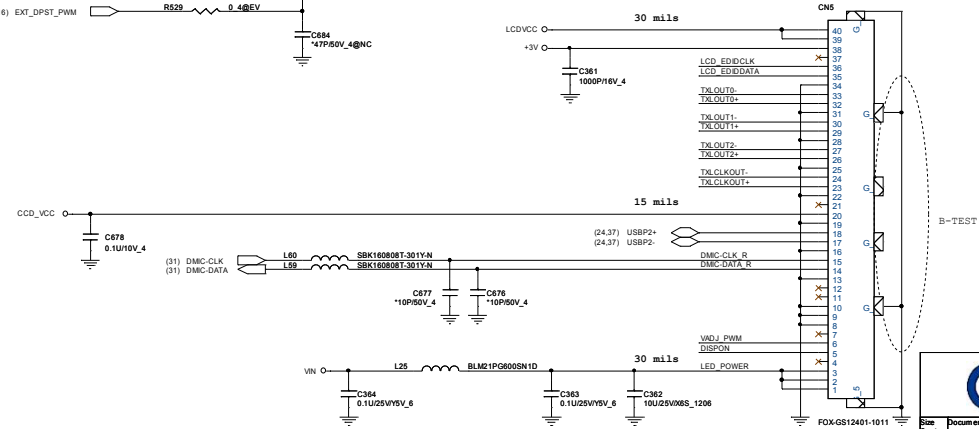
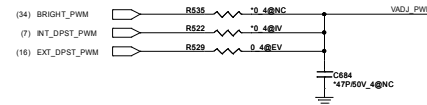
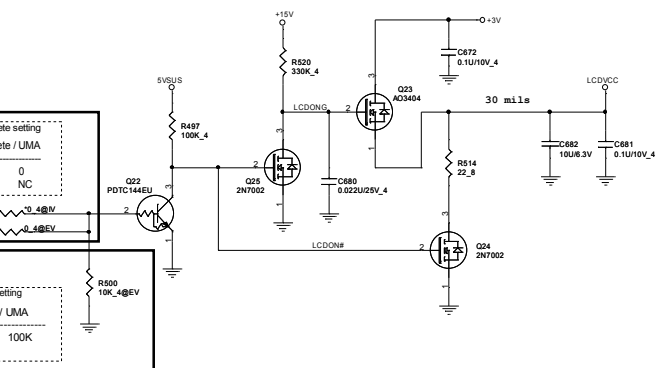
UMA & Discrete setting  
LVDS Discrete / UMA

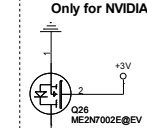
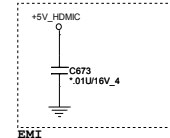
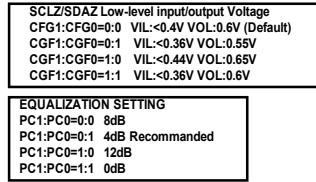
R27	0	NC
R33	0	NC
R51	0	NC
R400	0	NC
R18	0	NC
R5	0	NC
R422	0	NC
R28	NC	0
R36	NC	0
R53	NC	0
R401	NC	0
R17	NC	0
R4	NC	0
R417	NC	0



PROJECT : KL1  
Quanta Computer Inc.

Size Custom Document Number CRT CONN Rev A1A  
Date: Friday, March 06, 2009 Sheet 20 of 43







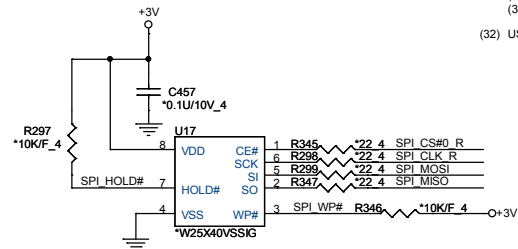
EXPRESS CARD (NEW CARD)

MINI CARD PCI-E (WWAN)

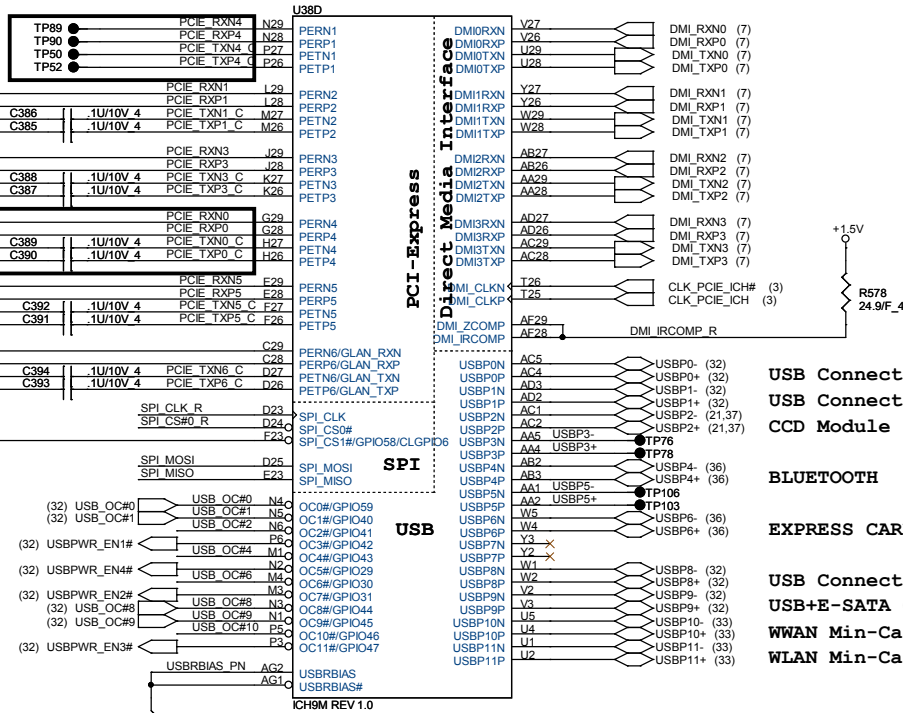
MINI CARD PCI-E (WLAN)

MINI CARD PCI-E (CARD)

PCI-E-LAN



512K byte SPI ROM  
For HDCP only

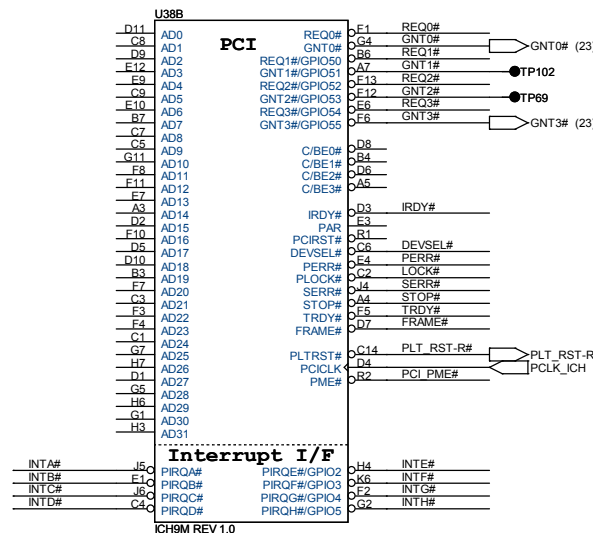
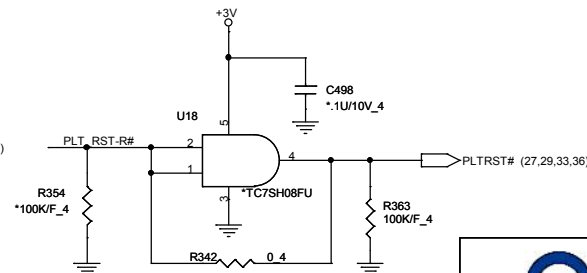
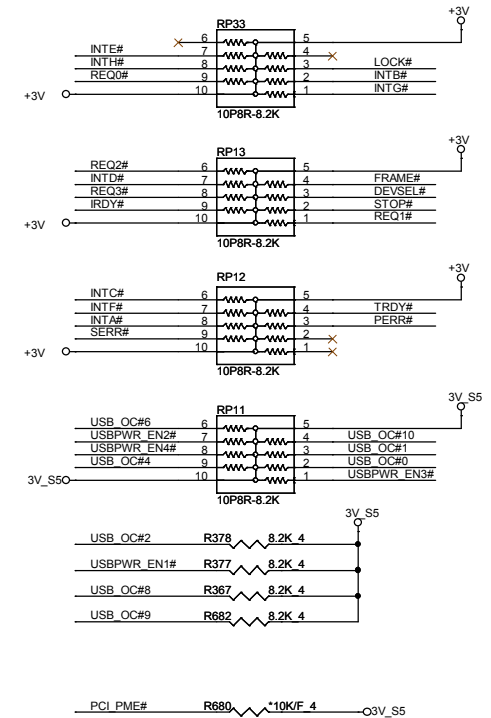


USB Connector  
USB Connector  
CCD Module

BLUETOOTH

EXPRESS CARD

USB Connector  
USB+E-SATA Connector  
WWAN Min-Card  
WLAN Min-Card

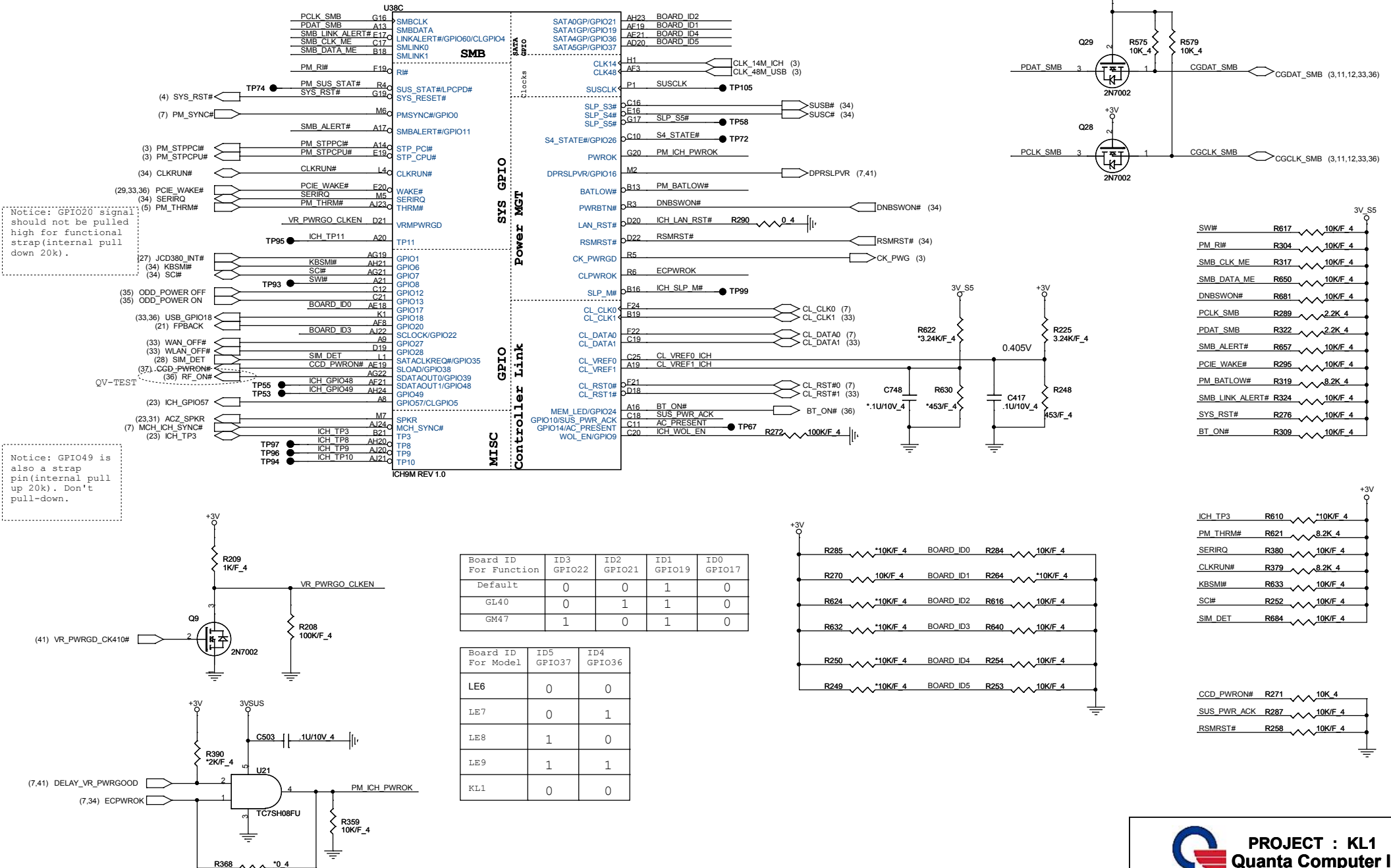


ICH9M REV1.0



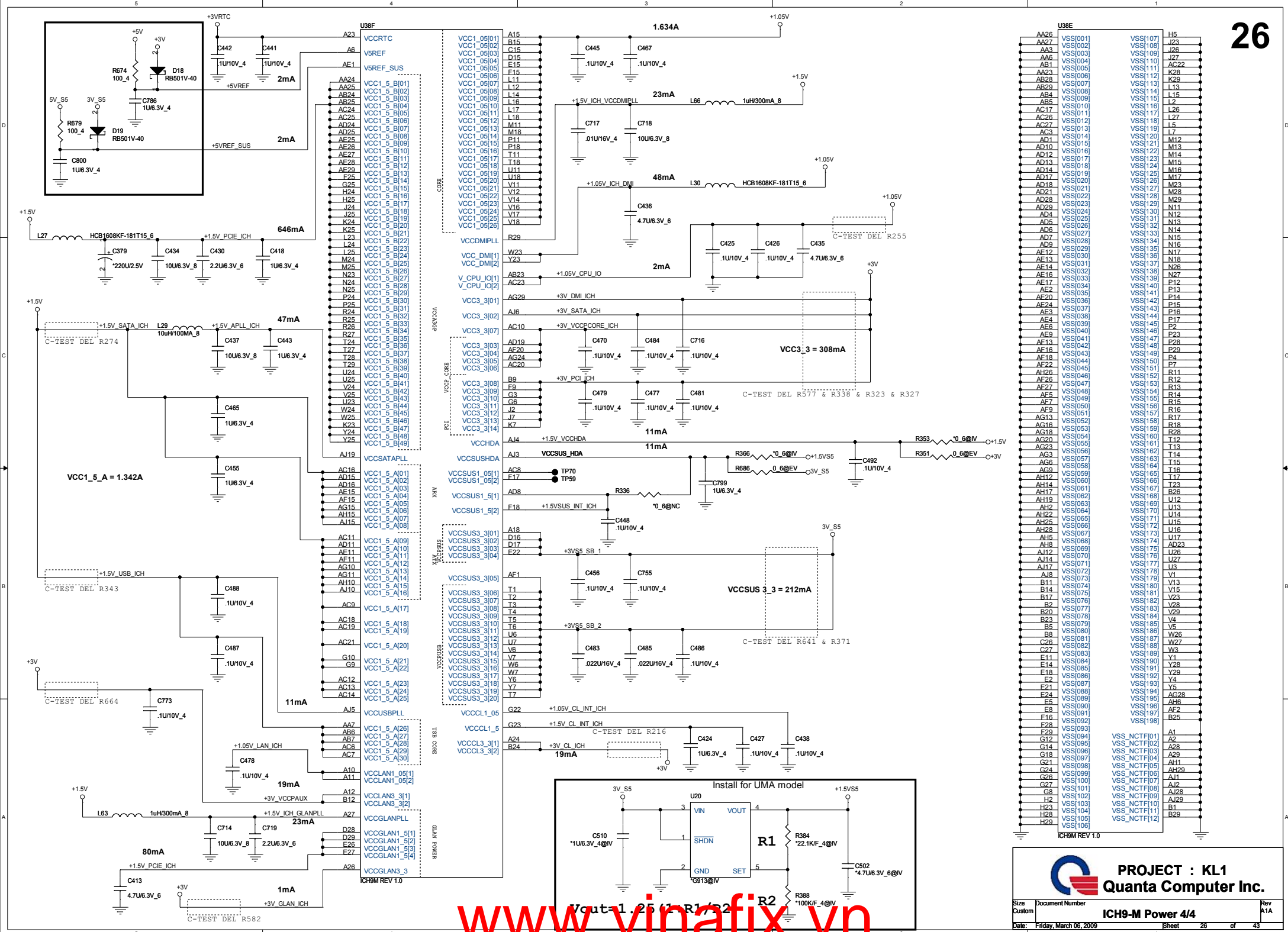
PROJECT : KL1  
Quanta Computer Inc.

(3,5,7,10,11,12,13,15,16,20,21,22,23,24,26,27,28,29,30,31,33,34,35,36,37,38,40,41) +3V  
(23,24,26,38) 3V\_S5  
(33,34,36,38,39,41,42) 3VSUS



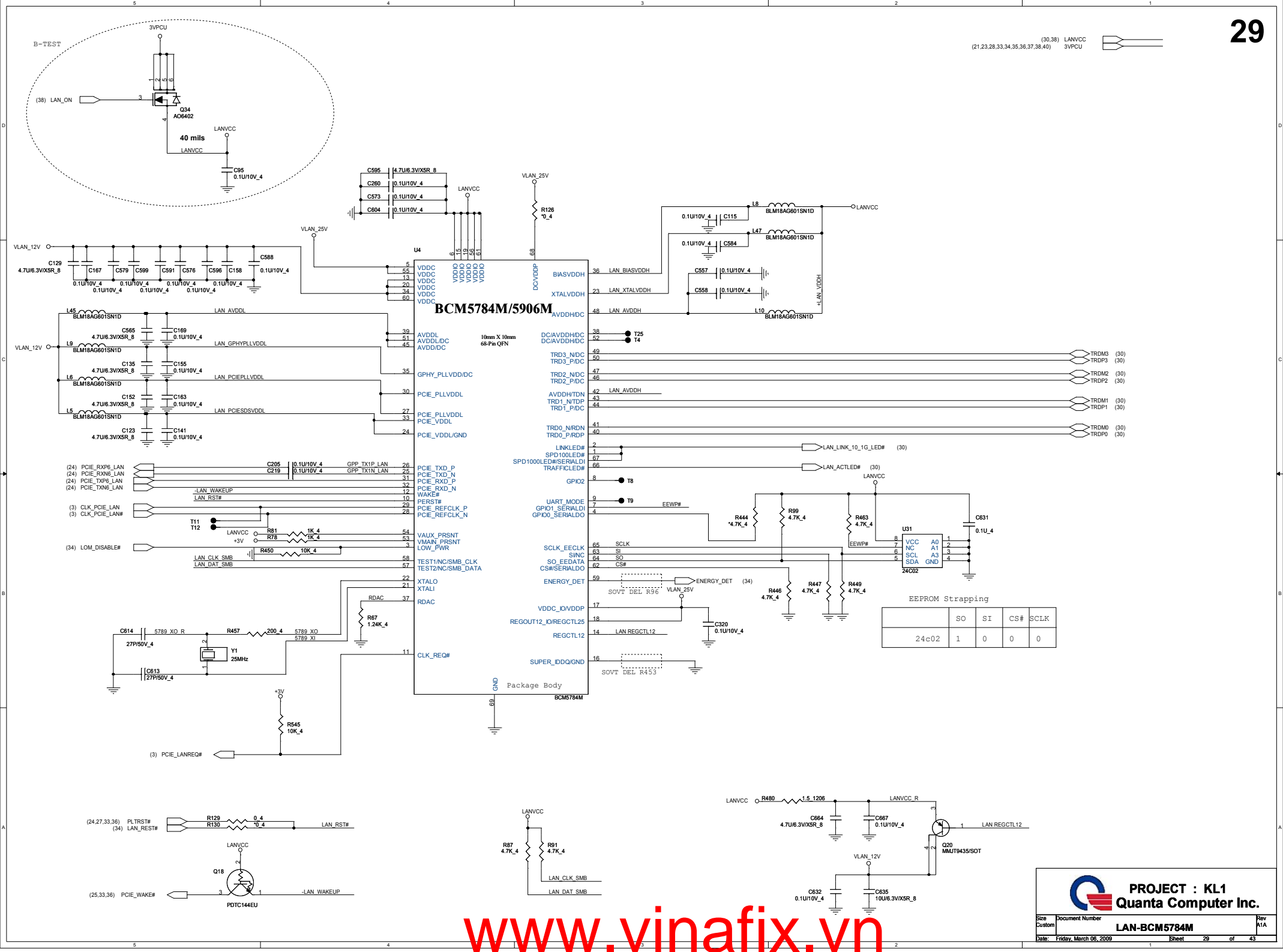
Board ID For Function	ID3 GPIO22	ID2 GPIO21	ID1 GPIO19	ID0 GPIO17
Default	0	0	1	0
GL40	0	1	1	0
GM47	1	0	1	0

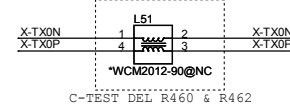
Board ID For Model	ID5 GPIO37	ID4 GPIO36
LE6	0	0
LE7	0	1
LE8	1	0
LE9	1	1
KL1	0	0











LAN\_VCC O  $R_{466}$  150.4 LAN\_ACTLED# R 9 9+

(29) LAN\_ACTLED#

X-TX0P	1
X-TX0N	2
X-TX1P	3
X-TX2P	4
X-TX2N	5
X-TX1N	6
X-TX3P	7
X-TX3N	8

LAN\_VCC O  $R_{125}$  150.4 LAN\_LINK\_10\_1G\_LED# R 11 11+

(29) LAN\_LINK\_10\_1G\_LED#

12 12+

CN22

AOP-C100K4-108M-L

G3 15

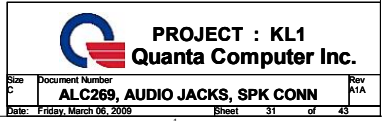
G4 16

G1 17

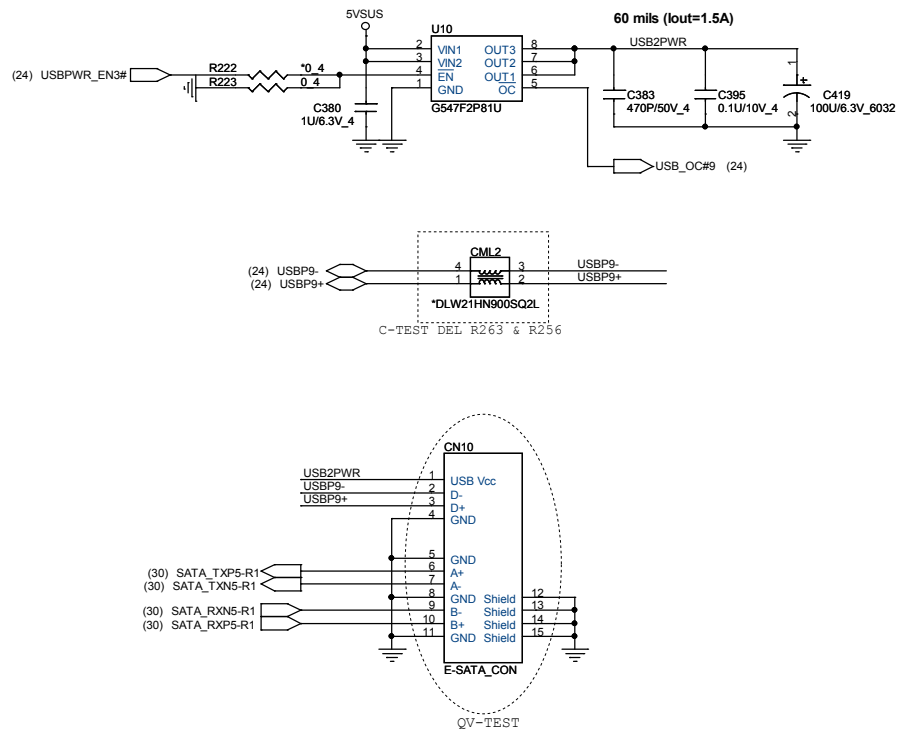
G2 14

Ground

EN	B0	B1	FUNCTION
0	X	X	Standby
1	0	0	Standard SATA Output
1	1	0	Ch 0 Boost Output
1	0	1	Ch 1 Boost Output
1	1	1	Ch 0.1 Boost Output

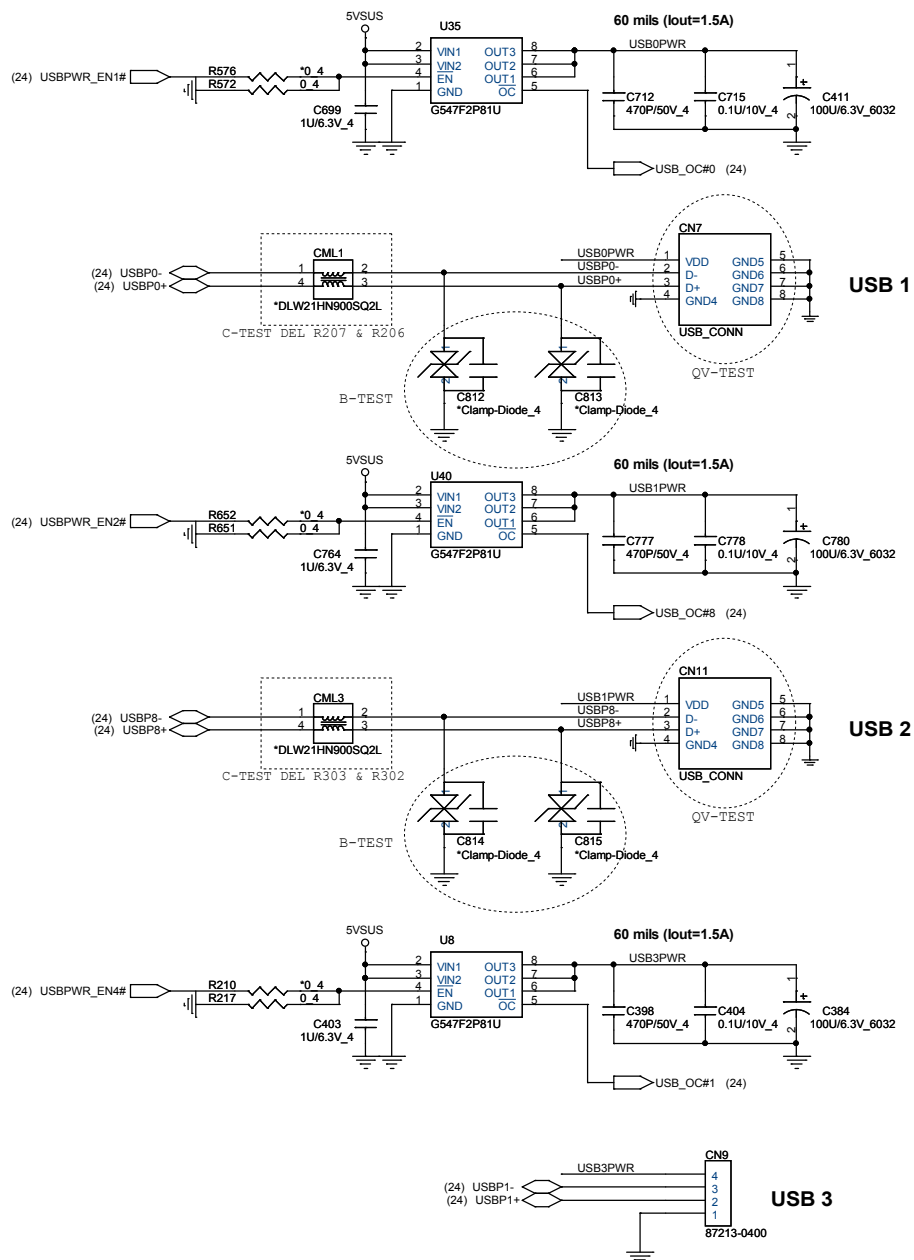


## USB + eSATA CONNECTOR

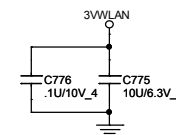
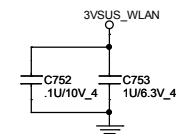
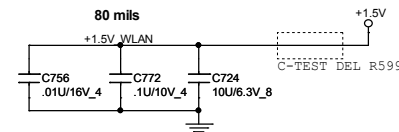


## USBX3

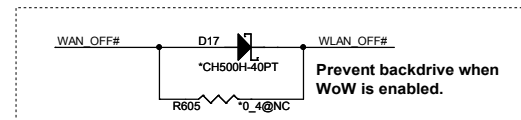
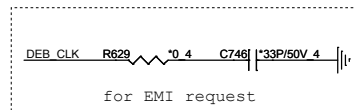
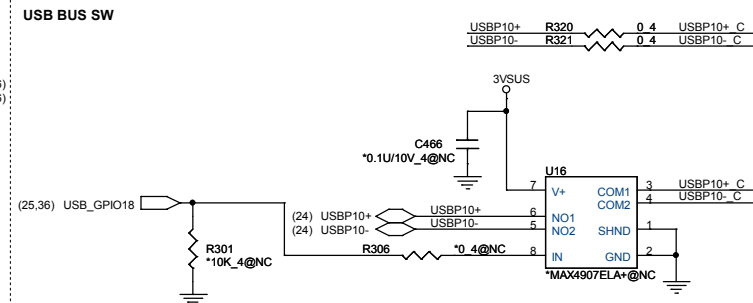
32



## 33

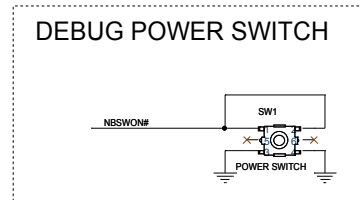


```
INTEL WLAN
CARD PIN 20
W_DISABLE#
have
internal
pull-up 110k
ohm
```

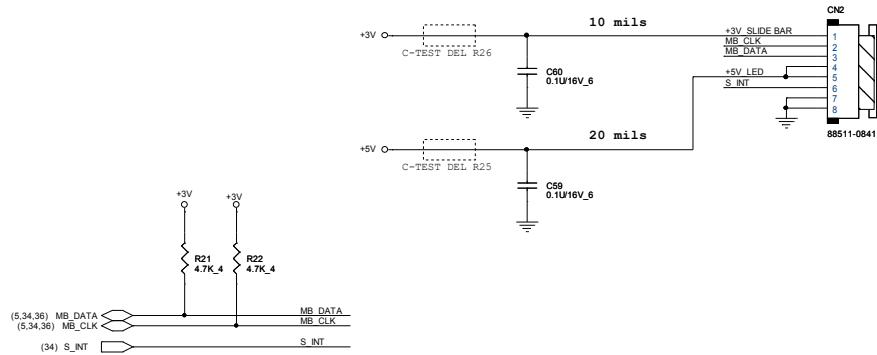
[illegible]

**PROJECT : KL1**  
**Quanta Computer Inc.**

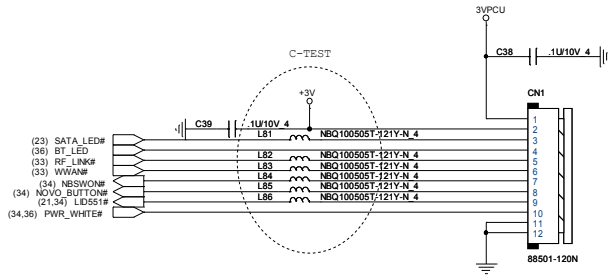
Size Custom	Document Number	<b>WLAN &amp; WWAN CONN</b>			Rev A1
Date:	Friday, March 06, 2009		Sheet	33	of 43



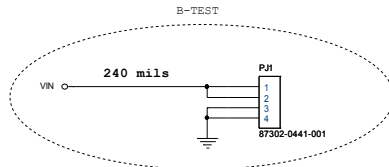
# SLIDE BAR CONN



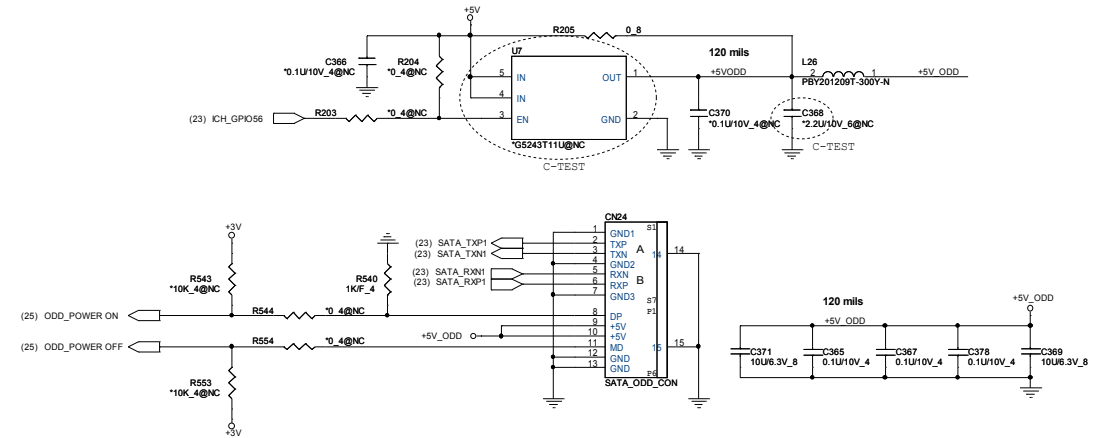
# POWER BUTTON/B CONN



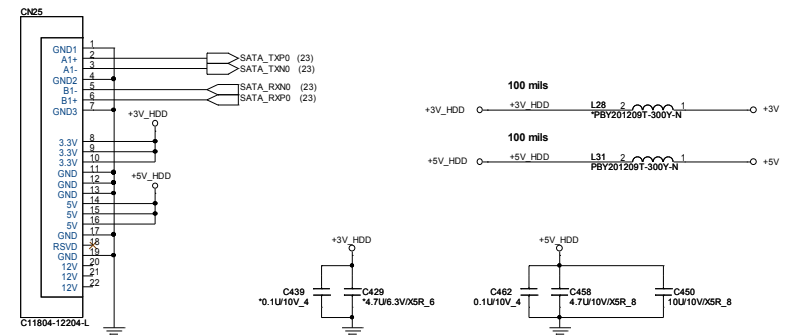
# VIN CABLE CONN

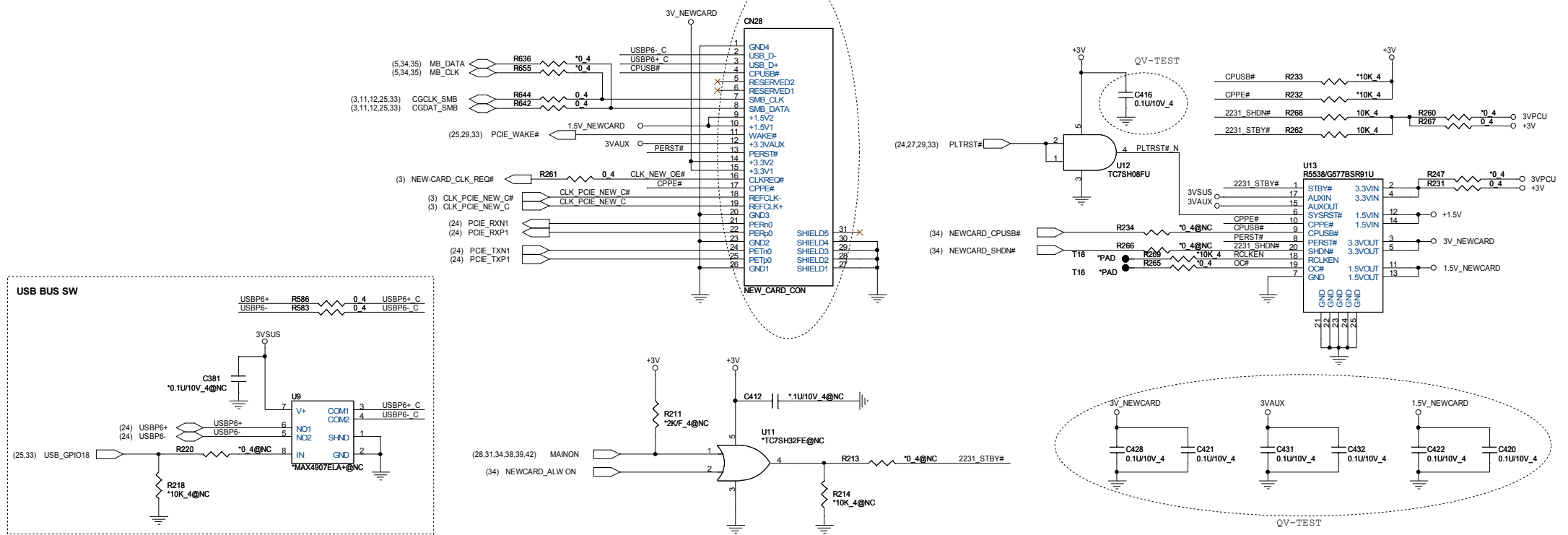


# SATA CD-ROM

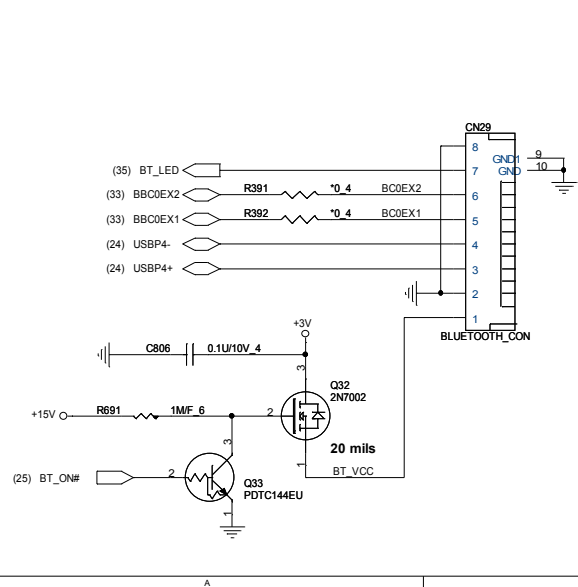


# SATA-HDD CONNECTOR

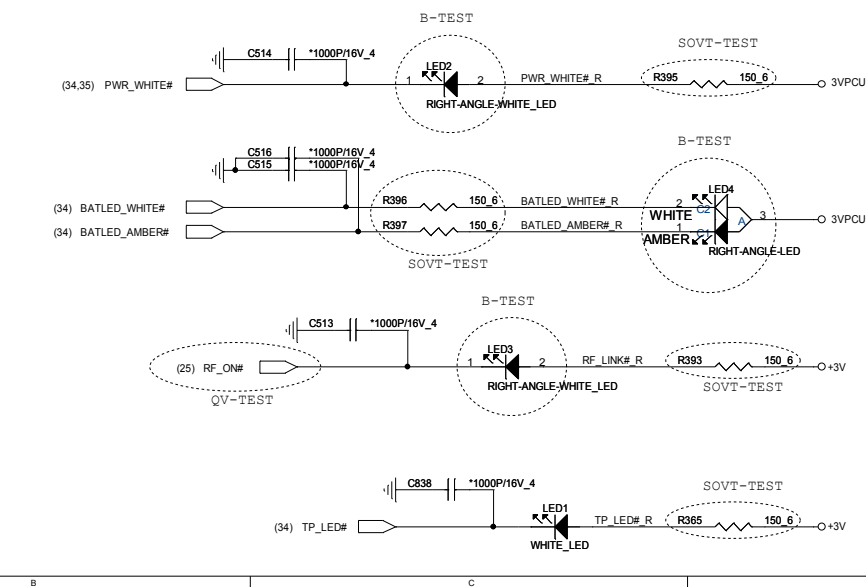




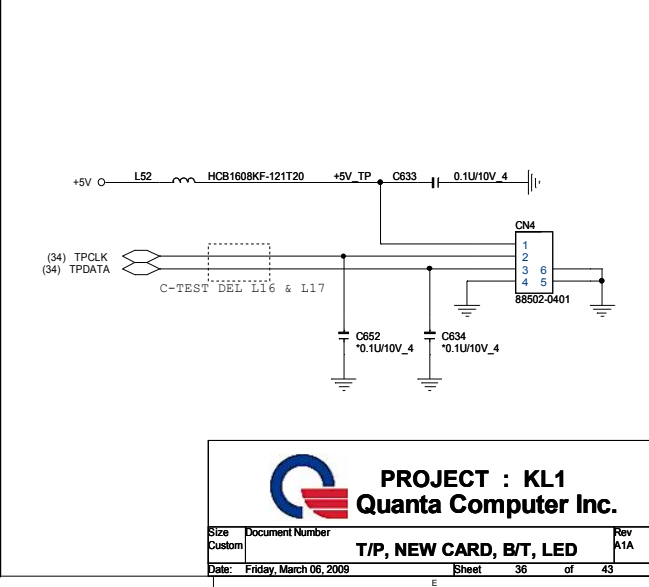
## BLUETOOTH



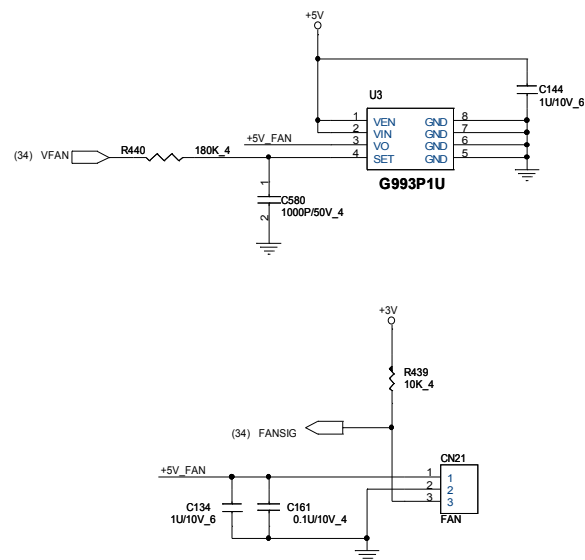
## LED



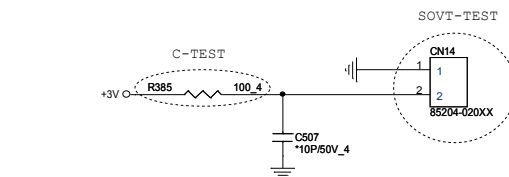
## TOUCH PAD



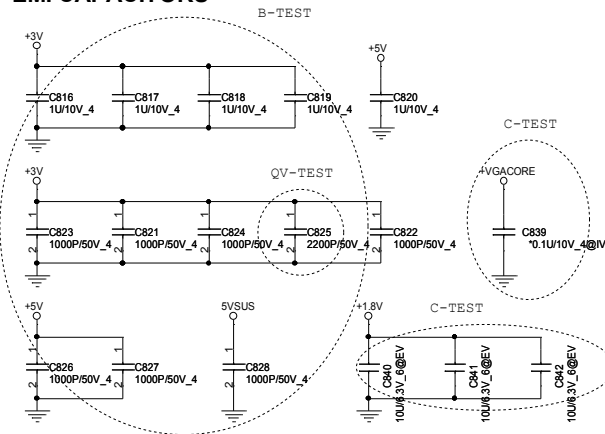
## FAN CONTROL



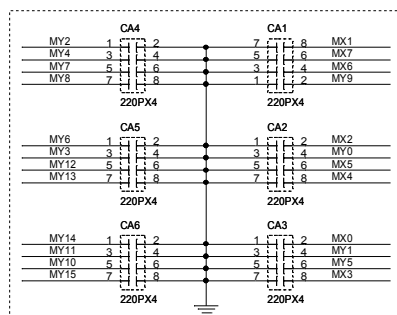
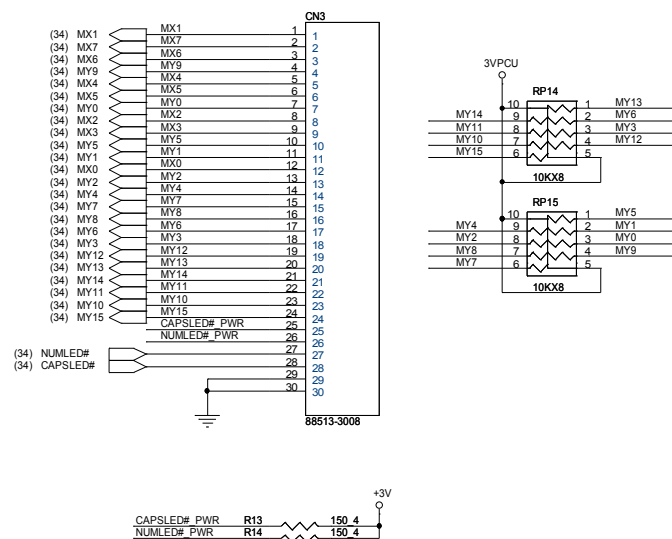
## Logo LED CONN



## EMI CAPACITORS

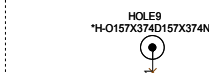


## KEYBOARD



For EMI request

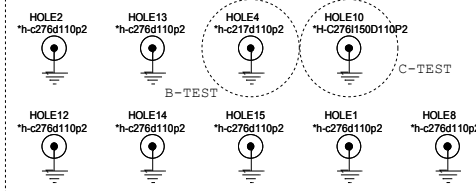
## WLAN & WWAN CABLE HOLE (NON-PTH)



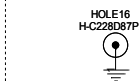
## (NON-PTH)



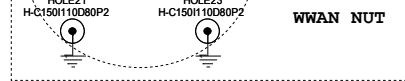
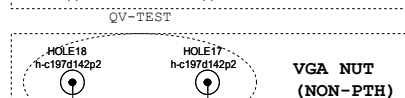
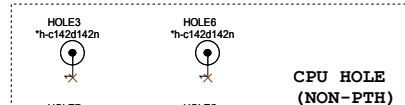
## M/B SCREW HOLE



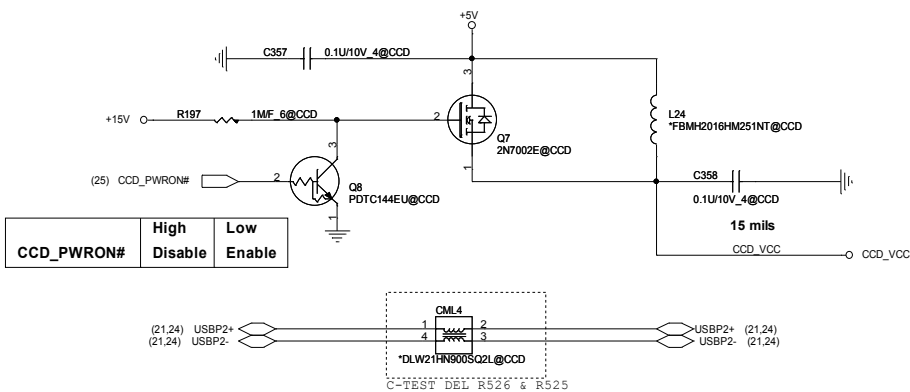
## CHARGER+SIM/B NUT



## POWER/B NUT



## CCD MODULE

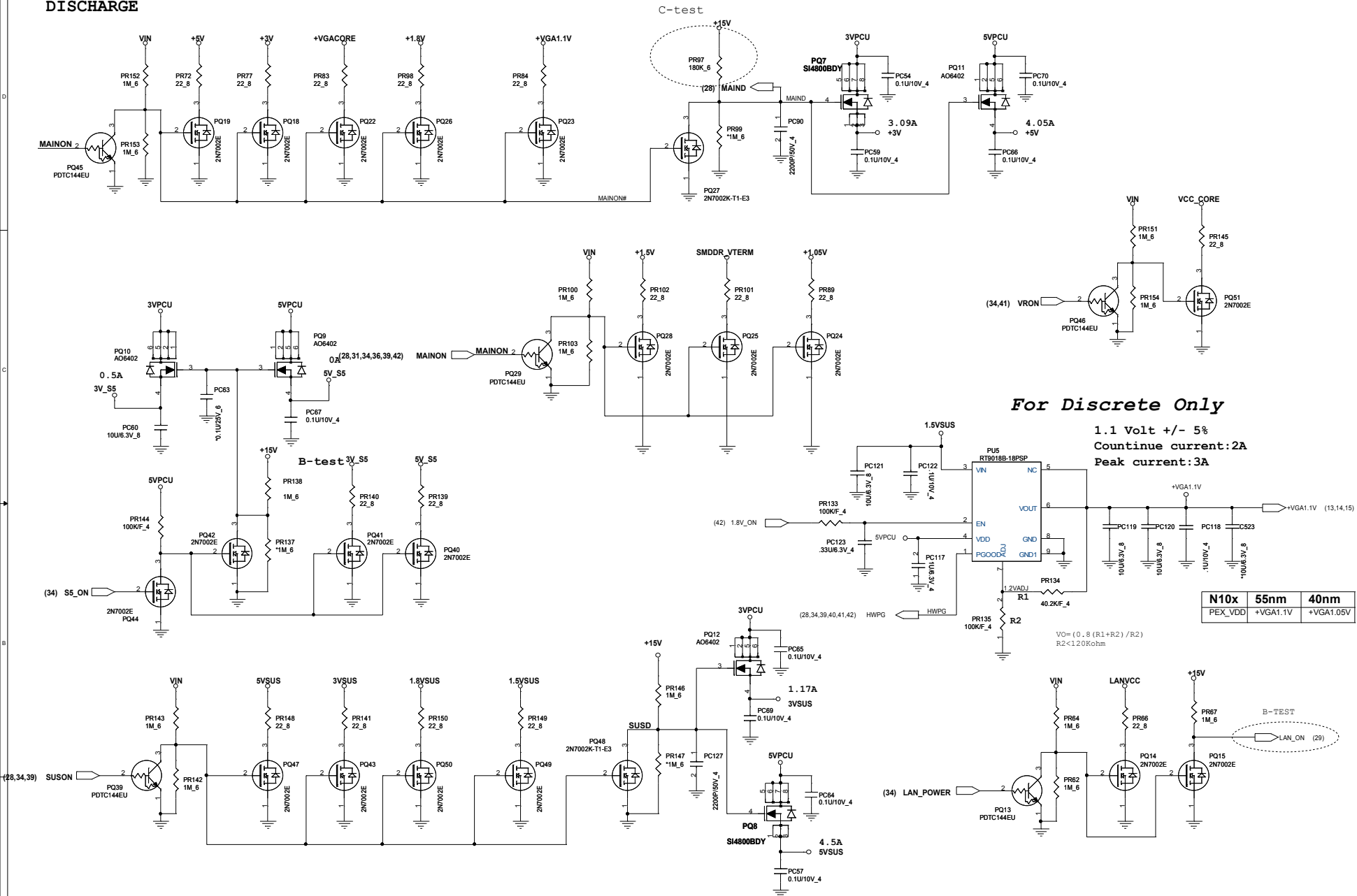


CCD_PWRON#	High	Low
	Disable	Enable

**PROJECT : KL1**  
**Quanta Computer Inc.**

Size Custom Document Number **FAN & K/B CONN, CCD, HOLES, EMI** Rev A1A  
Date: Friday, March 06, 2009 Sheet 37 of 43

## DISCHARGE

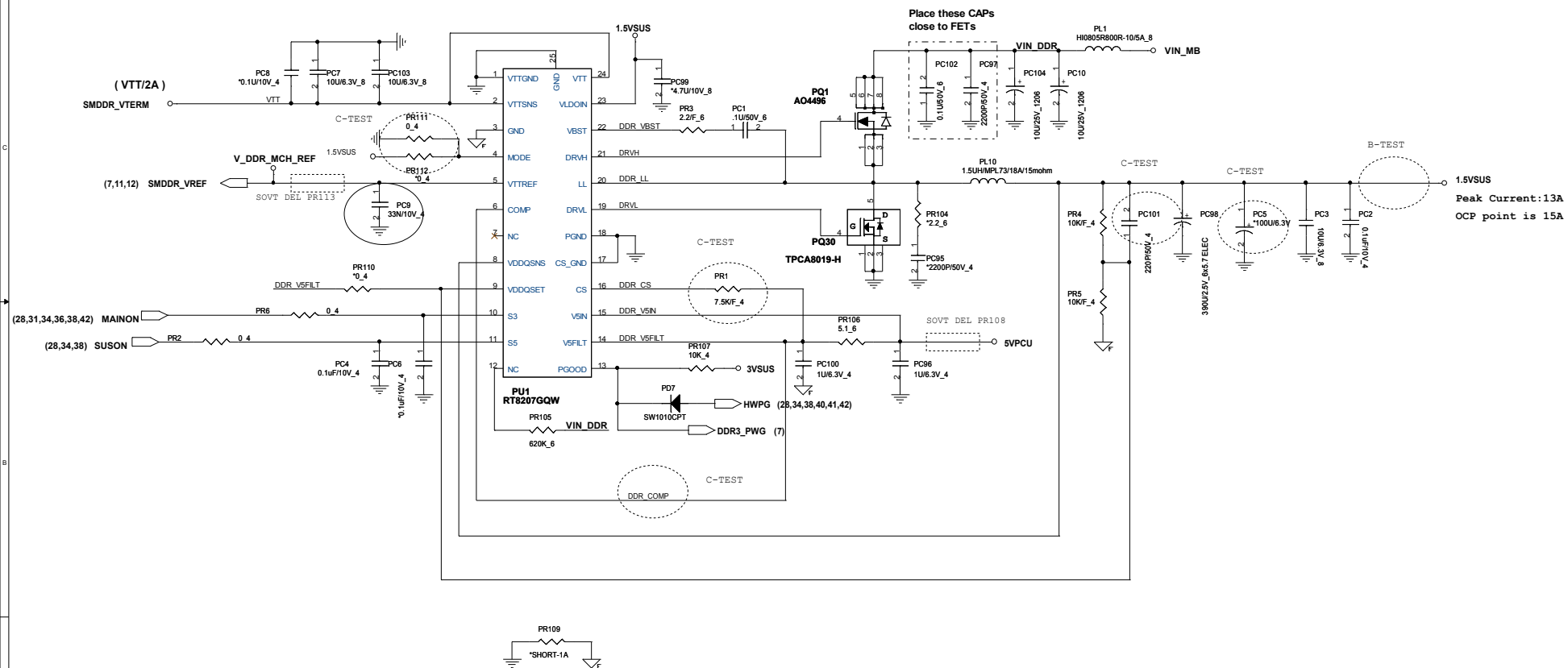


*For Discrete Only*

1.1 Volt +/- 5%  
Countinue current:2A  
Peak current:3A

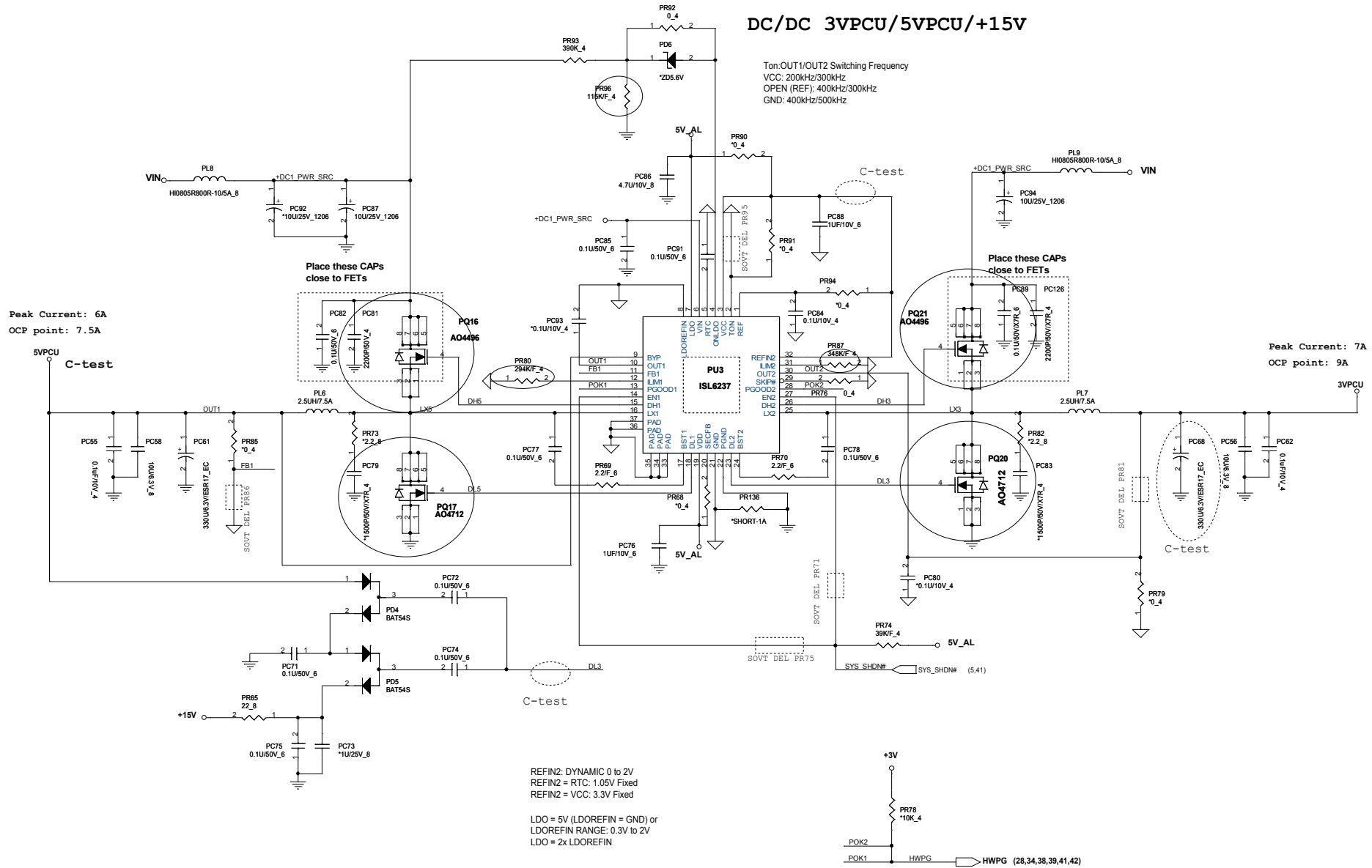
<b>N10x</b>	<b>55nm</b>	<b>40nm</b>
PEX_VDD	+VGA1.1V	+VGA1.05V

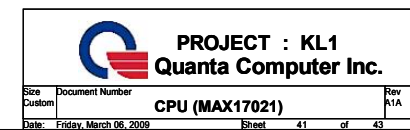
$$R2 < 120 \text{Kohm}$$

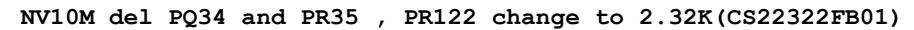


DC/DC 3VPCU/5VPCU/+15V

Ton:OUT1/OUT2 Switching Frequency  
VCC: 200kHz/300kHz  
OPEN (REF): 400kHz/300kHz  
GND: 400kHz/500kHz





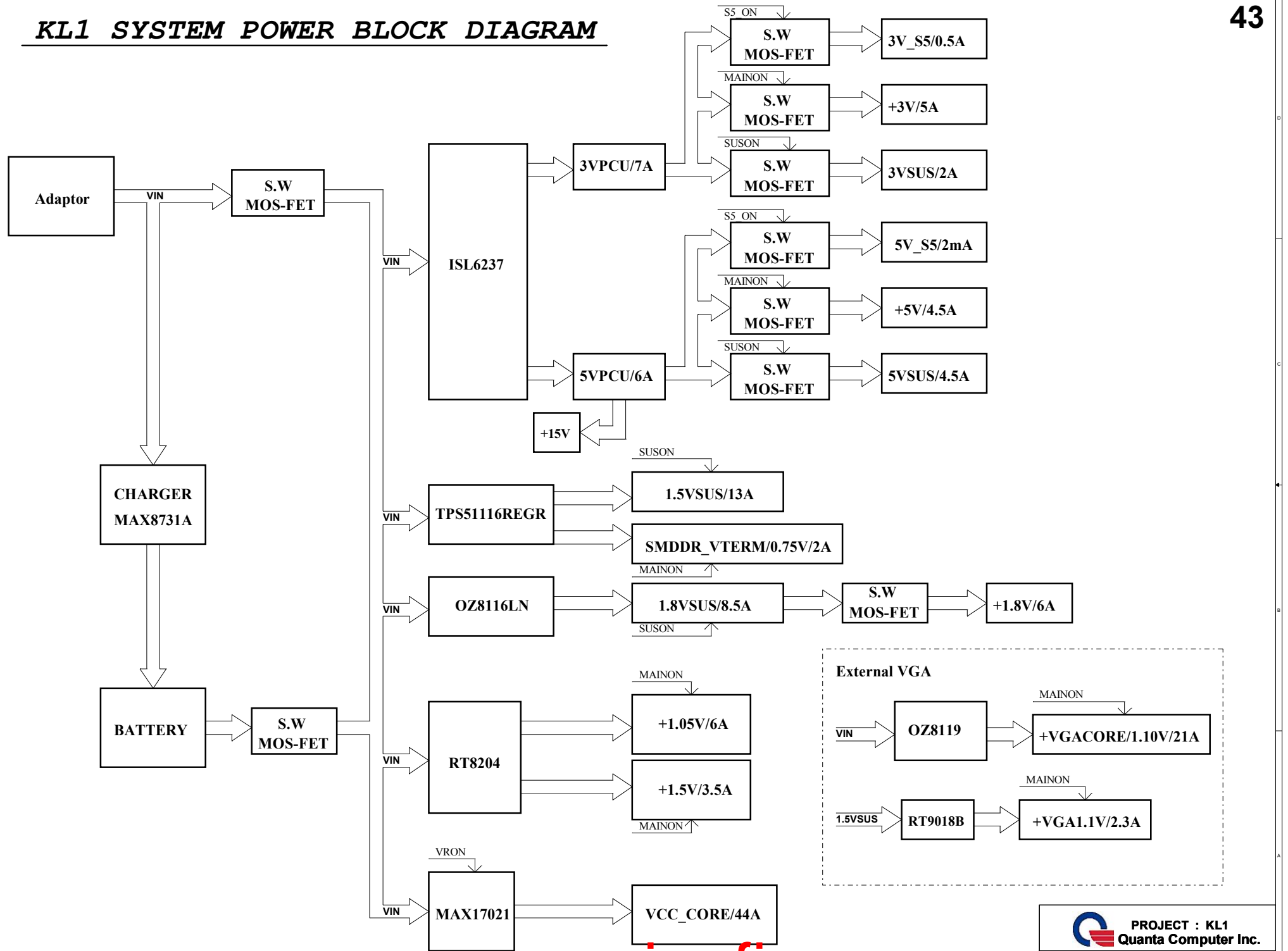


V_PWRCNTL		N10P-GE1	N10M-GS1
	PR15	56K/F P/N:CS35602FB11	47K/F P/N:CS34702FB11
	PR23	150K/F P/N:CS41502FB18	1.43M/F P/N:CS51432FB10
	PR120	82.5K/F P/N:CS38252FB17	93.1K/F P/N:CS39312FB15
	Low	0.9V	0.9V
	High	1.10V	0.92V

N10x	VGA_GPIO6 GPIO6	V_PWRCNTL GPIO5	PERFORMANCE STATE	N10P-GE1	N10M-GS1
55nm	Low	Low	HD DVD/SD DVD/MAX BAT	0.9V	0.9V
	High	High	MAX PERFORMANCE	1.10V	0.92V
40nm					

# KL1 SYSTEM POWER BLOCK DIAGRAM

43



www.vinafix.vn