TIGD-CI3 V : 1.1

SCHEMATICS TABLE:

Design Guide: Doc#417605 Ver:2.5

CRB: Doc#439675 Ver:1.0

REVISION HISTORY:

Rev	Date	Notes
A	2009.11.6	INITIAL RELEASE
1.0	2010.01.11	Page5:R12,R13 change to 39 ohm Fix H/VSYNC overshot & undershoot
	2010.01.11	Page5:+VCC change to +VGA_VCC ,and BC3 change to 1U For VGA noise
	2010.01.11	Page7:add BC133 for DC noise
	2010.01.11	Page8:add R234 pull high GPIO36
	2010.01.11	Page9:R271 change to 47 ohm for clock SI
	2010.01.11	Page9:Add R379,R309,R266,R252,RN26,RN35,default GPI,If not used,pull high to power
	2010.01.11	Page11:BC165 change to 0603,reserve BC181 for DC noise
	2010.01.11	Page12:ER28 change to 15.4K for OCP test,del EC30,add EC32 close to DIMM
	2010.01.11	Page13:R400,R52,R71,R398,R47 change to 47 ohm,R55,R397 change to 33 ohm for clock SI
	2010.01.11	Page15:add R449,R452,R453,R454 for Discharge,EC3,4,19,20 change to 220U 16V
	2010.01.11	Page16:L12 change footprint,+VCC3 change to +VCORE,Q15 change to 2N3904 for VRM_PWRGD glitch
	2010.01.11	Page17:add R347 for discharge,reserve R392 for disable EUP cost down
	2010.01.11	Page18:EC27 change to 16V value,+VCC3 change to +VCC,R377 change to 150-06,Increase LED brightness
	2010.01.11	Page18:DEL Q47,Q48 change EUP circuit control
	2010.01.11	Page19:BC181 change to 0.022uF for pin78 PWRGD glitch,
	2010.01.11	Page19:+IO_3VSB change to +5VSB,R424 change to 4.7K because power supply internal is 5V
	2010.01.11	Page20:+KBVCC change to +USBPWER1,del F2 FUSE for COST DOWN
	2010.01.11	Page21:MC16,MC27,MC28 change to 4.7U-X5R for EVDD12,DVDD12 DC noise
	2010.01.11	Page22:+5VSB change to +ATX_5VSB,D42 SS14 change to D24 BAT54 for power on noise (enable EUP)
	2010.01.11	Page22:add Q47,reserve R97 for +5VA leakage current to 12V & ground through 7805
CI3 V.A	2010.04.02	Page6:modify +V_1P8_PLLSFR circuit
	2010.04.02	Page11:change DDR2 to DDR3 slot & circuit
	2010.04.02	Page12:change DDR3 voltage to 1.5V level
	2010.04.02	Page17:modify +V_1P5,+V_1P05 LDO circuit
CI3 V.B	2010.05.13	Page07:ADD L18,BC111 follow CRB1.0 Page09:change CMOS circuit,add D30,R344 Page11:change to SODIMM Page18:modify BEEP circuit follow ECS MODULE Page19:change to 8721-DX
CI3 V.1.0	2010.07.02	Page19:Modify ATXPG circuit Page12:ER28 from 15.4K to 14.3K for OCP TEST Page16:R161 change to R159 for power report
CI3 V.1.1	2010.11.23	Page21:LAN chip 8111/8103 co-lay change to 8111/8105 co-lay Page09:ADD Case open function PageALL :bottom side component change to Top side (R81,R89,R79,R84,C91,C92,C93,C94,C2,C7,C104,C105,C96,C85,C75,C79,C83,RN19)

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Title: Cover Page

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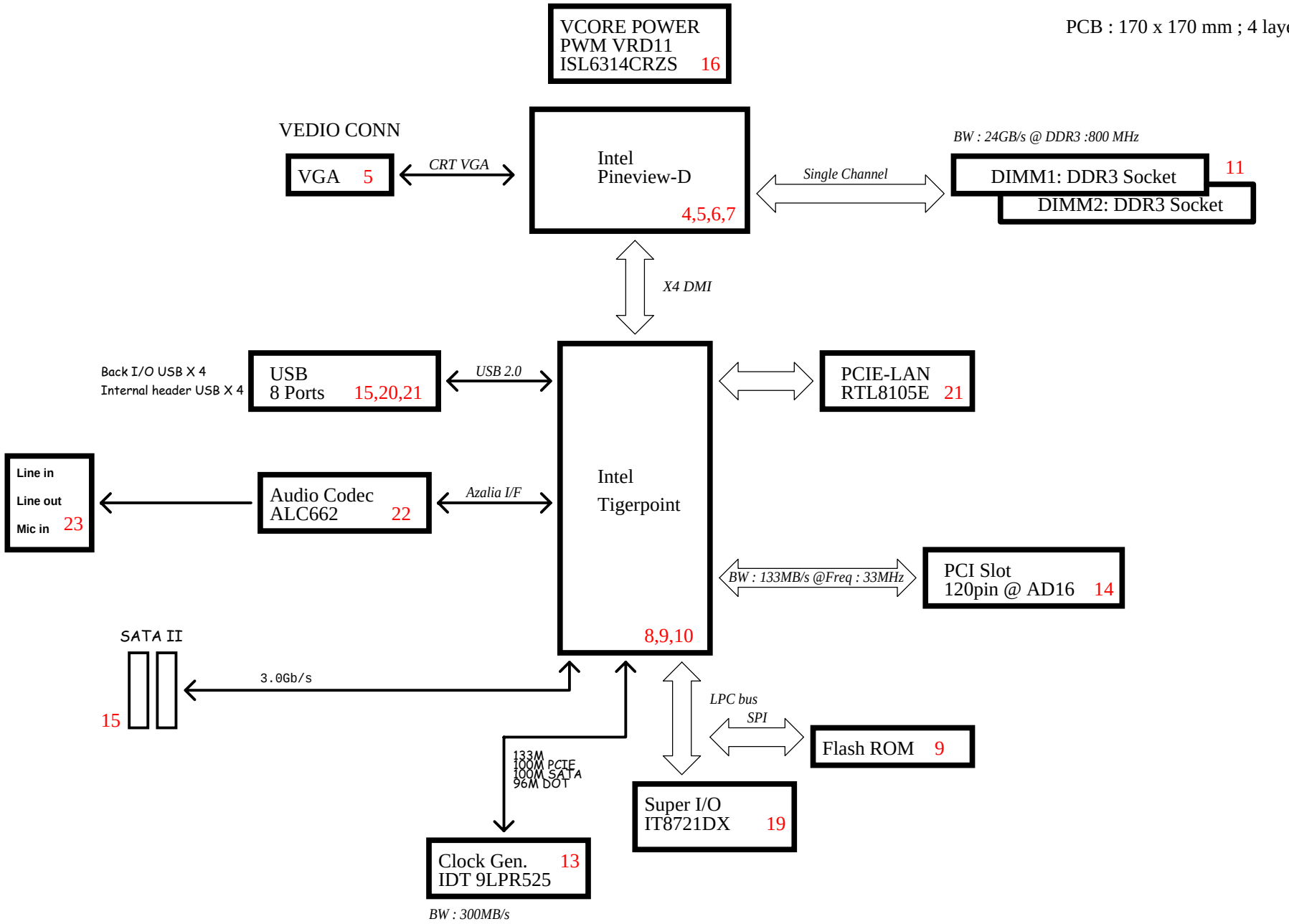
PCB : 170 x 170 mm ; 4 layers



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Title: Block Diagram		
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	Pin Name	Default	Power	USAGE	Function & Status
*	GPIO1	GPI	VCC	GPIO1	4.7K up to VCC3, if not used
	PIRQE#/GPIO2	GPI	VCC	INT-E	8.2K up to VCC3, to PCI
	PIRQE#/GPIO3	GPI	VCC	INT-F	8.2K up to VCC3, to PCI
	PIRQE#/GPIO4	GPI	VCC	INT-G	8.2K up to VCC3, to PCI
	PIRQE#/GPIO5	GPI	VCC	INT-H	8.2K up to VCC3, to PCI
*	GPIO17	GPO	VCC3	GPIO17	BOOT BIOS DESTINATION SELECTION 10K down to GND SPI Function
	GPIO22	GPI	VCC3	GPIO22	4.7K up to VCC3, if not used
	OC5#/GPIO29	OC5#	3VSB	USB3_OC_L	10K up to 3VSB, to uP7533
	OC6#/GPIO30	OC6#	3VSB	USB4_OC_L	10K up to 3VSB, to uP7533
	OC7#/GPIO31	OC7#	3VSB	USB5_OC_L	10K up to 3VSB, to uP7533
	GPIO36	GPI	VCC3	GPIO36	4.7K up to VCC3, if not used
	GPIO48	STRAP1#	VCC3	GPIO48	BOOT BIOS DESTINATION SELECTION GPI, Floating SPI Function

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	Pin Name	Default	Power	USAGE	Function & Status
*	BM_BUSY#/GPIO0	GPI	VCC3	FRONT_AUD_DET	4.7K up to VCC3
	GPIO6	GPI	VCC3	GPIO6	10K up to VCC3, (N/A)
	GPIO7	GPI	VCC3	GPIO7	10K up to VCC3, (N/A)
	GPIO8	GPI	3VSB	GPIO8	10K up to 3VSB, (N/A)
	GPIO9	GPI	3VSB	GPIO9	10K up to 3VSB, (N/A)
	GPIO10	GPI	3VSB	GPIO10	10K up to 3VSB, (N/A)
	SMBALERT#/GPIO11	SMBALERT#	3VSB	SMBALERT_L	10K up to 3VSB, to nowhere
	GPIO12	GPI	3VSB	TP108	10K up to 3VSB, if not used
	GPIO13	GPI	3VSB	LPCPME_L	4.7K up to 3VSB, to SIO
	GPIO14	GPI	3VSB	GPIO14	10K up to 3VSB, if not used
	GPIO15	GPI	3VSB	GPIO15	10K up to 3VSB, if not used
	LDRQ1#/GPIO23	LDRQ1#	VCC3	TP82	Test Point
	GPIO24	GPO	3VSB	TP84	Test Point
*	GPIO25	GPO	3VSB	GPIO25	DMI DC / AC COUPLING SELECTION 1K down to GND, AC COUPLING MODE
	GPIO26	GPO	3VSB	N/A	Floating
	GPIO27	GPO	3VSB	GPIO27	10K-O TO 3VSB control USB power
	GPIO28	GPO	3VSB	TP88	Test Point
	GPIO33	GPO	VCC3	GPIO33	4.7K-O up to VCC3, to nowhere
	GPIO34	GPO	VCC3	GPIO34	10K UP TO VCC3,for GPIO
	GPIO38	GPI	VCC3	GPIO38	10K UP TO VCC3,for GPIO
	GPIO39	GPI	VCC3	GPIO39	10K UP TO VCC3,for GPIO
	CPUPWRGD/GPIO49	CPUPWRGD	V_CPU_IO	H_CPUPWRGD	1K-O up to VCC_1P05, to Pineview

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	Pin Name	Default	Power	USAGE	Function & Status
	VCORE_GOOD/VID6/GP63	VCORE_GOOD	AVCC3	N/A	Floating
	VCORE_EN/VID7/GP64	VCORE_EN	AVCC3	N/A	Floating
	VDDA_EN/GP65	VDDA_EN	AVCC3	N/A	Floating
	VLDT_EN/GP66	VLDT_EN	AVCC3	N/A	Floating
	CPU_GD/GP67	CPU_GD	AVCC3	N/A	Floating
	PD0/GP70	PD0	AVCC3	PD0	1K up to VCC, to LPT circuit
	PD1/GP71	PD1	AVCC3	PD1	1K up to VCC, to LPT circuit
	BUSSI0/PD2/GP72	PD2	AVCC3	PD2	1K up to VCC, to LPT circuit
	BUSSI1/PD3/GP73	PD3	AVCC3	PD3	1K up to VCC, to LPT circuit
	BUSSI2/PD4/GP74	PD4	AVCC3	PD4	1K up to VCC, to LPT circuit
	BUSSO0/PD5/GP75	PD5	AVCC3	PD5	1K up to VCC, to LPT circuit
	BUSSO1/PD6/GP76	PD6	AVCC3	PD6	1K up to VCC, to LPT circuit
	BUSSO2/PD7/GP77	PD7	AVCC3	PD7	1K up to VCC, to LPT circuit
	SLCT#/GP80	SLCT#	AVCC3	SLCT	1K up to VCC, to LPT circuit
	PE#/GP81	PE#	AVCC3	PE	1K up to VCC, to LPT circuit
	BUSY#/GP82	BUSY#	AVCC3	BUSY	1K up to VCC, to LPT circuit
	ACK#/GP83	ACK#	AVCC3	ACK_L	1K up to VCC, to LPT circuit
	SMBD_R/SLIN#/GP84	SMBD_R	AVCC3	SIN_L	1K up to VCC, to LPT circuit
	SMBD_M/INIT#/GP85	PE#/GP81	AVCC3	INIT_L	1K up to VCC, to LPT circuit
	SMBC_R/AFD#/GP86	SMBC_R	AVCC3	AFD_L	1K up to VCC, to LPT circuit
	SMBC_M/STB#/GP87	SMBC_M	AVCC3	STB_L	1K up to VCC, to LPT circuit

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	Pin Name	Default	Power	USAGE	Function & Status
	PCIRST3#/GP10	PCI Reset	3VSB	N/A	Floating
	PCIRST2#/GP11	PCI Reset	AVCC3	N/A	Floating
	PCIRST1#/GP12	PCI Reset	AVCC3	PCIRST1	330-O up to VCC3, to LANRST
	SVC/PECI_RQT//GP14	SVC	AVCC3	THRM_L	10K up to VCC3, to SB THRM
*	SVD/PCIRSTIN#/ CIRTX2/GP15	CIRTX2	AVCC3	GPIO	10K up to VCC3, FOR GP15
	PSI_L/FAN_CTL5 /CIRRX2/GP16	PSI_L	AVCC3	N/A	Floating
	VID06/RI2/GP17	RI2	AVCC3	BEEP	4.7K-O up to VCC,to BEEP Circuit
	VIDO0/CTS2/GP20	GP20	3VSB	N/A	Floating
	VIDO1/DCD2#/GP21	GP21	3VSB	N/A	Floating
*	SCK/GP22	GP22	3VSB	LED0	2K up to 3VSB, to LED Circuit
*	SI/GP23	GP23	3VSB	LED1	2K up to 3VSB, to LED Circuit
	VIDO2/FAN_TAC5 /RTS2#/GP24	GP24/FAN_TAC5	3VSB	N/A	Floating
	VIDO3/FAN_TAC4 /DSR2#/GP25	GP25/FAN_TAC4	3VSB	N/A	Floating
*	VIDO4/SOUT2/GP26	GP26	3VSB	GPIO	4.7K up to 3VSB for GPIO
*	VIDO5/SIN2#/GP27	GP27	3VSB	GPIO	4.7K up to 3VSB for GPIO
*	VID0/GP30	GP30	AVCC3	GPIO	4.7K up to VCC3 for GPIO
*	GP34	GP34	AVCC3	GPIO	4.7Kup to VCC3 for GPIO
*	GP35	GP35	AVCC3	GPIO	4.7K up to VCC3 for GPIO
	FAN_CTL3/GP36	FAN_CTL3	AVCC3	N/A	Floating
	FAN_TAC3/GP37	FAN_TAC3	AVCC3	N/A	Floating
	3VSBSW#/GP40	3VSBSW#	3VSB	3VSBSW#	4.7K-O up to 3VSB, to control VDIMM circuit
	PSON#/GP42	PSON#	3VSB	PSON_L	4.7K up to 3VSB, to ATX PSON circuit
	PANSWH#/GP43	PANSWH#	3VSB	PWRSW	4.7K up to 3VSB, to PANEL PWRSW circuit
	PWRON#/GP44	PWRON#	3VSB	PWRBT_L	5.1K up to 3VSB, to SB PWRBTN circuit
*	GP47	GP47	AVCC3	GPIO47	4.7K up to VCC3 for GPIO47
	SO/GP50	SO	AVCC3	N/A	Floating
	FAN_CTL2/GP51	FAN_CTL2	AVCC3	FAN_CTL2	4.7K up to VCC,to CPU FAN CTL Circuit
	FAN_TAC2/GP52	FAN_TAC2	AVCC3	FAN_TAC2	4.7K up to VCC,to CPU FAN TAC Circuit
	SUSC#/GP53	SUSC#	3VSB	SLP4_L	4.7K-O up to 3VSB , to SLP4_L circuit
	PME#/GP54	PME#	3VSB	LPCPME_L	4.7K-O up to 3VSB , to SB PME circuit
	RSMRST#/CIRRX1/GP55	RSMRST#	3VSB	RSMRST_L	680 up to 3VSB , to SB RSMRST circuit
	MCLK/GP56	MCLK	AVC33	MCLK	2.2K up to KBVCC , to MCLK circuit
	MDAT/GP57	MDAT	AVCC33	MDATA	2.2K up to KBVCC , to MDATA circuit
	KCLK/GP60	KCLK	AVCC3	KCLK	2.2K up to KBVCC , to KCLK circuit
	KDAT/GP61	KDAT	AVCC3	KDATA	2.2K up to KBVCC , to KDATA circuit
	KRST#/GP62	KRST#	AVCC3	KRST_L	10K up to VCC3 , to SB KBRST_L circuit

ECS <OrgAddr1> Elitegroup Computer Systems

Title: GPIO, IRQ, IDSEL Map

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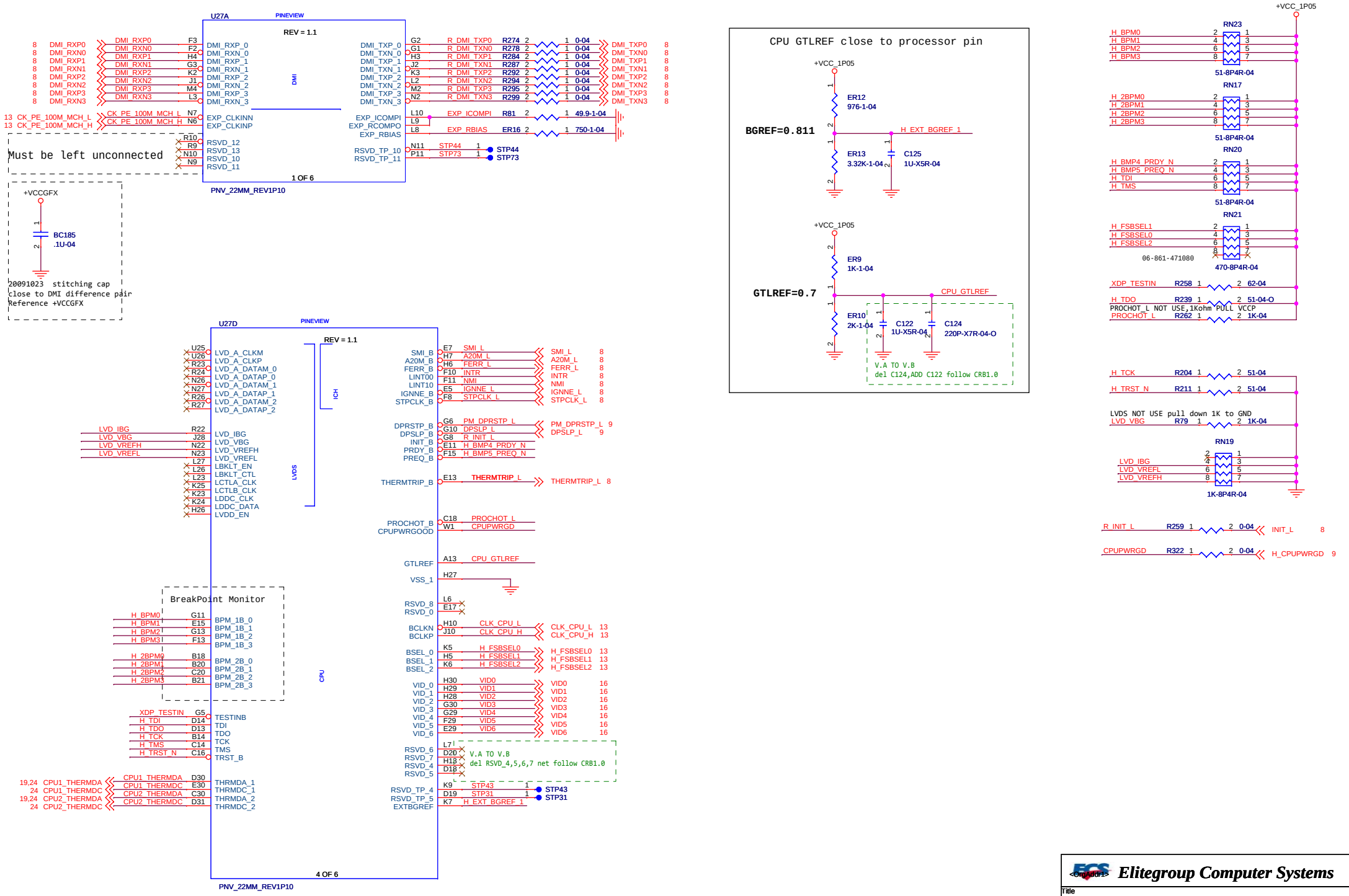
U27A
PINEVIEW
REV = 1.1
DMI_RXP0 F3
DMI_RXN0 F2
DMI_RXP1 H4
DMI_RXN1 G3
DMI_RXP2 K2
DMI_RXN2 J1
DMI_RXP3 M4
DMI_RXN3 L3
DMI_RXP_0
DMI_RXN_0
DMI_RXP_1
DMI_RXN_1
DMI_RXP_2
DMI_RXN_2
DMI_RXP_3
DMI_RXN_3
DMI
DMI_TXP_0 G2
DMI_TXN_0 G1
DMI_TXP_1 H3
DMI_TXN_1 J2
DMI_TXP_2 K3
DMI_TXN_2 L2
DMI_TXP_3 M2
DMI_TXN_3 N2
R_DMI_TXP0 R274
R_DMI_TXN0 R278
R_DMI_TXP1 R284
R_DMI_TXN1 R287
R_DMI_TXP2 R292
R_DMI_TXN2 R294
R_DMI_TXP3 R295
R_DMI_TXN3 R299
0-04
DMI_TXP0 8
DMI_TXN0 8
DMI_TXP1 8
DMI_TXN1 8
DMI_TXP2 8
DMI_TXN2 8
DMI_TXP3 8
DMI_TXN3 8
13 CK_PE_100M_MCH_L
13 CK_PE_100M_MCH_H
CK_PE_100M_MCH_L N7
CK_PE_100M_MCH_H N6
EXP_CLKINN
EXP_CLKINP
EXP_ICOMPI L10
EXP_RCOMPO L9
EXP_RBIAS L8
EXP_ICOMPI R81 49.9-1-04
EXP_RBIAS ER16 750-1-04
Must be left unconnected
R10
R9
N10
N9
RSVD_12
RSVD_13
RSVD_10
RSVD_11
RSVD_TP_10 N11
RSVD_TP_11 P11
STP44
STP73
1 OF 6
PNV_22MM_REV1P10
+VCCGFX
BC185
.1U-04
20091023 stitching cap
close to DMI difference pair
Reference +VCCGFX
U27D
PINEVIEW
REV = 1.1
U25
U26
R23
R24
N26
N27
R26
R27
LVD_A_CLKM
LVD_A_CLKP
LVD_A_DATAM_0
LVD_A_DATAP_0
LVD_A_DATAM_1
LVD_A_DATAP_1
LVD_A_DATAM_2
LVD_A_DATAP_2
ICH
LVD_IBG R22
LVD_VBG J28
LVD_VREFH N22
LVD_VREFL N23
L27
L26
L23
K25
K23
K24
H26
LVD_IBG
LVD_VBG
LVD_VREFH
LVD_VREFL
LBKLT_EN
LBKLT_CTL
LCTLA_CLK
LCTLB_CLK
LDDC_CLK
LDDC_DATA
LVDD_EN
LVDS
SMI_B E7
A20M_B H7
FERR_B H6
LINT00 F10
LINT10 F11
IGNNE_B E5
STPCLK_B F8
SMI_L
A20M_L
FERR_L
INTR
NMI
IGNNE_L
STPCLK_L
SMI_L 8
A20M_L 8
FERR_L 8
INTR 8
NMI 8
IGNNE_L 8
STPCLK_L 8
DPRSTP_B G6
DPSLP_B G10
INIT_B G8
PRDY_B E11
PREQ_B F15
PM_DPRSTP_L
DPSLP_L
R_INIT_L
H_BMP4_PRDY_N
H_BMP5_PREQ_N
PM_DPRSTP_L 9
DPSLP_L 9
THERMTRIP_B E13
THERMTRIP_L
THERMTRIP_L 8
PROCHOT_B C18
CPUPWRGOOD W1
PROCHOT_L
CPUPWRGD
GTLREF A13
VSS_1 H27
CPU_GTLREF
RSVD_8 L6
RSVD_0 E17
BreakPoint Monitor
H_BPM0 G11
H_BPM1 E15
H_BPM2 G13
H_BPM3 F13
BPM_1B_0
BPM_1B_1
BPM_1B_2
BPM_1B_3
H_2BPM0 B18
H_2BPM1 B20
H_2BPM2 C20
H_2BPM3 B21
BPM_2B_0
BPM_2B_1
BPM_2B_2
BPM_2B_3
CPU
BCLKN H10
BCLKP J10
CLK_CPU_L
CLK_CPU_H
CLK_CPU_L 13
CLK_CPU_H 13
BSEL_0 K5
BSEL_1 H5
BSEL_2 K6
H_FSBSEL0
H_FSBSEL1
H_FSBSEL2
H_FSBSEL0 13
H_FSBSEL1 13
H_FSBSEL2 13
VID_0 H30
VID_1 H29
VID_2 H28
VID_3 G30
VID_4 G29
VID_5 F29
VID_6 E29
VID0
VID1
VID2
VID3
VID4
VID5
VID6
VID0 16
VID1 16
VID2 16
VID3 16
VID4 16
VID5 16
VID6 16
RSVD_6 L7
RSVD_7 D20
RSVD_4 H18
RSVD_5 D18
V.A TO V.B
del RSVD_4,5,6,7 net follow CRB1.0
XDP_TESTIN G5
H_TDI D14
H_TDO D13
H_TCK B14
H_TMS C14
H_TRST_N C16
TESTINB
TDI
TDO
TCK
TMS
TRST_B
19,24 CPU1_THERMDA
24 CPU1_THERMDC
19,24 CPU2_THERMDA
24 CPU2_THERMDC
CPU1_THERMDA D30
CPU1_THERMDC E30
CPU2_THERMDA C30
CPU2_THERMDC D31
THRMDA_1
THRMDC_1
THRMDA_2
THRMDC_2
RSVD_TP_4 K9
RSVD_TP_5 D19
EXTBGREF K7
STP43
STP31
H_EXT_BGREF_1
4 OF 6
PNV_22MM_REV1P10
CPU GTLREF close to processor pin
+VCC_1P05
ER12
976-1-04
BGREF=0.811
H_EXT_BGREF_1
ER13
3.32K-1-04
C125
1U-X5R-04
ER9
1K-1-04
GTLREF=0.7
CPU_GTLREF
ER10
2K-1-04
C122
1U-X5R-04
C124
220P-X7R-04-O
V.A TO V.B
del C124,ADD C122 follow CRB1.0
RN23
H_BPM0
H_BPM1
H_BPM2
H_BPM3
51-8P4R-04
RN17
H_2BPM0
H_2BPM1
H_2BPM2
H_2BPM3
51-8P4R-04
RN20
H_BMP4_PRDY_N
H_BMP5_PREQ_N
H_TDI
H_TMS
51-8P4R-04
RN21
H_FSBSEL1
H_FSBSEL0
H_FSBSEL2
06-861-471080
470-8P4R-04
XDP_TESTIN R258 62-04
H_TDO R239 51-04-O
PROCHOT_L NOT USE,1Kohm PULL VCCP
PROCHOT_L R262 1K-04
H_TCK R204 51-04
H_TRST_N R211 51-04
LVDS NOT USE pull down 1K to GND
LVD_VBG R79 1K-04
RN19
LVD_IBG
LVD_VREFL
LVD_VREFH
1K-8P4R-04
R_INIT_L R259 0-04 INIT_L 8
CPUPWRGD R322 0-04 H_CPUPWRGD 9
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Title
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Size Custom
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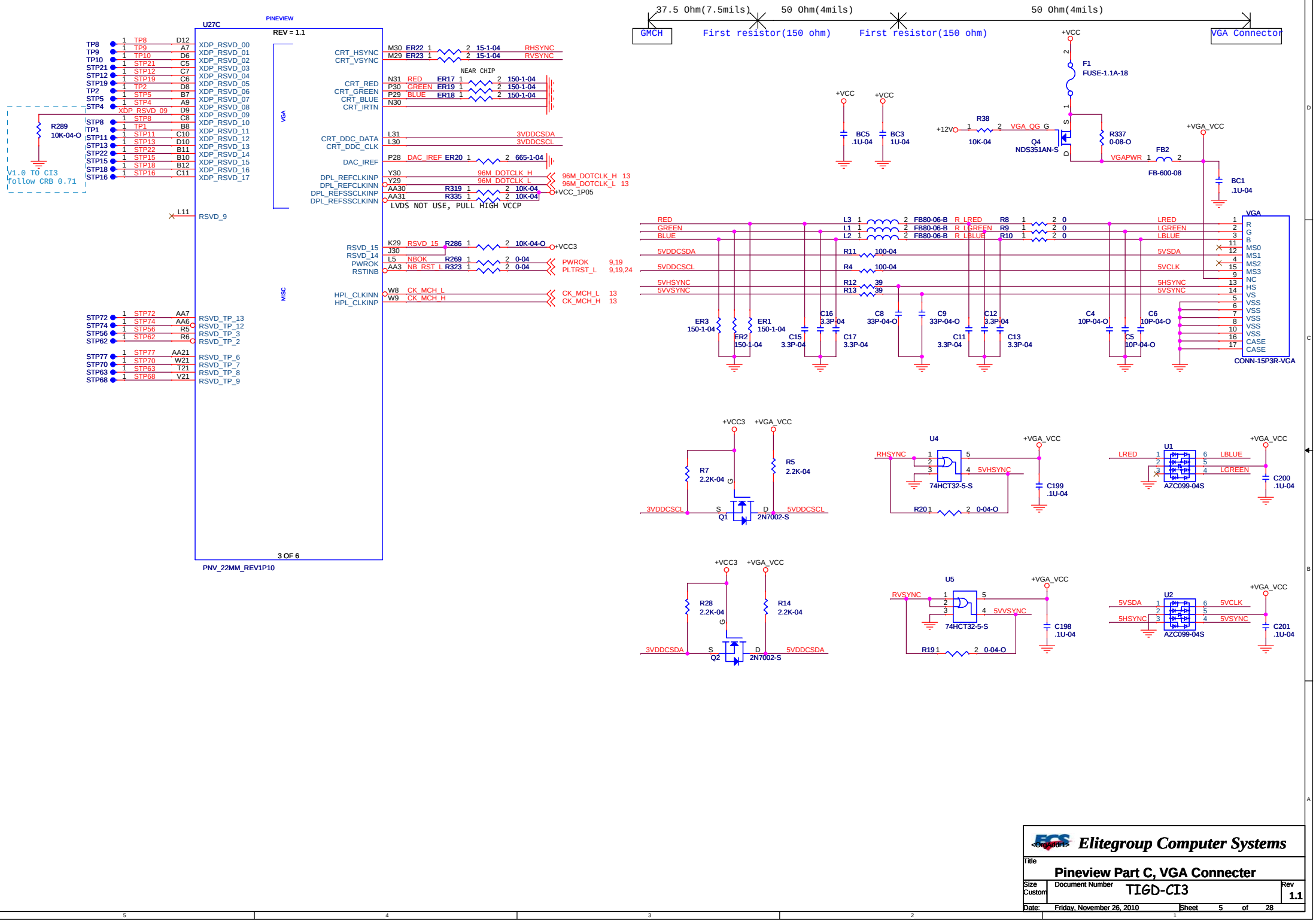
37.5 Ohm(7.5mils)
50 Ohm(4mils)
50 Ohm(4mils)
GMCH
First resistor(150 ohm)
First resistor(150 ohm)
VGA Connector
U27C
PINEVIEW
REV = 1.1
PNV_22MM_REV1P10
3 OF 6
V1.0 TO CI3
follow CRB 0.71
R289
10K-04-O
NEAR CHIP
LVDS NOT USE, PULL HIGH VCCP
CONN-15P3R-VGA
FUSE-1.1A-18
FB-600-08
Q4
NDS351AN-S
Q1
2N7002-S
Q2
2N7002-S
74HCT32-5-S
AZC099-04S
Elitegroup Computer Systems
Pineview Part C, VGA Connecter
TIGD-CI3
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PINEVIEW

U27B

REV = 1.1

MAAA_0	AH19	DDR_A_MA_0	DDR_A_DQS_0	AD3	DQS_H_A0
MAAA_1	AJ18	DDR_A_MA_1	DDR_A_DQSB_0	AD2	DQS_L_A0
MAAA_2	AK18	DDR_A_MA_2	DDR_A_DM_0	AD4	MPD_A0
MAAA_3	AK16	DDR_A_MA_3	DDR_A_DQ_0	AC4	MD_A0
MAAA_4	AJ14	DDR_A_MA_4	DDR_A_DQ_1	AC1	MD_A1
MAAA_5	AH14	DDR_A_MA_5	DDR_A_DQ_2	AF4	MD_A2
MAAA_6	AK14	DDR_A_MA_6	DDR_A_DQ_3	AG2	MD_A3
MAAA_7	AJ12	DDR_A_MA_7	DDR_A_DQ_4	AB2	MD_A4
MAAA_8	AH13	DDR_A_MA_8	DDR_A_DQ_5	AB3	MD_A5
MAAA_9	AK12	DDR_A_MA_9	DDR_A_DQ_6	AE2	MD_A6
MAAA_10	AK20	DDR_A_MA_10	DDR_A_DQ_7	AE3	MD_A7
MAAA_11	AH12	DDR_A_MA_11	DDR_A_DQS_1	AB8	DQS_H_A1
MAAA_12	AJ11	DDR_A_MA_12	DDR_A_DQSB_1	AD7	DQS_L_A1
MAAA_13	AJ24	DDR_A_MA_13	DDR_A_DM_1	AA9	MPD_A1
MAAA_14	AJ10	DDR_A_MA_14	DDR_A_DQ_8	AB6	MD_A8
			DDR_A_DQ_9	AB7	MD_A9
SWE_L_A	AK22	DDR_A_WEB	DDR_A_DQ_10	AE5	MD_A10
SCAS_L_A	AJ22	DDR_A_CASB	DDR_A_DQ_11	AG5	MD_A11
SRAS_L_A	AK21	DDR_A_RASB	DDR_A_DQ_12	AA5	MD_A12
			DDR_A_DQ_13	AB5	MD_A13
SBSA_0	AJ20	DDR_A_BS_0	DDR_A_DQ_14	AB9	MD_A14
SBSA_1	AH20	DDR_A_BS_1	DDR_A_DQ_15	AD6	MD_A15
SBSA_2	AK11	DDR_A_BS_2			
			DDR_A_DQS_2	AD8	DQS_H_A2
			DDR_A_DQSB_2	AD10	DQS_L_A2
CSA_L0	AH22	DDR_A_CSB_0	DDR_A_DM_2	AE8	MPD_A2
CSA_L1	AK25	DDR_A_CSB_1	DDR_A_DQ_16	AG8	MD_A16
CSA_L2	AJ21	DDR_A_CSB_2	DDR_A_DQ_17	AG7	MD_A17
CSA_L3	AJ25	DDR_A_CSB_3	DDR_A_DQ_18	AF10	MD_A18
			DDR_A_DQ_19	AG11	MD_A19
CKEA_0	AH10	DDR_A_CKE_0	DDR_A_DQ_20	AF7	MD_A20
CKEA_1	AH9	DDR_A_CKE_1	DDR_A_DQ_21	AF8	MD_A21
CKEA_2	AK10	DDR_A_CKE_2	DDR_A_DQ_22	AD11	MD_A22
CKEA_3	AJ8	DDR_A_CKE_3	DDR_A_DQ_23	AE10	MD_A23
ODTA_0	AK24	DDR_A_ODT_0	DDR_A_DQS_3	AK5	DQS_H_A3
ODTA_1	AH26	DDR_A_ODT_1	DDR_A_DQSB_3	AK3	DQS_L_A3
ODTA_2	AH24	DDR_A_ODT_2	DDR_A_DM_3	AJ3	MPD_A3
ODTA_3	AK27	DDR_A_ODT_3	DDR_A_DQ_24	AH1	MD_A24
			DDR_A_DQ_25	AJ2	MD_A25
DCLKA_H0	AG15	DDR_A_CK_0	DDR_A_DQ_26	AK6	MD_A26
DCLKA_L0	AF15	DDR_A_CKB_0	DDR_A_DQ_27	AJ7	MD_A27
DCLKA_H1	AD13	DDR_A_CK_1	DDR_A_DQ_28	AF3	MD_A28
DCLKA_L1	AC13	DDR_A_CKB_1	DDR_A_DQ_29	AH2	MD_A29
	AD17	DDR_A_CK_2	DDR_A_DQ_30	AL5	MD_A30
DCLKA_H3	AC15	DDR_A_CKB_2	DDR_A_DQ_31	AJ6	MD_A31
DCLKA_L3	AD15	DDR_A_CK_3	DDR_A_DQS_4	AG22	DQS_H_A4
DCLKA_H4	AF13	DDR_A_CKB_3	DDR_A_DQSB_4	AG21	DQS_L_A4
DCLKA_L4	AG13	DDR_A_CK_4	DDR_A_DM_4	AD19	MPD_A4
	AB15	DDR_A_CKB_4	DDR_A_DQ_32	AE19	MD_A32
	AB17	DDR_A_CK_5	DDR_A_DQ_33	AG19	MD_A33
		DDR_A_CKB_5	DDR_A_DQ_34	AF22	MD_A34
			DDR_A_DQ_35	AD22	MD_A35
			DDR_A_DQ_36	AG17	MD_A36
			DDR_A_DQ_37	AF19	MD_A37
			DDR_A_DQ_38	AE21	MD_A38
			DDR_A_DQ_39	AD21	MD_A39
			DDR_A_DQS_5	AE26	DQS_H_A5
			DDR_A_DQSB_5	AG27	DQS_L_A5
DDR_PWROK	AB4	DDR_PREF	DDR_A_DM_5	AJ27	MPD_A5
DDR3_RST_L	AK8	RSVD_2	DDR_A_DQ_40	AE24	MD_A40
			DDR_A_DQ_41	AG25	MD_A41
			DDR_A_DQ_42	AD25	MD_A42
STP79	AB11	RSVD_TP_0	DDR_A_DQ_43	AD24	MD_A43
STP76	AB13	RSVD_TP_1	DDR_A_DQ_44	AC22	MD_A44
			DDR_A_DQ_45	AG24	MD_A45
DDR_REF	AL28		DDR_A_DQ_46	AD27	MD_A46
DDR_RPD	AK28	DDR_VREF	DDR_A_DQ_47	AE27	MD_A47
DDR_RPU	AJ26	DDR_RPD	DDR_A_DQS_6	AE30	DQS_H_A6
		DDR_RPU	DDR_A_DQSB_6	AF29	DQS_L_A6
	AK29	RSVD_1	DDR_A_DM_6	AF30	MPD_A6
			DDR_A_DQ_48	AG31	MD_A48
			DDR_A_DQ_49	AG30	MD_A49
			DDR_A_DQ_50	AD30	MD_A50
			DDR_A_DQ_51	AD29	MD_A51
			DDR_A_DQ_52	AJ30	MD_A52
			DDR_A_DQ_53	AJ29	MD_A53
			DDR_A_DQ_54	AE29	MD_A54
			DDR_A_DQ_55	AD28	MD_A55
			DDR_A_DQS_7	AB27	DQS_H_A7
			DDR_A_DQSB_7	AA27	DQS_L_A7
			DDR_A_DM_7	AB26	MPD_A7
			DDR_A_DQ_56	AA24	MD_A56
			DDR_A_DQ_57	AB25	MD_A57
			DDR_A_DQ_58	W24	MD_A58
			DDR_A_DQ_59	W22	MD_A59
			DDR_A_DQ_60	AB24	MD_A60
			DDR_A_DQ_61	AB23	MD_A61
			DDR_A_DQ_62	AA23	MD_A62
			DDR_A_DQ_63	W27	MD_A63

DDR_A

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PNV_22MM_REV1P10

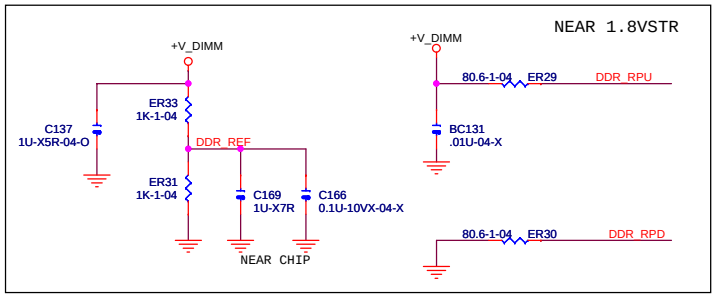
STP87 STP89 — V1.0 TO CI3 change to TP point

STP85 STP86

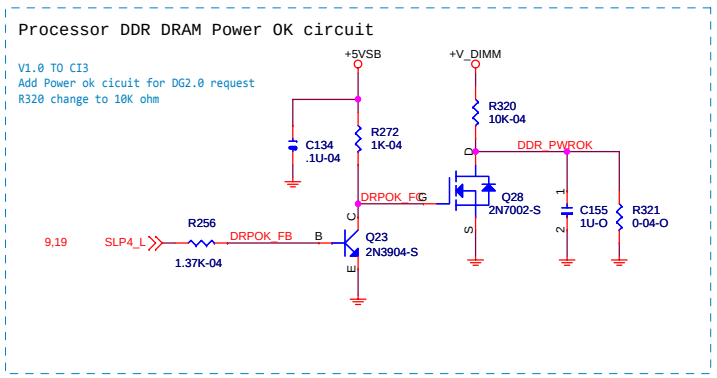
+V_DIMM — R457 10K-04-O — V1.0 TO CI3 add DDR3_RST_L

STP79 STP76

NEAR 1.8VSTR



Processor DDR DRAM Power OK circuit



V1.0 TO CI3 change net

11	MAAA_[0..14]	MAAA_[0..14]
11	CSA_L[0..3]	CSA_L[0..3]
11	CKEA_[0..3]	CKEA_[0..3]
11	ODTA_[0..3]	ODTA_[0..3]
11	DCLKA_L[0..1]	DCLKA_L[0..1]
11	DCLKA_H[0..1]	DCLKA_H[0..1]
11	DCLKA_L[3..4]	DCLKA_L[3..4]
11	DCLKA_H[3..4]	DCLKA_H[3..4]
11	MD_A[0..63]	MD_A[0..63]
11	DQS_L_A[0..7]	DQS_L_A[0..7]
11	DQS_H_A[0..7]	DQS_H_A[0..7]
11	MPD_A[0..7]	MPD_A[0..7]
11	SBSA_[0..2]	SBSA_[0..2]
11	SWE_L_A	SWE_L_A
11	SCAS_L_A	SCAS_L_A
11	SRAS_L_A	SRAS_L_A
11	DDR3_RST_L	DDR3_RST_L

Elitegroup Computer Systems			
Title: Pineview Part B			
Size: Custom	Document Number: TIGD-CI3		Rev: 1.1
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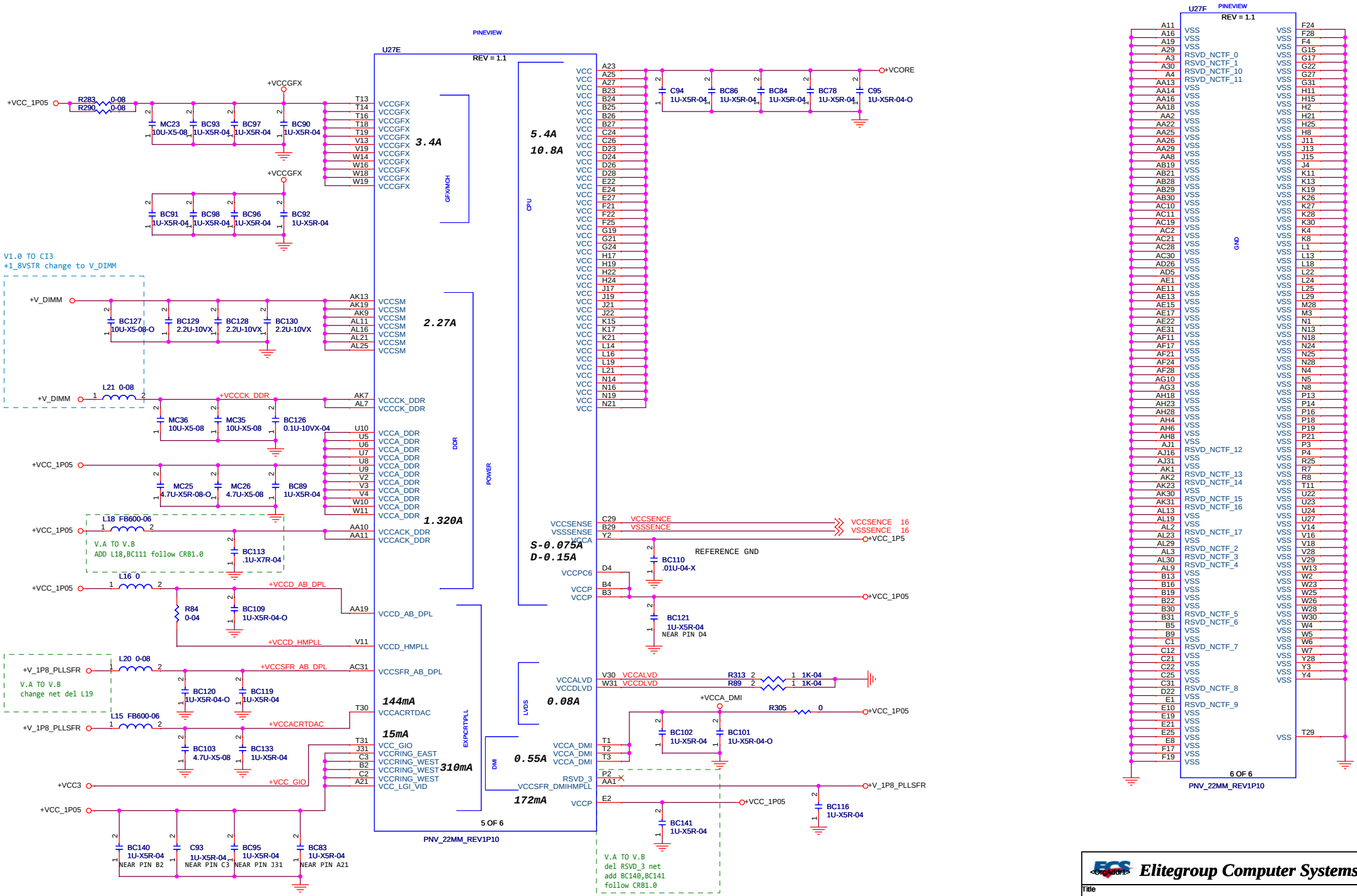
PINEVIEW
U27E
REV = 1.1
+VCCGFX
+VCC_1P05
R283 0-08
R290 0-08
MC23 10U-X5-08
BC93 1U-X5R-04
BC97 1U-X5R-04
BC90 1U-X5R-04
BC91 1U-X5R-04
BC98 1U-X5R-04
BC96 1U-X5R-04
BC92 1U-X5R-04
T13 T14 T16 T18 T19 V13 V19 W14 W16 W18 W19
VCCGFX
3.4A
GFX/MCH
V1.0 TO CI3
+1_8VSTR change to V_DIMM
+V_DIMM
BC127 10U-X5-08-O
BC129 2.2U-10VX
BC128 2.2U-10VX
BC130 2.2U-10VX
AK13 AK19 AK9 AL11 AL16 AL21 AL25
VCCSM
2.27A
L21 0-08
+VCCCK_DDR
MC36 10U-X5-08
MC35 10U-X5-08
BC126 0.1U-10VX-04
AK7 AL7
VCCCK_DDR
U10 U5 U6 U7 U8 U9 V2 V3 V4 W10 W11
VCCA_DDR
MC25 4.7U-X5R-08-O
MC26 4.7U-X5-08
BC89 1U-X5R-04
1.320A
DDR
L18 FB600-06
V.A TO V.B
ADD L18,BC111 follow CRB1.0
BC113 .1U-X7R-04
AA10 AA11
VCCACK_DDR
L16 0
+VCCD_AB_DPL
R84 0-04
BC109 1U-X5R-04-O
AA19
VCCD_AB_DPL
+VCCD_HMPLL
V11
VCCD_HMPLL
L20 0-08
+V_1P8_PLLSFR
V.A TO V.B
change net del L19
+VCCSFR_AB_DPL
AC31
VCCSFR_AB_DPL
BC120 1U-X5R-04-O
BC119 1U-X5R-04
144mA
L15 FB600-06
+VCCACRTDAC
T30
VCCACRTDAC
15mA
BC103 4.7U-X5-08
BC133 1U-X5R-04
T31 J31 C3 B2 C2 A21
VCC_GIO
VCCRING_EAST
VCCRING_WEST
VCCRING_WEST
VCCRING_WEST
VCC_LGI_VID
310mA
EXPCRTPLL
+VCC3
+VCC_GIO
BC140 1U-X5R-04 NEAR PIN B2
C93 1U-X5R-04 NEAR PIN C3
BC95 1U-X5R-04 NEAR PIN J31
BC83 1U-X5R-04 NEAR PIN A21
5 OF 6
PNV_22MM_REV1P10
POWER
CPU
A23 A25 A27 B23 B24 B25 B26 B27 C24 C26 D23 D24 D26 D28 E22 E24 E27 F21 F22 F25 G19 G21 G24 H17 H19 H22 H24 J17 J19 J21 J22 K15 K17 K21 L14 L16 L19 L21 N14 N16 N19 N21
VCC
5.4A
10.8A
+VCORE
C94 1U-X5R-04
BC86 1U-X5R-04
BC84 1U-X5R-04
BC78 1U-X5R-04
C95 1U-X5R-04-O
C29 B29 Y2
VCCSENSE
VSSSENSE
VCCA
VCCSENSE 16
VSSSENSE 16
+VCC_1P5
S-0.075A
D-0.15A
REFERENCE GND
BC110 .01U-04-X
D4 B4 B3
VCCPC6
VCCP
+VCC_1P05
BC121 1U-X5R-04 NEAR PIN D4
V30 W31
VCCALVD
VCCDLVD
R313 2 1 1K-04
R89 2 1 1K-04
LVDS
0.08A
+VCCA_DMI
R305 0
BC102 1U-X5R-04
BC101 1U-X5R-04-O
T1 T2 T3
VCCA_DMI
DMI
0.55A
P2 AA1
RSVD_3
VCCSFR_DMIHMPLL
172mA
+V_1P8_PLLSFR
E2
BC141 1U-X5R-04
BC116 1U-X5R-04
V.A TO V.B
del RSVD_3 net
add BC140,BC141
follow CRB1.0
U27F
PINEVIEW
REV = 1.1
A11 A16 A19 A29 A3 A30 A4 AA13 AA14 AA16 AA18 AA2 AA22 AA25 AA26 AA29 AA8 AB19 AB21 AB28 AB29 AB30 AC10 AC11 AC19 AC2 AC21 AC28 AC30 AD26 AD5 AE1 AE11 AE13 AE15 AE17 AE22 AE31 AF11 AF17 AF21 AF24 AF28 AG10 AG3 AH18 AH23 AH28 AH4 AH6 AH8 AJ1 AJ16 AJ31 AK1 AK2 AK23 AK30 AK31 AL13 AL19 AL2 AL23 AL29 AL3 AL30 AL9 B13 B16 B19 B22 B30 B31 B5 B9 C1 C12 C21 C22 C25 C31 D22 E1 E10 E19 E21 E25 E8 F17 F19
VSS
RSVD_NCTF_0
RSVD_NCTF_1
RSVD_NCTF_10
RSVD_NCTF_11
RSVD_NCTF_12
RSVD_NCTF_13
RSVD_NCTF_14
RSVD_NCTF_15
RSVD_NCTF_16
RSVD_NCTF_17
RSVD_NCTF_2
RSVD_NCTF_3
RSVD_NCTF_4
RSVD_NCTF_5
RSVD_NCTF_6
RSVD_NCTF_7
RSVD_NCTF_8
RSVD_NCTF_9
GND
F24 F28 F4 G15 G17 G22 G27 G31 H11 H15 H2 H21 H25 H8 J11 J13 J15 J4 K11 K13 K19 K26 K27 K28 K30 K4 K8 L1 L13 L18 L22 L24 L25 L29 M28 M3 N1 N13 N18 N24 N25 N28 N4 N5 N8 P13 P14 P16 P18 P19 P21 P3 P4 R25 R7 R8 T11 U22 U23 U24 U27 V14 V16 V18 V28 V29 W13 W2 W23 W25 W26 W28 W30 W4 W5 W6 W7 Y28 Y3 Y4 T29
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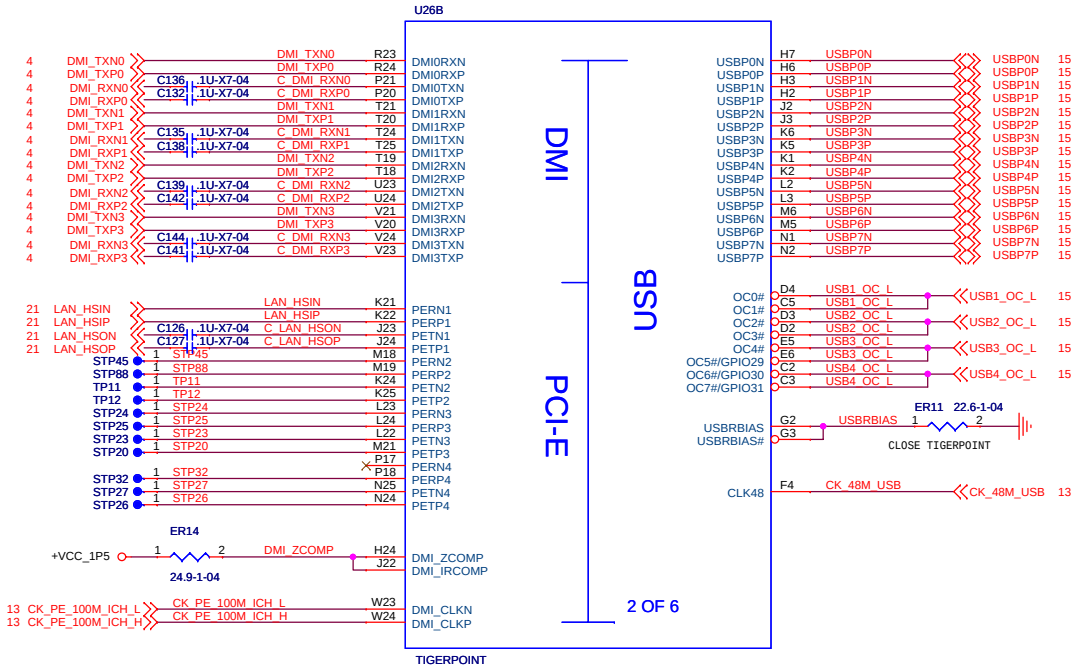
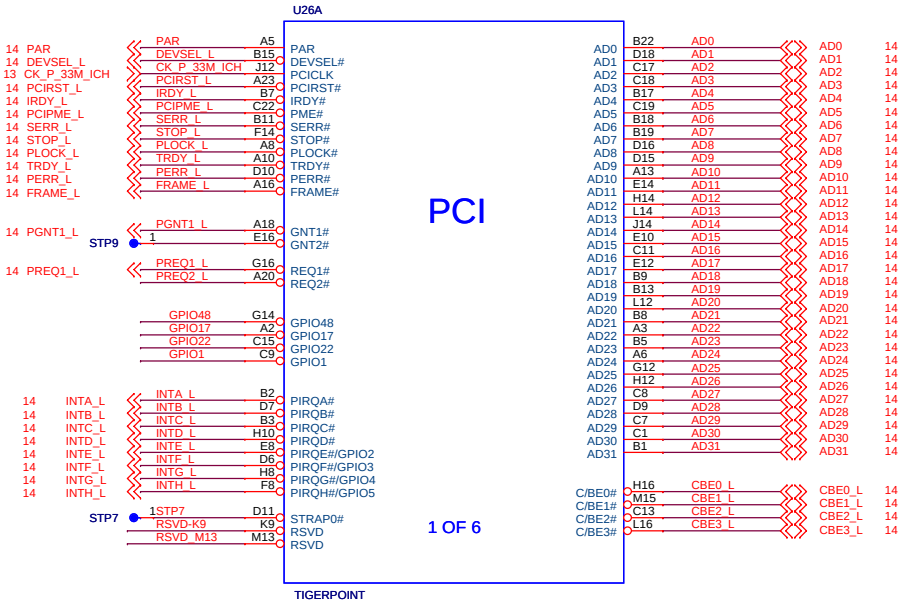
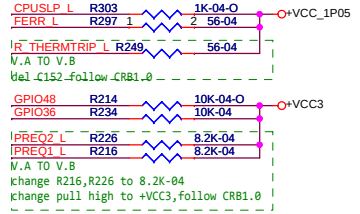
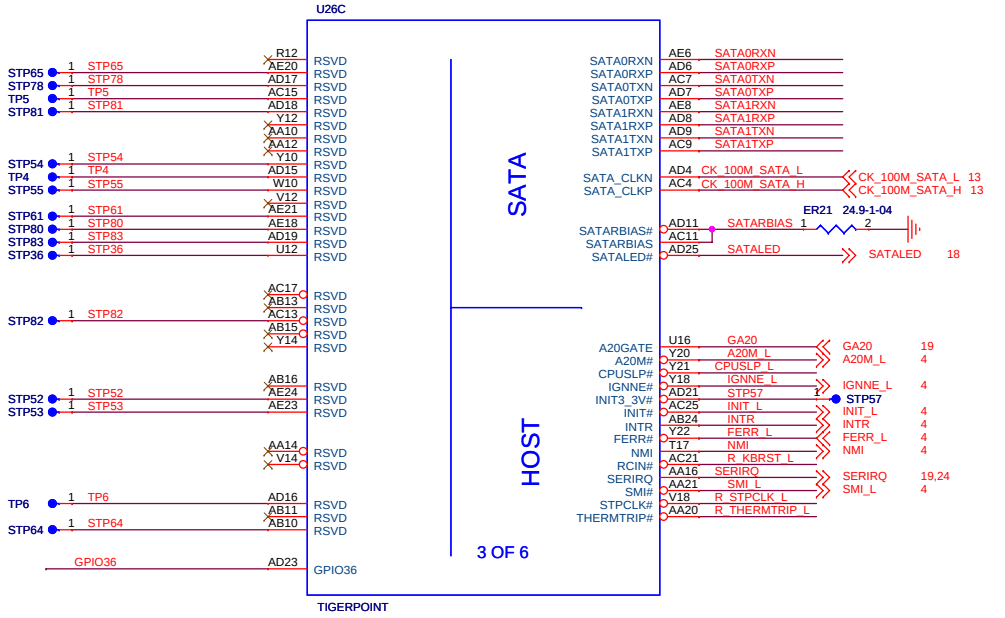
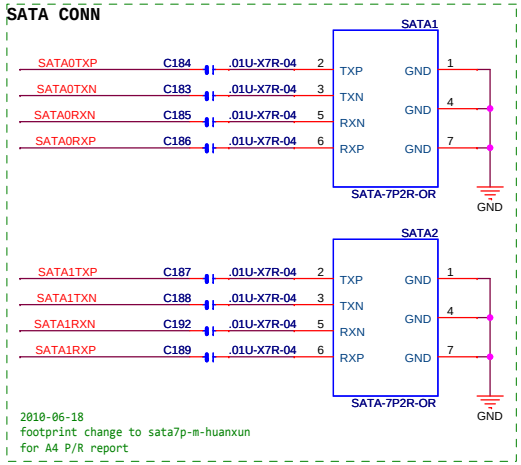
PNV_22MM_REV1P10
Elitegroup Computer Systems
Title
Pineview Part E & F (Power)
Size Custom
Document Number TIGD-CI3
Rev 1.1
Date: Friday, November 26, 2010
Sheet 7 of 28

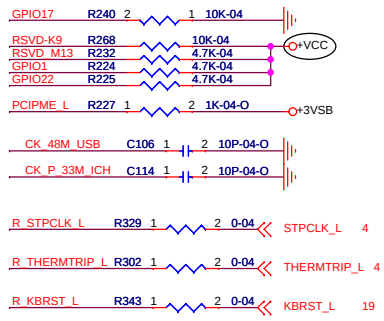












GPIO 48 internal pull up

BOOT BIOS DESTINATION SELECTION		
GPIO17	GPIO48	Function
0	1	* SPI
1	0	PCI
1	1	LPC

Elitegroup Computer Systems

Title: Tigerpoint Part A & B & C

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U26D

LPC
LAD0/FWH0
LAD1/FWH1
LAD2/FWH2
LAD3/FWH3
LDRQ0#
LFRAME#

AUDIO
HDA_BIT_CLK
HDA_RST#
HDA_SDI0
HDA_SDIN1
HDA_SDIN2
HDA_SDOUT
HDA_SYNC
CLKT4

EPROM
EE_CS
EE_DIN
EE_DOUT
EE_SHCLK

LAN
LAN_CLK
LANR_STSYNC
LAN_RST#
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2

RTC
RTCX1
RTCX2
RTCRST#

SMB
SMBALERT#/GPIO11
SMBCLK
SMBDATA
SMLALERT#
SMLINK0
SMLINK1

SPI
SPI_MISO
SPI_MOSI
SPI_CS#
SPI_CLK
SPI_ARB

MISC

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TIGERPOINT

STP46 1 STP46 AA5 — LAD0 V6 — LAD1 AA6 — LAD2 Y5 — LAD3 W8 — LDRQ0 Y8 — LFRAME_L Y4
R_AZ_BIT_CLK P6 — R_AZ_RST_L U2 — AZ_SDATA_IN W2 — V2 — P8 — R_AZ_SDATA_OUT AA1 — R_AZ_SYNC Y1 — CK_14M_ICH AA3
STP37 1 STP37 U3 — STP60 1 AE2 — STP38 1 T6 — STP39 1 V3
STP33 1 T4 — STP35 1 P7 — LAN_RST_L B23 — STP58 1 AA2 — STP49 1 AD1 — STP48 1 AC2 — STP47 1 W3 — T7 — STP41 1 U4
RTCX1 W4 — RTCX2 V5 — RTCRST_L T5
SMALERT_L E20 — SMCLK_RESUME H18 — SMDATA_RESUME E23 — ALERT_L H21 — SMLINK0 F25 — SMLINK1 F24
R_SPI_MISO R2 — R_SPI_MOSI T1 — R_SPI_CS M8 — R_SPI_CLK P9 — TP3 1 TP3 R4

Intel design guide request

BM_BUSY#/GPIO0 T15 — FRONT_AUD_DET — FRONT_AUD_DET 23
GPIO6 W16 — GPIO7 W14 — GPIO8 K18 — GPIO9 H19 — GPIO10 M17 — GPIO12 A24 — GPIO12
GPIO13 C23 — LPCPME_L — LPCPME_L 19
GPIO14 P5 — GPIO14 — GPIO15 E24 — GPIO15
DPRSLPVR AB20 — STP66 1 — STP66
STP_PCI# Y16 — STP_PCI_L — STP_PCI_L 13
STP_CPU# AB19 — STP_CPU_L — STP_CPU_L 13
GPIO24 R3 — STP34 1 — STP34
GPIO25 C24 — GPIO25 — STRAP
GPIO26 D19 — GPIO27 D20
GPIO27 F22 — STP14 1 — GPIO27 15
GPIO28 AC19 — STP69 1 — STP14
CLKRUN# U14 — GPIO33 — STP69
GPIO33 AC1 — GPIO34
GPIO34 AC23 — GPIO38
GPIO38 AC24 — GPIO39
GPIO39
CPUPWRGD/GPIO49 AB22 — H_CPUPWRGD — H_CPUPWRGD 4
THRM# AB17 — THRM_L — THRM_L 19
VRMPWRGD V16 — R_VRM_PWRGD
MCH_SYNC# AC18 — ICH_SYNC_L
PWRBTN# E21 — R_PWRBT_L
RI# H23 — RI_L — RI_L 20
SUS_STAT#/LPCPD# G22 — LPCPD_L — LPCPD_L 24
SUSCLK D22 — STP2 1 — STP2
SYS_RESET# G18 — HWRST_L — HWRST_L 18
PLTRSTB G23 — R_PLTRST_L
WAKE# C25 — PCIE_WAKE_L — PCIE_WAKE_L 21
INTRUDER# T8 — INTRUDER_L
PWROK U10 — SBOK
RSMRST# AC3 — RSMRST_L
INTVRMEN AD3 — INTVRMEN
SPKR J16 — SPKR — SPKR 18
SLP_S3# H20 — SLP3_L — SLP3_L 12,15,17,19
SLP_S4# E25 — SLP4_L — SLP4_L 6,19
SLP_S5# F21 — SLP5_L — SLP5_L 18
BATLOW# B25 — BATLOW_L
DPRSTP# AB23 — PM_DPRSTP_L — PM_DPRSTP_L 4
DPSLP# AA18 — DPSLP_L — DPSLP_L 4
RSVD F20

V1.0 TO CI3
add STP_PCI_L,STP_CPU_L,follow CRB1.0

CASE_OPEN
1
2
H2X1-W
INTRUDER_L
For CaseOpen 2010/11/15

V1.0 TO CI3
add stitching cap
close to R_AZ_BIT_CLK(R271)
+VCC3
C177 .1U-04

+12V
R237 8.2K-04
Q25 2N7002-S
SMDATA_RESUME — SMDATA_RESUME 14
R202 0-04-O
SMDATA_MAIN — SMDATA_MAIN 11,13,24
Q18 2N7002-S
SMCLK_RESUME — SMCLK_RESUME 14
R201 0-04-O
SMCLK_MAIN — SMCLK_MAIN 11,13,24

H_CPUPWRGD R304 1K-04-O — +VCC_1P05
PM_DPRSTP_L R298 56-04-O
DPSLP_L R341 56-04-O
INTVRMEN R307 390K-04 — +RTCVCC
INTRUDER_L R310 1M-04
ICH_SYNC_L R328 1K-04 — +VCC3
FRONT_AUD_DET R342 10K-04
SMDATA_MAIN R250 1.2K-1-04
SMCLK_MAIN R212 1.2K-1-04
SPKR R423 4.7K-04-O
GPIO33 R379 10K-04
GPIO34 R309 10K-04
GPIO38 R311 10K-04
GPIO39 R324 10K-04
SPI_HOLD0_L R386 1K-04 — +V_3P3_CLSPI
SPI_WP0_L R384 1K-04
RN24
SPI_CS
R_SPI_MISO
R_SPI_MOSI
8.2K-8P4R-04
ALERT_L R231 10K-04 — +3VSB
SMLINK0 R260 10K-04
SMLINK1 R230 10K-04
BATLOW_L R246 10K-04
GPIO27 R219 10K-04-O
SMALERT_L R218 10K-04
PLTRST_L R265 10K-04-O
SMDATA_RESUME R255 1.2K-1-04
SMCLK_RESUME R220 1.2K-1-04
GPIO14 R266 10K-04
GPIO15 R252 10K-04
GPIO12 R393 10K-04
R326 0-04
SBOK — PWROK 5,19
R217 0-04
R_PWRBT_L — PWRBT_L 19
R340 0-04
R_VRM_PWRGD — VRM_PWRGD 13,16

V.A TO V.B
ADD R300 DEL R228 follow DG2.5
RSMRST_L R300 0-04 LAN_RST_L
LAN_RST_L R228 0-04-O
RSMRST_L R275 10K-04-O
GPIO25 R253 1K-04

NEAR ICH
SPI_MOSI R282 47-04 R_SPI_MOSI
SPI_CLK R285 47-04 R_SPI_CLK
SPI_CS R277 47-04 R_SPI_CS
NEAR FLASH
SPI_MISO R385 47-04 R_SPI_MISO

R_PLTRST_L R264 0-04 — PLTRST_L 5,19,24
R_AZ_SDATA_OUT R296 33-04 — AZ_SDATA_OUT 22
R_AZ_SYNC R293 33-04 — AZ_SYNC 22
R_AZ_BIT_CLK R271 47-04 — AZ_BIT_CLK 22
R_AZ_RST_L R280 33-04 — AZ_RST_L 22
CK_14M_ICH C133 22P-04-X-O
R_AZ_RST_L C140 22P-04-X-O
R_AZ_BIT_CLK C131 22P-04-X-O

RSMRST

+3VSB
+5VSB
R327 680-04
RSMRST_L — RSMRST_L 19
R348 4.7K-04-O
RSMRST_FB
Q32 2N3904-S-O
C160 .1U-04-O
ER26 39.2K-1-04-O
0.92
Q33 2N3904-S-O
ER27 8.87K-1-04-O
C164 1U-04-O

1)AC ON: 3VSB vs RSMRST(t204: min 10ms)
2)AC OFF: 3VSB>2.1V when RSMRST<0.8V

CLR_CMOS

V.A TO V.B
change CMOS circuit
add D30,R344

CLR_CMOS	CLEAR_CMOS
N/A	NORMAL
1-2	NORMAL
2-3	CLEAR CMOS

+IO_VBAT
+RTCVCC
C143 1U-X7R
D30 BAT54C-S
D22 BAT54C-S
R351 0-04
R344
R336 1K-04
+IO_3VSB
R291 20K-04
CLR_CMOS
H3X1-R
TP14
RTCRST_L
R358 4.7K-04
VBAT
BAT1 SK-CR2032-RD
C167 1U-X7R

SPI

SPI_DEBUG
SPI_CS
SPI_MISO
SPI_WP0_L
SPI_HOLD0_L
SPI_CLK
SPI_MOSI
H4X2-B
+V_3P3_CLSPI
+3VSB
D21 BAT54C-S-O
R263 0
SMT ROM
ROM1
CS# VCC
DO HLD#
WP# SCK
GND DI
ST25VF080B-50-4C-S2AF
BC172 0.1U-10VX-04
MC45 10U-X5-08-O

RTCX1
R315 10M
RTCX2
X4
Y-32.768K
C153 15P-04
C154 15P-04

DMI DC / AC COUPLING SELECTION	
GPIO25	Function
0	* AC COUPLING MODE
1	DC COUPLING MODE

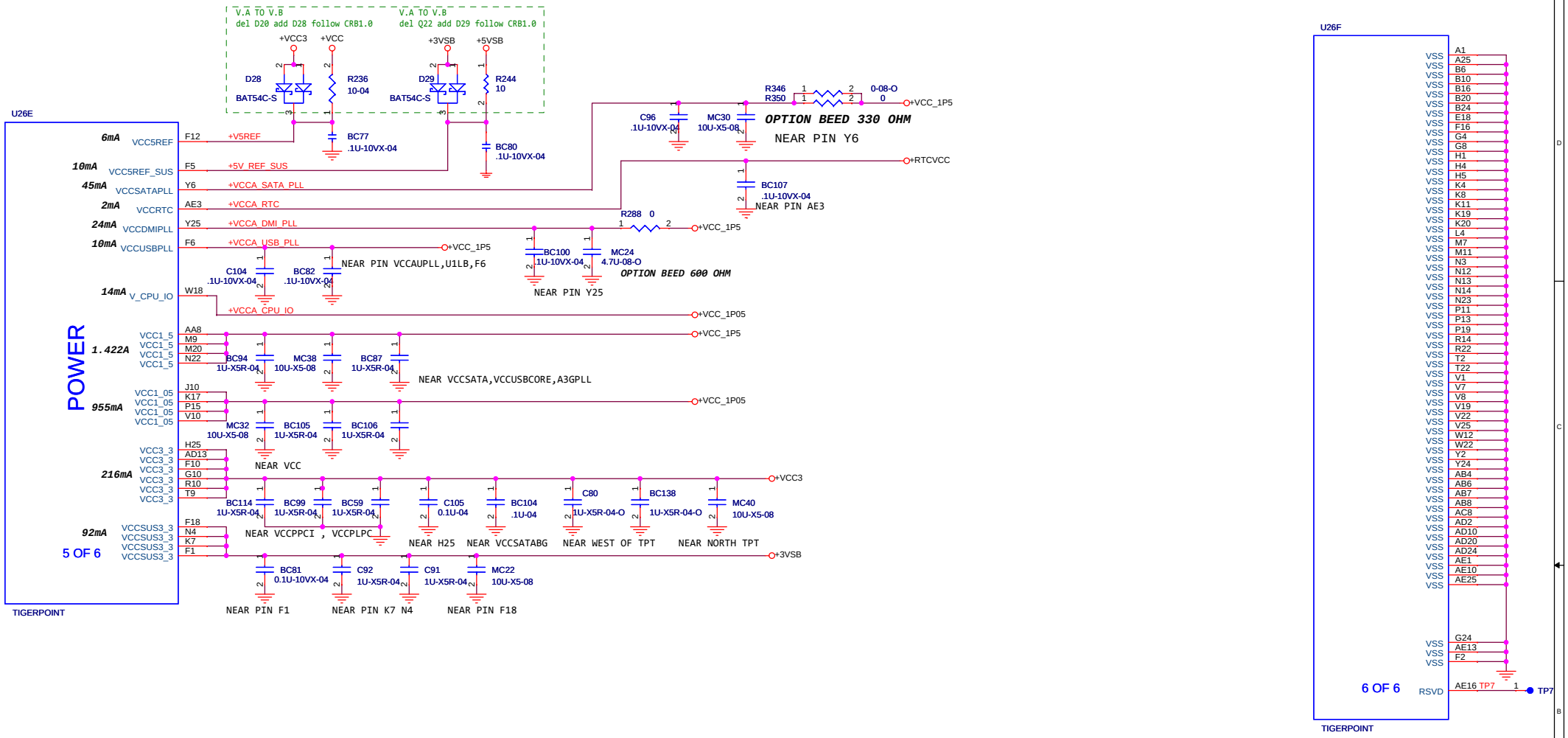
PCI EXPRESS * PORT CONFIG		
AZ_DOUT	AZ_SYNC	Function
0	0	4*1 Port
0	1	Reserved
1	0	Reserved
1	1	* 1*4 Port

Elitegroup Computer Systems

Title: Tigerpoint Part D, RTC, SPI

Size: Custom | Document Number: TIGD-CI3 | Rev: 1.1

Date: Friday, November 26, 2010 | Sheet 9 of 28



Elitegroup Computer Systems

Title: Tigerpoint Part E & F (Power)

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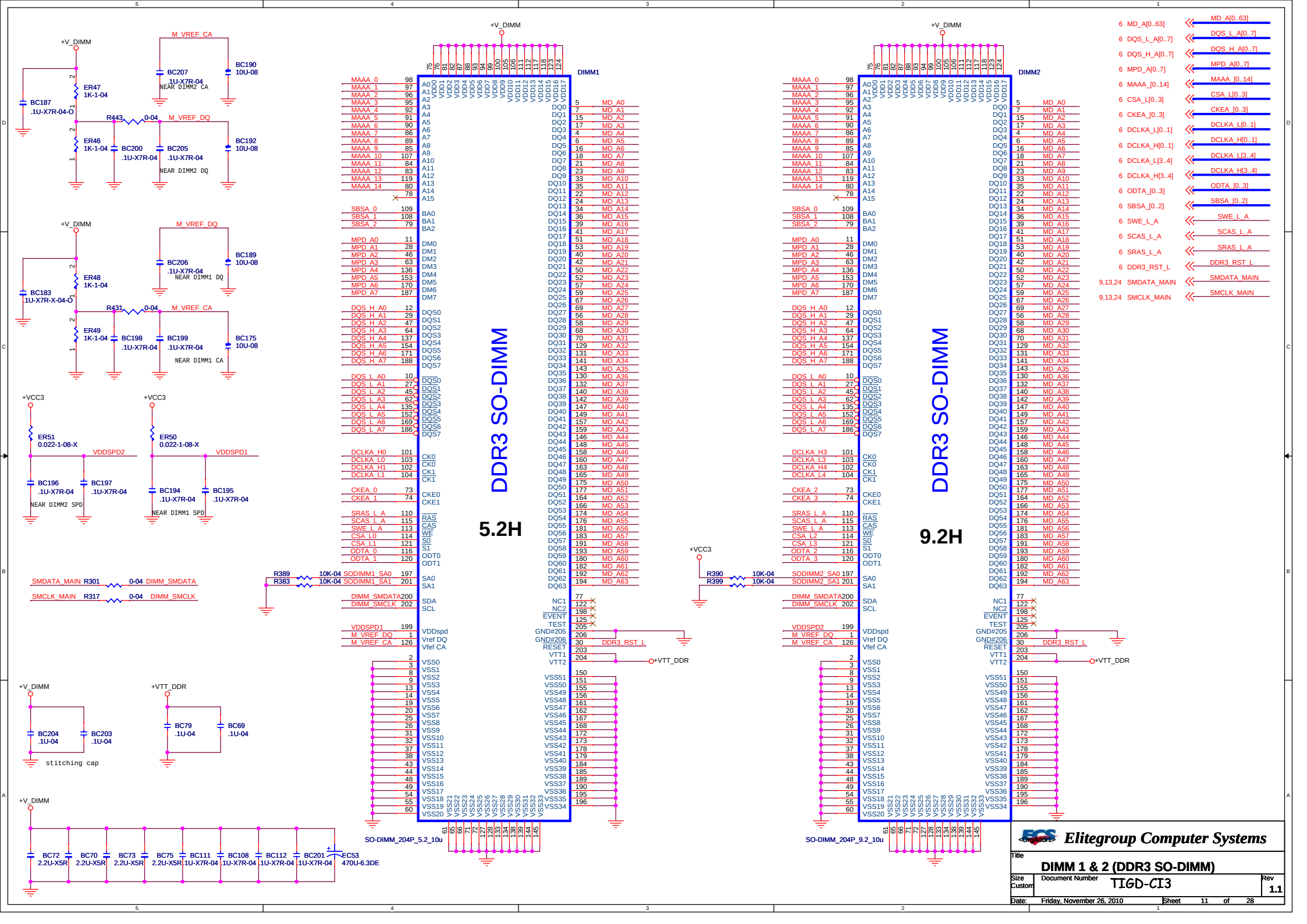
+V_DIMM
M_VREF_CA
BC207 .1U-X7R-04 NEAR DIMM2 CA
BC190 10U-08
ER47 1K-1-04
BC187 .1U-X7R-04-O
R443 0-04 M_VREF_DQ
ER46 1K-1-04
BC200 .1U-X7R-04
BC205 .1U-X7R-04 NEAR DIMM2 DQ
BC192 10U-08
M_VREF_DQ
BC206 .1U-X7R-04 NEAR DIMM1 DQ
BC189 10U-08
ER48 1K-1-04
BC183 .1U-X7R-X-04-O
R431 0-04 M_VREF_CA
ER49 1K-1-04
BC198 .1U-X7R-04
BC199 .1U-X7R-04 NEAR DIMM1 CA
BC175 10U-08
+VCC3
ER51 0.022-1-08-X
VDDSPD2
BC196 .1U-X7R-04
BC197 .1U-X7R-04 NEAR DIMM2 SPD
ER50 0.022-1-08-X
VDDSPD1
BC194 .1U-X7R-04
BC195 .1U-X7R-04 NEAR DIMM1 SPD
SMDATA_MAIN R301 0-04 DIMM_SMDATA
SMCLK_MAIN R317 0-04 DIMM_SMCLK
BC204 .1U-04
BC203 .1U-04 stitching cap
+VTT_DDR
BC79 .1U-04
BC69 .1U-04
BC72 2.2U-X5R
BC70 2.2U-X5R
BC73 2.2U-X5R
BC75 2.2U-X5R
BC111 1U-X7R-04
BC108 1U-X7R-04
BC112 1U-X7R-04
BC201 1U-X7R-04
EC53 470U-6.3DE
DIMM1
DDR3 SO-DIMM
5.2H
R389 10K-04 SODIMM1_SA0
R383 10K-04 SODIMM1_SA1
SO-DIMM_204P_5.2_10u
DIMM2
DDR3 SO-DIMM
9.2H
R390 10K-04 SODIMM2_SA0
R399 10K-04 SODIMM2_SA1
SO-DIMM_204P_9.2_10u
6 MD_A[0..63]
6 DQS_L_A[0..7]
6 DQS_H_A[0..7]
6 MPD_A[0..7]
6 MAAA_[0..14]
6 CSA_L[0..3]
6 CKEA_[0..3]
6 DCLKA_L[0..1]
6 DCLKA_H[0..1]
6 DCLKA_L[3..4]
6 DCLKA_H[3..4]
6 ODTA_[0..3]
6 SBSA_[0..2]
6 SWE_L_A
6 SCAS_L_A
6 SRAS_L_A
6 DDR3_RST_L
9,13,24 SMDATA_MAIN
9,13,24 SMCLK_MAIN
Elitegroup Computer Systems
Title
DIMM 1 & 2 (DDR3 SO-DIMM)
Size Custom
Document Number TIGD-CI3
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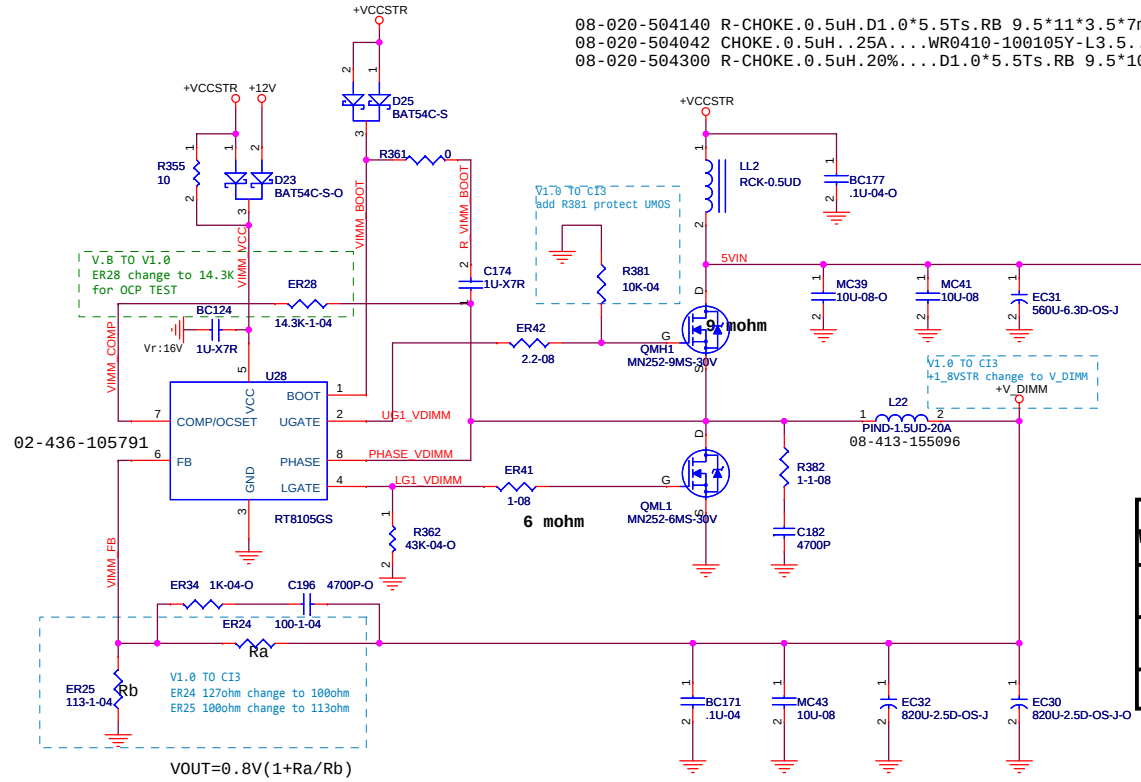
DDR / VTT_DDR

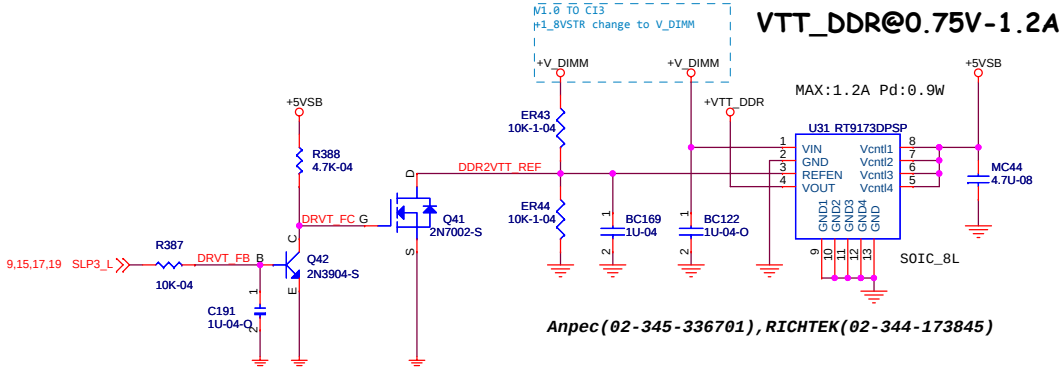
08-020-504140 R-CHOKE.0.5uH.D1.0*5.5Ts.RB 9.5*11*3.5*7mm.IPB0410N-R50.LEAD-FREE.MINGSTAR.
08-020-504042 CHOKE.0.5uH..25A....WR0410-100105Y-L3.5..LEAD-FREE.MAGIC
08-020-504300 R-CHOKE.0.5uH.20%....D1.0*5.5Ts.RB 9.5*10.5*3.5*7mm.R0410-0R5M-PF....LEAD-FREE.SUNLEI



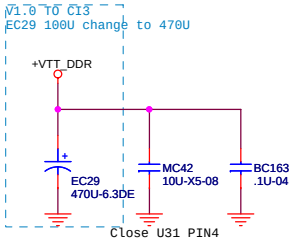
OCP 24.20A
V_DIMM@1.5V-12.10A

V_1P8_PLLSFR	0.32 A
VCC_1P5	8.202A
V_SM	3.27A
V_SM_VTT	0.3 A

VTT_DDR@0.75V-1.2A



Anpec(02-345-336701),RICHTEK(02-344-173845)



Elitegroup Computer Systems			
Title: DDR / VTT_DDR			
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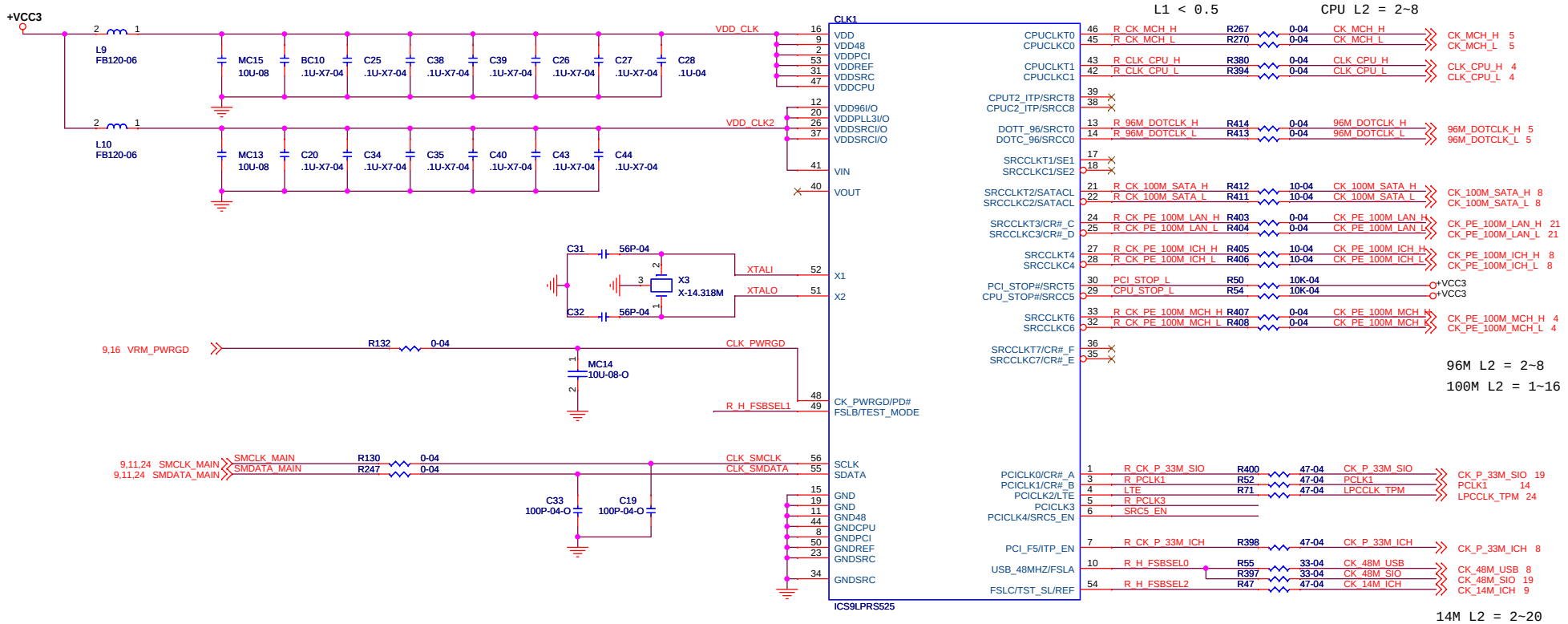

FSBSEL2	FSBSEL1	FSBSEL0	Frequence
0	0	0	266.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	100.00
1	1	0	400.00

	HIGH	LOW	FUNCTION
PIN4 LTE	* DISABLE	ENABLE	OVER CLOCK
PIN6 SRC5_EN	ENABLE	* DISABLE	SRC5
PIN7 ITP_EN	* ENABLE	DISABLE	ITP

Elitegroup Computer Systems

Title: Clock Generator - ICS9LP525

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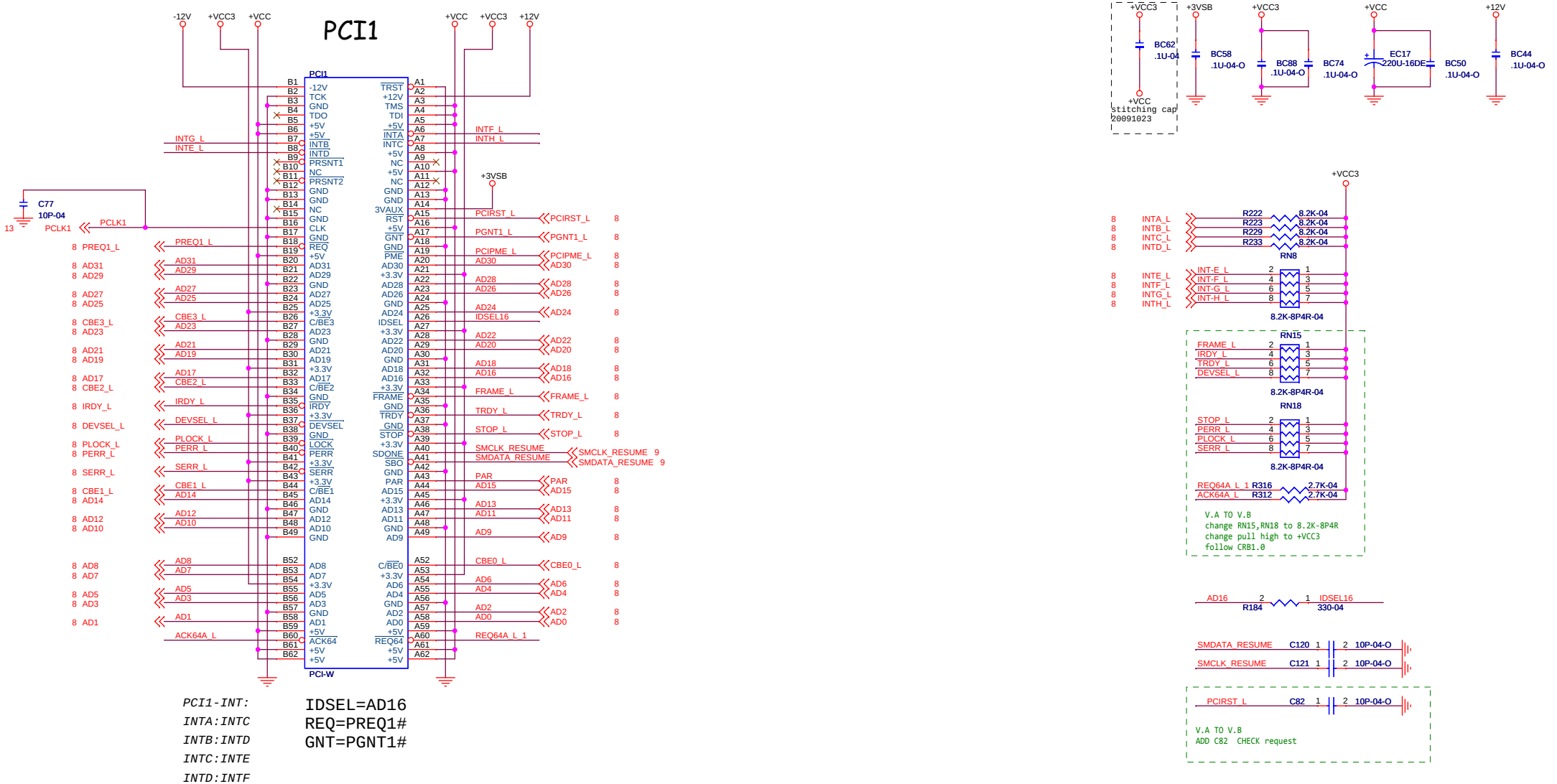

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Title	PCI Slot		
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USB Head1

02D348-536550 2009-9-16

9,12,17,19 SLP3_L → SLP3_L

+3VSB — RJ4 1K-04(1-2) — GPIO27 → GPIO27

R_USB_EN — R251 10K-04 — F_USB_EN

BC184 1U

U21 uP7536-SOT23-8: +VCC, +5VSB, GND, EN#/EN, 5VCCVOUT, 5VSBVOUT, OC#, S3# → USB3_OC_L, SLP3_L

BC57 .1U-04

+USBPWR3 — R449 1K-04 — EC20 220U-16DE

R248 10K-04: +3VSB → USB3_OC_L → USB3_OC_L 8

EN#	RJ4	USBVCC@S4/S5	Customer
GPIO27	0ohm(2-3)	Hi 5V Lo 0V	China one SPEC w/USBVCC @S4/S5
* 3VSB	1K(1-2)	Hi 5V	

RN43 0-8P4R

8 USBP4P — USBP4P — P4_P

8 USBP4N — USBP4N — P4_N

8 USBP5P — USBP5P — P5_P

8 USBP5N — USBP5N — P5_N

Co-lay CMK-90-8P4R

+USBPWR3 — U19 AZC099-04S-O: P4_N, P5_N → P4_P, P5_P

USB 4,5

+USBPWR3 — USB3 H5X2-P9E-Y: VCC1, VCC2, DATA0-, DATA1-, DATA0+, DATA1+, GND1, GND2, NC, OC

P4_N, P4_P → P5_N, P5_P

GND, GND

USB Head2

U23 uP7536-SOT23-8: +VCC, +5VSB, F_USB_EN, EN#/EN, 5VCCVOUT, 5VSBVOUT, GND, OC#, S3# → USB4_OC_L, SLP3_L

BC56 .1U-04

+USBPWR4 — R452 1K-04 — EC19 220U-16DE

+3VSB — R235 10K-04 — USB4_OC_L → USB4_OC_L 8

RN45 0-8P4R

8 USBP6P — USBP6P — P6_P

8 USBP6N — USBP6N — P6_N

8 USBP7P — USBP7P — P7_P

8 USBP7N — USBP7N — P7_N

Co-lay CMK-90-8P4R

+USBPWR4 — U20 AZC099-04S-O: P6_N, P7_N → P6_P, P7_P

USB 6,7

+USBPWR4 — USB4 H5X2-P9E-Y: VCC1, VCC2, DATA0-, DATA1-, DATA0+, DATA1+, GND1, GND2, NC, OC

P6_N, P6_P → P7_N, P7_P

GND, GND

REAL USB1

U6 uP7536-SOT23-8: +VCC, +5VSB, R_USB_EN, EN#/EN, 5VCCVOUT, 5VSBVOUT, GND, OC#, S3# → USB1_OC_L, SLP3_L

BC2 .1U-04 → UGND

+USBPWR1 — R453 1K-04 — EC3 220U-16DE

+3VSB — R18 10K-04 — USB1_OC_L → USB1_OC_L 8

CMF3

8 USBP0P — USBP0P — P0_P

8 USBP0N — USBP0N — P0_N

8 USBP1P — USBP1P — P1_P

8 USBP1N — USBP1N — P1_N

CMK-90-8P4R

Co-lay 0-8P4R

+USBPWR1 — U10 AZC099-04S-O: P0_N, P1_N → P0_P, P1_P → UGND

USB 0,1

+USBPWR1 — USB1 USB*2: VCC, -DATA1, +DATA1, GND, HOLE; -DATA0, +DATA0, GND, HOLE

P0_N, P0_P → P1_N, P1_P

G3, G4 → G2, G1

UGND, UGND

R23 0-08-short → UGND

REAL USB_LAN

U11 uP7536-SOT23-8: +VCC, +5VSB, R_USB_EN, EN#/EN, 5VCCVOUT, 5VSBVOUT, GND, OC#, S3# → USB2_OC_L, SLP3_L

BC6 .1U-04 → UGND

+USBPWR2 — R454 1K-04 — EC4 220U-16DE

R49 10K-04: +3VSB → USB2_OC_L → USB2_OC_L 8

CMF4

8 USBP2P — USBP2P — P2_P

8 USBP2N — USBP2N — P2_N

8 USBP3P — USBP3P — P3_P

8 USBP3N — USBP3N — P3_N

CMK-90-8P4R

Co-lay CMK-90-8P4R

+USBPWR2 — U9 AZC099-04S-O: P2_N, P3_N → P2_P, P3_P → UGND

USB 2,3

+USBPWR2 — USB_LAN1A USBX2-LAN-1000: VCC, -DATA0, +DATA0, GND, HOLE; VCC, -DATA1, +DATA1, GND, HOLE

P3_N, P3_P

P2_N, P2_P

G1, G2, G3, G4

UGND, UGND

R40 Short PAD → GND, UGND

Elitegroup Computer Systems

Title: USB / SATA

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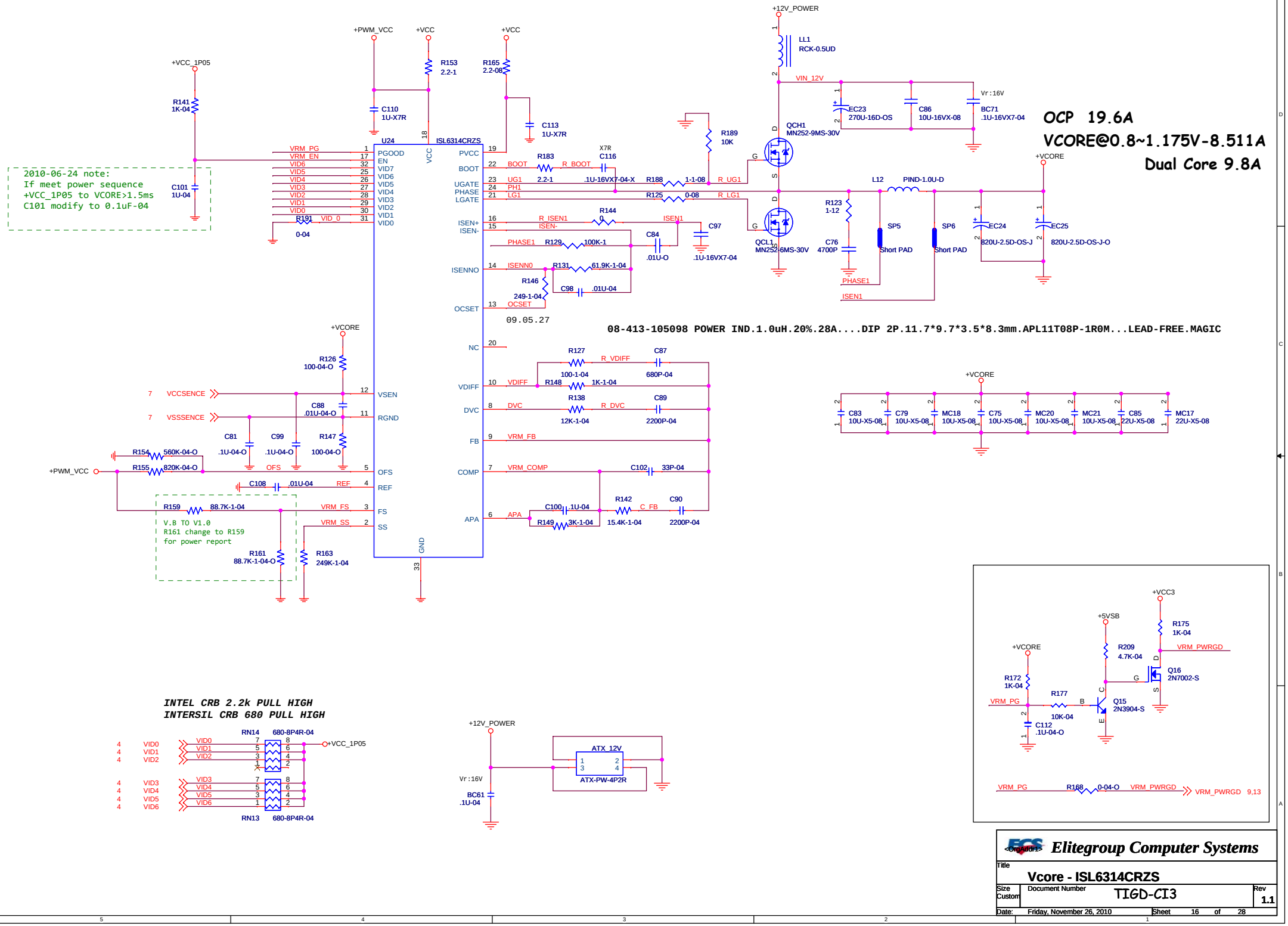
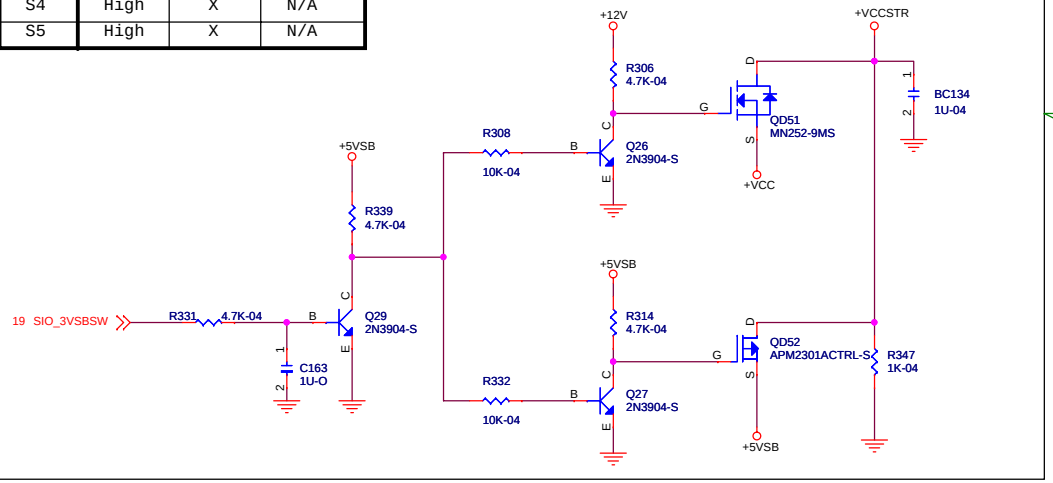

OCP 19.6A
VCORE@0.8~1.175V-8.511A
Dual Core 9.8A
2010-06-24 note:
If meet power sequence
+VCC_1P05 to VCORE>1.5ms
C101 modify to 0.1uF-04
09.05.27
08-413-105098 POWER IND.1.0uH.20%.28A....DIP 2P.11.7*9.7*3.5*8.3mm.APL11T08P-1R0M...LEAD-FREE.MAGIC
V.B TO V1.0
R161 change to R159
for power report
INTEL CRB 2.2k PULL HIGH
INTERSIL CRB 680 PULL HIGH
ISL6314CRZS
QCH1 MN252-9MS-30V
QCL1 MN252-6MS-30V
Short PAD
Short PAD
Elitegroup Computer Systems
Vcore - ISL6314CRZS
TIGD-CI3
1.1
Friday, November 26, 2010

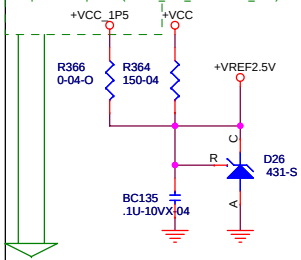
Default :

State	3VSBSW#	+VCCSTR	V Source
S0	High	v	+VCC
S1	High	v	+VCC
S2	High	v	+VCC
S3	Low	v	+5VSB
S4	High	X	N/A
S5	High	X	N/A

5V Dual(+VCCSTR for DIMM)



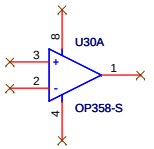
V.B TO V1.0
+VCC3 change to +VCC_1P5
for power sequence(+VCCA,CPU_IO to VCC_1P5)

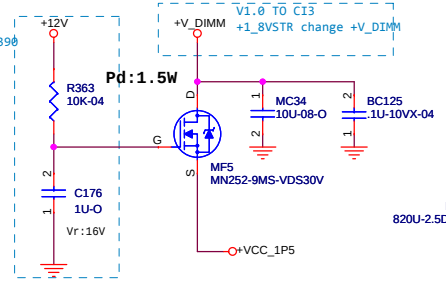


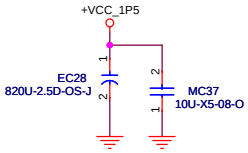
note:If use R366;
ER35,ER32 will modify value
to meet 1.05V level

Tigerpoint VCC_1P5@1.5V-1.5 A

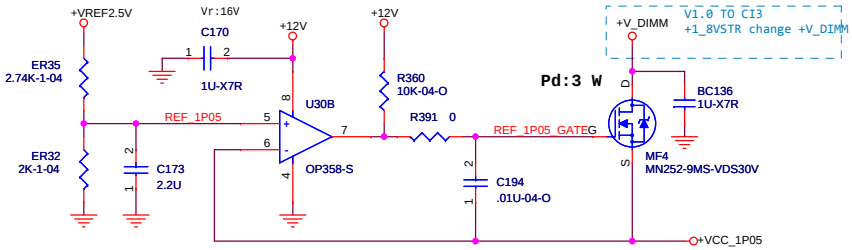
V1.0 TO CI3
change +VCC_1P5 circuit
del ER37,ER38,C176,C195,R390
add R363

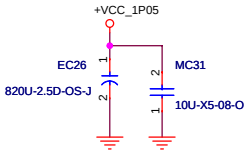






Pineview VCC_1P05@1.05V-6.34A

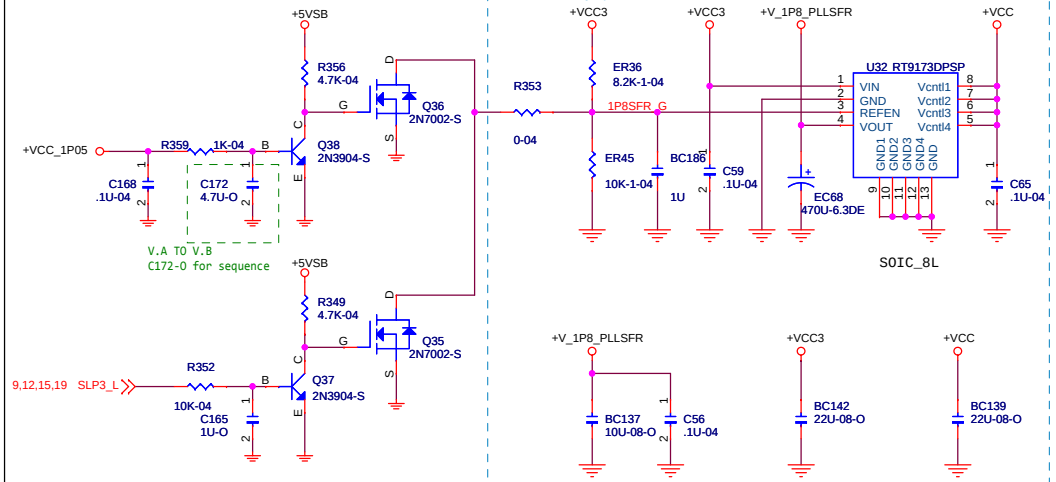




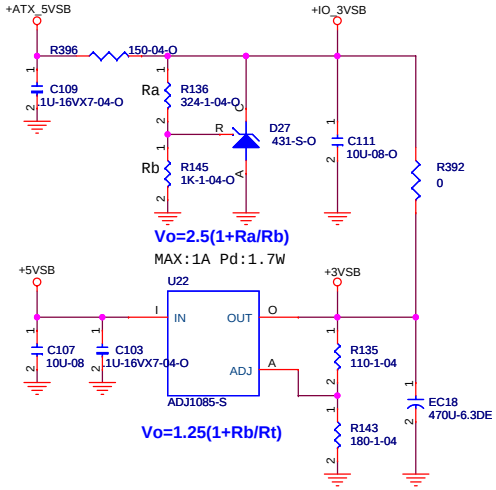
Pineview +V_1P8_PLLSFR(MAX:0.43A)

V1.0 TO CI3
Add V_1P8_PLLSFR circuit
del Q34,R351

MAX:0.43A Pd:0.65W



+3VSB(3.3V-1A);+IO_3VSB(10mA~15mA)



Elitegroup Computer Systems

Title	MIS DC-DC		
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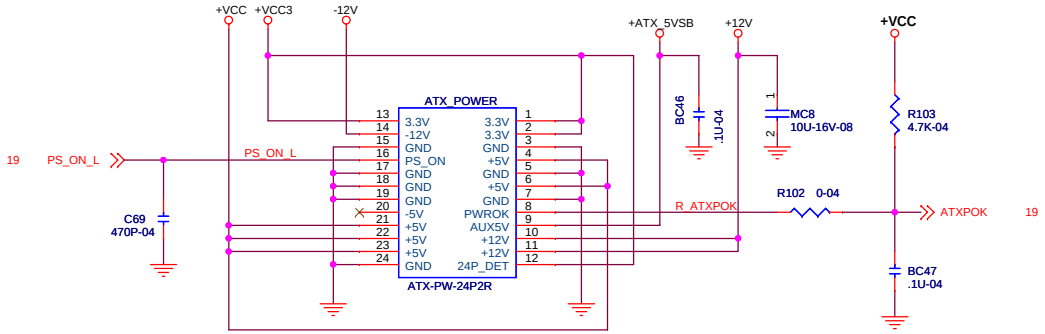
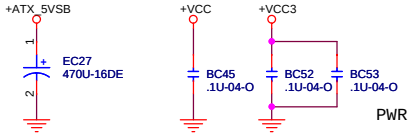
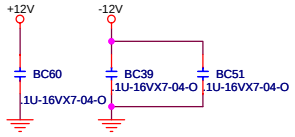
ATX Power



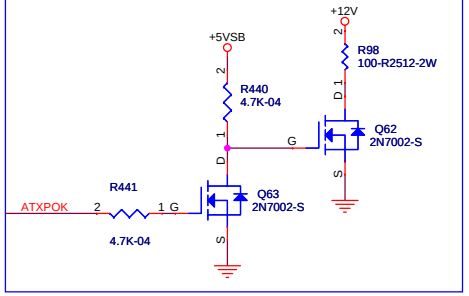


PWR CONN CAPS

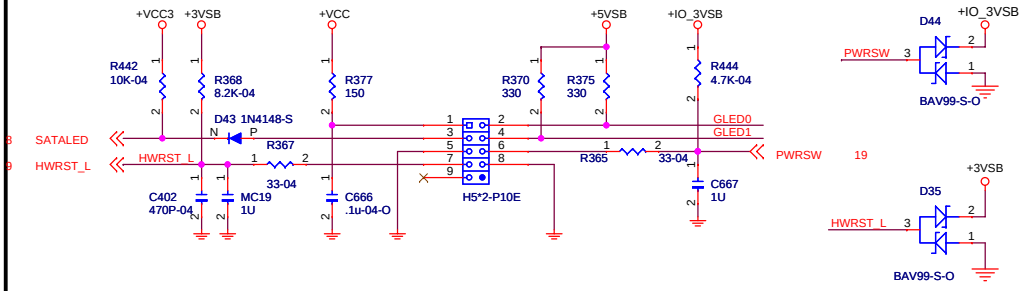
OUTPUT	Minimum Current (A)
+12V V1DC1	0.1
+12V V1DC2	0.5(CPU)
+5 VDC	0.2
+3.3 VDC	0.1
-12 VDC	0
+5 VSB	0



用100 ohm ，12V MIN LOAD 0.1A

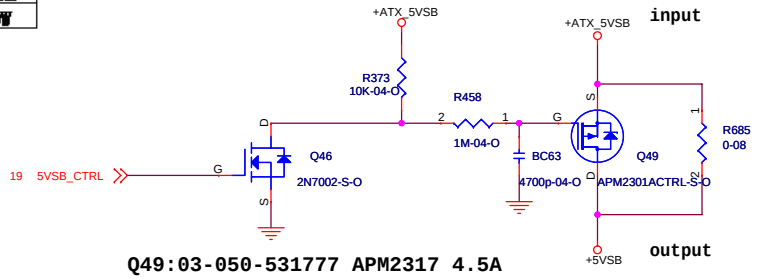


Front Panel

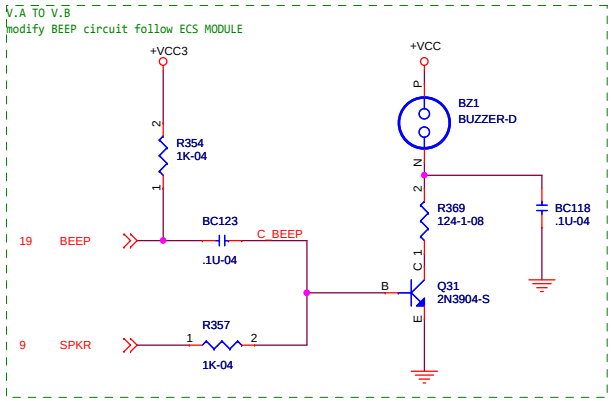


EUP Circuit

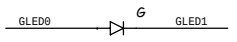
5VSB CTRL		
EUP6	+DISABLE	ENABLE
S0/S3/S4	HIGH	HIGH
S5	HIGH	LOW



Q49:03-050-531777 APM2317 4.5A

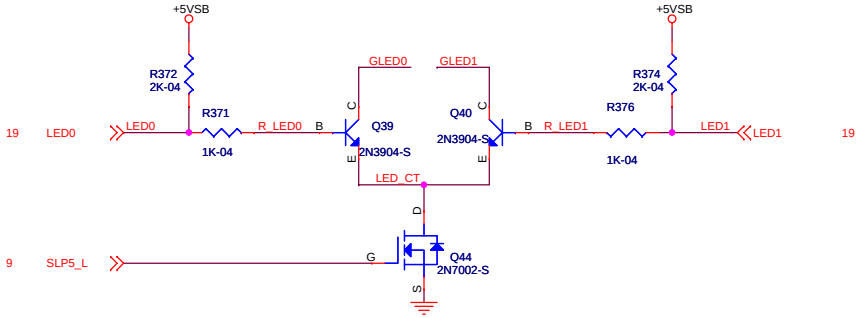


Intel



2-Pin single color LED	
S0	Steady Green
S1	Green-blinking
S3	Off
S4,S5	Off

LED



Elitegroup Computer Systems

Title	ATX Power & Front Pan	
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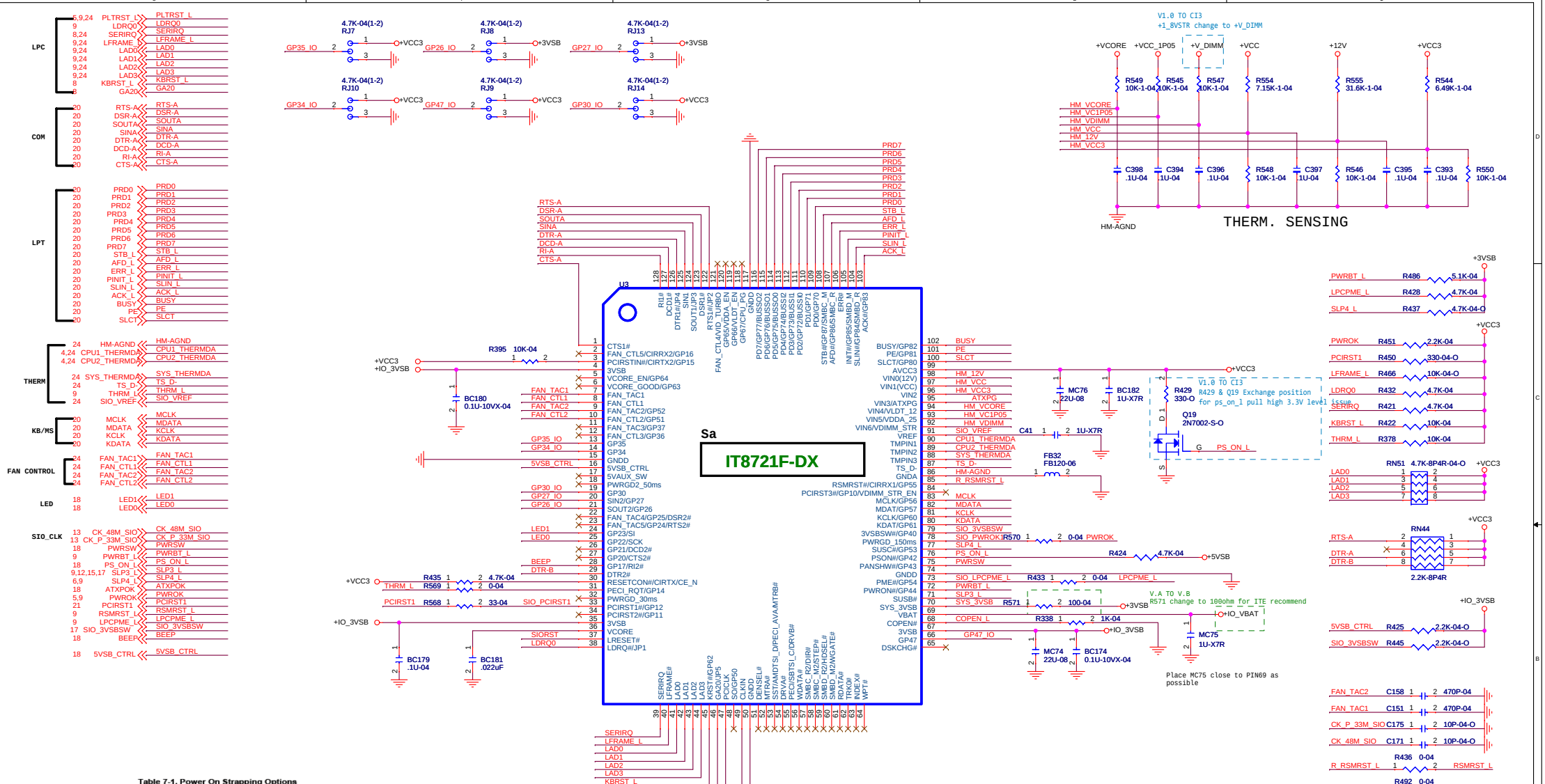

Table 7-1. Power On Strapping Options

	Symbol	Strapping Event	Value	Description
[JP2,JP6] Pin 122 & 29	VIDO_SEL	JP2: Internal VCC-OK/ LRESET# JP6: Internal VCC-OK	11	Disable VID/SVID output pins
			01	For Intel Platform Enable VIDO0~VIDO7 output pins
			10	For AMD Platform (always serial output mode) Enable SVD(pin3) / SVC(pin31) output pins
			00	For AMD Platform (Serial-in/serial-out or parallel-in/parallel-out determined by CPU) Enable VIDO0~VIDO7 output pins
JP3 Pin 124	Flashseg1_EN	Internal VCC-OK/ LRESET#	1	Disable
			0	Enable Flash I/F Address Segment FFF8_0000 ~ FFFF_FFFF & 000E_0000 ~ 000F_FFFF
JP4 Pin 126	K8PWR_EN	Internal VCC-OK	1	Disable K8 power sequence function
			0	Enable K8 power sequence function
[JP3,JP5] Pin 124 & 46	FAN_CTL_SEL	Internal VCC-OK	11	The default value of EC Index 63h/6Bh/73h is 80h.
			10	The default value of EC Index 63h/6Bh/73h is FFh.
			01	The default value of EC Index 63h/6Bh/73h is 00h.
			00	The default value of EC Index 63h/6Bh/73h is 40h.
JP5 Pin 46	WDT_EN	Internal VCC-OK	1	Disable WDT to rest PWROK
			0	Enable WDT to rest PWROK

Power On Strap

FAN_CTL_SEL
80h--> default 50%
FFh--> default 0%
00h--> default 100%
40h--> default 75%

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Title: SIO IT8721-DX

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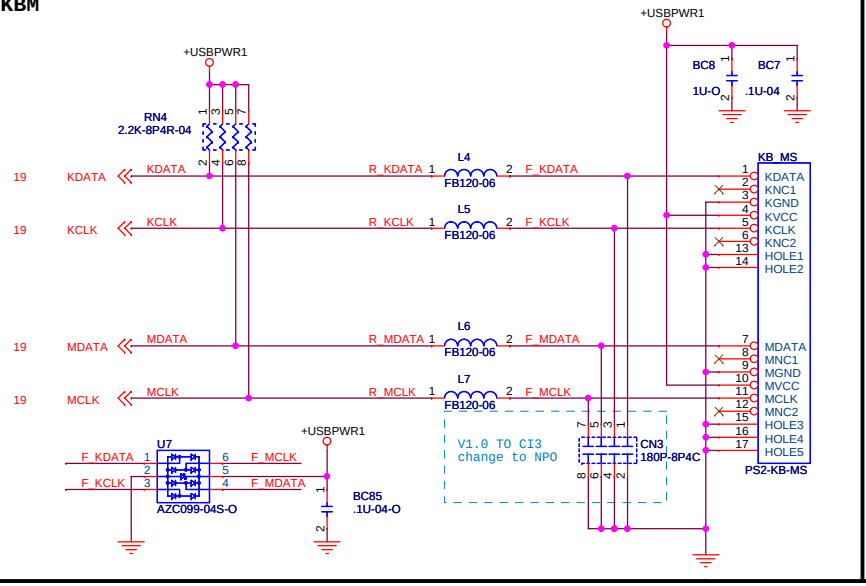
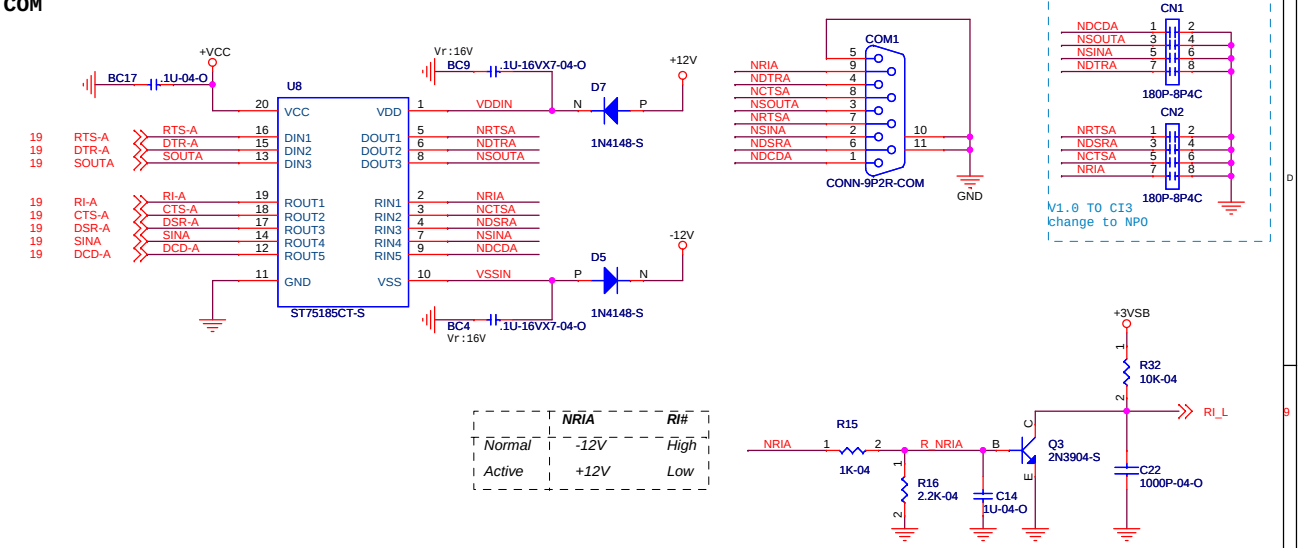
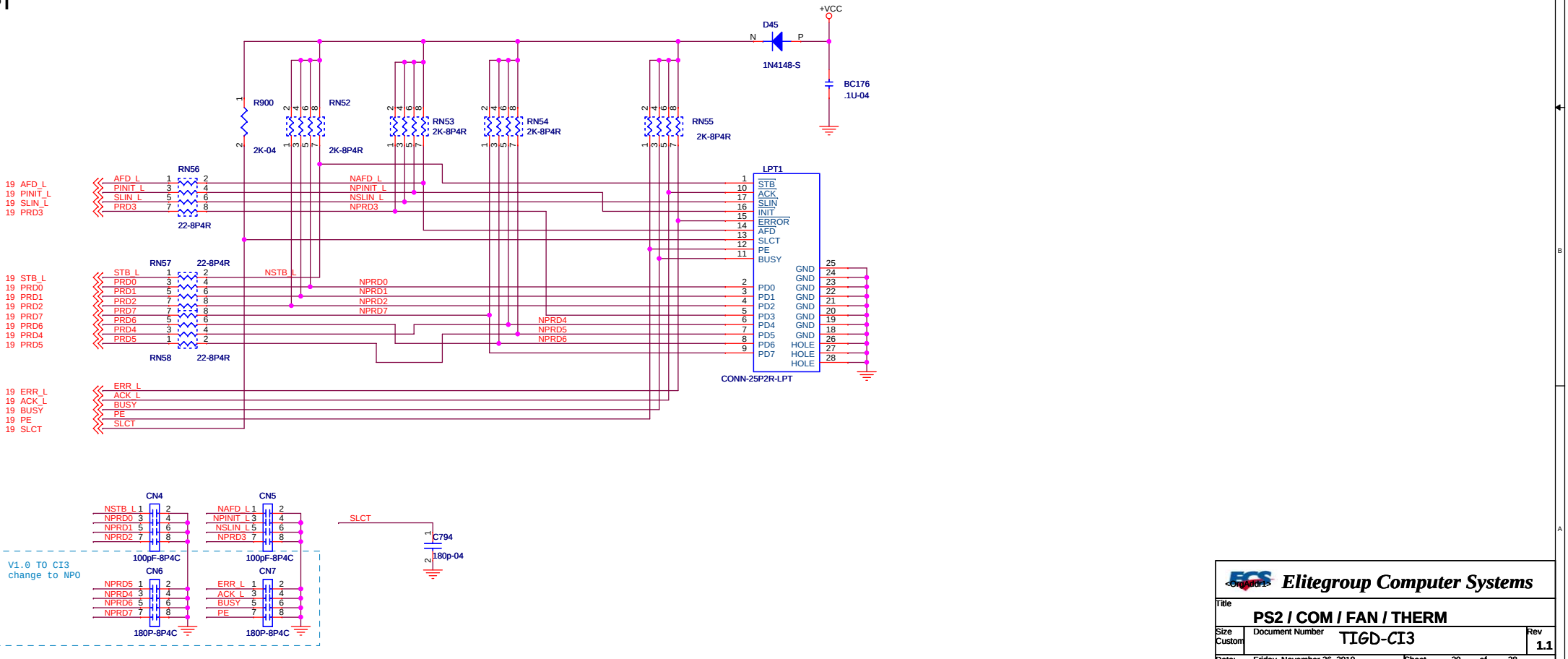
PSKBM



COM



LPT



Elitegroup Computer Systems		
Title: PS2 / COM / FAN / THERM		
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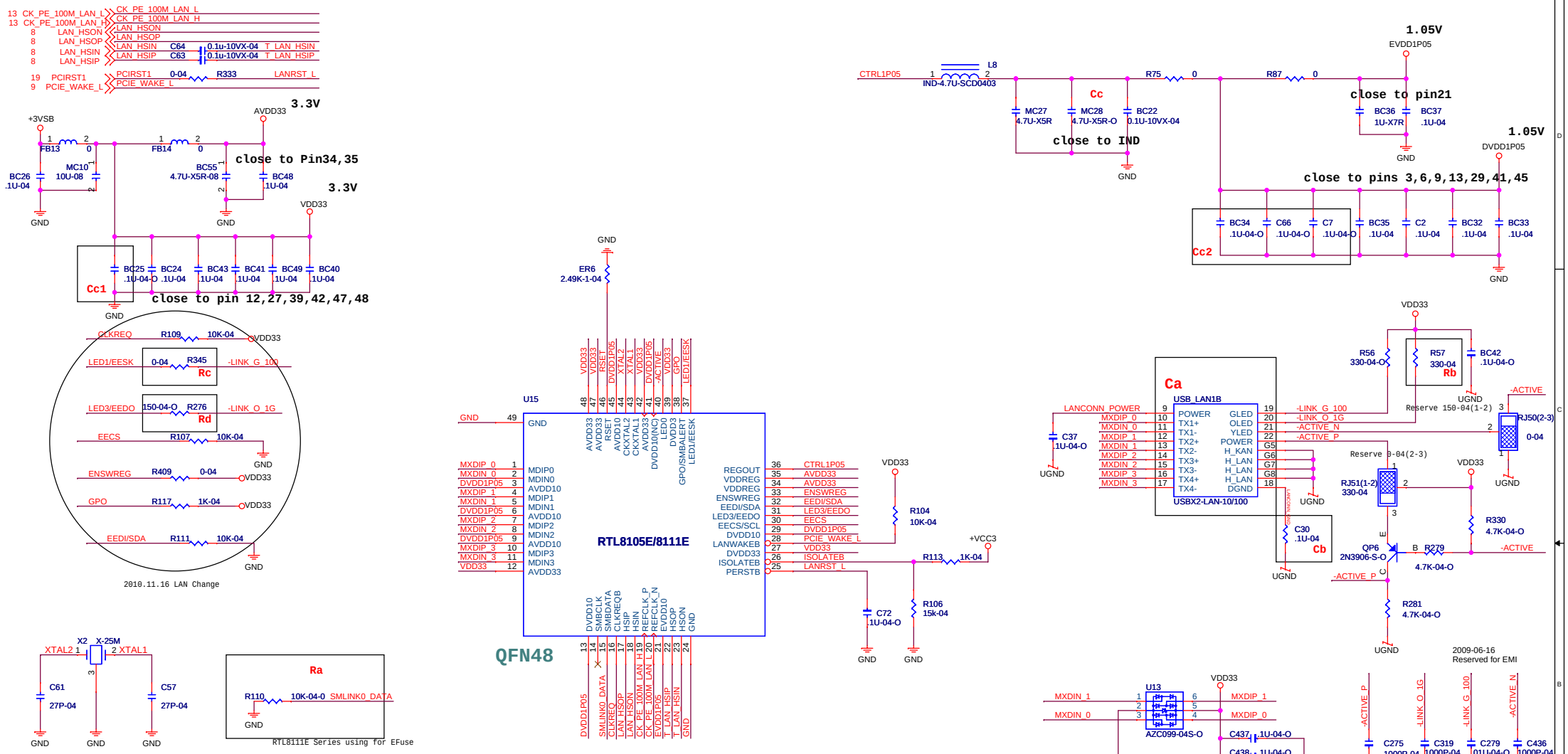


BOM Difference

*

Location	8111E Series	8105E Series
Ra	V	X
Rb	X	V
Rc	150 ohm	0 ohm
Rd	150 ohm	OPEN
Cc	V	X
Ca	USBX2-LAN-1000	USBX2-LAN-100
Cb	0 ohm	.1u-04

*

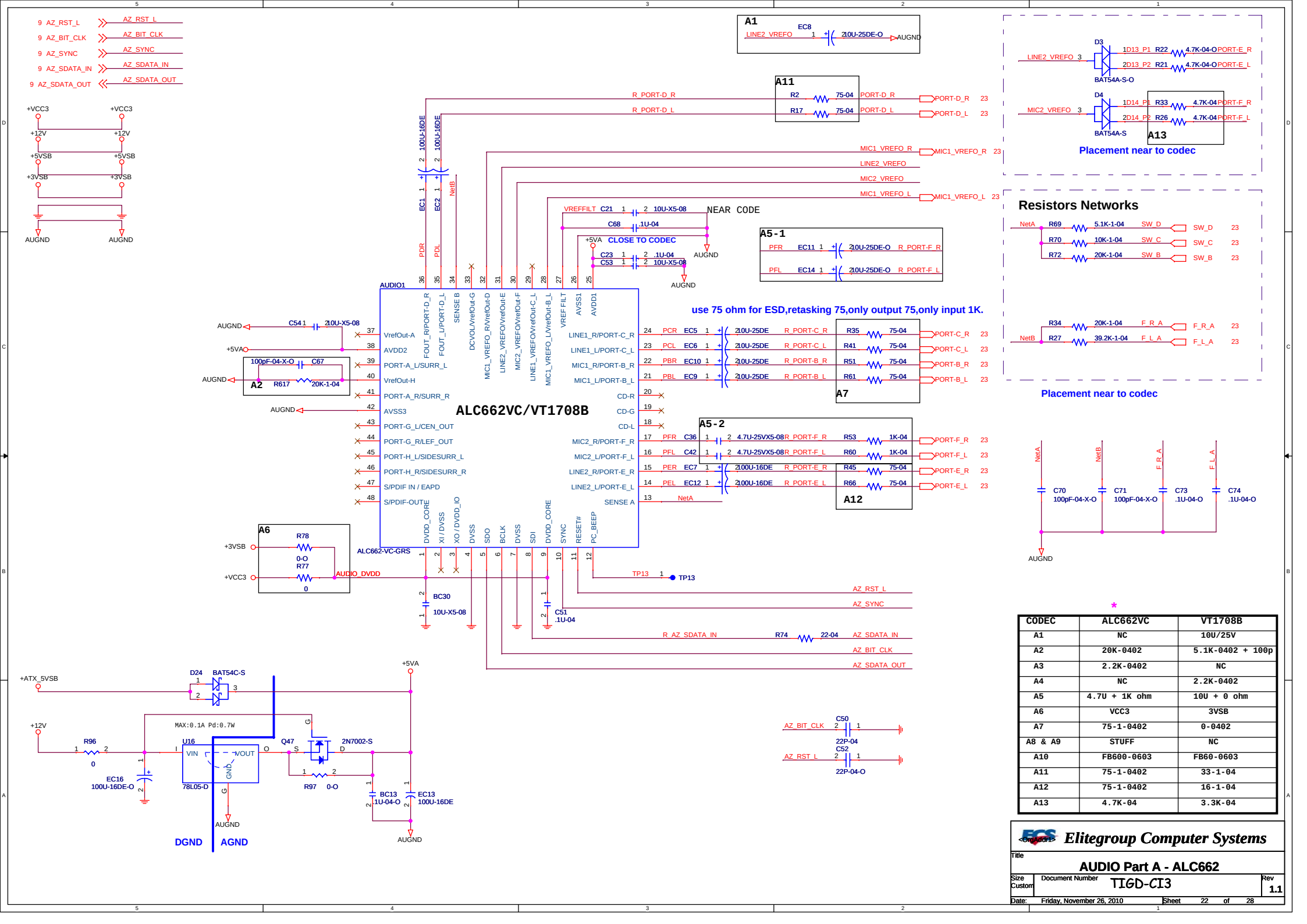
LEDS1-0	00	01	10	11
LED0	ACT_{ALL}	$Link_{ALL}$/ ACT_{ALL}	$Link10/ ACT_{ALL}$	$LINK10/ ACT_{10}$
LED1	LINK100	LINK100	LINK100	$LINK100 /ACT_{100}$
LED3	Reserved	Reserved	Reserved	Reserved

RTL8105EL(10/100) LAN LED TABLE

Speed	LINK			ACT/Full
	Link 10M	Link 100M	Link 1000M	
LED 0	Bit 0	Bit 1	Bit 2	Bit 3
LED 1	Bit 4	Bit 5	Bit 6	Bit 7
LED 3	Bit 8	Bit 9	Bit 10	Bit 11
Feature Control	Bit 12	Bit 13	Bit 14	Bit 15

RTL8111E(1G) LED TABLE

Status	Yellow	Grn/Org
No Link	Off	Off
S3/S4/S5	Off	Off
10M, inactive	Off	Off
10M, active		Off
100M, inactive	Off	
100M, active		
1G, inactive	Off	
1G, active		
Blinking		



CODEC	ALC662VC	VT1708B
A1	NC	10U/25V
A2	20K-0402	5.1K-0402 + 100p
A3	2.2K-0402	NC
A4	NC	2.2K-0402
A5	4.7U + 1K ohm	10U + 0 ohm
A6	VCC3	3VSB
A7	75-1-0402	0-0402
A8 & A9	STUFF	NC
A10	FB600-0603	FB60-0603
A11	75-1-0402	33-1-04
A12	75-1-0402	16-1-04
A13	4.7K-04	3.3K-04

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Title: AUDIO Part A - ALC662

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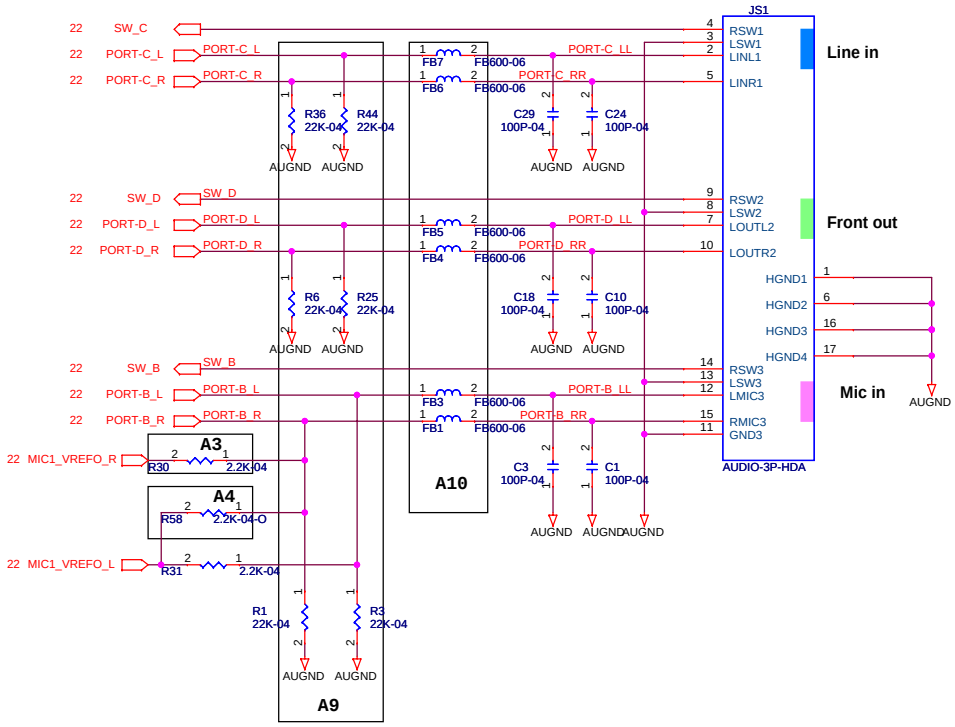

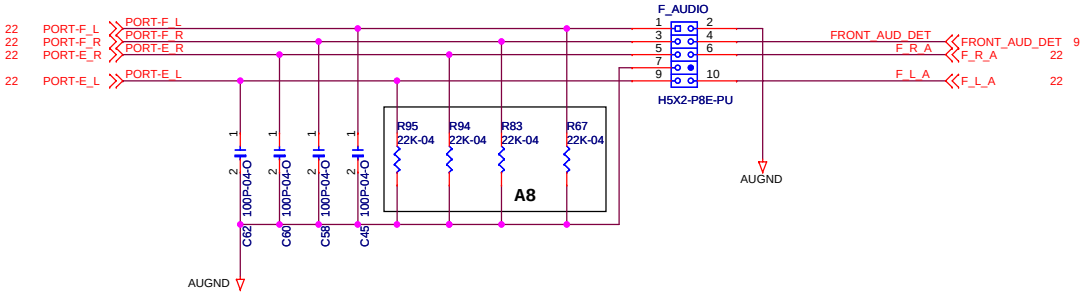

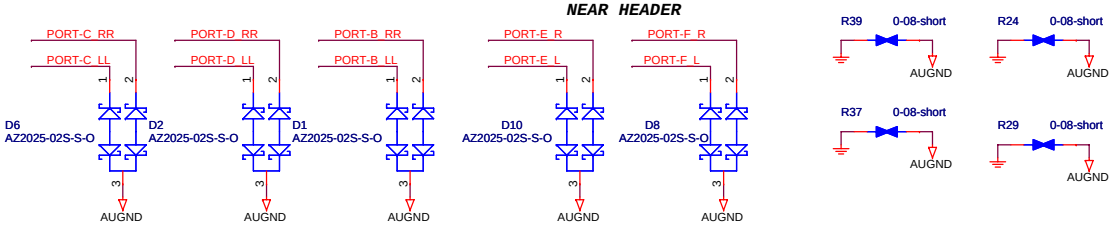

Elitegroup Computer Systems		
Title: AUDIO Part B - Panel		
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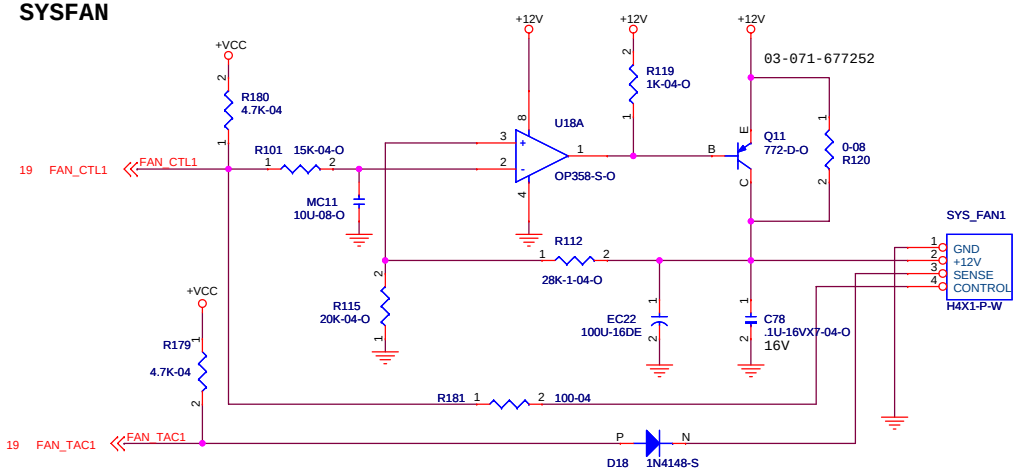
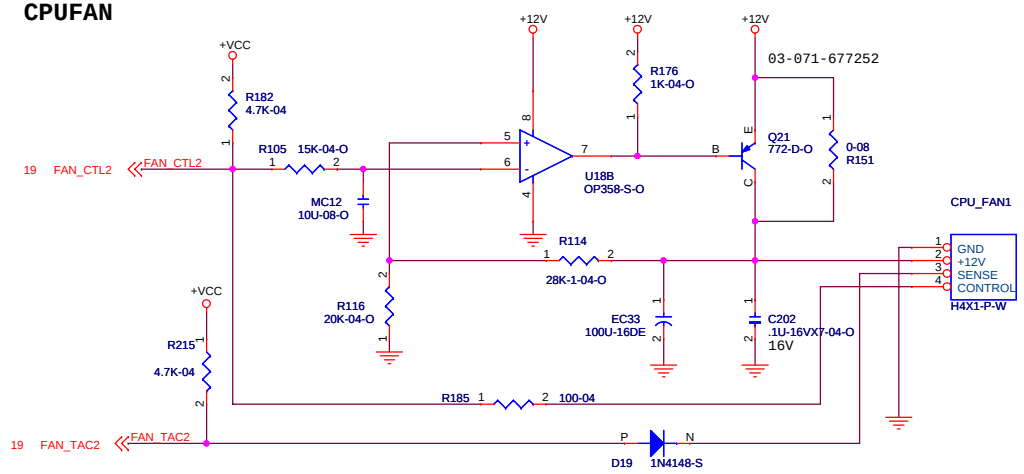
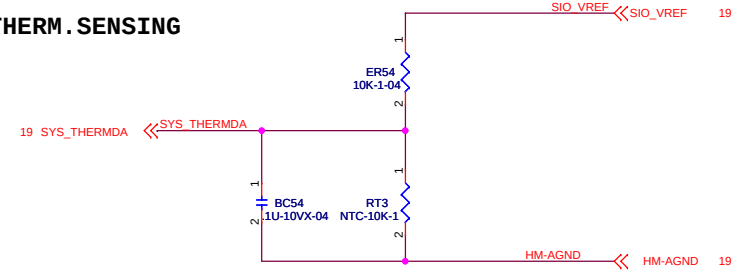
SYSFAN

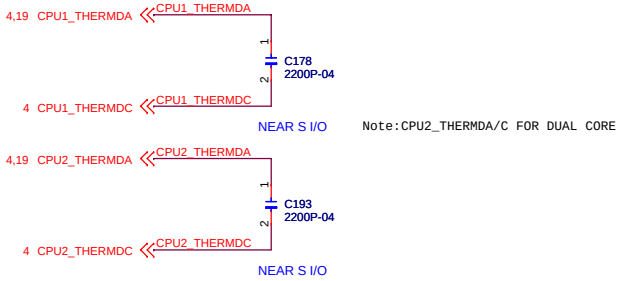


CPUFAN

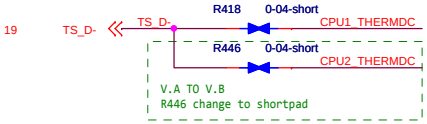


THERM.SENSING

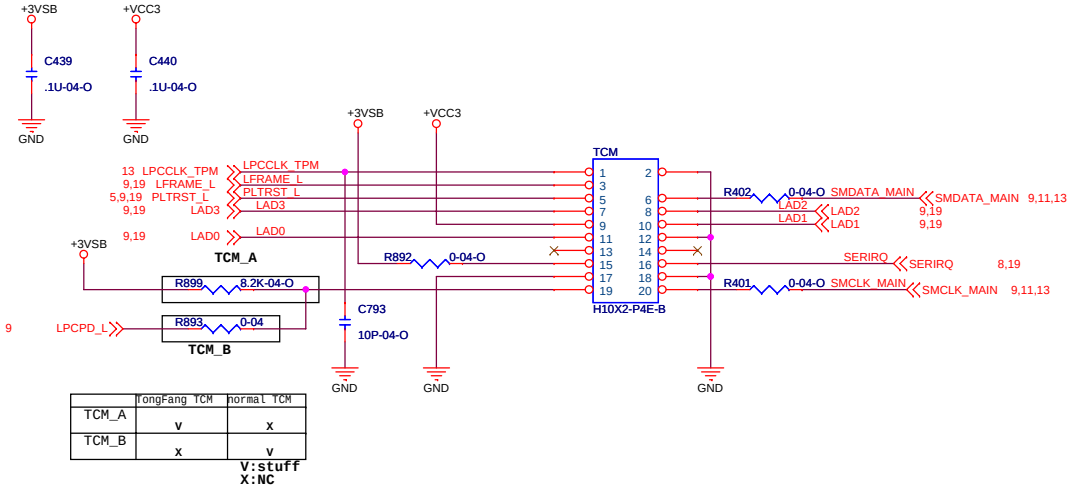




close to SIO



TCM



	TongFang TCM	normal TCM
TCM_A	v	x
TCM_B	x	v

V:stuff
X:NC

Elitegroup Computer Systems

Title: FAN / THERM / TCM

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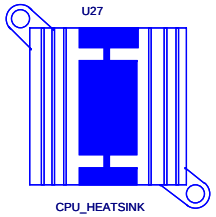
U27



CPU_HEATSINK

CLR_CMOS(1-2)

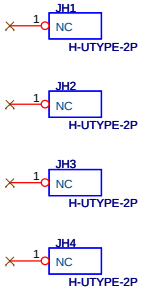
JP-R

BAT1

BATTERY

HEAT SINK setup

For 103



X4

JP-WI-P6.25

PCB Impedance control

Impedance (ohm)	Trace Width (mil) (S/W/S)	Trace Length (inch)	Pre-preg
60	5 (20/5/20)	6	2116
50	4 (50/4/50)	6	1080
42	6 (50/6/50)	6	1080

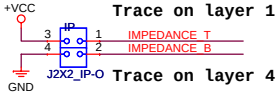
1)Circuit type 1

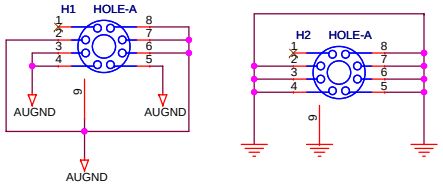
Layer 1:TOP

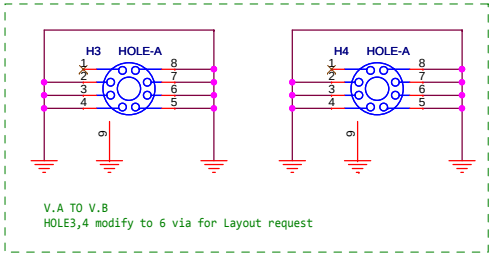
Layer 2:PWR

Layer 3:GND

Layer 4:BOTTOM







TigerPoint Strap

BOOT BIOS DESTINATION SELECTION		
GPIO17	GPIO48	Function
0	1	SPI
1	0	PCI
1	1	LPC

DMI DC / AC COUPLING SELECTION	
GPIO25	Function
0	AC COUPLING MODE
1	DC COUPLING MODE

PCI EXPRESS * PORT CONFIG		
AZ_DOUT	AZ_SYNC	Function
0	0	4 * 1 Port
0	1	Reserved
1	0	Reserved
1	1	1 * 4 Port

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Title: 104, Impedance, Attention

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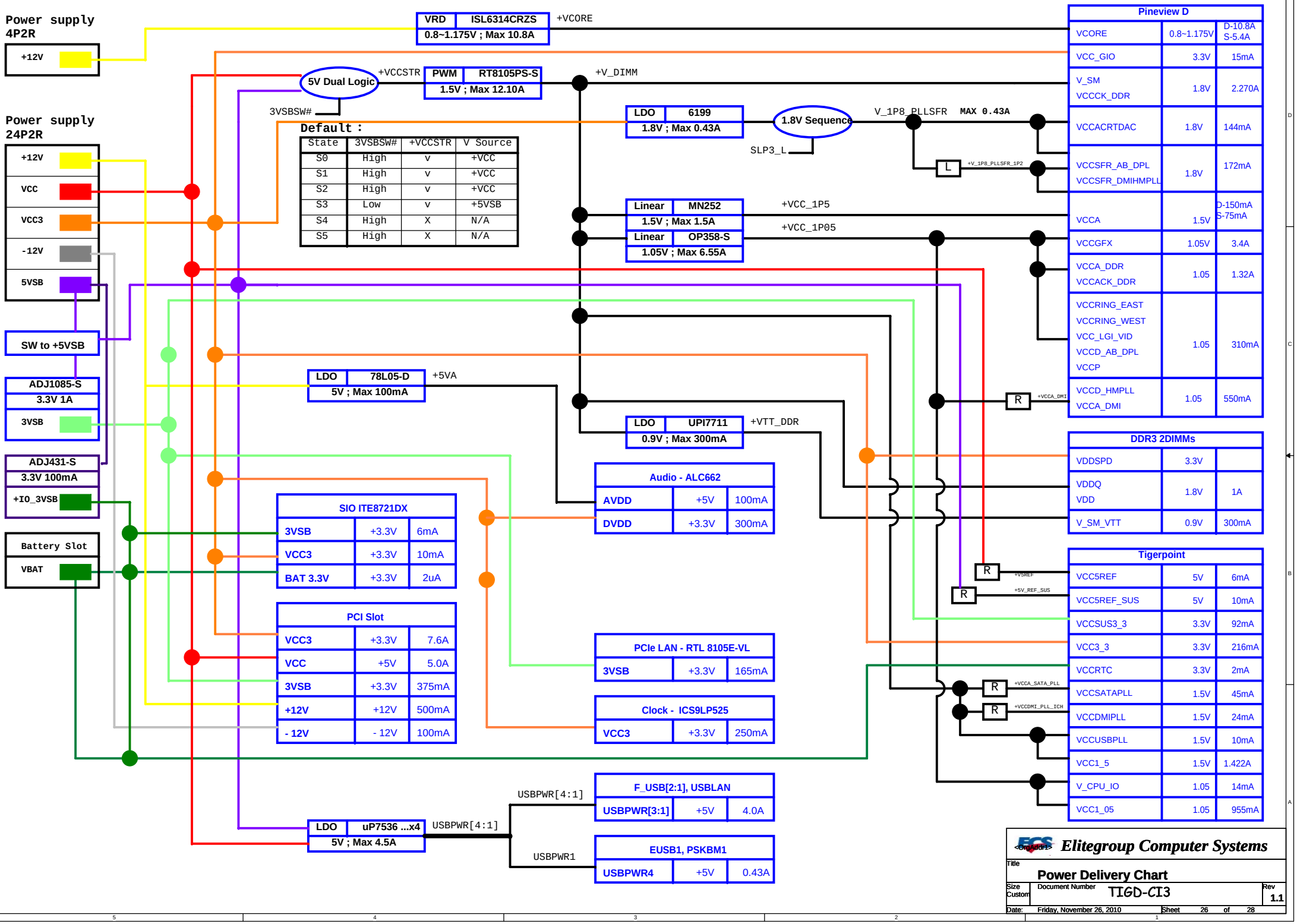
Power supply 4P2R
+12V
Power supply 24P2R
+12V
VCC
VCC3
-12V
5VSB
SW to +5VSB
ADJ1085-S
3.3V 1A
3VSB
ADJ431-S
3.3V 100mA
+IO_3VSB
Battery Slot
VBAT
VRD ISL6314CRZS
0.8~1.175V ; Max 10.8A
+VCORE
5V Dual Logic
+VCCSTR
PWM RT8105PS-S
1.5V ; Max 12.10A
+V_DIMM
3VSBSW#
Default :
State 3VSBSW# +VCCSTR V Source
S0 High v +VCC
S1 High v +VCC
S2 High v +VCC
S3 Low v +5VSB
S4 High X N/A
S5 High X N/A
LDO 6199
1.8V ; Max 0.43A
1.8V Sequence
SLP3_L
V_1P8_PLLSFR MAX 0.43A
L
+V_1P8_PLLSFR_1P2
Linear MN252
1.5V ; Max 1.5A
+VCC_1P5
Linear OP358-S
1.05V ; Max 6.55A
+VCC_1P05
LDO 78L05-D
5V ; Max 100mA
+5VA
LDO UPI7711
0.9V ; Max 300mA
+VTT_DDR
R
+VCCA_DMI
Audio - ALC662
AVDD +5V 100mA
DVDD +3.3V 300mA
SIO ITE8721DX
3VSB +3.3V 6mA
VCC3 +3.3V 10mA
BAT 3.3V +3.3V 2uA
PCI Slot
VCC3 +3.3V 7.6A
VCC +5V 5.0A
3VSB +3.3V 375mA
+12V +12V 500mA
- 12V - 12V 100mA
PCIe LAN - RTL 8105E-VL
3VSB +3.3V 165mA
Clock - ICS9LP525
VCC3 +3.3V 250mA
R
+VSREF
R
+5V_REF_SUS
R
+VCCA_SATA_PLL
R
+VCCDMI_PLL_ICH
LDO uP7536 ...x4
5V ; Max 4.5A
USBPWR[4:1]
USBPWR[4:1]
USBPWR1
F_USB[2:1], USBLAN
USBPWR[3:1] +5V 4.0A
EUSB1, PSKBM1
USBPWR4 +5V 0.43A
Pineview D
VCORE 0.8~1.175V D-10.8A S-5.4A
VCC_GIO 3.3V 15mA
V_SM VCCCK_DDR 1.8V 2.270A
VCCACRTDAC 1.8V 144mA
VCCSFR_AB_DPL VCCSFR_DMIHMPLL 1.8V 172mA
VCCA 1.5V D-150mA S-75mA
VCCGFX 1.05V 3.4A
VCCA_DDR VCCACK_DDR 1.05 1.32A
VCCRING_EAST VCCRING_WEST VCC_LGI_VID VCCD_AB_DPL VCCP 1.05 310mA
VCCD_HMPLL VCCA_DMI 1.05 550mA
DDR3 2DIMMs
VDDSPD 3.3V
VDDQ VDD 1.8V 1A
V_SM_VTT 0.9V 300mA
Tigerpoint
VCC5REF 5V 6mA
VCC5REF_SUS 5V 10mA
VCCSUS3_3 3.3V 92mA
VCC3_3 3.3V 216mA
VCCRTC 3.3V 2mA
VCCSATAPLL 1.5V 45mA
VCCDMIPLL 1.5V 24mA
VCCUSBPLL 1.5V 10mA
VCC1_5 1.5V 1.422A
V_CPU_IO 1.05 14mA
VCC1_05 1.05 955mA
Elitegroup Computer Systems
Title
Power Delivery Chart
Size Custom
Document Number TIGD-CI3
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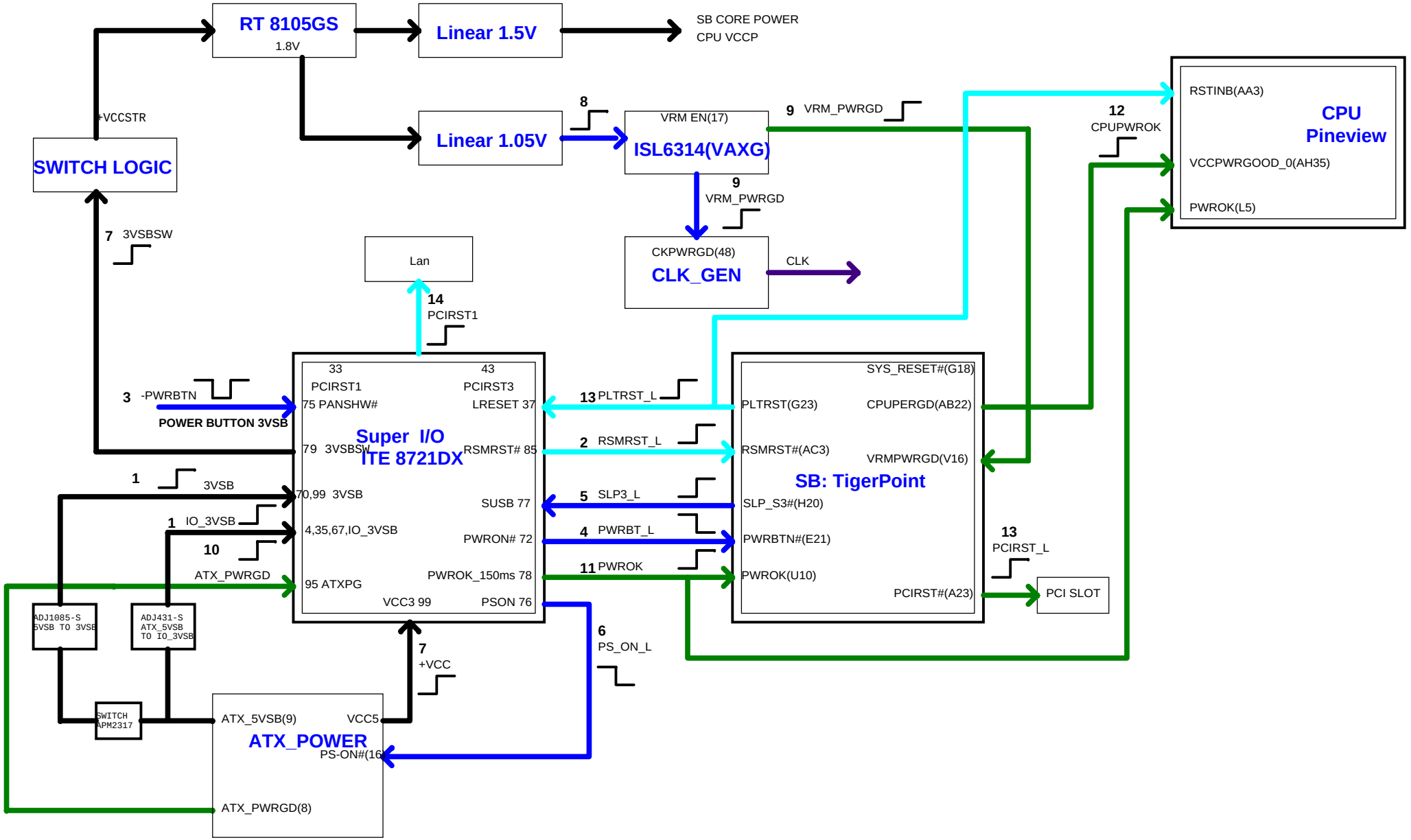

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Title: Power Sequencing Diagram

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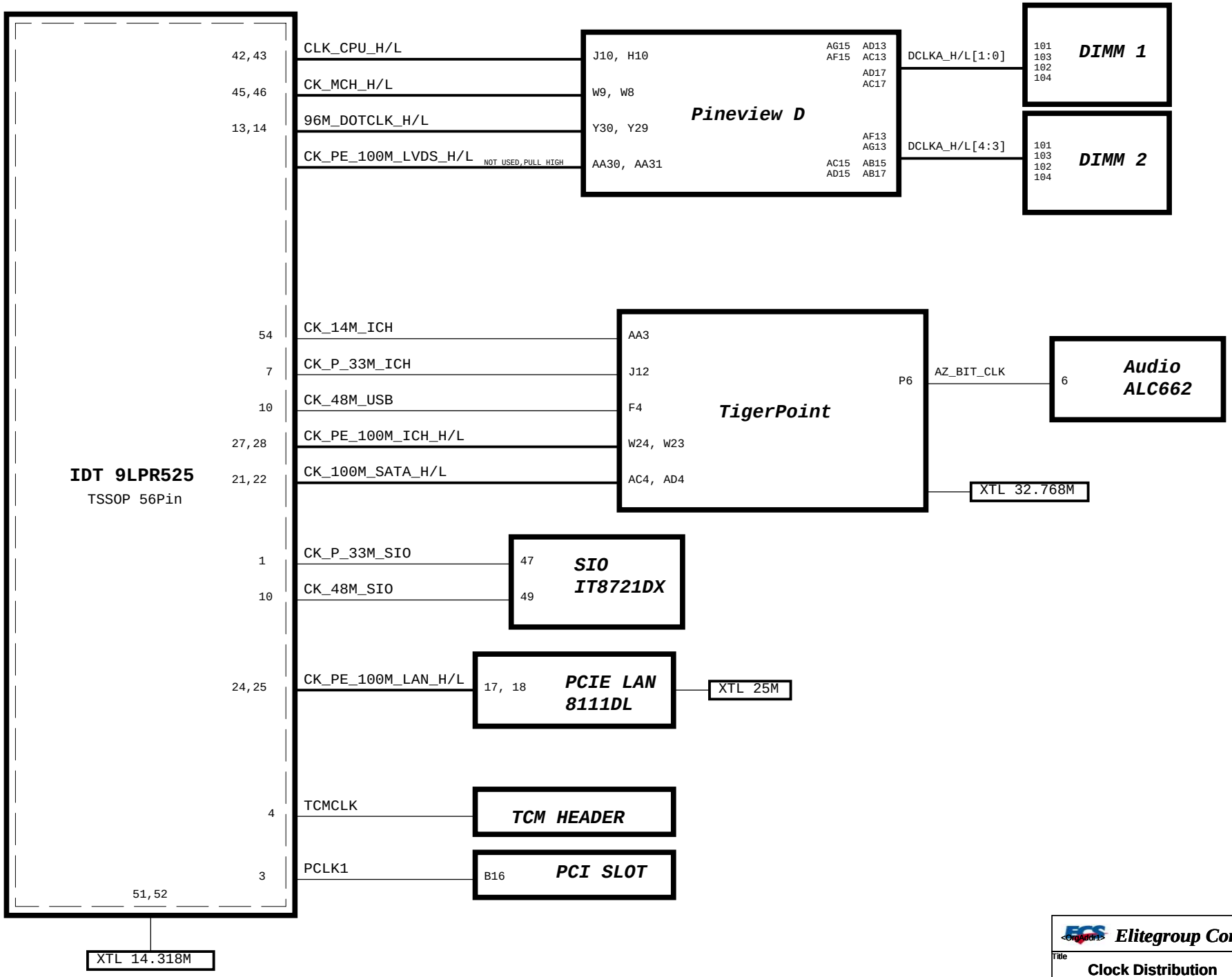

Elitegroup Computer Systems

Title: Clock Distribution

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