Compal Confidential

Model Name :Q5WV1/Q5WS1
Compal Project Name :
File Name : LA-7912P

Compal Confidential

Q5WV1 M/B Schematics Document

Intel Sandy/Ivy Bridge Processor with DDRIII + Panther Point PCH

Nvidia N13P GS/GL

2011-12-24

REV:0.2

MB PCB

Part Number	Description
DA60000SV00	PCB 0N4 LA-7912P REV0 M/B

ZZZ2 1G@ X76344BOL01

ZZZ3 2G@ X76344BOL02

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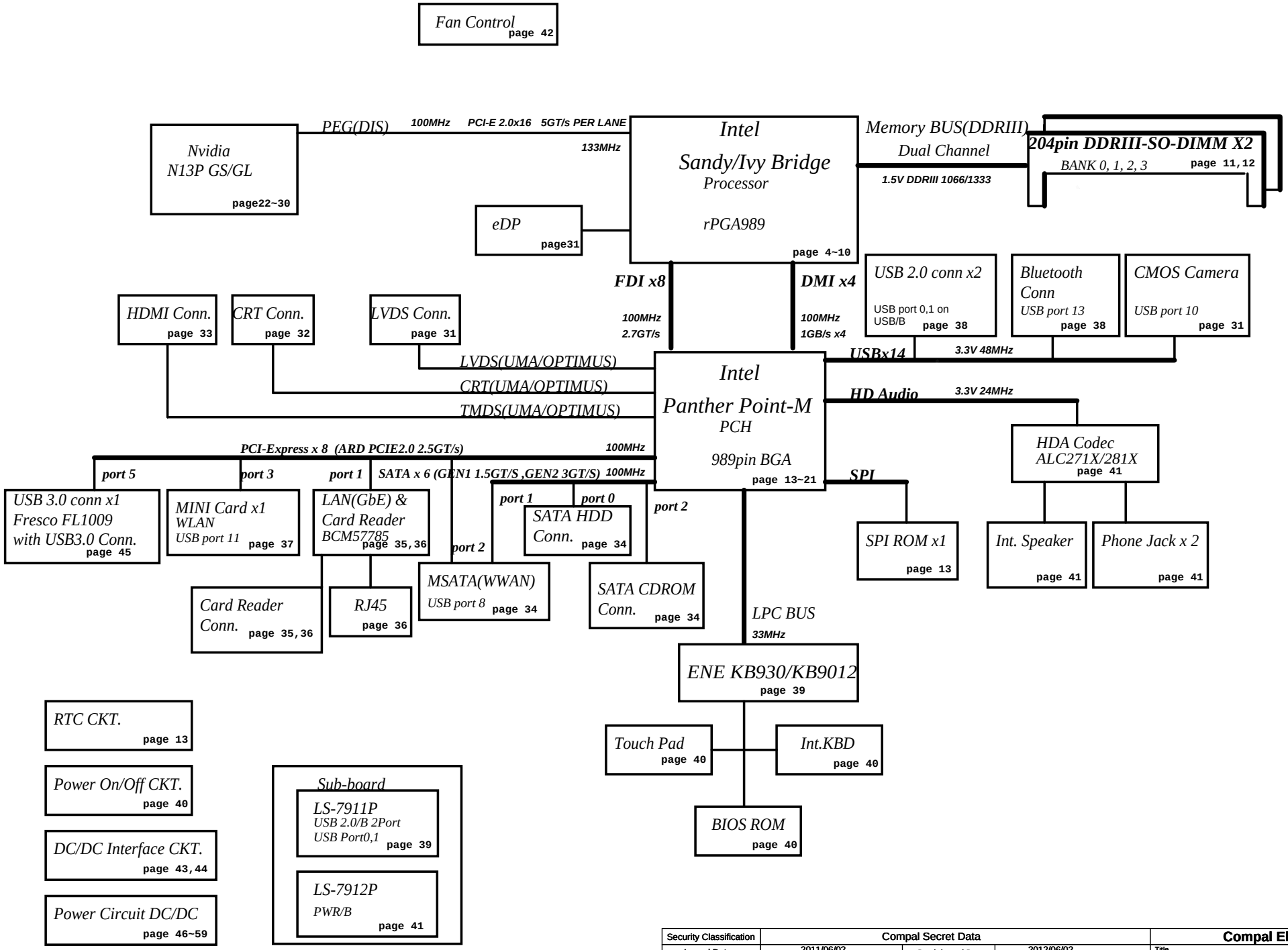

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+1.8VSDGPU	+1.8VS to +1.8VSDGPU switched power rail for GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BT & USB30 & USB20 Config

OPTMIUS SKU:DIS@ N13P-GL:GL@ N13P-GS:GS@ N13P-GF108_ES4:GF108@
BT SKU:BT@
internal USB SKU: PUSB@ DIS USB30 SKU:DUSB@
eDP SKU: EDP@
LVDS SKU: LVDS@
EC 930 SKU: 930@ EC 9012 SKU: 9012@
PCH HM65: HM65@ PCH HM76: HM76@
Win8: WIN8@

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	0.1
4	0.2
5	0.3
6	0.4
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
Dis with OPTIMUS	DIS@
Blue Tooth	BT@
Internal USB 3.0	PUSB@
eDP	eDP@
VRAM	X76@
Connector	CONN@
Unpop	@
N13P-GS	GS@
N13P-GL	GL@
Win8	Win8@
Audio ALC271X	271X@
Audio ALC281X	281X@
PCH HM65	HM65@
PCH HM76	HM76@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB3.0 colay USB2.0 Conn
		1	USB/B (Right Side)
	UHCI1	2	USB/B (Right Side)
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card 1(WLAN)
		9	
	UHCI5	10	Camera
		11	BlueTooth
	UHCI6	12	
		13	

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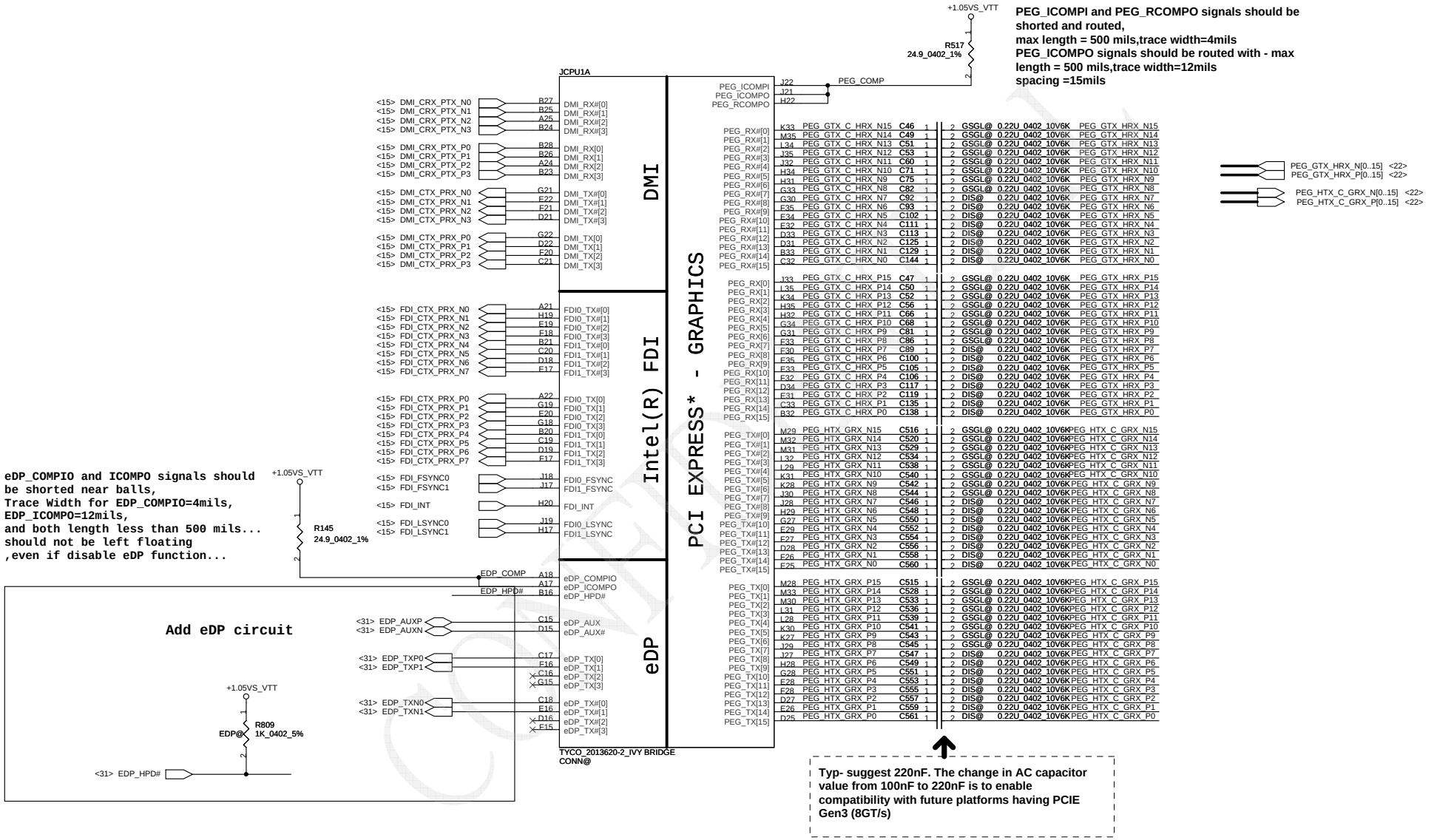

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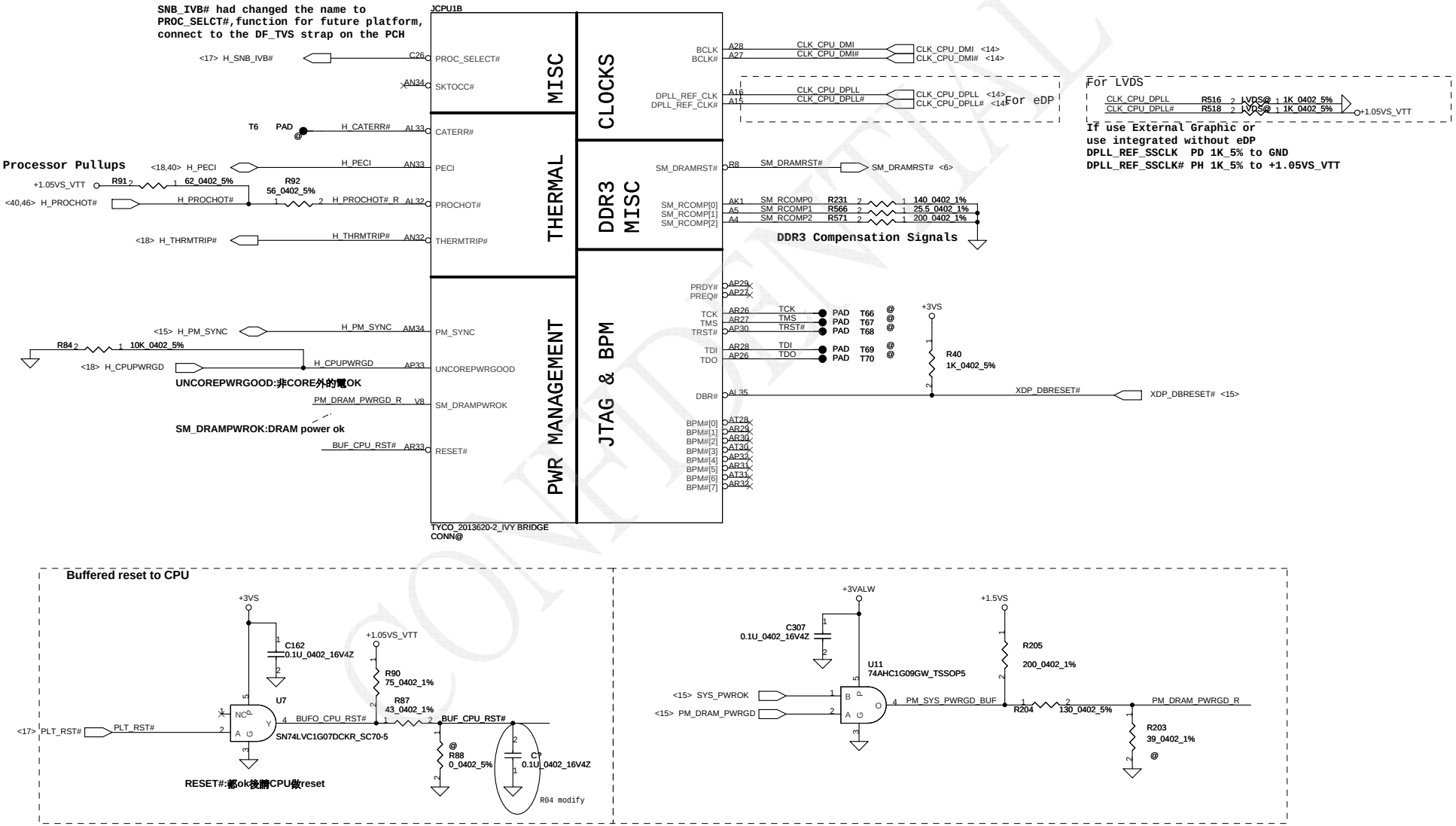

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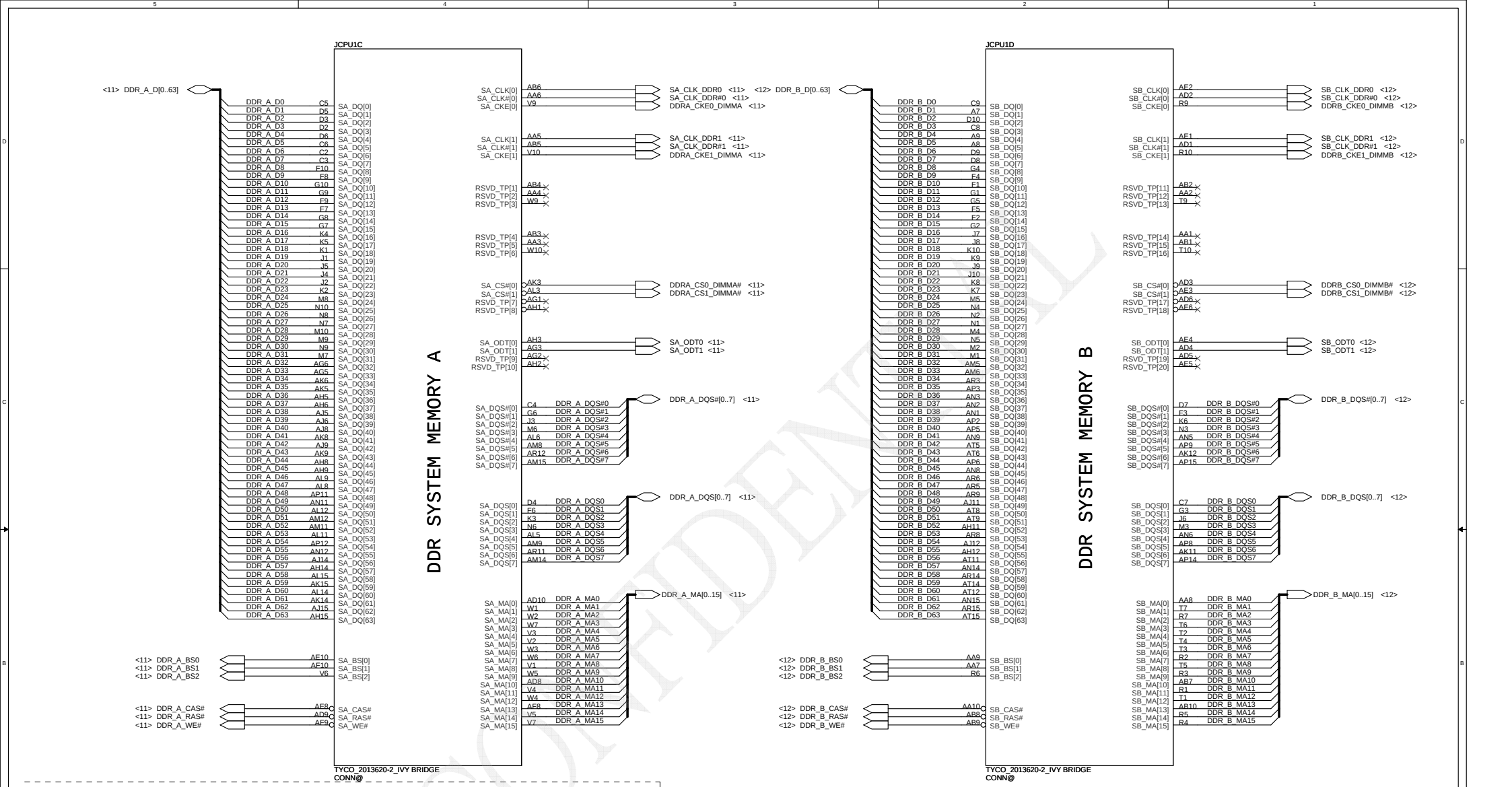

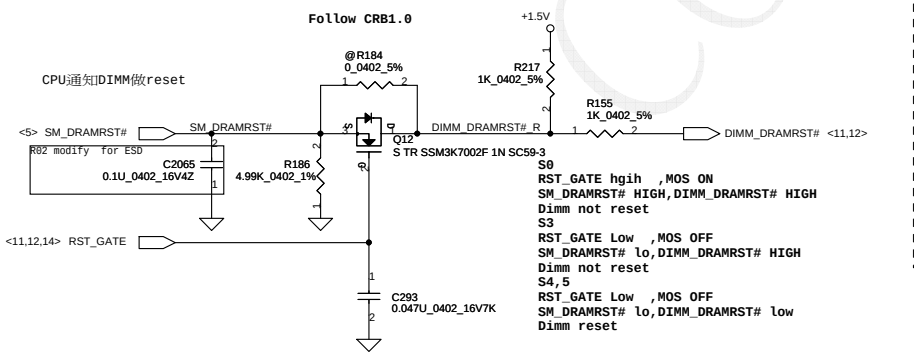

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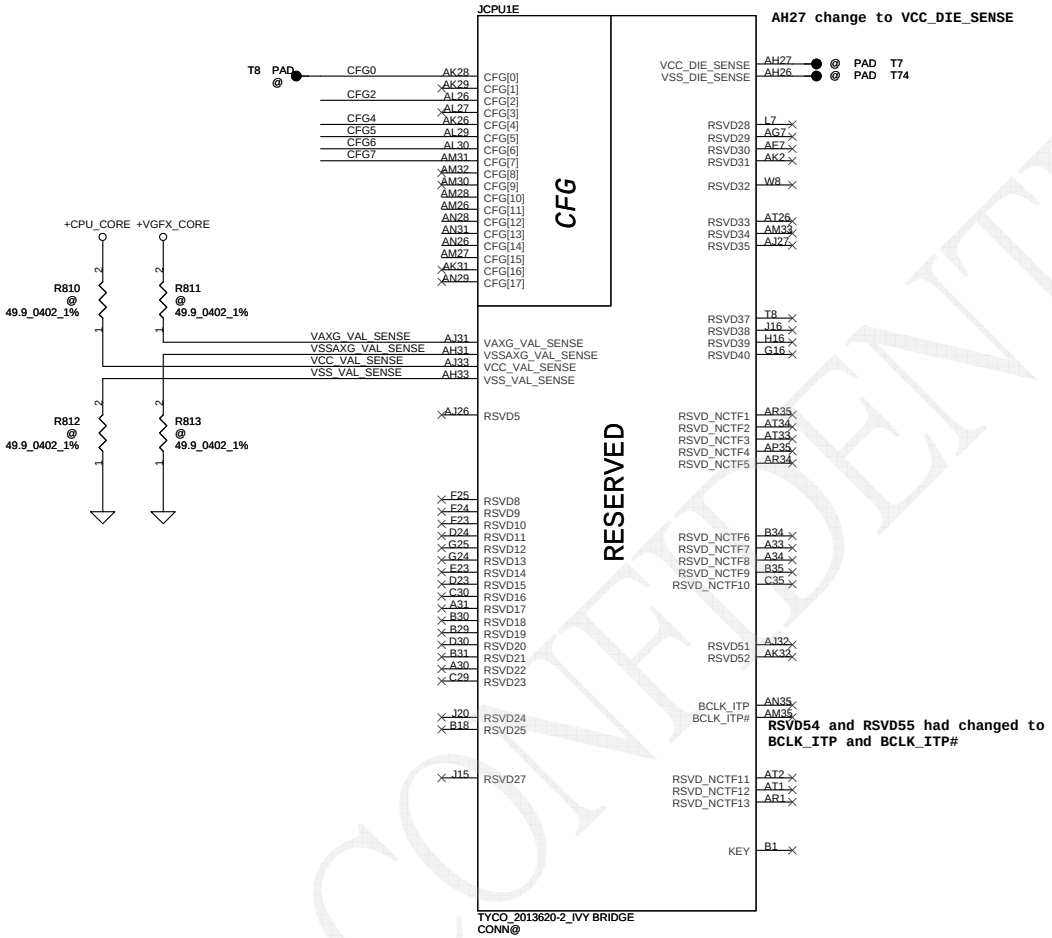
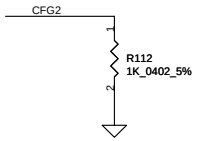
CFG Straps for Processor

AH26	Sandy	Ivy
	GND	VSS_DIE_SENSE

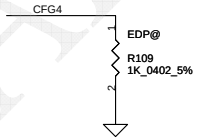


AH27 change to VCC_DIE_SENSE

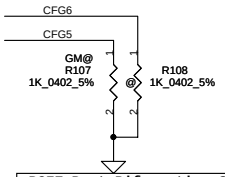
RSVD54 and RSVD55 had changed to BCLK_ITP and BCLK_ITP#



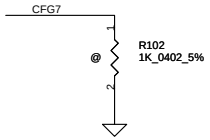
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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POWER

SV type CPU

QC 53A
DC 53A

JCPU1F

+CPU_CORE

CORE SUPPLY

AG35	VCC1	AE31	VCC15
AG34	VCC2	AE30	VCC16
AG33	VCC3	AE29	VCC17
AG32	VCC4	AE28	VCC18
AG31	VCC5	AE27	VCC19
AG30	VCC6	AE26	VCC20
AG29	VCC7	AD35	VCC21
AG28	VCC8	AD34	VCC22
AG27	VCC9	AD33	VCC23
AG26	VCC10	AD32	VCC24
AF35	VCC11	AD31	VCC25
AF34	VCC12	AD30	VCC26
AF33	VCC13	AD29	VCC27
AF32	VCC14	AD28	VCC28
AD27	VCC29	AC31	VCC35
AD26	VCC30	AC30	VCC36
AC35	VCC31	AC29	VCC37
AC34	VCC32	AC28	VCC38
AC33	VCC33	AC27	VCC39
AC32	VCC34	AC26	VCC40
AA35	VCC41	AA34	VCC42
AA33	VCC43	AA32	VCC44
AA31	VCC45	AA30	VCC46
AA29	VCC47	AA28	VCC48
AA27	VCC49	AA26	VCC50
Y35	VCC51	Y34	VCC52
Y33	VCC53	Y32	VCC54
Y31	VCC55	Y30	VCC56
Y29	VCC57	Y28	VCC58
Y27	VCC59	Y26	VCC60
V35	VCC61	V34	VCC62
V33	VCC63	V32	VCC64
V31	VCC65	V30	VCC66
V29	VCC67	V28	VCC68
V27	VCC69	V26	VCC70
U35	VCC71	U34	VCC72
U33	VCC73	U32	VCC74
U31	VCC75	U30	VCC76
U29	VCC77	U28	VCC78
U27	VCC79	U26	VCC80
R35	VCC81	R34	VCC82
R33	VCC83	R32	VCC84
R31	VCC85	R30	VCC86
R29	VCC87	R28	VCC88
R27	VCC89	R26	VCC90
P35	VCC91	P34	VCC92
P33	VCC93	P32	VCC94
P31	VCC95	P30	VCC96
P29	VCC97	P28	VCC98
P27	VCC99	P26	VCC100

PEG AND DDR

8.5A

+1.05VS_VTT

VCCIO1	AH13	VCCIO21	F12
VCCIO2	AH10	VCCIO22	F11
VCCIO3	AG10	VCCIO23	E14
VCCIO4	AC10	VCCIO24	E12
VCCIO5	Y10	VCCIO25	E11
VCCIO6	U10	VCCIO26	D14
VCCIO7	P10	VCCIO27	D13
VCCIO8	L10	VCCIO28	D12
VCCIO9	J14	VCCIO29	D11
VCCIO10	J13	VCCIO30	C14
VCCIO11	J12	VCCIO31	C13
VCCIO12	J11	VCCIO32	C12
VCCIO13	H14	VCCIO33	C11
VCCIO14	H12	VCCIO34	B14
VCCIO15	H11	VCCIO35	B12
VCCIO16	G14	VCCIO36	A14
VCCIO17	G13	VCCIO37	A13
VCCIO18	G12	VCCIO38	A12
VCCIO19	F14	VCCIO39	A11
VCCIO20	F13	VCCIO40	J23

SVID

+1.05VS_VTT

R450 130_0402_1%

+1.05VS_VTT

R447 75_0402_5%

R448 43_0402_1%

VIDALERT#	AJ29	H_CPU_SVIDALRT#			VR_SVID_ALRT# <52>
VIDSCLK	AJ30	H_CPU_SVIDCLK	R446	0_0402_5%	VR_SVID_CLK <52>
VIDSOUT	AJ28	H_CPU_SVIDDAT	R449	0_0402_5%	VR_SVID_DAT <52>

Place the PU resistors close to CPU

SENSE LINES

+CPU_CORE

R445 100_0402_1%

VCC_SENSE	AJ35	VCCSENSE_R	R444	0_0402_5%	VCCSENSE <52>
VSS_SENSE	AJ34	VSSSENSE_R	R443	0_0402_5%	VSSSENSE <52>

R442 100_0402_1%

R910 10_0402_5% +1.05VS_VTT

VCCIO_SENSE	B10	VCCIO_SENSE	VCCIO_SENSE <50>
VSS_SENSE_VCCIO	A10	VSSIO_SENSE	VSSIO_SENSE <50>

VSSIO_SENSE change to VSS_SENSE_VCCIO

R163 10_0402_5%

Should change to connect form power cirucit & layout differential with VCCIO_SENSE.

TYCO_2013620-2_IVY BRIDGE CONN@

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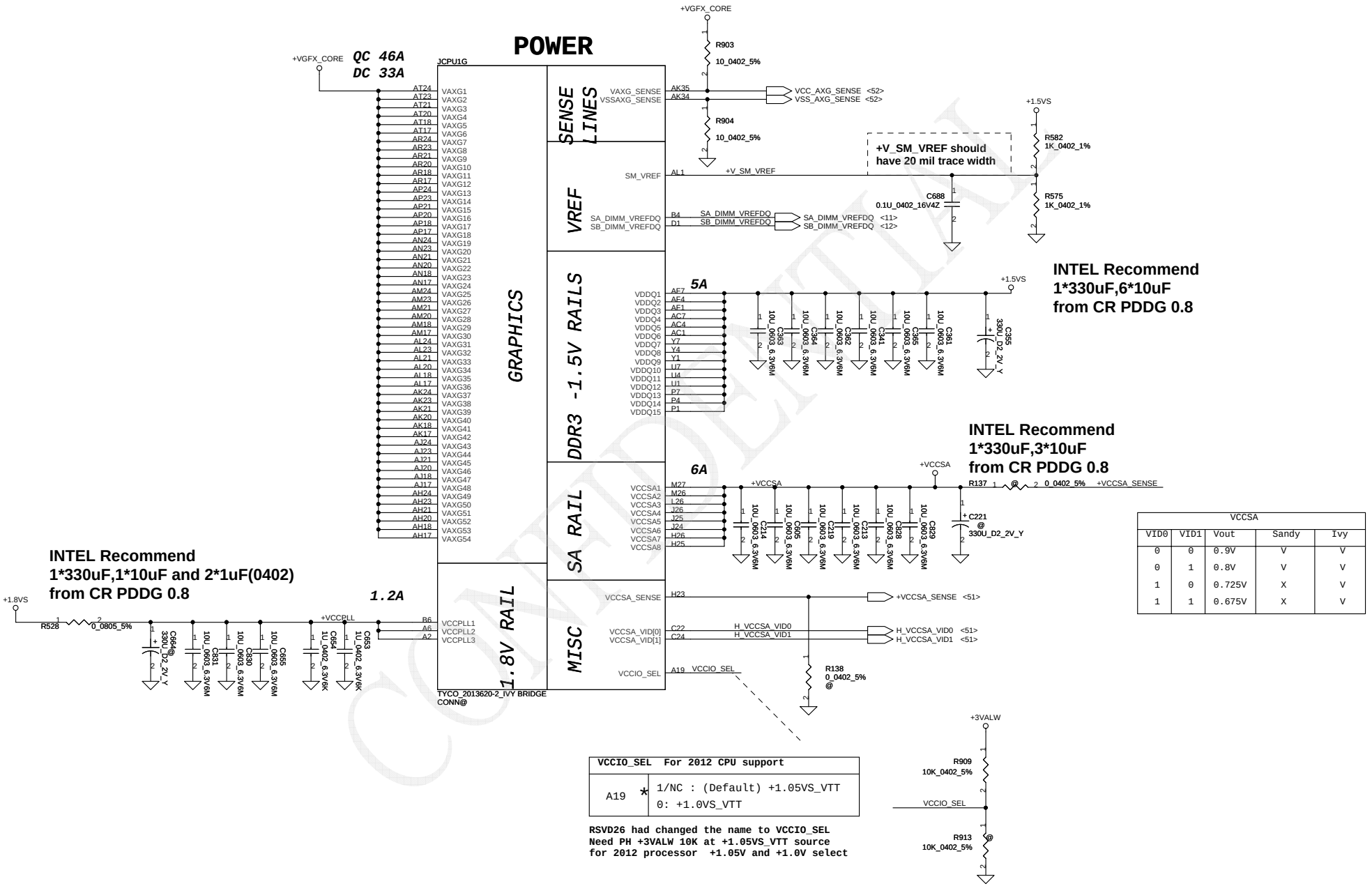

VCCSA				
VID0	VID1	Vout	Sandy	Ivy
0	0	0.9V	V	V
0	1	0.8V	V	V
1	0	0.725V	X	V
1	1	0.675V	X	V

VCCIO_SEL For 2012 CPU support		
A19	*	1/NC : (Default) +1.05VS_VTT 0: +1.0VS_VTT

RSVD26 had changed the name to VCCIO_SEL
Need PH +3VALW 10K at +1.05VS_VTT source
for 2012 processor +1.05V and +1.0V select

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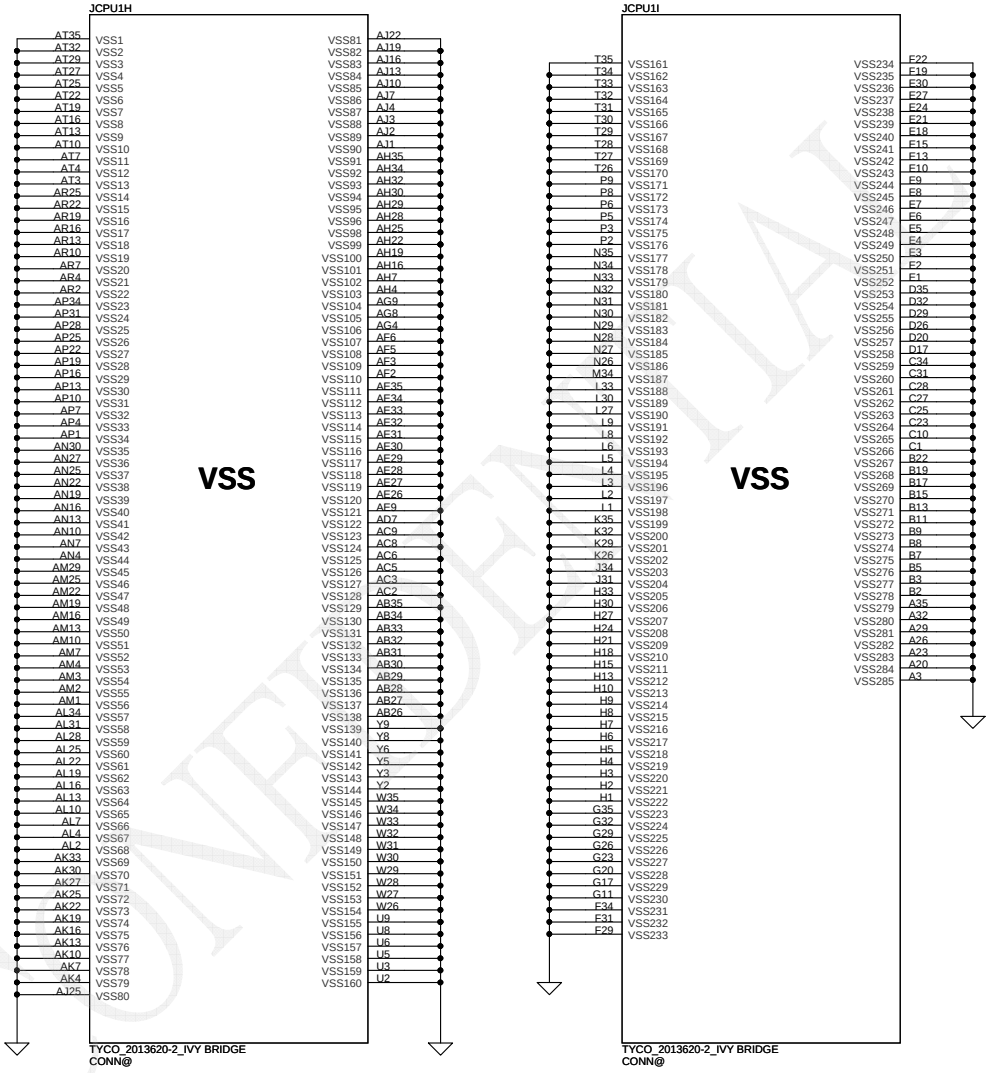

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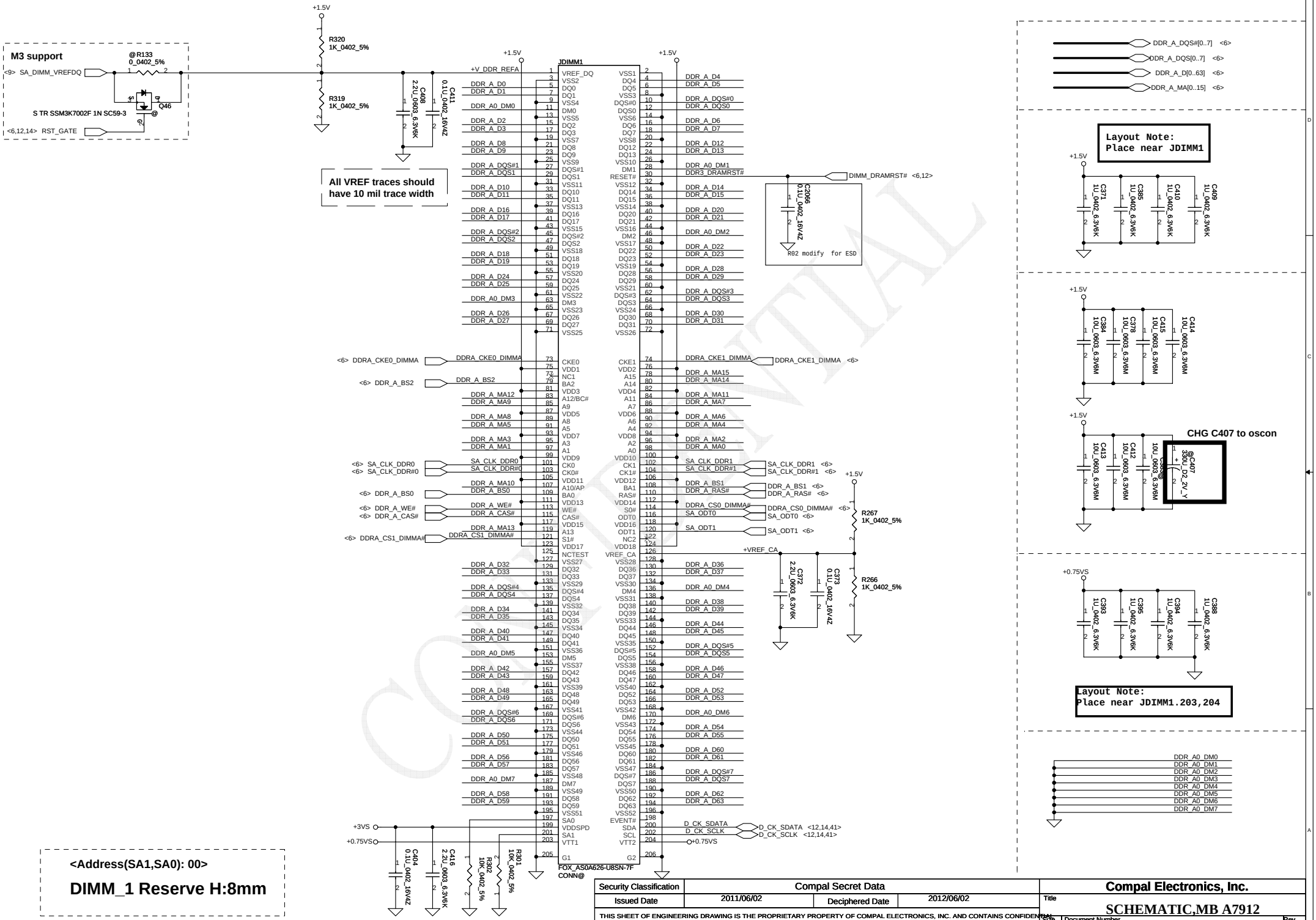

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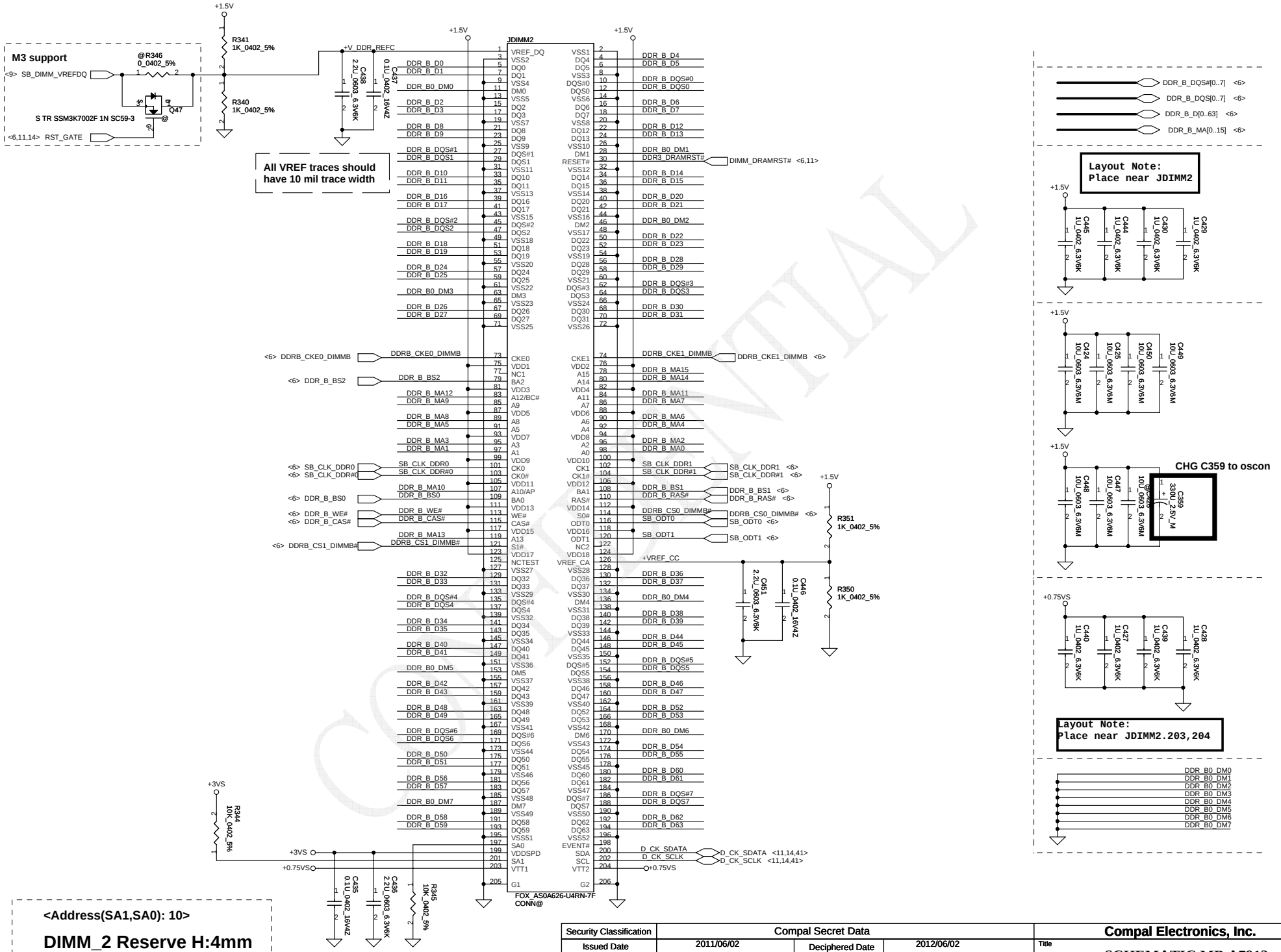

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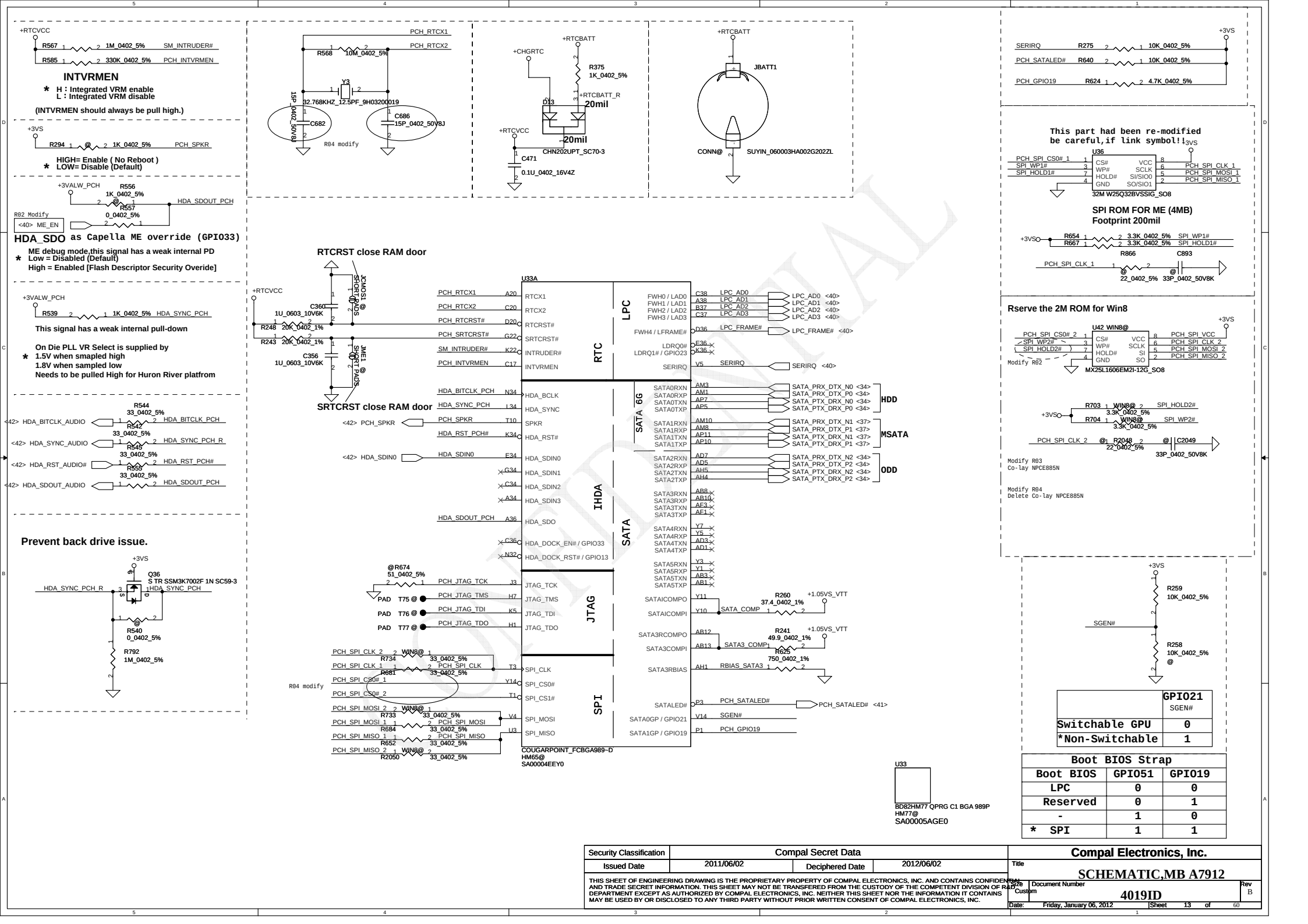

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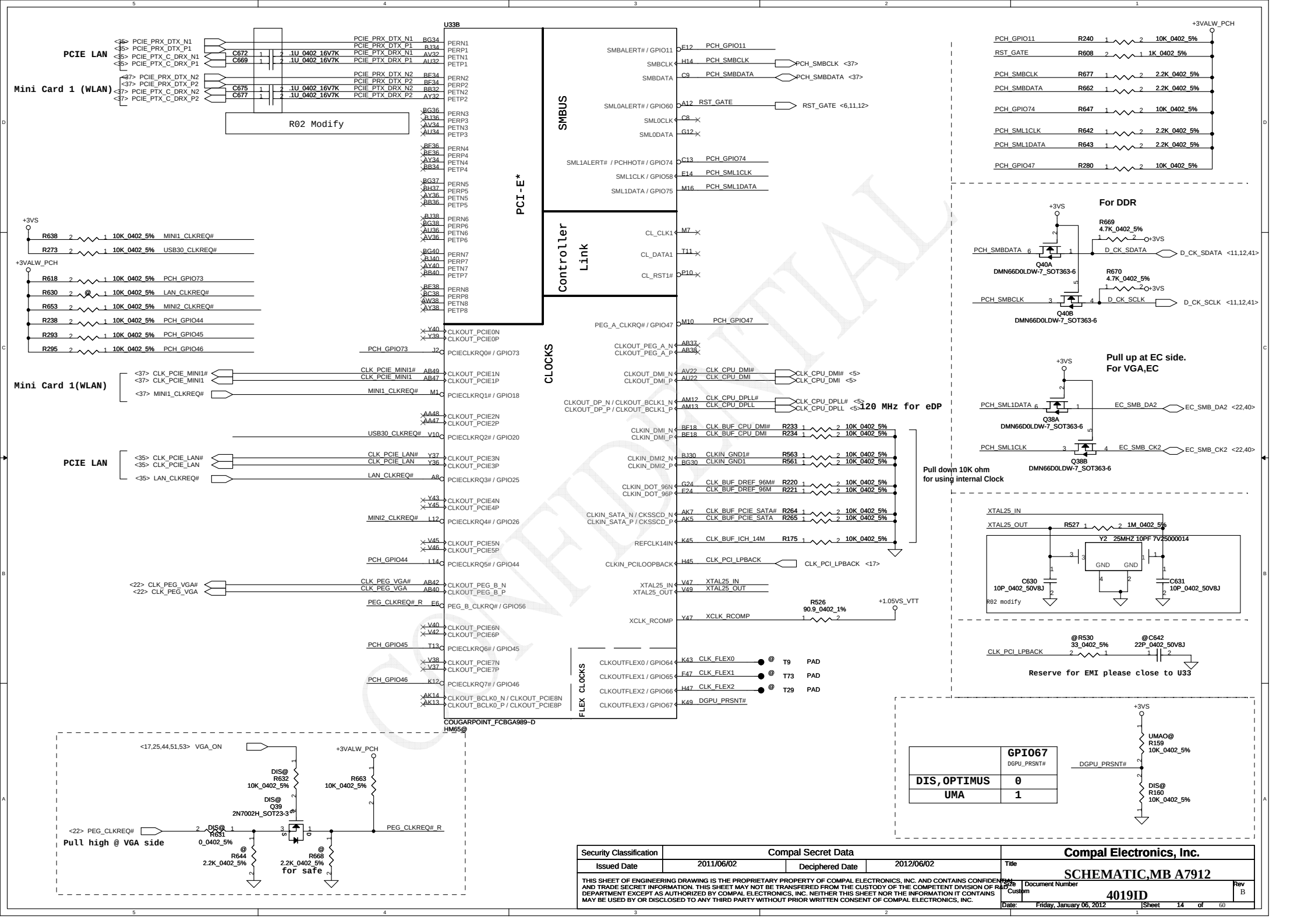
U33B
PCIE LAN
Mini Card 1 (WLAN)
R02 Modify
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
PCIE_PRX_DTX_N1
PCIE_PRX_DTX_P1
PCIE_PTX_C_DRX_N1
PCIE_PTX_C_DRX_P1
PCIE_PRX_DTX_N2
PCIE_PRX_DTX_P2
PCIE_PTX_C_DRX_N2
PCIE_PTX_C_DRX_P2
C672 .1U_0402_16V7K
C669 .1U_0402_16V7K
C675 .1U_0402_16V7K
C677 .1U_0402_16V7K
PCIE_PTX_DRX_N1
PCIE_PTX_DRX_P1
PCIE_PTX_DRX_N2
PCIE_PTX_DRX_P2
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PERP1
PETN1
PETP1
PERN2
PERP2
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PERP6
PETN6
PETP6
PERN7
PERP7
PETN7
PETP7
PERN8
PERP8
PETN8
PETP8
SMBALERT# / GPIO11
SMBCLK
SMBDATA
SML0ALERT# / GPIO60
SML0CLK
SML0DATA
SML1ALERT# / PCHHOT# / GPIO74
SML1CLK / GPIO58
SML1DATA / GPIO75
PCH_GPIO11
PCH_SMBCLK
PCH_SMBDATA
RST_GATE
PCH_GPIO74
PCH_SML1CLK
PCH_SML1DATA
PCH_SMBCLK <37>
PCH_SMBDATA <37>
RST_GATE <6,11,12>
RST_GATE <6,11,12>
CL_CLK1
CL_DATA1
CL_RST1#
PEG_A_CLKRQ# / GPIO47
PCH_GPIO47
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N / CLKOUT_BCLK1_N
CLKOUT_DP_P / CLKOUT_BCLK1_P
CLK_CPU_DMI#
CLK_CPU_DMI
CLK_CPU_DPLL#
CLK_CPU_DPLL
CLK_CPU_DMI# <5>
CLK_CPU_DMI <5>
CLK_CPU_DPLL# <5>
CLK_CPU_DPLL <5>
120 MHz for eDP
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_DMI2_N
CLKIN_DMI2_P
CLKIN_DOT_96N
CLKIN_DOT_96P
CLKIN_SATA_N / CKSSCD_N
CLKIN_SATA_P / CKSSCD_P
REFCLK14IN
CLKIN_PCILOOPBACK
CLK_BUF_CPU_DMI#
CLK_BUF_CPU_DMI
CLK_BUF_DREF_96M#
CLK_BUF_DREF_96M
CLK_BUF_PCIE_SATA#
CLK_BUF_PCIE_SATA
CLK_BUF_ICH_14M
CLK_PCI_LPBACK
CLK_PCI_LPBACK <17>
CLKIN_GND1#
CLKIN_GND1
10K_0402_5%
Pull down 10K ohm for using internal Clock
XTAL25_IN
XTAL25_OUT
XCLK_RCOMP
R526 90.9_0402_1%
+1.05VS_VTT
CLKOUTFLEX0 / GPIO64
CLKOUTFLEX1 / GPIO65
CLKOUTFLEX2 / GPIO66
CLKOUTFLEX3 / GPIO67
CLK_FLEX0
CLK_FLEX1
CLK_FLEX2
DGPU_PRSNT#
T9 PAD
T73 PAD
T29 PAD
COUGARPOINT_FCBGA989~D
HM65@
+3VALW_PCH
PCH_GPIO11 R240 10K_0402_5%
RST_GATE R608 1K_0402_5%
PCH_SMBCLK R677 2.2K_0402_5%
PCH_SMBDATA R662 2.2K_0402_5%
PCH_GPIO74 R647 10K_0402_5%
PCH_SML1CLK R642 2.2K_0402_5%
PCH_SML1DATA R643 2.2K_0402_5%
PCH_GPIO47 R280 10K_0402_5%
For DDR
+3VS
R669 4.7K_0402_5%
R670 4.7K_0402_5%
Q40A DMN66D0LDW-7_SOT363-6
Q40B DMN66D0LDW-7_SOT363-6
D_CK_SDATA <11,12,41>
D_CK_SCLK <11,12,41>
Pull up at EC side.
For VGA,EC
Q38A DMN66D0LDW-7_SOT363-6
Q38B DMN66D0LDW-7_SOT363-6
EC_SMB_DA2 <22,40>
EC_SMB_CK2 <22,40>
XTAL25_IN
XTAL25_OUT
R527 1M_0402_5%
Y2 25MHZ 10PF 7V25000014
C630 10P_0402_50V8J
C631 10P_0402_50V8J
R02 modify
@R530 33_0402_5%
@C642 22P_0402_50V8J
CLK_PCI_LPBACK
Reserve for EMI please close to U33
+3VS
R638 10K_0402_5% MINI1_CLKREQ#
R273 10K_0402_5% USB30_CLKREQ#
+3VALW_PCH
R618 10K_0402_5% PCH_GPIO73
R630 @ 10K_0402_5% LAN_CLKREQ#
R653 10K_0402_5% MINI2_CLKREQ#
R238 10K_0402_5% PCH_GPIO44
R293 10K_0402_5% PCH_GPIO45
R295 10K_0402_5% PCH_GPIO46
Mini Card 1(WLAN)
PCIE LAN
CLK_PCIE_MINI1#
CLK_PCIE_MINI1
MINI1_CLKREQ#
CLK_PCIE_LAN#
CLK_PCIE_LAN
LAN_CLKREQ#
USB30_CLKREQ#
MINI2_CLKREQ#
PCH_GPIO73
PCH_GPIO44
PCH_GPIO45
PCH_GPIO46
CLKOUT_PCIE0N
CLKOUT_PCIE0P
CLKOUT_PCIE1N
CLKOUT_PCIE1P
CLKOUT_PCIE2N
CLKOUT_PCIE2P
CLKOUT_PCIE3N
CLKOUT_PCIE3P
CLKOUT_PCIE4N
CLKOUT_PCIE4P
CLKOUT_PCIE5N
CLKOUT_PCIE5P
CLKOUT_PCIE6N
CLKOUT_PCIE6P
CLKOUT_PCIE7N
CLKOUT_PCIE7P
CLKOUT_BCLK0_N / CLKOUT_PCIE8N
CLKOUT_BCLK0_P / CLKOUT_PCIE8P
PCIECLKRQ0# / GPIO73
PCIECLKRQ1# / GPIO18
PCIECLKRQ2# / GPIO20
PCIECLKRQ3# / GPIO25
PCIECLKRQ4# / GPIO26
PCIECLKRQ5# / GPIO44
PEG_B_CLKRQ# / GPIO56
PCIECLKRQ6# / GPIO45
PCIECLKRQ7# / GPIO46
<22> CLK_PEG_VGA#
<22> CLK_PEG_VGA
CLK_PEG_VGA#
CLK_PEG_VGA
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PEG_CLKREQ# R
<17,25,44,51,53> VGA_ON
DIS@ R632 10K_0402_5%
R663 10K_0402_5%
DIS@ Q39 2N7002H_SOT23-3
<22> PEG_CLKREQ#
Pull high @ VGA side
DIS@ R631 0_0402_5%
@ R644 2.2K_0402_5%
@ R668 2.2K_0402_5%
for safe
PEG_CLKREQ# R
GPIO67
DGPU_PRSNT#
DIS,OPTIMUS 0
UMA 1
UMAO@ R159 10K_0402_5%
DIS@ R160 10K_0402_5%
Compal Secret Data
Issued Date 2011/06/02
Deciphered Date 2012/06/02
Compal Electronics, Inc.
SCHEMATIC,MB A7912
Size Custom
Document Number 4019ID
Rev B
Date: Friday, January 06, 2012
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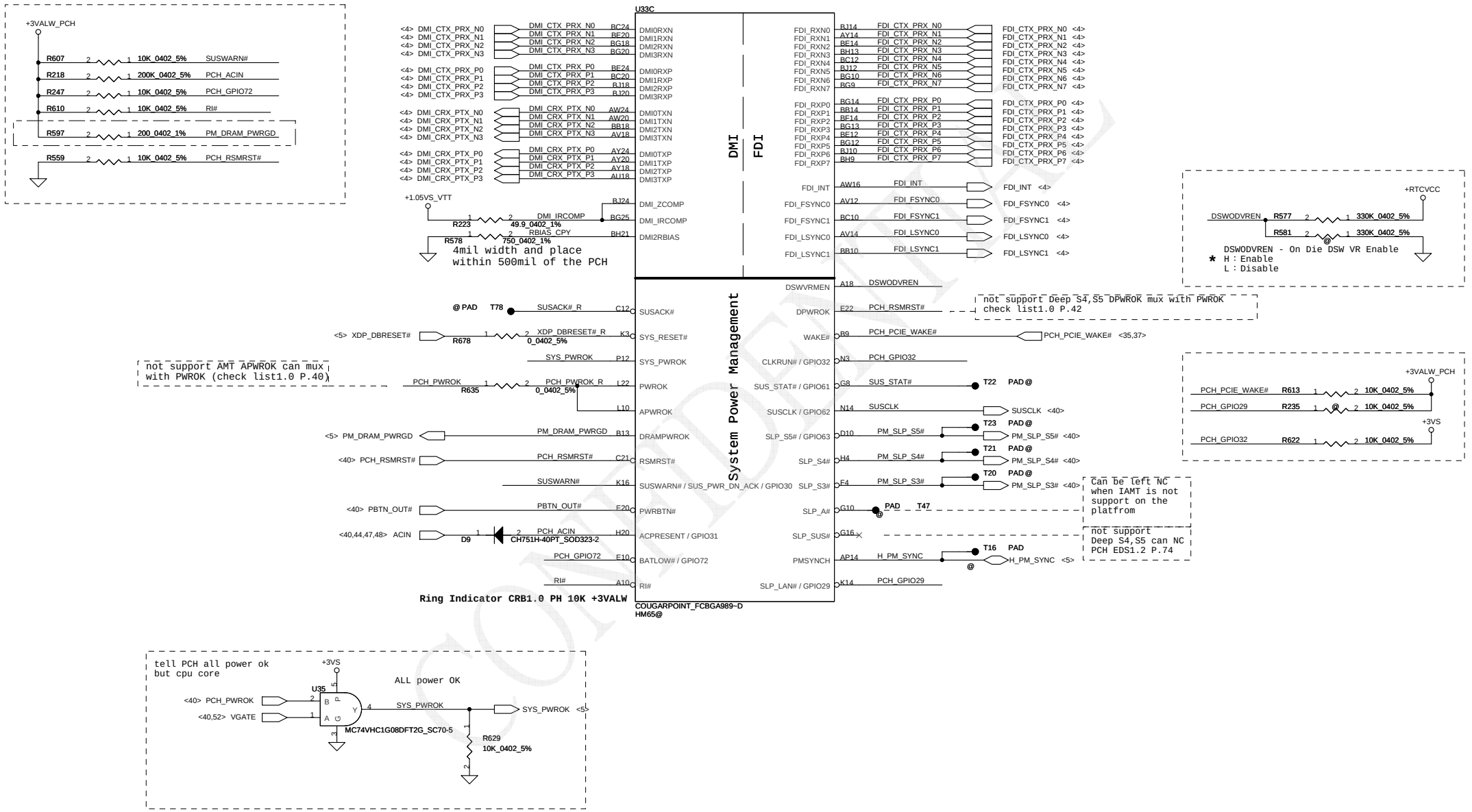

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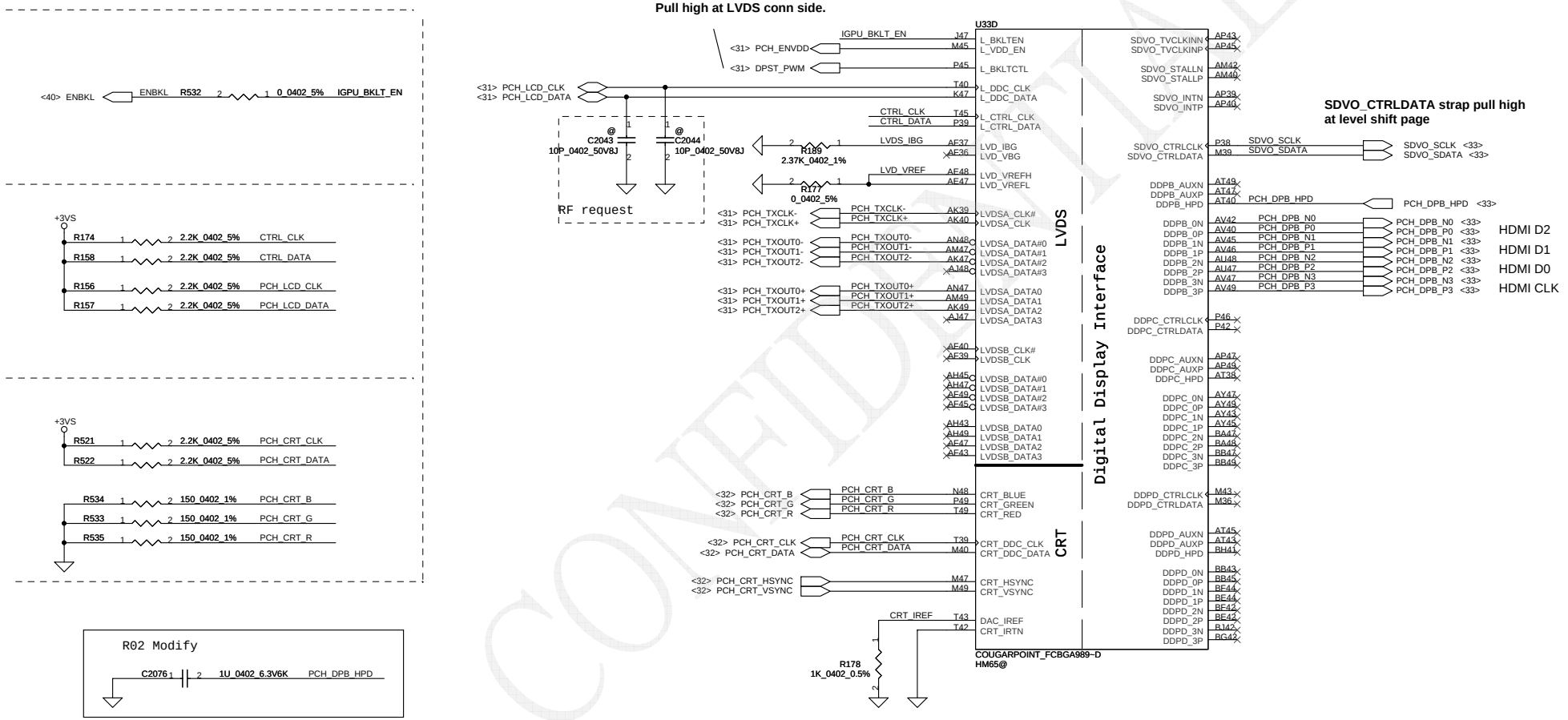

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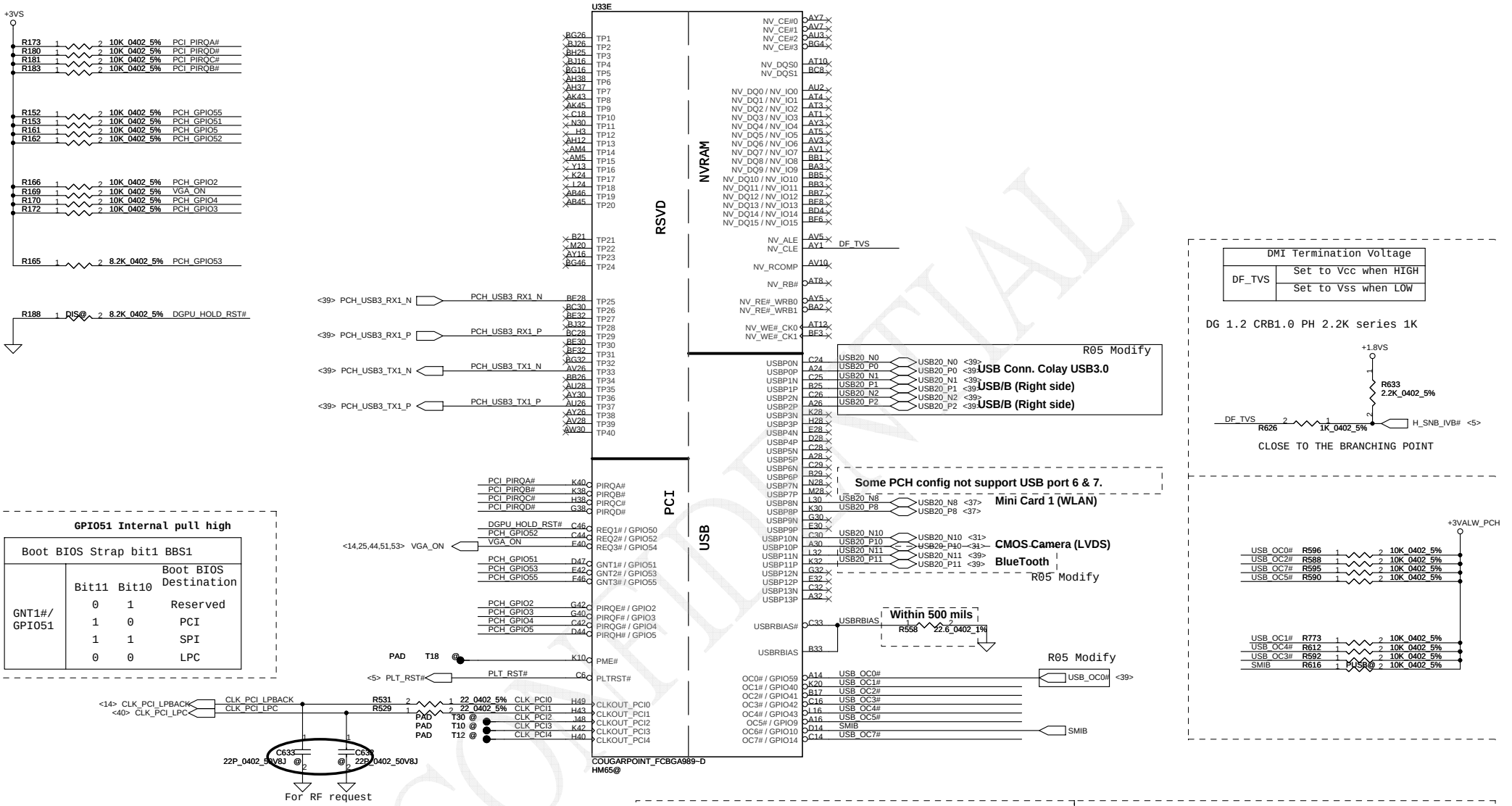

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HDA_SYNC PH(PLL =+1.5VS)

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

* H : On-Die voltage regulator enable
  L : On-Die PLL Voltage Regulator disable

+3VALW_PCH
R768 4.7K_0402_5%
R272 1K_0402_5%
PCH_GPIO28

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70

R661 10K_0402_5% PCH_GPIO27

+3VS
R623 @ 10K_0402_5% OPTIMUS_EN#
R639 DIS@ 10K_0402_5%

	GPIO38 OPTIMUS_EN#
* OPTIMUS	0
DIS Only	1

+3VS
R277 @ 200K_0402_5% WWAN_OFF#
R276 10K_0402_5% PCH_GPIO0
R546 10K_0402_5% WL_EN#
R191 10K_0402_5% PCH_GPIO6
R641 10K_0402_5% MSATA_DET#
R290 10K_0402_5% PCH_GPIO22
R649 10K_0402_5% PCH_GPIO39
R291 @ 200K_0402_5% PCH_GPIO36
R619 10K_0402_5% BT_ON#
R292 10K_0402_5% PCH_GPIO48
R274 10K_0402_5% WL_OFF#

+3VALW_PCH
R262 10K_0402_5% PCH_GPIO24
R620 10K_0402_5% PCH_GPIO12
R672 1K_0402_5% EC_LID_OUT#
R263 10K_0402_5% PCH_GPIO57

R911 10K_0402_5% PCH_GPIO36
R912 10K_0402_5% WWAN_OFF#

+3VS
R2053 10K_0402_5%
DGPU_PWROK
+3VSDGPU
DIS@ R2055 10K_0402_5%
DIS@ R2054 10K_0402_5%
Q2001A DIS@ DMN66D0LDW-7_SOT363-6
DIS@ Q2001B DMN66D0LDW-7_SOT363-6
DIS@ C2050 0.1U_0402_16V4Z
DIS@ C2051 1U_0402_6.3V6K

GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.

CRB1.0 PH10K to +3VALW

GPIO36/GPIO37 is Strap functionality
that requires internal pull down to be sampled at rising PWROK.
When uses as SATA2GP/SATA3GP for mechanical presence detect
-use a external pull up 150K-200K ohm to Vcc3_3
When used as GP input
-ensure GPI is not driven high during strap sampling window
When Unused as GPIO or SATA*GP
-use 8.2K-10K pull-down
check list page 47

U33F

PCH_GPIO0	T7	BMBUSY# / GPIO0		TACH4 / GPIO68	C40 PCH_GPIO68
<39> WL_EN#	A42	TACH1 / GPIO1		TACH5 / GPIO69	B41 PCH_GPIO69
PCH_GPIO6	H36	TACH2 / GPIO6		TACH6 / GPIO70	C41 PCH_GPIO70
<40> EC_SCI#	E38	TACH3 / GPIO7		TACH7 / GPIO71	A40 PCH_GPIO71 <31>
<40> EC_SMI#	C10	GPIO8			
PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12			
<40> EC_LID_OUT#	G2	GPIO15		A20GATE	P4 GATEA20 <40>
<37> MSATA_DET#	U2	SATA4GP / GPIO16		PECI	AU16 PCH_PECI_R 0_0402_5%@R239 H_PECI <5,40>
				RCIN#	P5 EC_KBRST# EC_KBRST# <40>
DGPU_PWROK	D40	TACH0 / GPIO17		PROCPWRGD	AY11 H_CPUPWRGD <5>
PCH_GPIO22	T5	SCLOCK / GPIO22		THRMTRIP#	AY10 PCH_THRMTRIP#_R R627 390_0402_5% H_THRMTRIP# H_THRMTRIP# <5>
PCH_GPIO24	E8	GPIO24 / MEM_LED		INIT3_3V#	T14
PCH_GPIO27	E16	GPIO27			
PCH_GPIO28	P8	GPIO28			
<37,39> BT_ON#	K1	STP_PCI# / GPIO34		NC_1	AH8
	K4	GPIO35		NC_2	AK11
PCH_GPIO36	V8	SATA2GP / GPIO36		NC_3	AH10
WWAN_OFF#	M5	SATA3GP / GPIO37		NC_4	AK10
OPTIMUS_EN#	N2	SLOAD / GPIO38		NC_5	P37
PCH_GPIO39	M3	SDATAOUT0 / GPIO39			
PCH_GPIO48	V13	SDATAOUT1 / GPIO48			
<37> WL_OFF#	V3	SATA5GP / GPIO49			
PCH_GPIO57	D6	GPIO57			
	A4	VSS_NCTF_1		VSS_NCTF_15	BG2
	A44	VSS_NCTF_2		VSS_NCTF_16	BG48
	A45	VSS_NCTF_3		VSS_NCTF_17	BH3
	A46	VSS_NCTF_4		VSS_NCTF_18	BH47
	A5	VSS_NCTF_5		VSS_NCTF_19	BJ4
	A6	VSS_NCTF_6		VSS_NCTF_20	BJ44
	B3	VSS_NCTF_7		VSS_NCTF_21	BJ45
	B47	VSS_NCTF_8		VSS_NCTF_22	BJ46
	BD1	VSS_NCTF_9		VSS_NCTF_23	BJ5
	BD49	VSS_NCTF_10		VSS_NCTF_24	BJ6
	BE1	VSS_NCTF_11		VSS_NCTF_25	C2
	BE49	VSS_NCTF_12		VSS_NCTF_26	C48
	BF1	VSS_NCTF_13		VSS_NCTF_27	D1
	BF49	VSS_NCTF_14		VSS_NCTF_28	D49
				VSS_NCTF_29	E1
				VSS_NCTF_30	E49
				VSS_NCTF_31	F1
				VSS_NCTF_32	F49

GPIO | CPU/MISC | NCTF

COUGARPOINT_FCBGA989~D
HM65@

+3VS
R278 10K_0402_5%

PECI CPU-EC
CTRL-ALT-DEL
non CPU power ok
130 degree shut sown

INIT3_3V Checklist1.0 P.59
This signal has weak internal PU, can't pull low,leave NC

TS_VSS1~4
PD to GND

+3VS
PCH_GPIO68 R771 10K_0402_5%
EC_KBRST# R279 10K_0402_5%

+3VS
R554 10K_0402_5%
R548 10K_0402_5%
PCH_GPIO69
PCH_GPIO70
R553 10K_0402_5%
R549 10K_0402_5%

Project ID	GPIO69	GPIO70
Q5WE0	0	0
Q7YE0	0	0
*Q5Wxx-QC	1	0
x	1	1

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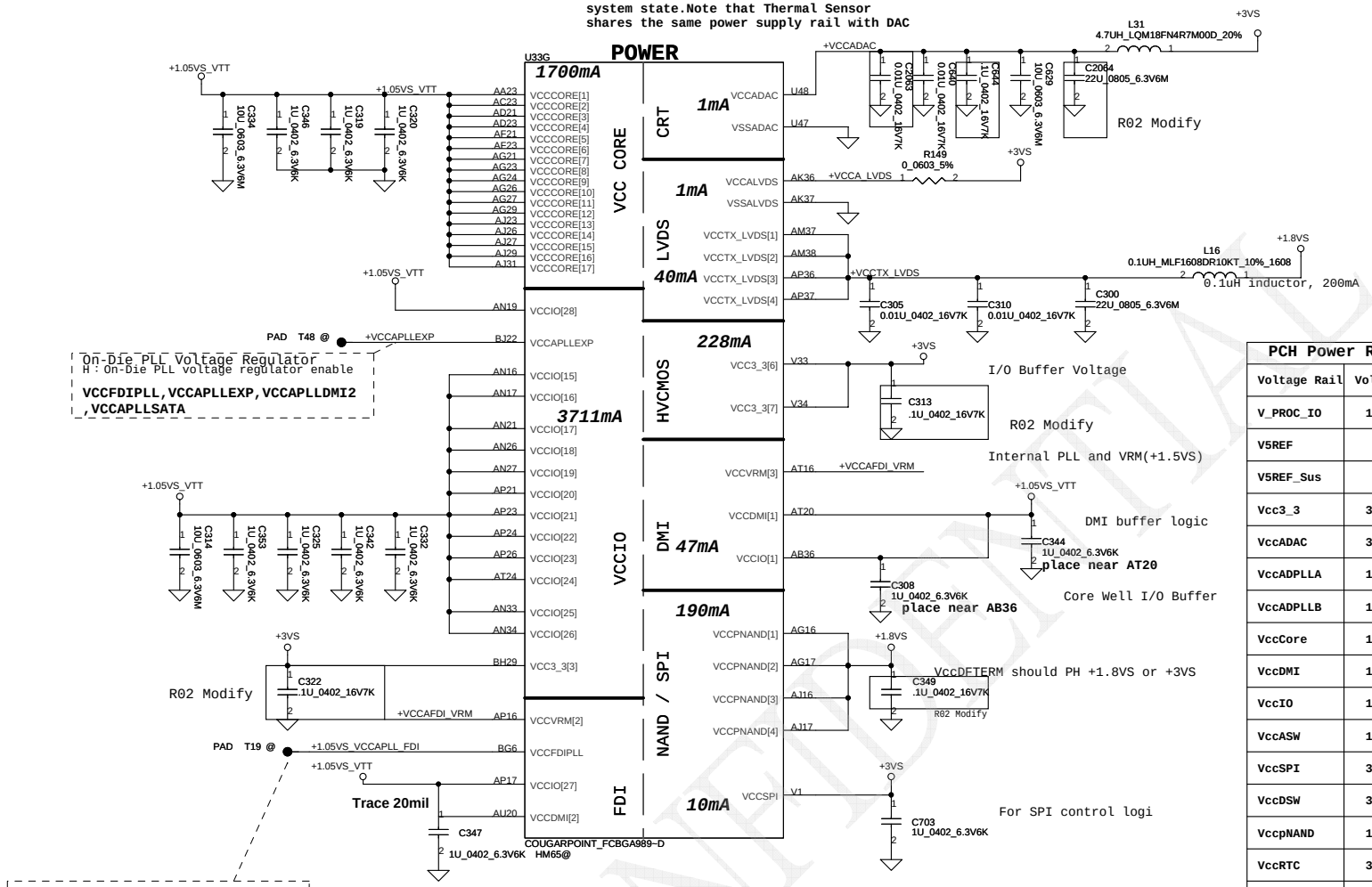

PCH Power Rail Table

Voltage Rail	Voltage	S0 Iccmax Current(A)	
V_PROC_IO	1.05	0.001	Processor I/F
V5REF	5	0.001	PCH Core Well Reference Voltage
V5REF_Sus	5	0.001	Suspend Well Reference Voltag
Vcc3_3	3.3	0.266	I/O Buffer Voltage
VccADAC	3.3	0.001	Display DAC Analog Power. This power is supplied by the core well.
VccADPLLA	1.05	0.08	Display PLL A power
VccADPLLB	1.05	0.08	Display PLL B power
VccCore	1.05	1.3	Internal Logic Voltage
VccDMI	1.05	0.042	DMI Buffer Voltage
VccIO	1.05	2.925	Core Well I/O buffers
VccASW	1.05	1.01	1.05 V Supply for Intel R Management Engine and Integrated LAN
VccSPI	3.3	0.02	3.3 V Supply for SPI Controller Logic
VccDSW	3.3	0.003	3.3v supply for Deep S4/S5 well
VccpNAND	1.8	0.19	1.8V power supply for DF_TVS
VccRTC	3.3	6 uA	Battery Voltage
VccSus3_3	3.3	0.266	Suspend Well I/O Buffer Voltage
VccSusHDA	3.3 / 1.5	0.01	High Definition Audio Controller Suspend Voltage
VccVRM	1.8 / 1.5	0.16	1.8 V Internal PLL and VRMs (1.8 V for Desktop)
VccCLKDMI	1.05	0.02	DMI Clock Buffer Voltage
VccSSC	1.05	0.095	Spread Modulators Power Supply
VccDIFFCLKN	1.05	0.055	Differential Clock Buffers Power Supply
VccALVDS	3.3	0.001	Analog power supply for LVDS (Mobile Only)
VccTX_LVDS	1.8	0.06	Analog power supply for LVDS (Mobile Only)

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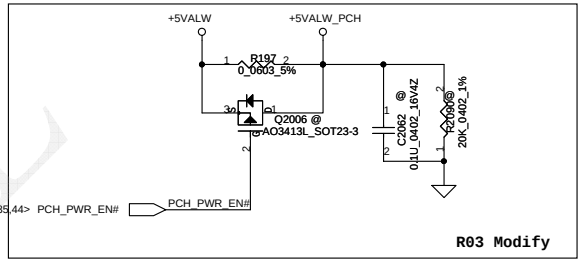
VCC3_3 = 266mA detal waiting for newest spec
VCCDMI = 42mA detal waiting for newest spec

+5VALW TO +5VALW_PCH(PCH AUX Power)



POWER

Have internal VRM

U33J

COUGARPOINT_FCBGA989-D
HM65@

Clock and Miscellaneous

- VCCACLK AD49
- VCCDSW3_3 T16 — 1mA
- DCPSUSBYP V12 — PAD T17 @ — +PCH_VCCDSW
- VCC3_3[5] T38 — +3VS_VCC_CLKF33
- VCCAPLLDMI2 BH23 — 95mA — PAD T11 @ — +VCCAPLL_CPY_PCH
- VCCIO[14] AL29 — +1.05VS_VTT
- DCPSUS[3] AL24 — PAD T13 @ — +VCCSUS1
- VCCASW[1] AA19 — 903mA
- VCCASW[2] AA21
- VCCASW[3] AA24
- VCCASW[4] AA26
- VCCASW[5] AA27
- VCCASW[6] AA29
- VCCASW[7] AA31
- VCCASW[8] AC26
- VCCASW[9] AC27
- VCCASW[10] AC29
- VCCASW[11] AC31
- VCCASW[12] AD29
- VCCASW[13] AD31
- VCCASW[14] W21
- VCCASW[15] W23
- VCCASW[16] W24
- VCCASW[17] W26
- VCCASW[18] W29
- VCCASW[19] W31
- VCCASW[20] W33

PCI/GPIO/LPC

- VCCIO[29] N26
- VCCIO[30] P26
- VCCIO[31] P28
- VCCIO[32] T27
- VCCIO[33] T29
- VCCSUS3_3[7] T23
- VCCSUS3_3[8] T24
- VCCSUS3_3[9] V23
- VCCSUS3_3[10] V24
- VCCSUS3_3[6] P24
- VCCIO[34] T26 — 1mA — V5REF_SUS M26 — +PCH_V5REF_SUS
- DCPSUS[4] AN23 — +VCCA_USBSUS — @ T14 PAD
- VCCSUS3_3[1] AN24 — +3VALW_PCH
- V5REF P34 — 1mA — +PCH_V5REF_RUN
- VCCSUS3_3[2] N20 — +3V_VCCPSUS
- VCCSUS3_3[3] N22
- VCCSUS3_3[4] P20
- VCCSUS3_3[5] P22
- VCC3_3[1] AA16
- VCC3_3[8] W16
- VCC3_3[4] T34

SATA

- VCC3_3[2] AJ2
- VCCIO[5] AF13
- VCCIO[12] AH13
- VCCIO[13] AH14
- VCCIO[6] AF14
- VCCAPLLSATA AK1 — +VCCSATAPLL — @ T62 PAD
- VCCVRM[1] AF11 — +VCCAFDI_VRM
- VCCADPLLA BD47 — 80mA — +1.05VS_VCCA_A_DPL
- VCCADPLLB BF47 — 80mA — +1.05VS_VCCA_B_DPL
- VCCVRM[4] Y49 — +VCCAFDI_VRM
- DCPRTC N16 — +VCCRTCEXT

USB

- VCCIO[7] AF17
- VCCIO[8] AF33
- VCCIO[9] AF34
- VCCIO[11] AG34 — 55mA
- VCCIO[10] AG33
- VCCIO[2] AC16
- VCCIO[3] AC17
- VCCIO[4] AD17
- DCPSST V16 — 130mA — C354 +VCCSST .1U_0402_16V7K R02 Modify

MISC

- VCCASW[22] T21
- VCCASW[23] V21
- VCCASW[21] T19
- DCPSUS[1] T17 — PAD T15 @ — +1.05VM_VCCSUS
- DCPSUS[2] V19

CPU

- V_PROC_IO BJ8 — 1mA

RTC

- VCCRTC A22 — +RTCVCC

HDA

- VCCSUSHDA P32 — 10mA — +3VALW_PCH

Need +3VALW and 0.1U close PCH

C315 0.1U_0402_16V4Z Close P32

Power Rails

- +3VS — L14 10UH_LB2012T100MR_20% — +3VS_VCC_CLKF33 — C277 10U_0603_6.3V6M — C309 1U_0402_6.3V6K
- +1.05VS_VTT — L12 10UH_LB2012T100MR_20% — +1.05VS_VCCA_A_DPL — C278 330U_D2_2V_Y — C296 1U_0402_6.3V6K — R808 0_0603_5% @ — L11 10UH_LB2012T100MR_20% — +1.05VS_VCCA_B_DPL — C295 1U_0402_6.3V6K
  - SGA00001700 220U 2.5V M B2 ESR 35mohm@100Khz
- +1.05VS_VTT — C336 22U_0805_6.3V6M — C335 22U_0805_6.3V6M — C326 1U_0402_6.3V6K — C327 1U_0402_6.3V6K — C316 1U_0402_6.3V6K
- +1.05VS_VTT — C321 1U_0402_6.3V6K
- +3VALW_PCH — C330 .1U_0402_16V7K Place near P24 — C333 .1U_0402_16V7K Place near P24
- +1.05VS_VTT — C352 1U_0402_6.3V6K
- +3VS — C704 .1U_0402_16V7K Place near AJ2 — C343 1U_0402_16V7K Place near AA16,W16 — C309 .1U_0402_16V7K Place near T34 — R02 Modify
- +1.05VS_VTT — C350 1U_0402_6.3V6K
- +1.05VS_VTT — C351 1U_0402_6.3V6K
- +1.05VS_VTT — C311 1U_0402_6.3V6K Place near AF17 — C312 1U_0402_6.3V6K Place near AG33 — C317 1U_0402_6.3V6K Place near AF33, AF34,AG34
- +1.05VS_VTT — C348 .1U_0402_16V7K — R02 Modify
- +1.05VS_VTT — C293 47U_0603_6.3V6M — C694 .1U_0402_16V7K — C693 .1U_0402_16V7K — Place near BJ8 — R02 Modify
- +RTCVCC — C293 1U_0402_6.3V6K — C685 1U_0402_16V7K — C687 1U_0402_16V7K — R02 Modify
- +5VALW_PCH — R202 100_0402_1% — D8 CH751H-40PT_SOD323-2 — +PCH_V5REF_SUS — C318 0.1U_0603_25V7K
- +5VS — R148 100_0402_1% — D7 CH751H-40PT_SOD323-2 — +PCH_V5REF_RUN — C244 1U_0603_10V6K

Notes

- Not support Deep S4,S5 connect to +3VALW
- suppied by internal 1.05V VR must NC
- suppied by internal 1.05V VR Must NC
- suppied by internal 1.05V VR Must NC
- GPIO28 — On-Die PLL Voltage Regulator — H : On-Die PLL voltage regulator enable — **VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA**
- GPIO28 — On-Die PLL Voltage Regulator — H : On-Die PLL voltage regulator enable — **VCCFDIPLL,VCCAPLLEXP,VCCAPLLDMI2 ,VCCAPLLSATA**

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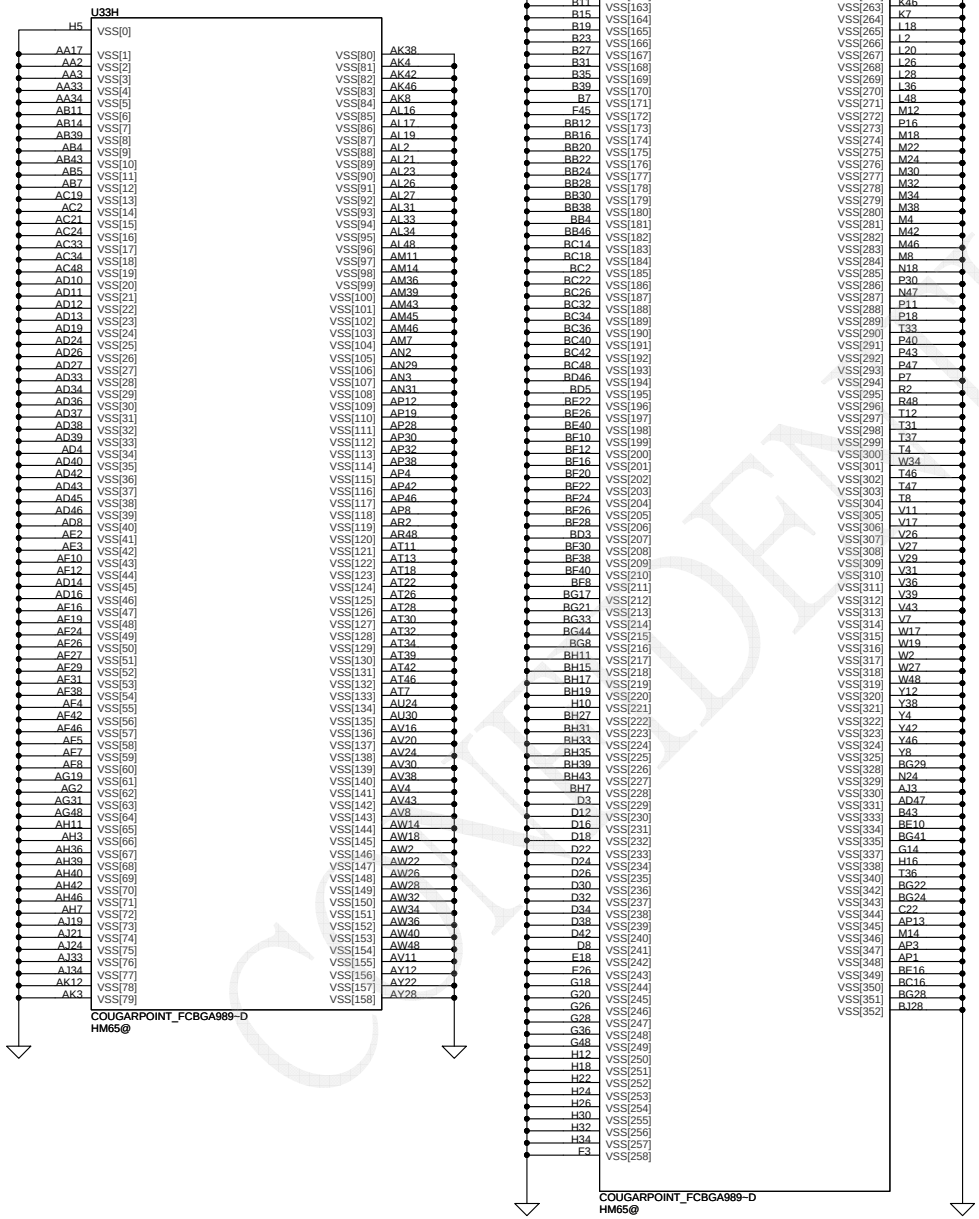

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Issued Date	2011/06/02	Deciphered Date	2012/06/02

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04/06 : Add 6bit VID Function.
for GS4, the boot voltage is 0.975V
for GV4, the boot voltage is 0.85V

R02 Modify
EC control ACIN

under GPU
close to ball : AD8

under GPU
close to ball : AE8,AD7

add ADPS function
follow Acer Request

R02 Modify

GPIO	I/O	USAGE
GPIO0	O	GPU_VID4
GPIO1	O	GPU_VID3
GPIO2	O	LCD_BL_PWM
GPIO3	O	LCD_VCC
GPIO4	O	LCD_BLEN
GPIO5	O	GPU_VID1
GPIO6	O	GPU_VID2
GPIO7	O	3D Vision
GPIO8	I/O	OVERT
GPIO9	I/O	ALERT
GPIO10	O	MEM_VREF_CTL
GPIO11	O	MEM_VDD_CTL(PES) GPU_VID0(Real N13P)
GPIO12	I	PWR_LEVEL
GPIO13	O	THERM_LOAD_STEP_DOWN
GPIO14	I	HPD_AB
GPIO15	I	HPD_C
GPIO16	O	THERM_LOAD_STEP_UP
GPIO17	I	HPD_D
GPIO18	I	HPD_E
GPIO19	I	HPD_F
GPIO20		Reserved
GPIO21		Reserved
GPIO22	I/O	SLI_RASTER_SYNC
GPIO23	O	SLI_SWAPRDY
GPIO24		

U1001
N13P-GS-A2 FCBGA 908P
GS@
SA000051880

U1001
N13P-GL-A1 FCBGA 908P
GL@
SA000051A00

U1001
N13M-GS FCBGA 908P GPU
GM@
SA000057F20

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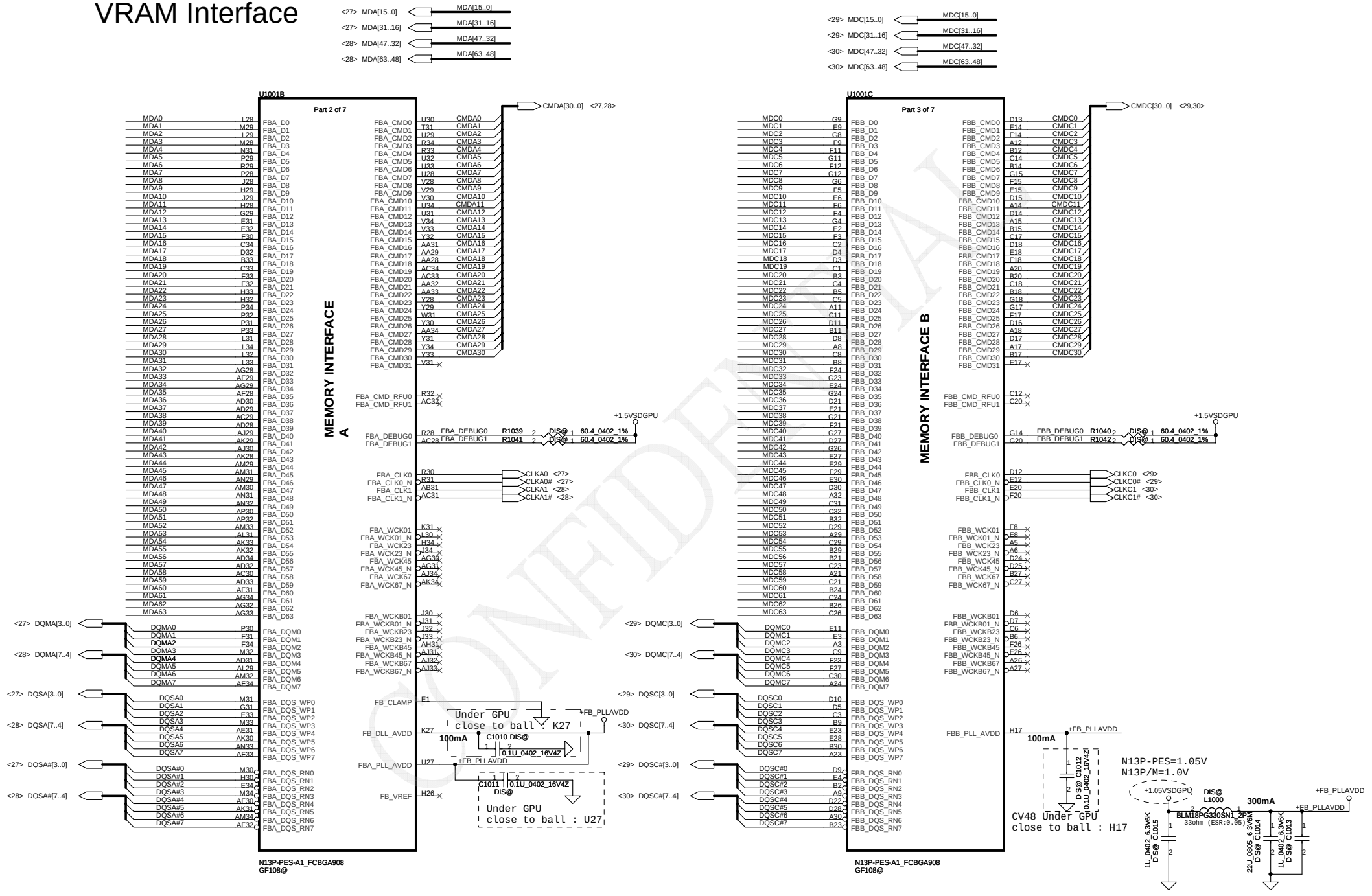
VRAM Interface



Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

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Title: SCHEMATIC,MB A7912

Size	Document Number	Rev
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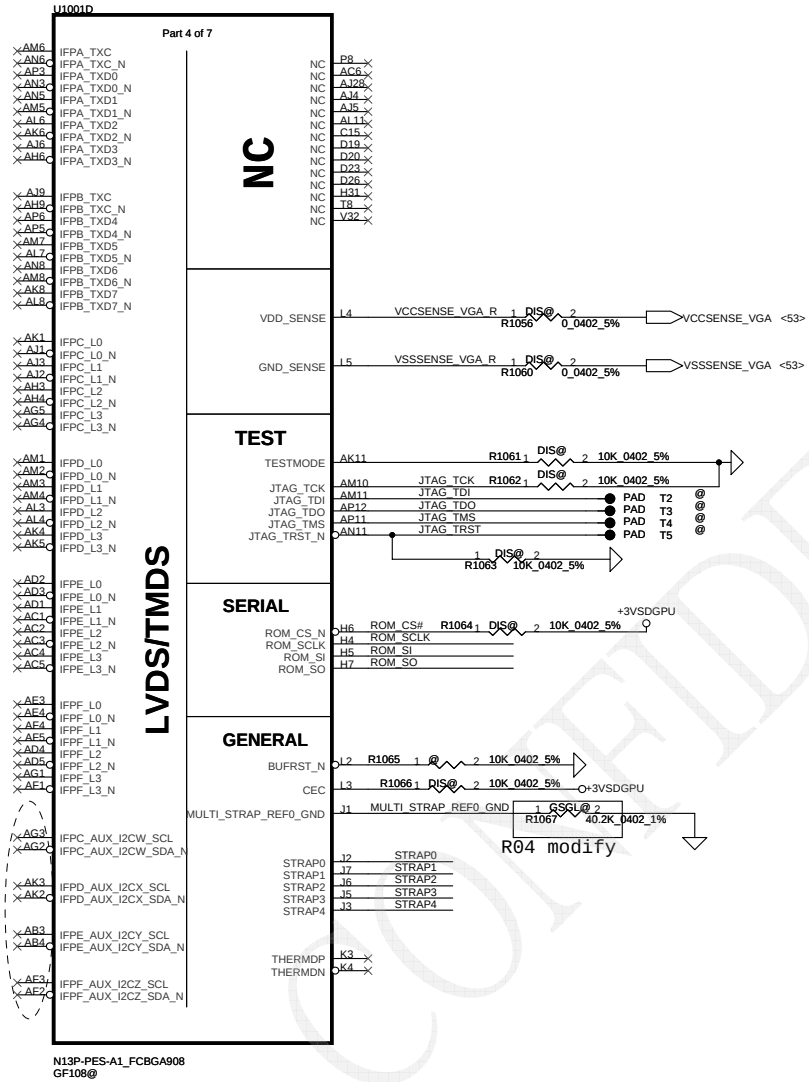

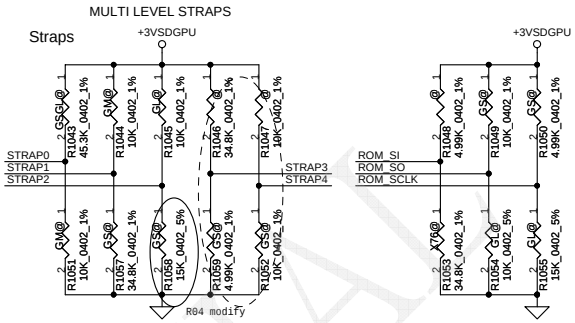

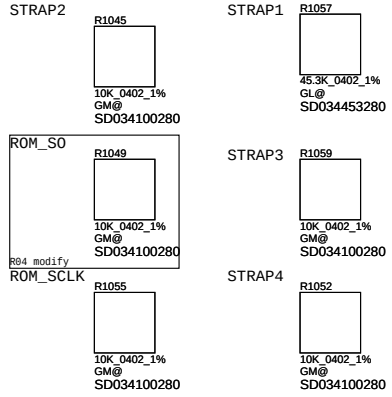

For N13P-GS(ES) strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO20	R PU 45K	R PD 35K	R PD 15K	R PD 5K	R PD 10K	R PD 35K	R PU 10K	R PU 5K
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S40	R PU 45K	R PD 35K	R PD 15K	R PD 5K	R PD 10K	R PD 15K	R PU 10K	R PU 5K

For N13P-GL(QS) strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13P-GS	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO20	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 35K	R PD 10K	R PD 15K
N13P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S40	R PU 45K	R PD 45K	R PU 10K	n/a	n/a	R PD 15K	R PD 10K	R PD 15K

For N13M-GS(QS) strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N13M-GS	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO20	R PD 10K	R PU 10K	R PU 10K	R PD 10K	R PD 10K	R PD 10K	R PU 10K	R PD 10K

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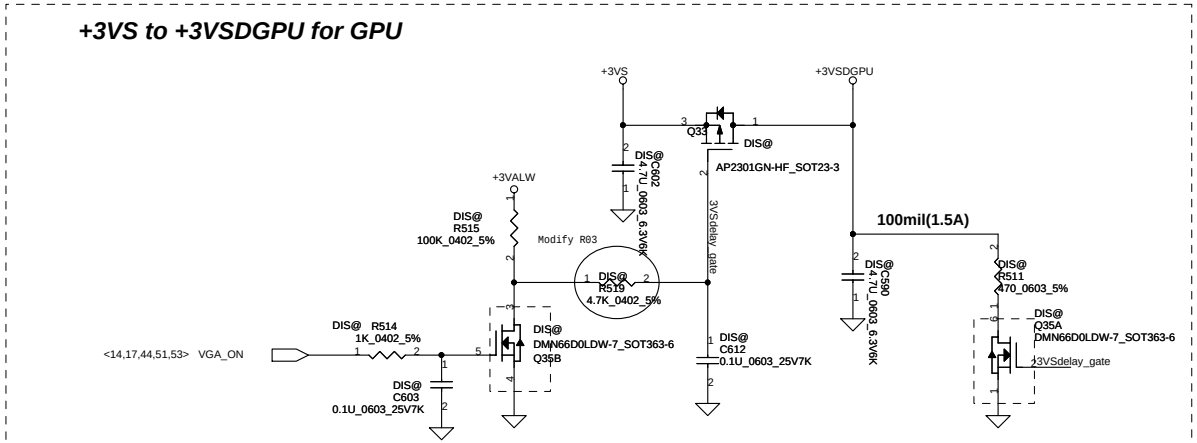
+3VS to +3VSDGPU for GPU



Design guide no define

U1001E

Part 5 of 7

POWER

7200mA

+1.5VSDGPU — Under GPU
DIS@ C1023 4.7U_0603_6.3V6K
DIS@ C1024 1U_0402_6.3V6K
DIS@ C1025 1U_0402_16V4Z
DIS@ C1026 0.1U_0402_16V4Z
DIS@ C1027 0.1U_0402_16V4Z
DIS@ C1037 0.1U_0402_16V4Z

Under GPU
DIS@ C1038 4.7U_0603_6.3V6K
DIS@ C1039 1U_0402_6.3V6K
DIS@ C1032 1U_0402_16V4Z
DIS@ C1033 0.1U_0402_16V4Z
DIS@ C1040 0.1U_0402_16V4Z
DIS@ C1041 0.1U_0402_16V4Z

Near GPU
DIS@ C1045 10U_0603_6.3V6M
DIS@ C1046 10U_0603_6.3V6M
DIS@ C1047 22U_0805_6.3V6M
DIS@ C1048 22U_0805_6.3V6M

FBVDDQ_0 AA27
FBVDDQ_1 AA30
FBVDDQ_2 AB27
FBVDDQ_3 AB33
FBVDDQ_4 AC27
FBVDDQ_5 AD27
FBVDDQ_6 AE27
FBVDDQ_7 AF27
FBVDDQ_8 AG27
FBVDDQ_9 B13
FBVDDQ_10 B16
FBVDDQ_11 B19
FBVDDQ_12 E13
FBVDDQ_13 E16
FBVDDQ_14 E19
FBVDDQ_15 H10
FBVDDQ_16 H11
FBVDDQ_17 H12
FBVDDQ_18 H13
FBVDDQ_19 H14
FBVDDQ_20 H15
FBVDDQ_21 H16
FBVDDQ_22 H18
FBVDDQ_23 H19
FBVDDQ_24 H20
FBVDDQ_25 H21
FBVDDQ_26 H22
FBVDDQ_27 H23
FBVDDQ_28 H24
FBVDDQ_29 H8
FBVDDQ_30 H9
FBVDDQ_31 L27
FBVDDQ_32 M27
FBVDDQ_33 N27
FBVDDQ_34 P27
FBVDDQ_35 R27
FBVDDQ_36 T27
FBVDDQ_37 T30
FBVDDQ_38 T33
FBVDDQ_39 V27
FBVDDQ_40 W27
FBVDDQ_41 W30
FBVDDQ_42 W33
FBVDDQ_43 Y27

PEX_IOVDDQ_0 AG19
PEX_IOVDDQ_1 AG21
PEX_IOVDDQ_2 AG22
PEX_IOVDDQ_3 AG24
PEX_IOVDDQ_4 AH21
PEX_IOVDDQ_5 AH25

PEX_IOVDDQ_0 AG13
PEX_IOVDDQ_1 AG15
PEX_IOVDDQ_2 AG16
PEX_IOVDDQ_3 AG18
PEX_IOVDDQ_4 AG25
PEX_IOVDDQ_5 AH15
PEX_IOVDDQ_6 AH18
PEX_IOVDDQ_7 AH26
PEX_IOVDDQ_8 AH27
PEX_IOVDDQ_9 AJ27
PEX_IOVDDQ_10 AK27
PEX_IOVDDQ_11 AL27
PEX_IOVDDQ_12 AM28
PEX_IOVDDQ_13 AN28

2700 mA
total 2700mA
Design guide page.68

Near GPU — Under GPU
DIS@ C1016 1U_0402_6.3V6K
DIS@ C1017 1U_0402_6.3V6K
DIS@ C1018 4.7U_0603_6.3V6K
DIS@ C1019 10U_0603_6.3V6M
DIS@ C1020 10U_0603_6.3V6M
DIS@ C1021 22U_0805_6.3V6M
DIS@ C1022 22U_0805_6.3V6M
+1.05VSDGPU

Near GPU — Under GPU
DIS@ C1028 1U_0402_6.3V6K
DIS@ C1034 1U_0402_6.3V6K
DIS@ C1029 4.7U_0603_6.3V6K
DIS@ C1035 10U_0603_6.3V6M
DIS@ C1030 10U_0603_6.3V6M
DIS@ C1031 22U_0805_6.3V6M
DIS@ C1036 22U_0805_6.3V6M
+1.05VSDGPU

PEX_PLL_HVDD AH12 — 150mA — +PEX_PLL_HVDD — DIS@ C1049 0.1U_0402_16V4Z
PEX_SVDD_3V3 AG12 — DIS@ C1050 0.1U_0402_16V4Z — +PEX_PLLVDD
PEX_PLLVDD AG26

370mA
Near GPU
DIS@ C1042 1U_0402_6.3V6K
DIS@ C1043 4.7U_0603_6.3V6K
DIS@ C1044 4.7U_0603_6.3V6K
+3VSDGPU

150mA
Under GPU — Near GPU
DIS@ C1051 0.1U_0402_16V4Z
DIS@ C1052 1U_0402_6.3V6K
DIS@ C1053 4.7U_0603_6.3V6K
+1.05VSDGPU
L1002 BLM18PG121SN1D_0603 GL@N13P

Reference Sch = 300R@100MHz
Design Guide page69 沒定義

L1004 0_0603_5% GM@ SD013000080
L1005 0_0603_5% GS@ SD013000080

VDD33_0 J8
VDD33_1 K8
VDD33_2 L8
VDD33_3 M8
+VDD33

120mA
Design guide no define

IFPAB_PLLVDD AH8 — +IFPAB_PLLVDD — R1130 DIS@ 10K_0402_5% — R1069 @ 1K_0402_5%
IFPAB_RSET AJ8
IFPA_IOVDD AG8 — +IFPAB_IOVDD — R1131 DIS@ 10K_0402_5%
IFPB_IOVDD AG9

IFPC_PLLVDD AF7 — +IFPC_PLLVDD — R1071 DIS@ 10K_0402_5% — R1073 @ 1K_0402_5%
IFPC_RSET AF8
IFPC_IOVDD AF6 — +IFPC_IOVDD — R1074 DIS@ 10K_0402_5%

IFPD_PLLVDD AG7 — +IFPD_PLLVDD — R1076 DIS@ 10K_0402_5% — R1078 @ 1K_0402_5%
IFPD_RSET AN2
IFPD_IOVDD AG6 — +IFPD_IOVDD — R1079 DIS@ 10K_0402_5%

IFPEF_PLVDD AB8 — +IFPEF_PLLVDD — R1081 DIS@ 10K_0402_5% — R1082 @ 1K_0402_5%
IFPEF_RSET AD6
IFPE_IOVDD AC7 — +IFPEF_IOVDD — R1083 DIS@ 10K_0402_5%
IFPF_IOVDD AC8

+1.5VSDGPU
R1070 DIS@ 10_0402_5% — FB_VDDQ_SENSE F1 — FB_VDDQ_SENSE
R1072 DIS@ 10_0402_5% — FB_GND_SENSE F2 — FB_GND_SENSE
+1.5VSDGPU
R1075 DIS@ 40.2_0402_1% — FB_CAL_PD_VDDQ J27 — FB_CAL_PD_VDDQ
R1077 DIS@ 42.2_0402_1% — FB_CAL_PU_GND H27 — FB_CAL_PU_GND
R1080 DIS@ 51.1_0402_1% — FB_CAL_TERM_GND H25 — FB_CAL_TERM_GND

Under GPU (one per pin)
DIS@ C1054 0.1U_0402_16V4Z
DIS@ C1055 0.1U_0402_16V4Z
DIS@ C1056 0.1U_0402_16V4Z
DIS@ C1057 0.1U_0402_16V4Z
DIS@ C1058 1U_0402_6.3V6K
DIS@ C1059 1U_0402_6.3V6K
DIS@ C1060 4.7U_0603_6.3V6K
+3VSDGPU
DIS@ R1068 0_0603_5%

N13P-PES-A1_FCBGA908
GF108@

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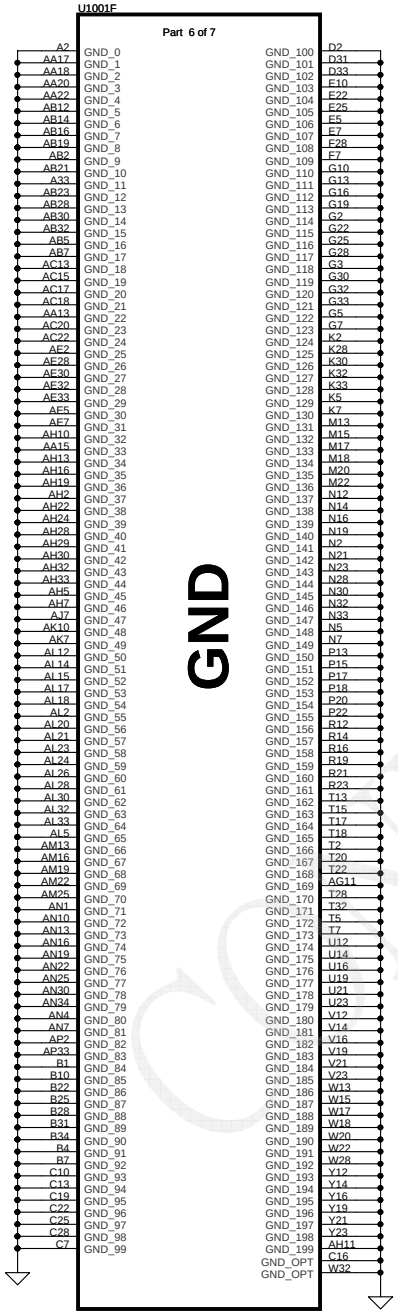

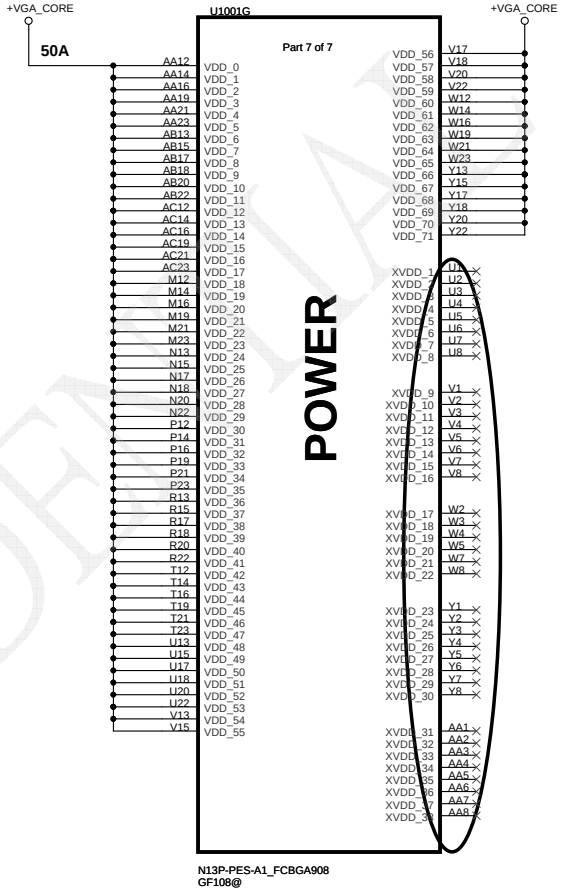

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VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB

R02 modify
Swap MDA13 and MDA14

Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Samsung : SA000035700 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA 96P)
Hynix : SA000032400 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)

R04 modify for EMI

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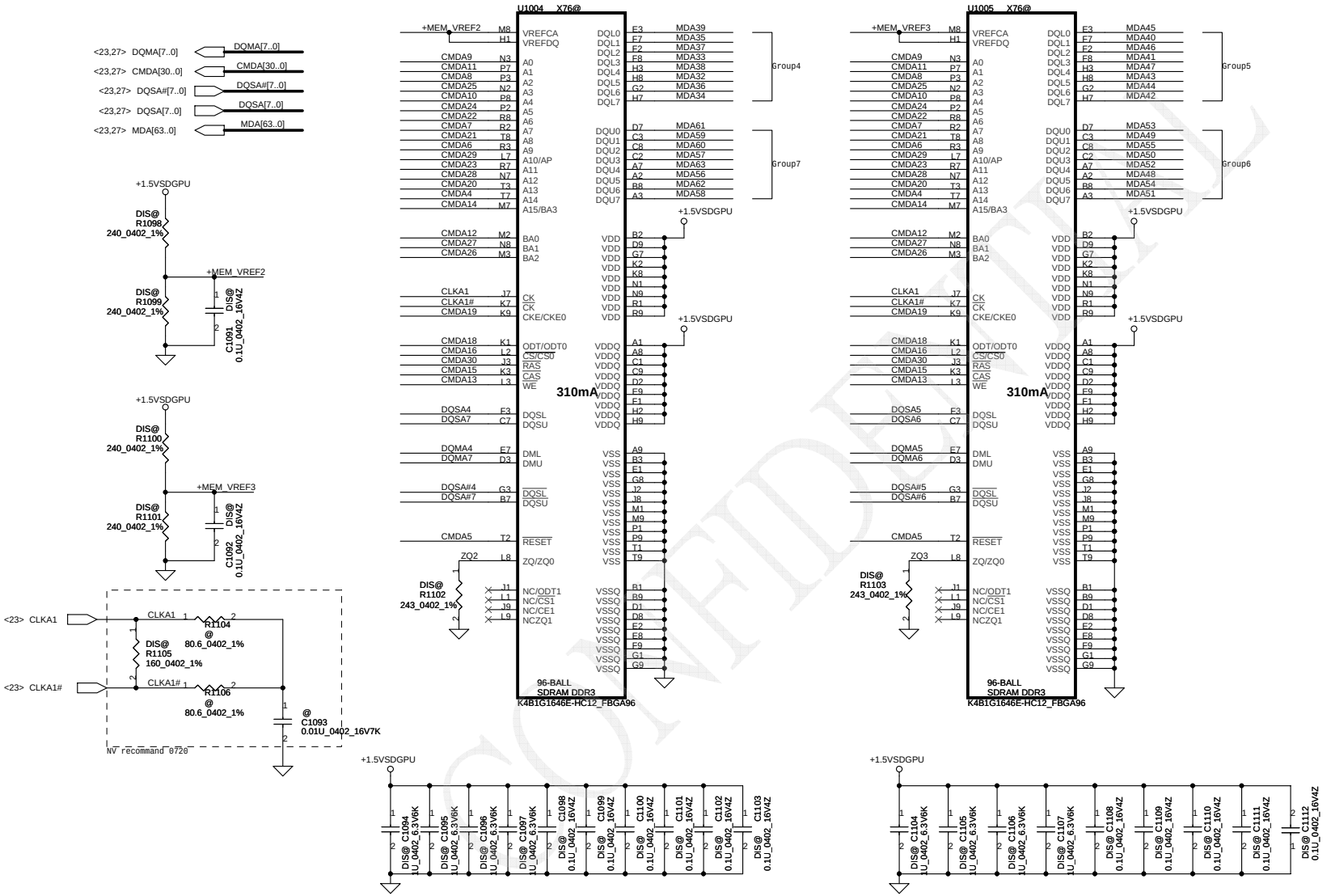
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB

128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

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Title	SCHEMATIC,MB A7912
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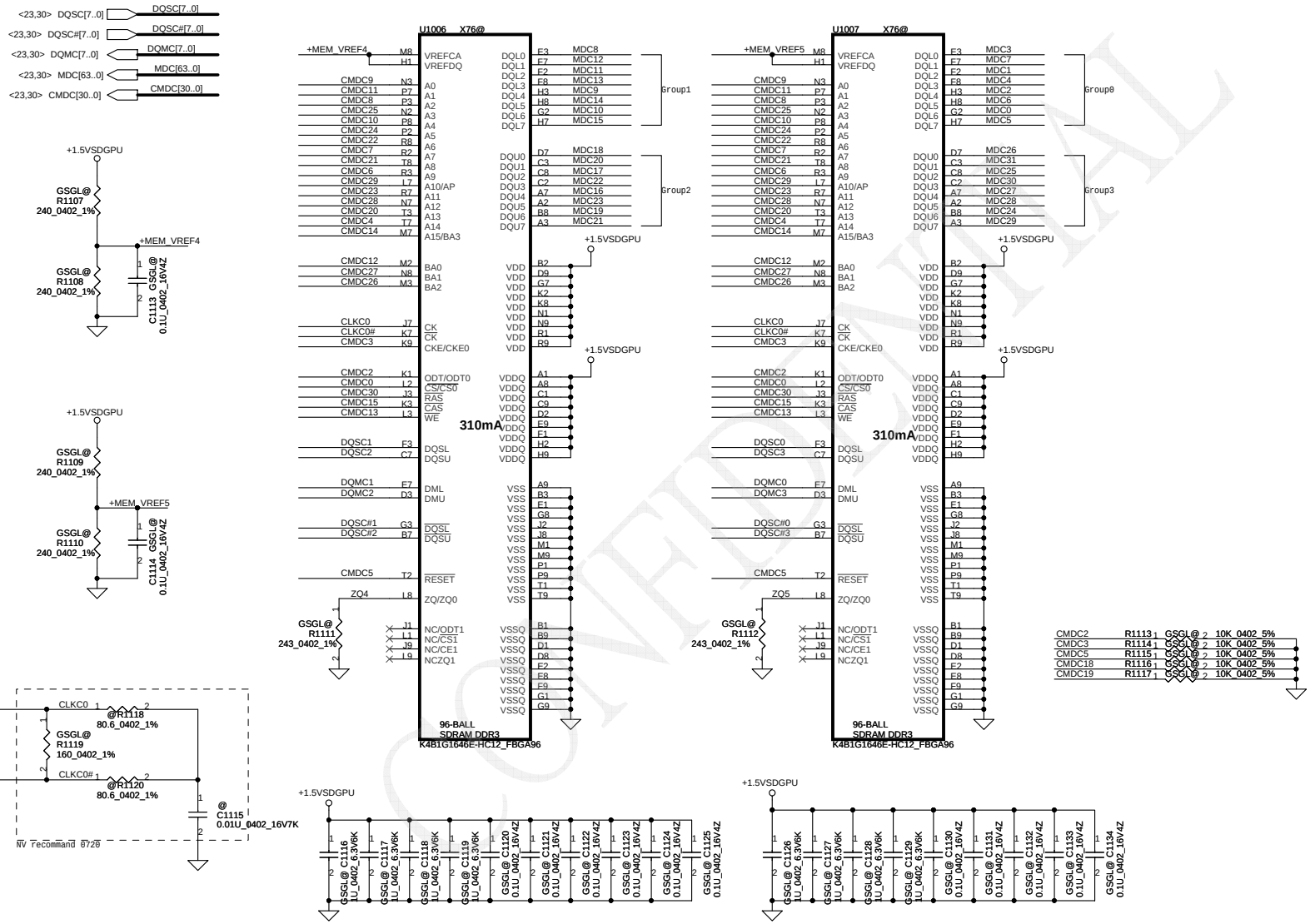
VRAM DDR3 chips (1GB)

64Mx16 DDR3 *8==>1GB
128Mx16 DDR3 *8==>2GB



Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

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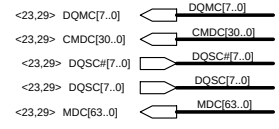
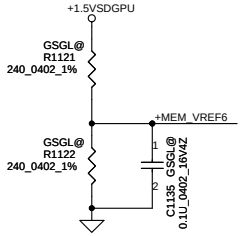
VRAM DDR3 chips (1GB)

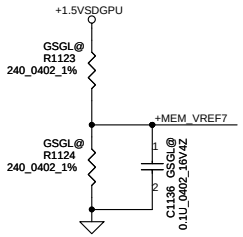
64Mx16 DDR3 *8==>1GB

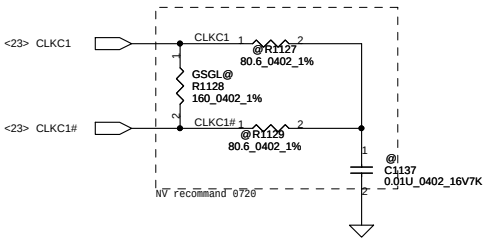
128Mx16 DDR3 *8==>2GB

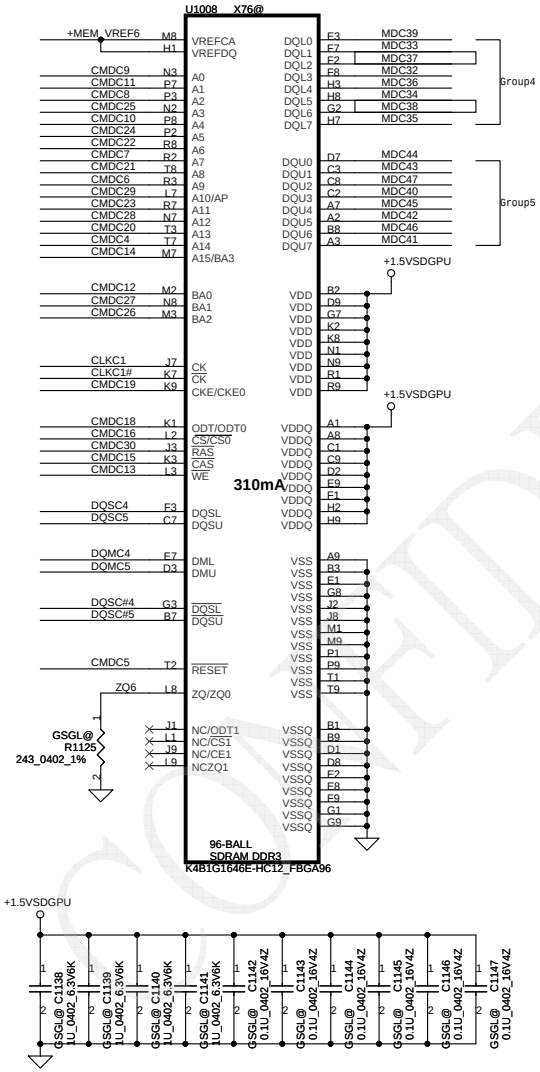
R02 modify
Swap MDC37 and MDC38

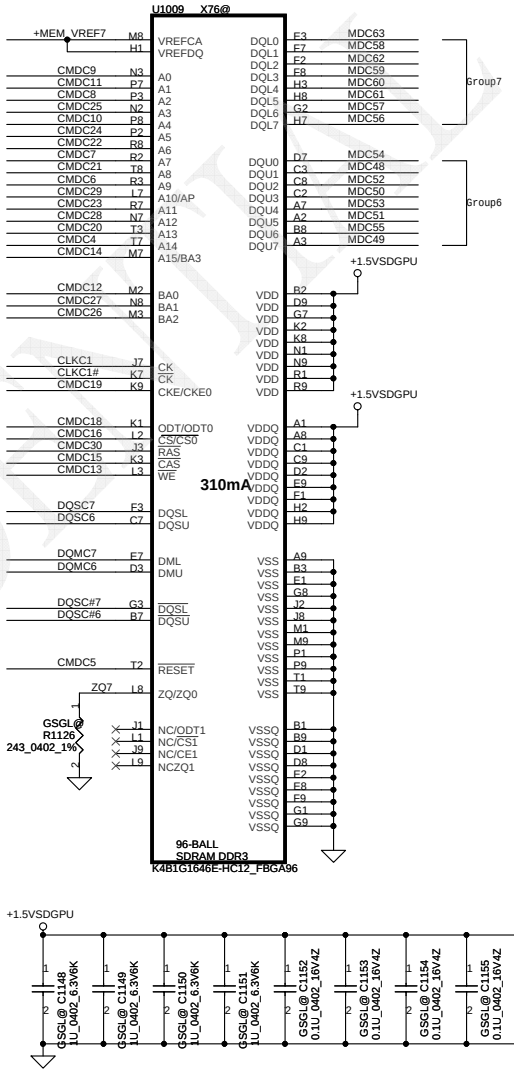












Mode D Address	0..31	32..63
CMD0	CS0_L#	
CMD1		
CMD2	ODT_L	
CMD3	CKE	
CMD4	A14	A14
CMD5	RST	RST
CMD6	A9	A9
CMD7	A7	A7
CMD8	A2	A2
CMD9	A0	A0
CMD10	A4	A4
CMD11	A1	A1
CMD12	BA0	BA0
CMD13	WE*	WE*
CMD14	A15	A15
CMD15	CAS*	CAS*
CMD16		CS0_H#
CMD17		
CMD18		ODT_H
CMD19		CKE_H
CMD20	A13	A13
CMD21	A8	A8
CMD22	A6	A6
CMD23	A11	A11
CMD24	A5	A5
CMD25	A3	A3
CMD26	BA2	BA2
CMD27	BA1	BA1
CMD28	A12	A12
CMD29	A10	A10
CMD30	RAS*	RAS*
Not Available		
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2011/06/02	Deciphered Date	2012/06/02

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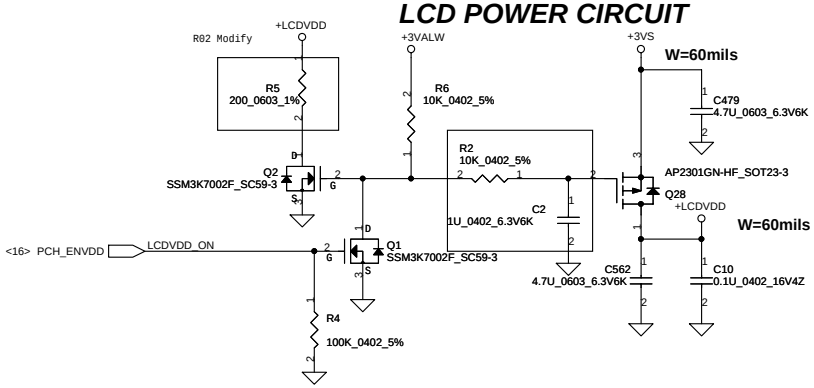
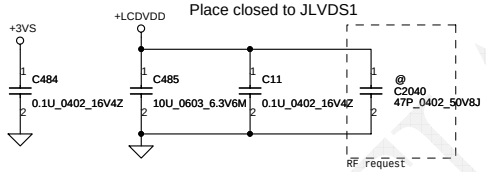
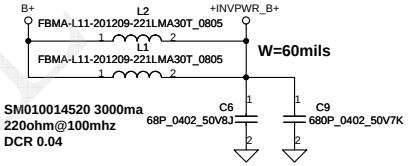
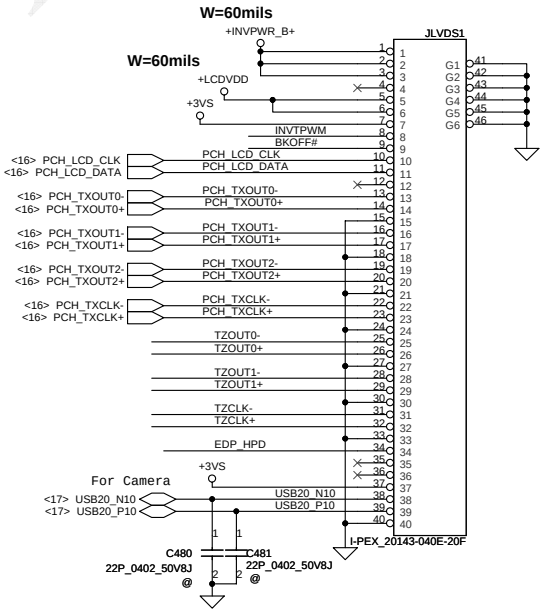
LCD POWER CIRCUIT

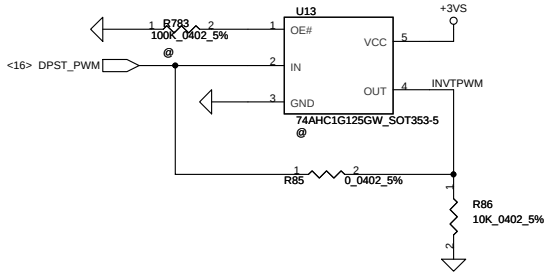


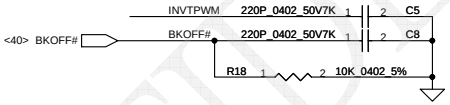




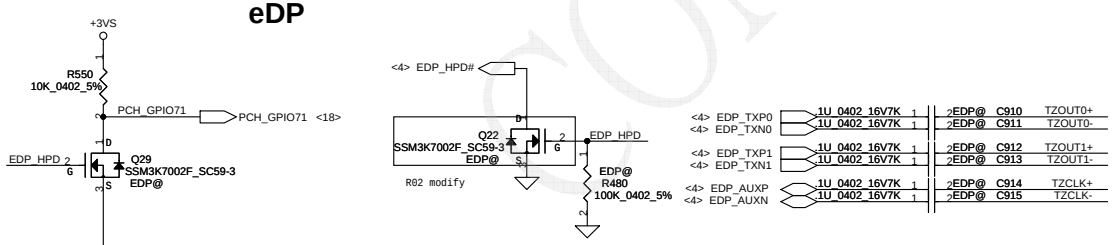
LCD/LED PANEL Conn.

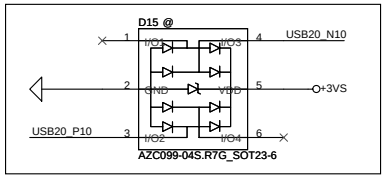






eDP





Modify R02

	GPIO71 PCH_GPIO71
eDP	0
LVDS	1

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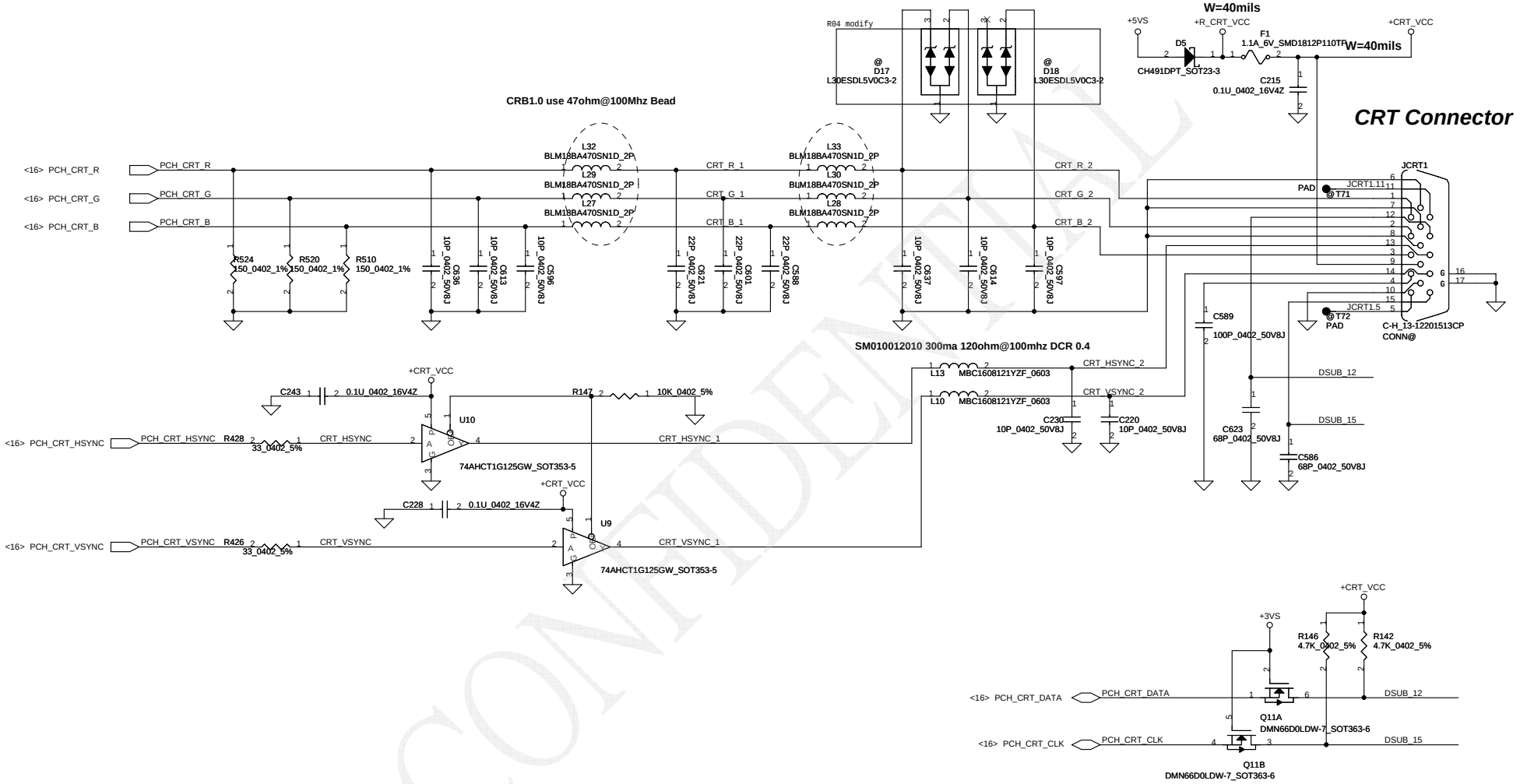

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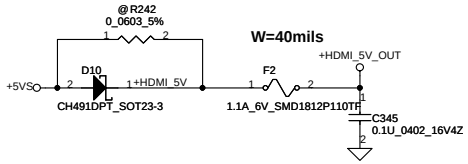
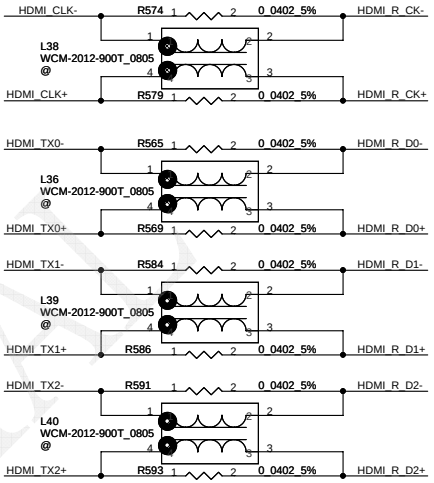
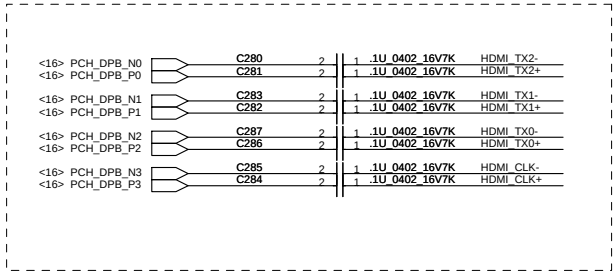
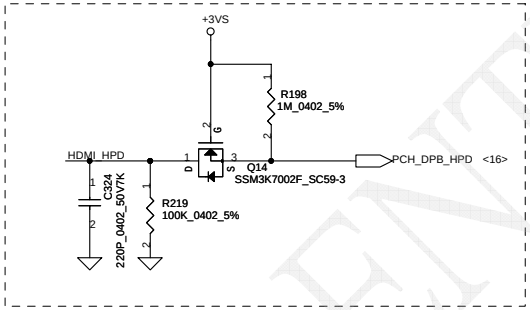
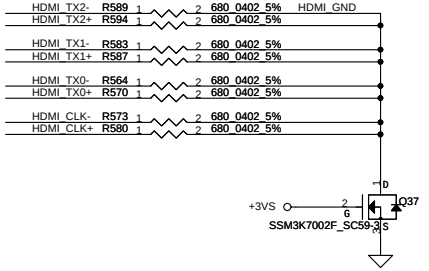


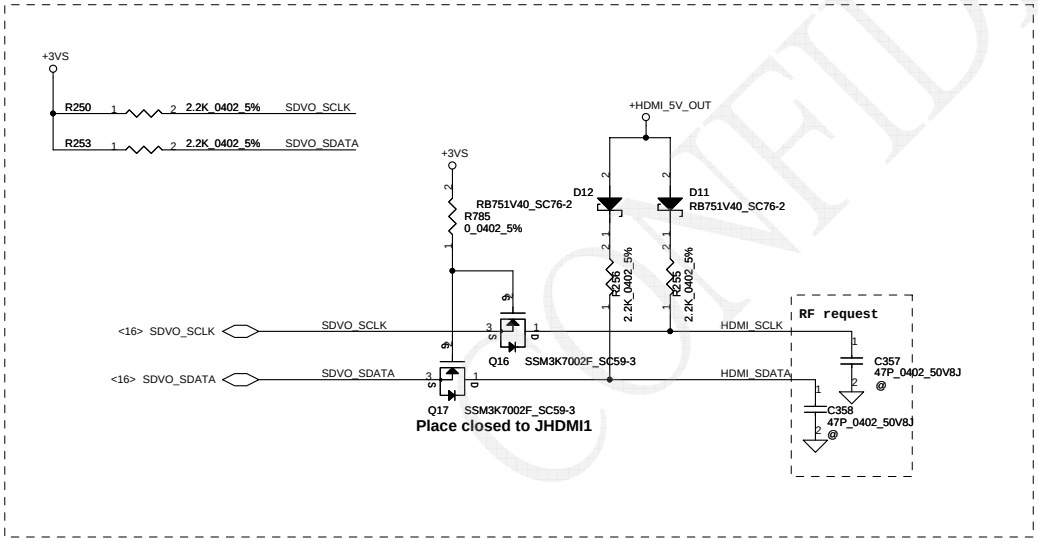
SM070001310 400ma 90ohm@100mhz DCR 0.3

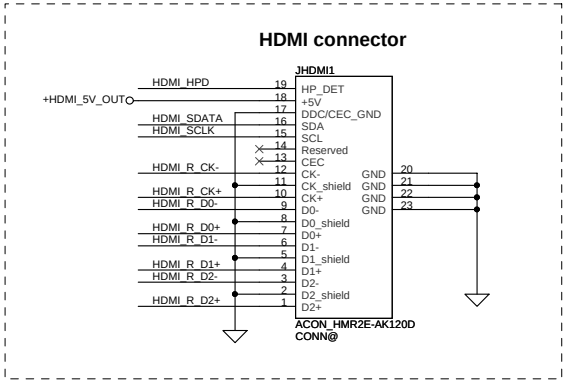












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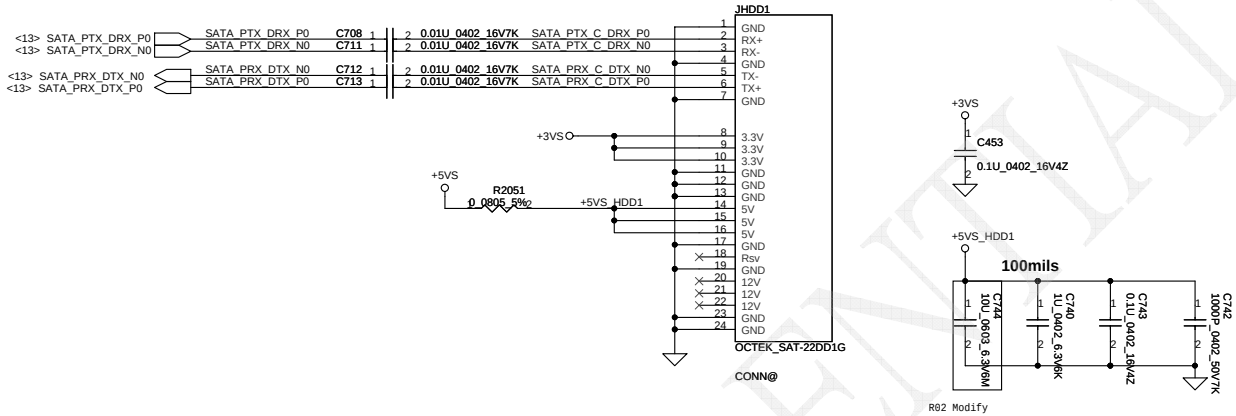
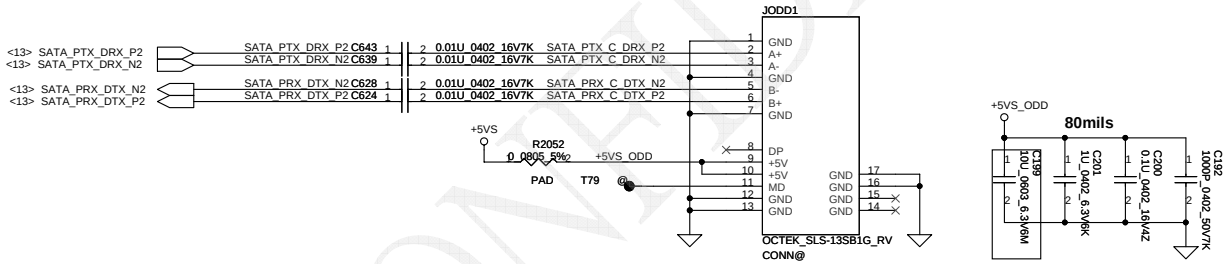
SATA HDD1 Conn.

CL 4.0 mm



SATA ODD Conn.



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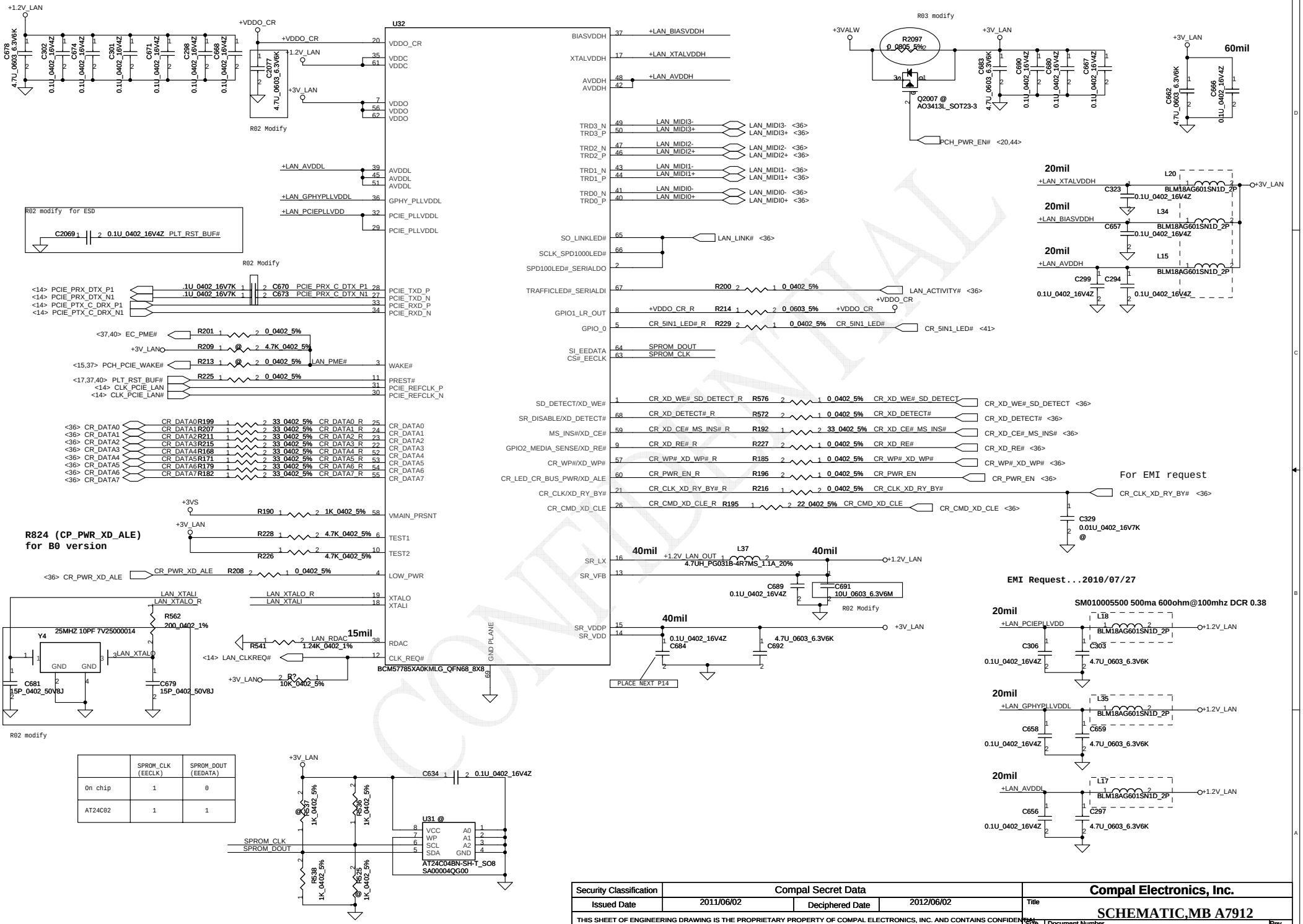

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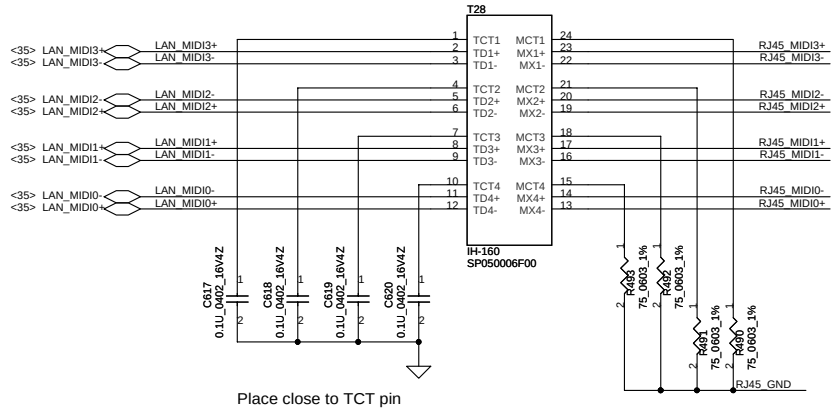
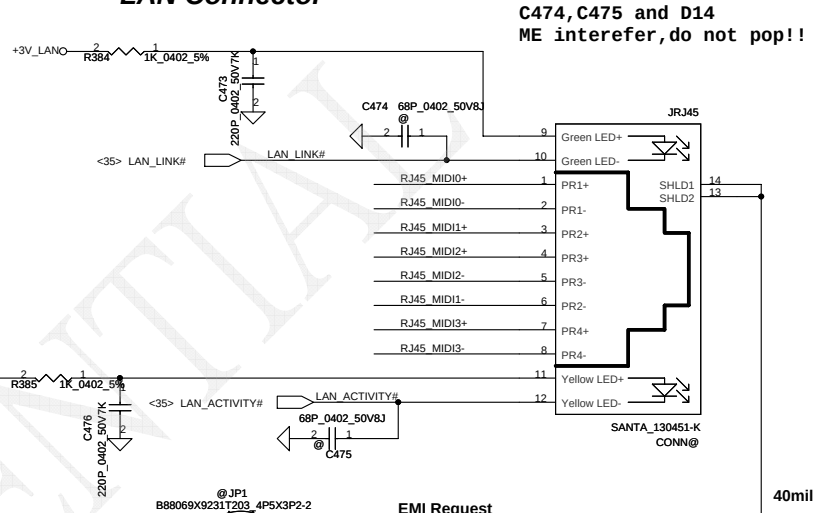
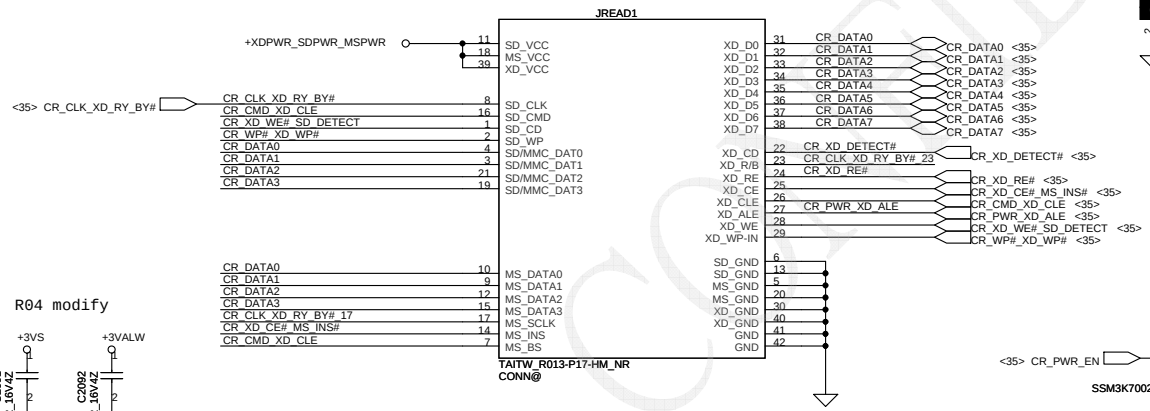
LAN Connector

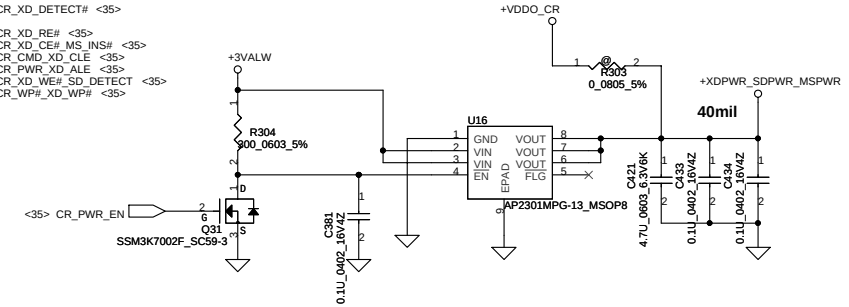


BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00

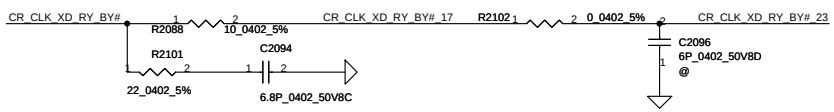


Card Reader Connector





R02 modify for SD3.0 issue



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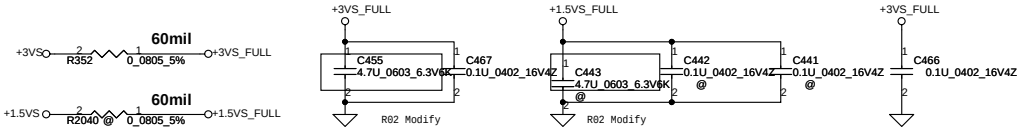
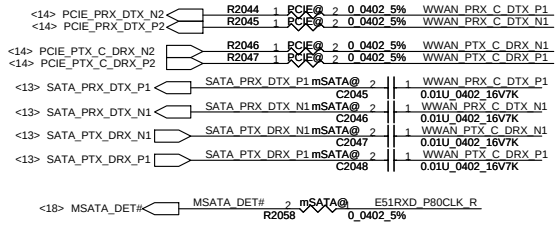
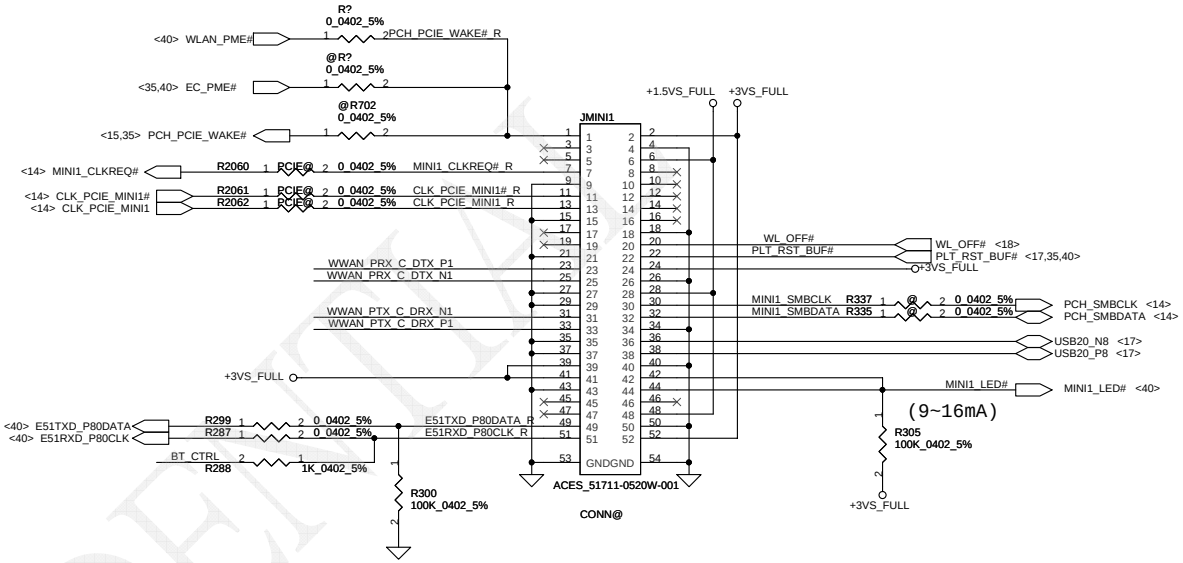
For Wireless LAN or MSATA

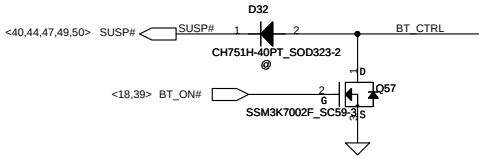


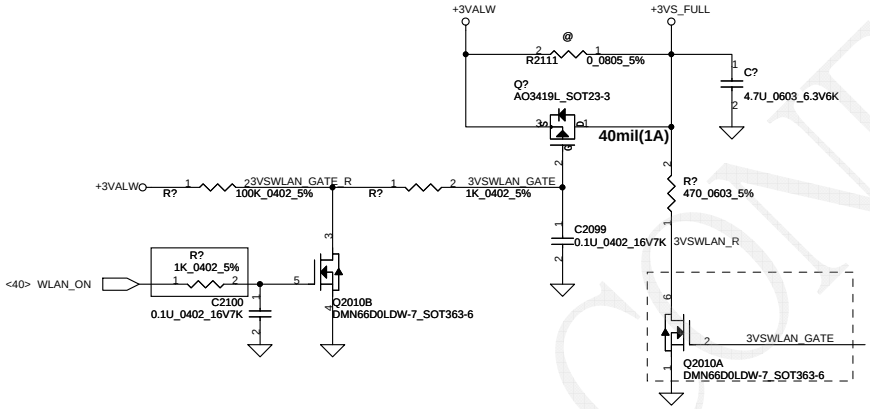




WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CTRL	H	L
BT_ON#	L	H





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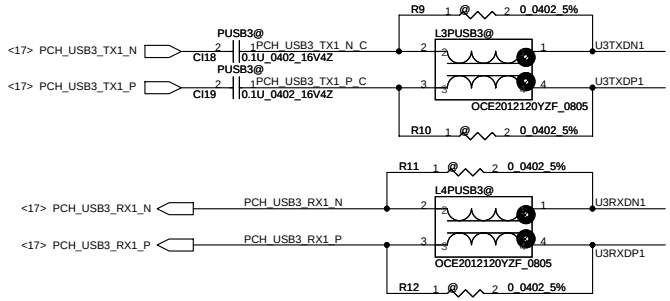
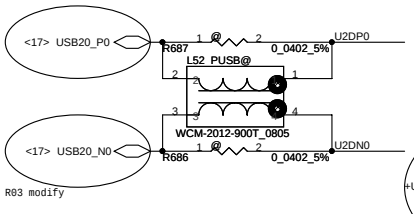
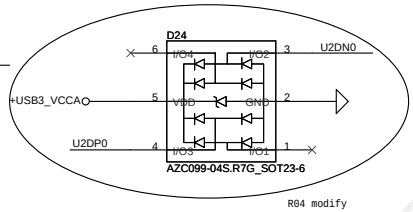
Deafult use PCH side USB3.0 signal

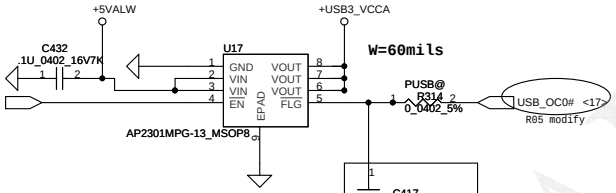
For USB2.0 ESD request



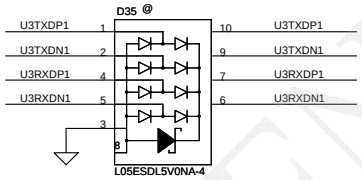


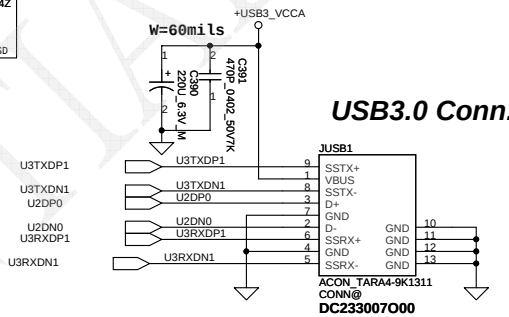
For USB2.0 ESD request



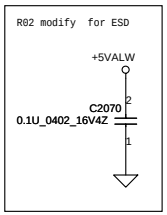


For ESD request

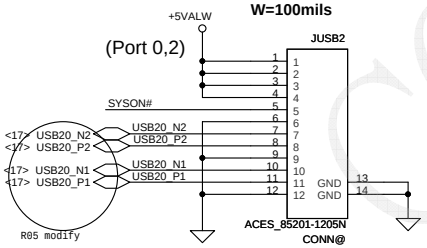




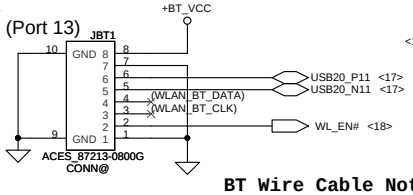
USB3.0 Conn.



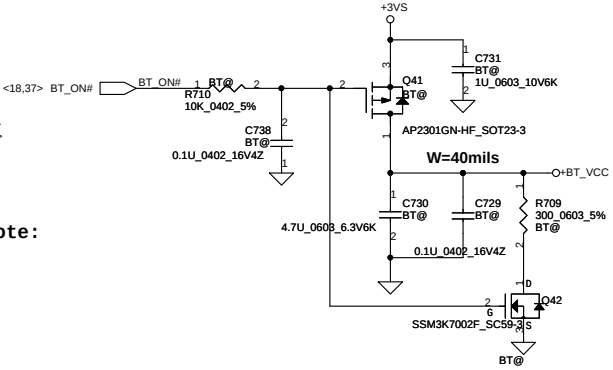
USB/B Conn.



BT Conn.



BT Wire Cable Note:
Pin 3, Pin 4 NC



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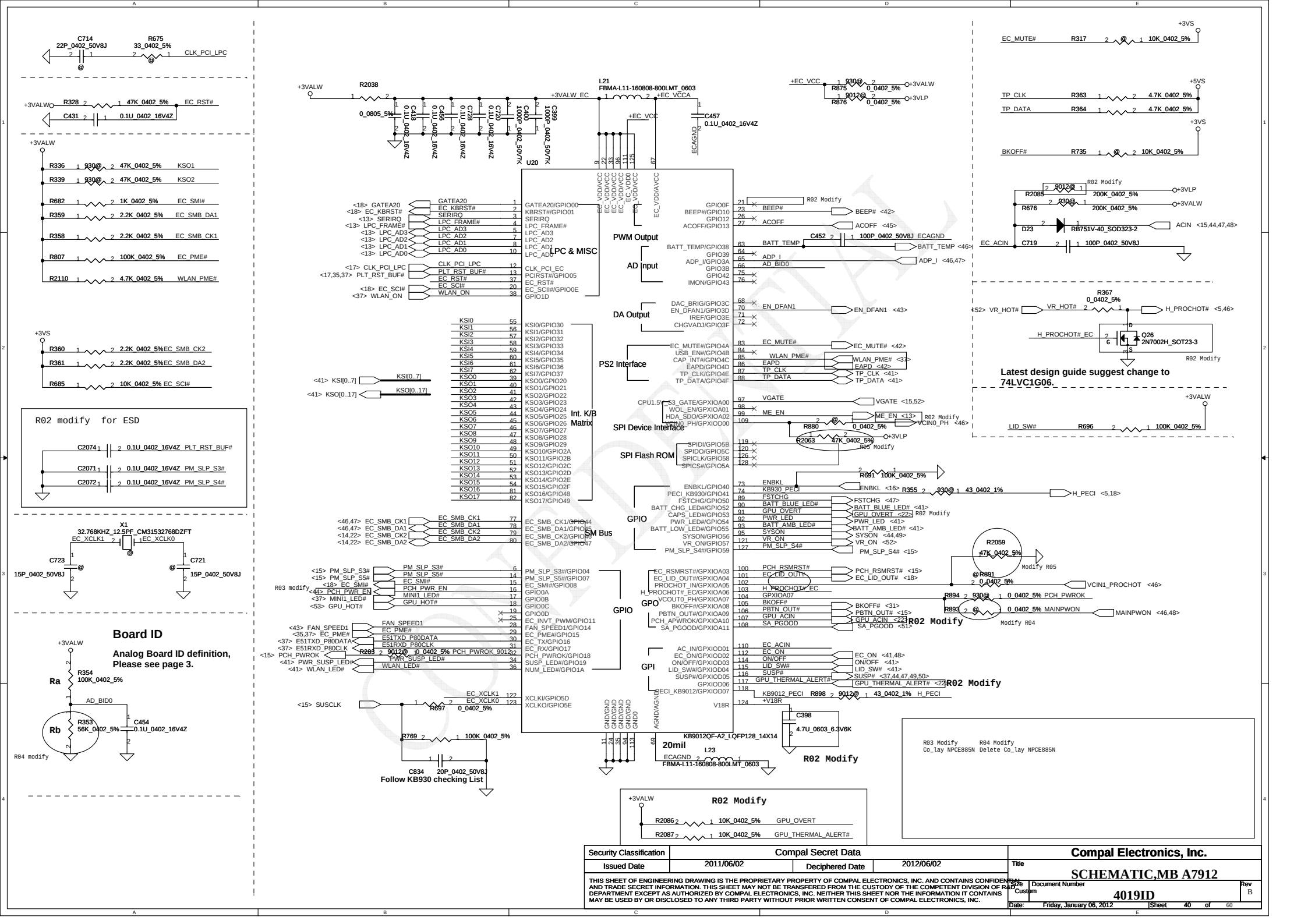

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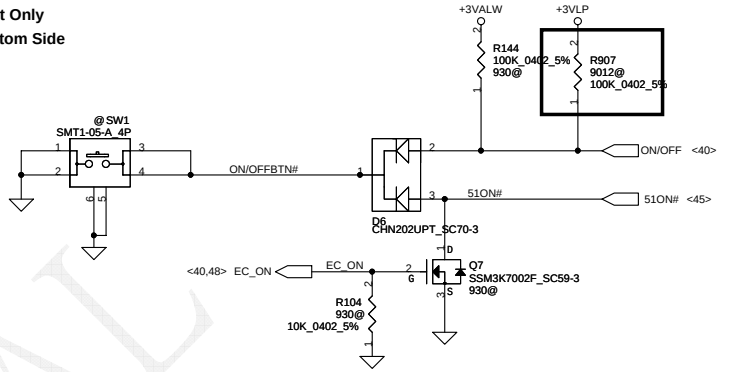
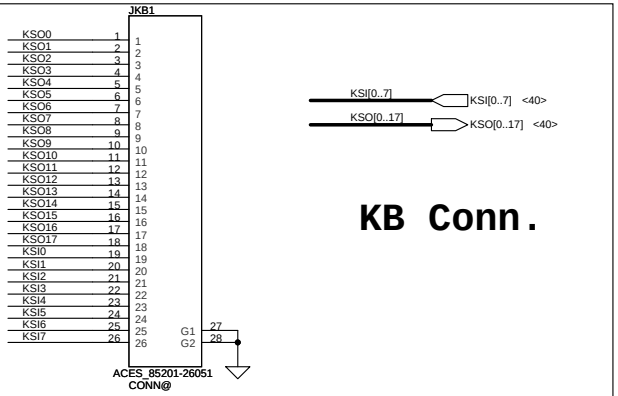
ON/OFF BTN

Test Only

Bottom Side



KB Conn.



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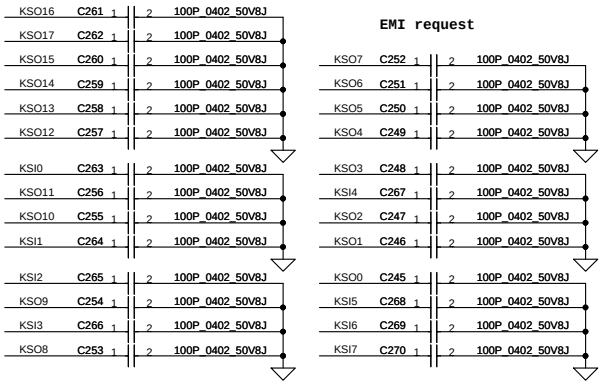
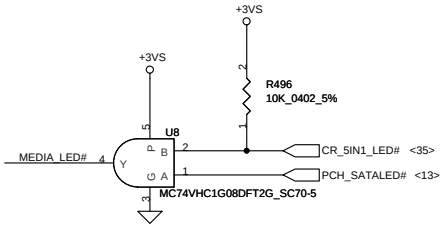
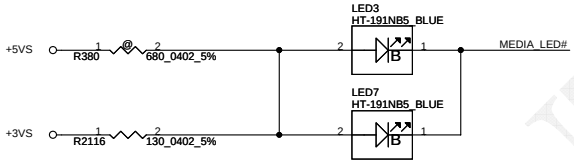
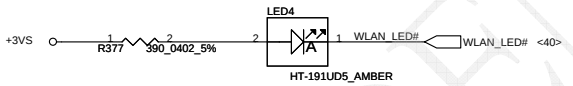
KSO[0..17] KSO[0..17] <40>

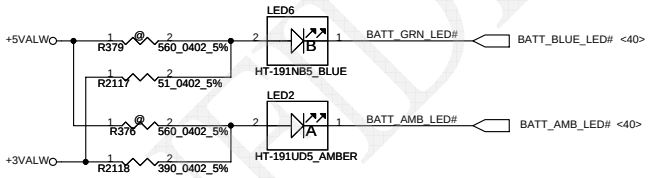
EMI request

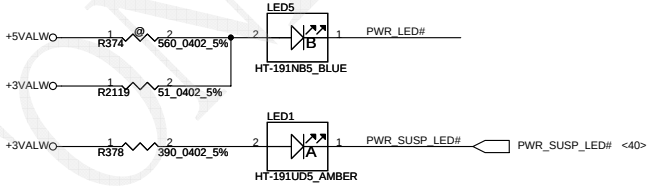


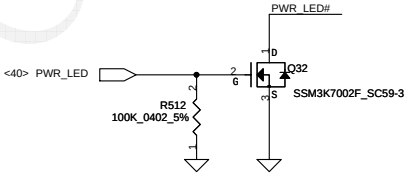




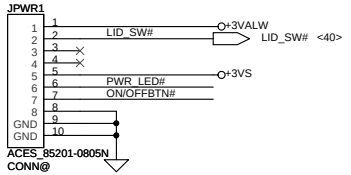




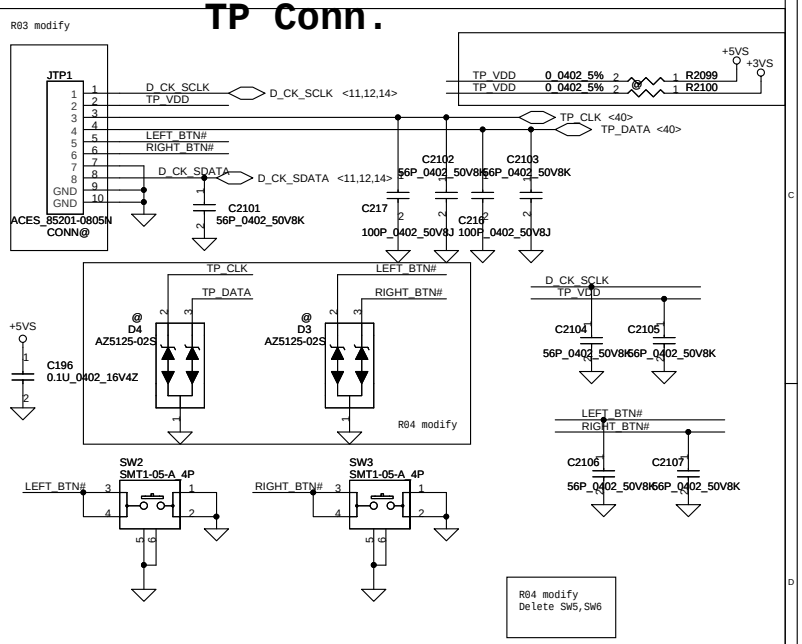




PWR/B



TP Conn.



R04 modify
Delete SW5,SW6

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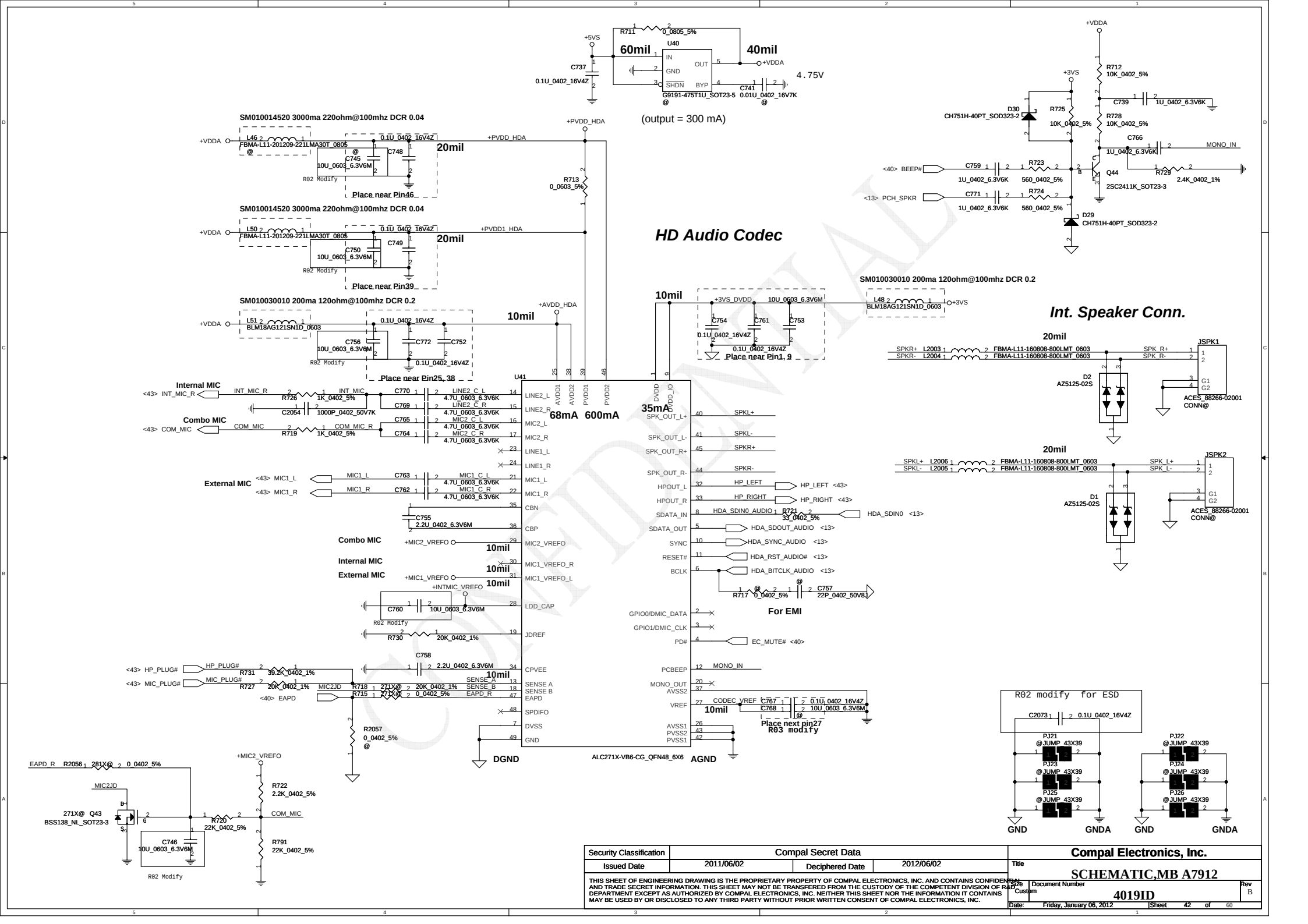

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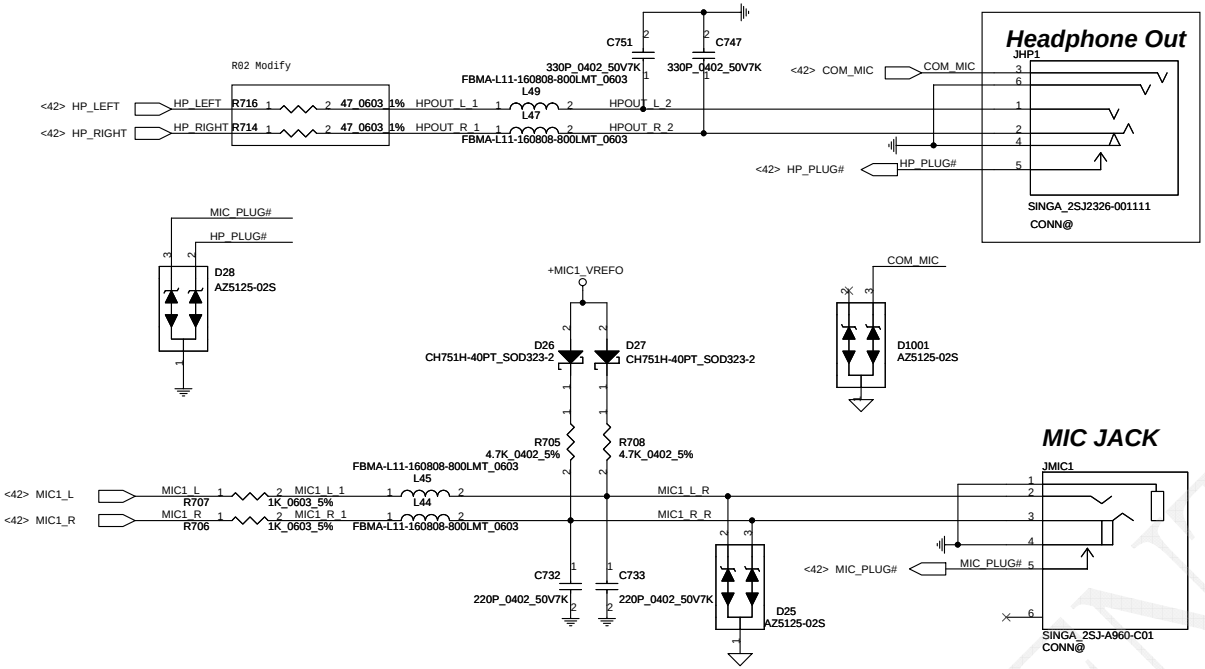

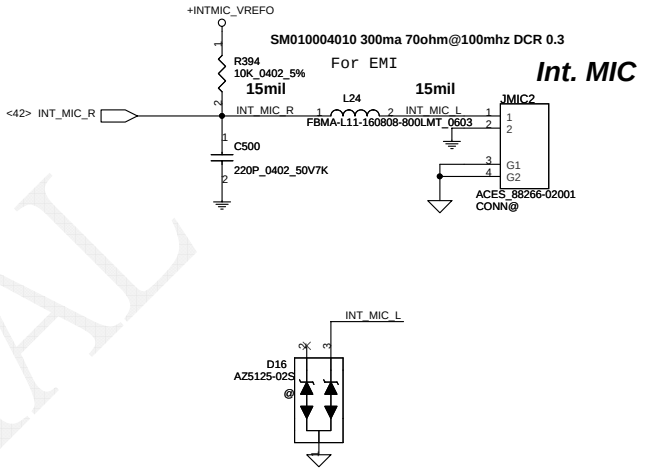

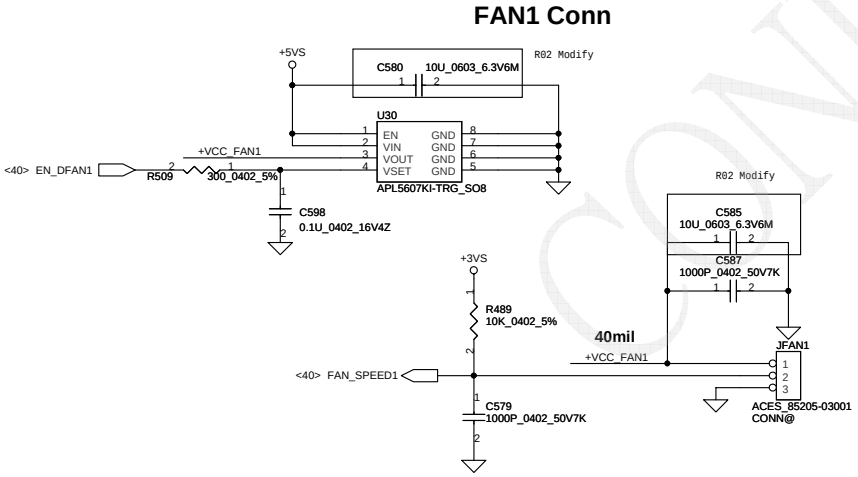

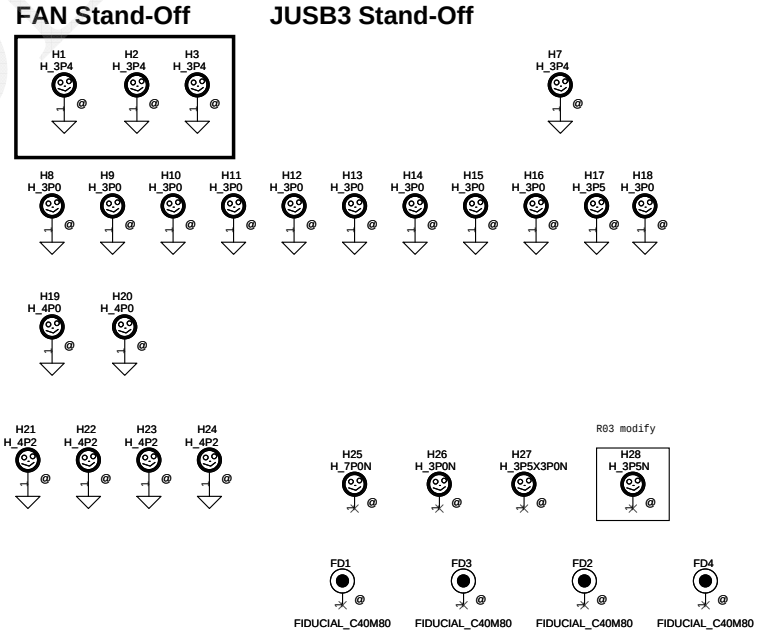

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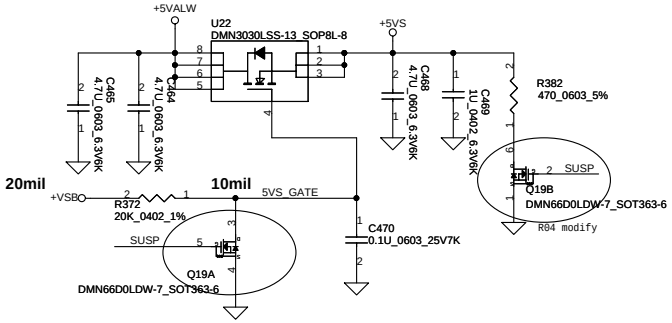
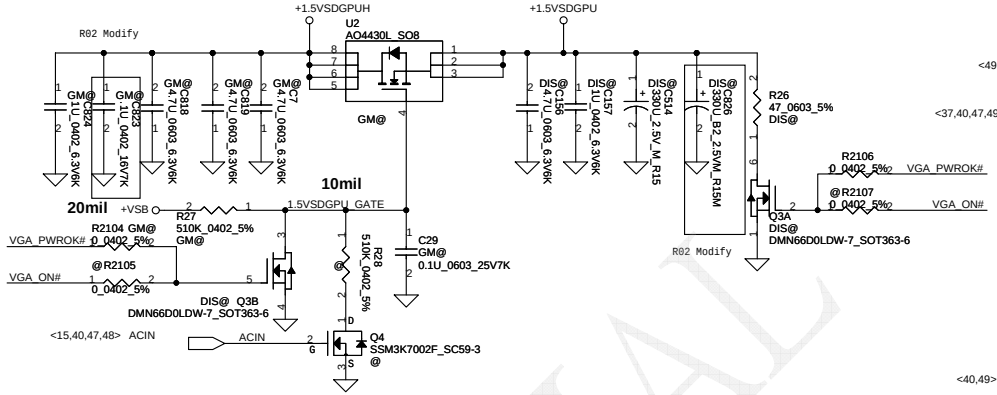
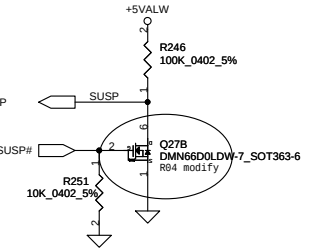
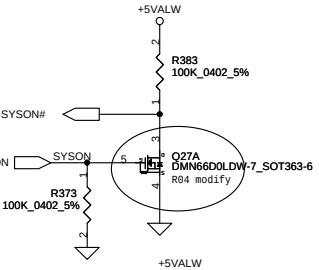
+5VALW TO +5VS

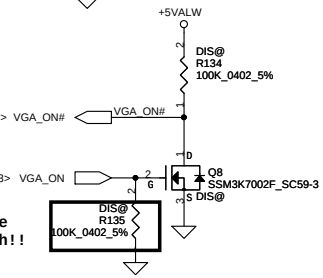


+1.5VSDGPUH to +1.5VSDGPU for GPU

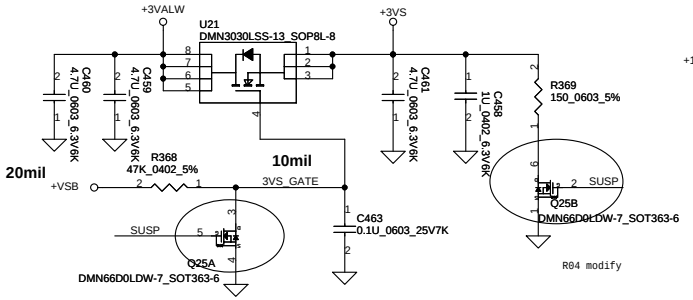


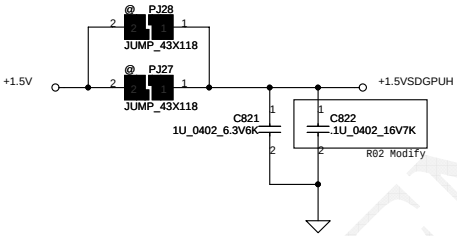


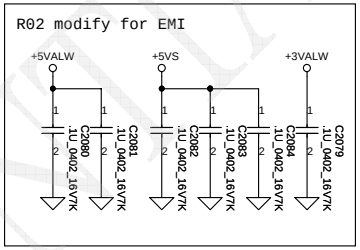




+3VALW TO +3VS

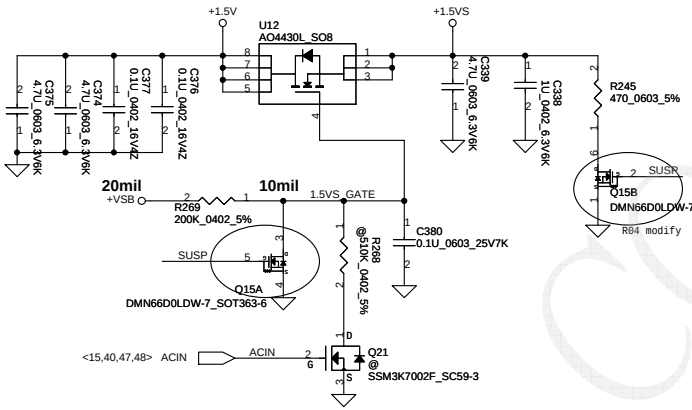




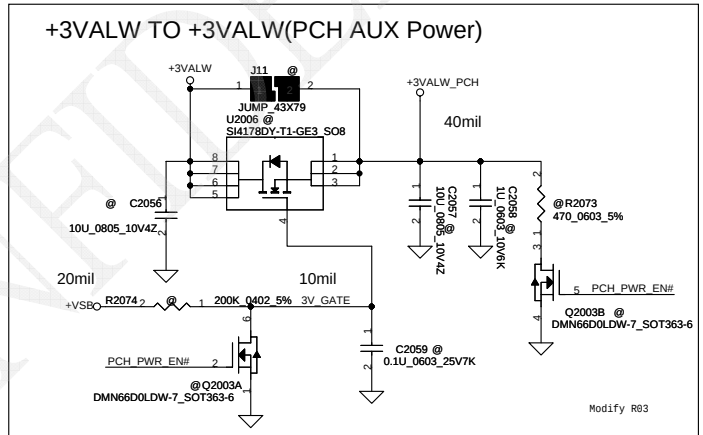


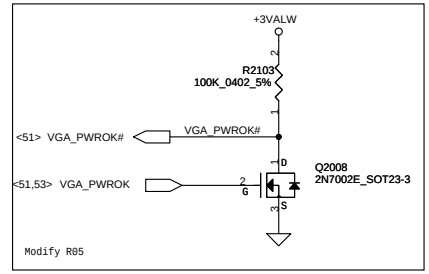
Use 100k to make sure the divided voltage is enough!!

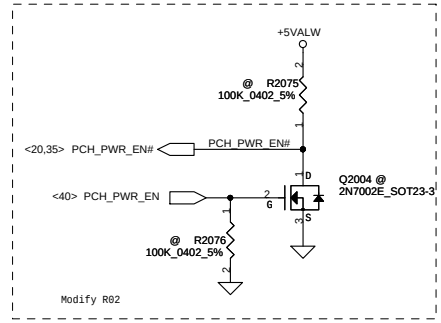
+1.5V to +1.5VS

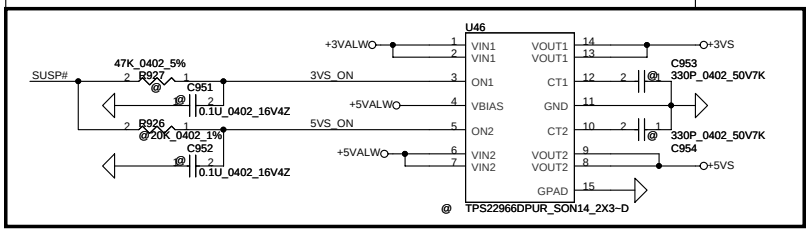


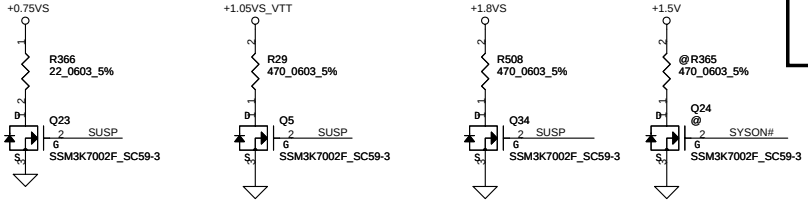
+3VALW TO +3VALW(PCH AUX Power)











Reserved

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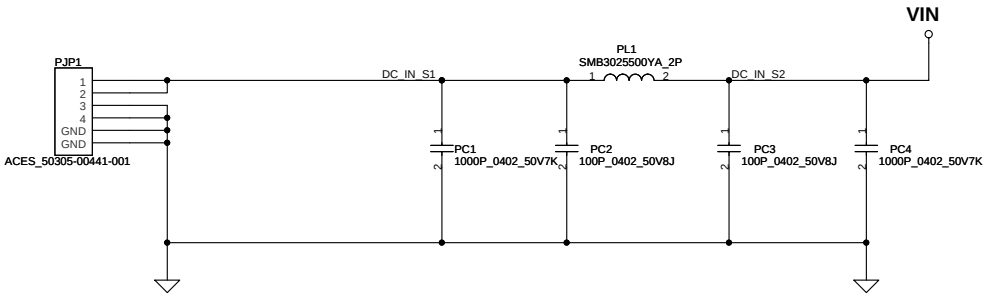

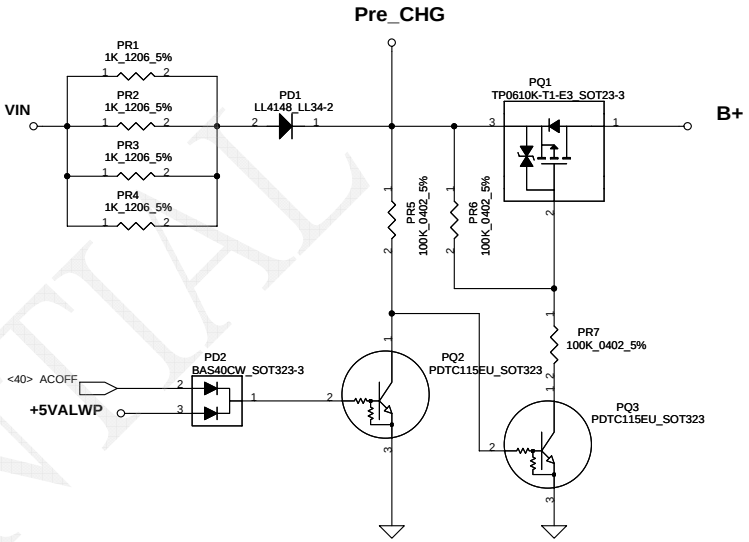

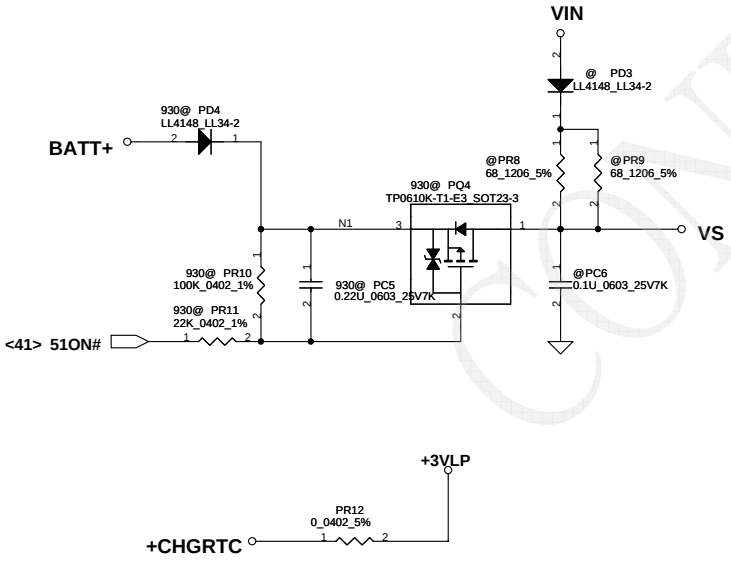

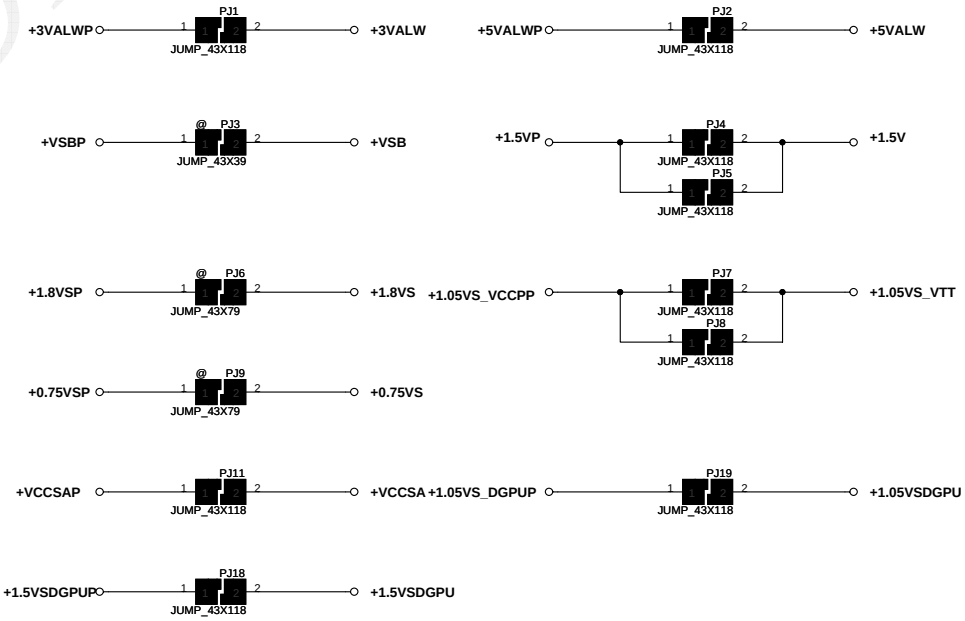

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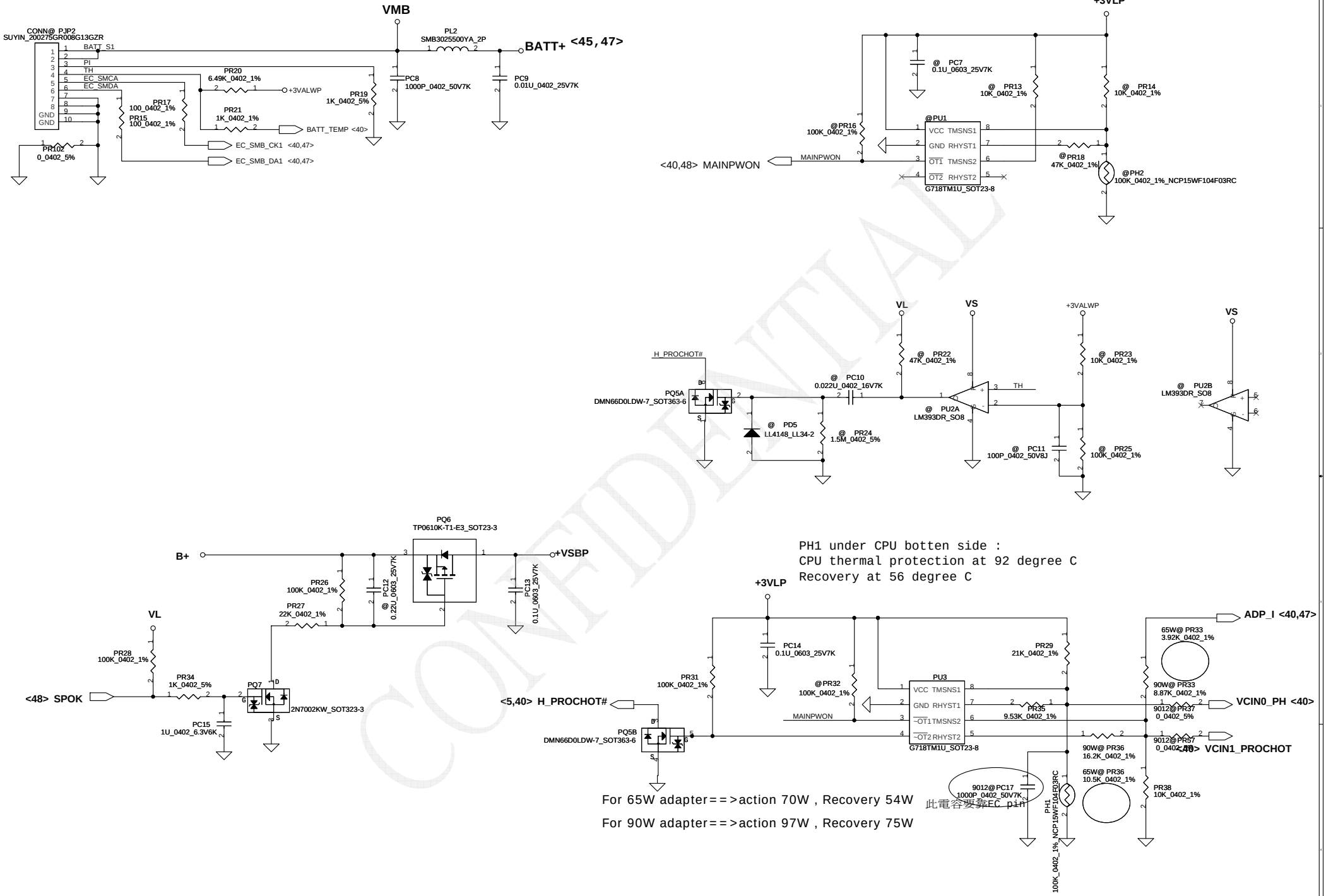

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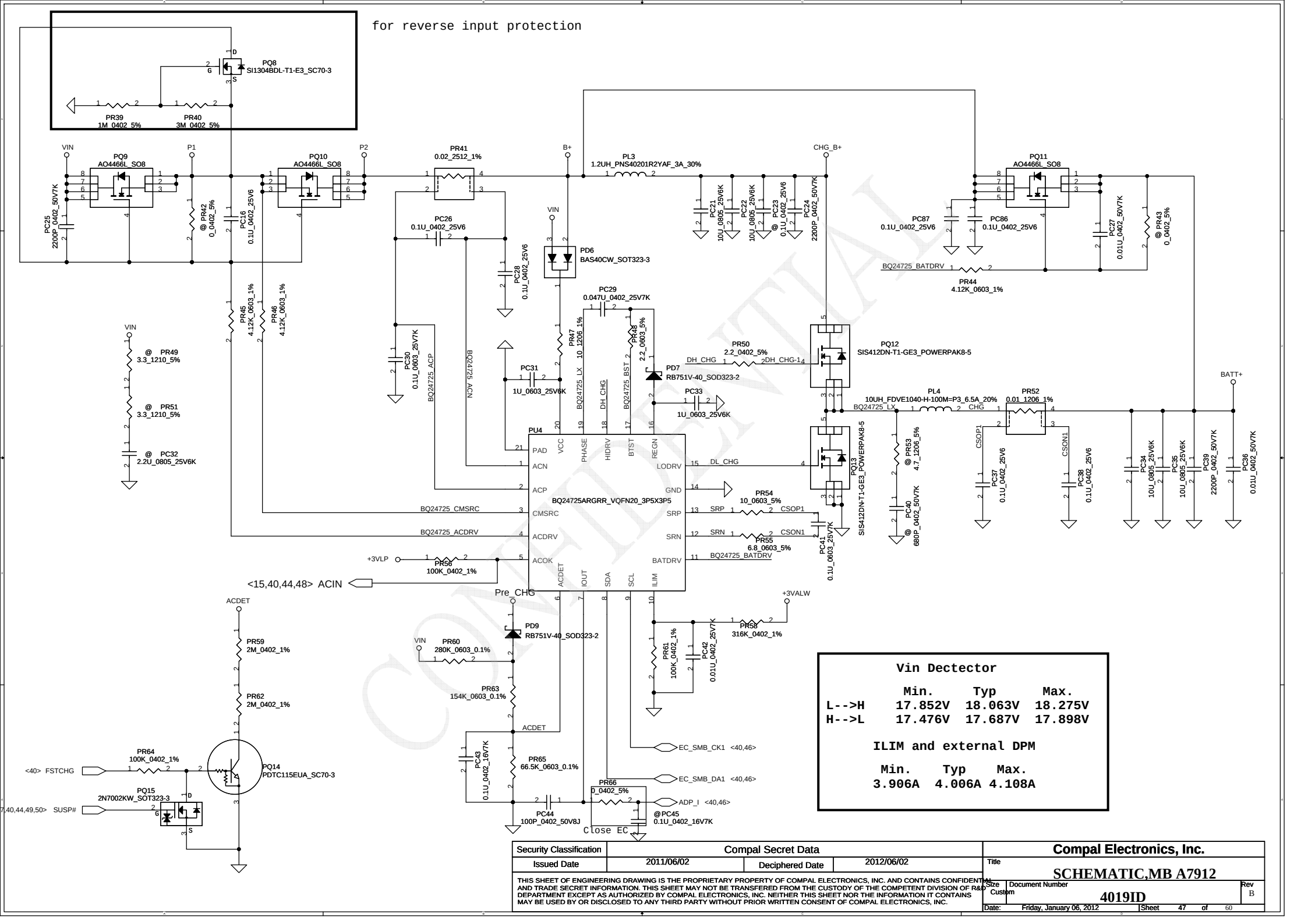

Vin Dectector

	Min.	Typ	Max.
L-->H	17.852V	18.063V	18.275V
H-->L	17.476V	17.687V	17.898V

ILIM and external DPM

Min.	Typ	Max.
3.906A	4.006A	4.108A

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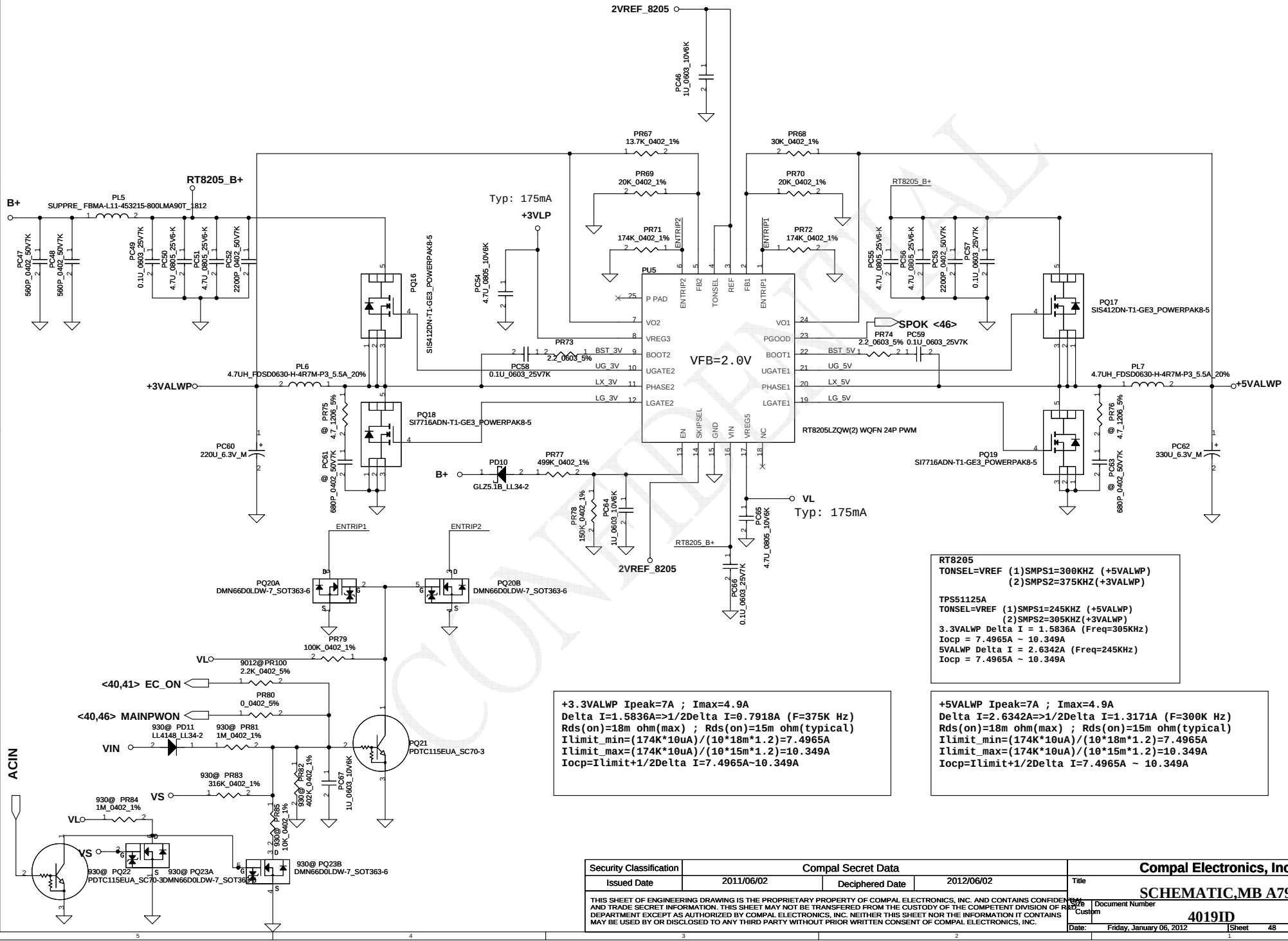
Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



RT8205
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ(+3VALWP)

TPS51125A
TONSEL=VREF (1)SMPS1=245KHZ (+5VALWP)
(2)SMPS2=305KHZ(+3VALWP)
3.3VALWP Delta I = 1.5836A (Freq=305KHz)
Iocp = 7.4965A ~ 10.349A
5VALWP Delta I = 2.6342A (Freq=245KHz)
Iocp = 7.4965A ~ 10.349A

+3.3VALWP Ipeak=7A ; Imax=4.9A
Delta I=1.5836A=>1/2Delta I=0.7918A (F=375K Hz)
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=(174K*10uA)/(10*18m*1.2)=7.4965A
Ilimit_max=(174K*10uA)/(10*15m*1.2)=10.349A
Iocp=Ilimit+1/2Delta I=7.4965A~10.349A

+5VALWP Ipeak=7A ; Imax=4.9A
Delta I=2.6342A=>1/2Delta I=1.3171A (F=300K Hz)
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=(174K*10uA)/(10*18m*1.2)=7.4965A
Ilimit_max=(174K*10uA)/(10*15m*1.2)=10.349A
Iocp=Ilimit+1/2Delta I=7.4965A ~ 10.349A

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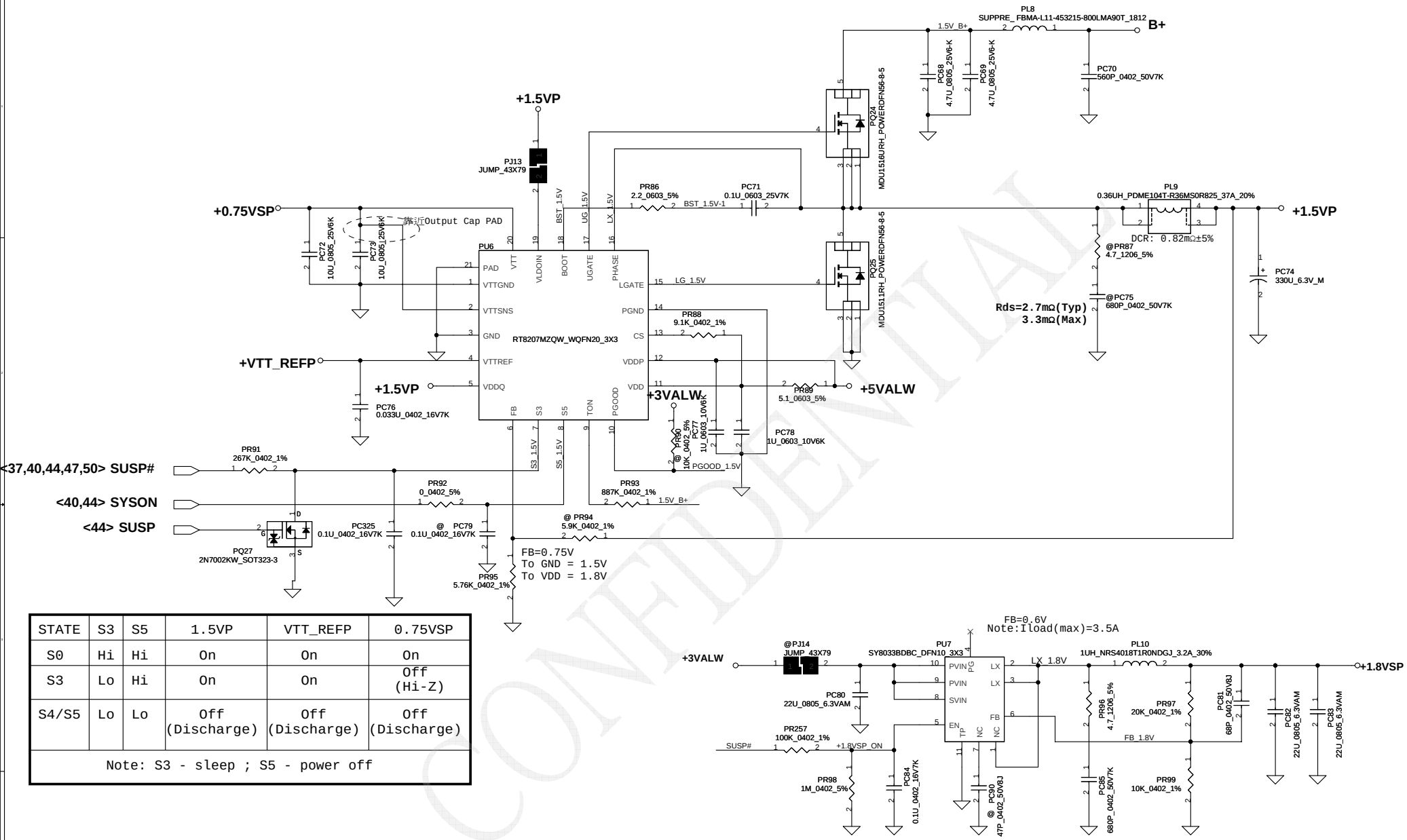

STATE	S3	S5	1.5VP	VTT_REFP	0.75VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)
Note: S3 - sleep ; S5 - power off					

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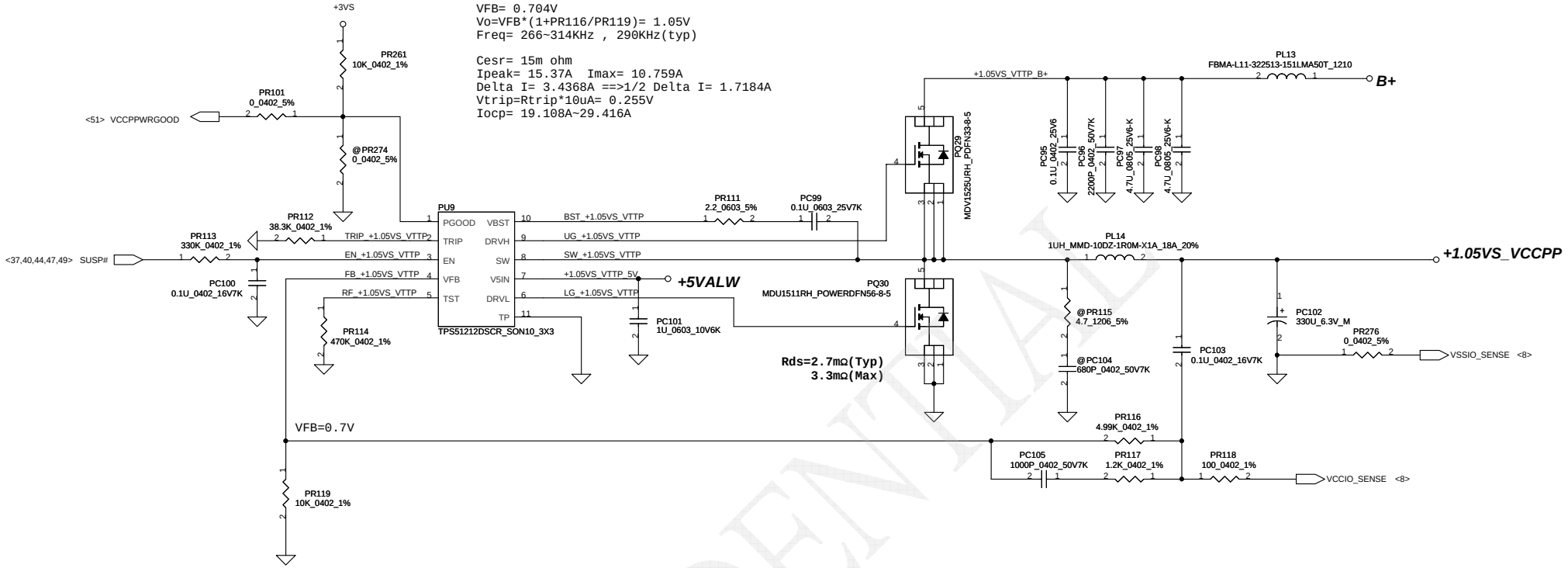

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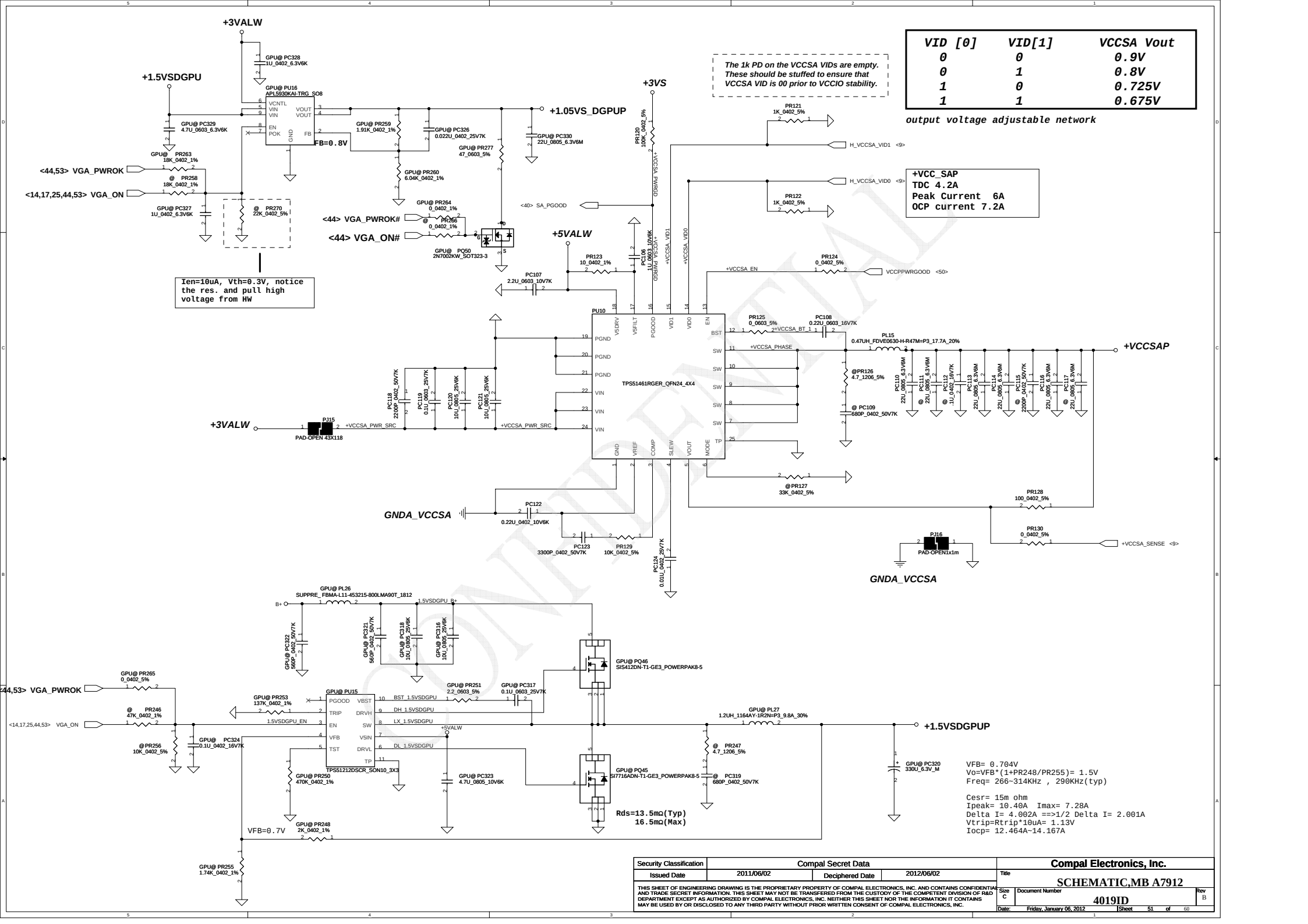

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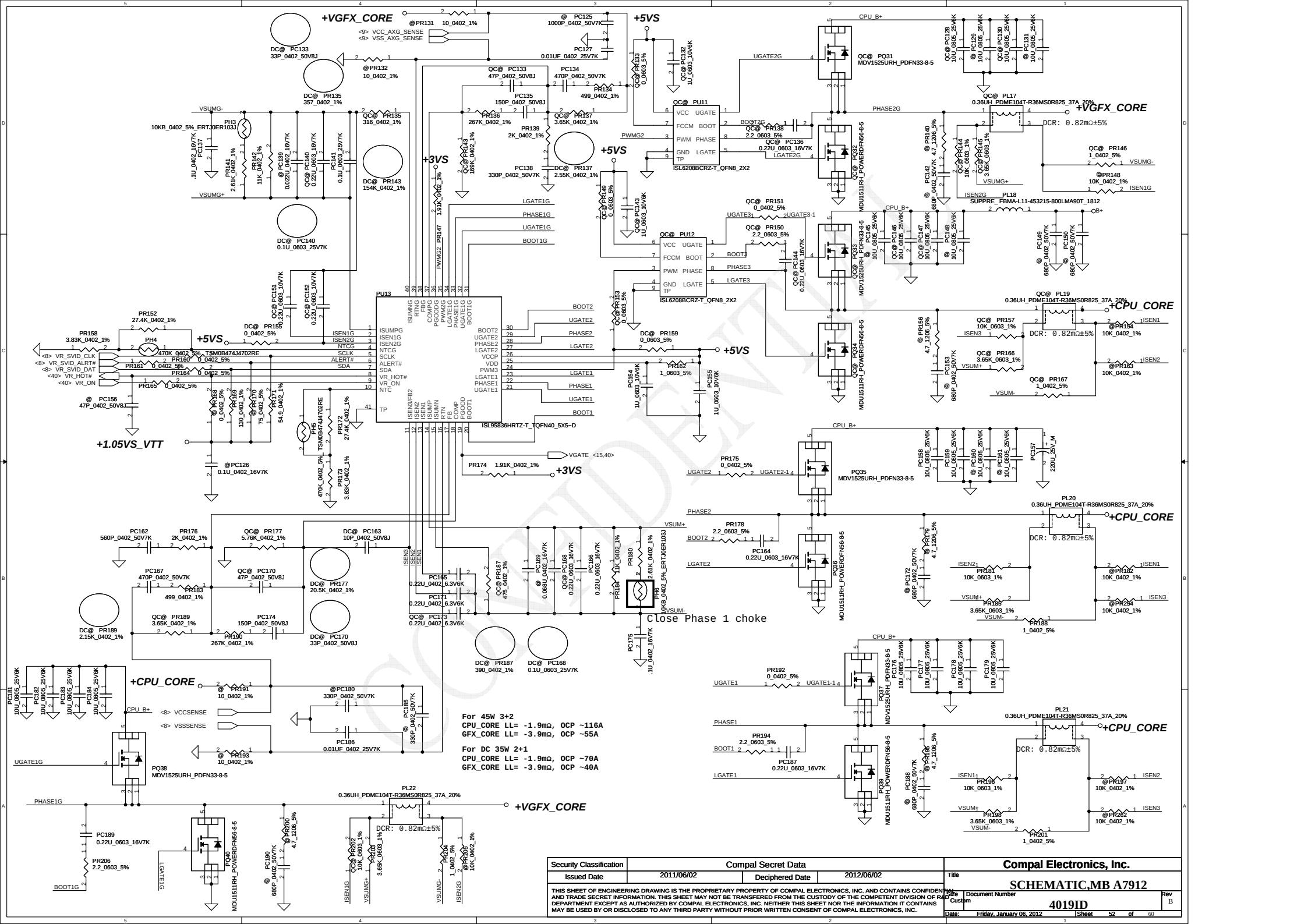
+VGFX_CORE
+5VS
+3VS
+1.05VS_VTT
+CPU_CORE
ISL6208BCRZ-T_QFN8_2X2
ISL95836HRTZ-T_TQFN40_5X5~D
MDV1525URH_PDFN33-8-5
MDU1511RH_POWERDFN56-8-5
Close Phase 1 choke
For 45W 3+2
CPU_CORE LL= -1.9mΩ, OCP ~116A
GFX_CORE LL= -3.9mΩ, OCP ~55A
For DC 35W 2+1
CPU_CORE LL= -1.9mΩ, OCP ~70A
GFX_CORE LL= -3.9mΩ, OCP ~40A
DCR: 0.82mΩ±5%
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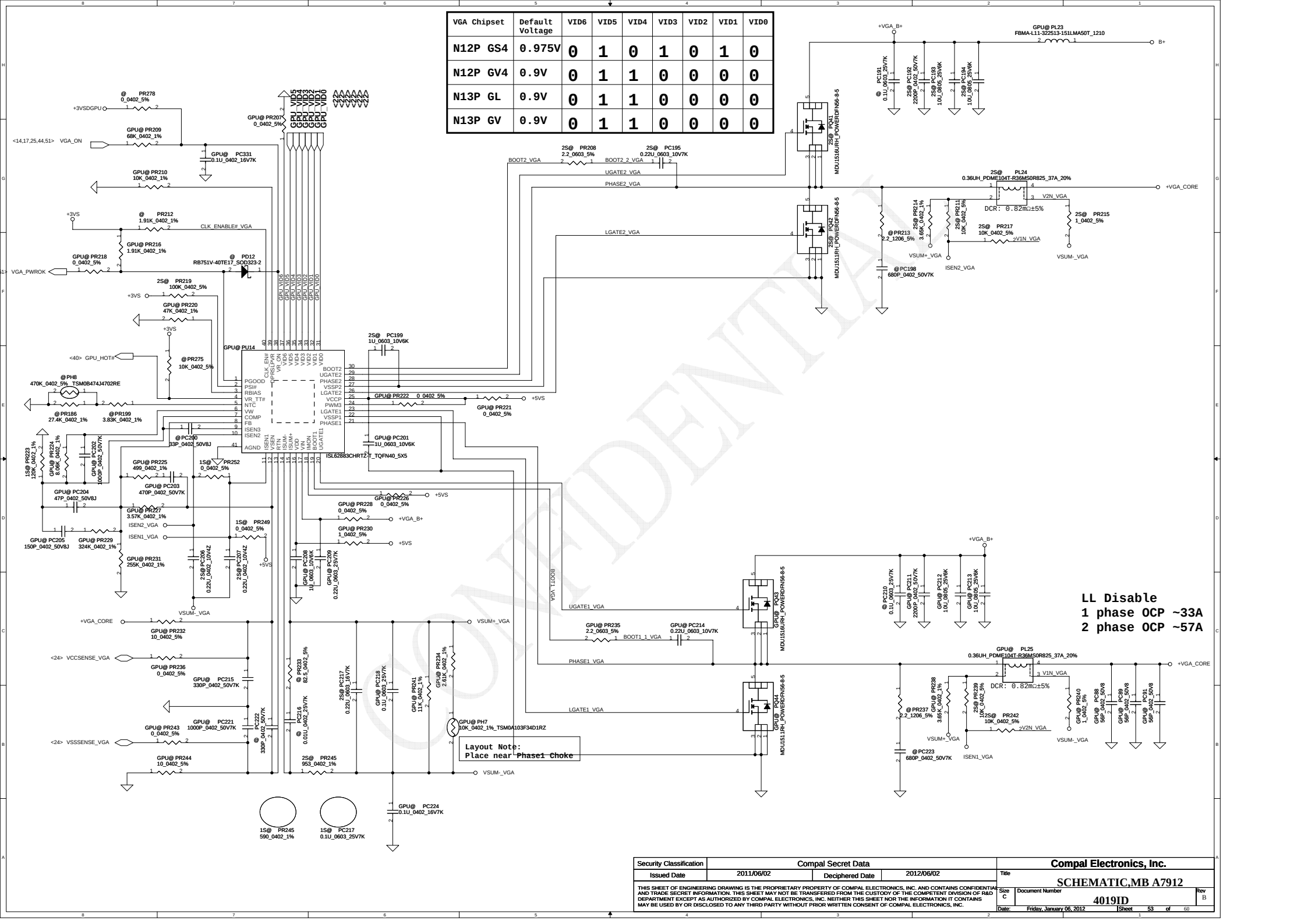
VGA Chipset	Default Voltage	VID6	VID5	VID4	VID3	VID2	VID1	VID0
N12P GS4	0.975V	0	1	0	1	0	1	0
N12P GV4	0.9V	0	1	1	0	0	0	0
N13P GL	0.9V	0	1	1	0	0	0	0
N13P GV	0.9V	0	1	1	0	0	0	0



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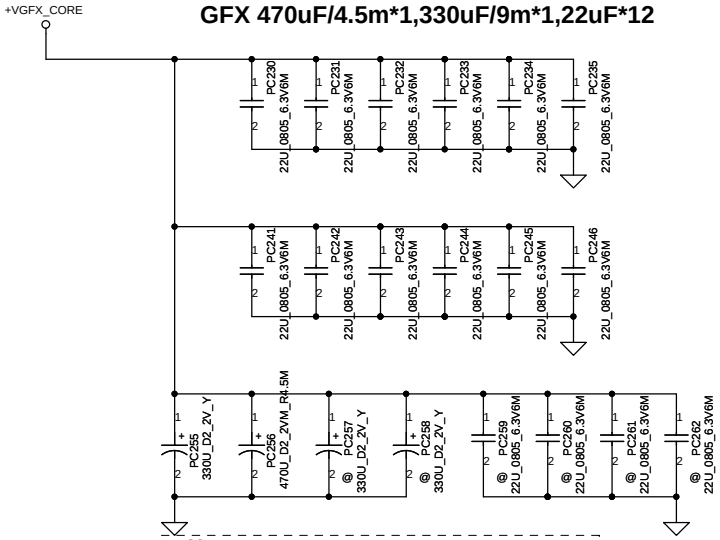
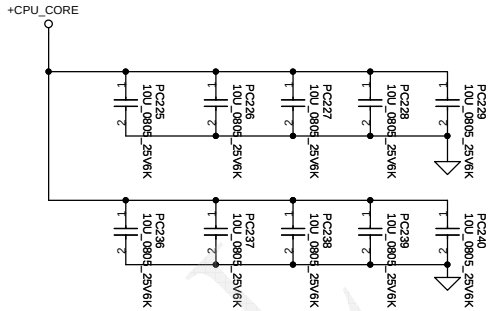
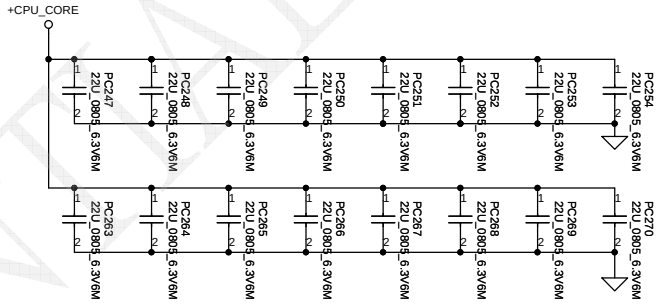
PWR Rule
CPU 330uF/9m *5,22uF *16,10uF*10
GFX 470uF/4.5m*1,330uF/9m*1,22uF*12

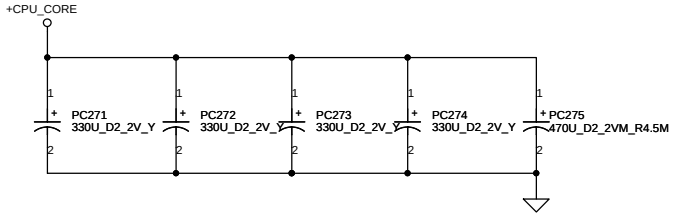


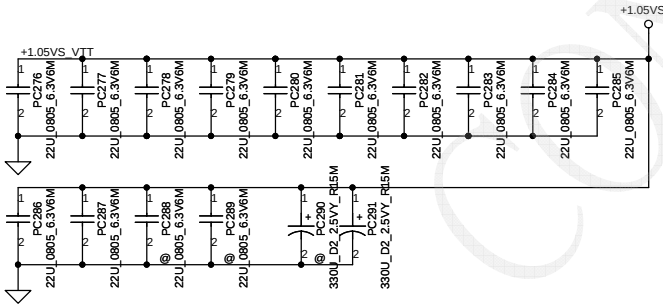
Vaxg

- **Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,**
- **VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed**









INTEL Recommend
3*330uF(1 in other page),12*22uF, 5 no stuff
from PDDG 1.0

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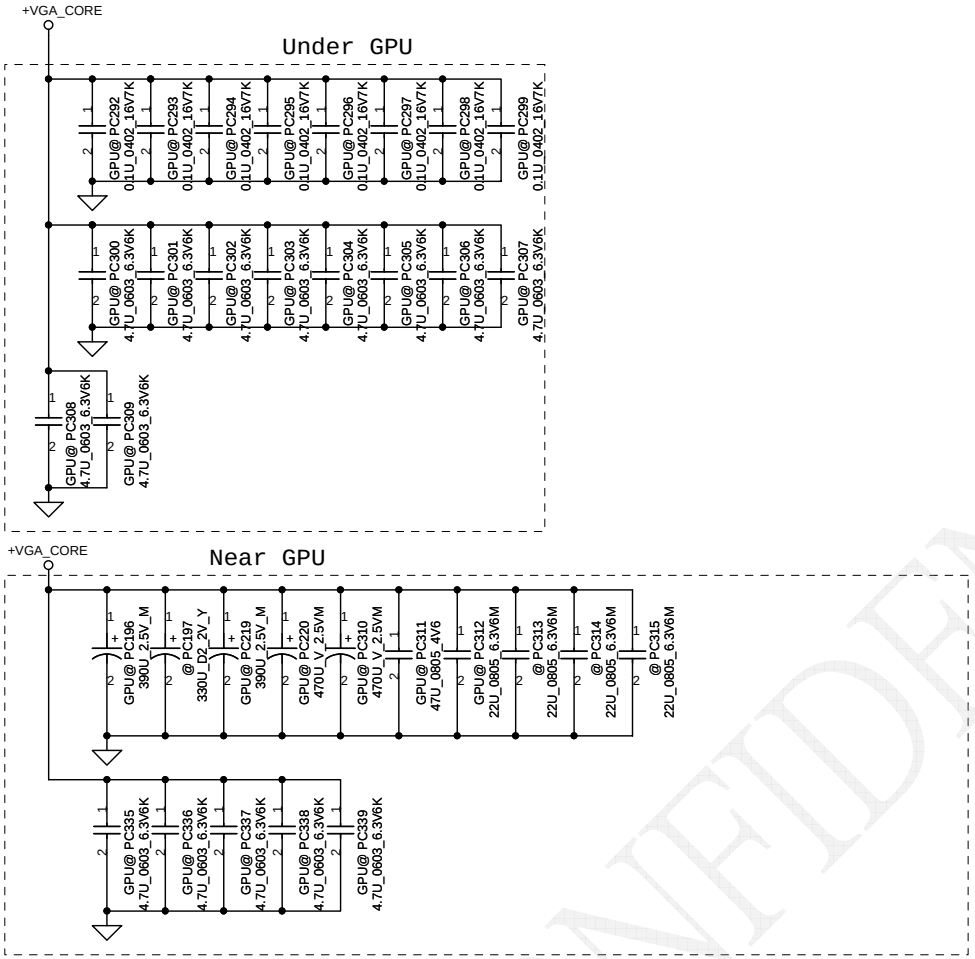

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	S3 sequence @ DC	Meet Intel sequence SPEC		49	Change RP91 to 267K	2011 1208	DVT
2	1.5VSDGPU lose	Improve FB pin anit-noise		51	Change RP248 to 2K, PR255 to 1.74K, PR253 to 137K	2011 1208	DVT
3	Cut-in SMT memo			52	Add PC182, PC184	2011 1208	DVT
4		Standard design			Change PR138, PR150, PR178, PR194, RP205 , PR235 to 2.2		
5	Vth has risk			51	Change PU16 from G971 to APL5930	2011 1212	DVT
6		Enable select		51	Add PR266	2011 1217	DVT
7	Cut-in EMI solution			53	Add PC88, PC89, PC91	2011 1221	DVT
8							
9							
10							
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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
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2							
3							
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							
17							

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P.40.13		9/7	EC	Change th HDA_SDO to ME_EN		0.2
2	P.40		9/7	HW	Add R2085 ,change the EC_ACIN pull high to +3VLP		0.2
3	P.37		9/7	HW	Add fl1009 USB3.0 TX coupling capacitor (c2060,c2061)		0.2
4	P.38.39.40		9/7	HW	~~Add USB chargaer schematic(C2060.C2061.R2077~R2084,R2065~R2072)~~		0.2
5	P.22.40		9/7	HW	Follow ABO request,add ADPS function(Q2005),R2086.R2087)		0.2
6	P.20		9/7	HW	~~Add +5VALW TO +5VALW_PCH schematic(Q2006.C2062.R2088)~~		0.2
7	P.44		9/7	HW	~~Add +3VALW TO +3VALW_PCH schematic(U2006,R2073~R2076,C2056~C2059,Q2003,Q2004)~~		0.2
8	P.43		9/7	HW	For FSOV spec,Chang R714,R716 from 75ohm to 47ohm.		0.2
9	P.13		9/7	HW	For WIN8,Change R681.R651.R684.R652 to 33ohm		0.2
10	P.44		9/7	HW	Delete C817,Change C826 from D2 size to B2 size		0.2
11	P.17.37		9/7	HW	Follow chief river common design, please chang Mini-Card 2(port 11) to port 9		0.2
12	P.38		9/7	HW	Delete +1.5V to +1.05V_V128 Transfer(U2002.R2002.R2003.R2005.C2002.C2003.C2005.R2008)		0.2
13	P.38		9/7	HW	Delete USB3.0 EEPROM(U2004.R2035.R2034.C2039)		0.2
14	P.37		9/7	HW	Reserve Mini-Card 2		0.2
15	P.19		9/7	HW	F2 flick issue on projector P5202 D-sub Add C2063.C2064		0.2
16	P.22.40		9/8	HW	Change VGA GPIO12 of dGPU connection to EC controlled for the power limited usage Add EC pin 107-->GPU_ACIN		0.2
17	P41		9/14	HW	Add SW5.SW6 for EG project.		0.2
18	P27.30		9/14	HW	Swap MDC37 and MDC38 Swap MDA13 and MDA14		0.2
19	P06.11.17.35. P39.40.42		9/14	HW	For ESD request Add C2065~C2075		0.2
20	P16		9/16	HW	For HDMI PCH_DPB_HPD noise Add C2076		0.2
21	P31		9/16	HW	For LVDS power sequence Change R5 from 300 to 200 ohm Change R2 from 1k to 10k ohm change C2 from 0.047uF to 1uF		0.2
22	P18		9/16	HW	Delete PCH test ponit(T31~T46,T49~T61,T63~T65)		0.2
23	P21,40		9/19	HW	Change Q22,Q26 from SB000008J10 to SB000009080		0.2
24	P14,22,35,38		9/19	HW	For Crystal Change Y2 ,Y4 from SJ10000DJ00 to SJ10000E800 Change Y1000 from SJ10000DK00 to SJ100009700 Change C630,C631,C2019,C2028,C1008,C1009 to 10pF Change C681,C679 to 15pF		0.2

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
25	P.44		9/20	EMI	For EMI request (Add C2079~C2084)		0.2
26	P.36		9/20	HW	For SD3.0 issue (Add R2088.R2089)		0.2
27	P.20		10/17	HW	Add +5VALW TO +5VALW_PCH schematic(Q2006.C2062.R2090)		0.3
28	P.44		10/17	HW	Add +3VALW TO +3VALW_PCH schematic(U2006,R2073~R2076,C2056~C2059,Q2003,Q2004)		0.3
29	P.40		10/17	HW	Board ID error. Add R353.		0.3
30	P.40		10/17	HW	Board ID 0.3. Change R353 to 18K		0.3
31	P.17,39		10/17	HW	Follow Intel's suggestion; Change USB3.0 from port 2 to port 1 Change USB2.0 from port 0,1 to port 2,9		0.3
32	P.18		10/18	HW	Support eDP GPIO71-->0 (eDP) GPIO71-->1 (LVDS)		0.3
33	P.13.40		10/25	HW	Co_lay NPCE885N Delete U38,C722,R690,R695,C727 Add C2085,R2091~R2096		0.3

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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
43	P.41		11/16	ME		Delete SW5,SW6, Pop SW2,SW3	0.4
44	P.05		11/16	HW	BUF_CPU_RST# noise	Add C2090	0.4
45	P.35		11/17	HW	LAN SPROM on Chip	De-pop U31,R537 Pop R538	0.4
46	P.36		11/17	EMI		Change C478 to 10P_50V	0.4
47	P.13		11/17	HW	RTC issue	Change C682,C686 to 15P	0.4
48	P.31,32,41		11/17	ESD		De-pop D3,D4,D17,D18,D15 Pop D24,D36	0.4
49	P.40		11/17	HW		De-pop R891,R893	0.4
50	P.24		11/21	HW		N13P_GS Change strap2 to PD 15k Change strap4 to PD 10k	0.4
51	P.13		11/21	HW		Chip Select Change R651,R2049 to 0ohm	0.4
52	P.13,40		11/21	HW		Delete NPCE885N (R2091.R2092.R2094.R2095.R2096,R698, R699,R692,C2085)	0.4
53	P.45		11/22	HW		Change +1.05VSDGPU JUMP size PJ19 change to 43x118	0.4
55	P.35,36		11/23	HW		Card Reader Change R216 to 22 ohm Change R2088 to 47ohm Change R2089 to 22 ohm Add C2091~C2093 Change R525,R536,R537,R538 to 1k	0.4
56	P.13		11/23	HW		Delete R2093,R2049,R651(0ohm)	0.4
57	P.13		11/23	HW		Change N13P-GS to SA000051880 Change U33 to SA00005AG00	0.4
58	P.35, P36		11/23	HW		Del C2093, R222, R2089, net(CR_CLK_XD_RY_BY#_23) Add R2101, C2094	0.4
59	P.36		11/24	HW		ADD R2102, C2096 for EMI ISSUE	0.4