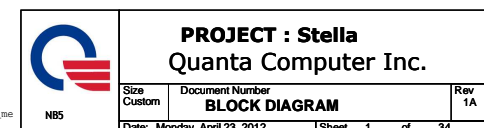
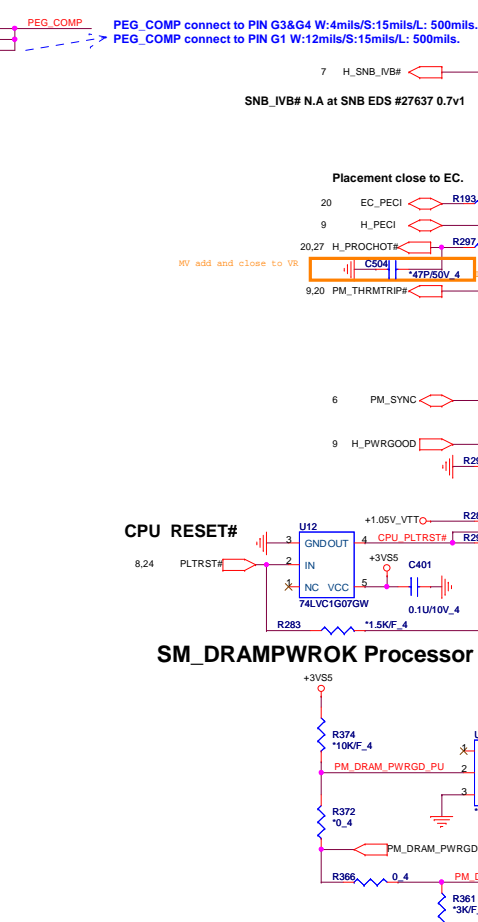
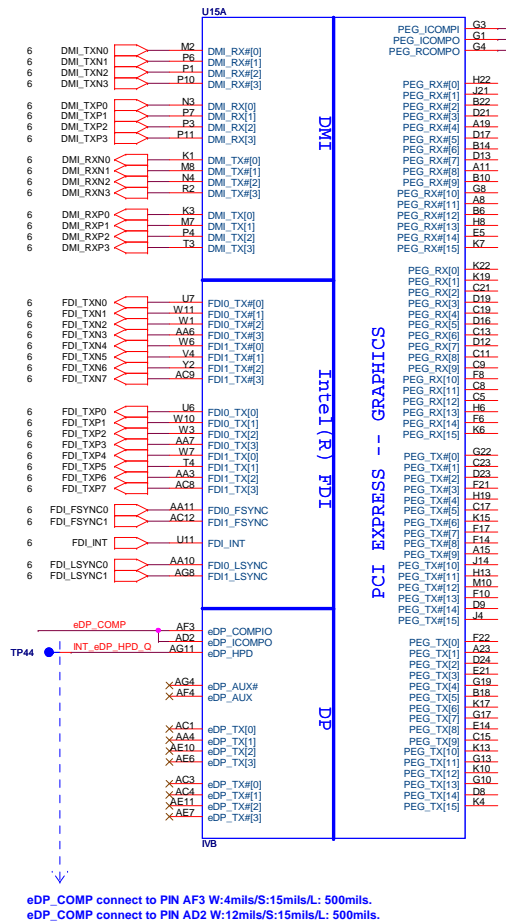
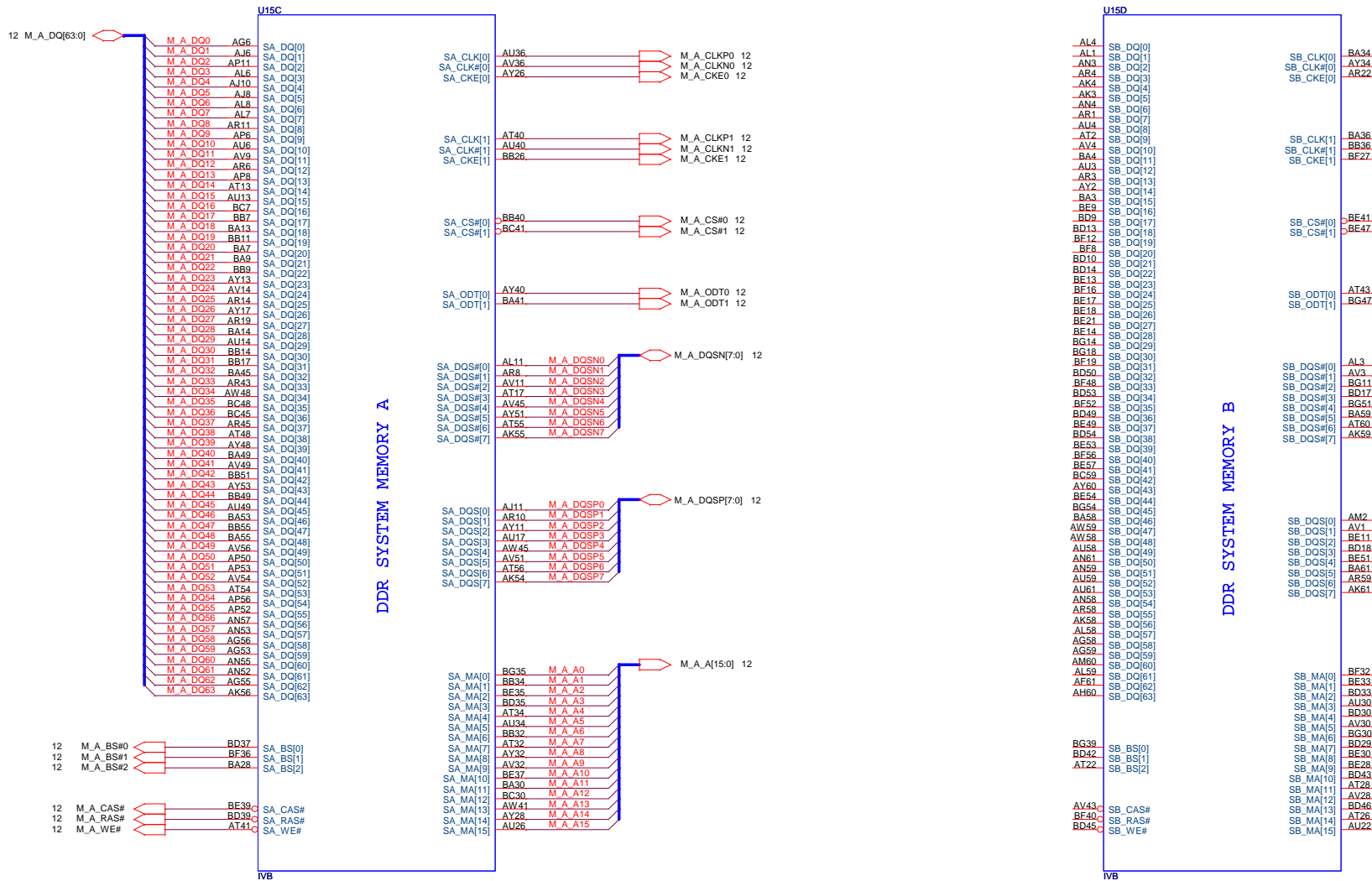


01



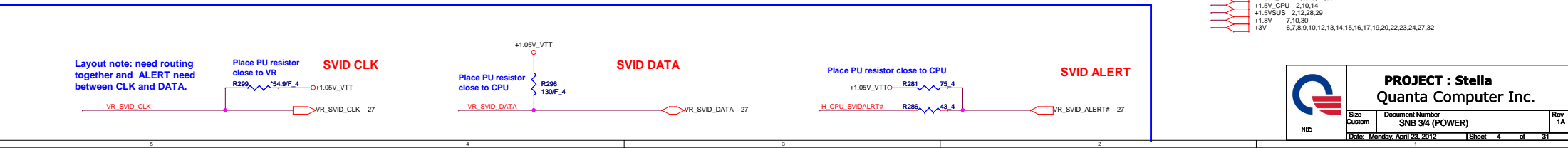
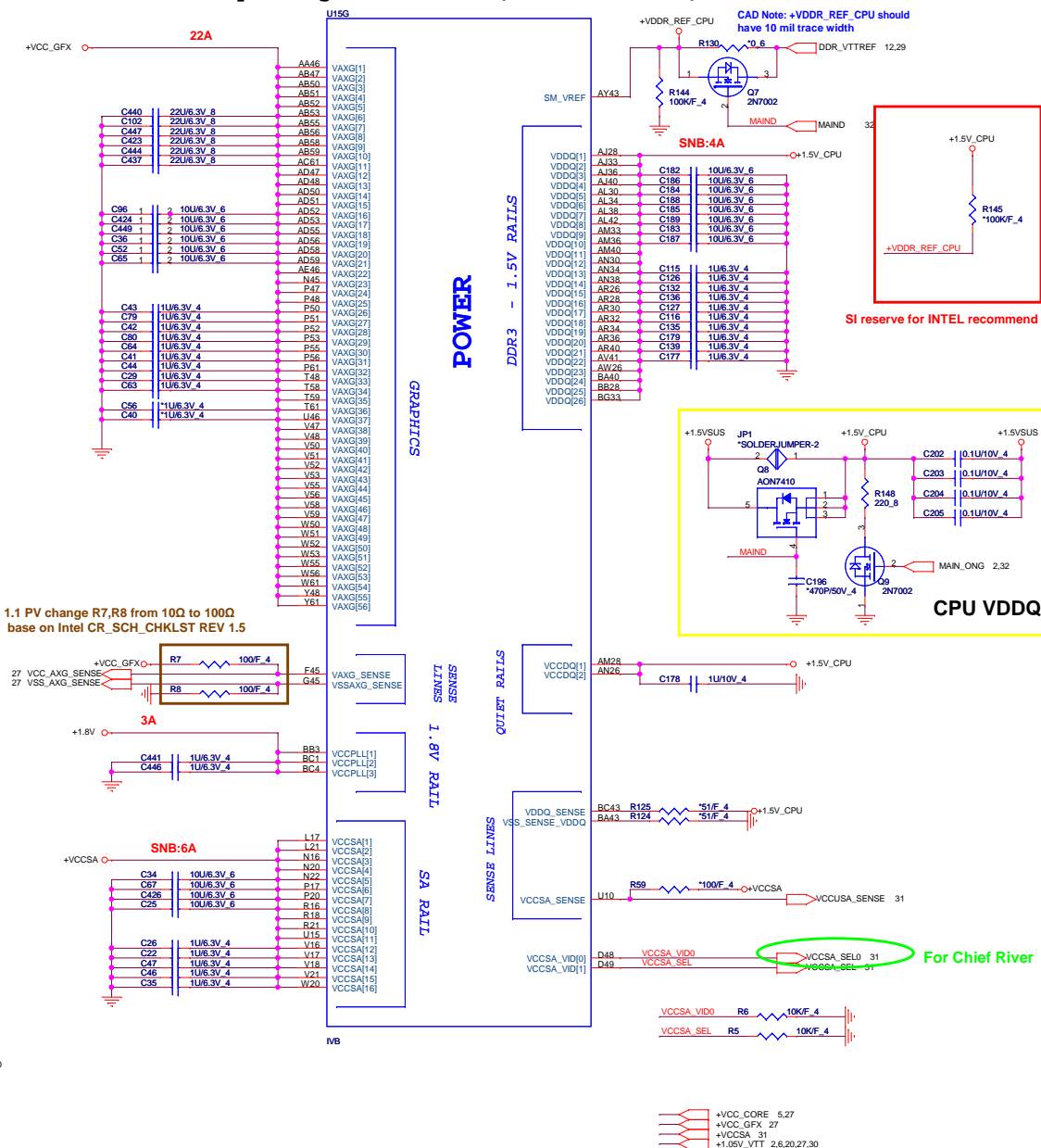
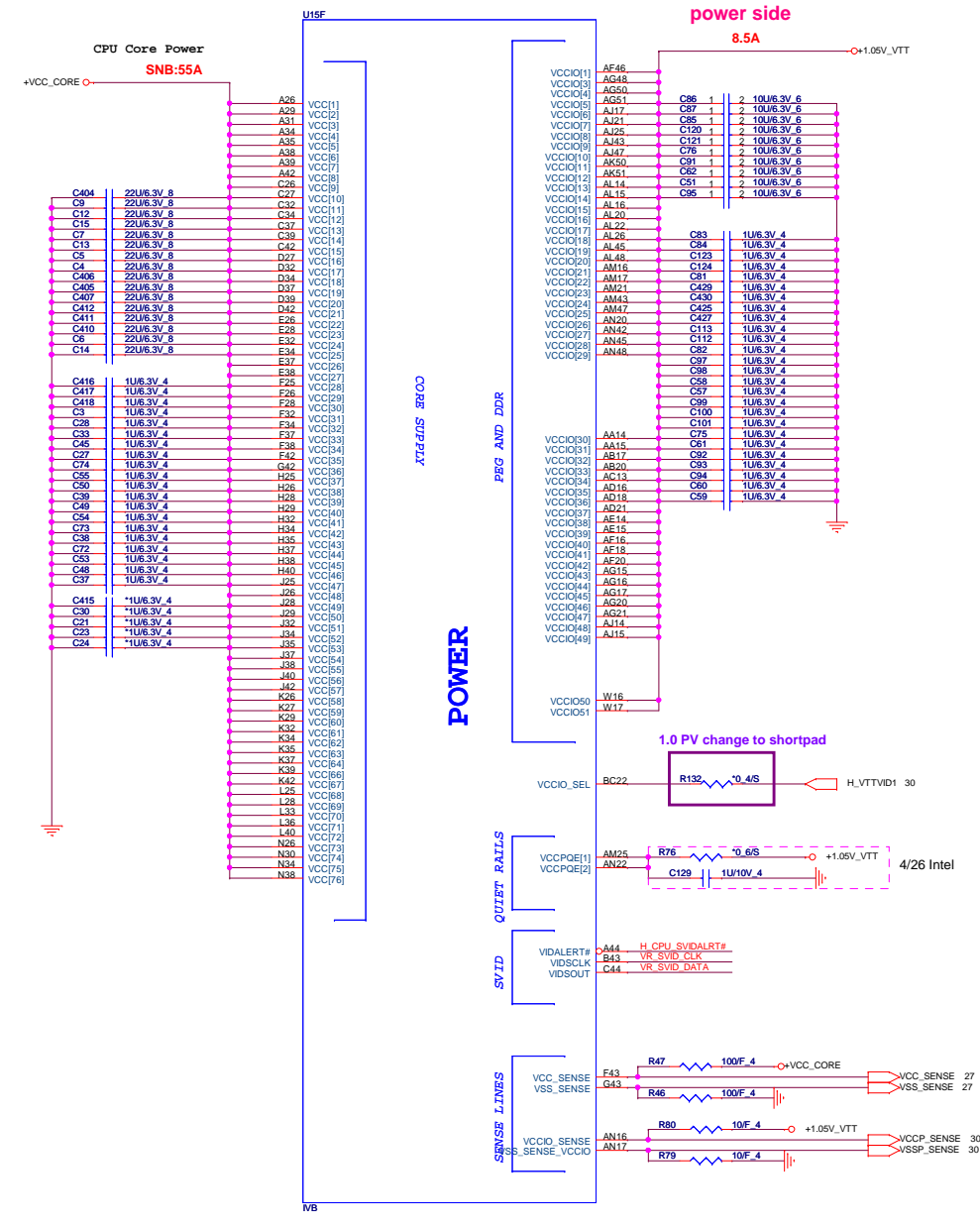


Ivy Bridge Processor (DDR3)

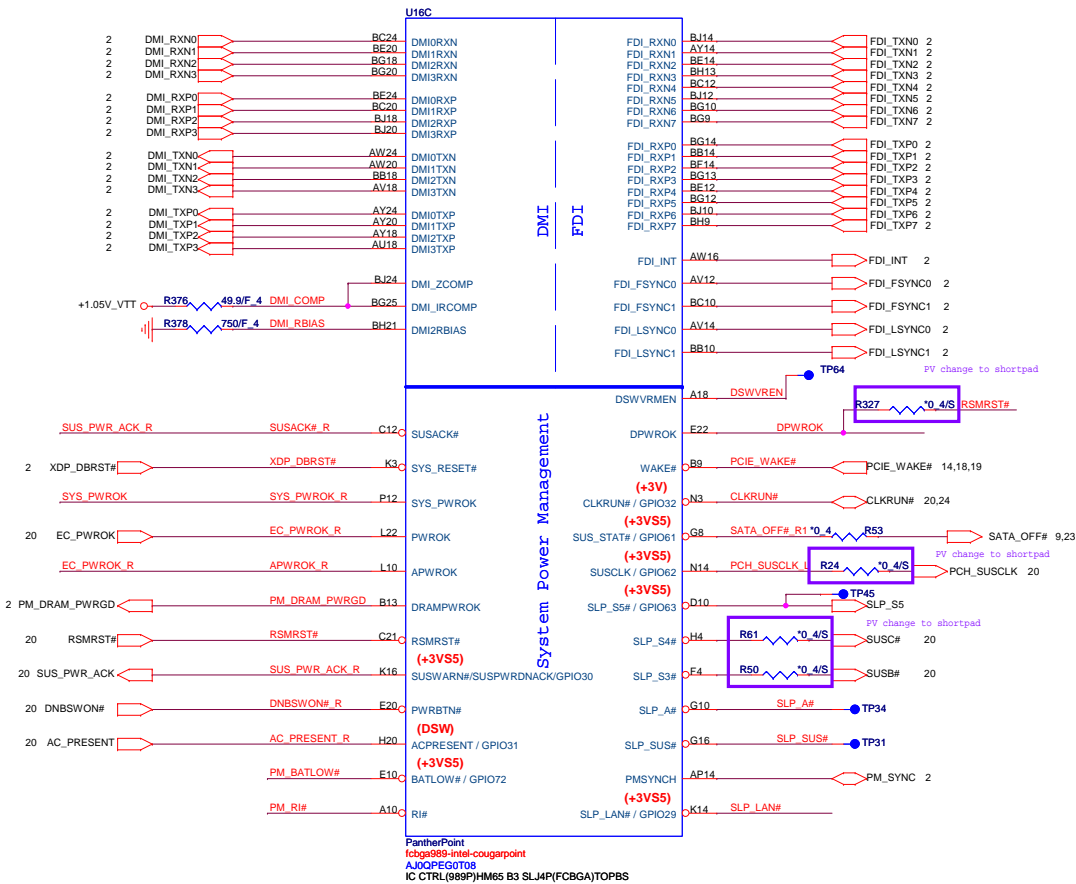


Ivy Bridge Processor (POWER)

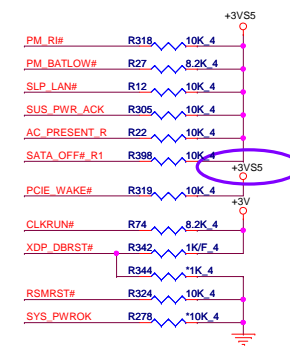
Ivy Bridge Processor (GRAPHIC POWER)



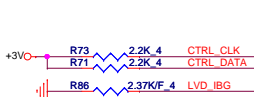
Panther Point (DMI, FDI, PM)



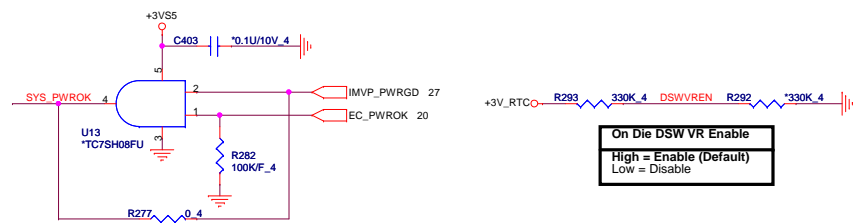
PCH Pull-high/low(CLG)



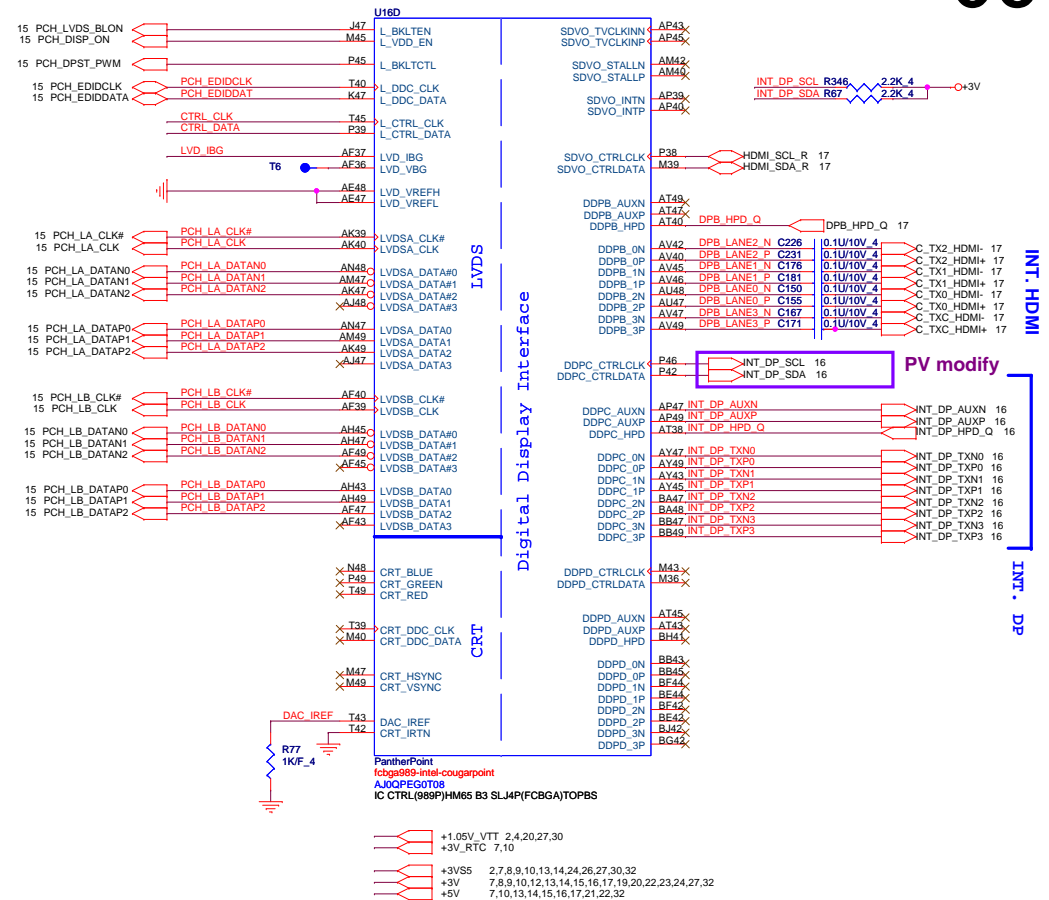
INT LVDS & CRT disable (DIS only remove)



System PWR_OK(CLG)

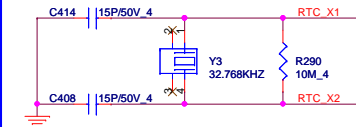


Panther Point (LVDS, DDI)

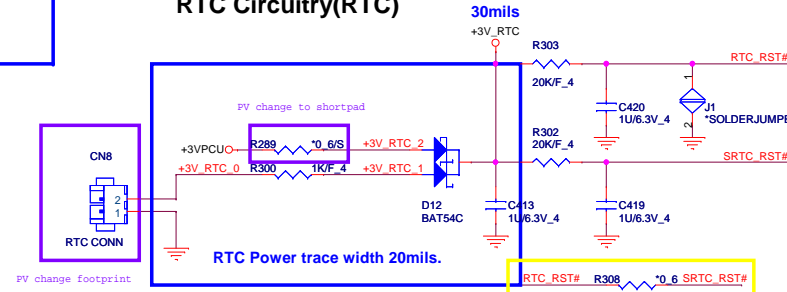


Panther Point (HDA,JTAG,SATA)

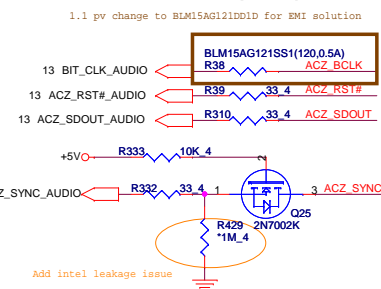
RTC Clock 32.768KHz



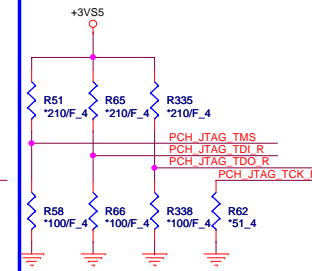
RTC Circuitry(RTC)



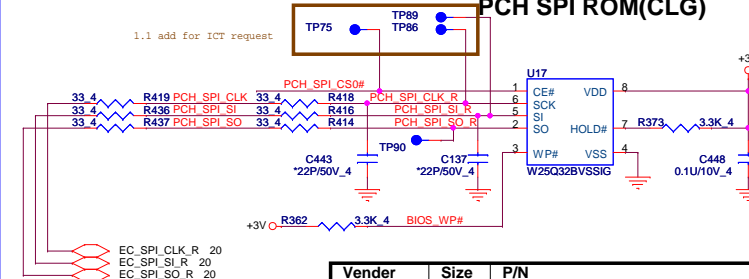
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM (CLG)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031



PROJECT : Stella
Quanta Computer Inc.

Size Custom	Document Number PCH 2/6 (SATA/HDA/SPI)	Rev 1
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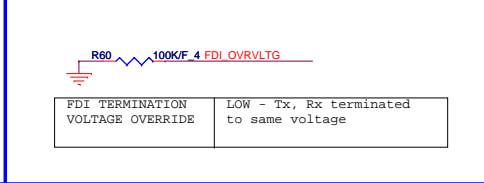
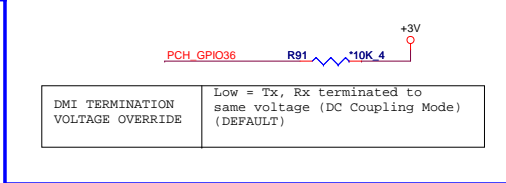
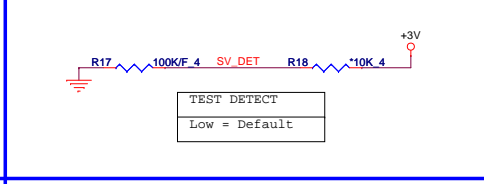
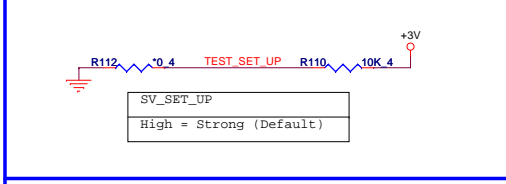
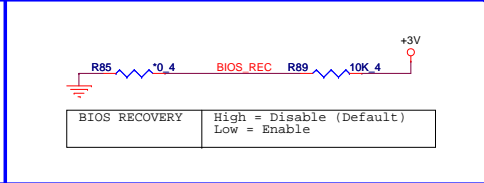
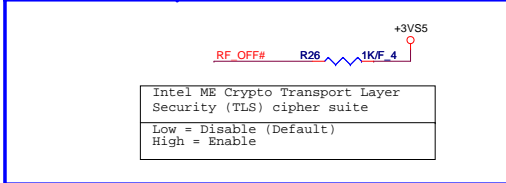
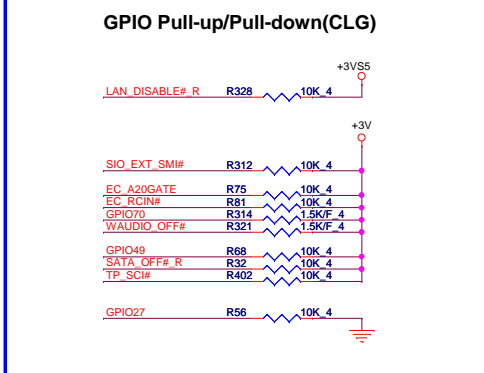
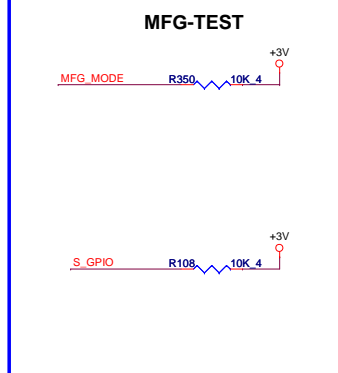
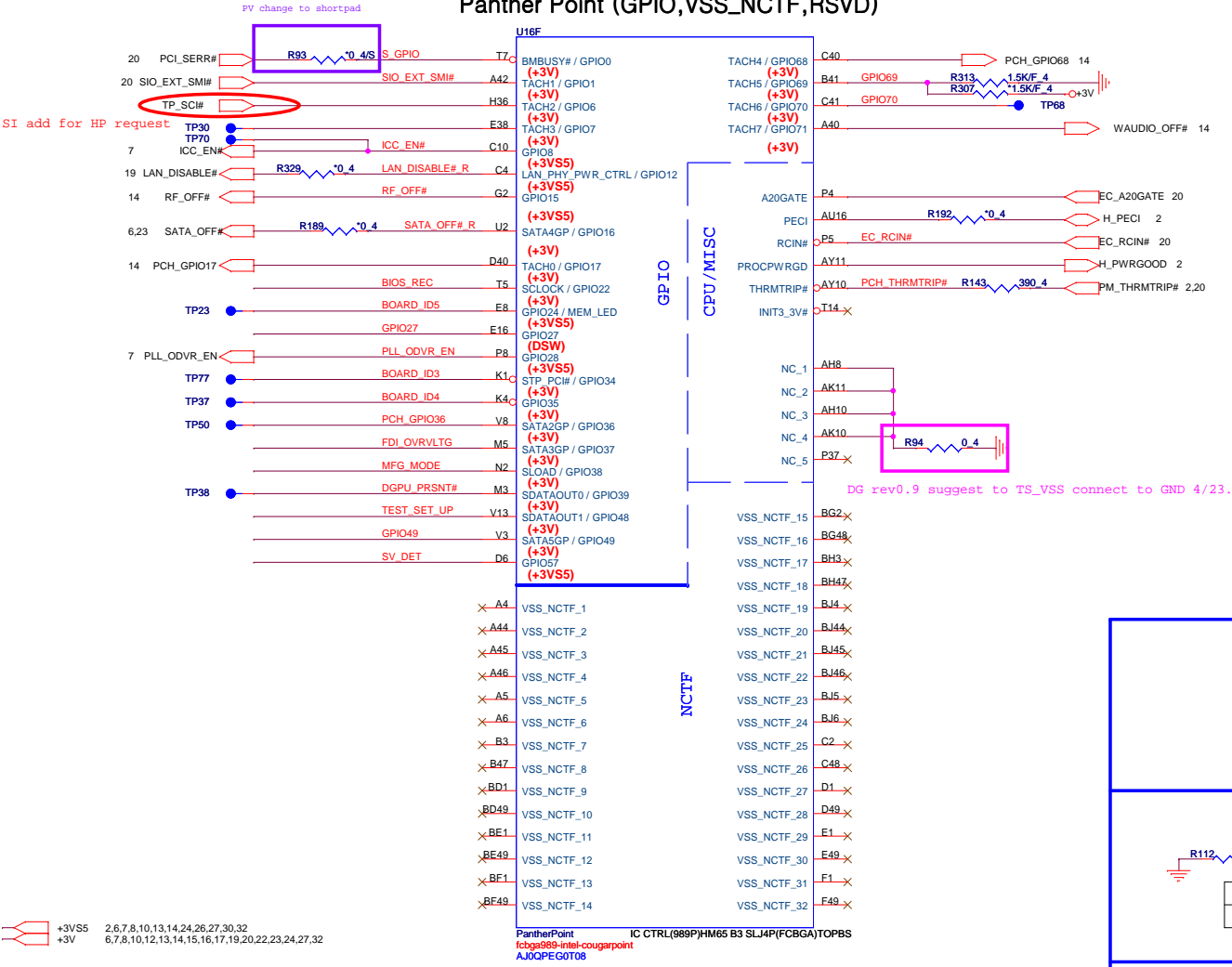
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR	Different from Calpella No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode							
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)							
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up							
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)							
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr><tr><td>0</td><td>0</td><td>SPI LPC</td></tr></table>	GNT1#	GNT0#	Boot Location	0	0	SPI LPC	
GNT1#	GNT0#	Boot Location								
0	0	SPI LPC								
GPIO19	Different from Calpella Boot BIOS Selection 0 [bit-0]	PWROK								
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN						
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)							
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm							
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V							
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)							
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)							
GPIO28	Different from Calpella On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)							
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable							



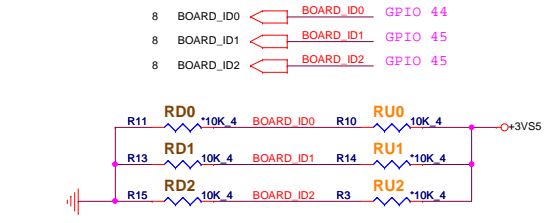
Panther Point (GPIO,VSS_NCTF,RSVD)

Clock Gen Power OK (CLG)

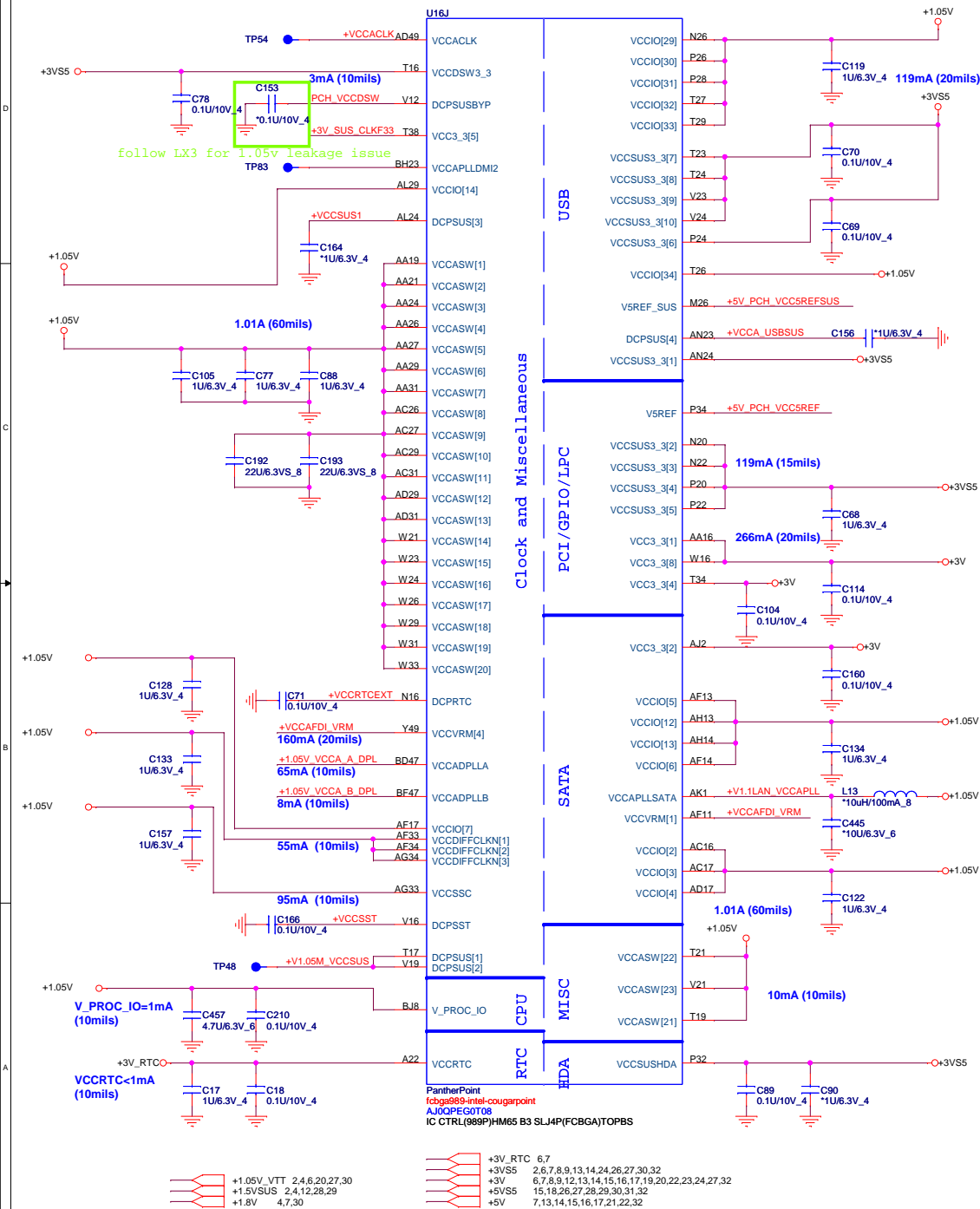


BOARD ID SETTING

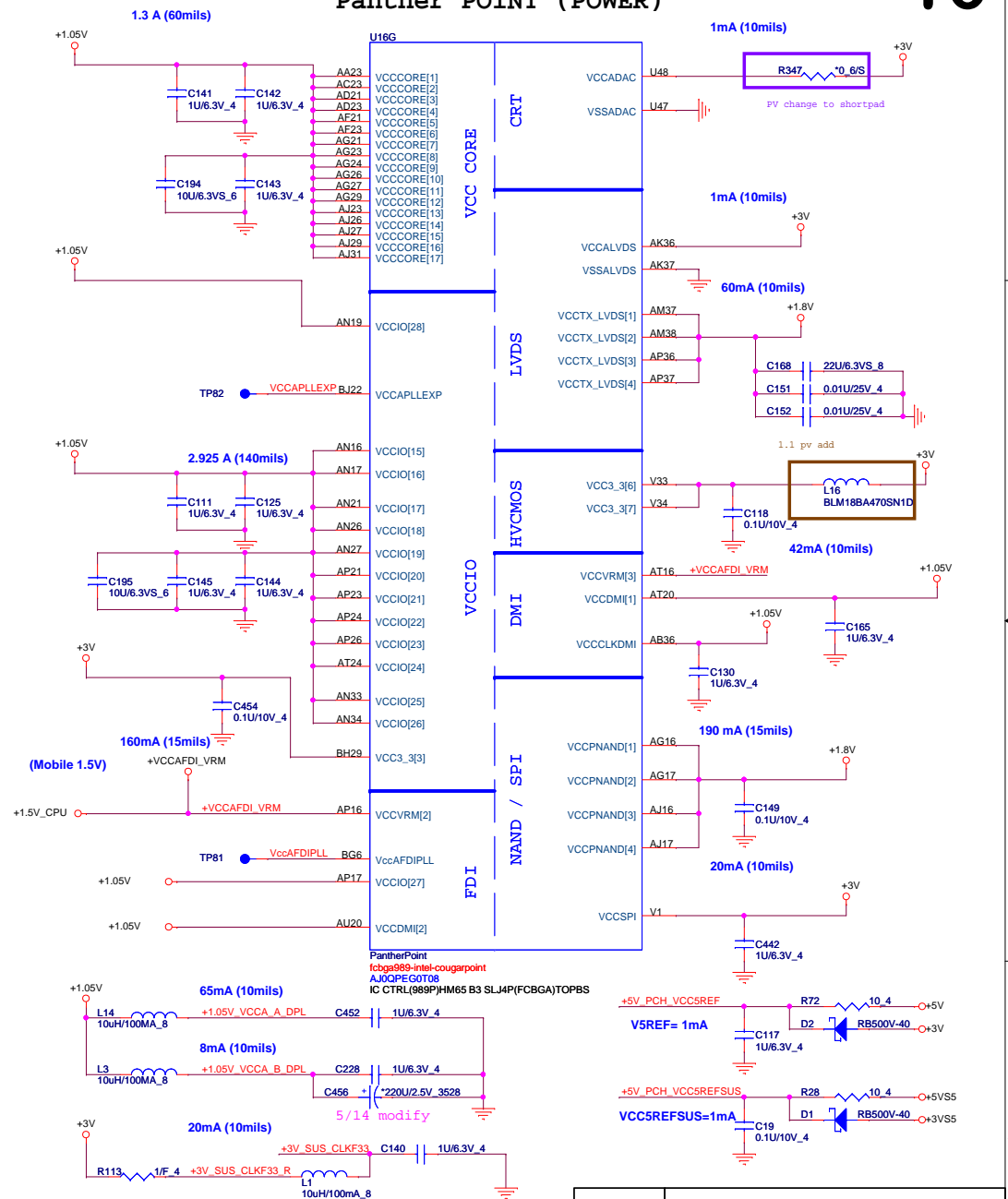
BOARD ID SETTING	BOARD_ID0 GPIO 44	BOARD_ID1 GPIO 45	BOARD_ID2 GPIO 46
HR	0	0	0
CR	1	0	0



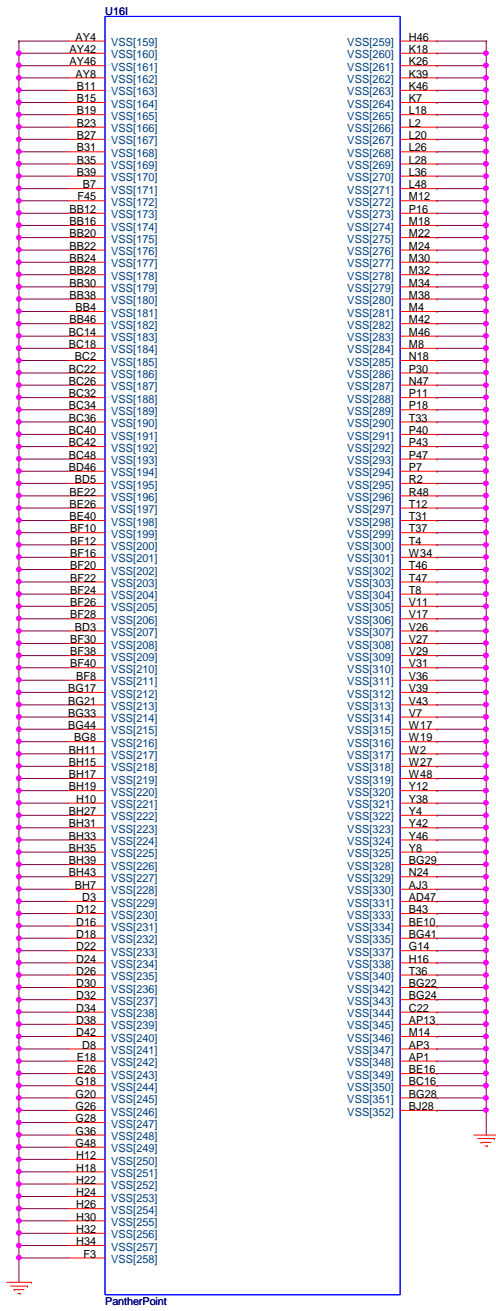
Panther Point (POWER)



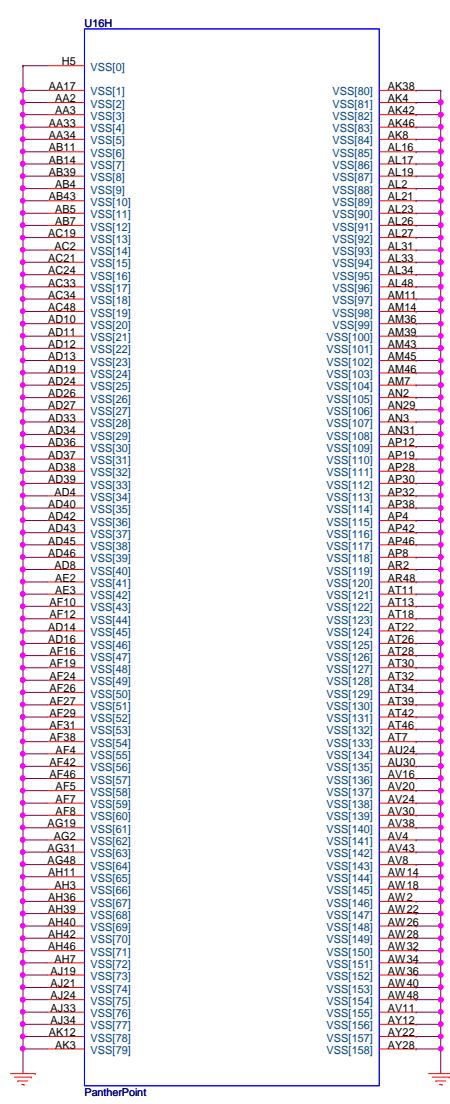
Panther POINT (POWER)

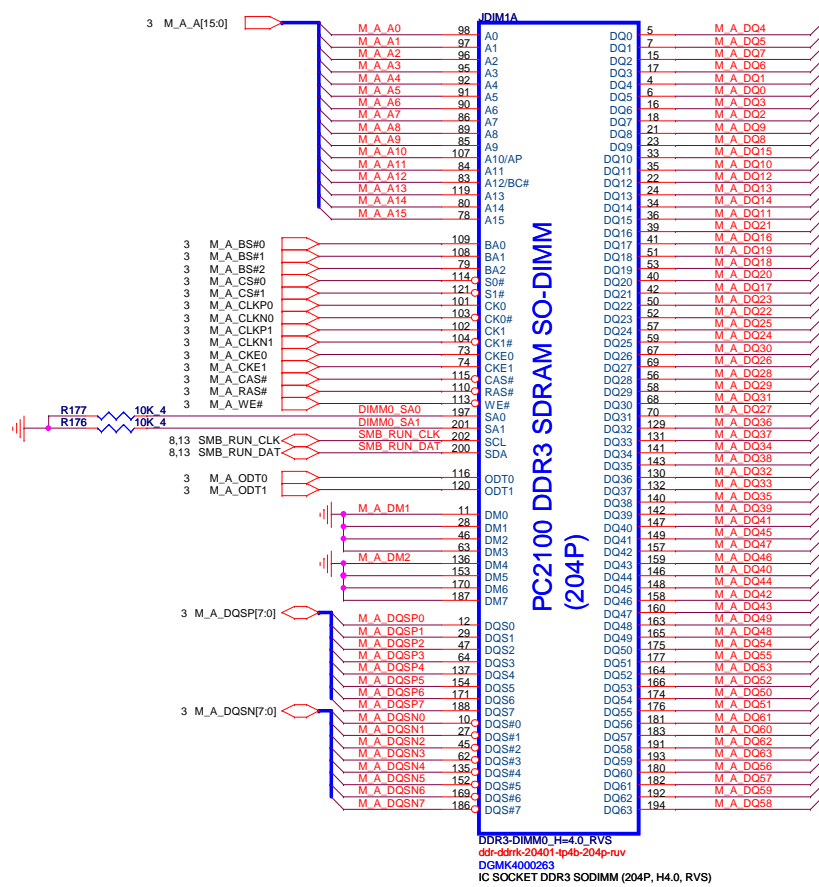


PantherPoint (GND)



PantherPoint (GND)





5 SMDDR_VREF_DQ0_M3

SMDDR_VREF_DQ0_M1 R179 0.6

SMDDR_VREF_DQ0_M3 R182 0.6

For Chief River M3

DDR3-DIMM0_H=4.0_RVS

ddr-ddr3k-20401-tp4b-204p-ruv

DGMK4000263

IC SOCKET DDR3 SODIMM (204P, H4.0, RVS)

Layout request.

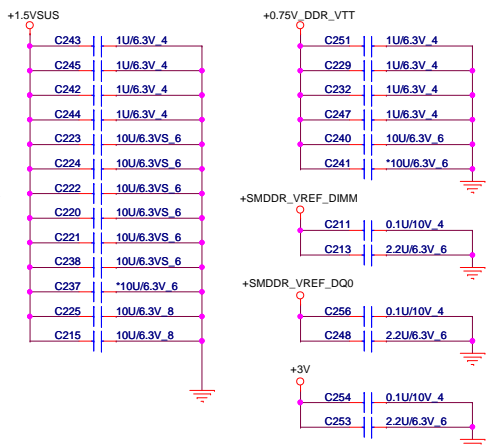
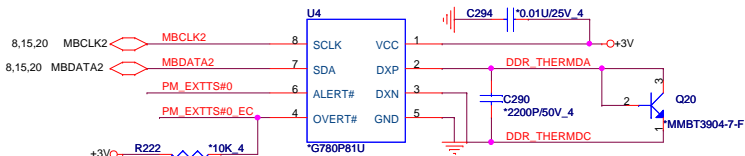
+0.75V_DDR_VTT 29.32

+1.5VSUS 2.4,28,29

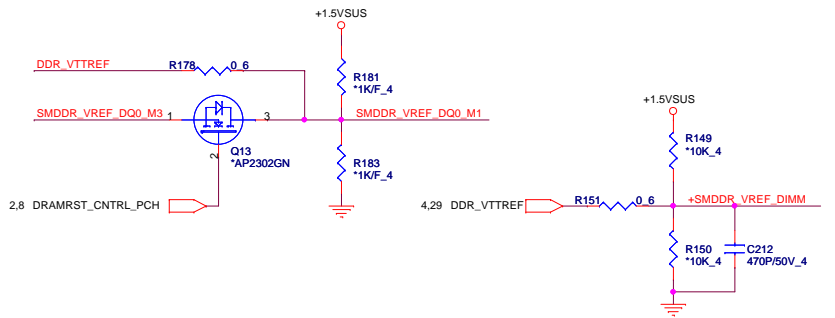
+3V 6,7,8,9,10,13,14,15,16,17,19,20,22,23,24,27,32

Place these Caps near So-Dimm0.

DDR3 Thermal Sensor



VREF DQ0 M1 Solution

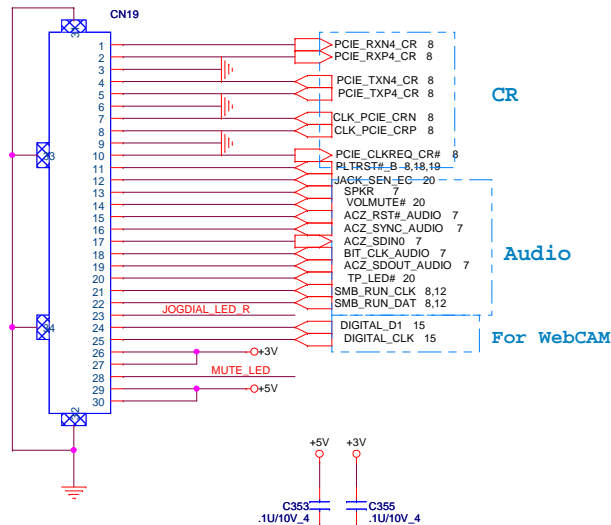


PROJECT : Stella

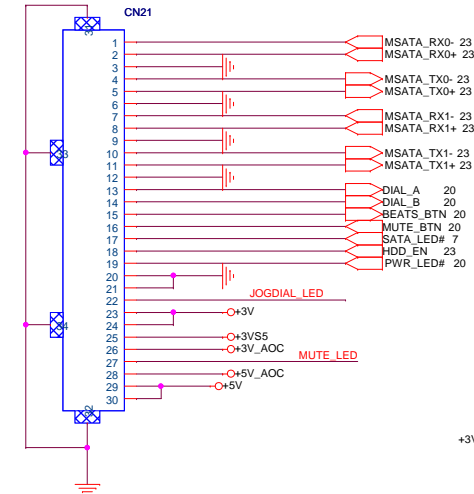
Quanta Computer Inc.

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Custom	DDR3 DIMM0-STD (5.2H)	1A
Date: Monday, April 23, 2012	Sheet 12	of 31

FOR AUDIO/CR



FOR mSATA

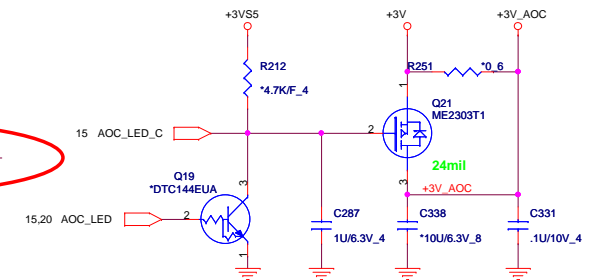
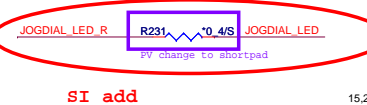
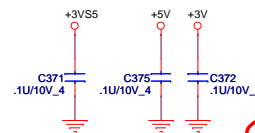


mSATA 1ST

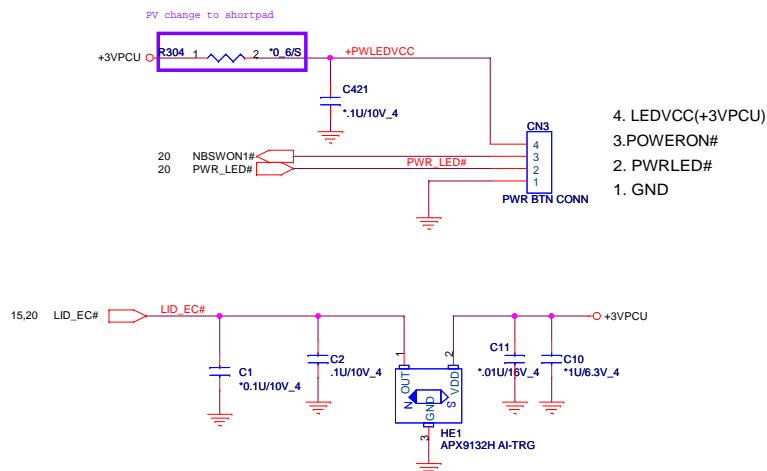
mSATA 2ND

JogDial

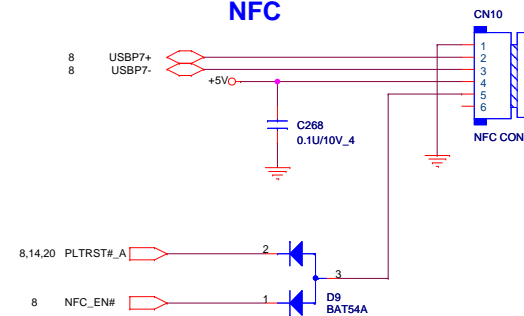
Mute Button



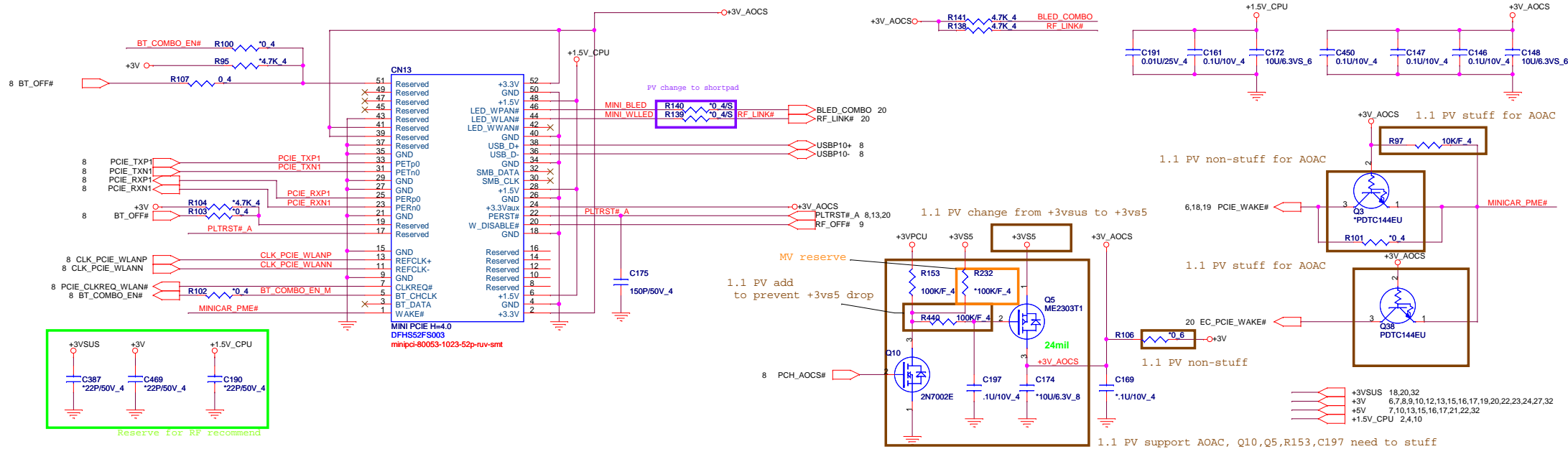
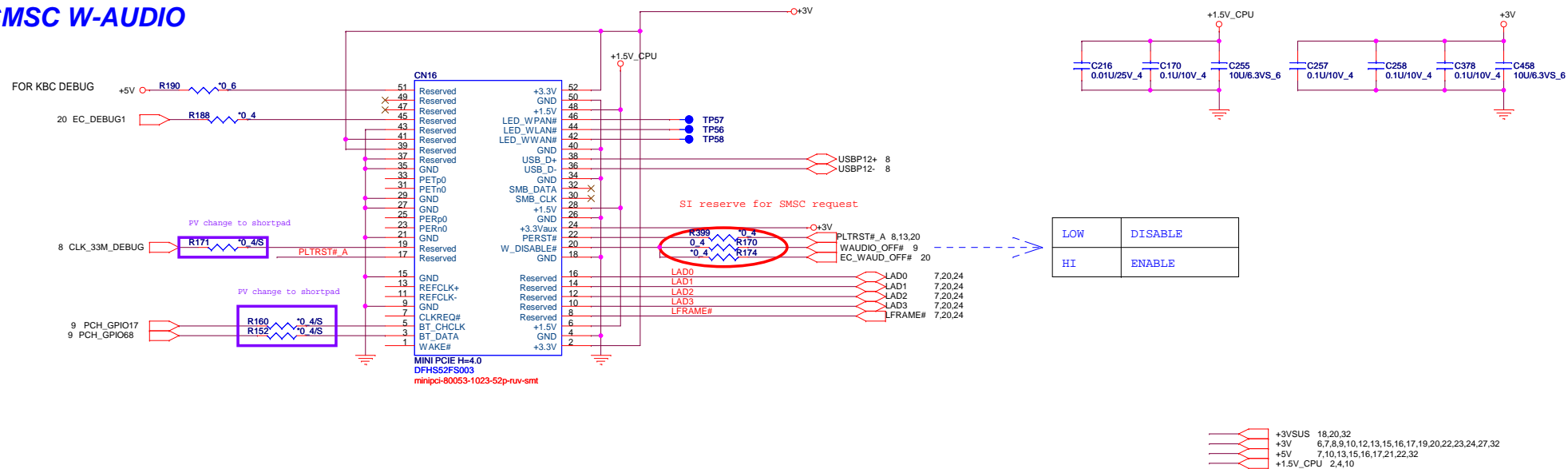
POWER BUTTON



NFC



Mini PCI-E Card 1 WLAN+BT

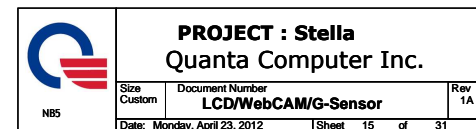
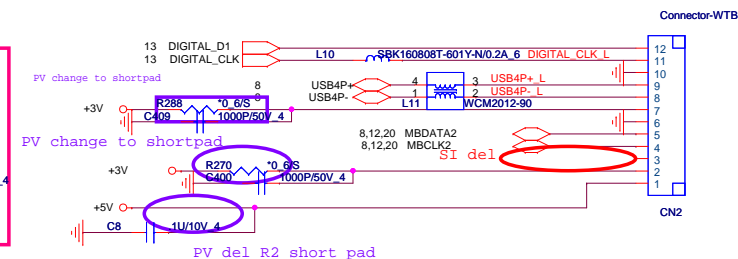
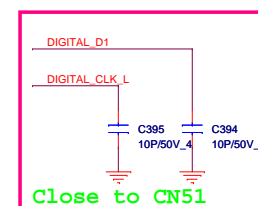
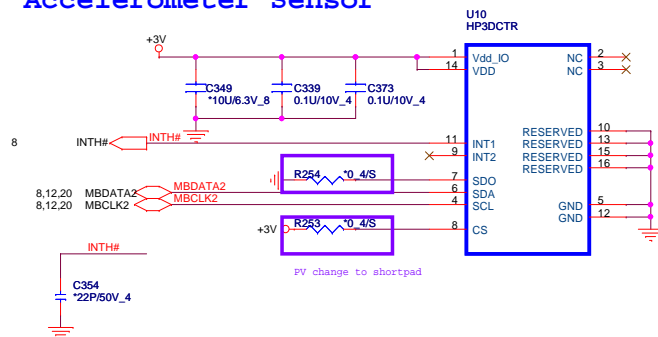
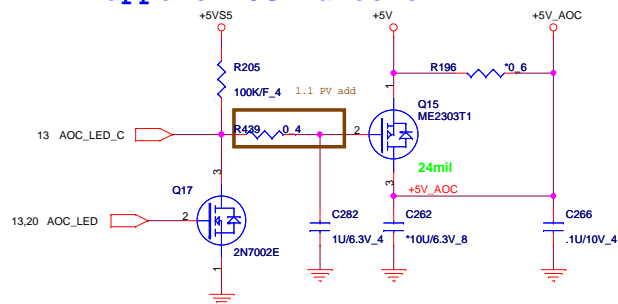
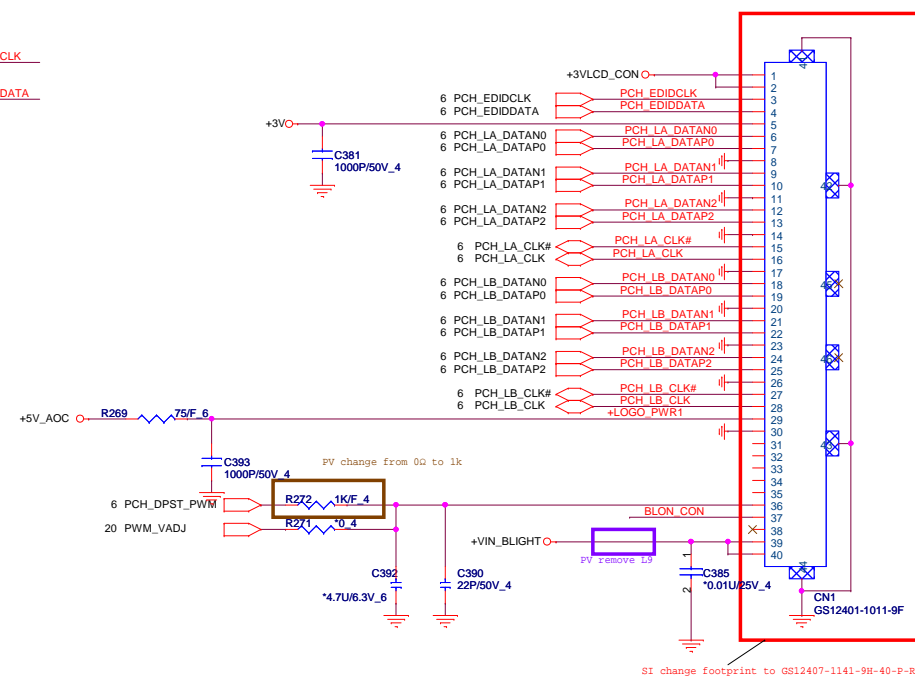
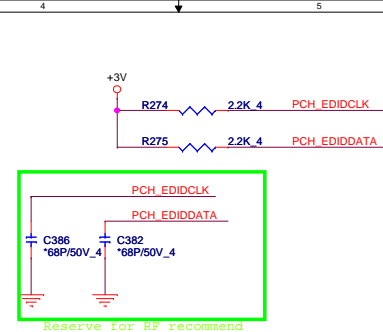
**Mini PCI-E Card 1**
SMSC W-AUDIO

LOW	DISABLE
HI	ENABLE

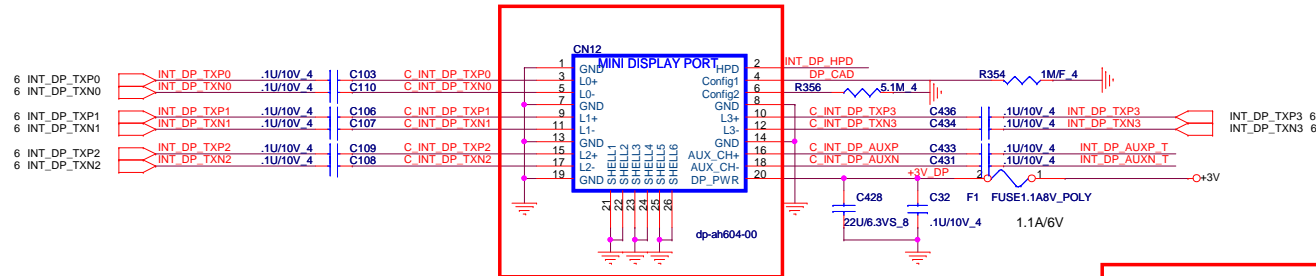


PROJECT : Stella
Quanta Computer Inc.

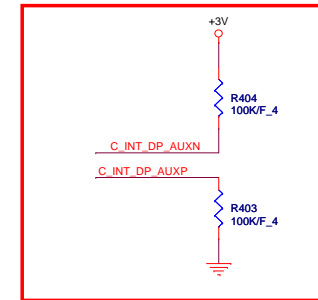
Size Custom	Document Number MINI PCIE CONN	Rev 1A
Date: Monday, April 23, 2012		Sheet 14 of 31



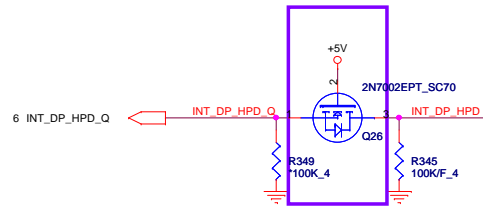
Mini Display



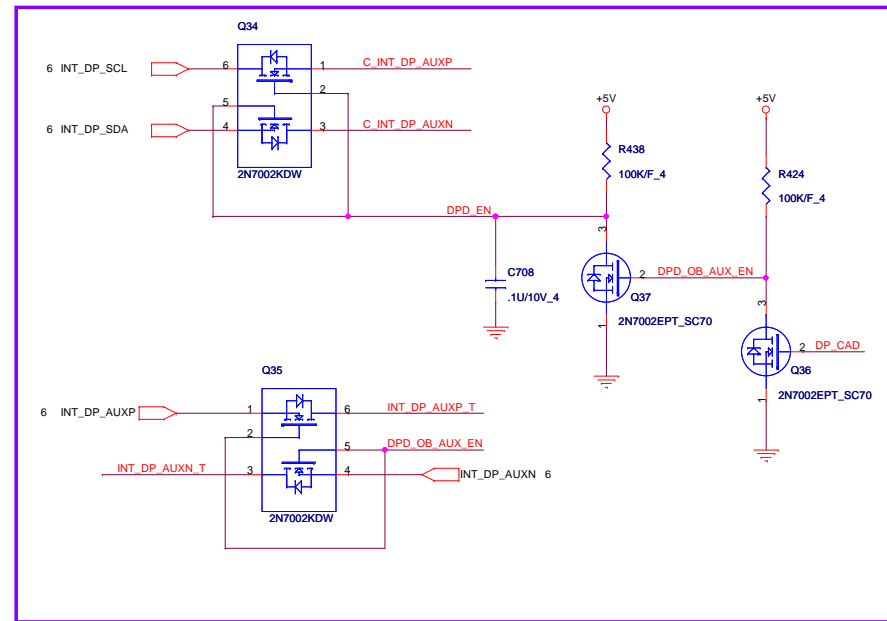
SI change footprint



SI add for intel recommend

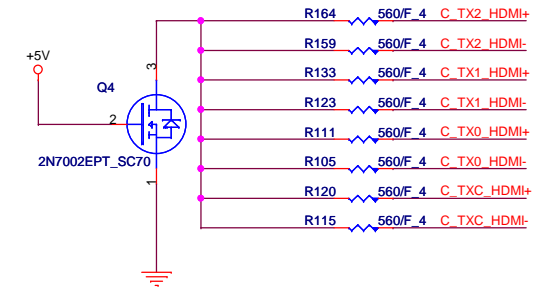
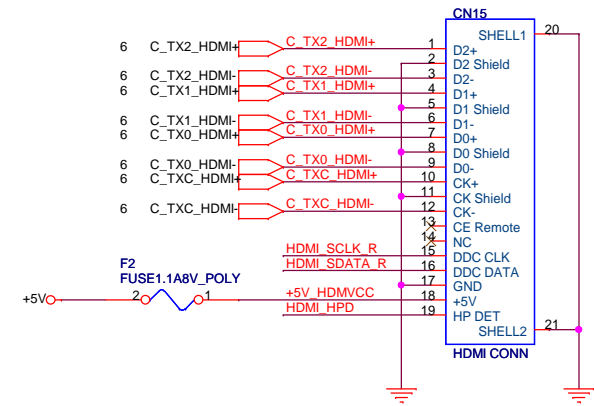
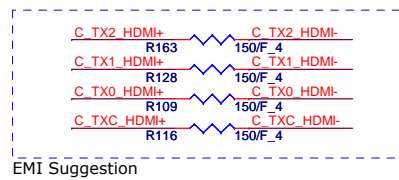
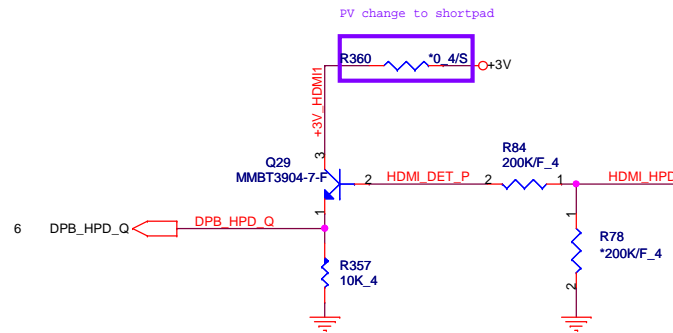
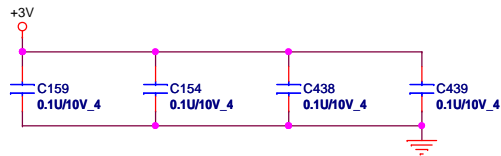
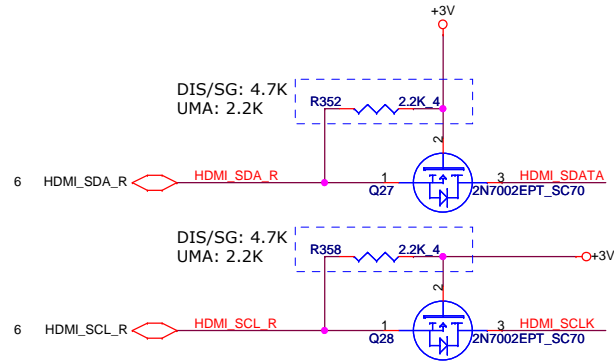
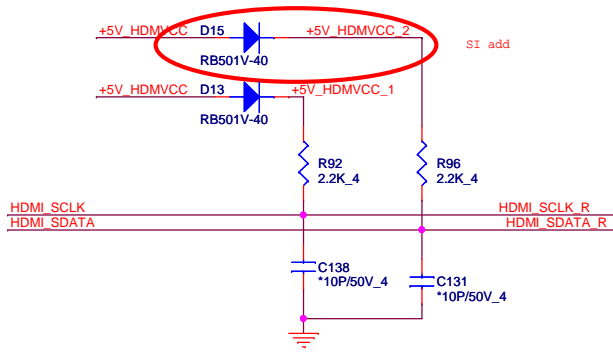


PV change footprint to SC70



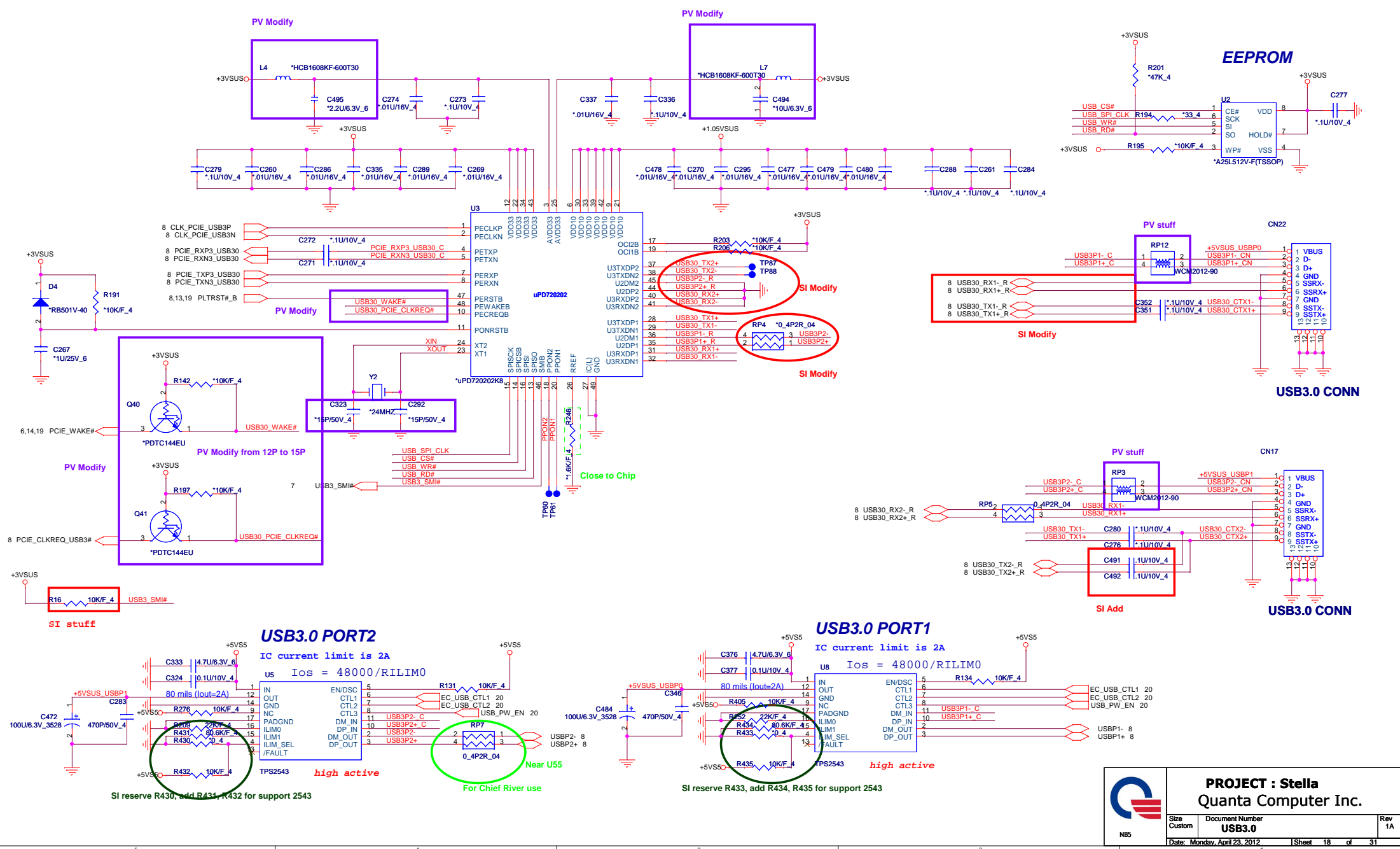
PV add for mini-display to HDMI dongle support

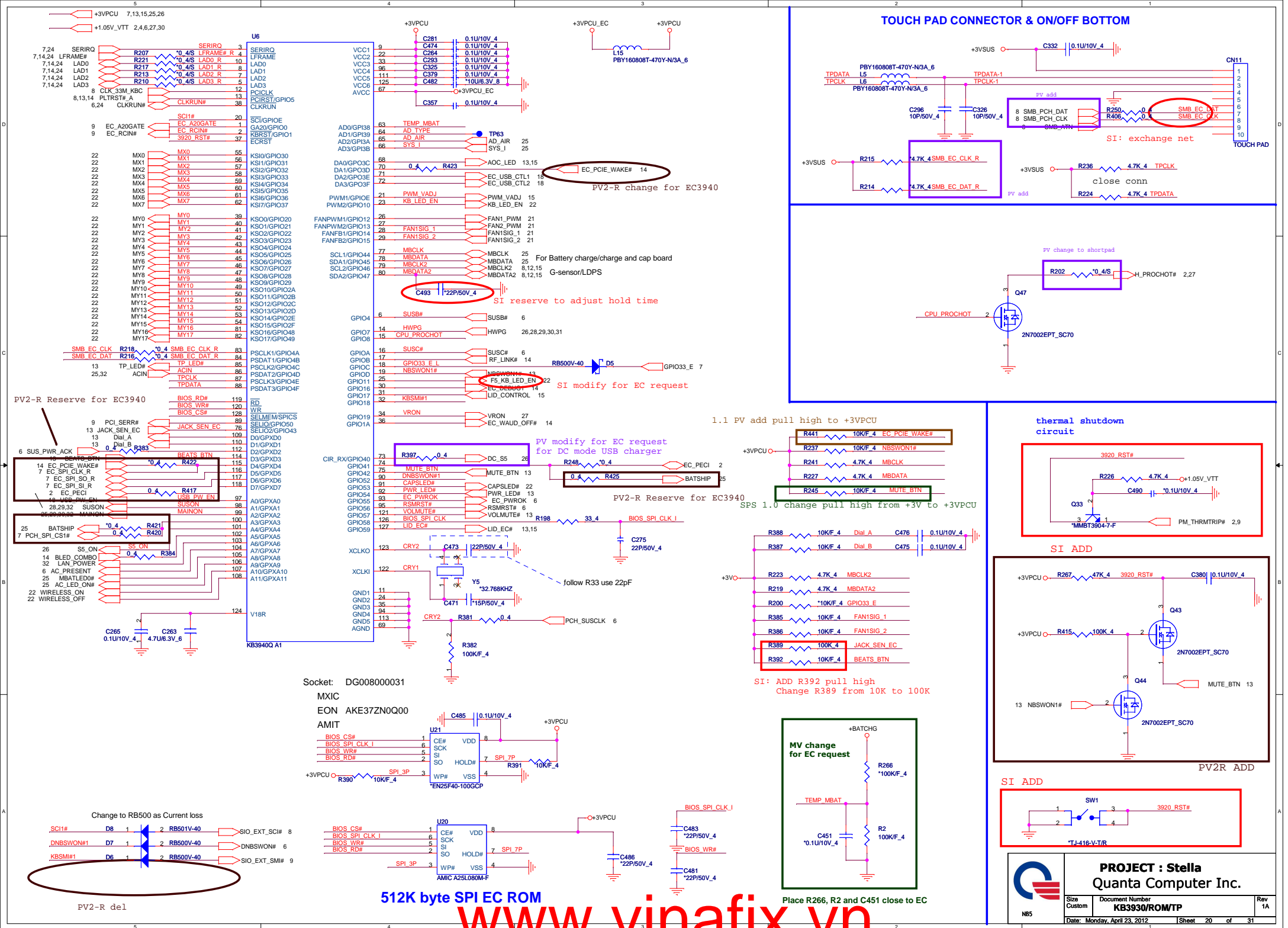
HDMI CON_COM



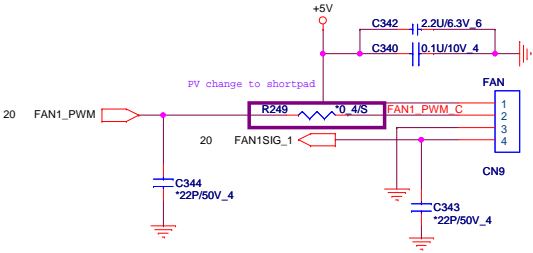
7,10,13,14,15,16,21,22,32 +5V
6,7,8,9,10,12,13,14,15,16,19,20,22,23,24,27,32 +3V

PROJECT : Stella Quanta Computer Inc.		
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Date: Monday, April 23, 2012 Sheet 17 of 31		

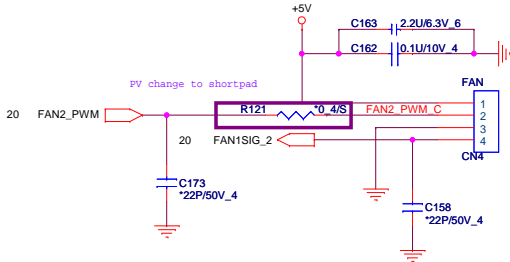




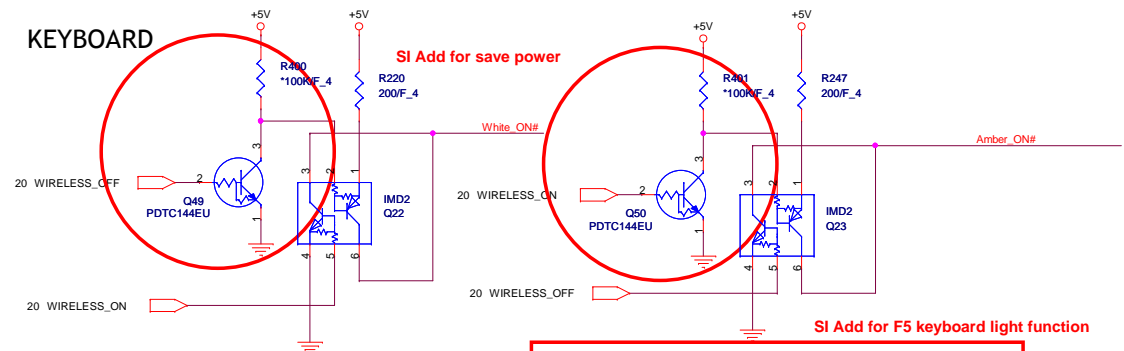
CPU FAN1



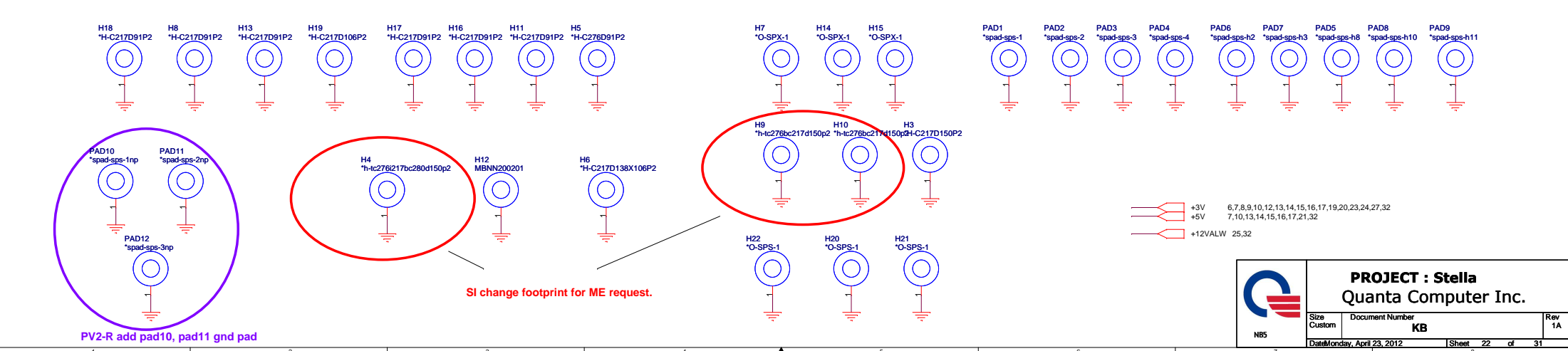
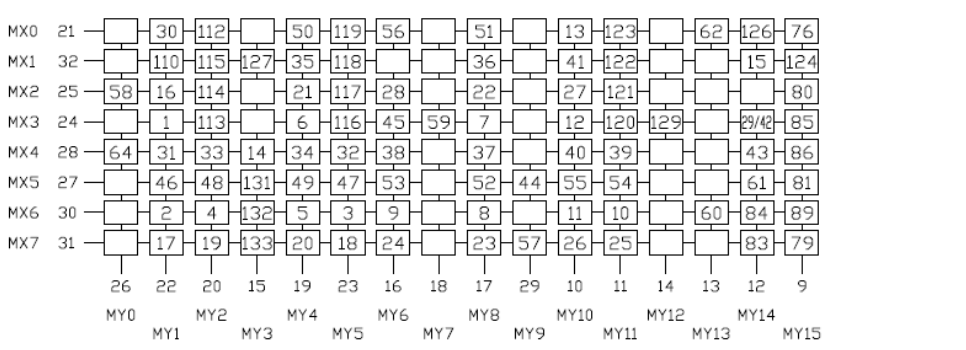
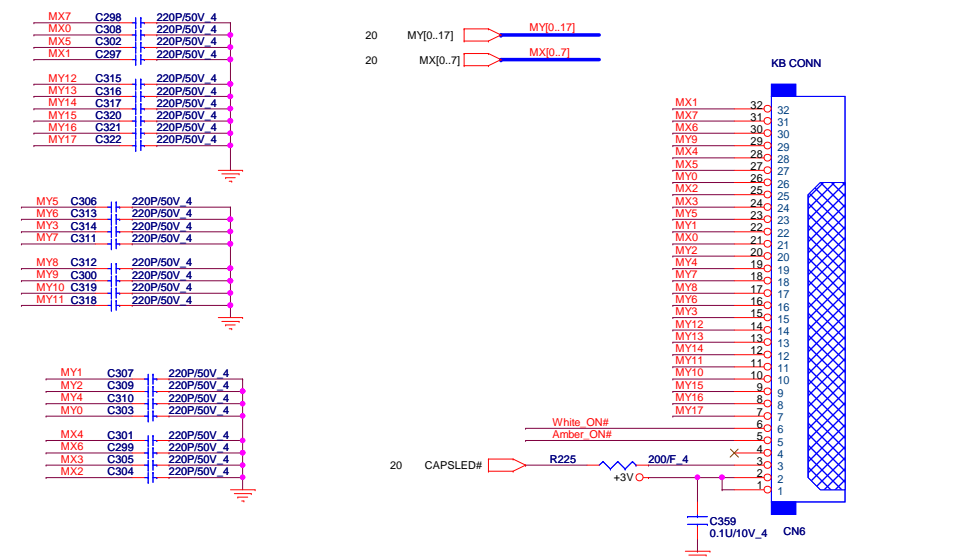
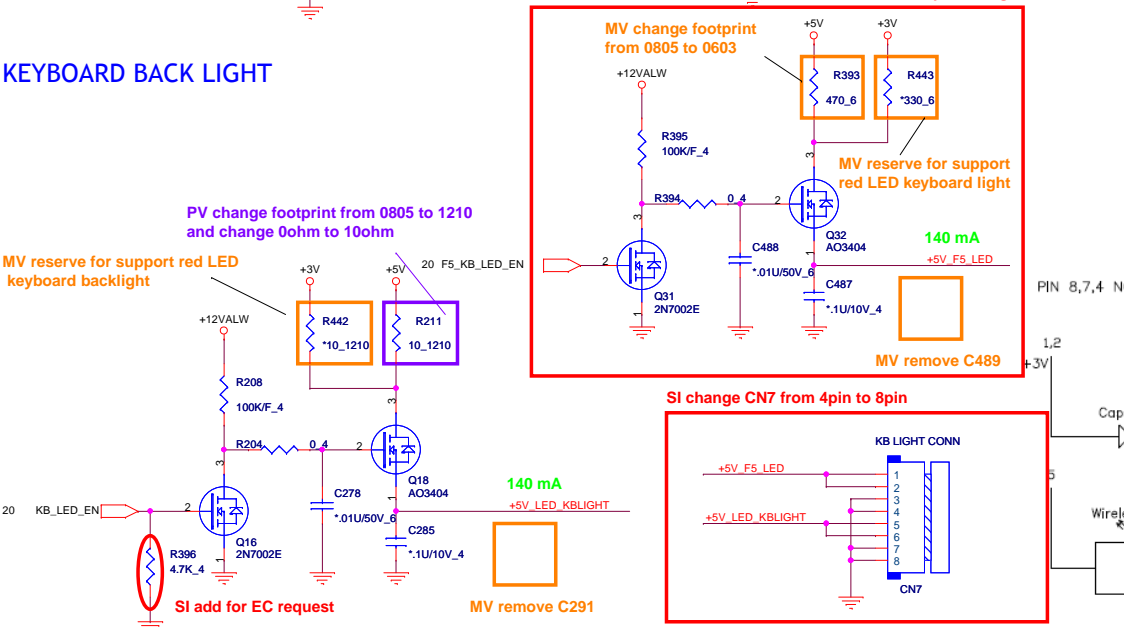
CPU FAN2



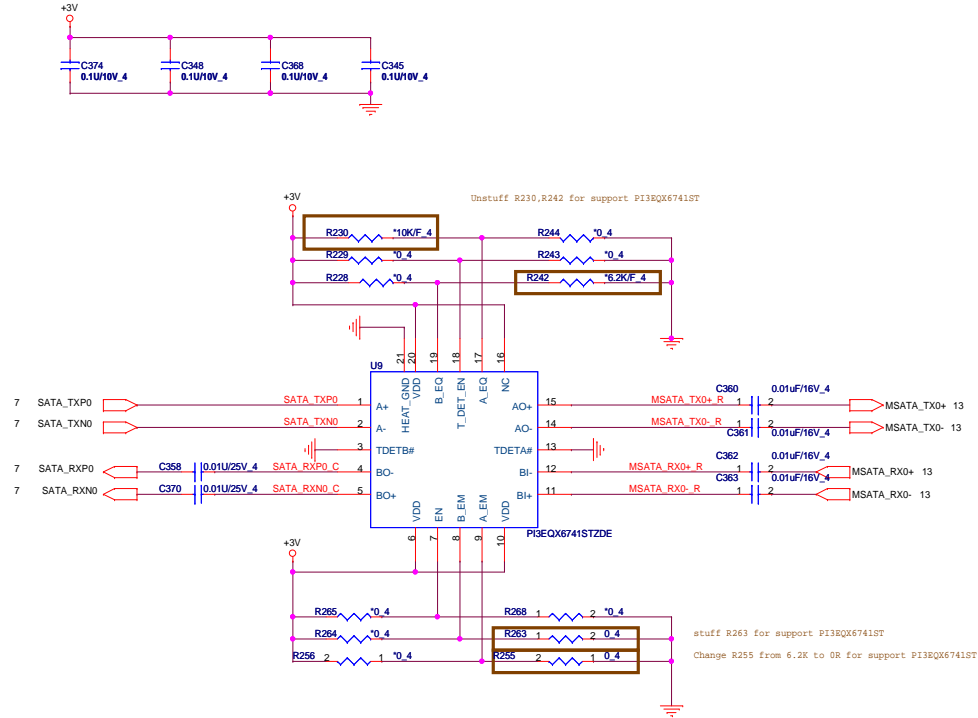
KEYBOARD



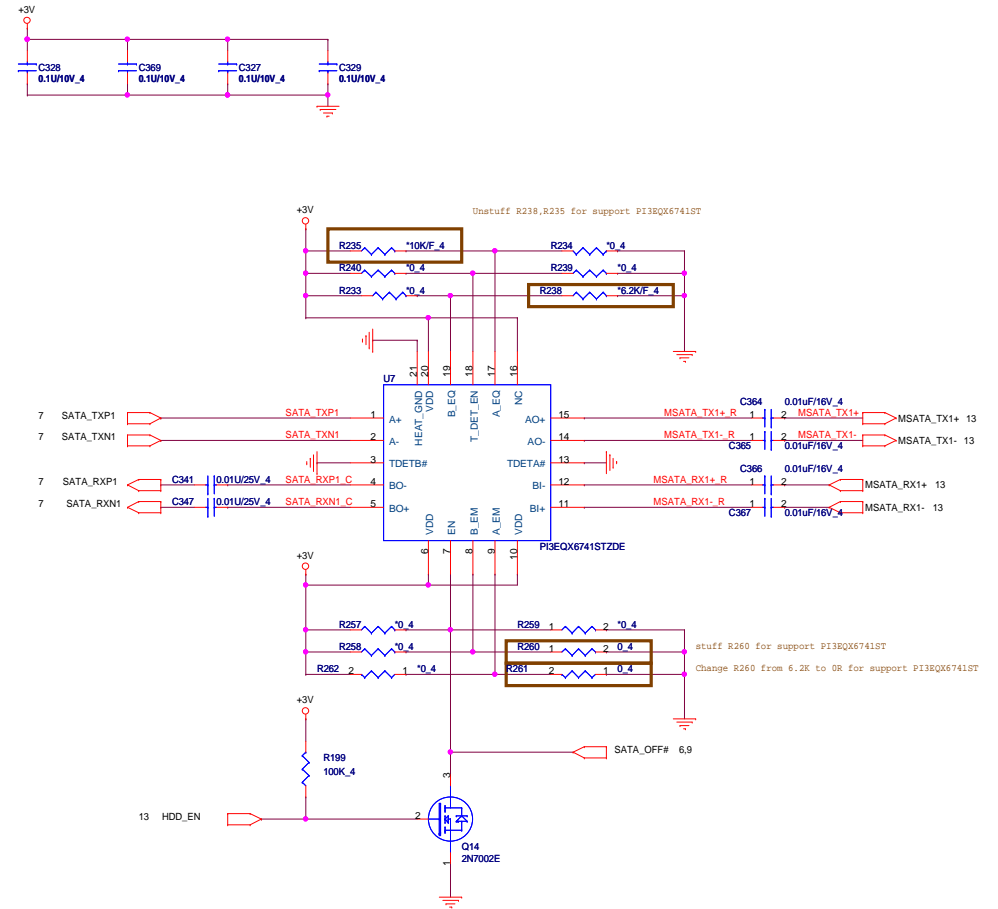
KEYBOARD BACK LIGHT



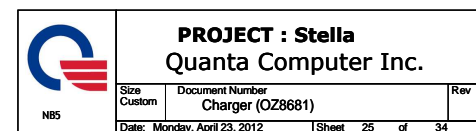
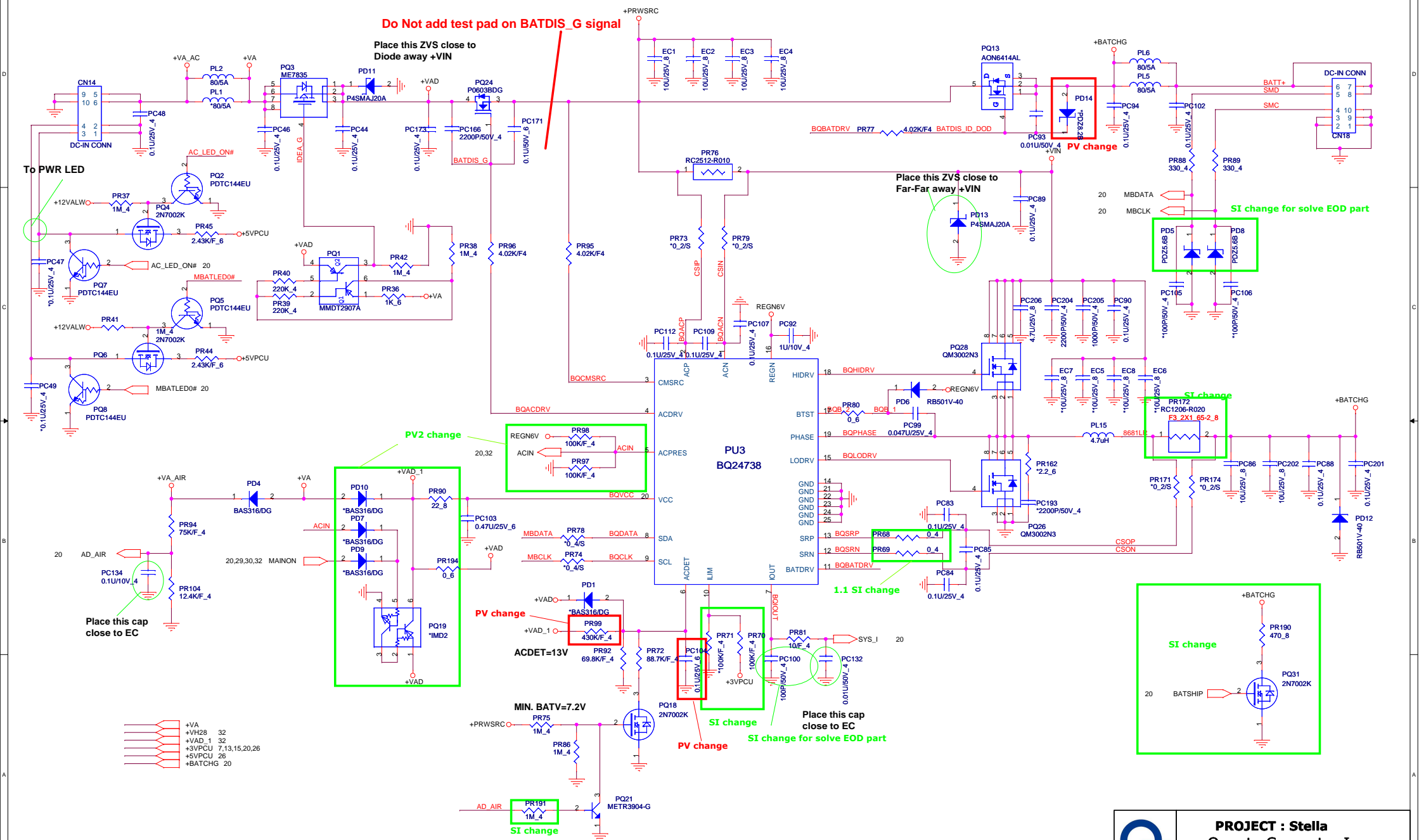
HDD0 mSATA 1ST



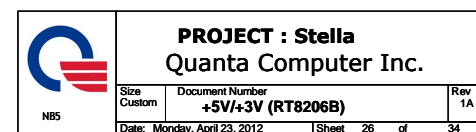
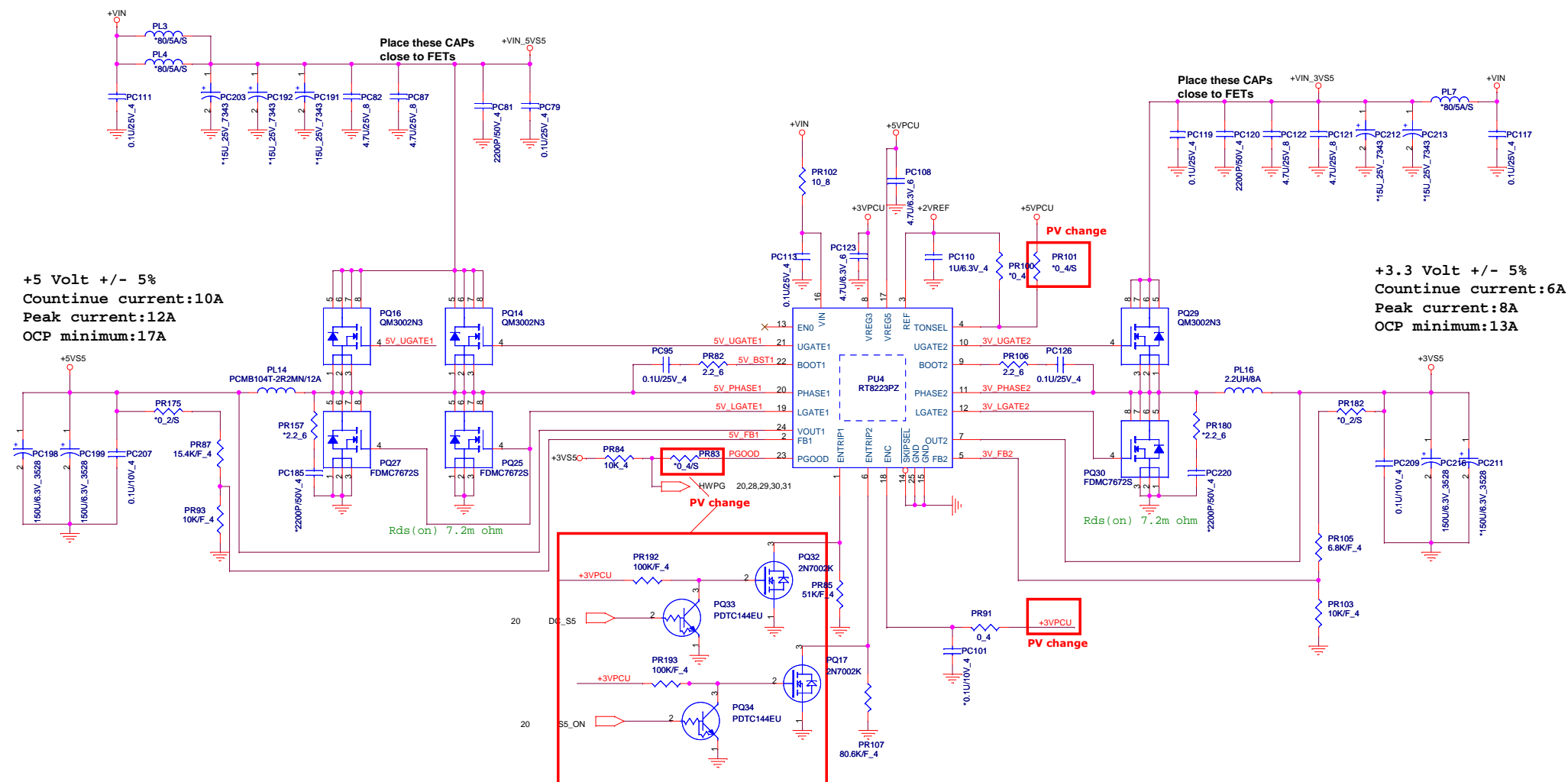
HDD1 mSATA 2ND



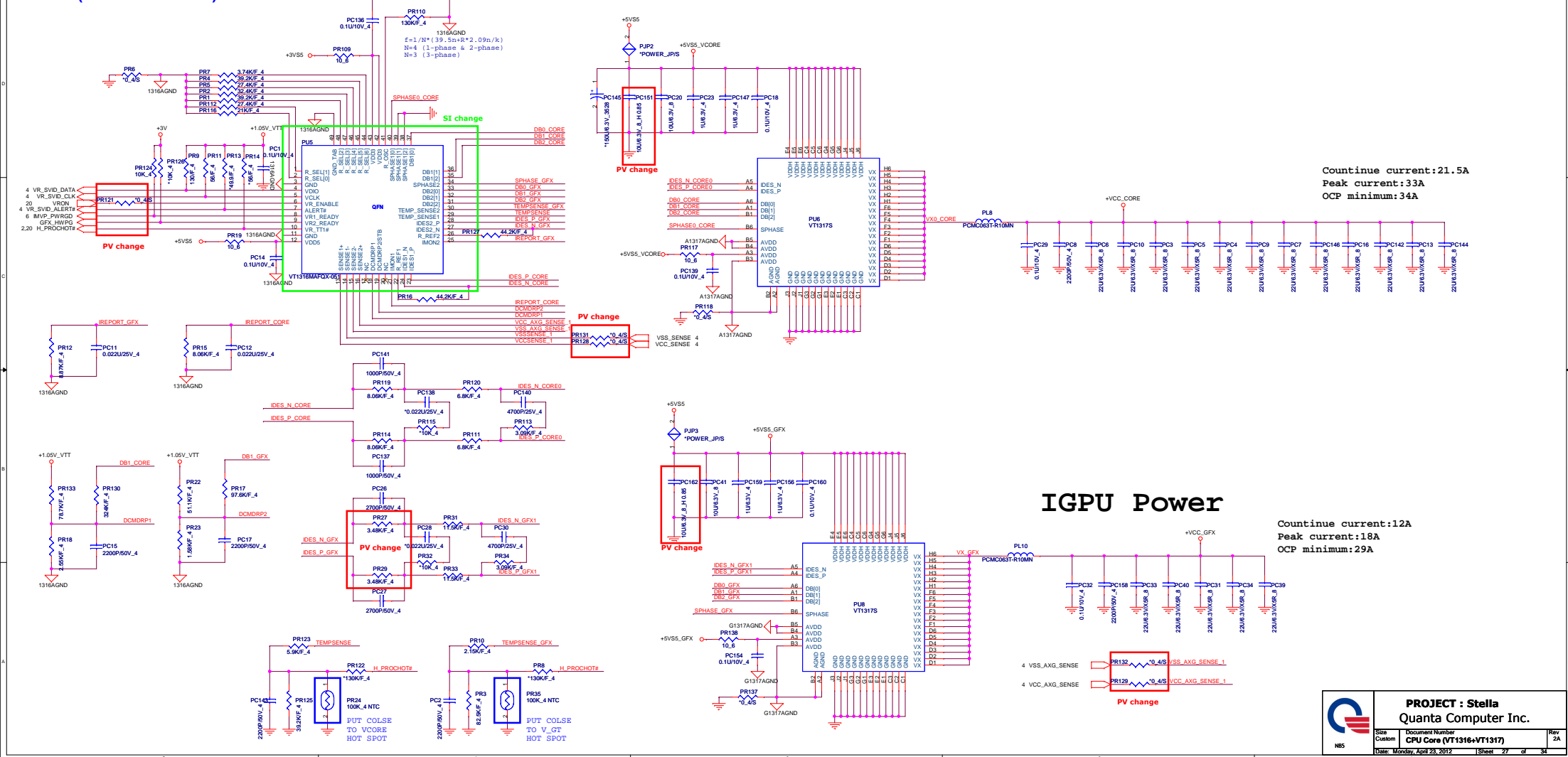
DC_JACK
65W



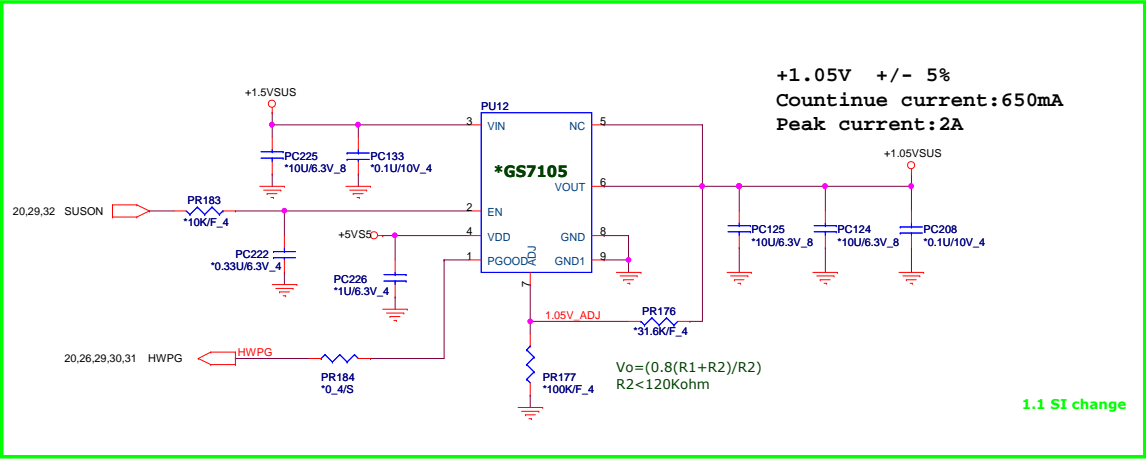
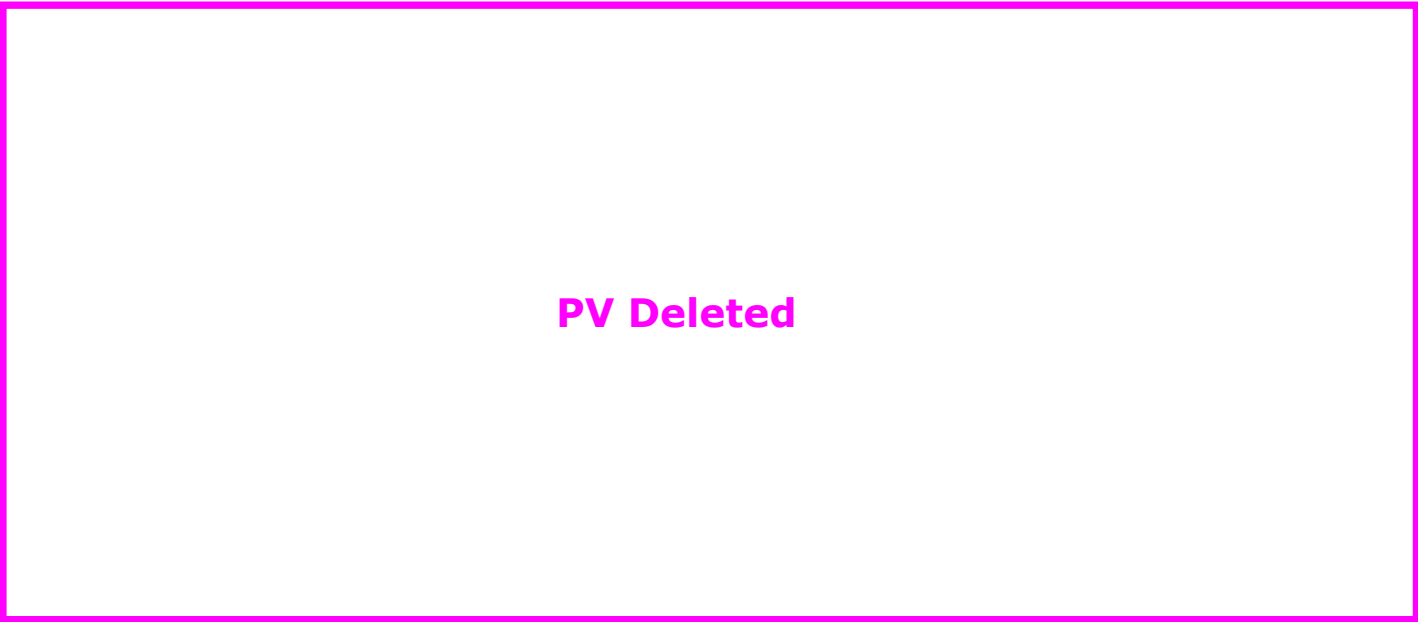
5
DC/DC +3VS5/+5VS5

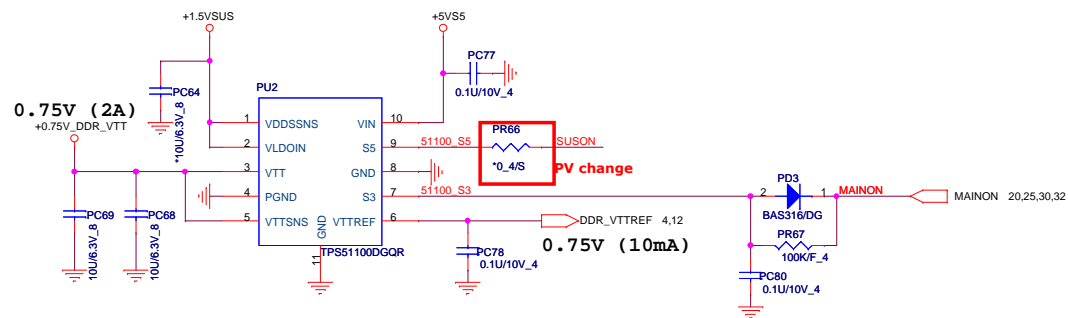
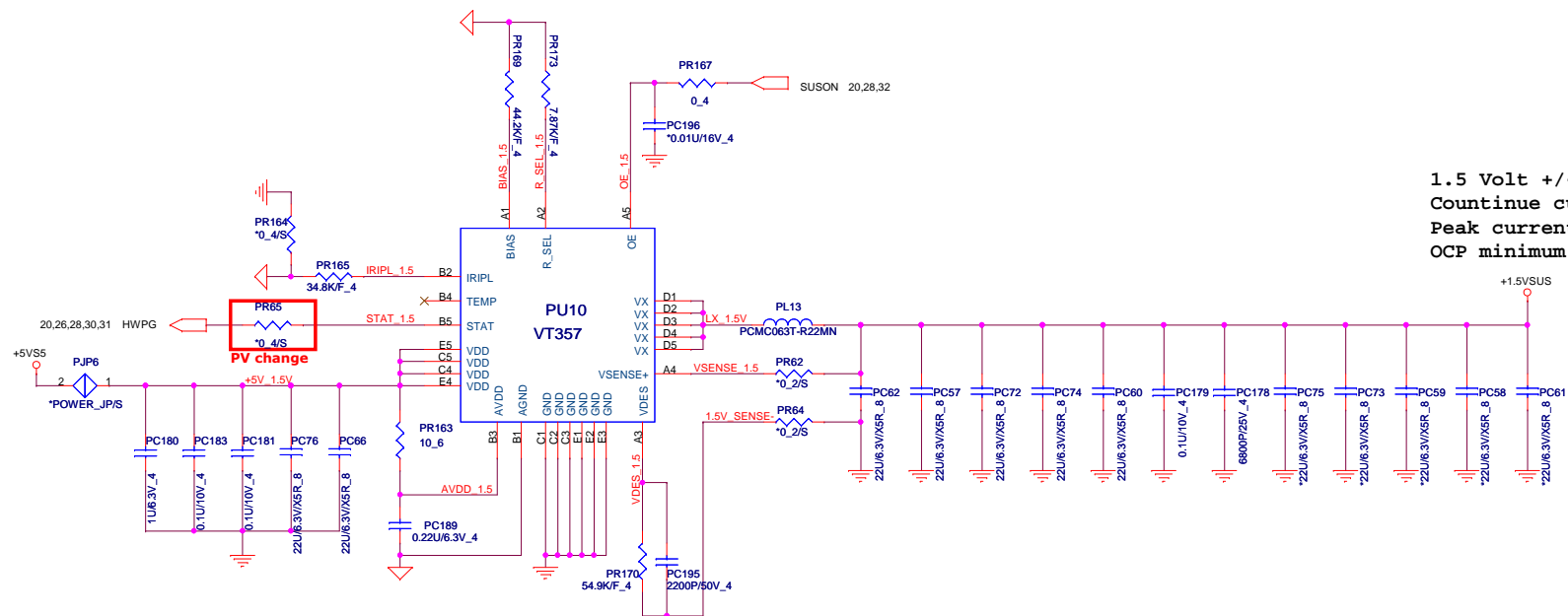


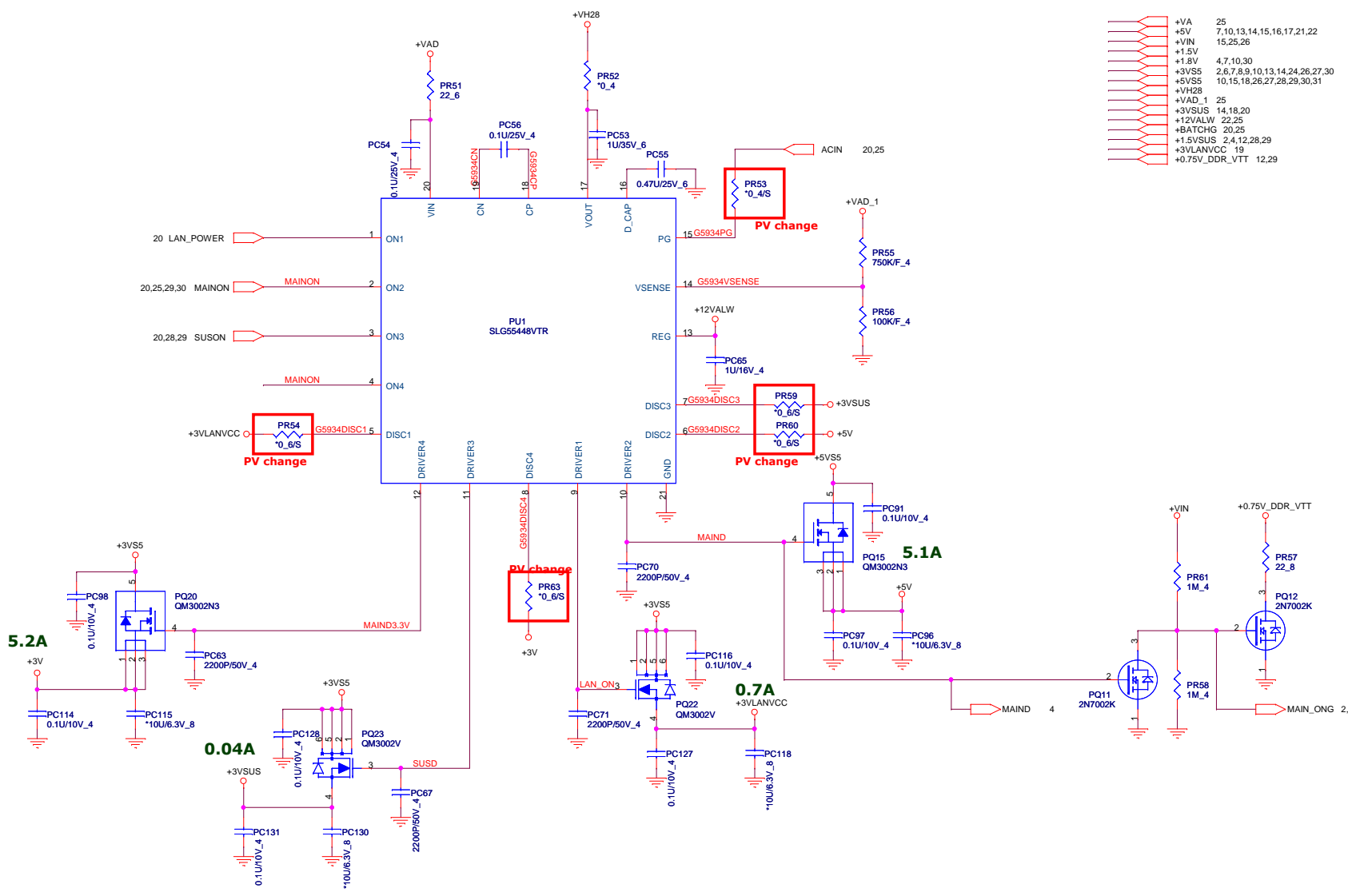
CPU Core(VT1316M+VT317S)



VCCP1.05V







+VA	25
+5V	7,10,13,14,15,16,17,21,22
+VIN	15,25,26
+1.5V	
+1.8V	4,7,10,30
+3VS5	2,6,7,8,9,10,13,14,24,26,27,30
+5VS5	10,15,18,26,27,28,29,30,31
+VH28	
+VAD_1	25
+3VSUS	14,18,20
+12VALW	22,25
+BATCHG	20,25
+1.5VSUS	2,4,12,28,29
+3VLAVCC	19
+0.75V_DDR_VTT	12,29