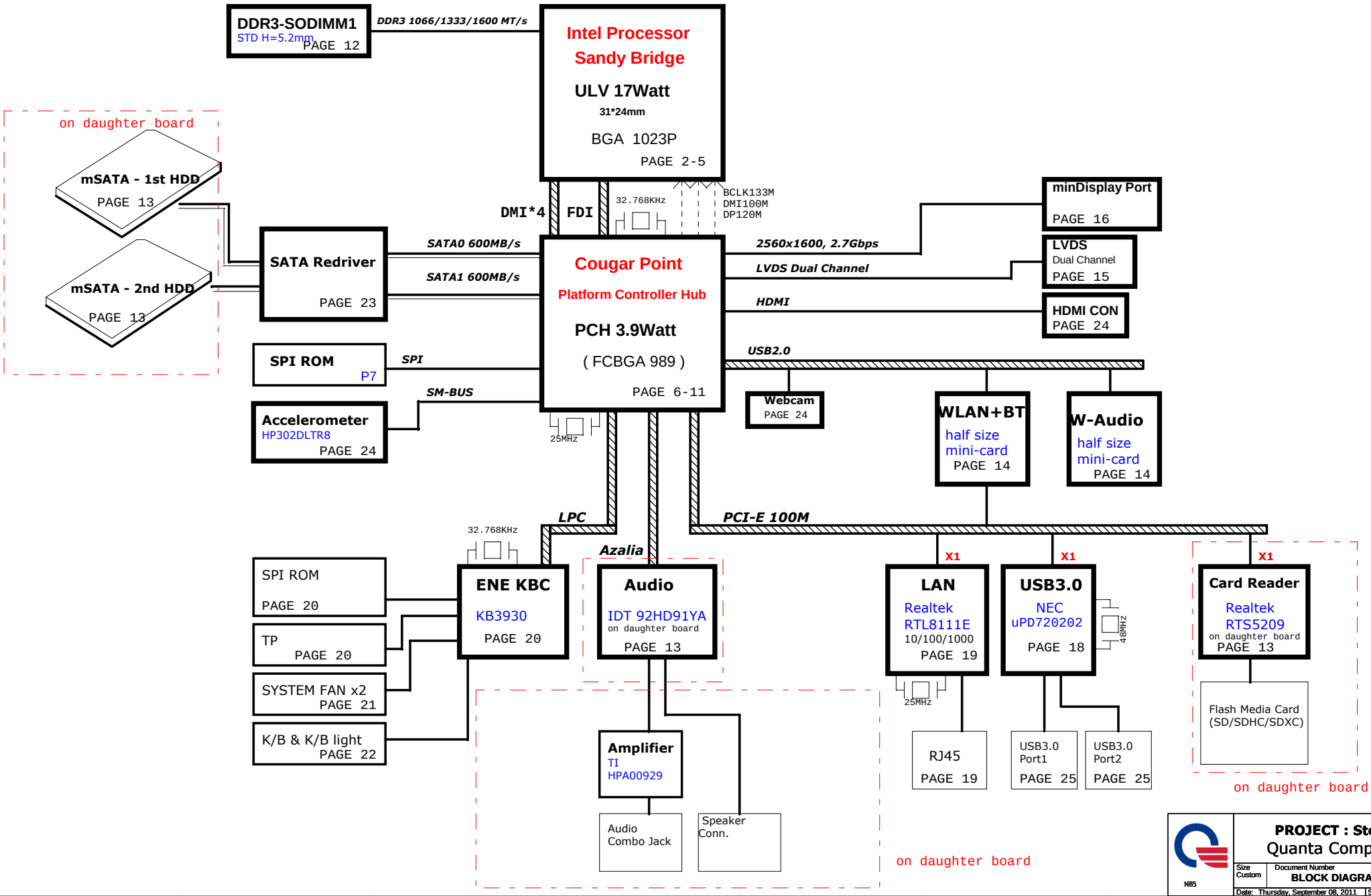
14 Envy (Huron/Chief River ULV 17W(BGA) UMA BLOCK DIAGRAM

01

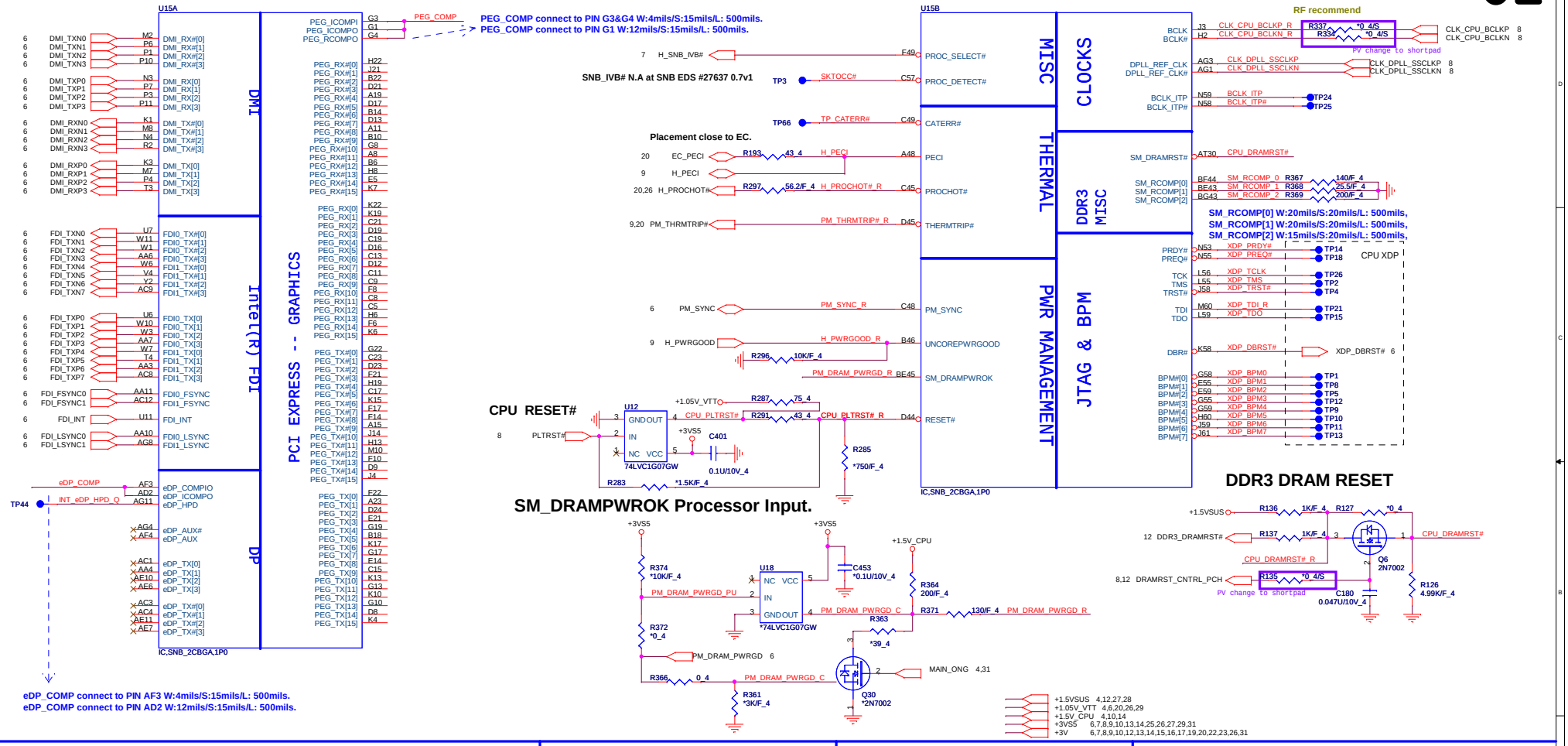


N85	PROJECT : Stella Quanta Computer Inc.	
Size: Custom	Document Number: BLOCK DIAGRAM	Rev: 1A
Date: Thursday, September 08, 2011	Sheet 1 of 31	

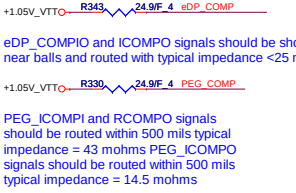
Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)

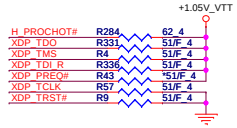
02



DP & PEG Compensation



Processor pull-up (CPU)



PROJECT : Stella

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 1/4 (PCIE&DMI&FDI)	1A

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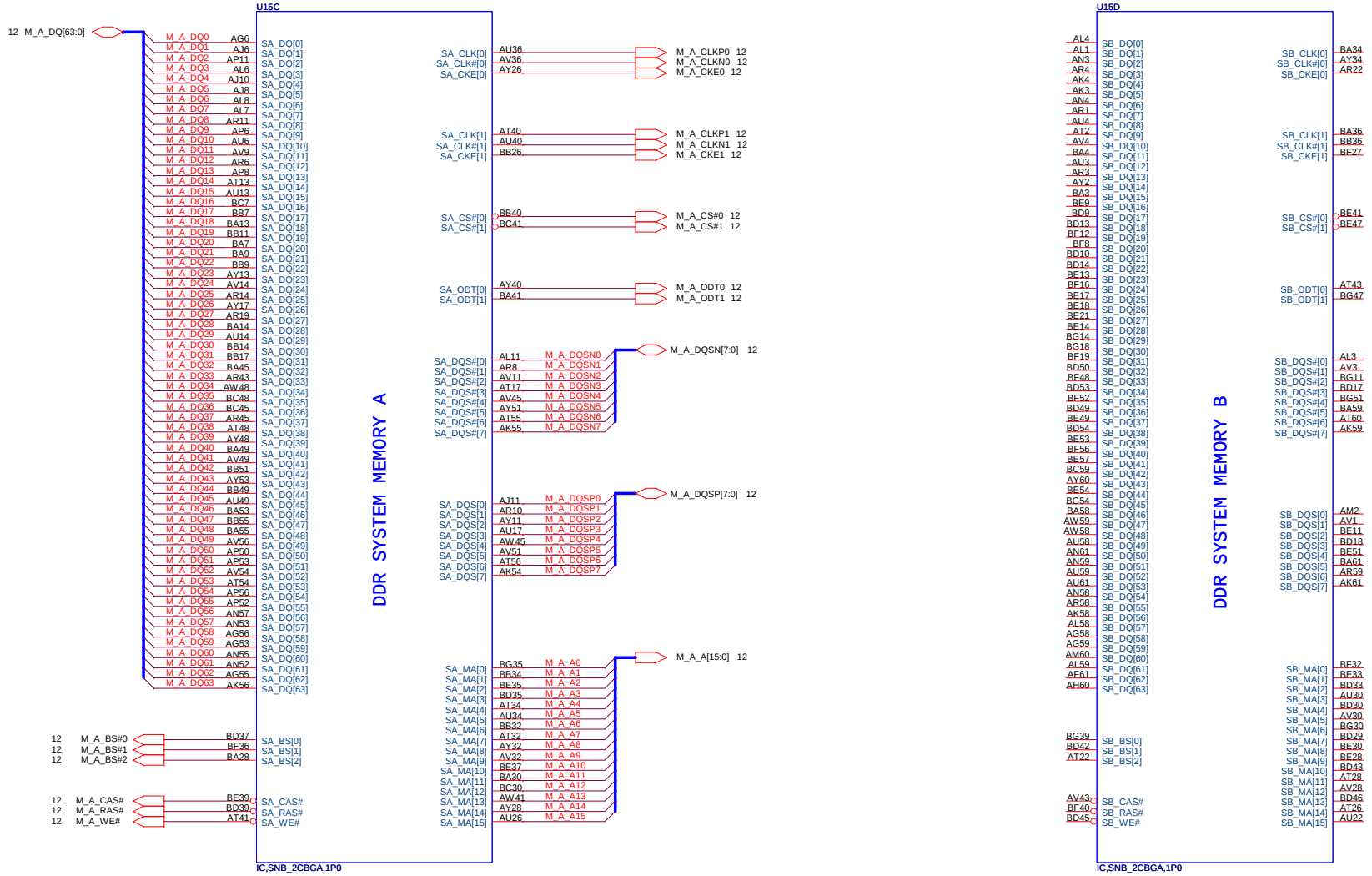
Sandy Bridge Processor (DDR3)



PROJECT : Stella

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SNB 2/4 (DDR3 I/F)	1A

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N85

Sandy Bridge Processor (POWER)

330uF locate power side

CPU Core Power

SNB:55A

8.5A

22A

SNB:6A

3A

PV change to shortpad

4/26 Intel

IC,SNB_2CBGA,1P0

Sandy Bridge Processor (GRAPHIC POWER)

04

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

SNB:4A

SI reserve for INTEL recommend

CPU VDDQ

For Chief River

Layout note: need routing together and ALERT need between CLK and DATA.

SVID CLK

SVID DATA

SVID ALERT

Place PU resistor close to VR

Place PU resistor close to CPU

Place PU resistor close to CPU

+VCC_CORE 5,26
+VCC_GFX 26
+VCCSA 30
+1.05V_VTT 2,6,20,26,29
+1.5V_CPU 2,10,14
+1.5VSUS 2,12,27,28
+1.8V 7,10,29
+3V 6,7,8,9,10,12,13,14,15,16,17,19,20,22,23,26,31

PROJECT : Stella
Quanta Computer Inc.

Size: Custom | Document Number: SNB 3/4 (POWER) | Rev: 1A
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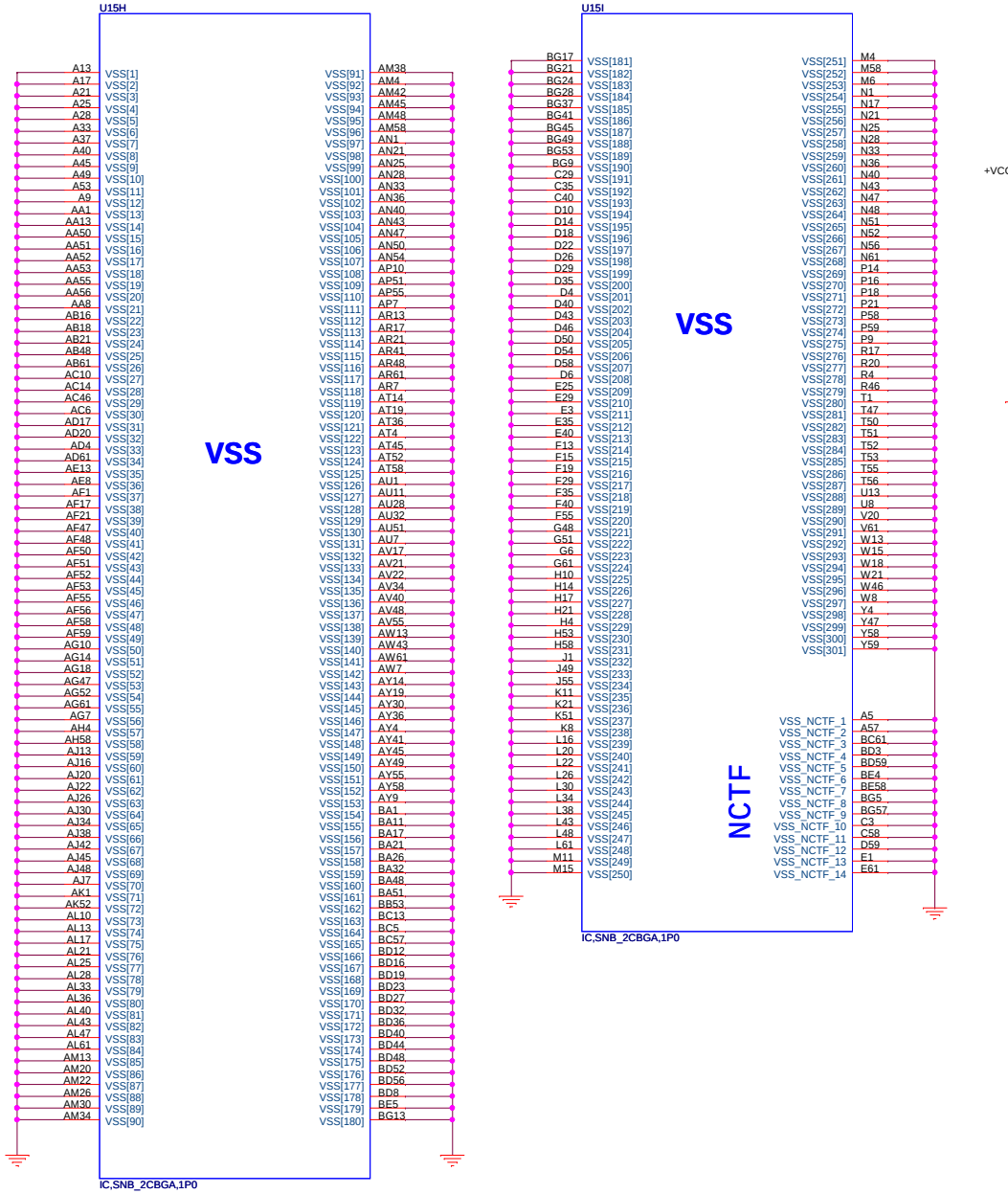
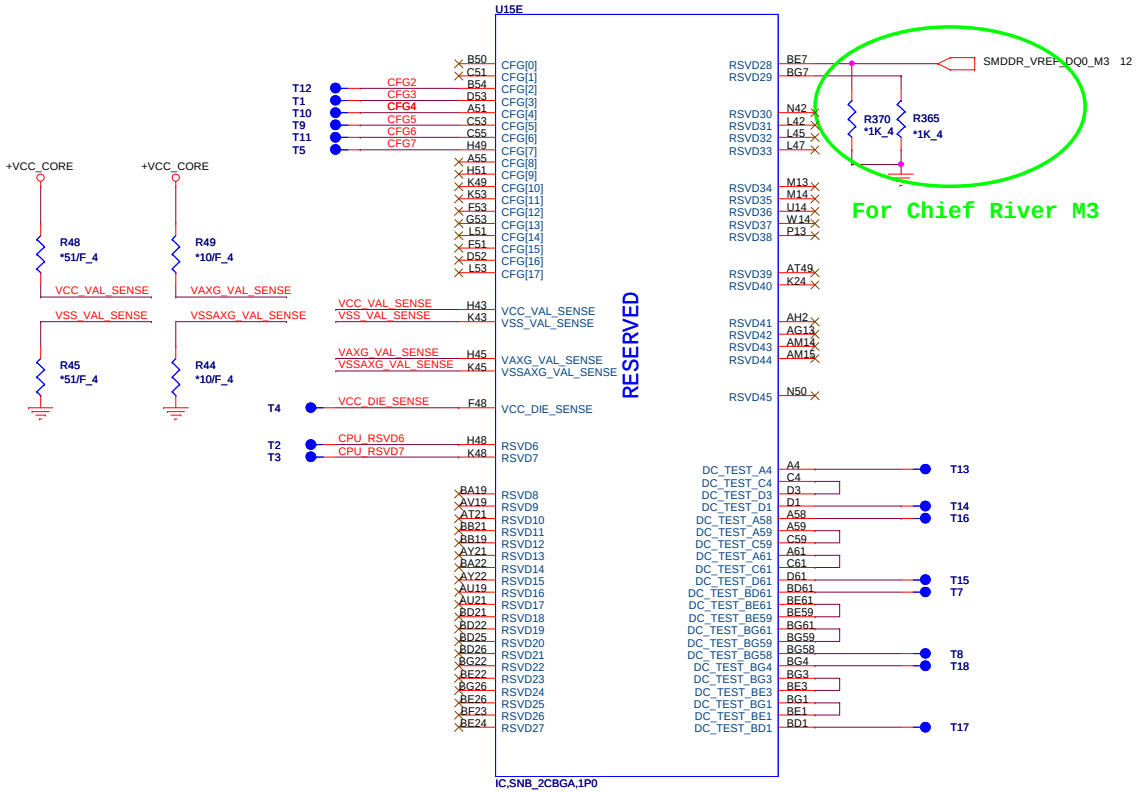
Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)



PROJECT : Stella		
Quanta Computer Inc.		
Size: Custom	Document Number: SNB 4/4 (GND)	Rev: 1A
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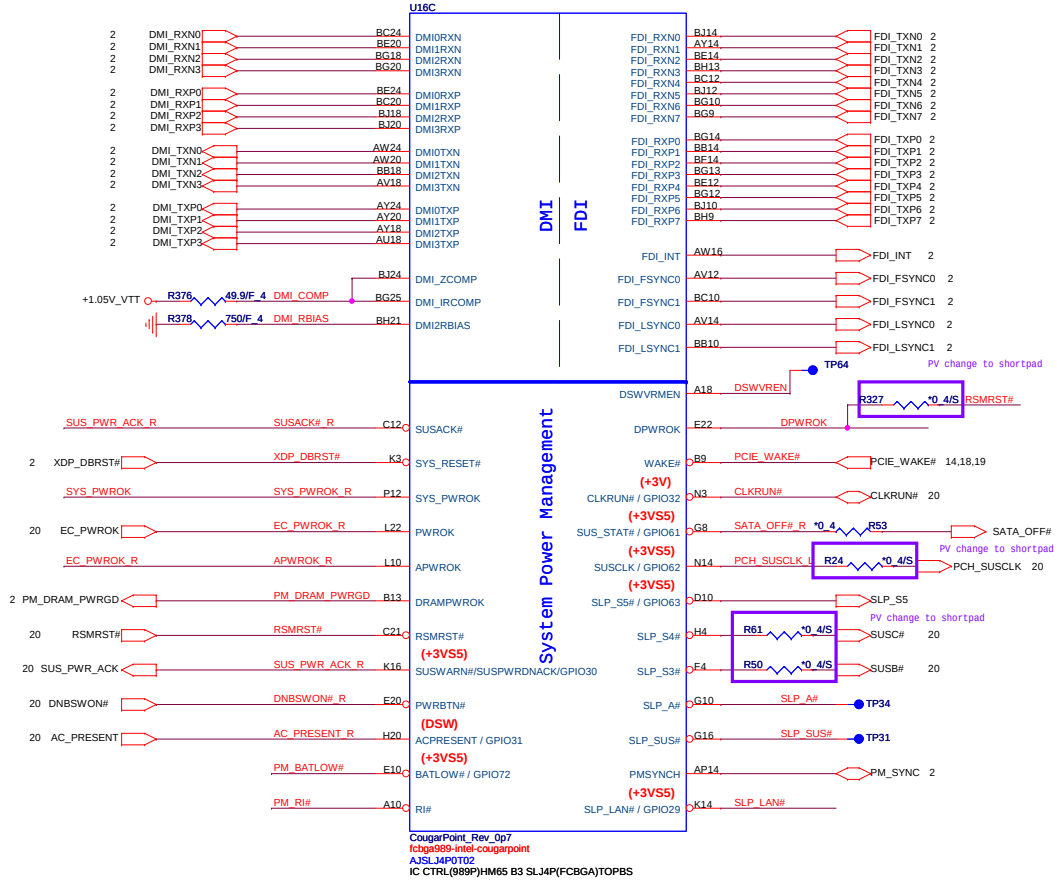
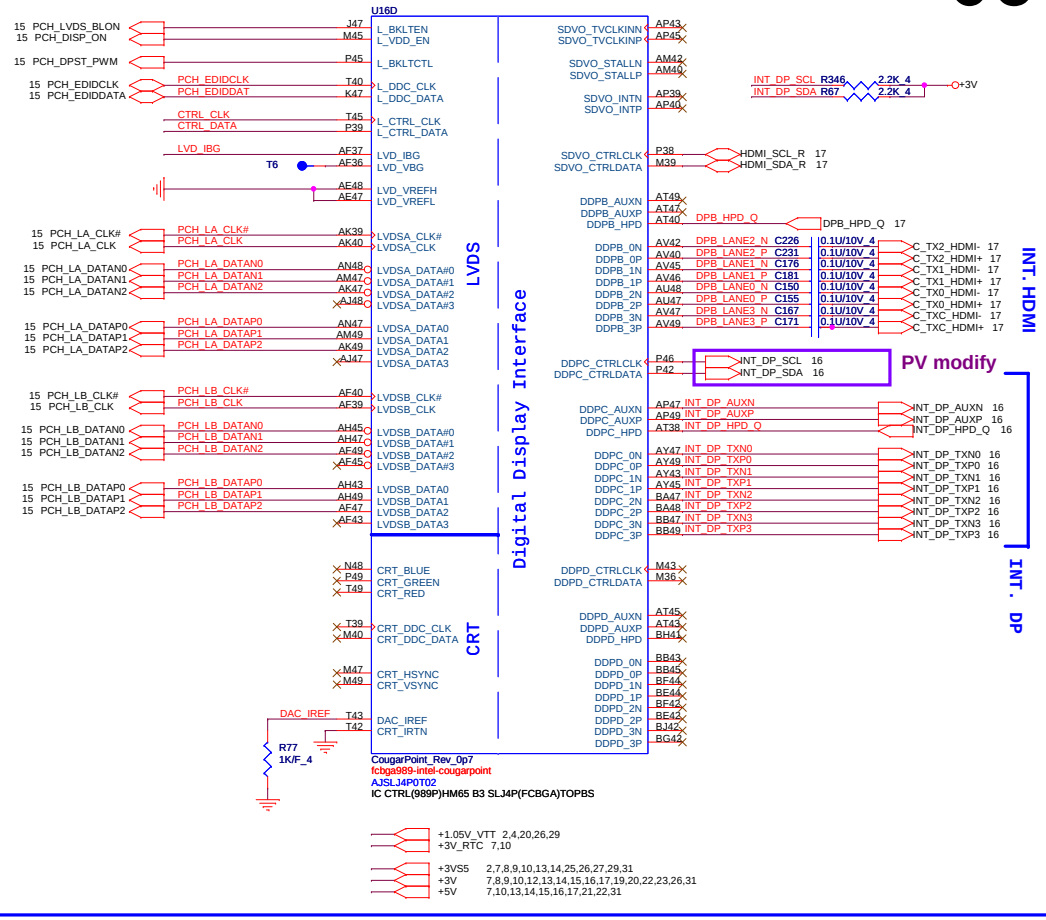
Cougar Point (DMI,FDI,PM)

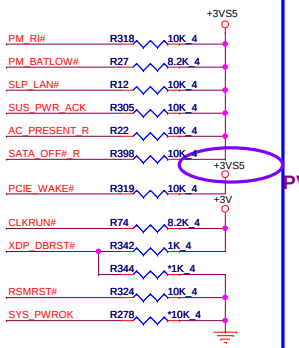
Cougar Point (LVDS,DDI)

06



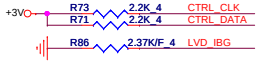


PCH Pull-high/low(CLG)

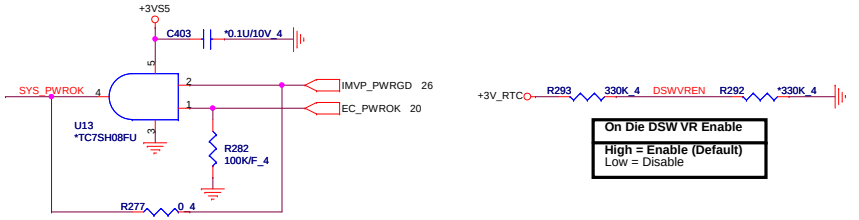


PV modify

INT LVDS & CRT disable (DIS only remove)



System PWR_OK(CLG)



On Die DSW VR Enable
High = Enable (Default)
Low = Disable

PROJECT : Stella			
Quanta Computer Inc.			
Size: Custom	Document Number: PCH 1/6 (DMI/FDI/VIDEO)		Rev: 1A
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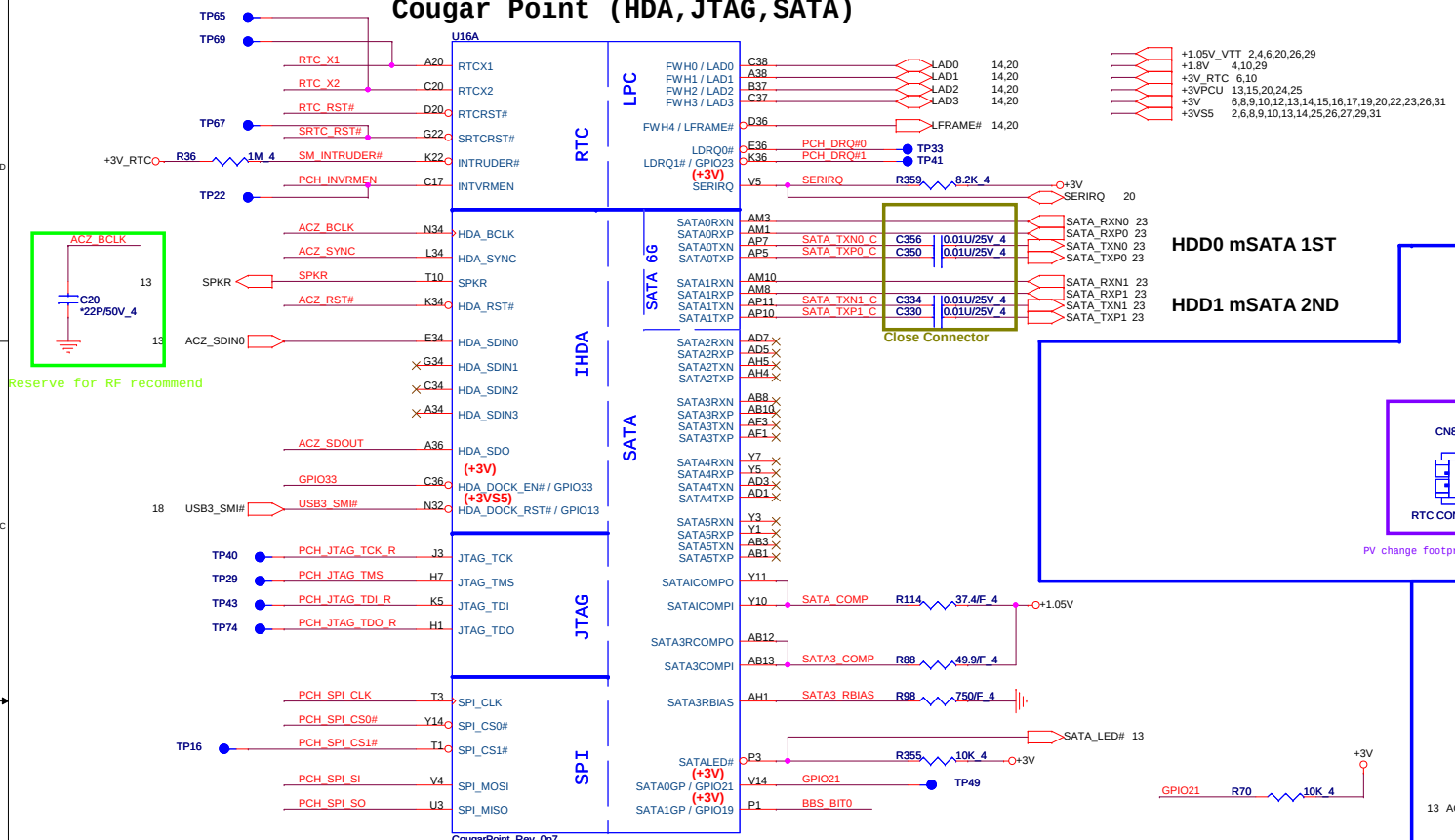
Cougar Point (HDA,JTAG,SATA)



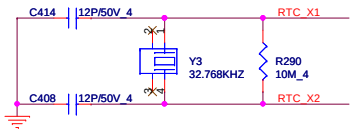
HDD0 mSATA 1ST

HDD1 mSATA 2ND

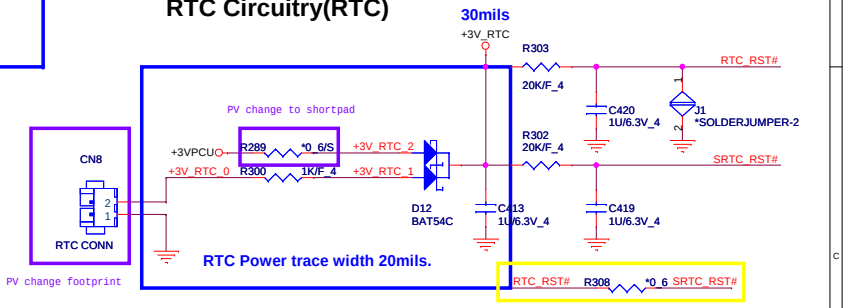
Close Connector

Reserve for RF recommend

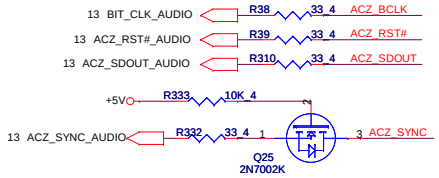
RTC Clock 32.768KHz



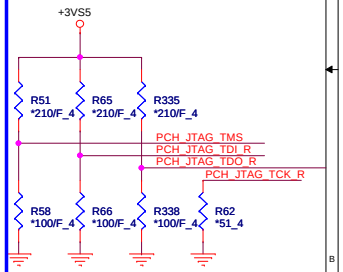
RTC Circuitry(RTC)



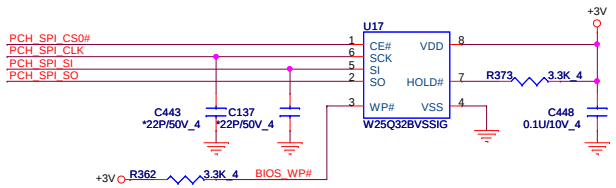
HDA Bus(CLG)



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



Vender	Size	P/N
EON	4MB	AKE39FN0Q00 (EN25F32-100HIP)
Winbond	4MB	AKE391P0N00 (W25Q32BVSSIG)
Socket		DG008000031

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR Different from Calpella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R87 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R31 *1K_4, R30 10K_4, +3V, PCI_GNT3# 8 — Bios request, for can't boot Capella 4/23.
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R41 330K_4 +3V_RTC
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	GPIO33 R326 *1K/F_4 GPIO33_E 20
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1#: 1 / GNT0#: 0 → Boot Location: SPI	[Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK	GNT1#: 1 / GNT0#: 1 → Boot Location: LPC	BBS_BIT0, R353 *1K_4, R339 *1K_4, BBS_BIT1 8
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)	+1.8V R119 *1K_4 NV_ALE 8 — Chief River change to 1K
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R117 2.2K_4, R118 4.7K_4, NV_CLE 8, H_SNB_IVB# 2
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3VS5 R29 1K/F_4 ACZ_SYNC
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	20 GPIO33_E ACZ_SDOUT R325 *1K_4 +3VS5
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)	R317 *1K_4 ICC_EN# 9
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R82 *1K_4 PLL_ODVR_EN 9
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable	PCH_SPI_SI R90 1K/F_4 +3V

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PROJECT : Stella

Quanta Computer Inc.

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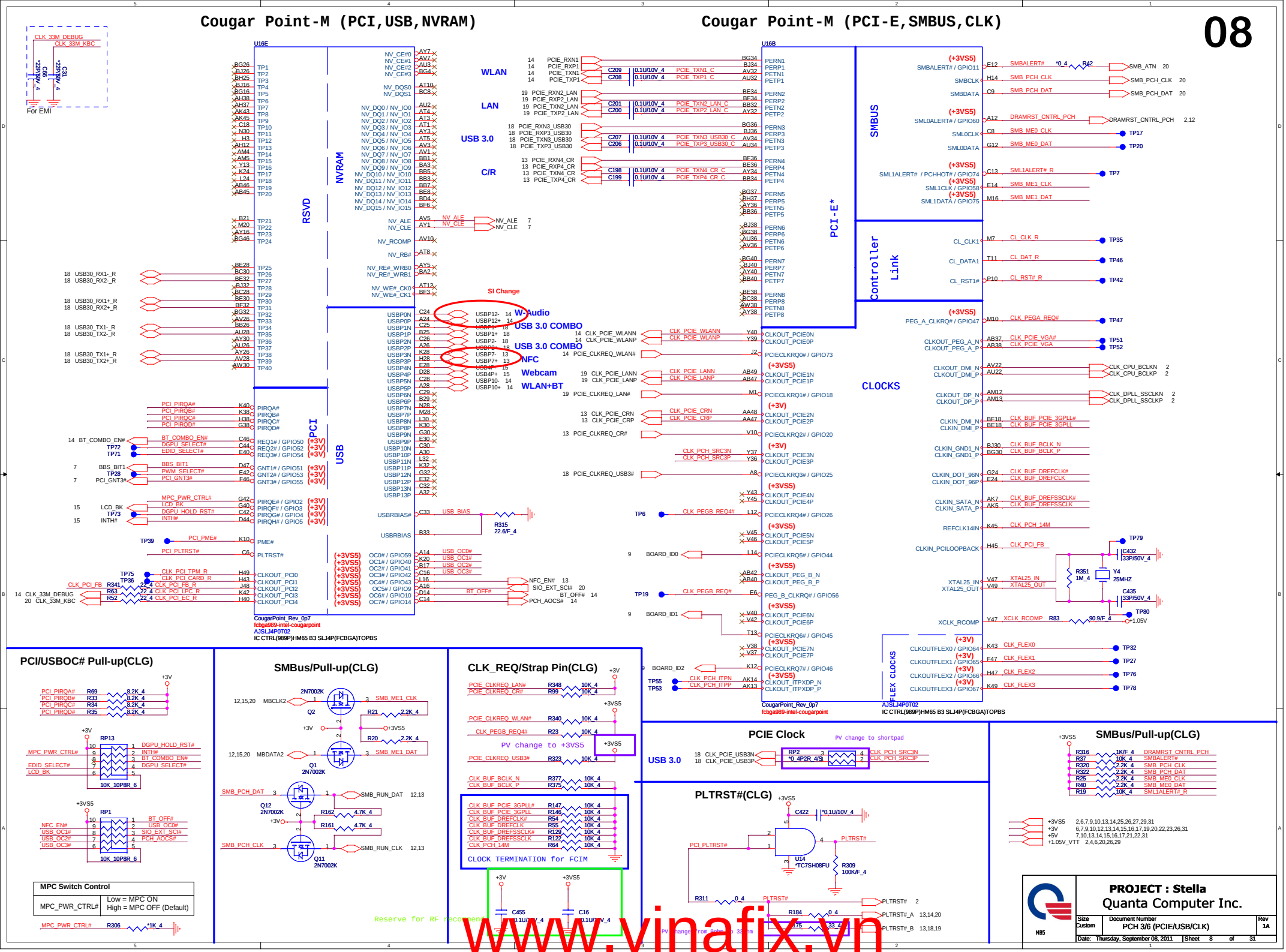
Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)

08



PCI/USBOC# Pull-up(CLG)

MPC Switch Control	
MPC_PWR_CTRL#	Low = MPC ON High = MPC OFF (Default)

MPC_PWR_CTRL# R306 *1K_4

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

PCIE Clock

PLTRST#(CLG)

SMBus/Pull-up(CLG)

+3VS5 2,6,7,9,10,13,14,25,26,27,29,31
+3V 6,7,9,10,12,13,14,15,16,17,19,20,22,23,26,31
+5V 7,10,13,14,15,16,17,21,22,31
+1.05V_VTT 2,4,6,20,26,29

N85	PROJECT : Stella Quanta Computer Inc.		
Size: Custom	Document Number: PCH 3/6 (PCIE/USB/CLK)		Rev: 1A
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Cougar Point (GPIO,VSS_NCTF,RSVD)

Clock Gen Power OK (CLG)

PV change to shortpad

SI add for HP request

U16F

GPIO

CPU/MISC

NCTF

DG rev0.9 suggest to TS_VSS connect to GND 4/23.

CougarPoint_Rev_0p7 IC CTRL(989P)HM65 B3 SLJ4P(FCBGA)TOPBS
fcbga989-intel-cougarpoint
AJSLJ4P0T02

+3VS5 2,6,7,8,10,13,14,25,26,27,29,31
+3V 6,7,8,10,12,13,14,15,16,17,19,20,22,23,26,31

BOARD ID SETTING

BOARD ID SETTING	BOARD_ID0 GPIO 44	BOARD_ID1 GPIO 45	BOARD_ID2 GPIO 46
HR	0	0	0

8 BOARD_ID0 BOARD_ID0 GPIO 44
8 BOARD_ID1 BOARD_ID1 GPIO 45
8 BOARD_ID2 BOARD_ID2 GPIO 45

RD0 R11 10K_4 BOARD_ID0 R10 *10K_4 RU0 +3VS5
RD1 R13 10K_4 BOARD_ID1 R14 *10K_4 RU1
RD2 R15 10K_4 BOARD_ID2 R3 *10K_4 RU2

MFG-TEST

MFG_MODE R350 10K_4 +3V

S_GPIO R108 10K_4 +3V

GPIO Pull-up/Pull-down(CLG)

LAN_DISABLE# R328 10K_4 +3VS5

SIO_EXT_SMI# R312 10K_4 +3V
EC_A20GATE R75 10K_4
EC_RCIN# R81 10K_4
GPIO70 R314 1.5K/F_4
WAUDIO_OFF# R321 1.5K/F_4

GPIO49 R68 10K_4
SATA_OFF# R32 10K_4
TP_SCI# R402 10K_4

GPIO27 R56 10K_4

RF_OFF# R26 1K/F_4 +3VS5

Intel ME Crypto Transport Layer Security (TLS) cipher suite
Low = Disable (Default) High = Enable

R85 *0_4 BIOS_REC R89 10K_4 +3V

BIOS RECOVERY	High = Disable (Default) Low = Enable

R112 *0_4 TEST_SET_UP R110 10K_4 +3V

SV_SET_UP
High = Strong (Default)

R17 100K/F_4 SV_DET R18 *10K_4 +3V

TEST DETECT
Low = Default

PCH_GPIO36 R91 *10K_4 +3V

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

R60 100K/F_4 FDI_OVRVLTG

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

PROJECT : Stella
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 4/6 (GPIO/MISC)	1A

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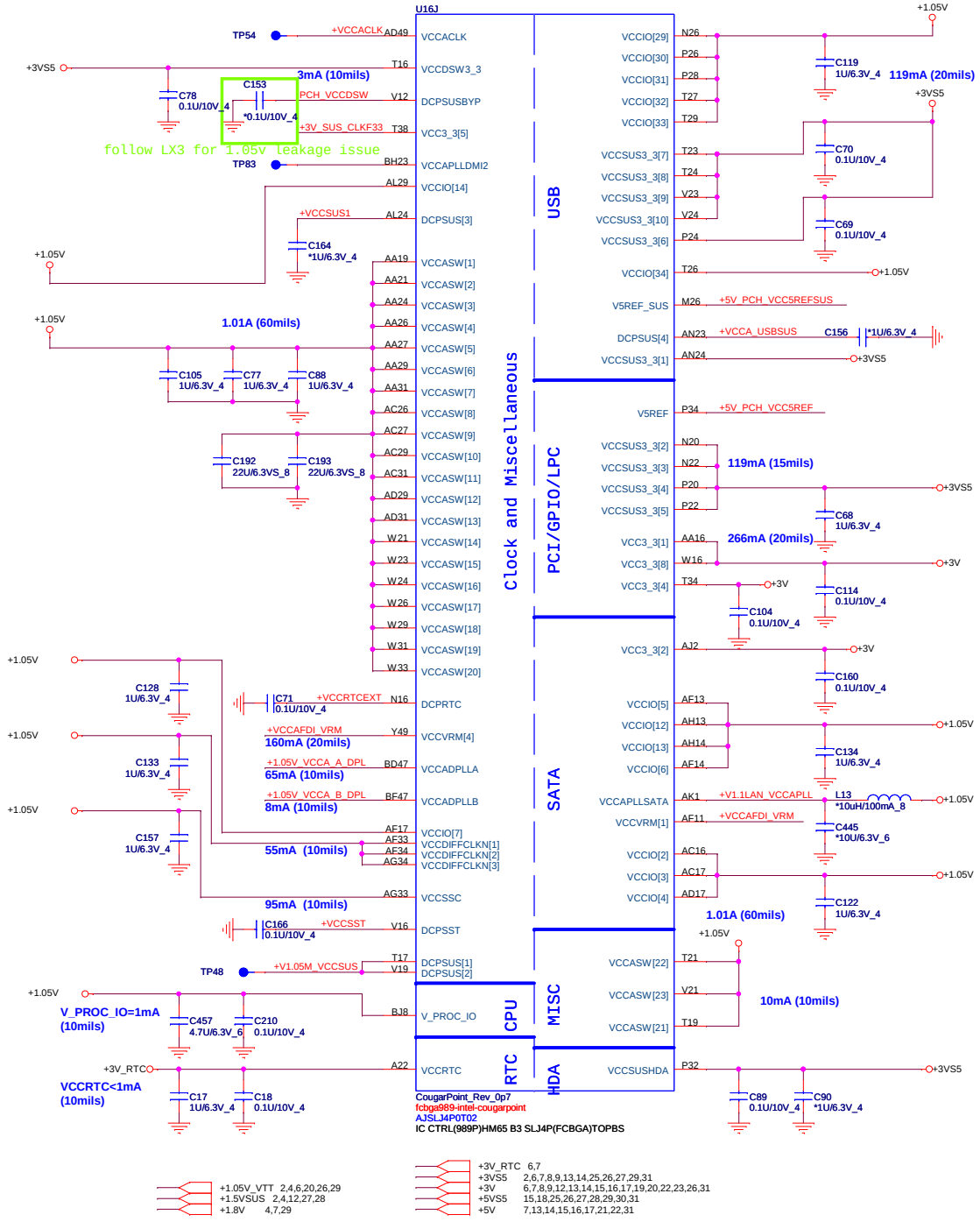
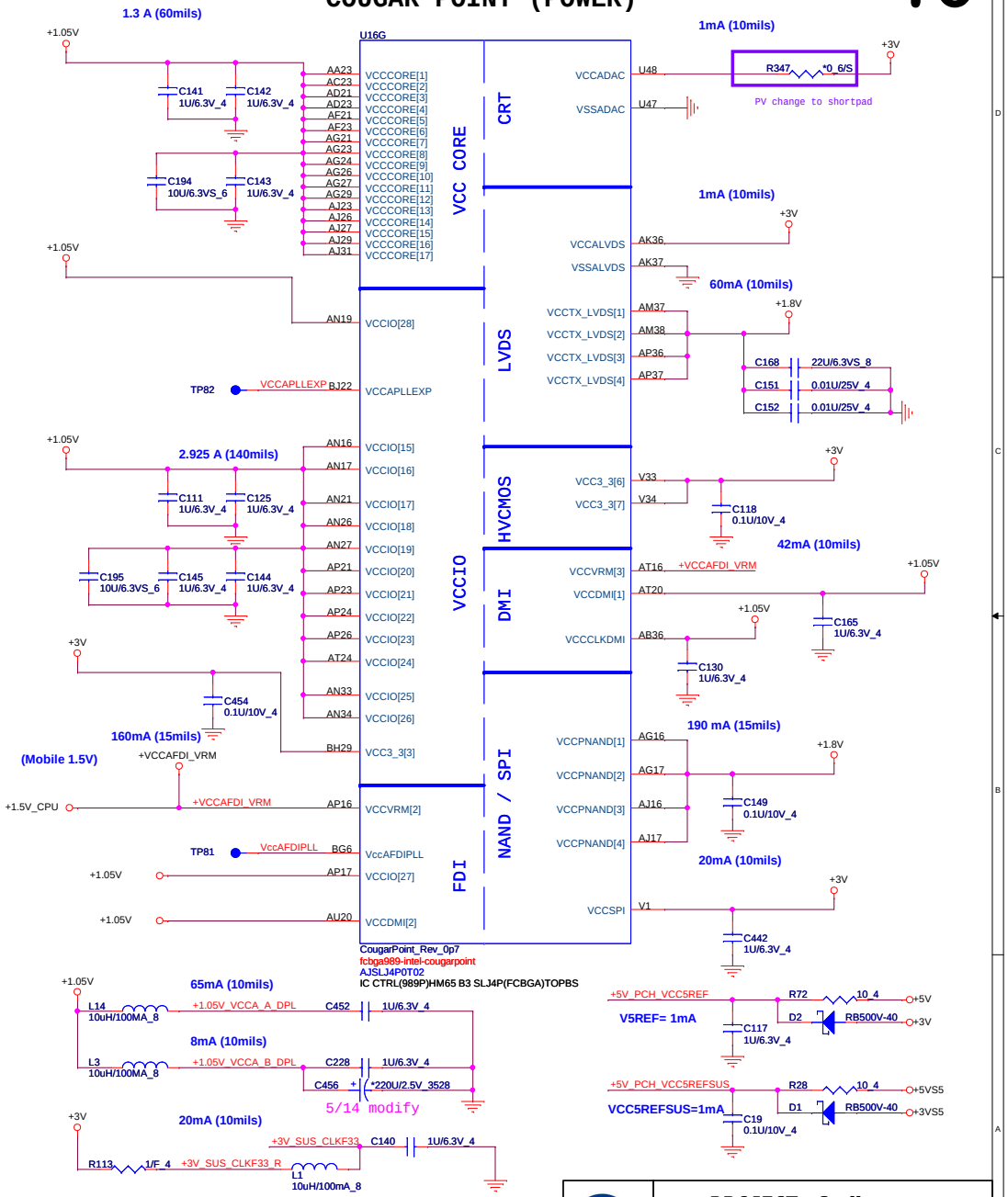
Cougar Point-M (POWER)



COUGAR POINT (POWER)



PROJECT : Stella			
Quanta Computer Inc.			
Size: Custom	Document Number: PCH 5/6 (POWER)		Rev: 1A
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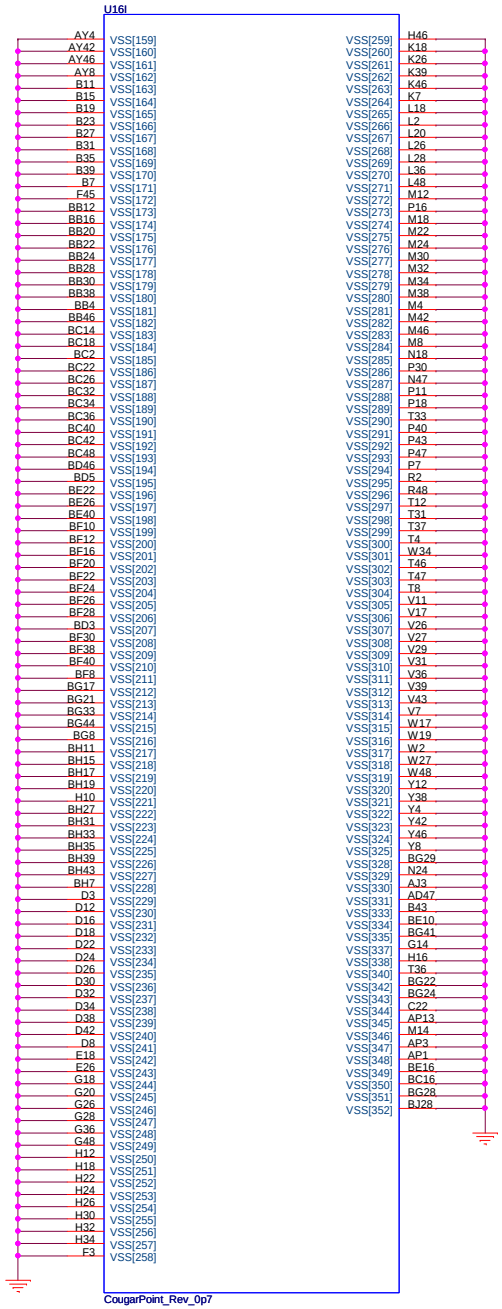
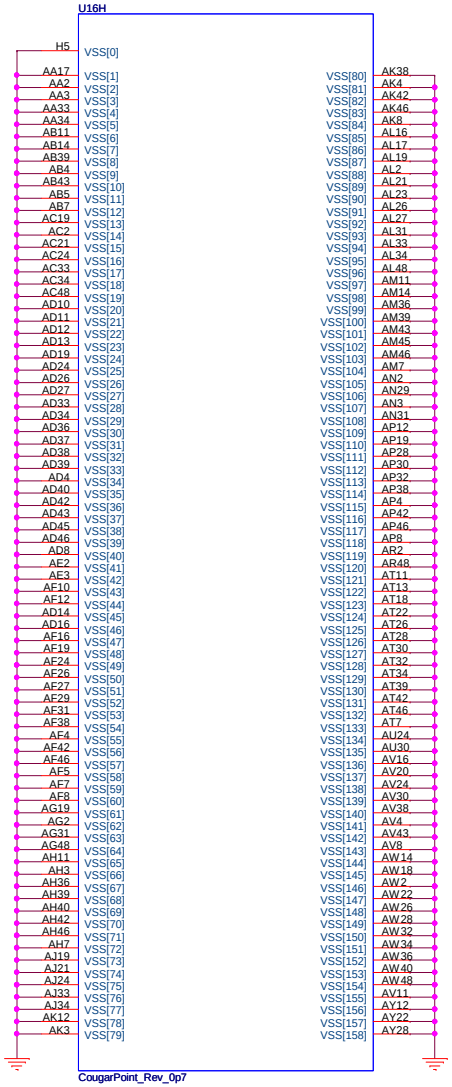
IBEX PEAK-M (GND)



IBEX PEAK-M (GND)



PROJECT : Stella
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 6/6 (GND)	1A

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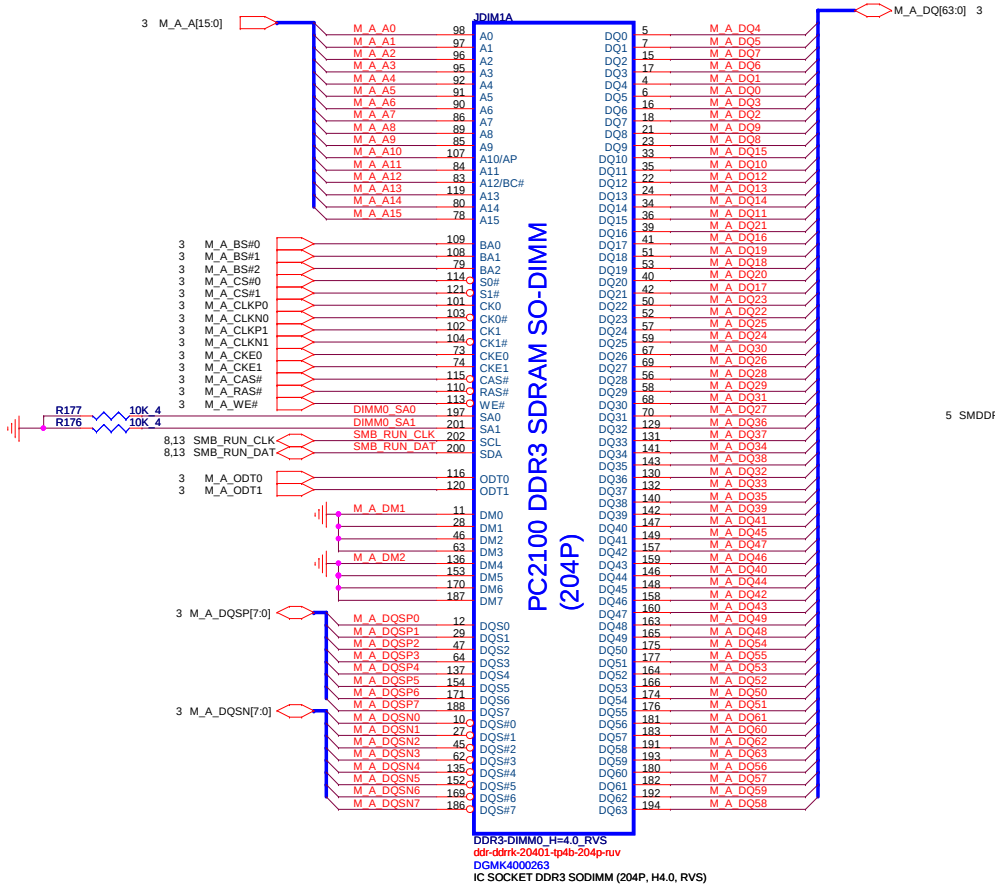

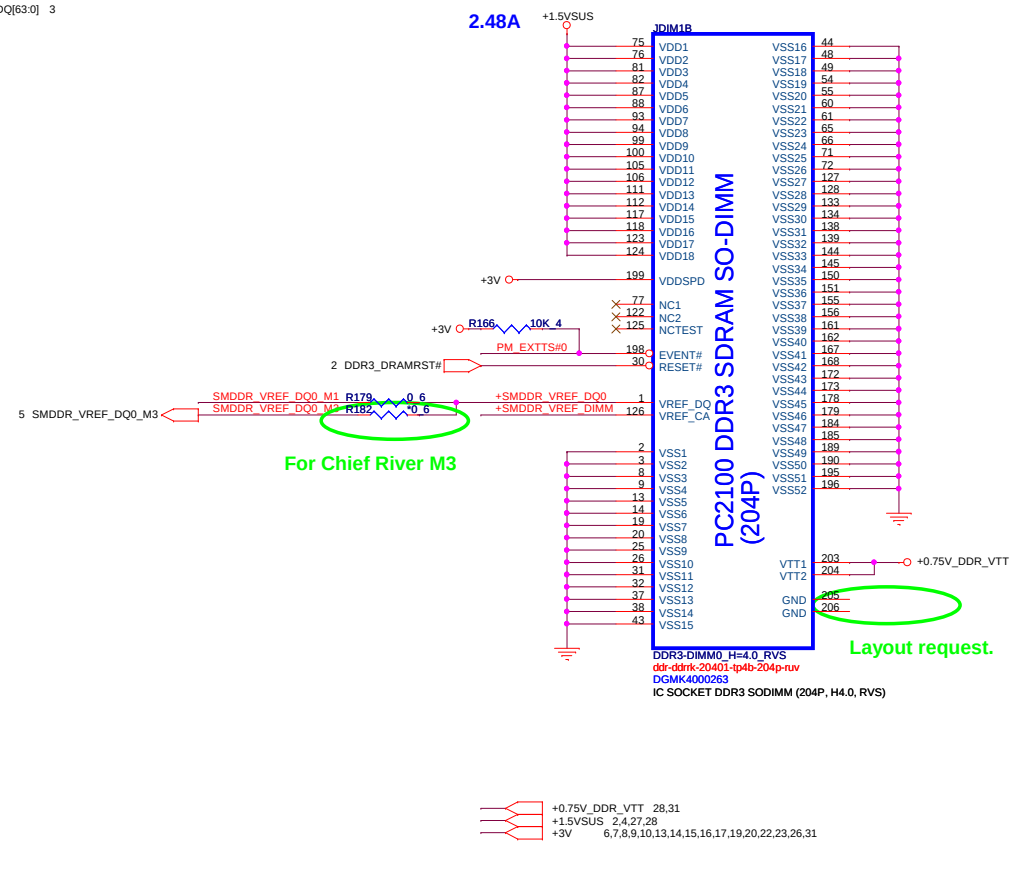

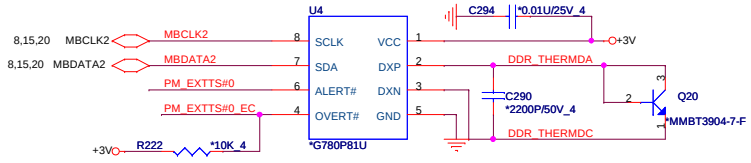

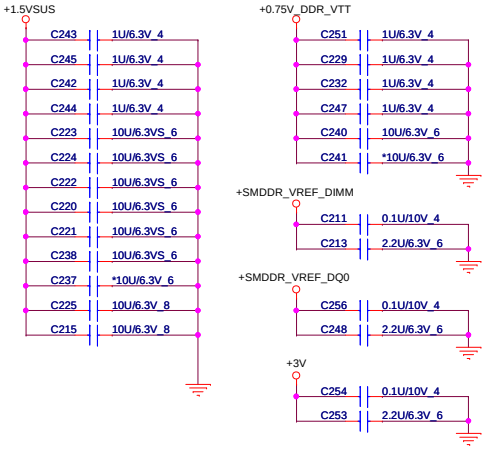

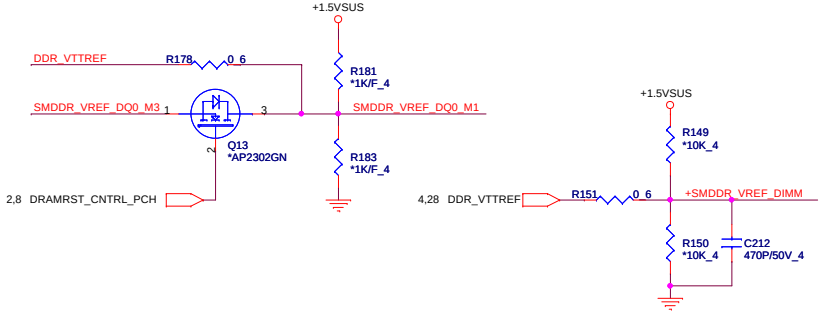

PROJECT : Stella

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-STD (5.2H)	1A

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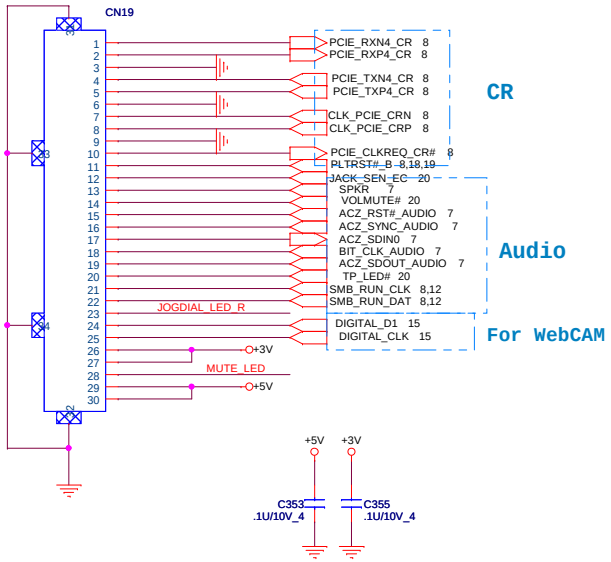
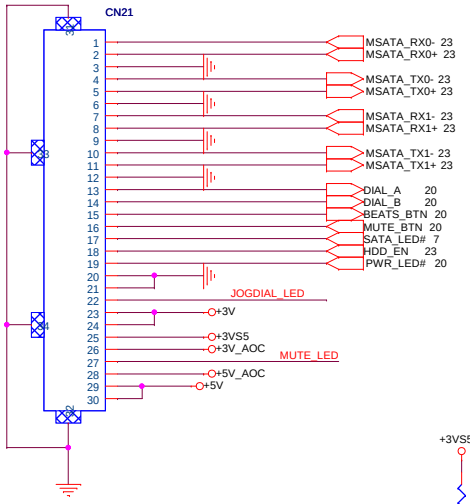
FOR AUDIO/CR



FOR mSATA

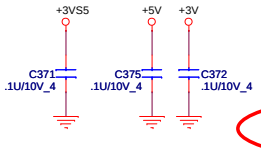


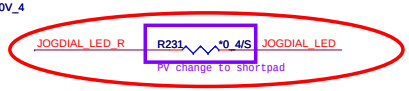
mSATA 1ST

mSATA 2ND

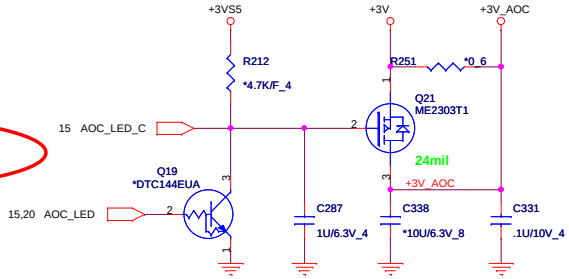
JogDial

Mute Button

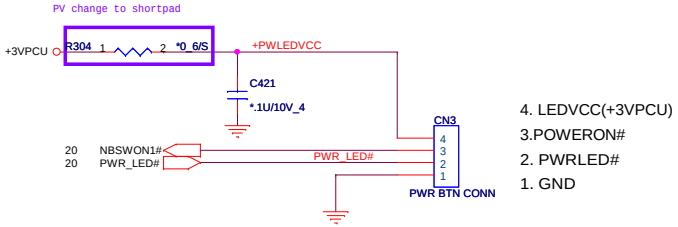




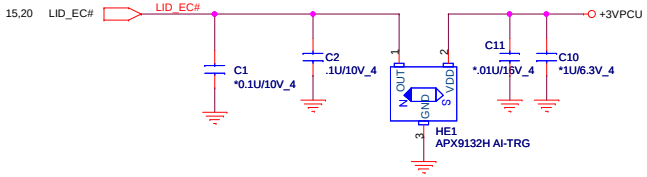
SI add



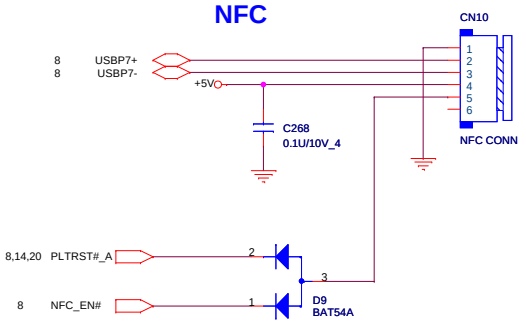
POWER BUTTON

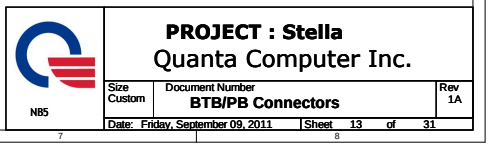


4. LEDVCC(+3VPCU)
3.POWERON#
2. PWRLED#
1. GND

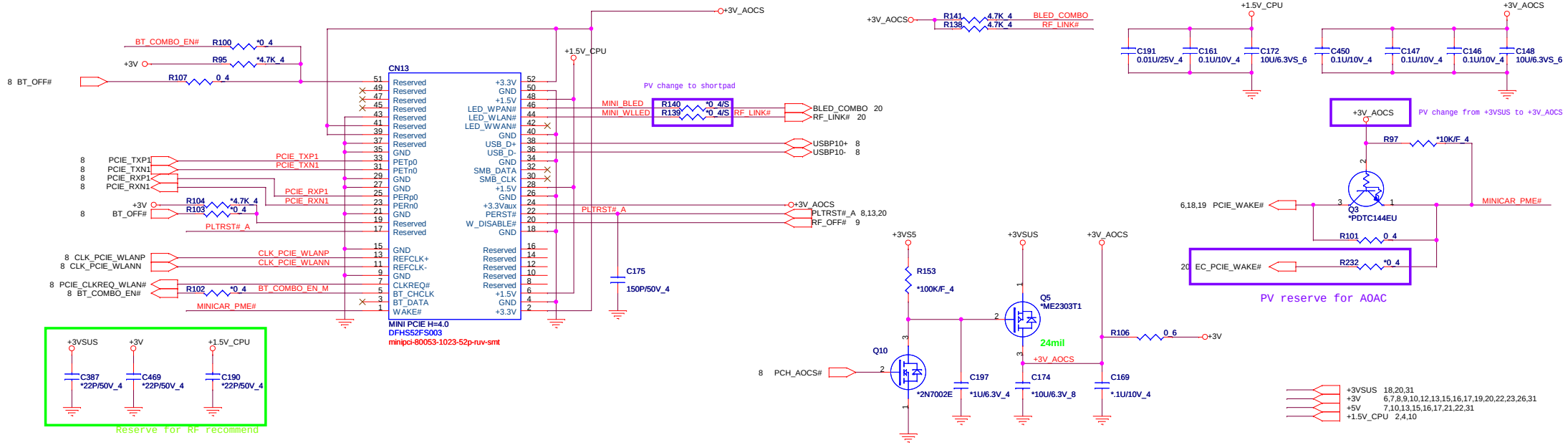


NFC

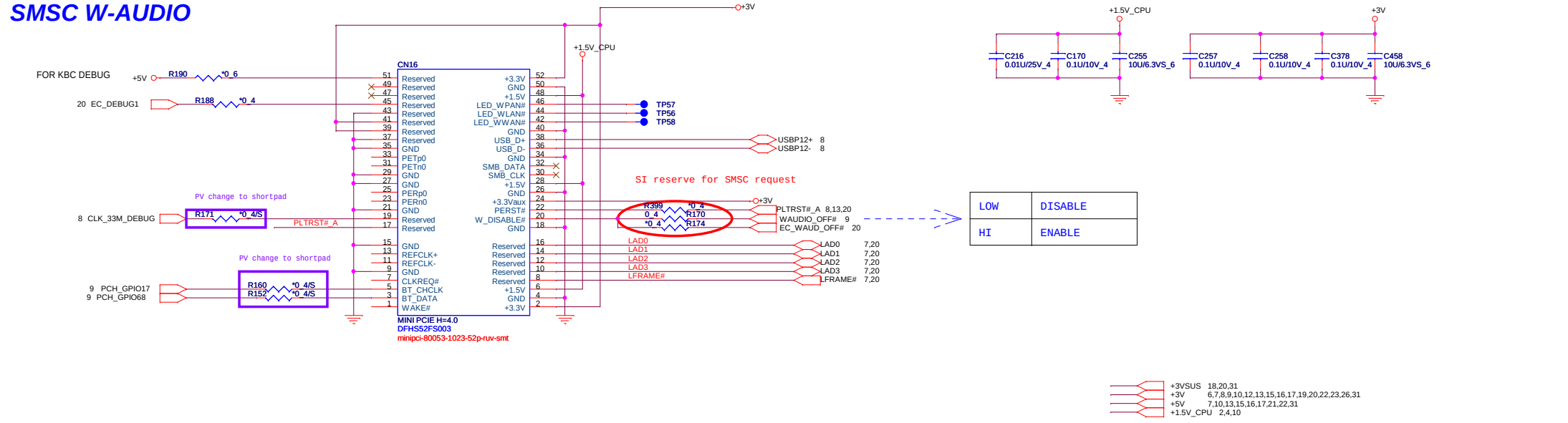




Mini PCI-E Card 1 WLAN+BT



Mini PCI-E Card 1
SMSC W-AUDIO



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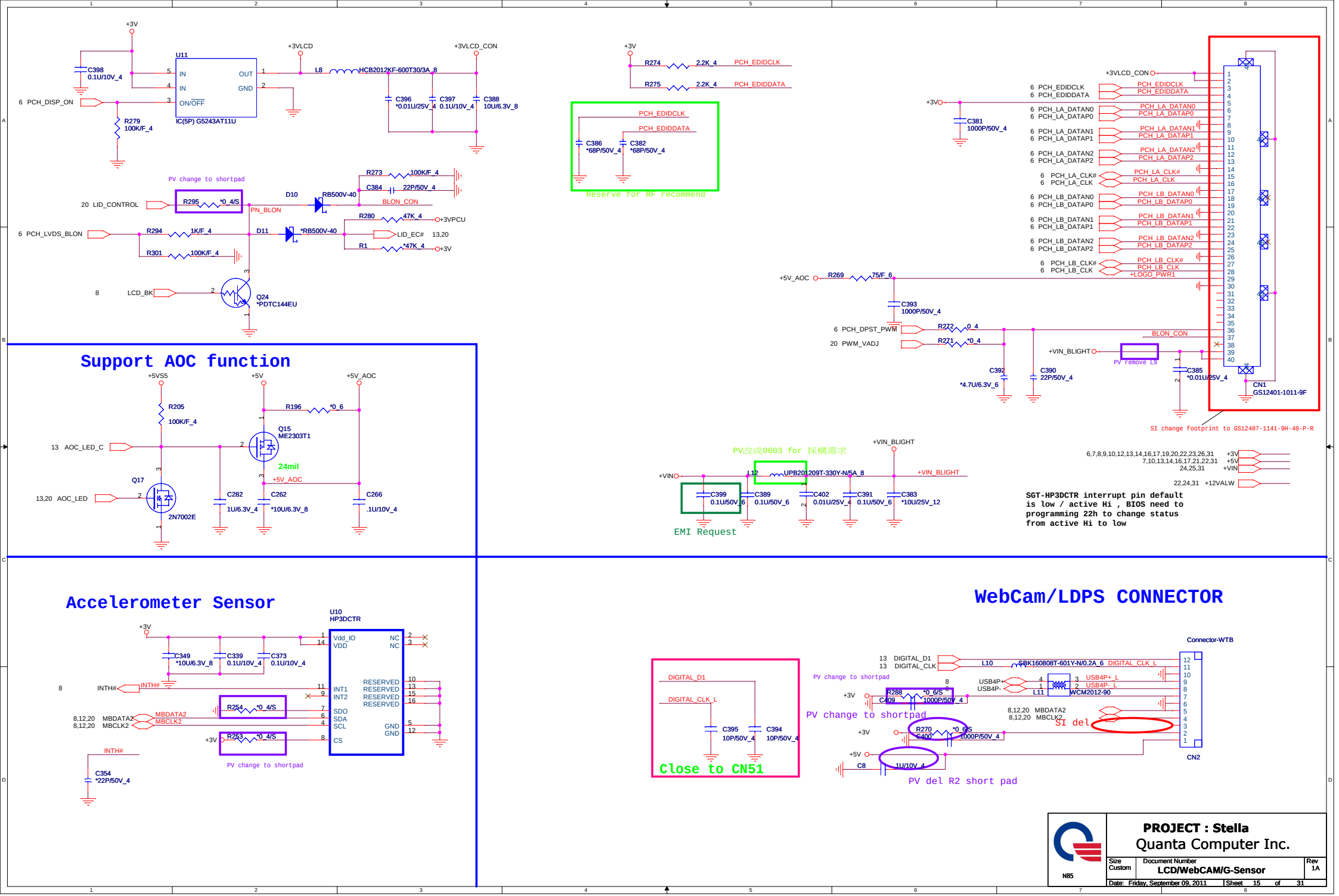
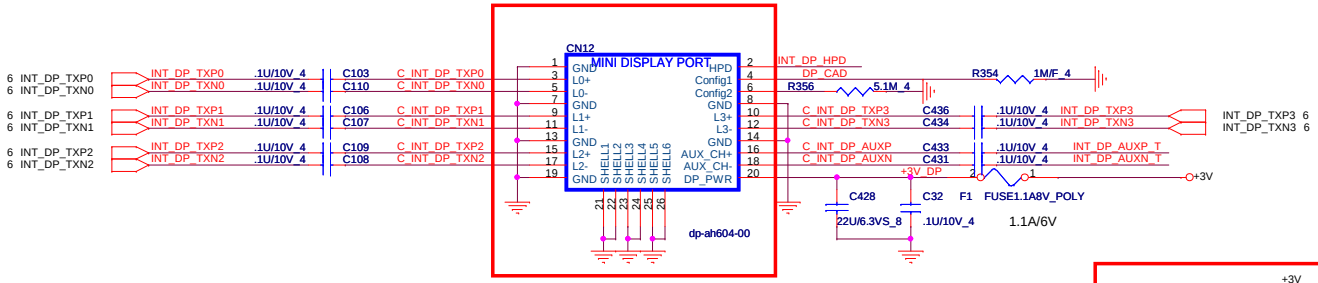
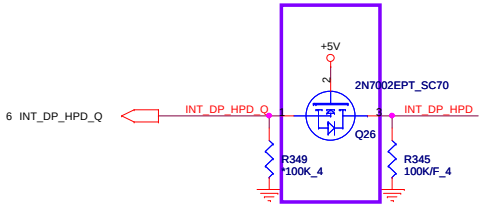


+5V 7,10,13,14,15,17,21,22,31
+3V 6,7,8,9,10,12,13,14,15,17,19,20,22,23,26,31

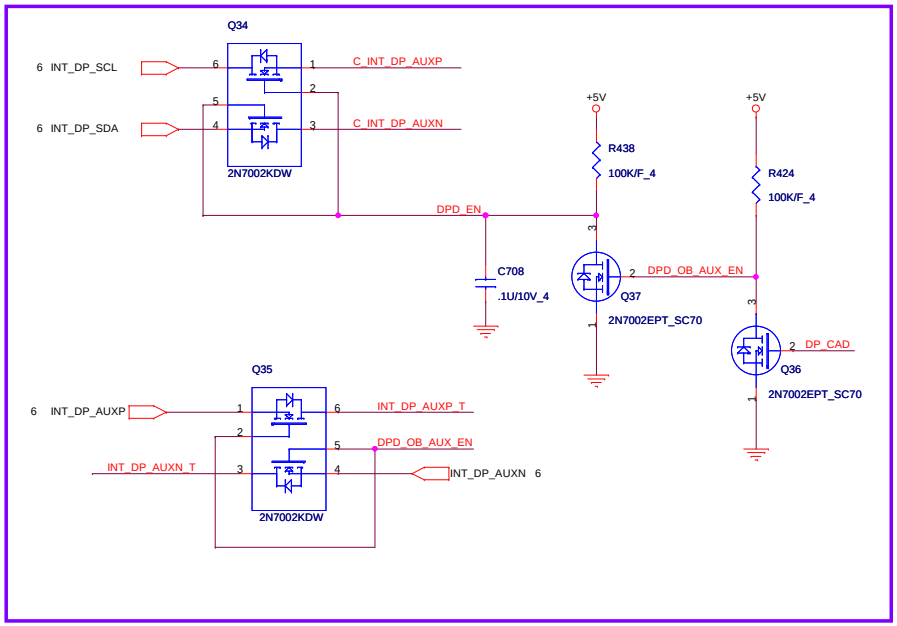
Mini Display



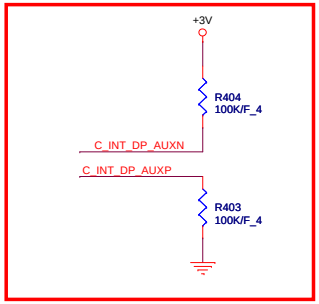
SI change footprint



PV change footprint to SC70



PV add for mini-display to HDMI dongle support



SI add for intel recommend

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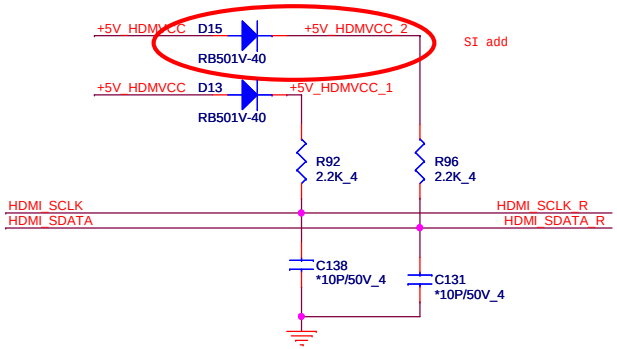
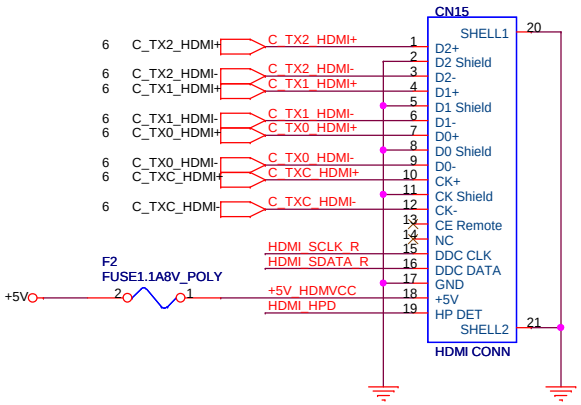
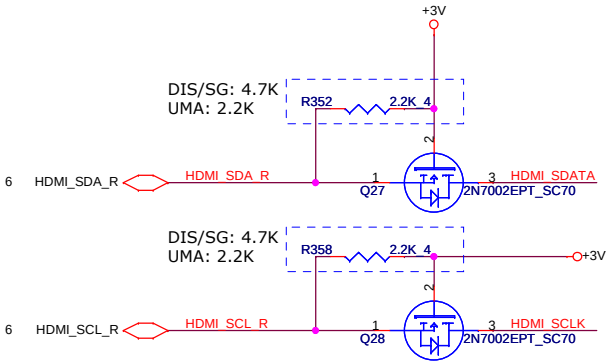
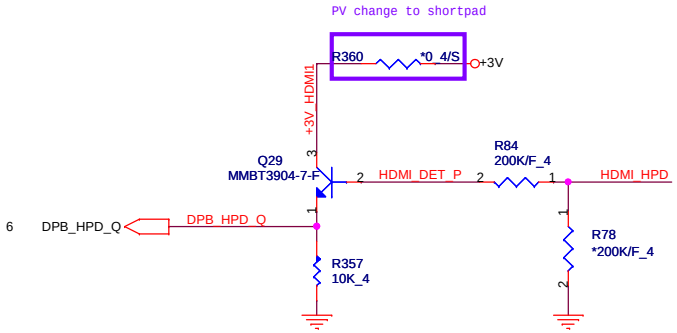
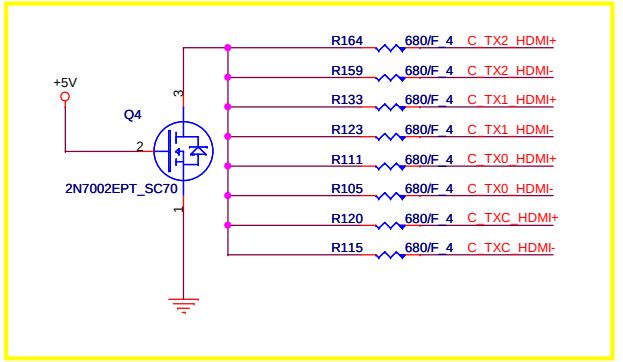
HDMI CON_COM

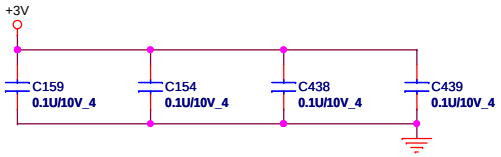


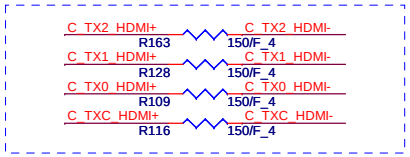












EMI Suggestion

7,10,13,14,15,16,21,22,31 +5V
6,7,8,9,10,12,13,14,15,16,19,20,22,23,26,31 +3V

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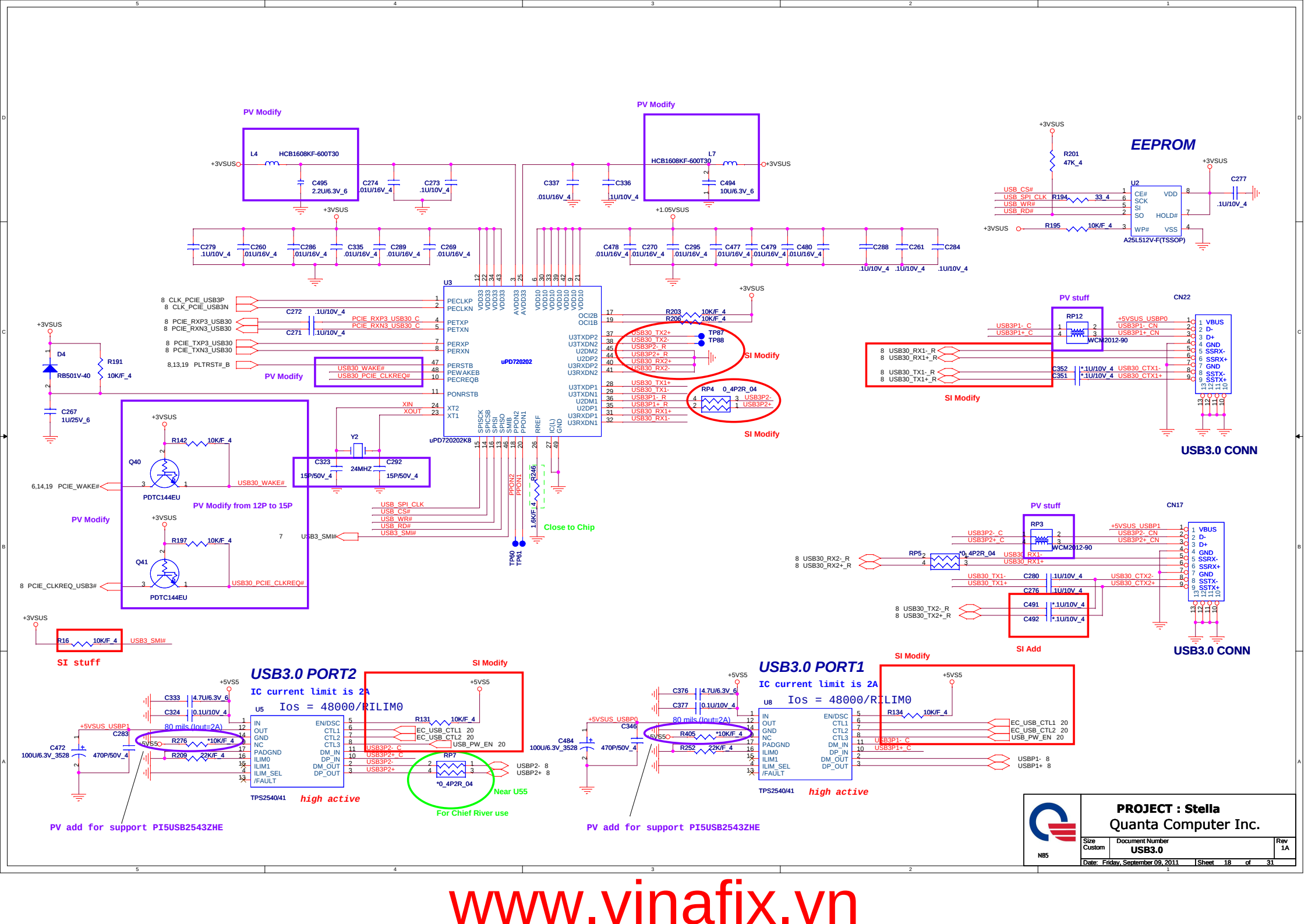
NB5



For EMI 0 ~ 22 ohm

RF recommend close PU8 Pin5

GND VIA x 9 Pcs

U1 RTL8111E-VL-CG

PV Change to RTL8111E-VL-CG

U19 NS892405

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

IND SMD 4.7UH +-20% 680MA(CBC2518T4R7M)
CV-4707MZ00

SI modify to use 0.8H part

>60mil

>60mil Power trace Layout 寬度> 60mil

Trace<30 mil
Width > 60 mil

Close to Pin 21

2P Amber LED(Side-View)

(Amber)

2P WHITE LED(Side-View)

(White)

朝前

EMI request

PV change to shortpad

RJ45

RJ45_CONN

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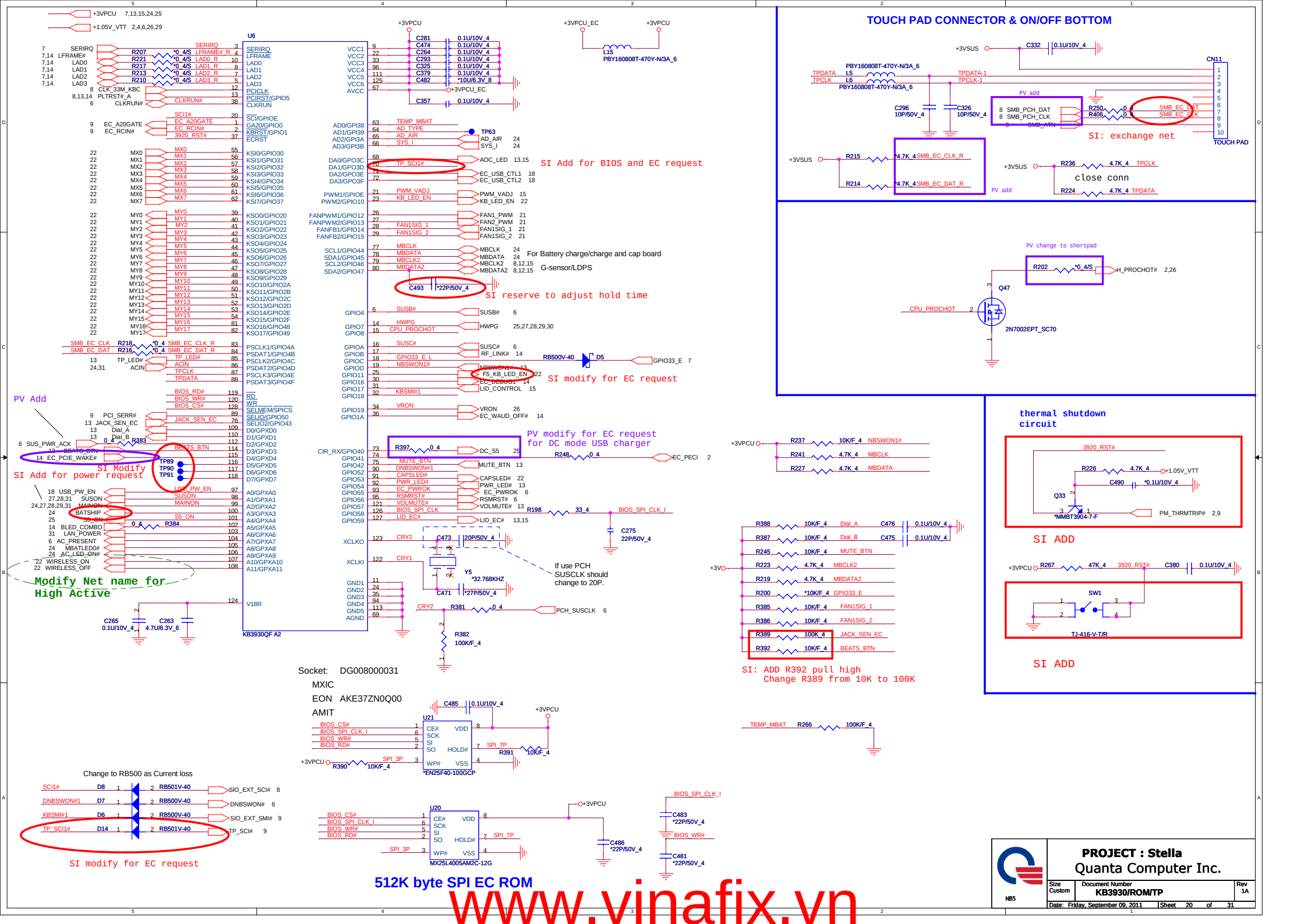
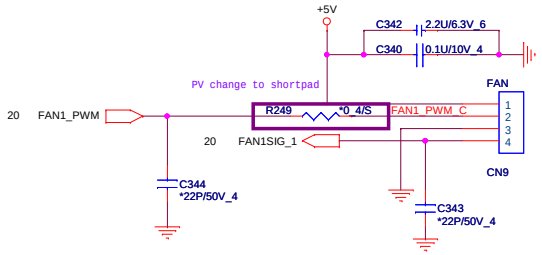
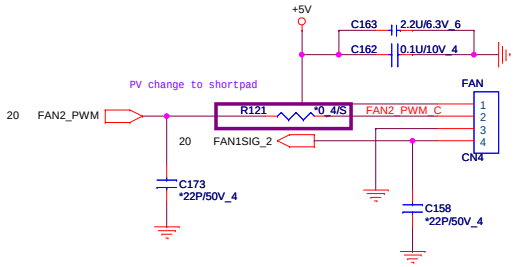
NB5


TOUCH PAD CONNECTOR & ON/OFF BOTTOM
SI: exchange net
close conn
SI Add for BIOS and EC request
SI reserve to adjust hold time
SI modify for EC request
PV modify for EC request for DC mode USB charger
PV Add
SI Modify
SI Add for power request
Modify Net name for High Active
thermal shutdown circuit
SI ADD
SI ADD
SI: ADD R392 pull high
Change R389 from 10K to 100K
Change to RB500 as Current loss
SI modify for EC request
512K byte SPI EC ROM
Socket: DG008000031
MXIC
EON AKE37ZN0Q00
AMIT
PROJECT : Stella
Quanta Computer Inc.
KB3930/ROM/TP
Friday, September 09, 2011
www.vinafix.vn

CPU FAN1



CPU FAN2



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KEYBOARD

SI Add for save power

20 WIRELESS_OFF
20 WIRELESS_ON
Q49 PDTC144EU
Q50 PDTC144EU
IMD2 Q22
IMD2 Q23
White_ON#
Amber_ON#

SI Add for F5 keyboard light function

KEYBOARD BACK LIGHT

PV change from 0ohm to 470ohm
PV change footprint from 0805 to 1210 and change 0ohm to 10ohm
20 F5_KB_LED_EN
20 KB_LED_EN
140 mA
+5V_F5_LED
+5V_LED_KBLIGHT
PIN 8,7,4 NC
SI add for EC request
SI change CN7 from 4pin to 8pin
KB LIGHT CONN
CN7
Caps led
Wireless LED

KB CONN
CN6
20 CAPSLED#
20 MY[0..17]
20 MX[0..7]

PV del H1 gnd pad
SI change footprint for ME request.

+3V 6,7,8,9,10,12,13,14,15,16,17,19,20,23,26,31
+5V 7,10,13,14,15,16,17,21,31
+12VALW 24,31

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Quanta Computer Inc.

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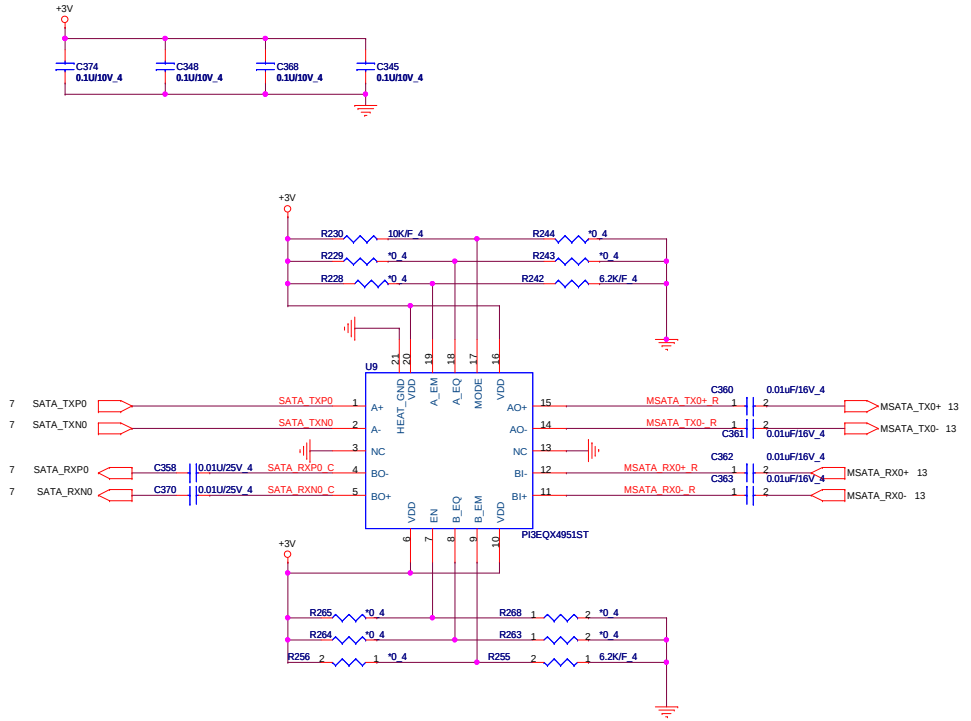
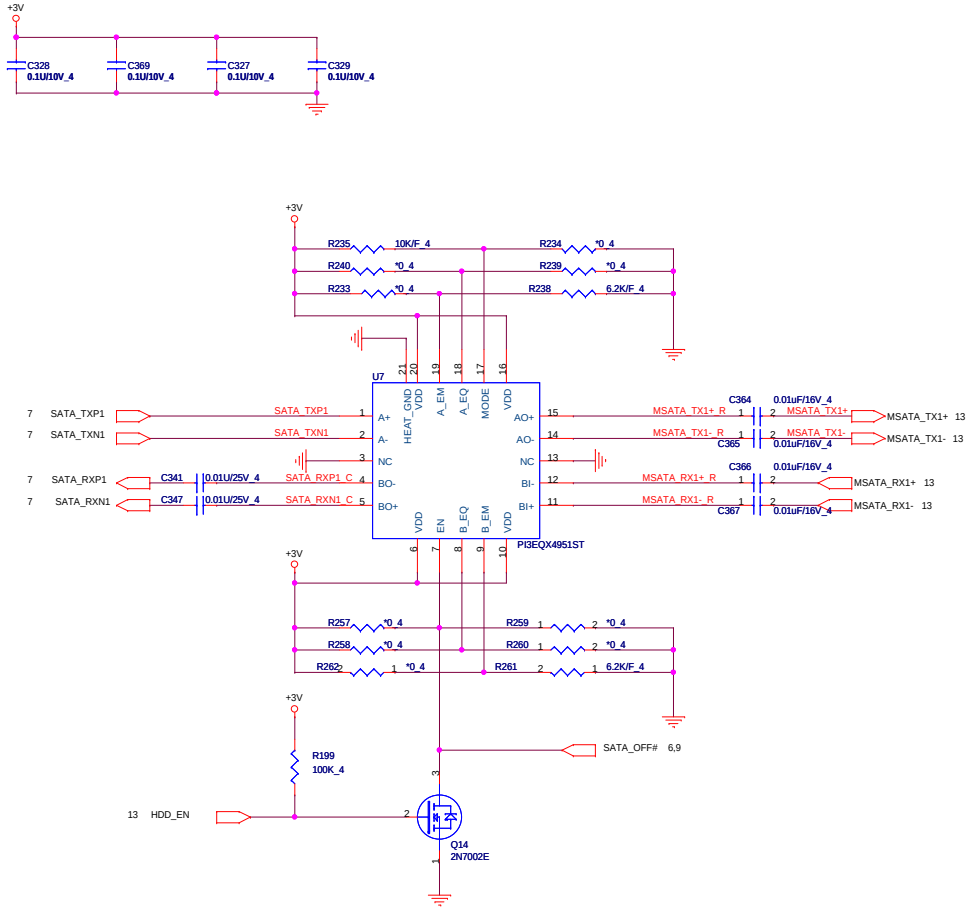
N85

HDD0 mSATA 1ST



HDD1 mSATA 2ND



N85	PROJECT : Stella Quanta Computer Inc.	
Size: Custom	Document Number: Azalia 92HD80	Rev: 1A
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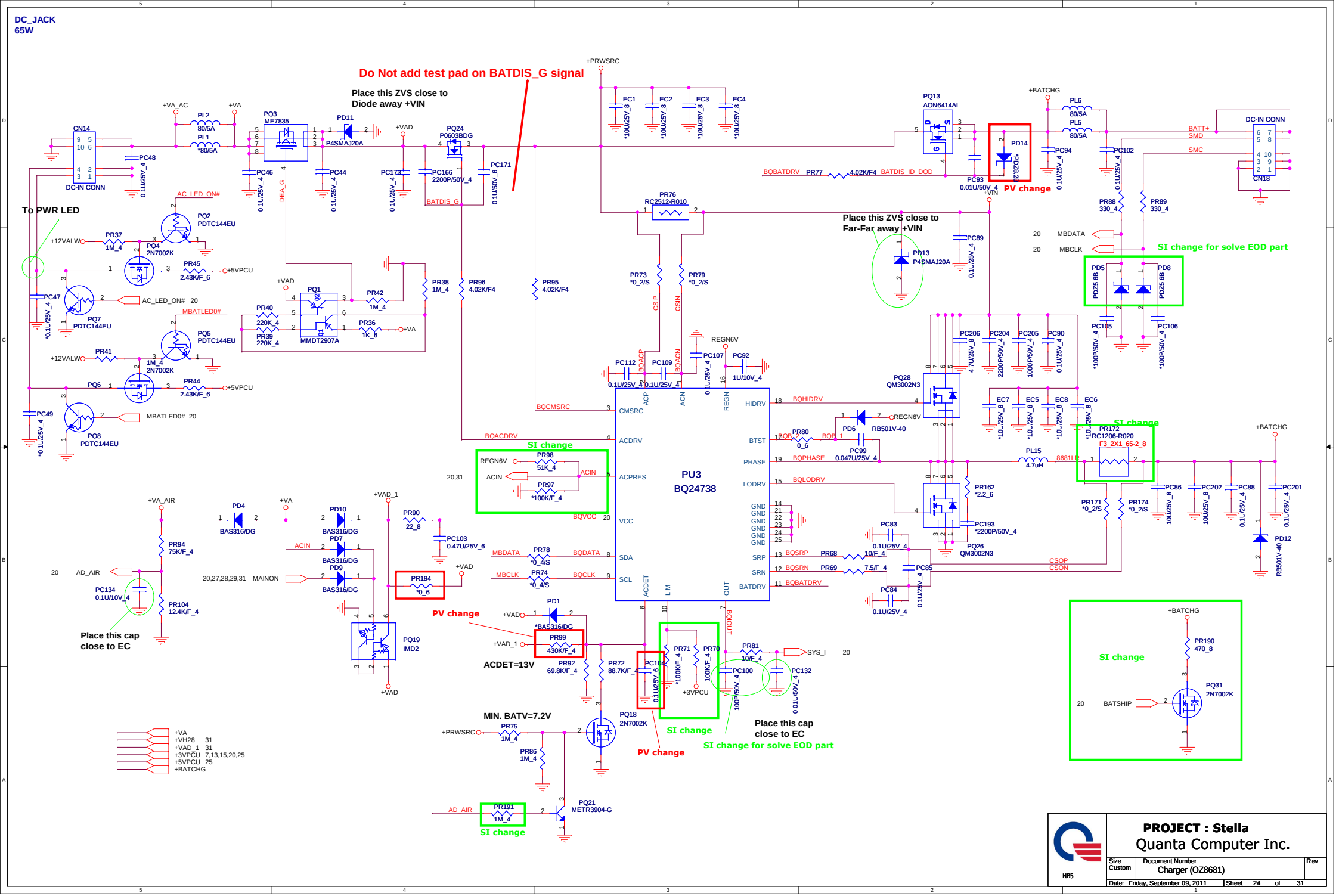
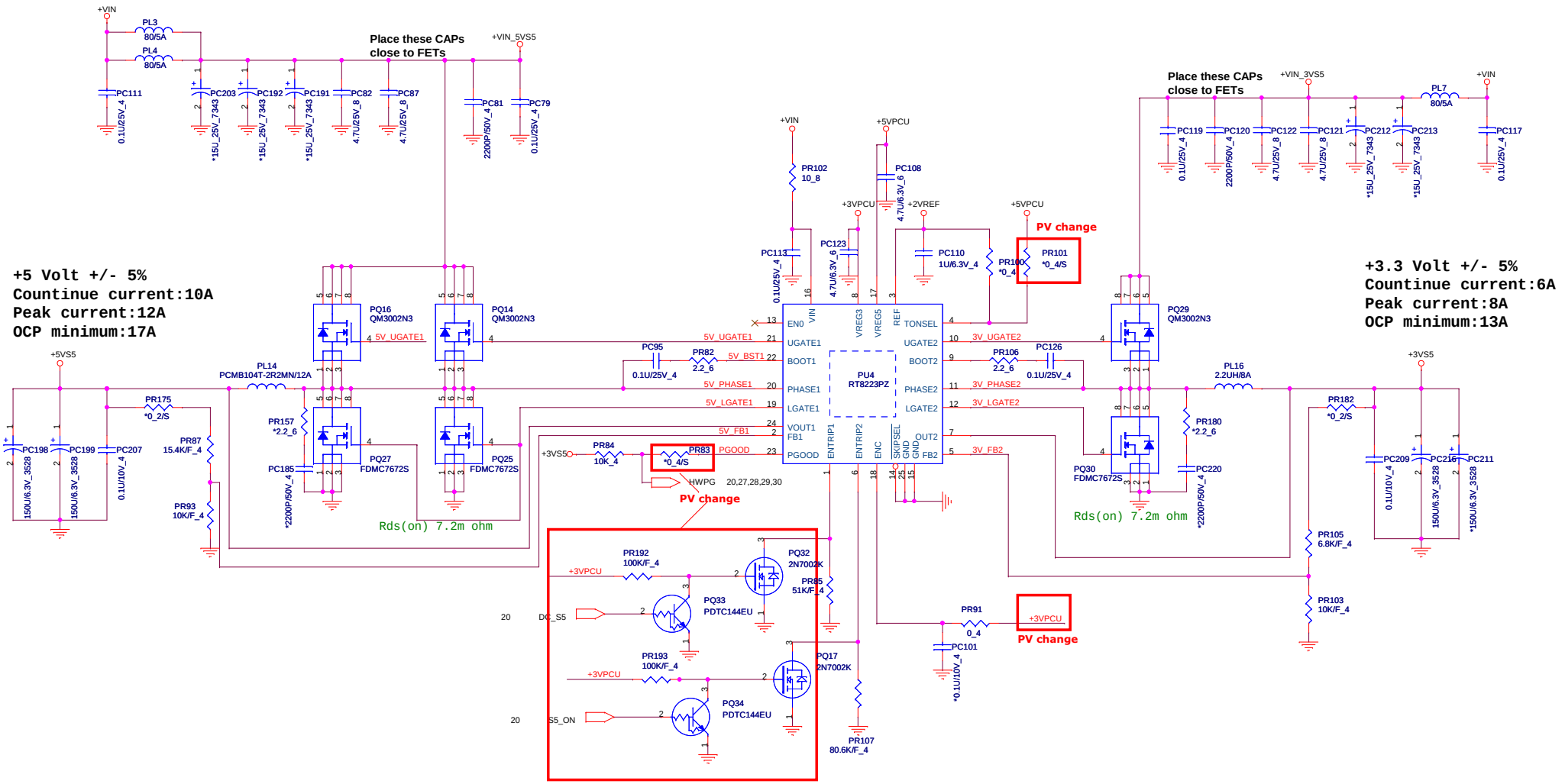


DC/DC +3VS5/+5VS5



Quanta Computer Inc.	PROJECT : Stella	
N85	Size: Custom; Document Number: +5V/+3V (RT8206B)	Rev: 1A
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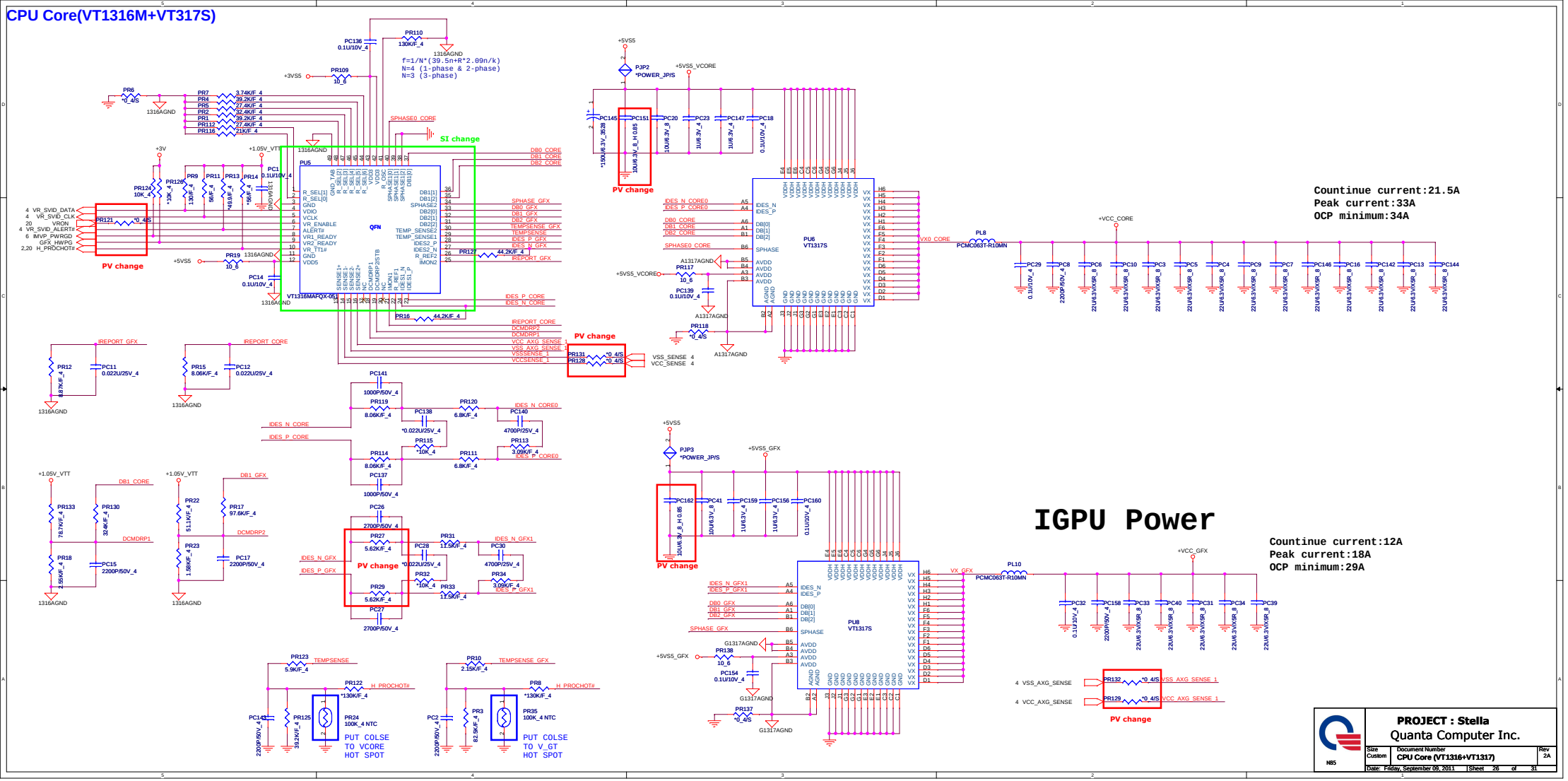
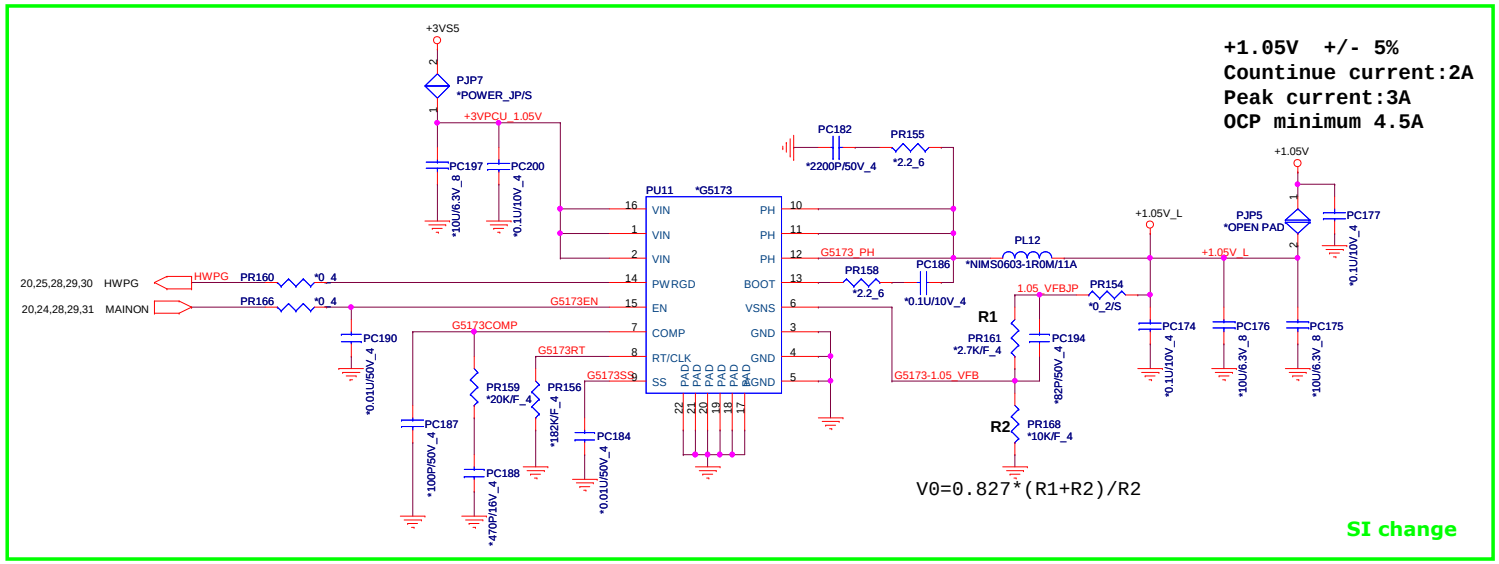
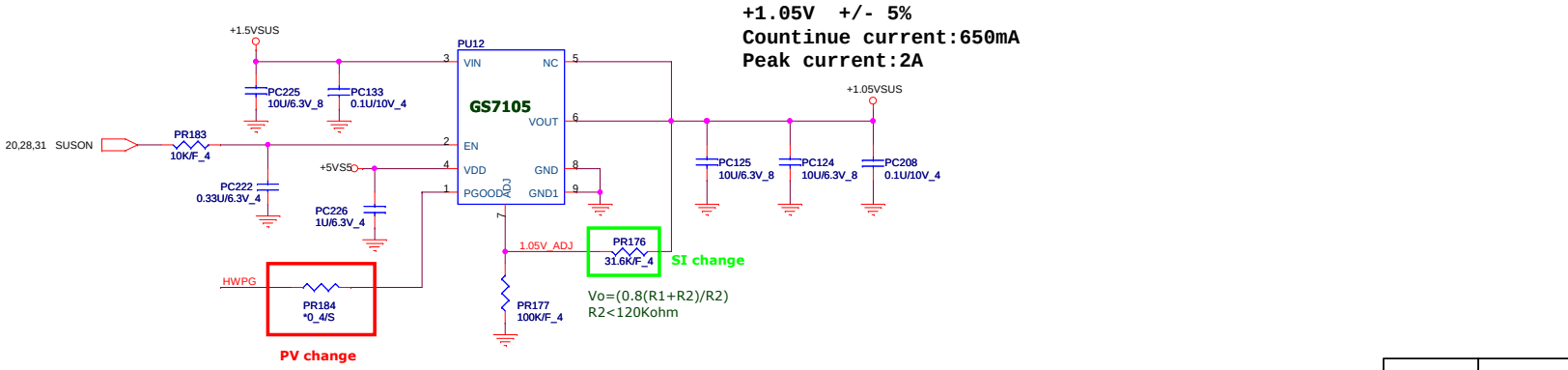
CPU Core(VT1316M+VT317S)



VCCP1.05V





Quanta Computer Inc.	PROJECT : Stella	
NB5	1.05V(G5173)/1.2V(G9661)	1A
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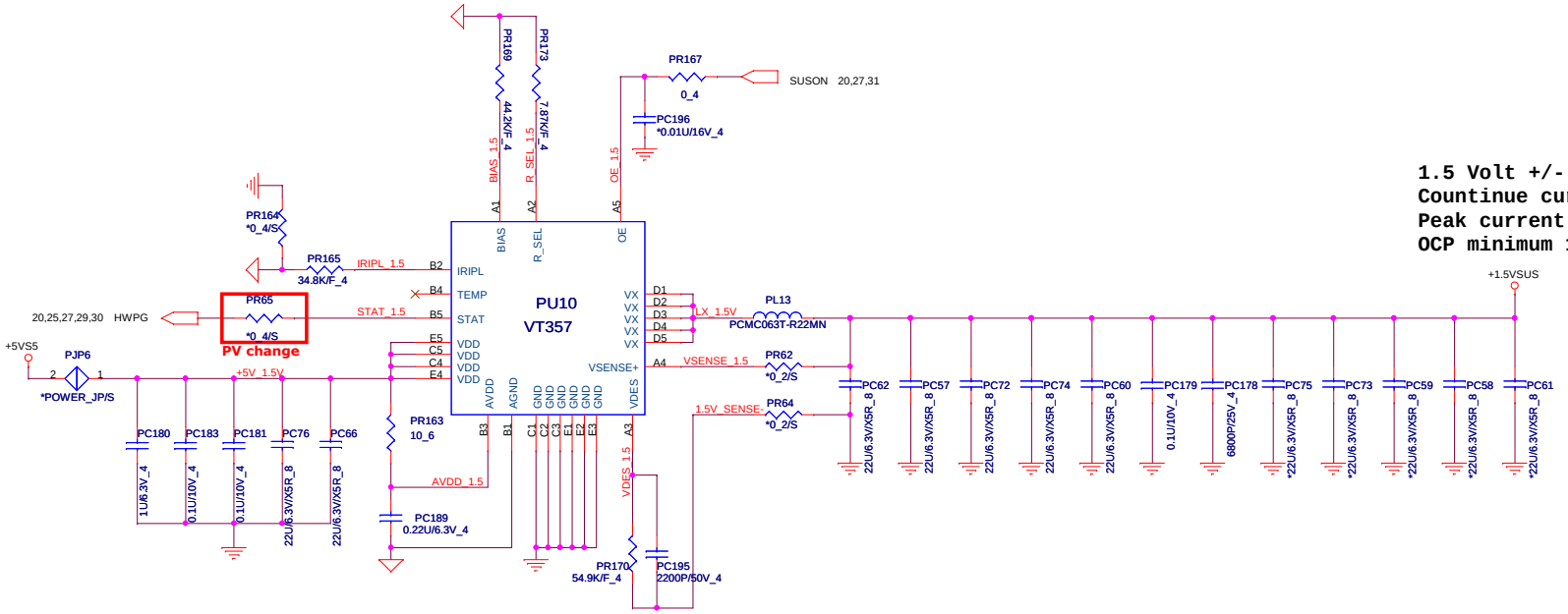

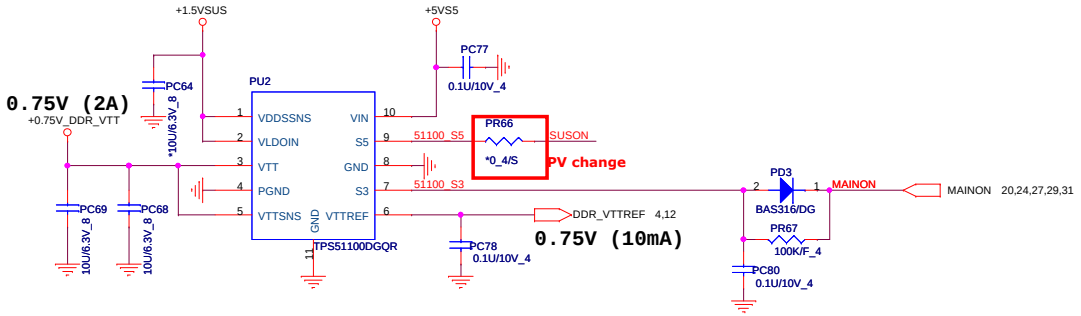

N85	**PROJECT : Stella** Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 (VT358)	Rev: ?
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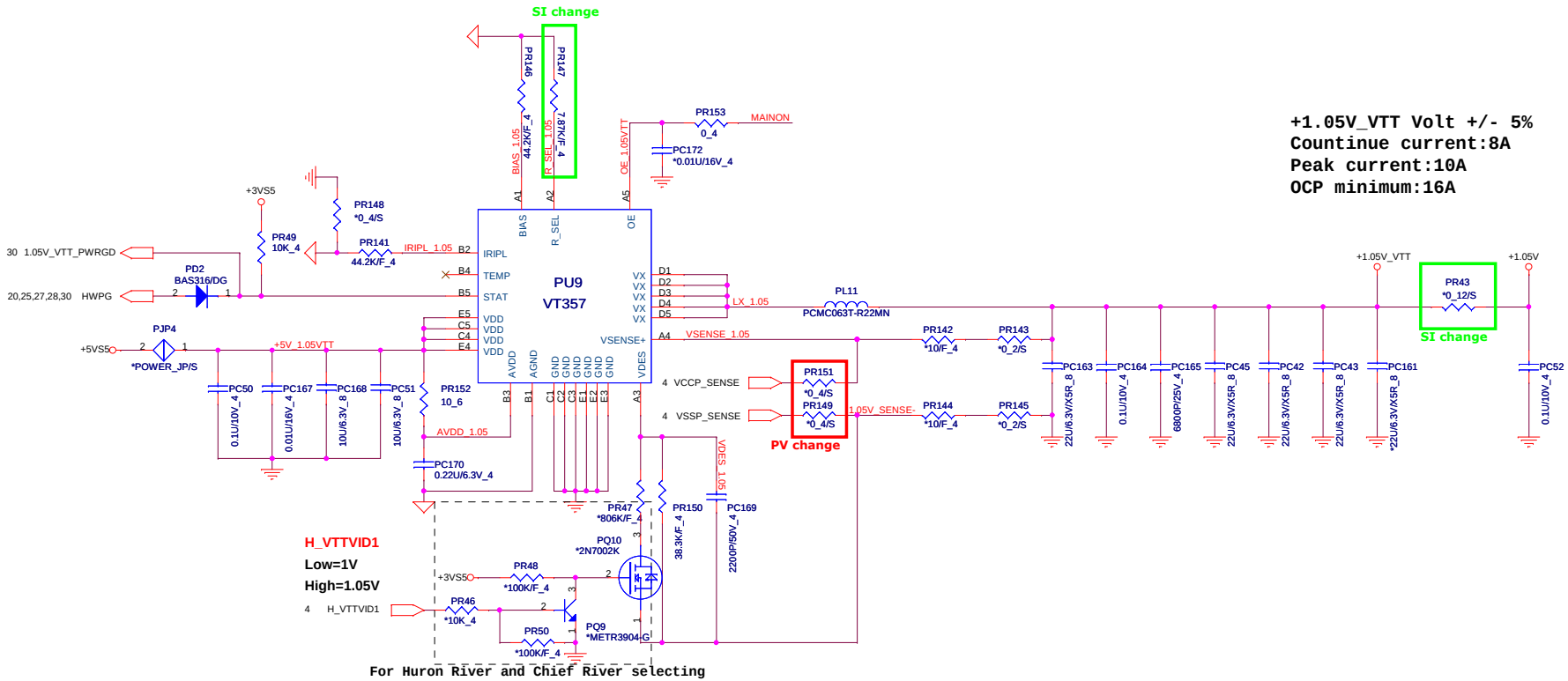
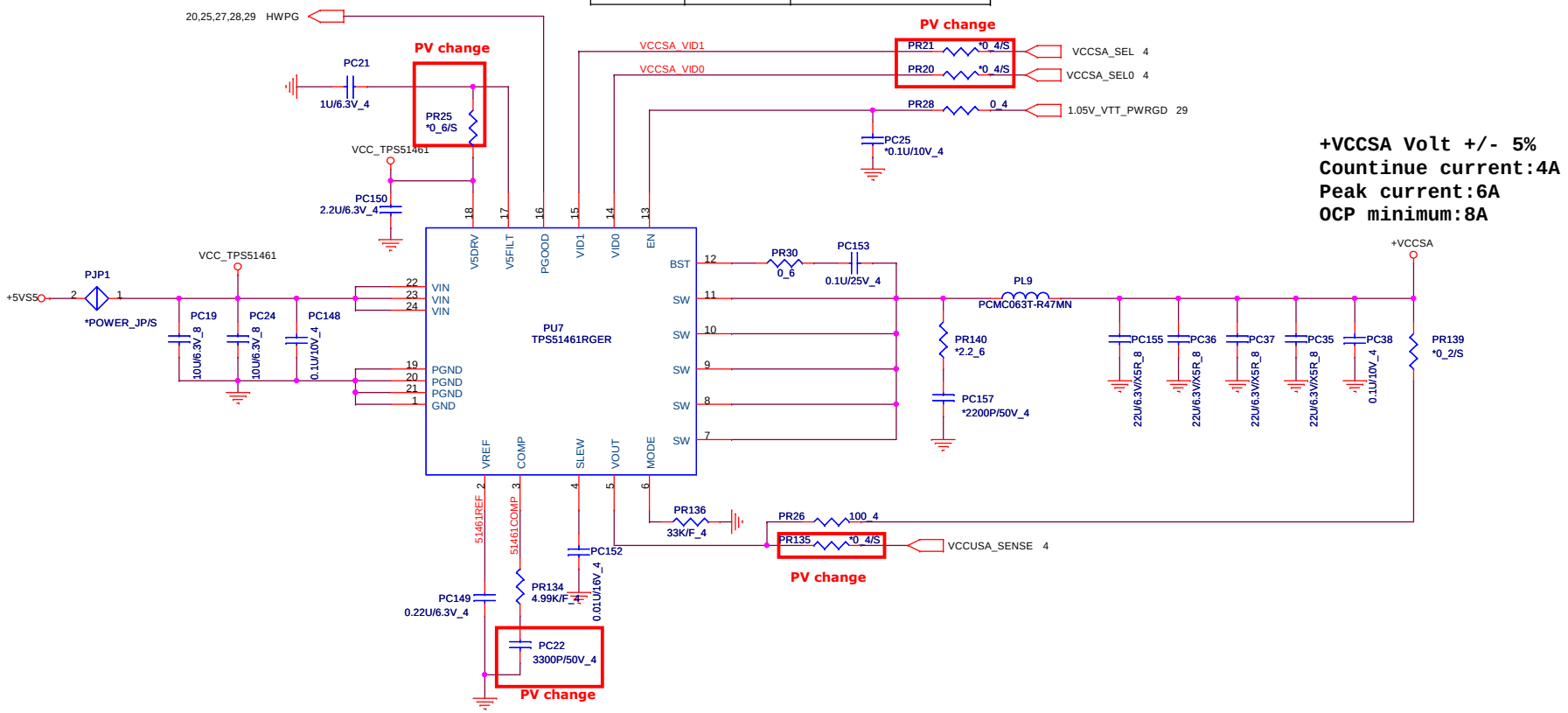


CPU system agent
voltage slew rate of 0.5 -10 mV/µs

H_FC_C22 VID0	VCCSA_SEL VID1	Vout
0	0	0.9V
0	1	0.85V
1	0	0.725V
1	1	0.675V



PROJECT : Stella
Quanta Computer Inc.
V02A/R01A

Size	Document Number	Rev
NB5	VCCSA (ISL95870A)	1A
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