EE 112 2 February 2015

Lab Project 2 Report due 13 February 2015

REDUCTION TECHNIQUES AND MULTILEVEL LOGIC

GENERAL LAB INSTRUCTIONS:

This project requires some preparation out of lab to minimize the time in lab. Please complete the pre-lab assignment to help you prepare for the lab.

You will be required to document your work and answer questions related to this project. I will expect one report from each group of two students. Remember, you are required to work in groups of two. Exceptions are only with permission of the instructor. For the write-up, follow the format for the Lab Report as described in the **" LAB REPORT GUIDELINES_2014 " document (on website). You will be penalized if you do not follow these guidelines.**

Provide data as required, and answer the questions in the Lab Handout. Reports are due at date specified by the instructor.

OBJECTIVE:

One objective of this lab is to continue to learn to use the lab equipment (Scope, DMM, Signal Generator, Power Supplies, and prototyping hardware).

Another objective of this lab is to use the laws of Boolean Algebra to manipulate logic functions and create simplified functions.

A third objective of this lab is to implement a few of these functions, using specific types of gates.

ASSIGNMENT

In each of the following equations, the AND symbol, " • ", is understood to be between the variables or groups of variables separated by parentheses. The prime symbol " ' "is used to indicate the *complement or NOT* of the variable or expression.

1) Use the laws of Boolean Algebra to prove the following:

a) A (A + B) = A

b) (A + B) (A + B') = A

c) (A + B) (A + C') = A + B C'

2) Simplify the following functions:

a) F(A,B,C) = B C' + A' B C + A B C

b) G(A,B,C) = (A + B) (A' + B + C) (A' + B + C')

3) Draw logic diagrams for the following functions using NAND and inverter gates:

a) F(A,B,C) = A B' + A' C + A' B C'

b) G(A,B,C) = (A' + C) (A + B')

4) Draw logic diagrams for the following functions using NOR and inverter gates:

a) F(A,B,C) = (A + C) (A + B')

b) G(A,B,C) = A B' + B C'

5) Design a logic circuit that takes a 3-bit binary input and produces a TRUE (Logic 1) output for a *prime number* input and a FALSE (Logic 0) otherwise. Obtain the truth table and an expression for the function by summing its minterms where the function is equal to 1. Simplify the function and obtain its logic diagram.

PROCEDURE

1) Set up the hardware for a NAND - NAND circuit for the function 3(a) above and check its operation with the truth table you derived for the function.

2) Set up the hardware for a NAND - NAND circuit for the function 3(b) above and check its operation with the truth table you derived for the function.

3) Set up the hardware for a NOR - NOR circuit for the function 4(a) above and check its operation with the truth table you derived for the function.

4) Set up the hardware for a NOR - NOR circuit for the function 4(b) above and check its operation with the truth table you derived for the function.

5) Fabricate the prime number detector circuit described in item 5 in the PROCEDURE SECTION above and verify its operation.

ADDITIONAL QUESTIONS TO BE ANSWERED AS PART OF THIS LAB.

1) Design a 3-input OR gate using only 2-input NAND gates.

2) Design a 3-input AND gate using only two-input NAND gates.

3) Design a circuit for the function F(A,B,C) = (A + B') C + A' B C' using

a) only AND, OR, and NOT gates

b) only NAND and NOT gates

For question 3), assume that both 2 and 3-input gates are available.

4) In error correction, a parity bit is appended to a binary message to make the total number of 1's either odd or even. Design an even parity generator for a 3-bit message using XOR gates only. First draw the truth table for the parity function, and then obtain an expression for it by summing its minterms. Simplify this function to obtain a logic circuit using XOR gates.