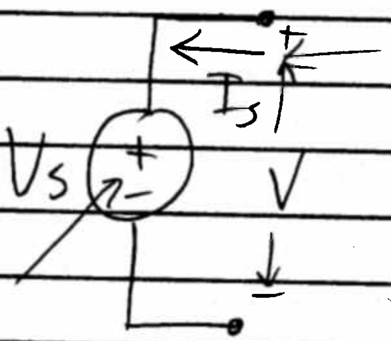
Let's quickly introduce 2 more elements, then we can get on to Circuit Constraints:

Ideal Sources:

Provide either a voltage or a current no matter what, ~~ea~~ can be constant (DC), sinusoidal, or other time-varying forms.

Ideal Voltage Source:

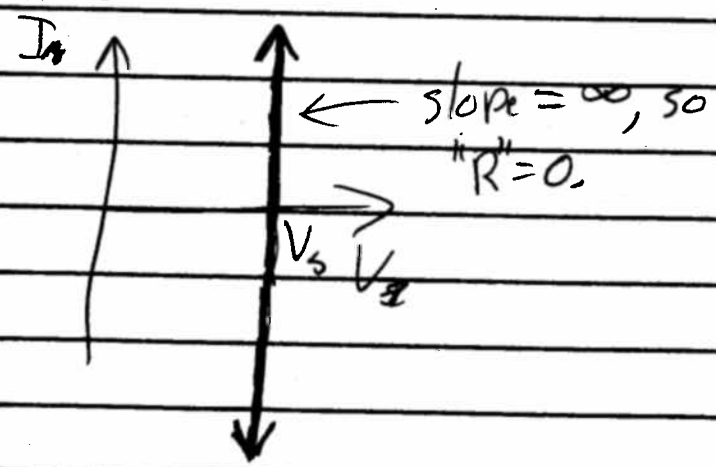


passive sign convention

here are the voltage labels +-

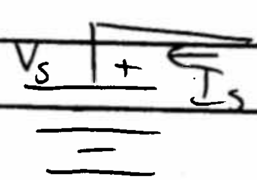
$V = V_s$, I_s = anything the rest of the circuit determines

IV curve:

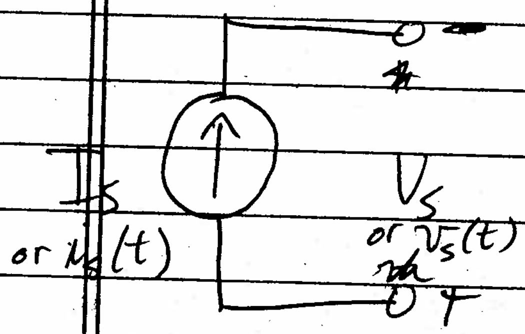


slope = ∞, so "R" = 0.

other symbols:

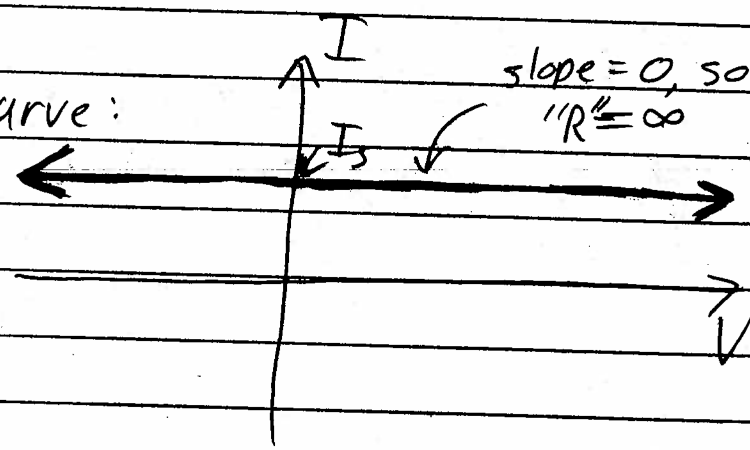


Ideal Current Source:



$I = I_s$, V_s = anything

IV curve:

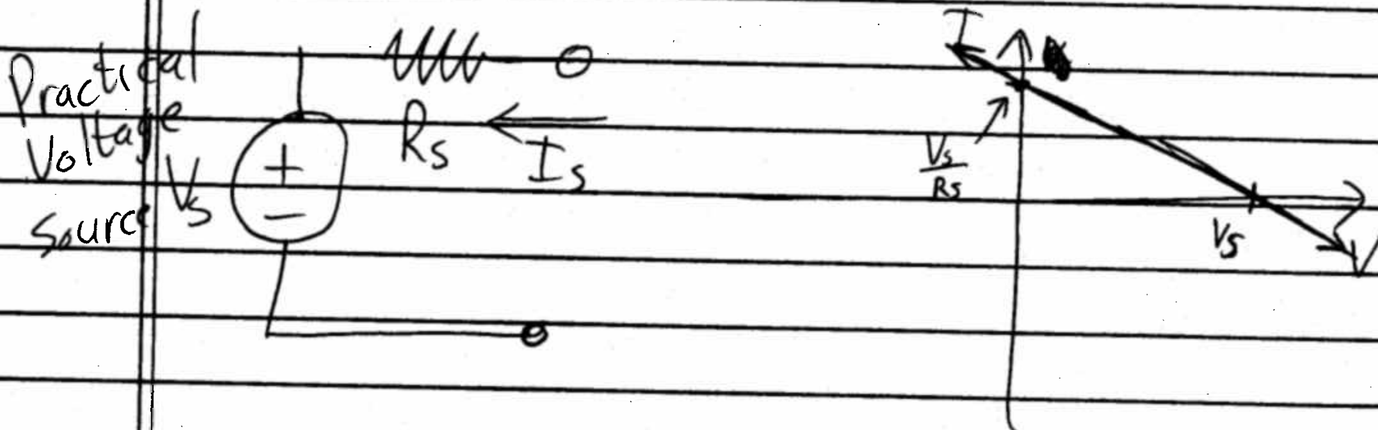


Practical Sources:

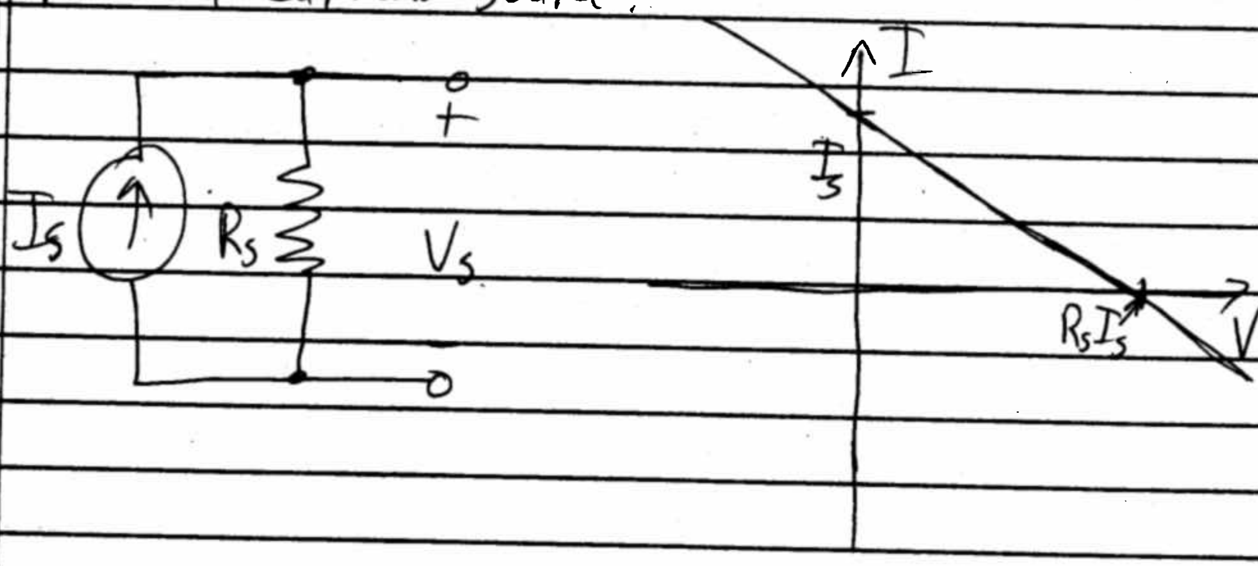
Ideal sources have problems. For example, if you disconnect a Current Source with a switch, it would crank up its voltage, to Mega or even giga Volts if necessary, to make a spark jump between electrodes so that I_s would still flow.

More importantly, they can supply infinite power, and therefore infinite energy, to a ckt.

We avoid those problems by always including a resistor with a source:



Practical Current Source:



Connection Constraints

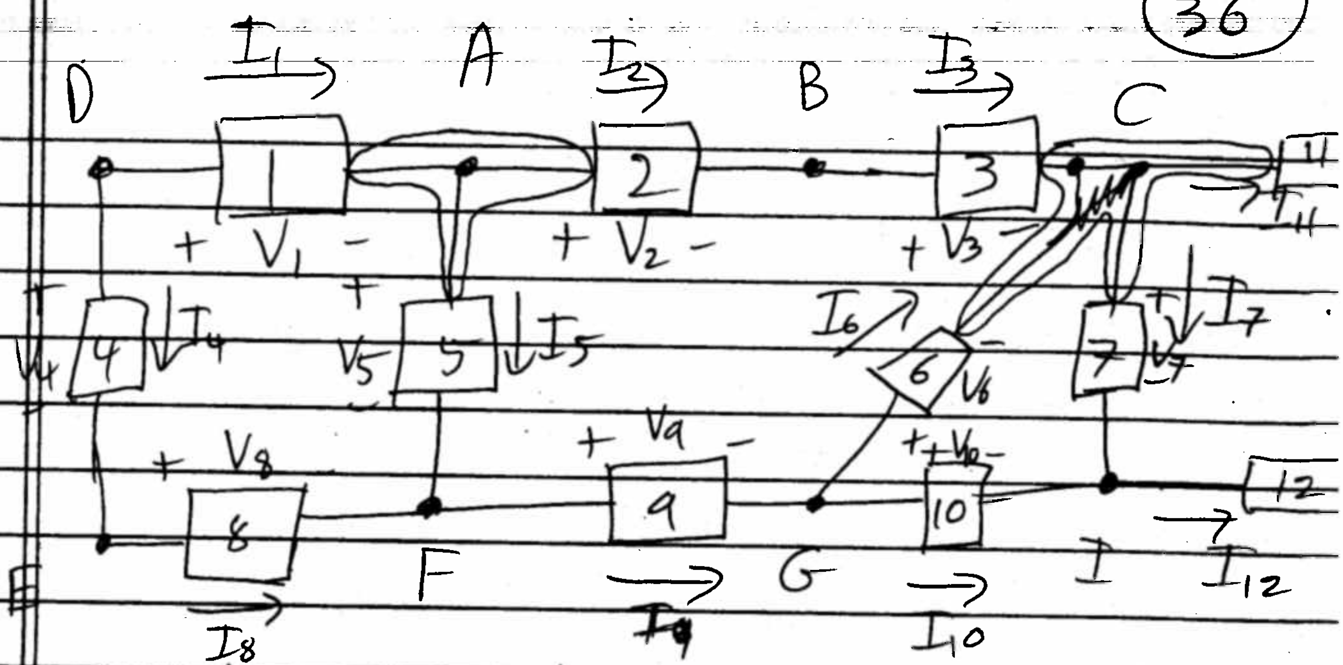
Finally, we know about some devices and we can put them together into useful circuits, or collections of devices. To then figure out what the circuit does we need to know and apply 2 "laws", named for Gustav Kirchhoff: These are essentially based on conservation ideas:

Kirchhoff's Current Law (KCL) says:

"The algebraic sum of currents leaving a node is zero."

First, what is a node?

A node is "all the points on all wires leading up to an element."



Node A includes every point on all 3 wires connected to it, all the way out to elements 1, 2, + 5. (Draw surface)

Now, KCL means "write the sum of all currents that exit through the surface $I_t = 0$"

Node A: $-I_1 + I_2 + I_5 = 0$

Node B: $-I_2 + I_3 = 0$

$\underline{I_3 = I_2}$ (2 + 3 are <u>in series</u>)

Node C: $-I_3 - I_6 + I_7 + I_{11} = 0$
(Draw sfc)

Alternative statements:

Σ currents entering a node $= 0$

Σ currents entering a node $= \Sigma$ current leaving that a node

~~Point: If I can find all currents, then I can completely describe the ckt~~

2nd Law: Kirchhoff's Voltage Law (KVL)

"The algebraic sum of voltage drops around a loop is zero."

Define: A loop is a node-to-node path through a circuit that starts and ends on the same node and does not repeat any node.

So, In our circuit:

$D \rightarrow A \rightarrow F \rightarrow E \rightarrow D$ is a loop,

but $D \rightarrow \underbrace{A \rightarrow B \rightarrow C \rightarrow G \rightarrow F \rightarrow A} \rightarrow D$ is not.

Let's write some equations:

(1)

Left Hand Loop: Start at top left + go CW:

$$+V_1 + V_5 - V_8 - V_4 = 0$$

Next loop: Start at A + CW:

$$+V_2 + V_3 - V_6 - V_9 - V_5 = 0$$

Note: If I add these two:

$$\cancel{+V_4 + V_2 + V_3}$$

$$V_1 + V_5 - V_8 - V_4 + V_2 + V_3 - V_6 - V_9 - V_5 = 0 + 0 = 0$$

cancel

$$V_1 + V_2 + V_3 - V_6 - V_9 - V_8 - V_4 = 0$$

This is what I would get going around a larger loop (go through terms)

Note: If I can find all E voltage drops, then I have completely described the ckt.