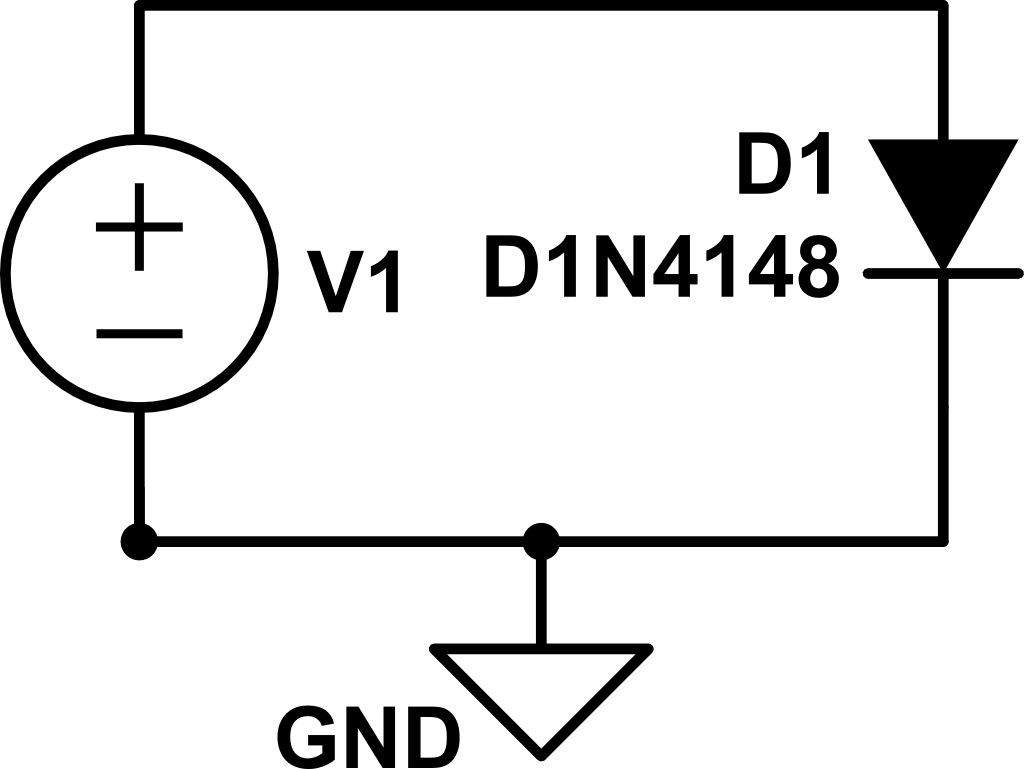
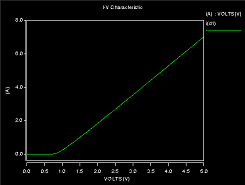
**Schematics**

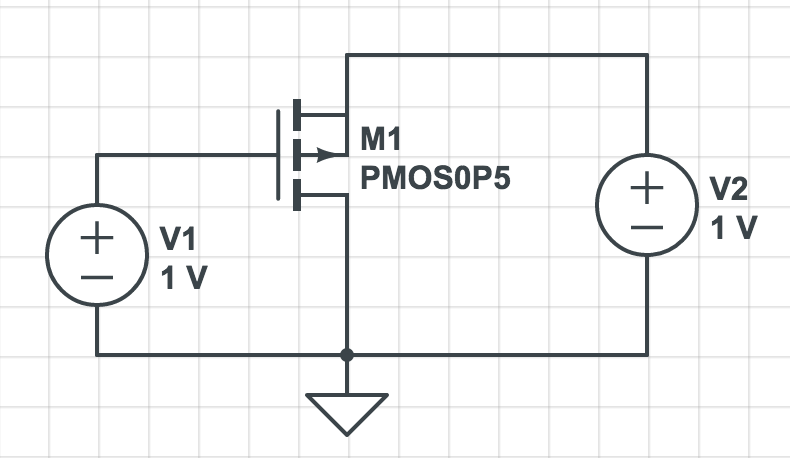
Part 1



This is the basic design for a diode circuit. With this design it is possible to measure the I-V characteristics using a DC sweep, measure the saturation current, and find the small signal diode capacitance. With just a voltage source connected across the terminals, it is simple to evaluate diode properties.

1. Vt = .7V
2. Is = -2.682nA
3. CD = 4.0007pF

I-V Characteristic

Part 2

This is a basic circuit to measure the effects of varying voltage on the gate and the drain on the current through the PMOS transistor.

2) Vgs Vds Id

7 6.2 244.277m

6 5.2 162.195m

5 4.1 98.858m

4 3.2 54.576m

3 2.2 24.479m

2 1.2 7.150m

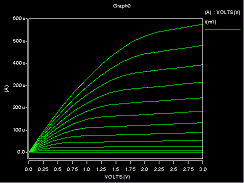
1 .3 .352270u

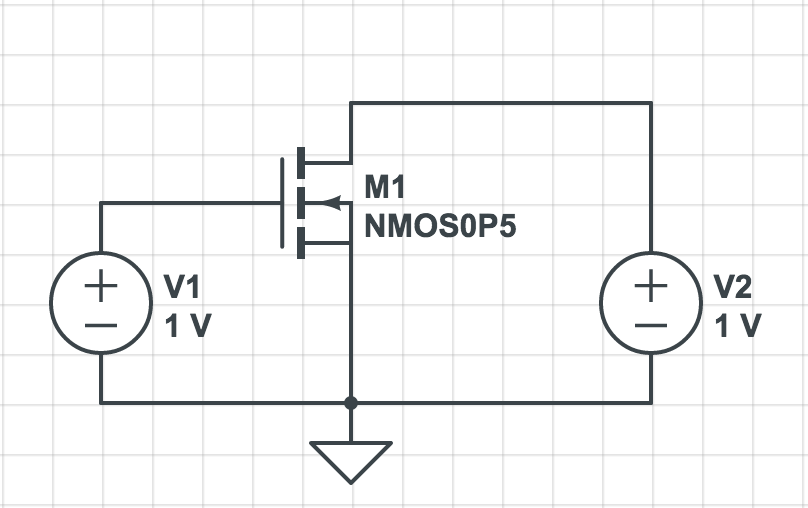
0 - -

3) Vt = .7V

4) ft =2.702Ghz

1. I-V Characteristic



 This is a basic circuit to measure the effects of varying voltage on the gate and the drain on the current through the PMOS transistor.

2) Vgd Vsd Id

7 7.9 -25.678u

6 6.9 -23.687u

5 5.9 -21.697u

4 4.9 -19.706u

3 3.9 -17.716u

2 2.9 -15.726u

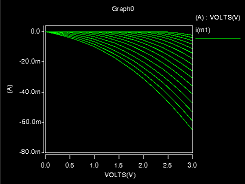
1 1.9 -13.735u

0 .9 -11.744u

3) Vt = .7V

4) ft = 5.344Ghz

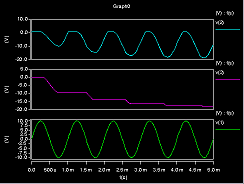
1) I-V Characteristic



Part 3

The circuit used for this section is the one presented in the lab, and is also the voltage doubler exercise from S&S 3.35

Transient behavior of the Voltages V2 and Vout



**Code**

TITLE Lab 1 Part 1

.INC 'sedra\_lib.lib'

$ Define Elements

Vcc 1 GND DC

D1 1 GND D1N4148

$ Control Statements

.OP

.DC Vcc -2 2 .05

$ Output

.OPTION POST

.MEAS DC satCurr Find I(D1) WHEN V(1)=-2V

.PRINT DC I(D1)

.END

TITLE Lab 1 Part 2 Number 1

.INC 'sedra\_lib.lib'

$ Elements

Vds Vd GND DC

Vgs Vg GND DC

M1 Vd Vg GND GND NMOS0P5

+ L=0.6U W=20U AS=20P AD=20P PS=22U PD=22U

$ Control Statements

.OP

.DC Vgs 0 3 0.2 Vds 0 3 1

$ Output Statements

.PRINT DC I(M1)

.END

TITLE Lab 1 Part 2 Number 2

.INC 'sedra\_lib.lib'

$ Elements

Vds Vd GND DC

Vgs Vg GND DC

M1 Vd Vg GND GND NMOS0P5

+ L=0.6U W=20U AS=20P AD=20P PS=22U PD=22U

$ Control Statements

.OP

.DC Vds 0 10 .1 Vgs 0 7 1

$ Output Statements

.PRINT DC I(M1)

.END

TITLE Lab 1 Part 2 Number 3

.INC 'sedra\_lib.lib'

$ Elements

Vds Vd GND DC=5

Vgs Vg GND DC

M1 Vd Vg GND GND NMOS0P5

+ L=0.6U W=20U AS=20P AD=20P PS=22U PD=22U

$ Control Statements

.OP

.DC Vgs 0 1 .01

$ Output Statements

\* .PRINT DC I(M1)

.PLOT DC I(M1)

.END

TITLE Lab 1 Part 2 Number 4

.INC 'sedra\_lib.lib'

$ Elements

Vds Vd GND DC

Vgs Vg GND DC

Rl Vd GND 1K

Cl Vd GND 1U

M1 Vd Vg GND GND NMOS0P5

+ L=0.6U W=20U AS=20P AD=20P PS=22U PD=22U

$ Control Statements

.OP

.DC Vds 0 3 .1 Vgs 1 2 1

$ Output Statements

\* .PRINT DC I(M1)

.PLOT DC I(M1)

.END

TITLE Lab 1 Part 2 Number 5.1

.INC 'sedra\_lib.lib'

$ Elements

Vsd Vs GND DC

Vgd Vg GND DC

M1 GND Vg Vs Vs PMOS0P5

+ L=0.6U W=20U AS=20P AD=20P PS=22U PD=22U

$ Control Statements

.OP

.DC Vgd 0 3 0.2 Vsd 0 3 1

$ Output Statements

.PRINT DC I(M1))

.END

TITLE Lab 1 Part 2 Number 5.2

.INC 'sedra\_lib.lib'

$ Elements

Vsd Vs GND DC

Vgd Vg GND DC

M1 GND Vg Vs Vs PMOS0P5

+ L=0.6U W=20U AS=20P AD=20P PS=22U PD=22U

$ Control Statements

.OP

.DC Vsd 0 3 0.2 Vgd 0 7 1

$ Output Statements

\* .PRINT DC I(M1)

.PLOT DC I(M1)

.END

TITLE Lab 1 Part 2 Number 5.3

.INC 'sedra\_lib.lib'

$ Elements

Vsd Vs GND DC

Vgd Vg GND DC

M1 GND Vg Vs Vs PMOS0P5

+ L=0.6U W=20U AS=20P AD=20P PS=22U PD=22U

$ Control Statements

.OP

.DC Vsd 0 10 0.1 Vgd 0 7 1

$ Output Statements

.PRINT DC I(M1)

\* .PLOT DC I(M1)

.END

TITLE Lab 1 Part 2 Number 5.4

.INC 'sedra\_lib.lib'

$ Elements

Vsd Vs GND DC

Vgd Vg GND DC

Rl Vs GND 1K

Cl Vs GND 1U

M1 GND Vg Vs Vs PMOS0P5

+ L=0.6U W=20U AS=20P AD=20P PS=22U PD=22U

$ Control Statements

.OP

.DC Vsd 0 10 0.1 Vgd 0 7 1

$ Output Statements

.PRINT DC I(M1)

\* .PLOT DC I(M1)

.END

TITLE Lab 1 Part 3

.INC 'sedra\_lib.lib'

$ Element Definitions

Vdd Vin GND AC 10

C1 Vin V2 1U

D1 V2 GND D1N4148

D2 V2 Vout D1N4148

C2 Vout GND 1U

$ Control Statements

.OP

.AC LIN 1 1K 1K

$ Output

.END