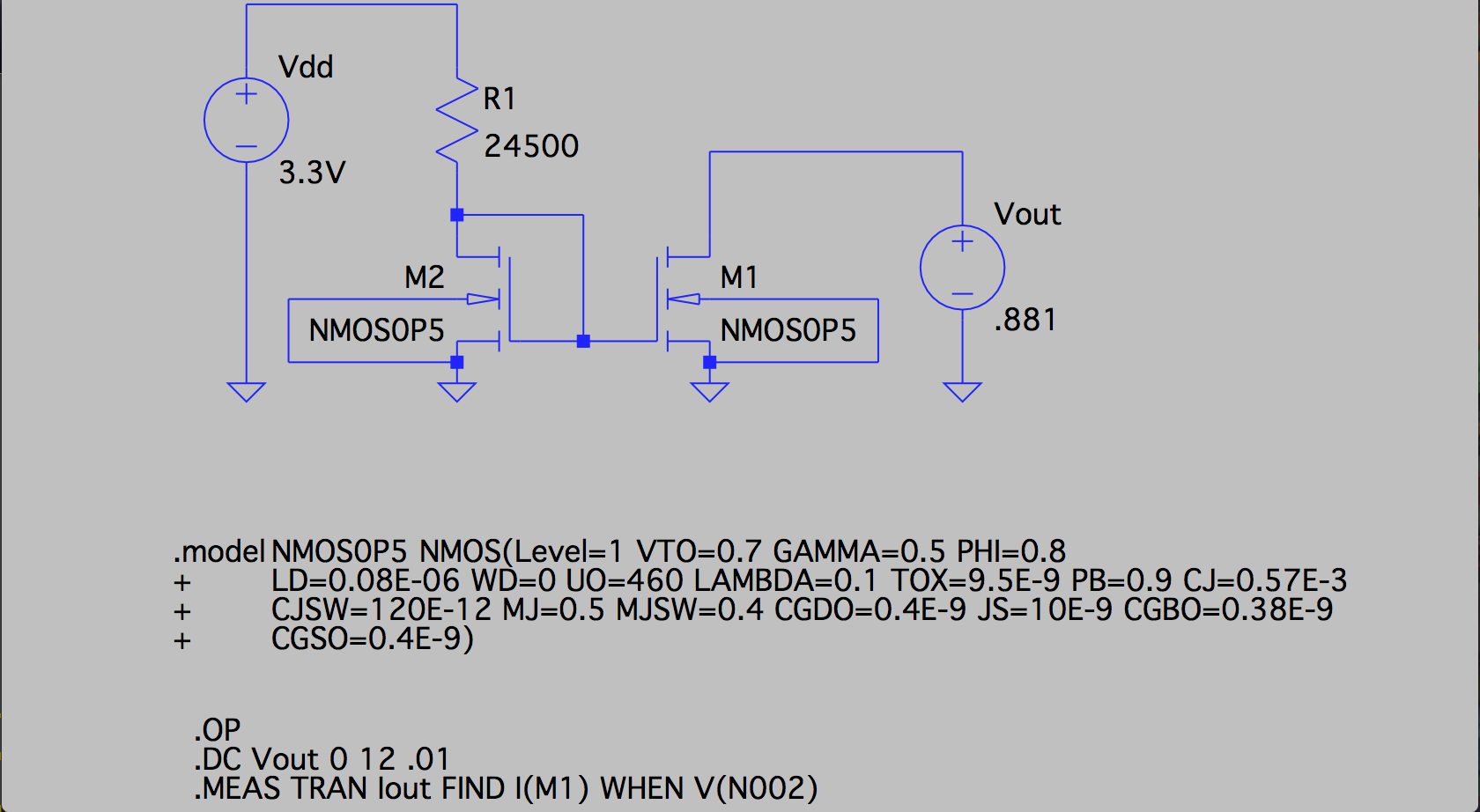
Lab 2

I. Current Mirror

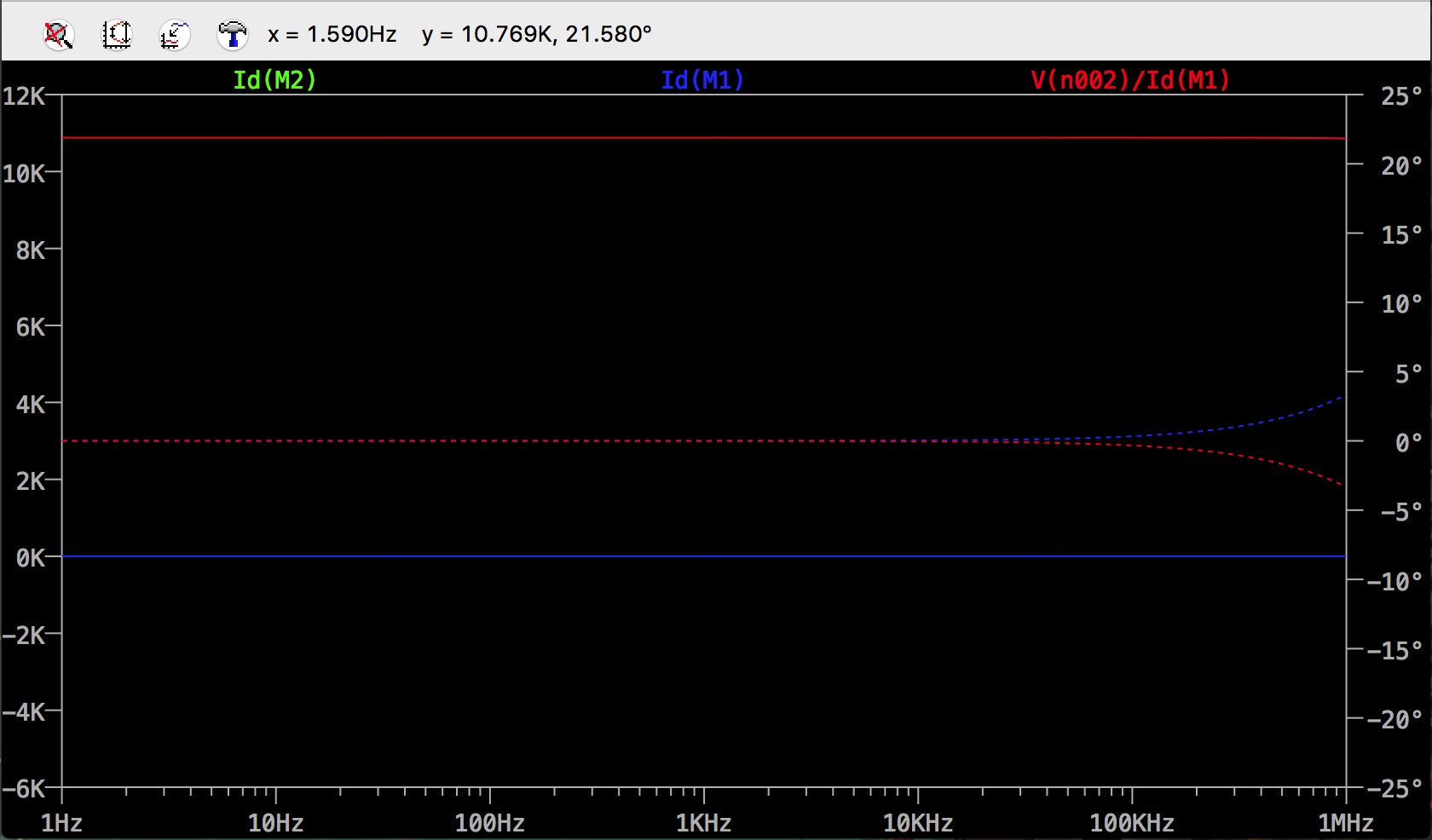


This circuit represents a current mirror. The design is straight forward. The M2 NMOSFET has its body and source connected to ground, its drain connected to its gate. It is also connected in series with a voltage source, representing the power source, and a resistor. This configuration forces the M2 NMOSFET to be in the saturation region. R1 has a value of 24.5KΩ, which makes the current through M2 nearly 100µA. Then, another NMOSFET, M1, has its gate connected M2’s gate, its bod and source connected to ground, and its drain connects to a voltage source representing Vout.

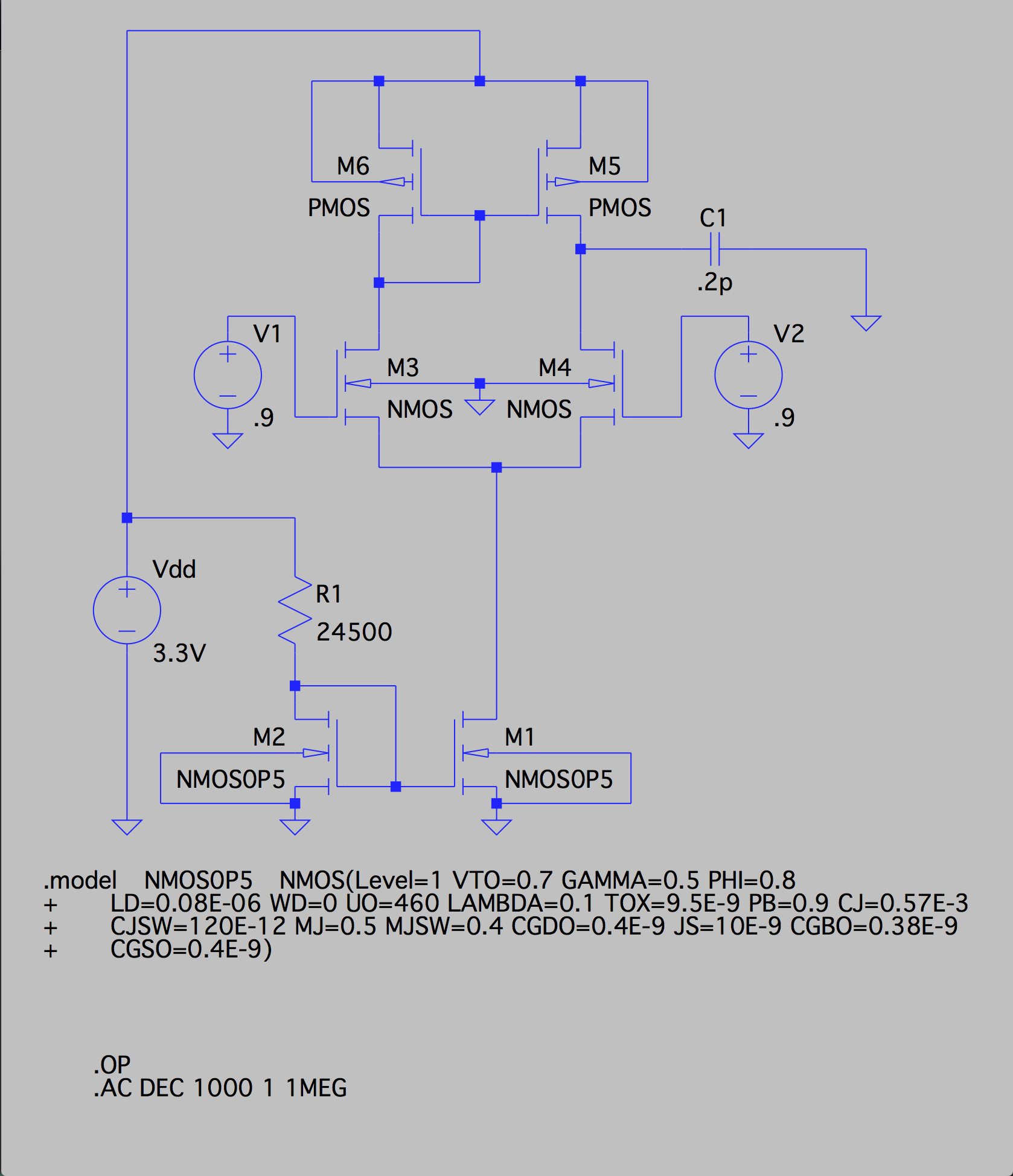
In order to achieve the desired characteristics for Rout and Vout, the width of M1 was set to 200µm, its length to .6µm, and Vout was set equal 881mV (M1 width = 20µm length = .6µm). This made the current through M1 equal 1mA with the desired gain and Rout = 10.652kΩ. Vout was found by sweeping from 0 to 12V and tracking the resulting current. The results are show in the following plot.



The small signal output resistance was found by sweeping a small AC signal on Vout and tracking the resulting ratio between the current and the voltage across M1. The result was a value close to 3kΩ. A plot with the relationships follows.

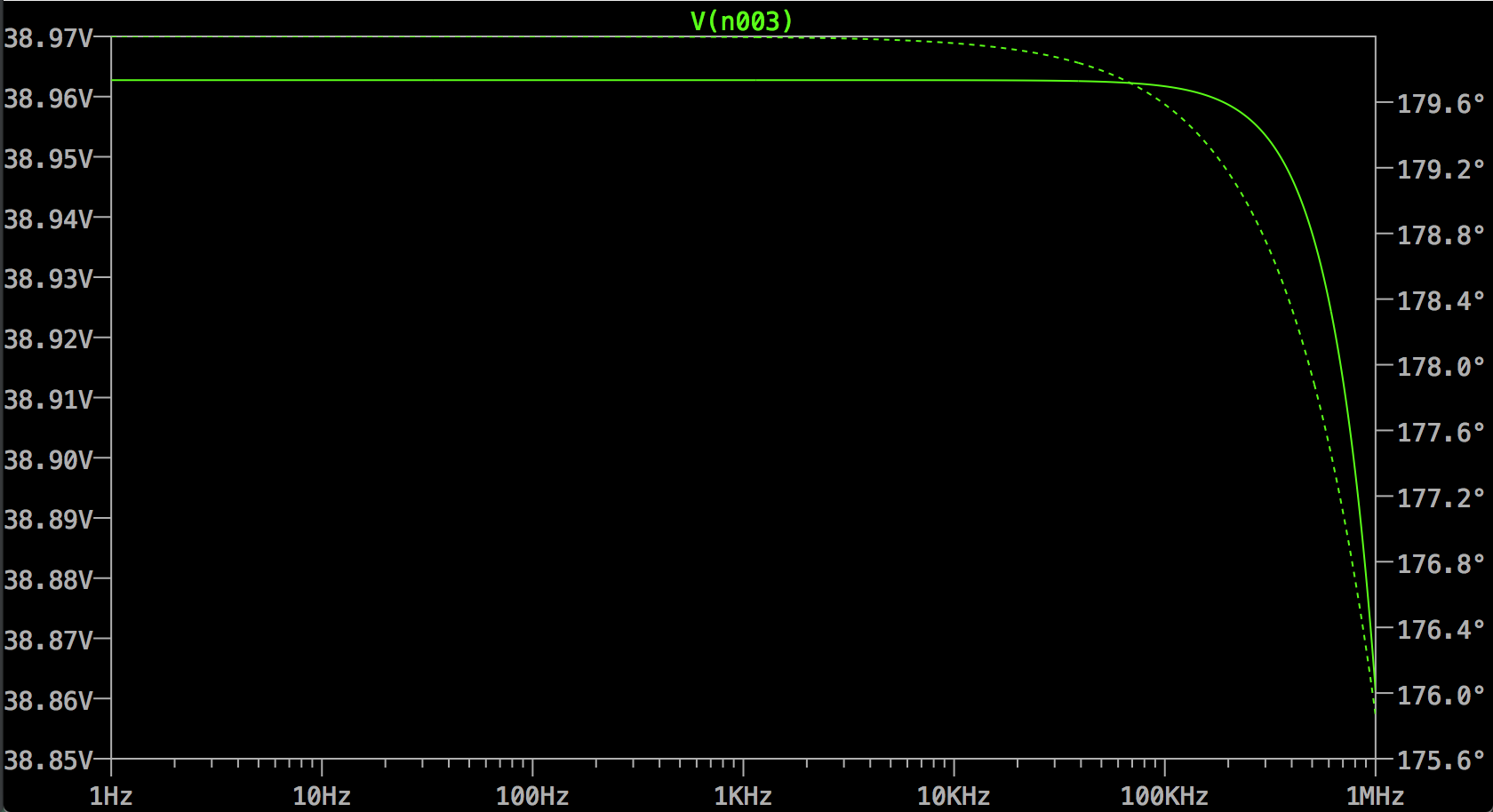


II. Active-Loaded Differential Amplifier



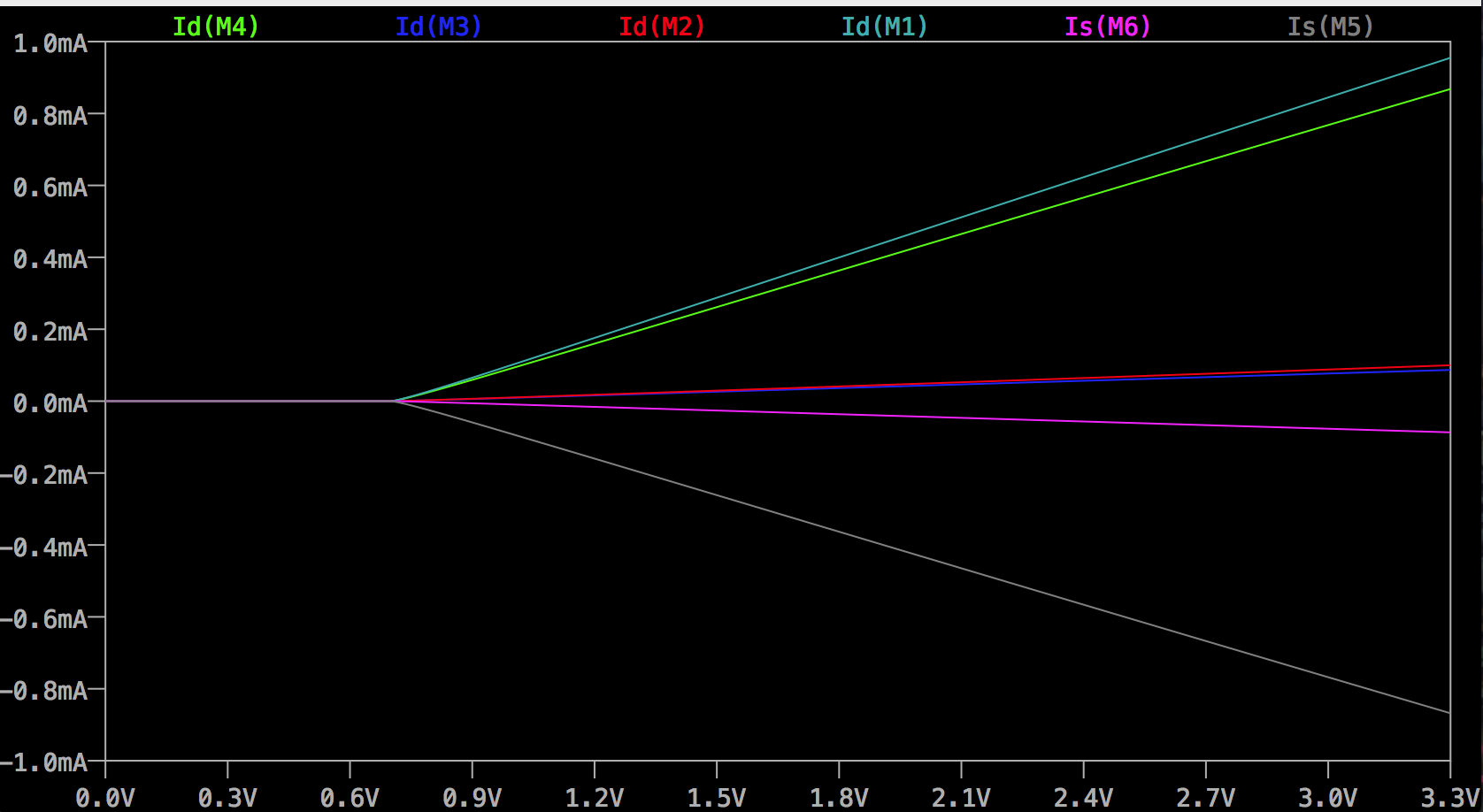
This circuit was also very straight forward and was modeled after the example in the lab. All transistors are connected together as the diagram is. There is a load capacitor that is connects Vout and ground with a value of .2pf. Both VG1 and VG2 are connected to their respective voltage sources. Finally, the current source at the bottom of the figure is replaced by the current mirror designed in part 1 of the lab by connecting the sources of the NMOS transistors in the amplifier to the drain of M1. The sources of the PMOSs are connected to Vdd.

The first goal of this design is to create a gain larger than 10 between the two inputs. This was achieved by many guess-and-checks when adjusting the different transistor parameters. Finally, a satisfactory set of values was found, where M1, M4, and M5 each have a width of 200µm and a length of .6µm. Also, the dc bias voltage on the gates was set to .9V. The gate voltage was chosen by first tuning the bias to 1V, then bringing it down little by little once the transistor parameters were set. The gain was measured by sweeping a small AC signal on VG2 of .2V and finding the ratio between the input and output amplitude. The following plot demonstrates this.



The final gain in the applicable bandwidth is nearly 200.

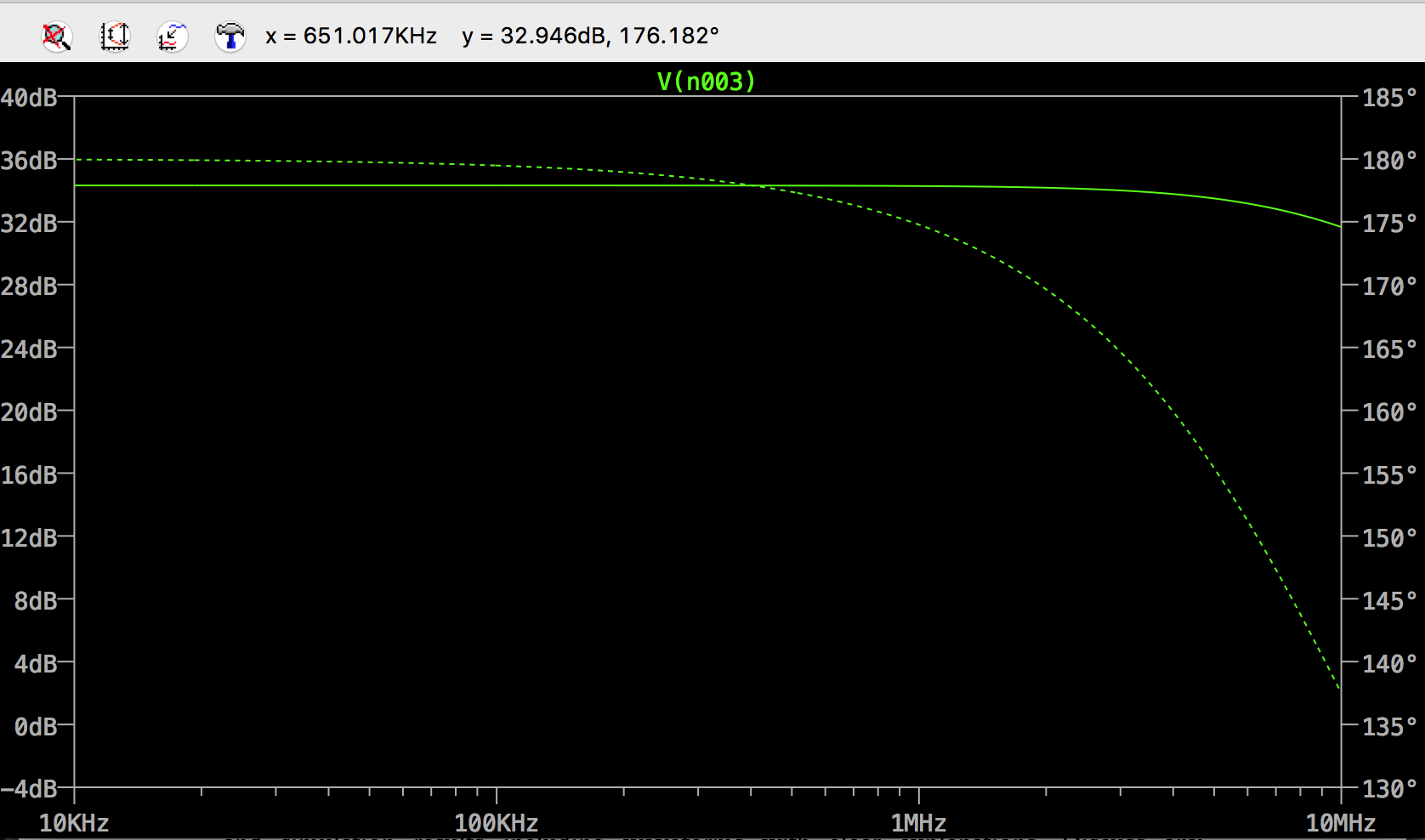
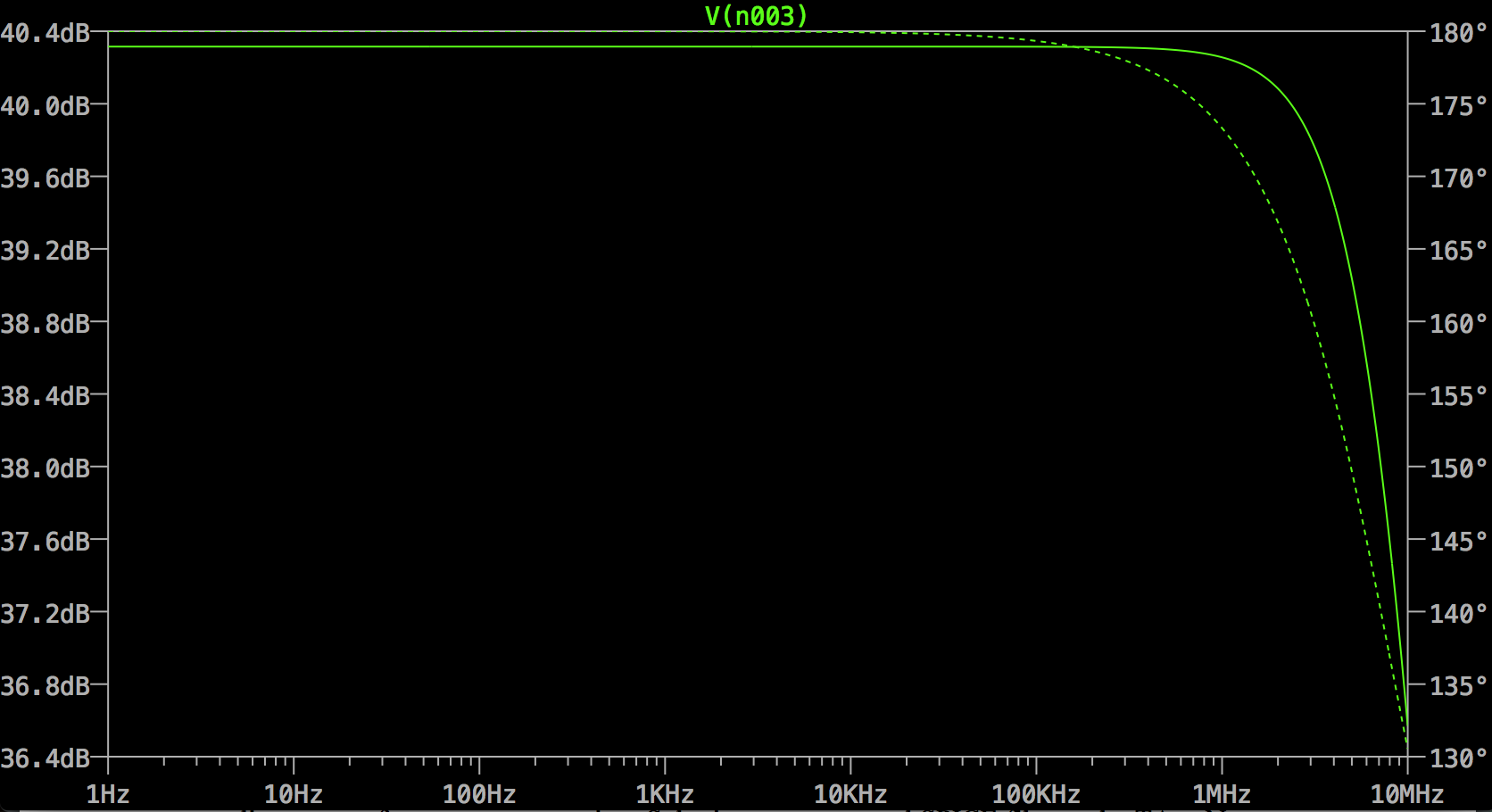
Luckily, the values set amongst the many parameters forced the transistors into the pinch off region. This was found by DC sweeping Vdd and looking at the current characteristics of each transistor. A plot with the characteristics follows.

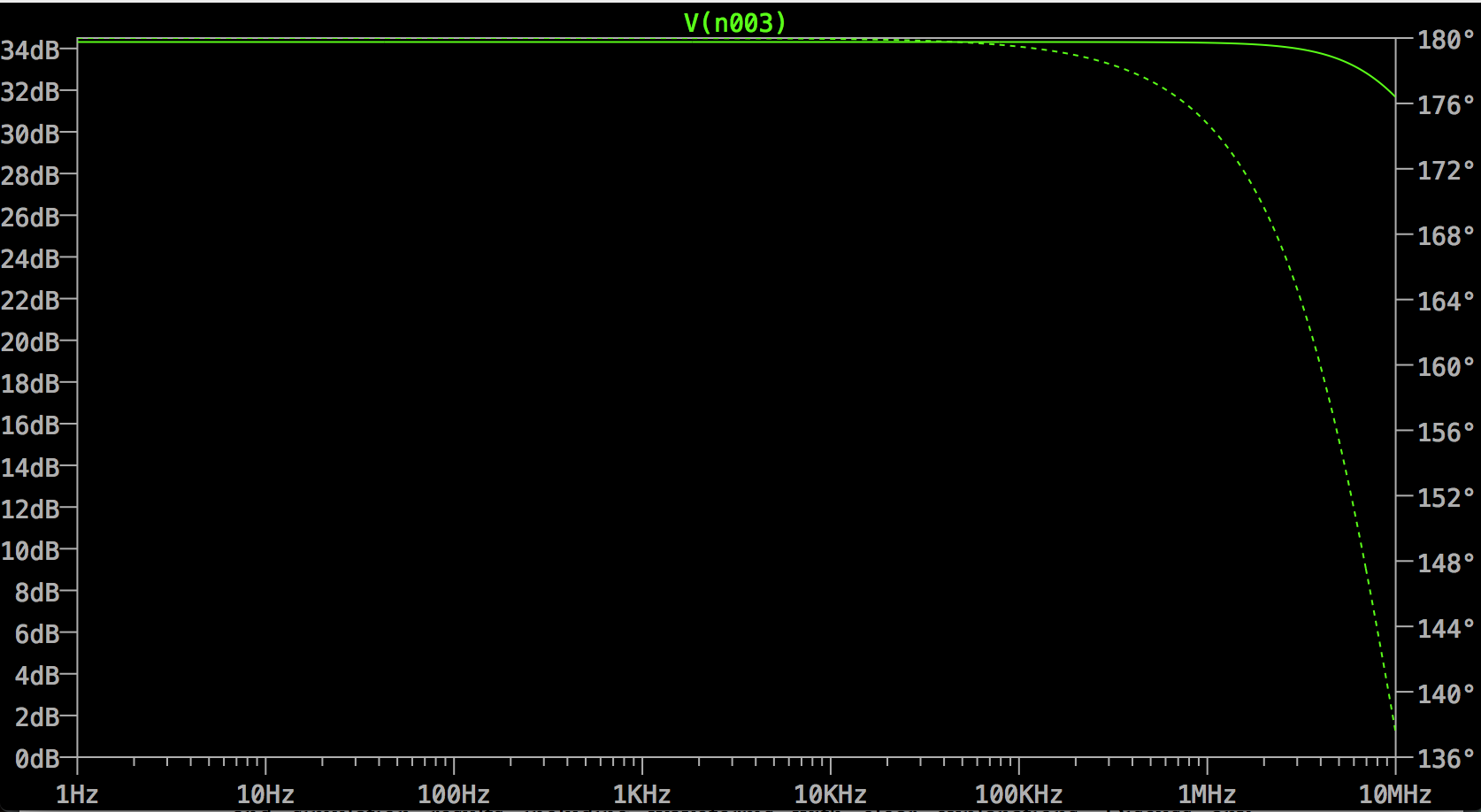


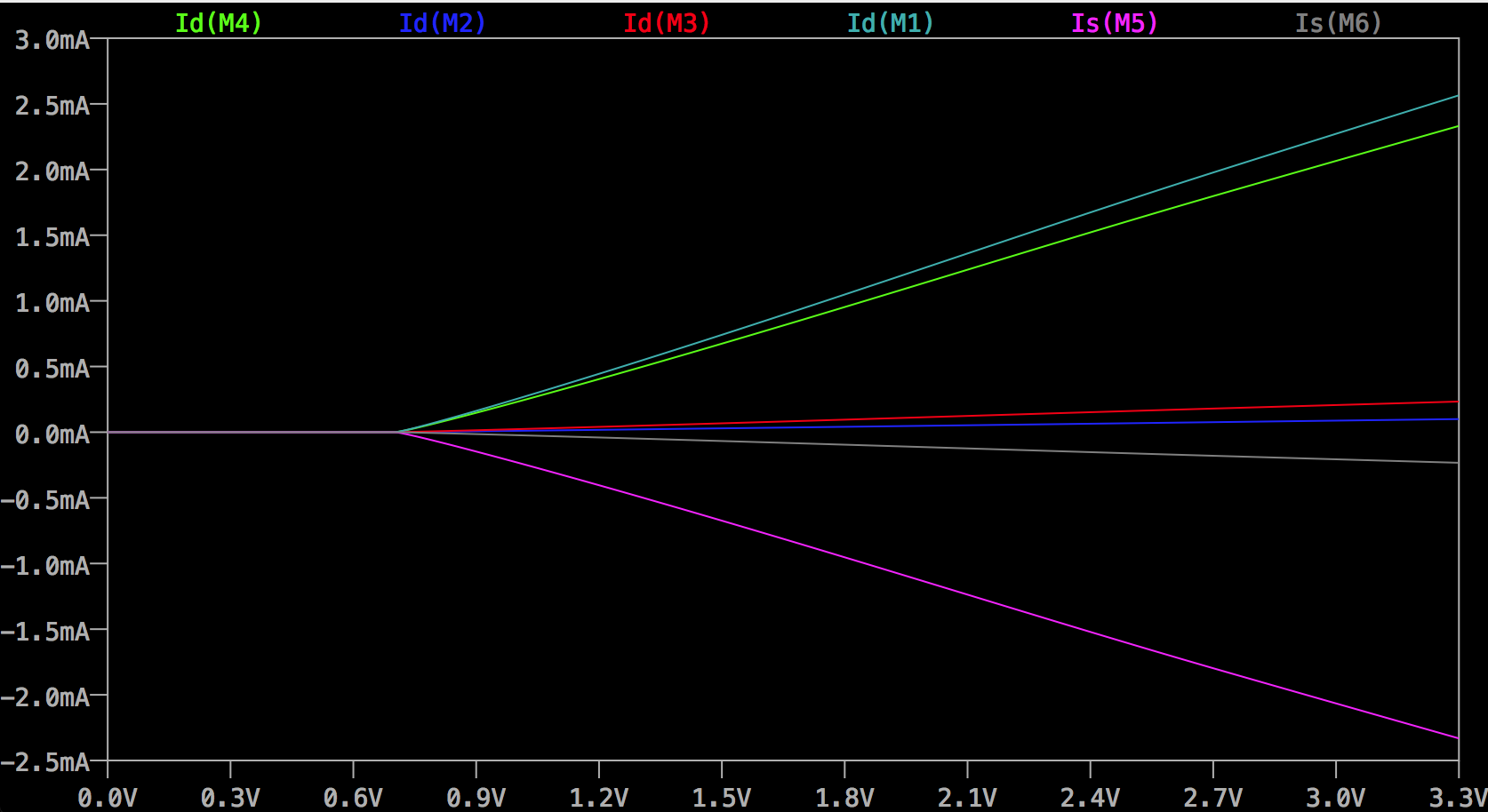
NOTICE: The source current of the PMOS transistors. They are negative.

*f*H was then found by AC sweeping the small AC signal in VG2­ and looking for when the 3dB drop occurs. It was found that the cut-off occurs at about 651kHz. Then, the width of M1 was adjusted to 500 µm, increasing the cut-off frequency from 651kHz to 6.51MHz, a whole magnitude difference. The gain is clearly still in specification and the bias still holds the transistors in the pinch-off region, found with the same methods from earlier. All relevant plots are available below.

AC Sweep



Change of M1 width.

Pinch-off check

It has been found that the relationship between Am and the bandwidth is inversely proportional. When trying to find the greatest bandwidth and Am­ together. It was consistently a trade off.