

Rishabh Ravi

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🌐 <https://borlaugg.github.io/>

🏛 Indian Institute of Technology Bombay

Education

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|-----------|---|-------------|
| 2020 – | 📖 Indian Institute of Technology Bombay, India | 9.09/10 GPA |
| | Dual Degree in Electrical Engineering | |
| 2018 – 20 | 📖 PSBB Learning Leadership Academy | 94.8% |
| | Higher Secondary | |


Internships

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|------|---|----------|
| 2023 | 📖 Modem Firmware Engineer | Qualcomm |
| | <ul style="list-style-type: none">Revived a GPRS-specific modem firmware and virtual platform for real-world applications and created test case scenarios, emulating L1 commands, to assess and validate functionalityTransitioned the firmware operations from 24 to 32 bits, reducing data conversion time to enhance operation speeds by roughly 2%Validated the implementation by maintaining signal-to-noise ratio within defined 21 dB thresholds, affirming the accuracy of decoded data | |
| 2022 | 📖 Parallel Computing & Profiling | Nvidia |
| | <ul style="list-style-type: none">Played a pivotal role in parallelizing ANUGA, an open-source hydrodynamic modeling software, by profiling and running time analysis of the program on Nvidia Nsight SystemsIdentified hot spots of the program that required parallelization to increase performanceMentored a batch of students for two online certification courses on CUDA C and Python | |




Research

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|------|---|------------------------------------|
| 2023 | 📖 A Comprehensive Study on Cache Partitioning | Guide: Prof. Virendra Singh IITB |
| | <ul style="list-style-type: none">Replicated the work on Utility-Based Cache Partitioning for shared LLCs in multi-core systems and analyzed the results on the SPEC 2005 benchmarks on the SNIPER simulatorPerformed a comparative study against static partitioning on the impact on Misses Per Kilo Instructions (MPKI), miss rates, partitioning pattern, and performanceIdentified a 30% performance advantage for UCP compared to static partitioning, with increased gains as improved replacement policies like SRRIP were implemented in the LLC | |
| 2022 | 📖 Cache Security from Side Channel Attacks | Guide: Prof. Virendra Singh IITB |
| | <ul style="list-style-type: none">Studied the vulnerabilities of shared cache and attacks like Flush+Reload, and Prime+ProbeReplicated the work of PASS-P, an adaptation that mitigates such side channel attacksModified PASS-P by introducing DAAIP as the replacement policy and observed a drop in performance, which could be due to PASS-P selectively reallocating clean lines <p>The work report and presentation can be found here and here</p> | |
| 2022 | 📖 Improving Bilateral Filter | Guide: Prof. Satish Mulleti IITB |
| | <ul style="list-style-type: none">Explored the work of Bilateral filters for image denoising and replicated the same on PythonDesigned an alternate penalty function that took pixels in close proximity into considerationLowered the MSE by 41.9% as compared to Bilateral Filtering, obtaining better picture quality <p>The code and report can be found here</p> | |






Research (continued)

- 2022  **Exploring Replacement Policies** *Guide: Prof. Virendra Singh | IITB*
- Studied the cache hierarchy, access patterns, and eviction policies of caches in computers
 - Learned about the various cache optimizations to decrease miss rates, penalties and hit times
 - Explored multiple cache replacement policies that included LRU, and MRU policies to more complex policies such as Re-Reference Interval Prediction (RRIP), Hawkeye, and Mockingjay



Major Projects

- 2022-23  **Processor Design** *Guide: Prof. Virendra Singh | Course Project | IITB*
- Developed a 16-bit RISC multi-staged processor that handled 17 instructions in VHDL
 - Devised a 16-bit pipelined processor, pipelined into six different stages to get a performance close to 1.94 cycle/instruction outpacing the multistage processor by 70%
 - Designed a hazard unit, branch predictor, and forwarding unit to tackle pipelining hazards
 - Designed a 16-bit RISC 2-way fetch superscalar processor handling out-of-order execution
 - Implemented a ROB and a PRF to handle hazards of instruction-level parallelism
- The code for the above was compiled and tested, and can be found [here](#)*
- 2023  **2D Mapping System** *Guide: Prof. Siddhath Talur | Course Project | IITB*
- Designed a four-wheeled robot capable of wirelessly mapping the trajectory traced
 - Utilized an IMU and a Rotary Encoder to track the robot's orientation and speed
 - Transmitted the data wirelessly using a Bluetooth module mounted on a custom PCB
 - Plotted a 3D map of the variation of luminous intensity along the traced trajectory
- Received recognition for outstanding performance and achieving top rankings in a competitive field of projects. This project was ranked among the **top 3** projects out of 60+ projects. The detailed report can be found [here](#).*
- 2020-22  **Matsya, Autonomous Underwater Vehicle (AUV)** *Guide: Prof. Leena Vachhani | IITB*
- AUV-IITB is a team of 40+ students working on the design and development of an AUV*
- Deployed a fully autonomous underwater submarine Matsya, capable of self-navigation and performing multiple tasks as described by the International RoboSub competition
 - Designed space-optimized PCBs on EAGLE with the facility for compact wire routings
 - Facilitated wireless communication using ESP modules following TCP (HTTP) protocol
 - Migrated the logic of the electrical stack to work on STM32G4 from the ATmega328P, enabling higher operation speeds provided by the increased number of I/O ports
 - Implemented 2-D SLAM (Simultaneous Localization and Mapping) in Python and predicted positions using Extended Kalman filter algorithm given inertial and odometric data.


Academic Achievements

- 2021 –  Ranked in the top 3 out of 100+ students in Electrical Engineering (Dual Degree) Department
- 2023  Ranked among the top three projects in the Electrical Design Lab out of 70+ projects.
- 2021  Among the top 30 students to be awarded Change of Branch to Electrical Engineering on excellent academic performance
- 2020  Achieved All India Rank **878** in **JEE Advanced 2020** out of 150,000 candidates.
- 2020  Secured **99.82 percentile** in **JEE Mains 2020** out of 1,100,000 candidates.



Mentorship

- 2023 –  Appointed as a mentor from a pool of 80+ applicants on the basis of ethics, interviews, and extensive peer reviews. Guiding and mentoring six sophomores on a one-to-one basis in their academic and co-curricular pursuits. Working with a team of 35 toward building an effective support system for students in the department
- 2022  Mentored a batch of new recruits to AUV-IITB as the RnD head, and helped in training them. This involved providing resources, solving doubts, and demonstrating the functionality of the AUV.

Teaching

- 2021-2023  Teaching assistant at IIT Bombay for the following courses.
- | Year | Course |
|------|--|
| 2023 | MA 106, Linear Algebra |
| 2023 | MA 111, Integral Calculus |
| 2022 | MA 205, Complex Analysis |
| 2022 | MA 207, Partial Differential Equations |

Technical Skills

- Languages  \LaTeX , C/C++, Python, FORTRAN, VHDL, Assembly, CUDA, MATLAB, GNU Octave, Bash, Heptagon, Perl
- Software  Quartus, Nvidia Nsights, Keil, CubeMX, GNU Radio, NGSPICE, Arduino, EAGLE PCB Design, SNIPER simulator, Fusion 360

Extracurricular

Football

- Participated in and won numerous football tournaments at both school and college levels.
- Represented the college football team at a third-division football league.

National Service Scheme

- Engaged in public speaking and outreach activities focusing on environmental education
- Empowered attendees with the significance of individual actions in preserving resources