Low-Power Retentive True Single-Phase-Clocked Flip-Flop With Redundant-Precharge-Free Operation

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***Abstract*— As basic components, optimizing power consumption of flip-flops (FFs) can significantly reduce the power of digital systems. In this article, an energy-efficient retentive true-single-phase-clocked (TSPC) FF is proposed. With the employment of input-aware precharge scheme, the proposed TSPC FF precharges only when necessary. In addition, floating node analysis and transistor level optimization are employed to further ensure the high energy efficiency of the FF without significantly increasing the area. Postlayout simulations based on SMIC 55-nm CMOS technology show that at a supply voltage of 1.2 V, the power consumption of the proposed FF is 84.37% lower than that of conventional transmission-gate flip-flop (TGFF) at 10% data activity. The reduction rate is increased to 98.53% as the data activity goes down to 0%. When the supply voltage decreases to 0.6 V, the proposed FF consumes only 0.411 fJ/cycle at 10% data activity, which is 84.23% lower than TGFF. Measurement results of ten test chips demonstrate the great energy efficiency of the proposed FF. Furthermore, the CK-to-Q delay of the proposed FF is 26.18% lower than that of TGFF at a supply voltage of 1.2 V.**

***Index Terms*— Flip-flop (FF), low voltage operation, low-power, redundant-precharge-free, true-single-phase-clocked (TSPC).**

I. Introduction

With the development of the process, the performance of digital system is greatly improved, and the power consumption is becoming an important limitation of digital systems. In addition, with the rapid development of the Internet of Things (IoT), IoT devices are deployed on a large scale [1]. In such battery-powered or self-powered devices, low-power design becomes the focus of attention [2]–[5]. As basic components, the power of flip-flops (FFs) accounts for a large part of the power of digital systems [6], [7]. Therefore, reducing the power consumption of FFs can significantly reduce the power consumption of the digital systems.

Voltage-scaling technique has been proved to be an attractive method to decrease the power consumption of digital systems [8]–[12]. In order to obtain the power benefits of voltage-scaling technique, it is necessary to design an FF capable of operating at both superthreshold and near/subthreshold supply voltage.

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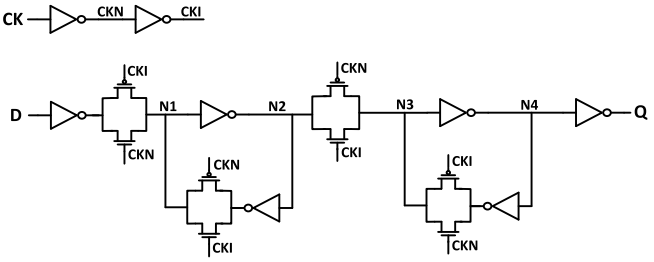

Fig. 1. Schematic of TGFF.

The transmission-gate flip-flop (TGFF) is the most widely used FF in current digital systems. The schematic of TGFF is shown in Fig. 1. The TGFF is a contention-free FF which is suitable for near-threshold operation. The main drawback of TGFF is the large clock network. The internal nodes CKN and CKI toggle no matter what the input data is, and the nodes CKN and CKI drive a larger number of transistors. Thus, the power consumption of TGFF is still large even if the data activity remains low. To reduce the power consumption of FF, the use of complementary clock signals should be optimized.

Many low-power single-phase-clocked FFs have been proposed in previous works [13]–[18]. But there are still some problems that affect the power consumption of these FFs. For example, some of the FFs fail at low supply voltage [13]–[16], [18], and some suffer from large precharge power [13], [16]–[18]. In order to solve these problems, a low-power true-single-phase-clocked (TSPC) FF is proposed in this article. The proposed FF is contention-free and suitable for wide supply voltage operation. Furthermore, redundant precharge operation is totally removed in the proposed FF and the power consumption is further optimized compared with previous low-power FFs.

The rest of this article is organized as follows. Section II reviews several popular low-power FFs. The proposed FF is described in detail in Section III. Simulation results are displayed in Section IV. Section V shows the experimental results. Finally, Section VI draws a conclusion.

II. Previous Low-Power Single-Phase-Clocked FFs

In this section, several state-of-the-art low-power FFs are reviewed and the limitations are analyzed. All the listed FFs

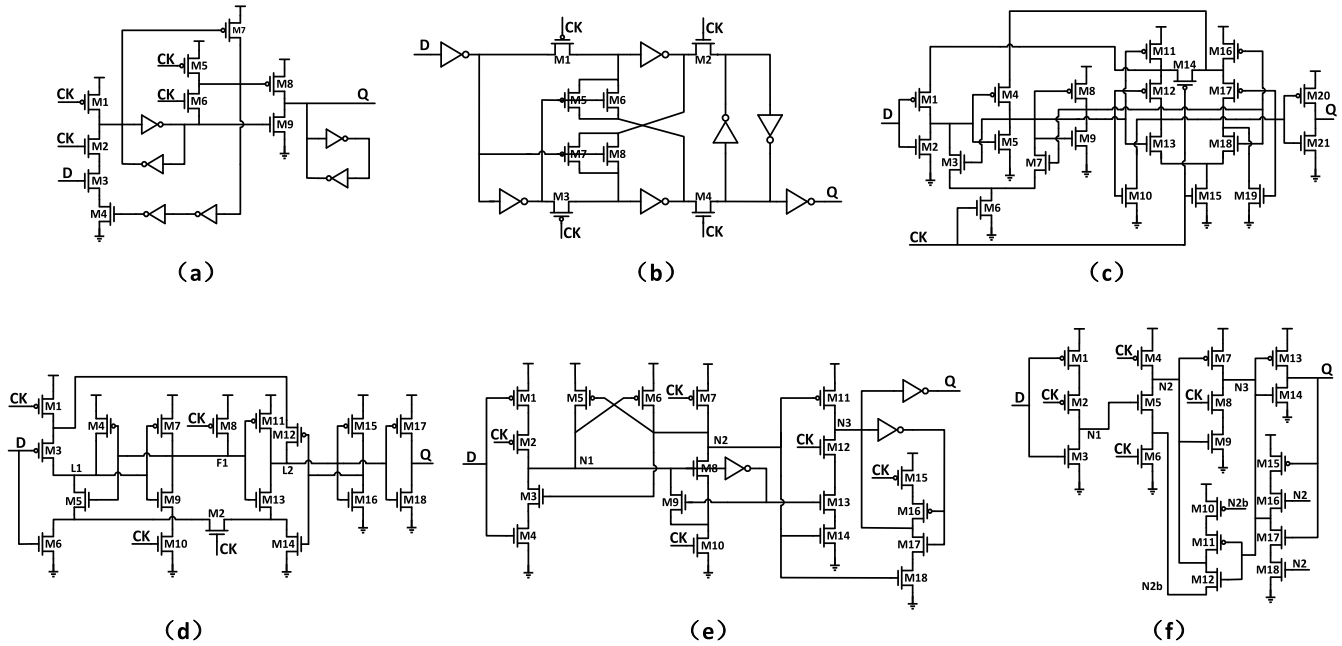

Fig. 2. Schematic of various FFs. (a) XCFF [13]. (b) ACFF [14]. (c) TCFF [15]. (d) SPC-18T FF [16]. (e) S^{2}CFF [17]. (f) RTFF [18].

are single-phase-clocked FFs, which optimize the number of transistors related to the clock signal compared to TGFF.

In [13], a cross-charge control FF (XCFF) is proposed to reduce charged gate capacitance so as to reduce power consumption. As shown in Fig. 2(a), there is strong current contention at the output node of XCFF, so XCFF is not suitable for low voltage operation. Furthermore, XCFF needs to precharge some internal nodes no matter what the input data is, and extra power is wasted during the precharge and discharge operation.

The adaptive-coupling FF (ACFF) [14] employs several single-channel transmission-gates and dynamic circuit to replace conventional double-channel transmission-gate, and the number of transistors related to the clock signal is greatly reduced. But the single-channel transmission-gates and dynamic circuit are easily affected by process variation. In addition, strong current contention is also existed in ACFF. As a result, ACFF cannot operate correctly at low supply voltage.

The topologically compressed FF (TCFF) proposed in [15] is shown in Fig. 2(c). TCFF is a kind of combinational-type FF with topologically compressed scheme to decrease the load of the clock signal as well as the area. But the large number of shared transistors leads to the significant voltage drop of internal nodes and decreases the robustness under low supply voltage. Thus, TCFF is also not a good choice for low voltage operation.

Another low-power single-phase-clocked combinational-type FF named 18T single-phase-clocked FF (SPC-18T FF) is proposed in [16]. Similar to that of TCFF, SPC-18T FF is obtained by simplifying combinational logic. As shown in Fig. 2(d), there are redundant precharge and discharge operations of internal node F1 which waste significant power consumption. Even though the number of shared transistors is reduced compared with TCFF, there is still a temporary short-circuit path which would influence the robustness of SPC-18T FF. When the input data D changes from 1 to 0, L1 and F1 are charged to VDD at the negative half cycle of CK. At the rising edge of CK, the voltage of L1 may be dropped through the path M5 $\rightarrow$ M2 $\rightarrow$ M14 (previous $Q = 1$, so M14 is on at the rising edge of CK) and the captured data is incorrect. The influence is not obvious at superthreshold supply voltage, but the robustness of the FF will be significantly affected at low supply voltage. Furthermore, the hold time of SPC-18T FF is increased as described in [16], which means more buffers are needed to fix the hold time violation.

A static single-phase-clocked contention-free FF (S^{2}CFF) is proposed in [17]. Since conventional TSPC FF is based on dynamic logic and the voltage of internal nodes is not retentive, it is not suitable for low voltage operation. In S^{2}CFF, the retentive problem of internal nodes is solved so that the FF can work correctly at low supply voltage. The main drawback of S^{2}CFF is the waste of power consumption in redundant precharge and discharge operations. When the input data D remains 0, the node N2 precharges to VDD through M7 during the negative half cycle of CK and discharges to GND through M8 and M10 at the rising edge of CK as shown in Fig. 3. The precharge and discharge operation does not change the state of the circuit, and the capacitance of the node N2 is quite large, so the operation is redundant and wastes much energy.

Another retentive true-single-phase-clocked FF (RTFF) is proposed in [18]. As shown in Fig. 2(f), there is a temporary short-circuit path in RTFF. When the input data changes from 0 to 1, N2 is precharged to VDD at CK $= 0$. At the rising edge of CK, M8 and M9 start to pull down the node N3, but

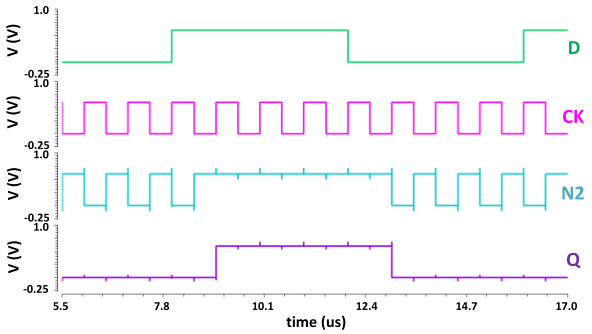

Fig. 3. Transient waveform of S^{2}CFF.

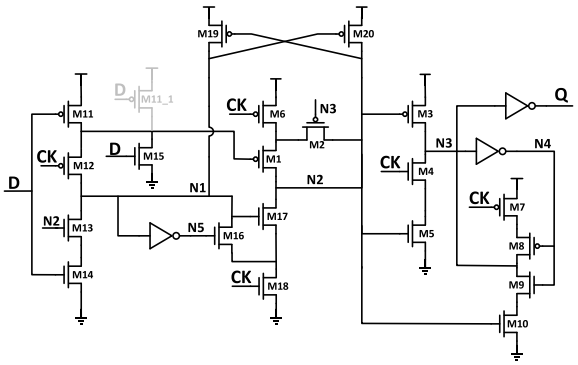

Fig. 4. Schematic of the proposed FF.

M15 and M16 still pull up N3 since the previous Q is 0. The temporary short-circuit path would influence the robustness especially at low supply voltage. An NMOS is used for pull-up operation in RTFF which would lead to a voltage drop of internal node and decrease the robustness. Furthermore, RTFF also suffers from redundant precharge and discharge operation which would waste much power consumption.

III. Structure of the Proposed FF

In this section, the structure of the proposed FF is described in detail. In order to minimize the power consumption of FF, any unnecessary transitions of internal nodes should be removed. We start with S^{2}CFF which is retentive TSPC and suitable for low voltage operations. To eliminate the redundant precharge and discharge operations, the FF is optimized by following steps. Firstly, unnecessary precharge operation of the internal node N2 is totally removed by the input-aware precharge scheme. Secondly, the floating node is under consideration to avoid short current which would greatly increase power consumption. Finally, unnecessary transistors are merged or removed to decrease the area.

A. Input-Aware Precharge Scheme

As shown in Fig. 3, the precharge operation of the node N2 in S^{2}CFF when the input data remains 0 is unnecessary. To eliminate the energy-wasted operation, the precharge path should be cutoff when $D = 0$. A PMOS M1 controlled by the inversion of the input data is inserted into the precharge path of the FF as shown in Fig. 4. When the input data is 1, the PMOS M1 is ON and the necessary precharge operation works as usual. When the input data remains 0, the PMOS M1 is OFF and the precharge path is cutoff by the inserted transistor. As a result, the redundant precharge operation is totally removed.

B. Floating Node Analysis

Since the voltage of floating nodes may change after transition due to the leakage current, it is necessary to carefully analyze floating nodes to avoid the generation of short-circuit paths. With the insertion of the input-aware transistor, the voltage of the node N2 is no longer precharged to VDD at the negative half cycle of CK when the input is 0. So the status of the node N2 needs to be analyzed carefully.

As shown in Fig. 4, when the output $Q = 1$, which means N3 $= 0$, the state of N3 is maintained by M9 and M10. To keep the transistor M3 OFF and the transistor M10 ON at that time, the voltage of N2 needs to keep high. In order to avoid N2 becoming floating while the next input data is 0, a transistor M2 is inserted to keep the voltage of N2. M2 is controlled by N3 and provides a precharge path for N2 when $Q = 1$.

When the output $Q = 0$, N3 $= 1$, the state of N3 is maintained by M7 and M8. If the precharge path of N2 is cutoff at that time, which means the input data is 0 and the voltage of N2 does not charge to high when CK is low, the only effect is that M3 is ON, which will not lead to a short circuit path. When N3 $= 1$, CK $= 0$, and $D = 0$, the node N3 is isolated from its pull-down path (M4 and M5) through M4 (CK $= 0$), so the voltage of N2 has no effect on the node N3. Similarly, N1 is isolated from its pull-down path (M13 and M14) through M14 ($D = 0$), and the voltage of N2 has no effect on the node N1. Therefore, the floating of the node N2 is negligible in this case.

C. Transistor Level Optimization

The function of the FF is correct and the redundant precharge operation is removed after adopting the input-aware precharge scheme and floating node analysis, but the FF can be further improved. The PMOS M11_1 which is used to generate the inversion of the input data can be merged into M11. But the NMOS M15 cannot be merged into M14 at the same time. Once both PMOS and NMOS are merged, which means the drain of M11 and M14 is directly connected, which can lead to functional failures of the FF. Thus, the NMOS M15 is reserved as shown in Fig. 4. The transistor M13 in S^{2}CFF [shown in Fig. 2(e)] is removed because it no longer plays a significant role in the proposed structure. In S^{2}CFF, M13 is used to prevent glitches when the input data stays 0. But in the proposed design, the node N2 does not need to precharge once the input data stays 0, and the voltage of N2 is relatively low. Thus, the output will not have obvious glitches even if the transistor is removed.

D. Operation of the Proposed FF

The detailed operation of the proposed FF at different D and CK is shown in Fig. 5. As shown in Fig. 5, the proposed FF works as follows.

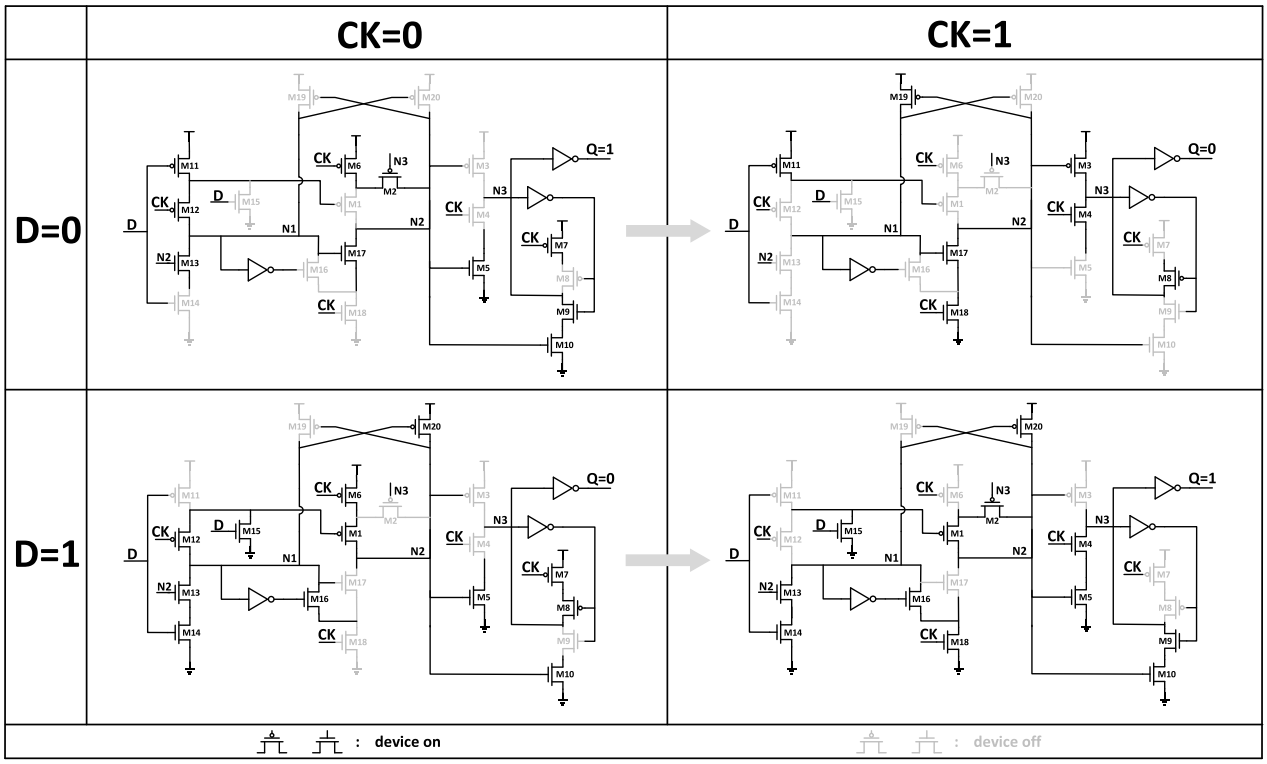

Fig. 5. Operation diagram of the proposed FF at different D and CK.

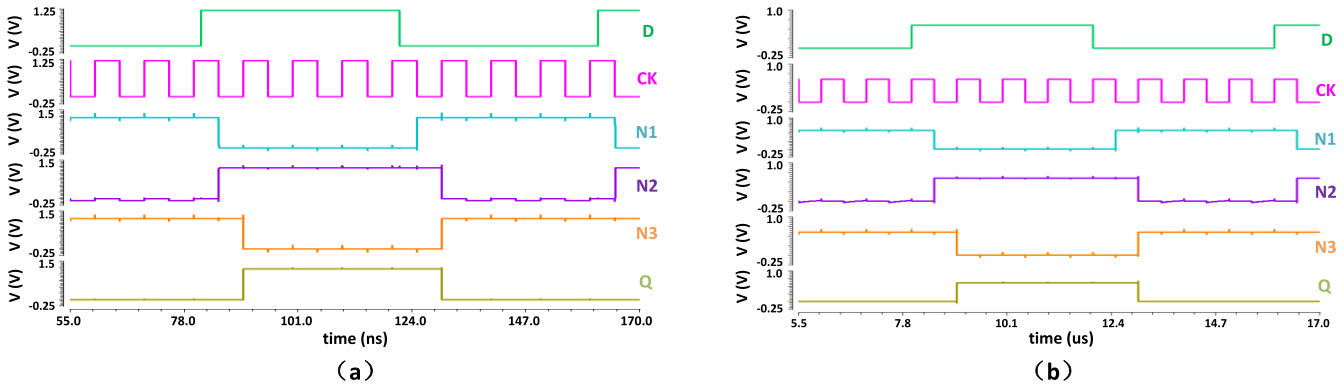

Fig. 6. Transient waveform of the proposed FF at (a) 1.2 and (b) 0.6 V.

High-to-Low Transition: When CK is low, the node N1 is charged to VDD through M11 and M12, the node N2 is charged to VDD through M6 and M2, the node N3 keeps low through M9 and M10, and the output Q keeps high. At the rising edge of CK, N2 is discharged to GND through M17 and M18, and then M13 is turned off to isolate the FF from changes in the input data. At the same time, the node N3 is charged to VDD through M3, and then the output Q changes to 0. The voltage of N1 keeps high through M19, while the voltage of N2 keeps low through M17 and M18 during the positive half cycle of CK.

Low-to-High Transition: When CK is low, N2 is charged to VDD through M6 and M1, N1 is discharged to GND through M13 and M14, the node N3 keeps high through M7 and M8, and the output keeps low. At the rising edge of CK, the input data is isolated through M12, and the node N3 is discharged to GND through M4 and M5, then the output Q changes to 1. The voltage of N1 keeps low through M16 and M18, while the voltage of N2 keeps high through M20 during the positive half cycle of CK.

Fig. 6 shows the transient waveform of the proposed FF at the supply voltage of 1.2 and 0.6 V, respectively. As shown in Fig. 6(a) and (b), the proposed FF works correctly at both superthreshold and near-threshold supply voltage. Moreover, the node N2 in the proposed FF no longer needs to be precharged to VDD when the input data remains 0, which saves much power compared with S^2CFF. It can also be seen from the transient waveform that N2 is floating only when the

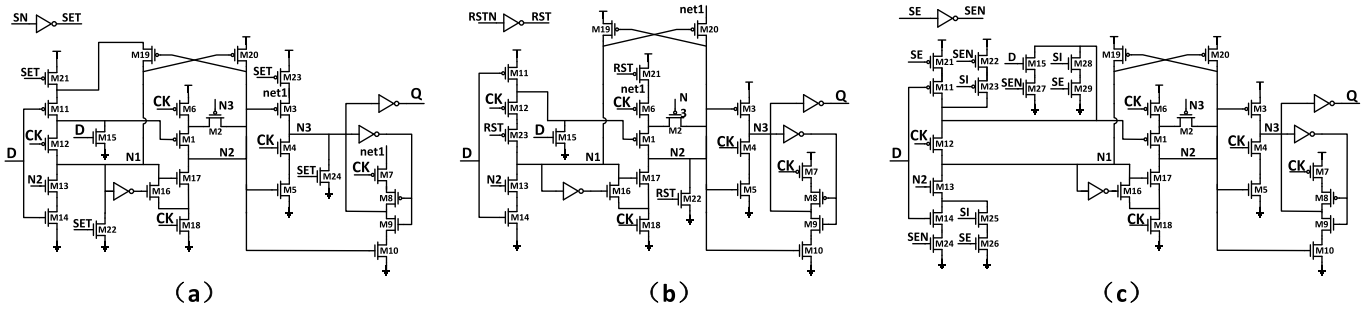

Fig. 7. Schematic of the proposed FF with (a) set, (b) reset, and (c) scan.

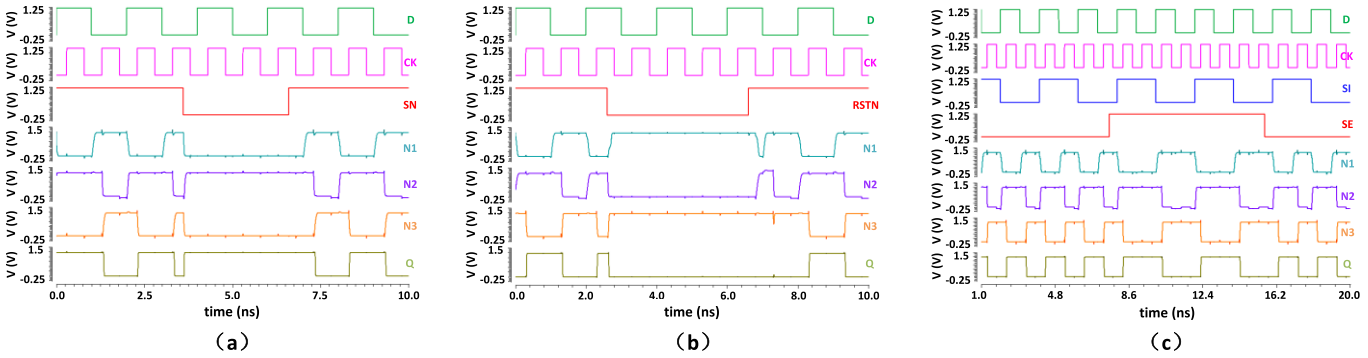

Fig. 8. Transient waveform of the proposed FF with (a) set, (b) reset, and (c) scan.

input remains 0 and the clock is low, which does not affect the function and power consumption of the FF as described in floating node analysis.

E. Additional Functions of the Proposed FF

In digital systems, FFs usually need to have additional functions such as set, reset, and scan. These additional functions can be easily added to the proposed FF. The schematic of the proposed FF with such additional functions is shown in Fig. 7.

As shown in Fig. 7(a), when the set signal SN is low, SET is high, the charging path of N1 is cutoff by M21, and N1 is pulled down through M22. Since the node N1 is low, N2 is charged to VDD through M20. At the same time, the charging path of N3 is cutoff by M23, N3 is pulled down through M24, and the output keeps high. Fig. 8(a) shows the transient waveform of the proposed FF with a set function. As shown in Fig. 8(a), when SN is low, which means that the FF is in the set state, the output Q keeps high. On the contrary, when SN is high, the FF works normally.

Fig. 7(b) shows the schematic of the proposed FF with reset function. As shown in Fig. 7(b), when the reset signal RSTN is low, RST is high, the charging path of N2 is cutoff by M21, and N2 is pulled down through M22. Since N2 is low, N3 is charged to high through M3, and the output Q keeps low. At the same time, N1 is charged to high through M19. A PMOS M23 is inserted to isolate N1 from the input to avoid short circuit current through M12 and M15 when CK $= 0$ and $D = 1$. Fig. 8(b) shows the transient waveform of the proposed FF with reset function. As shown in Fig. 8(b), when RSTN is low, which means that the FF is in the reset state, the output Q keeps low. On the contrary, when RSTN is high, the FF captures the input data correctly at the rising edge of CK.

Fig. 7(c) shows the schematic of the proposed FF with the scan function. As shown in Fig. 7(c), when the scan enable signal SE is high, the input data D is isolated from the FF, and the FF captures the data of scan input SI at the rising edge of CK. When SE is low, SI is isolated from the FF, and the FF captures the input data D at the rising edge of CK. The transient waveform of the proposed FF with scan function is shown in Fig. 8(c).

F. Soft-Error Tolerant Optimization of the Proposed FF

Although scaling down the supply voltage can significantly decrease the power consumption of digital systems, aggressive voltage scaling will increase the soft error susceptibility of the systems [19]. In order to improve the stability of low-voltage systems, the proposed FF can be hardened to resist the single event effect (SEE), which includes single event upset (SEU) and single event transient (SET) [20].

Fig. 9 shows the transient waveform of an SEU at node N2 in both TGFF and the proposed FF. As shown in Fig. 9, the node N2 in the proposed FF is susceptible to SEUs, similar to TGFF. This is because when the voltage of N2 drops from VDD to GND due to an SEU, M3 and M19 are ON, the nodes N3 and N1 are charged to VDD, and the data stored in the FF is overwritten. Similarly, the nodes N1, N3, N4, and N5 in the proposed FF are all susceptible to SEUs.

C-element-based logic has been proved to be an effective method for hardening [21]–[23]. By using C-element-based logic, the proposed FF can be insensitive to SEUs. The schematic of the proposed SEU-tolerant FF is shown

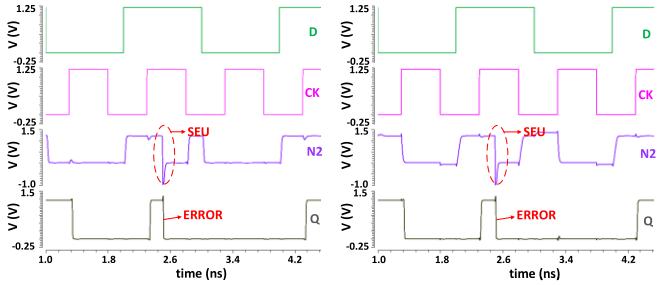

Fig. 9. Transient waveform of an SEU at node N2 in (a) TGFF and (b) proposed FF.

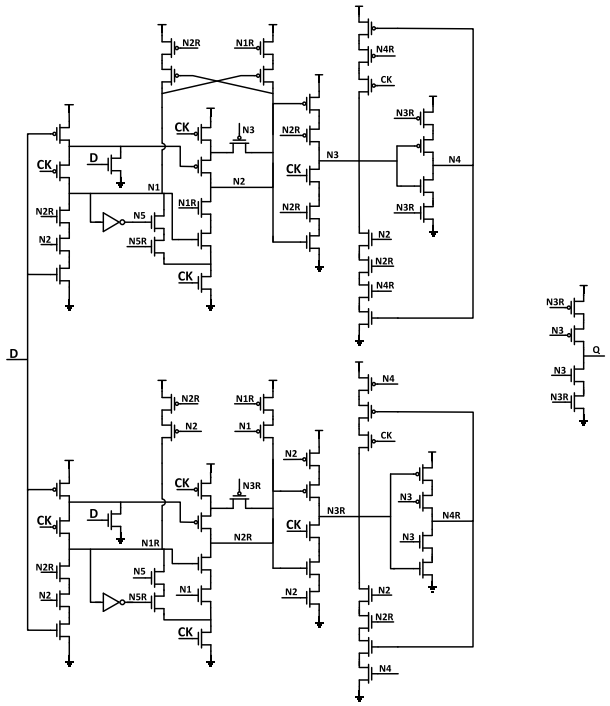

Fig. 10. Schematic of the proposed SEU-tolerant FF.

in Fig. 10. Again, the node N2 is taken as an example to analyze the susceptibility of the proposed SEU-tolerant FF to SEUs. When the node N2 in the proposed SEU-tolerant FF drops from VDD to GND due to an SEU, nodes N1 and N3 will not charge to VDD since nodes N1 and N3 are isolated from N2 by the transistors controlled by N2R. Similarly, other vulnerable nodes have also been hardened. Table I lists all vulnerable nodes in the proposed FF. As shown in Table I, all vulnerable nodes in the proposed SEU-tolerant FF have been hardened. Fig. 11 shows the transient waveform of the proposed SEU-tolerant FF with several SEUs at the internal nodes. As shown in Table I and Fig. 11, the proposed SEU-tolerant FF achieves complete SEU masking. As for SETs at the input ports, the proposed FF can use the C-element-based temporal filter in [24] to harden the input ports D and CK.

IV. Simulation Results

In order to evaluate the proposed FF, TGFF, SPC-18T FF, S^{2}CFF, ACFF, and TCFF have been designed based on SMIC 55-nm CMOS technology. Hspice with the same settings is adopted to perform all post-layout simulations for accurate

TABLE I
ALL VULNERABLE NODES IN THE PROPOSED FF

Node	N1	N2	N3	N4	N5
Unhardened FF	vulnerable	vulnerable	vulnerable	vulnerable	vulnerable
SEU-tolerant FF	hardened	hardened	hardened	hardened	hardened

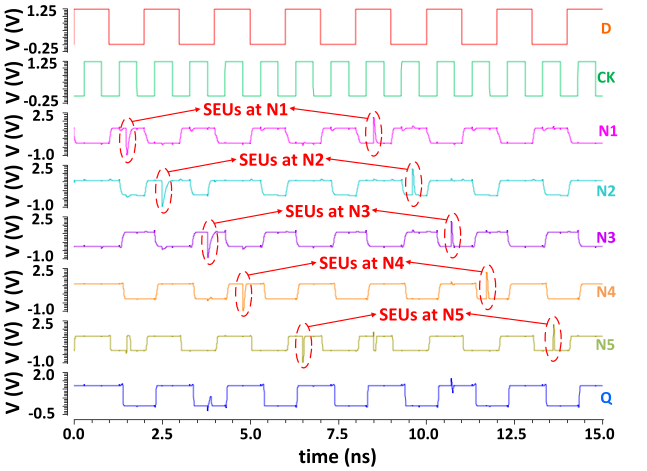

Fig. 11. Transient waveform of the proposed SEU-tolerant FF with several SEUs at the internal nodes.

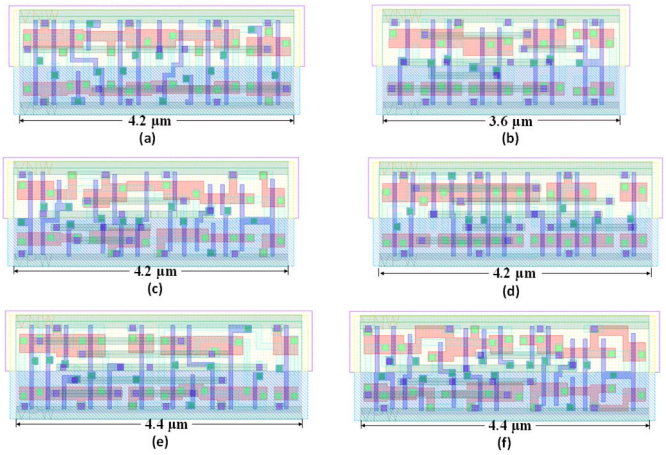

Fig. 12. Layouts of these FFs. (a) Layout of TGFF. (b) Layout of SPC-18T. (c) Layout of S^{2}CFF. (d) Layout of ACFF. (e) Layout of TCFF. (f) Layout of the proposed FF.

comparisons. The comparisons of the above FFs are described in detail in the following.

Fig. 12 shows the layouts of these FFs. The height of all layouts is fixed at 1.4 μm to improve compatibility in EDA tools. The area of the proposed FF is only 4.8% larger than that of S^{2}CFF, which indicates that the proposed FF does not bring a large area overhead in solving the redundant precharge operation. The proposed FF is also just 4.8% larger than that of TGFF which means the proposed FF is still suitable for large-scale integrated circuits design.

Fig. 13(a) demonstrates the normalized power of the proposed FF and other FFs at different data activity at 1.2 V. The clock frequency of all FFs is fixed at 100 MHz and the load is fixed at four inverters for a fair comparison. As described

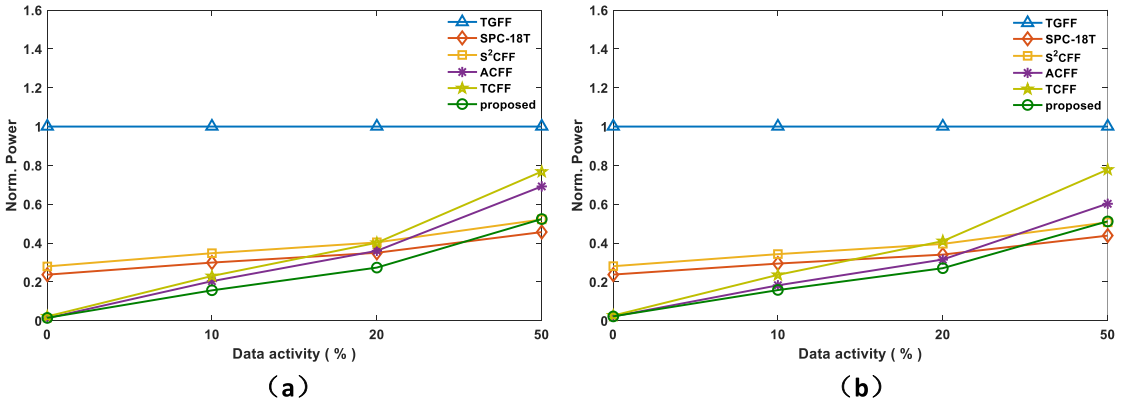

Fig. 13. Normalized power of the proposed FF and other FFs at different data activity at the supply voltage of (a) 1.2 and (b) 0.6 V.

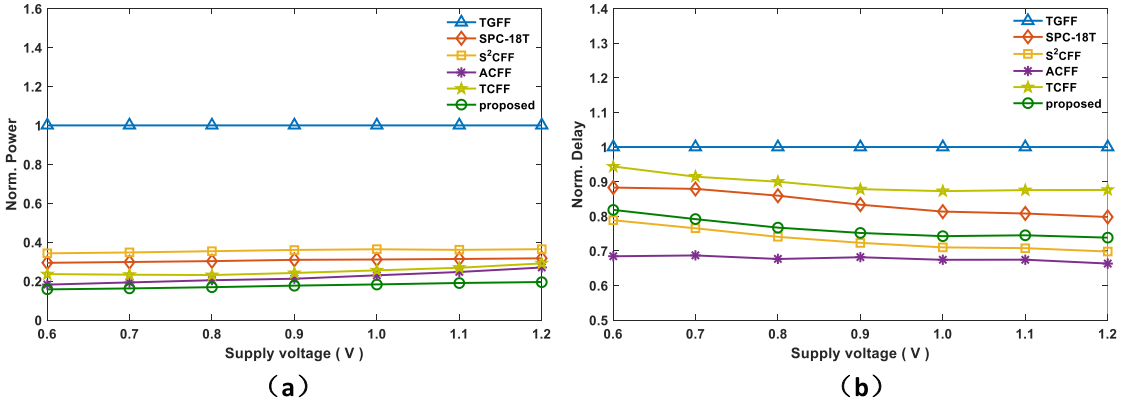

Fig. 14. Normalized parameters of the proposed FF and other FFs at different supply voltage varying from 0.6 to 1.2 V. (a) Power. (b) Delay.

in [15] that the average data activity of FFs in large-scale integrated circuits is typically between 5% and 15%, the proposed FF can provide significant energy efficiency improvements when applied to large-scale integrated circuits, which is due to the removal of redundant precharge operations. When the data activity drops to 0, the proposed FF consumes only 1.5% of the TGFF power consumption. This is mainly because when the data activity is 0, the proposed FF does not require any extra operation, and the power consumption at this time is only the leakage power. For TGFF, when the data activity is 0, the internal nodes in TGFF (CKN and CKI) still need to work as usual, which wastes much power consumption. As for other FFs such as SPC-18T FF and S^{2}CFF, precharge and discharge operations are still needed when the data remains 0, which shows lower energy efficiency compared with the proposed FF. There is no redundant precharge operation in ACFF and TCFF, and the two kinds of FFs show high energy efficiency when the data activity is 0. But the current contention (in ACFF) and a great number of shared transistors (in TCFF) make the power of the two FFs increase faster with the data activity, reducing their energy efficiency. In order to verify the power consumption of the proposed FF under near-threshold supply voltage, similar simulations have been applied to the FFs with a supply voltage of 0.6 V and clock frequency of 10 MHz. As shown in Fig. 13, the proposed FF has similar energy efficiency at 0.6 and 1.2 V, showing huge power advantages.

Fig. 14(a) shows the normalized power evaluation under the supply voltage settings varies from 0.6 to 1.2 V at the data activity of 10% and clock frequency of 10 MHz. As shown in Fig. 14(a), the proposed FF shows significant power consumption advantages at all supply voltages. Compared with TGFF, the proposed FF can save more than 80% of power consumption at different supply voltages.

Fig. 14(b) shows the normalized CK-to-Q delay under the supply voltage settings varies from 0.6 to 1.2 V. The proposed FF has a similar delay to S^{2}CFF, which is lower than that of TGFF, SPC-18T FF and TCFF at all supply voltages. Compared with TGFF, the delay of the proposed FF is 26.18% lower at a supply voltage of 1.2 V.

To verify the robustness of the proposed FF at near-threshold supply voltage, 1000-points Monte Carlo simulations considering both die-to-die global variations and within-die random mismatch variations have been performed to all kinds of FFs at a supply voltage of 0.6 V, data activity of 10%, and clock frequency of 10 MHz. Table II shows the results of the Monte Carlo simulations in detail. As shown in Table II, the power of the proposed FF is greatly reduced compared with other FFs. TGFF, S^{2}CFF, and the proposed FF show strong robustness under near-threshold supply voltage. The robustness of SPC-18T FF, ACFF, and TCFF at low supply voltage is poor, which is due to the contention path (SPC-18T FF and ACFF) and the voltage drop of too many shared transistors (TCFF).

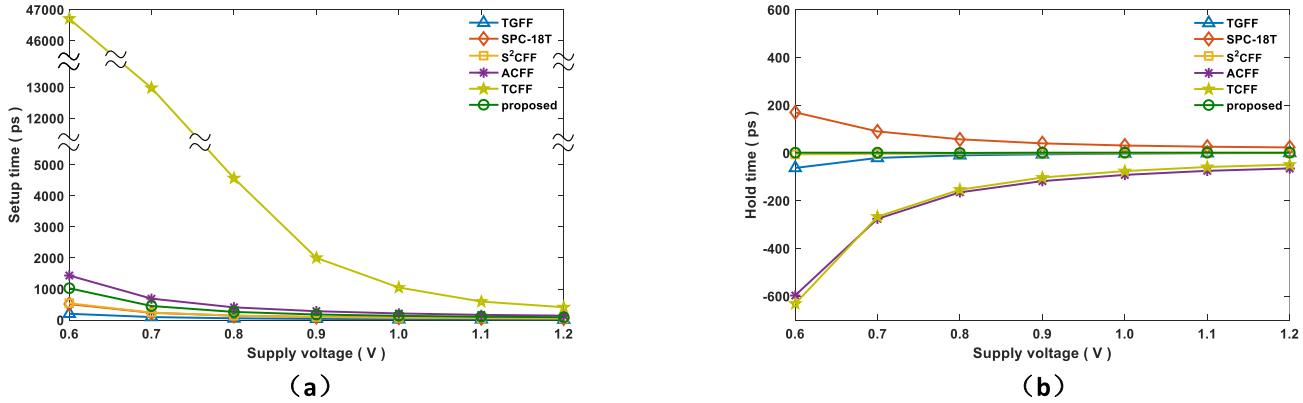

Fig. 15. Setup and hold time of the proposed FF and other FFs at different supply voltage varying from 0.6 to 1.2 V. (a) Setup time. (b) Hold time.

TABLE II
RESULTS OF MONTE CARLO SIMULATIONS

	TGFF	SPC-18T	S²CFF	ACFF	TCFF	proposed
Mean_delay (ps)	1047	1032	762.5	752.6	904.7	763.3
Sigma_delay (ps)	286.3	418.1	208.4	286.5	373.6	204.5
Mean_power (nW)	26.56	7.84	9.18	5.27	5.41	4.56
Sigma_power (nW)	1.19	0.68	0.79	1.03	1.32	1.19
Error count	0	32	0	56	525	0

Fig. 15(a) shows the setup time of these FFs. Setup time of TCFF and ACFF is larger than that of the proposed FF. Especially for TCFF, the setup time deteriorates sharply as the voltage drops, which is due to the aggressive logic simplification measures as described in [25]. Setup time of the proposed FF is a little larger than that of S^{2}CFF, which is mainly due to the fact that in the proposed FF, the precharge operation of the internal node N2 is data-dependent. To perform the precharge operation, the gate of M1 needs to be pulled down through M15 first, and then the precharge operation is completed through M6 and M1. Fig. 15(b) shows the hold time of these FFs. The hold time of the proposed FF is near zero which is similar to that of TGFF and S^{2}CFF, better than SPC-18T. Different from other FFs, the hold time of the proposed FF and S^{2}CFF changes little when the supply voltage drops. This is mainly because the hold time of the proposed FF and S^{2}CFF is mainly determined by the pull-down speed of the node N1 and N2. When the supply voltage drops, the pull-down speed of N1 and N2 decreases at a similar speed, and the hold time changes little. The hold time of TCFF and ACFF is negative at different supply voltages. This is because in these two FFs, the path delay from the clock CK to the latch circuit is much shorter than that from the input data *D* to the latch circuit, and the change of the input data in a short time before the rising edge of CK will not propagate to the latch circuit to rewrite the latched data, so the hold time of these two FFs can be negative.

Table III shows a comparison of the proposed FF with other state-of-the-art FFs. With the employment of the input-aware precharge scheme, the power of the proposed FF is much lower than that of other FFs. Thanks to the contention-free structure, the proposed FF shows great robustness under near-threshold

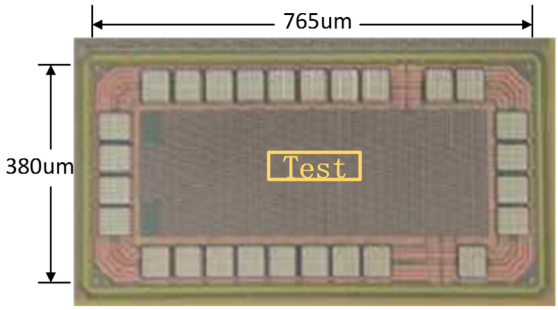

Fig. 16. Die micrograph of the test chip.

supply voltage. Also, the CK-to-Q delay of the proposed FF is reduced compared with TGFF. Both $PDP_{CK\text{-}to\text{-}Q}$ and $PDP_{D\text{-}to\text{-}Q}$ are employed to evaluate the composite performance of these FFs. As shown in Table III, the PDP of the proposed FF is the lowest among these FFs. The area of the proposed FF is just 4.8% larger than TGFF, showing little extra area overhead. Thus, the proposed FF is an excellent alternative to conventional TGFF in ultralow-power digital systems.

Table IV shows the performance of the proposed FF with additional functions. In the FF with set function, the pull-up path of N3 is weakened and the load of N3 is slightly increased, so the CK-to-Q delay of the FF is slightly increased. Since the load of N1 is slightly increased in the FF with set function, the setup time is also slightly increased. In the FF with reset function, the load of N2 is slightly increased, so the CK-to-Q delay is slightly increased. Since the precharge path of N2 is weakened in the FF with reset function, the setup time is increased. In the FF with scan function, the charge and discharge paths of N2 and N3 are not changed, so the CK-to-Q delay is not increased. Since the pull-down path of N1 and the pull-down path of the gate of M1 are weakened in the FF with scan function, the setup time is increased. The CK-to-Q delay of the SEU-tolerant FF is significantly increased due to the C-element-based logic. Also, the setup time of the SEU-tolerant FF is slightly increased. All these FFs have a similar hold time except the FF with scan function. This is because in the FF with scan function, the pull-down path of N1 is weakened while the pull-down path of N2 remains, so the input data needs longer time to pull down the node

TABLE III
PERFORMANCE SUMMARY AND COMPARISON OF VARIOUS FF

	TGFF conventional	SPC-18T JSSC 2019	S²CFF ISSCC 2014	ACFF ISSCC	TCFF JSSC 2014	proposed	XCFF [1] VLSI 2005	RTFF [1] TCAS-I 2018
Technology (Reported)	--	65nm	45nm SOI	40nm	40nm	55nm	100nm	28nm FDSOI
Single-Phase clocked	No [2]	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Low-voltage operation	Yes	No [3]	Yes	No [3]	No [4]	Yes	No [3]	No [3]
Output Inverter	Yes	Yes	Yes	Yes	Yes	Yes	No	No
Area (μm²) (Norm.)	5.88 (1x)	5.04 (0.857x)	5.88 (1x)	5.88 (1x)	6.16 (1.048x)	6.16 (1.048x)		
Power (nW) @ 1.2V, 100MHz, 10% Data Activity (Norm.)	1037.93 (1x)	310.64 (0.30x)	360.79 (0.35x)	211.26 (0.20x)	238.99 (0.23x)	162.18 (0.16x)		
Power (nW) @ 0.6V, 10MHz, 10% Data Activity (Norm.)	26.07 (1x)	7.67 (0.29x)	8.94 (0.34x)	4.75 (0.18x)	6.16 (0.24x)	4.11 (0.16x)		
Leakage (nW) @ 1.2V	10.34	3.82	4.59	12.22	8.89	5.76		
Setup Time (ps) @1.2V	18	54	52	142	414	92		
Hold Time (ps) @ 1.2V	0	23	-1	-65	-49	1		
Delay$_{CK\text{-}to\text{-}Q}$ (ps) @	104.73	83.56	73.11	69.47	91.74	77.31		
Delay$_{D\text{-}to\text{-}Q}$ (ps) @ 1.2V	122.7	137.6	125.1	211.5	505.7	169.3		
PDP$_{CK\text{-}to\text{-}Q}$ (fJ) [5] (Norm.)	0.109 (1x)	0.026 (0.24x)	0.026 (0.24x)	0.015 (0.14x)	0.022 (0.20x)	0.013 (0.12x)		
PDP$_{D\text{-}to\text{-}Q}$ (fJ) [5] (Norm.)	0.127 (1x)	0.043 (0.34x)	0.045 (0.35x)	0.045 (0.35x)	0.121 (0.95x)	0.027 (0.21x)		

1) : Not implemented.

2) : Inverted clock signal is used.

3) : There are contention paths in the circuit.

4) : Voltage drop of so many shared transistors.

5) : power-delay-product (PDP) @ 1.2V, 100MHz, 10% data activity.

TABLE IV
PERFORMANCE OF THE PROPOSED FF WITH ADDITIONAL FUNCTIONS

	proposed	With set	With Reset	With Scan	SEU-tolerant
Delay (ps)	77.31	98.25	88.40	77.46	161.45
Setup time	92	109	147	146	114
Hold time	1	1	4	-14	1
Power (nW) [1]	162.18	172.85	183.47	181.70	335.32
Area (μm²)	6.16	8.12	7.28	8.96	16.24

1) : @ 1.2V, 100MHz, 10% Data Activity.

TABLE V
FEATURE COMPARISON OF THE COUNTERS WITH DIFFERENT SEQUENCING ELEMENTS AT THE SUPPLY VOLTAGE OF 1.2 V

Design	TGFF	S²CFF	ACFF	TGPL	proposed
F_{MAX} (MHz)	899.3	882.6	846.0	950.6	859.8
Power (μW) [1]	27.12	19.56	17.28	21.36	16.92
Area (μm²)	171.36	175.84	175.84	147.84	180.32

1) : @ 100MHz.

N1, and the hold time is reduced. The area and power of the FFs with additional functions such as set, reset, and scan are slightly increased compared with the proposed FF, while the SEU-tolerant FF has slightly more than twice the area and power of the proposed FF.

To validate the benefit of the proposed FF in the real digital circuit, five 16-bit counters based on TGFF, S²CFF, ACFF, transmission-gate-pulsed latch (TGPL) [26], [27], and the proposed FF are designed for comparison. As shown in Table V, the counter based on the proposed FF has the lowest power consumption among these designs. Since the logic in TGPL is greatly simplified compared with TGFF, and the pulse generator can be reused, the power of the TGPL-based counter is greatly reduced compared with that of the TGFF-based counter. However, since the complementary clock signals are still required in the latch, the power of the TGPL-based counter is still significantly larger than that of the counter based on the proposed FF. Since the maximum frequency is related to the D-to-Q delay of the sequencing element, the counter based on TGPL has the largest maximum frequency due to its negative setup time, but TGPL is not suitable for low voltage circuits due to the enlarged variability of the pulsed width at low supply voltage as described in [27]. Also, the TGPL-based circuit shares a pulse generator to reduce power consumption, and the pulsewidth will change during propagation, which will further increase the uncertainty of the pulsewidth. Since the D-to-Q delay of the proposed FF is slightly smaller than that of ACFF, the maximum frequency of the counter based on the proposed FF is a little larger than that of the ACFF-based counter. Since the area of the proposed FF is just 4.8% larger than that of TGFF, the area of the counter based on the proposed FF is just 5.2% larger than that of the TGFF-based counter.

V. EXPERIMENTAL RESULTS

To validate the energy efficiency of the proposed design, two 5-bit * 10-stage shift registers based on the proposed FF and TGFF were fabricated in the SMIC 55-nm CMOS process. Fig. 16 shows the die micrograph of the test chip.

Fig. 17(a) demonstrates the measured waveform of the test chip at a supply voltage of 0.6 V, data activity of 10%, and clock frequency of 10 MHz. With the contention-free structure, the proposed FF can provide robust low voltage operations. Fig. 17(b) shows the measured waveform at a supply voltage of 1.2 V, data activity of 10%, and clock frequency of 1 Hz. With the retentive architecture, the proposed FF works correctly at ultralow clock frequency.

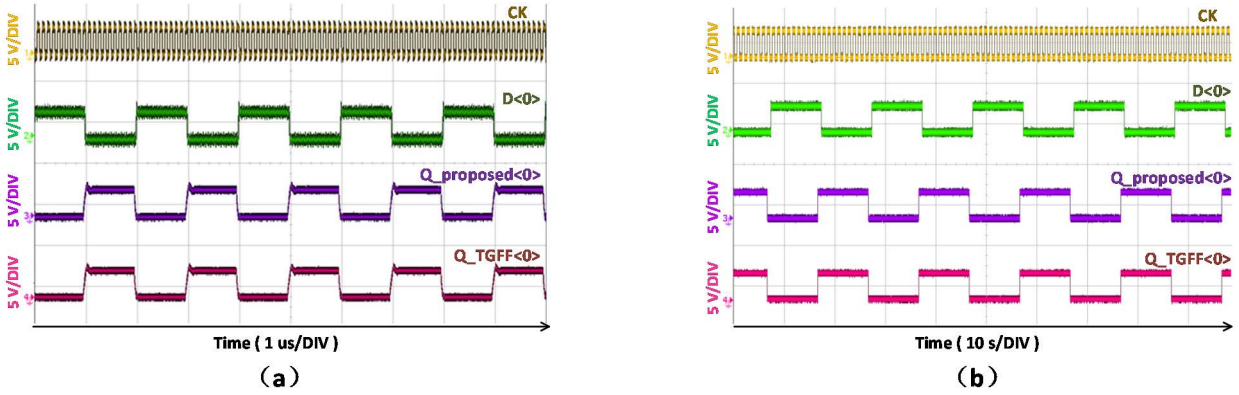

Fig. 17. Measured waveform of the shift registers at (a) 0.6 V, 10 MHz, 10% data activity and (b) 1.2 V, 1 Hz, 10% data activity.

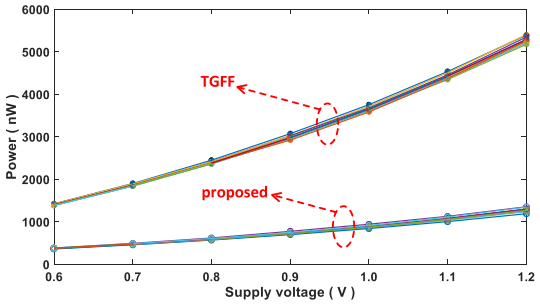

Fig. 18. Measured total power of the shift registers against the supply voltage (10 MHz, 10% data activity, ten test chips).

TABLE VI
MEASUREMENT RESULTS OF THE SHIFT REGISTERS AT ULTRALOW VOLTAGE

Design	V_{MIN} (V) @ 1MHz		Power (nW) @ 0.3V, 1MHz, 10% data activity	
	Mean	Sigma	Mean	Sigma
TGFF	0.217	0.012	38.74	1.42
proposed	0.225	0.011	12.85	1.07

Fig. 18 shows the measured total power of the two shift registers in ten test chips against the supply voltage. As can be observed, the proposed FF shows a great energy efficiency improvement compared with TGFF. At all test voltages of all test chips, the power consumption of the proposed FF is at least 73% lower than that of TGFF.

Table VI shows the measurement results on minimum operating voltage (V_{MIN}) of the two shift registers at the clock frequency of 1 MHz over ten test chips. All test chips work correctly even at the supply voltage of lower than 0.3 V (nominal supply voltage of SMIC 55-nm CMOS technology is 1.2 V). As shown in Table VI, the standard deviation of V_{MIN} of the shift register based on the proposed FF is even smaller than that of the TGFF-based shift register, which indicates that the proposed FF is robust to process variation even at ultralow supply voltage. The power consumption of the two shift registers at a supply voltage of 0.3 V, data activity of 10%, and clock frequency of 1 MHz is also shown in Table VI. As shown in Table VI, the power consumption of the shift register based on the proposed FF is much lower than that of the TGFF-based shifter register at ultralow supply voltage, showing a great power consumption advantage.

VI. CONCLUSION

In this article, an energy-efficient retentive TSPC FF is proposed. By removing redundant precharge and discharge operations with the input-aware precharge scheme, the power of the proposed FF is greatly reduced. Furthermore, floating node analysis is applied to the proposed structure to avoid the generation of short-circuit paths. Then, transistor level optimizations are applied to the circuit to further reduce the area and power consumption. Postlayout simulation results show that the proposed FF saves more than 80% power consumption compared with TGFF under 10% data activity. Measurement results of ten test chips also demonstrate that the proposed FF has a significant energy efficiency improvement compared with TGFF. The CK-to-Q delay of the proposed FF is 26.18% lower than that of TGFF. The area of the proposed FF is just 4.8% larger than that of TGFF, indicating little area overhead to achieve such benefits.

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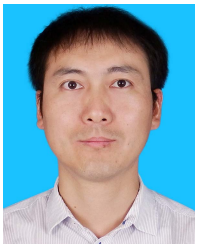

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