

INTERNATIONAL INSTITUTE OF INFORMATION TECHNOLOGY  
BANGALORE

VLSI SUMMER PROJECT

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# TRUE RANDOM NUMBER GENERATION

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# INTRODUCTION

A true random number generator (TRNG) uses a nondeterministic source to make randomness. Mostly generated by measuring unpredictable natural processes, like pulse detectors of ionizing radiation activities, gas discharge tubes, leaky capacitors. Physical phenomena like metastability and chaos are also used to generate random numbers in logical devices

## ARCHITECTURE

An entropy source is identified and the entropy is extracted to generate True Random Numbers. An entropy source is a physical source of information whose output either appears to be random in itself or by applying some filtering/distillation process. The design used in this project is Latched Ring Oscillators.

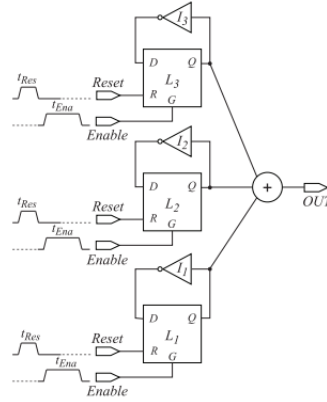


Figure 1: TRNG Architecture

## WORKING

There are three latches in a ring oscillator form using three inverters. The outputs of the latches(D) will be logic '0' when the reset signal is set as logic '1'. The latches will be transparent if enable signal is '1'. When the latches are transparent a free running oscillation comes out, whereas, when they enter in the hold state, the logic value of the output bit is sampled. The random bit is generated by following process. First, all three latches are reset to zero by setting reset signal high. Then, reset is set low and enable signal is set high, making the latch transparent. Now, since the latch makes a ring oscillator the output oscillates from low to high. Then, the enable signal is set low and output bit is sampled. Upon sampling the output bit, the latches are again reset.

## IMPLEMENTATION

The verilog implementation of the TRNG architecture (figure 1) is as follows.

////////////////////////////////////

```
module top(input clk);
    wire en,res;
    reg bits;
    wire q1,q2,q3;
    reg ena,wea;
    reg [3:0] addra;
    latch l1(~q1,res,en,q1);
    latch l2(~q2,res,en,q2);
    latch l3(~q3,res,en,q3);
    initial begin
        ena=1;
        wea=0; //read only
        addra = 4'b0000;
    end

    blk_mem_gen_0 bram_res (
        .clka(clk),    // input wire clka
        .ena(ena),     // input wire ena
        .wea(wea),     // input wire [0 : 0] wea
        .addra(addra), // input wire [3 : 0] addra
        .dina(dina),   // input wire [0 : 0] dina
        .douta(res)    // output wire [0 : 0] douta
    );

    blk_mem_gen_1 bram_en (
        .clka(clk),    // input wire clka
        .ena(ena),     // input wire ena
        .wea(wea),     // input wire [0 : 0] wea
        .addra(addra), // input wire [3 : 0] addra
        .dina(dina),   // input wire [0 : 0] dina
        .douta(en)     // output wire [0 : 0] douta
    );

    ila_0 inst_ila(
        .clk(clk), // input wire clk

        .probe0(en), // input wire [0:0] probe0
        .probe1(res), // input wire [0:0] probe1
        .probe2(bits), // input wire [0:0] probe2
        .probe3(q1), // input wire [0:0] probe3
    );
endmodule
```

```

.probe4(q2), // input wire [0:0]  probe4
.probe5(q3) // input wire [0:0]  probe5
);

always @(q1 or q2 or q3) begin
    bits=q1^q2^q3;
end

always @(posedge clk)
begin
    addra <= addra + 4'b0001;
end
endmodule

```

```

module latch( input d,input rst,input en,output reg q);
    always @(d or rst or en) begin
        if(rst)
            q=0;
        else begin
            if(en)
                q=d;
        end
    end
end
endmodule

```

////////////////////////////////////

The module latch is instantiated thrice in top module to implement three latches. The output of the latch is inverted and given as input to make a ring oscillator. The inputs are given using Block RAMs. There are 2 BRAMs, one for en(enable) signal and another for res(reset) signal. The ILA is used to probe the outputs. The below shows the inbuilt IPs used

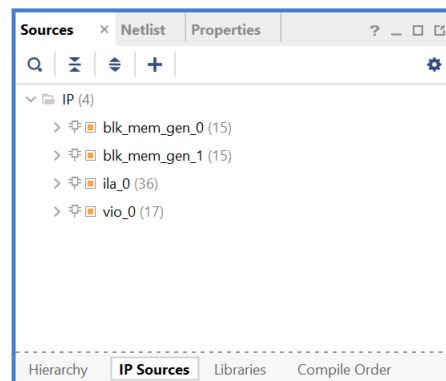


Figure 2: Schematic

# FPGA RESULTS

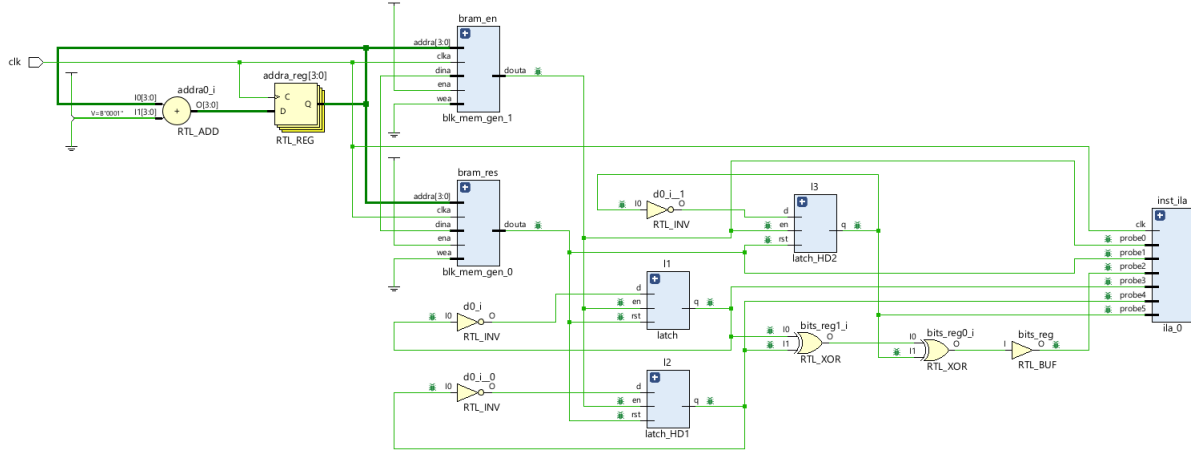


Figure 3: Schematic

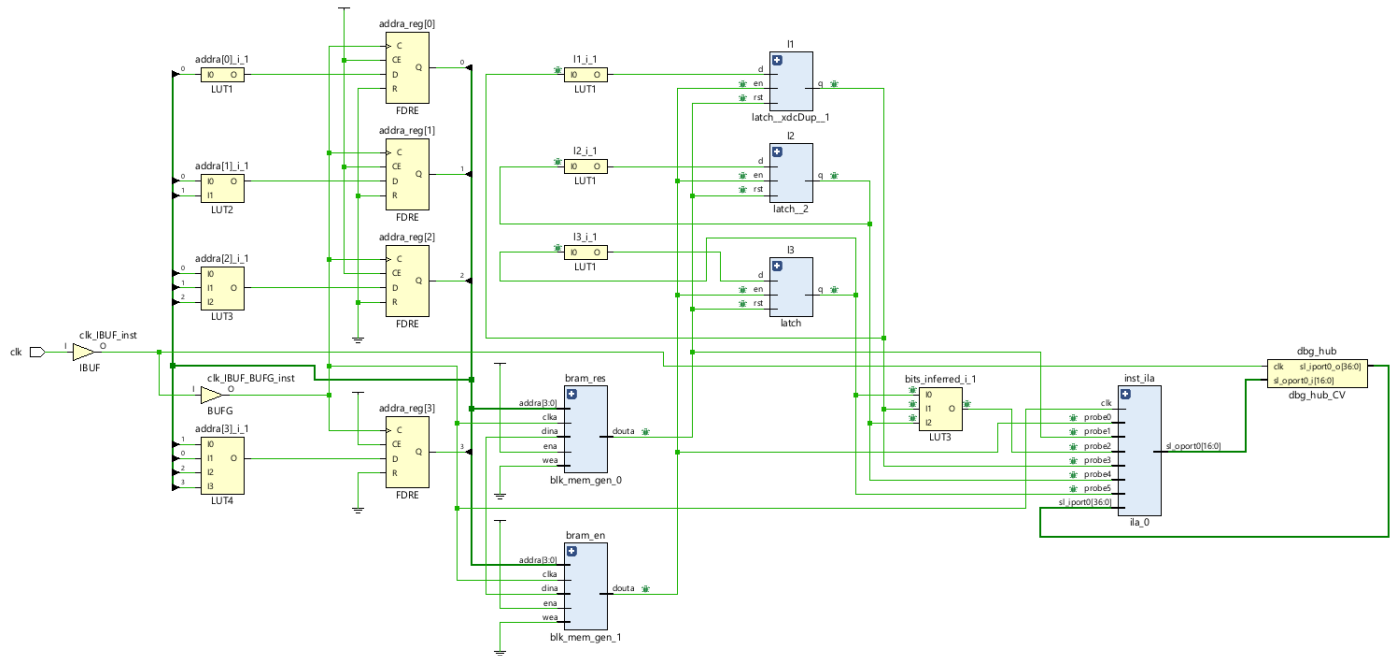


Figure 4: Synthesized Design

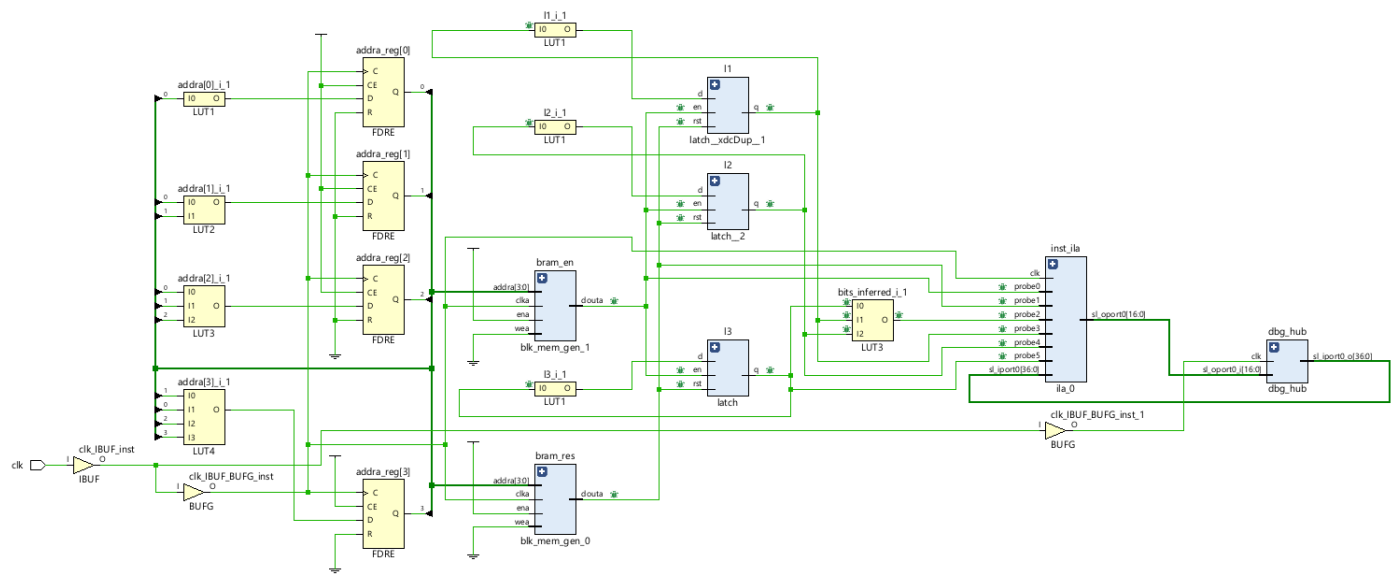


Figure 5: Post Implementation Schematic

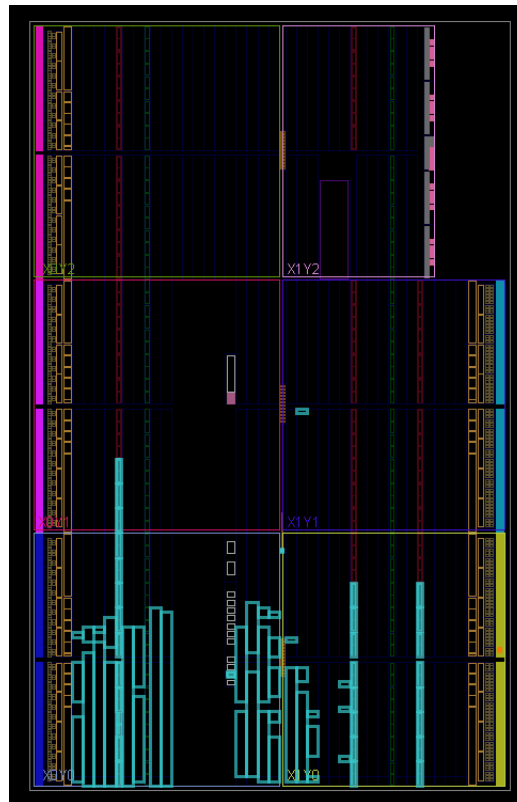


Figure 6: Implementation

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
▼ N top	1308	2092	3	693	1183	125	29	1	3	1
> I1 bram_en (blk_mem_gen_1)	0	0	0	0	0	0	0.5	0	0	0
> I1 bram_res (blk_mem_gen_0)	0	0	0	0	0	0	0.5	0	0	0
> I1 dbg_hub (dbg_hub)	450	741	0	245	426	24	0	0	1	1
> I1 inst_ila (ila_0)	853	1344	3	456	752	101	28	0	0	0
I1 I1 (latch_xdcDup_1)	0	1	0	1	0	0	0	0	0	0
I1 I2 (latch_2)	0	1	0	1	0	0	0	0	0	0
I1 I3 (latch)	0	1	0	1	0	0	0	0	0	0

Figure 7: Resource Utilisation

#### Design Timing Summary

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 2.559 ns	Worst Hold Slack (WHS): 0.051 ns	Worst Pulse Width Slack (WPWS): 3.750 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 5087	Total Number of Endpoints: 5071	Total Number of Endpoints: 2367

All user specified timing constraints are met.

Figure 8: Timing Results

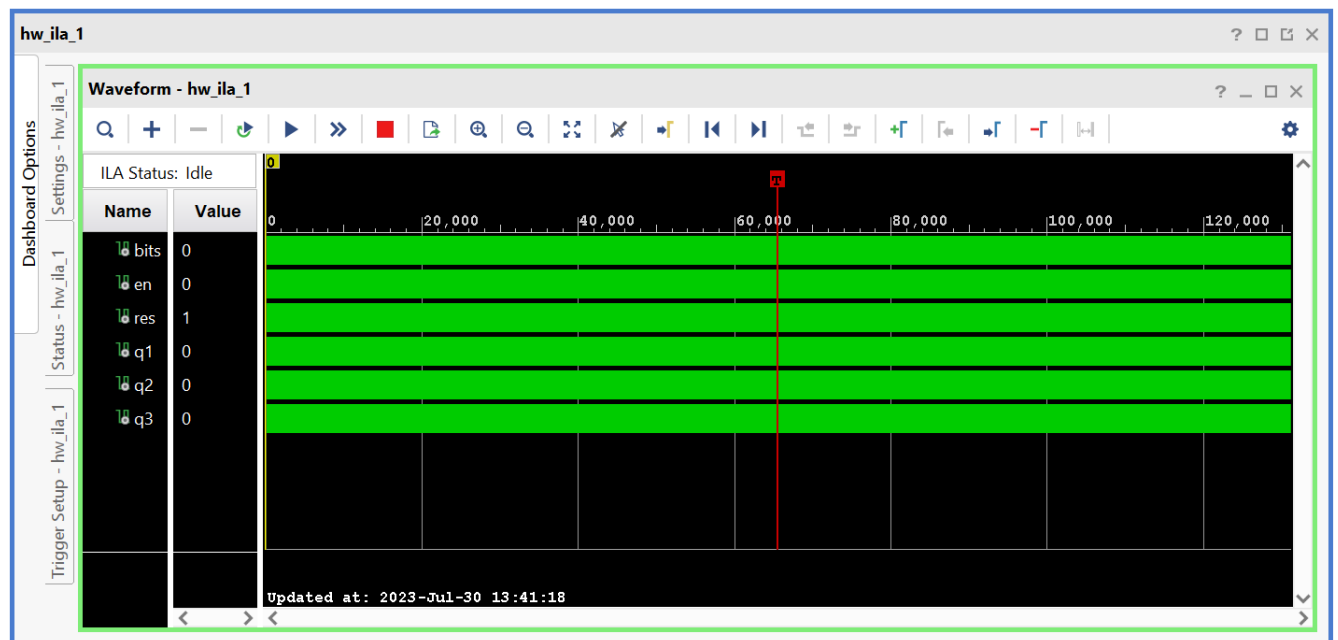


Figure 9: ILA Output



## Results

```
The following are the inputs given in the block ram using .coe file
////////////////////////////////////en////////////////////////////////////
memory_initialization_radix=2;
memory_initialization_vector=0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0;
////////////////////////////////////res////////////////////////////////////
memory_initialization_radix=2;
memory_initialization_vector=1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0;
```

There are 16 bits in each input file. Each bit is read in each clock cycle. Therefore en signal stays low for one cycle and high for 14 cycles then goes back to low. Similarly reset is high for only the first cycle and goes low for the rest of the 15 cycles. The latches get reset in the first clock cycle and then the latches are enabled. Then, upon closing the latches they go in a metastable state, where the output is sampled.

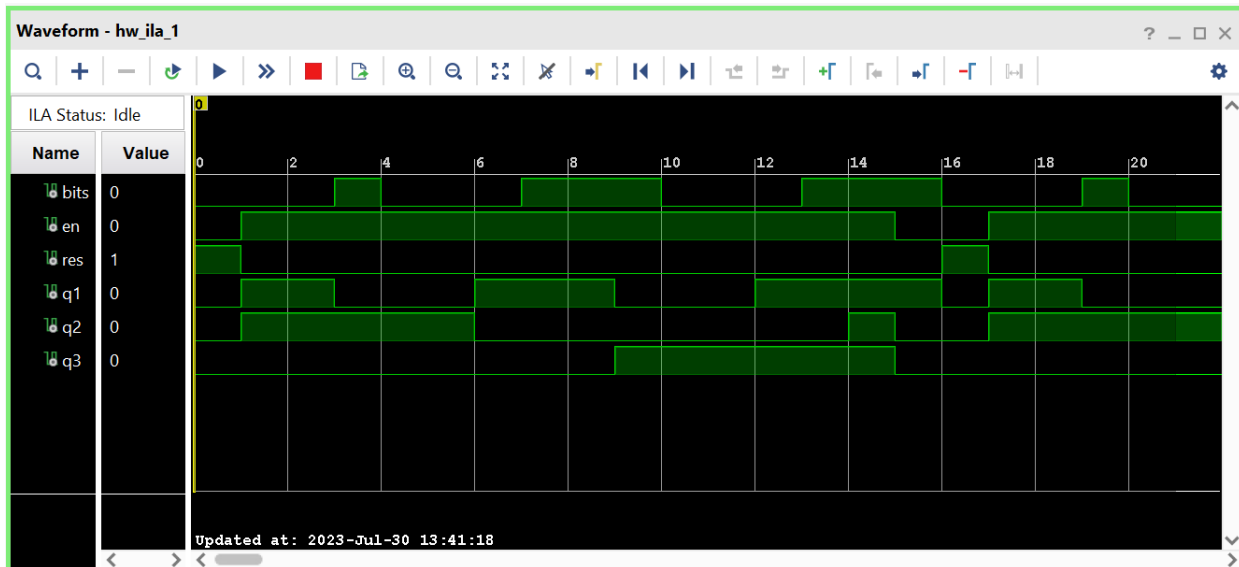


Figure 10: ILA Output

The same process is repeated. The random output bit is sampled every 16 clock cycles starting from the 15th clock cycle (both reset(res) and enable(en) should be low). The ILA data is exported and matlab was used to pick the bits where both res and en were low. The true random numbers were generated only by using three individual latches as well as by performing XOR on the outputs.

## NIST TEST

The NIST Test Suite is a statistical package consisting of 15 tests that were developed to test the randomness of binary sequences produced by either hardware or software based cryptographic random or pseudorandom number generators.

## Latch-1

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### RESULTS FOR THE UNIFORMITY OF P-VALUES AND THE PROPORTION OF PASSING SEQUENCES

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generator is <data/q1.txt>

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * Frequency
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * BlockFrequency
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * CumulativeSums
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * CumulativeSums
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * Runs
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * LongestRun
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * Rank
6	3	0	1	0	0	0	0	0	0	0.000040	*	8/10 FFT
3	0	0	0	0	0	0	3	0	4	0.004301		7/10 * NonOverlappingTemplate
4	3	0	0	1	0	0	1	0	1	0.035174		6/10 * NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
9	0	0	0	0	0	0	1	0	0	0.000000	*	2/10 * NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	1/10 * NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	3	0	7	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	2	0	8	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
1	0	0	0	0	0	0	2	0	7	0.000001	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	3	0	7	0.000000	*	10/10 NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate

[illegible]

[illegible]

## RESULTS FOR THE UNIFORMITY OF P-VALUES AND THE PROPORTION OF PASSING SEQUENCES

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
----	----	----	----	----	----	----	----	----	-----	---------	------------	------------------

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[illegible]

[illegible]

## Latch-3

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### RESULTS FOR THE UNIFORMITY OF P-VALUES AND THE PROPORTION OF PASSING SEQUENCES

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generator is <data/q3.txt>

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST
9	1	0	0	0	0	0	0	0	0	0.000000	*	2/10 * Frequency
9	1	0	0	0	0	0	0	0	0	0.000000	*	1/10 * BlockFrequency
9	1	0	0	0	0	0	0	0	0	0.000000	*	2/10 * CumulativeSums
10	0	0	0	0	0	0	0	0	0	0.000000	*	2/10 * CumulativeSums
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * Runs
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * LongestRun
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * Rank
1	0	0	1	0	3	0	3	0	2	0.122325	10/10	FFT
10	0	0	0	0	0	0	0	0	0	0.000000	*	3/10 * NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * NonOverlappingTemplate
0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10 NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * NonOverlappingTemplate
0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	2	0	8	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	4	0	6	0.000003	*	10/10 NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * NonOverlappingTemplate
0	0	0	0	0	0	0	3	0	7	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	1	0	0	1	0	8	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	2	0	8	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	1	0	0	4	0	5	0.000199	10/10	NonOverlappingTemplate
1	0	0	0	0	0	0	1	0	8	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	3	0	7	0.000000	*	10/10 NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * NonOverlappingTemplate
1	0	0	0	0	0	0	3	0	6	0.000040	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
2	0	0	0	3	0	0	3	0	2	0.066882	8/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	1	0	0	3	0	6	0.000040	*	10/10 NonOverlappingTemplate
0	1	0	0	0	0	0	2	0	7	0.000001	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
2	0	0	0	0	0	0	3	0	5	0.000954	10/10	NonOverlappingTemplate
2	2	0	0	2	0	0	3	0	1	0.213309	9/10	NonOverlappingTemplate
1	0	0	0	0	0	0	2	0	7	0.000001	*	10/10 NonOverlappingTemplate
0	0	0	0	2	0	0	3	0	5	0.000954	10/10	NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10 * NonOverlappingTemplate
2	3	0	0	3	0	0	2	0	0	0.066882	8/10	NonOverlappingTemplate



0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
1	1	0	0	2	0	0	4	0	2	0.066882		9/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
4	4	0	0	2	0	0	0	0	0	0.002043		7/10	* NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
1	0	0	0	1	0	0	3	0	5	0.002043		9/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
0	0	0	0	3	0	0	5	0	2	0.000954		10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
3	0	0	0	1	0	0	3	0	3	0.035174		9/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
1	0	0	0	1	0	0	1	0	7	0.000003	*	10/10	NonOverlappingTemplate
0	0	0	0	2	0	0	0	0	8	0.000000	*	10/10	NonOverlappingTemplate
0	0	0	0	1	0	0	2	0	7	0.000001	*	10/10	NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10	* NonOverlappingTemplate
5	0	0	0	3	0	0	2	0	0	0.000954		6/10	* NonOverlappingTemplate
4	1	0	0	2	0	0	2	0	1	0.066882		7/10	* NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
0	2	0	0	4	0	0	2	0	2	0.035174		10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
6	4	0	0	0	0	0	0	0	0	0.000003	*	6/10	* NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
1	0	0	0	0	0	0	4	0	5	0.000199		9/10	NonOverlappingTemplate
0	0	0	0	2	0	0	1	0	7	0.000001	*	10/10	NonOverlappingTemplate
1	1	0	0	3	0	0	4	0	1	0.035174		9/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
3	0	0	0	1	0	0	4	0	2	0.017912		9/10	NonOverlappingTemplate
1	0	0	0	2	0	0	1	0	6	0.000199		10/10	NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10	* NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	3/10	* NonOverlappingTemplate
1	2	0	0	3	0	0	2	0	2	0.213309		9/10	NonOverlappingTemplate
1	1	0	0	4	0	0	1	0	3	0.035174		9/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
1	0	0	0	0	0	0	3	0	6	0.000040	*	10/10	NonOverlappingTemplate

	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate	
	0	0	0	0	1	0	0	2	0	7	0.000001	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	2	0	8	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	2	0	8	0.000000	*	10/10	NonOverlappingTemplate
1	0	0	0	2	0	0	5	0	2	0.004301		9/10	NonOverlappingTemplate	
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10	* NonOverlappingTemplate	
	0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	1	0	0	4	0	5	0.000199		10/10	NonOverlappingTemplate
2	1	0	0	3	0	0	3	0	1	0.122325		9/10	NonOverlappingTemplate	
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
3	2	0	0	3	0	0	1	0	1	0.122325		7/10	* NonOverlappingTemplate	
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	4	0	6	0.000003	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	2	0	0	3	0	5	0.000954		10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	3	0	7	0.000000	*	10/10	NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10	* NonOverlappingTemplate	
	0	0	0	0	0	0	0	2	0	8	0.000000	*	10/10	NonOverlappingTemplate
3	3	0	0	1	0	0	2	0	1	0.122325		7/10	* NonOverlappingTemplate	
2	0	0	0	1	0	0	2	0	5	0.004301		10/10	NonOverlappingTemplate	
6	2	0	0	0	0	0	1	0	1	0.000199		6/10	* NonOverlappingTemplate	
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate
	0	0	0	0	3	0	0	4	0	3	0.004301		10/10	NonOverlappingTemplate
	0	0	0	0	3	0	0	4	0	3	0.004301		10/10	NonOverlappingTemplate
	0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10	NonOverlappingTemplate

## XOR-ed Bits

RESULTS FOR THE UNIFORMITY OF P-VALUES AND THE PROPORTION OF PASSING SEQUENCES

generator is <data/bits\_16.txt>

C1	C2	C3	C4	C5	C6	C7	C8	C9	C10	P-VALUE	PROPORTION	STATISTICAL TEST	
7	2	0	1	0	0	0	0	0	0	0.000001	*	9/10	Frequency
3	1	3	1	1	0	1	0	0	0	0.213309		10/10	BlockFrequency
6	2	1	1	0	0	0	0	0	0	0.000199		8/10	CumulativeSums
7	1	1	0	0	1	0	0	0	0	0.000003	*	8/10	CumulativeSums
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10	* Runs
9	1	0	0	0	0	0	0	0	0	0.000000	*	4/10	* LongestRun
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10	* Rank
1	0	0	2	0	1	0	5	0	1	0.008879		10/10	FFT
10	0	0	0	0	0	0	0	0	0	0.000000	*	3/10	* NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10	* NonOverlappingTemplate
9	1	0	0	0	0	0	0	0	0	0.000000	*	3/10	* NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10	* NonOverlappingTemplate
0	2	0	0	3	0	0	3	0	2	0.066882		10/10	NonOverlappingTemplate
8	1	0	0	1	0	0	0	0	0	0.000000	*	3/10	* NonOverlappingTemplate
2	1	0	0	1	0	0	4	0	2	0.066882		9/10	NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10	* NonOverlappingTemplate
2	0	0	0	2	0	0	6	0	0	0.000089	*	9/10	NonOverlappingTemplate
2	0	0	0	3	0	0	2	0	3	0.066882		10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	4	0	6	0.000003	*	10/10	NonOverlappingTemplate
7	2	0	0	0	0	0	0	0	1	0.000001	*	3/10	* NonOverlappingTemplate
0	0	0	0	2	0	0	6	0	2	0.000089	*	10/10	NonOverlappingTemplate
1	3	0	0	2	0	0	3	0	1	0.122325		9/10	NonOverlappingTemplate
0	3	0	0	1	0	0	3	0	3	0.035174		10/10	NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10	* NonOverlappingTemplate
2	2	0	0	2	0	0	4	0	0	0.035174		10/10	NonOverlappingTemplate
1	0	0	0	0	0	0	2	0	7	0.000001	*	10/10	NonOverlappingTemplate
1	2	0	0	2	0	0	3	0	2	0.213309		10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	4	0	6	0.000003	*	10/10	NonOverlappingTemplate
0	0	0	0	1	0	0	3	0	6	0.000040	*	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10	NonOverlappingTemplate
4	3	0	0	3	0	0	0	0	0	0.004301		7/10	* NonOverlappingTemplate
0	0	0	0	2	0	0	5	0	3	0.000954		10/10	NonOverlappingTemplate
0	0	0	0	1	0	0	1	0	8	0.000000	*	10/10	NonOverlappingTemplate
0	1	0	0	3	0	0	4	0	2	0.017912		10/10	NonOverlappingTemplate
2	2	0	0	3	0	0	2	0	1	0.213309		8/10	NonOverlappingTemplate
0	2	0	0	2	0	0	3	0	3	0.066882		10/10	NonOverlappingTemplate
7	1	0	0	2	0	0	0	0	0	0.000001	*	5/10	* NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	0/10	* NonOverlappingTemplate
5	1	0	0	4	0	0	0	0	0	0.000199		5/10	* NonOverlappingTemplate

0	0	0	0	3	0	0	2	0	5	0.000954	10/10	NonOverlappingTemplate
5	0	0	0	1	0	0	3	0	1	0.002043	7/10	* NonOverlappingTemplate
0	0	0	0	1	0	0	2	0	7	0.000001	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
1	0	0	0	0	0	0	6	0	3	0.000040	*	10/10 NonOverlappingTemplate
0	0	0	0	1	0	0	3	0	6	0.000040	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	5	0	5	0.000008	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
1	0	0	0	3	0	0	2	0	4	0.017912	10/10	NonOverlappingTemplate
4	0	0	0	1	0	0	5	0	0	0.000199	8/10	NonOverlappingTemplate
0	0	0	0	0	0	0	4	0	6	0.000003	*	10/10 NonOverlappingTemplate
0	0	0	0	1	0	0	5	0	4	0.000199	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	2	0	8	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	2	0	8	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	5	0	5	0.000008	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	4	0	6	0.000003	*	10/10 NonOverlappingTemplate
0	0	0	0	1	0	0	0	0	9	0.000000	*	10/10 NonOverlappingTemplate
3	0	0	0	5	0	0	0	0	2	0.000954	9/10	NonOverlappingTemplate
3	4	0	0	1	0	0	2	0	0	0.017912	8/10	NonOverlappingTemplate
7	2	0	0	0	0	0	0	0	1	0.000001	*	3/10 * NonOverlappingTemplate
6	2	0	0	1	0	0	0	0	1	0.000199	4/10	* NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000	*	1/10 * NonOverlappingTemplate
2	1	0	0	2	0	0	3	0	2	0.213309	8/10	NonOverlappingTemplate
5	3	0	0	1	0	0	1	0	0	0.002043	8/10	NonOverlappingTemplate
0	0	0	0	0	0	0	3	0	7	0.000000	*	10/10 NonOverlappingTemplate
3	0	0	0	2	0	0	1	0	4	0.017912	9/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000	*	10/10 NonOverlappingTemplate
2	1	0	0	0	0	0	5	0	2	0.004301	10/10	NonOverlappingTemplate
0	0	0	0	2	0	0	3	0	5	0.000954	10/10	NonOverlappingTemplate
0	0	0	0	2	0	0	2	0	6	0.000089	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	2	0	8	0.000000	*	10/10 NonOverlappingTemplate
0	2	0	0	0	0	0	3	0	5	0.000954	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	2	0	8	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	1	0	0	4	0	5	0.000199	10/10	NonOverlappingTemplate
1	1	0	0	2	0	0	5	0	1	0.008879	9/10	NonOverlappingTemplate
5	0	0	0	2	0	0	3	0	0	0.000954	7/10	* NonOverlappingTemplate
0	0	0	0	2	0	0	4	0	4	0.002043	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	2	0	8	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	3	0	7	0.000000	*	10/10 NonOverlappingTemplate
0	0	0	0	0	0	0	1	0	9	0.000000	*	10/10 NonOverlappingTemplate
0	1	0	0	3	0	0	4	0	2	0.017912	10/10	NonOverlappingTemplate
9	1	0	0	0	0	0	0	0	0	0.000000	*	3/10 * NonOverlappingTemplate
3	0	0	0	4	0	0	1	0	2	0.017912	8/10	NonOverlappingTemplate
3	2	0	0	2	0	0	2	0	1	0.213309	7/10	* NonOverlappingTemplate
0	1	0	0	0	0	0	4	0	5	0.000199	10/10	NonOverlappingTemplate
1	0	0	0	2	0	0	5	0	2	0.004301	10/10	NonOverlappingTemplate

2	1	0	0	4	0	0	1	0	2	0.066882	9/10	NonOverlappingTemplate
2	1	0	0	4	0	0	2	0	1	0.066882	9/10	NonOverlappingTemplate
0	0	0	0	1	0	0	1	0	8	0.000000 *	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	1	0	9	0.000000 *	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	1	0	9	0.000000 *	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	3	0	7	0.000000 *	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000 *	10/10	NonOverlappingTemplate
0	0	0	0	1	0	0	5	0	4	0.000199	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	2	0	8	0.000000 *	10/10	NonOverlappingTemplate
8	1	0	0	1	0	0	0	0	0	0.000000 *	4/10	* NonOverlappingTemplate
0	1	0	0	0	0	0	1	0	8	0.000000 *	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	5	0	5	0.000008 *	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	1	0	9	0.000000 *	10/10	NonOverlappingTemplate
5	1	0	0	2	0	0	2	0	0	0.004301	5/10	* NonOverlappingTemplate
0	0	0	0	0	0	0	4	0	6	0.000003 *	10/10	NonOverlappingTemplate
2	0	0	0	2	0	0	5	0	1	0.004301	10/10	NonOverlappingTemplate
0	0	0	0	1	0	0	4	0	5	0.000199	10/10	NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000 *	0/10	* NonOverlappingTemplate
3	1	0	0	4	0	0	2	0	0	0.017912	8/10	NonOverlappingTemplate
3	1	0	0	2	0	0	3	0	1	0.122325	8/10	NonOverlappingTemplate
4	1	0	0	2	0	0	2	0	1	0.066882	7/10	* NonOverlappingTemplate
0	0	0	0	1	0	0	3	0	6	0.000040 *	10/10	NonOverlappingTemplate
7	1	0	0	2	0	0	0	0	0	0.000001 *	4/10	* NonOverlappingTemplate
0	0	0	0	0	0	0	3	0	7	0.000000 *	10/10	NonOverlappingTemplate
0	1	0	0	1	0	0	3	0	5	0.002043	10/10	NonOverlappingTemplate
1	0	0	0	2	0	0	5	0	2	0.004301	9/10	NonOverlappingTemplate
0	0	0	0	0	0	0	0	0	10	0.000000 *	10/10	NonOverlappingTemplate
6	1	0	0	2	0	0	1	0	0	0.000199	4/10	* NonOverlappingTemplate
1	0	0	0	1	0	0	6	0	2	0.000199	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	2	0	8	0.000000 *	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	5	0	5	0.000008 *	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	1	0	9	0.000000 *	10/10	NonOverlappingTemplate
0	0	0	0	1	0	0	4	0	5	0.000199	10/10	NonOverlappingTemplate
7	0	0	0	2	0	0	1	0	0	0.000001 *	6/10	* NonOverlappingTemplate
0	0	0	0	1	0	0	1	0	8	0.000000 *	10/10	NonOverlappingTemplate
0	0	0	0	1	0	0	3	0	6	0.000040 *	10/10	NonOverlappingTemplate
1	1	0	0	2	0	0	2	0	4	0.066882	9/10	NonOverlappingTemplate
0	0	0	0	0	0	0	1	0	9	0.000000 *	10/10	NonOverlappingTemplate
0	0	0	0	0	0	0	4	0	6	0.000003 *	10/10	NonOverlappingTemplate
10	0	0	0	0	0	0	0	0	0	0.000000 *	0/10	* NonOverlappingTemplate
2	1	0	0	2	0	0	2	0	3	0.213309	8/10	NonOverlappingTemplate
2	0	0	0	4	0	0	4	0	0	0.002043	9/10	NonOverlappingTemplate
0	0	0	0	2	0	0	3	0	5	0.000954	10/10	NonOverlappingTemplate
8	1	0	0	1	0	0	0	0	0	0.000000 *	2/10	* NonOverlappingTemplate
0	0	0	0	2	0	0	4	0	4	0.002043	10/10	NonOverlappingTemplate
1	0	0	0	2	0	0	3	0	4	0.017912	9/10	NonOverlappingTemplate
9	0	0	0	1	0	0	0	0	0	0.000000 *	1/10	* NonOverlappingTemplate
2	0	0	0	1	0	0	2	0	5	0.004301	8/10	NonOverlappingTemplate

The generated random number bits were tested to check if they pass NIST TRN criteria. Frequency,BlockFrequency,CumulativeSums,Runs,LongestRun,Rank,FFT,NonOverlappingTemplate The score is out of 10 and lesser the score lesser random the bits are.For the latches Latch-1 has 8/10 only for one test and every other test is 0/10. Latch-2 has 6/10 only for one test and every other test is 0/10. Latch-3 has 10/10 for one test and scored 2,1,2,2 and two other tests scored 0/10 Whereas,the XOR ed bits has only two 0/10 and other test are 9,10,8,8,4. This confirms that XOR-ing the outputs of latches makes the bits more random. If the number of clock cycles for which the latch is transparent is increased,then the throughput decreases, but the entropy increases and randomness increases.

## References

- R. Della Sala, D. Bellizia and G. Scotti, "A Novel Ultra-Compact FPGA-Compatible TRNG Architecture Exploiting Latched Ring Oscillators," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 3, pp. 1672-1676, March 2022, doi: 10.1109/TC-SII.2021.3121537.
- <https://github.com/terrillmoore/NIST-Statistical-Test-Suite.git>
- <https://nvlpubs.nist.gov/nistpubs/legacy/sp/nistspecialpublication800-22r1a.pdf>