

Table 1

	ALUSrc	ALUOP	RegDst	MemWrite	MemRead
RT	0	010	0	0	0
Addi	1	011	1	0	0
Lw	1	000	1	0	1
Sw	1	000	0	1	0
beq	0	001	0	0	0
bne	0	001	0	0	0
j	0	0	0	0	0
jal	0	0	0	0	0
Jr	0	0	0	0	0

Table 1-1

	MemToReg	RegWrite	Branch	Jal	Jal_write
RT	0	1	0	0	0
Addi	0	1	0	0	0
Lw	1	1	0	0	0
Sw	0	0	0	0	0
beq	0	0	1	0	0
bne	0	0	1	0	0
j	0	0	0	0	0
jal	0	1	0	1	1
Jr	0	1	0	0	0