

Borna Tavassoli CA#6

ModelSim - INTEL FPGA STARTER EDITION 2020.1

File Edit View Compile Simulate Add Source Tools Layout Bookmarks Window Help

Layout Simulate

ColumnLayout Default

Search:

sim - Default

Design unit Design u

cosx_tb cosx_tb Module

my_circuit cosx Module

control controller Module

datapath dp Module

cnt cnt4bit Module

final_ro... rom_with_al Module

mux mux10bit Module

mult1 mult Module

mult2 mult Module

regx2 register10bit Module

rtemp register10bit Module

rres register10bit Module

add adder Module

cmp cmp10bit Module

#ASSIGN#... cosx Process

#ASSIGN#... cosx Process

#ALWAYS#22 cosx_tb Process

#INITIAL#23 cosx_tb Process

std std VIPackag

#sim_capacity# Capacity

Objects

Name Type (filtered) St

clk 0 Reg... Internal

rst 0 Reg... Internal

start 0 Reg... Internal

x 0100... Pack... Internal

y 0000... Pack... Internal

done S10 Net Internal

result 0100... Net Internal

ps 100 Net Internal

co S10 Net Internal

is_negg S10 Net Internal

Processes (Active)

Name Type (filtered) St

#INITIAL#23 Initial Ac

Ln#

50

51

52

53

54

55

56

57

58

59

60

61

62

63

64

65

66

67

68

69

70

71

72

endif

tril clock;

ifndef ALTERA_RESERVED_QIS

// synopsys translate_on

endif

wire [7:0] sub_wire0;

wire [7:0] q = sub_wire0[7:0];

altsyncram altsyncram_component (

.address_a (address),

.clock0 (clock),

.q_a (sub_wire0),

.aclr0 (1'b0),

.aclr1 (1'b0),

.address_b (1'b1),

.addressstall_a (1'b0),

.addressstall_b (1'b0),

.byteena_a (1'b1),

.byteena_b (1'b1),

.clock1 (1'b1),

.clocken0 (1'b1),

.clocken1 (1'b1),

Wave

datapath.v rom_with_al.v cosx.v

Transcript

Note: Setop : D:/CA6 - MODELSIM/cosx.v(27)

Time: 11002 ns Iteration: 0 Instance: /cosx_tb

Break in Module cosx_tb at D:/CA6 - MODELSIM/cosx.v line 27

V\$IM 17>

Ln: 40 Col: 10 Project: CA6 Now: 11,002 ns Delta: 0 sim/cosx_tb/#INITIAL#23

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ENG 10:21 PM 1/11/2021

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x 0100... Pack... Internal

y 0000... Pack... Internal

done S10 Net Internal

result 0100... Net Internal

ps 100 Net Internal

co S10 Net Internal

is_negg S10 Net Internal

Processes (Active)

Name Type (filtered) St

#INITIAL#23 Initial Ac

Wave - Default

Msgs

/cosx_tb/clk 0

/cosx_tb/rst 0

/cosx_tb/start 0

/cosx_tb/x 0100001100

/cosx_tb/y 00000000

/cosx_tb/done S10

/cosx_tb/result 0100000000

/cosx_tb/ps 100

/cosx_tb/co S10

/cosx_tb/is_negg S10

/cosx_tb/my_circuit... 0000

/cosx_tb/my_circuit... 10000000

Now 11002000 ps

Cursor 1 559952 ps

1200000 ps 1600000 ps

Transcript

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Time: 11002 ns Iteration: 0 Instance: /cosx_tb

Break in Module cosx_tb at D:/CA6 - MODELSIM/cosx.v line 27

V\$IM 17>

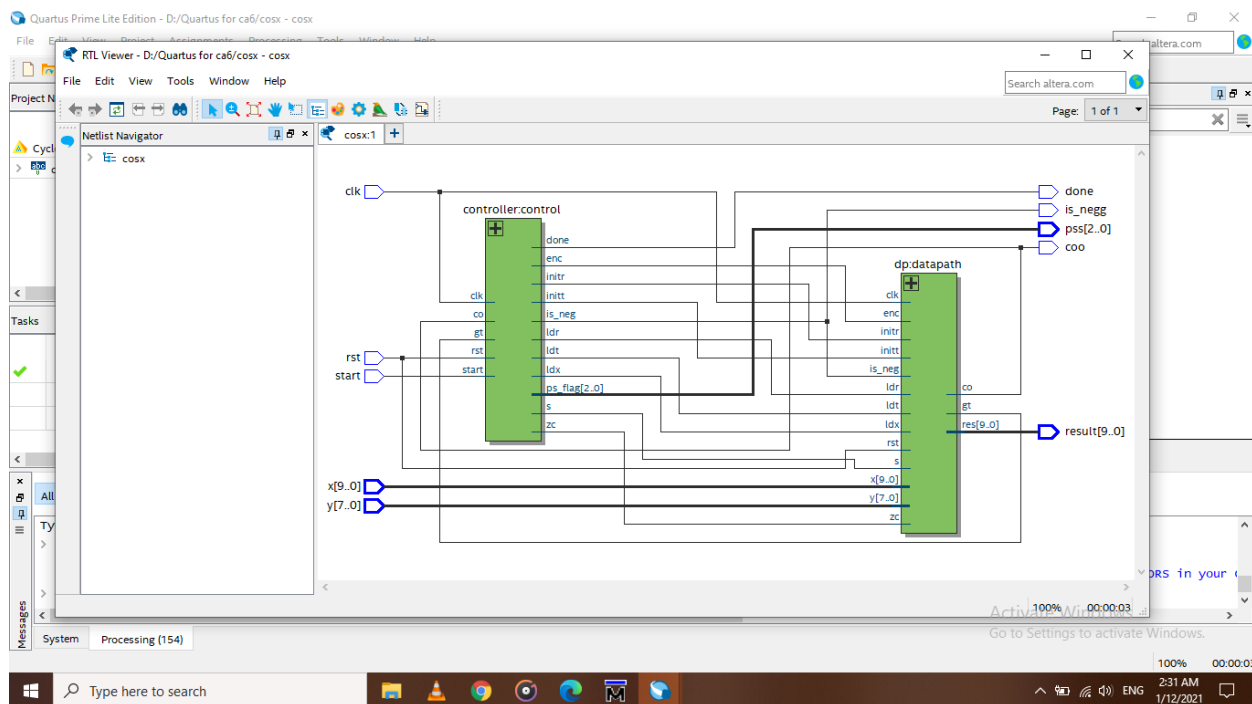
936851 ps to 1960851 ps Project: CA6 Now: 11,002 ns Delta: 0 sim/cosx_tb/#INITIAL#23

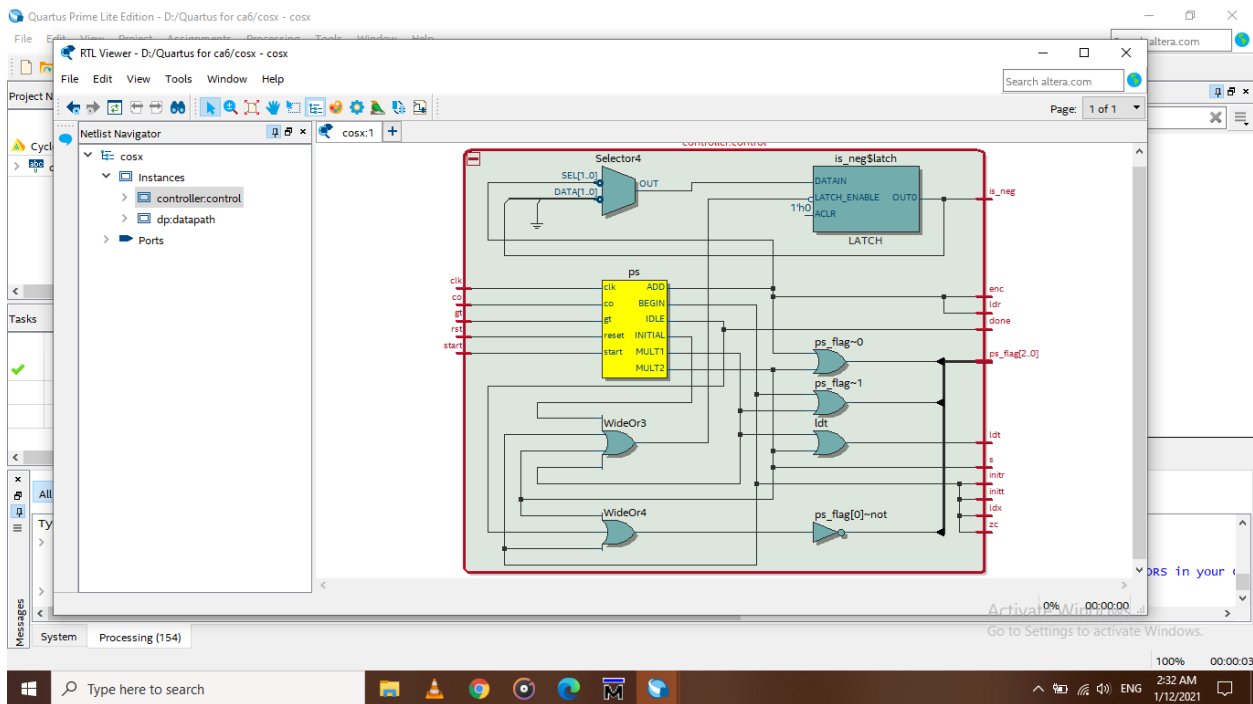
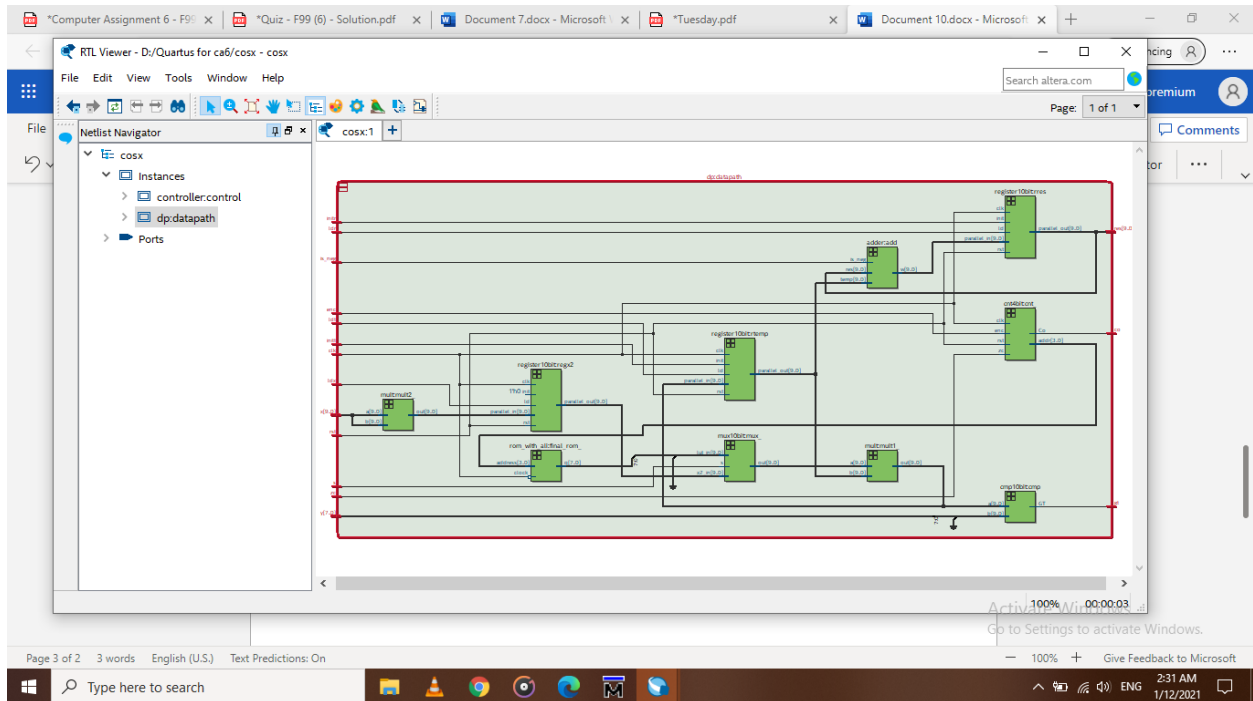
Type here to search

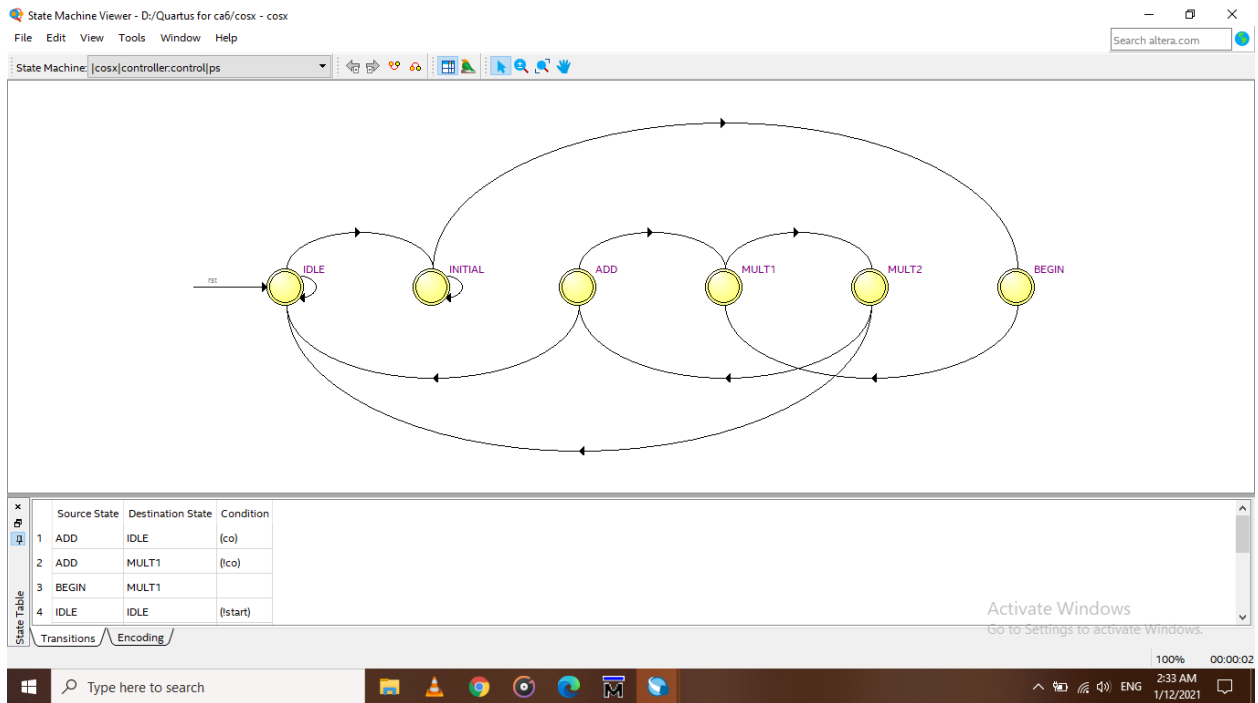
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Quartus Prime Lite Edition - D:/Quartus for ca6/cosx - cosx

File Edit View Project Assignments Processing Tools Window Help

Project Navigator

Entity: Instance

Cyclone IV E: EP4CE6E22A7

cosx

Compilation Report - cosx

Table of Contents

- Flow Summary
- Flow Settings
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- Flow Elapsed Time
- Flow OS Summary
- Flow Log
- Analysis & Synthesis
- Filter
- Assembler
- Timing Analyzer
- EDA Netlist Writer
- Flow Messages
- Flow Suppressed Messages

Flow Summary

Flow Status: Successful

Quartus Prime Version: 20.1.0 Build

Revision Name: cosx

Top-level Entity Name: cosx

Family: Cyclone IV E

Device: EP4CE6E22A7

Timing Models: Final

Total logic elements: 449 / 6,272

Total registers: 40

Total pins: 37 / 92 (40%)

Total virtual pins: 0

Total memory bits: 128 / 276,480

Embedded Multiplier 9-bit elements: 0 / 30 (0%)

Total PLLs: 0 / 2 (0%)

IP Catalog

Installed IP

Project Directory

No Selection Available

Library

- Basic Functions
- DSP
- Interface Protocols
- Processors and Peripherals
- University Program

Search for Partner IP

Tasks

Compilation

Task	Time
Compile Design	00:00:35
Analysis & Synthesis	00:00:15
Fitter (Place & Route)	00:00:11
Assembler (Generate programming files)	00:00:02

Messages

System Processing (159)

Running Quartus Prime Netlist Viewers Preprocess

Command: quartus_npp cosx -c cosx --netlist_type=sm_process

18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your project.

Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 1 warning

100% 00:00:02

Activate Windows
Go to Settings to activate Windows.

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