Experiment #4 – Integrated System

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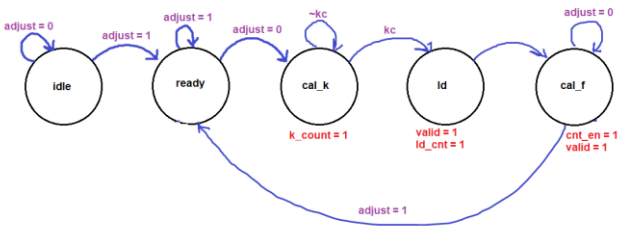
I. Introduction

In this lab, we try to build an integrated system. So, first we need to build a frequency multiplier and then we will build the main accelerator and connect the two modules using handshaking.

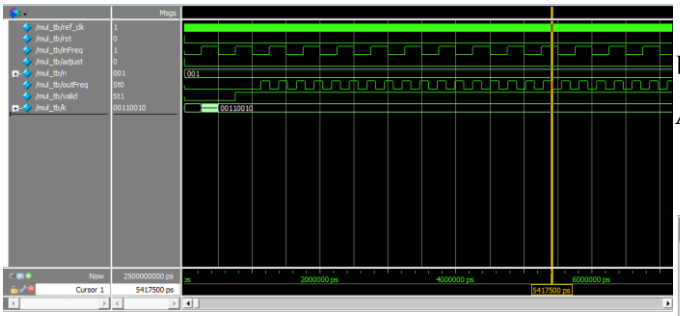
II. Frequency Multiplier

First we design the controller (state machine) the we write the Verilog code and test it's accuracy with the following samples.

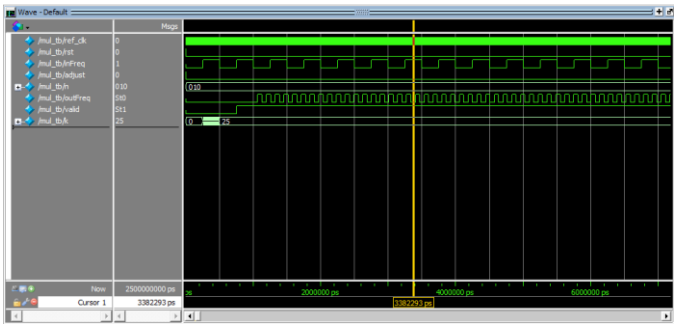
A. Modelsim Implementation



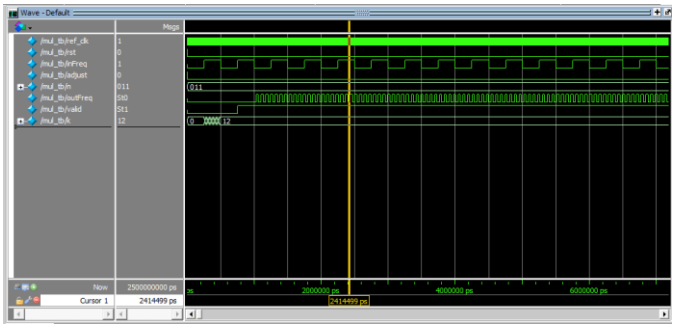
State Diagram



Sample 1: n = 1 & F_ref/F_in = 100, so k = 50.



Sample 2: n = 2 & F_ref/F_in = 100, so k = 25.



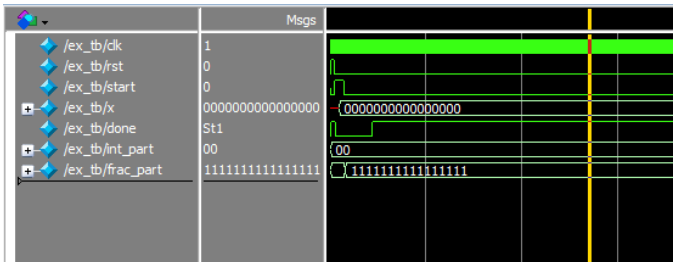
Sample3: n = 3 & F_ref/F_in = 100, so k = 12.

III. Exponential Accelerator

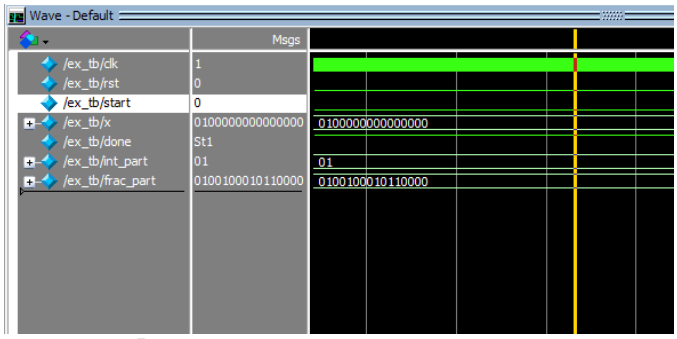
In this part, we design the frequency divider of lab1 to build a Frequency Selector and add it to the rest of the circuit.

A. Exponential Engine

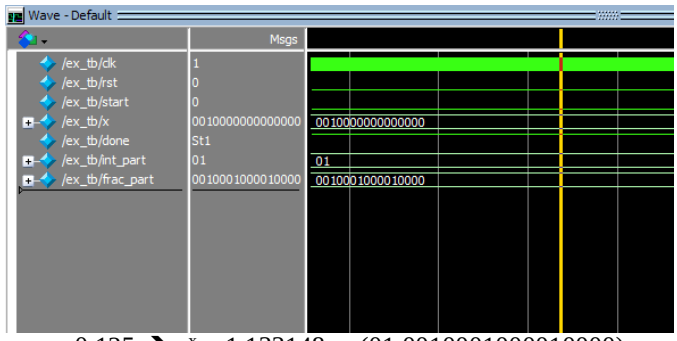
Below is the outputs to measure the accuracy.



$x = 0 \rightarrow e^x = 1 \approx (00.1111111111111111)_2$

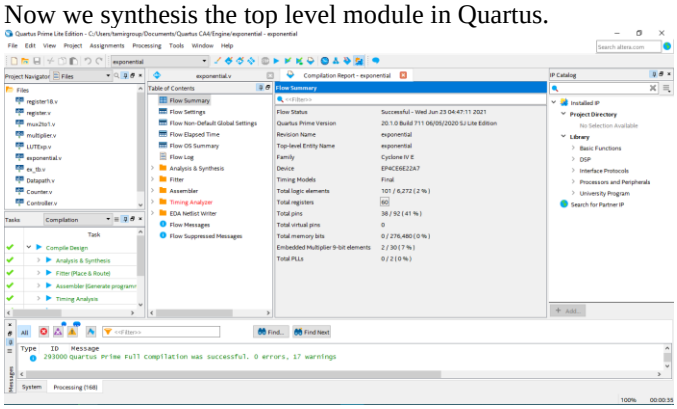


$x = 0.25 \rightarrow e^x \approx 1.284025 \approx (01.0100100010110000)_2$

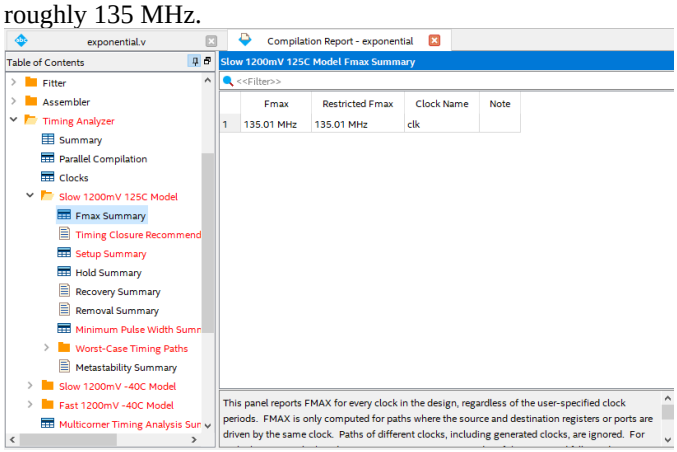


$x = 0.125 \rightarrow e^x \approx 1.133148 \approx (01.0010001000010000)_2$

Now we synthesis the top level module in Quartus.



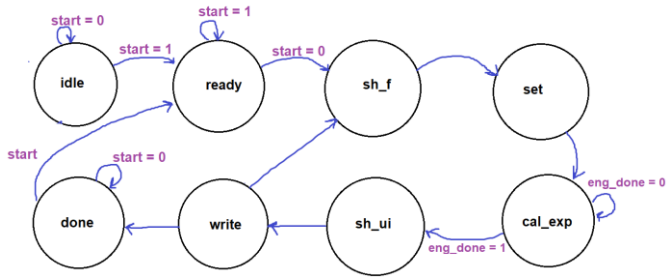
As it is shown below, the Max Frequency for this module is roughly 135 MHz.



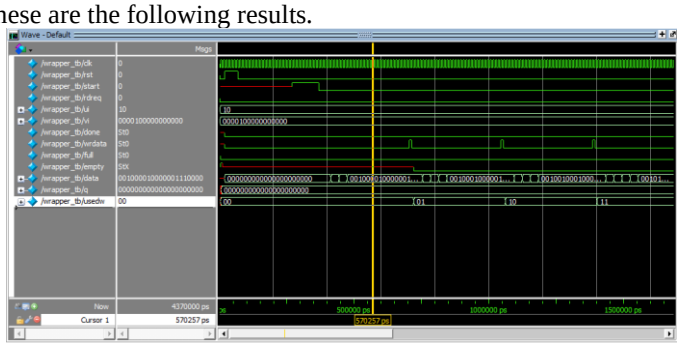
B.

B. Exponential Accelerator Wrapper

First we draw the controller.

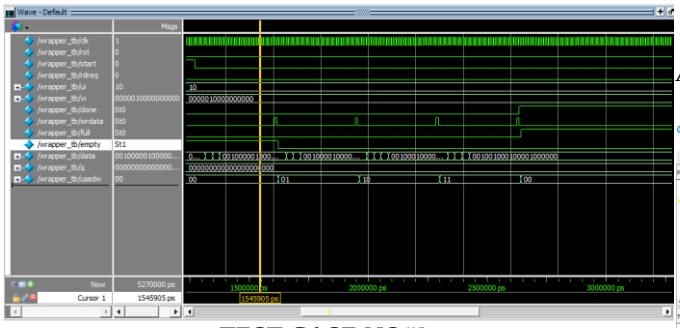


Then we synthesis the top level module and add a FIFO memory. After that we write a test bench to test our circuit. These are the following results.



TEST CASE NO#1

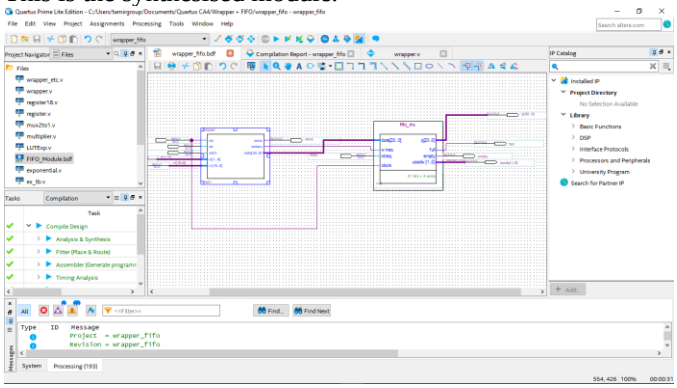
	UI	VI	N = 1
EXPECTED	10	000010…	2.063486815
REALITY	10	000010…	00100001000000001110000
	UI	VI	N = 2
EXPECTED	10	000010…	2.12898891784
REALITY	10	000010…	00100010000011111110000
	UI	VI	N = 3
EXPECTED	10	000010…	2.26629690613
REALITY	10	000010…	00100100010000010000000
	UI	VI	N = 4
EXPECTED	10	000010…	2.56805083338
REALITY	10	000010…	00101000111111110000



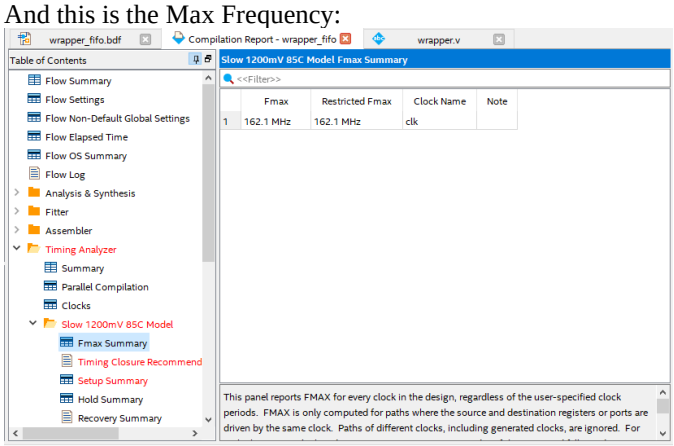
TEST CASE NO#2

	UI	VI	N = 1
EXPECTED	10	0000010…	2.03149541717
REALITY	10	0000010…	00100000100000010000
	UI	VI	N = 2
EXPECTED	10	0000010…	2.063486815
REALITY	10	0000010…	00100001000000111000
	UI	VI	N = 3
EXPECTED	10	0000010…	2.12898891784
REALITY	10	0000010…	00100010000011111000
	UI	VI	N = 4
EXPECTED	10	0000010…	2.26629690613
REALITY	10	0000010…	00100100010000100000

This is the synthesised module.



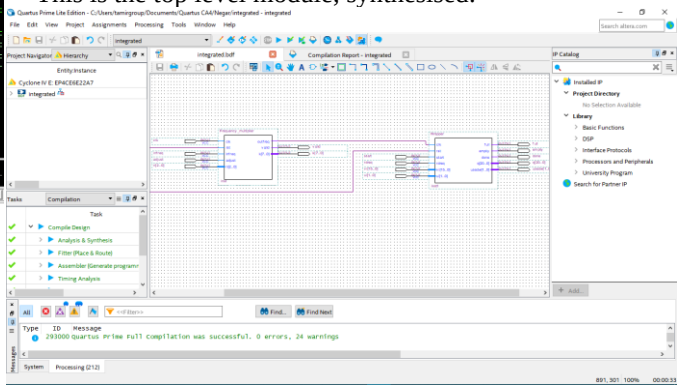
And this is the Max Frequency:



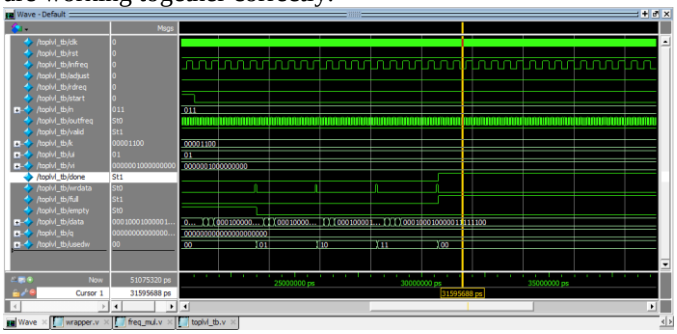
IV. Integrated Circuit

A. Design and Synthesis

This is the top level module, synthesised.

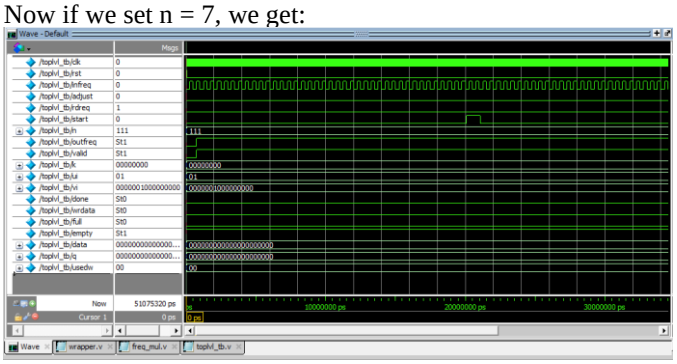


We test the module to see if frequency multiplier and wrapper are working together correctly.



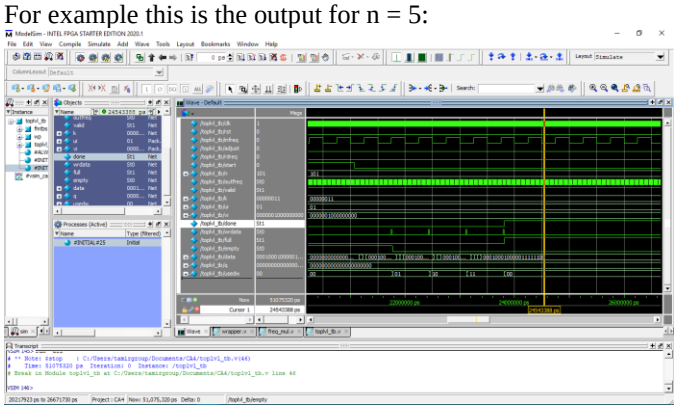
As it is shown, inFreq is working properly and the stack is getting full too.
Now to calculate the maximum n:
F = 2MHz ➔ $2 * 2^n < 162$ ➔ n <= 6

Now if we set n = 7, we get:



As one can see, outFreq is not changing!
So, the maximum value for our stack is 6 words.

For example this is the output for n = 5:



V. Conclusions

In this Lab, we learned to work with frequency multipliers.

Got the chance to work with wrappers and learned about handshaking and finally implemented an integrated circuit.