CA #4

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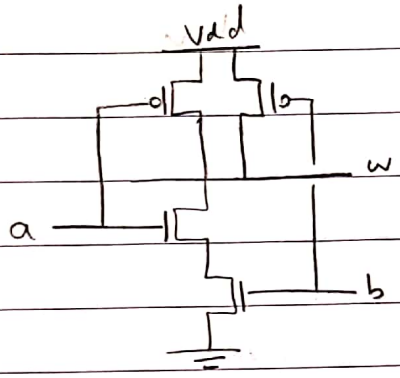
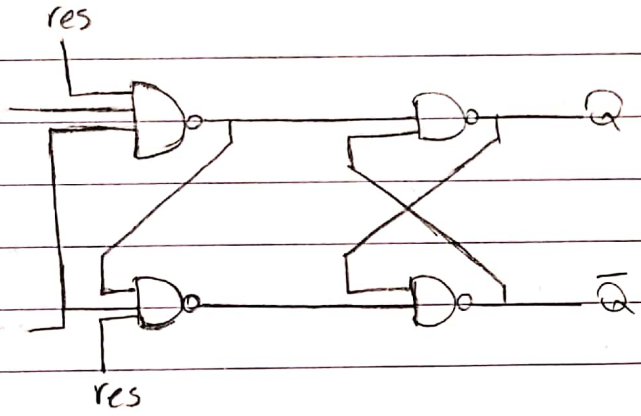
NAND GATE pMOS : 6NS
nMOS : 4NS
→ NAND delay : 8NS

2

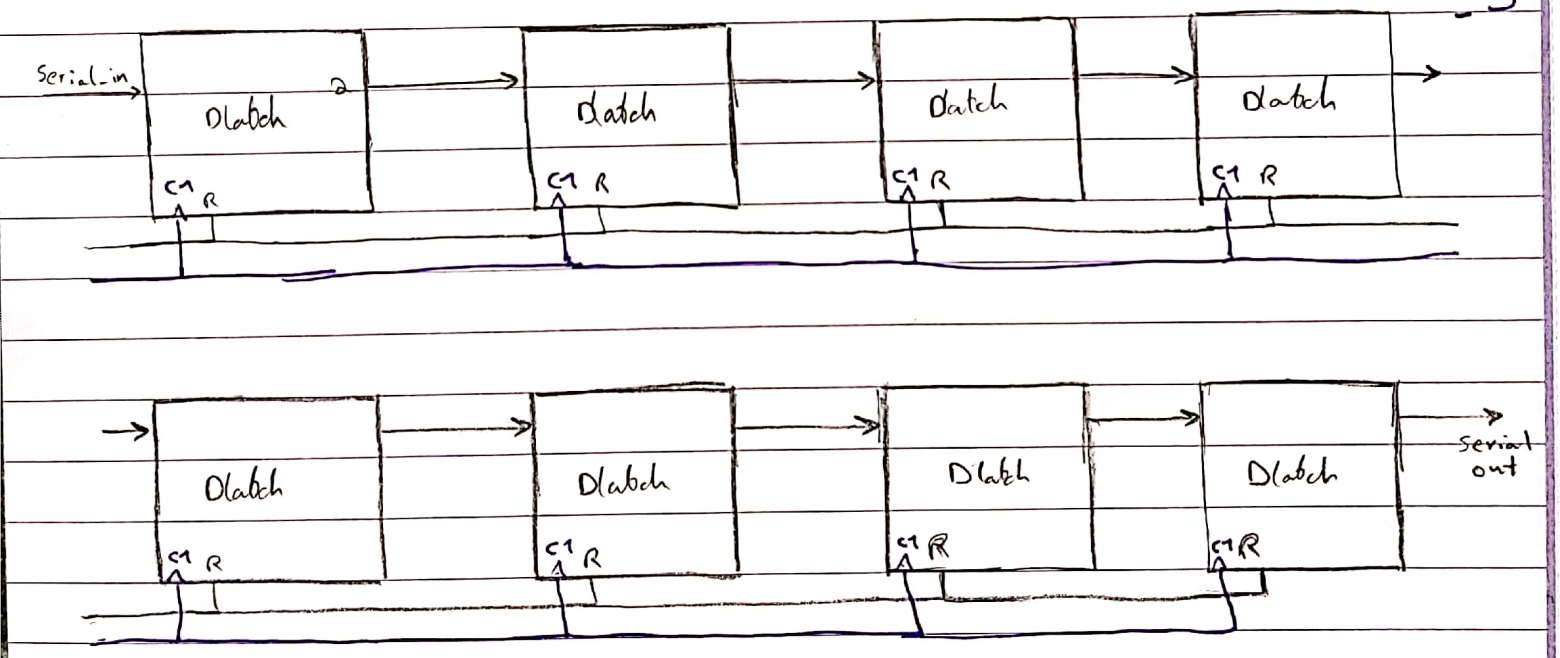


4

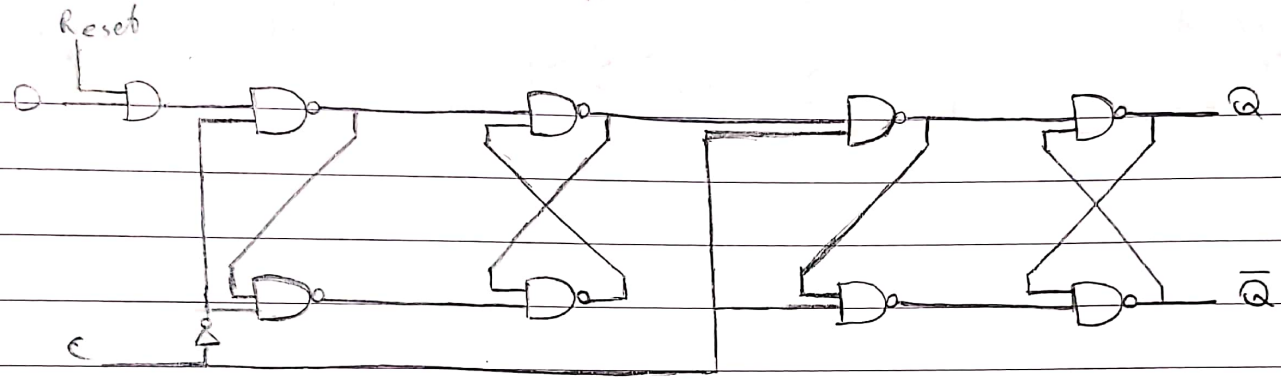


active low asynchronous Reset

5



when clock = 1, all D latches are connected to eachother (transparency) therefore input Sin will iterate through the 8 bits and if clock is equal to 1 long enough, all 8 bits will be equal to Sin! → Does NOT work as expected !!



-7

✓ #14 ns (NAND + NOT) AND delay

✓ basically the same circuit as 5, only now with Flip Flops -8

Differences : in always structure we don't face any glitches. -10

Always structure delay is way more than gate level delay

→ Always delay = worst case delay