

Report	Borna Towasseli 810198374	Bulan	rubble 1 921
Subject: \ :e16Q		Date:	Subject
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"ei		-	
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NOR		-	
porth deading	adjust: that is the	6 us delays	C /I
Delays -> 1	NOT Sto1:5 NANG	5to1. 10	
(to1: 10	shotto 0:7, son	to 05:8	Harringh
NOR)			
1.4 Hojo: 14	of second approx and	1:12 both	i) durable
Module 1. Jelan S	Francis allening blog	19 NS ch	of an
ne poblis will 18	de don wite that the	0.0:12	1 SQ 1
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91= k1= 190)	la not carry ? unla	that thea	not co
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- strongily day live	tox level worver, one w	marked Trans	Pointer
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of John John la	Cort chove, 12th less	all language	

6	Assignment #1 Barna Takes li Dr. Newslift
T	Subject: Date: / /2002
	NOTES:
	NOTE that module delays highly depend
	on the circuit's implementation and can vary from 12 or 14 to 24,26 or much higher! we have shown ddays that belong to the most efficient circuit.
	Show days that before to the most efficient circuit.
	The path with the most delay can have 2
	#26 ns delays atmost; that is the path iterating
	through XOR and NOR (e1) gates, which is also
	highlighted in orange in the previous page. note that
	no two 12 ns delays can ever occur, in the same path. please note that the paths with 18
	and 22 ns delays are also shown in the program.
	and 22 ns délays are also shown in the program.
	if we look dosely at the Gatelevel waves, are 4
	notice that they do not carry Z values! in other of words, despite facing a lot of Z values when
	examining Transistor level waves, one will not discover
	such nature in Gatelevel waves.
	Veep in mind the fact above, Gate level delays tend to
100	Both outputs are equal encept when Transistor level awares are Zvalu
	Both outputs are equal encept when Transistor level aboves are Ivalu