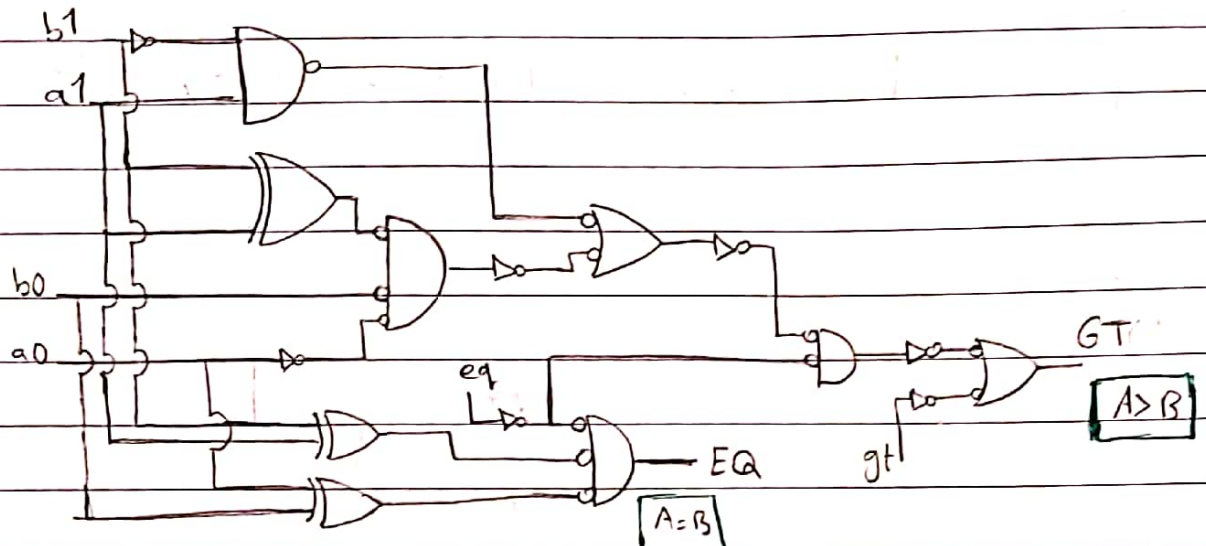


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Q1.3:



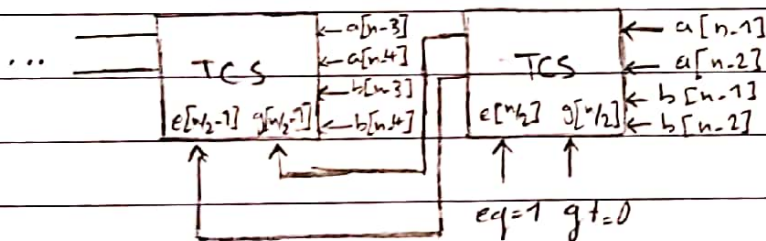
NOT $\begin{cases} t_{01}: 5 \\ t_{00}: 7 \end{cases}$

3input NOR $\begin{cases} t_{01}: 15 \\ t_{00}: 21 \end{cases}$

2input NAND $\begin{cases} t_{01}: 10 \\ t_{00}: 8 \end{cases}$

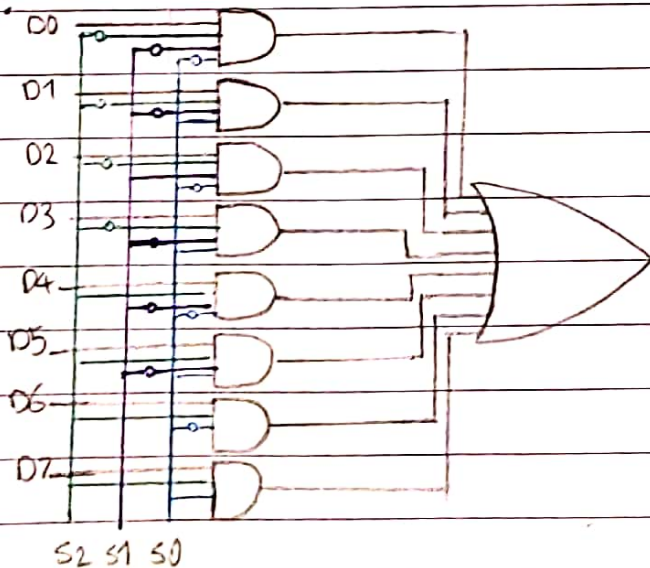
GT delay $\approx 6 + 9 = 15$ EQ delay $\approx 6 + 18 = 24$ \rightarrow Total delay ≈ 20 ns

NCS:



✓ we chose the path with the most bit shifts for the worst case delay.

Q4.6:



✓ Note that the little circles \rightarrow represent NOT gates \rightarrow

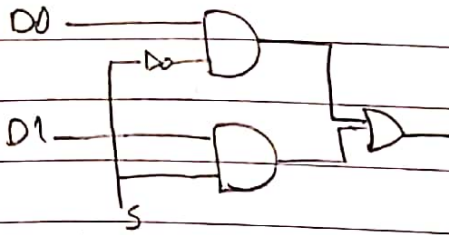
worst case delay = $7 + 20 + 40 = 67$
 $\downarrow \quad \downarrow \quad \downarrow$
 NOT AND OR

s.a.m

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worst case delay = 7 + 10 + 10 = 27
↓ ↓ ↓
NOT AND OR

A1A0 \ B1B0	00	01	11	10
00	0	0	1	1
01	0	1	0	1
11	1	0	1	0
10	1	1	0	0

$C_i = 0$ / s1

A1A0 \ B1B0	00	01	11	10
00	0	1	1	0
01	1	0	0	1
11	1	0	0	1
10	0	1	1	0

$C_i = 0$ / s0

A1A0 \ B1B0	00	01	11	10
00	0	0	0	0
01	0	0	1	0
11	0	1	1	1
10	0	0	1	1

$C_i = 0$ / c0

A1A0 \ B1B0	00	01	11	10
00	0	1	0	1
01	1	1	0	0
11	0	0	1	1
10	1	0	1	0

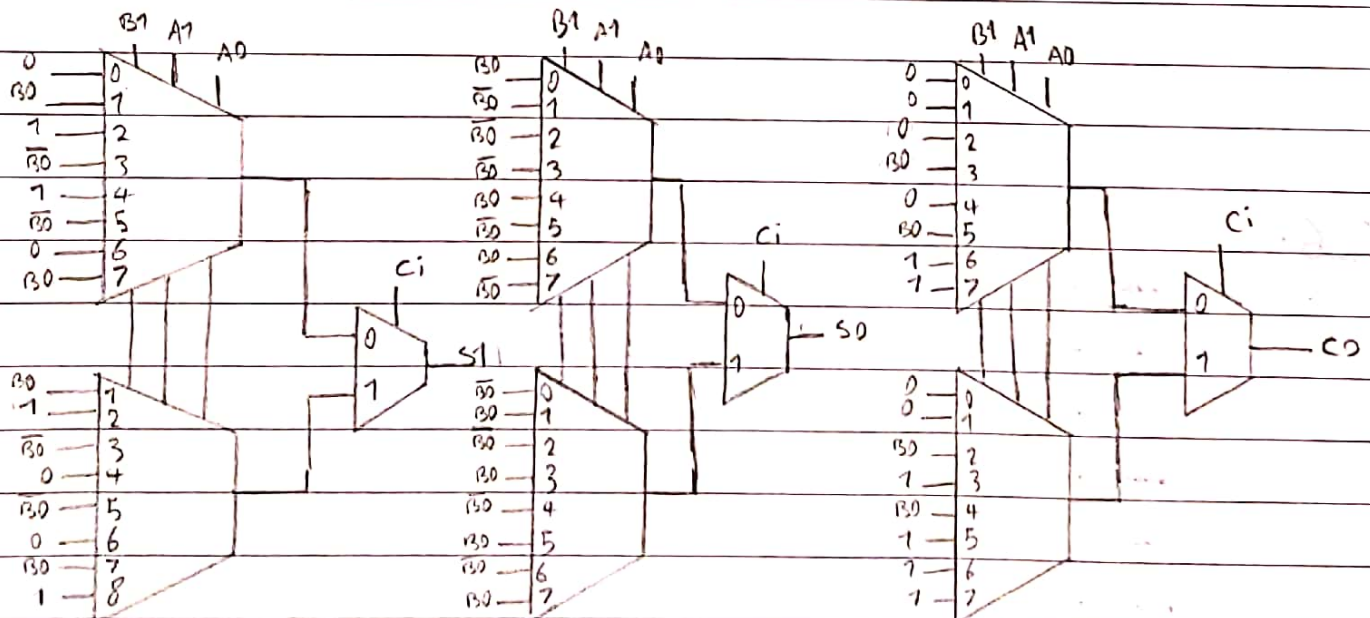
$C_i = 1$ / s1

A1A0 \ B1B0	00	01	11	10
00	1	0	0	1
01	0	1	1	0
11	0	1	1	0
10	1	0	0	1

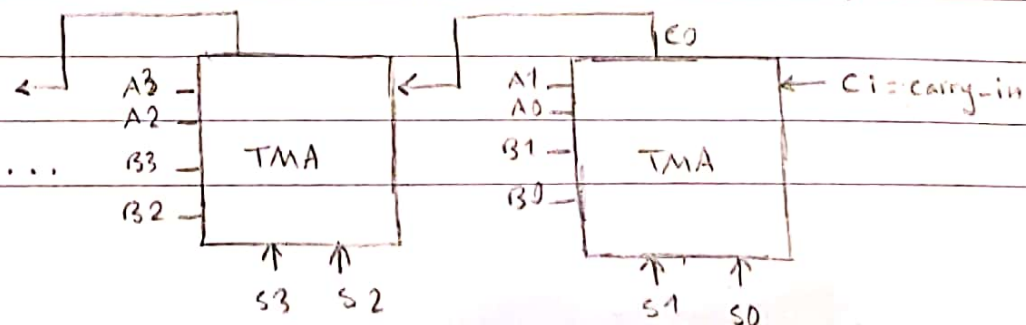
$C_i = 1$ / s0

A1A0 \ B1B0	00	01	11	10
00	0	0	1	0
01	0	0	1	1
11	1	1	1	1
10	0	1	1	1

$C_i = 1$ / c0

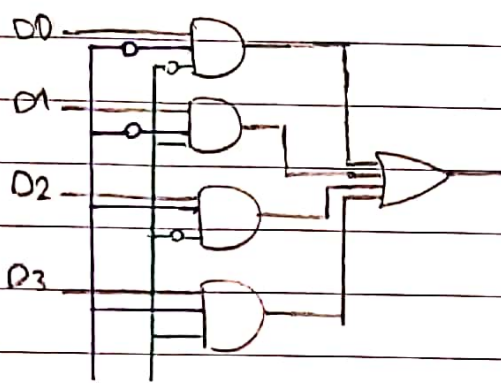


NMA:



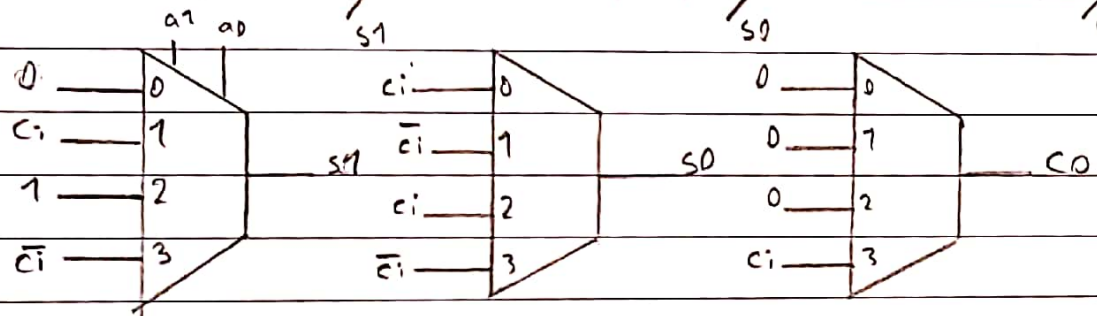
s.a.m

Q7-9:

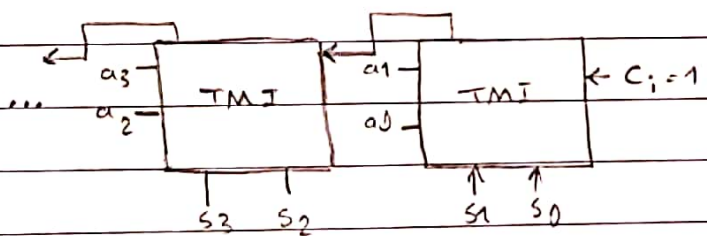


✓ Note that the little circles represent NOT gates

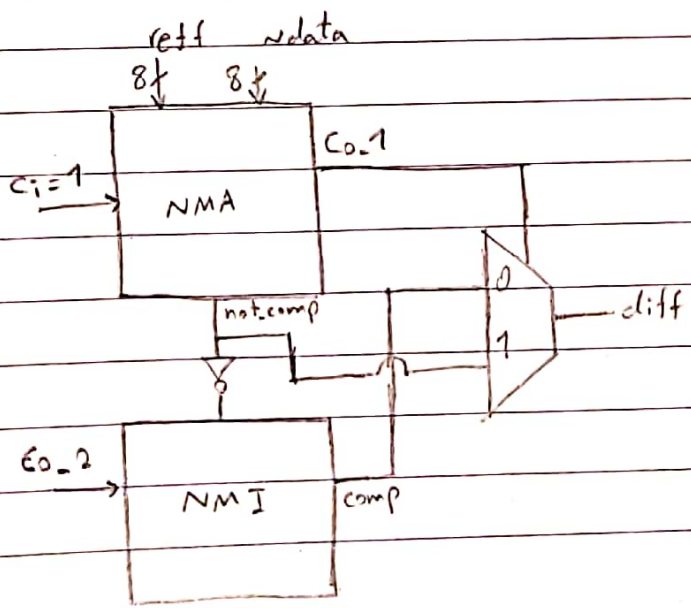
A_1A_0	C_i	00	01	11	10	S_1	S_0
0	0	0	0	1	1	0	0
1	0	0	1	0	1	0	0
0	1	0	0	1	0	1	1
1	1	0	0	1	0	1	1



NMT:



Q10-11:



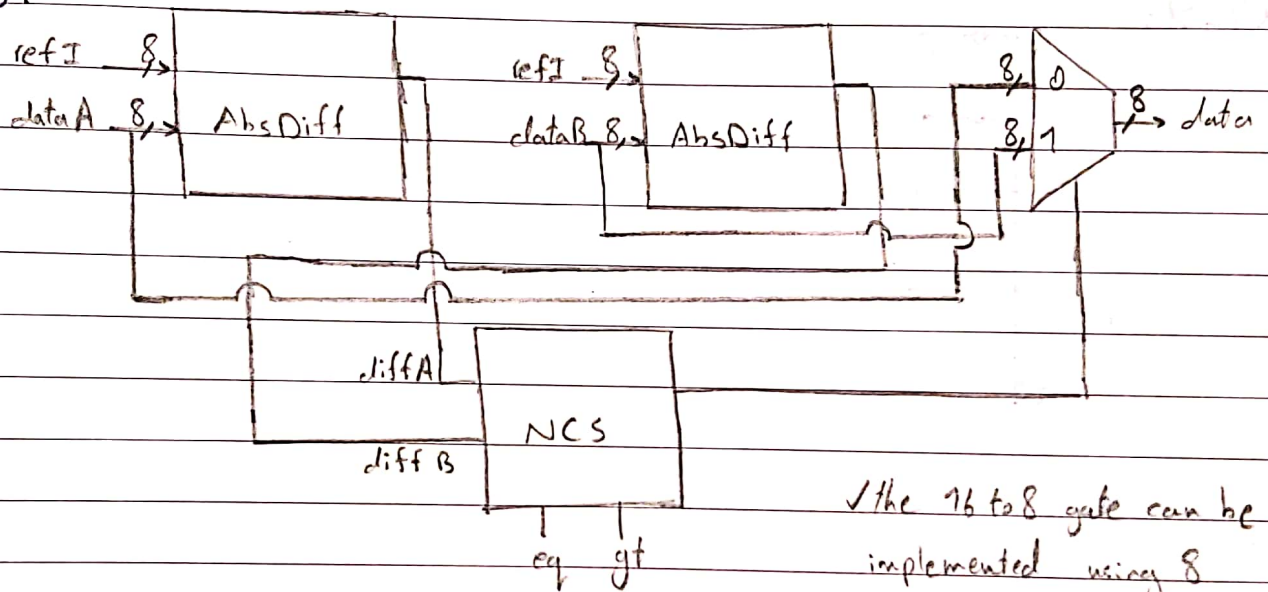
s.a.m

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Q12-13:



✓ the 16 to 8 gate can be
implemented using 8
2 to 1 mux's.