Experiment #3 – Function Generator

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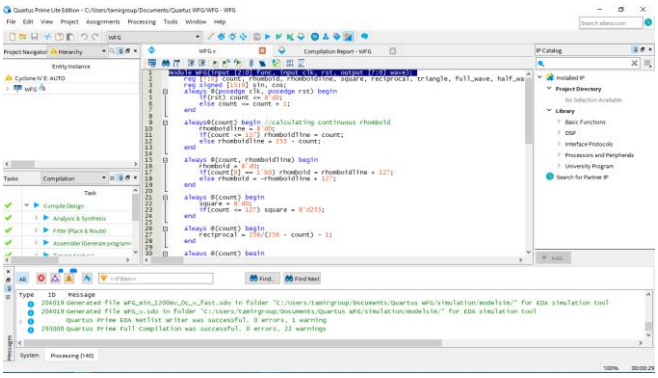
I. Introduction

In this lab, we try to build different waveforms. Then we'll set different frequencies for said waveforms and in the end, we try to decrease the output value with amplifier!

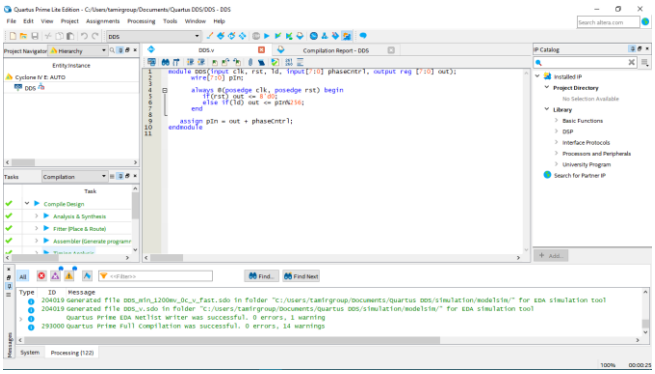
II. Waveform Generator

First, we write the WGP's Verilog code and synthesis it. Then we need to write and synthesis a DDS using the given file. Finally, we can set together a new circuit and synthesis the whole project.

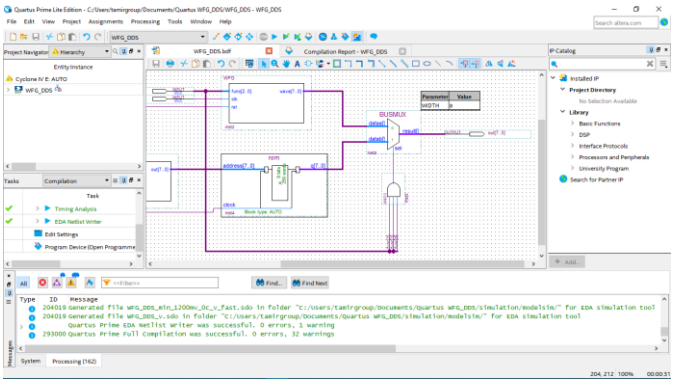
A. *Synthesis in Quartus*



WGP synthesis

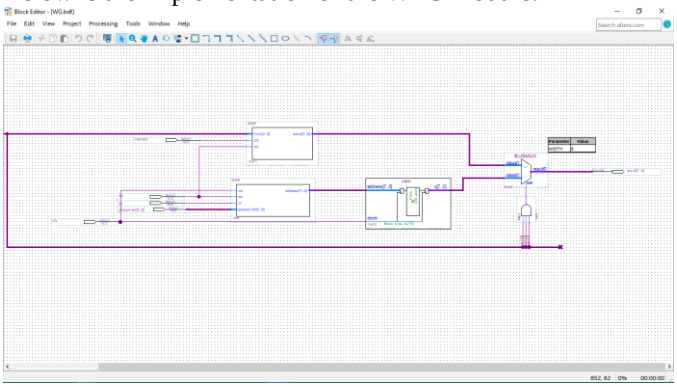


DDS synthesis



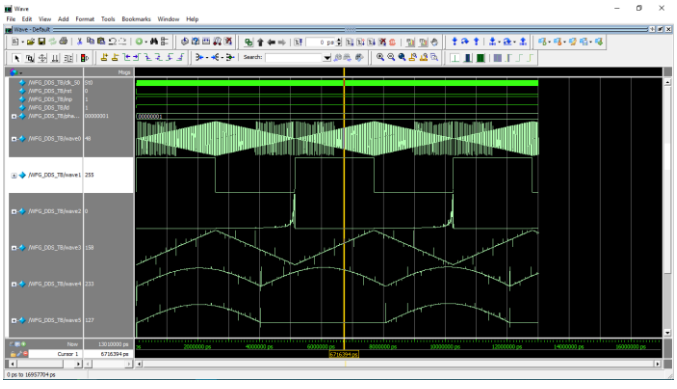
WFG synthesis

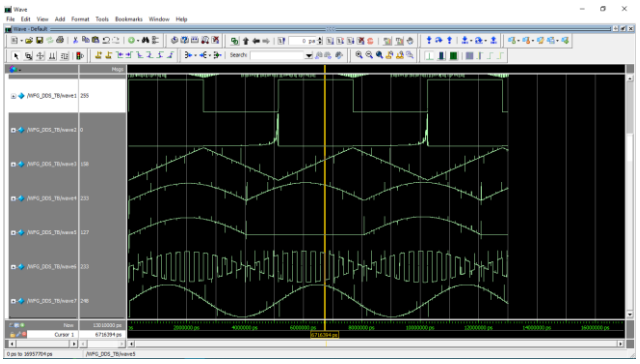
Below is the implementation of the WFG module:



B. *Testing in Modelsim*

We can check the accuracy of our circuit with a testbench, the result is shown below.





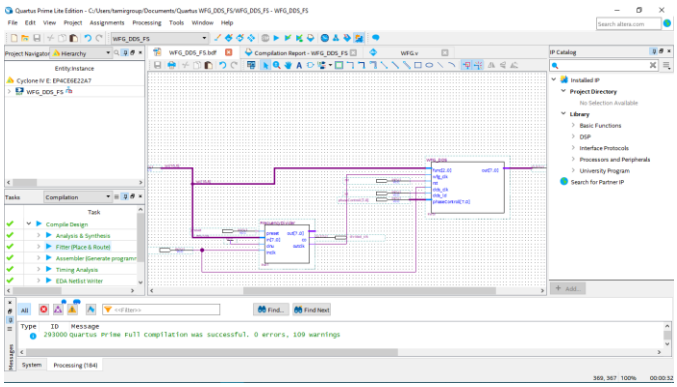
Note that the last waveform belongs to the DDS.

III. Frequency Selector

In this part, we design the frequency divider of lab1 to build a Frequency Selector and add it to the rest of the circuit.

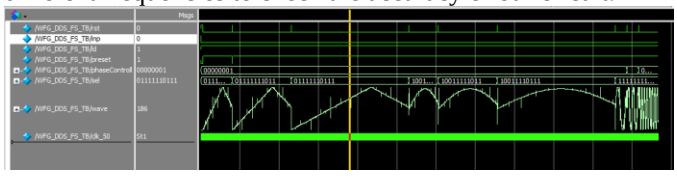
A. Design and Synthesis

Below is the compiled circuit in Quartus.



B. Simulation in Modelsim

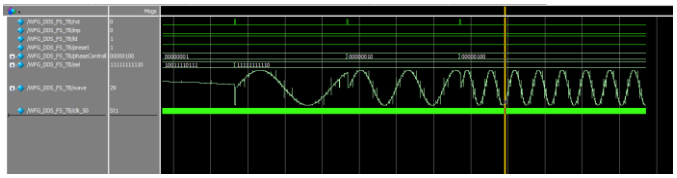
After synthesising is complete, we write a test bench with different frequencies to check the accuracy of our circuit.



It can be observed that the output frequency has changed 3 times because of the different load inputs.

LOAD	EXPECTED	ACHIEVED
253	50*1/2*1/2*1/256	0.045
251	50*1/2*1/4*1/256	0.023
247	50*1/2*1/8*1/256	0.011

Note that when we double the parallel load (255 – LOAD), the frequency becomes half the value of the previous state. This can be seen in the above picture too!

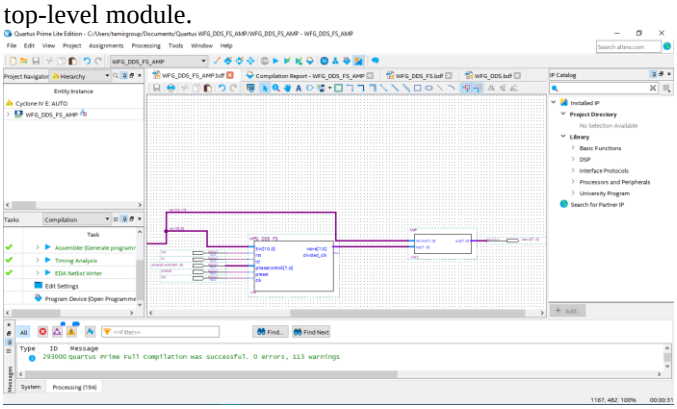


The DDS frequency also changes when we change phaseControll from 1 to 2 to 4. As it is shown, the frequency becomes nearly double every time. This is because our DDS adder is jumping twice distances as much.

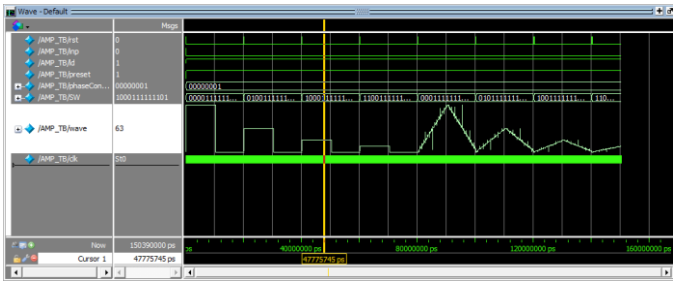
IV. Amplitude Selector

A. Design and Synthesis

First, we write the AMP Verilog code. Then we synthesis that code in Quartus and add the module to the circuit from the previous part. Then we synthesis the whole circuit as a top-level module.



B. Simulation in Modelsim



After writing the proper test bench we can observe that if we increase the divisor, the amplitude will decrease by half. You can verify this by checking the maximum value the waveforms hold in regards to the amplifier value.

V. Conclusions

In this Lab, we worked and generated different waveforms. we learned to change our waveforms' frequencies and even use amplifiers to set our output value to a certain amount.