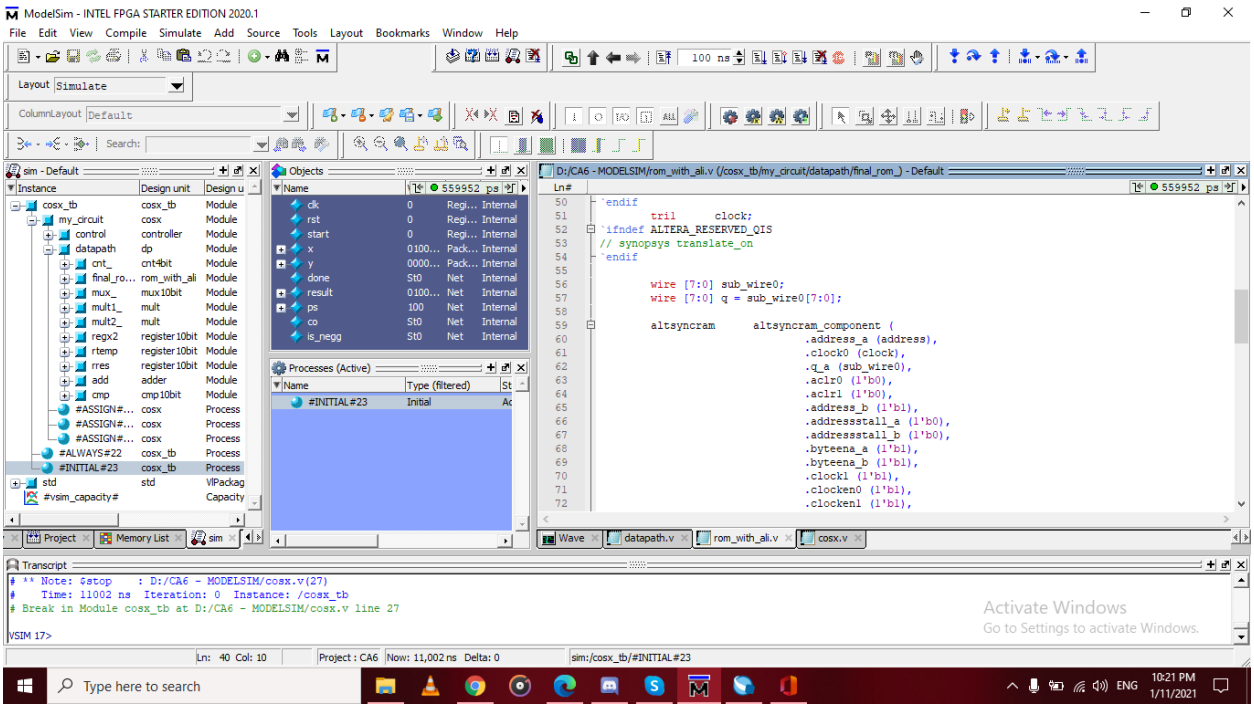
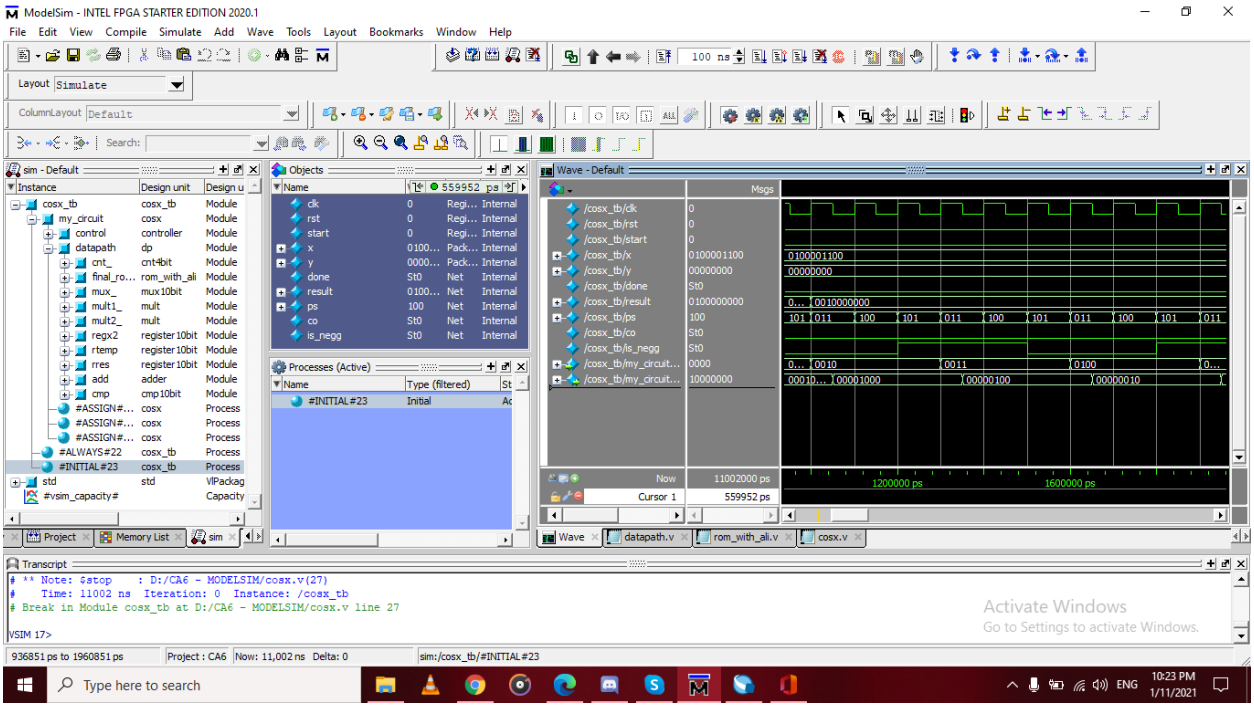
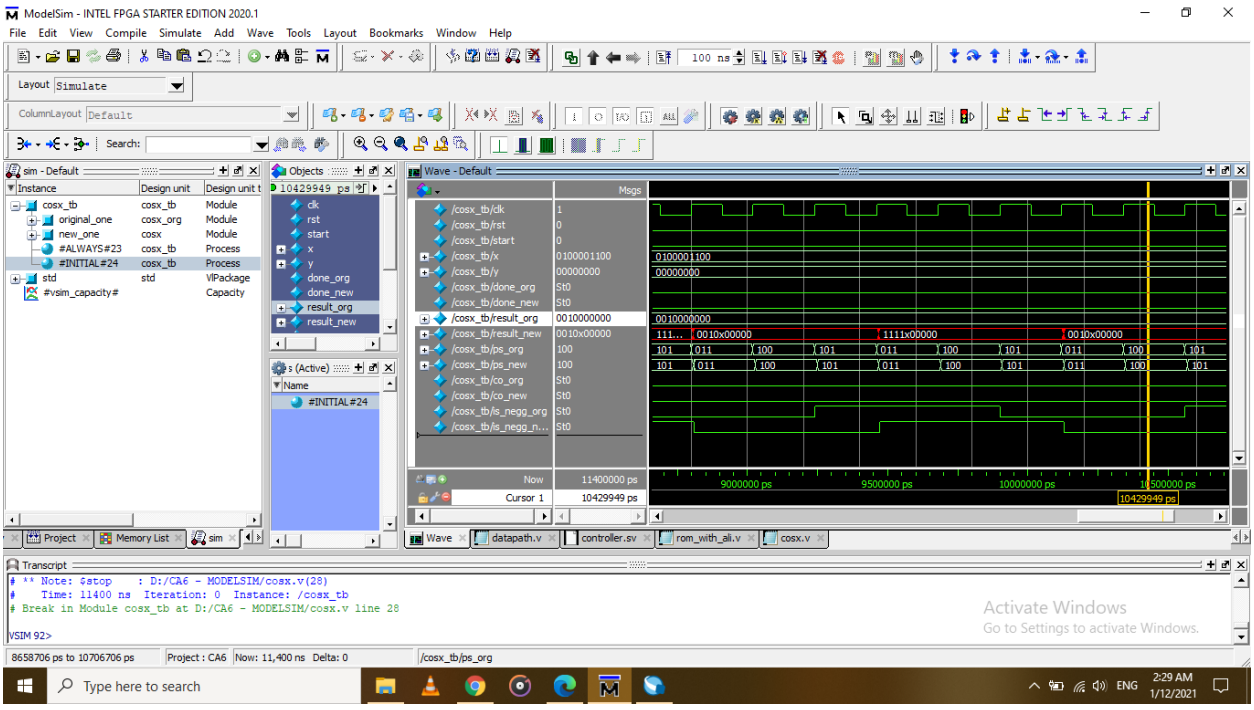
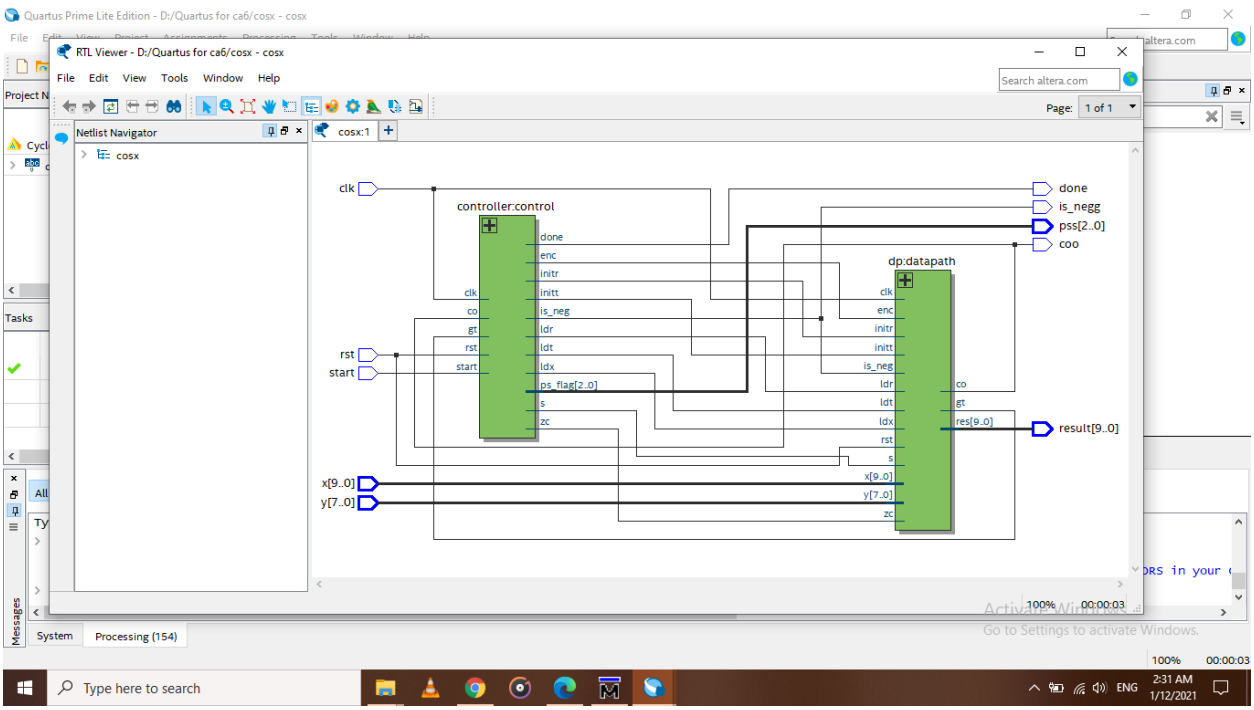
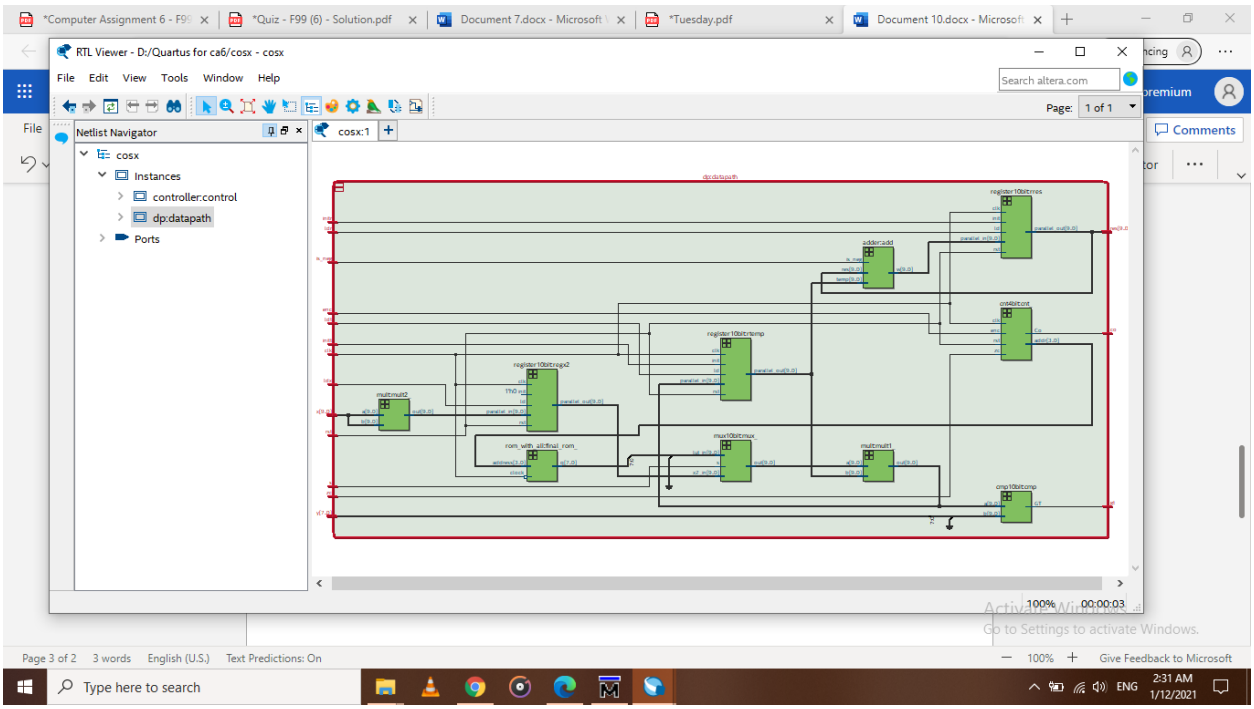
Borna Tavassoli CA#6

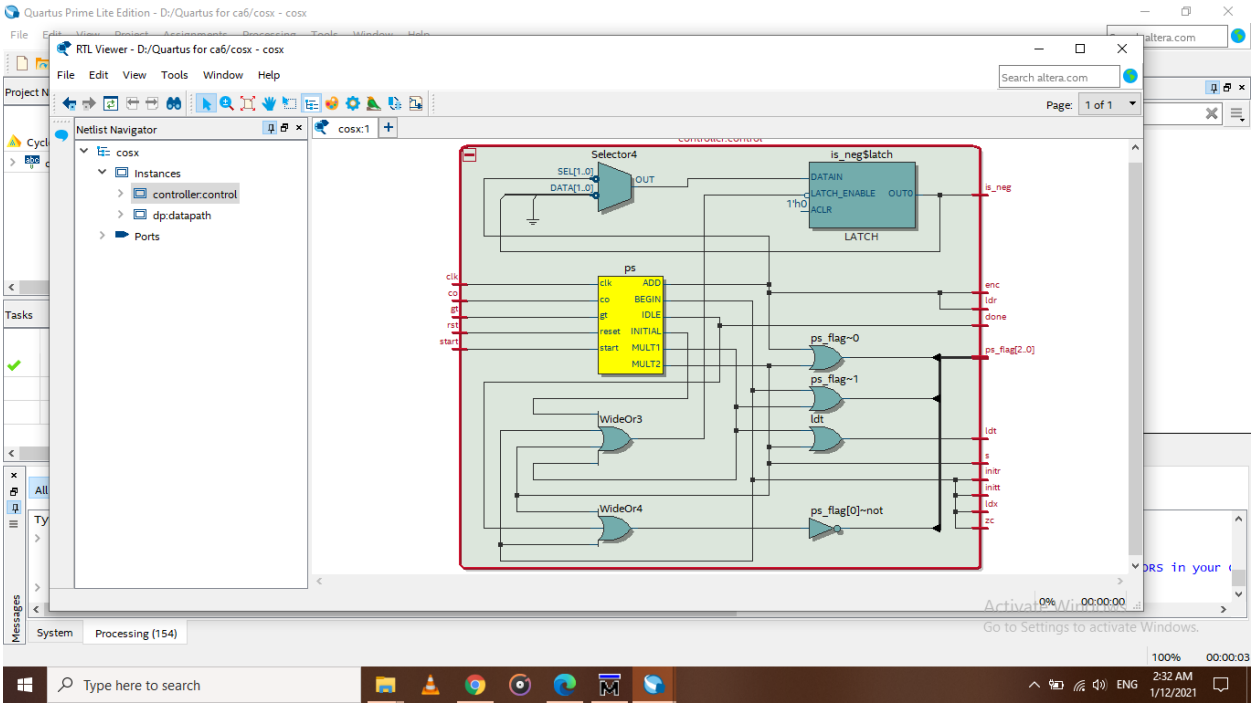


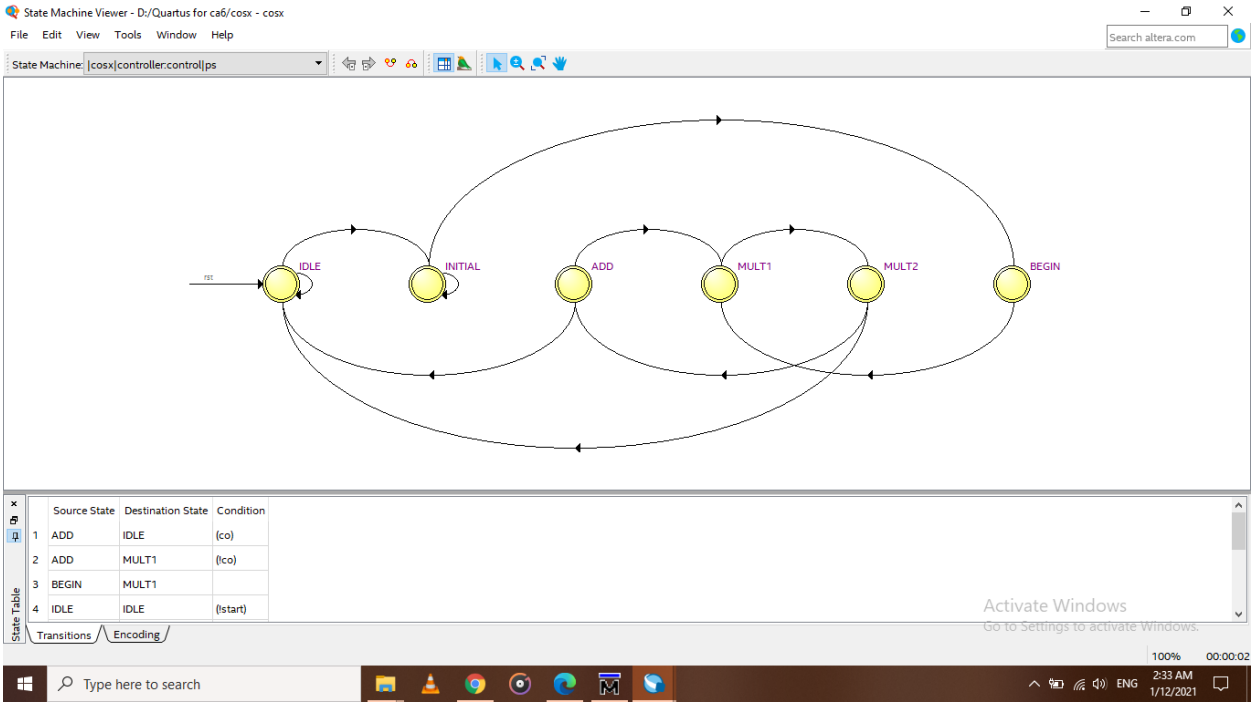


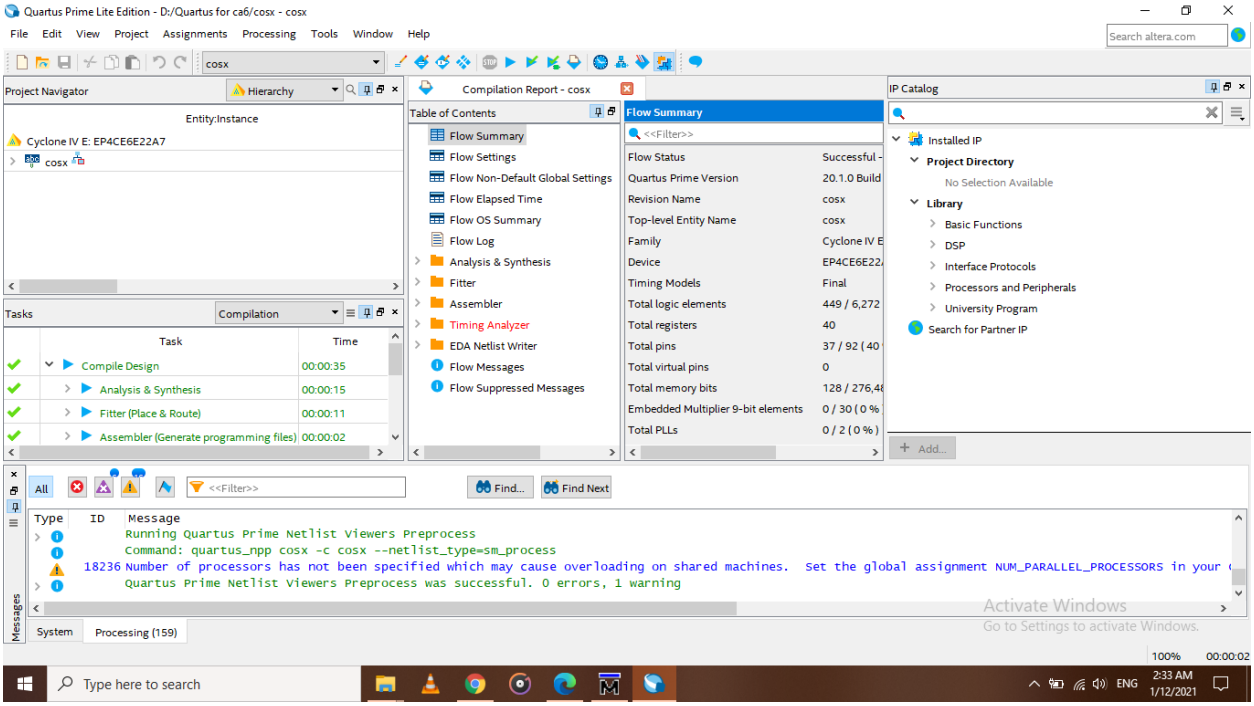

ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help
Wave - Default
Transcript
** Note: $stop : D:/CA6 - MODELSIM/cosx.v(28)
Time: 11400 ns Iteration: 0 Instance: /cosx_tb
Break in Module cosx_tb at D:/CA6 - MODELSIM/cosx.v line 28
VSIM 92>
Activate Windows
Go to Settings to activate Windows.
Type here to search
2:29 AM
1/12/2021


Quartus Prime Lite Edition - D:/Quartus for ca6/cosx - cosx
RTL Viewer - D:/Quartus for ca6/cosx - cosx
File Edit View Tools Window Help
Netlist Navigator
cosx
cosx:1
clk
rst
start
x[9..0]
y[7..0]
controller:control
done
enc
initr
initt
is_neg
ldr
ldt
ldx
ps_flag[2..0]
s
zc
dp:datapath
co
gt
res[9..0]
result[9..0]
done
is_negg
pss[2..0]
coo
100%
00:00:03
Activate Windows
Go to Settings to activate Windows.
Type here to search
2:31 AM
1/12/2021


RTL Viewer - D:/Quartus for ca6/cosx - cosx
File Edit View Tools Window Help
Netlist Navigator
cosx
Instances
controller:control
dp:datapath
Ports
cosx:1
Page: 1 of 1
100%
00:00:03


RTL Viewer - D:/Quartus for ca6/cosx - cosx
File Edit View Tools Window Help
Netlist Navigator
cosx
Instances
controller:control
dp:datapath
Ports
cosx:1
Page: 1 of 1
Selector4
SEL[1..0]
DATA[1..0]
OUT
is_neg$latch
DATAIN
LATCH_ENABLE
OUT0
ACLR
1'h0
LATCH
is_neg
ps
clk
ADD
BEGIN
IDLE
INITIAL
MULT1
MULT2
enc
ldr
done
ps_flag[2..0]
ps_flag~0
ps_flag~1
ldt
WideOr3
WideOr4
ps_flag[0]~not
initr
initt
ldx
zc
100%
00:00:00
System
Processing (154)


State Machine Viewer - D:/Quartus for ca6/cosx - cosx
File Edit View Tools Window Help
State Machine: |cosx|controller:control|ps
IDLE
INITIAL
ADD
MULT1
MULT2
BEGIN
Source State | Destination State | Condition
1 ADD | IDLE | (co)
2 ADD | MULT1 | (!co)
3 BEGIN | MULT1 |
4 IDLE | IDLE | (!start)
State Table
Transitions
Encoding
Activate Windows
Type here to search
ENG
2:33 AM
1/12/2021


Quartus Prime Lite Edition - D:/Quartus for ca6/cosx - cosx
File Edit View Project Assignments Processing Tools Window Help
Project Navigator
Hierarchy
Entity:Instance
Cyclone IV E: EP4CE6E22A7
cosx
Compilation Report - cosx
Table of Contents
Flow Summary
Flow Settings
Flow Non-Default Global Settings
Flow Elapsed Time
Flow OS Summary
Flow Log
Analysis & Synthesis
Fitter
Assembler
Timing Analyzer
EDA Netlist Writer
Flow Messages
Flow Suppressed Messages
Flow Status Successful -
Quartus Prime Version 20.1.0 Build
Revision Name cosx
Top-level Entity Name cosx
Family Cyclone IV E
Device EP4CE6E22
Timing Models Final
Total logic elements 449 / 6,272
Total registers 40
Total pins 37 / 92 (40
Total virtual pins 0
Total memory bits 128 / 276,4
Embedded Multiplier 9-bit elements 0 / 30 (0 %
Total PLLs 0 / 2 (0 %)
IP Catalog
Installed IP
Project Directory
No Selection Available
Library
Basic Functions
DSP
Interface Protocols
Processors and Peripherals
University Program
Search for Partner IP
Add...
Tasks
Compilation
Task Time
Compile Design 00:00:35
Analysis & Synthesis 00:00:15
Fitter (Place & Route) 00:00:11
Assembler (Generate programming files) 00:00:02
Find... Find Next
Type ID Message
Running Quartus Prime Netlist Viewers Preprocess
Command: quartus_npp cosx -c cosx --netlist_type=sm_process
18236 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your
Quartus Prime Netlist Viewers Preprocess was successful. 0 errors, 1 warning
Messages
System
Processing (159)
Activate Windows
Type here to search
ENG
2:33 AM
1/12/2021