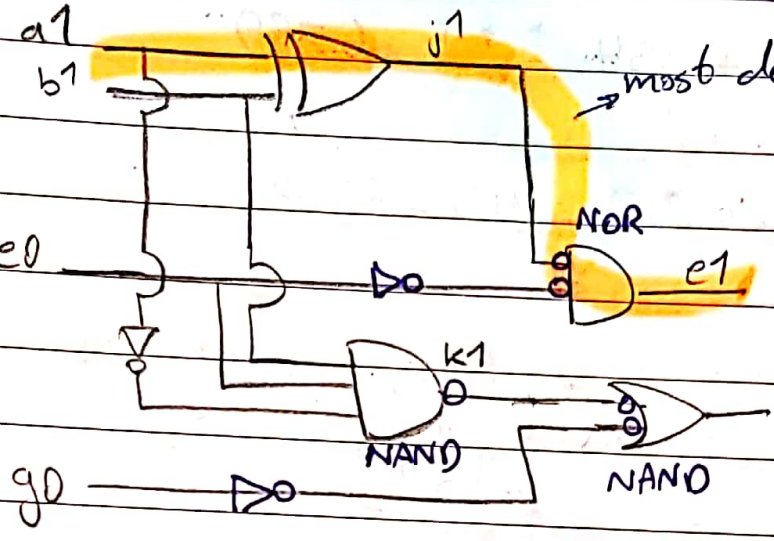
Subject:

Date: / /

Assignment #1 Report	Borna Tavassoli 810198374	Dr. Nowabi

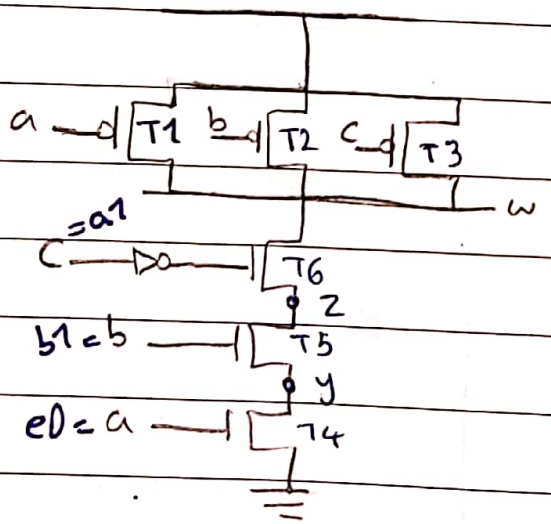


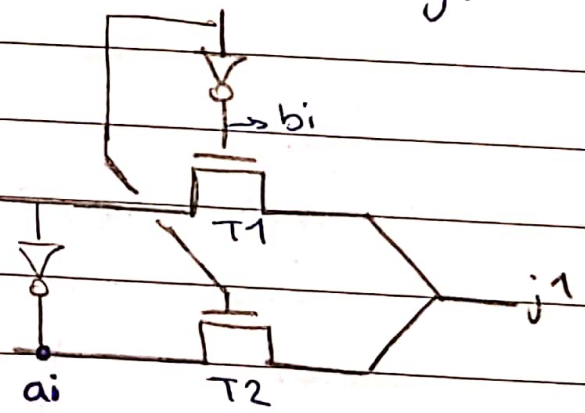
$j1 = \sim(a1 \hat{} b1)$

$e1 = \overline{a+b}$

$k1 = \sim(\sim a . b1 . e0)$

✓ we have simplified the circuit for more efficiency!





XOR

3input NAND

Assignment #1 Report

Borna Tavassoli
810198374

Dr. Nawabi

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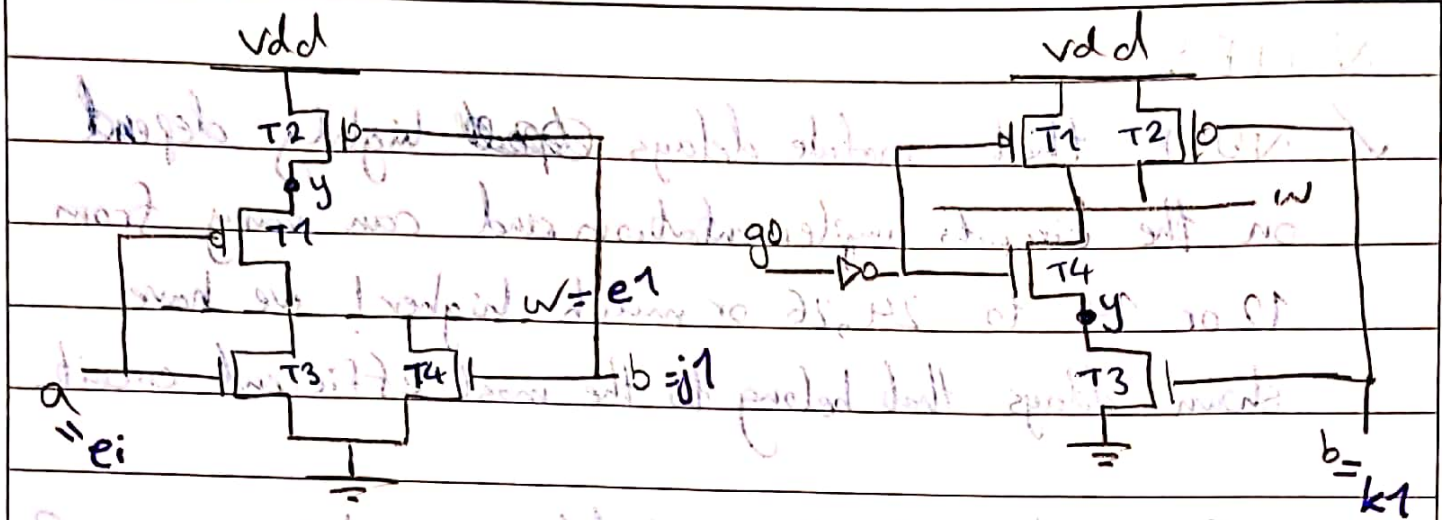

2 input NAND

NOR

Delays → NOT { to1: 5, to0: 7 } NAND { to1: 10, to0: 8 }

NOR { to1: 10, to0: 14 }

Module Delays : j1 = a1 ~^ b1 { to1: 12, to0: 12 }

e1 = j1 & e0 { to1: 12, to0: 14 }

k1 = ~a1 & b1 & e0 { to1: 12, to0: 12 }

g1 = k1 | g0 { to1: 12, to0: 12 }

Assignment #1 Report

Barna Tabrizi 810198374

Dr. Navabi

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NOTES:

✓ NOTE that module delays highly depend on the circuit's implementation and can vary from 12 or 14 to 24, 26 or much higher! we have shown delays that belong to the most efficient circuit.

The path with the most delay can have .2

#26 ns delays almost; that is the path iterating through XOR and NOR (e1) gates, which is also highlighted in orange in the previous page. note that no two 12 ns delays can ever occur in the same path.

please note that the paths with 18 and 22 ns delays are also shown in the program.

if we look closely at the Gate level waves, we .4 notice that they do not carry Z values! in other words, despite facing a lot of Z values when examining Transistor level waves, one will not discover such nature in Gate level waves.

✓ keep in mind the fact above, Gate level delays tend to be smaller than Transistor level delays (in a specific time). Both outputs are equal except when Transistor level waves are Z value.

YASHA