

**МИНИСТЕРСТВО НАУКИ И ВЫСШЕГО ОБРАЗОВАНИЯ
РОССИЙСКОЙ ФЕДЕРАЦИИ**

**ФЕДЕРАЛЬНОЕ ГОСУДАРСТВЕННОЕ АВТОНОМНОЕ ОБРАЗОВАТЕЛЬНОЕ
УЧРЕЖДЕНИЕ ВЫСШЕГО ОБРАЗОВАНИЯ**

**НОВОСИБИРСКИЙ НАЦИОНАЛЬНЫЙ ИССЛЕДОВАТЕЛЬСКИЙ
ГОСУДАРСТВЕННЫЙ УНИВЕРСИТЕТ**

**Факультет информационных технологий
Кафедра параллельных вычислений**

ОТЧЕТ

О ВЫПОЛНЕНИИ ЛАБОРАТОРНОЙ РАБОТЫ 3

студента х

Новосибирск, 2022

Цель

Научиться оптимизировать использование памяти в простых программах численного моделирования.

Задание

Решение волнового уравнения методом конечных объёмов. В качестве типов данных нужно использовать double.

Алгоритм моделирует распространение волны в двумерной области, инициированной импульсом из заданного узла сетки. В начальный момент времени значения искомой функции U на сетке инициализируются нулями. На каждом шаге моделирования значения искомой функции пересчитываются по заданной формуле.

Входные данные: $N_x=N_y=20000$, $N_t=120$.

Процессор: Intel(R) Xeon(R) Gold 6128 CPU @ 3.40GHz

Ход работы

Времена замеров

Оптимизации	Время, сек
AVX2-лаб2	155,3
AVX512-лаб2	146,1
AVX2	136,7
AVX512	93,6

Выводы:

1. Реорганизация операций дает прирост производительности, но ухудшает читаемость кода.

Характеристика варианта с AVX2

Elapsed Time: 172.295s

IPC: 2.838
SP GFLOPS: 0.000
DP GFLOPS: 6.406
x87 GFLOPS: 0.139
Average CPU Frequency: 3.6 GHz

Logical Core Utilization: 3.6% (0.865 out of 24)

Microarchitecture Usage: 80.2% of Pipeline Slots

Retiring: 80.2% of Pipeline Slots
Front-End Bound: 1.9% of Pipeline Slots
Bad Speculation: 0.7% of Pipeline Slots
Back-End Bound: 17.2% of Pipeline Slots

Memory Bound: 8.8% of Pipeline Slots

Vectorization: 91.9% of Packed FP Operations

Instruction Mix:
SP FLOPs: 0.0% of uOps
DP FLOPs: 16.1% of uOps
Packed: 99.9% from DP FP
128-bit: 0.0% from DP FP
256-bit: 99.9% from DP FP
512-bit: 0.0% from DP FP
Scalar: 0.1% from DP FP
x87 FLOPs: 1.4% of uOps
Non-FP: 82.5% of uOps
FP Arith/Mem Rd Instr. Ratio: 0.619
FP Arith/Mem Wr Instr. Ratio: 1.178

Характеристика варианта с AVX512

Elapsed Time[Ⓢ]: 123.436s

IPC[Ⓢ]: 1.638
SP GFLOPS[Ⓢ]: 0.000
DP GFLOPS[Ⓢ]: 8.960
x87 GFLOPS[Ⓢ]: 0.098
Average CPU Frequency[Ⓢ]: 3.5 GHz

Logical Core Utilization[Ⓢ]: 3.3% (0.782 out of 24) 🚩

Microarchitecture Usage[Ⓢ]: 45.5% 🚩 of Pipeline Slots 📄

Retiring[Ⓢ]: 45.5% of Pipeline Slots
Front-End Bound[Ⓢ]: 3.3% of Pipeline Slots
Bad Speculation[Ⓢ]: 1.3% of Pipeline Slots
✓ Back-End Bound[Ⓢ]: 49.9% 🚩 of Pipeline Slots
✓ Memory Bound[Ⓢ]: 26.8% 🚩 of Pipeline Slots
 ➤ L1 Bound[Ⓢ]: 4.5% of Clockticks
 L2 Bound[Ⓢ]: 11.4% 🚩 of Clockticks
 ➤ L3 Bound[Ⓢ]: 3.7% of Clockticks
✓ DRAM Bound[Ⓢ]: 10.1% 🚩 of Clockticks
 Memory Bandwidth[Ⓢ]: 66.0% 🚩 of Clockticks
 ✓ Memory Latency[Ⓢ]: 11.7% 🚩 of Clockticks
 Local DRAM[Ⓢ]: 22.0% 🚩 of Clockticks
 Remote DRAM[Ⓢ]: 6.7% of Clockticks
 Remote Cache[Ⓢ]: 0.0% of Clockticks
 Store Bound[Ⓢ]: 2.1% of Clockticks
Core Bound[Ⓢ]: 23.1% 🚩 of Pipeline Slots

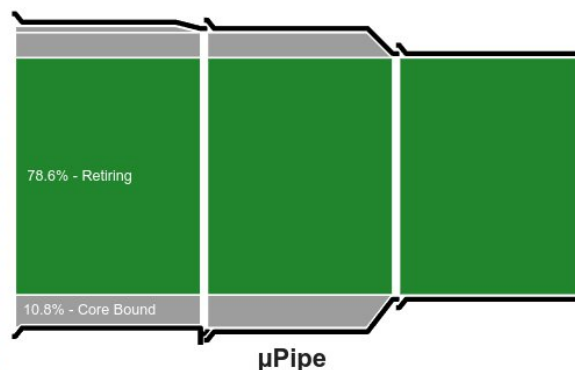
Memory Bound[Ⓢ]: 26.8% 🚩 of Pipeline Slots

Vectorization[Ⓢ]: 91.5% of Packed FP Operations

Ограничения варианта с AVX2

Elapsed Time: 179.534s

Clockticks:	546,822,000,000
Instructions Retired:	1,525,070,000,000
CPI Rate:	0.359
Retiring:	78.6% of Pipeline Slots
Light Operations:	68.1% of Pipeline Slots
FP Arithmetic:	17.1% of uOps
Memory Operations:	28.8% of Pipeline Slots
Fused Instructions:	1.4% of Pipeline Slots
Non Fused Branches:	1.8% of Pipeline Slots
Nop Instructions:	0.7% of Pipeline Slots
Other:	18.2% of Pipeline Slots
Heavy Operations:	10.5% of Pipeline Slots
Microcode Sequencer:	4.2% of Pipeline Slots
Front-End Bound:	2.1% of Pipeline Slots
Bad Speculation:	0.2% of Pipeline Slots
Back-End Bound:	19.1% of Pipeline Slots
Memory Bound:	8.3% of Pipeline Slots
Core Bound:	10.8% of Pipeline Slots
Divider:	17.4% of Clockticks
Port Utilization:	12.7% of Clockticks
Cycles of 0 Ports Utilized:	6.7% of Clockticks
Cycles of 1 Port Utilized:	2.3% of Clockticks
Cycles of 2 Ports Utilized:	5.2% of Clockticks
Cycles of 3+ Ports Utilized:	36.1% of Clockticks
Vector Capacity Usage (FPU):	46.5%
Average CPU Frequency:	3.6 GHz
Total Thread Count:	2
Paused Time:	0s

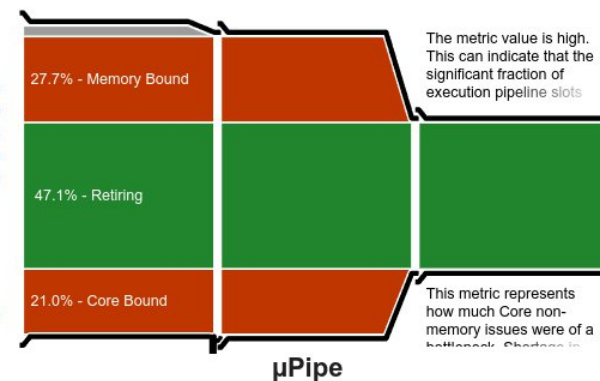


This diagram represents inefficiencies in CPU usage. Treat it as a pipe with an output flow equal to the "pipe efficiency" ratio: (Actual Instructions Retired)/(Maximum Possible Instruction Retired). If there are pipeline stalls decreasing the pipe efficiency, the pipe shape gets more narrow.

Ограничения варианта с AVX512

Elapsed Time: 132.130s

Clockticks:	329,426,000,000
Instructions Retired:	554,098,000,000
CPI Rate:	0.595
Retiring:	47.1% of Pipeline Slots
Front-End Bound:	3.5% of Pipeline Slots
Bad Speculation:	0.7% of Pipeline Slots
Back-End Bound:	48.7% of Pipeline Slots
Memory Bound:	27.7% of Pipeline Slots
L1 Bound:	5.0% of Clockticks
L2 Bound:	14.1% of Clockticks
L3 Bound:	2.5% of Clockticks
DRAM Bound:	9.4% of Clockticks
Store Bound:	1.7% of Clockticks
Core Bound:	21.0% of Pipeline Slots
Divider:	14.5% of Clockticks
Port Utilization:	19.9% of Clockticks
Cycles of 0 Ports Utilized:	18.2% of Clockticks
Cycles of 1 Port Utilized:	6.2% of Clockticks
Cycles of 2 Ports Utilized:	8.3% of Clockticks
Cycles of 3+ Ports Utilized:	17.6% of Clockticks
Vector Capacity Usage (FPU):	92.6%
Average CPU Frequency:	3.2 GHz
Total Thread Count:	2
Paused Time:	0s

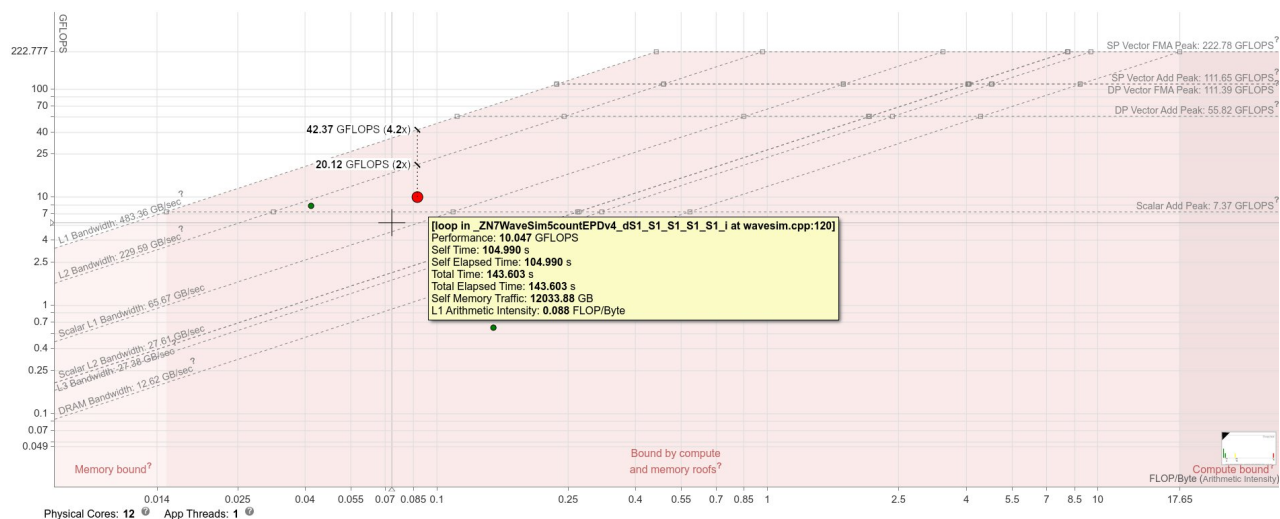


The metric value is high. This can indicate that the significant fraction of execution pipeline slots

This metric represents how much Core non-memory issues were of a bottleneck. Slows in

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Roofline варианта с AVX2



Roofline варианта с AVX512

