

1. Introduction

The aim of the laboratory was to familiarize with the principles of DAC. Using Analog Discovery 2 as a sine wave generator, we had to read STM32 ADC input and feed it to DAC in the first part. Then instead of using signal from ADC, hardcoded generated values of sine were used. Lastly DDS algorithm was used to tweak the base frequency of signal. Additionally, RC filter was added.

2. Results

2.1. DAC driven by ADC with oversampling

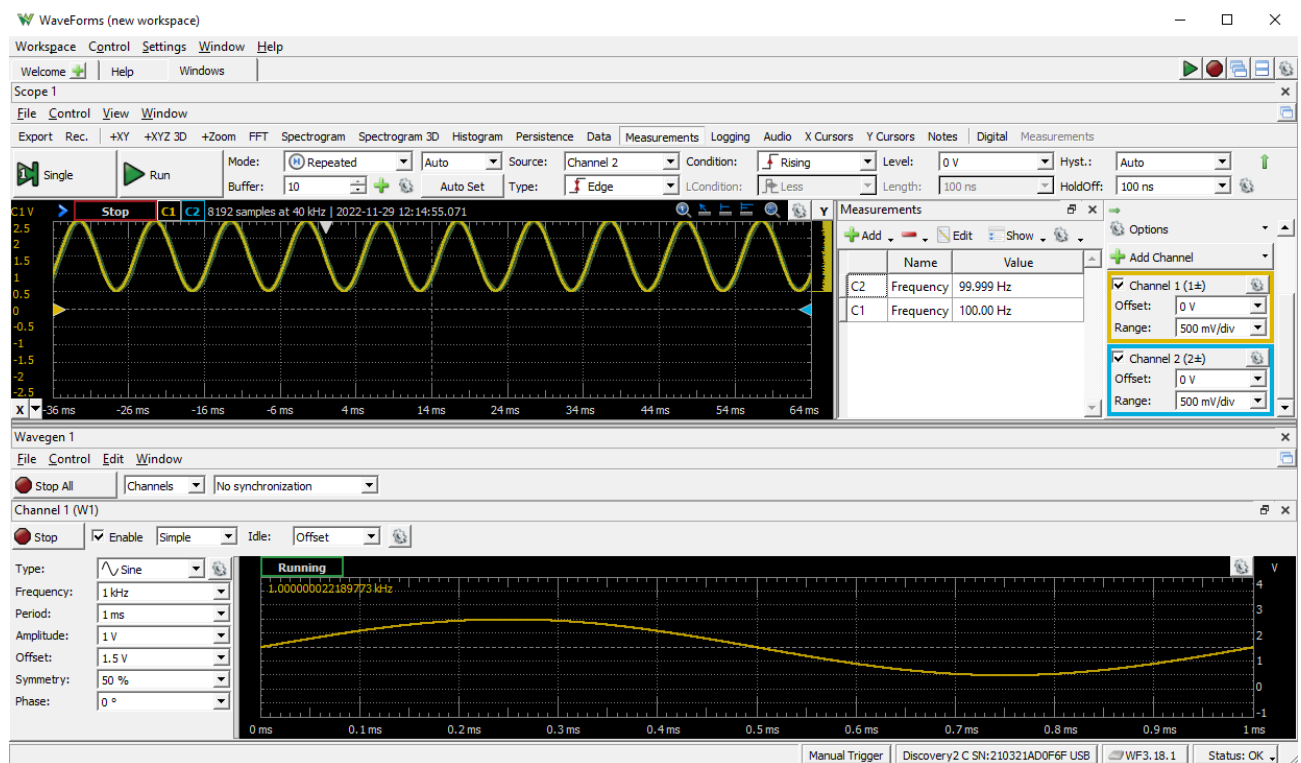


Figure 1 $f = 100$ Hz

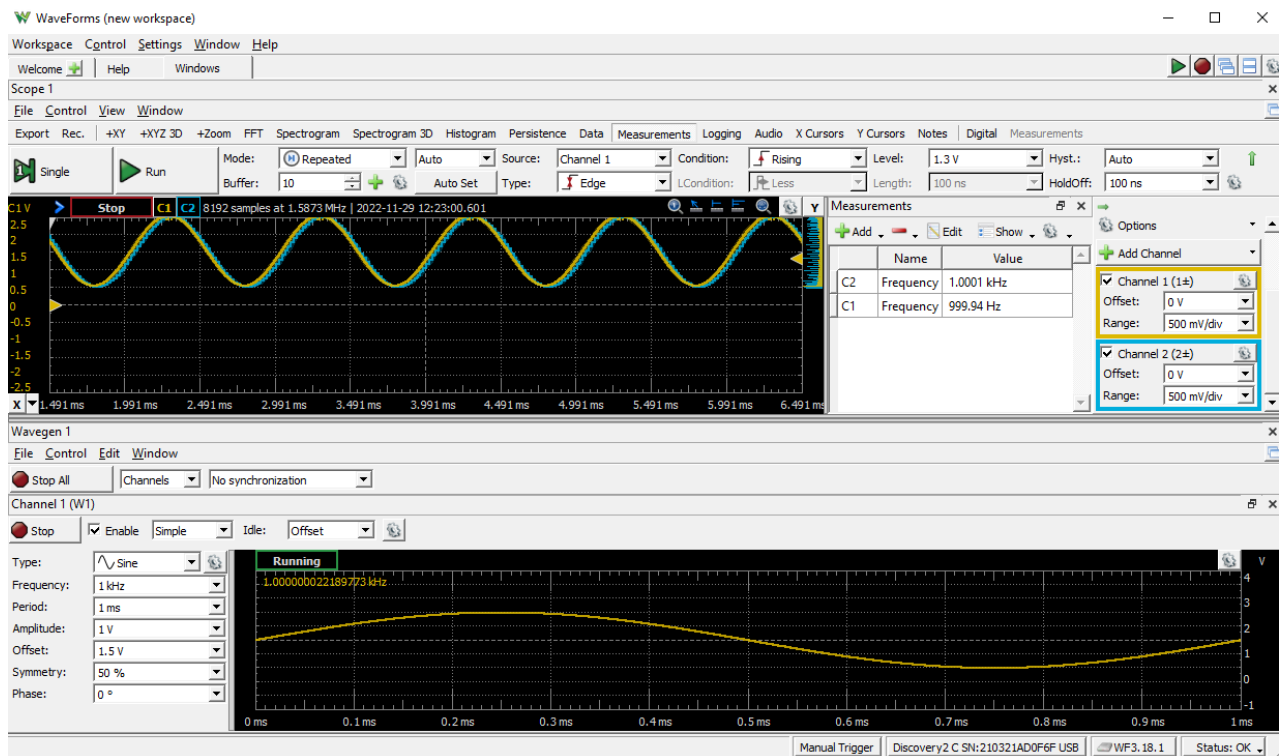


Figure 2 $f = 1 \text{ kHz}$

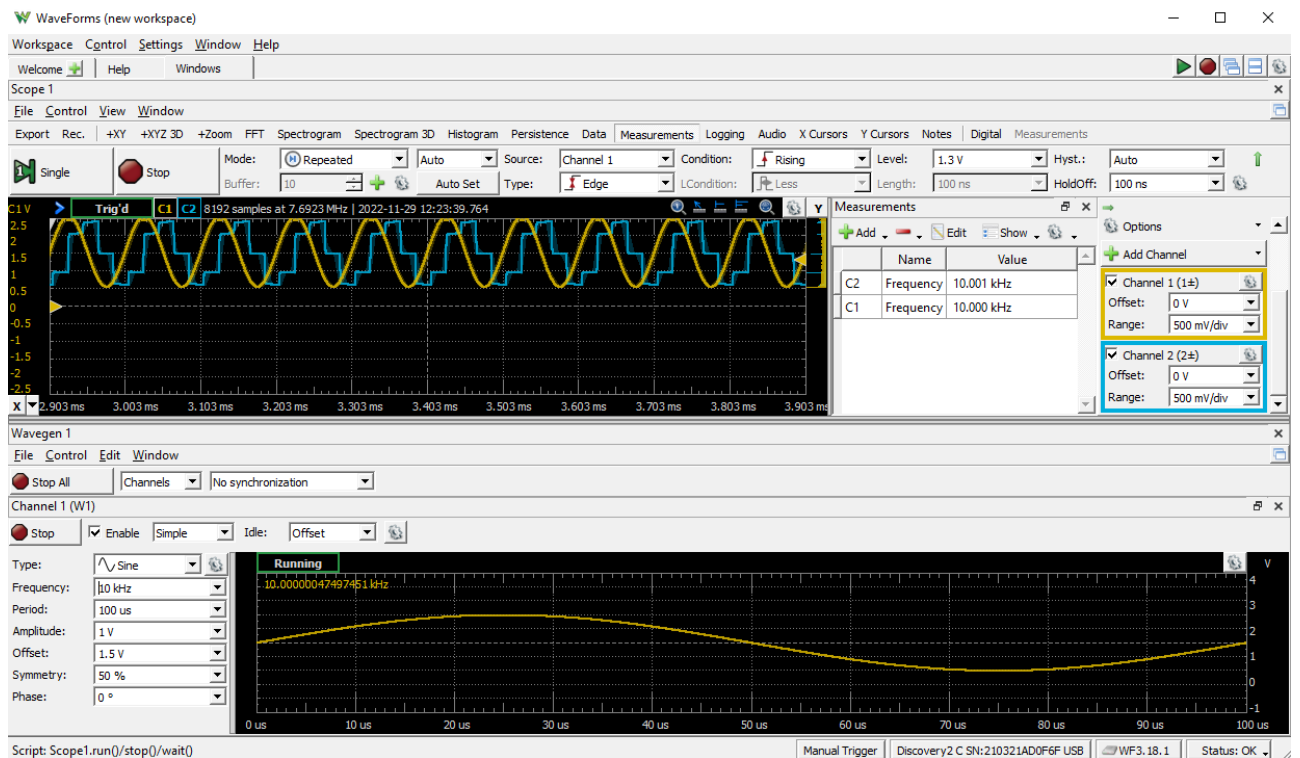


Figure 3 $f = 10 \text{ kHz}$

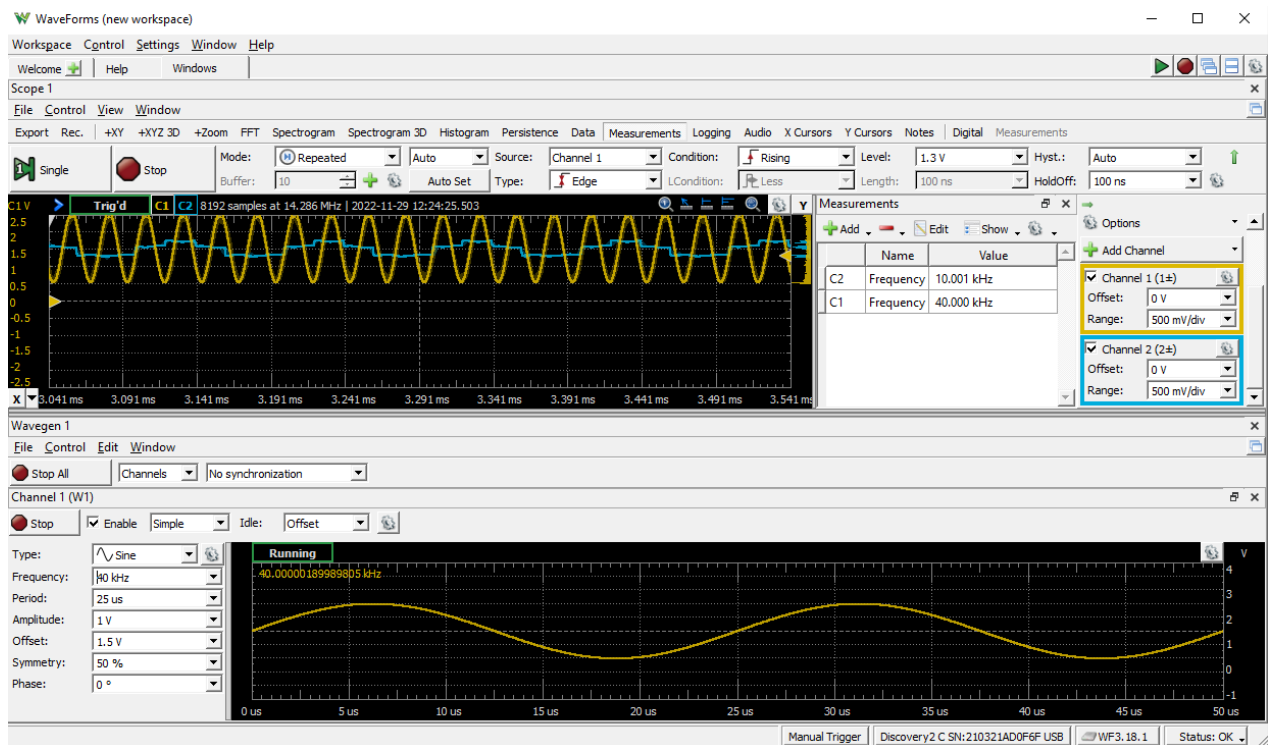


Figure 4 $f = 30 \text{ kHz}$

On the bottom part of each figure, we can see a signal as generated by Analog Discovery. Top part of them consists of signal outputted by DAC. DAC is fed by ADC converting first signal. Therefore it is limited by its sampling frequency equal to 50 kHz (parameters set as in the previous laboratory). We can see that 100 Hz and 1 kHz are nicely modelled with slight flaws. In the signal 10 kHz there are visible steps of sine, but the frequency is proper – there is no aliasing. The frequency is 5 times smaller than the sampling rate which can be seen as 5 visible steps for period. Last signal cannot be modelled properly because sampling is not twice larger. To avoid aliasing we should sample with at least 60 kHz.

2.2. Sine function generator

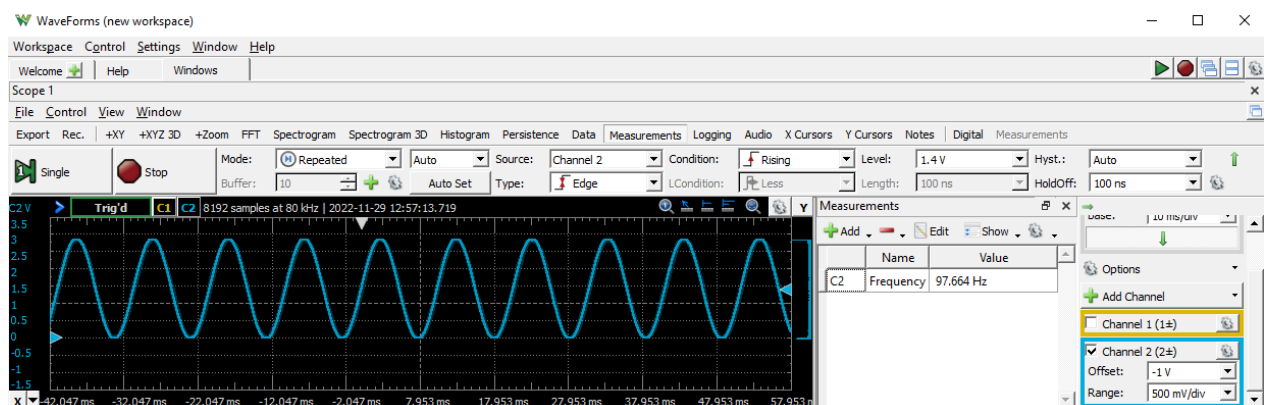


Figure 5 $f = 100 \text{ Hz}$

In the next step, signal is no longer taken from ADC. Instead it was generated as 1024 table of sine values and then fed to DAC triggered by Timer 2. The achievable frequency is limited by the maximum frequency of timer, divided by 2 (to avoid aliasing).

2.3. DAC with DDS

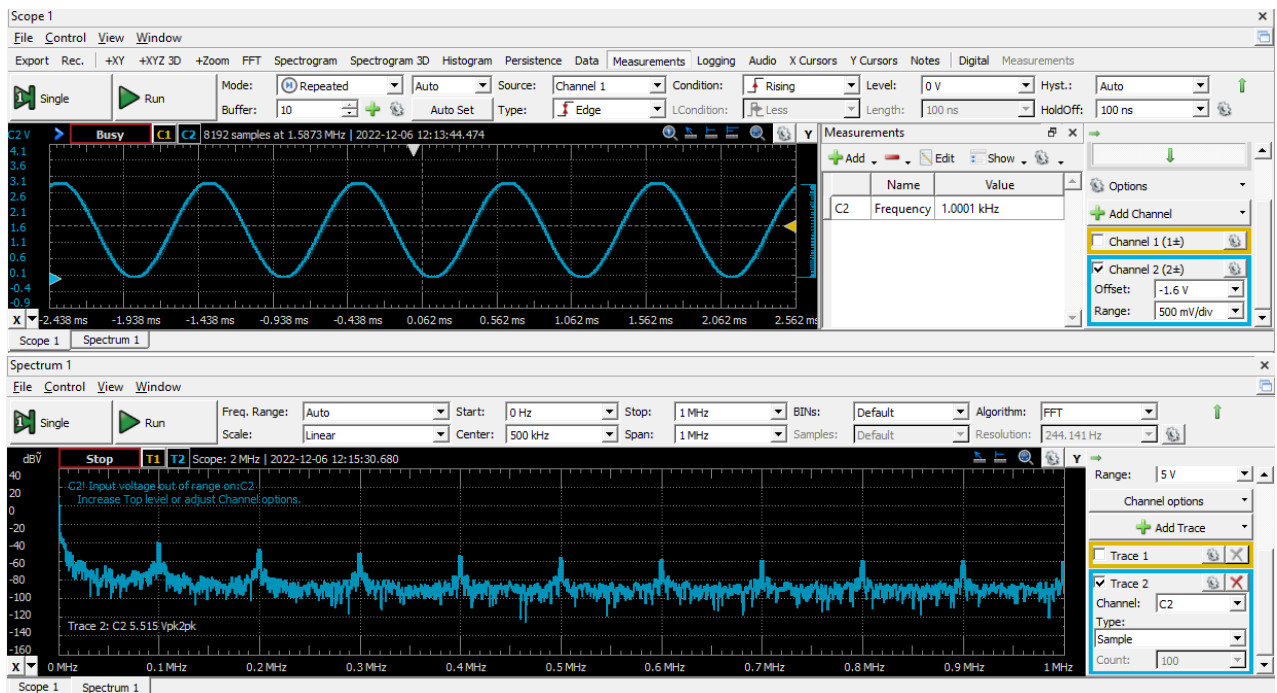


Figure 6 $f = 1 \text{ kHz}$



Figure 7 $f = 1.37 \text{ kHz}$

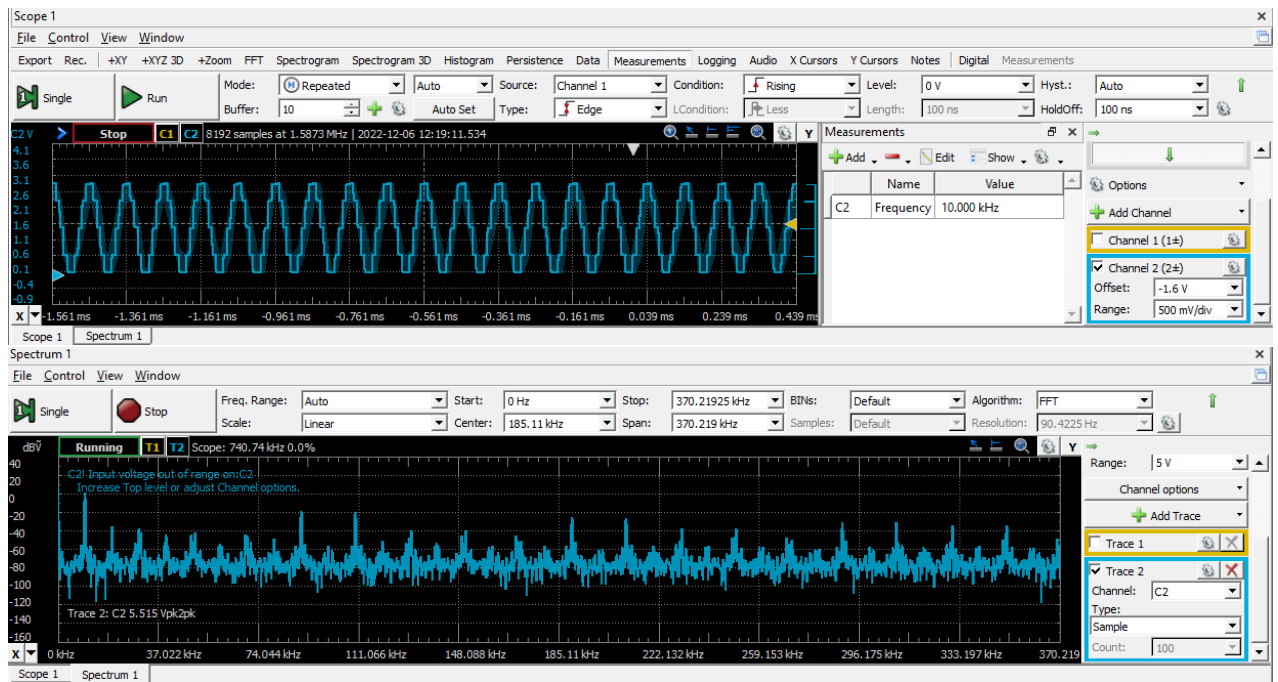


Figure 8 $f = 10$ kHz



Figure 9 $f = 30$ kHz

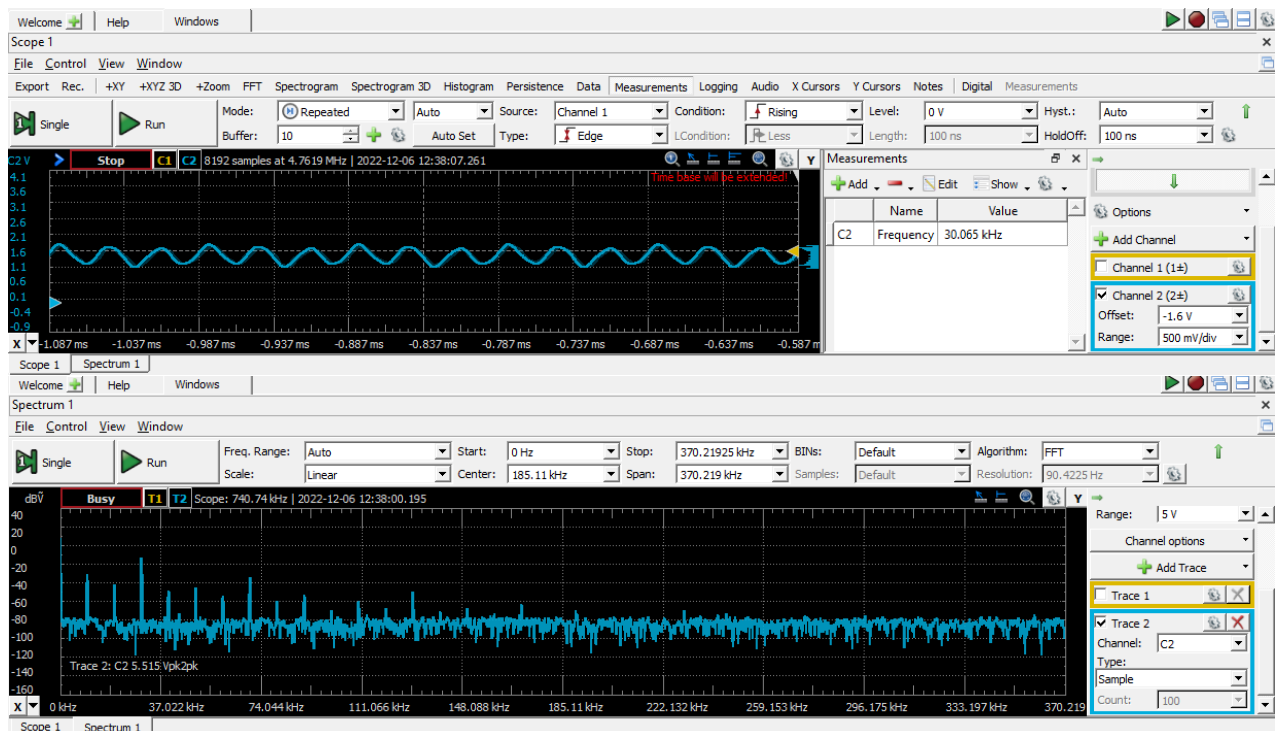


Figure 10 $f = 30$ kHz with RC filter

```

234 void HAL_TIM_PeriodElapsedCallback(TIM_HandleTypeDef *htim)
235 {
236     if(htim == &htim2)
237     {
238         DDSAlgorithm();
239     }
240 }
241
242 void DDSAlgorithm()
243 {
244     phaseStep = SINE_BUF_SIZE / SAMPLE_FREQ * outFreq;
245
246     static float phaseAccumulator = 0;
247     phaseAccumulator += phaseStep;
248
249     if (phaseAccumulator >= SINE_BUF_SIZE)
250         phaseAccumulator -= SINE_BUF_SIZE;
251
252     HAL_DAC_SetValue(&hdac, DAC_CHANNEL_2, DAC_ALIGN_12B_L, lookup[(int)phaseAccumulator]);
253 }

```

Figure 11 DDS algorithm

DDS main advantage is that it allows us to tweak base frequency purely in software. As seen above it is possible to implement it using DAC with DMA but of course there are some limitations. As shown, signals up to 10 kHz are modelled properly. It cannot be said about 30 kHz. Also, spectrum analyzer shows that generated signal has a lot of harmonics. The higher the frequency the worse is the quality of signal. However it can be helped with low-pass RC filter (figure 10). Such filter blocks signal of a frequency higher than cut-off frequency (by grounding them through capacitor) and allows those lower through a resistor. It lowered the amplitude of harmonics and smoothened the signal itself.