CONFIGURING THE Si5356A

1. Introduction

The Si5356A is a highly flexible and configurable clock generator. A block diagram of the Si5356A is shown in Figure 1.

To support this flexibility, Silicon Labs has provided the ClockBuilder Desktop™ application. This tool allows seamless creation of register maps for a given configuration and is the recommended method of register map generation for the majority of the users. However, some users may have a need to modify their configuration multiple times and would prefer to write code optimized to write only the minimum number of registers each time.

This application note provides details for both options. Section "2. Generating a Register Map with ClockBuilder Desktop" illustrates the steps required to generate a frequency plan in ClockBuilder Desktop, and the later sections are geared towards the latter group of users.

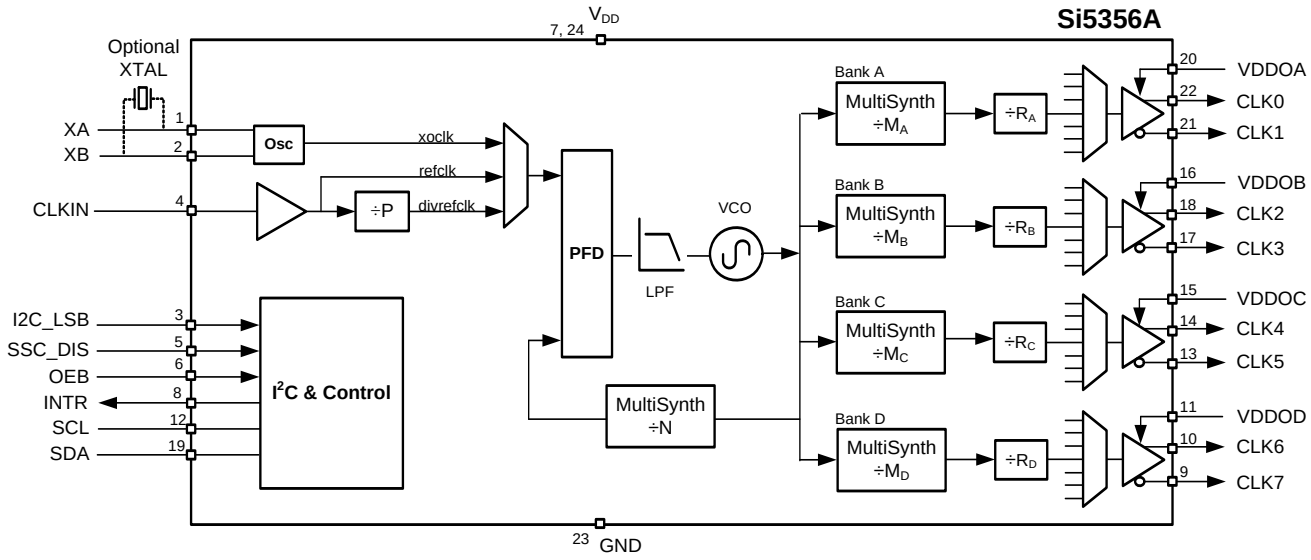

Figure 1. Si5356A Block Diagram

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2. Generating a Register Map with ClockBuilder Desktop

The ClockBuilder Desktop can be downloaded from http://www.silabs.com/ClockBuilder and runs on Windows XP, Windows Vista, and Windows 7. The optimal configuration can be saved from the software in text files that can be used in any system that configures the device over I^2C. To generate a register map file, follow the steps in this section and save the file using the menu Options → Save Register Map File... or Options → Save C Code Header File... , the latter of which can be used in conjunction with the sample device programming code provided in "AN428: Jump Start: In-System, Flash-based Programming for Silicon Labs' Timing Products."

2.1. Setting up the Frequency Plan

The Frequency Plan tab is used to configure the reference source and output frequencies. Valid inputs are 25 MHz crystal, 27 MHz crystal, or a 5–200 MHz CMOS Clock on pin 4.

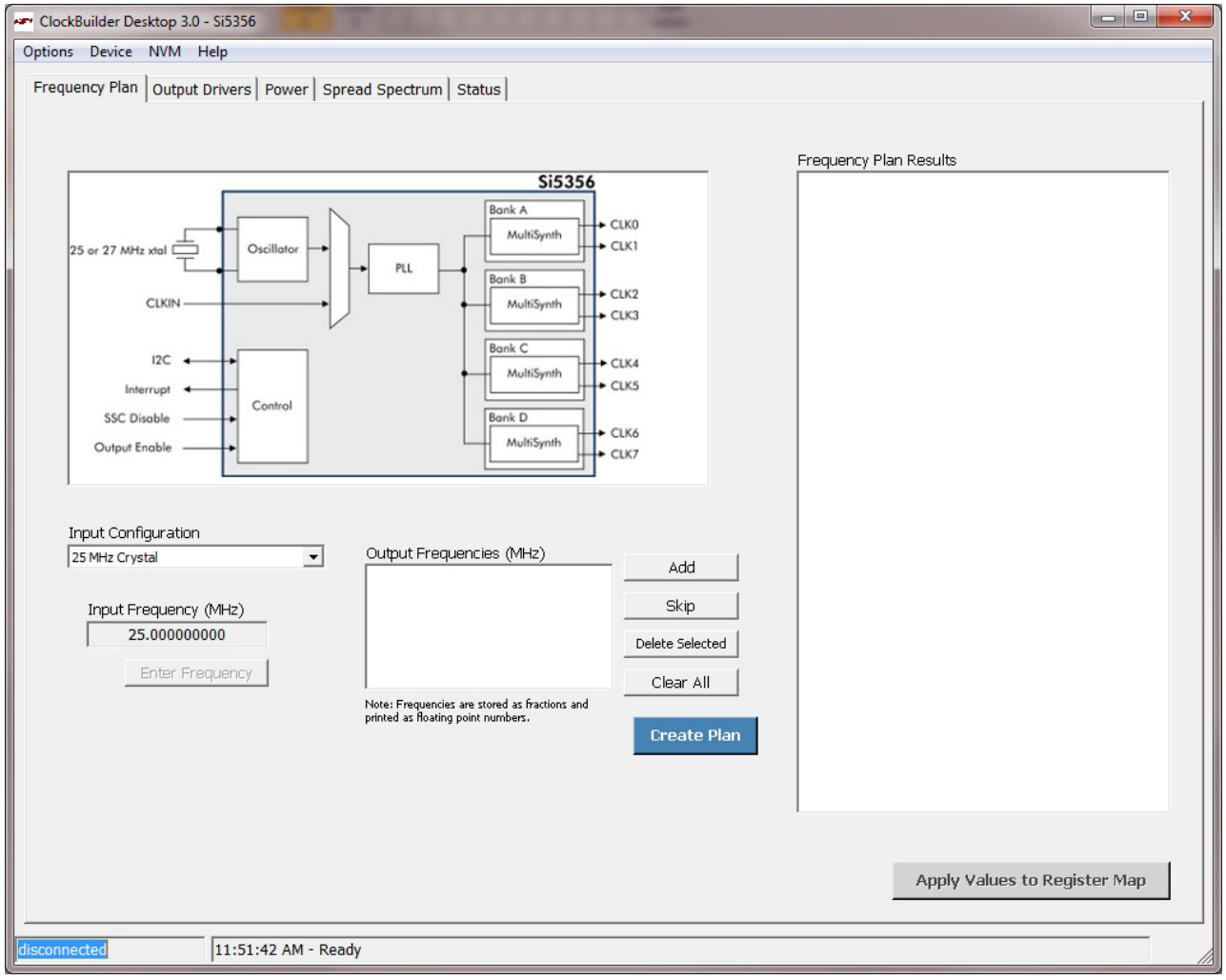


Figure 2. ClockBuilder Desktop Frequency Plan Tab

If CMOS Clock is selected, click Enter Frequency to specify the input frequency. The input frequency can be specified in decimal form, as a fraction, or as a frequency times a ratio.

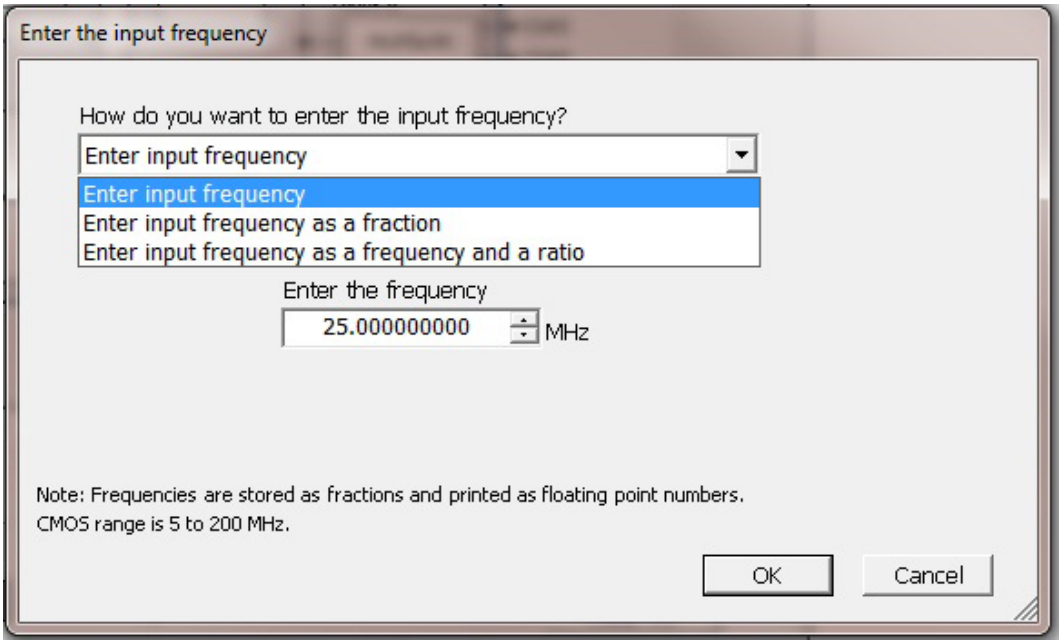


Figure 3. Enter Input Frequency in ClockBuilder Desktop

Valid output frequencies are 1–200 MHz and can be specified in decimal or fraction form, as a frequency times a ratio, or in relation to CLKIN or any other output frequency. Click Add to enter output frequency.

Once the input and all output frequencies have been entered, click Create Plan. This will display a summary of the frequency plan including all frequencies and feedback and output Multisynth divide ratios. Click the Apply Values to Register Map button.

2.2. Setting up the Output Driver

The Output Driver tab allows the user to modify all the settings associated with the output drivers. For each bank of clocks, the following settings can be controlled:

- Output Voltage and Format—used to specify the outputs on each clock bank that are enabled and the output voltage for each bank.
- Output State when Disabled—used to specify state of the outputs when either the OEB pin or the appropriate bit in register 230 is asserted.
- Driver Inversion—used to specify the outputs, if any, on each clock bank that is inverted (180° out of phase).
- Initial Phase Offset—used to specify a static time delay with respect to other outputs.

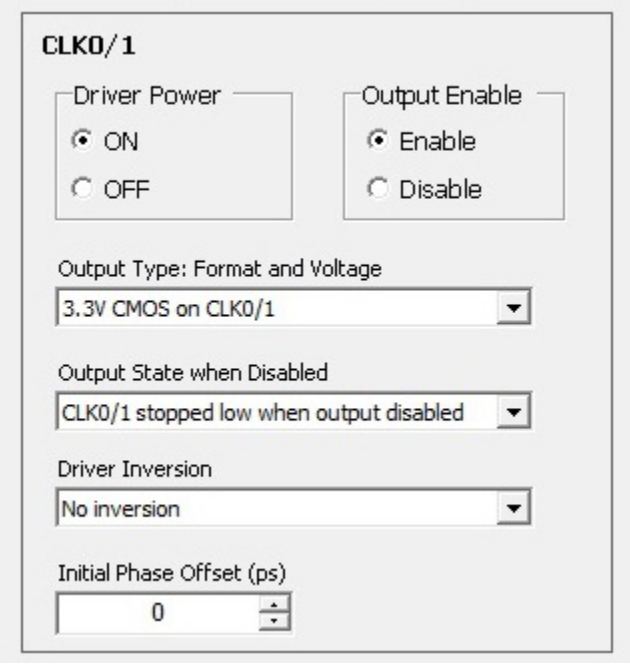


Figure 4. Output Driver Settings in ClockBuilder Desktop

After any changes have been made to this tab, click Apply Values to Register Map.

2.3. Setting up Spread Spectrum

The Spread Spectrum tab allows the user to enable spread spectrum on each Multisynth block if desired. Enter the desired spread profile, amplitude, and modulation rate for each of the Multisynth blocks, and click Apply Values to Register Map.

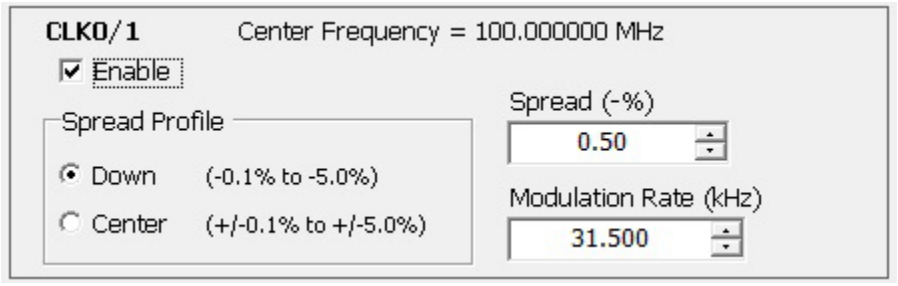


Figure 5. Spread Spectrum Settings in ClockBuilder Desktop

The Si5356 supports spread spectrum under the following conditions:

1. MultiSynth output frequencies between 5 MHz and 200 MHz
2. Spreading rates from 31.5 to 63 kHz
3. Down spread from 0.1 to 5% in 0.01% steps
4. Center spread from ±0.1 to ±5.0 % in .01% steps

If your spread spectrum requirements are outside of these parameters, contact Silicon Labs.

3. Overview of Configuring the Si5356A without ClockBuilder Desktop

In order to replicate the functionality of the ClockBuilder Desktop, a full register map must be created for all desired features. To create the register map, the programmer must perform the following steps:

1. Configure the Input Clock & PLL.
   - See Section "4.1. Configuring Reference Input" on page 8.
   - See Section "4.2. Configuring PLL Parameters" on page 10.
2. Determine the divider values for the desired output frequencies.
   - See Section "4.3. Configuring the Output Frequency Plan" on page 12.
3. Configure the output drivers
   - See Section "5. Configuring the Output Drivers" on page 13.
4. Configure spread spectrum (if needed).
   - See Section "6. Configuring Spread Spectrum" on page 19.
5. Assemble the register map.
   - See Section "7. Si5356A Registers" on page 21.

When fully assembled, continue with the writing procedure outlined in the Si5356 device data sheet.

4. Configuring the Frequency Plan

4.1. Configuring Reference Input

The Si5356A is capable of locking to a single-ended clock or an external crystal resonator. A crystal allows the device to generate a free-running clock, whereas the part can synchronize to an external CMOS clock using the CLKIN pin. A block diagram of the input configuration is shown in Figure 6.

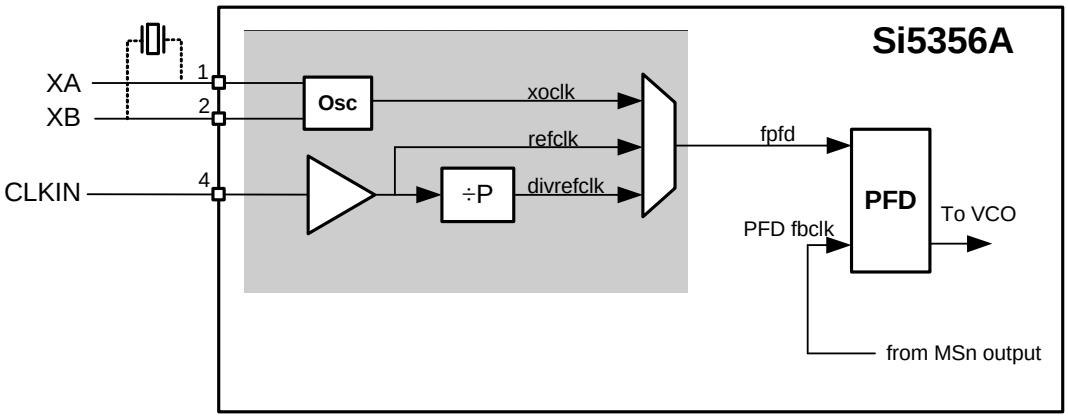
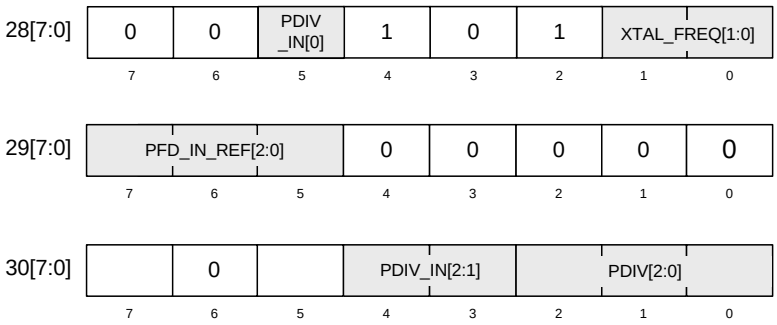


Figure 6. Si5356A Input Selection Block Diagram

The reference frequency to the PFD, fpfd, must be kept between 5 and 40MHz. When using a CMOS clock on CLKIN greater than 40 MHz, the P divider must be used.

The register settings for setting up the reference source are given in Figure 7.



Reference Clock (fpfd)	PFD_IN_REF[2:0]	PDIV_IN[2:0]
xoclk*	100	000 or 001
5MHz > CLKIN ≥ 40MHz (refclk)	001	011
CLKIN > 40MHz (divrefclk)**	111	011

* If xoclk is selected XTAL_FREQ must be set; otherwise it is a don't care.
** If divrefclk is selected PDIV must be set such that divrefclk is in the range of 5 to 40MHz; otherwise PDIV[2:0] = 000.

Crystal Frequency	XTAL_FREQ[1:0]
27MHz	11
25MHz	10

P divider setting	PDIV[2:0]
÷1	000
÷2	001
÷4	010
÷8	011
÷16	100
÷32	101

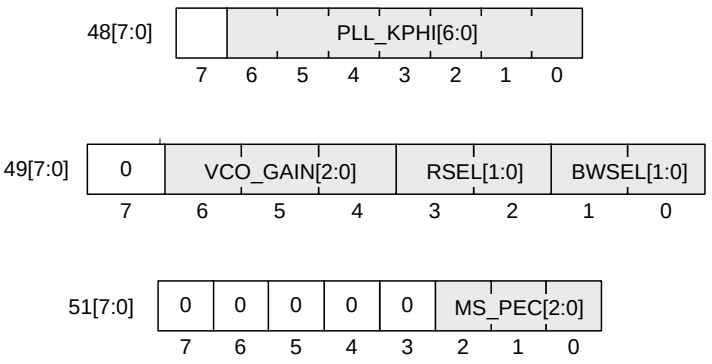
Figure 7. Reference Clock Configuration Registers

4.2. Configuring PLL Parameters

When the input source has been selected and the input frequency known, PLL parameters and feedback divider ratio must be calculated and set.

4.2.1. PLL Parameters

The PLL parameters PLL_Kphi, VCO_GAIN, RSEL, BWSEL and MS_PEC must be set according to Figure 8.



f_{pfd}	K	RSEL[1:0]	BWSEL[1:0]
f_{pfd} >= 15 MHz	925	00	00
8 MHz <= f_{pfd} < 15 MHz	325	01	01
5 MHz <= f_{pfd} < 8 MHz	185	11	10

$$PLL\_KPHI[6:0] = \text{Round}\left(\frac{1.51 \times K}{f_{pfd\ (MHz)}}\right)$$

MS_PEC[2:0] = 111
VCO_GAIN[2:0] = 001

Figure 8. Setting the PLL Parameters

4.2.2. Feedback Multisynth

Once f_{pfd} is known (see "4.1. Configuring Reference Input" on page 8), the feedback Multisynth divider must be configured.

$$MSN\_P1 = Floor\left(\frac{281{,}600}{f_{pfd}*}\right) - 512$$

$$MSN\_P2 = Floor\left(10^9 * \left(\frac{281{,}600}{f_{pfd}*} - MSN\_P1 - 512\right)\right)$$

$$MSN\_P3 = 10^9 \text{ (decimal)}$$

*where f_{pfd} is in MHz; f_{pfd} must be between 5 and 40 MHz

Figure 9. Feedback Multisynth Calculations

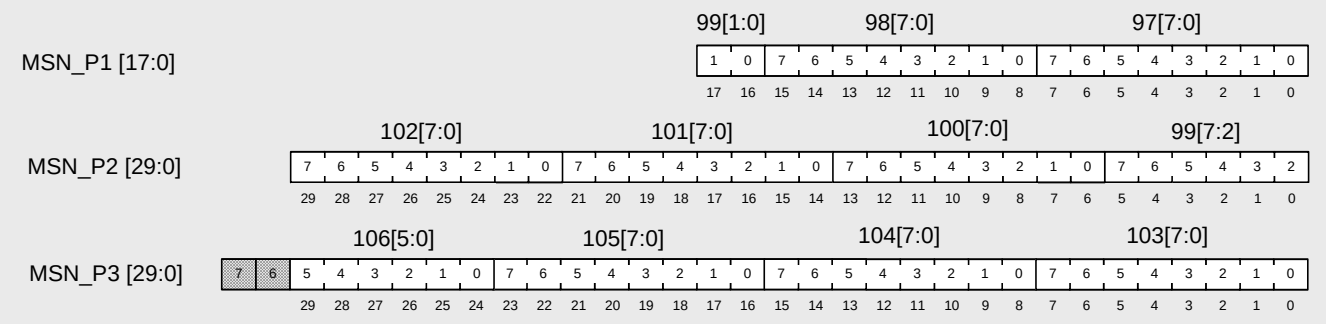
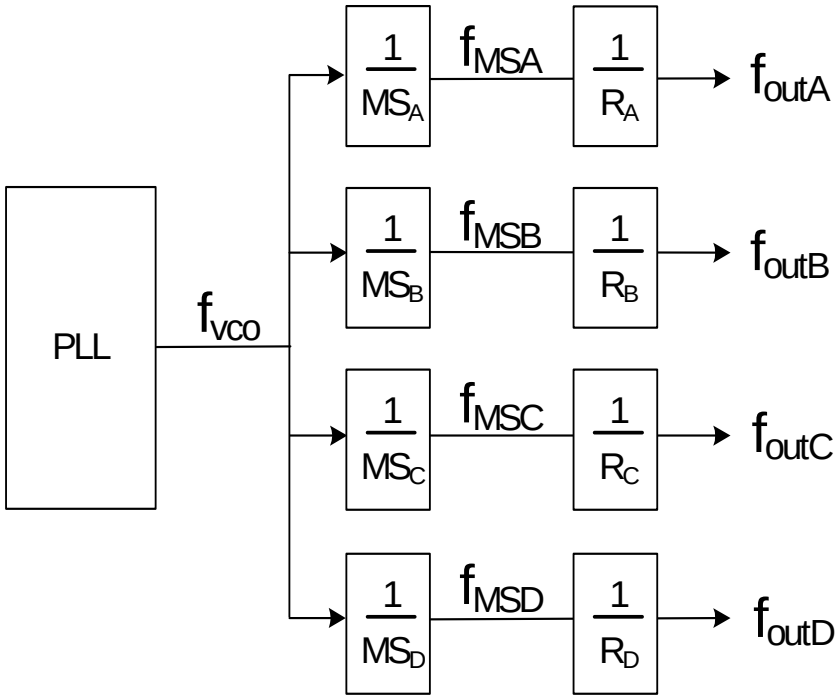


Figure 10. Feedback Multisynth Registers

4.3. Configuring the Output Frequency Plan



$$MS_x\_P1 = \text{Floor}\left(\frac{281{,}600}{f_{MSx}^*}\right) - 512$$

$$MS_x\_P2 = \text{Floor}\left(10^9 * \left(\frac{281{,}600}{f_{MSx}^*} - MS_x\_P1 - 512\right)\right)$$

$$MS_x\_P3 = 10^9 \text{ (decimal)}$$

* f_{MSx} is the Multisynth output frequency in MHz, and must be between 5 and 200 MHz. To generate f_{out} < 5MHz, R dividers must be used, see Sec 5.7. Output Clock Select.

Figure 11. Output Multisynth Registers

5. Configuring the Output Drivers

5.1. Output Driver Powerup/Powerdown

The device allows powering down unused output clocks (CLK_n) to save on overall power consumption. Register 31[0] controls this function for CLK0, 32[0] controls CLK1, 33[0] controls CLK1, and 34[0] controls CLK1. Setting the register bit to 0 enables power to the CLK output; setting it to 1 powers it down. The default value is set to 0.

5.2. Output Driver Enable/Disable

Each of the output drivers can be enabled or disabled once they have been powered up as described in Section 5.1. Register 230 controls this function as shown in Figure 12. Drivers are enabled by default. Register 230[4] disables/enables all outputs simultaneously, and, when disabled, overrides the effect of OEB_0,1,2,3. Set each OEB_x to 0 to enable.

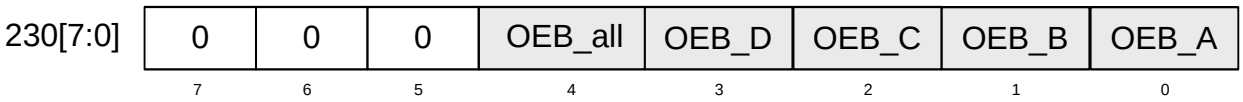
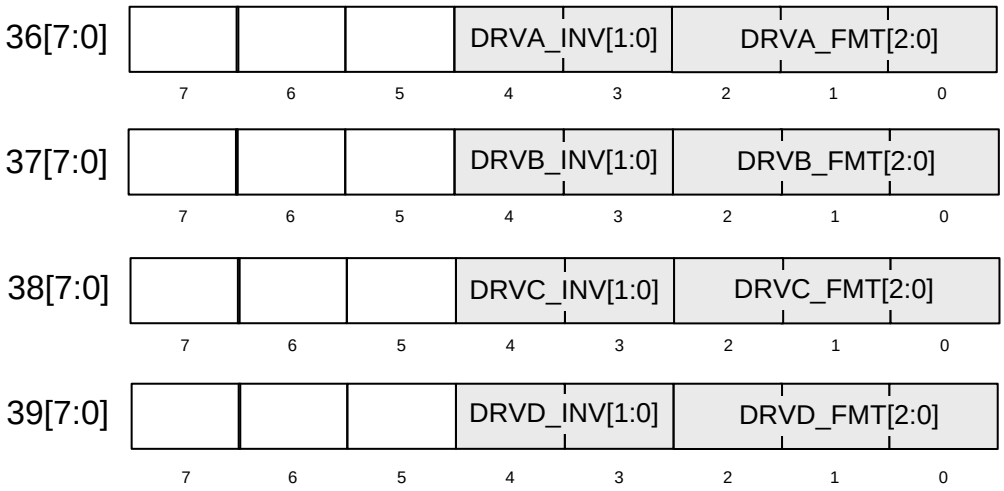


Figure 12. Setting Output Driver Enable/Disable

5.3. Output Signal Format and Inversion

Each of the 8 output clocks can be individually enabled and inverted. Registers 36-39 control this feature as shown in Figure 13. Register 36 controls the clocks on Driver A, register 37 the clocks on Driver B, and so on.



Output Signal Format	DRVx_FMT x=A,B,C,D
Reserved	000
Even clock = on; Odd clock = off	001
Even clock = off; Odd clock = on	010
Even clock = on; Odd clock = on	011

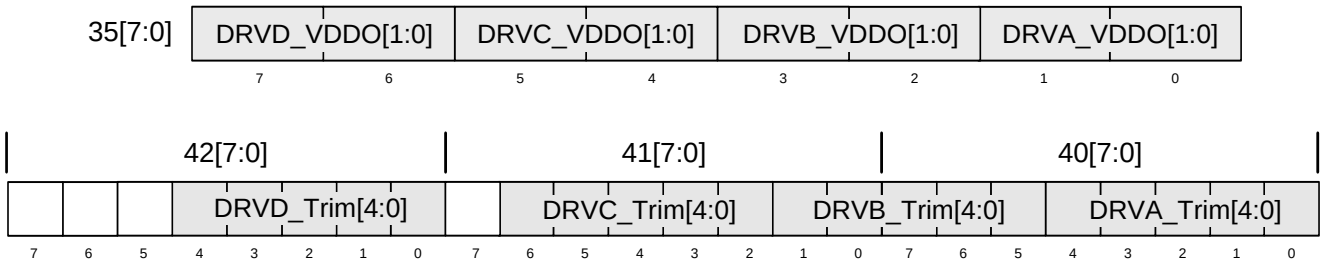
Inversion	DRVx_INV[1:0] x=A,B,C,D
No inversion	00
Invert even clock	01
Invert odd Clock	10
Invert both clocks	11

Figure 13. Setting Output Signal Format and Inversion

5.4. Output Voltage and Trim

Each of the output drivers can operate from independent VDDO supplies at 3.3, 2.5, or 1.8 V. Registers 35 and 40-42 must be written according to Figure 14.

Note: The actual VDDOx supply voltage at the pin needs to agree to within 10% of the associate register settings.



VDDO Supply Voltage	DRVx_VDDO[1:0] x=A,B,C,D	DRVx_Trim[4:0] x=A,B,C,D
3.3V	00	10111
2.5V	01	10011
1.8V	10	10101

Figure 14. Setting Output Driver Supply Voltage

5.5. Output Driver State when Disabled

When an output is disabled, its state is configurable as Hi-Z, Low, High, or Always On. Registers 110[7:6], 114[7:6], 118[7:6], and 122[7:6] control this feature as shown in Figure 15.

Driver State When Disabled	CLKx_DISST[1:0] x=A,B,C,D
Hi-Z	00
Disables Low	01
Disables High	10

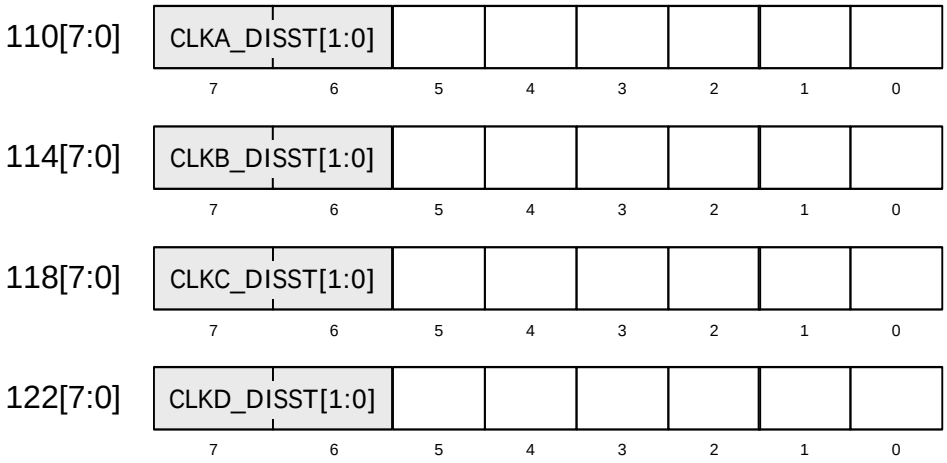


Figure 15. Setting Output Drive State

5.6. Configuring Initial Phase Offset

Each clock bank of the Si5356A can be programmed with an independent initial phase offset. The phase offset is represented as a 2s complement integer and is calculated as follows:

$$MSx\_PHOFF = ROUND\ [0.2816 \times Offset_{ps}]$$

If a negative value is required, PHOFF must be converted to a 2s complement number. The initial phase offset adjustment has a range of ±45 ns. A soft reset must be applied for the phase offset values to take effect.

5.7. Output Clock Select

The source of each output driver can be selected as shown in Figure 16. The Si5356 allows each driver to output any of the synthesized clocks (MSx) or to bypass the PLL completely and output any of the input clocks directly. The output clock select register settings are shown in Figure 17.

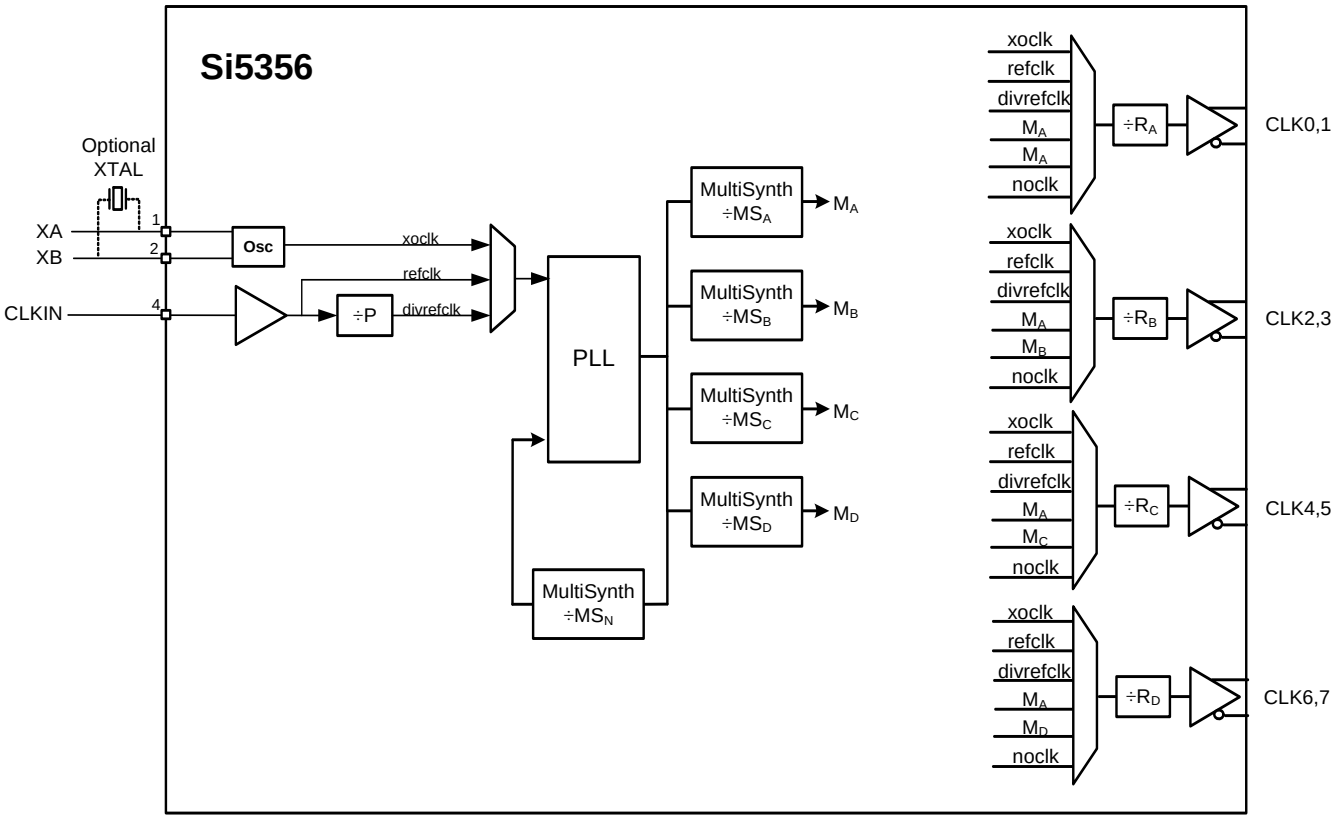
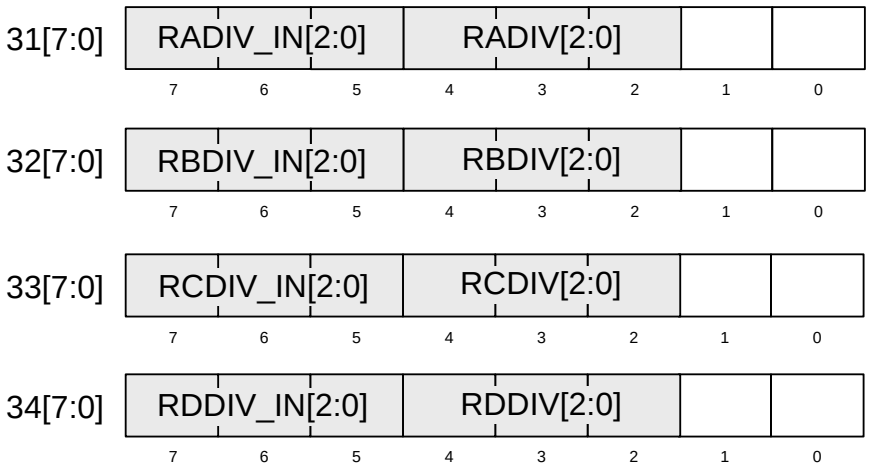


Figure 16. Output Clock Diagram



Selected Source	RxDIV_IN[2:0] x=A,B,C,D
refclk	000
divrefclk	010
xoclk	100
M_A*	101
M_x	110
No clock	111

* To select this output, Multisynth A fanout must be enabled in reg 144[7].
** 001/011 are invalid values.

Output Divider Value	RxDIV[2:0] x=A,B,C,D
1	000
2	001
4	010
8	011
16	100
32	101
Reserved	110
Reserved	111

Figure 17. Selecting Output Clocks

The output Multisynth dividers (Mx) can generate any frequency from 5 to 200 MHz. The output clock dividers (RX) allow a final stage of division to generate output clocks < 5 MHz. This division ratio is configurable using registers 31–34 as shown in Figure 17 above. When using a division value other than 1, the outputs may not be in phase.

6. Configuring Spread Spectrum

Spread spectrum is available on each of the clock outputs. The device can be set up in down or center spread mode. The Si5356A supports spread spectrum under the following conditions:

1. MultiSynth output frequencies ≥ 5 MHz and 200 MHz.
2. Spreading rates from 31.5 to 63 kHz.
3. Down spread from 0.1 to 5% in 0.01% steps..
4. Center spread from ±0.1 to ±2.5% in .01% steps".

If your spread spectrum requirements are outside of these parameters, contact Silicon Labs.

6.1. Down Spread

To configure down spread, use the Equation 1.

Up/Down Parameter:

$$MSx\_SSUDP1 = Floor\left(\frac{F_{out}}{4 * sscFreq}\right)$$

where
Fout = MultiSynthx output frequency in Hz
sscFreq = spreading frequency in Hz

Down Parameters:

Let x and y be defined as:

x = Floor(1e12*(64 * sscAmp * (a + b/c)))
y = Floor(1e12*(1 – sscAmp) * MSx_SSUDP1)

where
sscAmp = spread amplitude (e.g, for 1.3 % down spread, sscAmp = .013)
a +b/c is the MultiSynth divider ratio from section 5

$$MSx\_SSDNP1 = Floor\left(\frac{x}{y}\right)$$

$$MSx\_SSDNP2 = \frac{Mod(x,y)}{GCD\ (x, y)}$$

GCD (x,y) returns the greatest common denominator of x and y
Mod(x,y) returns the remainder of x/y

$$MSx\_SSDNP3 = \frac{y}{GCD\ (x, y)}$$

Up Parameters:

MSx_SSUPP1 = 0

MSx_SSUPP2 = 0

MSx_SSUPP3 = 1

Equation 1. SSC Down-Spread Equations

6.2. Center Spread

Rev B devices do not provide native support for center-spread clocking. Center-spread clocks must be implemented as modified down-spread clocks. For example, to implement 100 MHz ±1% on CLKx, you must modify the associated Multisynth and R dividers to output 101 MHz (see "4.3. Configuring the Output Frequency Plan" on page 12) and configure the device for 2% down-spread according to the equations in "6.1. Down Spread". Note that ClockBuilder Desktop 6.0 (or later) takes care of configuring the registers properly for center spread operation on rev B devices.

6.2.1. Center Spread Equations for Rev A Devices

The part can be configured for this mode using Equation 2.

Up/Down Parameter:

$$MSx\_SSUDP1 = \text{Floor}\left(\frac{F_{out}}{4 * sscFreq}\right)$$

where
Fout = MultiSynthx output frequency in Hz
sscFreq = spreading frequency in Hz

Down Parameters:

Let x and y_{down} be defined as:

$x = \text{Floor}(1e12*(128 * sscAmp * (a + b/c)))$
$y_{down} = \text{Floor}(1e12*(1 – sscAmp) * MSx\_SSUDP1)$

where
sscAmp = spread amplitude (e.g, for +/-1.3 % center spread, sscAmp = .013) a +b/c is the MultiSynth divider ratio from section 5

$$MSx\_SSDNP1 = \text{Floor}\left(\frac{x}{y_{down}}\right)$$

$$MSx\_SSDNP2 = \frac{\text{Mod}(x,y_{down})}{\text{GCD}(x, y_{down})}$$

$$MSx\_SSDNP3 = \frac{y_{down}}{\text{GCD}(x, y_{down})}$$

Up Parameters:

Let y_{up} be defined as:

$y_{up} = \text{Floor}(1e12*(1 + sscAmp) * MSx\_SSUDP1)$

$$MSx\_SSUPP1 = \text{Floor}\left(\frac{x}{y_{up}}\right)$$

$$MSx\_SSUPP2 = \frac{\text{Mod}(x,y_{up})}{\text{GCD}(x, y_{up})}$$

$$MSx\_SSUPP3 = \frac{y_{up}}{\text{GCD}(x, y_{up})}$$

Equation 2. SSC Center-Spread Equations

7. Si5356A Registers

This section describes the registers and their usage in detail. These values are easily configured using ClockBuilder Desktop. See “AN428: Jump Start: In-System, Flash-Based Programming for Silicon Labs’ Timing Products” for a working example using Silicon Labs' F301 MCU.

7.1. Assembling the Si5338 Register Map

When all of the desired features have been configured, the values should be collected into a single list in order to write to the device. Collect register values for the required registers:

1. All MultiSynth, N, and R divider ratios.
2. PLL parameters.
3. Output driver parameters and output mux.
4. Input mux.
5. Miscellaneous register values.
6. Any additional/optional features:
   - Initial phase offset
   - Spread spectrum

When the full register map is established, continue with the write procedure as outlined in the device data sheet.

7.2. Miscellaneous Register Writes

The following register bits must also be written to ensure proper device functionality.

- Register 47[5:2] = 0101b
- Register 241 = 0x65
- Register 106[7] = 1b
- Register 116[7] = 1b
- Register 42[5] = 1b
- Register 6[7:5] = 000b
- Register 6[1] = 0b
- Register 28[7:6] = 00b

7.3. Register Write-Allowed Mask

The masks listed in Table 1 indicate which bits in each register of the Si5356 can be modified and which bits cannot. Therefore, these masks are write-allowed or write-enabled bits. These masks must be used to perform a read-modify-write on each register.

If a mask is 0x00, all bits in the associated register are reserved and must remain unchanged. If the mask is 0xFF, all the bits in the register can be changed. All other registers require a read-modify-write procedure to write to the registers. ClockBuilder Desktop can be used to create ANSI C code (Options → Save C code header file) with the register contents and mask values. “AN428: Jump Start: In-System, Flash-based Programming for Silicon Labs’ Timing Products” demonstrates the usage of this header file and the read-modify-write procedure.

The following code demonstrates the application of the above write allowed mask.

- Let addr be the address of the register to access.
- Let data be the data or value to write to the register located at addr.
- Let mask be the write-allowed bits defined for the corresponding register.

```
// ignore registers with masks of 0x00
if(mask != 0x00){

        if(mask == 0xFF){
                // do a regular I2C write to the register
                // at addr with the desired data value
                write_Si5356(addr, data);

        } else {
                // do a read-modify-write using I2C and
                // bit-wise operations

                // get the current value from the device at the
                // register located at addr
                curr_val = read_Si5356(addr);

                // clear the bits that are allowed to be
                // accessed in the current value of the register
                clear_curr_val = curr_val AND (NOT mask);

                // clear the bits in the desired data that
                // are not allowed to be accessed
                clear_new_val = data AND mask;

                // combine the cleared values to get the new
                // value to write to the desired register
                combined = clear_curr_val OR clear_new_val;

                write_Si5356(addr, combined);
        }

}
```

Table 1. Register Write-Allowed Masks

Address (Decimal)	Mask (Hex)
0	0x00
1	0x00
2	0x00
3	0x00
4	0x00
5	0x00
6	0x1D
7	0x00
8	0x00
9	0x00
10	0x00
11	0x00
12	0x00
13	0x00
14	0x00
15	0x00
16	0x00
17	0x00
18	0x00
19	0x00
20	0x00
21	0x00
22	0x00
23	0x00
24	0x00
25	0x00
26	0x00
27	0x80
28	0xFF
29	0xFF
30	0xFF
31	0xFF
***Note:** These registers are not saved in the register map or C code header file from the ClockBuilder Desktop. Refer to the I^2C programming procedure provided in the Si5356 datasheet for more details.	

Table 1. Register Write-Allowed Masks

Address (Decimal)	Mask (Hex)
32	0xFF
33	0xFF
34	0xFF
35	0xFF
36	0x1F
37	0x1F
38	0x1F
39	0x1F
40	0xFF
41	0x7F
42	0x3F
43	0x00
44	0x00
45	0x00
46	0x00
47	0x3C
48	0x7F
49	0x7F
50	0xC0
51	0x00
52	0x0C
53	0xFF
54	0xFF
55	0xFF
56	0xFF
57	0xFF
58	0xFF
59	0xFF
60	0xFF
61	0xFF
62	0x3F
63	0x0C
64	0xFF
***Note:** These registers are not saved in the register map or C code header file from the ClockBuilder Desktop. Refer to the I^2C programming procedure provided in the Si5356 datasheet for more details.	

Table 1. Register Write-Allowed Masks

Address (Decimal)	Mask (Hex)
65	0xFF
66	0xFF
67	0xFF
68	0xFF
69	0xFF
70	0xFF
71	0xFF
72	0xFF
73	0x3F
74	0x0C
75	0xFF
76	0xFF
77	0xFF
78	0xFF
79	0xFF
80	0xFF
81	0xFF
82	0xFF
83	0xFF
84	0x3F
85	0x0C
86	0xFF
87	0xFF
88	0xFF
89	0xFF
90	0xFF
91	0xFF
92	0xFF
93	0xFF
94	0xFF
95	0x3F
96	0x00
97	0xFF

***Note:** These registers are not saved in the register map or C code header file from the ClockBuilder Desktop. Refer to the I^2C programming procedure provided in the Si5356 datasheet for more details.

Table 1. Register Write-Allowed Masks

Address (Decimal)	Mask (Hex)
98	0xFF
99	0xFF
100	0xFF
101	0xFF
102	0xFF
103	0xFF
104	0xFF
105	0xFF
106	0x3F
107	0xFF
108	0x7F
109	0x00
110	0xC0
111	0xFF
112	0x7F
113	0x00
114	0xC0
115	0xFF
116	0x7F
117	0x00
118	0xC0
119	0xFF
120	0xFF
121	0x00
122	0xC0
123	0x00
124	0x00
125	0x00
126	0x00
127	0x00
128	0x00
129	0x0F
130	0x0F
***Note:** These registers are not saved in the register map or C code header file from the ClockBuilder Desktop. Refer to the I^2C programming procedure provided in the Si5356 datasheet for more details.	

Table 1. Register Write-Allowed Masks

Address (Decimal)	Mask (Hex)
131	0x00
132	0x00
133	0x00
134	0x00
135	0x00
136	0x00
137	0x00
138	0x00
139	0x00
140	0x00
141	0x00
142	0x00
143	0x00
144	0x80
145	0x00
146	0x00
147	0x00
148	0x00
149	0x00
150	0x00
151	0x00
152	0x00
153	0x00
154	0x00
155	0x00
156	0x00
157	0x00
158	0x0F
159	0x0F
160	0x00
161	0x00
162	0x00
163	0x00
***Note:** These registers are not saved in the register map or C code header file from the ClockBuilder Desktop. Refer to the I^2C programming procedure provided in the Si5356 datasheet for more details.	

Table 1. Register Write-Allowed Masks

Address (Decimal)	Mask (Hex)
164	0x00
165	0x00
166	0x00
167	0x00
168	0x00
169	0x00
170	0x00
171	0x00
172	0x00
173	0x00
174	0x00
175	0x00
176	0x00
177	0x00
178	0x00
179	0x00
180	0x00
181	0x0F
182	0x00
183	0x00
184	0x00
185	0x00
186	0x00
187	0x00
188	0x00
189	0x00
190	0x00
191	0x00
192	0x00
193	0x00
194	0x00
195	0x00
196	0x00
***Note:** These registers are not saved in the register map or C code header file from the ClockBuilder Desktop. Refer to the I^2C programming procedure provided in the Si5356 datasheet for more details.	

Table 1. Register Write-Allowed Masks

Address (Decimal)	Mask (Hex)
197	0x00
198	0x00
199	0x00
200	0x00
201	0x00
202	0x00
203	0x0F
204	0x00
205	0x00
206	0x00
207	0x00
208	0x00
209	0x00
210	0x00
211	0x00
212	0x00
213	0x00
214	0x00
215	0x00
216	0x00
217	0x00
218	0x00
219	0x00
220	0x00
221	0x00
222	0x00
223	0x00
224	0x00
225	0x00
226	0x00
227	0x00
228	0x00
229	0x00
***Note:** These registers are not saved in the register map or C code header file from the ClockBuilder Desktop. Refer to the I^2C programming procedure provided in the Si5356 datasheet for more details.	

Table 1. Register Write-Allowed Masks

Address (Decimal)	Mask (Hex)
230*	0xFF
231	0x00
232	0x00
233	0x00
234	0x00
235	0x00
236	0x00
237	0x00
238	0x00
239	0x00
240	0x00
241*	0xFF
242	0x00
243	0x00
244	0x00
245	0x00
246*	0xFF
247	0x00
248	0x00
249	0x00
250	0x00
251	0x00
252	0x00
253	0x00
254	0x00
255	0xFF
256	0x00
257	0x00
258	0x00
259	0x00
260	0x00
261	0x00
262	0x00

***Note:** These registers are not saved in the register map or C code header file from the ClockBuilder Desktop. Refer to the I^2C programming procedure provided in the Si5356 datasheet for more details.

Table 1. Register Write-Allowed Masks

Address (Decimal)	Mask (Hex)
263	0x00
264	0x00
265	0x00
266	0x00
267	0x00
268	0x00
269	0x00
270	0x00
271	0x00
272	0x00
273	0x00
274	0x00
275	0x00
276	0x00
277	0x00
278	0x00
279	0x00
280	0x00
281	0x00
282	0x00
283	0x00
284	0x00
285	0x00
286	0x00
287	0xFF
288	0xFF
289	0xFF
290	0xFF
291	0xFF
292	0xFF
293	0xFF
294	0xFF
295	0xFF
***Note:** These registers are not saved in the register map or C code header file from the ClockBuilder Desktop. Refer to the I^2C programming procedure provided in the Si5356 datasheet for more details.	

Table 1. Register Write-Allowed Masks

Address (Decimal)	Mask (Hex)
296	0xFF
297	0xFF
298	0xFF
299	0x0F
300	0x00
301	0x00
302	0x00
303	0xFF
304	0xFF
305	0xFF
306	0xFF
307	0xFF
308	0xFF
309	0xFF
310	0xFF
311	0xFF
312	0xFF
313	0xFF
314	0xFF
315	0x0F
316	0x00
317	0x00
318	0x00
319	0xFF
320	0xFF
321	0xFF
322	0xFF
323	0xFF
324	0xFF
325	0xFF
326	0xFF
327	0xFF
328	0xFF
***Note:** These registers are not saved in the register map or C code header file from the ClockBuilder Desktop. Refer to the I^2C programming procedure provided in the Si5356 datasheet for more details.	

Table 1. Register Write-Allowed Masks

Address (Decimal)	Mask (Hex)
329	0xFF
330	0xFF
331	0x0F
332	0x00
333	0x00
334	0x00
335	0xFF
336	0xFF
337	0xFF
338	0xFF
339	0xFF
340	0xFF
341	0xFF
342	0xFF
343	0xFF
344	0xFF
345	0xFF
346	0xFF
347	0x0F
348	0x00
349	0x00
350	0x00
***Note:** These registers are not saved in the register map or C code header file from the ClockBuilder Desktop. Refer to the I^2C programming procedure provided in the Si5356 datasheet for more details.	

7.4. Register Categories

This is a list of registers needed to define the Configuration of a device. Set the PAGEBIT to access registers with addresses greater than 255.

Address (Decimal)	Bits	Function
6	4:0	Mask bits for LOS_CLKIN,LOS_FB, LOL, SYS_CAL
27	7:6	I^2C Configuration
27	7	
28–30	7:0	Input Mux Configuration
31–39	7:0	Output Configuration
40	7:0	Output Driver Trim Bits
41	6:0	
42	4:0	
47	5:2	Input Configuration
48	7:0	PLL Configuration
49	6:0	
50	7:0	
51	2:0	
52	6:0	MultiSynth A Frequency Configuration
53–61	7:0	
62	5:0	
63	6:0	MultiSynth B Frequency Configuration
64–72	7:0	
73	5:0	
74	6:0	MultiSynth C Frequency Configuration
75–83	7:0	
84	5:0	
85	6:0	MultiSynth D Frequency Configuration
86–94	7:0	
95	5:0	
97–105	7:0	MultiSynth N Feedback divider Configuration
106	5:0	
107	7:0	MultiSynth A Phase Offset
108	6:0	
110	7:6	MultiSynth A Disable State
111	7:0	MultiSynth B Phase Offset
112	6:0	

Address (Decimal)	Bits	Function
114	7:6	MultiSynth B Disable State
115	7:0	MultiSynth C Phase Offset
116	6:0	
118	7:6	MultiSynth C Disable State
119	7:0	MultiSynth D Phase Offset
120	6:0	
122	7:6	MultiSynth D Disable State
144	7	MultiSynth A Fanout Enable
241	7:0	Reserved—set to 0x65 if not factory-programmed.
287	7:0	MultiSynth A spread spectrum Configuration
288	6:0	
289	7:0	
290	6:0	
291	7:0	
292	7:0	
293	7:0	
294	7:0	
295	6:0	
296	7:0	
297	6:0	
298	7:0	
299	7:0	
303	7:0	MultiSynth B spread spectrum Configuration
304	6:0	
305	7:0	
306	6:0	
307	7:0	
308	7:0	
309	7:0	
310	7:0	
311	6:0	
312	7:0	
313	6:0	
314	7:0	
315	7:0	

Address (Decimal)	Bits	Function
319	7:0	MultiSynth C spread spectrum Configuration
320	6:0	
321	7:0	
322	6:0	
323	7:0	
324	7:0	
325	7:0	
326	7:0	
327	6:0	
328	7:0	
329	6:0	
330	7:0	
331	7:0	
335	7:0	MultiSynth D spread spectrum Configuration
336	6:0	
337	7:0	
338	6:0	
339	7:0	
340	7:0	
341	7:0	
342	7:0	
343	6:0	
344	7:0	
345	6:0	
346	7:0	
347	7:0	

7.5. Register Summary

Table 2. Register Summary

Register	7	6	5	4	3	2	1	0
0						REVID[2:0]		
6				PLL_LOL_MASK	LOS_-CLKIN_MASK	LOS_X-TAL_MASK		SYS_CAL_MASK
27	I2C_1P8_-SEL	I2C_ADDR[6:0]						
28	FDBK_PDN		PDIV_IN[0]				XTAL_FREQ[1:0]	
29	PFD_IN_REF[2:0]							
30				PDIV_IN[2:1]		PDIV[2:0]		
31	RADIV_IN[2:0]			RADIV[2:0]			MSA_PDN	DRVA_PDN
32	RBDIV_IN[2:0]			RBDIV[2:0]			MSB_PDN	DRVB_PDN
33	RCDIV_IN[2:0]			RCDIV[2:0]			MSC_PDN	DRVC_PDN
34	RDDIV_IN[2:0]			RDDIV[2:0]			MSD_PDN	DRVD_PDN
35	DRVD_VDDO[1:0]		DRVC_VDDO[1:0]		DRVB_VDDO[1:0]		DRVA_VDDO[1:0]	
36				DRVA_INV[1:0]		DRVA_FMT[2:0]		
37				DRVB_INV[1:0]		DRVB_FMT[2:0]		
38				DRVC_INV[1:0]		DRVC_FMT[2:0]		
39				DRVD_INV[1:0]		DRVD_FMT[2:0]		
40	DRVB_TRIM[2:0]			DRVA_TRIM[4:0]				
41		DRVC_TRIM[4:0]					DRVB_TRIM[4:3]	
42				DRVD_TRIM[4:0]				
48		PLL_KPHI[6:0]						
49		VCO_GAIN[2:0]			RSEL[1:0]		BWSEL[1:0]	
50	PLL_ENABLE[1:0]							
51						MS_PEC[2:0]		
53	MSA_P1[7:0]							
54	MSA_P1[15:8]							
55	MSA_P2[5:0]						MSA_P1[17:16]	
56	MSA_P2[13:6]							
57	MSA_P2[21:14]							
58	MSA_P2[29:22]							
59	MSA_P3[7:0]							
60	MSA_P3[15:8]							

Table 2. Register Summary (Continued)

Register	7	6	5	4	3	2	1	0
61	MSA_P3[23:16]							
62			MSA_P3[29:24]					
64	MSB_P1[7:0]							
65	MSB_P1[15:8]							
66	MSB_P2[5:0]						MSB_P1[17:16]	
67	MSB_P2[13:6]							
68	MSB_P2[21:14]							
69	MSB_P2[29:22]							
70	MSB_P3[7:0]							
71	MSB_P3[15:8]							
72	MSB_P3[23:16]							
73			MSB_P3[29:24]					
75	MSC_P1[7:0]							
76	MSC_P1[15:8]							
77	MSC_P2[5:0]						MSC_P1[17:16]	
78	MSC_P2[13:6]							
79	MSC_P2[21:14]							
80	MSC_P2[29:22]							
81	MSC_P3[7:0]							
82	MSC_P3[15:8]							
83	MSC_P3[23:16]							
84			MSC_P3[29:24]					
86	MSD_P1[7:0]							
87	MSD_P1[15:8]							
88	MSD_P2[5:0]						MSD_P1[17:16]	
89	MSD_P2[13:6]							
90	MSD_P2[21:14]							
91	MSD_P2[29:22]							
92	MSD_P3[7:0]							
93	MSD_P3[15:8]							
94	MSD_P3[23:16]							
95			MSD_P3[29:24]					
97	MSN_P1[7:0]							
98	MSN_P1[15:8]							

Table 2. Register Summary (Continued)

Register	7	6	5	4	3	2	1	0
99	MSN_P2[5:0]						MSN_P1[17:16]	
100	MSN_P2[13:6]							
101	MSN_P2[21:14]							
102	MSN_P2[29:22]							
103	MSN_P3[7:0]							
104	MSN_P3[15:8]							
105	MSN_P3[23:16]							
106			MSN_P3[29:24]					
107	MSA_PHOFF[7:0]							
108		MSA_PHOFF[14:8]						
110	DRVA_DISST[1:0]							
111	MSB_PHOFF[7:0]							
112		MSB_PHOFF[14:8]						
114	DRVB_DISST[1:0]							
115	MSC_PHOFF[7:0]							
116		MSC_PHOFF[14:8]						
118	DRVC_DISST[1:0]							
119	MSD_PHOFF[7:0]							
120		MSD_PHOFF[14:8]						
122	DRVD_DISST[1:0]							
144	MSA_ALL							
218				PLL_LOL	LOS_CLKIN	LOS_XTAL		SYS_CAL
226						MS_RESET		
230				OEB_ALL	OEB_D	OEB_C	OEB_B	OEB_A
235	FCAL[7:0]							
236	FCAL[15:8]							
237						FCAL[17:16]		
241	DIS_LOL							
246							SOFT_RE-SET	
247				PLL_LOL_STK	LOS_-CLKIN_STK	LOS_X-TAL_STK		SYS_-CAL_STK
255								PAGE_SEL
287	MSA_SSUPP2[7:0]							

Table 2. Register Summary (Continued)

Register	7	6	5	4	3	2	1	0
288		MSA_SSUPP2[14:8]						
289		MSA_SSUPP3[7:0]						
290		MSA_SSUPP3[14:8]						
291	MSA_SSUPP1[7:0]							
292	MSA_SSUDP1[3:0]				MSA_SSUPP1[11:8]			
293	MSA_SSUDP1[11:4]							
294	MSA_SSDNP2[7:0]							
295		MSA_SSDNP2[14:8]						
296	MSA_SSDNP3[7:0]							
297		MSA_SSDNP3[14:8]						
298	MSA_SSDNP1[7:0]							
299					MSA_SSDNP1[11:8]			
303	MSB_SSUPP2[7:0]							
304		MSB_SSUPP2[14:8]						
305	MSB_SSUPP3[7:0]							
306		MSB_SSUPP3[14:8]						
307	MSB_SSUPP1[7:0]							
308	MSB_SSUDP1[3:0]				MSB_SSUPP1[11:8]			
309	MSB_SSUDP1[11:4]							
310	MSB_SSDNP2[7:0]							
311		MSB_SSDNP2[14:8]						
312	MSB_SSDNP3[7:0]							
313		MSB_SSDNP3[14:8]						
314	MSB_SSDNP1[7:0]							
315					MSB_SSDNP1[11:8]			
319	MSC_SSUPP2[7:0]							
320		MSC_SSUPP2[14:8]						
321	MSC_SSUPP3[7:0]							
322		MSC_SSUPP3[14:8]						
323	MSC_SSUPP1[7:0]							
324	MSC_SSUDP1[3:0]				MSC_SSUPP1[11:8]			
325	MSC_SSUDP1[11:4]							
326	MSC_SSDNP2[7:0]							
327		MSC_SSDNP2[14:8]						

Table 2. Register Summary (Continued)

Register	7	6	5	4	3	2	1	0
328	MSC_SSDNP3[7:0]							
329		MSC_SSDNP3[14:8]						
330	MSC_SSDNP1[7:0]							
331					MSC_SSDNP1[11:8]			
335	MSD_SSUPP2[7:0]							
336		MSD_SSUPP2[14:8]						
337	MSD_SSUPP3[7:0]							
338		MSD_SSUPP3[14:8]						
339	MSD_SSUPP1[7:0]							
340	MSD_SSUDP1[3:0]				MSD_SSUPP1[11:8]			
341	MSD_SSUDP1[11:4]							
342	MSD_SSDNP2[7:0]							
343		MSD_SSDNP2[14:8]						
344	MSD_SSDNP3[7:0]							
345		MSD_SSDNP3[14:8]						
346	MSD_SSDNP1[7:0]							
347					MSD_SSDNP1[11:8]			

7.6. Register Descriptions

In many registers, the byte reset value contains one or more “x”s because a factory-programmed device can have multiple values for these bits.

Register 0.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						REVID[2:0]		
Type	R							

Reset value = xxxx xxxx

Bit	Name	Function
7:3	Reserved	**Reserved.**
2:0	REVID[2:0]	**Device Revision ID.** Rev A = 000b Rev B = 001b

Register 2.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			Dev_Config2[5:0]					
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	**Reserved.**
5:0	Dev_Config2[5:0]	Bits 5:0 represent the last two digits of the base part number: "56" for Si5338. See "7.6.1. Example Part Number for Device ID Registers" on page 44 for complete part number example.

Register 3.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Dev_Config3[7:3]							Dev_Config3[0]
Type	R/W							R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:3	Dev_Config3[7:3]	Bits 7:3 represent the device grade: 1 for Si5356A. See "7.6.1. Example Part Number for Device ID Registers" on page 44 for complete part number example.
2:1	Reserved	**Reserved.**
0	Dev_Config3[0]	Bit 0 represents bit 16 of the NVM code assigned by Silicon Labs: 00000 through 99999. See "7.6.1. Example Part Number for Device ID Registers" on page 44 for complete part number example.

Register 4.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Dev_Config4[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	Dev_Config4[7:0]	Bits 7:0 represent bits 15:8 of the NVM code assigned by Silicon Labs: 00000 through 99999. See "7.6.1. Example Part Number for Device ID Registers" on page 44 for complete part number example.

Register 5.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Dev_Config5[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	Dev_Config5[7:0]	Bits 7:0 represent bits 7:0 of the NVM code assigned by Silicon Labs: 00000 through 99999. See "7.6.1. Example Part Number for Device ID Registers" on page 44 for complete part number example.

7.6.1. Example Part Number for Device ID Registers

Device ID register contents for an example part number Si5356A-B12345-GM:

Register 0[2:0] = 1h = 001
Register 2 = 78h = 0111 1000
Register 3 = 08h = 0000 1000
Register 4 = 30h = 0011 0000
Register 5 = 39h = 0011 1001

REVID = B
Dev_Config2[5:0] = 10 0110 = 56 (base part number).
Dev_Config3[7:3] = 0 0001 = 1 = A (device grade).
Dev_Config3[0], Dev_Config4[7:0], Dev_Config5[7:0] = 0 0011 0000 0011 1001 = 12345 (NVM code number).

Refer to the Si5356A data sheet's Ordering Guide section for detailed information about ordering part numbers.

Register 6.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				PLL_LOL_MASK	LOS_-CLKIN_MASK	LOS_-CLKIN_MASK	Reserved	SYS_-CAL_MASK
Type				R/W	R/W	R/W		R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	**Reserved.** Must only write 000b to these bits.
4	PLL_LOL_MASK	**Mask Bit for PLL_LOL.** When true, the PLL_LOL bit (Register 218) will not cause an interrupt. See also Register 247. 0: PLL Loss of Lock (LOL) triggers active interrupt on INTR output pin. 1: PLL Loss of Lock (LOL) ignored in generating interrupt output.
3	LOS_CLKIN_MASK	**Mask Bit for CLKIN Loss of Signal.** When true, the LOS_CLKIN bit (Register 218) will not cause an interrupt. See also Register 247. 0: CLKIN LOS triggers active interrupt on INTR output pin. 1: CLKIN LOS ignored in generating interrupt output.
2	LOS_XTAL_MASK	**Mask Bit for XTAL Loss of Signal.** When true, the LOS_XTAL bit (Register 218) will not cause an interrupt. See also Register 247. 0: XTAL LOS triggers active interrupt on INTR output pin. 1: XTAL LOS ignored in generating interrupt output.
1	Reserved	**Reserved.** Must only write 0 to this bit.
0	SYS_CAL_MASK	**Chip Calibration Mask Bit.** When true, the SYS_CAL bit (Register 218) will not cause an interrupt. See also Register 247. 0:PLL self-calibration triggers active interrupt on INTR output pin. 1:PLL self-calibration ignored in generating interrupt output.

Register 27.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	I2C_1P8_SEL	I2C_ADDR[6:0]						
Type	R/W	R/W*						

Reset value = xxxx xxxx

Bit	Name	Function
7	I2C_1P8_SEL	**I^2C Reference V_{DD}.** External I2C VDD 0 = 3.3 V/2.5 V, 1 = 1.8 V. 0: 3.3 V/2.5 V (default) 1: 1.8 V
6:0*	I2C_ADDR[6:0]	**7-Bit I^2C Address.** If and only if there is an I2C_LSB pin, the actual I^2C LSB address is the logical “or” of the bit in position 0 with the state of the I2C_LSB pin. Otherwise, the actual I2C_LSB is the LSB of this 7-bit address. Custom 7-bit I^2C addresses may be requested but must be even numbers if pin control of the I^2C address is to be implemented. For example, if the I^2C address = 70h, the I2C_LSB pin can change the LSB from 0 to 1. However, if the I^2C address = 71h, the I2C_LSB pin will have no effect upon the I^2C address.
***Note:** Although these bits are R/W, writing them is not supported. Custom I^2C addresses can be set at the factory. Contact your local sales office for details.		

Register 28.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			PDIV_IN[0]				XTAL_FREQ[1:0]	
Type	W	W	R/W	R/W	R/W	R/W	R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	**Reserved.** Must only write 00b to these bits.
5	PDIV_IN[0]	This bit and Register 30[4:3] create a 3-bit field that selects the input to the P divider [reg30[4:3] reg28[5]] = PDIV_IN[2:0]. 011b: Clock from CLKIN pin is input to P divider All other bit values are reserved.
4:2	Reserved	**Reserved.** Must only write 000b to these bits.
1:0	XTAL_FREQ[1:0]	**Crystal Frequency Range.** Select Xtal Frequency that you are using. For more information on using crystals, see “AN360: Crystal Selection Guide for Si533x/5x Devices”. 0: 8–11 MHz 1: 11–19 MHz 2: 19–26 MHz 3: 26–30 MHz

Register 29.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PFD_IN_REF[2:0]							
Type	R/W			W	W	W	W	W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	PFD_IN_REF[2:0]	**PFD Reference Input (fpfd).** Selects the input clock to be provided to the reference input of PLL Phase Frequency Detector (PFD). 0: Reserved 1: PDIV_IN selected 2: Reserved 3: PDIV_OUT (P2 divider output) selected 4: XOCLK selected 5: No Clock selected 6: Reserved 7: Reserved
4:0	Reserved	**Reserved.** Must only write 00000b to these bits.

Register 30.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				PDVIN_IN[2:1]		PDIV[2:0]		
Type	R/W					R/W		

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	**Reserved.** Must only write 000b or 101b to these bits.
4:3	PDVIN_IN[2:1]	This bit and Register 28[5] create a 3-bit field that selects the input to the P divider [reg30[4:3] reg28[5]] = PDIV_IN[2:0]. 011b: Clock from CLKIN pin is input to P divider All other bit values are reserved.
2:0	PDIV[2:0]	**P Divide Value.** Sets the value of the P divider. 0: Divide by 1 1: Divide by 2 2: Divide by 4 3: Divide by 8 4: Divide by 16 5: Divide by 32

Register 31.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RADIV_IN[2:0]			RADIV[2:0]			MSA_PDN	DRVA_PDN
Type	R/W			R/W			R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	RADIV_IN[2:0]	**RA Divider Input Selection.** Selects the input to the RA divider. RA divider output goes to CLK0/1. 0: REFCLK 1: Reserved 2: DIVREFCLK 3: Reserved 4: XOCLK 5: Reserved 6: Multisynth A output 7: No Clock
4:2	RADIV[2:0]	**RA Output Divider.** 0: Divide by 1 1: Divide by 2 2: Divide by 4 3: Divide by 8 4: Divide by 16 5: Divide by 32
1	MSA_PDN	**Multisynth A Power Down.** 0: MSA MultiSynth powered up 1: MSA MultiSynth powered down
0	DRVA_PDN	**RA and CLK0/1 Power Down.** 0: RA output divider and CLK0/1 driver powered up 1: RA output divider and CLK0/1 driver powered down

Register 32.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RBDIV_IN[2:0]			RBDIV[2:0]			MSB_PDN	DRVB_PDN
Type	R/W			R/W			R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	RBDIV_IN[2:0]	**RB Divider Input Selection.** Selects the input to the RB divider. RB divider output goes to CLK2/3. 0: REFCLK 1: Reserved 2: DIVREFCLK 3: Reserved 4: XOCLK 5: Multisynth A output* 6: Multisynth B output 7: No Clock ***Note:** To select this output, MSA fanout must be enabled in register 144 [bit 7].
4:2	RBDIV[2:0]	**RB Output Divider.** 0: Divide by 1 1: Divide by 2 2: Divide by 4 3: Divide by 8 4: Divide by 16 5: Divide by 32
1	MSB_PDN	**Multisynth B Power Down.** 0: Multisynth B is powered up. 1: Multisynth B is powered down.
0	DRVB_PDN	**RB and CLK2/3 Power Down.** 0: RB output divider and CLK2/3 driver powered up. 1: RB output divider and CLK2/3 driver powered down.

Register 33.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RCDIV_IN[2:0]			RCDIV[2:0]			MSC_PDN	DRVC_PDN
Type	R/W			R/W			R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	RCDIV_IN[2:0]	**RC Divider Input Selection.** Selects the input to the RC divider. RC divider output goes to CLK4/5. 0: REFCLK 1: Reserved 2: DIVREFCLK 3: Reserved 4: XOCLK 5: Multisynth A output* 6: Multisynth C output 7: No Clock ***Note:** To select this output, MSA fanout must be enabled in register 144 [bit 7].
4:2	RCDIV[2:0]	**RC Output Divider.** 0: Divide by 1. 1: Divide by 2. 2: Divide by 4. 3: Divide by 8. 4: Divide by 16. 5: Divide by 32.
1	MSC_PDN	**Multisynth C Power Down.** 0: Multisynth C powered up. 1: Multisynth C powered down.
0	DRVC_PDN	**RC and CLK4/5 Power Down.** 0: RC output divider and CLK4/5 driver powered up. 1: RC output divider and CLK4/5 driver powered down.

Register 34.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	RDDIV_IN[2:0]			RDDIV[2:0]			MSD_PDN	DRVD_PDN
Type	R/W			R/W			R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	RDDIV_IN[2:0]	**RD Divider Input Selection.** Selects the input to the RD divider. RD divider output goes to CLK6/7. 0: REFCLK 1: Reserved 2: DIVREFCLK 3: Reserved 4: XOCLK 5: Multisynth A output* 6: Multisynth D output 7: No Clock ***Note:** To select this output, MSA fanout must be enabled in register 144 [bit 7].
4:2	RDDIV[2:0]	**RD Output Divider.** 0: Divide by 1. 1: Divide by 2. 2: Divide by 4. 3: Divide by 8. 4: Divide by 16. 5: Divide by 32.
1	MSD_PDN	**Multisynth D Power Down.** 0: Multisynth D is power up. 1: Multisynth D powered down.
0	DRVD_PDN	**RD and CLK6/7 Powerdown.** 0: RD output divider and CLK6/7 driver powered up. 1: RD output divider and CLK6/7 driver powered down.

Register 35.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DRVD_VDDO[1:0]		DRVC_VDDO[1:0]		DRVB_VDDO[1:0]		DRVA_VDDO[1:0]	
Type	R/W		R/W		R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:6	DRVD_VDDO[1:0]	**VDDO Setting for Driver D.** 0: VDDO3 = 3.3 V 1: VDDO3 = 2.5 V 2: VDDO3 = 1.8 V 3: Reserved
5:4	DRVC_VDDO[1:0]	**VDDO Setting for Driver C.** 0: VDDO2 = 3.3 V 1: VDDO2 = 2.5 V 2: VDDO2 = 1.8 V 3: Reserved
3:2	DRVB_VDDO[1:0]	**VDDO Setting for Driver B.** 0: VDDO1 = 3.3 V 1: VDDO1 = 2.5 V 2: VDDO1 = 1.8 V 3: Reserved
1:0	DRVA_VDDO[1:0]	**VDDO Setting for Driver A.** 0: VDDO0 = 3.3 V 1: VDDO0 = 2.5 V 2: VDDO0 = 1.8 V 3: Reserved
Note: If the VDDOx voltage is below the minimum allowed voltage of the programmed voltage setting in Register 35, the output driver may not turn on.		

Register 36.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DRVA_INV[1:0]			DRVA_FMT[1:0]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	**Reserved.**
4:3	DRVA_INV[1:0]	**Driver A Invert (CLK0/1).** 0: Both outputs are in phase 1: CLK0 inverted 2: CLK1 inverted 3: CLK0/1 inverted and in phase
2	Reserved	**Reserved.**
1:0	DRVA_FMT[1:0]	**Driver A Signal Format (CLK0/1).** 0: Reserved 1: CLK0 = on, CLK1 = off 2: CLK0 = off, CLK1 = on 3: CLK0/1 = on

Register 37.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DRVB_INV[1:0]			DRVB_FMT[1:0]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	**Reserved.**
4:3	DRVB_INV[1:0]	**Driver B Invert (CLK2/3).** 0: Both outputs are in phase 1: CLK2 inverted 2: CLK3 inverted 3: CLK2/3 inverted and in phase
2	Reserved	**Reserved.**
1:0	DRVB_FMT[1:0]	**Driver B Signal Format (CLK2/3).** 0: Reserved 1: CLK2 = on, CLK3 = off 2: CLK2 = off, CLK3 = on 3: CLK2/3 = on

Register 38.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DRVC_INV[1:0]			DRVC_FMT[1:0]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	**Reserved.**
4:3	DRVC_INV[1:0]	**Driver C Invert (CLK4/5).** 0: Both outputs are in phase 1: CLK4 inverted 2: CLK5 inverted 3: CLK4/5 inverted and in phase
2	Reserved	**Reserved.**
1:0	DRVC_FMT[1:0]	**Driver C Signal Format (CLK4/5).** 0: Reserved 1: CLK4 = on, CLK5 = off 2: CLK4 = off, CLK5 = on 3: CLK4/5 = on

Register 39.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DRVD_INV[1:0]			DRVD_FMT[1:0]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	**Reserved.**
4:3	DRVD_INV[1:0]	**Driver D Invert (CLK6/7).** 0: Both outputs are in phase 1: CLK6 inverted 2: CLK7 inverted 3: CLK6/7 inverted and in phase
2	Reserved	**Reserved.**
1:0	DRVD_FMT[1:0]	**Driver D Signal Format (CLK6/7).** 0: Reserved 1: CLK6 = on, CLK/7 = off 2: CLK6 = off, CLK7 = on 3: CLK6/7 = on

Register 40.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DRVB_TRIM [2:0]			DRVA_TRIM [4:0]				
Type	R/W			R/W				

Reset value = xxxx xxxx

Bit	Name	Function
7:5	DRVB_TRIM [2:0]	**Trim Bits for Driver B (CLK2/3).** ClockBuilder Desktop sets these values automatically. See AN565 for required manual settings information
4:3	DRVA_TRIM [4:0]	**Trim Bits for Driver A (CLK0/1).** ClockBuilder Desktop sets these values automatically. See AN565 for required manual settings information

Register 41.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		DRVC_TRIM [4:0]					DRVB_TRIM [4:3]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	**Reserved.**
6:2	DRVC_TRIM [4:0]	**Trim Bits for Driver C (CLK4/5).** ClockBuilder Desktop sets these values automatically. See AN565 for required manual settings information.
1:0	DRVB_TRIM [4:3]	**Trim Bits for Driver B (CLK2/3).** ClockBuilder Desktop sets these values automatically. See AN565 for required settings information.

Register 42.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				DRVD_TRIM [4:0]				
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	**Reserved.**
5	Reserved	Must write 1b to this bit.
4:0	DRVD_TRIM [4:0]	**Trim Bits for Driver D (CLK6/7).** ClockBuilder Desktop sets these values automatically. See AN565 for required manual settings information.

Register 47.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved							
Type	R							

Reset value = xxxx xxxx

Bit	Name	Function
7:2	Reserved	**Reserved.** Must write 000101b to these bits if the device is not factory programmed.
1:0	Reserved	**Reserved.**

Register 48.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		PLL_KPHI[6:0]						
Type	R/W	R/W						

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	**Reserved.**
6:0	PLL_KPHI[6:0]	Sets the charge pump current for the PFD. ClockBuilder Desktop sets these values automatically. See AN565 for manual setting.

Register 49.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		VCO_GAIN[2:0]			RSEL[1:0]		BWSEL[1:0]	
Type	R/W	R/W			R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	**Reserved.**
6:4	VCO_GAIN[2:0]	**Sets the VCO Gain.** ClockBuilder Desktop sets these values automatically. See AN565 for manual setting.
3:2	RSEL[1:0]	**Loop Filter Resistor Select.** ClockBuilder Desktop sets these values automatically. See AN565 for manual setting.
1:0	BWSEL[1:0]	**Select the PLL Loopfilter.** ClockBuilder Desktop sets these values automatically. See AN565 for manual setting.

Register 50.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	PLL_ENABLE[1:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	PLL_ENABLE[1:0]	**NAME** 00: Disable PLL 11: Enable PLL It is expected that all Si5356 applications will need to have the PLL enabled; however, the PLL may be disabled when all clock output muxes are set to output XOCLK, REFCLK, and/or DIVREFCLK (RxDIV_IN, see registers 31, 32, 33, 34).
5:0	Reserved	**Reserved.**

Register 51.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						MS_PEC[2:0]		
Type	R/W	R/W	R/W	R/W				

Reset value = xxxx x111

Bit	Name	Function
7:4	Reserved	**Reserved.**
3	Unused	**Unused.**
2:0	MS_PEC[2:0]	**MultiSynth Phase Error Correction.** All non-factory programmed devices must have 111b written to these bits.

Register 52.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MSA_SSMODE[1:0]			
Type	R/W	R/W	R/W	R/W	R/W		R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:2	MSA_SSMODE[1:0]	**Multisynth A Spread Spectrum Mode Select.** 0: No SSC on MSA 01b or 10b or 11b: Down spread on MSA
1:0	Reserved	**Reserved.**

Register 53.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSA_P1[7:0]	**Multisynth A Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth A divider.

Register 54.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
15:8	MSA_P1[15:8]	**Multisynth A Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth A divider.

Register 55.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_P2[5:0]						MSA_P1[17:16]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	MSA_P2[5:0]	**Multisynth A Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the Multisynth A Divider.
1:0	MSA_P1[17:16]	**Multisynth A Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth A divider.

Register 56.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_P2[13:6]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSA_P2[13:6]	**Multisynth A Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the Multisynth A Divider.

Register 57.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_P2[21:14]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSA_P2[21:14]	**Multisynth A Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the Multisynth A Divider.

Register 58.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_P2[29:22]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSA_P2[29:22]	**Multisynth A Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the Multisynth A Divider.

Register 59.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSA_P3[7:0]	**Multisynth A Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth A divider.

Register 60.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSA_P3[15:8]	**Multisynth A Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth A divider.

Register 61.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_P3[23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSA_P3[23:16]	**Multisynth A Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth A divider.

Register 62.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			MSA_P3[29:24]					
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	**Reserved.**
5:0	MSA_P3[29:24]	**Multisynth A Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth A divider.

Register 63.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MSB_SSMODE[1:0]			
Type	R/W	R/W	R/W	R/W	R/W		R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:2	MSB_SSMODE[1:0]	**Multisynth B Spread Spectrum Mode Select.** 0: No SSC on MSB 01b or 10b or 11b: Down spread on MSB
1:0	Reserved	**Reserved.**

Register 64.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSB_P1[7:0]	**Multisynth B Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth B divider.

Register 65.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSB_P1[15:8]	**Multisynth B Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth B divider.

Register 66.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_P2[5:0]						MSB_P1[17:16]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	MSB_P2[5:0]	**Multisynth B Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the Multisynth B Divider.
1:0	MSB_P1[17:16]	**Multisynth B Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth B divider.

Register 67.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_P2[13:6]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSB_P2[13:6]	**Multisynth B Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the Multisynth B Divider.

Register 68.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_P2[21:14]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSB_P2[21:14]	**Multisynth B Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the Multisynth B Divider.

Register 69.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_P2[29:22]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSB_P2[29:22]	**Multisynth B Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the Multisynth B Divider.

Register 70.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSB_P3[7:0]	**Multisynth B Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth B Divider.

Register 71.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSB_P3[15:8]	**Multisynth B Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth B Divider.

Register 72.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_P3[23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSB_P3[23:16]	**Multisynth B Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth B Divider.

Register 73.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			MSB_P3[29:24]					
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	**Reserved.**
5:0	MSB_P3[29:24]	**Multisynth B Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth B Divider.

Register 74.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MSC_SSMODE[1:0]			
Type	R/W	R/W	R/W	R/W	R/W		R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:2	MSC_SSMODE[1:0]	**Multisynth C Spread Spectrum Mode Select.** 0: No SSC on MSC 01b or 10b or 11b: Down spread on MSC
1:0	Reserved	**Reserved.**

Register 75.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSC_P1[7:0]	**Multisynth C Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth C divider.

Register 76.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSC_P1[15:8]	**Multisynth C Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth C divider.

Register 77.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_P2[5:0]						MSC_P1[17:16]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	MSC_P2[5:0]	**Multisynth C Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the Multisynth C Divider.
1:0	MSC_P1[17:16]	**Multisynth C Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth C divider.

Register 78.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_P2[13:6]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSC_P2[13:6]	**Multisynth C Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the Multisynth C Divider.

Register 79.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_P2[21:14]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSC_P2[21:14]	**Multisynth C Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the Multisynth C Divider.

Register 80.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_P2[29:22]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSC_P2[29:22]	**Multisynth C Parameter 2.** This 30-bit number is an encoded representation of the numerator for the fractional part of the Multisynth C Divider.

Register 81.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
	MSC_P3[7:0]	**Multisynth C Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth C Divider.

Register 82.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSC_P3[15:8]	**Multisynth C Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth C Divider.

Register 83.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_P3[23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSC_P3[23:16]	**Multisynth C Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth C Divider.

Register 84.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			MSC_P3[29:24]					
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	**Reserved.**
	MSC_P3[29:24]	**Multisynth C Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth C Divider.

Register 85.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MSD_SSMODE[1:0]			
Type	R/W	R/W	R/W	R/W	R/W		R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:2	MSD_SSMODE[1:0]	**Multisynth D Spread Spectrum Mode Select.** 0: No SSC on MSD 01b or 10b or 11b: Down spread on MSD
1:0	Reserved	**Reserved.**

Register 86.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSD_P1[7:0]	**Multisynth D Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth D divider.

Register 87.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSD_P1[15:8]	**Multisynth D Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth D divider

Register 88.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_P2[5:0]						MSD_P1[17:16]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	MSD_P2[5:0]	**Multisynth D Parameter 2.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth D Divider.
1:0	MSD_P1[17:16]	**Multisynth D Parameter 1.** This 18-bit number is an encoded representation of the integer part of the Multisynth D divider.

Register 89.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_P2[13:6]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSD_P2[13:6]	**Multisynth D Parameter 2.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth D Divider.

Register 90.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_P2[21:14]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSD_P2[21:14]	**Multisynth D Parameter 2.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth D Divider.

Register 91.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_P2[29:22]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSD_P2[29:22]	**Multisynth D Parameter 2.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth D Divider.

Register 92.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSD_P3[7:0]	**Multisynth D Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth D Divider.

Register 93.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSD_P3[15:8]	**Multisynth D Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth D Divider

Register 94.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_P3[23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSD_P3[23:16]	**Multisynth D Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth D Divider

Register 95.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name			MSD_P3[29:24]					
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:6	Reserved	**Reserved.**
5:0	MSD_P3[29:24]	**Multisynth D Parameter 3.** This 30-bit number is an encoded representation of the denominator for the fractional part of the Multisynth D Divider.

Register 97.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P1[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P1[7:0]	**Feedback MultiSynthN Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth Feedback divider.

Register 98.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P1[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P1[15:8]	**Feedback MultiSynthN Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth Feedback divider.

Register 99.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P2[5:0]						MSN_P1[17:16]	
Type	R/W						R/W	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	MSN_P2[5:0]	**Feedback MultiSynthN Parameter 2.** This 18-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth Feedback divider.
1:0	MSN_P1[17:16]	**Feedback MultiSynthN Parameter 1.** This 18-bit number is an encoded representation of the integer part of the MultiSynth Feedback divider.

Register 100.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P2[13:6]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P2[13:6]	**Feedback MultiSynthN Parameter 2.** This 18-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth Feedback divider.

Register 101.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P2[21:14]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P2[21:14]	**Feedback MultiSynthN Parameter 2.** This 18-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth Feedback divider.

Register 102.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P2[29:22]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P2[29:22]	**Feedback MultiSynthN Parameter 2.** This 18-bit number is an encoded representation of the numerator for the fractional part of the MultiSynth Feedback divider.

Register 103.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P3[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P3[7:0]	**Feedback MultiSynthN Parameter 3.** This 18-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth Feedback divider.

Register 104.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P3[15:8]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P3[15:8]	**Feedback MultiSynthN Parameter 3.** This 18-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth Feedback divider

Register 105.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSN_P3[23:16]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSN_P3[23:16]	**Feedback MultiSynthN Parameter 3.** This 18-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth Feedback divider.

Register 106.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	NOTERM_FB		MSN_P3[29:24]					
Type	R/W		R/W					

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	**Reserved.** Must write 1b to this bit.
6	Reserved	**Reserved.**
5:0	MSN_P3[29:24]	**Feedback MultiSynthN Parameter 3.** This 18-bit number is an encoded representation of the denominator for the fractional part of the MultiSynth Feedback divider.

Register 107.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_PHOFF[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSA_PHOFF[7:0]	**Multisynth A Initial Phase Offset.** Multisynth A_PHOFF[14:0] is a 2s complement number. The initial phase offset is Multisynth A_PHOFF[14:0]*Tvco/128 where Tvco is the period of the VCO.

Register 108.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSA_PHOFF[14:8]						
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	**Reserved.**
6:0	MSA_PHOFF[14:8]	**Multisynth A Initial Phase Offset.** Multisynth A_PHOFF[14:0] is a 2s complement number. The initial phase offset is Multisynth A_PHOFF[14:0]*Tvco/128 where Tvco is the period of the VCO.

Register 110.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DRVA_DISST[1:0]							
Type	R/W		R/W	R/W	R/W	R/W	R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:6	DRVA_DISST[1:0]	**Driver A (CLK0/1) Output State When Disabled.** 00: High impedance 01: Logic low 10: Logic high 11: Always on even if disabled
5:0	Reserved	**Reserved.**

Register 111.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_PHOFF[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSB_PHOFF[7:0]	**Multisynth B Initial Phase Offset.** Multisynth B_PHOFF[14:0] is a 2s complement number. The initial phase offset is Multisynth B_PHOFF[14:0]*Tvco/128 where Tvco is the period of the VCO.

Register 112.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSB_PHOFF[14:8]						
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	**Reserved.**
6:0	MSB_PHOFF[14:8]	**Multisynth B Initial Phase Offset.** Multisynth B_PHOFF[14:0] is a 2s complement number. The initial phase offset is Multisynth B_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO.

Register 114.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DRVB_DISST[1:0]							
Type	R/W		R/W	R/W	R/W	R/W	R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:6	DRVB_DISST[1:0]	**Driver B (CLK2/3) Output State When Disabled.** 00: High impedance 01: Logic low 10: Logic high 11: Always on even if disabled
5:0	Reserved	**Reserved.**

Register 115.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_PHOFF[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSC_PHOFF[7:0]	**Multisynth C Initial Phase Offset.** Multisynth C_PHOFF[14:0] is a 2s complement number. The initial phase offset is Multisynth C_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO.

Register 116.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSC_PHOFF[14:8]						
Type	R/W	R/W						

Reset value = xxxx xxxx

Bit	Name	Function
7	Reserved	**Reserved.** Must write 1b to this bit.
6:0	MSC_PHOFF[14:8]	**Multisynth C Initial Phase Offset.** Multisynth C_PHOFF[14:0] is a 2s complement number. The initial phase offset is Multisynth C_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO.

Register 118.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DRVC_DISST[1:0]							
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:6	DRVC_DISST[1:0]	**Driver C (CLK4/5) Output State When Disabled.** 00: High impedance 01: Logic low 10: Logic high 11: Always on even if disabled
5:0	Reserved	**Reserved.**

Register 119.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_PHOFF[7:0]							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	MSD_PHOFF[7:0]	**Multisynth D Initial Phase Offset.** Multisynth D_PHOFF[14:0] is a 2s complement number. The initial phase offset is Multisynth D_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO.

Register 120.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSD_PHOFF[14:8]						
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7	Unused	**Unused.**
6:0	MSD_PHOFF[14:8]	**Multisynth D Initial Phase Offset.** Multisynth D_PHOFF[14:0] is a 2s complement number. The initial phase offset is Multisynth D_PHOFF[14:0] x Tvco/128 where Tvco is the period of the VCO.

Register 122.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DRVD_DISST[1:0]							
Type	R/W		R/W	R/W	R/W	R/W	R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:6	DRVD_DISST[1:0]	**Driver D (CLK6/7) Output State When Disabled.** 00: High impedance 01: Logic low 10: Logic high 11: Always on even if disabled
5:0	Reserved	**Reserved.**

Register 144.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_ALL							
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7	MSA_ALL	**Enable Multisynth A Fanout for All Outputs.** If set, the Multisynth A output is routed to the mux at the input of each R divider. Unused MultiSynths should be powered down to save power. RxDIV_IN must be set to Multisynth A for any outputs requiring Multisynth A fanout.
6:0	Reserved	**Reserved.**

Register 218.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				PLL_LOL	LOS_CLKIN	LOS_XTAL		SYS_CAL
Type				R	R	R		R

Reset value = 0000 0000

Bit	Name	Function
7:5	Reserved	**Reserved.**
4	PLL_LOL	**PLL Loss of Lock (LOL).** Asserts when the two PFD inputs have a frequency difference > 5000 ppm. This bit is held high during a POR_reset until the PLL has locked. This bit will not chatter while the PLL is locking. PLL_LOL does not assert when the input from IN1,IN2 or IN3 is lost. When PLL_LOL asserts, the part will automatically try to re-acquire to the input clock. See Register 241[7].
3	LOS_CLKIN	**Loss of Signal on CLKLIN.**
2	LOS_XTAL	**Loss of Signal on XTAL input.**
1	Reserved	**Reserved.**
0	SYS_CAL	**Device Calibration in Process.**

Register 226.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						MS_RESET		
Type	R							

Reset value = 0000 0000

Bit	Name	Function
7:3	Reserved	
2	MS_RESET	**Multisynth Master Reset.** This reset will disable all clock outputs, reset all Multisynth blocks, and then enable all the clock outputs. Retains device configuration stored in RAM. Do not use read-modify-write procedure to perform soft reset. Instead, write reg242 = 0x04 or 0x00. All Multisynth blocks will remain in reset until a 0 is written to this bit.
1:0	Reserved	

Register 230.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				OEB_ALL	OEB_D	OEB_C	OEB_B	OEB_A
Type				R/W	R/W	R/W	R/W	R/W

Reset value = 0000 0000

Bit	Name	Function
7:5	Unused	**Unused.**
4	OEB_ALL	**Disable All Clock Outputs.** 0: All outputs enabled. 1: All outputs disabled.
3	OEB_D	**Driver D (CLK6/7) Output Disable.** 0: CLK6/7 outputs enabled. 1: CLK6/7 outputs disabled.
2	OEB_C	**Driver C (CLK4/5) Output Disable.** 0: CLK4/5 outputs enabled. 1: CLK4/5 outputs disabled.
1	OEB_B	**Driver B (CLK2/3) Output Disable.** 0: CLK2/3 outputs enabled. 1: CLK2/3 outputs disabled.
0	OEB_A	**Driver A (CLK0/1) Output Disable.** 0: CLK0/1 outputs enabled. 1: CLK0/1 outputs disabled.

Register 235.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FCAL[7:0]							
Type	R							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	FCAL[7:0]	**Bits 7:0 of the Frequency Calibration for the VCO.**

Register 236.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	FCAL[15:8]							
Type	R							

Reset value = xxxx xxxx

Bit	Name	Function
7:0	FCAL[15:8]	**Bits 15:8 of the Frequency Calibration for the VCO.**

Register 237.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Reserved						FCAL[17:16]	
Type	R						R	

Reset value = xxxx xxxx

Bit	Name	Function
7:2	Reserved	**Reserved.**
1:0	FCAL[17:16]	**Bits 17:16 of the Frequency Calibration for the VCO.**

Register 241.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIS_LOL	Reserved. Write to 0x65.						
Type	R/W							

Reset value = xxxx xxxx

Bit	Name	Function
7	DIS_LOL	When asserted, the PLL_LOL status in register 218 is prevented from asserting.
6:0	Reserved	**Reserved.** On a non-factory-programmed device this register must be set to 0x65. On a factory programmed device, this register must stay 0x65.

Register 246.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name							SOFT_RESET	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:2	Reserved	**Reserved.**
1	SOFT_RESET	**Soft Reset.** This reset will disable all clock outputs, then re-acquire the PLL to the input clock and then enable all the clock outputs. Retains device configuration stored in RAM. Do not use read-modify-write procedure to perform soft reset. Instead, write reg246=0x02, regardless of the current value of this bit. Reading this bit after a soft reset will return a 1.
0	Reserved	**Reserved.**

Register 247.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name				PLL_LOL_STK	LOS_FDBK_STK	LOS_CLKIN_STK		SYS_CAL_STK
Type				R/W	R/W	R/W		R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:5	Reserved	**Reserved.**
4	PLL_LOL_STK	**PLL Loss of Lock Sticky Bit.** Sticky version of PLL_LOL. See also Registers 6 and 218. Only a soft or POR reset or writing a “0” to this bit will clear it.
3	LOS_CLKIN_STK	**CLKIN Loss of Signal Sticky Bit.** Sticky version of LOS_CLKIN. See also Registers 6 and 218. Only a soft or POR reset or writing a “0” to this bit will clear it.
2	LOS_XTAL_STK	**XTAL Loss of Signal Sticky Bit.** Sticky version of LOS_XTAL_STK. See also Registers 6 and 218. Only a soft or POR reset or writing a “0” to this bit will clear it.
1	Reserved	**Reserved.**
0	SYS_CAL_STK	**System Calibration in Process Sticky Bit.** Sticky version of SYS_CAL. See also Registers 6 and 218. Only a soft or POR reset or writing a “0” to this bit will clear it.

Register 255.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								PAGE_SEL
Type								R/W

Reset value = xxxx xxxx

Bit	Name	Function
7:1	Unused	**Unused.**
0	PAGE_SEL	Set to 0 to access registers 0–254, set to 1 to access register 256 to 347.

Register 287.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_SSUPP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSA_SSUPP2[7:0]	**Multisynth A Spread Spectrum Up Parameter 2.**

Register 288.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSA_SSUPP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MSA_SSUPP2[14:8]	**Multisynth A Spread Spectrum Up Parameter 2.**

Register 289.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_SSUPP3[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSA_SSUPP3[7:0]	**Multisynth A Spread Spectrum Up Parameter 3.**

Register 290.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSA_SSUPP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	Unused
6:0	MSA_SSUPP3[14:8]	**Multisynth A Spread Spectrum Up Parameter 3.**

Register 291.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_SSUPP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSA_SSUPP1[7:0]	**Multisynth A Spread Spectrum Up Parameter 1.**

Register 292.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_SSUDP1[3:0]				MSA_SSUPP1[11:8]			
Type	R/W				R/W			

Reset value = 0011 0001

Bit	Name	Function
7:4	MSA_SSUDP1[3:0]	**Multisynth A Spread Spectrum Up/Down Parameter 1.**
3:0	MSA_SSUPP1[11:8]	**Multisynth A Spread Spectrum Up Parameter 1.**

Register 293.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_SSUDP1[11:4]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	MSA_SSUDP1[11:4]	**Multisynth A Spread Spectrum Up Parameter 1.**

Register 294.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_SSDNP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSA_SSDNP2[7:0]	**Multisynth A Spread Spectrum Down Parameter 2.**

Register 295.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSA_SSDNP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	Unused.
6:0	MSA_SSDNP2[14:8]	**Multisynth A Spread Spectrum Down Parameter 2.**

Register 296.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_SSDNP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MSA_SSDNP3[7:0]	**Multisynth A Spread Spectrum Down Parameter 3.**

Register 297.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSA_SSDNP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	Unused.
6:0	MSA_SSDNP3[14:8]	**Multisynth A Spread Spectrum Down Parameter 3.**

Register 298.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSA_SSDNP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSA_SSDNP1[7:0]	**Multisynth A Spread Spectrum Down Parameter 1.**

Register 299.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MSA_SSDNP1[11:8]			
Type	R/W				R/W			

Reset value = 0011 0001

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:0	MSA_SSDNP1[11:8]	**Multisynth A Spread Spectrum Down Parameter 1.**

Register 303.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_SSUPP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSB_SSUPP2[7:0]	**Multisynth B Spread Spectrum Up Parameter 2.**

Register 304.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSB_SSUPP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MSB_SSUPP2[14:8]	**Multisynth B Spread Spectrum Up Parameter 2.**

Register 305.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_SSUPP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MSB_SSUPP3[7:0]	**Multisynth B Spread Spectrum Up Parameter 3.**

Register 306.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSB_SSUPP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MSB_SSUPP3[14:8]	**Multisynth B Spread Spectrum Up Parameter 3.**

Register 307.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_SSUPP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSB_SSUPP1[7:0]	**Multisynth B Spread Spectrum Up Parameter 1.**

Register 308.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_SSUDP1[3:0]				MSB_SSUPP1[11:8]			
Type	R/W				R/W			

Reset value = 1001 0000

Bit	Name	Function
7:4	MSB_SSUDP1[3:0]	**Multisynth B Spread Spectrum Up/Down Parameter 1.**
3:0	MSB_SSUPP1[11:8]	**Multisynth B Spread Spectrum Up Parameter 1.**

Register 309.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_SSUDP1[11:4]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	MSB_SSUDP1[11:4]	**Multisynth B Spread Spectrum Up Parameter 1.**

Register 310.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_SSDNP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSB_SSDNP2[7:0]	**Multisynth B Spread Spectrum Down Parameter 2.**

Register 311.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSB_SSDNP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MSB_SSDNP2[14:8]	**Multisynth B Spread Spectrum Down Parameter 2.**

Register 312.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_SSDNP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MSB_SSDNP3[7:0]	**Multisynth B Spread Spectrum Down Parameter 3.**

Register 313.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSB_SSDNP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MSB_SSDNP3[14:8]	**Multisynth B Spread Spectrum Down Parameter 3.**

Register 314.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSB_SSDNP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSB_SSDNP1[7:0]	**Multisynth B Spread Spectrum Down Parameter 1.**

Register 315.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MSB_SSDNP1[11:8]			
Type	R/W				R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:0	MSB_SSDNP1[11:8]	**Multisynth B Spread Spectrum Down Parameter 1.**

Register 319.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_SSUPP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSC_SSUPP2[7:0]	**Multisynth C Spread Spectrum Up Parameter 2.**

Register 320.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSC_SSUPP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MSC_SSUPP2[14:8]	**Multisynth C Spread Spectrum Up Parameter 2.**

Register 321.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_SSUPP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MSC_SSUPP3[7:0]	**Multisynth C Spread Spectrum Up Parameter 3.**

Register 322.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSC_SSUPP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MSC_SSUPP3[14:8]	**Multisynth C Spread Spectrum Up Parameter 3.**

Register 323.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_SSUPP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSC_SSUPP1[7:0]	**Multisynth C Spread Spectrum Up Parameter 1.**

Register 324.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_SSUDP1[3:0]				MSC_SSUPP1[11:8]			
Type	R/W				R/W			

Reset value = 1001 0000

Bit	Name	Function
7:4	MSC_SSUDP1[3:0]	**Multisynth C Spread Spectrum Up/Down Parameter 1.**
3:0	MSC_SSUPP1[11:8]	**Multisynth C Spread Spectrum Up Parameter 1.**

Register 325.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_SSUDP1[11:4]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	MSC_SSUDP1[11:4]	**Multisynth C Spread Spectrum Up/Down Parameter 1.**

Register 326.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_SSDNP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSC_SSDNP2[7:0]	**Multisynth C Spread Spectrum Down Parameter 2.**

Register 327.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSC_SSDNP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MSC_SSDNP2[14:8]	**Multisynth C Spread Spectrum Down Parameter 2.**

Register 328.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_SSDNP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MSC_SSDNP3[7:0]	**Multisynth C Spread Spectrum Down Parameter 3.**

Register 329.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSC_SSDNP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MSC_SSDNP3[14:8]	**Multisynth C Spread Spectrum Down Parameter 3.**

Register 330.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSC_SSDNP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSC_SSDNP1[7:0]	**Multisynth C Spread Spectrum Down Parameter 1.**

Register 331.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MSC_SSDNP1[11:8]			
Type	R/W				R/W			

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:0	MSC_SSDNP1[11:8]	**Multisynth C Spread Spectrum Down Parameter 1.**

Register 335.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_SSUPP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSD_SSUPP2[7:0]	**Multisynth D Spread Spectrum Up Parameter 2.**

Register 336.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSD_SSUPP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MSD_SSUPP2[14:8]	**Multisynth D Spread Spectrum Up Parameter 2.**

Register 337.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_SSUPP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MSD_SSUPP3[7:0]	**Multisynth D Spread Spectrum Up Parameter 3.**

Register 338.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSD_SSUPP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MSD_SSUPP3[14:8]	**Multisynth D Spread Spectrum Up Parameter 3.**

Register 339.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_SSUPP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSD_SSUPP1[7:0]	**Multisynth D Spread Spectrum Up Parameter 1.**

Register 340.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_SSUDP1[3:0]				MSD_SSUPP1[11:8]			
Type	R/W				R/W			

Reset value = 1001 0000

Bit	Name	Function
7:4	MSD_SSUDP1[3:0]	**Multisynth D Spread Spectrum Up/Down Parameter 1.**
3:0	MSD_SSUPP1[11:8]	**Multisynth D Spread Spectrum Up Parameter 1.**

Register 341.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_SSUDP1[11:4]							
Type	R/W							

Reset value = 0011 0001

Bit	Name	Function
7:0	MSD_SSUDP1[11:4]	**Multisynth D Spread Spectrum Up Parameter 2.**

Register 342.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_SSDNP2[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSD_SSDNP2[7:0]	**Multisynth D Spread Spectrum Down Parameter 2.**

Register 343.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSD_SSDNP2[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MSD_SSDNP2[14:8]	**Multisynth D Spread Spectrum Down Parameter 2.**

Register 344.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_SSDNP3[7:0]							
Type	R/W							

Reset value = 0000 0001

Bit	Name	Function
7:0	MSD_SSDNP3[7:0]	**Multisynth D Spread Spectrum Down Parameter 3.**

Register 345.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name		MSD_SSDNP3[14:8]						
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7	Unused	**Unused.**
6:0	MSD_SSDNP3[14:8]	**Multisynth D Spread Spectrum Down Parameter 3.**

Register 346.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	MSD_SSDNP1[7:0]							
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:0	MSD_SSDNP1[7:0]	**Multisynth D Spread Spectrum Down Parameter 1.**

Register 347.

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name					MSD_SSDNP1[11:8]			
Type	R/W							

Reset value = 0000 0000

Bit	Name	Function
7:4	Reserved	**Reserved.**
3:0	MSD_SSDNP1[11:8]	**Multisynth D Spread Spectrum Down Parameter 1.**

Document Change List

Revision 0.1 to Revision 0.2

- Updated "7. Si5356A Registers" on page 21.
  - Added information on Multisynth Reset (MS_RESET) register bit.

Revision 0.2 to Revision 0.3

- Updated "6.2. Center Spread" on page 20 and added "6.2.1. Center Spread Equations for Rev A Devices"
- Updated description in Registers 0, 52, 63, 74, and 85.
- Added description to Registers 2, 3, 4, and 5.
- Added new section 7.6.1. Example Part Number for Device ID Registers

Revision 0.3 to Revision 0.4

- Fixed typos in Up Parameters in "6.1. Down Spread" on page 19.

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