PSoC® Creator™
Project Datasheet for GobeeDir

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Table of Contents

1 Overview

The Cypress PSoC 5 is a family of 32-bit devices with the following characteristics:

- High-performance 32-bit ARM Cortex-M3 core with a nested vectored interrupt controller (NVIC) and a high-performance DMA controller
- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals, such as USB, I2C and SPI
- Analog subsystem that includes 20-bit Delta Sigma converters (ADC), SAR ADCs, 8-bit DACs that can be configured for 12-bit operation, comparators, op amps and configurable switched capacitor (SC) and continuous time (CT) blocks to create PGAs, TIAs, mixers, and more
- Several types of memory elements, including SRAM, flash, and EEPROM
- Programming and debug system through Serial Wire Debug (SWD), and Single Wire Viewer (SWV)
- Flexible routing to all pins

Figure 1 shows the major components of a typical CY8C58LP family member PSoC 5LP device. For details on all the systems listed above, please refer to the PSoC 5LP Technical Reference Manual.

Figure 1. CY8C58LP Device Family Block Diagram

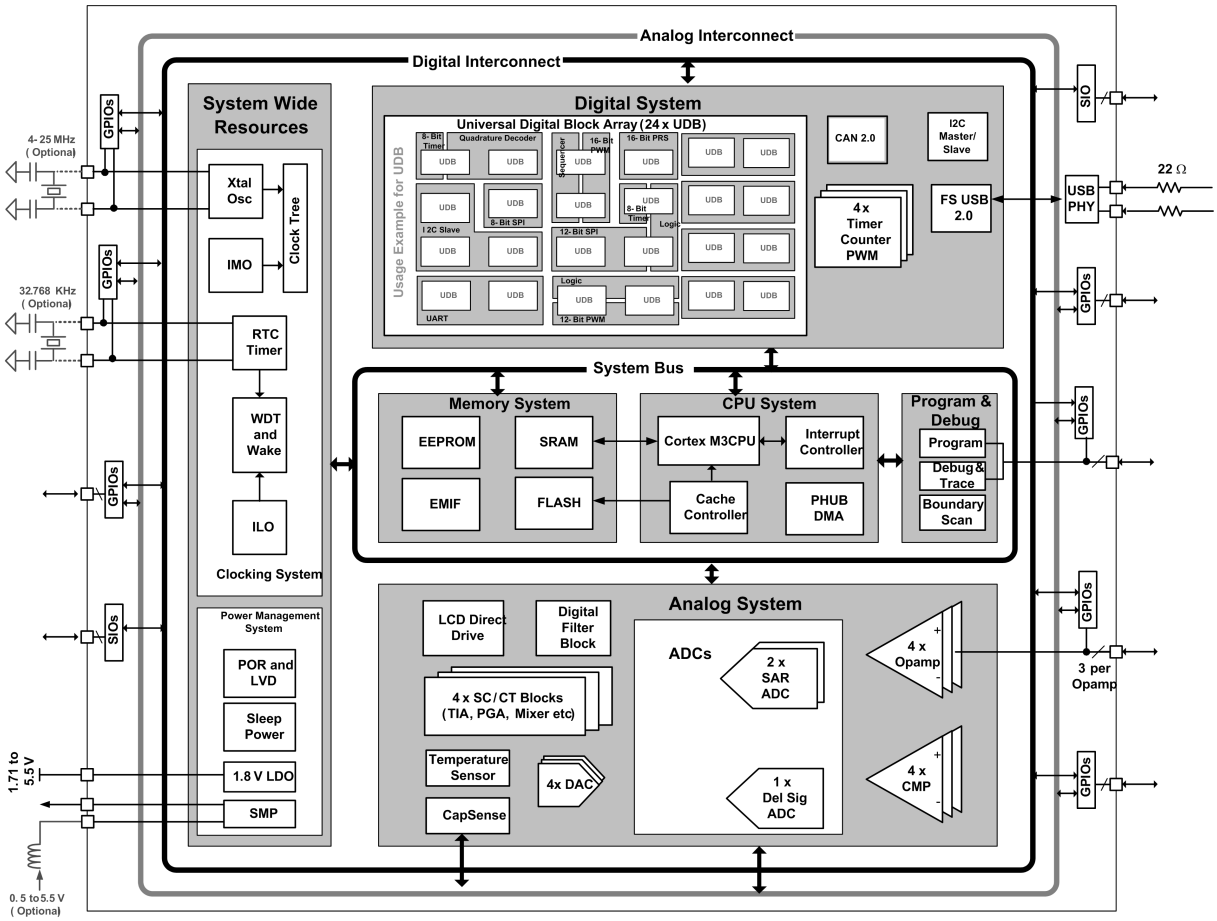


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Architecture	PSoC 5LP
Family	CY8C58LP
CPU speed (MHz)	67
Flash size (kBytes)	256
SRAM size (kBytes)	64
EEPROM size (Bytes)	2048
Trace Buffer (kBytes)	0
Vdd range (V)	1.71 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celcius)	-40 to 85
JTAG ID	0x2E123069

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by BUS_CLK, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

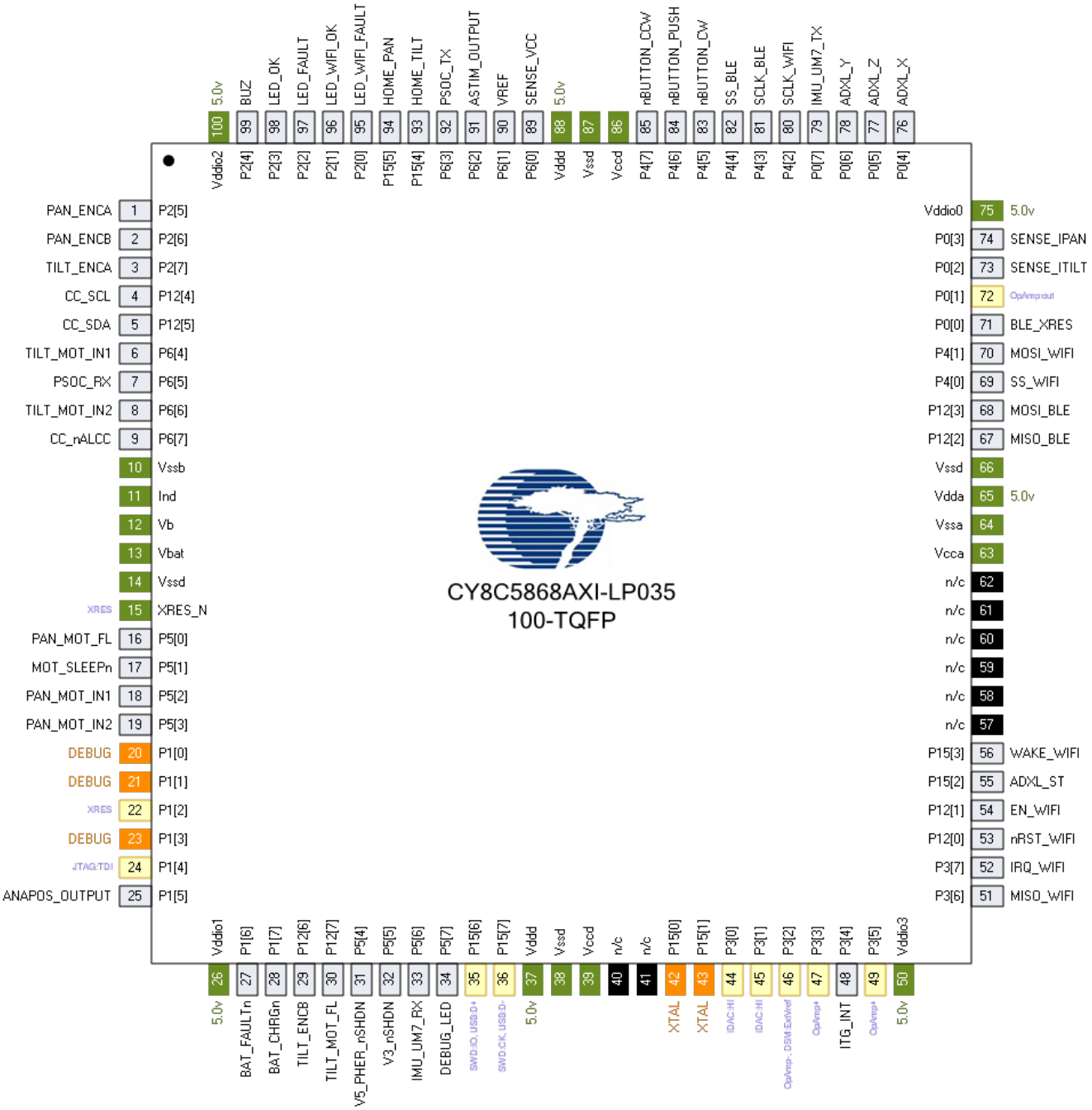
Table 2. Device Resources

Name	Resources in Use	Total Resources Available
Digital clock dividers	8 (100.0%)	8
Analog clock dividers	1 (25.0%)	4
Pins	62 (86.1%)	72
UDB Macrocells	132 (68.8%)	192
UDB Unique Pterms	251 (65.4%)	384
UDB Datapath Cells	12 (50.0%)	24
UDB Status Cells	20 (83.3%)	24
UDB Control Cells	11 (45.8%)	24
DMA Channels	2 (8.3%)	24
Interrupts	10 (31.3%)	32
DSM Fixed Blocks	1 (100.0%)	1
VIDAC Fixed Blocks	2 (50.0%)	4
SC Fixed Blocks	1 (25.0%)	4
Comparator Fixed Blocks	0 (0.0%)	4
Opamp Fixed Blocks	1 (25.0%)	4
CapSense Buffers	0 (0.0%)	2
CAN Fixed Blocks	0 (0.0%)	1
Decimator Fixed Blocks	1 (100.0%)	1
I2C Fixed Blocks	1 (100.0%)	1
Timer Fixed Blocks	3 (75.0%)	4
DFB Fixed Blocks	0 (0.0%)	1
USB Fixed Blocks	0 (0.0%)	1
LCD Fixed Blocks	0 (0.0%)	1
EMIF Fixed Blocks	0 (0.0%)	1
LPF Fixed Blocks	0 (0.0%)	2
SAR Fixed Blocks	0 (0.0%)	2

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode	Reset State
1	P2[5]	PAN_ENCA	Dgtl In	HiZ digital	HiZ Analog Unb
2	P2[6]	PAN_ENCB	Dgtl In	HiZ digital	HiZ Analog Unb
3	P2[7]	TILT_ENCA	Dgtl In	HiZ digital	HiZ Analog Unb
4	P12[4]	CC_SCL	Dgtl I/O	OD, DL	HiZ Analog Unb
5	P12[5]	CC_SDA	Dgtl I/O	OD, DL	HiZ Analog Unb
6	P6[4]	TILT_MOT_IN1	Dgtl Out	Strong drive	HiZ Analog Unb
7	P6[5]	PSOC_RX	Dgtl In	HiZ digital	HiZ Analog Unb
8	P6[6]	TILT_MOT_IN2	Dgtl Out	Strong drive	HiZ Analog Unb
9	P6[7]	CC_nALCC	Dgtl In	HiZ digital	HiZ Analog Unb
10	Vssb	Vssb	Power		
11	Ind	Power			
12	Vb	Vb	Power		
13	Vbat	Vbat	Power		
14	Vssd	Vssd	Power		
15	XRES_N	XRES_N	Power		
16	P5[0]	PAN_MOT_FL	Dgtl In	HiZ digital	HiZ Analog Unb
17	P5[1]	MOT_SLEEPn	Dgtl Out	Strong drive	HiZ Analog Unb
18	P5[2]	PAN_MOT_IN1	Dgtl Out	Strong drive	HiZ Analog Unb
19	P5[3]	PAN_MOT_IN2	Dgtl Out	Strong drive	HiZ Analog Unb
20	P1[0]	GPIO [unused]			HiZ Analog Unb
21	P1[1]	GPIO [unused]			HiZ Analog Unb
22	P1[2]	GPIO [unused]			HiZ Analog Unb
23	P1[3]	GPIO [unused]			HiZ Analog Unb
24	P1[4]	GPIO [unused]			HiZ Analog Unb
25	P1[5]	ANAPOS_OUTPUT	Analog	HiZ analog	HiZ Analog Unb
26	Vio1	Vio1	Power		
27	P1[6]	BAT_FAULTn	Dgtl In	HiZ digital	HiZ Analog Unb
28	P1[7]	BAT_CHRGn	Dgtl In	HiZ digital	HiZ Analog Unb
29	P12[6]	TILT_ENCB	Dgtl In	HiZ digital	HiZ Analog Unb
30	P12[7]	TILT_MOT_FL	Dgtl In	HiZ digital	HiZ Analog Unb
31	P5[4]	V5_PHER_nSHDN	Dgtl Out	Strong drive	HiZ Analog Unb
32	P5[5]	V3_nSHDN	Dgtl Out	Strong drive	HiZ Analog Unb
33	P5[6]	IMU_UM7_RX	Dgtl Out	Strong drive	HiZ Analog Unb
34	P5[7]	DEBUG_LED		Strong drive	HiZ Analog Unb
35	P15[6]	USB [unused]			HiZ Analog Unb
36	P15[7]	USB [unused]			HiZ Analog Unb
37	Vddd	Vddd	Power		
38	Vssd	Vssd	Power		
39	Vccd	Vccd	Power		
42	P15[0]	GPIO [unused]			HiZ Analog Unb
43	P15[1]	GPIO [unused]			HiZ Analog Unb
44	P3[0]	GPIO [unused]			HiZ Analog Unb
45	P3[1]	GPIO [unused]			HiZ Analog Unb
46	P3[2]	GPIO [unused]			HiZ Analog Unb
47	P3[3]	GPIO [unused]			HiZ Analog Unb

Pin	Port	Name	Type	Drive Mode	Reset State
48	P3[4]	ITG_INT	Dgtl In	HiZ digital	HiZ Analog Unb
49	P3[5]	GPIO [unused]			HiZ Analog Unb
50	Vio3	Vio3	Power		
51	P3[6]	MISO_WIFI	Dgtl In	HiZ digital	HiZ Analog Unb
52	P3[7]	IRQ_WIFI	Dgtl In	HiZ digital	HiZ Analog Unb
53	P12[0]	nRST_WIFI		Strong drive	HiZ Analog Unb
54	P12[1]	EN_WIFI		Strong drive	HiZ Analog Unb
55	P15[2]	ADXL_ST	Dgtl Out	Strong drive	HiZ Analog Unb
56	P15[3]	WAKE_WIFI		Strong drive	HiZ Analog Unb
63	Vcca	Vcca	Power		
64	Vssa	Vssa	Power		
65	Vdda	Vdda	Power		
66	Vssd	Vssd	Power		
67	P12[2]	MISO_BLE	Dgtl In	HiZ digital	HiZ Analog Unb
68	P12[3]	MOSI_BLE	Dgtl Out	Strong drive	HiZ Analog Unb
69	P4[0]	SS_WIFI	Dgtl Out	Strong drive	HiZ Analog Unb
70	P4[1]	MOSI_WIFI	Dgtl Out	Strong drive	HiZ Analog Unb
71	P0[0]	BLE_XRES	Dgtl Out	Strong drive	HiZ Analog Unb
72	P0[1]	GPIO [unused]	Analog	HiZ analog	HiZ Analog Unb
73	P0[2]	SENSE_ITILT	Analog	HiZ analog	HiZ Analog Unb
74	P0[3]	SENSE_IPAN	Analog	HiZ analog	HiZ Analog Unb
75	Vio0	Vio0	Power		
76	P0[4]	ADXL_X	Analog	HiZ analog	HiZ Analog Unb
77	P0[5]	ADXL_Z	Analog	HiZ analog	HiZ Analog Unb
78	P0[6]	ADXL_Y	Analog	HiZ analog	HiZ Analog Unb
79	P0[7]	IMU_UM7_TX	Dgtl In	HiZ digital	HiZ Analog Unb
80	P4[2]	SCLK_WIFI	Dgtl Out	Strong drive	HiZ Analog Unb
81	P4[3]	SCLK_BLE	Dgtl Out	Strong drive	HiZ Analog Unb
82	P4[4]	SS_BLE	Dgtl Out	Strong drive	HiZ Analog Unb
83	P4[5]	nBUTTON_CW	Dgtl In	Res pull up	HiZ Analog Unb
84	P4[6]	nBUTTON_PUSH	Dgtl In	Res pull up	HiZ Analog Unb
85	P4[7]	nBUTTON_CCW	Dgtl In	Res pull up	HiZ Analog Unb
86	Vccd	Vccd	Power		
87	Vssd	Vssd	Power		
88	Vddd	Vddd	Power		
89	P6[0]	SENSE_VCC	Analog	HiZ analog	HiZ Analog Unb
90	P6[1]	VREF	Analog	HiZ analog	HiZ Analog Unb
91	P6[2]	ASTIM_OUTPUT	Analog	HiZ analog	HiZ Analog Unb
92	P6[3]	PSOC_TX	Dgtl Out	Strong drive	HiZ Analog Unb
93	P15[4]	HOME_TILT	Dgtl In	HiZ digital	HiZ Analog Unb
94	P15[5]	HOME_PAN	Dgtl In	HiZ digital	HiZ Analog Unb
95	P2[0]	LED_WIFI_FAULT	Dgtl Out	Strong drive	HiZ Analog Unb
96	P2[1]	LED_WIFI_OK	Dgtl Out	Strong drive	HiZ Analog Unb
97	P2[2]	LED_FAULT	Dgtl Out	Strong drive	HiZ Analog Unb
98	P2[3]	LED_OK	Dgtl Out	Strong drive	HiZ Analog Unb
99	P2[4]	BUZ	Dgtl Out	Strong drive	HiZ Analog Unb
100	Vio2	Vio2	Power		

Abbreviations used in Table 3 have the following meanings:

- Dgtl In = Digital Input
- HiZ digital = High impedance digital
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl I/O = Digital In/Out
- OD, DL = Open drain, drives low

- Dgtl Out = Digital Output
- HiZ analog = High impedance analog
- Res pull up = Resistive pull up

2.2 Software Pins

Table 4 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 4. Software Pins

Name	Port	Type	Reset State
ADXL_ST	P15[2]	Dgtl Out	HiZ Analog Unb
ADXL_X	P0[4]	Analog	HiZ Analog Unb
ADXL_Y	P0[6]	Analog	HiZ Analog Unb
ADXL_Z	P0[5]	Analog	HiZ Analog Unb
ANAPOS_OUTPUT	P1[5]	Analog	HiZ Analog Unb
ASTIM_OUTPUT	P6[2]	Analog	HiZ Analog Unb
BAT_CHRGn	P1[7]	Dgtl In	HiZ Analog Unb
BAT_FAULTn	P1[6]	Dgtl In	HiZ Analog Unb
BLE_XRES	P0[0]	Dgtl Out	HiZ Analog Unb
BUZ	P2[4]	Dgtl Out	HiZ Analog Unb
CC_nALCC	P6[7]	Dgtl In	HiZ Analog Unb
CC_SCL	P12[4]	Dgtl I/O	HiZ Analog Unb
CC_SDA	P12[5]	Dgtl I/O	HiZ Analog Unb
DEBUG_LED	P5[7]		HiZ Analog Unb
EN_WIFI	P12[1]		HiZ Analog Unb
HOME_PAN	P15[5]	Dgtl In	HiZ Analog Unb
HOME_TILT	P15[4]	Dgtl In	HiZ Analog Unb
IMU_UM7_RX	P5[6]	Dgtl Out	HiZ Analog Unb
IMU_UM7_TX	P0[7]	Dgtl In	HiZ Analog Unb
IRQ_WIFI	P3[7]	Dgtl In	HiZ Analog Unb
ITG_INT	P3[4]	Dgtl In	HiZ Analog Unb
LED_FAULT	P2[2]	Dgtl Out	HiZ Analog Unb
LED_OK	P2[3]	Dgtl Out	HiZ Analog Unb
LED_WIFI_FAULT	P2[0]	Dgtl Out	HiZ Analog Unb
LED_WIFI_OK	P2[1]	Dgtl Out	HiZ Analog Unb
MISO_BLE	P12[2]	Dgtl In	HiZ Analog Unb
MISO_WIFI	P3[6]	Dgtl In	HiZ Analog Unb
MOSI_BLE	P12[3]	Dgtl Out	HiZ Analog Unb
MOSI_WIFI	P4[1]	Dgtl Out	HiZ Analog Unb
MOT_SLEEPn	P5[1]	Dgtl Out	HiZ Analog Unb
nBUTTON_CCW	P4[7]	Dgtl In	HiZ Analog Unb
nBUTTON_CW	P4[5]	Dgtl In	HiZ Analog Unb
nBUTTON_PUSH	P4[6]	Dgtl In	HiZ Analog Unb
nRST_WIFI	P12[0]		HiZ Analog Unb
PAN_ENCA	P2[5]	Dgtl In	HiZ Analog Unb
PAN_ENCB	P2[6]	Dgtl In	HiZ Analog Unb
PAN_MOT_FL	P5[0]	Dgtl In	HiZ Analog Unb
PAN_MOT_IN1	P5[2]	Dgtl Out	HiZ Analog Unb
PAN_MOT_IN2	P5[3]	Dgtl Out	HiZ Analog Unb
Power	Ind		
PSOC_RX	P6[5]	Dgtl In	HiZ Analog Unb
PSOC_TX	P6[3]	Dgtl Out	HiZ Analog Unb
SCLK_BLE	P4[3]	Dgtl Out	HiZ Analog Unb
SCLK_WIFI	P4[2]	Dgtl Out	HiZ Analog Unb
SENSE_IPAN	P0[3]	Analog	HiZ Analog Unb

Name	Port	Type	Reset State
SENSE_ITILT	P0[2]	Analog	HiZ Analog Unb
SENSE_VCC	P6[0]	Analog	HiZ Analog Unb
SS_BLE	P4[4]	Dgtl Out	HiZ Analog Unb
SS_WIFI	P4[0]	Dgtl Out	HiZ Analog Unb
TILT_ENCA	P2[7]	Dgtl In	HiZ Analog Unb
TILT_ENCB	P12[6]	Dgtl In	HiZ Analog Unb
TILT_MOT_FL	P12[7]	Dgtl In	HiZ Analog Unb
TILT_MOT_IN1	P6[4]	Dgtl Out	HiZ Analog Unb
TILT_MOT_IN2	P6[6]	Dgtl Out	HiZ Analog Unb
V3_nSHDN	P5[5]	Dgtl Out	HiZ Analog Unb
V5_PHER_nSHDN	P5[4]	Dgtl Out	HiZ Analog Unb
VREF	P6[1]	Analog	HiZ Analog Unb
WAKE_WIFI	P15[3]		HiZ Analog Unb

Abbreviations used in Table 4 have the following meanings:

- Dgtl Out = Digital Output
- HiZ Analog Unb = Hi-Z Analog Unbuffered
- Dgtl In = Digital Input
- Dgtl I/O = Digital In/Out

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 5. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Enable Error Correcting Code (ECC)	False
Store Configuration Data in ECC Memory	True
Instruction Cache Enabled	True
Enable Fast IMO During Startup	True
Unused Bonded IO	Allow but warn
Heap Size (bytes)	0x1000
Stack Size (bytes)	0x4000
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 6. System Debug Settings

Name	Value
Debug Select	SWD+SWV (serial wire debug and viewer)
Enable Device Protection	False
Embedded Trace (ETM)	False
Use Optional XRES	False

3.3 System Operating Conditions

Table 7. System Operating Conditions

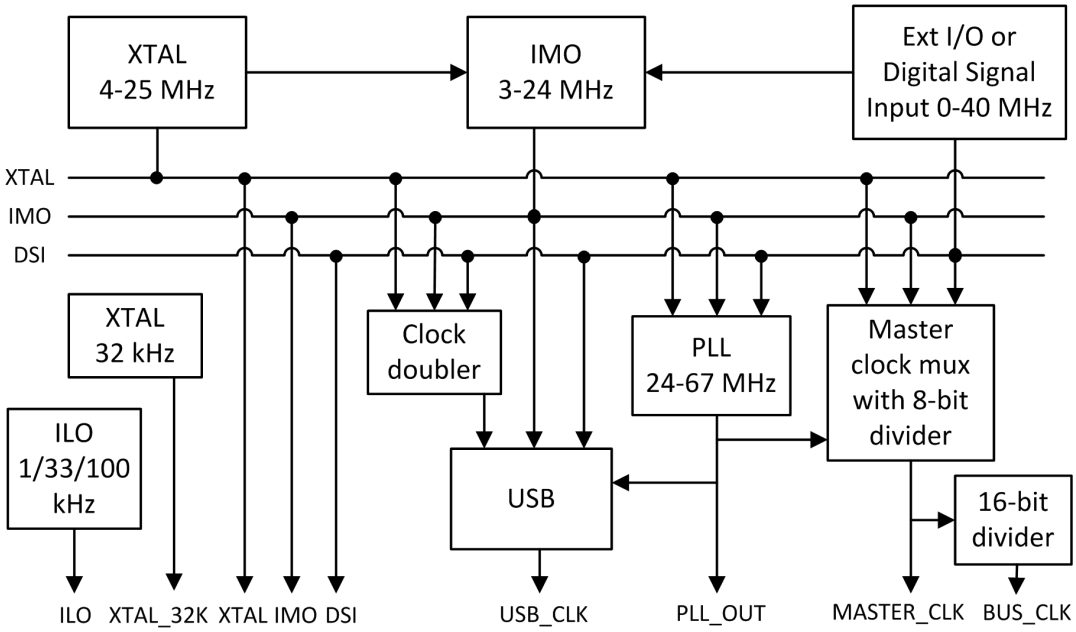
Name	Value
Vddd (V)	5.0
Vdda (V)	5.0
Variable Vdda	False
Vddio0 (V)	5.0
Vddio1 (V)	5.0
Vddio2 (V)	5.0
Vddio3 (V)	5.0
Temperature Range	-40C - 85/125C

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources increase system integration:
  - 3 to 48 MHz Internal Main Oscillator (IMO) ±5% at 3 MHz
  - 1 kHz, 33 kHz, 100 kHz Internal Low Speed Oscillator (ILO) outputs
  - USB Clock Domain, sourced from IMO, MHz External Crystal Oscillator (MHzECO), and Digital System Interconnect (DSI)
  - 24 to 67 MHz fractional Phase-Locked Loop (PLL) sourced from IMO, MHzECO, and DSI
- Clock generated using a DSI signal from an external I/O pin or other logic
- Two external clock sources provide high precision clocks:
  - 4 to 25 MHz External Crystal Oscillator (MHzECO)
  - 32.768 kHz External Crystal Oscillator (kHzECO) for Real Time Clock (RTC)
- Dedicated 16-bit divider for bus clock
- Eight individually sourced 16-bit clock dividers for the digital system peripherals
- Four individually sourced 16-bit clock dividers with skew for the analog system peripherals
- IMO has a USB mode that synchronizes to USB host traffic, requiring no external crystal for USB. (USB equipped parts only)

Figure 3. System Clock Configuration



4.1 System Clocks

Table 8 lists the system clocks used in this design.

Table 8. System Clocks

Name	Domain	Source	Desired Freq (MHz)	Nominal Freq (MHz)	Accuracy (%)	Start at Reset	Enabled
USB_CLK	DIGITAL	IMO	48	0	±0	False	False
BUS_CLK	DIGITAL	MASTER_CLK	0	66	±1	True	True
MASTER_CLK	DIGITAL	PLL_OUT	0	66	±1	True	True
Digital Signal	DIGITAL		0	0	±0	False	False
XTAL 32kHz	DIGITAL		0.0328	0	±0	False	False
XTAL	DIGITAL		8	8	±0	False	True
ILO	DIGITAL		0	0.001	-50,+100	True	True
PLL_OUT	DIGITAL	IMO	66	66	±1	True	True
IMO	DIGITAL		3	3	±1	True	True

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

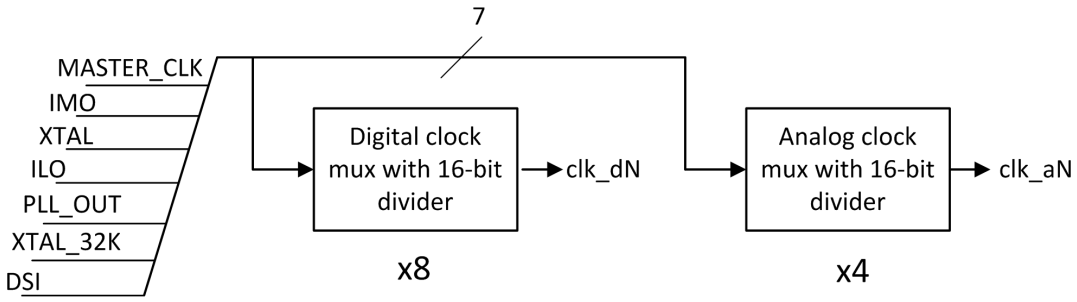


Table 9 lists the local clocks used in this design.

Table 9. Local Clocks

Name	Domain	Source	Desired Freq (MHz)	Nominal Freq (MHz)	Accuracy (%)	Start at Reset	Enabled
ADC_Ext_CP_-Clk	DIGITAL	MASTER_CLK	0	66	±1	True	True
ADC_theACLK	ANALOG	MASTER_CLK	3.6	3.6667	±1	True	True
UART_USB_-IntClock	DIGITAL	MASTER_CLK	0.4608	0.4615	±1	True	True
Clock_CTRL	DIGITAL	IMO	0.003	0.003	±1	True	True
Clock_SPI	DIGITAL	BUS_CLK	0	66	±1	True	True
Clock_5	DIGITAL	BUS_CLK	0	66	±1	True	True
Clock_WIFI	DIGITAL	XTAL	1.6	1.6	±0	True	True
Clock_1	DIGITAL	BUS_CLK	0	66	±1	True	True
WaveDAC8_D-acClk	DIGITAL	IMO	0.01	0.01	±1	True	True

Name	Domain	Source	Desired Freq (MHz)	Nominal Freq (MHz)	Accuracy (%)	Start at Reset	Enabled
Clock_SYS	DIGITAL	IMO	0.0001	0.0001	±1	True	True
Clock_2	DIGITAL	MASTER_CLK	20	22	±1	True	True
I2C_COULOM-B_BusClock	DIGITAL	BUS_CLK	0	66	±1	True	True
Clock_3	DIGITAL	BUS_CLK	0	66	±1	True	True
Clock_4	DIGITAL	BUS_CLK	0	66	±1	True	True
UART_IMU_-IntClock	DIGITAL	MASTER_CLK	0.9216	0.9167	±1	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 5LP Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CyPLL API routines
  - CyIMO API routines
  - CyILO API routines
  - CyMaster API routines
  - CyXTAL API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 10. Interrupts

Name	Priority	Vector
ADC_IRQ	4	29
isr_CTRL	5	3
isr_EVENTS_IDENTIF	6	5
I2C_COULOMB_I2C_IRQ	7	15
isr_BUTTON	7	2
isr_DAS	7	4
isr_Ticks	7	6
isr_WIFI	7	7
QuadDec_PAN_isr	7	0
QuadDec_TILT_isr	7	1

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 5LP Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains the following DMA components: (0 is the highest priority)

Table 11. DMAs

Name	Priority	Channel Number
WaveDAC8_Wave1_DMA	2	0
WaveDAC8_Wave2_DMA	2	1

For more information on DMAs, please refer to:

- PHUB and DMAC chapter in the PSoC 5LP Technical Reference Manual
- DMA chapter in the System Reference Guide
  - DMA API routines and related registers
- Datasheet for cy_dma component

6 Flash Memory

PSoC 5LP devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x3FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- F - External read protect (Factory upgrade)
- R - External write protect (Field upgrade)
- W - Full Protection

For more information on Flash memory and protection, please refer to:

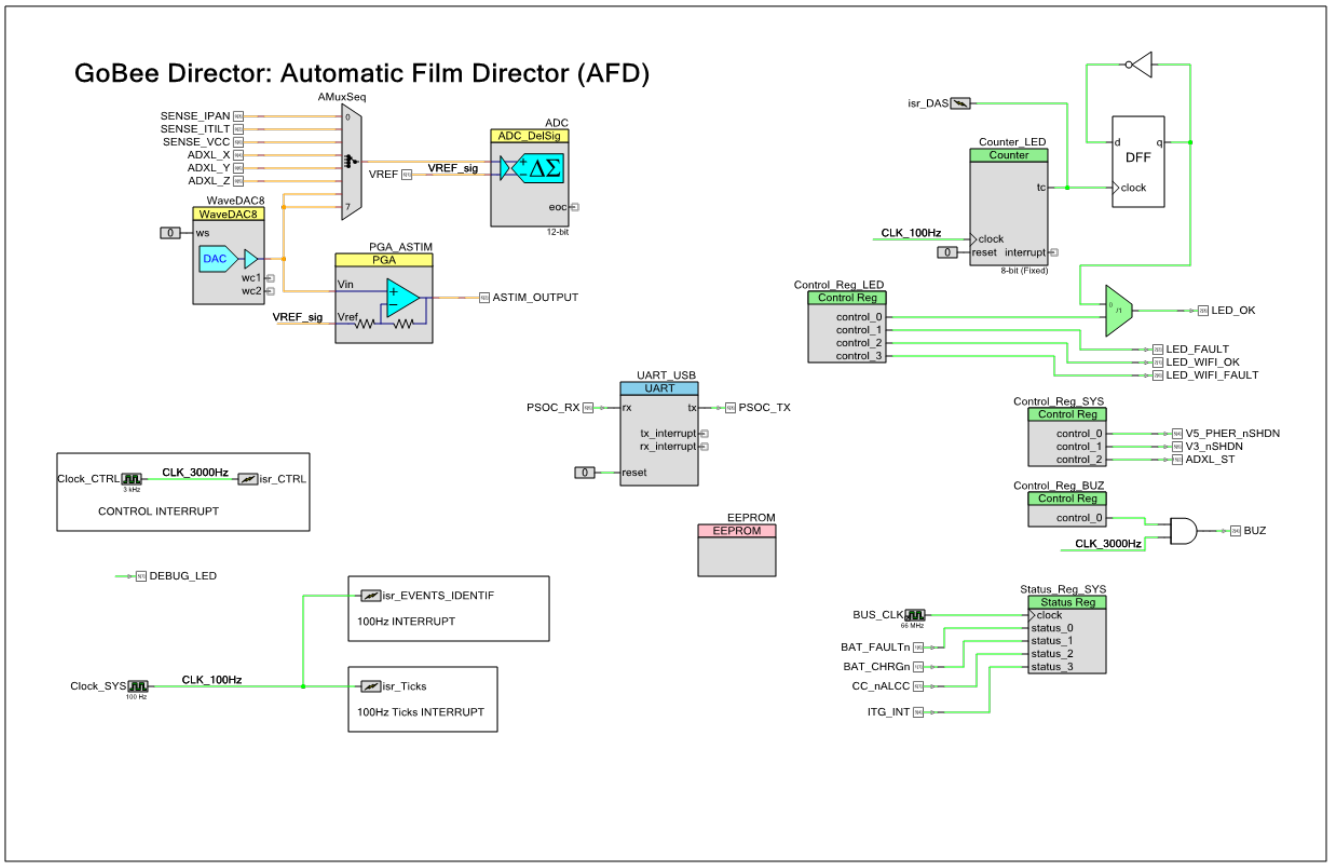
- Flash Protection chapter in the PSoC 5LP Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CyFlash API routines
  - CyWrite API routines

7 Design Contents

This design's schematic content consists of the following 9 schematic sheets:

7.1 Schematic Sheet: GoBee Director

Figure 5. Schematic Sheet: GoBee Director

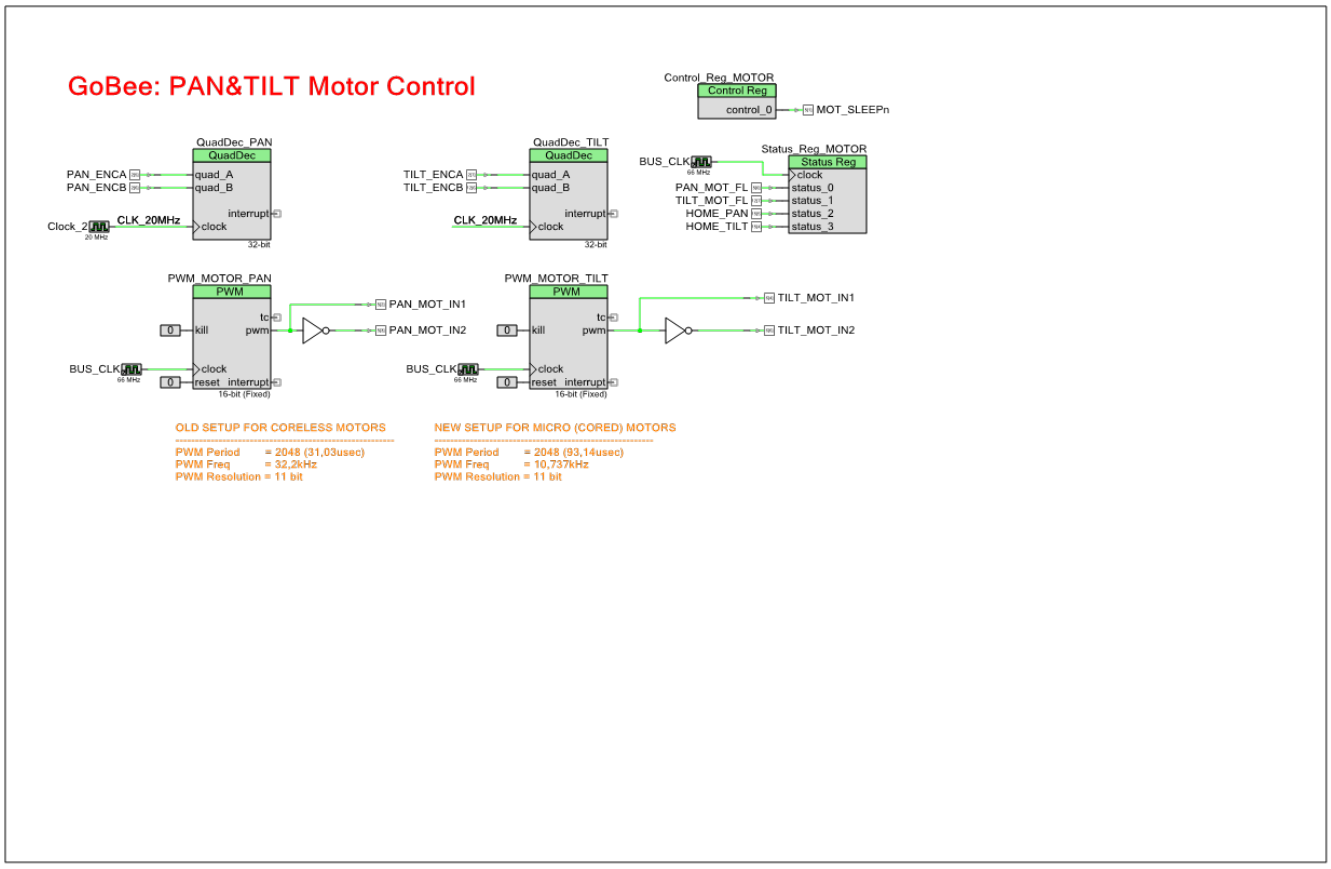


This schematic sheet contains the following component instances:

- Instance ADC (type: ADC_DelSig_v3_10)
- Instance AMuxSeq (type: AMuxSeq_v1_80)
- Instance Control_Reg_BUZ (type: CyControlReg_v1_70)
- Instance Control_Reg_LED (type: CyControlReg_v1_70)
- Instance Control_Reg_SYS (type: CyControlReg_v1_70)
- Instance Counter_LED (type: Counter_v2_40)
- Instance EEPROM (type: EEPROM_v2_10)
- Instance PGA_ASTIM (type: PGA_v2_0)
- Instance Status_Reg_SYS (type: CyStatusReg_v1_80)
- Instance UART_USB (type: UART_v2_30)
- Instance WaveDAC8 (type: WaveDAC8_v2_0)

7.2 Schematic Sheet: MOTOR Ctrl

Figure 6. Schematic Sheet: MOTOR Ctrl

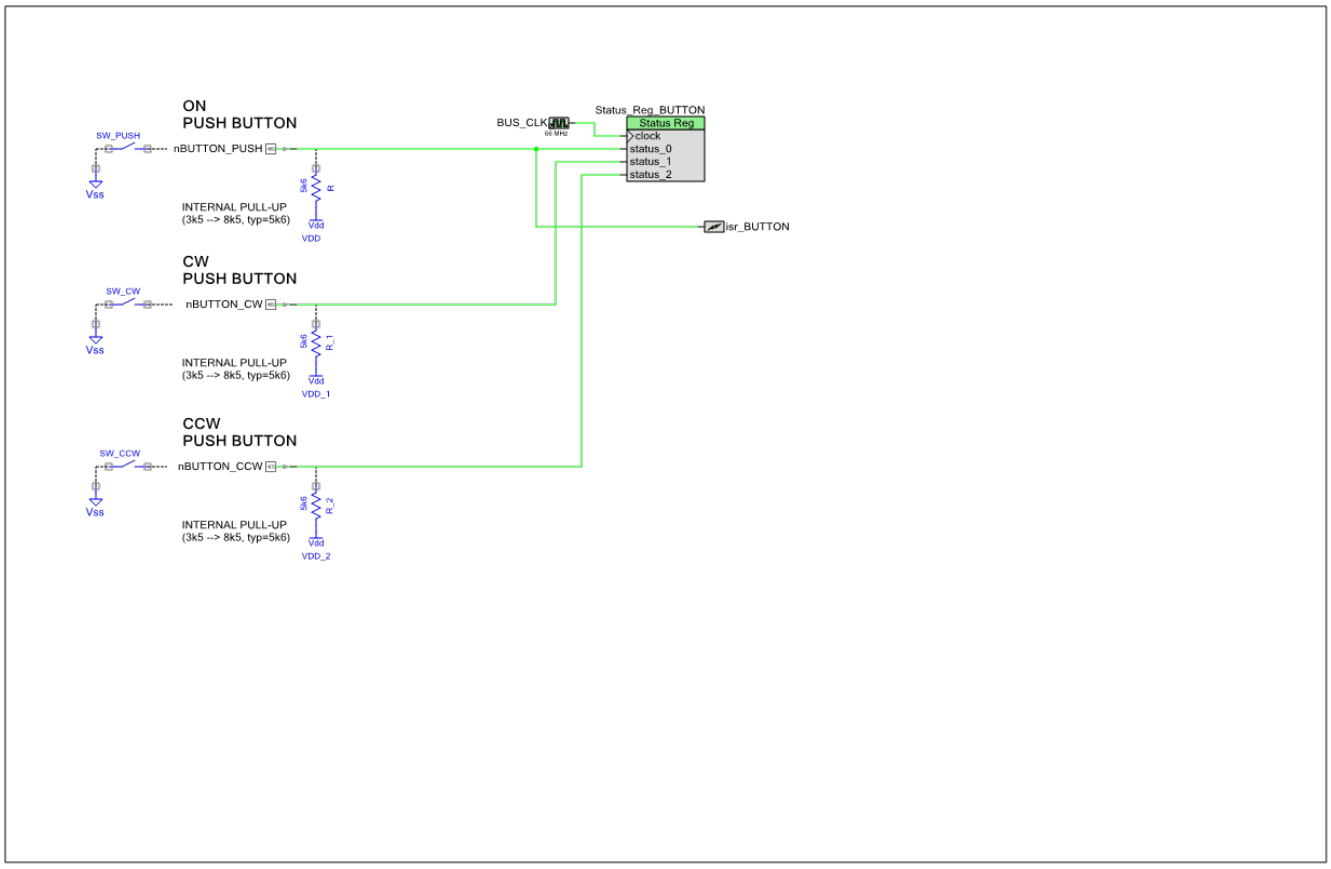


This schematic sheet contains the following component instances:

- Instance Control_Reg_MOTOR (type: CyControlReg_v1_70)
- Instance PWM_MOTOR_PAN (type: PWM_v3_0)
- Instance PWM_MOTOR_TILT (type: PWM_v3_0)
- Instance QuadDec_PAN (type: QuadDec_v2_40)
- Instance QuadDec_TILT (type: QuadDec_v2_40)
- Instance Status_Reg_MOTOR (type: CyStatusReg_v1_80)

7.3 Schematic Sheet: Pushbutton

Figure 7. Schematic Sheet: Pushbutton

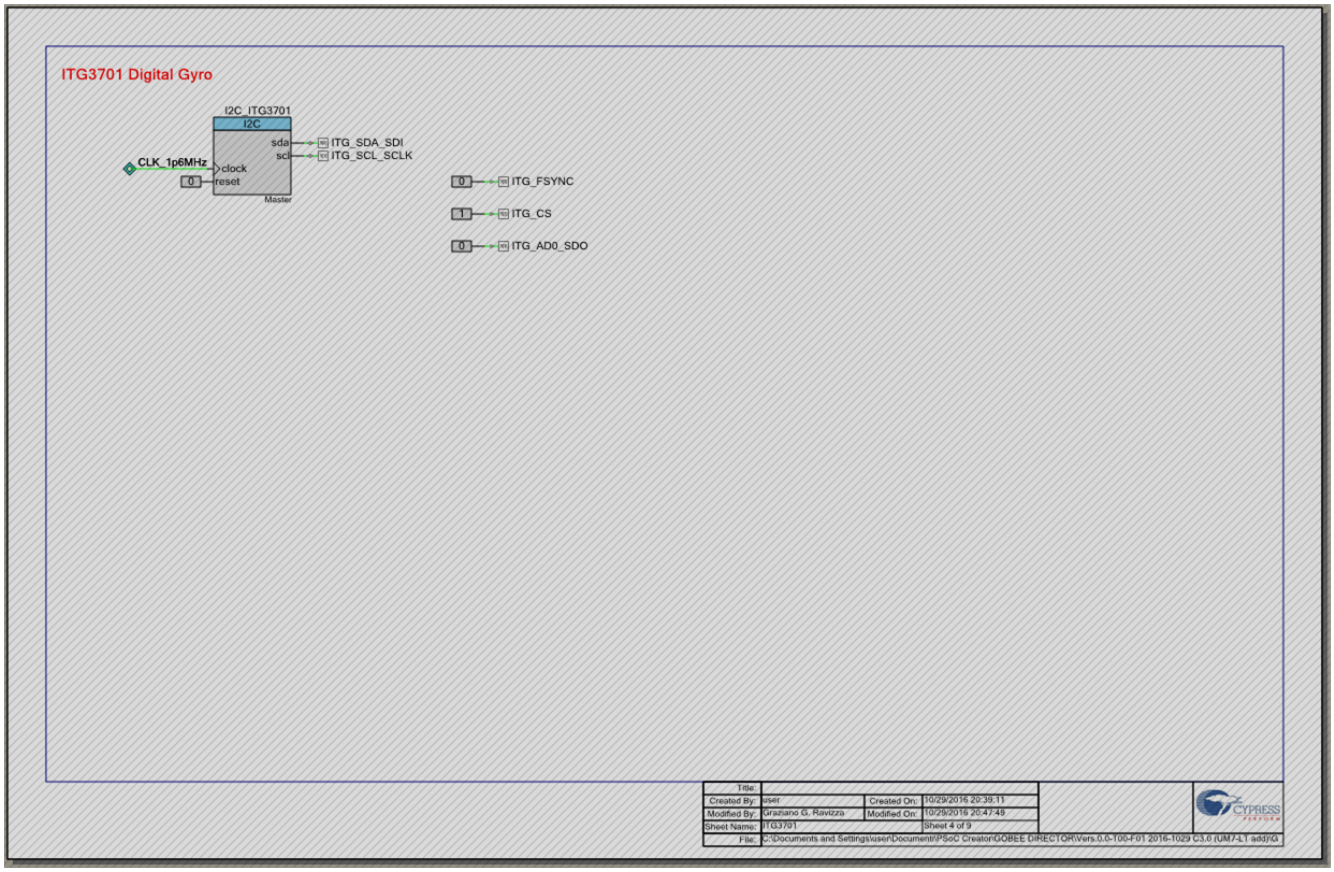


This schematic sheet contains the following component instances:

- Instance Status_Reg_BUTTON (type: CyStatusReg_v1_80)

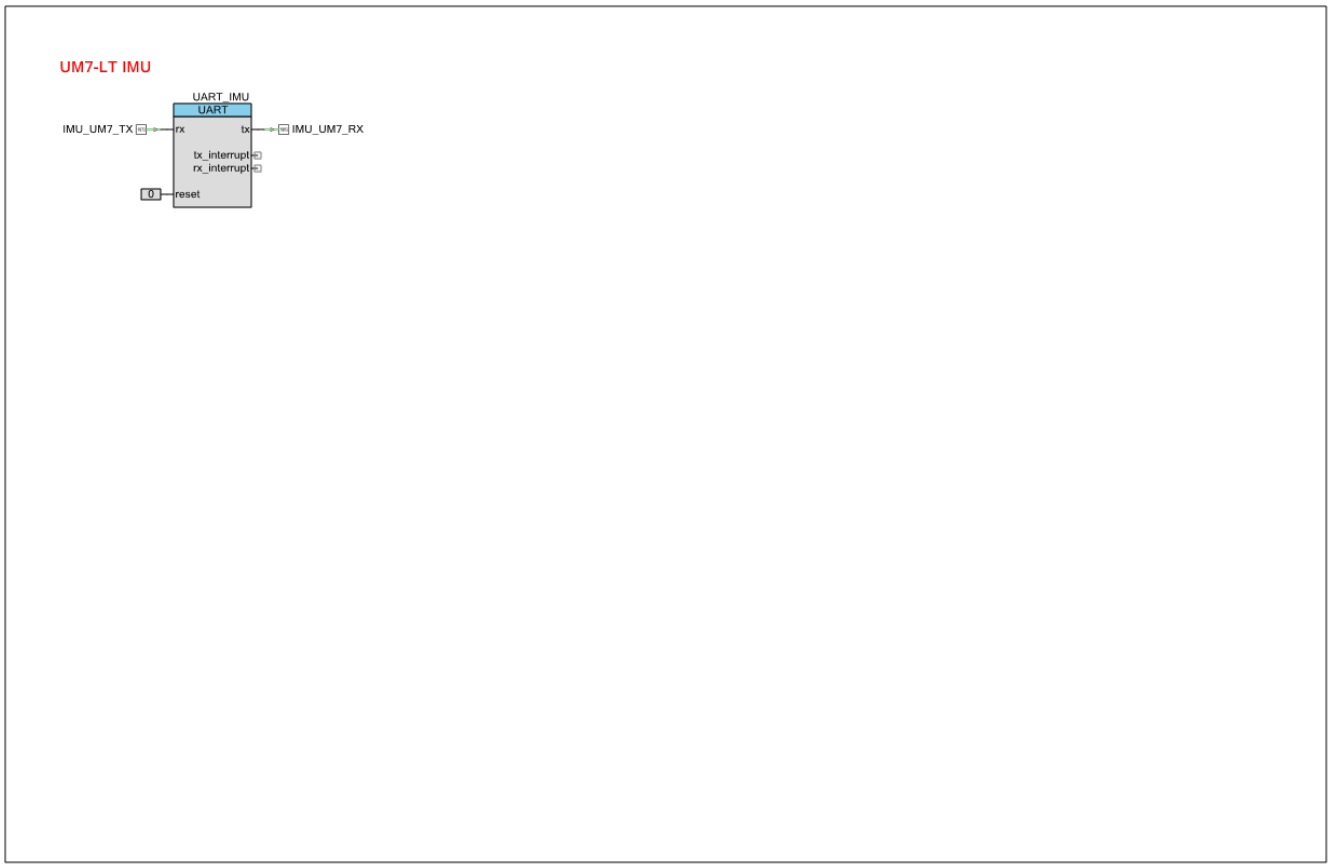
7.4 Schematic Sheet: ITG3701

Figure 8. Schematic Sheet: ITG3701



7.5 Schematic Sheet: IMU

Figure 9. Schematic Sheet: IMU

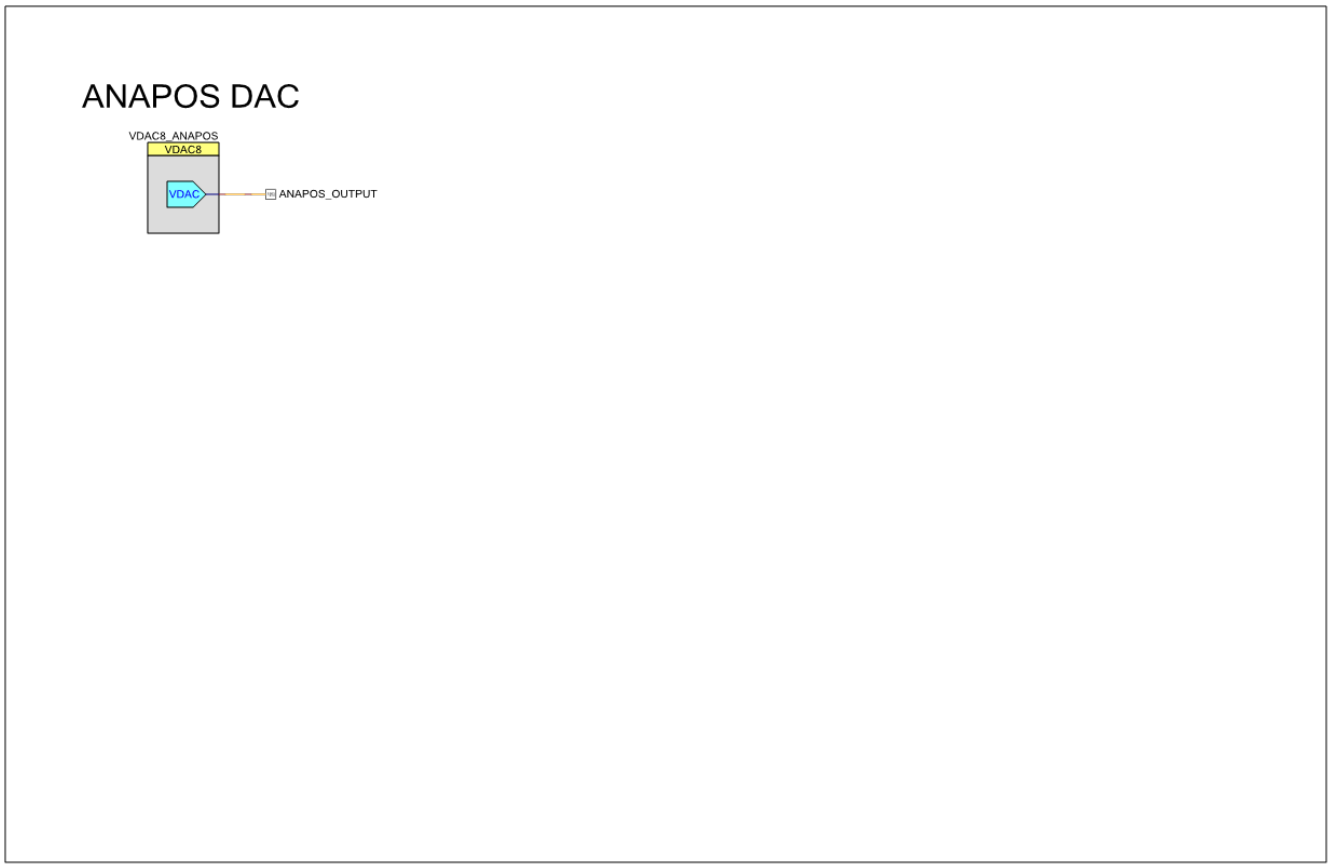


This schematic sheet contains the following component instances:

- Instance UART_IMU (type: UART_v2_30)

7.6 Schematic Sheet: ANAPOS DAC

Figure 10. Schematic Sheet: ANAPOS DAC



This schematic sheet contains the following component instances:

- Instance VDAC8_ANAPOS (type: VDAC8_v1_90)

7.7 Schematic Sheet: Coulomb Counter

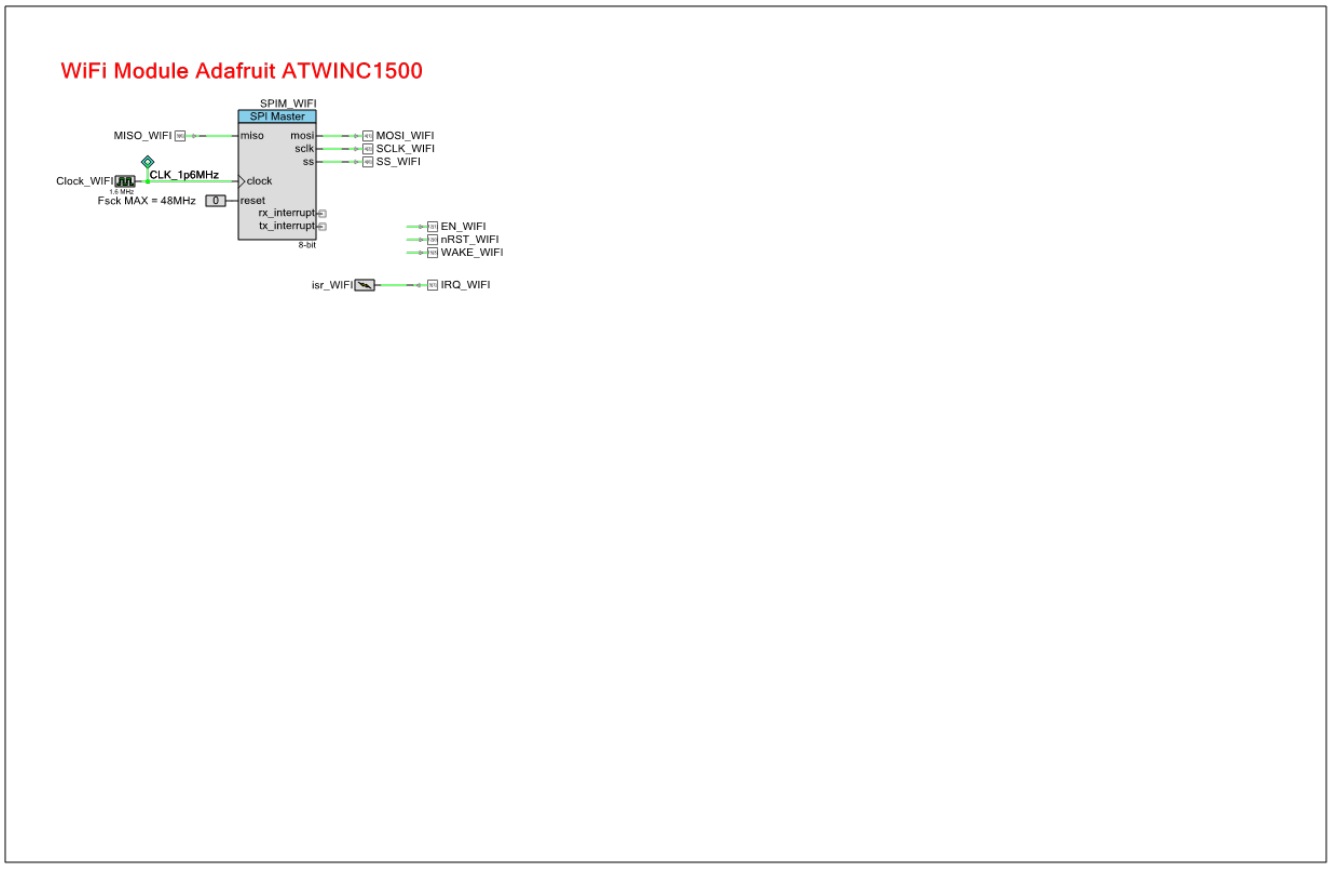
Figure 11. Schematic Sheet: Coulomb Counter

This schematic sheet contains the following component instances:

- Instance I2C_COULOMB (type: I2C_v3_30)

7.8 Schematic Sheet: WiFi

Figure 12. Schematic Sheet: WiFi

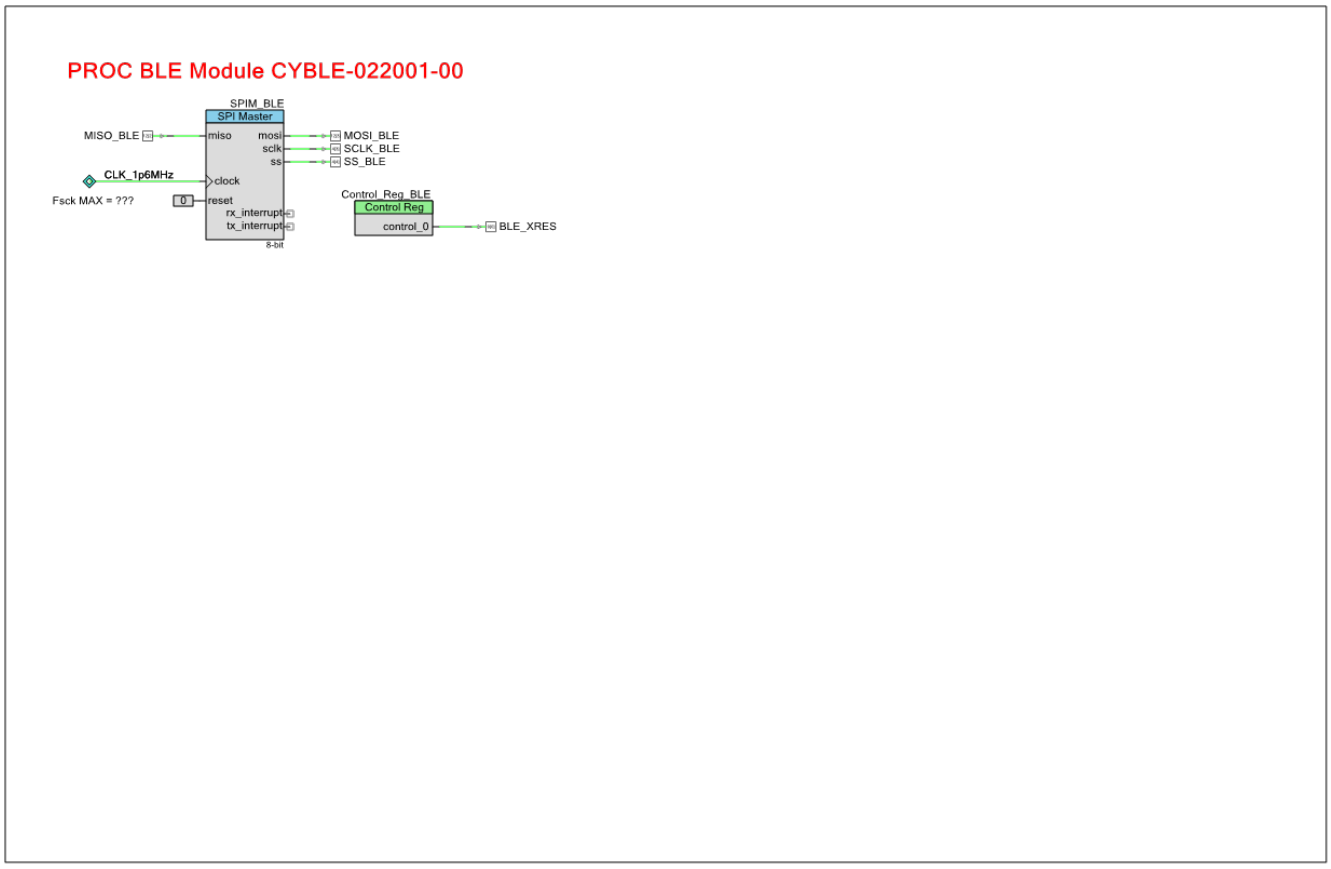


This schematic sheet contains the following component instances:

- Instance SPIM_WIFI (type: SPI_Master_v2_40)

7.9 Schematic Sheet: BLE

Figure 13. Schematic Sheet: BLE



This schematic sheet contains the following component instances:

- Instance Control_Reg_BLE (type: CyControlReg_v1_70)
- Instance SPIM_BLE (type: SPI_Master_v2_40)

8 Components

8.1 Component type: ADC_DelSig [v3.10]

8.1.1 Instance ADC

Description: Delta-Sigma ADC
Instance type: ADC_DelSig [v3.10]
Datasheet: online component datasheet for ADC_DelSig

Table 13. Component Parameters for ADC

Parameter Name	Value	Description
ADC_Alignment	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config2	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config3	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Alignment_Config4	Right	This parameter determines how the result is aligned in the 24 bit result word.
ADC_Charge_Pump_Clock	false	Low power charge pump clock selection
ADC_Clock	Internal	Parameter for selecting the ADC clock type.
ADC_Input_Mode	Differential	Differential or Single ended input mode
ADC_Input_Range	-Input +/- 2*Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config2	-Input +/- Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config3	-Input +/- Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Input_Range_Config4	-Input +/- Vref	Choose input operating mode that best supports the range of the signals being measured.
ADC_Power	Medium Power	Sets power level of ADC.
ADC_Reference	Internal Vdda/4	Selects voltage reference source and configuration.
ADC_Reference_Config2	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config3	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Reference_Config4	Internal 1.024 Volts	Selects voltage reference source and configuration.
ADC_Resolution	12	ADC Resolution in bits
ADC_Resolution_Config2	16	ADC Resolution in bits
ADC_Resolution_Config3	16	ADC Resolution in bits
ADC_Resolution_Config4	16	ADC Resolution in bits

Parameter Name	Value	Description
Clock_Frequency	64000	Determines the ADC clock frequency.
Comment_Config1	Default Config	Parameter which holds the user comment for the config1.
Comment_Config2	Second Config	Parameter which holds the user comment for the config2.
Comment_Config3	Third Config	Parameter which holds the user comment for the config3.
Comment_Config4	Fourth Config	Parameter which holds the user comment for the config4.
Config1_Name	CFG1	This parameter is used to create constants in the header file for config 1.
Config2_Name	CFG2	This parameter is used to create constants in the header file for config 2.
Config3_Name	CFG3	This parameter is used to create constants in the header file for config 3.
Config4_Name	CFG4	This parameter is used to create constants in the header file for config 4.
Configs	1	Number of active configurations
Conversion_Mode	0 - Single Sample	ADC conversion mode
Conversion_Mode_Config2	2 - Continuous	ADC conversion mode
Conversion_Mode_Config3	2 - Continuous	ADC conversion mode
Conversion_Mode_Config4	2 - Continuous	ADC conversion mode
Enable_Vref_Vss	false	Determines whether or not to connect ADC's reference Vssa to AGL[6].
EnableModulatorInput	false	When this parameter is enabled, the modulator input terminal will be enabled on the symbol.
Input_Buffer_Gain	1	Gain of input amplifier
Input_Buffer_Gain_Config2	1	Gain of input amplifier
Input_Buffer_Gain_Config3	1	Gain of input amplifier
Input_Buffer_Gain_Config4	1	Gain of input amplifier
Input_Buffer_Mode	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config2	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config3	Rail to Rail	Buffer Mode type selection
Input_Buffer_Mode_Config4	Rail to Rail	Buffer Mode type selection
Ref_Voltage	1.25	Set reference voltage
Ref_Voltage_Config2	1.024	Set reference voltage
Ref_Voltage_Config3	1.024	Set reference voltage
Ref_Voltage_Config4	1.024	Set reference voltage
rm_int	false	Removes internal interrupt (IRQ)
Sample_Rate	24000	Sample Rate in Hz
Sample_Rate_Config2	10000	Sample Rate in Hz
Sample_Rate_Config3	10000	Sample Rate in Hz
Sample_Rate_Config4	10000	Sample Rate in Hz
Start_of_Conversion	Software	Continuous conversions or hardware controlled

8.2 Component type: AMuxSeq [v1.80]

8.2.1 Instance AMuxSeq

Description: Multiplexer used to route analog signals.
Instance type: AMuxSeq [v1.80]
Datasheet: online component datasheet for AMuxSeq

Table 14. Component Parameters for AMuxSeq

Parameter Name	Value	Description
Channels	8	Channel count.
Isolation	Medium	Specify minimum, medium, or maximum switch control; affects channel isolation and switching time.
MuxType	Single	Select between single or differential inputs.

8.3 Component type: Counter [v2.40]

8.3.1 Instance Counter_LED

Description: 8, 16, 24 or 32-bit Counter
Instance type: Counter [v2.40]
Datasheet: online component datasheet for Counter

Table 15. Component Parameters for Counter_LED

Parameter Name	Value	Description
CaptureMode	None	Defines the functionality of the capture input. Default is None which does not have a capture input pin
ClockMode	Down Counter	Defines the operation of the counter. \nBasic: Count is incremented on the rising edge of the clock input. \n Clock_And_Direction: Clock is incremented or decremented on the rising edge of the clock input based on the direction of the input. \nClock_And_UpCnt_DwnCnt: Clock is an oversampling clock. On the rising edge of UpCnt, the counter is incremented and on the rising edge of DwnCnt, the counter is decremented.
CompareMode	Less Than	Specifies the compare output mode.
CompareStatusEdgeSense	true	Specifies whether rising edge sense for interrupt generation with the Compare output will be used. May be disabled to reduce resource usage.
CompareValue	0	Defines the compare value. Valid vales are from 0 to the period value.

Parameter Name	Value	Description
EnableMode	Software Only	Choose which enable controls the enable of the counter. This can be either through software with the control register, through hardware with the input pin or a combination of both where both must be active for the counter to be enabled.
FixedFunction	true	Defines whether Fixed Function Block usage is required.
InterruptOnCapture	false	Enables the counter status register to produce an interrupt output signal on a capture event.
InterruptOnCompare	false	Enables the counter status register to produce an interrupt output signal on compare true.
InterruptOnOverUnderFlow	false	Enables the counter status register to produce an interrupt output signal on over flow or under flow.
InterruptOnTC	false	Enables the counter status register to produce an interrupt output signal on terminal count.
Period	20	Defines the counter period value in clock counts from 1 to 2^Width-1.
ReloadOnCapture	false	Reloads the counter value to a set value on a capture input event.
ReloadOnCompare	false	Reloads the counter value to a set value on a compare equal event.
ReloadOnOverUnder	true	Reloads the counter value to a set value when overflow or underflow is detected.
ReloadOnReset	true	Reloads the counter value to a set value when reset input is high.
Resolution	8	Defines the width of the counter. It can be 8, 16, 24 or 32 (24 or 32 cannot use Fixed Function block).
RunMode	Continuous	Define the hardware operation to run continuously or run till a terminal count.
UseInterrupt	true	Allows for complete optimization of resource usage down to removing the status register if not required by the user.

8.4 Component type: CyControlReg [v1.70]

8.4.1 Instance Control_Reg_BLE

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.70]

Datasheet: **online component datasheet for CyControlReg**

Table 16. Component Parameters for Control_Reg_BLE

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	1	Defines the number of outputs needed (1-8)

8.4.2 Instance Control_Reg_BUZ

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.70]
Datasheet: **online component datasheet for CyControlReg**

Table 17. Component Parameters for Control_Reg_BUZ

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	1	Defines the number of outputs needed (1-8)

8.4.3 Instance Control_Reg_LED

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.70]
Datasheet: **online component datasheet for CyControlReg**

Table 18. Component Parameters for Control_Reg_LED

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode

Parameter Name	Value	Description
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	4	Defines the number of outputs needed (1-8)

8.4.4 Instance Control_Reg_MOTOR

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.70]
Datasheet: online component datasheet for CyControlReg

Table 19. Component Parameters for Control_Reg_MOTOR

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	1	Defines the number of outputs needed (1-8)

8.4.5 Instance Control_Reg_SYS

Description: The Control Register allows the firmware to set values for to use for digital signals.
Instance type: CyControlReg [v1.70]
Datasheet: online component datasheet for CyControlReg

Table 20. Component Parameters for Control_Reg_SYS

Parameter Name	Value	Description
Bit0Mode	DirectMode	Defines bit 0 mode
Bit1Mode	DirectMode	Defines bit 1 mode
Bit2Mode	DirectMode	Defines bit 2 mode
Bit3Mode	DirectMode	Defines bit 3 mode
Bit4Mode	DirectMode	Defines bit 4 mode
Bit5Mode	DirectMode	Defines bit 5 mode
Bit6Mode	DirectMode	Defines bit 6 mode

Parameter Name	Value	Description
Bit7Mode	DirectMode	Defines bit 7 mode
BitValue	0	Defines bit value
BusDisplay	false	Displays the output terminals as bus
ExternalReset	false	Shows the reset terminal
NumOutputs	3	Defines the number of outputs needed (1-8)

8.5 Component type: CyStatusReg [v1.80]

8.5.1 Instance Status_Reg_BUTTON

Description: The Status Register allows the firmware to read values from digital signals.
Instance type: CyStatusReg [v1.80]
Datasheet: online component datasheet for CyStatusReg

Table 21. Component Parameters for Status_Reg_BUTTON

Parameter Name	Value	Description
Bit0Mode	Transparent	Bit Mode for Bit 0 of the Status Register
Bit1Mode	Transparent	Bit Mode for Bit 1 of the Status Register
Bit2Mode	Transparent	Bit Mode for Bit 2 of the Status Register
Bit3Mode	Transparent	Bit Mode for Bit 3 of the Status Register
Bit4Mode	Transparent	Bit Mode for Bit 4 of the Status Register
Bit5Mode	Transparent	Bit Mode for Bit 5 of the Status Register
Bit6Mode	Transparent	Bit Mode for Bit 6 of the Status Register
Bit7Mode	Transparent	Bit Mode for Bit 7 of the Status Register
BusDisplay	false	Displays the input terminals as bus
Interrupt	false	Shows the interrupt terminal
MaskValue	0	Defines the value of the interrupt mask
NumInputs	3	Defines the number of status inputs (1-8)

8.5.2 Instance Status_Reg_MOTOR

Description: The Status Register allows the firmware to read values from digital signals.
Instance type: CyStatusReg [v1.80]
Datasheet: online component datasheet for CyStatusReg

Table 22. Component Parameters for Status_Reg_MOTOR

Parameter Name	Value	Description
Bit0Mode	Transparent	Bit Mode for Bit 0 of the Status Register

Parameter Name	Value	Description
Bit1Mode	Transparent	Bit Mode for Bit 1 of the Status Register
Bit2Mode	Transparent	Bit Mode for Bit 2 of the Status Register
Bit3Mode	Transparent	Bit Mode for Bit 3 of the Status Register
Bit4Mode	Transparent	Bit Mode for Bit 4 of the Status Register
Bit5Mode	Transparent	Bit Mode for Bit 5 of the Status Register
Bit6Mode	Transparent	Bit Mode for Bit 6 of the Status Register
Bit7Mode	Transparent	Bit Mode for Bit 7 of the Status Register
BusDisplay	false	Displays the input terminals as bus
Interrupt	false	Shows the interrupt terminal
MaskValue	0	Defines the value of the interrupt mask
NumInputs	4	Defines the number of status inputs (1-8)

8.5.3 Instance Status_Reg_SYS

Description: The Status Register allows the firmware to read values from digital signals.
Instance type: CyStatusReg [v1.80]
Datasheet: online component datasheet for CyStatusReg

Table 23. Component Parameters for Status_Reg_SYS

Parameter Name	Value	Description
Bit0Mode	Transparent	Bit Mode for Bit 0 of the Status Register
Bit1Mode	Transparent	Bit Mode for Bit 1 of the Status Register
Bit2Mode	Transparent	Bit Mode for Bit 2 of the Status Register
Bit3Mode	Transparent	Bit Mode for Bit 3 of the Status Register
Bit4Mode	Transparent	Bit Mode for Bit 4 of the Status Register
Bit5Mode	Transparent	Bit Mode for Bit 5 of the Status Register
Bit6Mode	Transparent	Bit Mode for Bit 6 of the Status Register
Bit7Mode	Transparent	Bit Mode for Bit 7 of the Status Register
BusDisplay	false	Displays the input terminals as bus
Interrupt	false	Shows the interrupt terminal
MaskValue	0	Defines the value of the interrupt mask
NumInputs	4	Defines the number of status inputs (1-8)

8.6 Component type: EEPROM [v2.10]

8.6.1 Instance EEPROM

Description: Provides an API to Erase and Write EEPROM.
Instance type: EEPROM [v2.10]
Datasheet: online component datasheet for EEPROM

8.7 Component type: I2C [v3.30]

8.7.1 Instance I2C_COULOMB

Description: Standard I2C communication interface
Instance type: I2C [v3.30]
Datasheet: online component datasheet for I2C

Table 24. Component Parameters for I2C_COULOMB

Parameter Name	Value	Description
Address_Decode	Hardware	Determines either hardware or software address match logic.
BusSpeed_kHz	50	I2C Data Rate in kbps. Standard settings are 50, 100, 400 or 1000. The value must be between 1 and 1000.
EnableWakeup	false	Determines if I2C is selected as wakeup source.
ExternalBuffer	false	Exposes scl and sda in and out terminals outside the component.
Externi2cIntrHandler	false	Allows I2C interrupt handler to be set outside the I2C component. This feature intended only for PM/SM bus usage.
ExternTmoutIntrHandler	false	Allows I2C timeout interrupt handler to be set outside the I2C component. This feature intended only for PM/SM bus usage.
Hex	false	Indicates that address has been input in hexadecimal format.
I2C_Mode	Master	Determines I2C mode - (Slave/Master/Multi--Master/Multi-Master-Slave).
I2cBusPort	I2C0	Determines which I2C pins have been selected. Select I2C0/I2C1 and connect to corresponding pins to be able use I2C as wakeup source.
Implementation	FixedFunction	Determines either I2C implementation Fixed Function or UDB.
NotSlaveClockMinusTolerance	25	Internal component clock negative tolerance value in Master, Multi-Master or Multi-Master-Slave mode.

Parameter Name	Value	Description
NotSlaveClockPlusTolerance	5	Internal component clock positive tolerance value in Master, Multi-Master or Multi-Master-Slave mode.
PrescalerEnabled	false	Enables prescaler (7-bit counter) to expand timeout timer range.
PrescalerPeriod	3	Prescaler period of timeout timer.
SclTimeoutEnabled	false	Enables low time monitoring of scl line.
SdaTimeoutEnabled	false	Enables low time monitoring of sda line.
Slave_Address	8	7-bits I2C slave address.
SlaveClockMinusTolerance	5	Internal component clock negative tolerance value in Slave mode.
SlaveClockPlusTolerance	50	Internal component clock positive tolerance value in Slave mode.
TimeoutImplementation	UDB	Determines either timeout timer feature implementation as UDB or Fixed Function. The Fixed Function implementation only available for PSoC5LP.
TimeOutms	25	Determines maximum time allowed for scl or sda to be low state (in mS). The timeout timer generates interrupt after timeout expires.
TimeoutPeriodff	39999	Period of timeout timer (Fixed Function).
TimeoutPeriodUdb	39999	Period of timeout timer (UDB).
UdbInternalClock	false	Determines either internal or external clock source for I2C UDB.
UdbSlaveFixedPlacementEnable	false	Enables fixed placement for I2C UDB. Only available in slave mode.

8.8 Component type: PGA [v2.0]

8.8.1 Instance PGA_ASTIM

Description: Programmable Gain Amplifier
Instance type: PGA [v2.0]
Datasheet: online component datasheet for PGA

Table 25. Component Parameters for PGA_ASTIM

Parameter Name	Value	Description
Gain	1	Selects supported gain value.
Power	Low Power	Selects the device power.
Vref_Input	External	Enables direct connection from the Analog ground (Agnd) to the inverting input.

8.9 Component type: PWM [v3.0]

8.9.1 Instance PWM_MOTOR_PAN

Description: 8 or 16-bit Pulse Width Modulator
Instance type: PWM [v3.0]
Datasheet: online component datasheet for PWM

Table 26. Component Parameters for PWM_MOTOR_PAN

Parameter Name	Value	Description
CaptureMode	None	Defines the functionality of the capture Input. The parameter determines which signal on the capture input is required to capture the current count value to the FIFO.
CompareStatusEdgeSense	true	Enables edge sense detection on compare outputs for use in edge sensitive interrupts
CompareType1	Less	Sets the compare value comparison type setting for the compare 1 output
CompareType2	Less	Sets the compare value comparison type setting for the compare 2 output
CompareValue1	1500	Compares Output 1 to value
CompareValue2	63	Compares Output 2 to value
DeadBand	2-4 Clock Cycles	Defines whether dead band outputs are desired or not.
DeadTime	3	Defines the number of required dead band clock cycles
DitherOffset	0.00	Allows the user to implement dither to get more bits out of a 8 or 16 bit PWM.
EnableMode	Software Only	Specifies the method of enabling the PWM. This can be either hardware or software.
FixedFunction	true	Determines whether the fixed function counter timer is used or the UDB implementation is used.
InterruptOnCMP1	false	Enables the interrupt on compare1 true event
InterruptOnCMP2	false	Enables the interrupt on compare2 true event
InterruptOnKill	false	Enables the interrupt on a kill event
InterruptOnTC	false	Enables the interrupt on terminal count event
KillMode	Asynchronous	Parameter to select the kill mode for build time.
MinimumKillTime	1	Sets the minimum number of clock cycles that a kill must be active on the outputs when KillMode is set to Minimum Kill Time mode
Period	2048	Defines the PWM period value

Parameter Name	Value	Description
PWMMode	One Output	Defines the overall mode of the PWM
Resolution	16	Defines the bit width of the PWM (8 or 16 bits)
RunMode	Continuous	Defines the run mode options to be either continuous or one shot
TriggerMode	None	Determines the mode of starting the PWM, i.e. triggering the PWM counter to start
UseInterrupt	true	Enables the placement and usage of the status register

8.9.2 Instance PWM_MOTOR_TILT

Description: 8 or 16-bit Pulse Width Modulator
Instance type: PWM [v3.0]
Datasheet: online component datasheet for PWM

Table 27. Component Parameters for PWM_MOTOR_TILT

Parameter Name	Value	Description
CaptureMode	None	Defines the functionality of the capture Input. The parameter determines which signal on the capture input is required to capture the current count value to the FIFO.
CompareStatusEdgeSense	true	Enables edge sense detection on compare outputs for use in edge sensitive interrupts
CompareType1	Less	Sets the compare value comparison type setting for the compare 1 output
CompareType2	Less	Sets the compare value comparison type setting for the compare 2 output
CompareValue1	1500	Compares Output 1 to value
CompareValue2	63	Compares Output 2 to value
DeadBand	2-4 Clock Cycles	Defines whether dead band outputs are desired or not.
DeadTime	3	Defines the number of required dead band clock cycles
DitherOffset	0.00	Allows the user to implement dither to get more bits out of a 8 or 16 bit PWM.
EnableMode	Software Only	Specifies the method of enabling the PWM. This can be either hardware or software.
FixedFunction	true	Determines whether the fixed function counter timer is used or the UDB implementation is used.
InterruptOnCMP1	false	Enables the interrupt on compare1 true event
InterruptOnCMP2	false	Enables the interrupt on compare2 true event

Parameter Name	Value	Description
InterruptOnKill	false	Enables the interrupt on a kill event
InterruptOnTC	false	Enables the interrupt on terminal count event
KillMode	Asynchronous	Parameter to select the kill mode for build time.
MinimumKillTime	1	Sets the minimum number of clock cycles that a kill must be active on the outputs when KillMode is set to Minimum Kill Time mode
Period	2048	Defines the PWM period value
PWMMode	One Output	Defines the overall mode of the PWM
Resolution	16	Defines the bit width of the PWM (8 or 16 bits)
RunMode	Continuous	Defines the run mode options to be either continuous or one shot
TriggerMode	None	Determines the mode of starting the PWM, i.e. triggering the PWM counter to start
UseInterrupt	true	Enables the placement and usage of the status register

8.10 Component type: QuadDec [v2.40]

8.10.1 Instance QuadDec_PAN

Description: Quadrature Decoder Component provides the ability to count transitions on a pair of digital signals
Instance type: QuadDec [v2.40]
Datasheet: online component datasheet for QuadDec

Table 28. Component Parameters for QuadDec_PAN

Parameter Name	Value	Description
CounterResolution	4	Defines the number of counts recorded in one period of the A and B inputs.
CounterSize	32	Specifies the counter bit width
UsingGlitchFiltering	false	This is a boolean parameter used to set whether or not to apply glitch filtering to all inputs.
UsingIndexInput	false	This is a boolean parameter used to set whether or not a third input – index – exists and will be used.

8.10.2 Instance QuadDec_TILT

Description: Quadrature Decoder Component provides the ability to count transitions on a pair of digital signals
Instance type: QuadDec [v2.40]
Datasheet: online component datasheet for QuadDec

Table 29. Component Parameters for QuadDec_TILT

Parameter Name	Value	Description
CounterResolution	4	Defines the number of counts recorded in one period of the A and B inputs.
CounterSize	32	Specifies the counter bit width
UsingGlitchFiltering	true	This is a boolean parameter used to set whether or not to apply glitch filtering to all inputs.
UsingIndexInput	false	This is a boolean parameter used to set whether or not a third input – index – exists and will be used.

8.11 Component type: SPI_Master [v2.40]

8.11.1 Instance SPIM_BLE

Description: Serial Peripheral Interface Master
Instance type: SPI_Master [v2.40]
Datasheet: online component datasheet for SPI_Master

Table 30. Component Parameters for SPIM_BLE

Parameter Name	Value	Description
BidirectMode	false	Bidirectional mode setting
ClockInternal	false	Allow use of the internal clock and desired bit rate or an external clock source
DesiredBitRate	1000000	Desired Bit Rate in bps
HighSpeedMode	false	Enables using of the High Speed Mode
InterruptOnByteComplete	false	Set Initial Interrupt Source to Enable Interrupt on Byte Transfer Complete
InterruptOnRXFull	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Full
InterruptOnRXNotEmpty	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Not Empty
InterruptOnRXOverrun	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Overrun
InterruptOnSPIDone	false	Set Initial Interrupt Source to Enable Interrupt on SPI Done
InterruptOnSPIIdle	false	Set Initial Interrupt Source to Enable Interrupt on SPI Idle
InterruptOnTXEmpty	false	Set Initial Interrupt Source to Enable Interrupt on TX FIFO Empty
InterruptOnTXNotFull	false	Set Initial Interrupt Source to Enable Interrupt on TX FIFO Not Full
Mode	CPHA = 0, CPOL = 0	SPI mode defines the Clock Phase and Clock Polarity desired
NumberOfDataBits	8	Set the Number of Data bits 3-16

Parameter Name	Value	Description
RxBufferSize	4	Defines the amount of RAM Set asside for the RX Buffer
ShiftDir	MSB First	Set the Shift Out Direction
TxBufferSize	4	Defines the amount of RAM Set asside for the TX Buffer
UseRxInternalInterrupt	false	Defines whether Rx internal interrupt is used or not
UseTxInternalInterrupt	false	Defines whether Tx internal interrupt is used or not

8.11.2 Instance SPIM_WIFI

Description: Serial Peripheral Interface Master
Instance type: SPI_Master [v2.40]
Datasheet: online component datasheet for SPI_Master

Table 31. Component Parameters for SPIM_WIFI

Parameter Name	Value	Description
BidirectMode	false	Bidirectional mode setting
ClockInternal	false	Allow use of the internal clock and desired bit rate or an external clock source
DesiredBitRate	1000000	Desired Bit Rate in bps
HighSpeedMode	false	Enables using of the High Speed Mode
InterruptOnByteComplete	false	Set Initial Interrupt Source to Enable Interrupt on Byte Transfer Complete
InterruptOnRXFull	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Full
InterruptOnRXNotEmpty	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Not Empty
InterruptOnRXOverrun	false	Set Initial Interrupt Source to Enable Interrupt on RX FIFO Overrun
InterruptOnSPIDone	false	Set Initial Interrupt Source to Enable Interrupt on SPI Done
InterruptOnSPIIdle	false	Set Initial Interrupt Source to Enable Interrupt on SPI Idle
InterruptOnTXEmpty	false	Set Initial Interrupt Source to Enable Interrupt on TX FIFO Empty
InterruptOnTXNotFull	false	Set Initial Interrupt Source to Enable Interrupt on TX FIFO Not Full
Mode	CPHA = 0, CPOL = 0	SPI mode defines the Clock Phase and Clock Polarity desired
NumberOfDataBits	8	Set the Number of Data bits 3-16
RxBufferSize	4	Defines the amount of RAM Set asside for the RX Buffer

Parameter Name	Value	Description
ShiftDir	MSB First	Set the Shift Out Direction
TxBufferSize	4	Defines the amount of RAM Set asside for the TX Buffer
UseRxInternalInterrupt	false	Defines whether Rx internal interrupt is used or not
UseTxInternalInterrupt	false	Defines whether Tx internal interrupt is used or not

8.12 Component type: UART [v2.30]

8.12.1 Instance UART_IMU

Description: Universal Asynchronous Receiver Transmitter
Instance type: UART [v2.30]
Datasheet: online component datasheet for UART

Table 32. Component Parameters for UART_IMU

Parameter Name	Value	Description
Address1	0	This parameter specifies the RX Hardware Address #1.
Address2	0	This parameter specifies the RX Hardware Address #2.
BaudRate	115200	Sets the target baud rate.
BreakBitsRX	13	Specifies the break signal length for the RX (detection) channel.
BreakBitsTX	13	Specifies the break signal length for the TX channel.
BreakDetect	false	Enables the break detect hardware.
CRCoutputsEn	false	Enables the CRC outputs.
EnIntRXInterrupt	false	Enables the internal RX interrupt configuration and the ISR.
EnIntTXInterrupt	false	Enables the internal TX interrupt configuration and the ISR.
FlowControl	None	Enable the flow control signals.
HalfDuplexEn	false	Enables half duplex mode on the RX Half of the UART module.
HwTXEnSignal	false	Enables the external TX enable signal output.
InternalClock	true	Enables the internal clock. This parameter removes the clock input pin.
InterruptOnTXComplete	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX complete' event.
InterruptOnTXFifoEmpty	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO empty' event.
InterruptOnTXFifoFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO full' event.

Parameter Name	Value	Description
InterruptOnTXFifoNotFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO not full' event.
IntOnAddressDetect	false	Enables the interrupt on hardware address detected event by default
IntOnAddressMatch	false	Enables the interrupt on hardware address match detected event by default
IntOnBreak	false	Enables the interrupt on break signal detected event by default
IntOnByteRcvd	true	Enables the interrupt on RX byte received event by default
IntOnOverrunError	false	Enables the interrupt on overrun error event by default
IntOnParityError	false	Enables the interrupt on parity error event by default
IntOnStopError	false	Enables the interrupt on stop error event by default
NumDataBits	8	Defines the number of data bits. Values can be 5, 6, 7 or 8 bits.
NumStopBits	1	Defines the number of stop bits. Values can be 1 or 2 bits.
OverSamplingRate	8	This parameter defines the over sampling rate.
ParityType	None	Sets the parity type as Odd, Even or Mark/Space
ParityTypeSw	false	This parameter allows the parity type to be changed through - software by using the WriteControlRegister API
RXAddressMode	None	Configures the RX hardware address detection mode
RXBufferSize	4	The size of the RAM space allocated for the RX input buffer.
RXEnable	true	Enables the RX in the UART
TXBitClkGenDP	true	When enabled, this parameter enables the TX clock generation on DataPath resource. When disabled, TX clock is generated from Clock7.
TXBufferSize	4	The size of the RAM space allocated for the TX output buffer.
TXEnable	true	Enables the TX in the UART
Use23Polling	true	Allows the use of 2 out of 3 polling resources on the RX UART sampler.

8.12.2 Instance UART_USB

Description: Universal Asynchronous Receiver Transmitter
Instance type: UART [v2.30]
Datasheet: online component datasheet for UART

Table 33. Component Parameters for UART_USB

Parameter Name	Value	Description
Address1	0	This parameter specifies the RX Hardware Address #1.
Address2	0	This parameter specifies the RX Hardware Address #2.
BaudRate	57600	Sets the target baud rate.
BreakBitsRX	13	Specifies the break signal length for the RX (detection) channel.
BreakBitsTX	13	Specifies the break signal length for the TX channel.
BreakDetect	false	Enables the break detect hardware.
CRCoutputsEn	false	Enables the CRC outputs.
EnIntRXInterrupt	false	Enables the internal RX interrupt configuration and the ISR.
EnIntTXInterrupt	false	Enables the internal TX interrupt configuration and the ISR.
FlowControl	None	Enable the flow control signals.
HalfDuplexEn	false	Enables half duplex mode on the RX Half of the UART module.
HwTXEnSignal	false	Enables the external TX enable signal output.
InternalClock	true	Enables the internal clock. This parameter removes the clock input pin.
InterruptOnTXComplete	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX complete' event.
InterruptOnTXFifoEmpty	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO empty' event.
InterruptOnTXFifoFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO full' event.
InterruptOnTXFifoNotFull	false	This is an Interrupt mask used to enable/disable the interrupt on 'TX FIFO not full' event.
IntOnAddressDetect	false	Enables the interrupt on hardware address detected event by default
IntOnAddressMatch	false	Enables the interrupt on hardware address match detected event by default
IntOnBreak	false	Enables the interrupt on break signal detected event by default
IntOnByteRcvd	true	Enables the interrupt on RX byte received event by default
IntOnOverrunError	false	Enables the interrupt on overrun error event by default
IntOnParityError	false	Enables the interrupt on parity error event by default
IntOnStopError	false	Enables the interrupt on stop error event by default
NumDataBits	8	Defines the number of data bits. Values can be 5, 6, 7 or 8 bits.

Parameter Name	Value	Description
NumStopBits	1	Defines the number of stop bits. Values can be 1 or 2 bits.
OverSamplingRate	8	This parameter defines the over sampling rate.
ParityType	None	Sets the parity type as Odd, Even or Mark/Space
ParityTypeSw	false	This parameter allows the parity type to be changed through - software by using the WriteControlRegister API
RXAddressMode	None	Configures the RX hardware address detection mode
RXBufferSize	4	The size of the RAM space allocated for the RX input buffer.
RXEnable	true	Enables the RX in the UART
TXBitClkGenDP	true	When enabled, this parameter enables the TX clock generation on DataPath resource. When disabled, TX clock is generated from Clock7.
TXBufferSize	4	The size of the RAM space allocated for the TX output buffer.
TXEnable	true	Enables the TX in the UART
Use23Polling	true	Allows the use of 2 out of 3 polling resources on the RX UART sampler.

8.13 Component type: VDAC8 [v1.90]

8.13.1 Instance VDAC8_ANAPOS

Description: 8-Bit Voltage DAC
Instance type: VDAC8 [v1.90]
Datasheet: online component datasheet for VDAC8

Table 34. Component Parameters for VDAC8_ANAPOS

Parameter Name	Value	Description
Data_Source	CPU or DMA (Data Bus)	Selects the method in which the data is written to the vDAC.
Initial_Value	128	Configures the initial vDAC output voltage. The output uses - the following relation: Initial output voltage = value*(Ful-lRange/255). This calculated output voltage value is invalid if DAC Bus is used.
Strobe_Mode	Register Write	Selects how the data is strobed into the DAC. For a register write, the data is strobed into the DAC on each CPU or DMA write. If operating in External mode, an external data strobe signal is required.
VDAC_Range	0 - 4.080V (16mV/bit)	Specifies the full voltage scale range of the vDAC

Parameter Name	Value	Description
VDAC_Speed	High Speed	Specifies the vDAC settling speed. Note that the 'Slow Speed' selection consumes less power.
Voltage	2048	This parameter sets the voltage value.

8.14 Component type: WaveDAC8 [v2.0]

8.14.1 Instance WaveDAC8

Description: 8-Bit Waveform DAC
Instance type: WaveDAC8 [v2.0]
Datasheet: online component datasheet for WaveDAC8

Table 35. Component Parameters for WaveDAC8

Parameter Name	Value	Description
Clock_SRC	Internal	Select either internal or external clock source
DAC_Range	VDAC 0 - 4.080V (Buffered)	Define the type and range of the DAC
Sample_Clock_Freq	10000	Define the sample rate
Wave1_Amplitude	4	Defines the peak-to-peak amplitude of the non-arbitrary waveform

Parameter Name	Value	Description
Wave1_Data	128u,128u,128u,128u,- 128u,129u,129u,129u,- 129u,130u,130u,130u,- 130u,131u,131u,131u,- 131u,132u,132u,132u,- 132u,132u,133u,133u,- 133u,133u,134u,134u,- 134u,134u,135u,135u,- 135u,135u,136u,136u,- 136u,136u,136u,137u,- 137u,137u,137u,138u,- 138u,138u,138u,139u,- 139u,139u,139u,139u,- 140u,140u,140u,140u,- 141u,141u,141u,141u,- 142u,142u,142u,142u,- 143u,143u,143u,143u,- 143u,144u,144u,144u,- 144u,145u,145u,145u,- 145u,146u,146u,146u,- 146u,147u,147u,147u,- 147u,147u,148u,148u,- 148u,148u,149u,149u,- 149u,149u,150u,150u,- 150u,150u,150u,151u,- 151u,151u,151u,152u,- 152u,152u,152u,153u,- 153u,153u,153u,153u,- 154u,154u,154u,154u,- 155u,155u,155u,155u,- 156u,156u,156u,156u,- 156u,157u,157u,157u,- 157u,158u,158u,158u,- 158u,159u,159u,159u,- 159u,159u,160u,160u,- 160u,160u,161u,161u,- 161u,161u,161u,162u,- 162u,162u,162u,163u,- 163u,163u,163u,164u,- 164u,164u,164u,164u,- 165u,165u,165u,165u,- 166u,166u,166u,166u,- 166u,167u,167u,167u,- 167u,168u,168u,168u,- 168u,168u,169u,169u,- 169u,169u,170u,170u,- 170u,170u,170u,171u,- 171u,171u,171u,172u,- 172u,172u,172u,172u,- 173u,173u,173u,173u,- 174u,174u,174u,174u,- 174u,175u,175u,175u,- 175u,175u,176u,176u,- 176u,176u,177u,177u,- 177u,177u,177u,178u,- 178u,178u,178u,179u,- 179u,179u,179u,179u,- 180u,180u,180u,180u,- 180u,181u,181u,181u,- 181u,182u,182u,182u,- 182u,182u,183u,183u,- 183u,183u,184u,184u,- 184u,184u,184u,184u,- 185u,185u,185u,185u,- 186u,186u,186u,186u,- 186u,187u,187u,187u,-	This is the storage data array for the content of the waveform

Parameter Name	Value	Description
Wave1_DCOffset	2.04	Defines the non-arbitrary DC offset (relative to GND) of the waveform
Wave1_Length	3333	Defines the number of data points in the waveform
Wave1_PhaseShift	0	Defines the Phase Shift relative to the beginning of the waveform
Wave1_Type	Sine	Defines the waveform Type
Wave2_Amplitude	4	Defines the peak-to-peak amplitude of the non-arbitrary waveform

Parameter Name	Value	Description
Wave2_Data	252u,252u,252u,252u,- 252u,252u,252u,252u,-	This is the storage data array for the content of the waveform

Parameter Name	Value	Description
Wave2_DCOffset	2.04	Defines the non-arbitrary DC offset (relative to GND) of the waveform
Wave2_Length	3333	Defines the number of data points in the waveform
Wave2_PhaseShift	0	Defines the Phase Shift relative to the beginning of the waveform
Wave2_Type	Square	Defines the waveform Type

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 5LP register map is covered in the PSoC 5LP Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 5LP Technical Reference Manual
  - Low Power Modes chapter in the PSoC 5LP Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines
- Cache Management
  - Cache Controller chapter in the PSoC 5LP Technical Reference Manual
  - Cache chapter in the System Reference Guide
    - CyFlushCache() API routine