Physics 117 Lab 7:Introduction to Logic Gates

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1. MOFSET logic inverters

1.1. Part A

This lab focuses on Logic with electronics, as such out first experiment dealt with building a simple NMOS inverter, where we simply drive a voltages through the gate and drain, and see the gate voltage turns it off, and then measure the voltage change along the drain, the circuit diagram can be seen in figure 1. We are then asked to plot the input vs output voltage which can be seen in figure 2. the last objective of the first part was to answer why we couldn't hook the drain directly to the 5 volts, this can be also seen as why we need the resistor, first the 10 $k\Omega$ resistor, to see the voltage drop in the drain and secondly because we need to limit the current to the JFET, so that the gain does not break down due to excess current called.

1.2. Part B

The next section simply had us build a PMOS inverter, without help, which can be seen in figure 3.

1.3. Part C

The next next section had us calculate the output impedance of the NMOS inverter. We were able to do this using a simple equation of $\frac{V_{out}}{V_{in}} = \frac{R_t}{R_t+R_1}$. Not only this we replaced our 10 $k\Omega$ resistor with an 11 Ω resistor when measuring the output when off to get a more accurate read on the impedance, which we got around .5 .5Ω, we are then asked to see if its the same when the circuit is true or false, the reality is that when the circuit is on, it has an high output impedance around 10 kΩ, so the impedance is different for 1 true and 0 false.

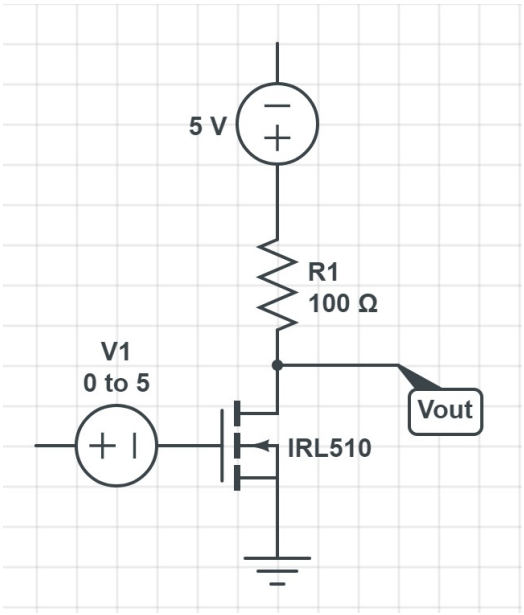

Figure 1: This simple schematic represents NMOS logic circuit

1.4. Part D

The next part of the lab had us set the amplitude and offset of our function generator to produce a square wave, and then confirm with a 100Hz square wave, that the circuit was inverting which it was and can be seen in figure 4.We are then asked to see how long it takes the circuit from 0 to 1 which was 1.3 μs and then 1 to 0 which was 0 to 1 which was 130 ns. The last thing we are asked to do is find the highest frequency where the circuit still works which was around 1356 HZ, where a computer would have something of 3 GHz, so the NMOS is lacking.

1.5. Part E

The last thing we are asked for this section is to measure the rise and fall times of the PMOS and NMOS inverters and explain why they are different. For the NMOS, fall time was 50 ns, and rise was 7.5 μs, for the PMOS the rise time was 100 ns and the fall time was 10 μs. You can see the measurements in figure 5. The reason why they are so different is the nature of the PMOS has a well of electrons and NMOS does not, particularly electrons and holes travel at different speeds where holes are slower, so for the PMOS the holes it

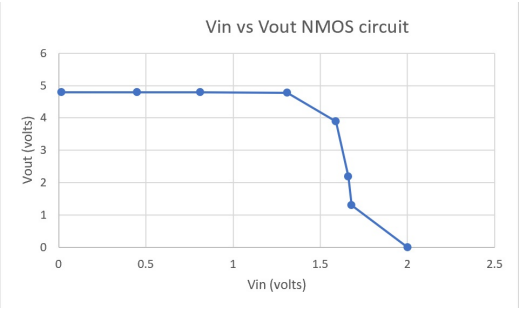

Figure 2: This shows the Vin versus Vout of the NMOS circuit

uses causes it to have a slow rise but the fall is due to the N's where electrons are utilized.

2. Homemade CMOS inverter

2.1. Part F

For the next part we are asked to create a CMOS inverter which can be seen in figure 6. We are asked to find the rise and fall times of the CMOS where we got 120 ns for the rise and 90ns for the fall, this is substantially faster than the previous NMOS and PMOS inverters. We are then lastly asked to find the frequency at which breaking occurs which was around 1.37 MHz. The rise and fall time can be seen in figure 7.

3. Off-the-shelf CMOS inverter

3.1. Part G

The next stage of the lab had us use a chip CMOS (74HCT04), and feed it the correct voltages, which can be seen in figure 8. Then we are asked to measure the range of input voltages that correspond to the 0 and 1 logic levels, for which we get the same range of corresponding voltages as we did on the NMOS inverter. You can see the output of the circuit in figure 9.

4. Homemade NAND (13-5)

4.1. Part H

The last thing we had to do was build a NAND gate using a NMOS and PMOS in tandem, which can be seen in figure 10. We are asked to

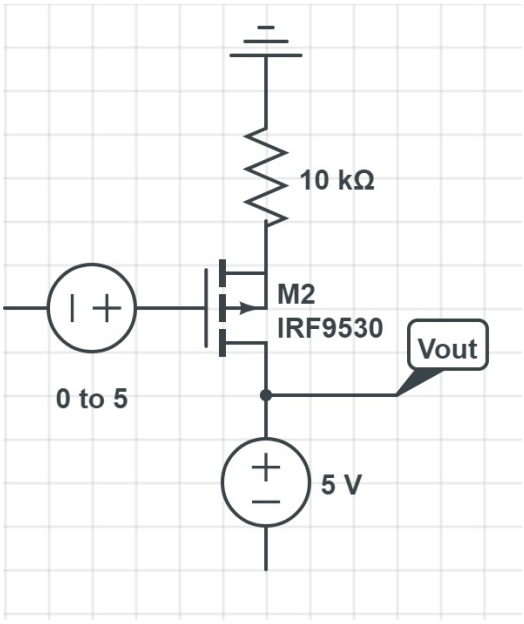

Figure 3: This shows the PMOS inverter circuit

evaluate the truth table for a NAND gate where in only functions with no input basically, you can see our output in figure 11. Lastly we are asked to explain why this circuit behaves as a NAND where no or 1 input yields a 5 volt DC, at Q, and 2 inputs yields no voltage, the voltages are fed in at A and B, A feeds the gate of a NMOS and PMOS, where the NMOS drain goes to Q and the sink goes to the NMOS B feeds, B also feeds another PMOS gate that has a sink feeding the Q point, So the way these gates work is that if a voltage is fed then the gate shuts off its supply to the voltage, the PMOS because there sinks dont go and the NMOS because there drains do not, particularly the B NMOS cannot function unless no A voltage is feeding making the PMOS, thus this functions as an NAND gate because when A and B feed voltages it causes the gates to close there voltages from the Q point but if 1 voltage is on, the other that is off has gates that feed the Q point 5 volts.

4.2. Part I

The last section of the lab had us use a NAND chip (74HCT00), and to show it follows the truth table as well, you can see our chip configuration in figure 12 and its outputs in figure 13.

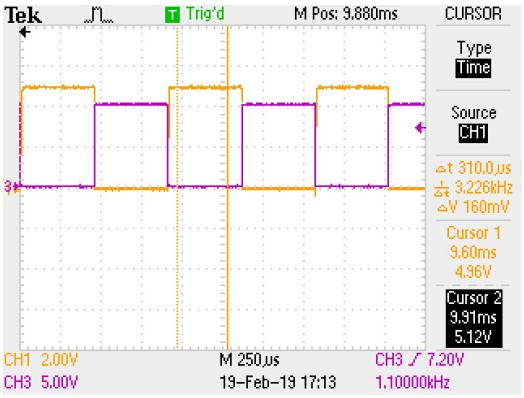

Figure 4: This shows the NMOS inverter circuit handling a 100Hz square wave

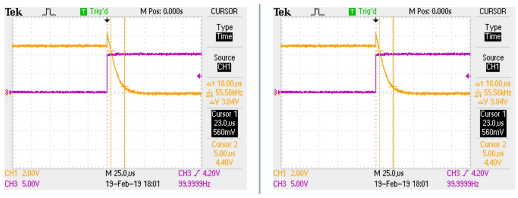

Figure 5: This shows the NMOS inverter circuit handling a square wave, that we then got the rise and fall time

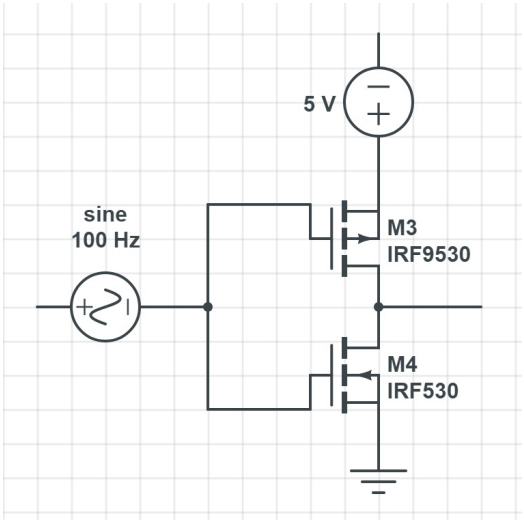

Figure 6: This shows CMOS inverter circuit

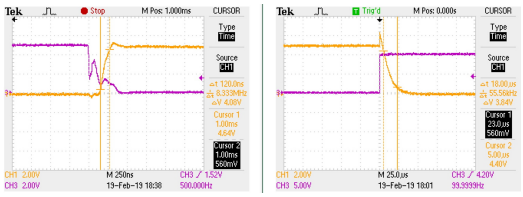

Figure 7: This shows CMOS inverter circuit, handling a square wave where we read the fall and rise time

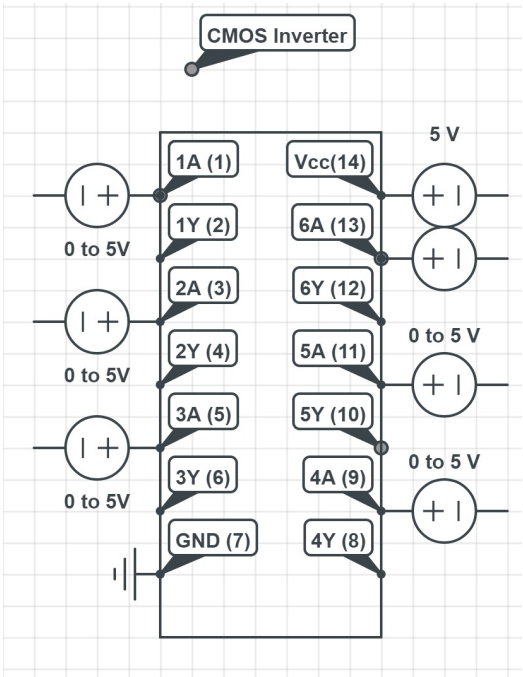

Figure 8: This shows CMOS inverter circuit chip setup

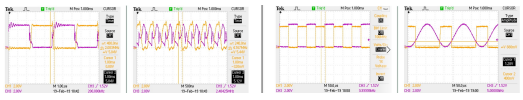

Figure 9: This shows CMOS inverter circuit chip readibgs that it made for the 0 an 1 logic levels

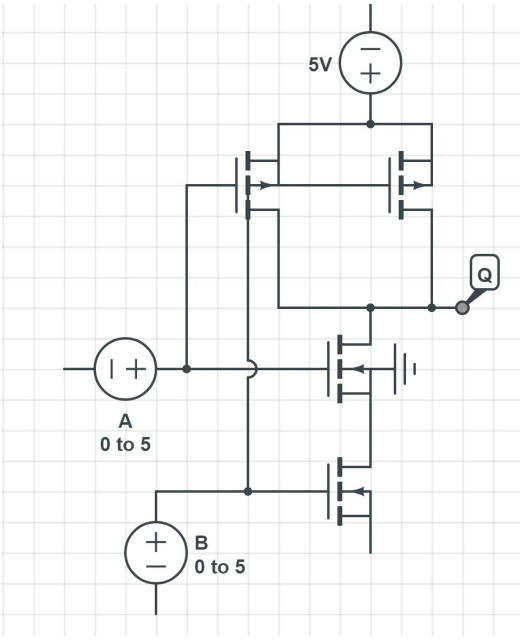

Figure 10: This shows NAND gate we made from NMOS and PMOS MOFSETS

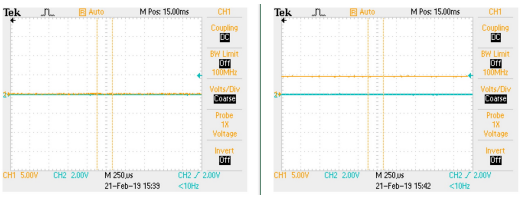

Figure 11: This shows the output for the Homemade NAND circuit

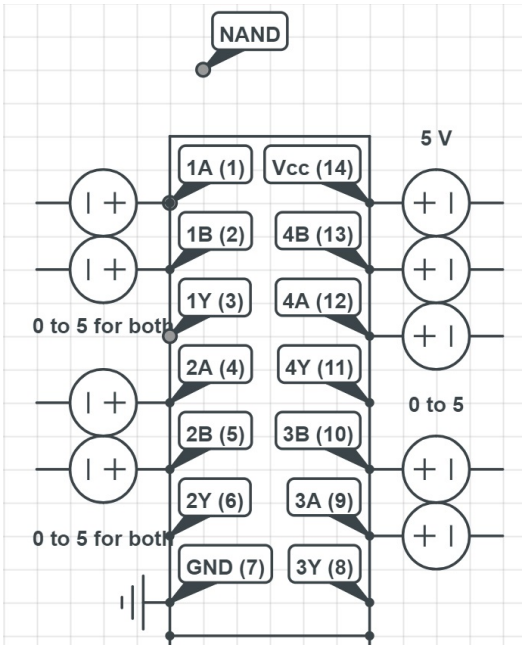

Figure 12: This shows NAND chip diagram and setup

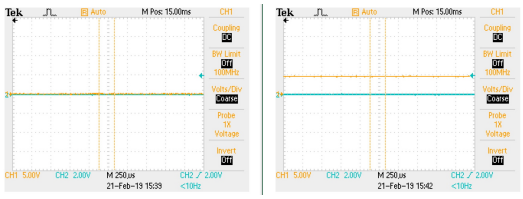

Figure 13: This shows NAND chip readings that it made for two inputs and no inputs