

Physics 117 Lab 8:Introduction to Switches and Displays

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1. On/off logic switch with LED

1.1. Part A

The first part of this lab had us focus on preparing a switch for use in digital circuits, this allows for a current of 5V to be cut on or off with a simple flip. The switch we use is the SPDT switch. To correctly configure the circuits we made sure all inputs were at 0 or 5 and the use of a LED can show whether the switch is on. To work an SPDT we need to connect a wire connecting two switches and run a voltage through 1 input as well as placing a resistor and diode across the output of the gate to indicate if it is receiving logic levels. You can see our circuit in figure 1 and our output in figure 2.

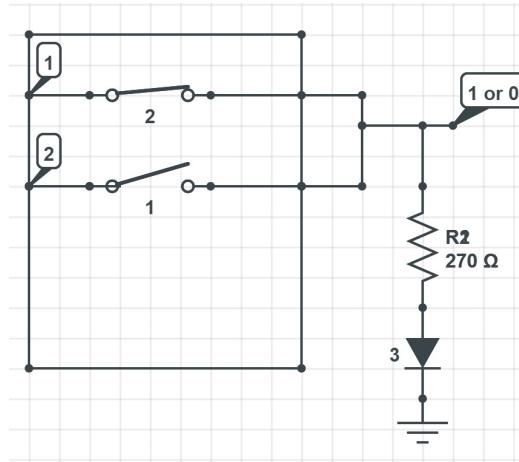


Figure 1: This simple schematic represents SPDT circuit supplying the LED

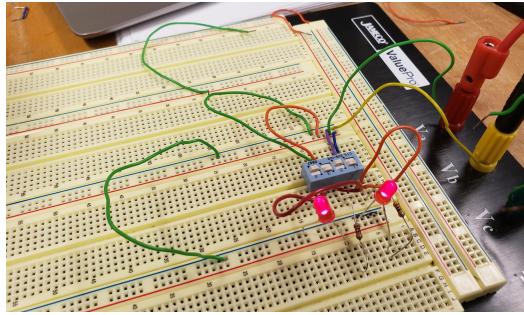


Figure 2: This shows the LED on and off for the SPDT gate

2. Various off-the-shelf Gates

2.1. Part B

The next section simply had us build a wire up various NAND, NOR, and XOR chips and confirm if there logic levels were consistent. To see the chips look at figures 3-5, and to see the logic which they worked in see figure 6. All the chips we viewed were consistent for the truth tables they represent.

3. Applying NAND's to Generate Particular Logic Functions (13-2)

3.1. Part C

The next next section had us create different logic gates by using only NANDS. We were instructed to make an AND, OR, and XOR gate using NANDS. To see how the construction of NAND gates can lead to AND, OR, and XOR respectively look at figures 7,8, and 9.

4. S-R Latch (14-1)

4.1. Part D

The next circuit we had to build was a S-R latch which is a memory circuit, which can be build with NOR gates as seen in figure 10.

4.2. Part E

We are then asked a few things about the S-R latch, first we are asked to drive an LED with its output which we accomplished, then we are asked the question why are they called S and R. S in this case would be Set as it sets a certain memory for the system, as the s channel output feeds the inputs, and then R is reset because it resets the voltage of the system back to zeros. We are then asked which state is the memory state, and that is (0,0) because the system does not change the stored memory and is not inputting or moving in any way it is stagnant; holding whatever is inside.

5. D-type Flip-Flop (14-2)

5.1. Part F

The next section had us use a D-type flip-flop which is basically a chip that flip-flops based the inputs it receives at a point D and saves it as an output of Q, where it takes the last clocked edge. You can see the circuit of the D-type in figure 11. We are asked the following, to set up the circuit in junction with our SPDT switch so we can control when to end the clocking, changing D output, and setting and resetting the circuit, which we are able to accomplish. We are then asked the following questions, confirm that the D flop ignores information presented to Input which it does because it only allows input of the clock is high. We then are asked to assert Reset with a wire, bounce is harmless because we don't expect any change. If we try to clock in a High at D while Resetting meaning that no input is at reset no data is transferred since the circuit is continuously trying to reset. We are lastly asked to assert both set and reset at the same time, and observe what happens, and what happens is we get garbage data because the circuit is again continuously changing itself. We are lastly asked what determines the state the flop rests after release, and the answer is whatever was plugged in last will assert dominance as the circuit basically holds whatever was last given to it when everything is off.

5.2. Part G

For this section we are asked to check the flip flop only changes when Q when clock is rising, which we are able to confirm that it does with some rattiness. We are asked to draw the transition but we simply present the oscilloscope of the transition where a clear indent shows the failure point. We show the output in figure 12

5.3. Part H

We are then asked to place a capacitor at the output along side the resistor and it cleared the ratiness. We can see the circuit diagram with capacitor in figure 13 and the clean output in figure 14

5.4. Part I

The last question we are asked is when Q is on, connect Reset to 0V, and what happens is that it causes the circuit to reset and basically the D type loses whatever it was holding. We are then asked to make the output change by using D and clock which shows that the input D receives is determined when the clock ends/a rising edge. Reset resets the system to 0 and Set does the opposite setting the system to 5 Volts.

6. Seven Segment Display

6.1. Part J

The next section simply had us wire up a 7 segment display LDS-C514RI, it is 7 diodes in parallel to a cathode and we apply a $270\ \Omega$ resistor. We show the circuit diagram in figure 15 and a picture of the display in figure 16.

7. Divide-by-10 and Counter

7.1. Part K

The last segment of the lab had us use a CD4026 decade counter as a divide-by-10 and then input a square wave in the input clock to show its output. The circuit diagram is shown in figure 17 and the output in figure 18. We are also asked to fill out the pin order which is seen in the following table.

Pin	16	5V power
Pin	8	Ground Power
Pin	1	clock input
Pin	5	output
Pin	4	V enable
Pin	2	V inhibit
Pin	15	V reset

7.2. Part L

The last segment of the lab had us connect the 7 segment LED with the CD4026, at 1Hz and see the output, we can also see it jump from 5 to 7 when we move the gates fast enough, due to bounce. The circuit diagram for the final circuit can be seen in figure 19 and the output in figure 20.

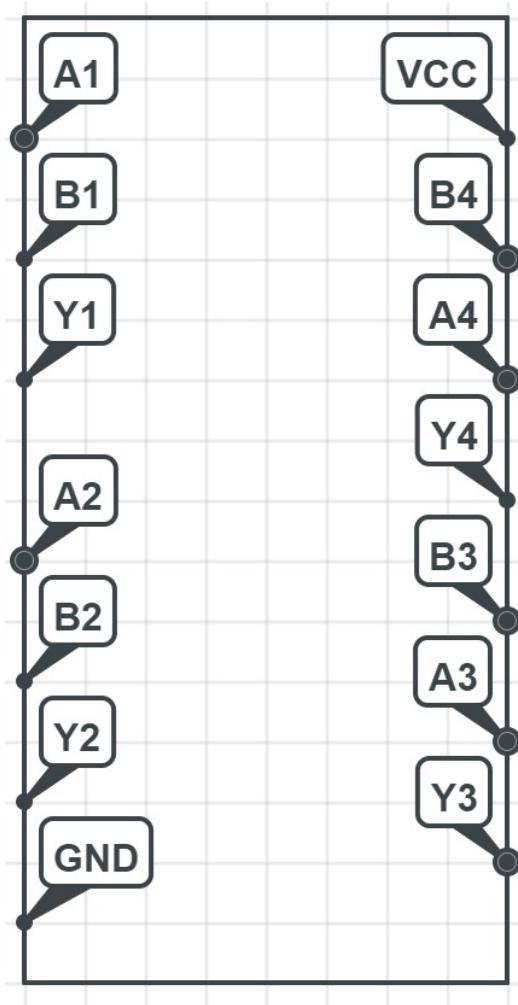


Figure 3: This shows the NAND chip

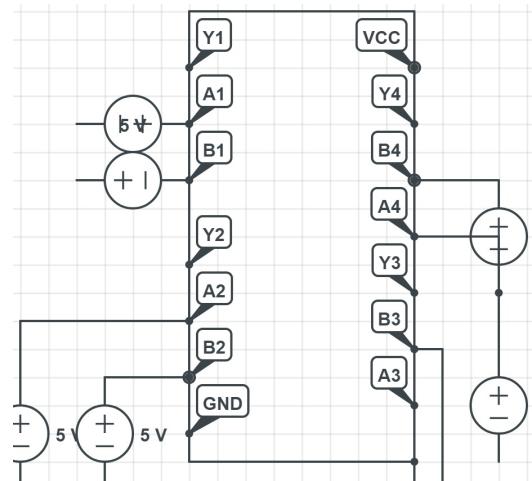


Figure 4: This shows the NOR chip

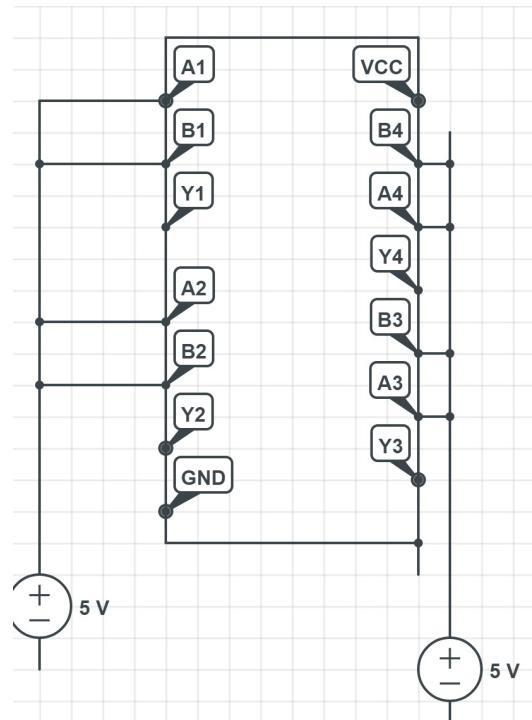


Figure 5: This shows the XOR chip

NAND		
A	B	Q
0	0	1
1	0	1
0	1	1
1	1	0

NOR		
A	B	Q
0	0	1
1	0	0
0	1	0
1	1	0

XOR		
A	B	Q
0	0	0
1	0	1
0	1	1
1	1	0

Figure 6: This shows The truth tables for NAND, NOR, and XOR

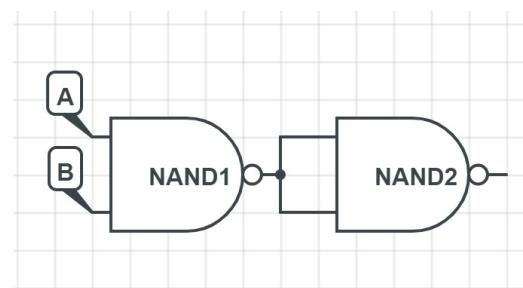


Figure 7: This shows the AND gate created by NAND gates

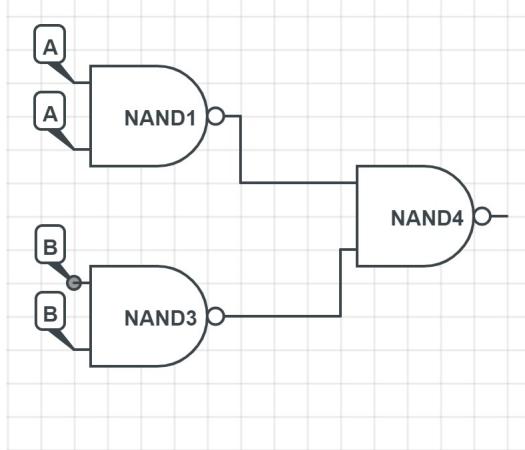


Figure 8: This shows the OR gate created by NAND gates

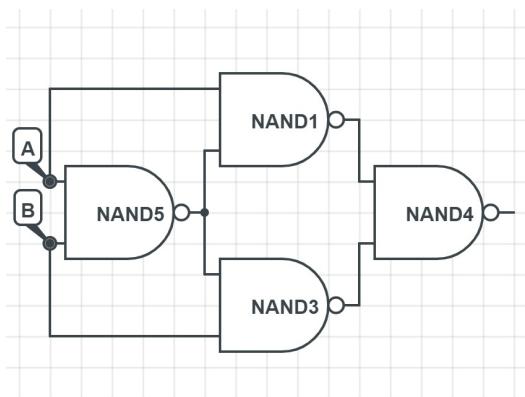


Figure 9: This shows XOR gate created by NAND gates

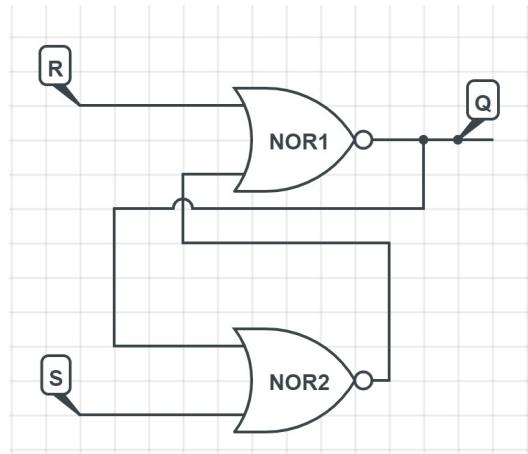


Figure 10: This shows the circuit for the SR latch

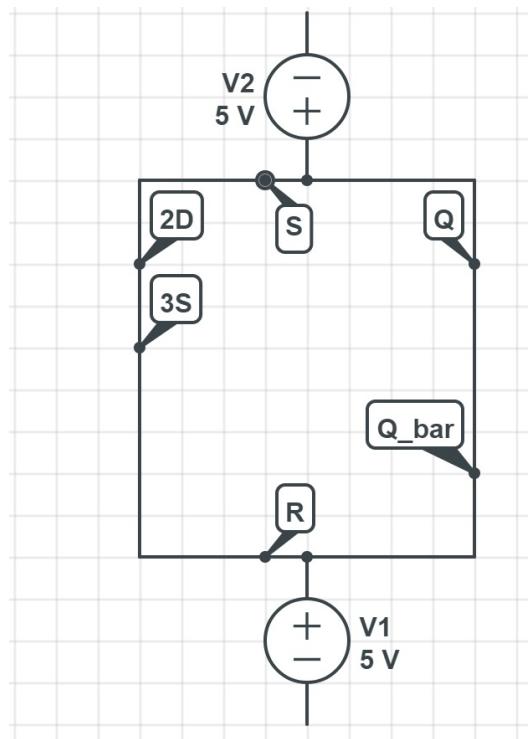


Figure 11: This shows the circuit for the D-type flip flop

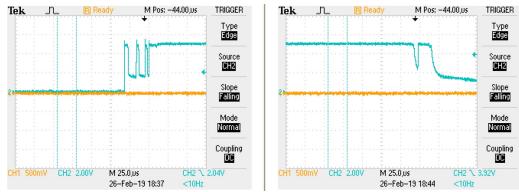


Figure 12: This shows the D-type flip-flop output with some ratiness

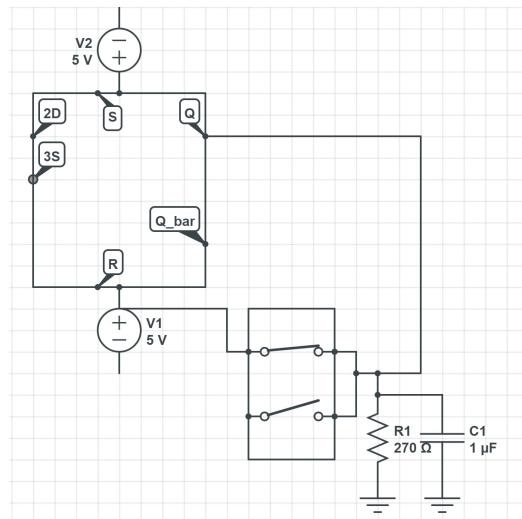


Figure 13: This shows a switch with a capacitor at the end, making the input from Flip-Flop clean

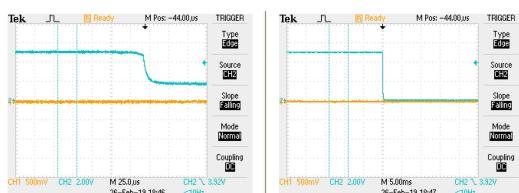


Figure 14: This shows the clean output from the flip-flop

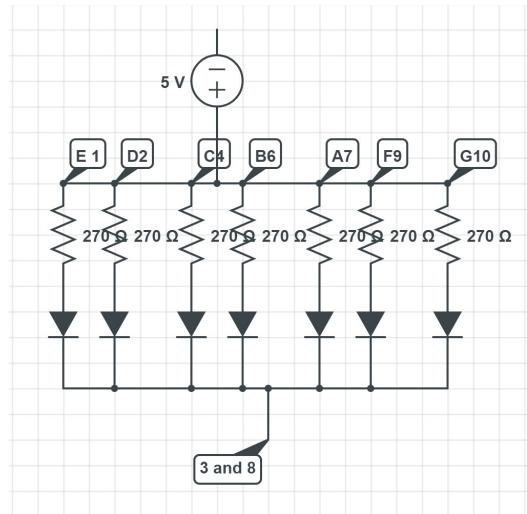


Figure 15: This shows the circuit diagram for 7 segment LED

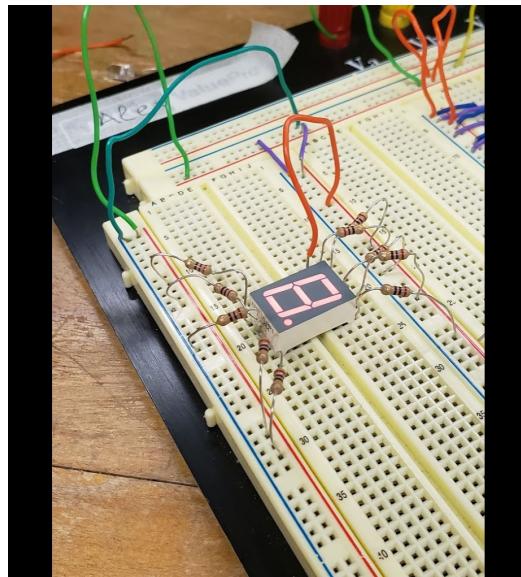


Figure 16: This shows the output of 7 segment LED

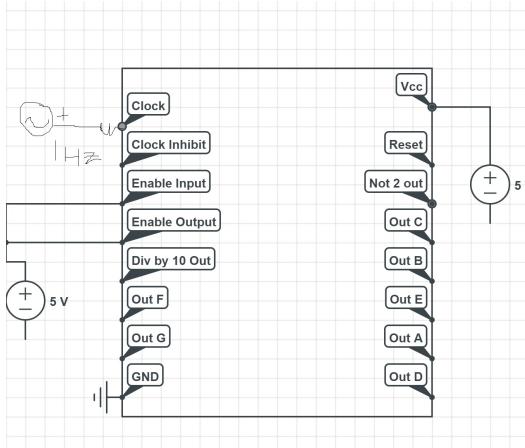


Figure 17: This shows the divide by 10 counter circuit

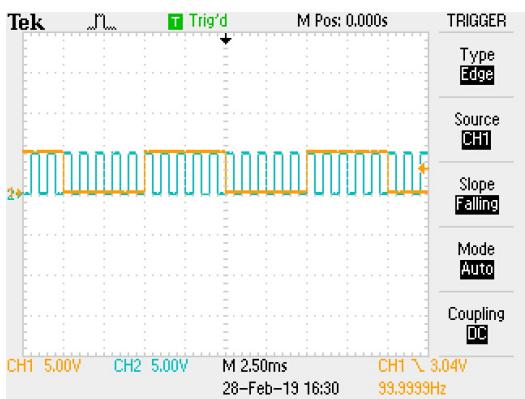


Figure 18: This shows the output for the divider counter

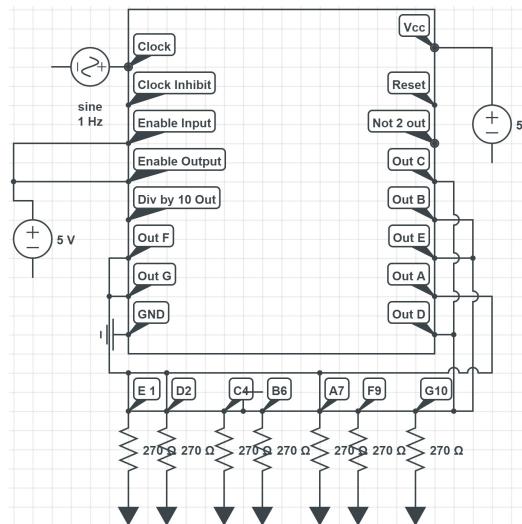


Figure 19: This shows the circuit diagram for LED connected to Counter

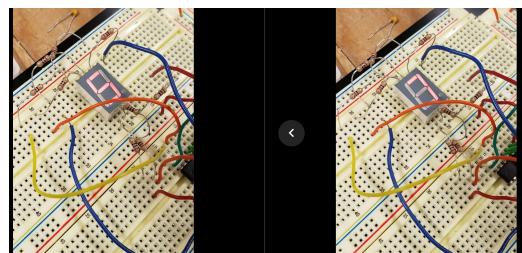


Figure 20: This shows the for the 7 segment LED connected to CD4026 and a bounce output