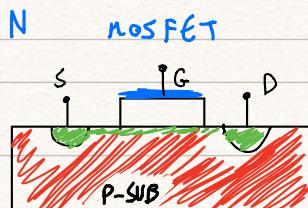


IL TRANSISTORE P-MOSFET (a differenza con l'N mosfet)



- $V_{Tn} > 0$, canale di elettroni
- substrato di tipo P
- zona ohmica
 $V_{GSn} > V_{Tn}$
 $V_{GDr} > V_{Tn}$

$$V_{GD} = V_G - V_D = V_G - V_S + V_S - V_D = V_{GS} - V_{DS}$$

$\hookrightarrow V_{GD} = V_T$
 $V_{GS} - V_{DS} = V_T \rightarrow V_{DS} > V_{GS} - V_T$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} \left[2(V_{GS} - V_{Tn}) V_{DS} - V_{DS}^2 \right]$$

FATTORE E D I TRANS CONDUTTANZA

$$[K_n] = \frac{I}{V^2} \quad \left[\frac{mA}{V^2} \right]$$

$$K_n > 0$$

zona di saturazione

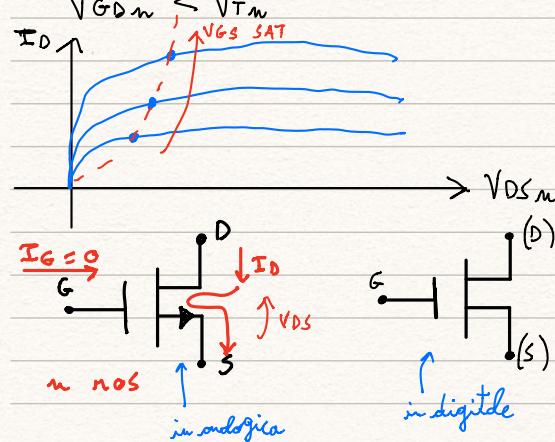
$$V_{GSn} > V_{Tn}$$

$$V_{GDr} < V_{Tn}$$

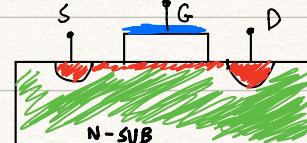
$$I_D = K_n (V_{GS} - V_{Tn})^2$$

mos spento

$$V_{GSn} < V_{Tn} \quad \text{non c'è canale}$$



P MOSFET



- $V_{Tp} < 0$, canale di lacune
- substrato di tipo n
- MOS off, no canale
 $V_{GSp} > V_{Tp}$
 $V_{GDP} > V_{Tp}$
- MOS acceso
 $V_{GSp} < V_{Tp}$ canale laterale source

$V_{GD} < V_{Tp}$
canale laterale drain

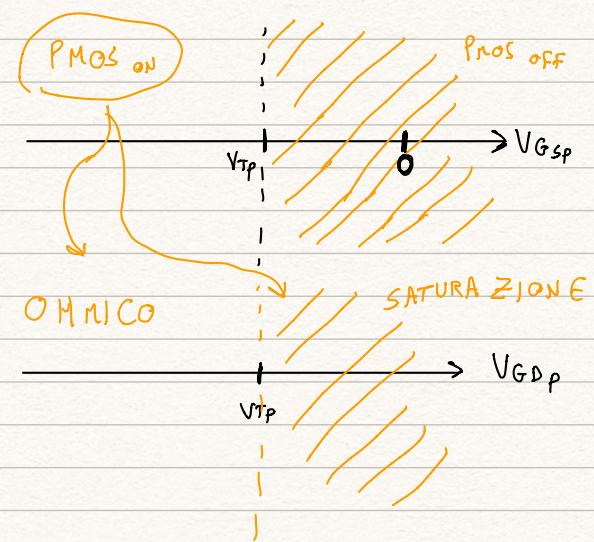
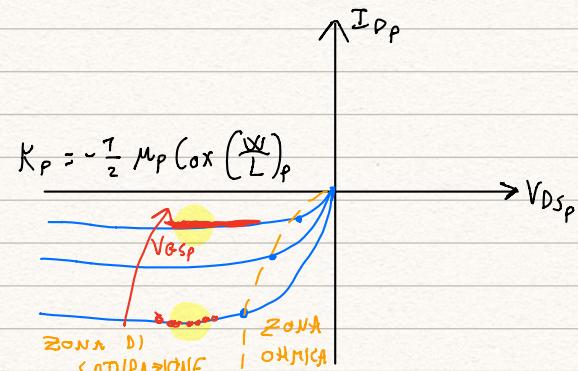
$$I_{Dp} = K_p [2(V_{GSp} - V_{Tp}) V_{DSp} - V_{DSp}^2]$$

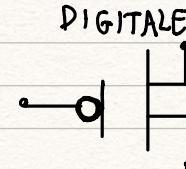
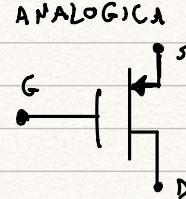
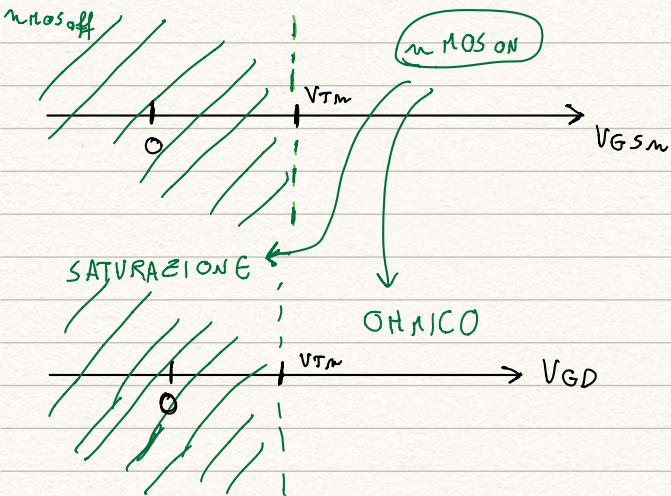
$$V_{GD} > V_{Tp}$$

canale laterale drain
(pinch-off laterale drain)

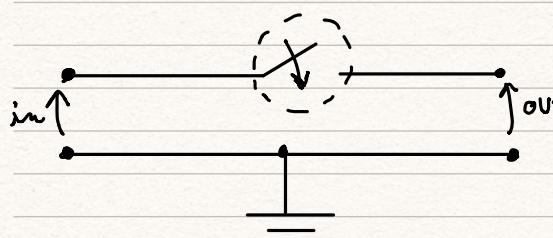
zona di saturazione

$$I_{Dp} = K_p (V_{GSp} - V_{Tp})^2$$





TRANSISTORE MOS COME INTERRUTTORE:



- interruttore aperto ↙ mos aperto ↙ OUT e in collegati ↗ circuito aperto
- interruttore chiuso ↙ mos acceso ↙ OUT e in cortocircuito ↗ cortocircuito
- in zona ohmica

• MOS ACCESO IN ZONA OHMICA:

$$R_{DS_{ON}} \triangleq \left. \frac{\partial V_{DS}}{\partial I_{D_{ON}} \cdot \partial V_{DS}} \right|_{V_{DS}=0} \approx \left[\frac{1}{\frac{\partial I_{D_{ON}}}{\partial V_{DS}}} \right]_{V_{DS}=0}$$

(n mos)

$$I_D = K_m \left[2 (V_{GS_m} - V_{Tn}) V_{DS_m} - V_{DS_m}^2 \right]$$

$$\begin{cases} V_{GS_m} > V_{Tn} \\ V_{GD_m} > V_{Tn} \end{cases}$$

ZONA OHMICA

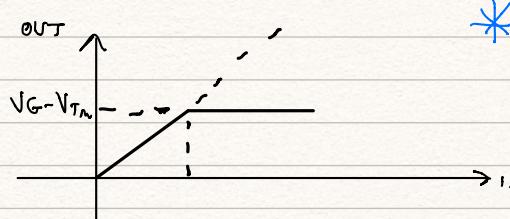
$$\frac{\partial I_{D_{ON}}}{\partial V_{DS}} = 2 K_m (V_{GS_m} - V_{Tn}) - 2 K_m V_{DS_m} \stackrel{V_{DS_m} \neq 0}{=} 0$$

$R_{DS_{ON}} = \frac{1}{2 [V_2 \mu_n C_{ox} (V_{GS_m} - V_{Tn})]}$

TENSIONE DI OVERDRIVE
 $V_{GS_m} - V_{Tn}$

FATTORE DI FORMA
un transistor più "lungo" ha resistenza minore

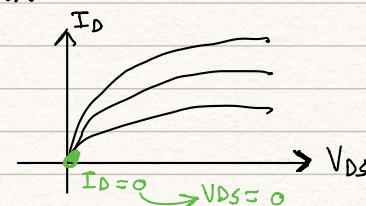
PORTA DI TRASMISSIONE nMOS:



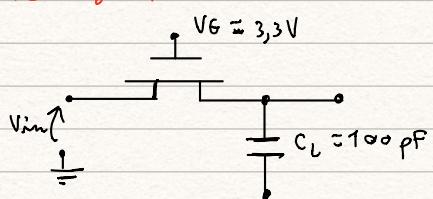
$$V_G - V_{GT} = V_{TN}$$

$$IN = V_G - V_{TN}$$

* $V_{GS} > V_{TN}$ mosfet on



esercizio:



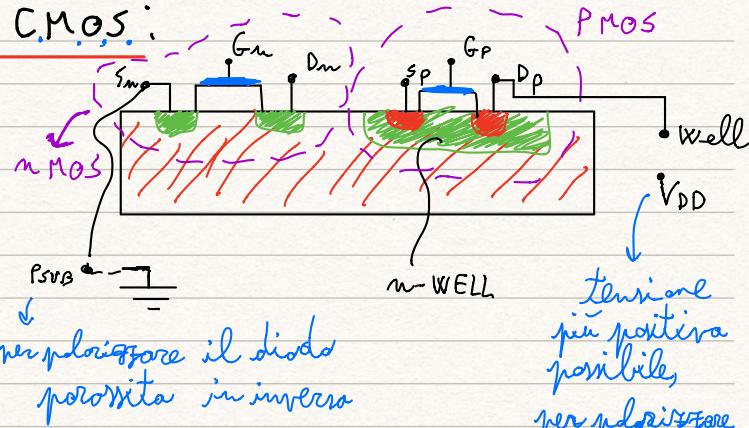
$$V_{TN} = 0,8V$$

(a) V_{out} se $V_{in} = 0V$?
(cerawiti transitori)

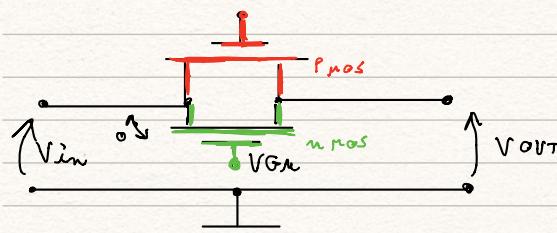
(b) V_{out} se $V_{in} = 3,3V$?
(cerawiti transitori)

PORTA DI TRASMISSIONE C.MOS:

- Complementary
- Metal
- Oxide
- Semiconductor



tensione più positiva possibile per polarizzare il diodo parassita in inverso



$$\ast V_{Gn} = 0, V_{Gp} = 5V - V_{DD}$$

$V_{in} = 0V$ mosfet interdetto

\downarrow
in e out sono collegati

$$\ast V_{Gn} = V_{DD}, V_{Gp} = 0V$$

$$V_{in} = 0V$$

n-MOS on

$$I_D = 0 \rightarrow V_{DS} = 0$$

$$\downarrow$$

$$V_{out} = 0$$

p-MOS interdetto

$$\ast V_{Gn} = V_{DD}, V_{Gp} = 0V$$

$$V_{in} = V_{DD}$$

$$* V_{Gm} = V_{DD}, V_{Gp} = 0V$$

$$V_{in} = V_{DD}$$

pMOS acceso

$$V_{out} = V_{DD}$$

$$V_{out} = V_{in}$$

VANTAGGI:

- $V_{out} = V_{in}$ senza necessità di V_0 maggiore dell'intervallo di tensioni di V_{in}
- $R_{DS_{on,transistor}} = R_{DS_{on,n}} // R_{DS_{on,p}}$, più piccolo di quelli di un solo transistor

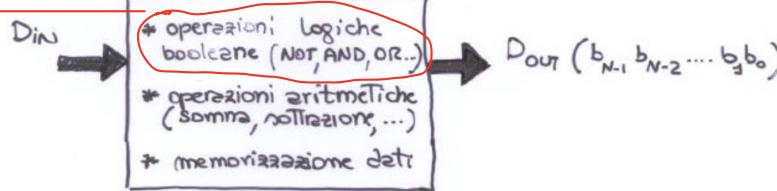
SVENTAGGI:

- 2 transistori complementari con tensioni di comando duali

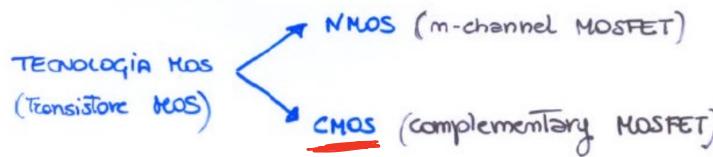
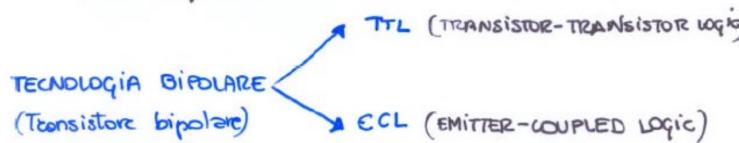
LOGICA CMOS

* SISTEMA DIGITALE

IN QUESTO CORSO

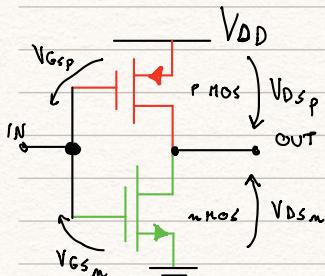


* FAMIGLIE LOGICHE



C. Guazzoni, Fondamenti di Elettronica

INVERTER CMOS:



$$V_{GSn} = IN - 0 = IN$$

$$V_{DSn} = OUT - 0 = OUT$$

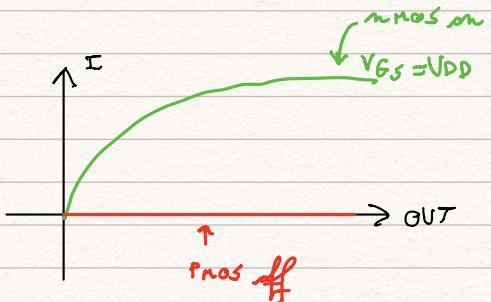
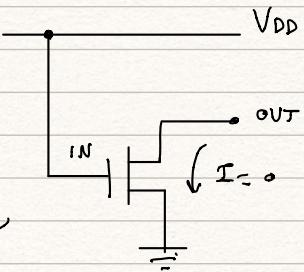
$$V_{GSp} = IN - V_{DD}$$

$$V_{DSp} = OUT - V_{DD}$$

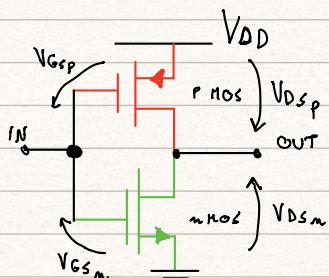
$$IN = 1 \rightarrow IN = V_{DD}$$

$$V_{GSn} = V_{DD} > V_{Tn} \rightarrow nMOS \text{ on}$$

$$V_{GSp} = V_{DD} - V_{DD} = 0 \rightarrow pMOS \text{ off}$$



nMOS chimerico con $V_{DS,n} = 0$
 $\rightarrow OUT = 0V \rightarrow OUT = '0'$



$IN = '0' \rightarrow V_{GS,m} = 0 < V_{T_{on}} \rightarrow nMOS\ off$

$$V_{GS,p} = 0 - V_{DD} = -V_{DD} < V_{T_p}$$

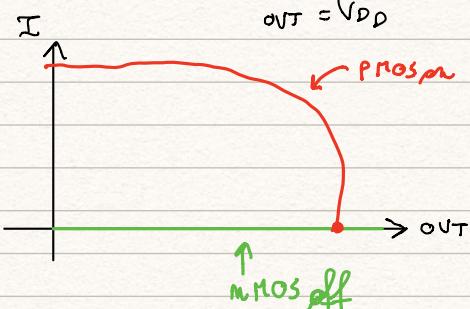
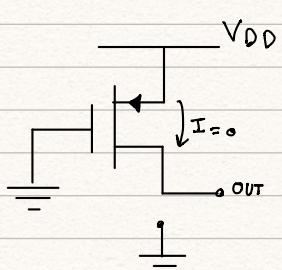
$\rightarrow pMOS\ on$

$$I = 0$$

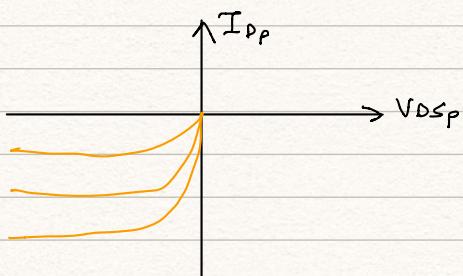
$$V_{DS,p} = 0$$

$$\downarrow$$

$$OUT = V_{DD}$$

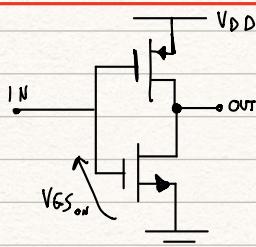
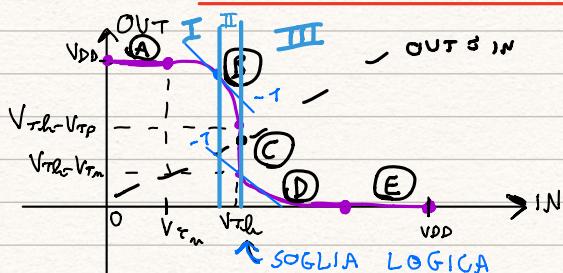


caratteristica I/V pMOS



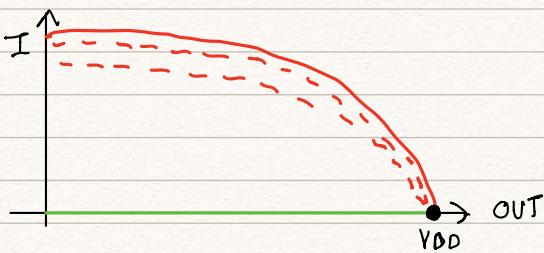
$I_{statica} = 0$ sia per $IN = '0'$ che per $IN = '1'$

CARATTERISTICA DI TRASFERIMENTO STATICA:

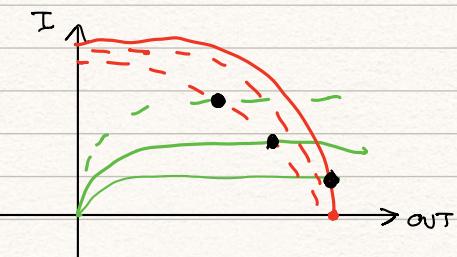


(A) nMOS off

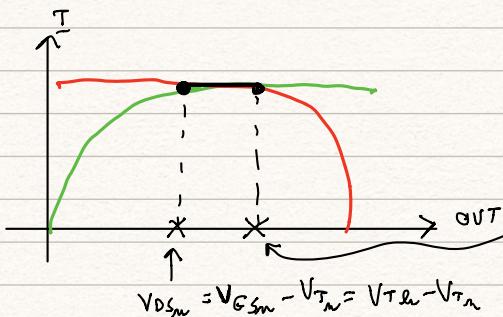
pMOS on in zona ohmica



(B) nMOS on in zona di saturazione
pMOS on in zona ohmica



(C)



$$\text{pMOS} \quad V_{DSp} = V_{GSp} - V_{Tp}$$

$$OUT - V_{DD} = IN - V_{DD} - V_{Tp} \rightarrow OUT = V_{Th} - V_{Tp}$$

$$V_{DSn} = V_{GSn} - V_{Tn} = V_{Th} - V_{Tn}$$

INVERTER SIMMETRICO

$$\frac{1}{2} \mu_n C_o x \left(\frac{w}{L} \right)_n = \frac{1}{2} \mu_p C_o x \left(\frac{w}{L} \right)_p \rightarrow \mu_n \left(\frac{w}{L} \right)_n = \mu_p \left(\frac{w}{L} \right)_p$$

$$\rightarrow K_n = |K_p|$$

CALCOLO DELLA SOGLIA LOGICA:

$$I_{Dn, \text{sat}} = |I_{Dp, \text{sat}}|$$

$$K_n (V_{GSn} - V_{Tn})^2 = |K_p| (V_{GSp} - V_{Tp})^2$$

inverter simmetrico

$$K_n = |K_p|$$

$$(IN - V_{Tn})^2 = [(IN - V_{DD}) - V_{Tp}]^2 \quad V_{Tn} = |V_{Tp}| = V_T > 0$$

$$(IN - V_T)^2 = [(IN - V_{DD}) + V_T]^2$$

estraggo le radici quadrate

$$IN - V_T = -[(IN - V_{DD}) + V_T]$$

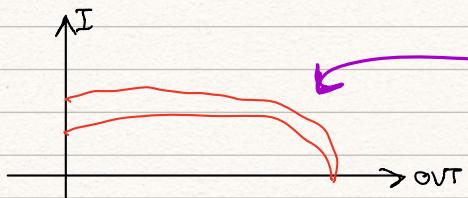
$$IN - V_T = -IN + V_{DD} - V_T$$

$$2IN = V_{DD}$$

$$IN \stackrel{\Delta}{=} V_{Th} = \frac{V_{DD}}{2}$$

\rightarrow SOGLIA LOGICA DI COMMUTAZIONE

①



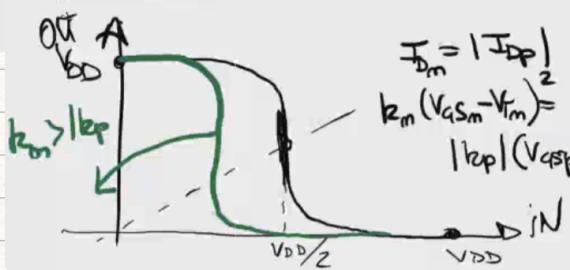
$V_{IL} = \max \text{ in interpretato come livello logico basso}$

$V_{IH} = \min \text{ in interpretato come livello logico alto.}$

EFFETTO DELLA TENS. DI ALIMENTAZ.



INVERTER NON SIMMETRICO



$$I_Dm = |I_{DP}|$$

$$k_m(V_{GSm} - V_{Im})^2 = |k_{pL}|(V_{GSP} - V_{Tp})^2$$

