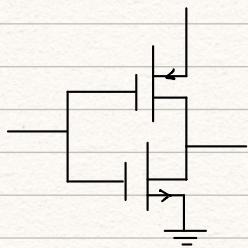


POTENZA NEI CMOS:

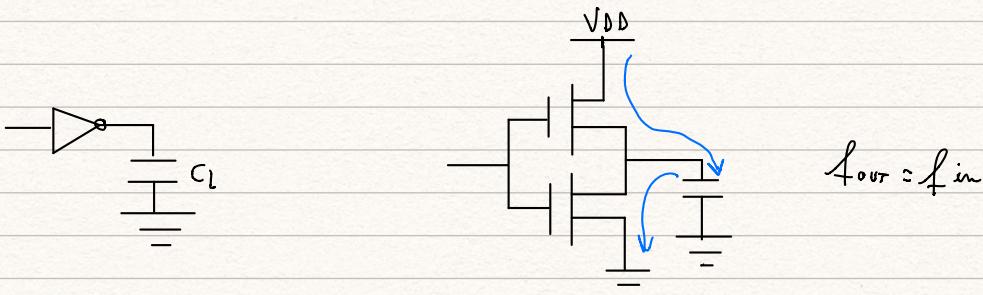


POTENZA DISSIPATA:

3 POSSIBILI CONTRIBUTI:

- POTENZA STATIC A → NULLA

- POTENZA DI COMMUTAZIONE



$$Q_{CL} = C_L \cdot \Delta V_{CL}$$

$$E = C_L \Delta V_{CL} \cdot V_{DD}$$

$$P_{comm} = C_L \Delta V_{CL} \cdot V_{DD} \cdot f_{out}$$

$$\downarrow$$

$$P_{comm} = C_L \cdot V_{DD}^2 f_{out}$$

dall'esercizio della scorsa esercitazione:

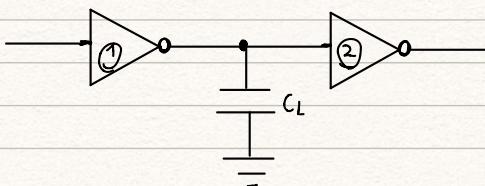
$$f_{in} = f_{CLK} : 100 \text{ MHz}$$

$$C_L = 0,5 \text{ pF}$$

$$V_{DD} = 5 \text{ V}$$

$$P_{comm} = 0,5 \text{ pF} \cdot 25 \text{ V}^2 \cdot 100 \text{ MHz} = 1,25 \text{ mW}$$

- POTENZA DI CROSS CONDUZIONE

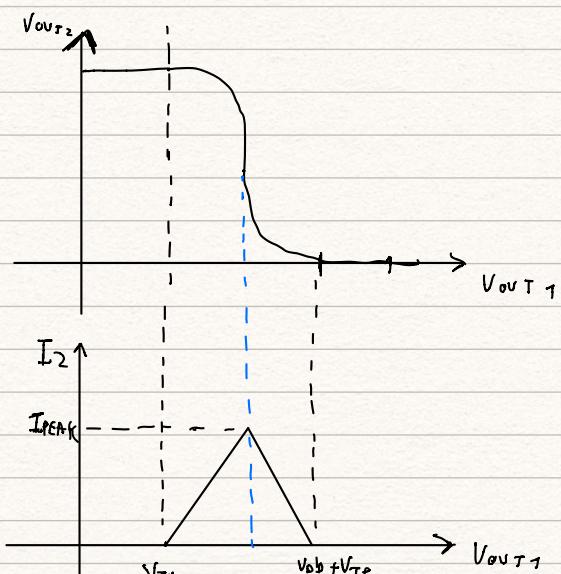


$$I_{PEAK} = I_{DSAT}$$

$$V_{GS} = V_{TH}$$

$$I_{PEAK} \approx 150 \mu\text{A}/V^2 (\text{?}, 3,5 \text{ V})$$

$$I_{cc} = I_{PEAK} \cdot V_{DD} + V_{TP} - V_{TN} \approx 147 \mu\text{A}$$

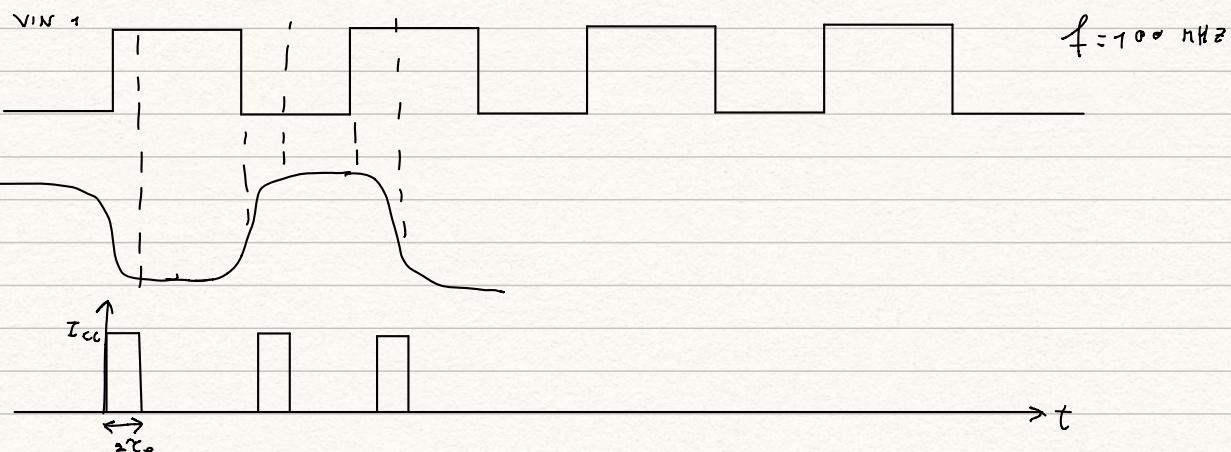




Approssimo il tempo totale di commutazione della porta con $2\tau_p$

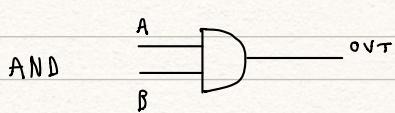
Sceglio τ_p calcolato con approssimazione ③ (I_{DSS} + R_g)

$$\tau_p = 561 \text{ ps}$$



$$P_{CC} = (I_{CC} \cdot 2\tau_p \cdot 2 \cdot f_{in}) V_{DD} = 147 \mu\text{A} \cdot 2 \cdot 561 \text{ ps} \cdot 2 \cdot 100 \text{ nHz} \cdot 5 \text{ V} = 165 \mu\text{W}$$

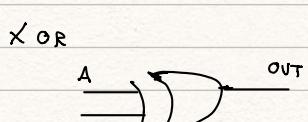
PORTE LOGICHE PRINCIPALI:



A	B	OUT
0	0	0
0	1	0
1	0	0
1	1	1



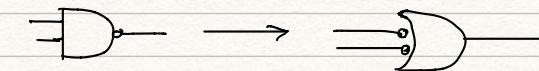
A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	1



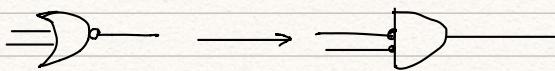
A	B	OUT
0	0	0
0	1	1
1	0	1
1	1	0

LEGGI DI DE MORGAN

$$\overline{xy} = \bar{x} + \bar{y}$$

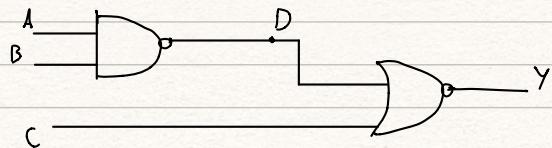


$$\overline{x+y} = \bar{x} \cdot \bar{y}$$



esercizio 0:

$$V_{DD} = 5V$$

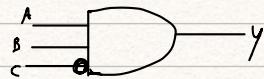


1) funzione logica e tabella della verità

$$Y = \overline{c+d}$$

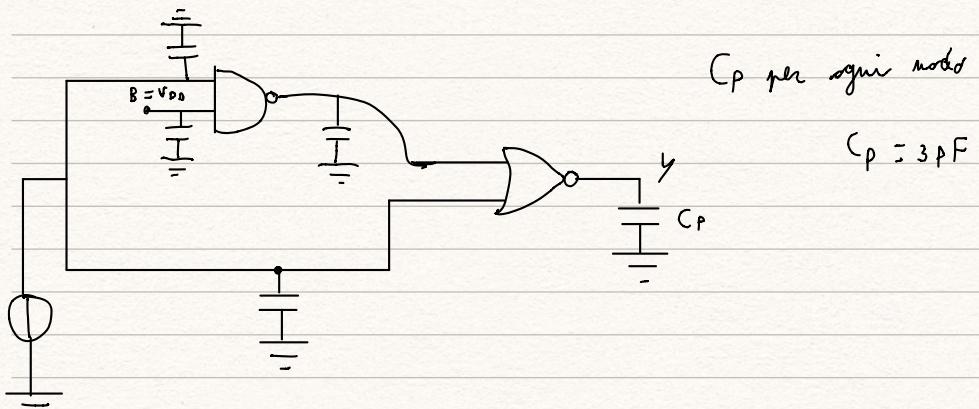
$$Y = \overline{c + \overline{a \cdot b}} = \bar{c} \cdot a \cdot b$$

$$D = \overline{a \cdot b}$$



A	B	C	D	OUT
0	0	0	1	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	1	0
1	0	1	1	0
1	1	0	0	1
1	1	1	0	0

esercizio 1:



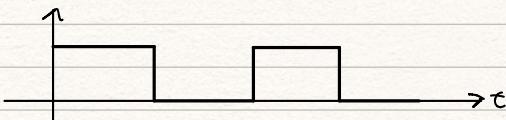
C_p per ogni nodo

$$C_p = 3 \text{ pF}$$

V_{CK} con $f_{CK} = 2 \text{ MHz}$

$$\tau_p = 0$$

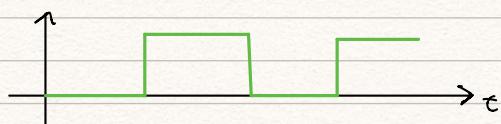
Calcolare la potenza dissipata dalle porte logiche:



$$f_D = f_{CK}$$

$$\Delta V_{CPD} = V_{DD}$$

$$P_{COMM_D} = C_p \cdot V_{DD}^2 \cdot f_{CK} = 3 \text{ pF} \cdot 2.5V^2 \cdot 2 \text{ MHz}^2 = 150 \mu\text{W}$$



NON COMMUTA

3) Si ipotizzi di cambiare la tecnologia con utilizzata, dimezzando V_A e C_p

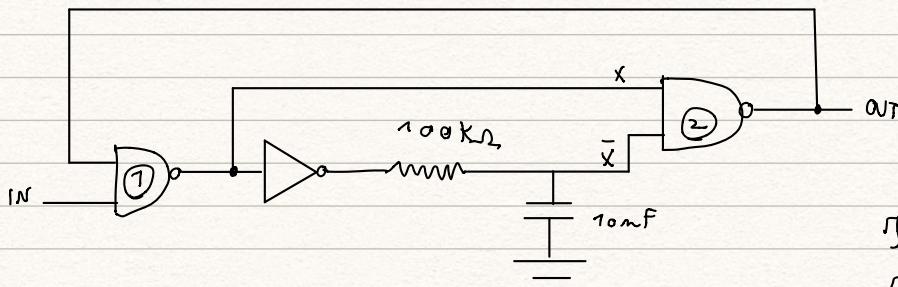
Di quanto posso aumentare f_{CK} mantenendo invariata la P_{DISS} ?

$$P_{DOL} = f_{CKAD} \cdot C_p \cdot V_{DD}^2$$

$$P_{NGW} = f_{CK_{NEW}} \cdot \frac{C_F}{2} \left(\frac{V_{DD}}{2}\right)^2 \approx f_{CK_{NEW}} \cdot C_p \cdot \frac{V_{DD}^2}{8}$$

$$f_{CK_{NEW}} = 8 f_{CK_{OLD}}$$

Esercizio 2

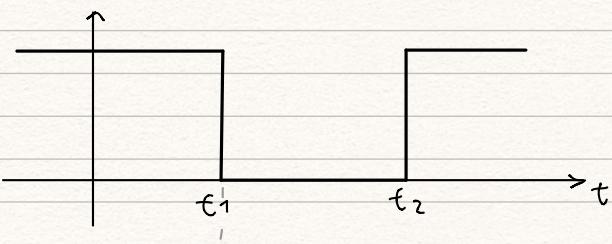


In condizioni statiche la NAND riceve in ingresso X e \bar{X}

$$OUT_2 = 1$$

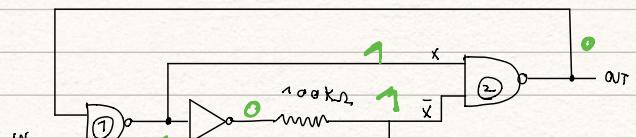
Si considerino porte con $V_{TH} = \frac{V_{DD}}{2}$, $T_P = 0$

Si consideri come ingresso

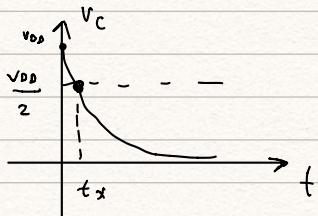
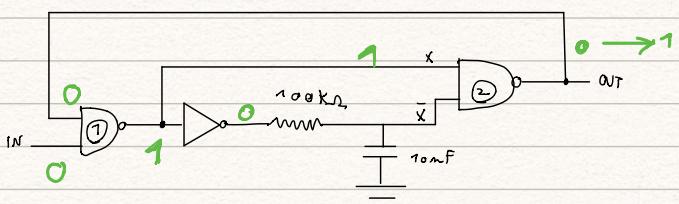


$$\Delta t_{low,in} = t_2 - t_1 = 15$$

$$V_C(t) = V_{DD} \quad \text{per } t < t_1$$



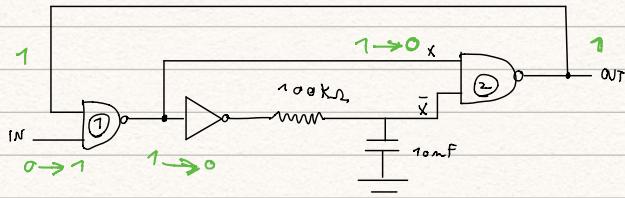
\leftrightarrow
 $690 \mu s$



$$V_C \approx 5V e^{-t/\tau} \quad \tau = 100 k\Omega \cdot 10 nF = 1 \mu s$$

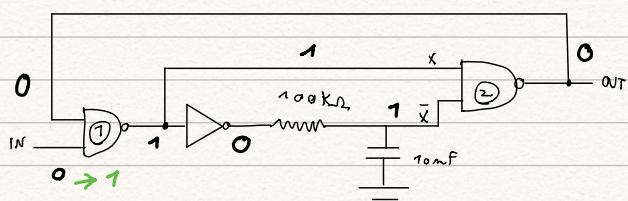
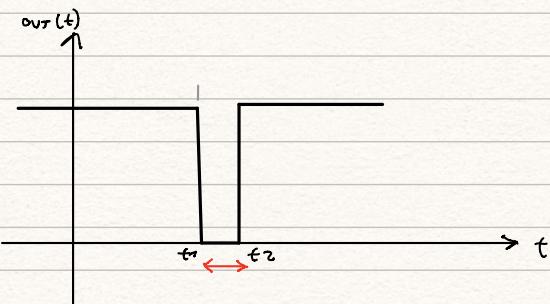
$$V_C(t_K) : \frac{V_{DD}}{2} \rightarrow t_K = 0,69 \tau = 690 \mu s$$

per t appena prima di t_2

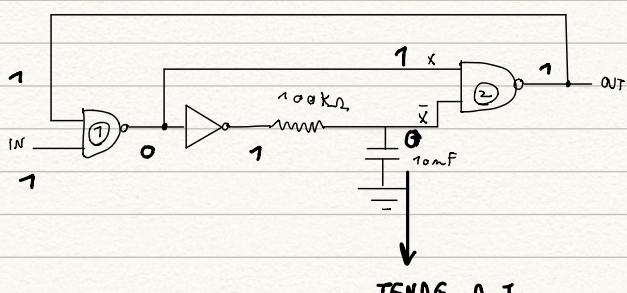
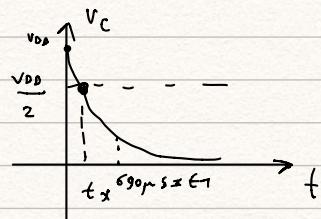


$$2) \text{ Lìa ora } t_2 - t_1 = 20 \mu s$$

per $t = t_1$ per $t = t_2$



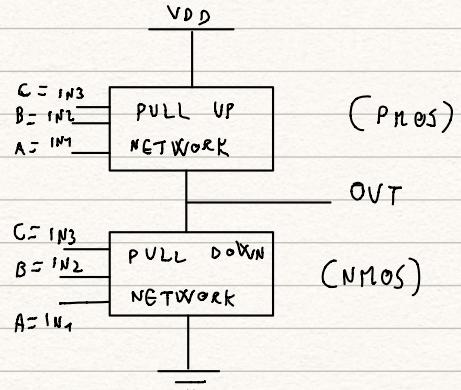
per $t = t_1 + 690 \mu s$



MONOSTABILE

TENDE A 1

porte logiche CMOS:



$$OUT = f(\bar{A}, \bar{B}, \bar{C})$$

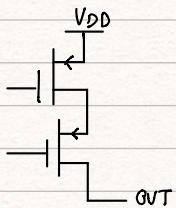
$$\overline{OUT} = f(A, B, C)$$

NOR

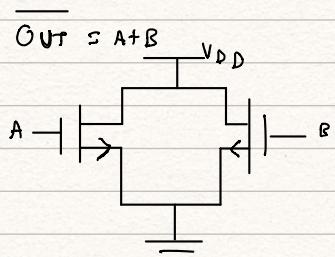
$$OUT = \overline{A+B}$$

$$OUT = \bar{A} \cdot \bar{B}$$

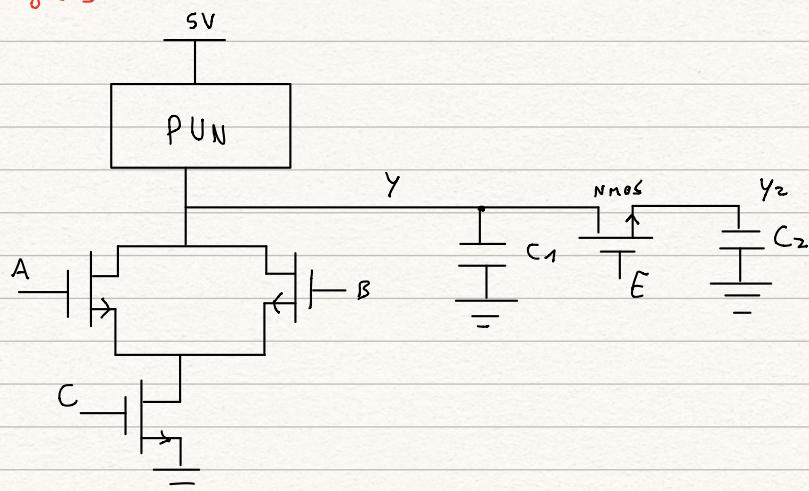
per costruire PUN



per costruire PDN



Esercizio 3 :



$$V_{TN} = |V_{TP}| = \tau v$$

$$K_m = |K_p| = 2mA/V^2$$

$$C_1 = C_2 = 1\text{ pF}$$

$$f_{CK} = 1\text{ MHz}$$

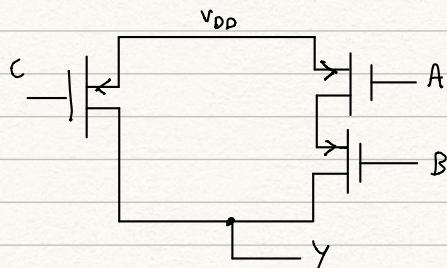
Si consideri E = 0

1) funzione logica $Y = f(A, B, C)$

$$Y = 0 \text{ se } C \cdot (A+B)$$

2) Disegnare la PUN

$$Y = \overline{C(A+B)} \approx \bar{C} + \overline{A+B} = \bar{C} + \bar{A} \cdot \bar{B}$$

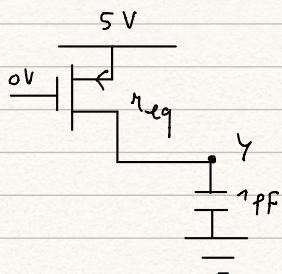


$$Y = C \cdot (A+B)$$

3) Calcolare il tempo di propagazione di Y per arrivare a $\frac{V_{DD}}{2}$ nel caso pessimo

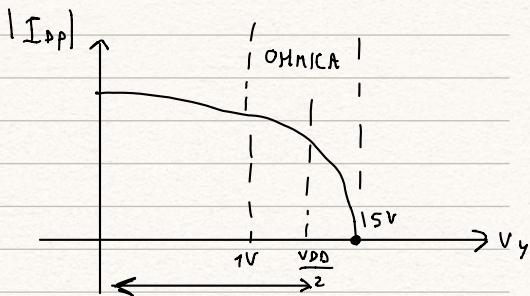
t_{PLH} attraverso via di $pnas_1$ e $pnas_2$

$$|K_{eq}| = |K_A|_1 / |K_B| = \frac{|K_P|}{2} = 1 \text{ mA}/\text{V}^2$$



$$\text{con } |K_{eq}| = 1 \text{ mA}/\text{V}^2$$

$$|V_{TP}| = 1V$$



Sceglio di calcolare

$$t_{PLH} = t_{PLH}^{SAT} + t_{PLH}^{OHMICA}$$

$$|I_{SAT}| = |K_{eq}| (V_{GS} - V_{TP})^2 = 1 \text{ mA}/\text{V}^2 (-5V + 1)^2 = 16 \text{ mA}$$

$$t_{PLH}^{SAT} = \frac{C_1}{|I_{SAT}|} \cdot \Delta V_C^{SAT} = \frac{1 \text{ pF}}{16 \text{ mA}} \cdot 1V = 62,5 \text{ ps}$$

$$t_{PLH}^{OHMICA} \quad \text{considerando } R_{eq} = \frac{5V - 1V}{|I_{SAT}|} = \frac{6V}{16 \text{ mA}} \sim 250 \Omega$$

$$V_{out}(t) = 1V + 4V(1 - e^{-\frac{t}{R_{eq}}}) \quad ?$$

$$t_{PLH} = 62,5 \text{ ps} + 117,5 \text{ ps} = 180 \text{ ps}$$

4) Verificare che $t_{PHL} = t_{PLH}$

4 - P_{DIN} con $A=B=C$ si considera sonda quadrata di $f_{CK} = 1 \text{ MHz}$

nei casi $E=0$ e $E=1$

$$\textcircled{1} \quad E=0 \quad f_Y = f_{CK}$$

$$P_{DIN} = C_1 \cdot V_{DD}^2 \cdot f_{CK} = 2,5 \text{ uW}$$

② $E=1$

Si somma anche $V_2 = \alpha V_1 + V_{TN}$

$$P_{DIN} = C_1 \cdot V_{DD}^2 \cdot f_{CE} + C_2 (V_{DD} - V_{TN}) \cdot V_{DD} \cdot f_{CE} = 25 \mu W + 20 \mu W = 45 \mu W$$