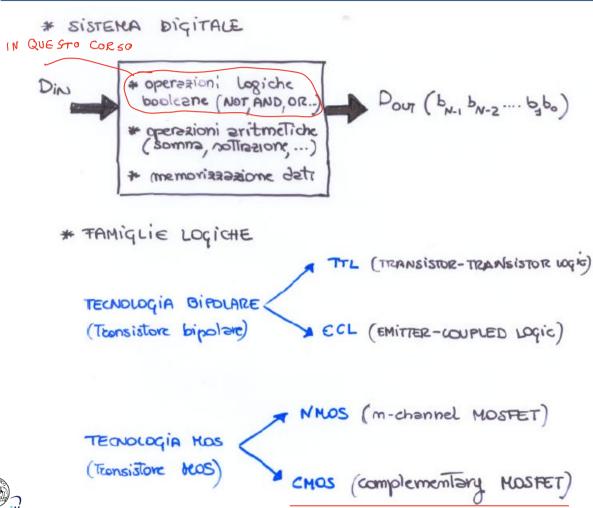
LOGICA CMOS

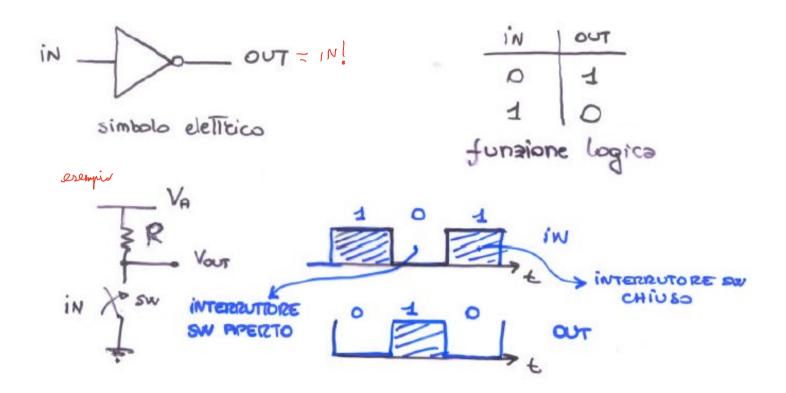




COME SI ANALIZZA UNA PORTA LOGICA?

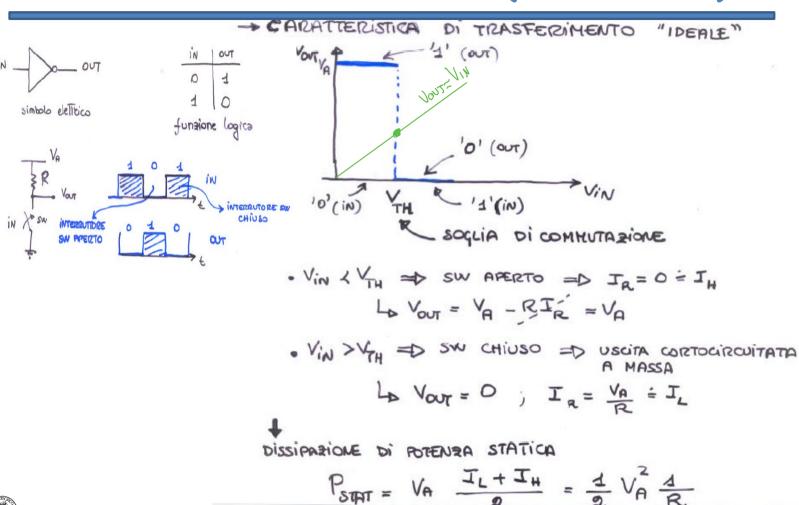


INVERTITORE LOGICO (NOT GATE)





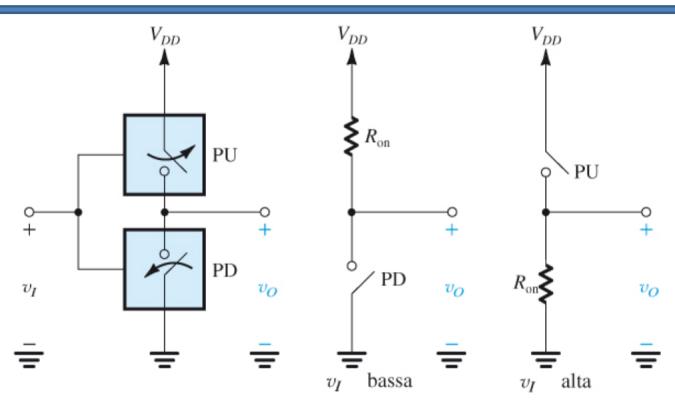
INVERTITORE LOGICO (NOT GATE)



THE MORNING C. Guazzoni, Fondo

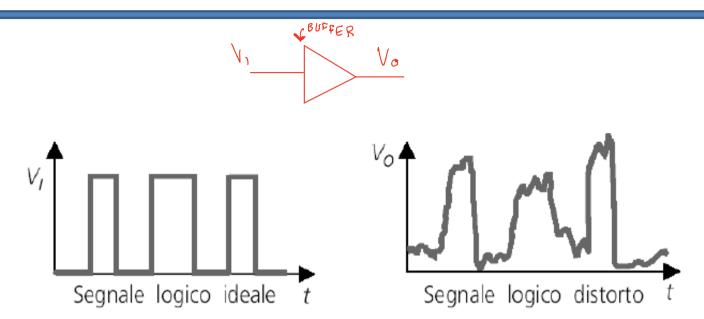
C. Guazzoni, Fondamenti di Elettronica

INVERTITORE LOGICO A 2 INTERRUTTORI

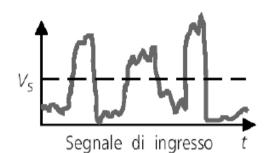


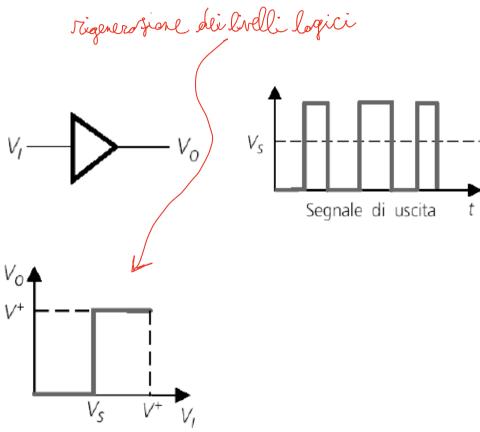
- ✓ La rete di pull-up e' costituita da un interruttore controllato in tensione che si chiude quando V₁e' bassa. La rete di pull-down e' costituita da un interruttore controllato in tensione che si apre quando V₁e' bassa.
- ✓ La dissipazione di potenza statica e' nulla

SEGNALE LOGICO



BUFFER LOGICO

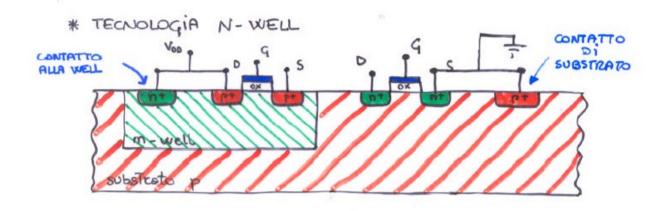


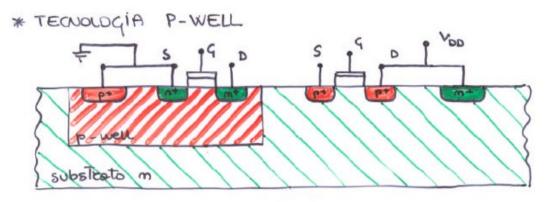


Caratteristica di trasferimento



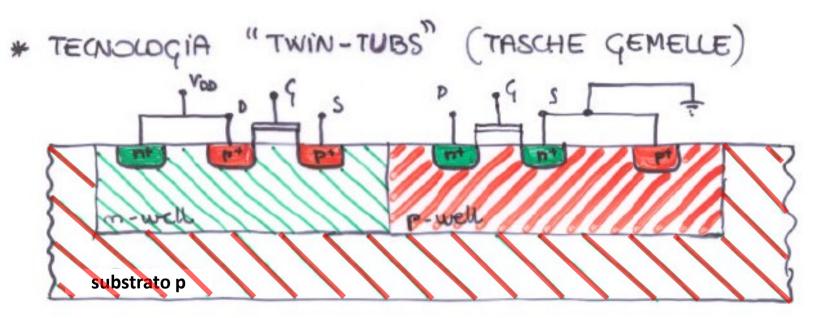
TECNOLOGIE CMOS (Complementary Metal Oxide Silicon)







TECNOLOGIE CMOS (Complementary Metal Oxide Silicon)





TECNOLOGIA DI FABBRICAZIONE DI CIRCUITI INTEGRATI - PROCESSO CMOS







