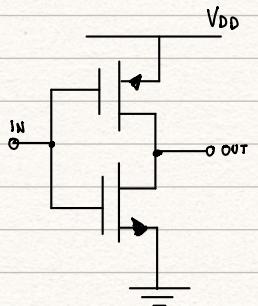


INVERTER CMOS - MARGINI DI RUMORE:

(NOISE MARGINS)



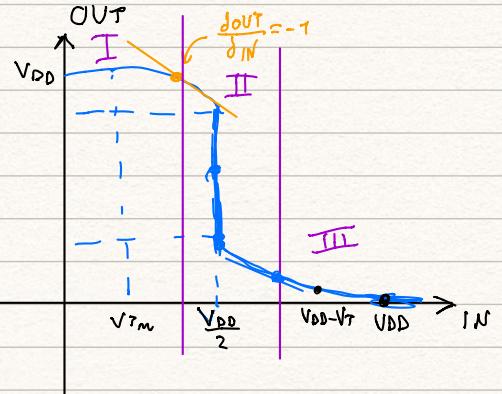
$$V_{Tm} = |V_{Tp}| = V_T$$

$K_m = |K_p|$ INVERTER SIMMETRICO

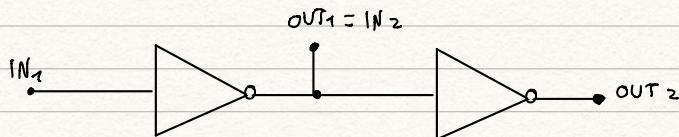
$$\left(\frac{W}{L}\right)_p = 2 \cdot S \left(\frac{W}{L}\right)_n$$

V_{iL} tale che $IN < V_{iL} \rightarrow OUT = '1'$

V_{iH} tale che $IN > V_{iH} \rightarrow OUT = '0'$



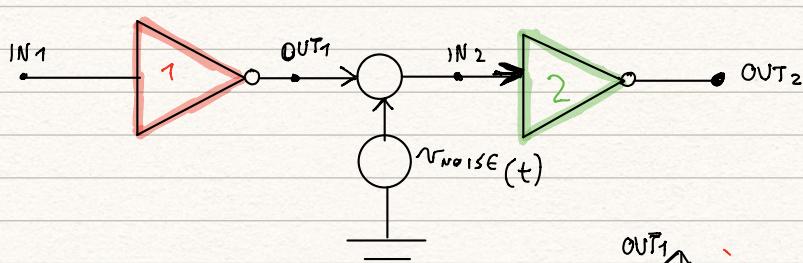
II: ZONA DI TRANSIZIONE



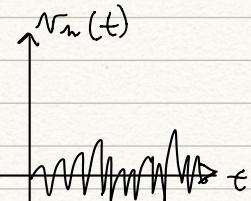
$IN_1 = '1' \rightarrow OUT_1 = '0' \rightarrow IN_2 = '0' \rightarrow OUT_2 = '1'$

$$OUT_2 = \overline{IN_2} = \overline{OUT_1} = \overline{\overline{IN_1}} = IN_1$$

nella realtà però:



$$IN_2 = OUT_1 + v_{noise}(t)$$

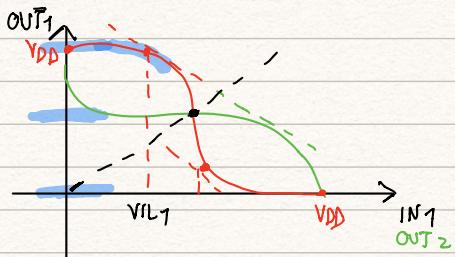


↗ NOISE MARGIN LOW

$$N_{NL} \triangleq V_{iL} - 0 = V_{iL}$$

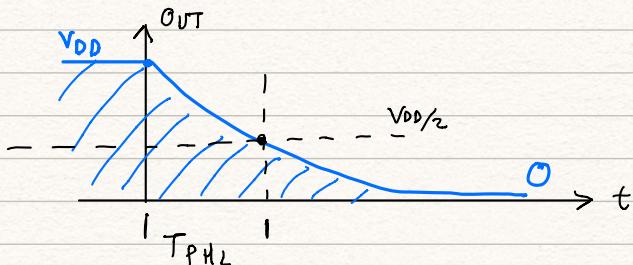
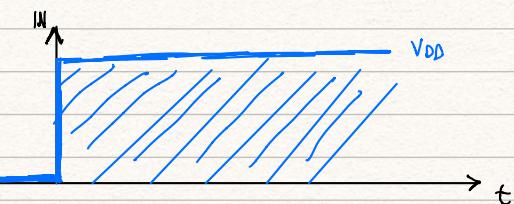
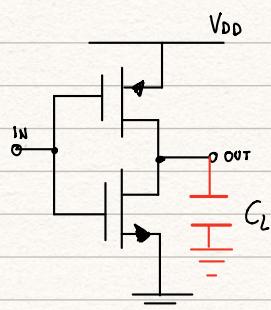
$$N_{MH} \triangleq V_{DD} - V_{iH}$$

↘ NOISE MARGIN HIGH



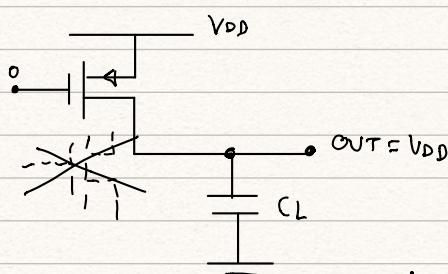
inverter simmetrici $\rightarrow N_{NL} = N_{MH}$

COMPORTAMENTO DINAMICO INVERTER CMOS:

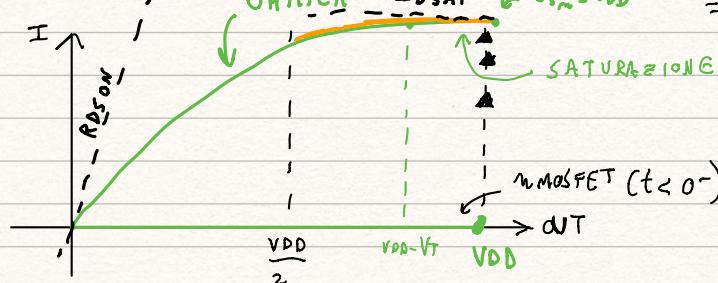
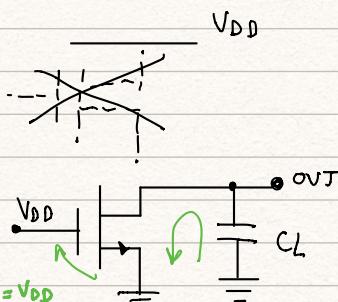


- t_{PHL} : TEMPO DI PROPAGAZIONE ALTO-BASSO: tempo necessario perché l'uscita raggiunga il 50% del suo valore ($V_{DD}/2$)
- t_{PLH} : TEMPO DI PROPAGAZIONE BASSO-ALTO: tempo necessario perché $V_{OUT} = \frac{V_{DD}}{2}$

per $t \leq 0^-$

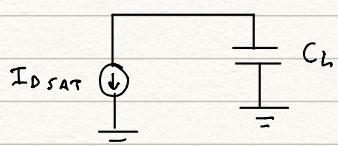


per $t \geq 0^+$



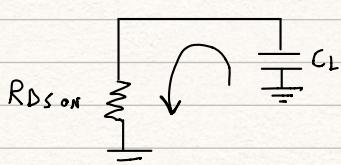
APPROXIMAZIONE SATURA

$$I_{DSAT} = K_m (V_{GS} - V_{TM})^2 = K_m (V_{DD} - V_{TM})^2$$



$$t_{PHL} = \frac{Q_{50\%}}{I_{DSAT}} = \frac{C_L (V_{DD} - V_{DD}/2)}{K_m (V_{DD} - V_{TM})^2} = \frac{C_L V_{DD}/2}{K_m (V_{DD} - V_T)}$$

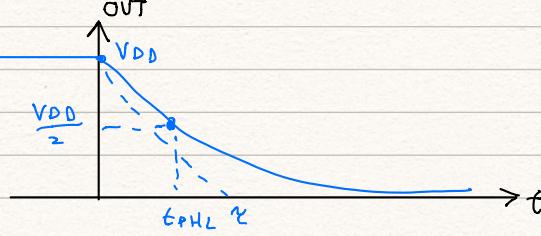
APPROXIMAZIONE OHMICA:



$$\tau = R_{DSon} C_L$$

$$R_{DSon} \approx \left| \frac{\partial V_S}{\partial I_{DSon}} \right| \Big|_{V_{DS}=0} = \frac{1}{2K_m (V_{DD} - V_{TM})}$$

$$OUT = V_{DD} \exp(-t/\tau)$$



$$\frac{V_{DD}}{2} = V_{DD} \exp\left(-\frac{t_{PHL}}{\tau}\right)$$

$$\frac{1}{2} = \exp\left(-\frac{t_{PHL}}{\tau}\right)$$

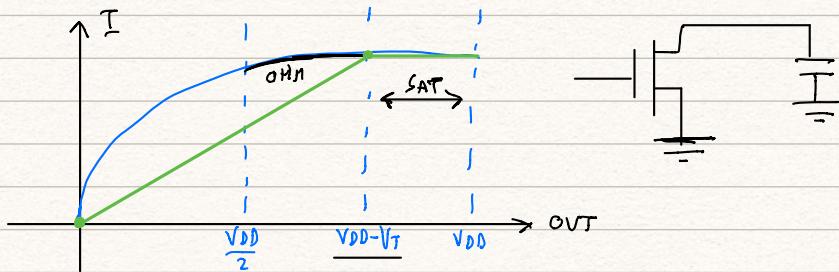
$$\ln\frac{1}{2} = \ln\left(\exp\left(-\frac{t_{PHL}}{\tau}\right)\right)$$

$$\ln\frac{1}{2} = -\frac{t_{PHL}}{\tau}$$

$$t_{PHL} = \tau \ln 2 \approx 0.69 \tau$$

"fotina del tempo" \rightarrow soluzioone del tempo

APPROSSIMAZIONE PER ECCESSO: (più precisa)



$$t_{PHL} = t_{PHL_{SAT}} + t_{PHL_{OHM}}$$

$$t_{PHL_{SAT}} = \frac{\alpha [V_{DD} - (V_{DD} - V_T)]}{I_{DSAT}} \approx \frac{C_L (V_{DD} - V_{DD} + V_T)}{I_{DSAT}} = \frac{C_L V_T}{K_n (V_{DD} - V_{Tn})^2}$$

$\Delta t_{PHL_{OHM}}$:

$$R_{eq} = \frac{[V_{DD} - V_T - \sigma]}{I_{DSAT}}$$

$$= \frac{V_{DD} - V_T}{K_n (V_{DD} - V_T)^2}$$

$$\tau \approx R_{eq}$$

$$OUT = (V_{DD} - V_T) \exp(-t/\tau)$$

$$\frac{V_{DD}}{2} = (V_{DD} - V_T) \exp(-t/\tau)$$

$$\frac{V_{DD}}{V_{DD} - V_T} = \exp(-t/\tau)$$

$$\ln \frac{V_{DD}/2}{V_{DD} - V_T} = (-t/\tau)$$

$$t_{PHL_{OHM}} = \tau \ln \frac{V_{DD} - V_T}{V_{DD}/2}$$

$$t_{PHL} = t_{PHL_{OHM}} + t_{PHL_{SATURATED}}$$

$$\tau_p \stackrel{\Delta}{=} \frac{t_{PHL} + t_{PLH}}{2}$$

RITARDO DI PROPAGAZIONE

inverter simmetrici $\rightarrow t_{PHL} = t_{PLH}$

DISSIPAZIONE DI POTENZA INVERTER CMOS:

POTENZA STATICA:

$$P_{\text{STATICA}} = 0 \quad (\text{teoricamente})$$

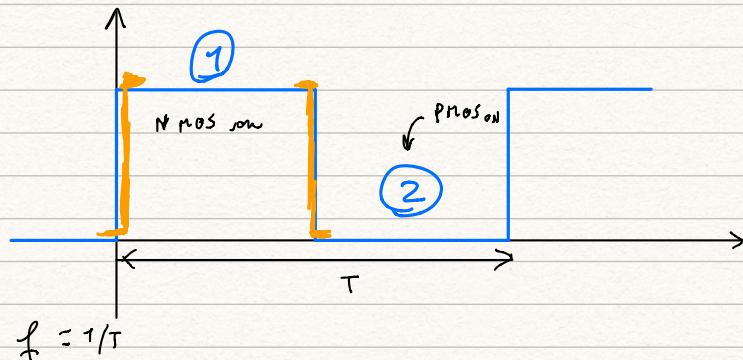
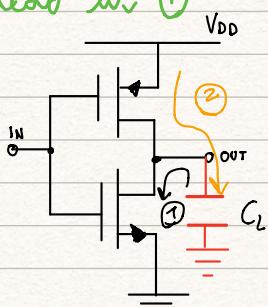
POTENZA DINAMICA:

① POTENZA SPESA PER LA CARICA E SCARICA DELLA CAPACITÀ (P_{CL})

② POTENZA DI CROSS-CONDUZIONE (P_{CC})

$$P_{CC} \ll P_{CL}$$

calcolo di ①



① C_L è carica a V_{DD}

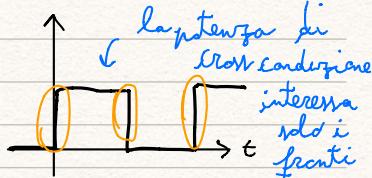
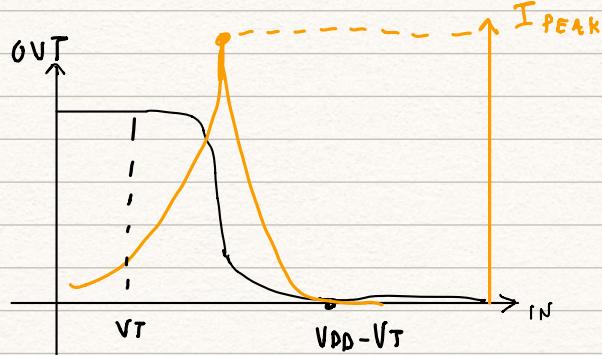
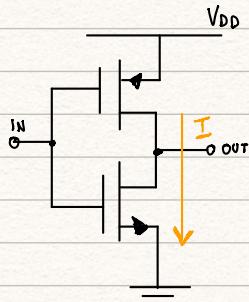
$$E = \frac{1}{2} C_L V_{DD}^2 \quad \text{durante la scarica} \quad E \text{ è dissipata dall'NMOS}$$

$$② E = \int i(t) v(t) dt = V_{DD} \int i(t) dt = V_{DD} C_L \cdot V_{DD} = C_L V_{DD}^2 \quad \begin{array}{l} \frac{1}{2} C_L V_{DD}^2 \text{ in } Q \\ \frac{1}{2} C_L V_{DD}^2 \text{ dissipata dal PMOS} \end{array}$$

$$P_{CL} = C_L V_{DD}^2 f \quad \begin{array}{l} \text{ridurre le tensioni di alimentazione} \\ \text{ridurre i periodi} \end{array}$$

ridurre le tensioni di alimentazione
ridurre i periodi

CALCOLO DI ②



$$I_{\text{PEAK}} = K_n (V_{GS} - V_{Tn})^2 = K_n \left(\frac{V_{DD}}{2} - V_{Tn} \right)^2 = |K_p| \left(-\frac{V_{DD}}{2} - V_{Tp} \right)^2$$

$$P_{CC} = I_{CC} V = (*)$$

$$I_{CC} = \frac{1}{2} I_{PEAK} (V_{DD} - V_{Tn} - |V_{Tp}|)$$

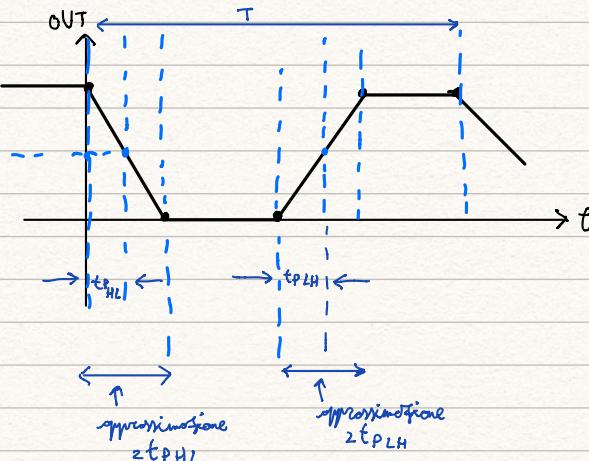
corrente di crono-conduzione media

$$(*) = \left(\frac{1}{2} I_{PEAK} \frac{V_{DD} - 2V_T}{V_{DD}} \right) \cdot V_{DD}$$

I_{CC}

$$\frac{2t_{PHL} + 2t_{PLH}}{T}$$

$$P_{CC} = \frac{1}{2} I_{peak} (V_{DD} - 2V_T) \cdot 2(2V_T) \neq$$



$$P_{CC} < P_{CL}$$

$$P_{TOT} = P_{STATICA} + P_{CC} + P_{CL} = 0$$

PORTE LOGICHE:

NOT



$$Y = \bar{A}$$

A	Y
1	0
0	1

OR



$$Y = A + B$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

AND



$$Y = A \cdot B$$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

porta normalmente bassa

NOR



$$Y = \bar{A} + \bar{B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

NAND



$$Y = \bar{A} \cdot \bar{B}$$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

porta normalmente alta

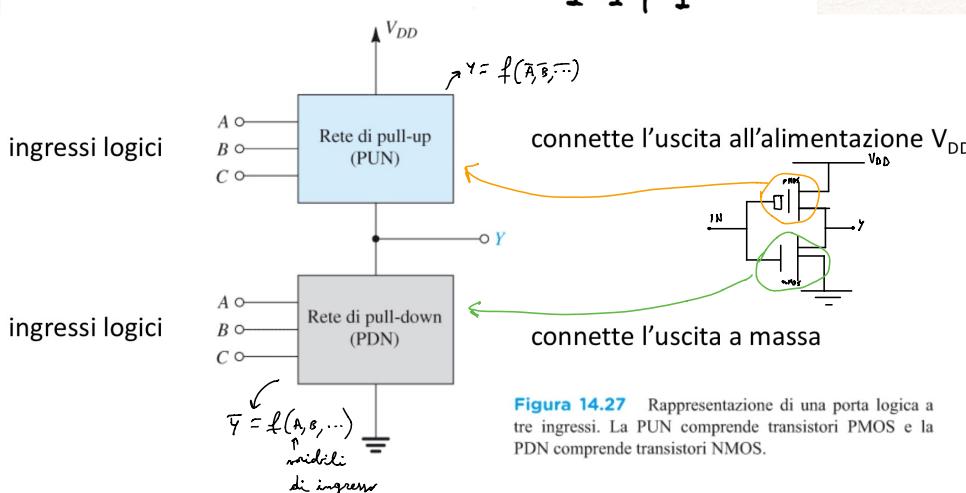


Figura 14.27 Rappresentazione di una porta logica a tre ingressi. La PUN comprende transistori PMOS e la PDN comprende transistori NMOS.

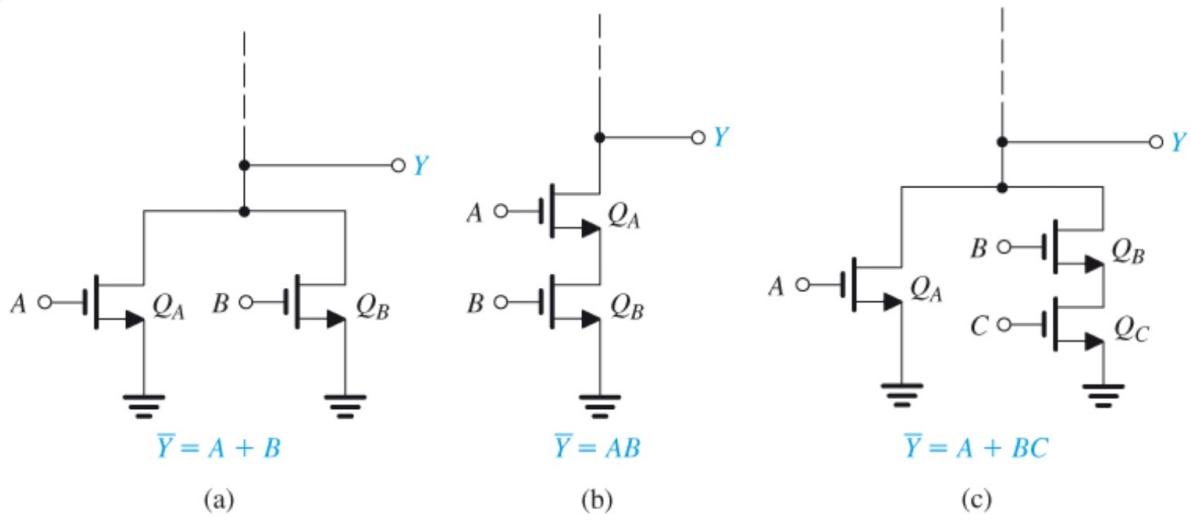
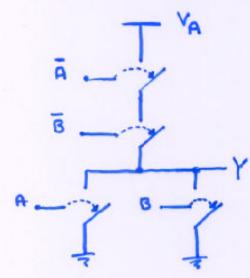


Figura 14.28 Esempi di reti di pull-down.

PORTE LOGICHE NOR CMOS



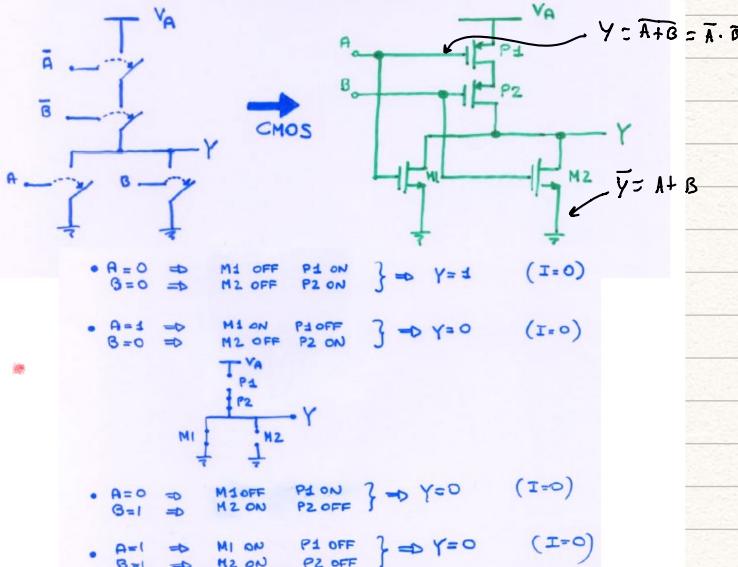
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



COME IMPLEMENTARE QUESTA
TABELLA DELLE VERITÀ?

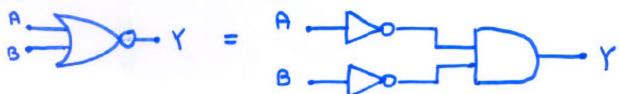
- C. Guazzoni - Fondamenti di Elettronica

PORTE LOGICHE NOR CMOS

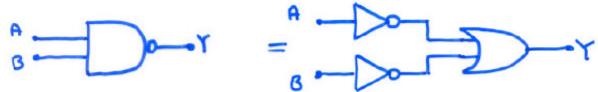


TEOREMA DI DE MORGAN

$$\bullet \overline{A+B} = \overline{A} \cdot \overline{B}$$

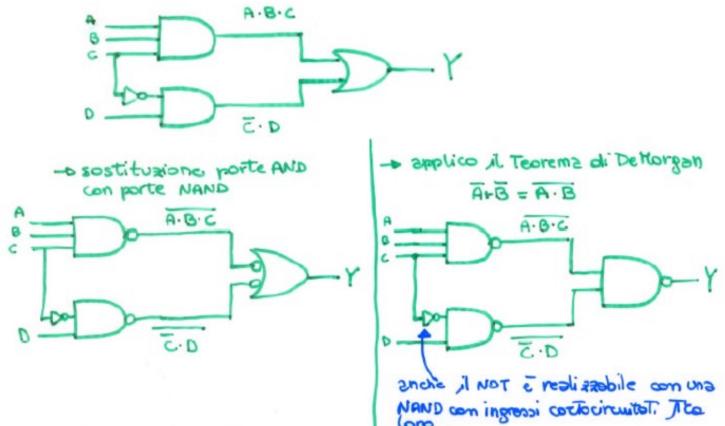


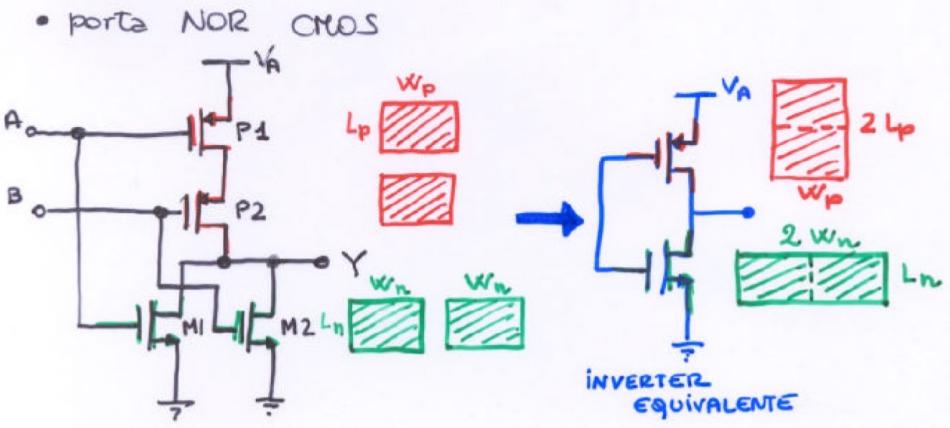
$$\bullet \overline{A \cdot B} = \overline{A} + \overline{B}$$



ESEMPIO DI APPLICAZIONE DEL TEOREMA DI DE MORGAN

$$Y = A \cdot B \cdot C + \overline{C} \cdot D$$

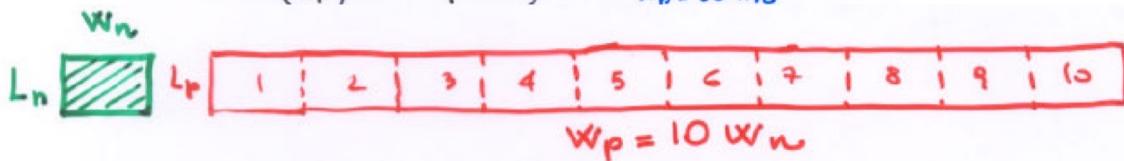




d'inverter sarà simmetrico (uguaglianza dei noise margin, uguaglianza di t_{PLH} e t_{PHL} , ...) se $|k_n| = |k_p|$ → il più piccolo corrisponde una commutazione più lenta

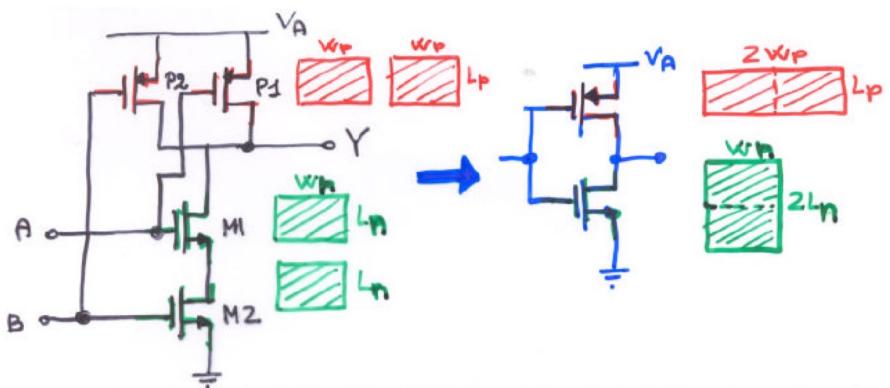
$$\hookrightarrow \left(\frac{W_p}{2L_p} \right) = 2.5 \left(\frac{2W_n}{L_n} \right) \quad \text{La rete di PULL-UP occupa più della rete di PULL-DOWN}$$

$$\left(\frac{W_p}{L_p} \right) = 10 \left(\frac{W_n}{L_n} \right) \rightarrow \text{a parità di } L \\ W_p = 10 W_n$$



Le tecnologie vengono nominate in base alla lunghezza minima del canale raggiungibile (ad esempio 22 nm → canale lungo 22 nm)

PORTA LOGICA NAND CMOS



- $|k_m| = |k_p| \rightarrow \left(\frac{2W_p}{L_p} \right) = 2.5 \left(\frac{W_n}{2L_n} \right)$

$$\hookrightarrow \left(\frac{W_p}{L_p} \right) = \frac{2.5}{4} \left(\frac{W_n}{L_n} \right) = 0.625 \left(\frac{W_n}{L_n} \right)$$

PERCHE' E' PIU' CONVENIENTE UNA LOGICA NAND CMOS DI UNA LOGICA NOR CMOS?

Assuming a symmetric equivalent inverter:

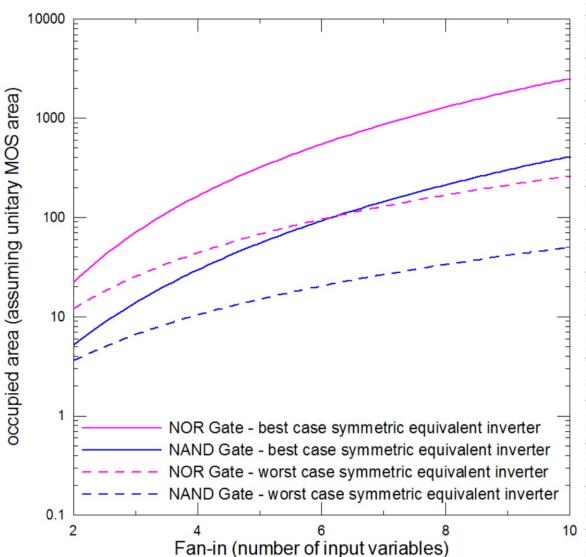
- worst case: longest propagation time
- best case: shortest propagation time

$$AREA_{NOR,BEST\ CASE} = AREA_{MIN} N \left(1 + 2.5N^2 \right)$$

$$AREA_{NOR,WORST\ CASE} = AREA_{MIN} N \left(1 + 2.5N \right)$$

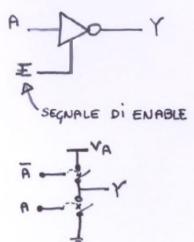
$$AREA_{NAND,BEST\ CASE} = AREA_{MIN} N \left(1 + \frac{N^2}{2.5} \right)$$

$$AREA_{NAND,WORST\ CASE} = AREA_{MIN} N \left(1 + \frac{N}{2.5} \right)$$



PORTE LOGICHE TRI-STATE

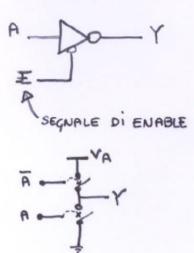
□ SEGNALE DI ENABLE ATTIVO ALTO



E	A	Y
1	0	1
1	1	0
0	0	High Z
0	1	High Z

è come se entrambi gli interruttori dell'inverter fossero aperti

□ SEGNALE DI ENABLE ATTIVO BASSO

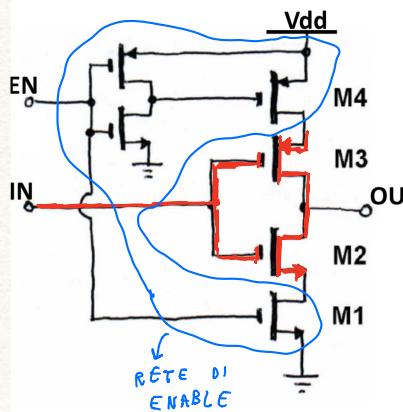


E	A	Y
0	0	1
0	1	0
1	0	High Z
1	1	High Z

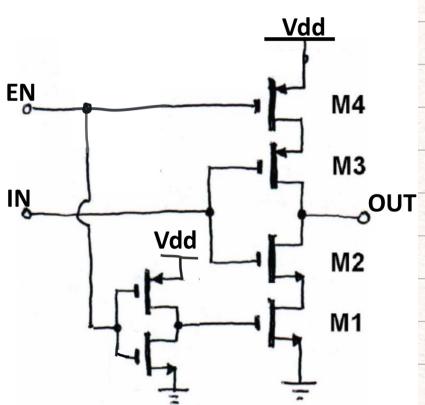
è come se entrambi gli interruttori dell'inverter fossero aperti

PORTE LOGICHE TRI-STATE

□ SEGNALE DI ENABLE ATTIVO ALTO

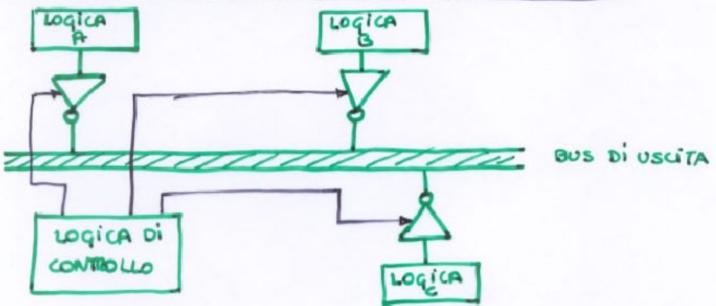


□ SEGNALE DI ENABLE ATTIVO BASSO

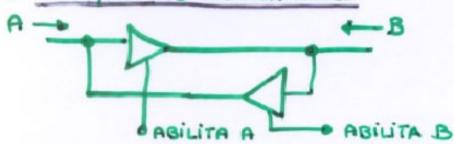


PORTE LOGICHE TRI-STATE

* CONNESSIONI MULTIPLE AD UN SINGOLO BUS DI USCITA



* COLLEGAMENTO BIDIRZIONALE



* TERMINALE INGRESSO/ USCITA



ESEMPI DI USO DELLE PORTE TRI-STATE