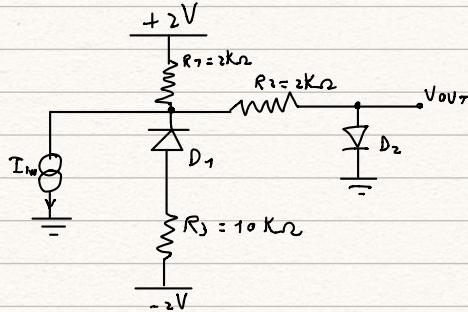
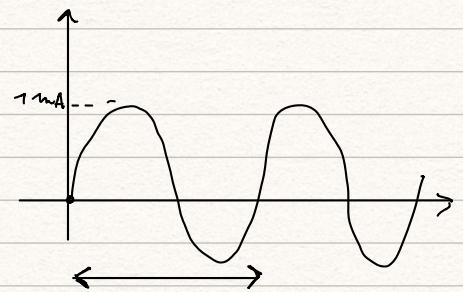


esercizio 4 prova in itinere 2018



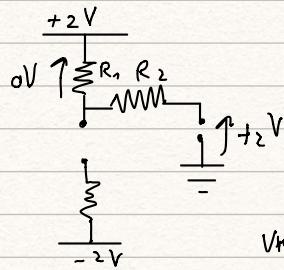
$$\begin{aligned} I_{in} \text{ minima:} \\ \left\{ \begin{array}{l} A = 1 \text{ mA} \\ f = 500 \text{ Hz} \end{array} \right. \end{aligned}$$



A) Disegnare V_{out}

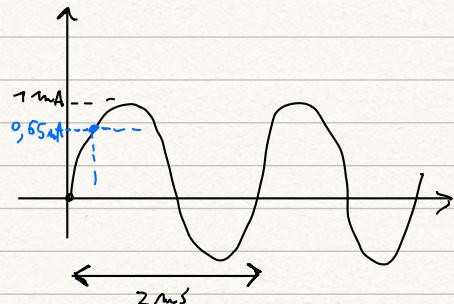
per $I_{in} = 0$ D_1 sicuramente spento

Se D_2 fosse spento

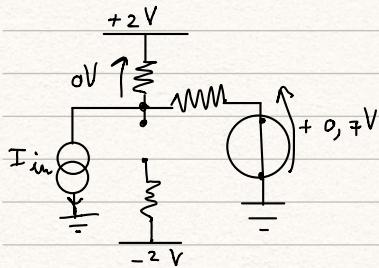


D_2 NON è spento
 D_2 è acceso

$$V_{KD1} = (2V - 0,7V) \frac{R_1}{R_1 + R_2} = 2V - \frac{1,3V}{2} = 0,35V$$



quindi ha:



D_2 è acceso finché

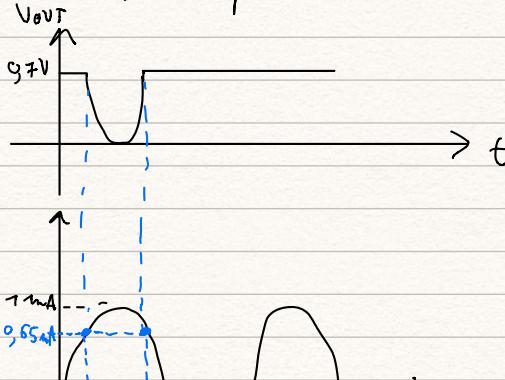
$$2V - I_{in} R_1 > 0,7V$$

$$I_{in} < 0,65 \text{ mA}$$

$$\text{con } I_{in} = 0,65 \text{ mA}$$

$$V_{K7} = 0,7V$$

con D_1, D_2 spenti

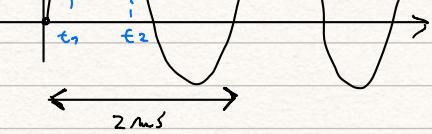


$$\text{Per } I_{in} = 1 \text{ mA}$$

$$V_{out} = 2V - 1 \text{ mA} R_1 = 0,8V$$

Per $I_{in} < 0$ D_2 è sempre acceso

$$V_{out} = 0,7V$$

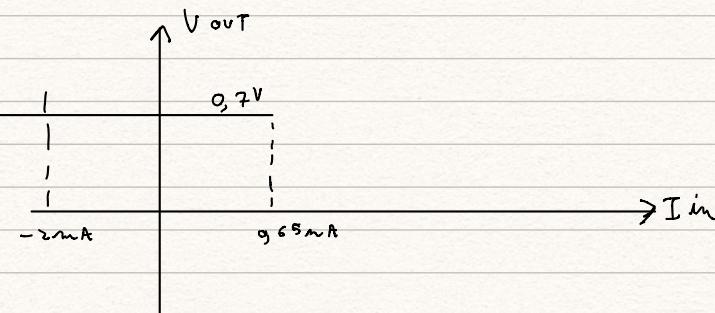


B) Tracciare la caratteristica di trasferimento del circuito $V_{OUT} - I_{in}$

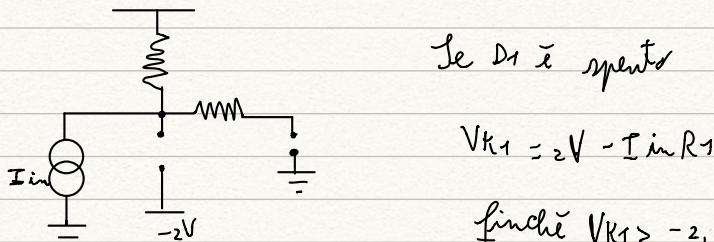
$$D_1, D_2 \quad V_{BD} = -4,7V$$

$$I_{in} \in [-2mA, +2mA]$$

per $I_{in} < 0,65mA$ D_2 è acceso in diretta



per $I_{in} > 0,65mA$ D_2 è spento



Se D_1 è spento

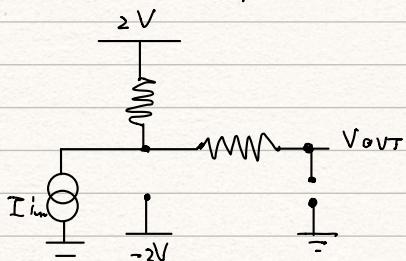
$$V_{R1} = 2V - I_{in}R_1$$

finché $V_{R1} > -2,7V$ D_1 è spento

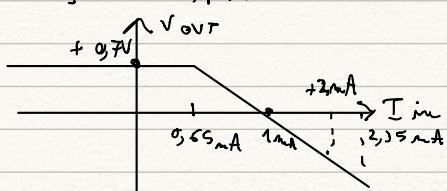
$$I_{in} < 3,35mA \quad (\text{Ho verificato})$$

Per $0,65mA < I_{in} < 2mA$

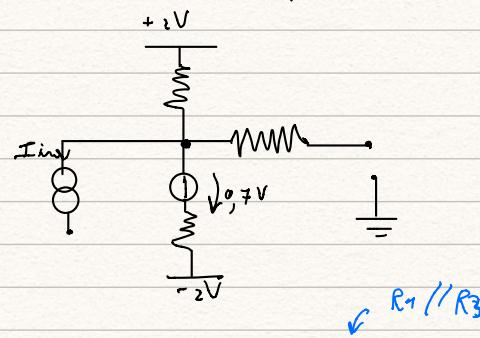
D_1 e D_2 spenti



$$V_{OUT} = 2V - I_{in}R_1$$



con D_1 acceso, D_2 spento

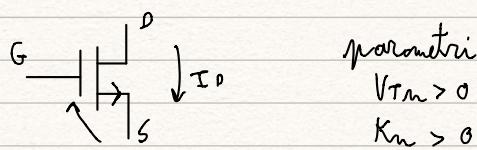


$$V_{OUT} = 1,2V - I_{in} \approx 1,67mA$$

$$V_{OUT_{MIN}} = -4,7V$$

Esercizi sui Transistor:

N MOS:



parametri
 $V_{TN} > 0$
 $K_n > 0$

N MOS è acceso se

$$V_{GS} > V_{TN} \quad I_D \text{ è positiva}$$

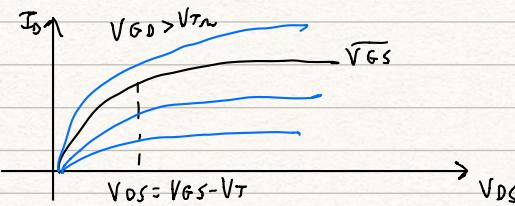
in saturazione se

$$V_{DS} > V_{GS} - V_T$$

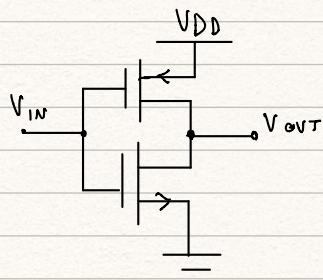
in ohmico se

$$V_{DS} < V_{GS} - V_T$$

$$V_D - V_S < V_G - V_T$$



INVERTER CMOS:



Dati:
 $V_{DD} = 5V$
 $V_{TN} = 0.8V$ $V_{TP} = -0.8V$

$$\frac{1}{2} \mu_n C_{ox} = 75 \mu A/V^2$$

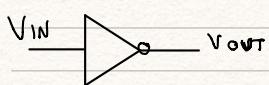
$$\frac{1}{2} \mu_p C_{ox} = -30 \mu A/V^2$$

$$\left. \frac{W}{L} \right|_n = \frac{2 \mu m}{1 \mu m} \quad \left. \frac{W}{L} \right|_p = \frac{5 \mu m}{1 \mu m}$$

$$k_n = |K_p| = 150 \mu A/V^2$$

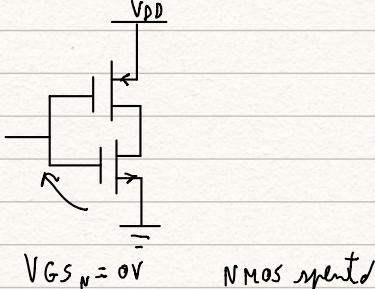
simbolo

TABELLA DELLA VERITÀ:

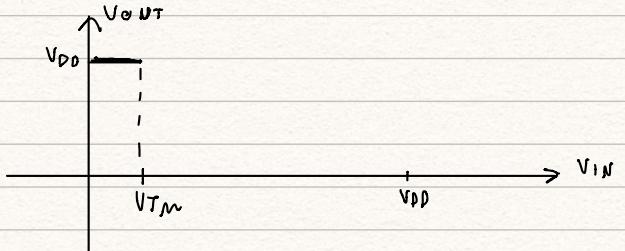


V_{IN}	V_{OUT}
0	1
1	0

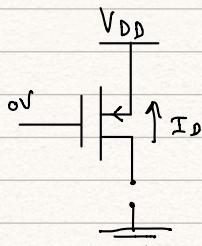
$$V_{IN} = 0 \text{ V}$$



$$V_{GS} = -5\text{V} < V_{GSp} \text{ per MOS ACCESSO}$$

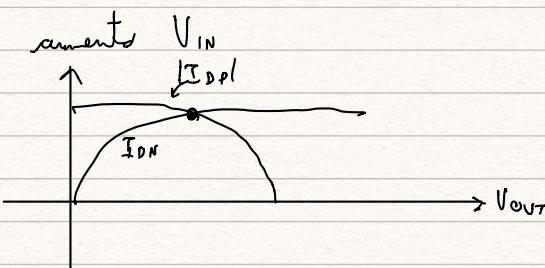
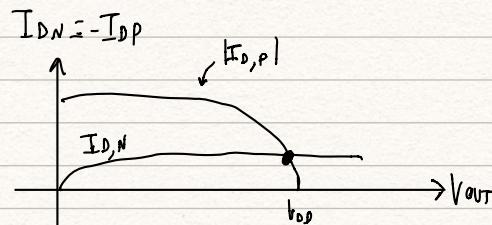
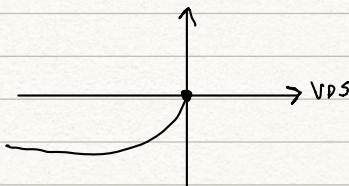


Con V_{IN} leggermente $> V_{TN}$ "overdrive"
NMOS è acceso con V_{ov} piccolo
($V_{ov} = V_{GS} - V_{TN}$)



PMOS è acceso con $|V_{ov}|$ grande
($|V_{ov}| = |V_{GS} - V_{TP}|$)

$$I_D \leq 0 \rightarrow V_{DS} = 0\text{V} \rightarrow V_D = V_S = V_{DD}$$



Esiste un punto della caratteristica statica tale per cui sia PMOS che NMOS siano in saturazione?

(HP) NMOS e PMOS in saturazione

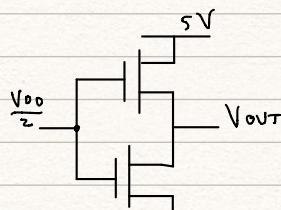
$$|K_p| (V_{GSp} - V_{Tp})^2 = K_n (V_{GS_N} - V_{TN})^2$$

$$V_{GSp} = V_{IN} - V_{DD} ; V_{GS_N} = V_{IN}$$

$$|K_p| (V_{IN} - V_{DD} - V_{Tp})^2 = K_n (V_{IN} - V_{TN})^2$$

$$V_{IN} = \frac{V_{DD}}{2}$$

V_{IN} può assumere qualsiasi valore purché entrambi i MOS siano in saturazione



NMOS è in saturazione

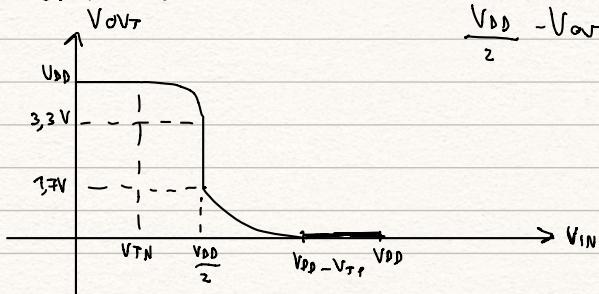
$$V_{GD} < V_{TN}$$

$$\frac{V_{IN}}{2} - V_{OUT} < V_{TN}$$

pmos è in saturazione

$$V_{GD} > V_{TP}$$

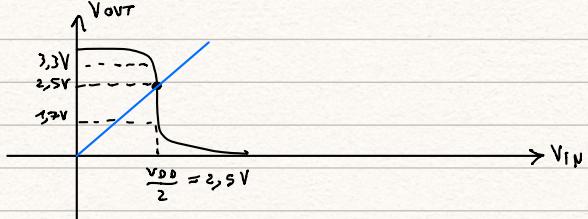
CARATTERISTICA STATICÀ



$$\frac{V_{DD}}{2} - V_{OUT} > V_{TP} \rightarrow V_{OUT} < \frac{V_{DD}}{2} - V_{TP}$$

SOGLI A LOGICA :

Tensione V_{IN} tale che $V_{IN} = V_{OUT}$



$$V_{TH} = \frac{V_{DD}}{2} = 2.5V$$

Calcolare V_{TH} con NMOS e PMOS con $w=1\mu m$:

$$K_n = 75 \mu A/V^2$$

$$K_p = -30 \mu A/V^2$$

Hp: entrambi i mos sono accesi

per definizione $V_{IN} = V_{OUT} \rightarrow V_{GD} = 0V \rightarrow$ entrambi i mos in saturazione

$$I_{Dn} = -I_{Dp}$$

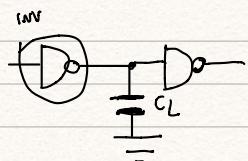
$$K_n (V_{GSN} - V_{TN})^2 = |K_p| (V_{GSP} - V_{TP})^2$$

$$K_n (V_{Th} - V_{TN})^2 = |K_p| (V_{Th} - V_{DD} - V_{TP})^2$$

$$\text{SOLUZIONE } V_{Th} = 2.11V$$

$$K_m = -K_p$$

COMPORTAMENTO DINAMICO:



consideriamo $C_L = 0,5 \text{ pF}$

Tempi di propagazione \rightarrow per raggiungere la soglia logica della porta successiva

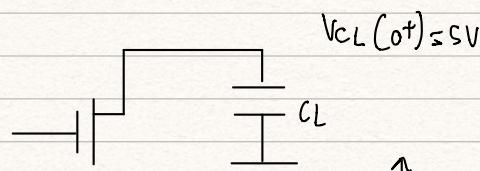
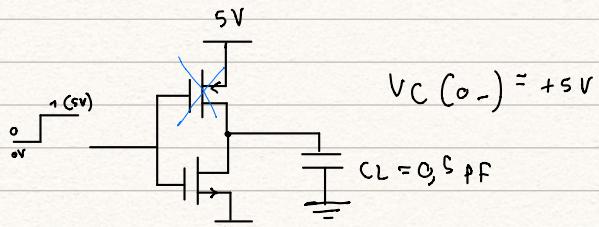
$$t_{PHL}$$

$$t_{PLH}$$

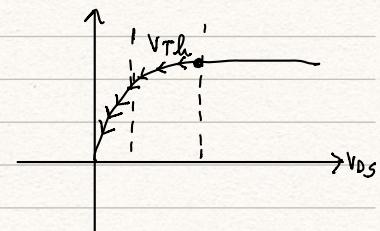
ritardo di propagazione

$$T_p = \frac{t_{PHL} + t_{PLH}}{2}$$

t_{PHL} dell'uscita ($0 \rightarrow 1$) \rightarrow quando ingresso $0 \rightarrow 1$ istantaneamente



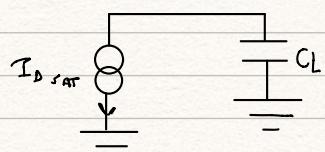
$$V_{DS}(0^+) = 5V$$



APPROSSIMAZIONI PER CALCOLARE I TEMPI:

1) approssimazione natura

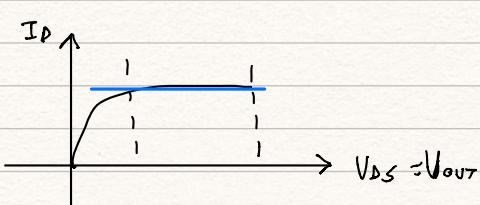
$$I_D = I_{DSAT}$$



$$\Delta V = V_{DD} - \frac{V_{DD}}{2} = 2,5V$$

$$t_{PHL} = \frac{C_L}{I_{DSAT}} \Delta V = \frac{0,5 \text{ pF}}{3,65 \text{ mA}} \cdot 2,5V = 472 \text{ ps}$$

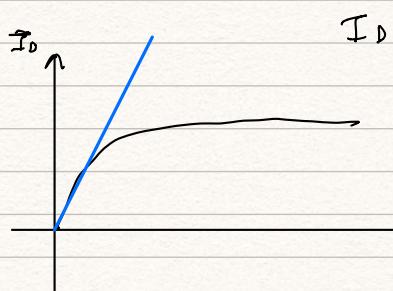
$$I_{DSAT} = K_N (V_{GS} - V_{TN})^2 = 150 \mu A/V^2 (5V - 0,8V)^2 = 3,65 \text{ mA}$$



ottima del tempo
di propagazione

2) approssimazione ohmica

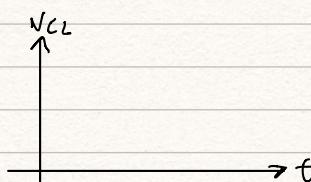
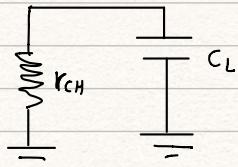
$$r_{CH} = R_{DS\text{ ON}} \Big|_{V_{DS} = 0}$$



$$I_D = k_m \left[2(V_{GS} - V_T) V_{DS} - V_{DS}^2 \right]$$

$$\frac{\partial I_D}{\partial V_{DS}} = k_m \left[2(V_{GS} - V_{Tm}) - 2V_{DS} \right]$$

$$r_{CH} = \frac{1}{2k_m(V_{GS} - V_{Tm})} = 274 \Omega$$



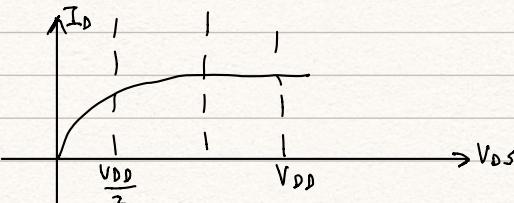
$$\tau = R_{TH} \cdot C_L$$

$$V_{CL} = 5V \cdot e^{-\frac{t}{\tau}}$$

raggiunge $\frac{V_{DD}}{2}$

$$t_{PHL} = 0,69 \quad R_{TH} C_L = 274 \text{ ps}$$

3) approssimazione per eccesso



$$t_{PHL} = t_{PHL\text{ SAT}} + t_{PHL\text{ OHMICA}}$$

$$t_{PHL\text{ SAT}}$$

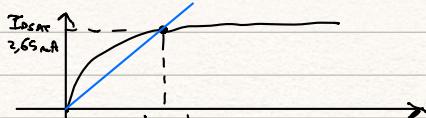
$$\Delta V = V_{DD} - (V_{GS} - V_T) = 5V - 4,2V = 0,8V$$

$$I_{DSAT} = 2,65 \text{ mA}$$

$$C_L = 0,5 \text{ pF}$$

$$t_{PHL\text{ SAT}} = \frac{C_L}{I_{DSAT}} \cdot \Delta V = \frac{0,5 \text{ pF}}{2,65 \text{ mA}} \cdot 0,8V = 151 \text{ ps}$$

in zona ohmica consideriamo R_{eq}



$$t_{PHL}^{\text{OHMICA}} = 410 \text{ ps}$$

$$t_{PHL} = 151 \text{ ps} + 410 \text{ ps} = 561 \text{ ps} \rightarrow \text{sostituiamo la corrente}$$