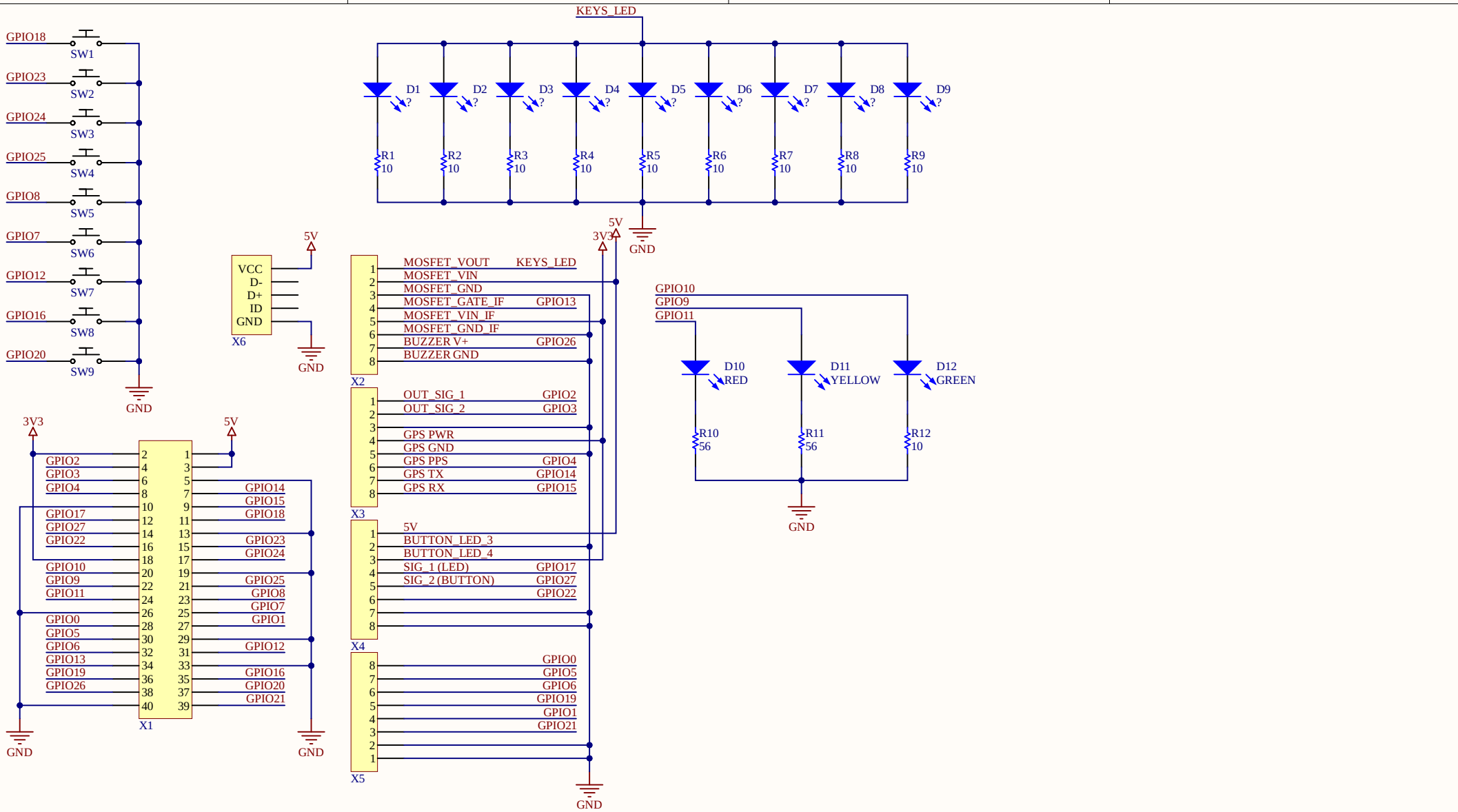
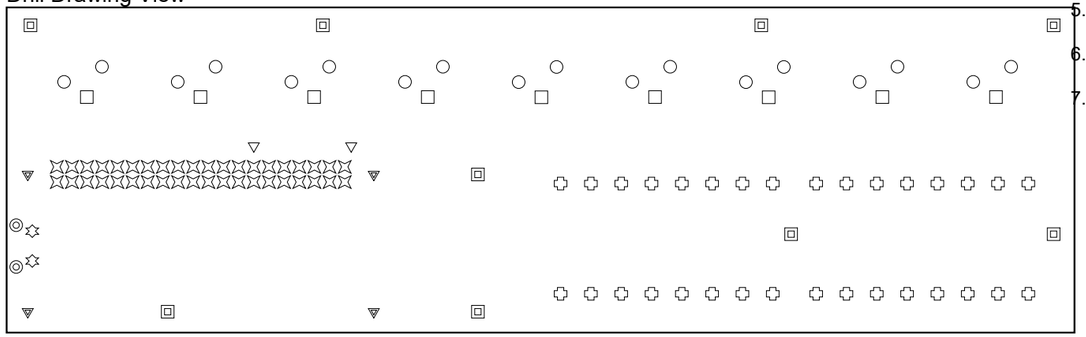


Title		
Size A4	Number	Revision
Date: 9-06-2022		Sheet of
File: C:\Users\..\KSS.SchDoc		Drawn By:

Note:

1. Text element with square border.
2. Text element with no border
3. Text element with circle border
4. Text element with no border
5. Text element with no border
6. Text element with no border
7. Text element with no border

Drill Drawing View



Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
◎	2	0.60	Plated	+/-0.05
✡	2	0.55	Plated	+/-0.05
✣	32	1.40	Plated	
○	18	1.50	Plated	
□	9	4.10	Plated	
⛝	40	1.00	Plated	
▽	4	4.50	Plated	
⧈	9	2.75	Plated	
▽	2	0.71	Plated	

NEXT ASSY	USED ON	
APPLICATION		

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
FRACTIONAL±
ANGULAR: MACH± BEND ±
TWO PLACE DECIMAL ±
THREE PLACE DECIMAL ±
INTERPRET GEOMETRIC TOLERANCING PER:
MATERIAL
FINISH
DO NOT SCALE DRAWING

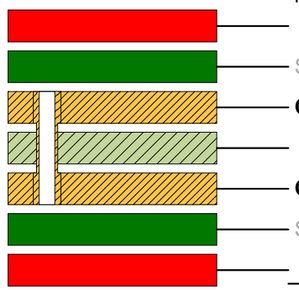
	NAME	DATE
DRAWN		2022-09-06
CHECKED		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

TITLE

SIZE	DWG. NO.	
SCALE: 1:1	WEIGHT:	SHEET 1 OF 3

Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.01mm	Solder Resist	Solder Mask	GTS
Copper	**Top Layer**	**0.04mm**		**Signal**	**GTL**
		0.32mm	*FR-4*	*Dielectric*	
Copper	**Bottom Layer**	**0.04mm**		**Signal**	**GBL**
Surface Material	Bottom Solder	0.01mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 0.41mm

		UNLESS OTHERWISE SPECIFIED:	
		DIMENSIONS ARE IN INCHES TOLERANCES: FRACTIONAL± ANGULAR: MACH± BEND ± TWO PLACE DECIMAL ± THREE PLACE DECIMAL ±	
		INTERPRET GEOMETRIC TOLERANCING PER:	
		MATERIAL	
NEXT ASSY	USED ON	FINISH	
APPLICATION		DO NOT SCALE DRAWING	

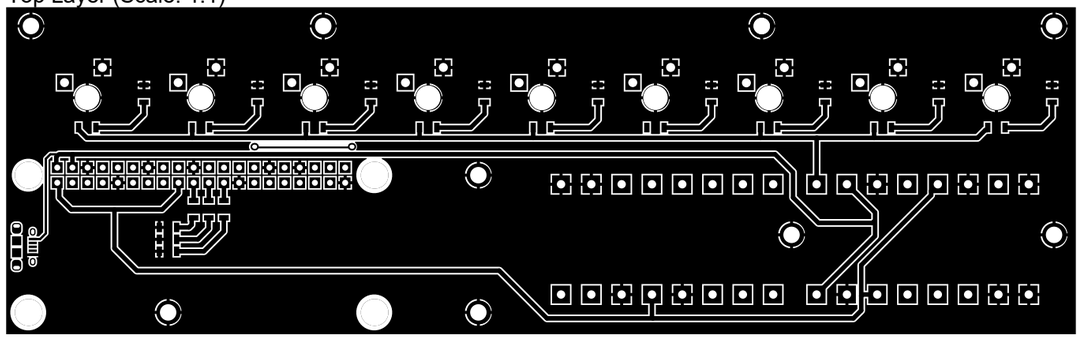
	NAME	DATE
DRAWN		2022-09-06
CHECKED		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

TITLE

SIZE	DWG. NO.	
SCALE: 1:1	WEIGHT:	SHEET 2 OF 3

Top Layer (Scale: 1:1)



NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED:
DIMENSIONS ARE IN INCHES
TOLERANCES:
FRACTIONAL±
ANGULAR: MACH± BEND ±
TWO PLACE DECIMAL ±
THREE PLACE DECIMAL ±
INTERPRET GEOMETRIC TOLERANCING PER:
MATERIAL
FINISH
DO NOT SCALE DRAWING

	NAME	DATE
DRAWN		2022-09-06
CHECKED		
ENG APPR.		
MFG APPR.		
Q.A.		

COMMENTS:

TITLE

SIZE	DWG. NO.	
SCALE: 1:1	WEIGHT:	SHEET 3 OF 3

Design Rules Verification Report

Filename : C:\Users\bhbo9\Documents\PROJECTS\BartoszOStrowski\PCB\STM32H7

Warnings 0
Rule Violations 201

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	1
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.762mm) (Preferred=0.254mm) (All)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	23
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	1
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	12
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	164
Silk to Silk (Clearance=0.254mm) (All),(All)	0
Net Antennae (Tolerance=0mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	201

Un-Routed Net Constraint ((All))
Un-Routed Net Constraint: Net KEYS_LED Between Pad D5-1(61.19mm,30.98mm) on Top Layer And Pad D6-1(80.24mm,30.98mm) on Top Layer

Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)
Hole Size Constraint: (2.75mm > 2.54mm) Pad Free-MH(0mm,0mm) on Multi-Layer Actual Hole Size = 2.75mm
Hole Size Constraint: (2.75mm > 2.54mm) Pad Free-MH(104.5mm,13mm) on Multi-Layer Actual Hole Size = 2.75mm
Hole Size Constraint: (2.75mm > 2.54mm) Pad Free-MH(148.5mm,13mm) on Multi-Layer Actual Hole Size = 2.75mm
Hole Size Constraint: (2.75mm > 2.54mm) Pad Free-MH(148.5mm,48mm) on Multi-Layer Actual Hole Size = 2.75mm
Hole Size Constraint: (4.5mm > 2.54mm) Pad Free-MH(-23.454mm,0mm) on Multi-Layer Actual Hole Size = 4.5mm
Hole Size Constraint: (4.5mm > 2.54mm) Pad Free-MH(-23.454mm,23mm) on Multi-Layer Actual Hole Size = 4.5mm
Hole Size Constraint: (2.75mm > 2.54mm) Pad Free-MH(-23mm,48mm) on Multi-Layer Actual Hole Size = 2.75mm
Hole Size Constraint: (2.75mm > 2.54mm) Pad Free-MH(26mm,48mm) on Multi-Layer Actual Hole Size = 2.75mm
Hole Size Constraint: (4.5mm > 2.54mm) Pad Free-MH(34.546mm,0mm) on Multi-Layer Actual Hole Size = 4.5mm
Hole Size Constraint: (4.5mm > 2.54mm) Pad Free-MH(34.546mm,23mm) on Multi-Layer Actual Hole Size = 4.5mm
Hole Size Constraint: (2.75mm > 2.54mm) Pad Free-MH(52mm,0mm) on Multi-Layer Actual Hole Size = 2.75mm
Hole Size Constraint: (2.75mm > 2.54mm) Pad Free-MH(52mm,23mm) on Multi-Layer Actual Hole Size = 2.75mm
Hole Size Constraint: (2.75mm > 2.54mm) Pad Free-MH(99.5mm,48mm) on Multi-Layer Actual Hole Size = 2.75mm
Hole Size Constraint: (2.75mm > 2.54mm) Pad Free-MH(99.5mm,48mm) on Multi-Layer Actual Hole Size = 2.75mm
Hole Size Constraint: (4.1mm > 2.54mm) Pad SW1-MH(-13.56mm,35.98mm) on Multi-Layer Actual Hole Size = 4.1mm
Hole Size Constraint: (4.1mm > 2.54mm) Pad SW2-MH(5.49mm,35.98mm) on Multi-Layer Actual Hole Size = 4.1mm
Hole Size Constraint: (4.1mm > 2.54mm) Pad SW3-MH(24.54mm,35.98mm) on Multi-Layer Actual Hole Size = 4.1mm
Hole Size Constraint: (4.1mm > 2.54mm) Pad SW4-MH(43.59mm,35.98mm) on Multi-Layer Actual Hole Size = 4.1mm
Hole Size Constraint: (4.1mm > 2.54mm) Pad SW5-MH(62.64mm,35.94mm) on Multi-Layer Actual Hole Size = 4.1mm
Hole Size Constraint: (4.1mm > 2.54mm) Pad SW6-MH(81.69mm,35.98mm) on Multi-Layer Actual Hole Size = 4.1mm
Hole Size Constraint: (4.1mm > 2.54mm) Pad SW7-MH(100.74mm,35.94mm) on Multi-Layer Actual Hole Size = 4.1mm
Hole Size Constraint: (4.1mm > 2.54mm) Pad SW8-MH(119.79mm,35.98mm) on Multi-Layer Actual Hole Size = 4.1mm
Hole Size Constraint: (4.1mm > 2.54mm) Pad SW9-MH(138.84mm,35.98mm) on Multi-Layer Actual Hole Size = 4.1mm

Hole To Hole Clearance (Gap=0.254mm) (All),(All)
Hole To Hole Clearance Constraint: (Collision < 0.254mm) Between Pad Free-MH(99.5mm,48mm) on Multi-Layer And Pad Free-MH(99.5mm,48mm)

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad R10-1(-1.48mm,10.25mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad R10-2(1.42mm,10.25mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad R11-1(-1.48mm,12.25mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.197mm < 0.254mm) Between Pad R11-2(1.42mm,12.25mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad X6-1(-22.7mm,12.3mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.172mm < 0.254mm) Between Pad X6-1(-22.7mm,12.3mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad X6-2(-22.7mm,11.65mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad X6-3(-22.7mm,11mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm) Between Pad X6-4(-22.7mm,10.35mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.172mm < 0.254mm) Between Pad X6-5(-22.7mm,9.7mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad X6-MH(-25.4mm,14.5mm) on Multi-Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.247mm < 0.254mm) Between Pad X6-MH(-25.4mm,7.5mm) on Multi-Layer And Pad

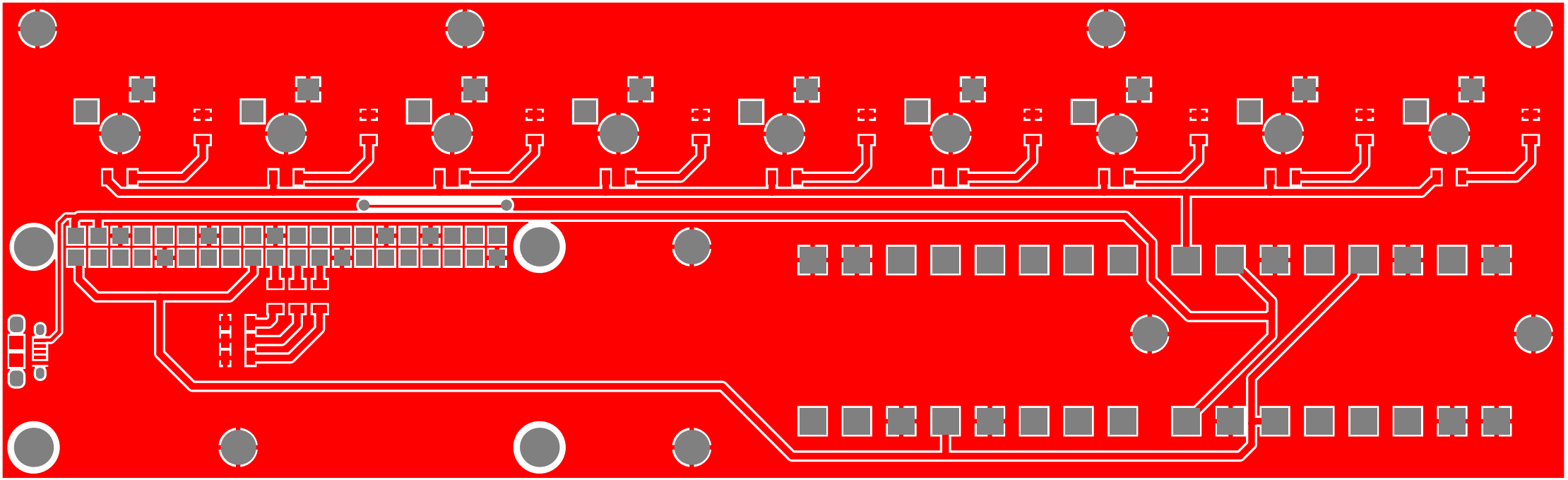
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D10-1(9.356mm,18.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D10-1(9.356mm,18.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D10-1(9.356mm,18.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D10-2(9.356mm,15.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D10-2(9.356mm,15.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D10-2(9.356mm,15.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D1-1(-15.01mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D1-1(-15.01mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D1-1(-15.01mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D11-1(6.816mm,18.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D11-1(6.816mm,18.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D11-1(6.816mm,18.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D11-2(6.816mm,15.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D11-2(6.816mm,15.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D11-2(6.816mm,15.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D1-2(-12.11mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D1-2(-12.11mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D1-2(-12.11mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D12-1(4.276mm,18.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D12-1(4.276mm,18.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D12-1(4.276mm,18.75mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D12-2(4.276mm,15.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D12-2(4.276mm,15.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D12-2(4.276mm,15.85mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D2-1(4.04mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D2-1(4.04mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D2-1(4.04mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D2-2(6.94mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D2-2(6.94mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D2-2(6.94mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D3-1(23.09mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D3-1(23.09mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D3-1(23.09mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D3-2(25.99mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D3-2(25.99mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D3-2(25.99mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D4-1(42.14mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D4-1(42.14mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D4-1(42.14mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D4-2(45.04mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D4-2(45.04mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D4-2(45.04mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D5-1(61.19mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D5-1(61.19mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D5-1(61.19mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D5-2(64.09mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D5-2(64.09mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D5-2(64.09mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D6-1(80.24mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D6-1(80.24mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D6-1(80.24mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D6-2(83.14mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D6-2(83.14mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D6-2(83.14mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D7-1(99.29mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D7-1(99.29mm,30.98mm) on Top Layer And Track

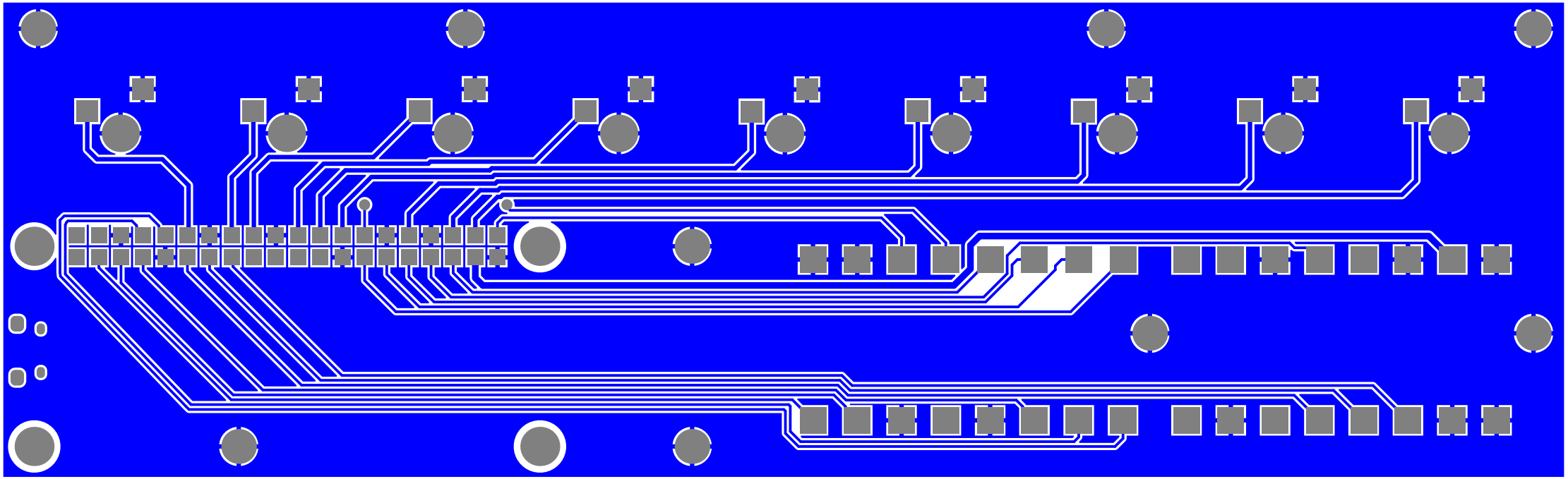
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D7-1(99.29mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D7-2(102.19mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D7-2(102.19mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D7-2(102.19mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D8-1(118.34mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D8-1(118.34mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D8-1(118.34mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D8-2(121.24mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D8-2(121.24mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D8-2(121.24mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D9-1(137.39mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D9-1(137.39mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D9-1(137.39mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D9-2(140.29mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D9-2(140.29mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad D9-2(140.29mm,30.98mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R10-1(-1.48mm,10.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R10-1(-1.48mm,10.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.254mm) Between Pad R10-1(-1.48mm,10.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R10-1(-1.48mm,10.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R10-1(-1.48mm,10.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.254mm) Between Pad R10-2(1.42mm,10.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R10-2(1.42mm,10.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R10-2(1.42mm,10.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R10-2(1.42mm,10.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R10-2(1.42mm,10.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R1-1(-4.06mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R1-1(-4.06mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R1-1(-4.06mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R11-1(-1.48mm,12.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R11-1(-1.48mm,12.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R11-1(-1.48mm,12.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R11-1(-1.48mm,12.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R11-1(-1.48mm,12.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.254mm) Between Pad R11-1(-1.48mm,12.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.254mm) Between Pad R11-1(-1.48mm,12.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R11-2(1.42mm,12.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.254mm) Between Pad R11-2(1.42mm,12.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.254mm) Between Pad R11-2(1.42mm,12.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R11-2(1.42mm,12.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R11-2(1.42mm,12.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R11-2(1.42mm,12.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R11-2(1.42mm,12.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R1-2(-4.06mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R1-2(-4.06mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R1-2(-4.06mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.254mm) Between Pad R12-1(-1.48mm,14.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R12-1(-1.48mm,14.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R12-1(-1.48mm,14.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R12-1(-1.48mm,14.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R12-1(-1.48mm,14.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.156mm < 0.254mm) Between Pad R12-2(1.42mm,14.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R12-2(1.42mm,14.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R12-2(1.42mm,14.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R12-2(1.42mm,14.25mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R12-2(1.42mm,14.25mm) on Top Layer And Track

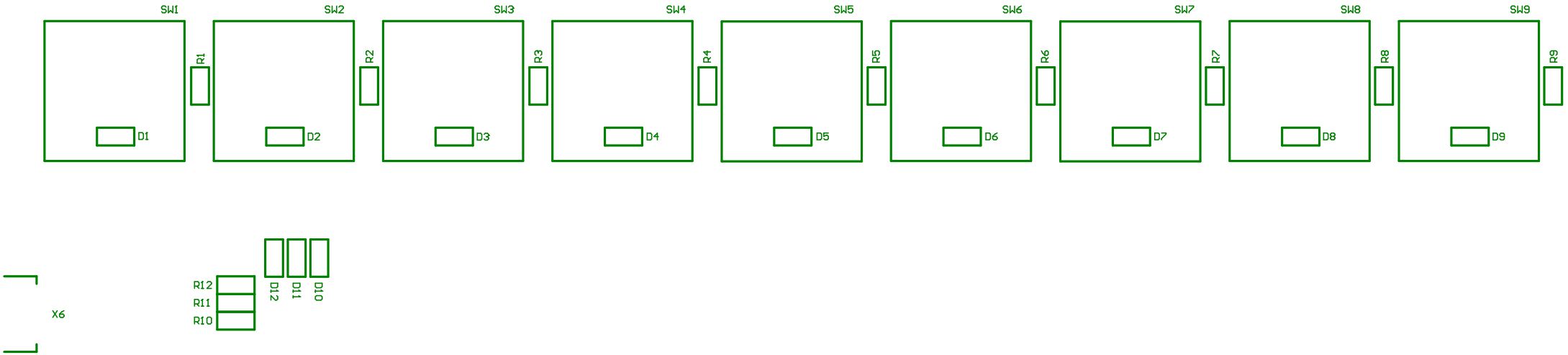
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R2-1(14.971mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R2-1(14.971mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R2-1(14.971mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R2-2(14.971mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R2-2(14.971mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R2-2(14.971mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R3-1(34.002mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R3-1(34.002mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R3-1(34.002mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R3-2(34.002mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R3-2(34.002mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R3-2(34.002mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R4-1(53.034mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R4-1(53.034mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R4-1(53.034mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R4-2(53.034mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R4-2(53.034mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R4-2(53.034mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R5-1(72.065mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R5-1(72.065mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R5-1(72.065mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R5-2(72.065mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R5-2(72.065mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R5-2(72.065mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R6-1(91.096mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R6-1(91.096mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R6-1(91.096mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R6-2(91.096mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R6-2(91.096mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R6-2(91.096mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R7-1(110.127mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R7-1(110.127mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R7-1(110.127mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R7-2(110.127mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R7-2(110.127mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R7-2(110.127mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R8-1(129.159mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R8-1(129.159mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R8-1(129.159mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R8-2(129.159mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R8-2(129.159mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R8-2(129.159mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R9-1(148.19mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R9-1(148.19mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R9-1(148.19mm,38.13mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R9-2(148.19mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R9-2(148.19mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.073mm < 0.254mm) Between Pad R9-2(148.19mm,35.23mm) on Top Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.254mm) Between Pad X6-MH(-22.7mm,13.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.176mm < 0.254mm) Between Pad X6-MH(-22.7mm,8.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad X6-MH(-25.4mm,14.5mm) on Multi-Layer And Track
Silk To Solder Mask Clearance Constraint: (0.123mm < 0.254mm) Between Pad X6-MH(-25.4mm,7.5mm) on Multi-Layer And Track

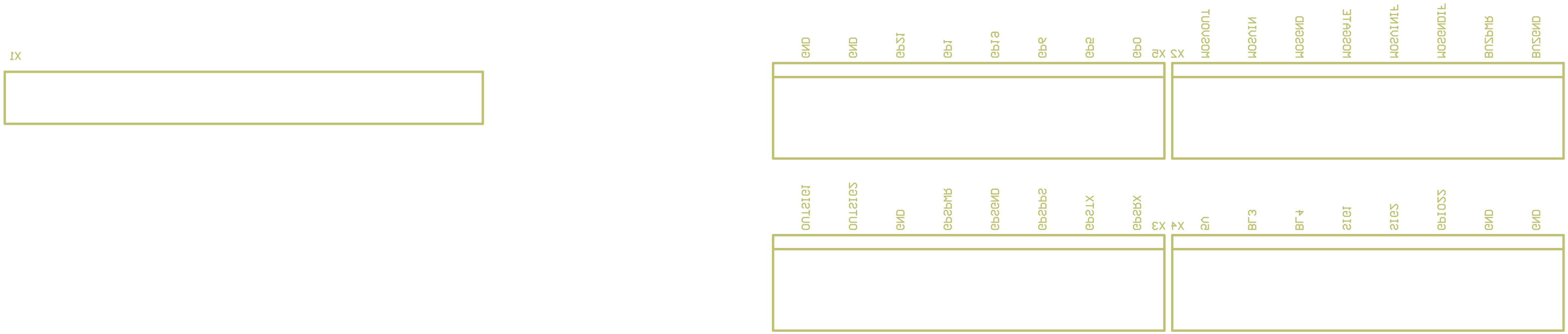
Electrical Rules Check Report

Class	Document	Message
Warning	KSS.SchDoc	Nets Wire 5V has multiple names (Net Label 5V, Net Label MOSFET_VIN, Power Object 5V (3))
Warning	KSS.SchDoc	Nets Wire BUTTON_LED_3 has multiple names (Net Label BUTTON_LED_3, Net Label BUZZER GND, Net Label GPS GND, Net Label MOSFET_GND, Net Label MOSFET_GND_IF, Power Object GND (7))
Warning	KSS.SchDoc	Nets Wire BUTTON_LED_4 has multiple names (Net Label BUTTON_LED_4, Net Label GPS PWR, Net Label MOSFET_VIN_IF, Power Object 3V3 (2))
Warning	KSS.SchDoc	Nets Wire BUZZER V+ has multiple names (Net Label BUZZER V+, Net Label GPIO26 (2))
Warning	KSS.SchDoc	Nets Wire GPIO2 has multiple names (Net Label GPIO2 (2), Net Label OUT_SIG_1)
Warning	KSS.SchDoc	Nets Wire GPIO3 has multiple names (Net Label GPIO3 (2), Net Label OUT_SIG_2)
Warning	KSS.SchDoc	Nets Wire GPIO4 has multiple names (Net Label GPIO4 (2), Net Label GPS PPS)
Warning	KSS.SchDoc	Nets Wire GPIO13 has multiple names (Net Label GPIO13 (2), Net Label MOSFET_GATE_IF)
Warning	KSS.SchDoc	Nets Wire GPIO14 has multiple names (Net Label GPIO14 (2), Net Label GPS TX)
Warning	KSS.SchDoc	Nets Wire GPIO15 has multiple names (Net Label GPIO15 (2), Net Label GPS RX)
Warning	KSS.SchDoc	Nets Wire GPIO17 has multiple names (Net Label GPIO17 (2), Net Label SIG_1 (LED))
Warning	KSS.SchDoc	Nets Wire GPIO27 has multiple names (Net Label GPIO27 (2), Net Label SIG_2 (BUTTON))
Warning	KSS.SchDoc	Nets Wire KEYS_LED has multiple names (Net Label KEYS_LED (2), Net Label MOSFET_VOUT)






SW1
SW2
SW3
SW4
SW5
SW6
SW7
SW8
SW9
R1
R2
R3
R4
R5
R6
R7
R8
R9
D1
D2
D3
D4
D5
D6
D7
D8
D9
R12
R11
R10
D12
D11
D10
X6


X1
GND
GND
GP21
GP1
GP19
GP9
GP5
GP0
X5
X2
MOSOUT
MOSVIN
MOSGND
MOSGATE
MOSVINF
MOSGNDF
BUZPWR
BUZGND
OUTSIG1
OUTSIG2
GND
GPSPWR
GPSGND
GPSPPS
GPSTX
GPSRX
X3
X4
5V
BL3
BL4
SIG1
SIG2
GPIO22
GND
GND